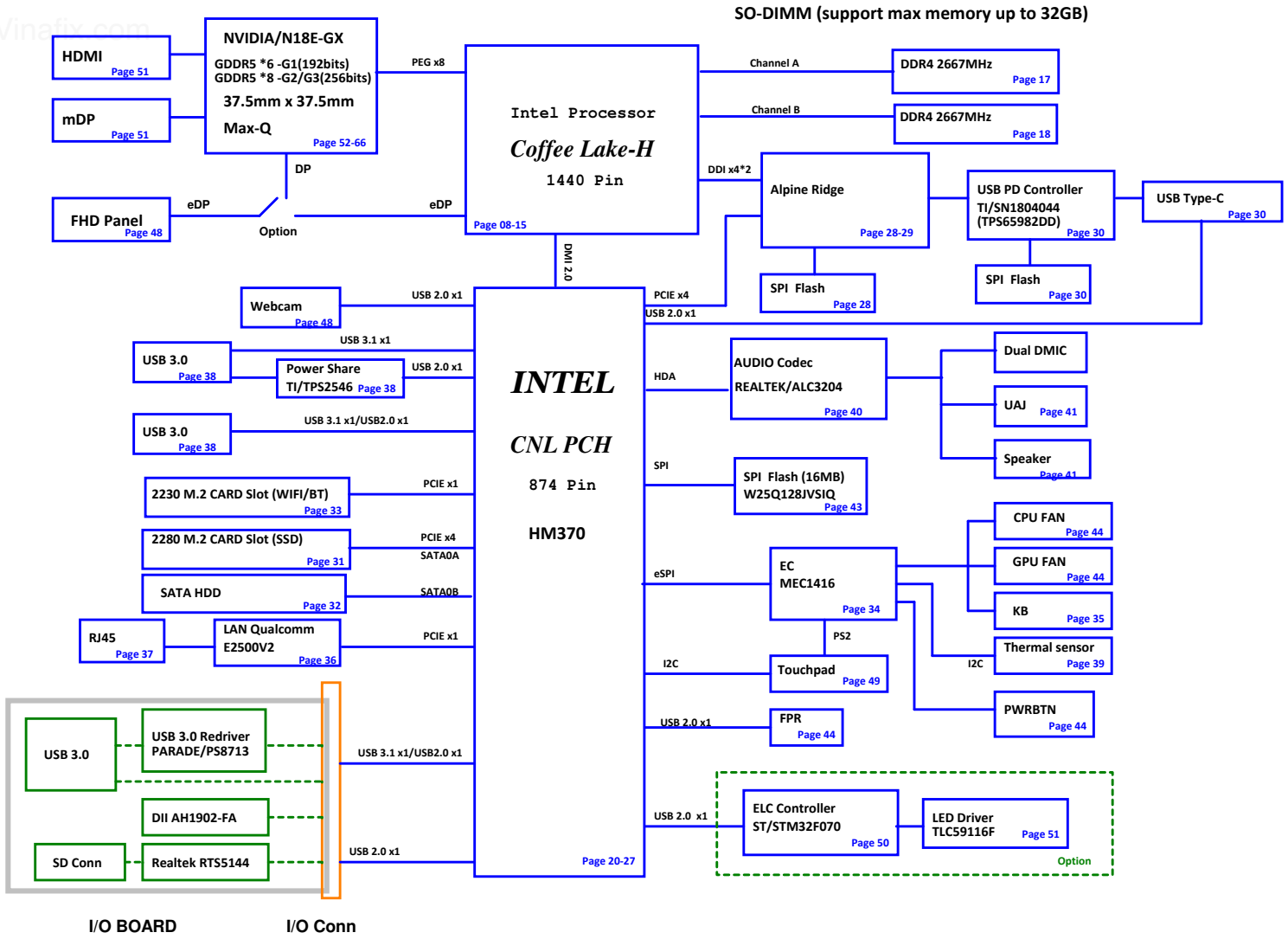
Vulcan (Coffee Lake-H)Revision_1.0

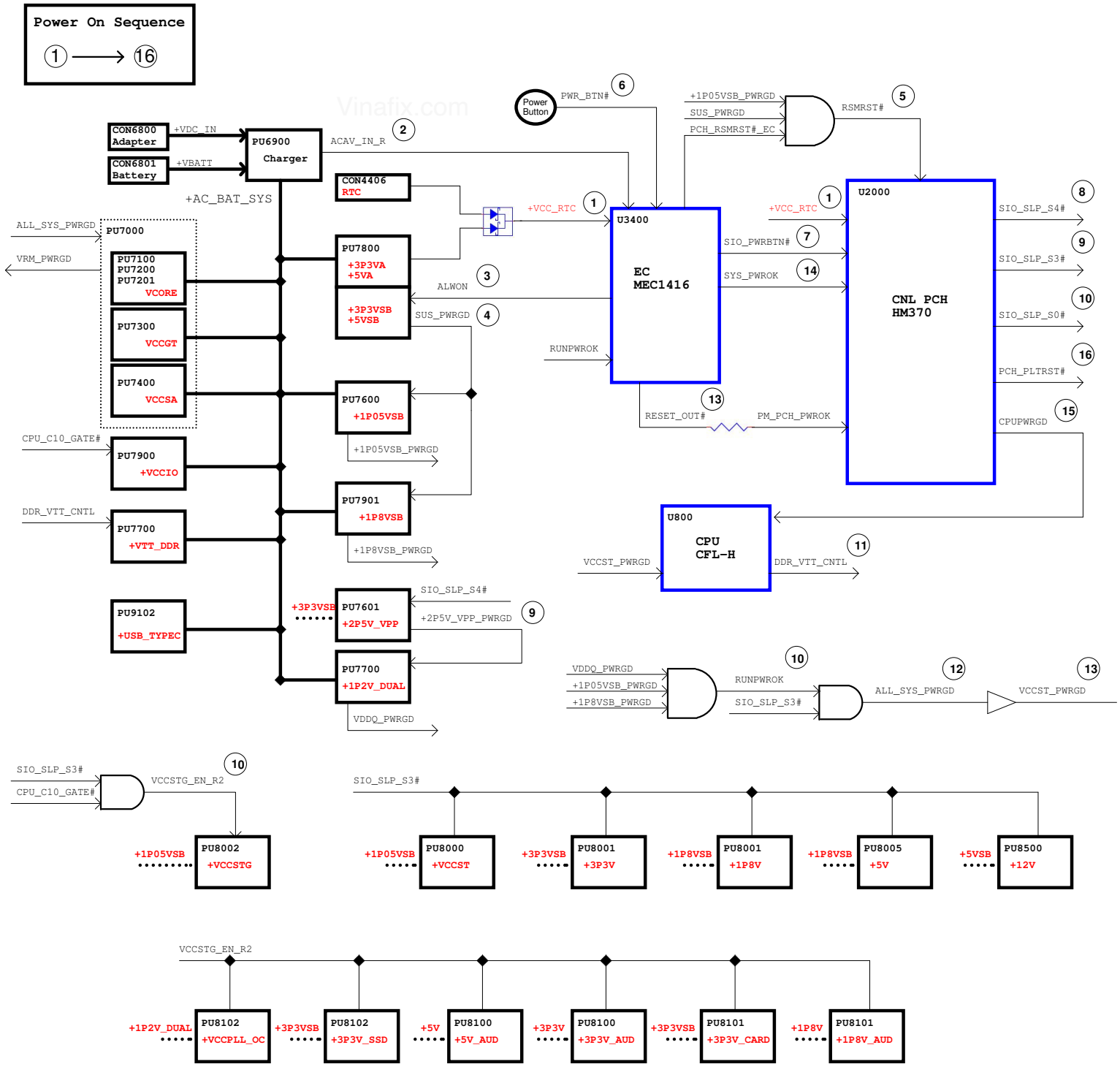


PEGATRON Title : BLOCK DIAGRAM

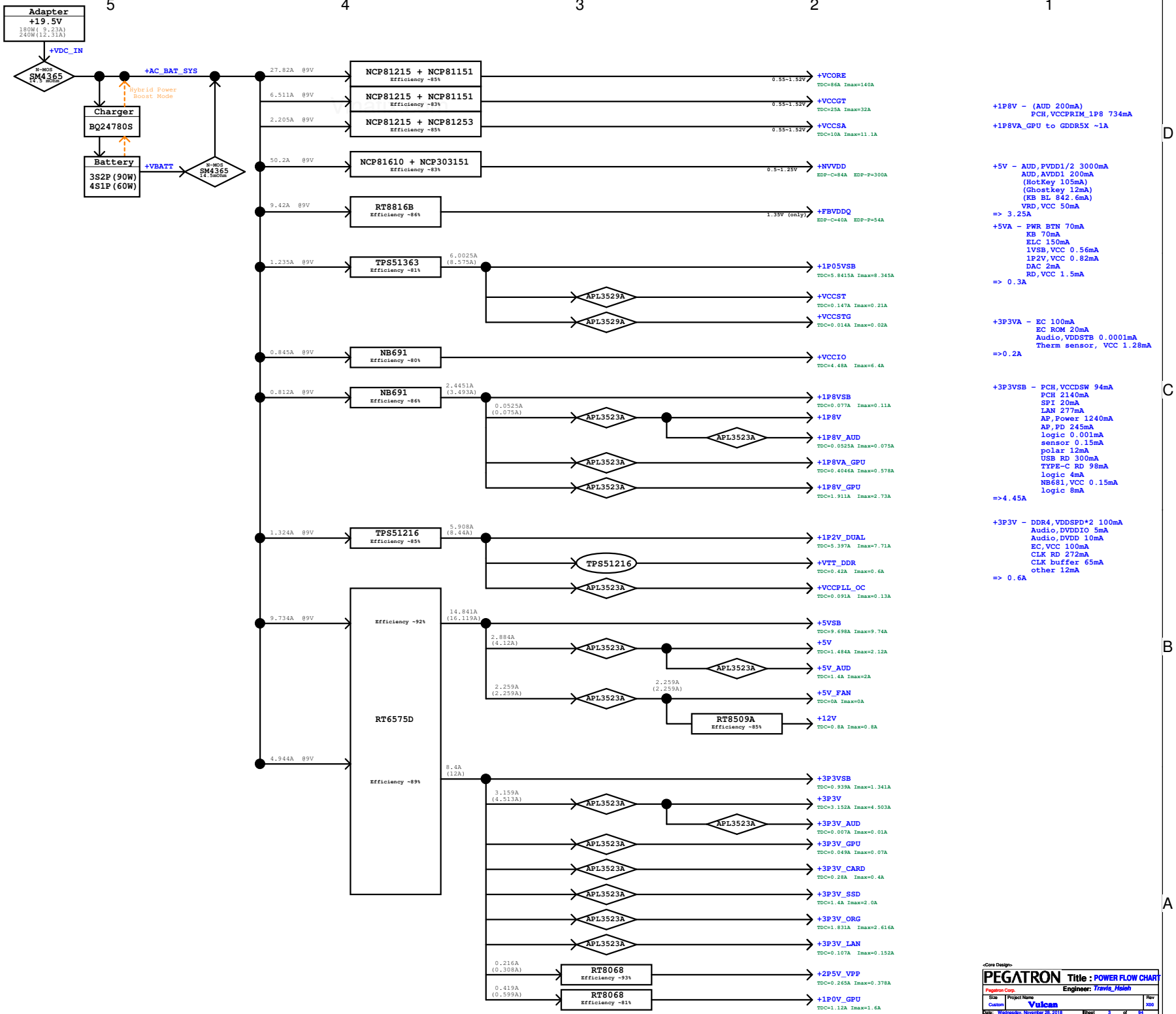
Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
C	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 1 of 94



PEGATRON Title : SIGNAL&RESET MAP
Pegatron Corp. Engineer: Travis_Haleh
Size: Custom Project Name: Vulcan Rev: X00
Date: Wednesday, November 28, 2018 Sheet 2 of 94


Adapter
+19.5V
180W(9.23A)
240W(12.31A)
+VDC_IN
N-MOS
SM4365
14.5 mOhm
+AC_BAT_SYS
Hybrid Power Boost Mode
Charger
BQ24780S
Battery
3S2P(90W)
4S1P(60W)
+VBATT
N-MOS
SM4365
14.5mOhm
27.82A @9V
NCP81215 + NCP81151
Efficiency ~85%
0.55~1.52V
+VCORE
TDC=86A Imax=140A
6.511A @9V
NCP81215 + NCP81151
Efficiency ~83%
0.55~1.52V
+VCCGT
TDC=25A Imax=32A
2.205A @9V
NCP81215 + NCP81253
Efficiency ~85%
0.55~1.52V
+VCCSA
TDC=10A Imax=11.1A
50.2A @9V
NCP81610 + NCP303151
Efficiency ~83%
0.5~1.25V
+NVVDD
EDP-C=84A EDP-P=300A
9.42A @9V
RT8816B
Efficiency ~86%
1.35V (only)
+FBVDDQ
EDP-C=40A EDP-P=54A
1.235A @9V
TPS51363
Efficiency ~81%
6.0025A
(8.575A)
+1P05VSB
TDC=5.8415A Imax=8.345A
APL3529A
+VCCST
TDC=0.147A Imax=0.21A
APL3529A
+VCCSTG
TDC=0.014A Imax=0.02A
0.845A @9V
NB691
Efficiency ~80%
+VCCIO
TDC=4.48A Imax=6.4A
0.812A @9V
NB691
Efficiency ~86%
2.4451A
(3.493A)
+1P8VSB
TDC=0.077A Imax=0.11A
0.0525A
(0.075A)
APL3523A
+1P8V
APL3523A
+1P8V_AUD
TDC=0.0525A Imax=0.075A
APL3523A
+1P8VA_GPU
TDC=0.4046A Imax=0.578A
APL3523A
+1P8V_GPU
TDC=1.911A Imax=2.73A
1.324A @9V
TPS51216
Efficiency ~85%
5.908A
(8.44A)
+1P2V_DUAL
TDC=5.397A Imax=7.71A
TPS51216
+VTT_DDR
TDC=0.42A Imax=0.6A
APL3523A
+VCCPLL_OC
TDC=0.091A Imax=0.13A
9.734A @9V
Efficiency ~92%
14.841A
(16.119A)
+5VSB
TDC=9.698A Imax=9.74A
2.884A
(4.12A)
APL3523A
+5V
TDC=1.484A Imax=2.12A
APL3523A
+5V_AUD
TDC=1.4A Imax=2A
2.259A
(2.259A)
APL3523A
2.259A
(2.259A)
+5V_FAN
TDC=0A Imax=0A
RT8509A
Efficiency ~85%
+12V
TDC=0.8A Imax=0.8A
RT6575D
4.944A @9V
Efficiency ~89%
8.4A
(12A)
+3P3VSB
TDC=0.939A Imax=1.341A
3.159A
(4.513A)
APL3523A
+3P3V
TDC=3.152A Imax=4.503A
APL3523A
+3P3V_AUD
TDC=0.007A Imax=0.01A
APL3523A
+3P3V_GPU
TDC=0.049A Imax=0.07A
APL3523A
+3P3V_CARD
TDC=0.28A Imax=0.4A
APL3523A
+3P3V_SSD
TDC=1.4A Imax=2.0A
APL3523A
+3P3V_ORG
TDC=1.831A Imax=2.616A
APL3523A
+3P3V_LAN
TDC=0.107A Imax=0.152A
0.216A
(0.308A)
RT8068
Efficiency ~93%
+2P5V_VPP
TDC=0.265A Imax=0.378A
0.419A
(0.599A)
RT8068
Efficiency ~81%
+1P0V_GPU
TDC=1.12A Imax=1.6A
+1P8V - (AUD 200mA)
PCH,VCCPRIM_1P8 734mA
+1P8VA_GPU to GDDR5X ~1A
+5V - AUD,PVDD1/2 3000mA
AUD,AVDD1 200mA
(HotKey 105mA)
(Ghostkey 12mA)
(KB BL 842.6mA)
VRD,VCC 50mA
=> 3.25A
+5VA - PWR BTN 70mA
KB 70mA
ELC 150mA
1VSB,VCC 0.56mA
1P2V,VCC 0.82mA
DAC 2mA
RD,VCC 1.5mA
=> 0.3A
+3P3VA - EC 100mA
EC ROM 20mA
Audio,VDDSTB 0.0001mA
Therm sensor, VCC 1.28mA
=>0.2A
+3P3VSB - PCH,VCCDSW 94mA
PCH 2140mA
SPI 20mA
LAN 277mA
AP,Power 1240mA
AP,PD 245mA
logic 0.001mA
sensor 0.15mA
polar 12mA
USB RD 300mA
TYPE-C RD 98mA
logic 4mA
NB681,VCC 0.15mA
logic 8mA
=>4.45A
+3P3V - DDR4,VDDSPD*2 100mA
Audio,DVDDIO 5mA
Audio,DVDD 10mA
EC,VCC 100mA
CLK RD 272mA
CLK buffer 65mA
other 12mA
=> 0.6A
<Core Design>
PEGATRON
Title : POWER FLOW CHART
Pegatron Corp.
Engineer: Travis_Hsieh
Size: Custom
Project Name: Vulcan
Rev: X00
Date: Wednesday, November 28, 2018
Sheet 3 of 54

Schematics Change History

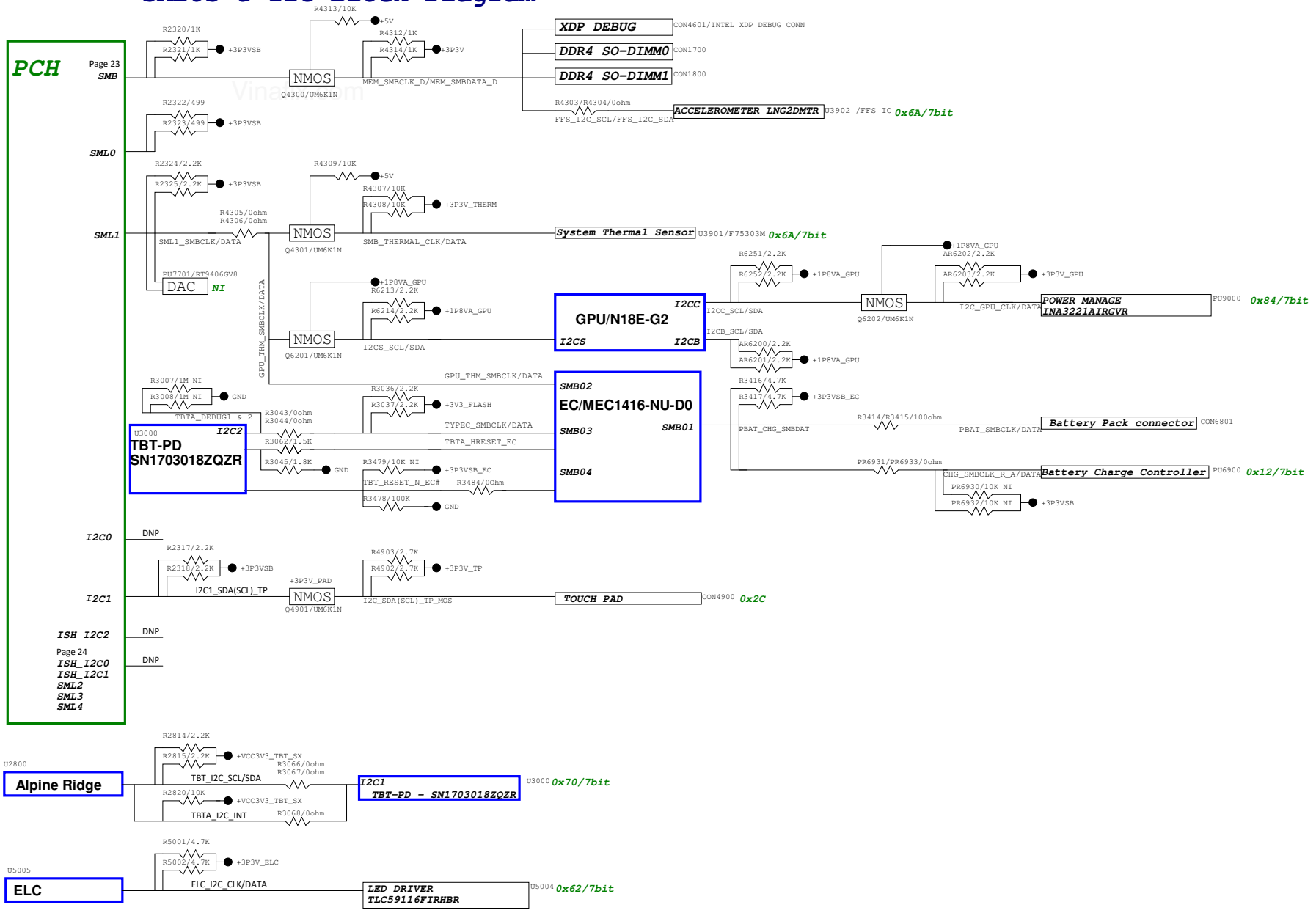
Version	Date	Description	Comments
1.00			

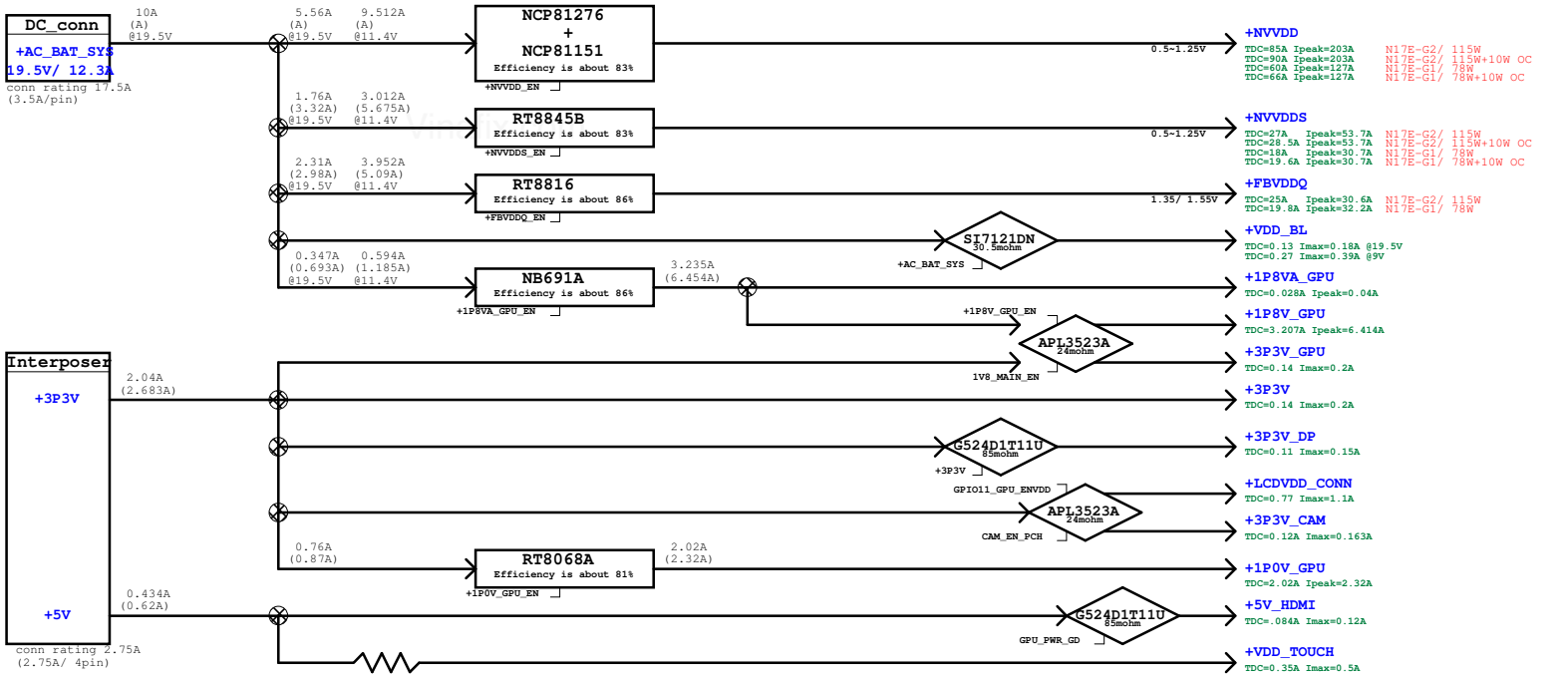
<Core Design>

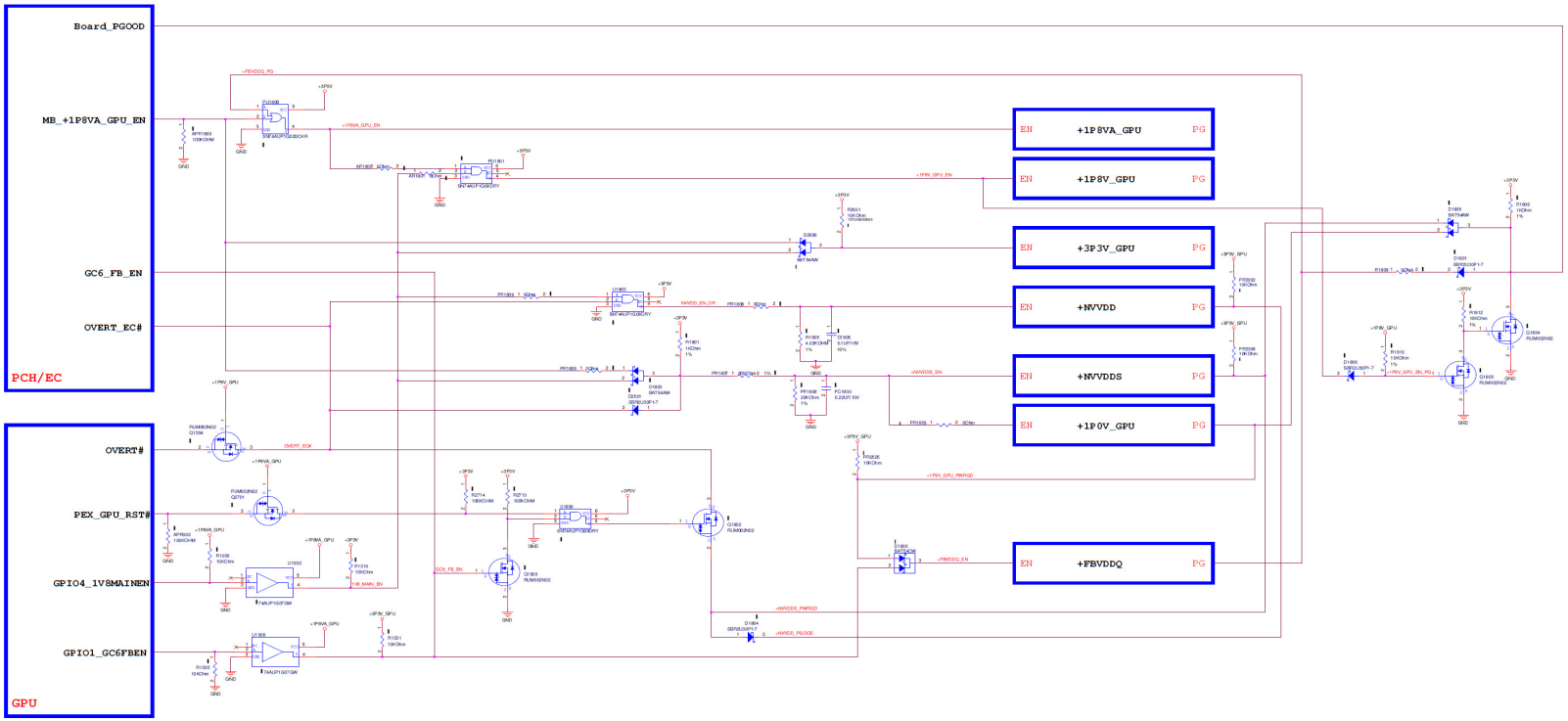
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CHANGE HISTORY		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A3	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018		Sheet 4	of 94

SMBUS & I2C Block Diagram







<Core Design>

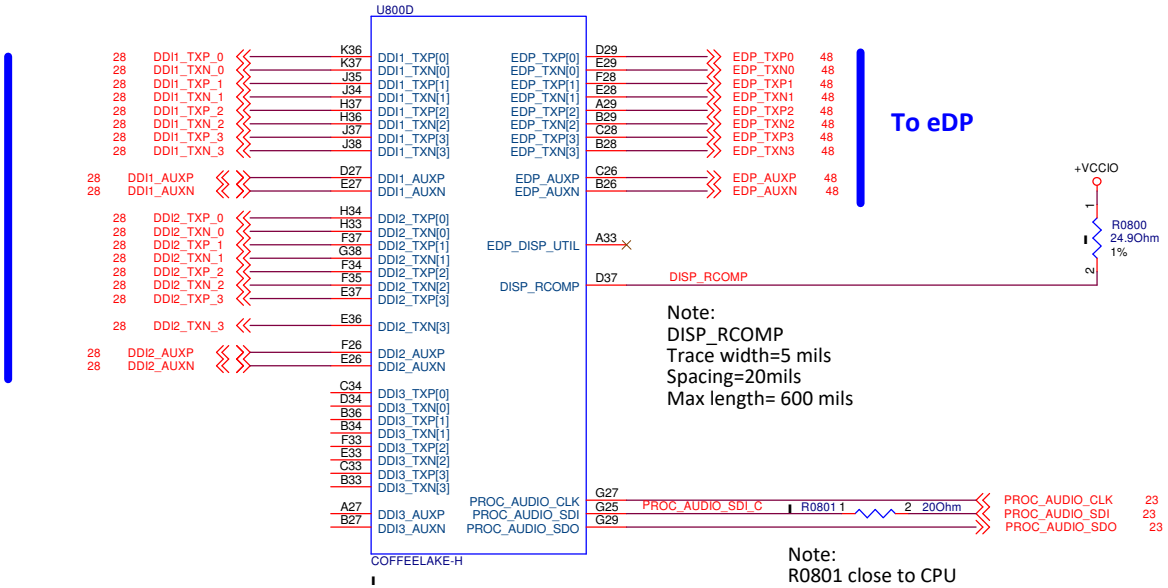
PEGATRON Title : GPU Power flow & sequence

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 6 of 94

Reserved Page



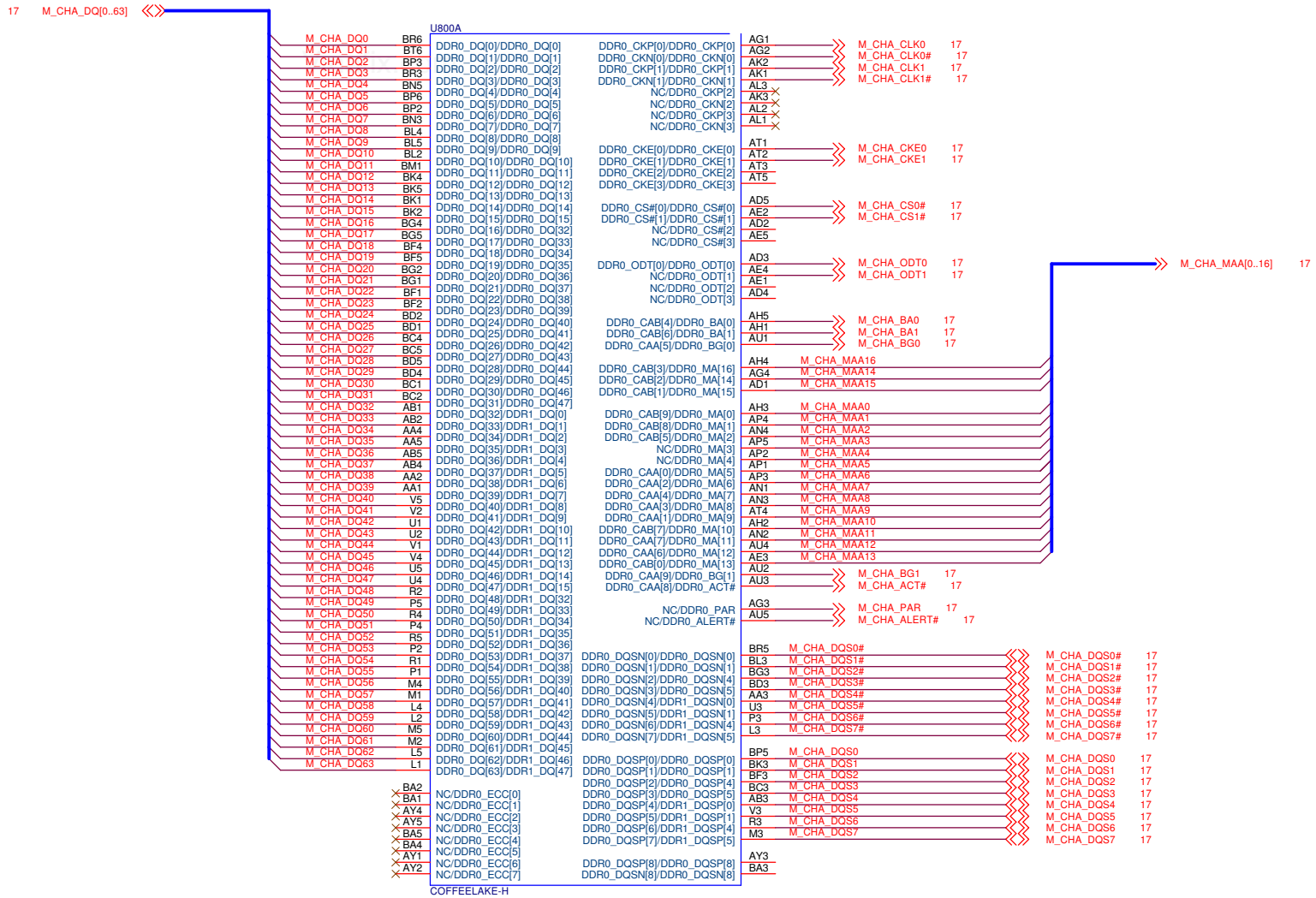
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDI/EDP

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 8 of 94



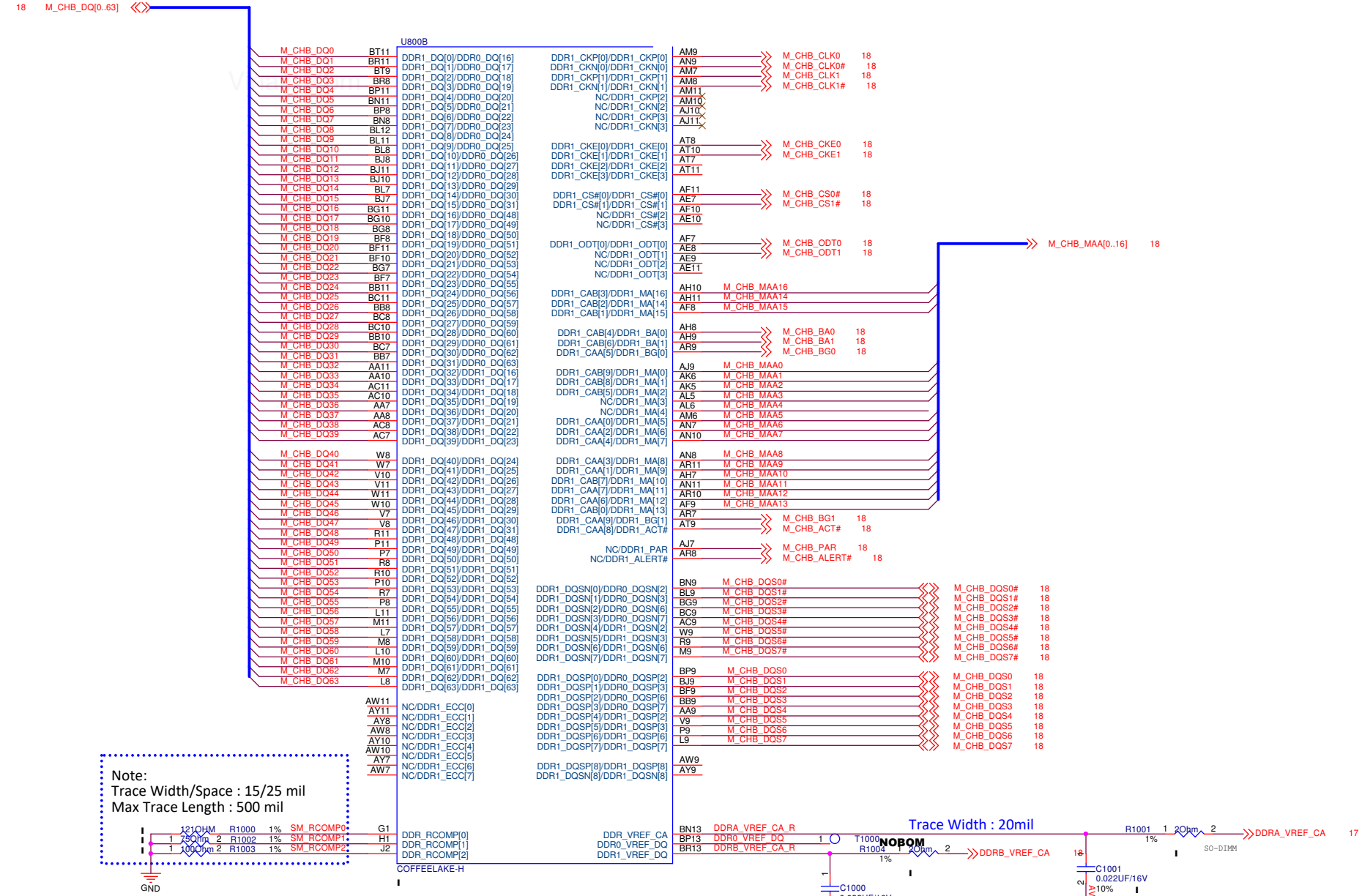
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHA

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 9 of 94



Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)				Max Length (mils)			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group [1]/[2]	Byte [1]/[2]	Region	Breakout [1,2]	Total		
RCOMP [0]	M	MS	VSS	2	12-15					20	25/25				500	121	
RCOMP [1]	M	MS	VSS	2	12-15					20	25/25				500	75	
RCOMP [2]	M	MS	VSS	2	12-15					20	25/25				500	100	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHB

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

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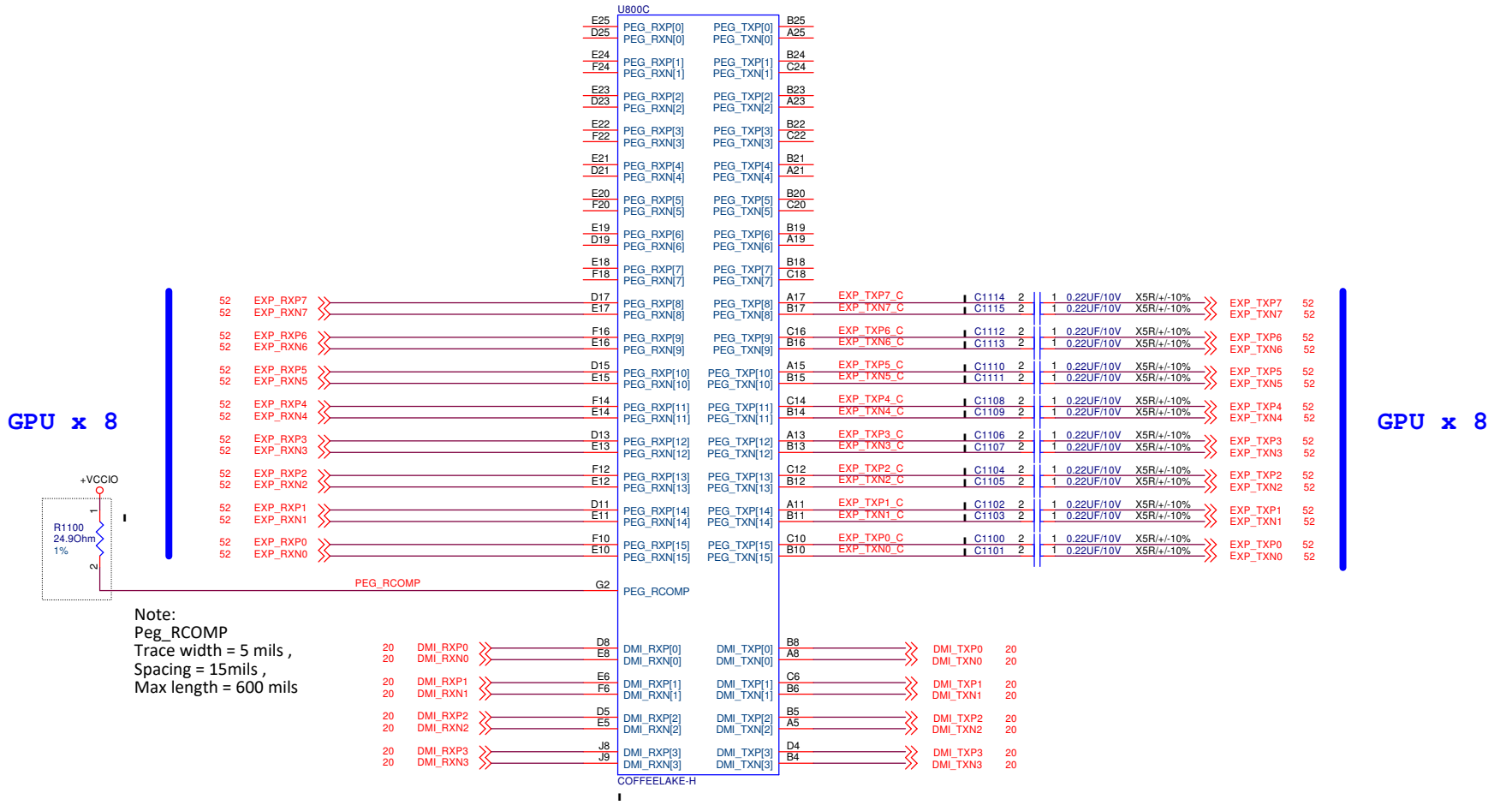


Note:
Peg_RCOMP
Trace width = 5 mils ,
Spacing = 15mils ,
Max length = 600 mils

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU PEG/DMI

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 11 of 94

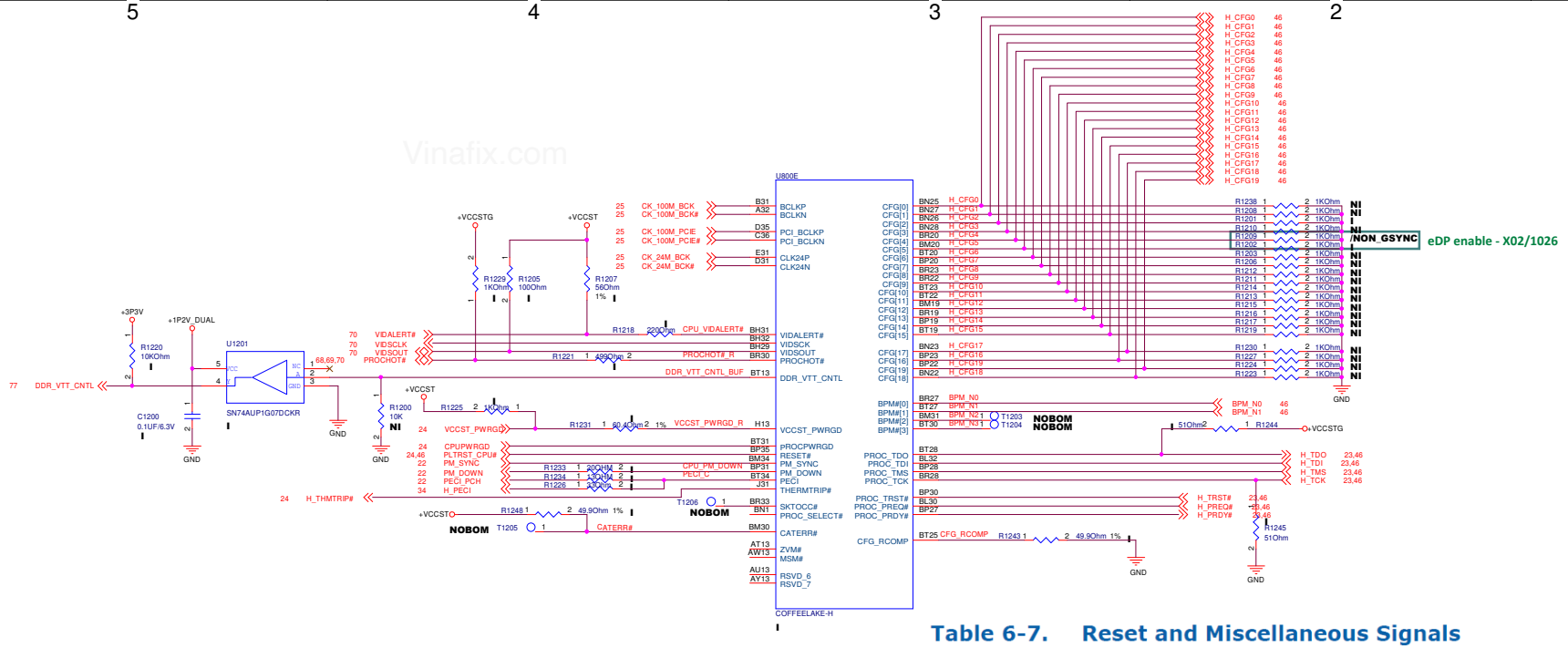


Table 6-7. Reset and Miscellaneous Signals

Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.

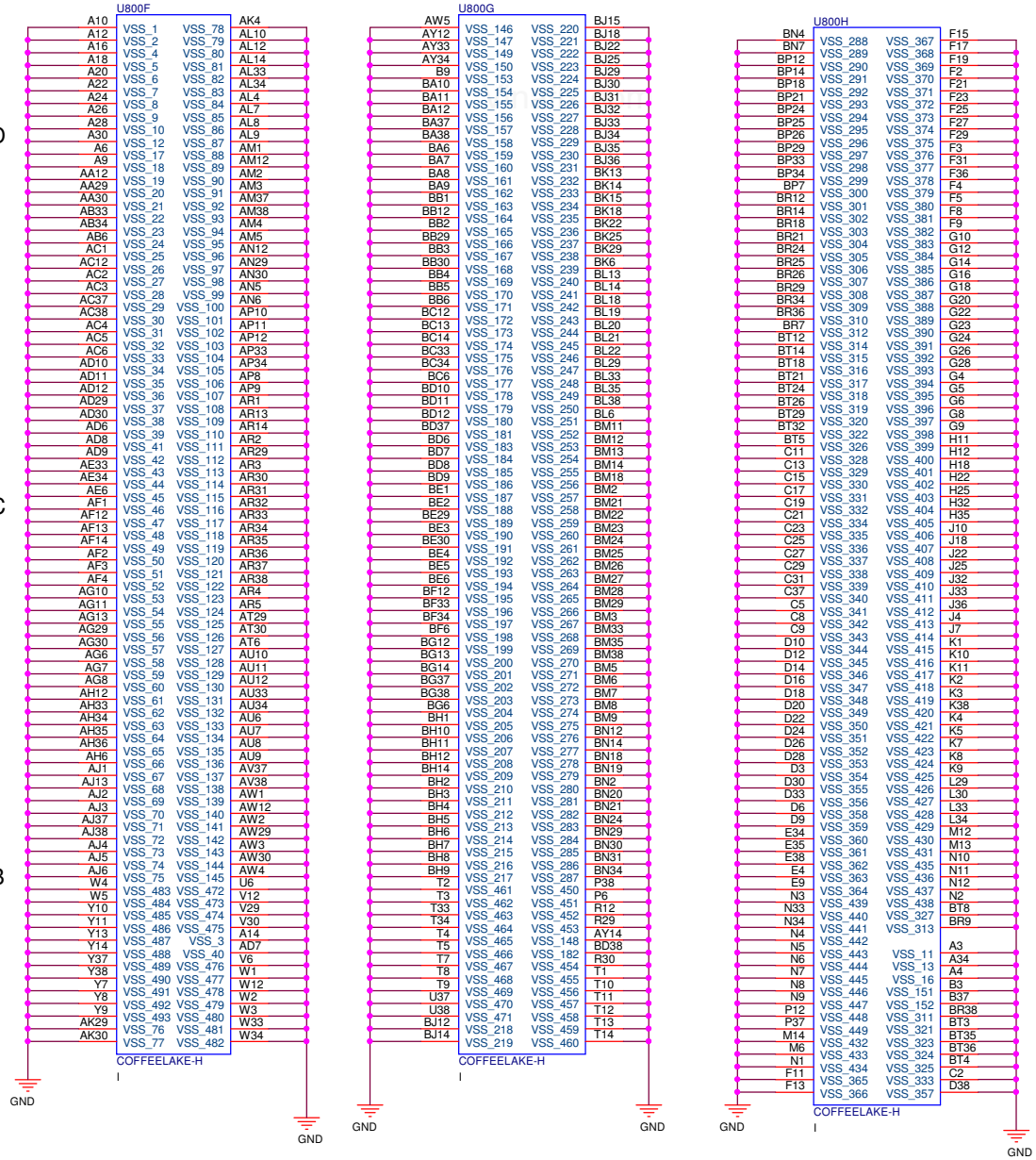
Table 6-10. Processor Clocking Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	H and S-Processor Line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	

Table 51-39. Processor/PCH Strapping Checklist (Sheet 2 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[19:8]	Reserved configuration lands.			

PEGATRON	Title : CPU other	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A2	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 12 of 94	



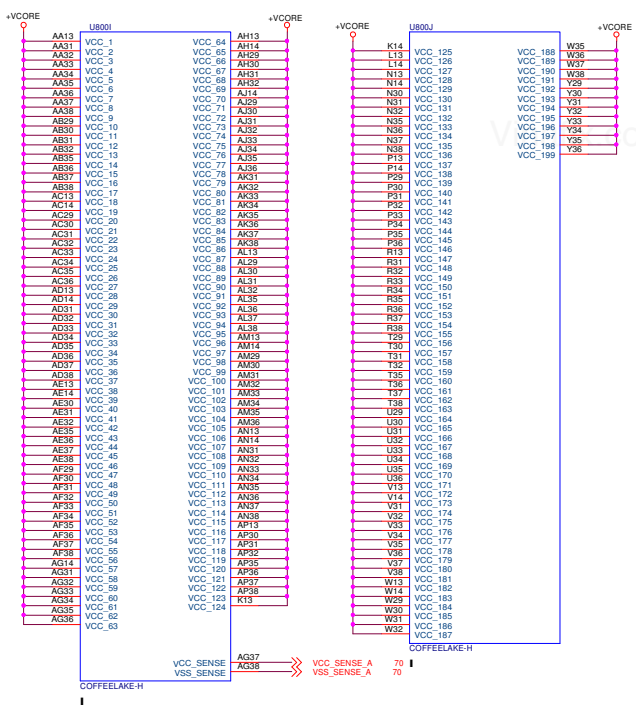
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU VSS

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 13 of 94

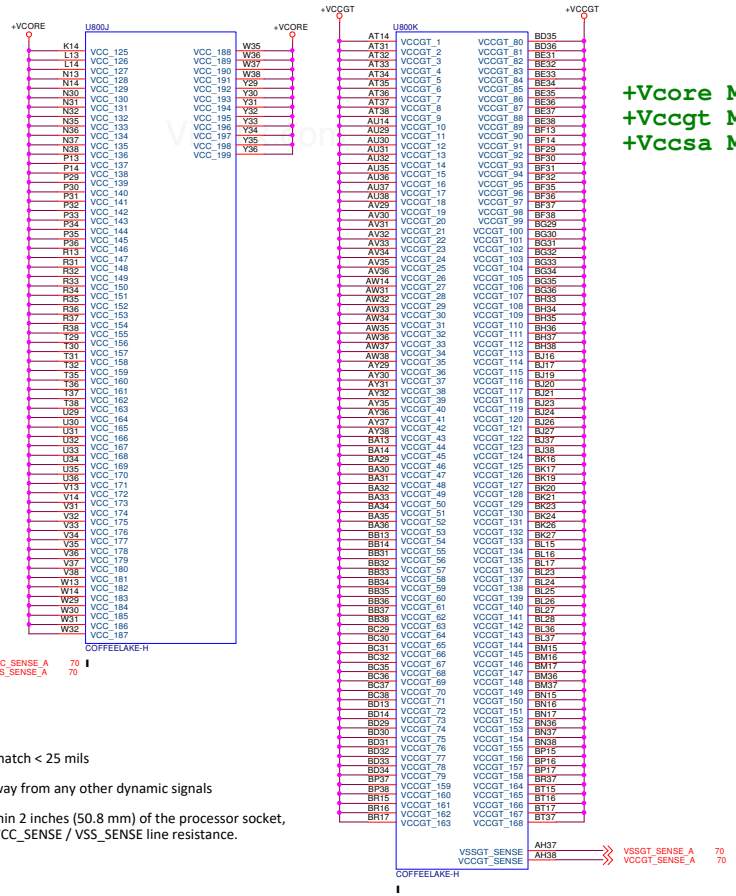


Note:

1. VCC_SENSE / VSS_SENSE trace length match < 25 mils

2. Maintain 25-mil separation distance away from any other dynamic signals

3. PR7038 / PR7043 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCC_SENSE / VSS_SENSE line resistance.



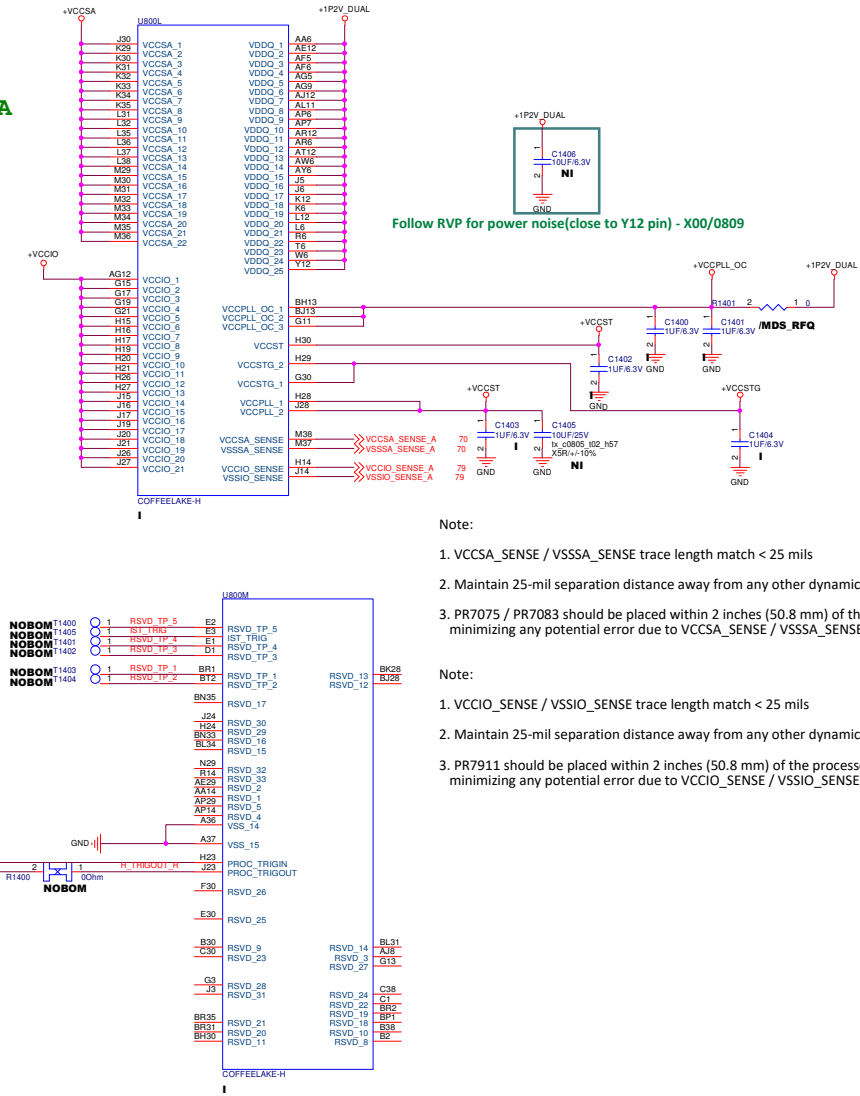
Note:

1. VSSGT_SENSE / VCCGT_SENSE trace length match < 25 mils

2. Maintain 25-mil separation distance away from any other dynamic signals

3. PR7059 / PR7067 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VSSGT_SENSE / VCCGT_SENSE line resistance.

+Vcore Max 140A
+Vccgt Max 32A
+Vccsa Max 11.1A



Note:

1. VCCSA_SENSE / VSSSA_SENSE trace length match < 25 mils

2. Maintain 25-mil separation distance away from any other dynamic signals

3. PR7075 / PR7083 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCSA_SENSE / VSSSA_SENSE line resistance.

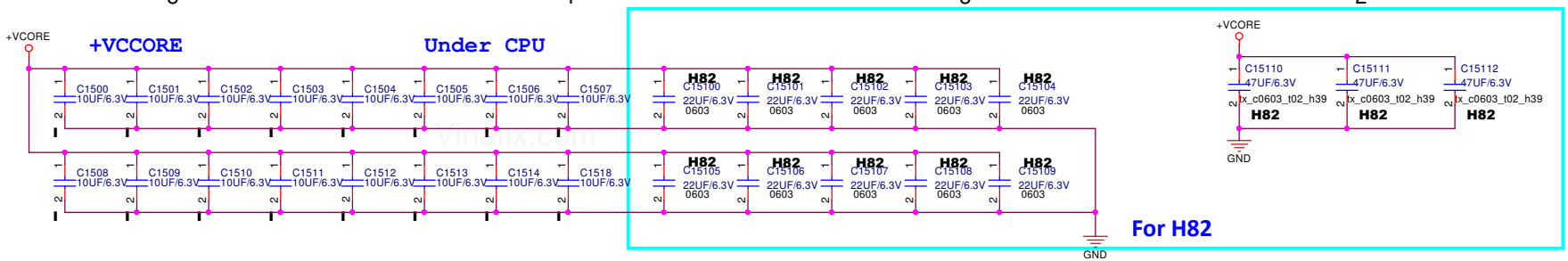
Note:

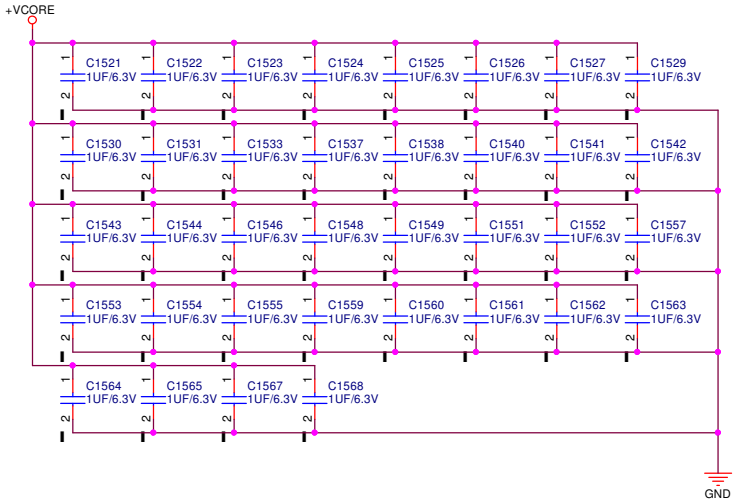
1. VCCIO_SENSE / VSSIO_SENSE trace length match < 25 mils

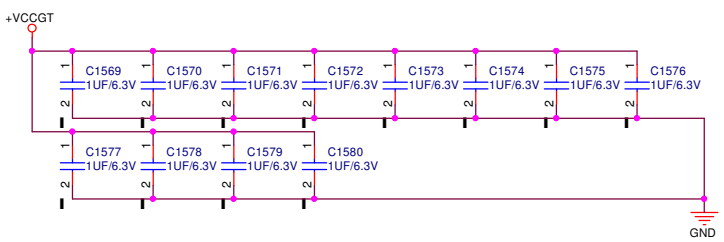
2. Maintain 25-mil separation distance away from any other dynamic signals

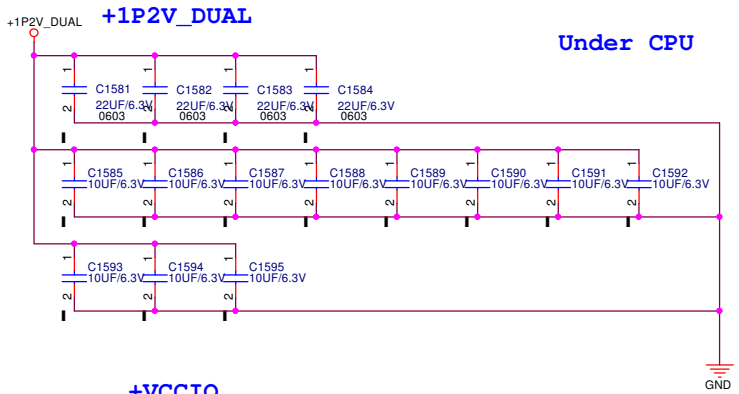
3. PR7911 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCIO_SENSE / VSSIO_SENSE line resistance.

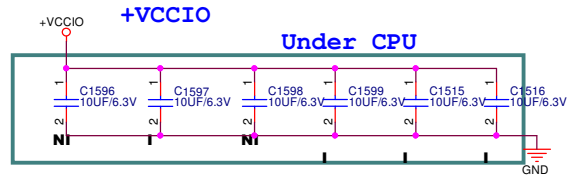
PEGATRON	Title : CPU POWER		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 14 of 94		











Change for power noise fail - X00/0717

Table 50-3. Decoupling Requirements for CFL H Processor

Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
Vcc_{SA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.

PEGATRON Title : CPU DECOUPLING

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

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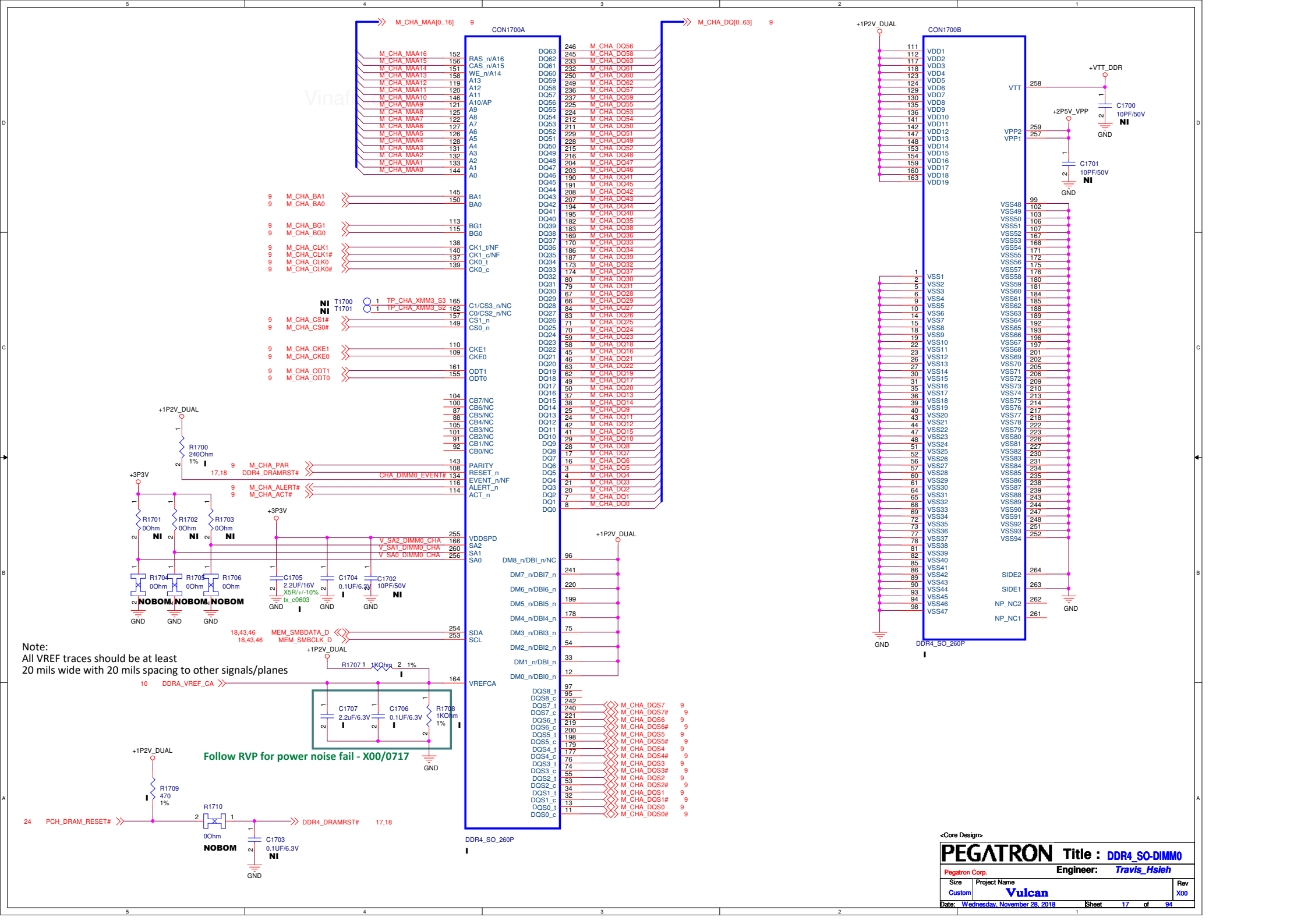
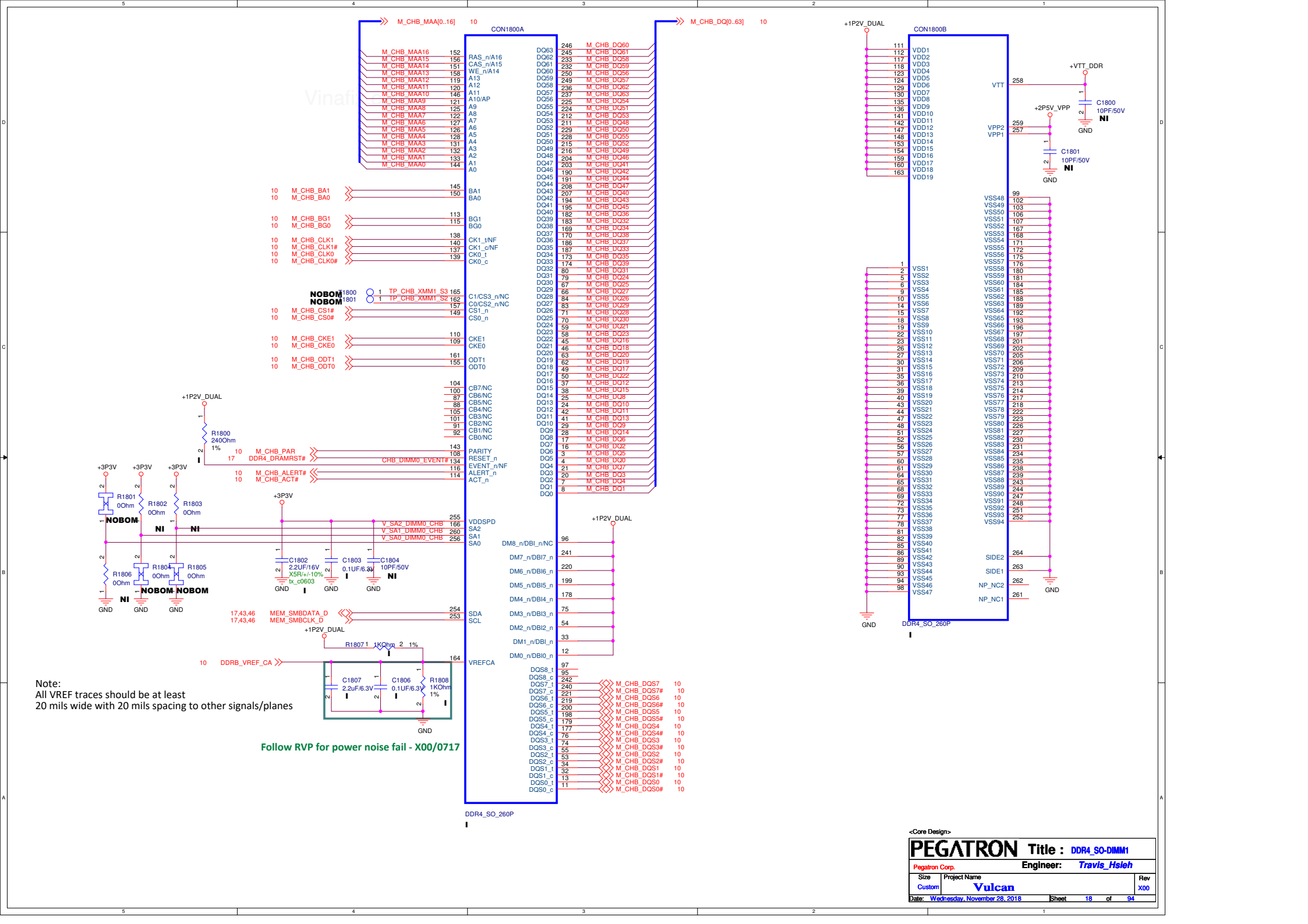
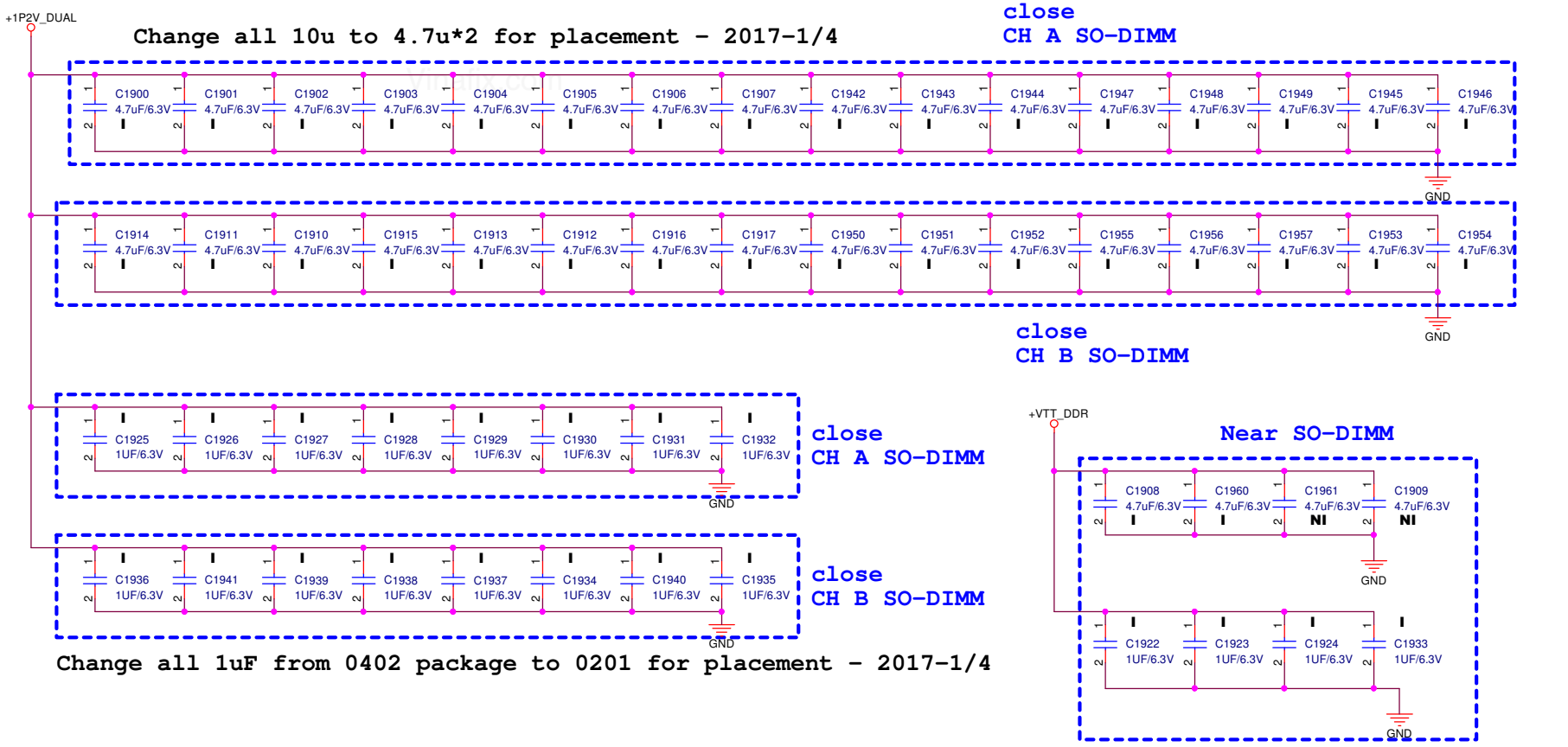
Reserved Page

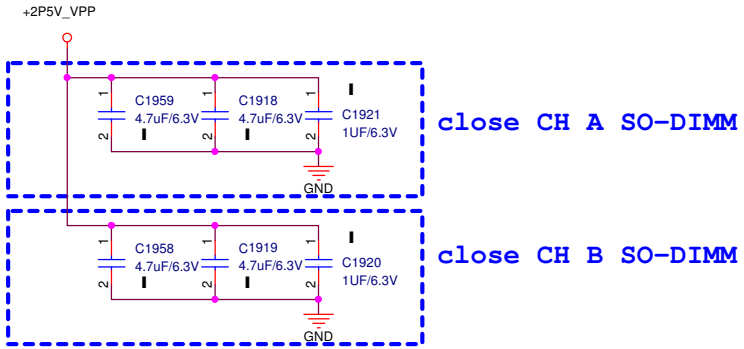

M_CHA_MAA[0..16] 9
M_CHA_DQ[0..63] 9
CON1700A
CON1700B
DDR4_SO_260P
DDR4_SO_260P
M_CHA_MAA16 M_CHA_MAA15 M_CHA_MAA14 M_CHA_MAA13 M_CHA_MAA12 M_CHA_MAA11 M_CHA_MAA10 M_CHA_MAA9 M_CHA_MAA8 M_CHA_MAA7 M_CHA_MAA6 M_CHA_MAA5 M_CHA_MAA4 M_CHA_MAA3 M_CHA_MAA2 M_CHA_MAA1 M_CHA_MAA0
RAS_n/A16 CAS_n/A15 WE_n/A14 A13 A12 A11 A10/AP A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
M_CHA_BA1 M_CHA_BA0
BA1 BA0
M_CHA_BG1 M_CHA_BG0
BG1 BG0
M_CHA_CLK1 M_CHA_CLK1# M_CHA_CLK0 M_CHA_CLK0#
CK1_t/NF CK1_c/NF CK0_t CK0_c
NI T1700 NI T1701
TP_CHA_XMM3_S3 TP_CHA_XMM3_S2
C1/CS3_n/NC C0/CS2_n/NC
M_CHA_CS1# M_CHA_CS0#
CS1_n CS0_n
M_CHA_CKE1 M_CHA_CKE0
CKE1 CKE0
M_CHA_ODT1 M_CHA_ODT0
ODT1 ODT0
CB7/NC CB6/NC CB5/NC CB4/NC CB3/NC CB2/NC CB1/NC CB0/NC
+1P2V_DUAL
R1700 240Ohm 1%
M_CHA_PAR
17,18 DDR4_DRAMRST#
CHA_DIMM0_EVENT#
PARITY RESET_n EVENT_n/NF ALERT_n ACT_n
M_CHA_ALERT# M_CHA_ACT#
+3P3V
R1701 R1702 R1703 0Ohm NI
+3P3V
V_SA2_DIMM0_CHA V_SA1_DIMM0_CHA V_SA0_DIMM0_CHA
VDDSPD SA2 SA1 SA0
R1704 R1705 R1706 0Ohm NOBOM
C1705 2.2UF/16V X5R/+/-10% tx_c0603
C1704 0.1UF/6.3V
C1702 10PF/50V NI
GND
18,43,46 MEM_SMBDATA_D
18,43,46 MEM_SMBCLK_D
SDA SCL
+1P2V_DUAL
R1707 1KOhm 1%
10 DDRA_VREF_CA
VREFCA
C1707 2.2uF/6.3V
C1706 0.1UF/6.3V
R1708 1KOhm 1%
Follow RVP for power noise fail - X00/0717
+1P2V_DUAL
R1709 470 1%
24 PCH_DRAM_RESET#
R1710 0Ohm NOBOM
DDR4_DRAMRST# 17,18
C1703 0.1UF/6.3V NI
DM8_n/DBI_n/NC DM7_n/DBI7_n DM6_n/DBI6_n DM5_n/DBI5_n DM4_n/DBI4_n DM3_n/DBI3_n DM2_n/DBI2_n DM1_n/DBI_n DM0_n/DBI0_n
DQS8_t DQS8_c DQS7_t DQS7_c DQS6_t DQS6_c DQS5_t DQS5_c DQS4_t DQS4_c DQS3_t DQS3_c DQS2_t DQS2_c DQS1_t DQS1_c DQS0_t DQS0_c
M_CHA_DQS7 M_CHA_DQS7# M_CHA_DQS6 M_CHA_DQS6# M_CHA_DQS5 M_CHA_DQS5# M_CHA_DQS4 M_CHA_DQS4# M_CHA_DQS3 M_CHA_DQS3# M_CHA_DQS2 M_CHA_DQS2# M_CHA_DQS1 M_CHA_DQS1# M_CHA_DQS0 M_CHA_DQS0#
+1P2V_DUAL
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18 VDD19
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47
VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94
+VTT_DDR
VTT
C1700 10PF/50V NI
+2P5V_VPP
VPP2 VPP1
C1701 10PF/50V NI
SIDE2 SIDE1
NP_NC2 NP_NC1
GND
Note:
All VREF traces should be at least
20 mils wide with 20 mils spacing to other signals/planes
<Core Design>
PEGATRON
Title : DDR4_SO-DIMM0
Pegatron Corp.
Engineer: Travis_Hsieh
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 17 of 94


M_CHB_MAA[0..16] 10
M_CHB_DQ[0..63] 10
CON1800A
CON1800B
DDR4_SO_260P
+1P2V_DUAL
+3P3V
+VTT_DDR
+2P5V_VPP
GND
NOBOM
NI
Note:
All VREF traces should be at least
20 mils wide with 20 mils spacing to other signals/planes
Follow RVP for power noise fail - X00/0717
<Core Design>
PEGATRON
Title : DDR4_SO-DIMM1
Pegatron Corp.
Engineer: Travis_Hsieh
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 18 of 94



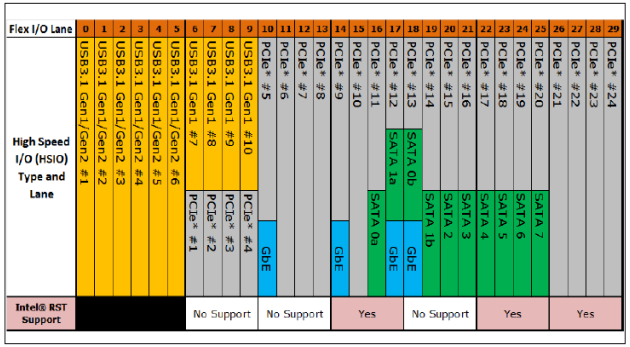
DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR DECOUPLING	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 19 of 94	



PCH-H Details	PCIe* Controller #1	PCIe* Controller #2	PCIe* Controller #3	PCIe* Controller #4	PCIe* Controller #5	PCIe* Controller #6
			Cycle Router #1		Cycle Router #3	Cycle Router #2
Flex I/O Lane #	6 7 8 9	10 11 12 13	14 15 16 17	18 15 20 21	22 23 24 25	26 27 28 29
PCIe* Lane #	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24
HM370 1x4			RP 9	RP 13	RP 17	RP 21
HM370 1x4 LR			RP 9	RP 13	RP 17	RP 21
HM370 2x2			RP 9 RP 11	RP 13 RP 15	RP 17 RP 19	RP 21 RP 23
HM370 1x2+2x1			RP 9 RP 11 RP 12	RP 13 RP 15 RP 16	RP 17 RP 19 RP 20	RP 21 RP 23 RP 24
HM370 2x1+1x2			RP 12 RP 11 RP 9	RP 16 RP 15 RP 13	RP 20 RP 19 RP 17	RP 24 RP 23 RP 21
HM370 4x1			RP 9 RP 10 RP 11 RP 12	RP 13 RP 14 RP 15 RP 16	RP 17 RP 18 RP 19 RP 20	RP 21 RP 22 RP 23 RP 24

U2000A

DMI

DMI0_RXN K34
DMI0_RXP J35
DMI0_TXN C33
DMI0_TXP B33
DMI1_RXN G33
DMI1_RXP F34
DMI1_TXN C32
DMI1_TXP B32
DMI2_RXN K32
DMI2_RXP J32
DMI2_TXN C31
DMI2_TXP B31
DMI3_RXN G30
DMI3_RXP F30
DMI3_TXN C29
DMI3_TXP B29

11 DMI_TXN0
11 DMI_TXP0
11 DMI_RXN0
11 DMI_RXP0
11 DMI_TXN1
11 DMI_TXP1
11 DMI_RXN1
11 DMI_RXP1
11 DMI_TXN2
11 DMI_TXP2
11 DMI_RXN2
11 DMI_RXP2
11 DMI_TXN3
11 DMI_TXP3
11 DMI_RXN3
11 DMI_RXP3

DMI4_RXN M29
DMI4_RXP K29
DMI4_TXN E28
DMI4_TXP D29
DMI5_RXN M26
DMI5_RXP L26
DMI5_TXN C27
DMI5_TXP B27
DMI6_RXN G26
DMI6_RXP F26
DMI6_TXN B26
DMI6_TXP C26
DMI7_RXN R24
DMI7_RXP P24
DMI7_TXN B25
DMI7_TXP A25

PCIE/USB/SATA

PCIE1_TXP/USB31_7_TXP B17
PCIE1_TXN/USB31_7_TXN A17
PCIE1_RXP/USB31_7_RXP F16
PCIE1_RXN/USB31_7_RXN G17
PCIE2_TXP/USB31_8_TXP C18
PCIE2_TXN/USB31_8_TXN B18
PCIE2_RXP/USB31_8_RXP P21
PCIE2_RXN/USB31_8_RXN R21
PCIE3_TXP/USB31_9_TXP C19
PCIE3_TXN/USB31_9_TXN B19
PCIE3_RXP/USB31_9_RXP J18
PCIE3_RXN/USB31_9_RXN K18
PCIE4_TXP/USB31_10_TXP C20
PCIE4_TXN/USB31_10_TXN D20
PCIE4_RXP/USB31_10_RXP R18
PCIE4_RXN/USB31_10_RXN N18
PCIE5_TXP A22
PCIE5_TXN B21
PCIE5_RXP G20
PCIE5_RXN F20
PCIE6_TXP C21
PCIE6_TXN D21
PCIE6_RXP J21
PCIE6_RXN K21
PCIE7_TXP B23
PCIE7_TXN C23
PCIE7_RXP J24
PCIE7_RXN L24
PCIE8_TXP C24
PCIE8_TXN B24
PCIE8_RXP G24
PCIE8_RXN F24
PCIE9_TXP D34
PCIE9_TXN C34
PCIE9_RXP F36
PCIE9_RXN G36
PCIE10_TXP B35
PCIE10_TXN C35
PCIE10_RXP J37
PCIE10_RXN K37
PCIE11_TXP/SATA0A_TXP C36
PCIE11_TXN/SATA0A_TXN B36
PCIE11_RXP/SATA0A_RXP F39
PCIE11_RXN/SATA0A_RXN G38
PCIE12_TXP/SATA1A_TXP E37
PCIE12_TXN/SATA1A_TXN D38
PCIE12_RXP/SATA_1A_RXP J41
PCIE12_RXN/SATA1A_RXN H42

31 PCIE9_SSD1_TXP
31 PCIE9_SSD1_TXN
31 PCIE9_SSD1_RXP
31 PCIE9_SSD1_RXN
31 PCIE10_SSD1_TXP
31 PCIE10_SSD1_TXN
31 PCIE10_SSD1_RXP
31 PCIE10_SSD1_RXN
31 PCIE11_SSD1_TXP
31 PCIE11_SSD1_TXN
31 PCIE11_SSD1_RXP
31 PCIE11_SSD1_RXN
31 PCIE12_SATA1A_SSD1_TXP
31 PCIE12_SATA1A_SSD1_TXN
31 PCIE12_SATA1A_SSD1_RXP
31 PCIE12_SATA1A_SSD1_RXN

M.2 PCIE X4 #1

PCH-H

USB2.0

USB2P_1 J2 IPD 14~24KOHM
USB2N_1 J3 IPD 14~24KOHM
USBP1 44
USBN1 44
IO USB3.1(Type-A_1)

USB2P_2 N15 IPD 14~24KOHM
USB2N_2 N13 IPD 14~24KOHM
USBP2 38
USBN2 38
RIGHT USB3.1(Type-A) -Power share

USB2P_3 K3 IPD 14~24KOHM
USB2N_3 K4 IPD 14~24KOHM
USBP3 38
USBN3 38
USB3.1(Type-A Rear)

USB2P_4 L9 IPD 14~24KOHM
USB2N_4 M10 IPD 14~24KOHM
USBP4 30
USBN4 30
TBT USB3.1(Type-C)

USB2P_5 L2 IPD 14~24KOHM
USB2N_5 M1 IPD 14~24KOHM
USBP5 48
USBN5 48
WEBCAM

USB2P_6 K6 IPD 14~24KOHM
USB2N_6 K7 IPD 14~24KOHM
USBP6 44
USBN6 44
Card Reader

USB2P_7 L3 IPD 14~24KOHM
USB2N_7 L4 IPD 14~24KOHM
1
1
T2000 NOBOM
T2001 NOBOM

USB2P_8 G5 IPD 14~24KOHM
USB2N_8 G4 IPD 14~24KOHM

USB2P_9 N8 IPD 14~24KOHM
USB2N_9 M6 IPD 14~24KOHM
USBP9 44
USBN9 44
Finger Print Reader

USB2P_10 H2 IPD 14~24KOHM
USB2N_10 H3 IPD 14~24KOHM

USB2P_11 P9 IPD 14~24KOHM
USB2N_11 R10 IPD 14~24KOHM
USBP11 50
USBN11 50
ELC

USB2P_12 G2 IPD 14~24KOHM
USB2N_12 G1 IPD 14~24KOHM

USB2P_13 N2 IPD 14~24KOHM
USB2N_13 N3 IPD 14~24KOHM

USB2P_14 F6 IPD 14~24KOHM
USB2N_14 E5 IPD 14~24KOHM
USBP14 33
USBN14 33
M.2 2230 WLAN KEY-E

Change from port7 due to INTEL CNVi uggest - X01/0801

USB3.1

USB31_1_TXP F7 USB3_TX_P1
USB31_1_TXN F9 USB3_TX_N1
USB31_1_RXP C11
USB31_1_RXN D11
USB3_TX_P1 44
USB3_TX_N1 44
USB3_RX_P1 44
USB3_RX_N1 44
IO USB3.1(Type-A_1)

USB31_2_TXP D4 USB3_TX_P2_C C2002 1 2 0.1UF/6.3V
USB31_2_TXN C3 USB3_TX_N2_C C2003 1 2 0.1UF/6.3V
USB31_2_RXP C9
USB31_2_RXN B9
USB3_TX_P2 38
USB3_TX_N2 38
USB3_RX_P2 38
USB3_RX_N2 38
RIGHT USB3.1(Type-A) -Power share

USB31_3_TXP G12 USB3_TX_P3_C C2004 1 2 0.1UF/6.3V
USB31_3_TXN F11 USB3_TX_N3_C C2005 1 2 0.1UF/6.3V
USB31_3_RXP C10
USB31_3_RXN B10
USB3_TX_P3 38
USB3_TX_N3 38
USB3_RX_P3 38
USB3_RX_N3 38
USB3.1(Type-A Rear)

USB31_4_TXP C14
USB31_4_TXN B14
USB31_4_RXP J15
USB31_4_RXN K16

USB31_5_TXP B15
USB31_5_TXN C15
USB31_5_RXP K13
USB31_5_RXN J13

USB31_6_TXP C16
USB31_6_TXN C17
USB31_6_RXP F14
USB31_6_RXN G14

USB2_ID G3
USB2_VBUSSENSE F3 USB2_VBUSSENSE

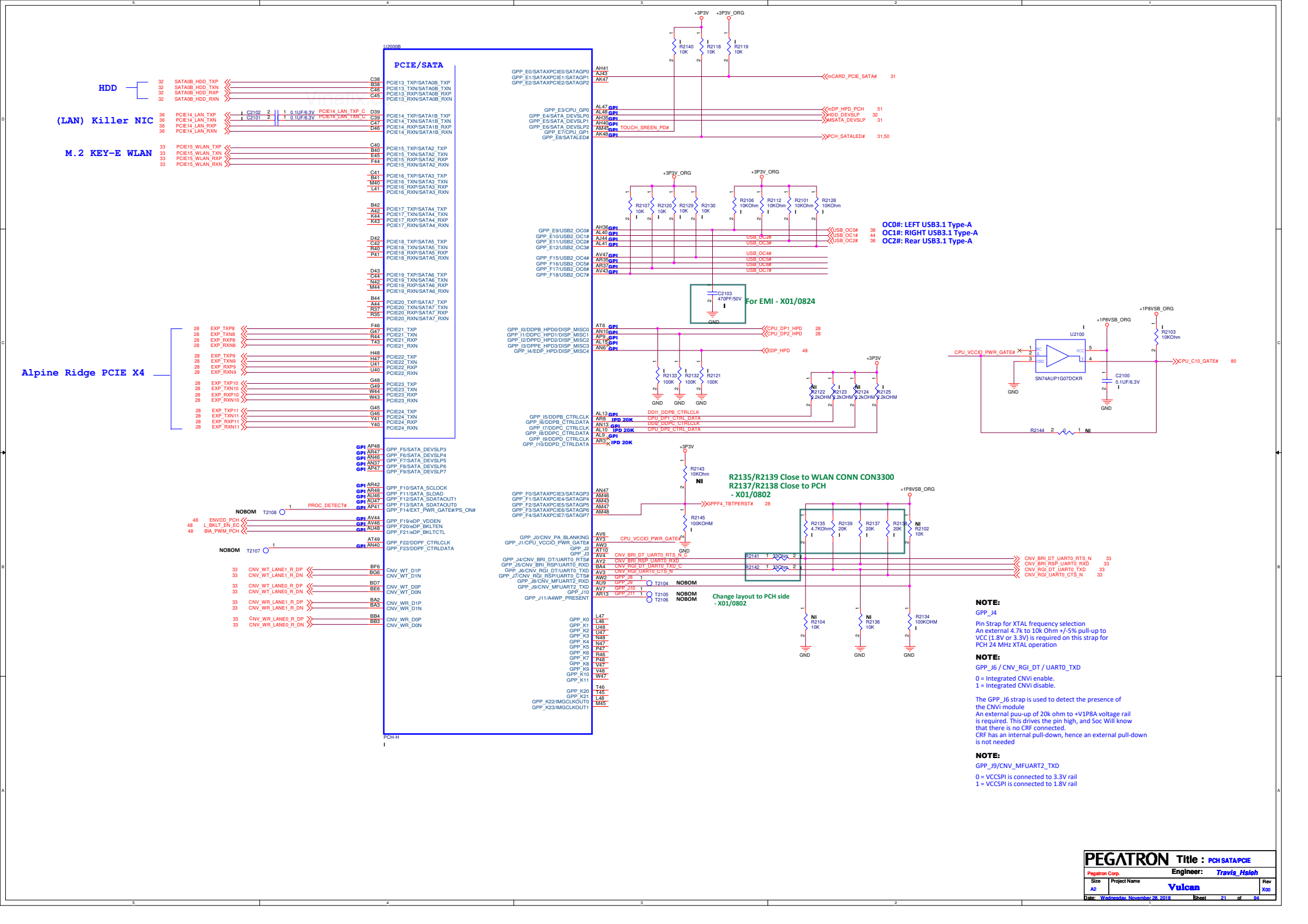
R2000 1K NI
R2001 0Ohm NOBOM
GND
GND

PEGATRON Title : PCH DMI_PCIE_USB_SATA

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 20 of 94


HDD
(LAN) Killer NIC
M.2 KEY-E WLAN
Alpine Ridge PCIE X4
PCIE/SATA
U2000B
PCH-H
OC0#: LEFT USB3.1 Type-A
OC1#: RIGHT USB3.1 Type-A
OC2#: Rear USB3.1 Type-A
For EMI - X01/0824
R2135/R2139 Close to WLAN CONN CON3300
R2137/R2138 Close to PCH
- X01/0802
Change layout to PCH side
- X01/0802
NOTE:
GPP_J4
Pin Strap for XTAL frequency selection
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation
NOTE:
GPP_J6 / CNV_RGI_DT / UART0_TXD
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
The GPP_J6 strap is used to detect the presence of the CNVi module
An external puu-up of 20k ohm to +V1P8A voltage rail is required. This drives the pin high, and Soc Will know that there is no CRF connected.
CRF has an internal pull-down, hence an external pull-down is not needed
NOTE:
GPP_J9/CNV_MFUART2_TXD
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
PEGATRON
Title : PCH SATA/PCIE
Pegatron Corp.
Engineer: Travis_Hsieh
Size A2
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 21 of 94

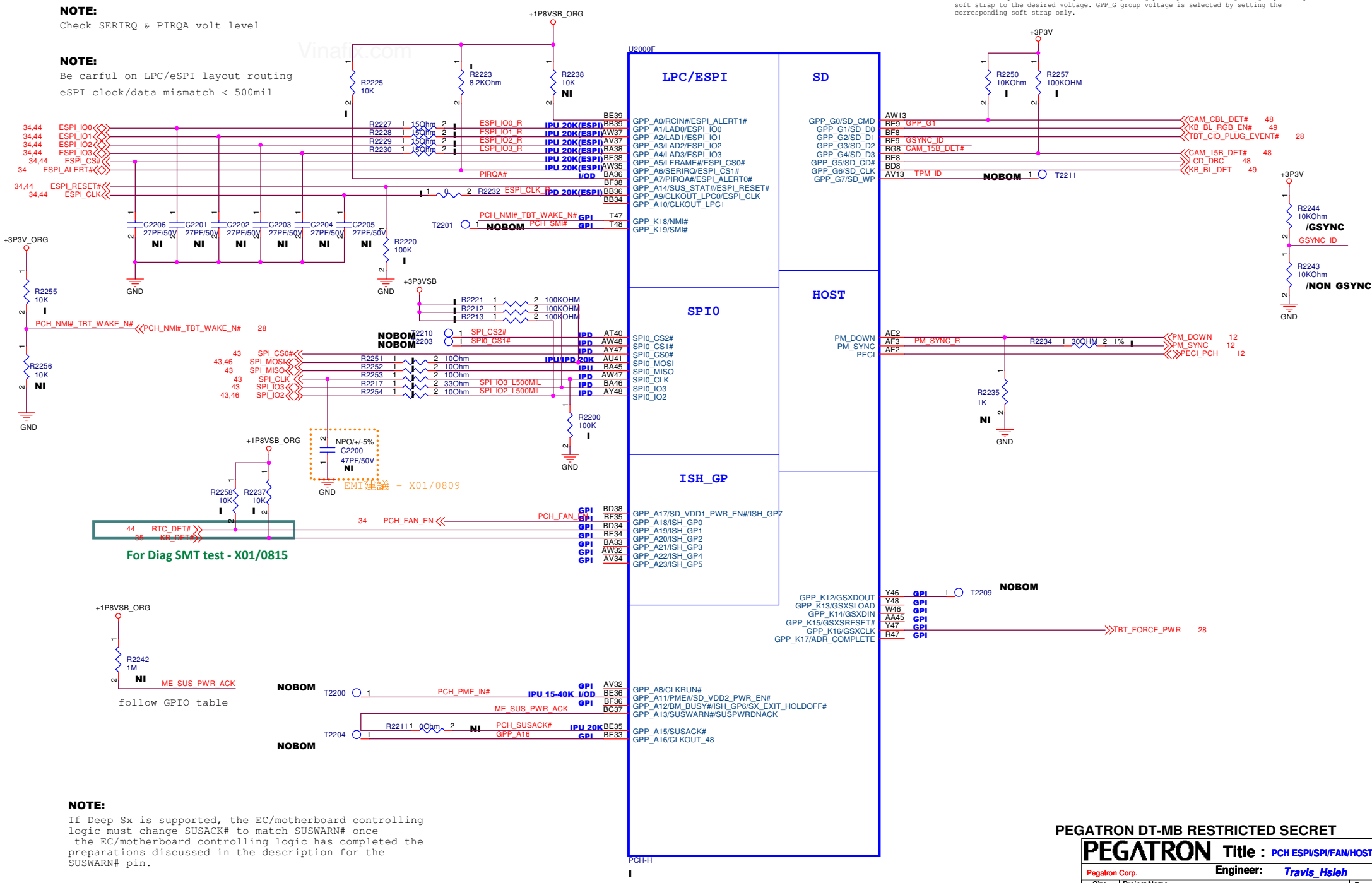
NOTE:
eSPI operates at 1.8V

NOTE:
Check SERIRQ & PIRQA volt level

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

NOTE:
Check GPP_A0 power well

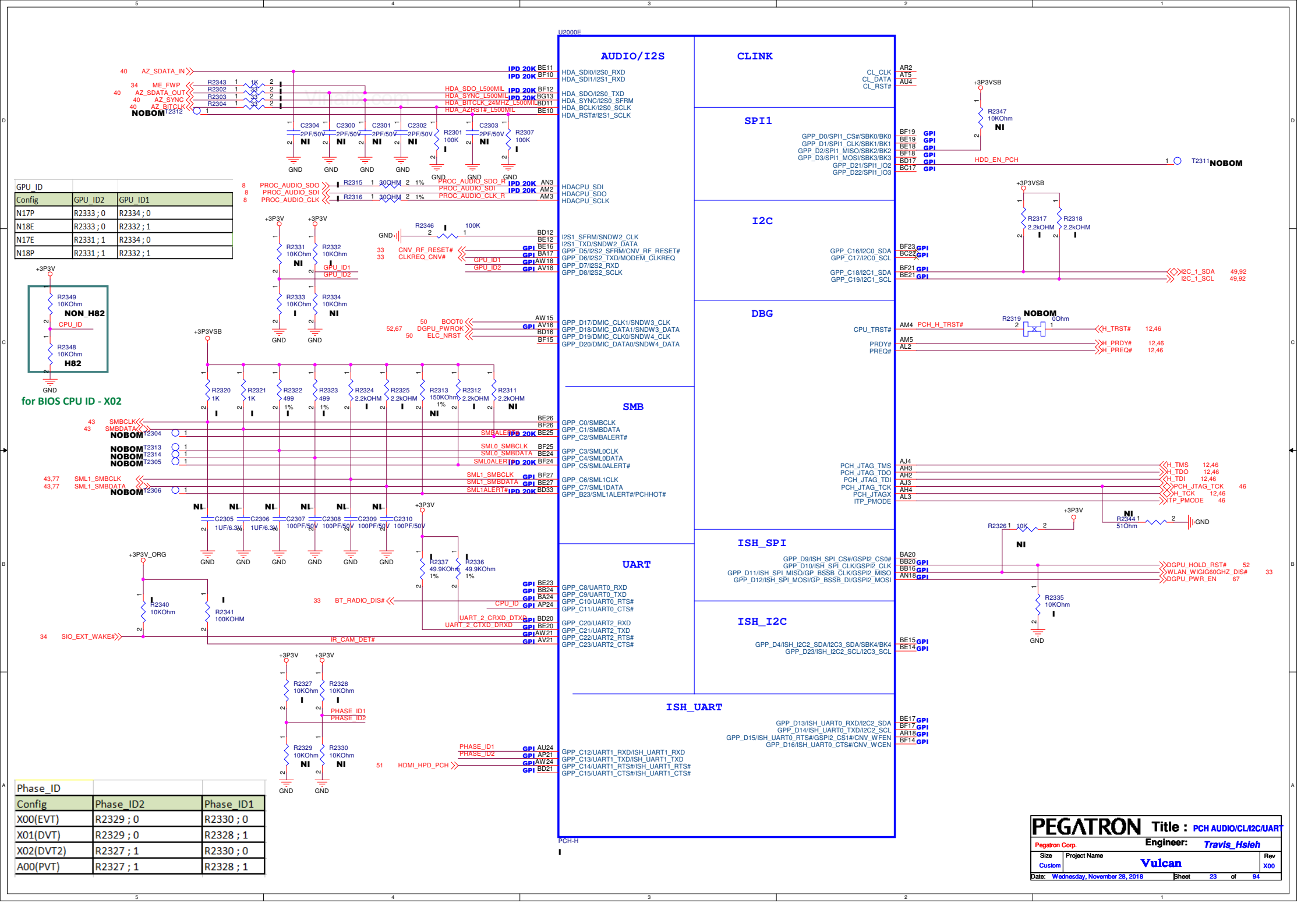
NOTE: GPP_G 1.8V for GPU
GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltageselection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.



NOTE:
If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCH ESPI/SPI/FAN/HOST	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 22 of 94	



GPU_ID		
Config	GPU_ID2	GPU_ID1
N17P	R2333 ; 0	R2334 ; 0
N18E	R2333 ; 0	R2332 ; 1
N17E	R2331 ; 1	R2334 ; 0
N18P	R2331 ; 1	R2332 ; 1

Phase_ID		
Config	Phase_ID2	Phase_ID1
X00(EVT)	R2329 ; 0	R2330 ; 0
X01(DVT)	R2329 ; 0	R2328 ; 1
X02(DVT2)	R2327 ; 1	R2330 ; 0
A00(PVT)	R2327 ; 1	R2328 ; 1

PEGATRON Title : PCH AUDIO/CL/I2C/UART

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 23 of 94

NOTE:
GPP_B22/GSPI1_MOSI

This Signal has a weak internal pull-down.
Offset 3410h:Bit 10
0: SPI
1: LPC

NOTE:
GSPI0_MOSI/GPP_B18

The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

for EA - X01/0830

for EA - X01/0830

for EA - X02/1121

for EA - X01/0830

for sequence - X01/0830

NOTE:
GPP_B14 / SPKR

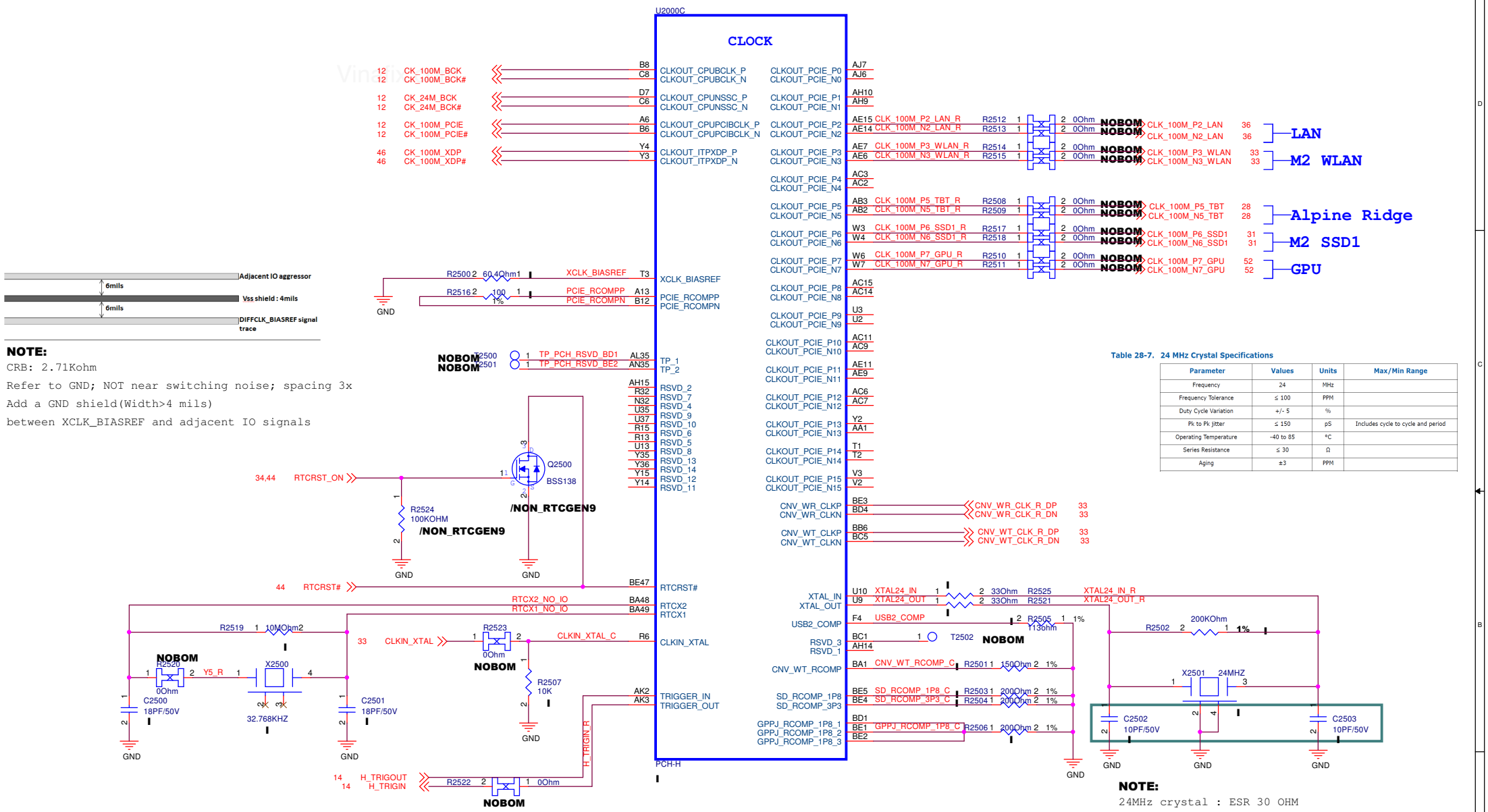
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

NOTE:
GPP_H15/SML3ALERT#
External pull-up is required. Recommend 100K if pulled

NOTE:
GPP_H12/SML2ALERT#

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

PEGATRON	Title : PCH SML/I2C/MISC		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 24 of 94		



NOTE:

CRB: 2.71Kohm

Refer to GND; NOT near switching noise; spacing 3x

Add a GND shield(Width>4 mils)

between XCLK_BIASREF and adjacent IO signals

Table 28-7. 24 MHz Crystal Specifications

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

NOTE:

24MHz crystal : ESR 30 OHM

follow vendor test report - X01/0829

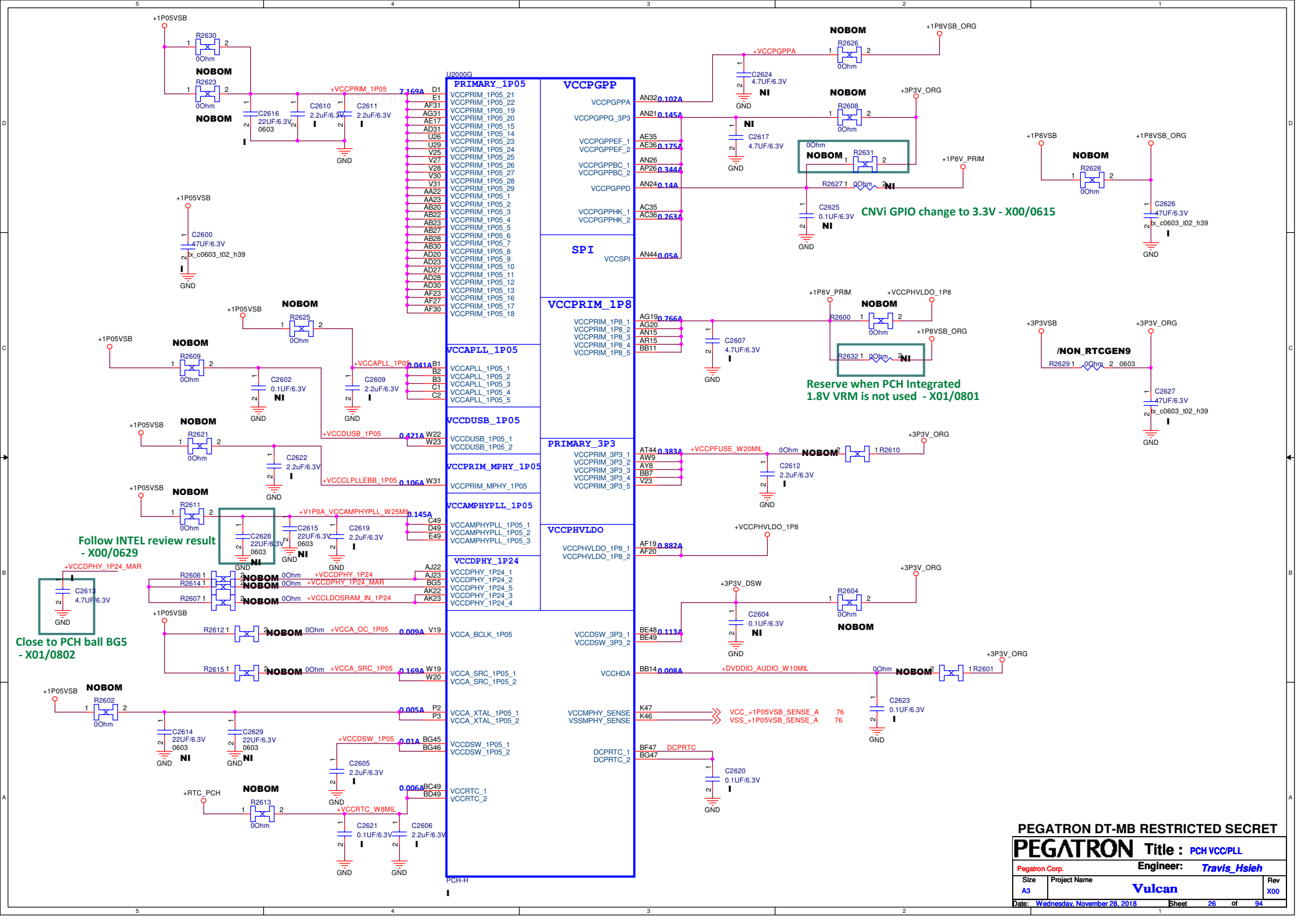
PEGATRON DT-MB RESTRICTED SECRET

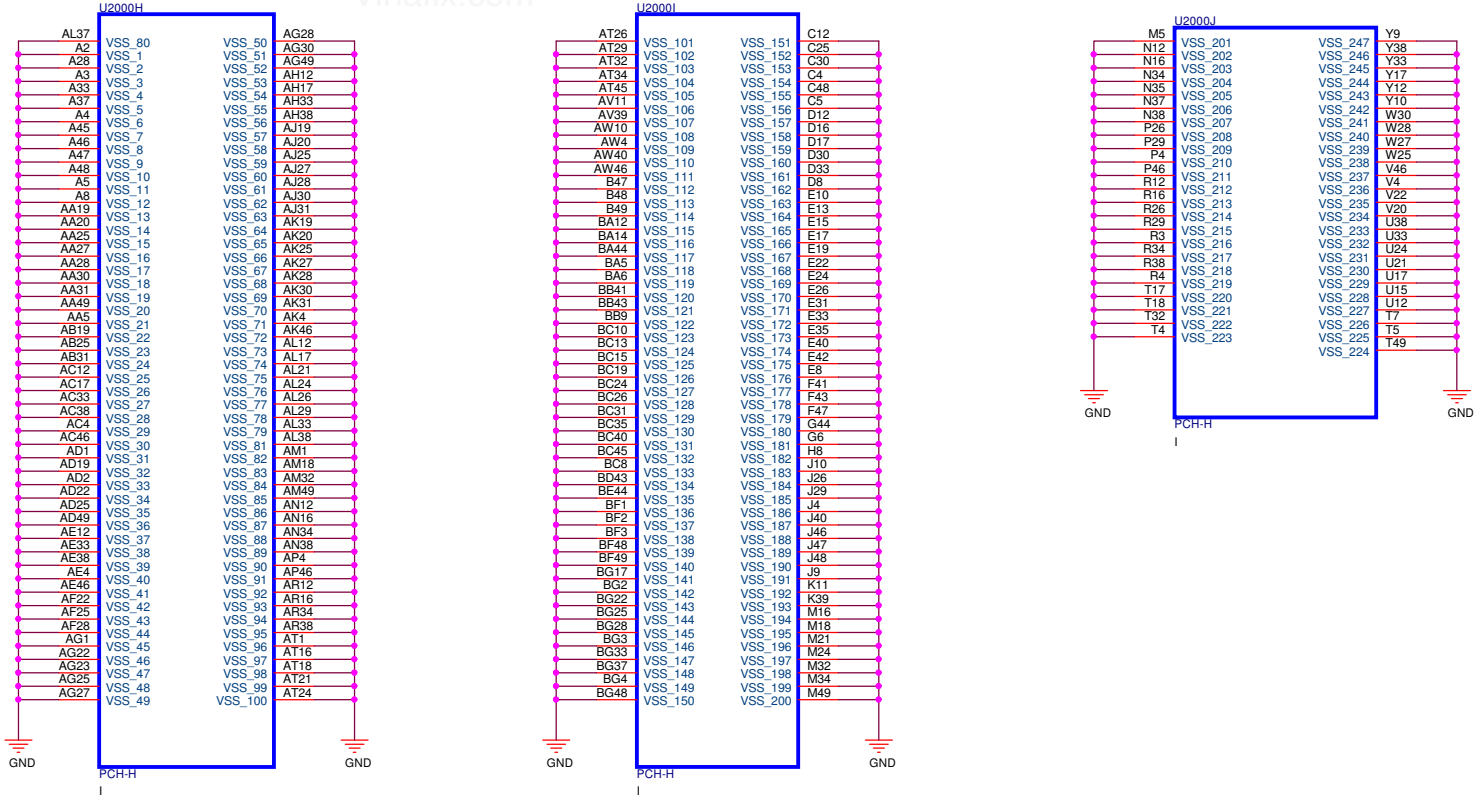
PEGATRON Title : PCH CLOCK

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 25 of 94


U2000G
PRIMARY_1P05
VCCPRIM_1P05_21
VCCPRIM_1P05_22
VCCPRIM_1P05_19
VCCPRIM_1P05_20
VCCPRIM_1P05_15
VCCPRIM_1P05_14
VCCPRIM_1P05_23
VCCPRIM_1P05_24
VCCPRIM_1P05_25
VCCPRIM_1P05_26
VCCPRIM_1P05_27
VCCPRIM_1P05_28
VCCPRIM_1P05_29
VCCPRIM_1P05_1
VCCPRIM_1P05_2
VCCPRIM_1P05_3
VCCPRIM_1P05_4
VCCPRIM_1P05_5
VCCPRIM_1P05_6
VCCPRIM_1P05_7
VCCPRIM_1P05_8
VCCPRIM_1P05_9
VCCPRIM_1P05_10
VCCPRIM_1P05_11
VCCPRIM_1P05_12
VCCPRIM_1P05_13
VCCPRIM_1P05_16
VCCPRIM_1P05_17
VCCPRIM_1P05_18
VCCAPLL_1P05
VCCAPLL_1P05_1
VCCAPLL_1P05_2
VCCAPLL_1P05_3
VCCAPLL_1P05_4
VCCAPLL_1P05_5
VCCDUSB_1P05
VCCDUSB_1P05_1
VCCDUSB_1P05_2
VCCPRIM_MPHY_1P05
VCCPRIM_MPHY_1P05
VCCAMPHYPLL_1P05
VCCAMPHYPLL_1P05_1
VCCAMPHYPLL_1P05_2
VCCAMPHYPLL_1P05_3
VCCDPHY_1P24
VCCDPHY_1P24_1
VCCDPHY_1P24_2
VCCDPHY_1P24_5
VCCDPHY_1P24_3
VCCDPHY_1P24_4
VCCA_BCLK_1P05
VCCA_SRC_1P05_1
VCCA_SRC_1P05_2
VCCA_XTAL_1P05_1
VCCA_XTAL_1P05_2
VCCDSW_1P05_1
VCCDSW_1P05_2
VCCRTC_1
VCCRTC_2
PCH-H
VCCPGPP
VCCPGPPA
VCCPGPPG_3P3
VCCPGPPEF_1
VCCPGPPEF_2
VCCPGPPBC_1
VCCPGPPBC_2
VCCPGPPD
VCCPGPPHK_1
VCCPGPPHK_2
SPI
VCCSPI
VCCPRIM_1P8
VCCPRIM_1P8_1
VCCPRIM_1P8_2
VCCPRIM_1P8_3
VCCPRIM_1P8_4
VCCPRIM_1P8_5
PRIMARY_3P3
VCCPRIM_3P3_1
VCCPRIM_3P3_2
VCCPRIM_3P3_3
VCCPRIM_3P3_4
VCCPRIM_3P3_5
VCCPHVLDO
VCCPHVLDO_1P8_1
VCCPHVLDO_1P8_2
VCCDSW_3P3_1
VCCDSW_3P3_2
VCCHDA
VCCMPHY_SENSE
VSSMPHY_SENSE
DCPRTC_1
DCPRTC_2
+1P05VSB
+VCCPRIM_1P05
+VCCAPLL_1P05
+VCCDUSB_1P05
+VCCCLPLLEBB_1P05
+V1P0A_VCCAMPHYPLL_W25MIL
+VCCDPHY_1P24
+VCCDPHY_1P24_MAR
+VCCLDOSRAM_IN_1P24
+VCCA_OC_1P05
+VCCA_SRC_1P05
+VCCDSW_1P05
+VCCRTC_W8MIL
+RTC_PCH
+VCCPGPPA
+3P3V_ORG
+1P8V_PRIM
+1P8VSB
+1P8VSB_ORG
+VCCPHVLDO_1P8
+3P3VSB
+3P3V_DSW
+VCCPFUSE_W20MIL
+DVDDIO_AUDIO_W10MIL
VCC_+1P05VSB_SENSE_A
VSS_+1P05VSB_SENSE_A
DCPRTC
NOBOM
NI
GND
CNVi GPIO change to 3.3V - X00/0615
Reserve when PCH Integrated
1.8V VRM is not used - X01/0801
Follow INTEL review result
- X00/0629
Close to PCH ball BG5
- X01/0802
/NON_RTCGEN9
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCH VCC/PLL
Pegatron Corp.
Engineer: Travis_Hsieh
Size A3
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 26 of 94



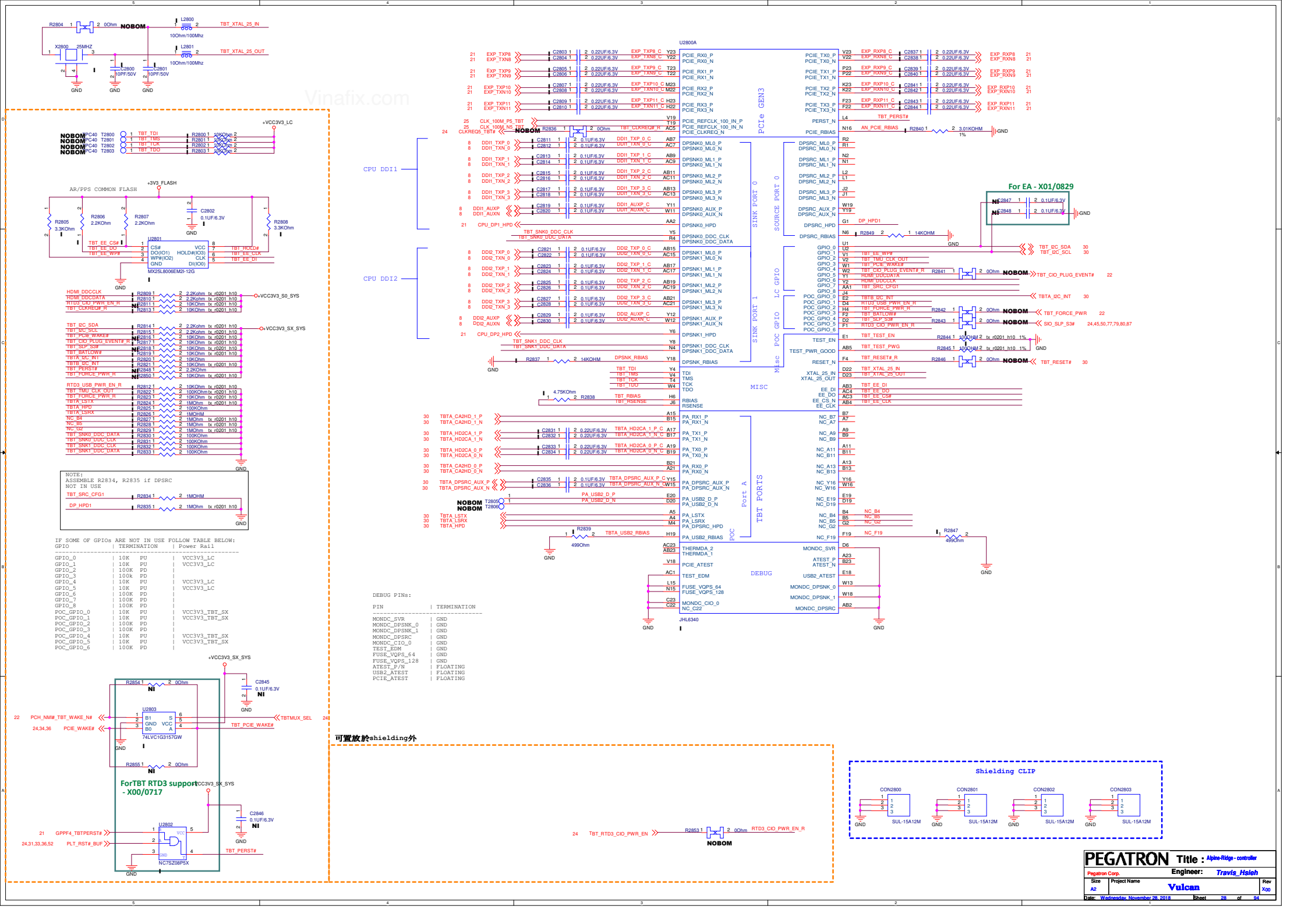
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH VSS

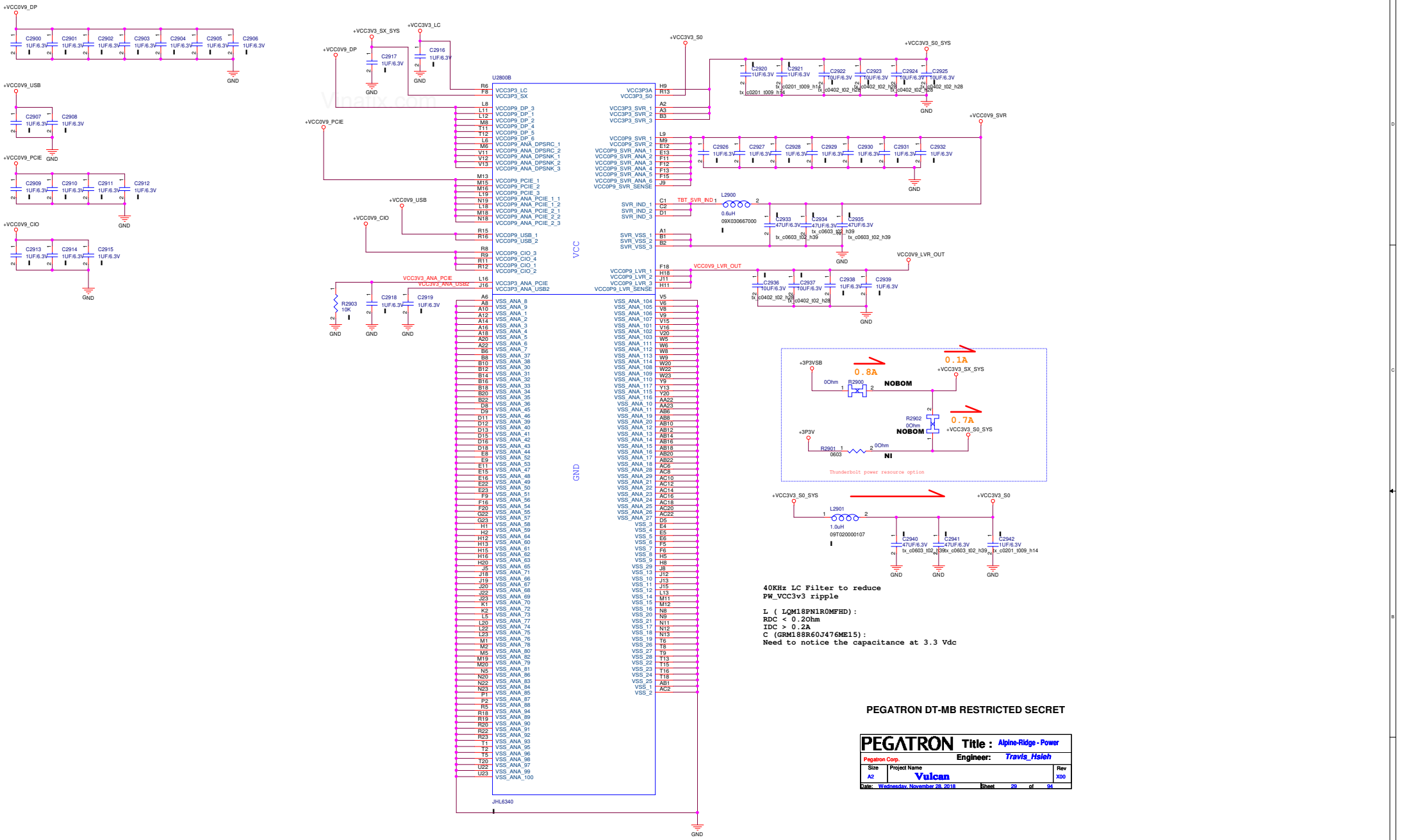
Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 27 of 94

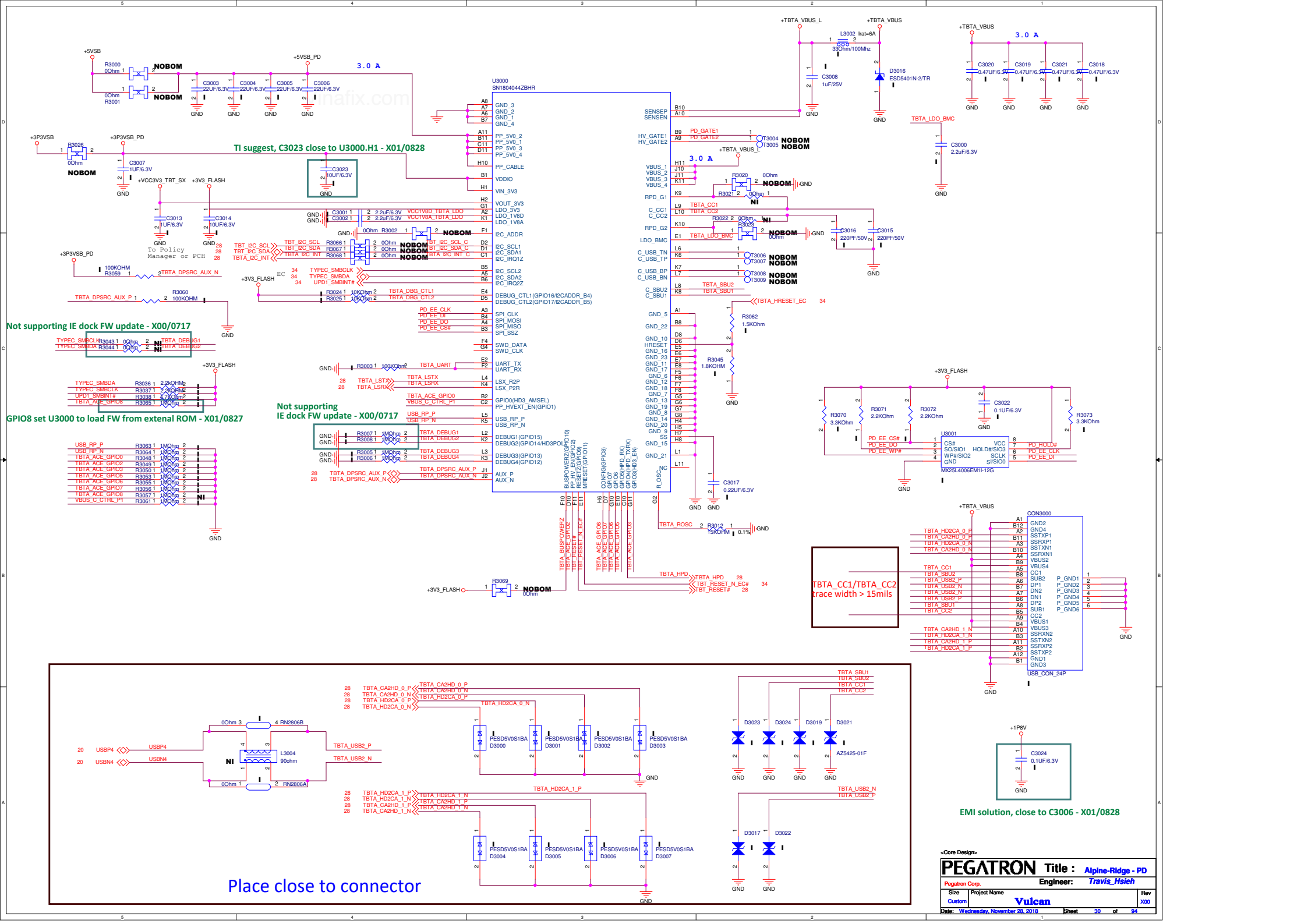


Title	Alpine-Ridge - controller
Company	Pegatron Corp.
Engineer	Travis_Hsieh
Size	A2
Project Name	Vulcan
Rev	X00
Date	Wednesday, November 28, 2018
Sheet	28 of 94

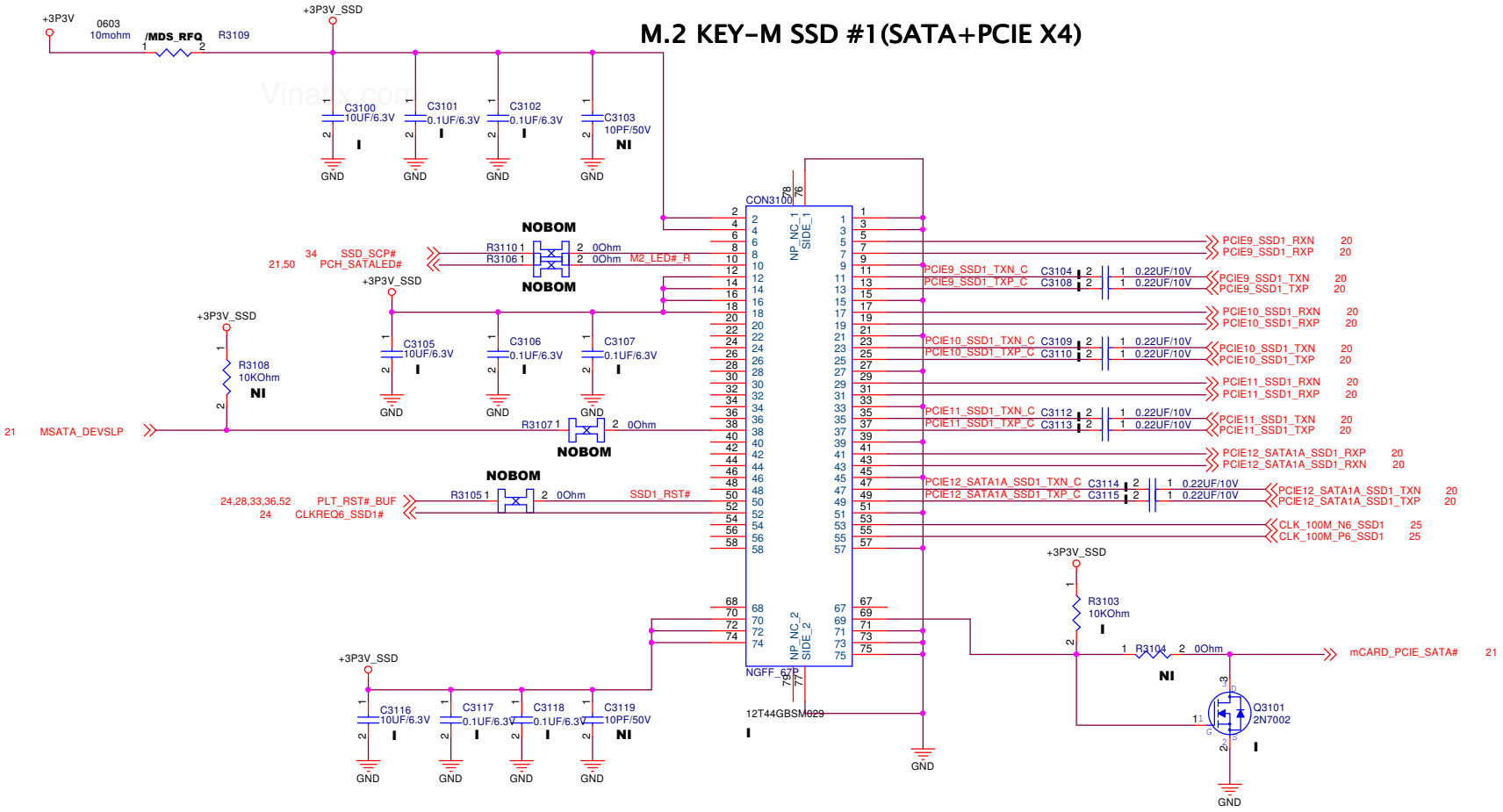


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : Alpine-Ridge - Power		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 29 of 94		

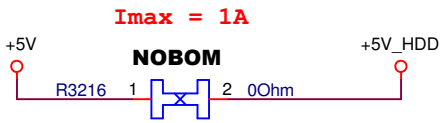

TI suggest, C3023 close to U3000.H1 - X01/0828
Not supporting IE dock FW update - X00/0717
GPIO8 set U3000 to load FW from extenal ROM - X01/0827
Not supporting IE dock FW update - X00/0717
TBTA_CC1/TBTA_CC2 trace width > 15mils
EMI solution, close to C3006 - X01/0828
Place close to connector
U3000
SN1804044ZBHR
3.0 A
NOBOM
NI
To Policy Manager or PCH
USB_CON_24P
MX25L4006EM1I-12G
PEGATRON
Title : Alpine-Ridge - PD
Engineer: Travis_Hsieh
Pegatron Corp.
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 30 of 94

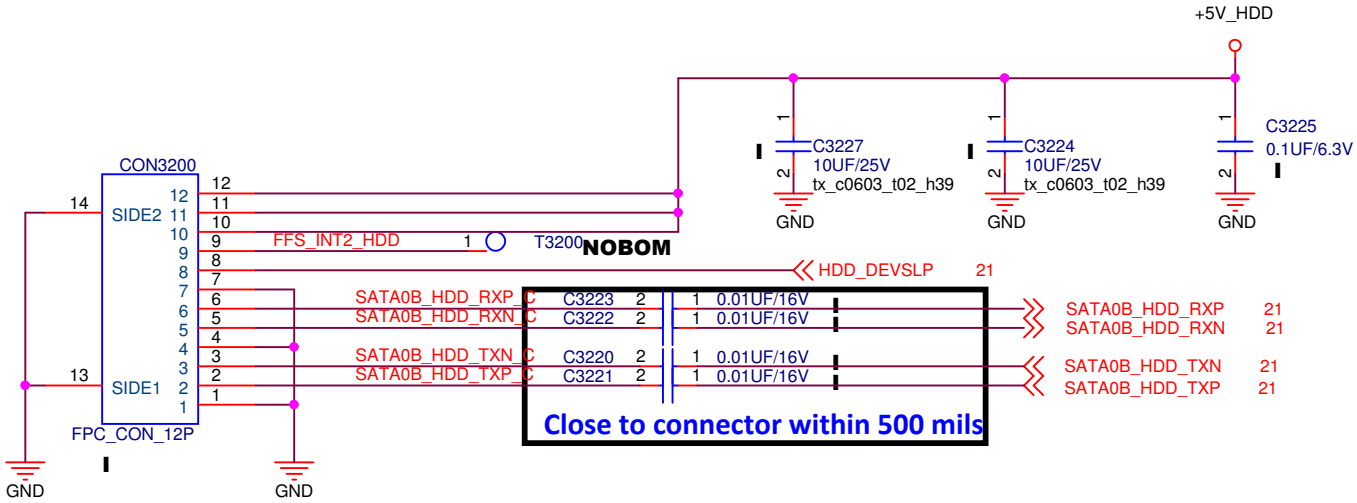
M.2 KEY-M SSD #1(SATA+PCIE X4)



PEGATRON	Title : M.2 2280 SSD #1	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 31 of 94	

HDD

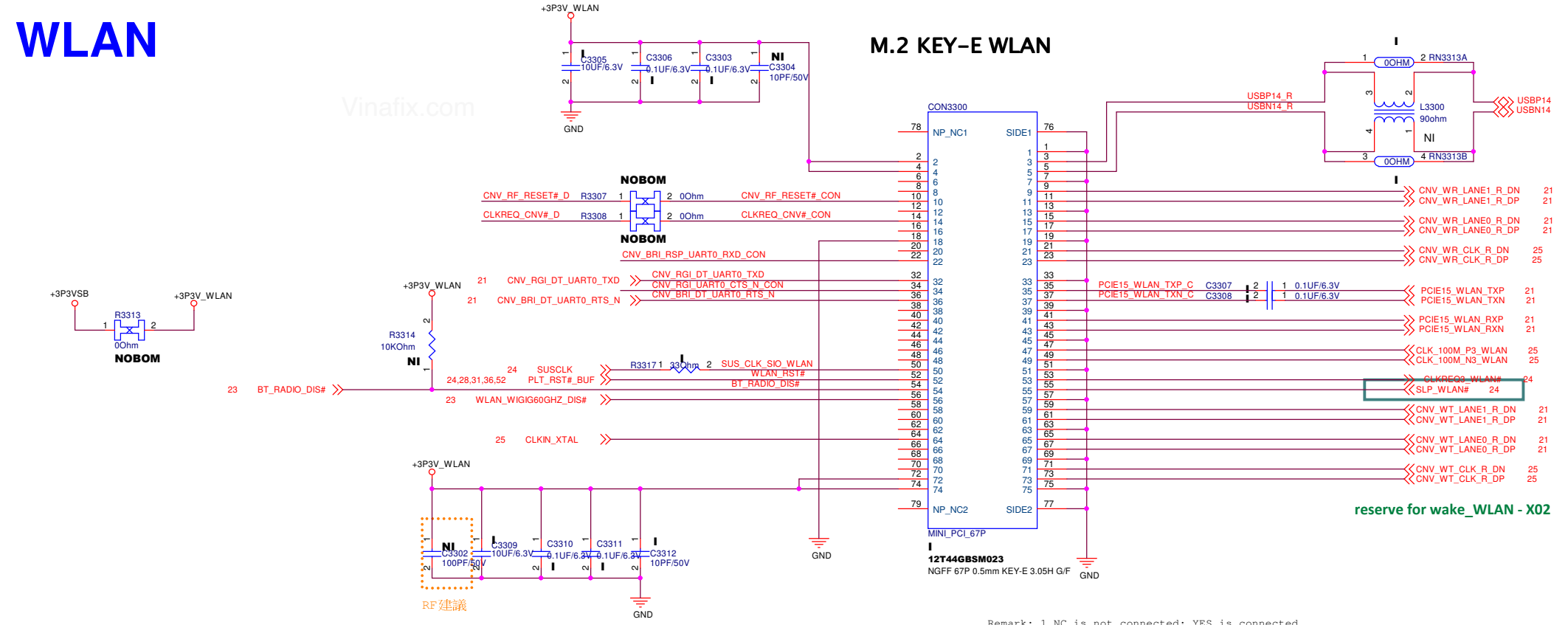




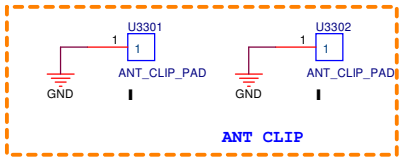
PEGATRON	Title : SATA HDD	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 32 of 94	

WLAN

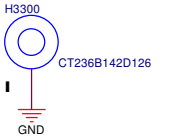
M.2 KEY-E WLAN

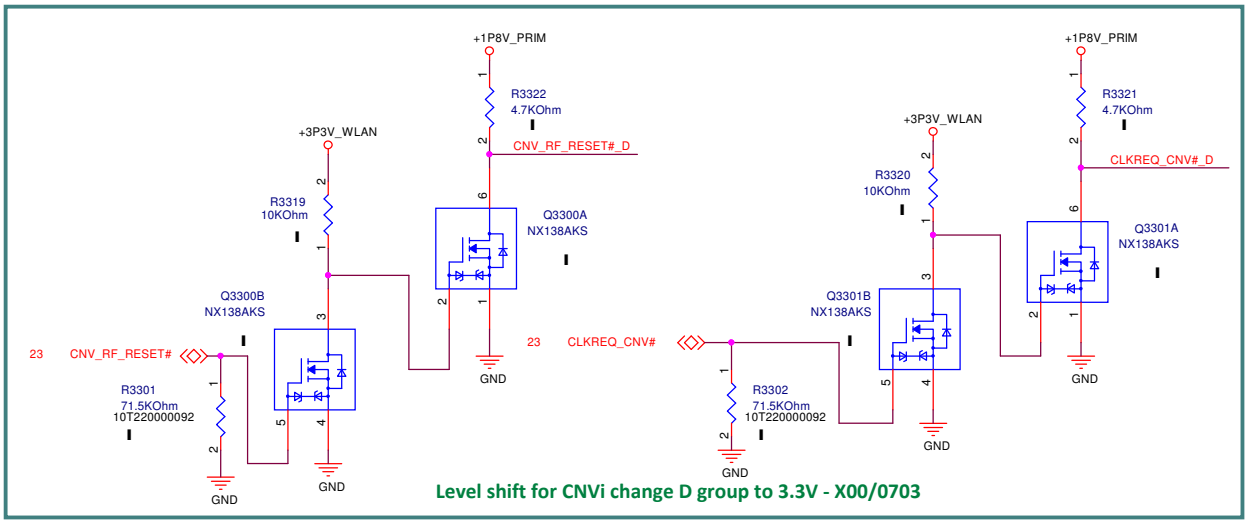


Remark: 1.NC is not connected; YES is connected.
2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A?5), Suggest platform NC those pins.
4. Pin44, 46, 48, QCA suggest platform to NC.
5. Pin17 and 19 suggest reserve test point at platform side.



RTC CLIP
13X020219000
U3303





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : M.2 KEY-A 2230 WLAN

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 33 of 94

Pull Up

EC Power

eSPI Strap

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note:
If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel.
If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Imax:12.5mA

PD reset follow reference design - X00

R3493 for EMC - X01/0730

debug test point placement together bottom side

Adapter power monitor to EC ADC pin

Battery power monitor to EC ADC pin

Turn off ELC in MDS - X02 10/24

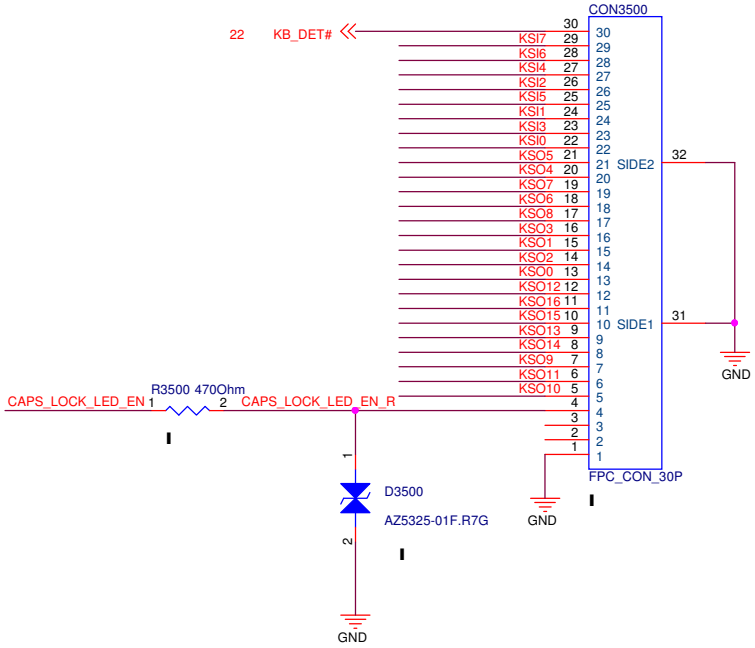
4 Resistor colay (R3497,R3410,R3498,R3499)

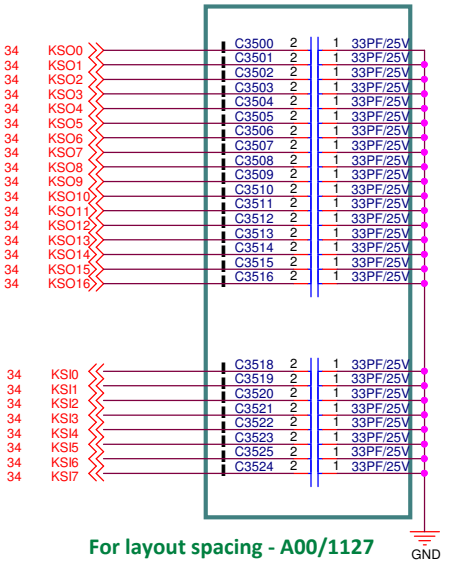
Board_ID		
config	Pull-High res ; R3412	Voltage
X00(EVT)	10K	3
X01(DVT)	17.8K	2.801
X02(DVT2)	27K	2.598
X03(reserve1)	37.4K	2.402
A00(PVT)	49.9K	2.201
A01	64.9K	2.001
A02	82.5K	1.808
A03	107K	1.594
Reserve2	154K	1.299
Reserve3	200K	1.1

MODEL_ID					
config	CPU	GPU	Pull-High res ; R3410	Voltage	
0	H62	N17P_G1/N18P_G0	10K	3	P-50W
1	H82	N17P_G1/N18P_G0	17.8K	2.801	
2	H62	N18P_G1	27K	2.598	P-60W
3	H82	N18P_G1	37.4K	2.402	
4	Reserve		49.9K	2.201	
5	Reserve		64.9K	2.001	
6	H62	N17E_G1/N18E_G1/N18E_G0	82.5K	1.808	E-60W/65W
7	H82	N17E_G1/N18E_G1/N18E_G0	107K	1.594	
8	H62	N18E_G2_G3	154K	1.299	E-80W
9	H82	N18E_G2_G3	200K	1.1	

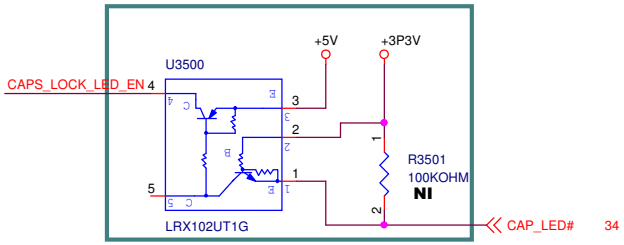
PEGATRON Title : EC
Pegatron Corp. Engineer: Travis_Hsieh
Size A2 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 Sheet 34 of 94

KeyBoard connector





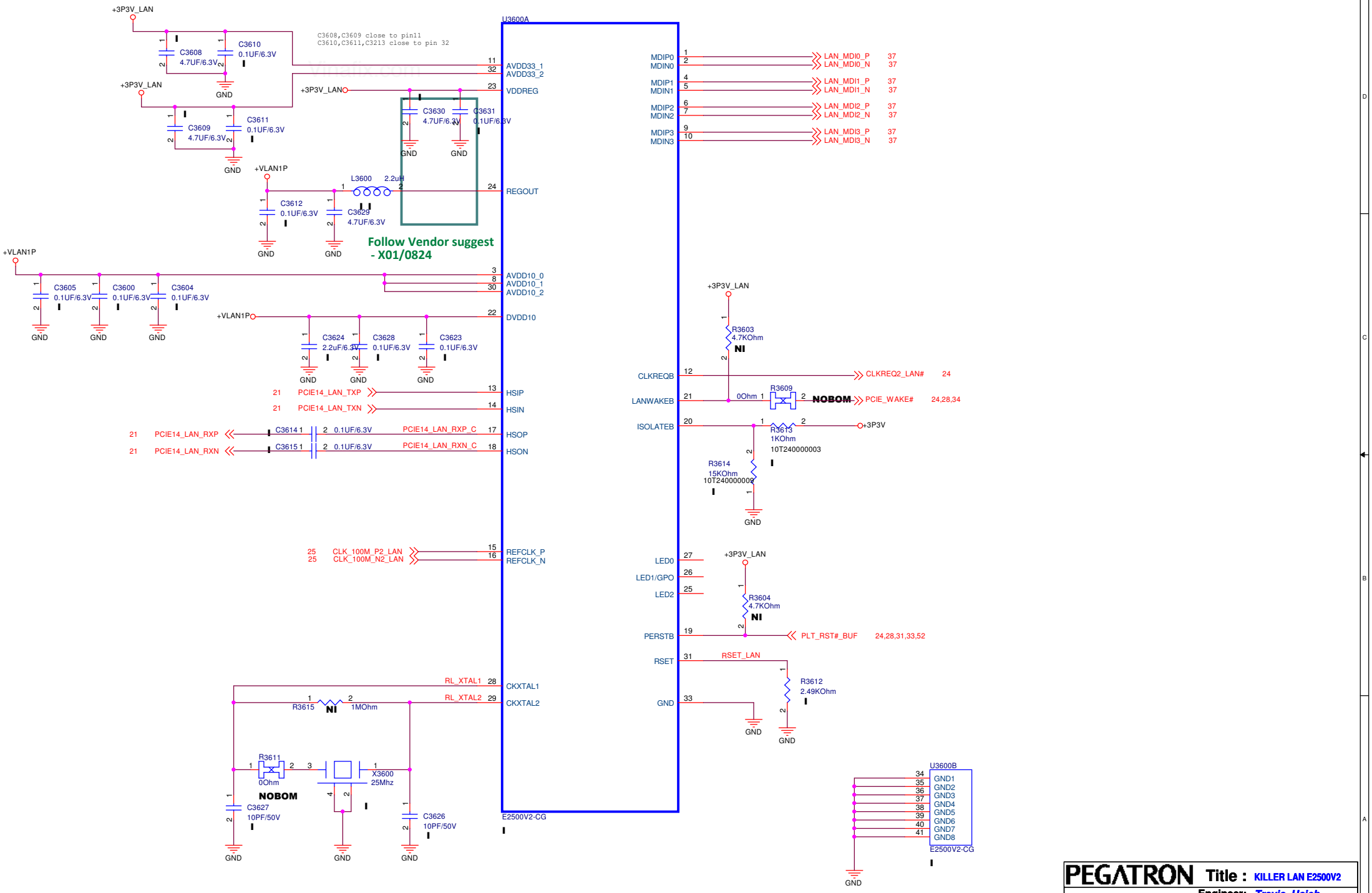
For layout spacing - A00/1127



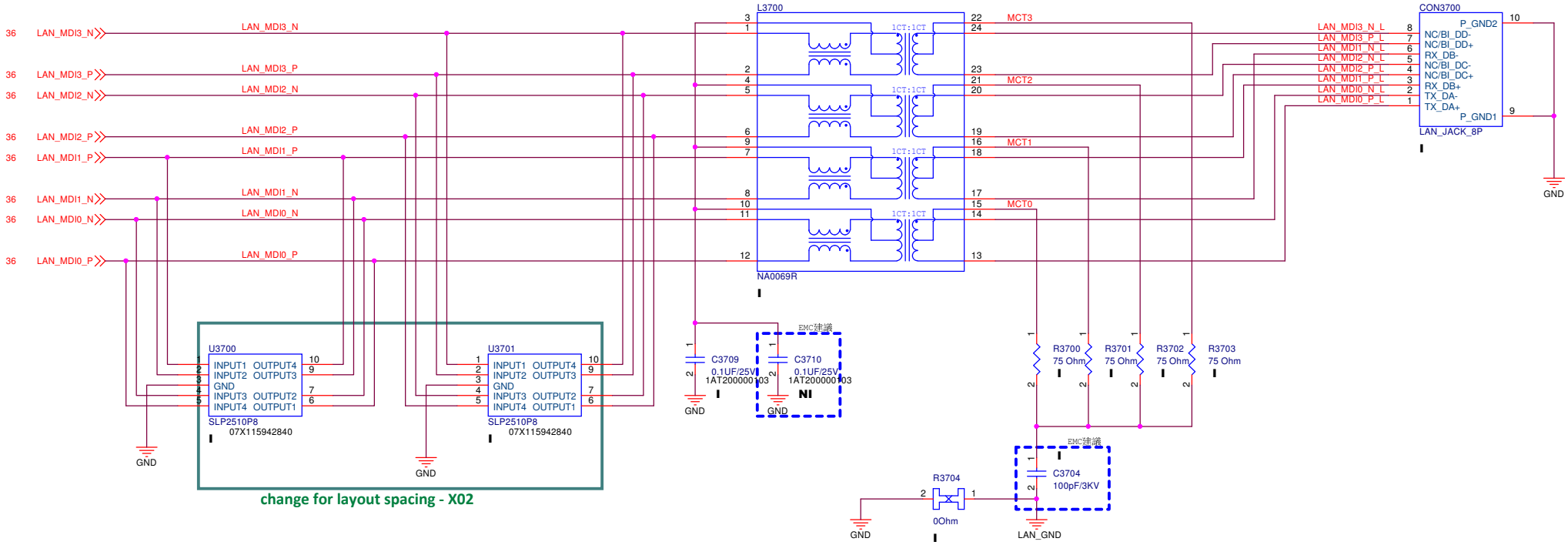
TX pool change to MX per CE request - X01/0801

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : KB & NKRO	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: B	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 35 of 94	



PEGATRON	Title : KILLER LAN E2500V2		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A3	Project Name: Vulcan		Rev: B00
Date: Wednesday, November 28, 2018	Sheet 36 of 95		



<Core Design>

PEGATRON Title : LAN JACK

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 37 of 94

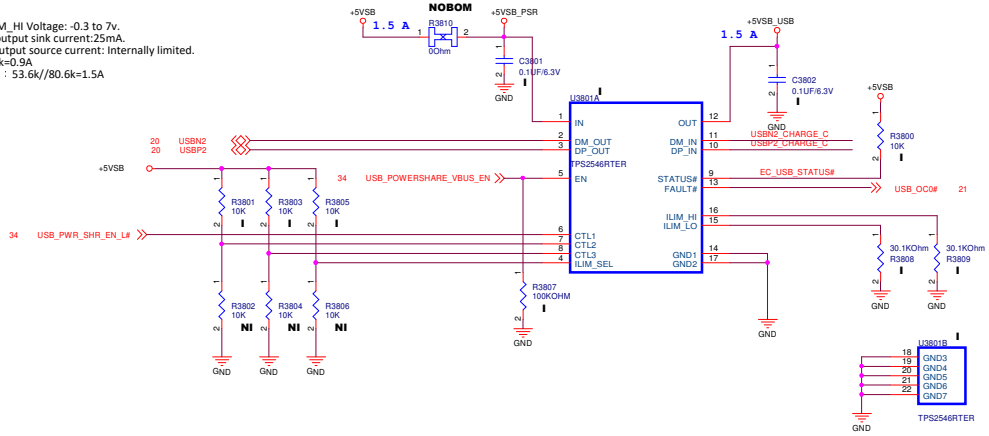
Power Share

Table 2. Truth Table

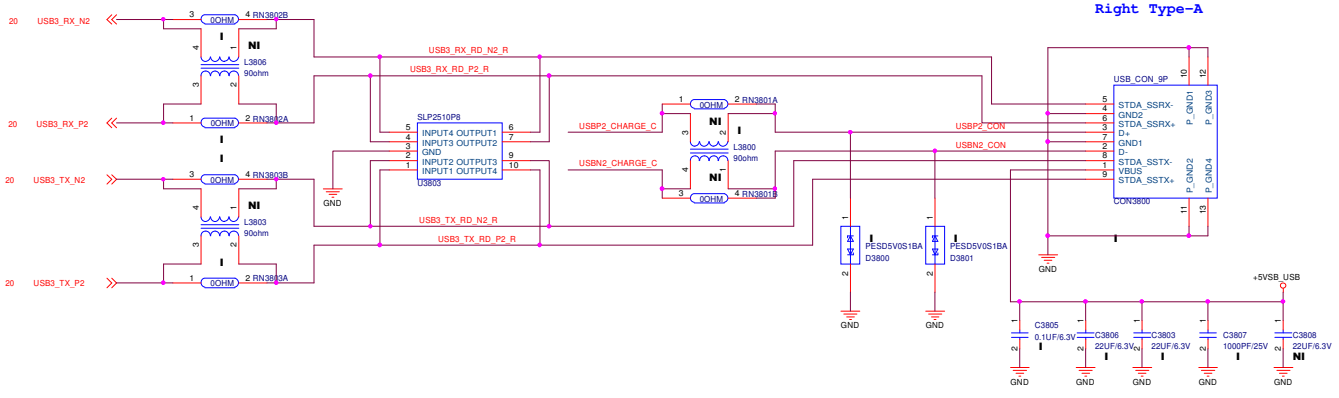
CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	I_{OS_PW} & ILIM_HI(1)	DCP load present(2)	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP _Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2(4)	ILIM_LO	OFF	
1	1	1	1	CDP(4)	ILIM_HI	CDP load present(5)	Data Lines Connected and Load Detect Active

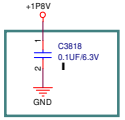
(1) TPS2546 : Current limit (I_{OS}) is automatically switched between I_{OS_PW} and the value set by ILIM_HI according to the Load Detect – Power Wake functionality.
(2) DCP Load present governed by the "Load Detection – Power Wake" limits.
(3) DCP Load present governed by the "Load Detection – Non Power Wake" limits.
(4) No OUT discharge when changing between 1111 and 1110.
(5) CDP Load present governed by the "Load Detection – Non Power Wake" limits and BC1.2 primary detection.

STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: -0.3 to 7v.
STATUS#, FAULT# Continuous output sink current:25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.
SDP Mode(S0/S3/S4/S5) : 53.6k=0.9A
CDP(S0)& DCP(S3/S4/S5) Mode : 53.6k//80.6k=1.5A



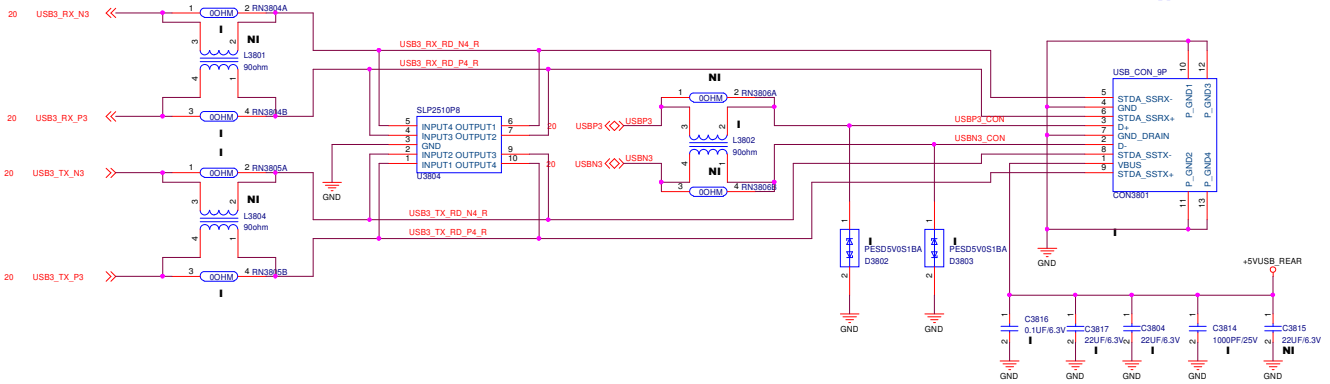
Right Type-A

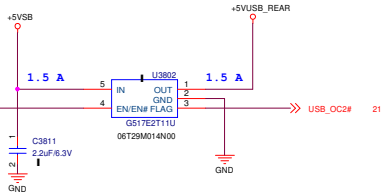




EMI solution, close to CON3800 - X01/0828

Rear Type-A





<Core Design>

PEGATRON Corp.

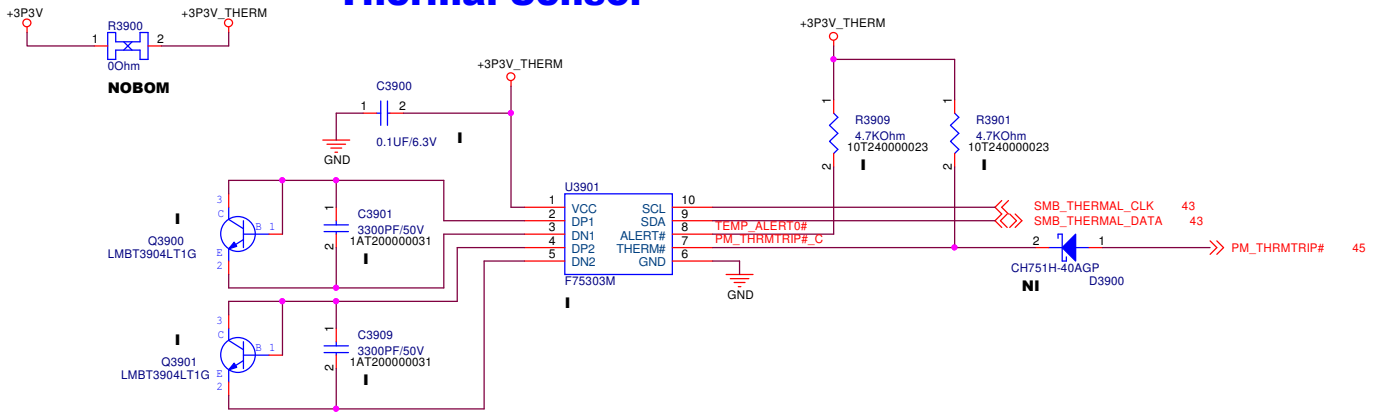
Title : USB CONN & POWER

Engineer: Travis_Hsieh

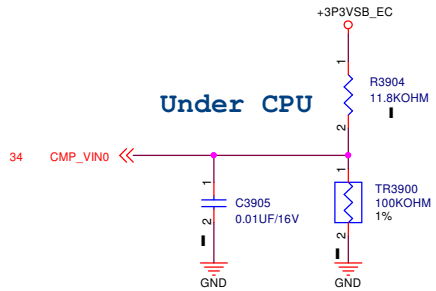
Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 38 of 94

Thermal Sensor



U3901: Under GPU thermal pipe
Q3900: Under CPU thermal pipe
Q3901: Close to SSD connector



<Core Design>

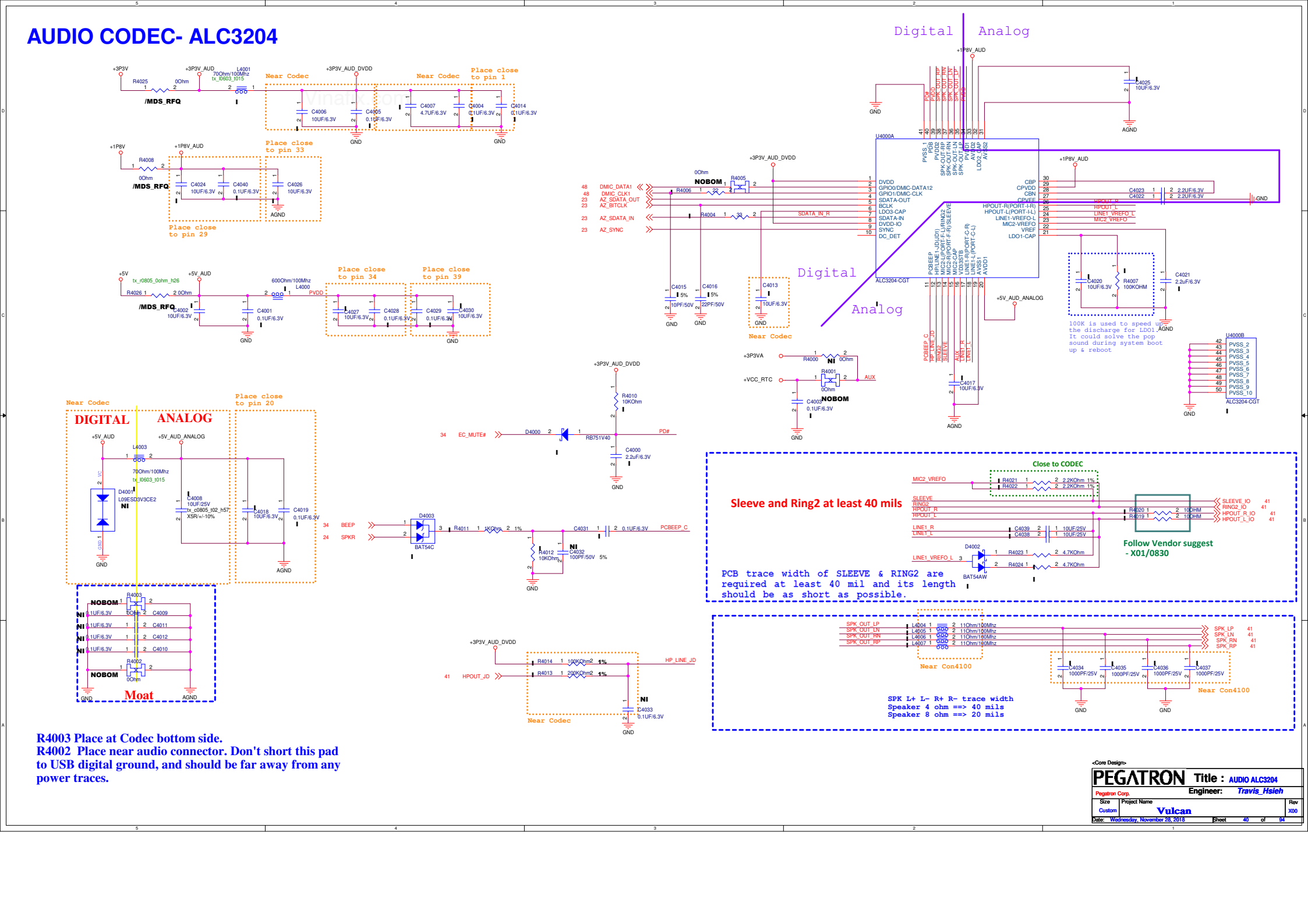
PEGATRON Title : SENSOR

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 39 of 94

AUDIO CODEC- ALC3204



R4003 Place at Codec bottom side.
R4002 Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

<Core Design>

PEGATRON Title : AUDIO ALC3204

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 40 of 94

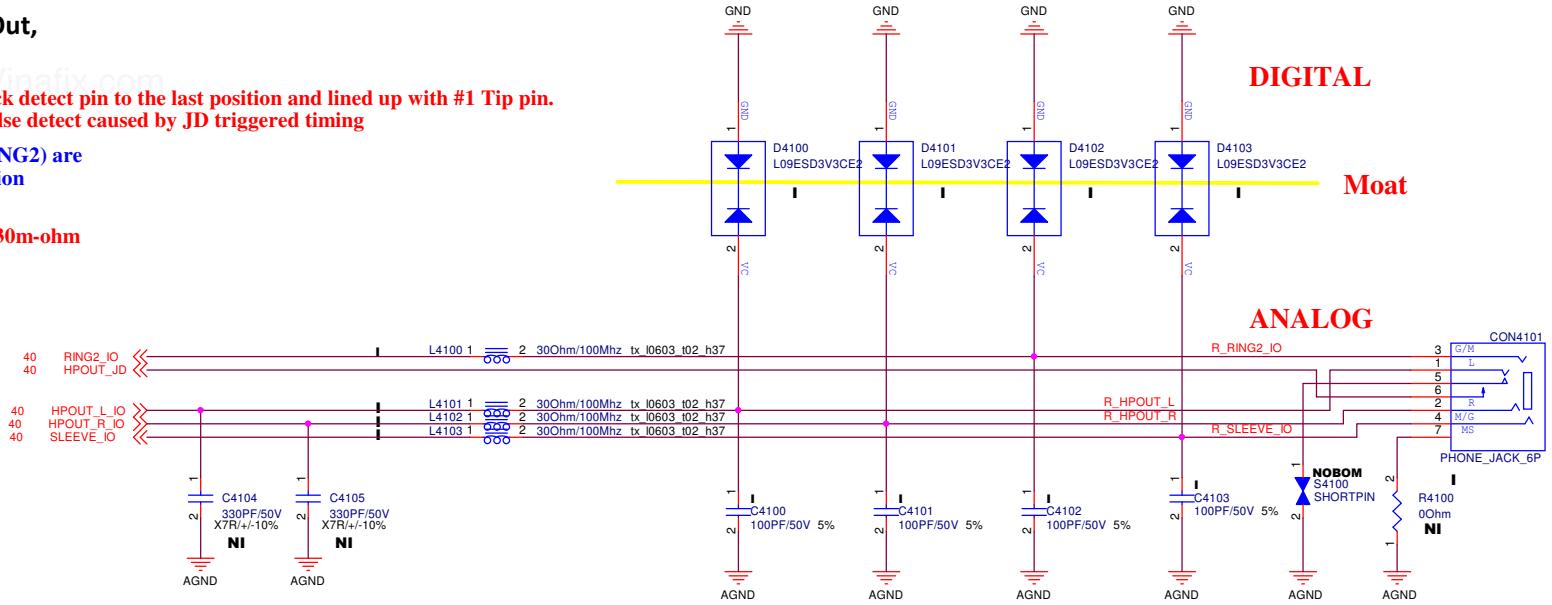
GLOBAL HEADSET CONNECTOR

OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

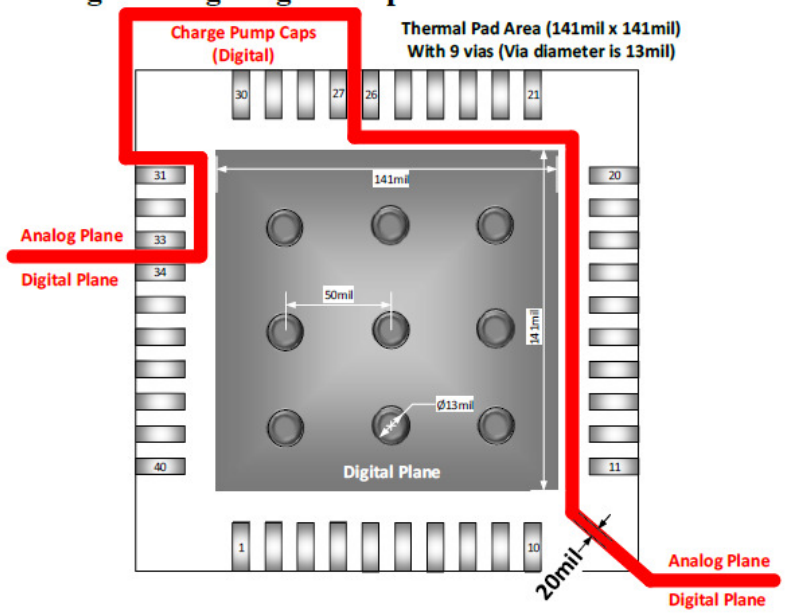
This recommended phone-jack has moved #5/#6 Jack detect pin to the last position and lined up with #1 Tip pin. This kind of design will significantly improve the false detect caused by JD triggered timing

PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.

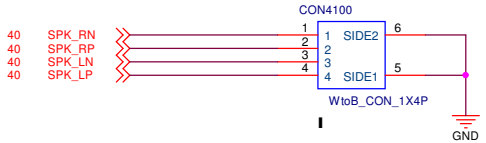
L4100/L4103 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.



Separate Analog and Digital ground plane



SPEAKER CONN



<Core Design>

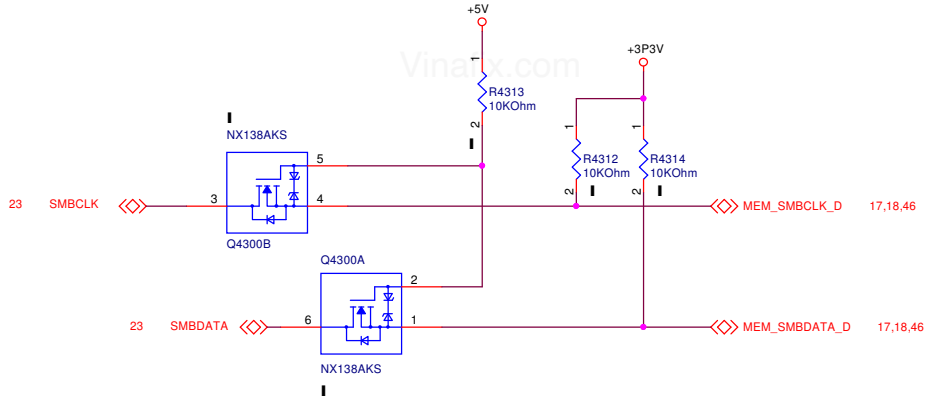
PEGATRON	Title :	AUDIO JACK	
Pegatron Corp.	Engineer:	Travis_Hsieh	
Size: A3	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 41 of 94		

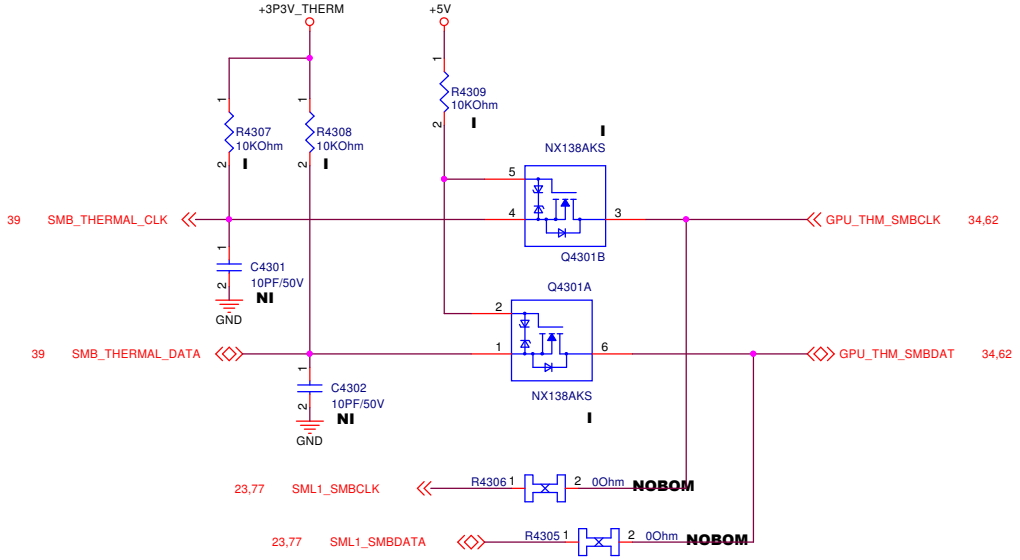
Reserved Page

<Core Design>

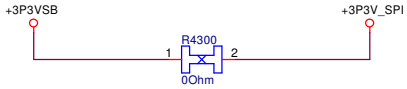
PEGATRON	Title : Reserved	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 42 of 94	

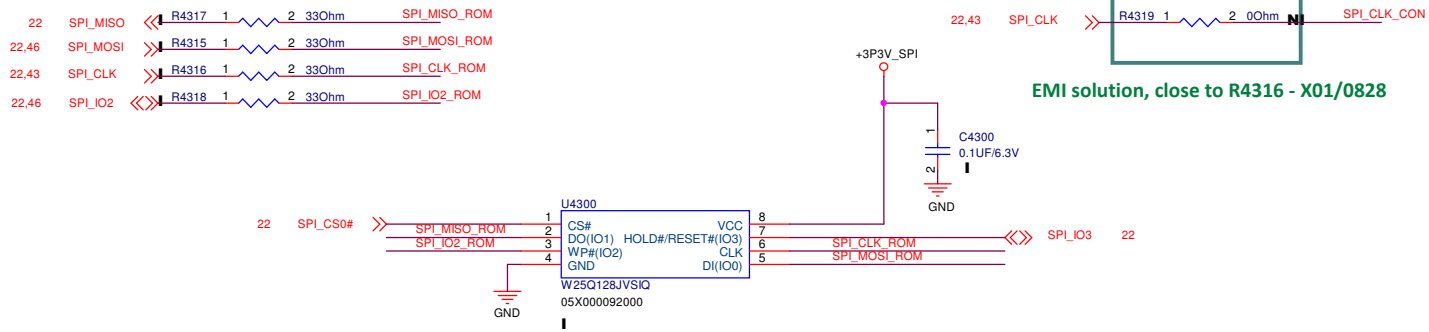
SMBUS

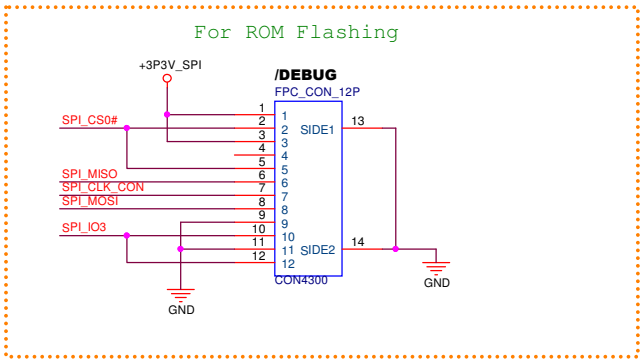




SPI ROM (Quad I/O Supported)

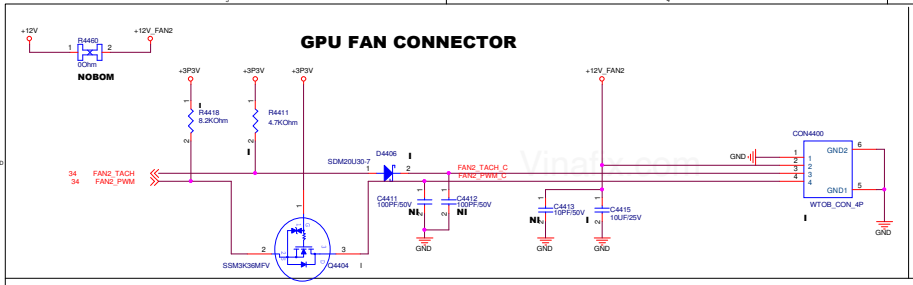


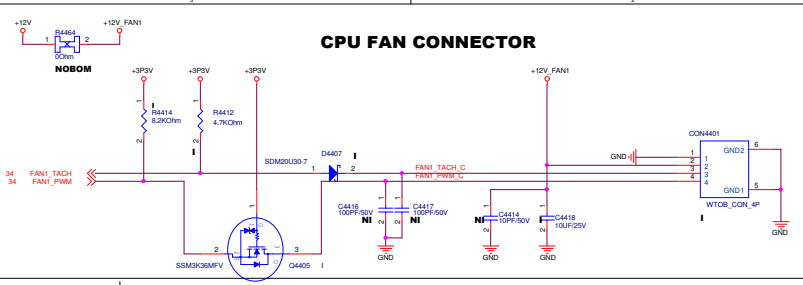


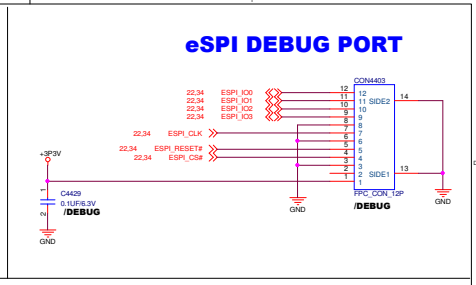


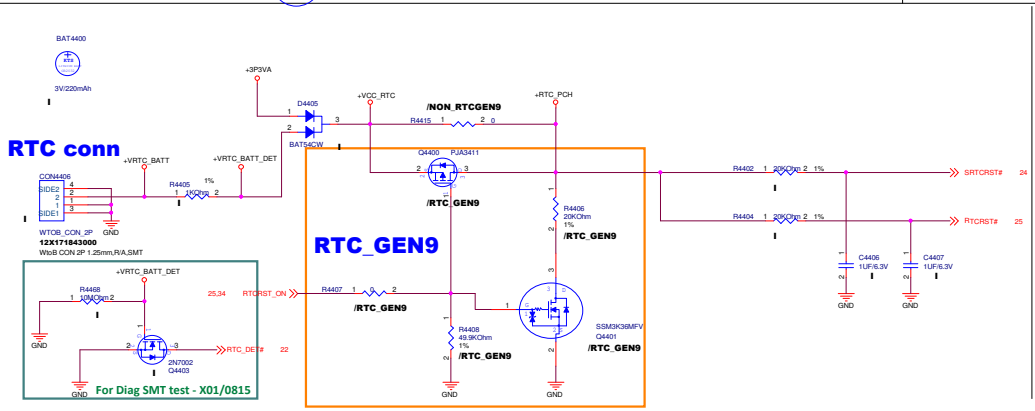
PEGATRON DT-MB RESTRICTED SECRET

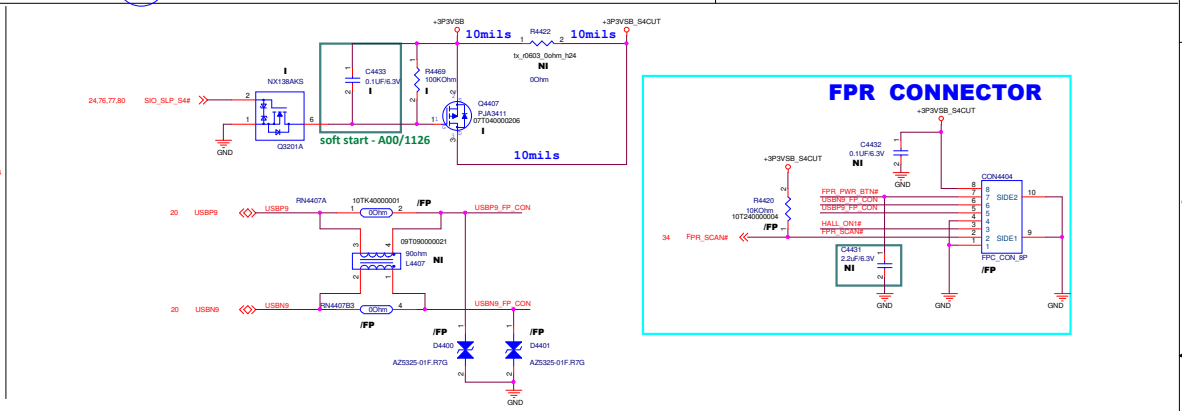
PEGATRON	Title : SM BUS & SPI ROM		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size A3	Project Name Vulcan		Rev X00
Date: Wednesday, November 28, 2018	Sheet 43 of 94		

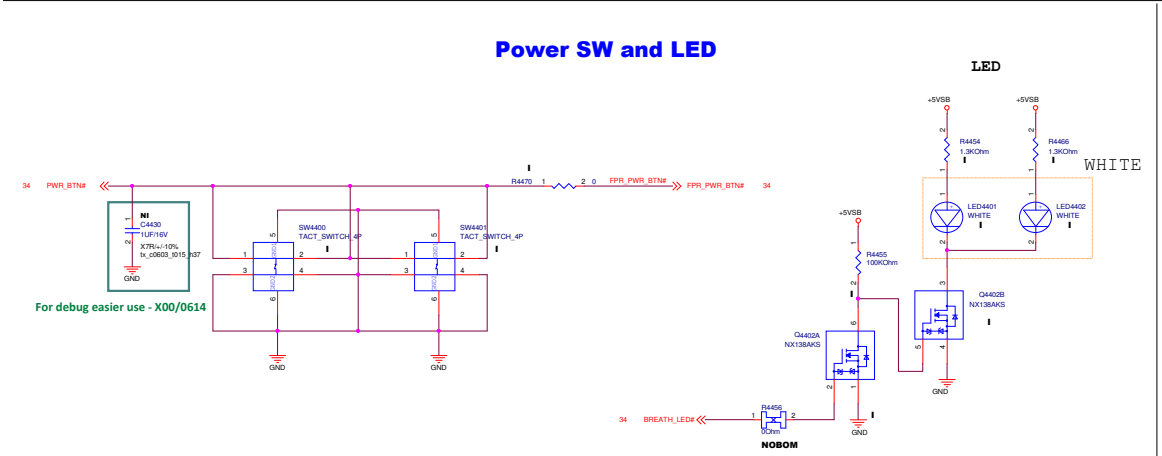


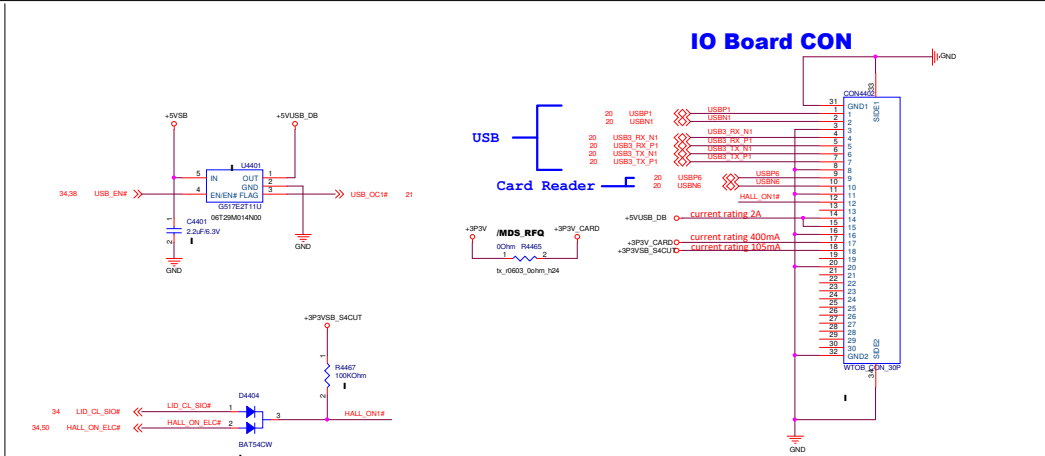












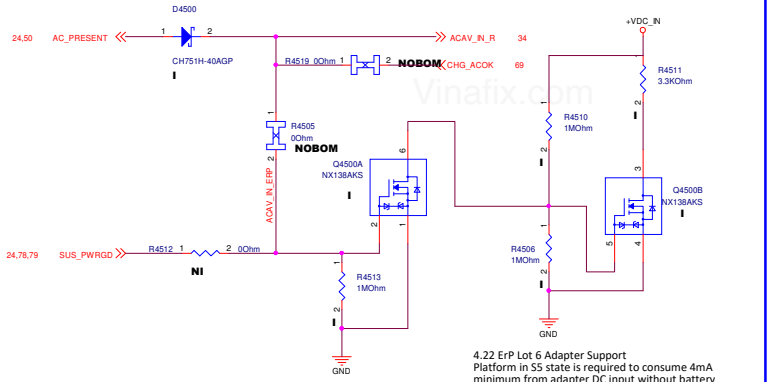
PEGATRON Title : Other CONN

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
Custom	Vulcan	X00

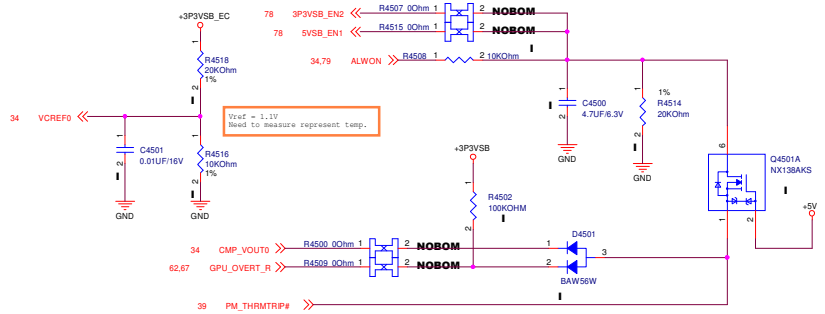
Date: Wednesday, November 28, 2018 Sheet 44 of 94

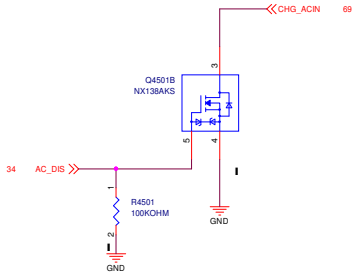
ACAV_IN Circuit



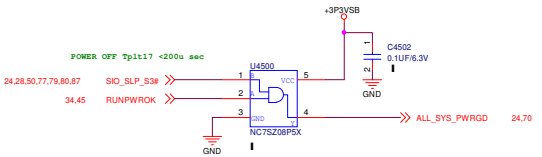
4.22 ErP Lot 6 Adapter Support
Platform in S5 state is required to consume 4mA minimum from adapter DC input without battery attached at the moment of plugging in system.

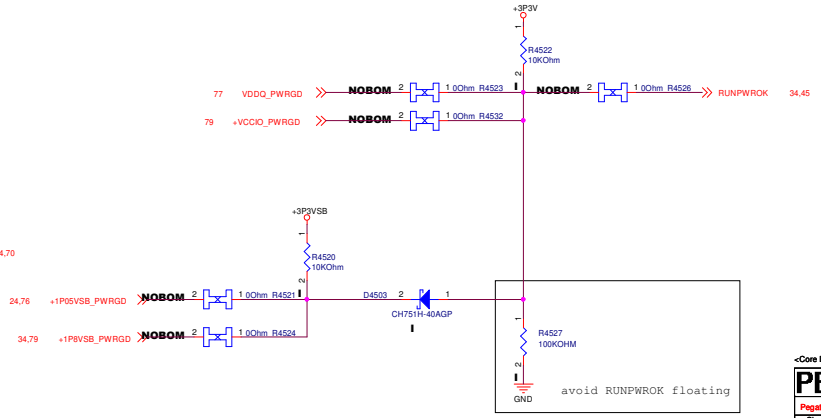
Thermal CMP Circuit





POWER GOOD DETECTER





<Core Design>

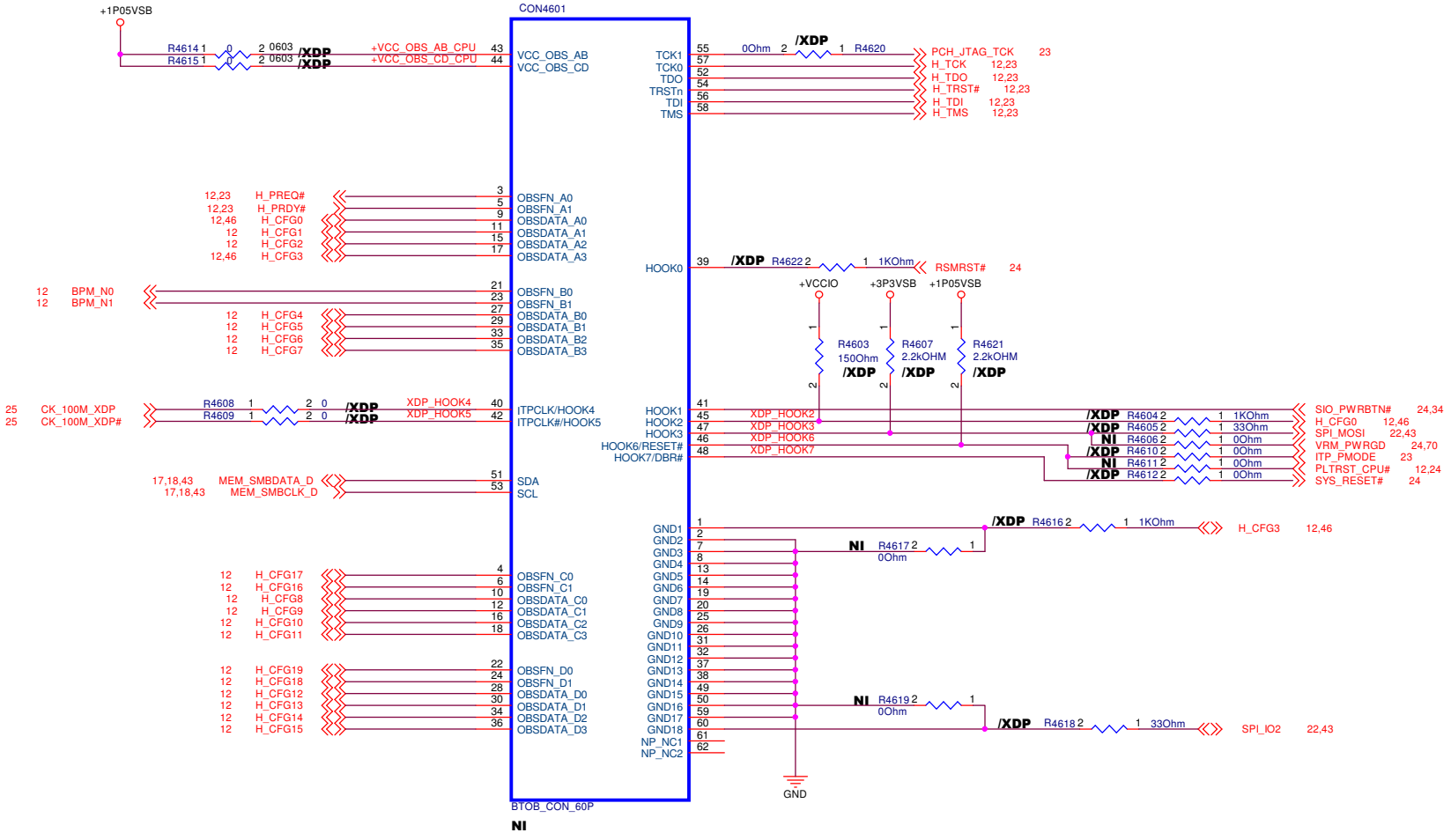
PEGATRON Title : ACAV_IN

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 45 of 94

INTEL XDP DEBUG CONN



PEGATRON	Title : XDP	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 46 of 94	

NOBOM

PCB4700

PCB

PCB_BOARD

CCL = Y

H4730 CT217B142D126 GND

H4729 CT217B142D126 GND

I

Fan Nut

H4708 1 C276D157 NOBOM

H4710 1 C276D157 NOBOM

H4712 1 C276D157 NOBOM

H4719 1 C276D157 NOBOM

NOBOM

For CPU

H4723 1 NOBOM C236D157

H4716 1 NOBOM C236D157

H4700 1 NOBOM C236D157

For GPU

GND

H4748 1 C315D157 NOBOM

H4747 1 C315D157 NOBOM

H4746 1 C315D157 NOBOM B

H4745 1 C315D157 NOBOM

H4744 1 C315D236 NOBOM N

H4743 1 C315D217 NOBOM G

H4742 1 RT374X276B276D157 NOBOM E

H4750 1 O122x83DO122x83N NOBOM J

H4751 1 C118D118N NOBOM K

H4753 1 C315D157 NOBOM

H4754 1 C315D157 NOBOM M

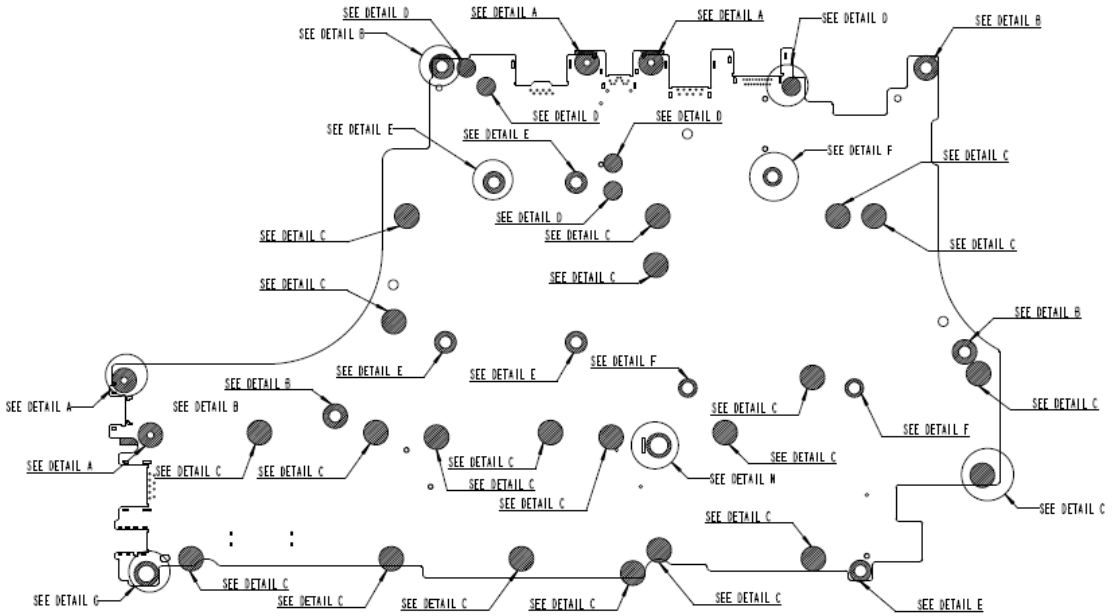
H4755 1 CT315BR315X311D91 NOBOM O

H4756 1 RT339X394RB528D91 NOBOM P

H4757 1 O39x197DO39x197N NOBOM Q

GND

TOP VIEW



PEGATRON Title : PCB & Label & Screw

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 47 of 94

Supply max 2.5A

Panel power

+3P3VSB → NOBOM R4852 0Ohm (W=100mils) → +3P3VSB_PANEL_IN

change for power drop test - X01/0828

+3P3VSB_PANEL_IN → C4834 2.2uF/6.3V, U4800 G5250A1T12U (IN, OUT, GND, DSG, EN), R4859 33Ohm → +3P3V_PANEL_O

+3P3V_PANEL_O → R4835 0Ohm NOBOM (W=100mils) → +3P3V_PANEL → C4833 4.7UF/6.3V

+AC_BAT_SYS → W=60mils → L4801 120Ohm/100Mhz, C4808 0.1UF/25V

NOBOM R4857 0Ohm → F4800 4A/32V → +VDD_BL_CONN

C4806 2.2UF/25V X5R/+/-10%, C4807 0.1UF/25V, C4809 68PF/50V, C4810 2200PF/50V

EMC預留 - X02 10/24

34 LCD_VCC_TEST_EN, 21 ENVDD_PCH → R4853 0Ohm /NON_GSYNC → D4801 BAT54C → R4836 100KOHM

62 LCD_VCC_EN_GPU → D4807 SDM20U30-7 /GSYNC → GND

21 L_BKLT_EN_EC, 62 LCD_BLEN_GPU → R4854 0Ohm /NON_GSYNC → D4808 BAT54C → BKLT_IN_EC_D 34; R4847 100KOHM → GND

NON G-SYNC ; CPU

8 EDP_TXN0 → R4800 0Ohm /NON_GSYNC

8 EDP_TXP0 → R4801 0Ohm /NON_GSYNC

8 EDP_TXN1 → R4802 0Ohm /NON_GSYNC

8 EDP_TXP1 → R4803 0Ohm /NON_GSYNC

8 EDP_TXN2 → R4804 0Ohm /NON_GSYNC

8 EDP_TXP2 → R4805 0Ohm /NON_GSYNC

8 EDP_TXN3 → R4806 0Ohm /NON_GSYNC

8 EDP_TXP3 → R4807 0Ohm /NON_GSYNC

8 EDP_AUXN → R4808 0Ohm /NON_GSYNC

8 EDP_AUXP → R4809 0Ohm /NON_GSYNC

21 EDP_HPD → R4810 0Ohm /NON_GSYNC

G-SYNC ; GPU

61 IFPD_EDP_AUXN → R4811 0Ohm /GSYNC

61 IFPD_EDP_AUXP → R4812 0Ohm /GSYNC

62 IFPD_HPD → R4813 0Ohm /GSYNC

61 IFPD_EDP_TXN0 → R4814 0Ohm /GSYNC

61 IFPD_EDP_TXP0 → R4815 0Ohm /GSYNC

61 IFPD_EDP_TXN1 → R4816 0Ohm /GSYNC

61 IFPD_EDP_TXP1 → R4817 0Ohm /GSYNC

61 IFPD_EDP_TXN2 → R4818 0Ohm /GSYNC

61 IFPD_EDP_TXP2 → R4819 0Ohm /GSYNC

61 IFPD_EDP_TXN3 → R4820 0Ohm /GSYNC

61 IFPD_EDP_TXP3 → R4821 0Ohm /GSYNC

EDP_MUX_TXN0, EDP_MUX_TXP0, EDP_MUX_TXN1, EDP_MUX_TXP1, EDP_MUX_AUXN, EDP_MUX_AUXP, EDP_MUX_TXN2, EDP_MUX_TXP2, EDP_MUX_TXN3, EDP_MUX_TXP3

+3P3V → F4801 0.5A/32V → +3P3V_MIC → C4837 0.1UF/6.3V

Follow Vendor comment - X00/0516

+3P3V_CAM → R4851 0Ohm NOBOM → C4805 0.1UF/6.3V

eDP CONNECTOR

FPC_CON_40P

22 LCD_DBC

USBP5_RD_R, USBN5_RD_R

40 DMIC_CLK1, 40 DMIC_DATA1

EDP_MUX_TXP0 → C4813 0.1UF/6.3V → EDP_TXP0_C; EDP_MUX_TXN0 → C4815 → EDP_TXN0_C

EDP_MUX_TXP1 → C4817 → EDP_TXP1_C; EDP_MUX_TXN1 → C4819 → EDP_TXN1_C

EDP_MUX_TXP2 → C4821 → EDP_TXP2_C; EDP_MUX_TXN2 → C4823 → EDP_TXN2_C

EDP_MUX_TXP3 → C4824 → EDP_TXP3_C; EDP_MUX_TXN3 → C4826 → EDP_TXN3_C

EDP_MUX_AUXP → C4832 → EDP_AUXP_C; EDP_MUX_AUXN → C4830 → EDP_AUXN_C

EDP_HPD_CON → R4840 0Ohm NOBOM

22 CAM_CBL_DET#

SIDE1 41, SIDE2 42, CON4800

20 USBP5 → 0OHM RN4800B → USBP5_RD_R

20 USBN5 → 0OHM RN4800A → USBN5_RD_R

NI L4800 90ohm 0910900021100

DMIC_CLK1, DMIC_DATA1 → C4835 12PF/50V NI, C4836 12PF/50V NI → D4804 AZ5125-01J, D4805 AZ5125-01J → GND

+3P3V_PANEL → C4803 0.1UF/6.3V; W=60mils → NI C4839 10PF/50V

Reserve for Panel Overdrive - X00/0717

34 PANEL_OVERDRI, 22 CAM_15B_DET# → R4856 0Ohm NI; CAM_15B_DET#

34 LCD_TST → R4828 0Ohm NOBOM; BIA_PWM_PCH_R

34 PANEL_BKEN_EC → R4858 0Ohm → D4809 SDM20U30-7

RF預留 - X02 10/24

21 BIA_PWM_PCH → D4802 SDM20U30-7 /NON_GSYNC

LCD_VCC_TEST_EN → D4803 SDM20U30-7

62 BL_PWM_GPU → D4806 SDM20U30-7 /GSYNC

+VDD_BL_CONN → R4834 100KOHM, R4839 100KOHM; NI C4838 10PF/50V

RF預留 - X02 10/24

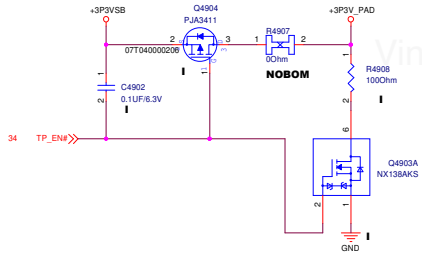
<Core Design>

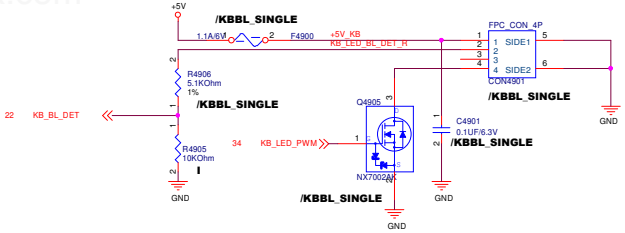
PEGATRON Title : eDP CON.

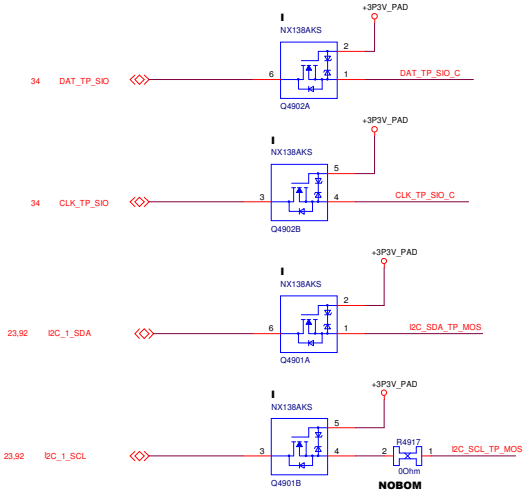
Pegatron Corp. Engineer: Travis_Hsieh

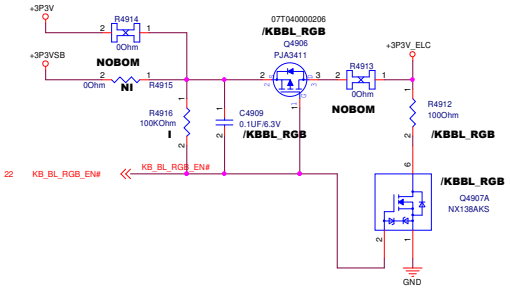
Size A2 | Project Name Vulcan | Rev X00

Date: Wednesday, November 28, 2018 | Sheet 48 of 94

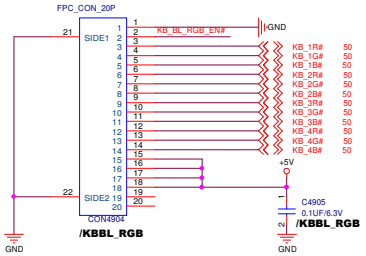




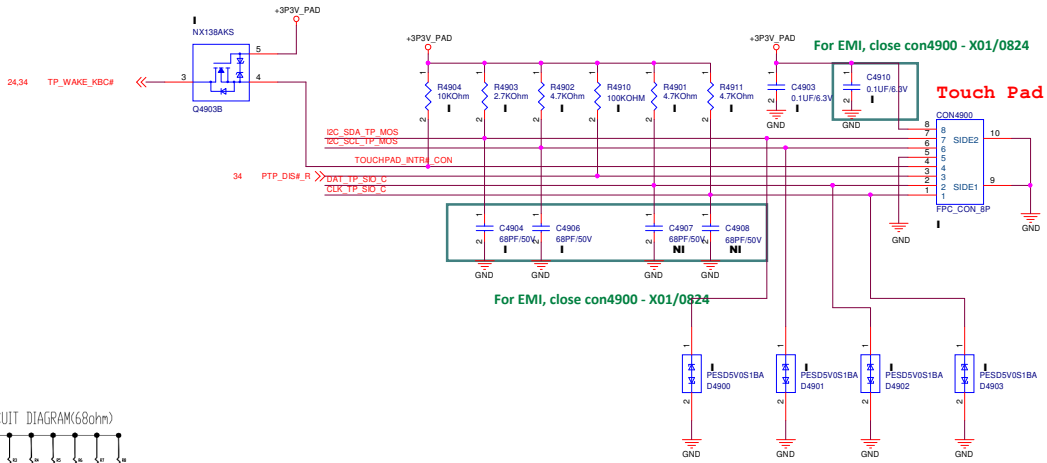


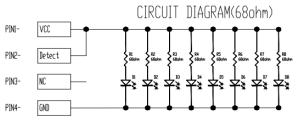


KB_BL_ID		
Config	KB_BL_RGB_EN#	KB_BL_DET
KB_BL_RGB	0	0
KB_BL_SINGLE	1	1
KB_NON_BL	1	0
N/A	1	1



Keyboard backlight





VCC : +5V
LED Vf : 2.8 ~ 3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.8V)
Power consumption	158.82 mA	284.71 mA

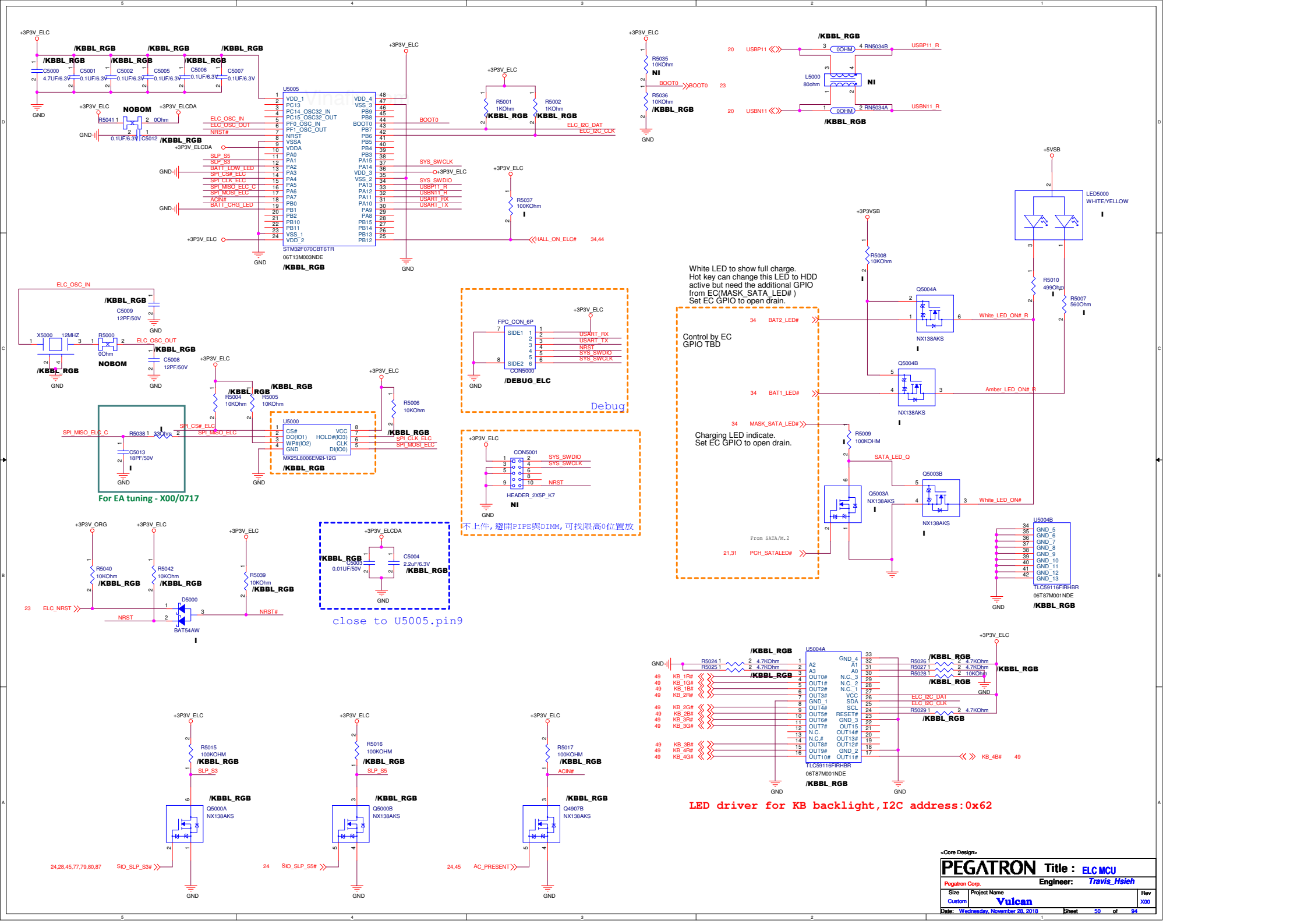
<Core Design>

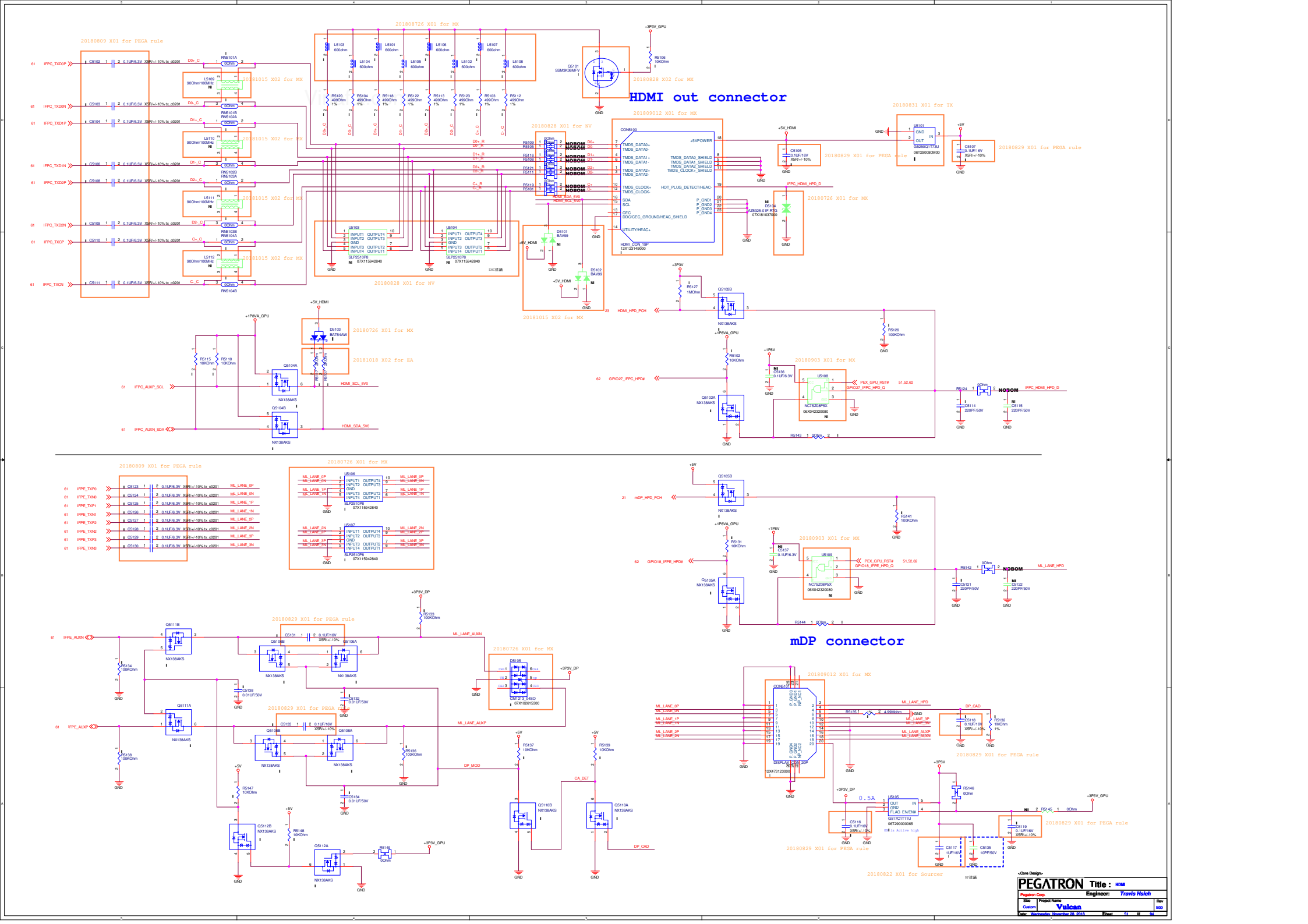
PEGATRON Title : Touch & Keyboard BL

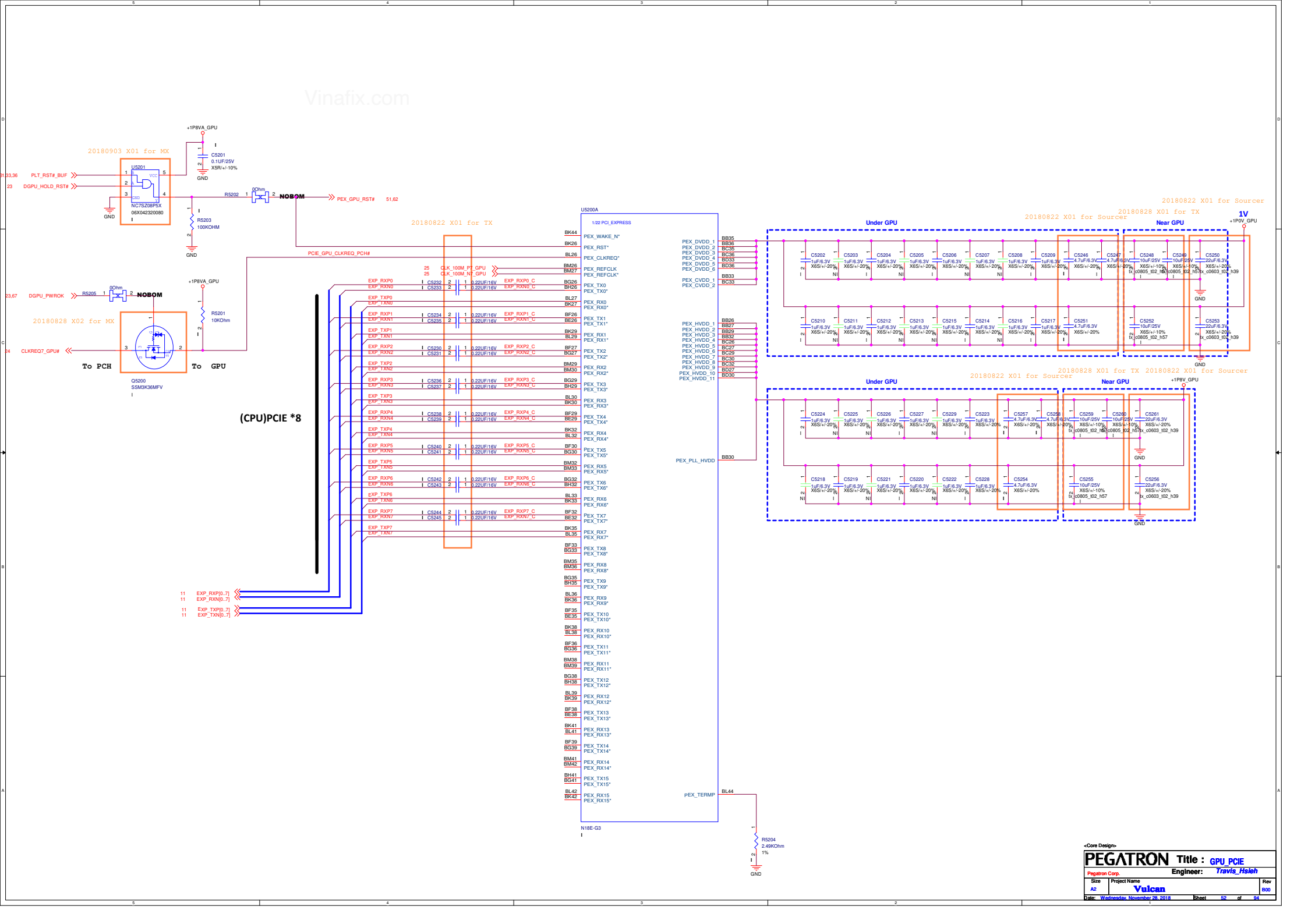
Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	X00

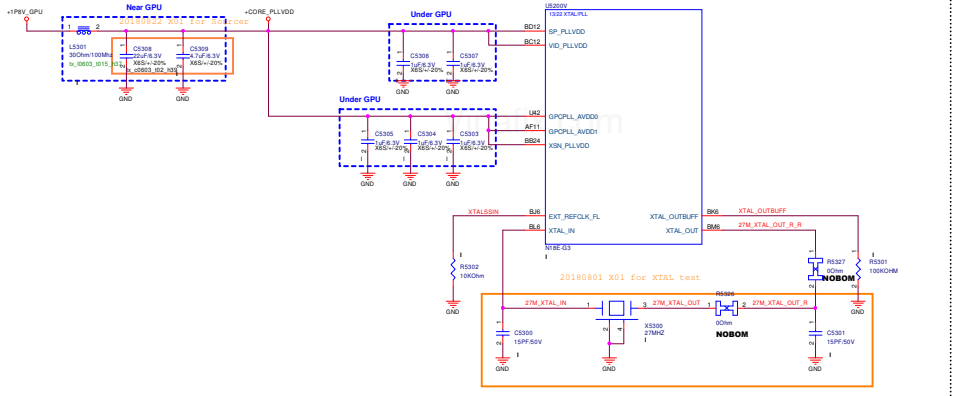
Date: Wednesday, November 28, 2018 Sheet 49 of 94


+3P3V_ELC
/KBBL_RGB
C5000 4.7UF/6.3V
C5001 0.1UF/6.3V
C5002 0.1UF/6.3V
C5005 0.1UF/6.3V
C5006 0.1UF/6.3V
C5007 0.1UF/6.3V
GND
+3P3V_ELCDA
NOBOM
R5041 0Ohm
C5012 0.1UF/6.3V
U5005
STM32F070CBT6TR
06T13M003NDE
ELC_OSC_IN
ELC_OSC_OUT
NRST#
SLP_S5
SLP_S3
BAT1_LOW_LED
SPI_CS#_ELC
SPI_CLK_ELC
SPI_MISO_ELC_C
SPI_MOSI_ELC
ACIN#
BAT1_CHG_LED
BOOT0
SYS_SWCLK
SYS_SWDIO
USBPT1_R
USBNT1_R
USART_RX
USART_TX
HALL_ON_ELC#
34,44
R5001 1KOhm
R5002 1KOhm
ELC_I2C_DAT
ELC_I2C_CLK
R5037 100KOhm
R5035 10KOhm
NI
R5036 10KOhm
USBP11
USBN11
0OHM
RN5034B
RN5034A
L5000 80ohm
USBP11_R
USBN11_R
LED5000 WHITE/YELLOW
+5VSB
+3P3VSB
R5008 10KOhm
R5010 499Ohm
R5007 560Ohm
Q5004A
Q5004B
NX138AKS
White_LED_ON#_R
Amber_LED_ON#_R
White_LED_ON#
White LED to show full charge.
Hot key can change this LED to HDD active but need the additional GPIO from EC(MASK_SATA_LED#)
Set EC GPIO to open drain.
Control by EC GPIO TBD
Charging LED indicate.
Set EC GPIO to open drain.
BAT2_LED#
BAT1_LED#
MASK_SATA_LED#
SATA_LED_Q
PCH_SATALED#
From SATA/M.2
R5009 100KOHM
Q5003A
Q5003B
U5004B
TLC59116FIRHBR
06T87M001NDE
ELC_OSC_IN
X5000 12MHZ
C5009 12PF/50V
R5000 0Ohm
C5008 12PF/50V
ELC_OSC_OUT
R5004 10KOhm
R5005 10KOhm
R5006 10KOhm
U5000
MX25L8006EM2I-12G
SPI_MISO_ELC_C
R5038 33Ohm
C5013 18PF/50V
SPI_CS#_ELC
SPI_MISO_ELC
SPI_CLK_ELC
SPI_MOSI_ELC
For EA tuning - X00/0717
FPC_CON_6P
CON5000
USART_RX
USART_TX
NRST
SYS_SWDIO
SYS_SWCLK
/DEBUG_ELC
Debug
CON5001
HEADER_2X5P_K7
NI
不上件，避開PIPE與DIMM，可找限高0位置放
+3P3V_ORG
R5040 10KOhm
R5042 10KOhm
R5039 10KOhm
D5000
BAT54AW
ELC_NRST
NRST
NRST#
+3P3V_ELCDA
C5003 0.01UF/50V
C5004 2.2uF/6.3V
close to U5005.pin9
U5004A
TLC59116FIRHBR
06T87M001NDE
R5024 4.7KOhm
R5025 4.7KOhm
R5026 4.7KOhm
R5027 4.7KOhm
R5028 10KOhm
R5029 4.7KOhm
KB_1R#
KB_1G#
KB_1B#
KB_2R#
KB_2G#
KB_2B#
KB_3R#
KB_3G#
KB_3B#
KB_4R#
KB_4G#
KB_4B#
LED driver for KB backlight,I2C address:0x62
R5015 100KOHM
R5016 100KOHM
R5017 100KOHM
SLP_S3
SLP_S5
ACIN#
Q5000A NX138AKS
Q5000B NX138AKS
Q4907B NX138AKS
24,28,45,77,79,80,87
SIO_SLP_S3#
24
SIO_SLP_S5#
24,45
AC_PRESENT
<Core Design>
PEGATRON
Title : ELC MCU
Engineer: Travis_Hsieh
Pegatron Corp.
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 50 of 94


HDMI out connector
mDP connector
20180809 X01 for PEGA rule
20180726 X01 for MX
20180828 X01 for NV
20180828 X02 for MX
20181015 X02 for MX
20180829 X01 for PEGA rule
20180831 X01 for TX
20180903 X01 for MX
20180822 X01 for Sourcer
20181018 X02 for EA
20180809012 X01 for MX
IFPC_TXD0P
IFPC_TXD0N
IFPC_TXD1P
IFPC_TXD1N
IFPC_TXD2P
IFPC_TXD2N
IFPC_TXCP
IFPC_TXCN
IFPC_AUXP_SCL
IFPC_AUXN_SDA
HDMI_SCL_5V0
HDMI_SDA_5V0
HDMI_HPD_PCH
IFPC_HDMI_HPD_D
GPIO27_IFPC_HPD#
PEX_GPU_RST#
GPIO27_IFPC_HPD_Q
IFPE_TXP0
IFPE_TXN0
IFPE_TXP1
IFPE_TXN1
IFPE_TXP2
IFPE_TXN2
IFPE_TXP3
IFPE_TXN3
IFPE_AUXN
IFPE_AUXP
nDP_HPD_PCH
GPIO18_IFPE_HPD#
PEX_GPU_RST#
GPIO18_IFPE_HPD_Q
ML_LANE_HPD
ML_LANE_AUXP
ML_LANE_AUXN
DP_MOD
CA_DET
DP_CAD
+5V_HDMI
+3P3V_GPU
+3P3V_DP
+1P8VA_GPU
+1P8V
+3P3V
+5V
GND
NOBOM
NI
Title : HDMI
Engineer: Travis Hsieh
Pegatron Corp.
Project Name: Vulcan
Size: Custom
Rev: B00
Date: Wednesday, November 28, 2018
Sheet 51 of 94



<Core Design>
PEGATRON Title : GPU_PCIE
Pegatron Corp. Engineer: Travis_Hsieh
Size A2 | Project Name Vulcan | Rev B00
Date: Wednesday, November 28, 2018 Sheet 52 of 94



Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

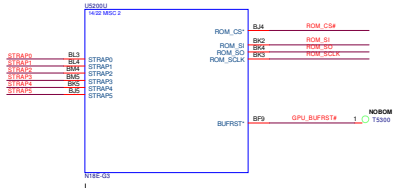
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

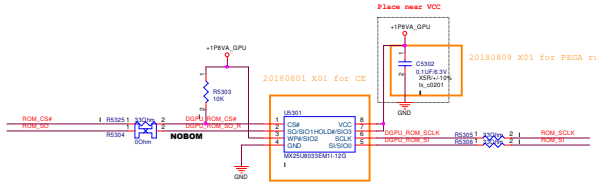
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Straps 需確認strap及ROM(Memory 還未確定)



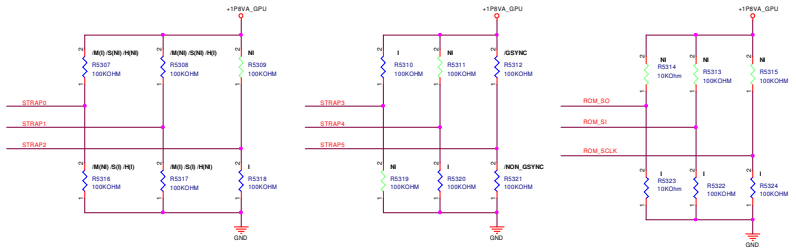


Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx2Chx16	1.35V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:

1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.

Need NV check

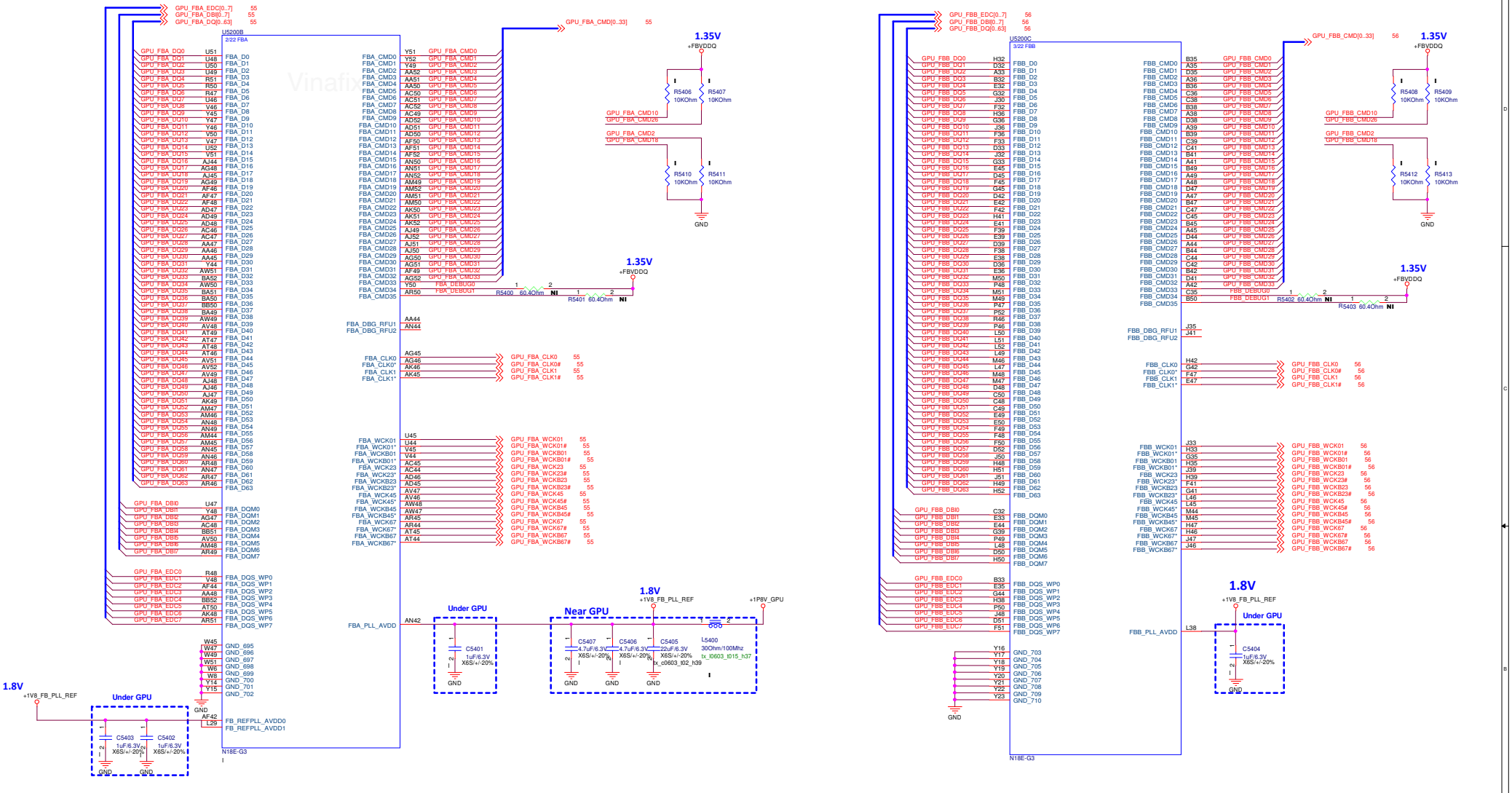


Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate
			Hynix	H56C8H24MJR-S2C	M-die	0x2	14 Gbps	N/A	Full	Production candidate

Notes:

1. For N18E-G2, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

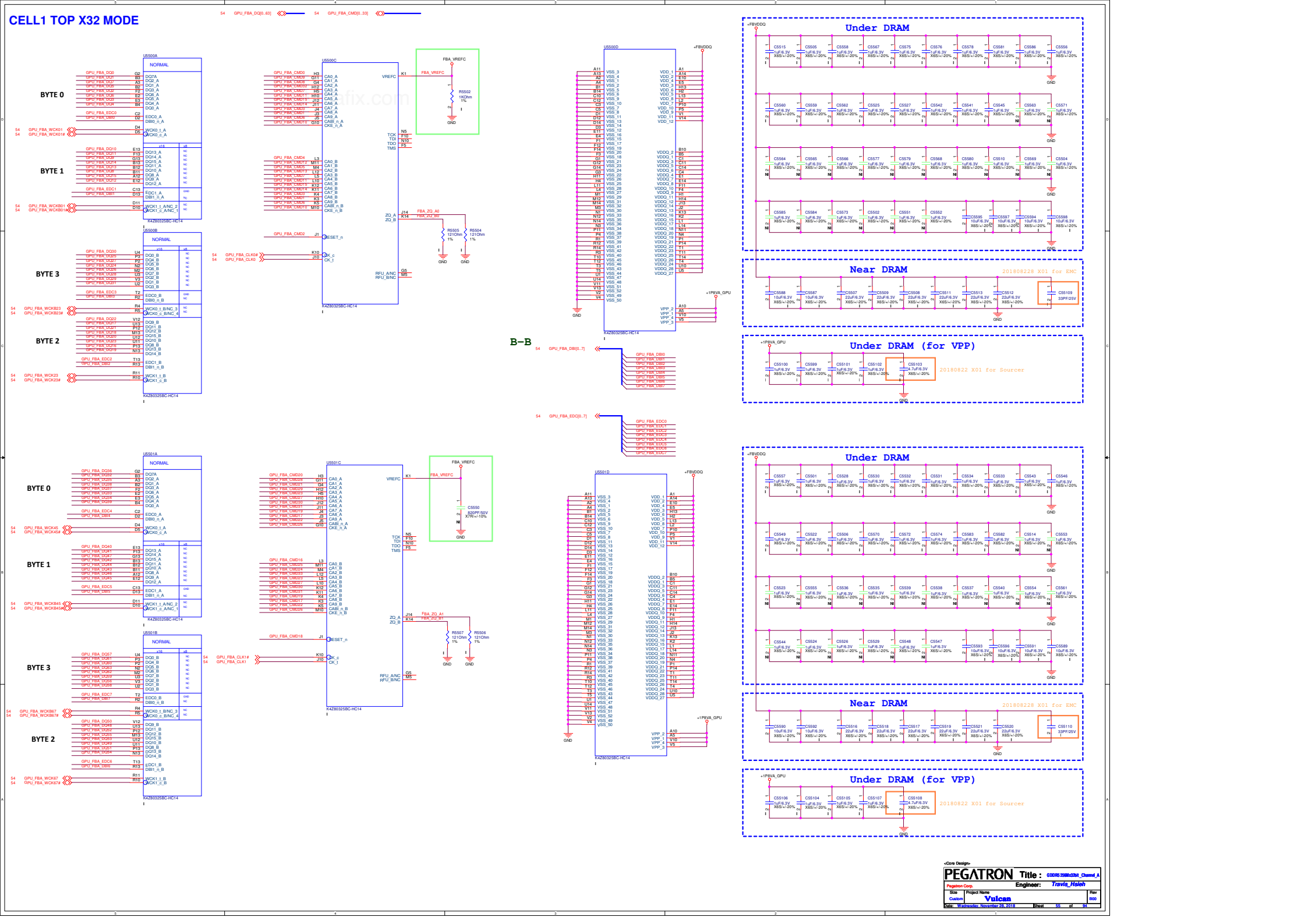
<Core Design>
PEGATRON Title : GPU-Xtal & Straps
Pegatron Corp. Engineer: Travis_Haleh
Size: Custom | Project Name: Vulcan | Rev: B00
Date: Wednesday, November 28, 2018 Sheet 53 of 94



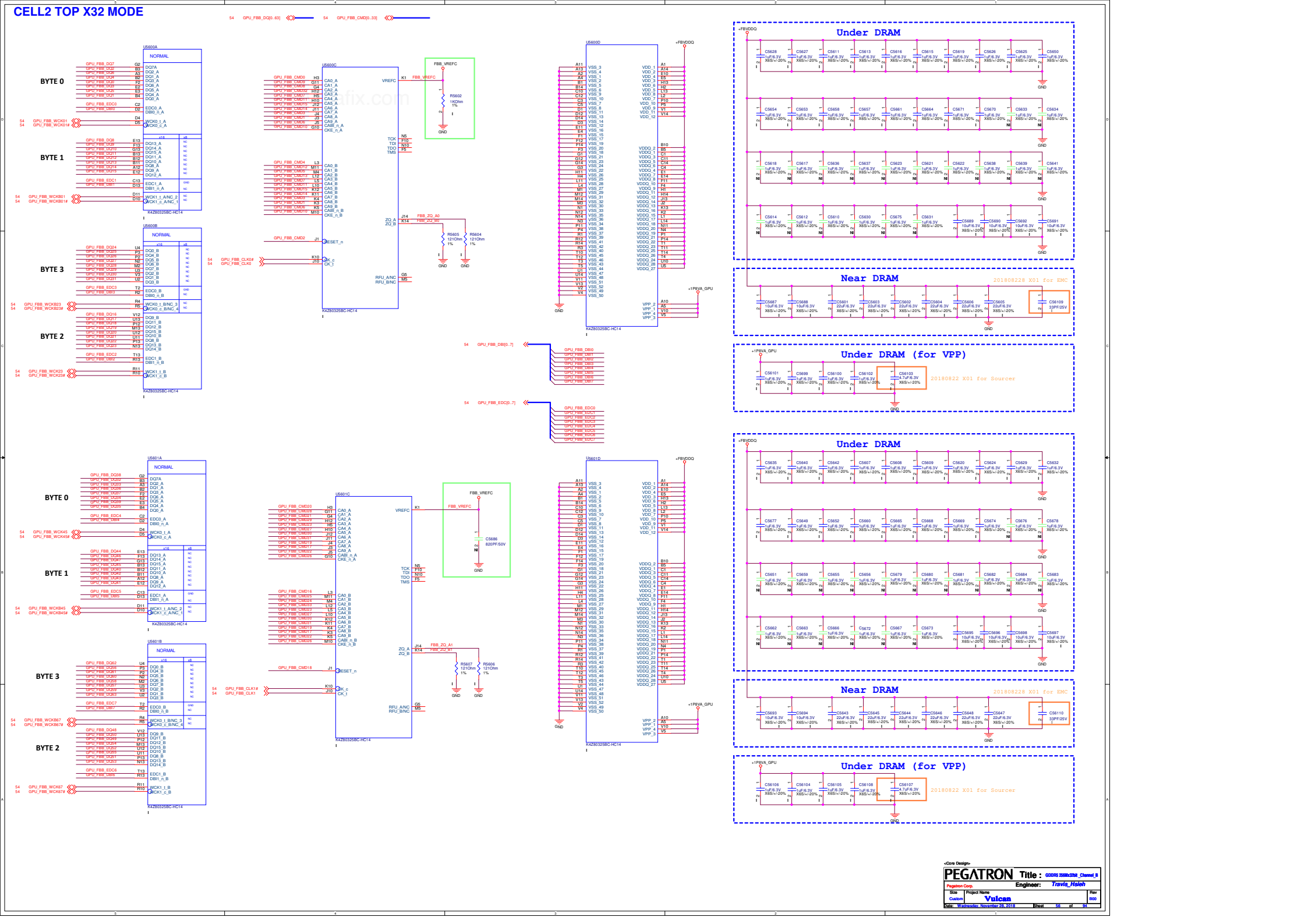
<core_design>

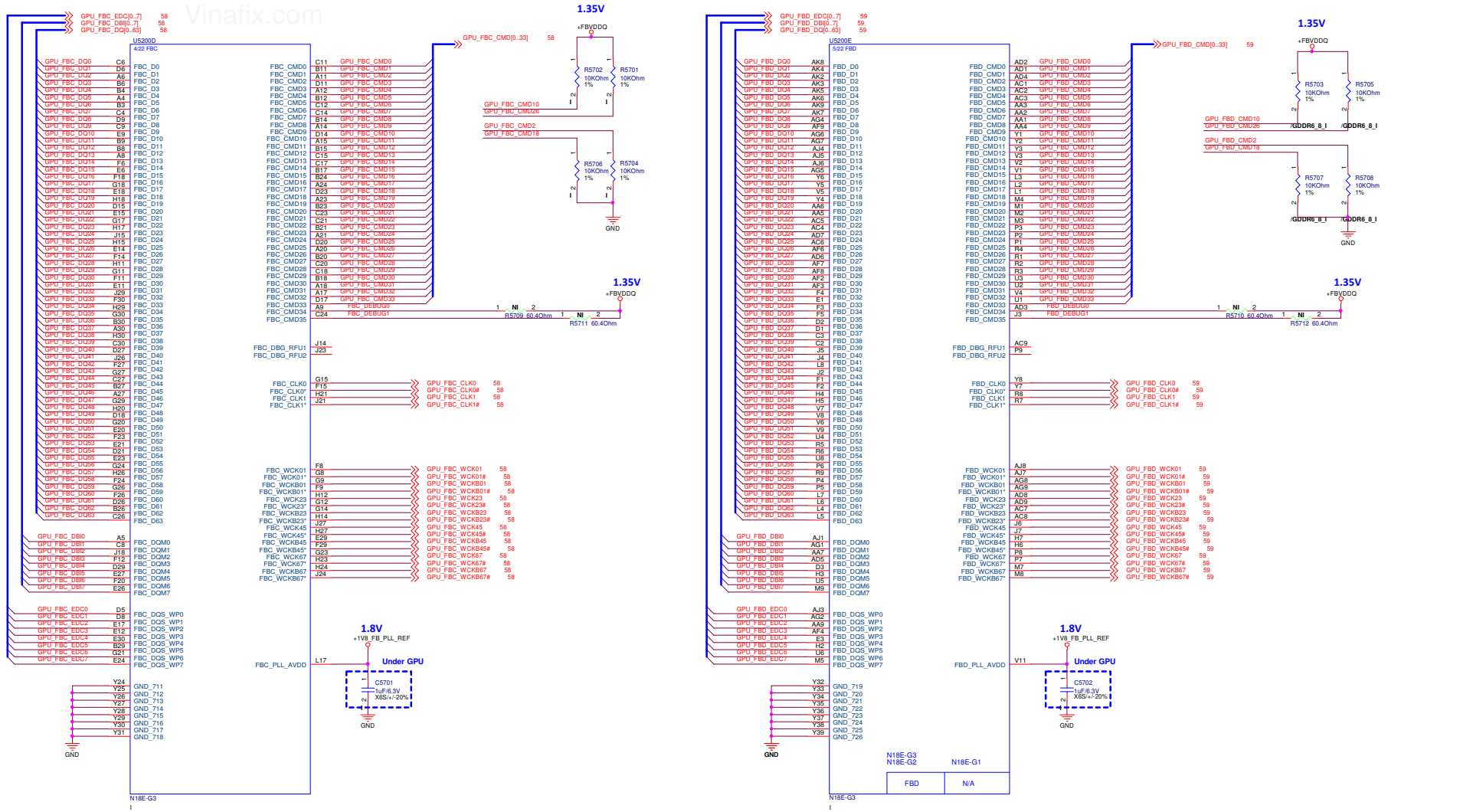
PEGATRON	Title : GPU-BUFFER PARTITION A/B		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: B00
Date: Wednesday, November 28, 2018	Sheet 54 of 94		
</core_design>

CELL1 TOP X32 MODE



CELL2 TOP X32 MODE





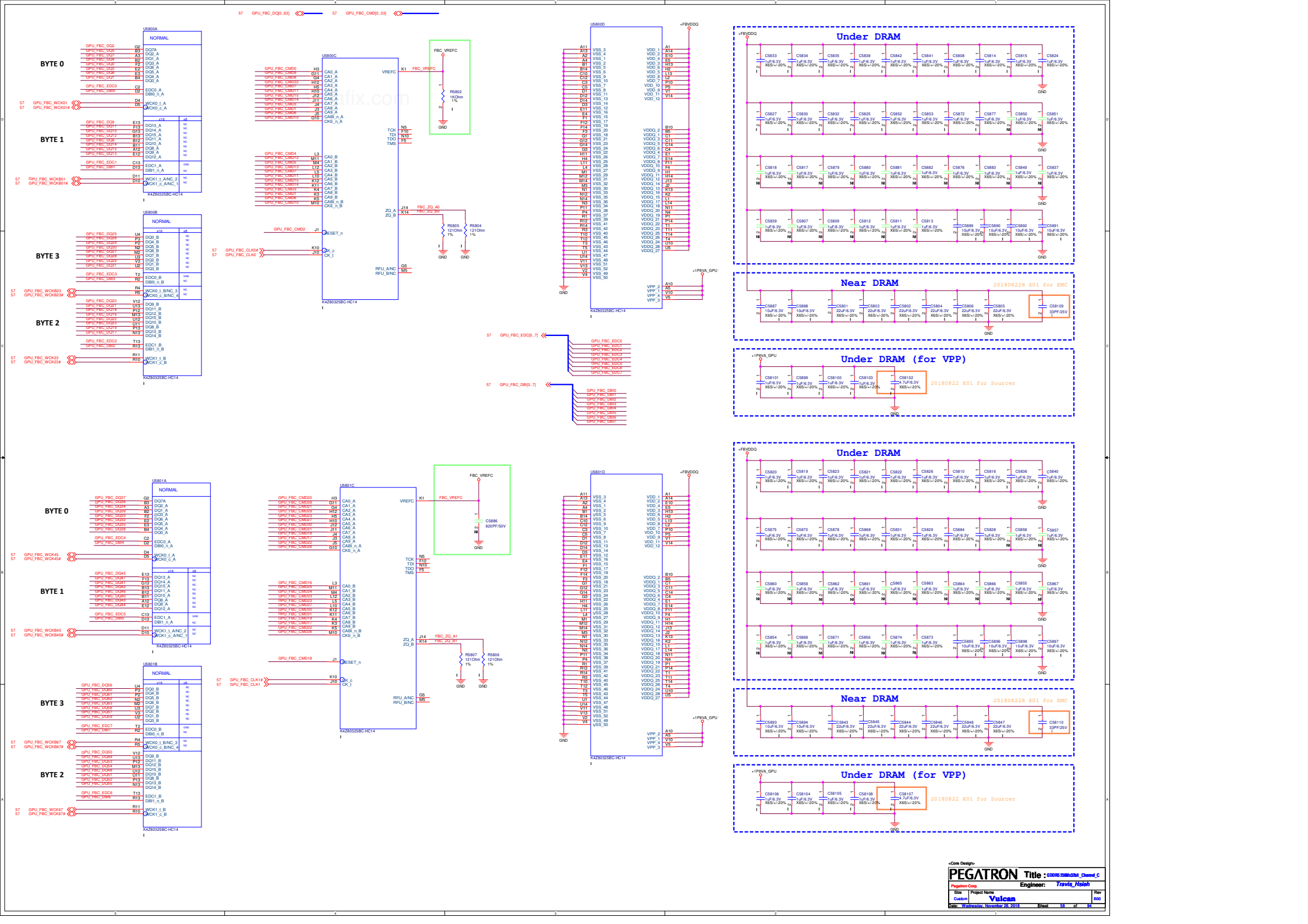
<Core Design>

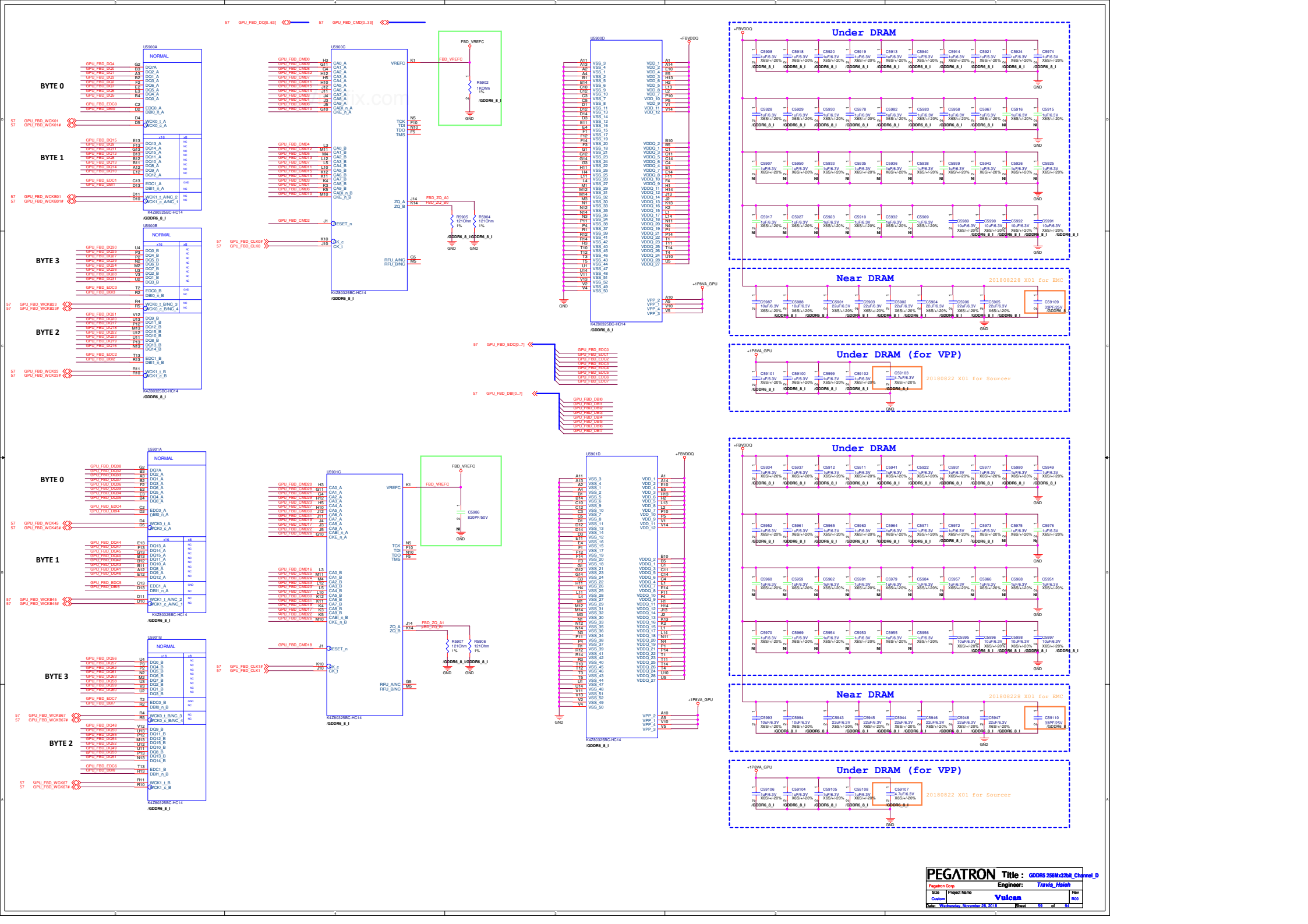
PEGATRON Title : GPU-BUFFER PARTITION C/D

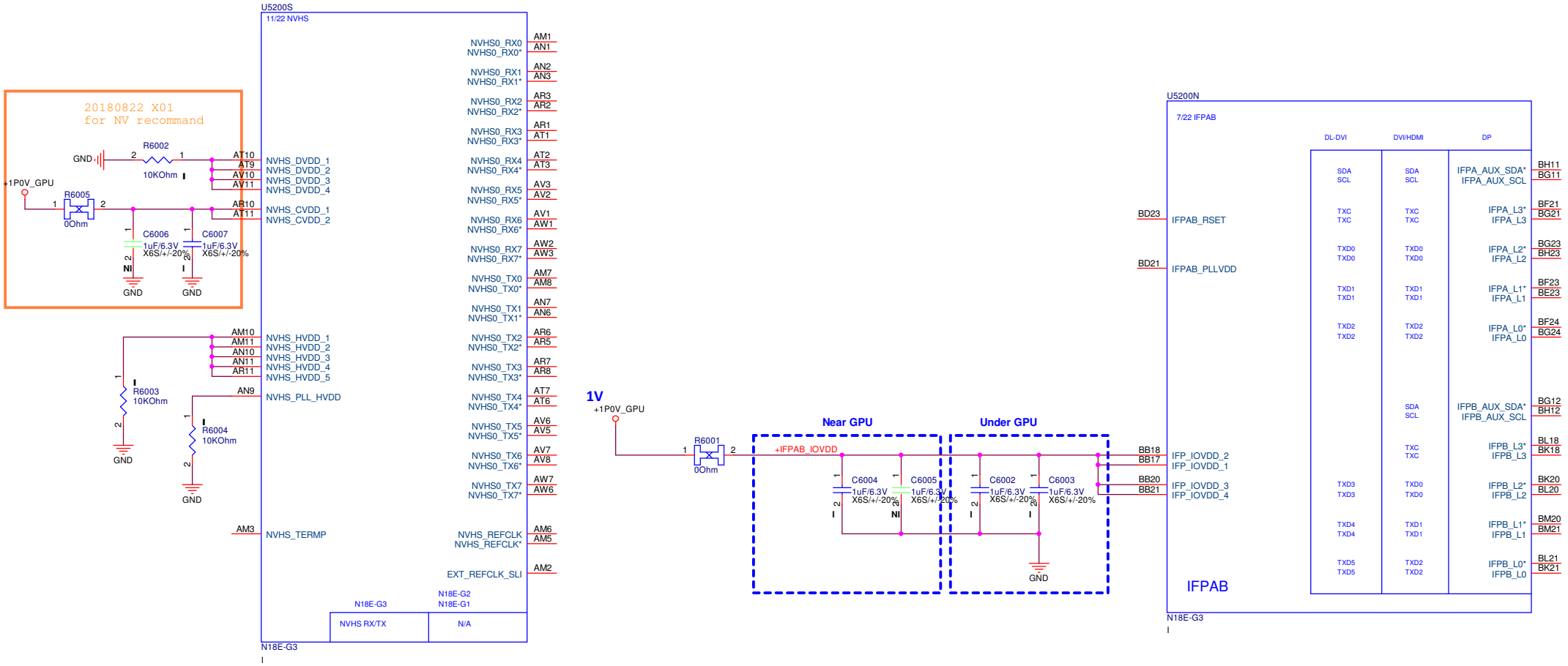
Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 57 of 94




BYTE 0
BYTE 1
BYTE 2
BYTE 3
U5900A
U5900B
U5900C
U5900D
U5901A
U5901B
U5901C
U5901D
NORMAL
X4Z80325BC-HC14
/GDDR8_8_I
FBD_VREFC
R5902
1KOhm
1%
R5905
121Ohm
1%
R5904
121Ohm
1%
R5907
121Ohm
1%
R5906
121Ohm
1%
C5986
820PF/50V
+FBVDDQ
+1P8VA_GPU
Under DRAM
Near DRAM
Under DRAM (for VPP)
20180822 X01 for Sourcer
201808228 X01 for EMC
PEGATRON
Title : GDDR5 256Mx32bit Channel_D
Pegatron Corp.
Engineer: Travis_Hsieh
Size: Custom
Project Name: Vulcan
Rev: B00
Date: Wednesday, November 28, 2018
Sheet 59 of 94



PEGATRON Title : GPU_MIO

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 60 of 94

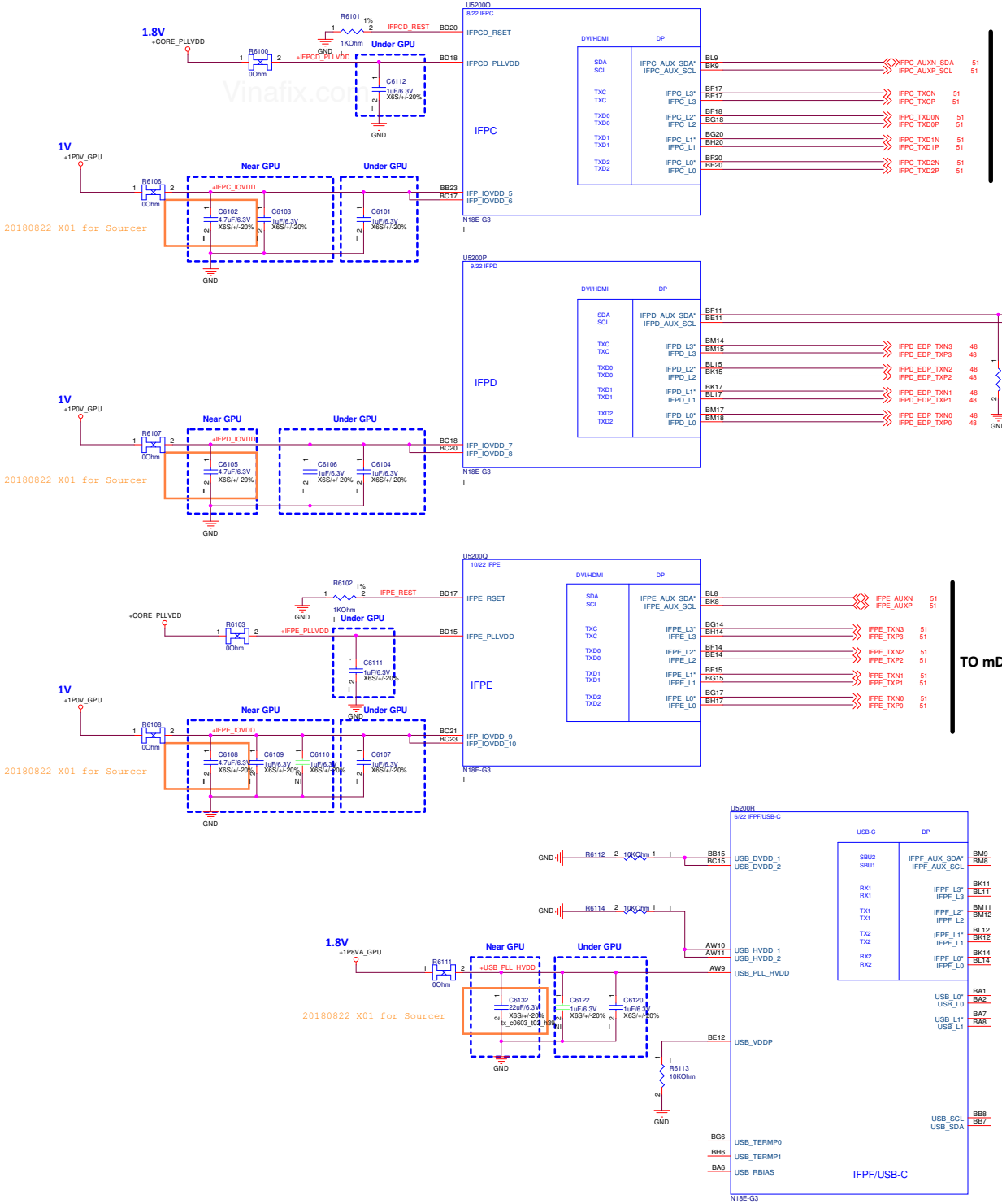


Table 9.6 HDMI Power Rails

Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 10%	~98 mA
IFPCD_PLLVDD	1.8 V ± 10%	~98 mA
IFPEF_PLLVDD	1.8 V ± 10%	~98 mA

Table 9.11 DP Power Rails

Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA
IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA

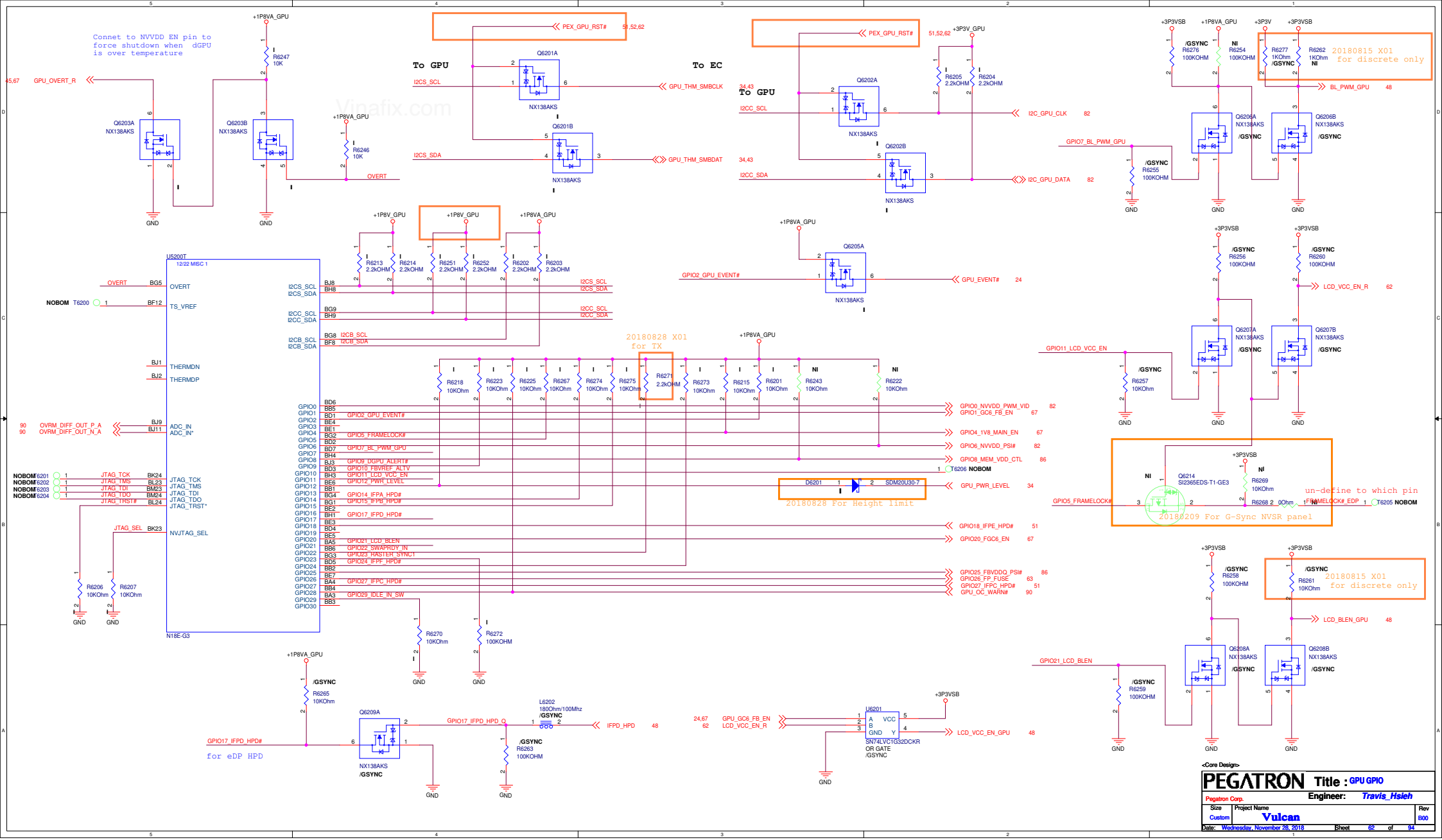
<Core Design>

PEGATRON Title : GPU mini DP/HDMI/MUX

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 61 of 94


Connet to NVVDD EN pin to force shutdown when dGPU is over temperature
GPU_OVERT_R
OVERT
To GPU
I2CS_SCL
I2CS_SDA
GPU_THM_SMBCLK
GPU_THM_SMBDAT
PEX_GPU_RST#
To EC
I2CC_SCL
I2CC_SDA
I2C_GPU_CLK
I2C_GPU_DATA
BL_PWM_GPU
GPIO7_BL_PWM_GPU
GPIO2_GPU_EVENT#
GPU_EVENT#
LCD_VCC_EN_R
GPIO11_LCD_VCC_EN
20180828 X01 for TX
20180815 X01 for discrete only
20180828 For Height limit
20180209 For G-Sync NVSR panel
un-define to which pin
for eDP HPD
U5200T
12/22 MISC 1
N18E-G3
NOBOM T6200
OVRM_DIFF_OUT_P_A
OVRM_DIFF_OUT_N_A
ADC_IN
ADC_IN*
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*
JTAG_SEL
NVJTAG_SEL
THERMDN
THERMDP
GPIO0_NVVDD_PWM_VID
GPIO1_GC6_FB_EN
GPIO4_1V8_MAIN_EN
GPIO6_NVVDD_PSI#
GPIO8_MEM_VDD_CTL
GPIO9_DGPU_ALERT#
GPIO10_FBVREF_ALTV
GPIO11_LCD_VCC_EN
GPIO12_PWR_LEVEL
GPIO14_IFPA_HPD#
GPIO15_IFPB_HPD#
GPIO17_IFPD_HPD#
GPIO18_IFPE_HPD#
GPIO20_FGC6_EN
GPIO21_LCD_BLEN
GPIO22_SWAPRDY_IN
GPIO23_HASH_SYNC1
GPIO24_IFPF_HPD#
GPIO25_FBVDDQ_PSI#
GPIO26_FP_FUSE
GPIO27_IFPC_HPD#
GPIO29_IDLE_IN_SW
GPU_OC_WARN#
GPU_PWR_LEVEL
T6206 NOBOM
T6205 NOBOM
FRAMELOCK#_EDP
IFPD_HPD
GPU_GC6_FB_EN
LCD_VCC_EN_R
LCD_VCC_EN_GPU
SN74LVC1G32DCKR
OR GATE
/GSYNC
NI
Vipafix.com
<Core Design>
PEGATRON
Title : GPU GPIO
Pegatron Corp.
Engineer: Travis_Hsieh
Size Custom
Project Name Vulcan
Rev B00
Date: Wednesday, November 28, 2018
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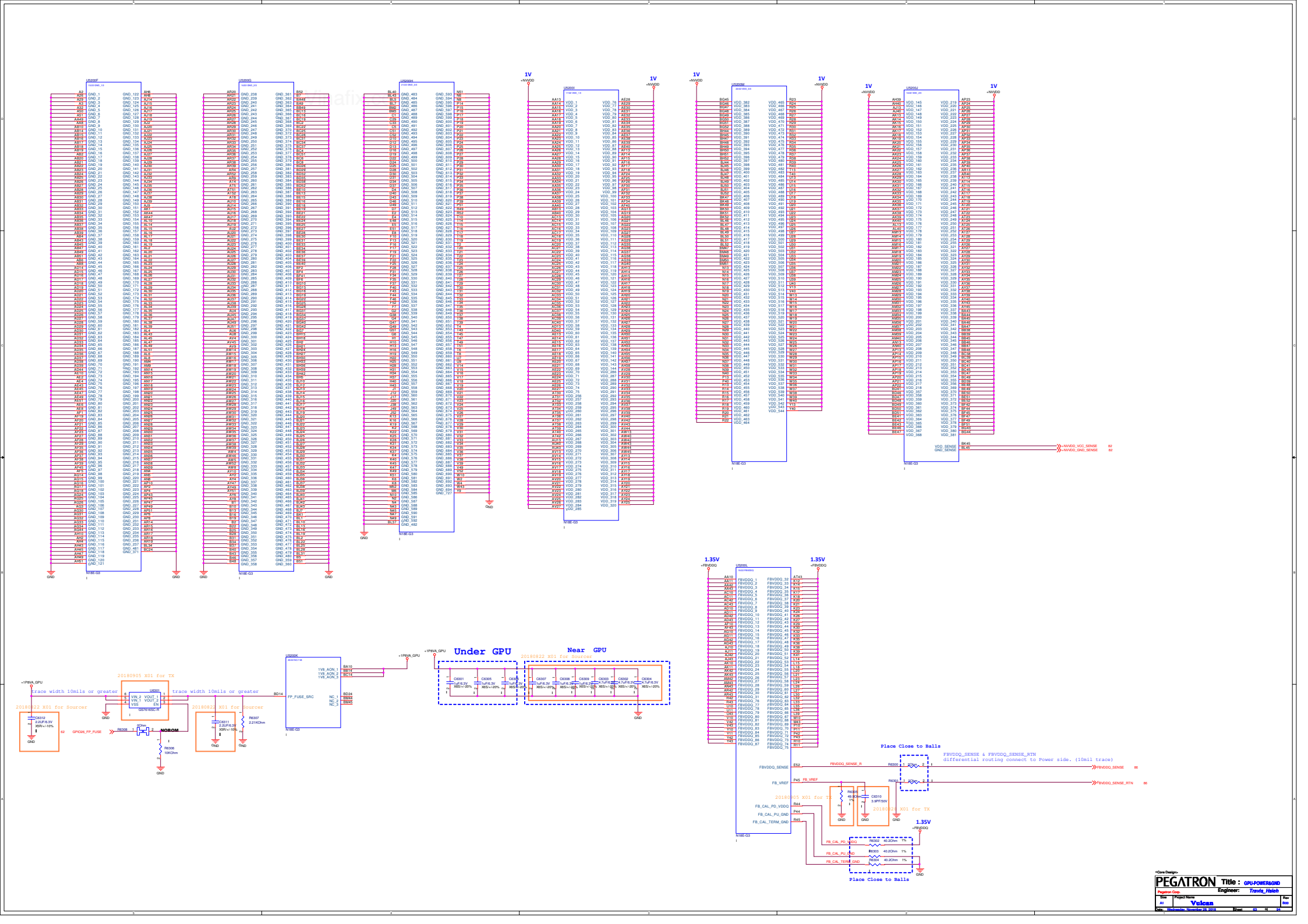
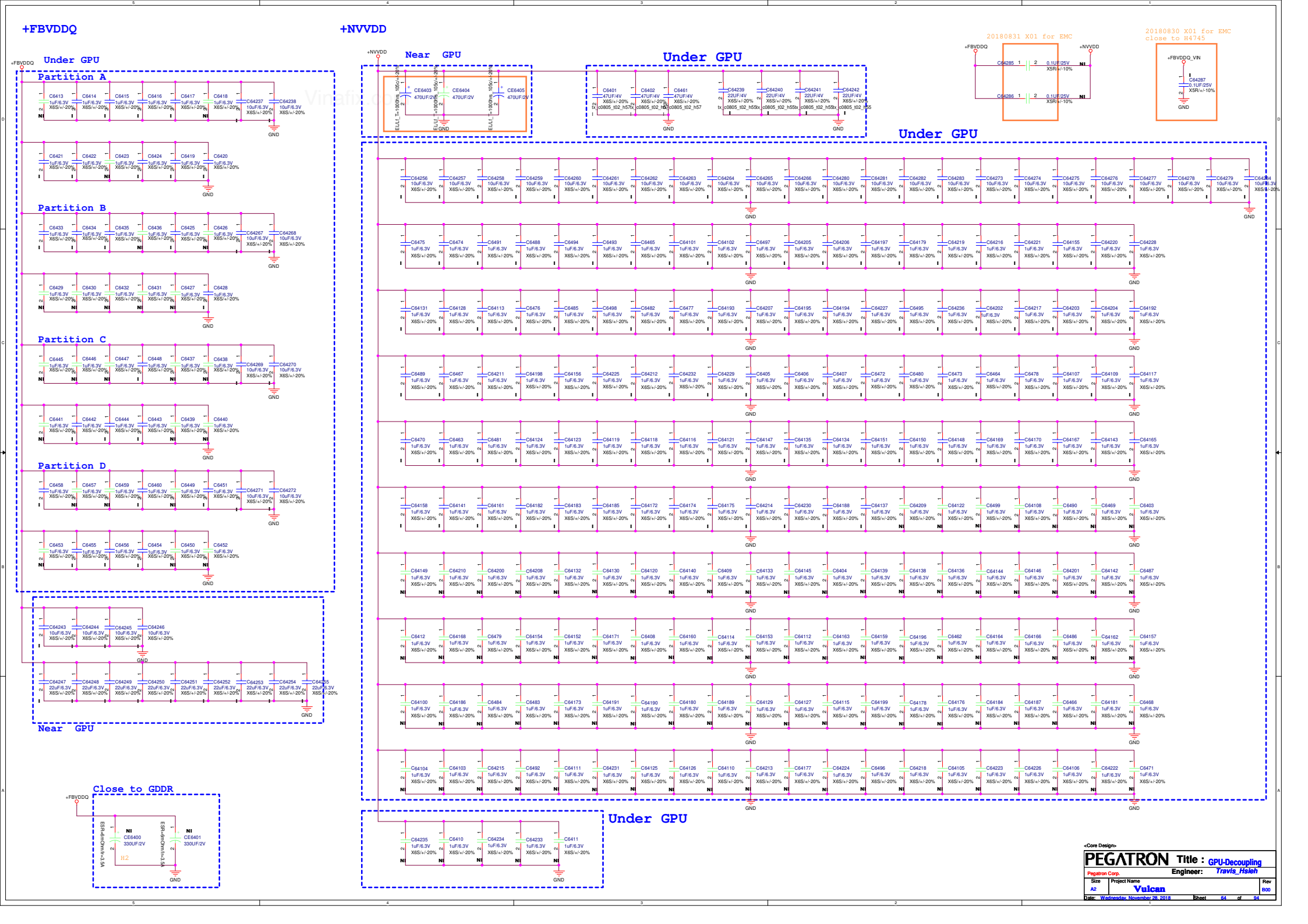

Under GPU
Near GPU
20180822 X01 for Sourcer
20180905 X01 for TX
trace width 10mils or greater
NOBOM
Place Close to Balls
FBVDDQ_SENSE & FBVDDQ_SENSE_RTN
differential routing connect to Power side. (10mil trace)
PEGATRON
Title : GPU-POWER&GND
Engineer: Travis_Haleh
Project Name: Vulcan
Wednesday, November 28, 2018


+FBVDDQ
Under GPU
Partition A
Partition B
Partition C
Partition D
Near GPU
Close to GDDR
+NVVDD
Near GPU
Under GPU
Under GPU
Under GPU
20180831 X01 for EMC
20180830 X01 for EMC close to H4745
+FBVDDQ_VIN
GND
<Core Design>
PEGATRON
Title : GPU-Decoupling
Pegatron Corp.
Engineer: Travis_Hsieh
Size A2
Project Name Vulcan
Rev B00
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PEGATRON Title : TYPE-C_PD

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
C	Vulcan	B00

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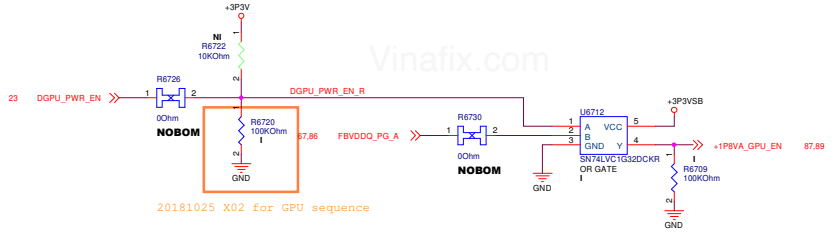
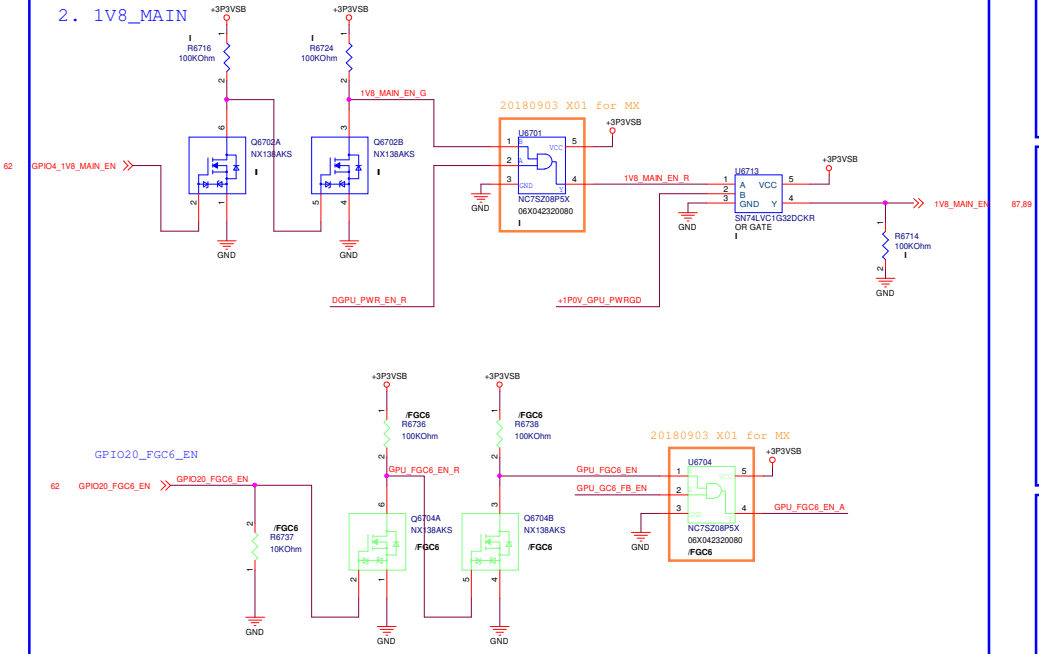
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : Type-C MUX	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: 800
Date: Wednesday, November 28, 2018	Sheet 68 of 94	

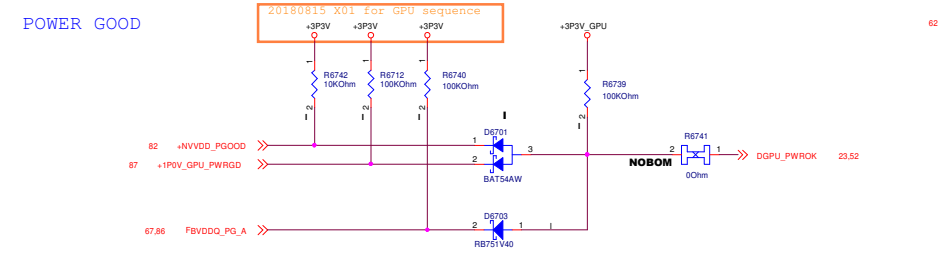
1.1V8_AON



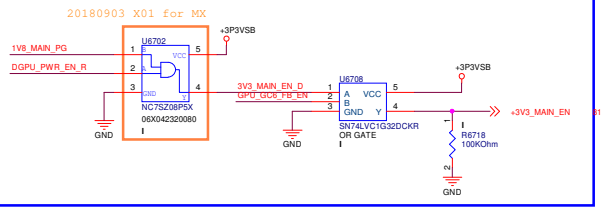
2. 1V8_MAIN



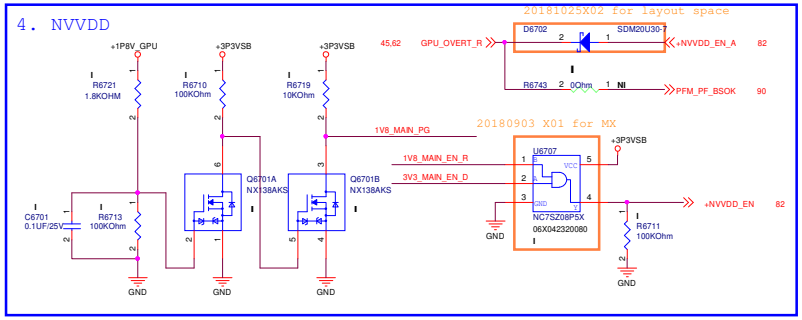
POWER GOOD



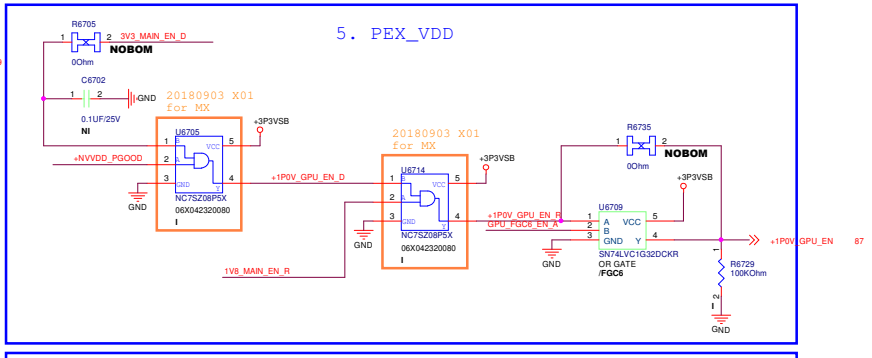
3. 3V3_MAIN



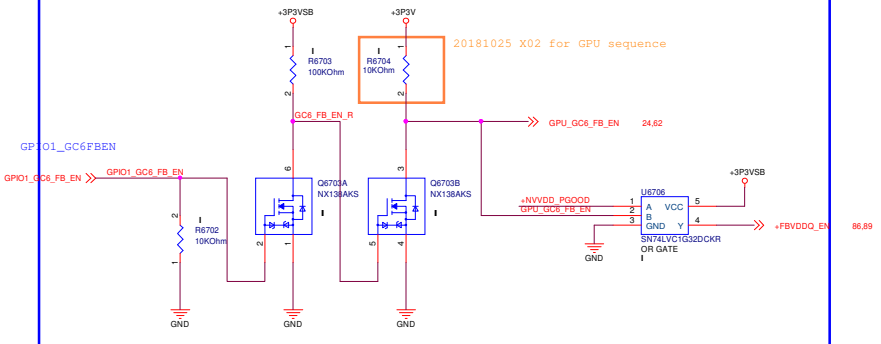
4. NVVDD



5. PEX_VDD



6. FBVDDQ



<Core Design>

PEGATRON Title : GPU_POWER Sequence

Pegatron Corp. Engineer: Travis_Hsieh

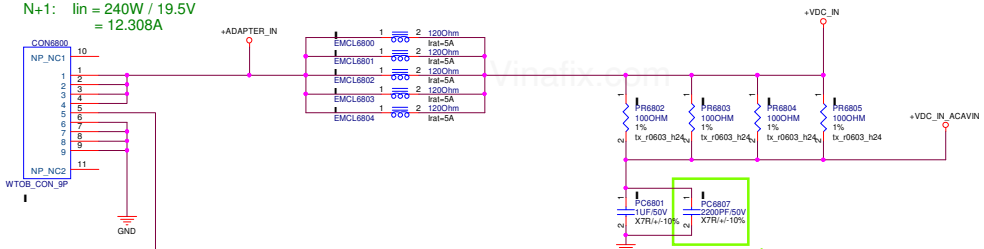
Size	Project Name	Rev
A2	Vulcan	800

Date: Wednesday, November 28, 2018 Sheet 67 of 94

DC-IN connector

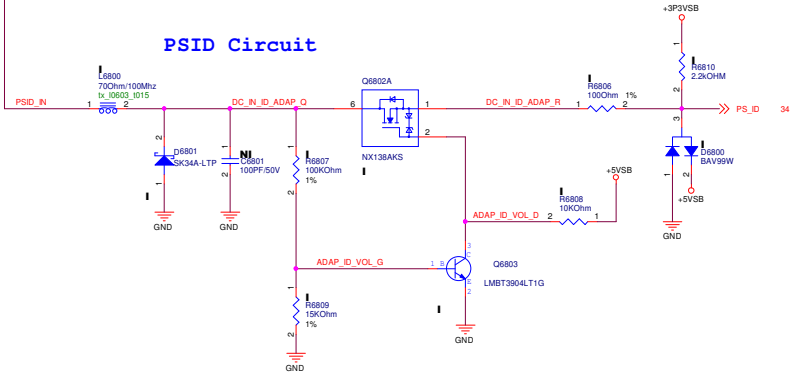
N : Iin = 180W / 19.5V
= 9.231A

N+1: Iin = 240W / 19.5V
= 12.308A



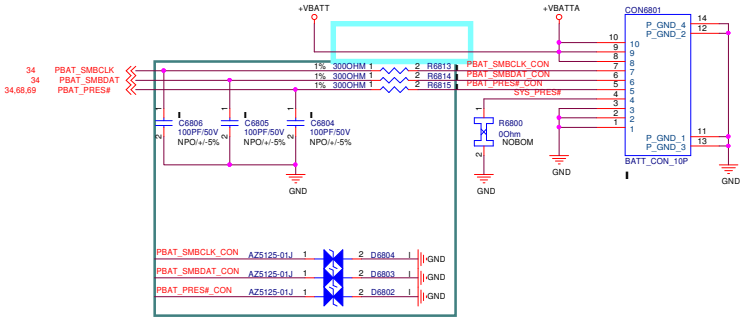
For EMI - X02/1020

PSID Circuit



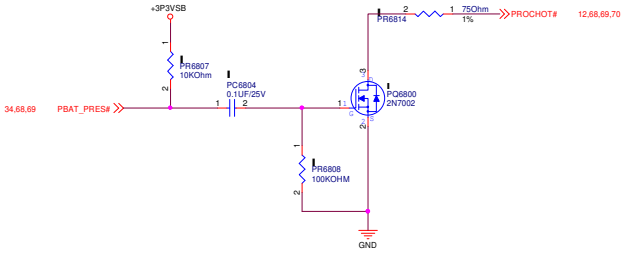
Remove JP6800 and JP6801

Battery Pack connector

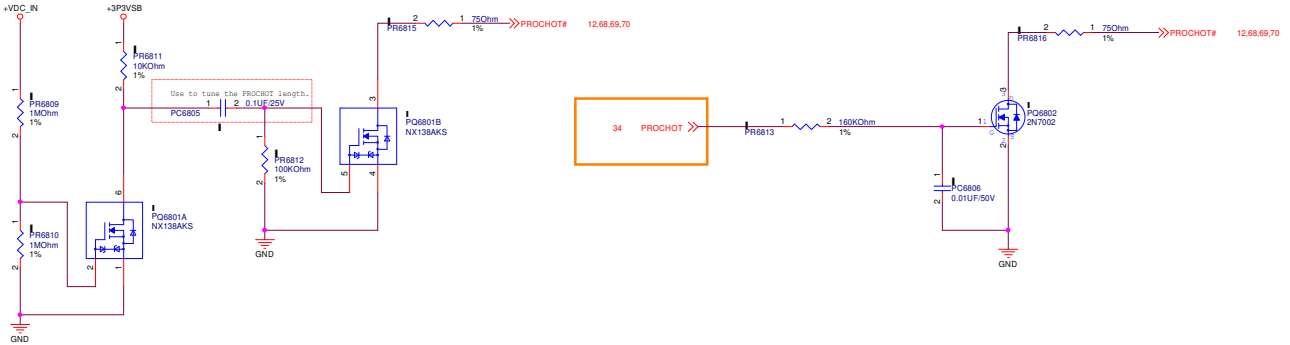


For Battery damage EC issue - X01/0824

Adapter Protection Circuit



Battery Protection Circuit



<Core Design>

PEGATRON Title : DC_IN

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A2	Vulcan	X00

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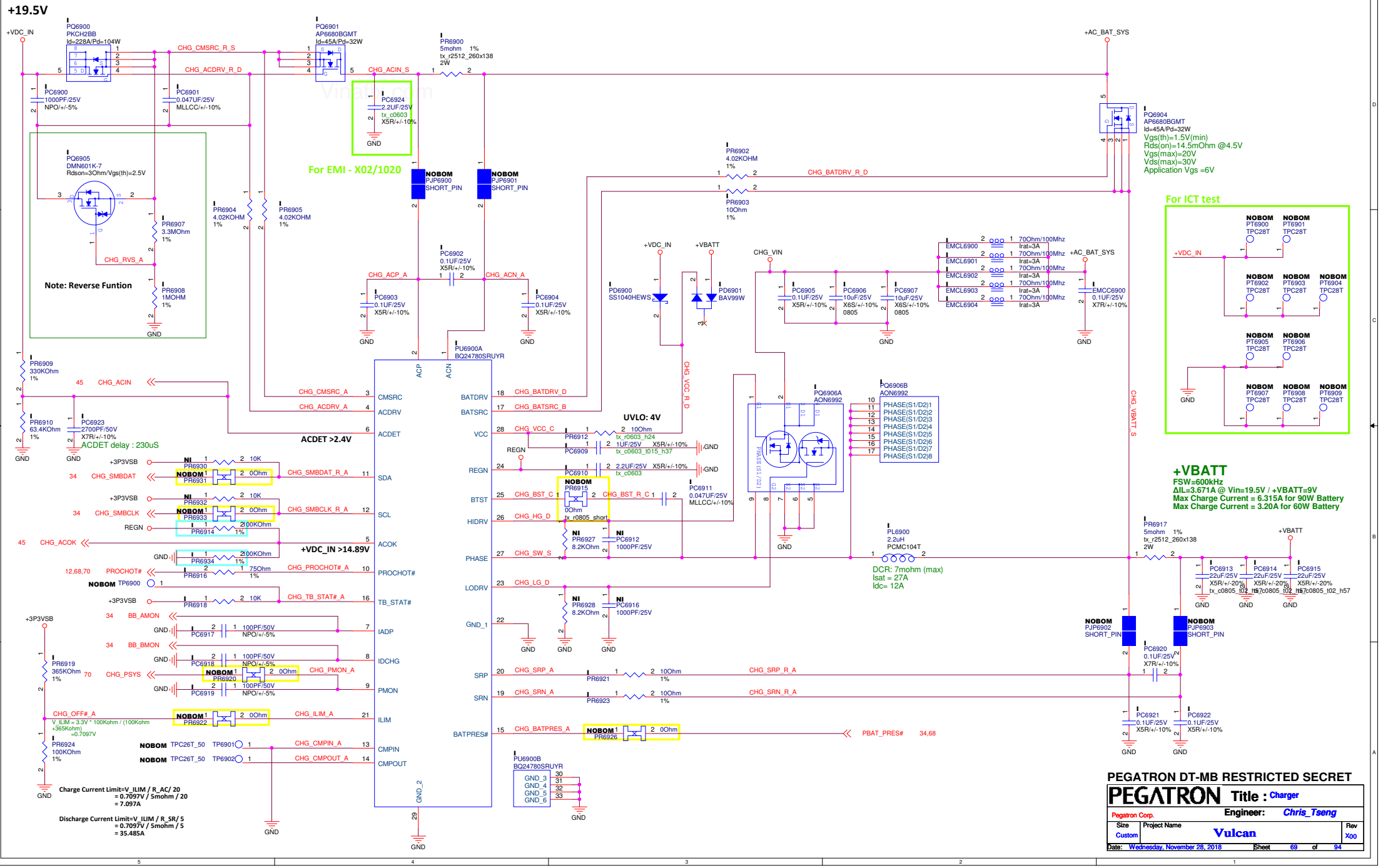
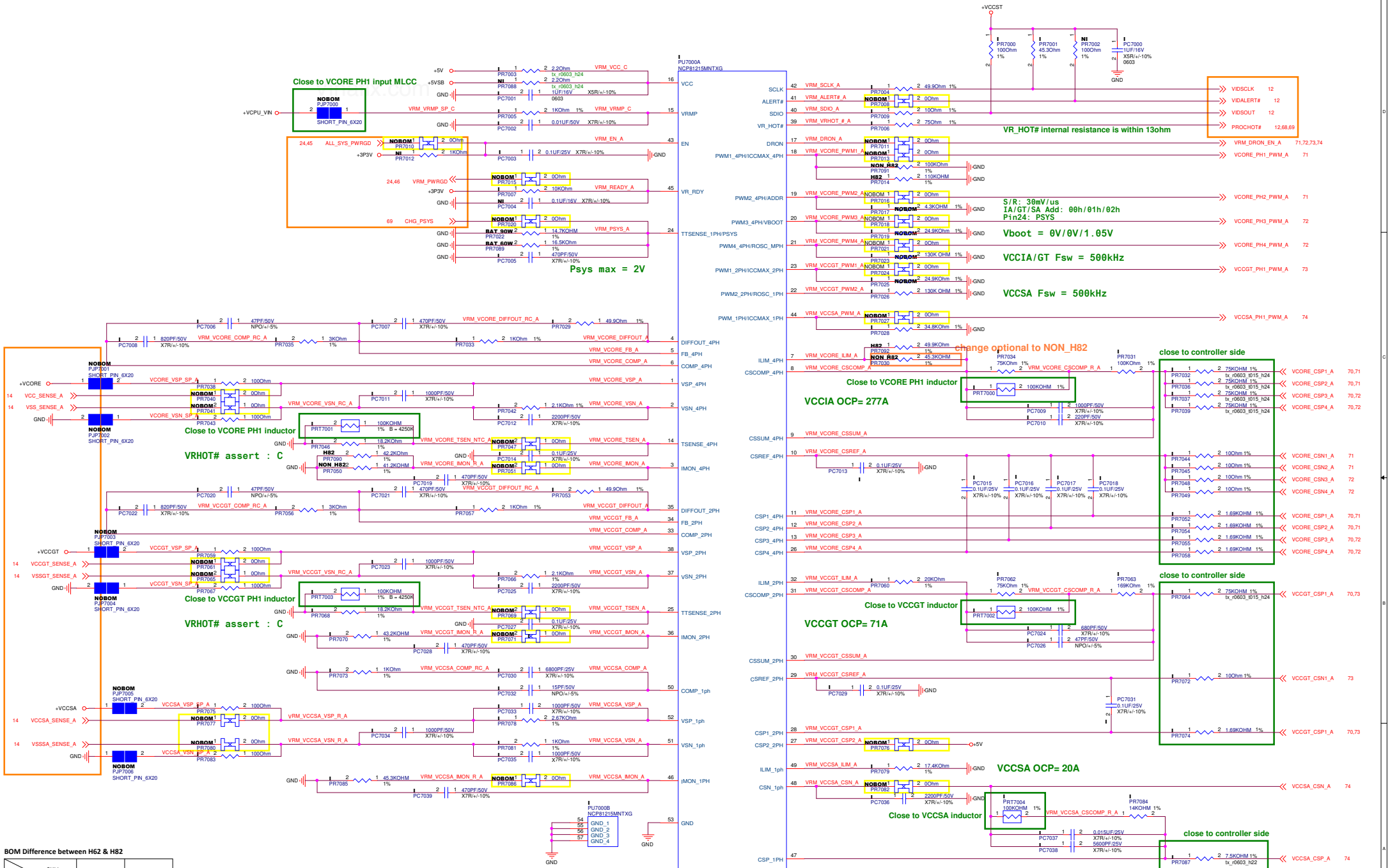

+19.5V
+VDC_IN
PQ6900
PKCH2BB
Id=228A/Pd=104W
CHG_CMSRC_R_S
CHG_ACDRV_R_D
PQ6901
AP6680BGMT
Id=45A/Pd=32W
CHG_ACIN_S
PR6900
5mohm 1%
tx_r2512_260x138
2W
+AC_BAT_SYS
PC6900
1000PF/25V
NPO/+/-5%
PC6901
0.047UF/25V
MLLCC/+/-10%
PC6924
2.2UF/25V
tx_c0603
X5R/+/-10%
GND
For EMI - X02/1020
NOBOM
PJP6900
SHORT_PIN
NOBOM
PJP6901
SHORT_PIN
PQ6904
AP6680BGMT
Id=45A/Pd=32W
Vgs(th)=1.5V(min)
Rds(on)=14.5mOhm @4.5V
Vgs(max)=20V
Vds(max)=30V
Application Vgs =6V
PR6902
4.02KOHM
1%
CHG_BATDRV_R_D
PR6903
10Ohm
1%
For ICT test
PQ6905
DMN601K-7
Rdson=3Ohm/Vgs(th)=2.5V
PR6907
3.3MOhm
1%
CHG_RVS_A
Note: Reverse Funtion
PR6908
1MOHM
1%
PR6904
4.02KOHM
1%
PR6905
4.02KOHM
1%
PC6902
0.1UF/25V
X5R/+/-10%
CHG_ACP_A
CHG_ACN_A
PC6903
0.1UF/25V
X5R/+/-10%
PC6904
0.1UF/25V
X5R/+/-10%
PU6900A
BQ24780SRUYR
+VDC_IN
+VBATT
CHG_VIN
PD6900
SS1040HEWS
PD6901
BAV99W
PC6905
0.1UF/25V
X5R/+/-10%
PC6906
10uF/25V
X6S/+/-10%
0805
PC6907
10uF/25V
X6S/+/-10%
0805
EMCL6900
EMCL6901
EMCL6902
EMCL6903
EMCL6904
70Ohm/100Mhz
Irat=3A
EMCC6900
0.1UF/25V
X7R/+/-10%
PR6909
330KOhm
1%
PR6910
63.4KOhm
1%
PC6923
2700PF/50V
X7R/+/-10%
ACDET delay : 230uS
ACDET >2.4V
UVLO: 4V
CHG_VCC_R_D
CHG_VBATT_S
PQ6906A
AON6992
PQ6906B
AON6992
PHASE(S1/D2)1
PHASE(S1/D2)2
PHASE(S1/D2)3
PHASE(S1/D2)4
PHASE(S1/D2)5
PHASE(S1/D2)6
PHASE(S1/D2)7
PHASE(S1/D2)8
+VBATT
FSW=600kHz
ΔIL=3.671A @ Vin=19.5V / +VBATT=9V
Max Charge Current = 6.315A for 90W Battery
Max Charge Current = 3.20A for 60W Battery
PR6917
5mohm 1%
tx_r2512_260x138
2W
PL6900
2.2uH
PCMC104T
DCR: 7mohm (max)
Isat = 27A
Idc= 12A
PC6913
22uF/25V
X5R/+/-20%
tx_c0805_t02_h57
PC6914
22uF/25V
X5R/+/-20%
tx_c0805_t02_h57
PC6915
22uF/25V
X5R/+/-20%
tx_c0805_t02_h57
NOBOM
PJP6902
SHORT_PIN
NOBOM
PJP6903
SHORT_PIN
PC6920
0.1UF/25V
X7R/+/-10%
PC6921
0.1UF/25V
X5R/+/-10%
PC6922
0.1UF/25V
X5R/+/-10%
CMSRC
ACDRV
ACDET
SDA
SCL
ACOK
PROCHOT#
TB_STAT#
IADP
IDCHG
PMON
ILIM
CMPIN
CMPOUT
ACP
ACN
BATDRV
BATSRC
VCC
REGN
BTST
HIDRV
PHASE
LODRV
GND_1
SRP
SRN
BATPRES#
GND_2
CHG_CMSRC_A
CHG_ACDRV_A
CHG_BATDRV_D
CHG_BATSRC_B
CHG_VCC_C
CHG_BST_C
CHG_HG_D
CHG_SW_S
CHG_LG_D
CHG_SRP_A
CHG_SRN_A
CHG_BATPRES_A
CHG_SRP_R_A
CHG_SRN_R_A
PBAT_PRES#
34,68
CHG_ACIN
CHG_SMBDAT
CHG_SMBCLK
CHG_ACOK
PROCHOT#
CHG_PROCHOT#_A
CHG_TB_STAT#_A
BB_AMON
BB_BMON
CHG_PSYS
CHG_PMON_A
CHG_OFF#_A
CHG_ILIM_A
CHG_CMPIN_A
CHG_CMPOUT_A
CHG_SMBDAT_R_A
CHG_SMBCLK_R_A
+3P3VSB
REGN
+VDC_IN >14.89V
PR6930
PR6931
PR6932
PR6933
PR6914
PR6934
PR6916
PR6918
PR6917
PR6918
PR6919
365KOhm
1%
PR6920
PR6924
100KOhm
1%
V_ILIM = 3.3V * 100Kohm / (100Kohm +365Kohm)
=0.7097V
Charge Current Limit=V_ILIM / R_AC/ 20
= 0.7097V / 5mohm / 20
= 7.097A
Discharge Current Limit=V_ILIM / R_SR/ 5
= 0.7097V / 5mohm / 5
= 35.485A
TPC26T_50
TP6900
TP6901
TP6902
PR6912
PC6909
PC6910
PR6915
PC6911
0.047UF/25V
MLLCC/+/-10%
PR6927
8.2KOhm
PC6912
1000PF/25V
PR6928
8.2KOhm
PC6916
1000PF/25V
PR6921
PR6923
PR6926
PU6900B
BQ24780SRUYR
GND_3
GND_4
GND_5
GND_6
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : Charger
Pegatron Corp.
Engineer: Chris_Tseng
Size
Custom
Project Name
Vulcan
Rev
X00
Date: Wednesday, November 28, 2018
Sheet 69 of 94



BOM Difference between H62 & H82

SKU / Part Reference	H62	H82
PR7050 / PR7090	41.2KΩ	42.2KΩ
PR7014 / PR7091	110KΩ	100KΩ
PR7030 / PR7092	45.3KΩ (OCP = 252A)	49.9KΩ (OCP = 277A)

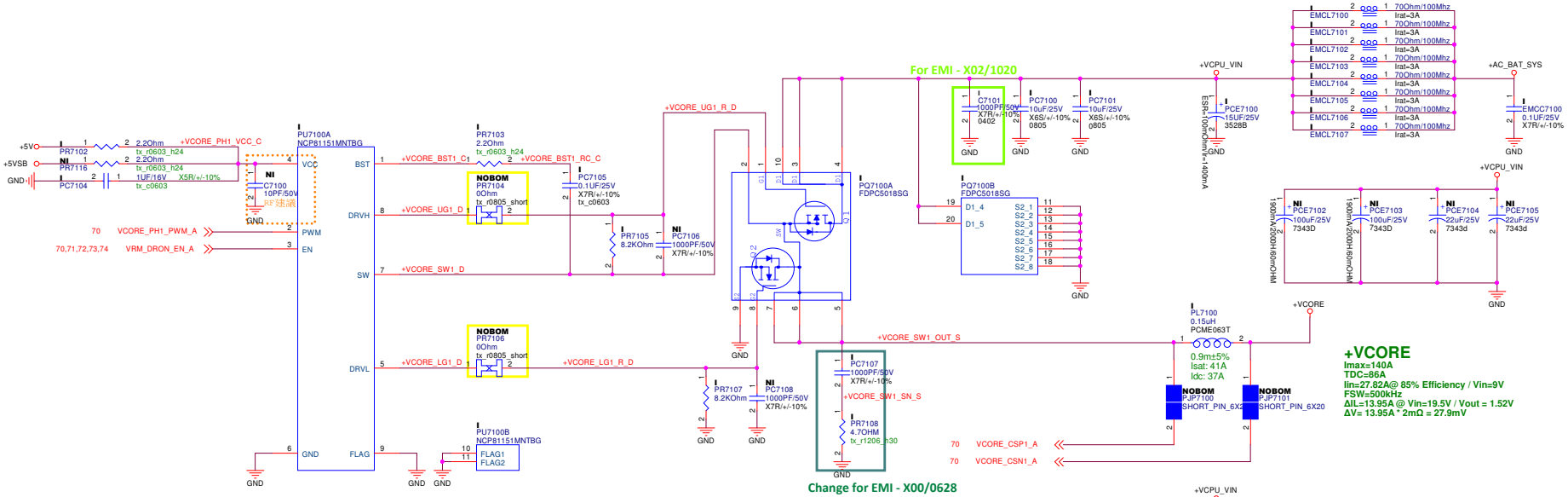
<Core Design>

PEGATRON Title : VR CONTROLLER

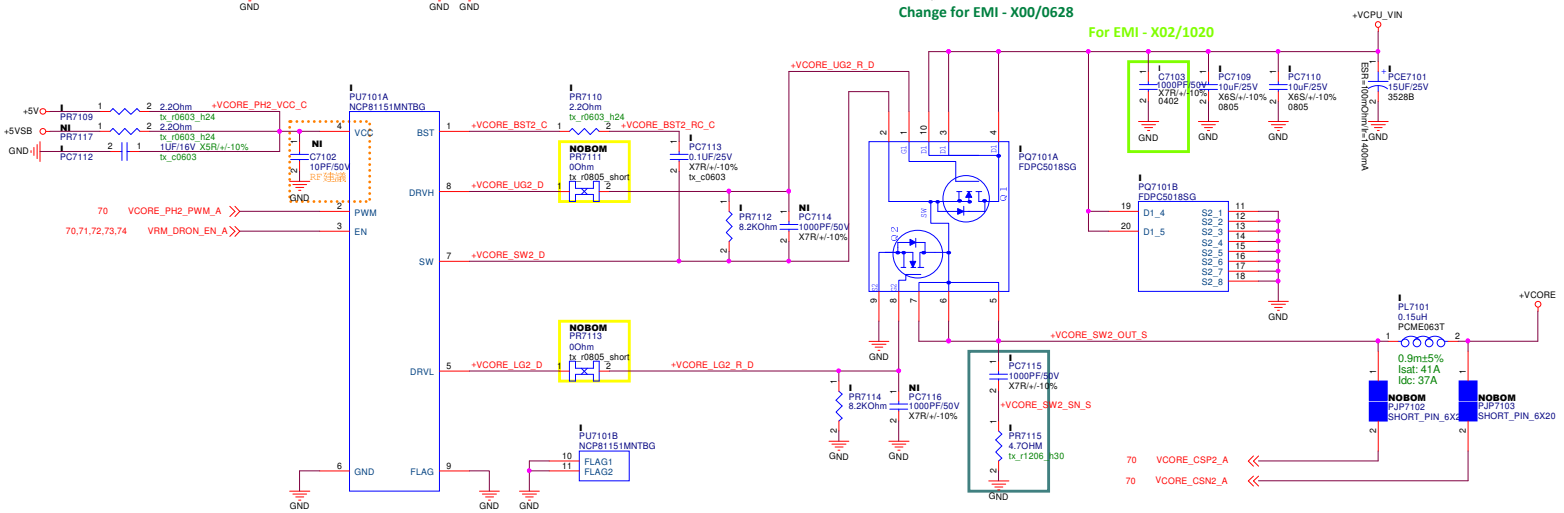
Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 70 of 94



+VCORE
Imax=140A
TDC=86A
Iin=27.82A@ 85% Efficiency / Vin=9V
FSW=500kHz
ΔIL=13.95A @ Vin=19.5V / Vout = 1.52V
ΔV= 13.95A * 2mΩ = 27.9mV



OWNER	+VCORE OC Point	Low Limit	High Limit
Atticus	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)
Terry	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)

```
I_Low Limit = I_DVID + Io_Cout
            = 26A + (30mV/uS) * 1748uF
            = 78.44A
```

※ Controller will shut down after 50uS when 184.99A ≤ Iout < 277.49A
Controller will shut down immediately when Iout trigger 277.49A

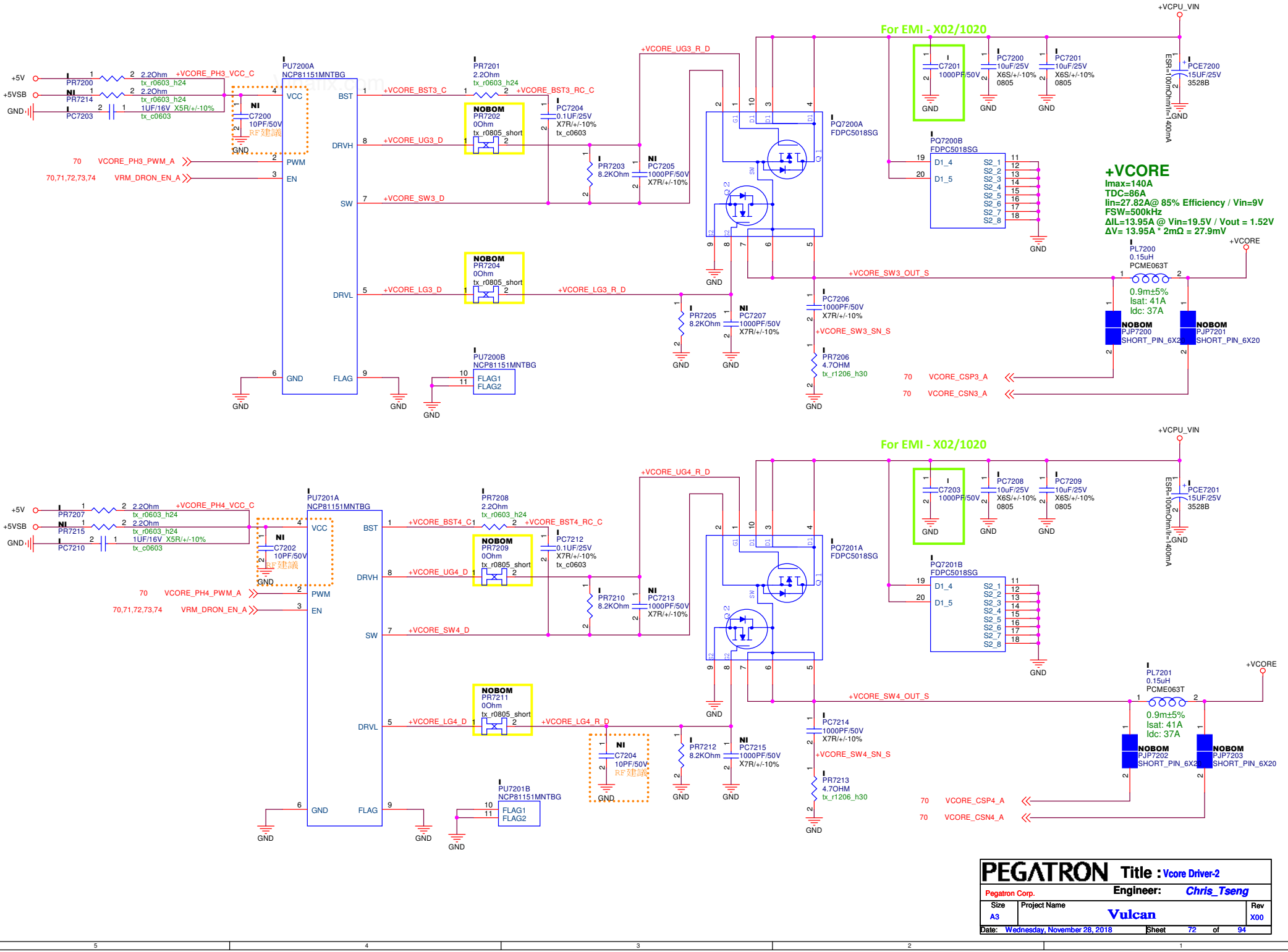
PEGATRON DT-MB RESTRICTED SECRET

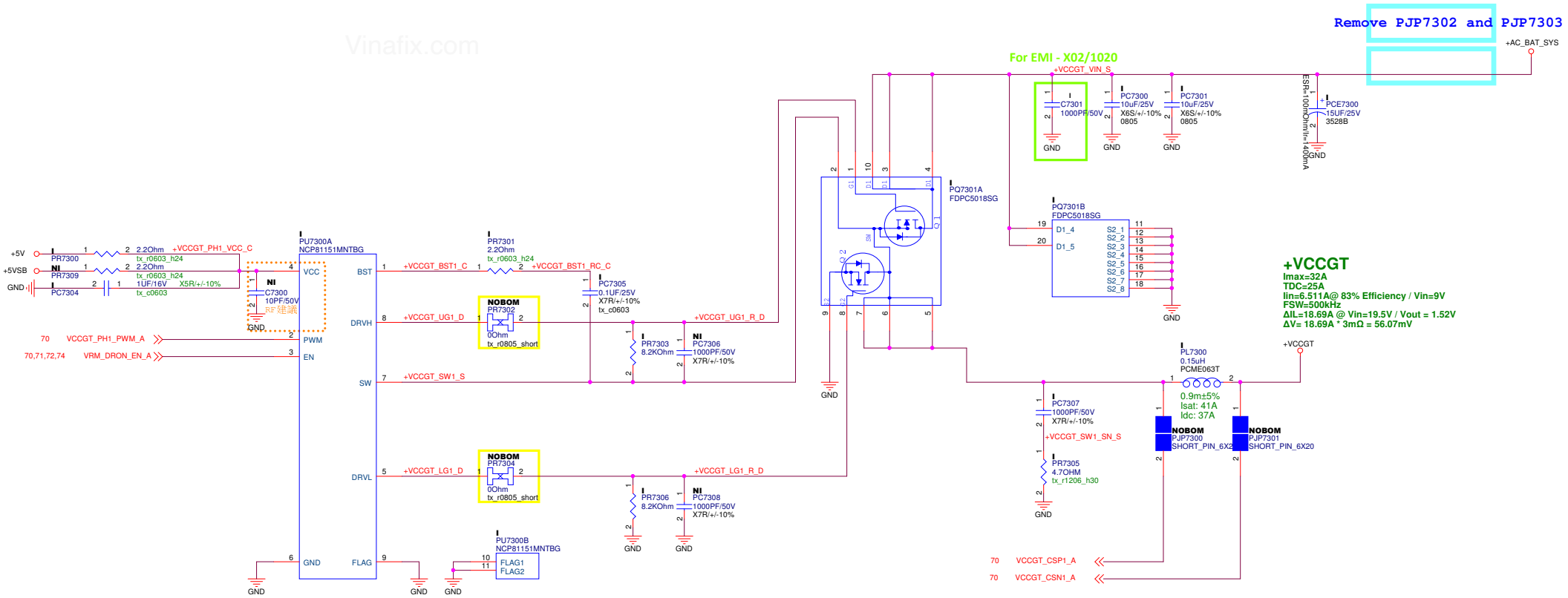
PEGATRON Title : Vcore Driver-1

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 71 of 94


For EMI - X02/1020
+VCPU_VIN
PU7200A
NCP81151MNTBG
+5V
+5VSB
GND
PR7200
PR7214
PC7203
2.2Ohm
tx_r0603_h24
1UF/16V X5R/+/-10%
tx_c0603
+VCORE_PH3_VCC_C
C7200
10PF/50V
RF建議
70 VCORE_PH3_PWM_A
70,71,72,73,74 VRM_DRON_EN_A
PWM
EN
VCC
BST
DRVH
SW
DRVL
FLAG
+VCORE_BST3_C
+VCORE_UG3_D
+VCORE_SW3_D
+VCORE_LG3_D
PR7201
+VCORE_BST3_RC_C
NOBOM
PR7202
PR7203
8.2KOhm
PC7204
0.1UF/25V
X7R/+/-10%
PC7205
1000PF/50V
PR7204
PR7205
PC7207
PU7200B
FLAG1
FLAG2
+VCORE_UG3_R_D
+VCORE_LG3_R_D
PQ7200A
FDPC5018SG
PQ7200B
C7201
PC7200
PC7201
10uF/25V
X6S/+/-10%
0805
PCE7200
15UF/25V
3528B
ESR=100mOhm/I=1400mA
+VCORE_SW3_OUT_S
+VCORE_SW3_SN_S
PC7206
PR7206
4.7OHM
tx_r1206_h30
70 VCORE_CSP3_A
70 VCORE_CSN3_A
+VCORE
Imax=140A
TDC=86A
Iin=27.82A@ 85% Efficiency / Vin=9V
FSW=500kHz
ΔIL=13.95A @ Vin=19.5V / Vout = 1.52V
ΔV= 13.95A * 2mΩ = 27.9mV
PL7200
0.15uH
PCME063T
0.9m±5%
Isat: 41A
Idc: 37A
PJP7200
SHORT_PIN_6X2
PJP7201
SHORT_PIN_6X20
For EMI - X02/1020
+VCPU_VIN
PU7201A
NCP81151MNTBG
+5V
+5VSB
GND
PR7207
PR7215
PC7210
2.2Ohm
tx_r0603_h24
1UF/16V X5R/+/-10%
tx_c0603
+VCORE_PH4_VCC_C
C7202
10PF/50V
RF建議
70 VCORE_PH4_PWM_A
70,71,72,73,74 VRM_DRON_EN_A
PWM
EN
VCC
BST
DRVH
SW
DRVL
FLAG
+VCORE_BST4_C
+VCORE_UG4_D
+VCORE_SW4_D
+VCORE_LG4_D
PR7208
+VCORE_BST4_RC_C
NOBOM
PR7209
PR7210
8.2KOhm
PC7212
0.1UF/25V
X7R/+/-10%
PC7213
1000PF/50V
PR7211
PR7212
PC7215
PU7201B
FLAG1
FLAG2
+VCORE_UG4_R_D
+VCORE_LG4_R_D
PQ7201A
FDPC5018SG
PQ7201B
C7203
PC7208
PC7209
10uF/25V
X6S/+/-10%
0805
PCE7201
15UF/25V
3528B
ESR=100mOhm/I=1400mA
+VCORE_SW4_OUT_S
+VCORE_SW4_SN_S
PC7214
PR7213
4.7OHM
tx_r1206_h30
70 VCORE_CSP4_A
70 VCORE_CSN4_A
+VCORE
PL7201
0.15uH
PCME063T
0.9m±5%
Isat: 41A
Idc: 37A
PJP7202
SHORT_PIN_6X2
PJP7203
SHORT_PIN_6X20
PEGATRON
Title : Vcore Driver-2
Pegatron Corp.
Engineer: Chris_Tseng
Size A3
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 72 of 94



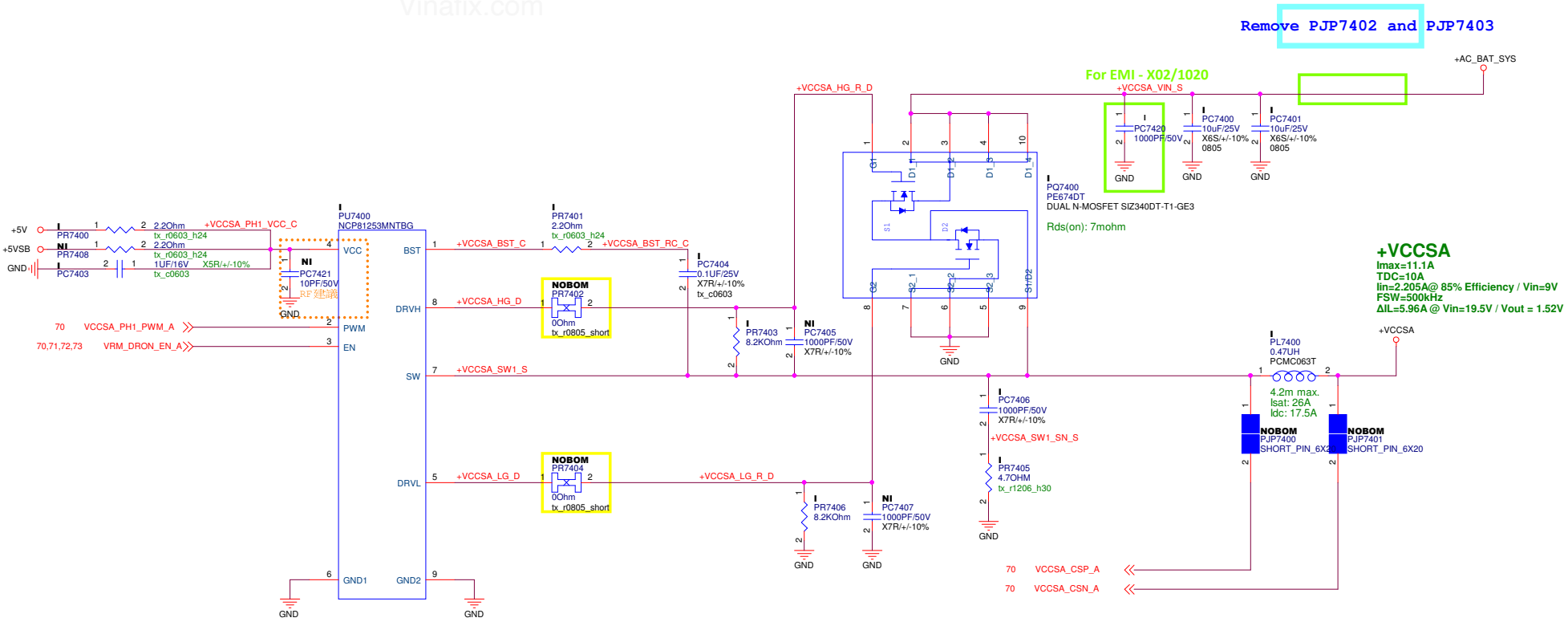
OWNER	+VCCGT OC Point	Low Limit	High Limit
Atticus	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A
Terry	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A

I_Low Limit = I_DVID + Io_Cout
= 8A + (30mV/uS) * 1156uF
= 42.68A

※ Controller will shut down after 50uS when 47.51A ≤ Iout < 71.27A
Controller will shut down immediately when Iout trigger 71.27A

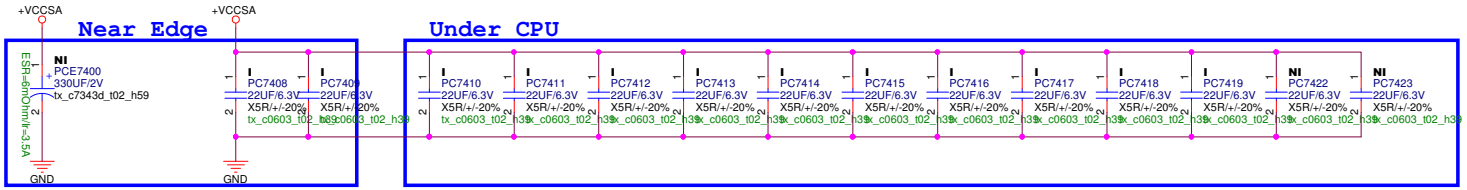
PEGATRON DT-MB RESTRICTED SECRET
<Core Design>

PEGATRON Title : VccGT Driver
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 73 of 94



OWNER	+VCCSA OC Point	Low Limit	High Limit
Atticus	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A
Terry	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A

```
I_Low Limit = I_DVID + Io_Cout
            = 5A + (30mV/uS) * 265uF
            = 12.95A
```



VCCSA Output CAP

330uF/2V/H=2mm * 1(NI)
22uF/6.3V * 12 (I)
22uF/6.3V * 2 (NI)

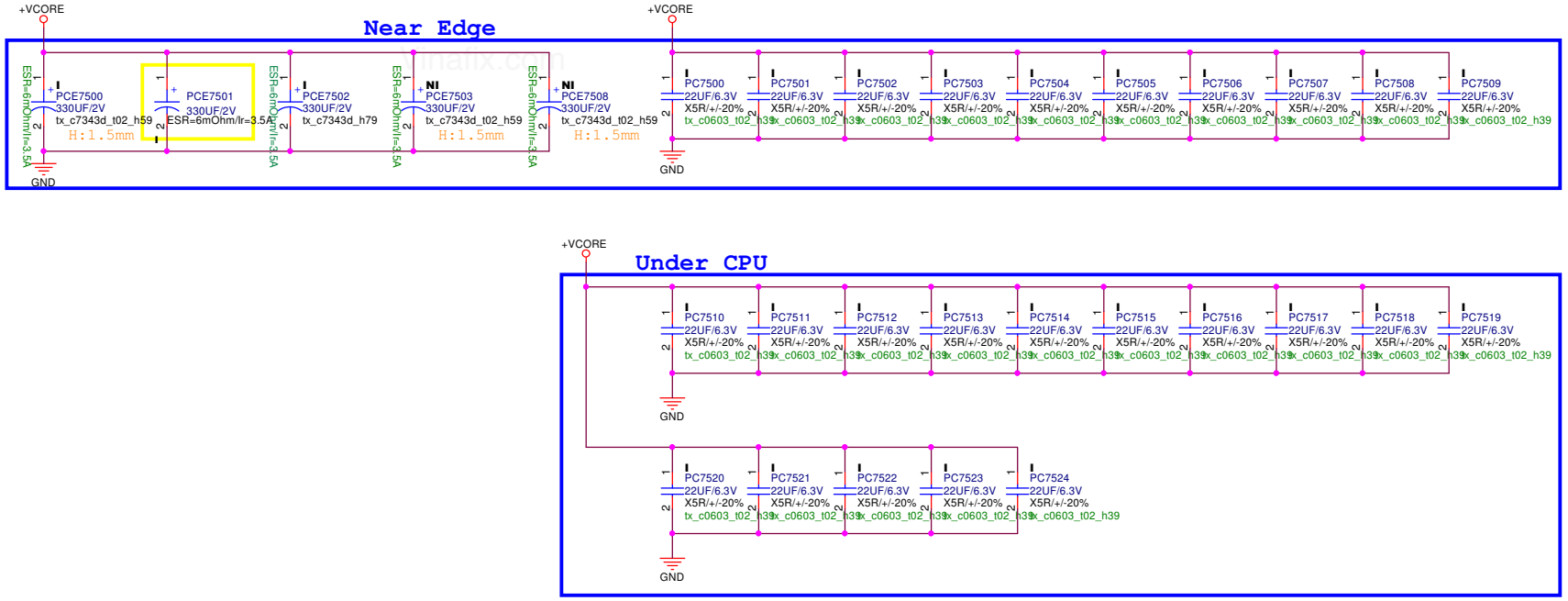
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VccSA Driver

Pegatron Corp. Engineer: Chris_Tseng

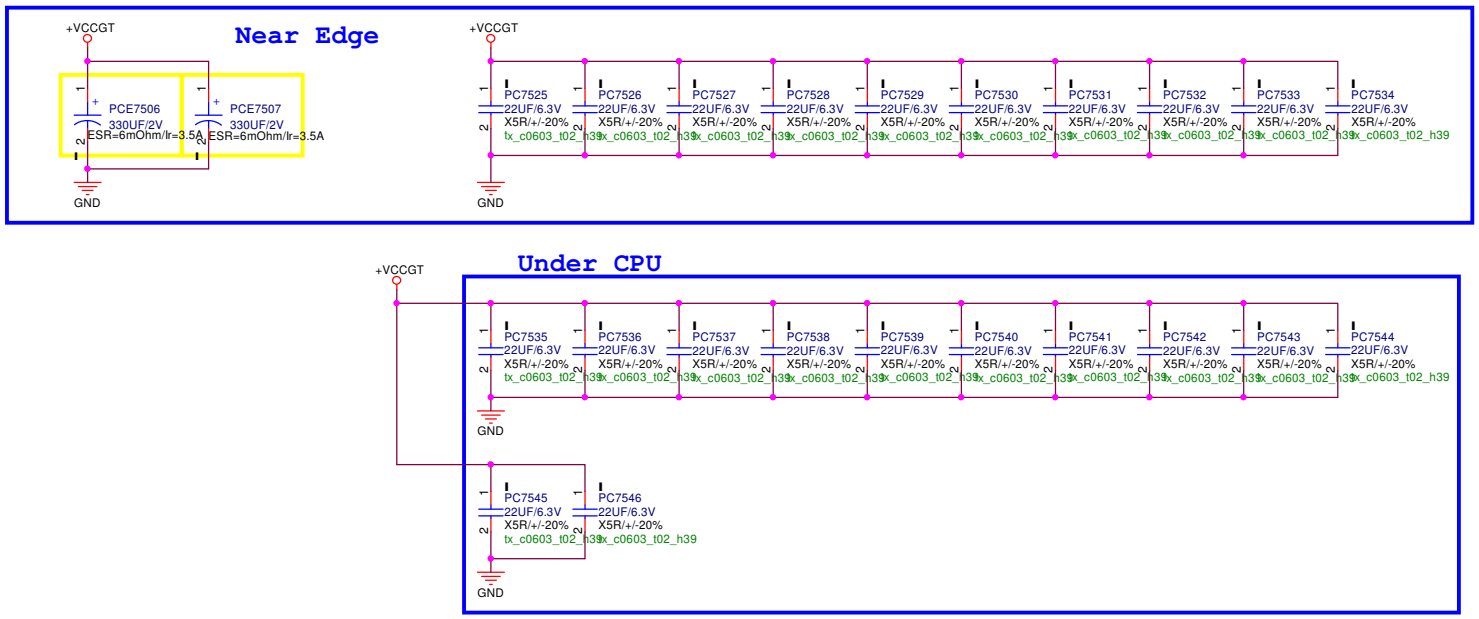
Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 74 of 94



Vcore Output CAP

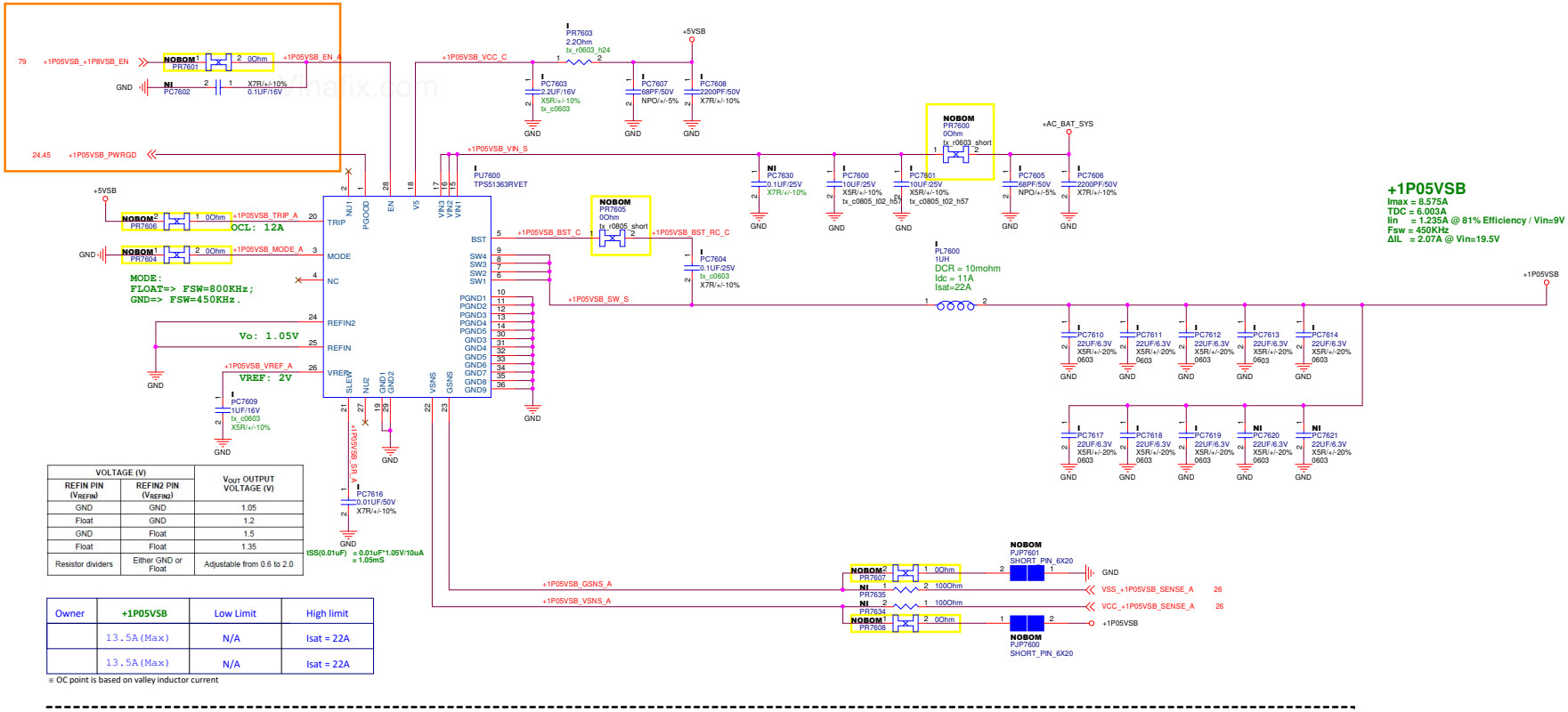
330uF/2V/H=2mm * 2 (I)
330uF/2V/H=1.5mm * 1(I)
330uF/2V/H=1.5mm * 2(NI)
22uF * 25



VCCGT Output CAP

330uF/2V/H=2mm * 2 (I)
22uF * 22

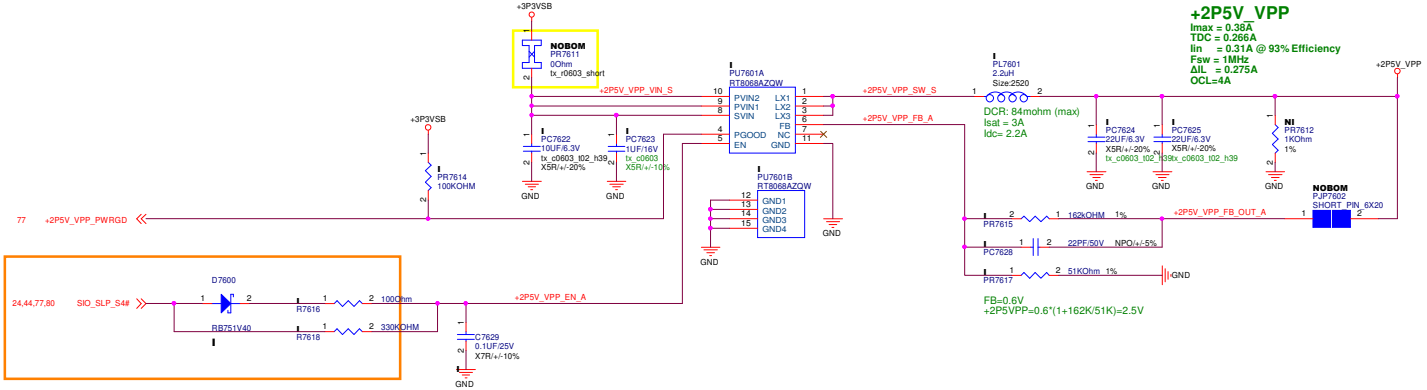
PEGATRON	Title :	Vcore & VccGT CAP
Pegatron Corp.	Engineer:	Chris_Tseng
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 75 of 94	



VOLTAGE (V)		
REFIN PIN (V_{REFIN})	REFIN2 PIN (V_{REFIN2})	V_{OUT} OUTPUT VOLTAGE (V)
GND	GND	1.05
Float	GND	1.2
GND	Float	1.5
Float	Float	1.35
Resistor dividers	Either GND or Float	Adjustable from 0.6 to 2.0

Owner	+1P05VSB	Low Limit	High limit
	13.5A(Max)	N/A	Isat = 22A
	13.5A(Max)	N/A	Isat = 22A

※ OC point is based on valley inductor current



Owner	+2P5V_VPP	Low Limit	High limit
	4.0A	N/A	0.66uH @ 6A
	4.0A	N/A	0.66uH @ 6A

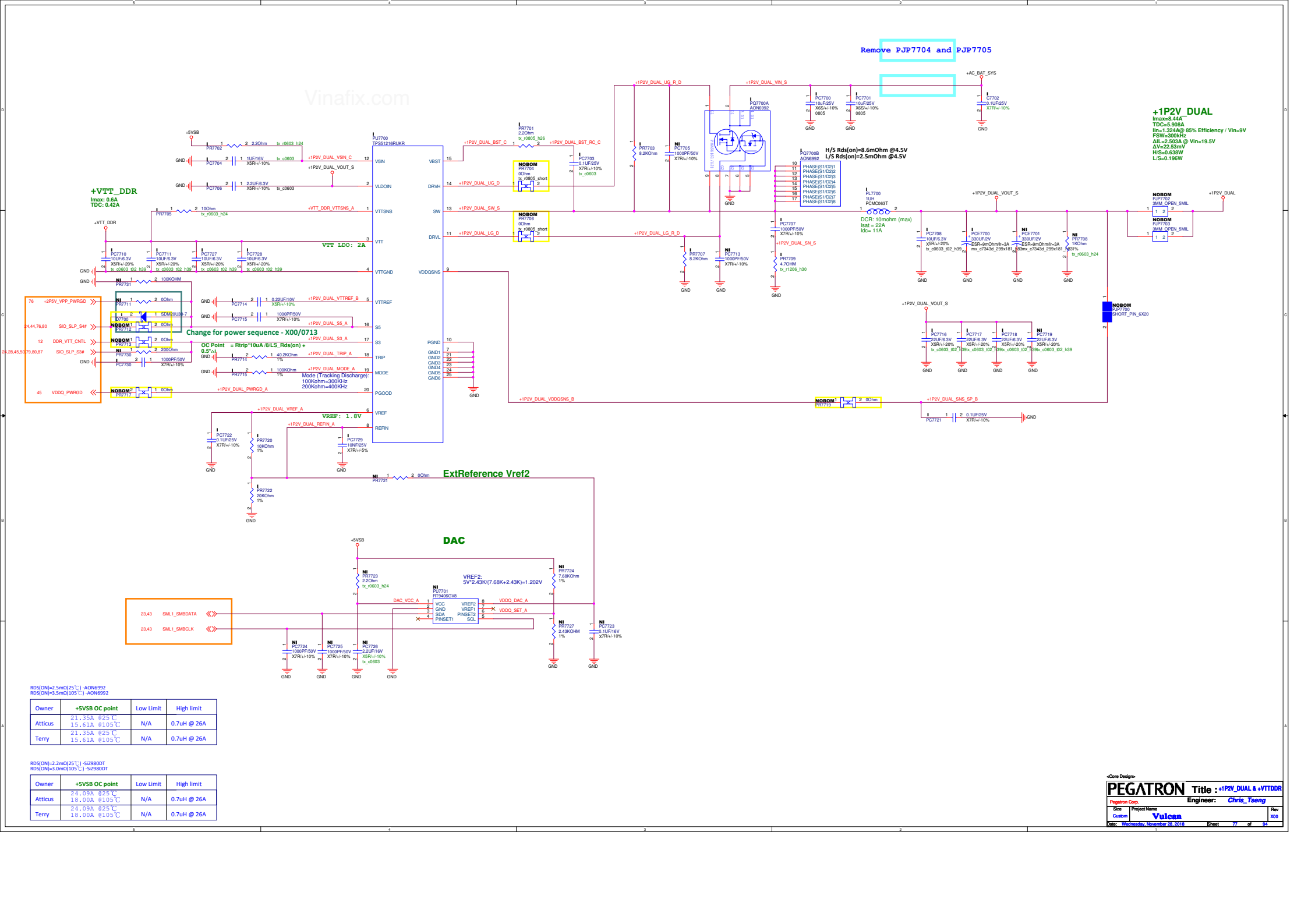
※ OC point is based on peak inductor current

PEGATRON Title : +1P05VSB/+2P5VPP

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 76 of 94



RDS(ON)=2.5mΩ(25℃) -AON6992
RDS(ON)=3.5mΩ(105℃) -AON6992

Owner	+5VSB OC point	Low Limit	High limit
Atticus	21.35A @25℃ 15.61A @105℃	N/A	0.7uH @ 26A
Terry	21.35A @25℃ 15.61A @105℃	N/A	0.7uH @ 26A

RDS(ON)=2.2mΩ(25℃) -SiZ980DT
RDS(ON)=3.0mΩ(105℃) -SiZ980DT

Owner	+5VSB OC point	Low Limit	High limit
Atticus	24.09A @25℃ 18.00A @105℃	N/A	0.7uH @ 26A
Terry	24.09A @25℃ 18.00A @105℃	N/A	0.7uH @ 26A

<Core Design>

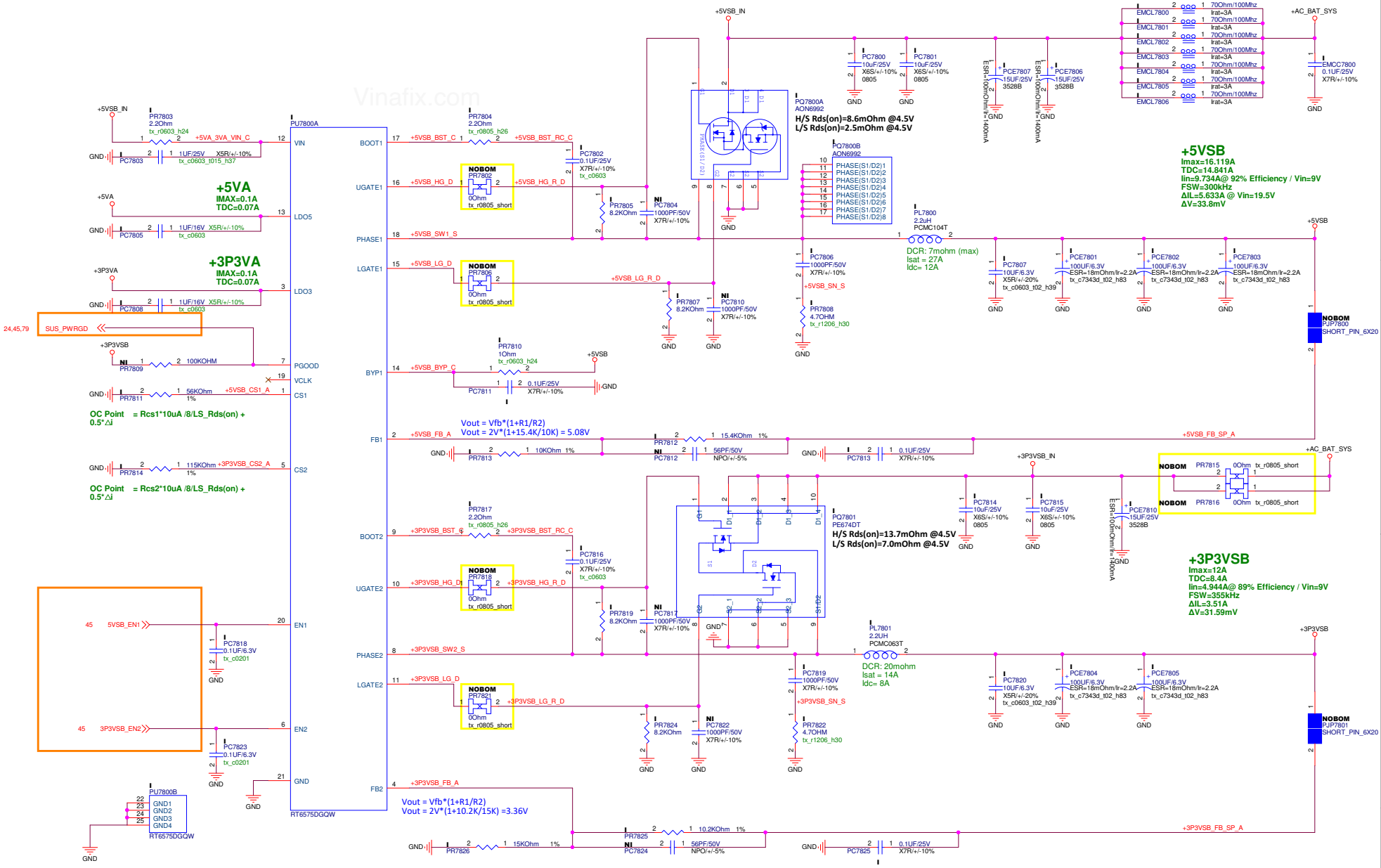
PEGATRON Corp.

Title : +1P2V_DUAL & +VTTDDR

Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 77 of 94



RDS(ON)=2.5mΩ(25℃) -AON6992
RDS(ON)=3.5mΩ(105℃) -AON6992

Owner	+5VSB OC point	Low Limit	High limit
	30.82A @25℃ 22.82A @105℃	N/A	1.6uH @ 36A
	32.3165A @25℃ 23.89A @105℃	N/A	1.6uH @ 36A

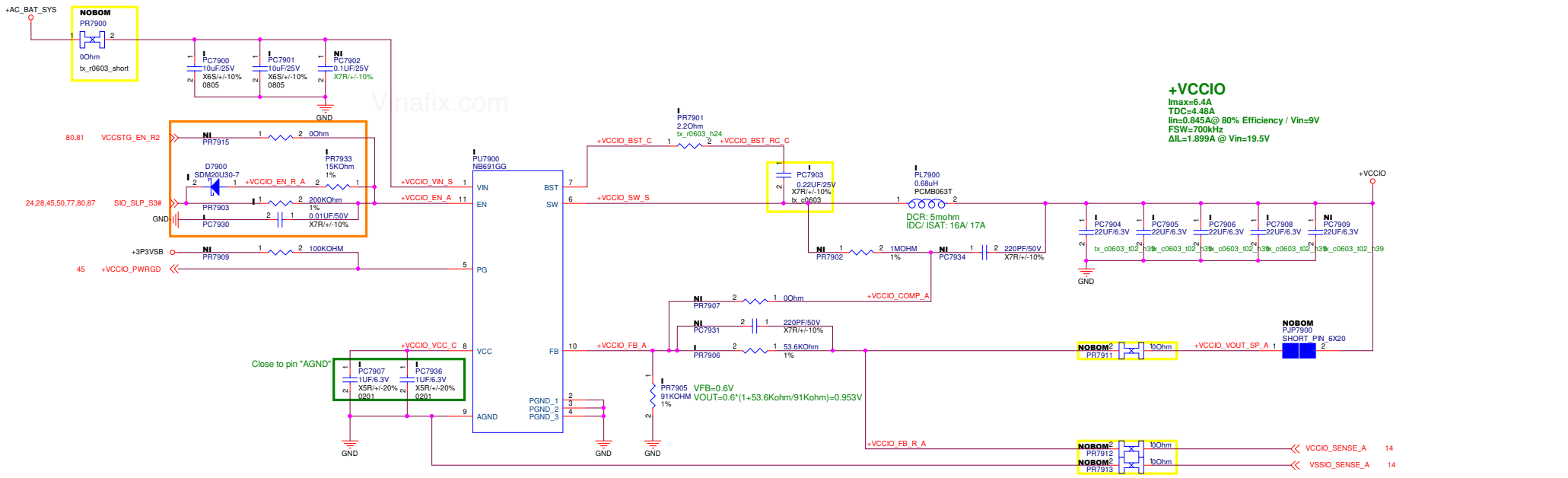
RDS(ON)=7.0mΩ(25℃) -SIZ340DT-T1-GE3
RDS(ON)=9.8mΩ(105℃) -SIZ340DT-T1-GE3

Owner	+3P3VSB OC point	Low Limit	High limit
	22.29A @25C 16.463A @105C	N/A	1.5uH @ 23A
	22.29A @25C 16.463A @105C	N/A	1.5uH @ 23A

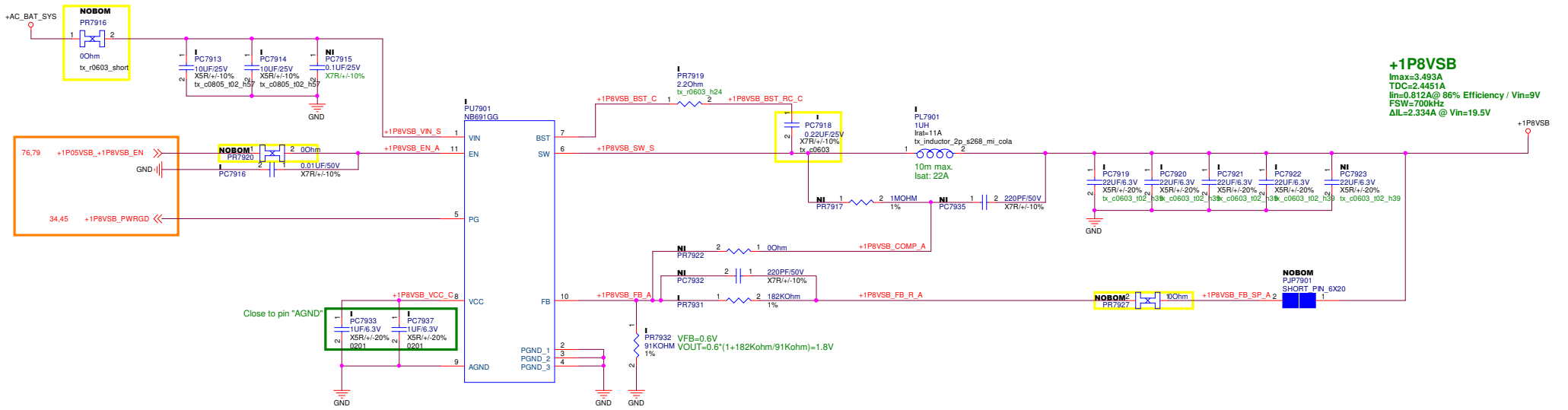
RDS(ON)=2.2mΩ(25℃) -SIZ980DT
RDS(ON)=3.08mΩ(105℃) -SIZ980DT

Owner	+5VSB OC point	Low Limit	High limit
	34.63A @25℃ 25.54A @105℃	N/A	1.6uH @ 36A
	34.63A @25℃ 25.54A @105℃	N/A	1.6uH @ 36A

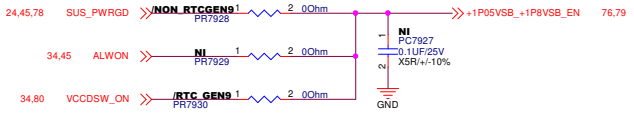
PEGATRON Title : +3P3VSB / +5VSB
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 78 of 94



Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Atticus	7A (min.) 8A (max.)	N/A	L_Isat = 17A
Terry	7A (min.) 8A (max.)	N/A	L_Isat = 17A



Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Atticus	7A (min.) 8A (max.)	N/A	L_Isat = 22A
Terry	7A (min.) 8A (max.)	N/A	L_Isat = 22A



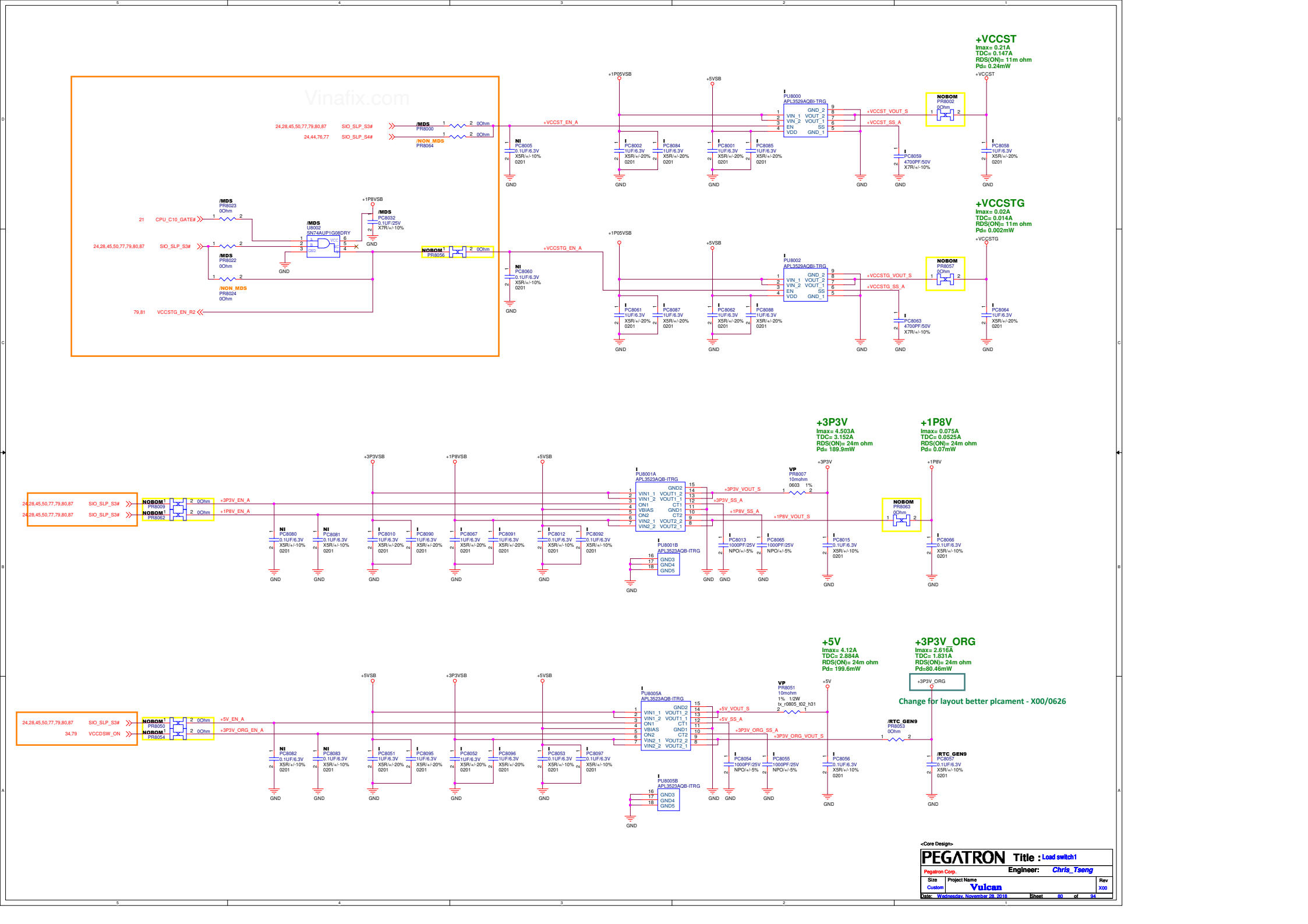
<Core Design>

PEGATRON Title : 79.+VCCIO/ +1P8V

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 79 of 94


+VCCST
Imax= 0.21A
TDC= 0.147A
RDS(ON)= 11m ohm
Pd= 0.24mW
+VCCSTG
Imax= 0.02A
TDC= 0.014A
RDS(ON)= 11m ohm
Pd= 0.002mW
+3P3V
Imax= 4.503A
TDC= 3.152A
RDS(ON)= 24m ohm
Pd= 189.9mW
+1P8V
Imax= 0.075A
TDC= 0.0525A
RDS(ON)= 24m ohm
Pd= 0.07mW
+5V
Imax= 4.12A
TDC= 2.884A
RDS(ON)= 24m ohm
Pd= 199.6mW
+3P3V_ORG
Imax= 2.616A
TDC= 1.831A
RDS(ON)= 24m ohm
Pd=80.46mW
Change for layout better plcament - X00/0626
PEGATRON
Title : Load switch1
Pegatron Corp.
Engineer: Chris_Tseng
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
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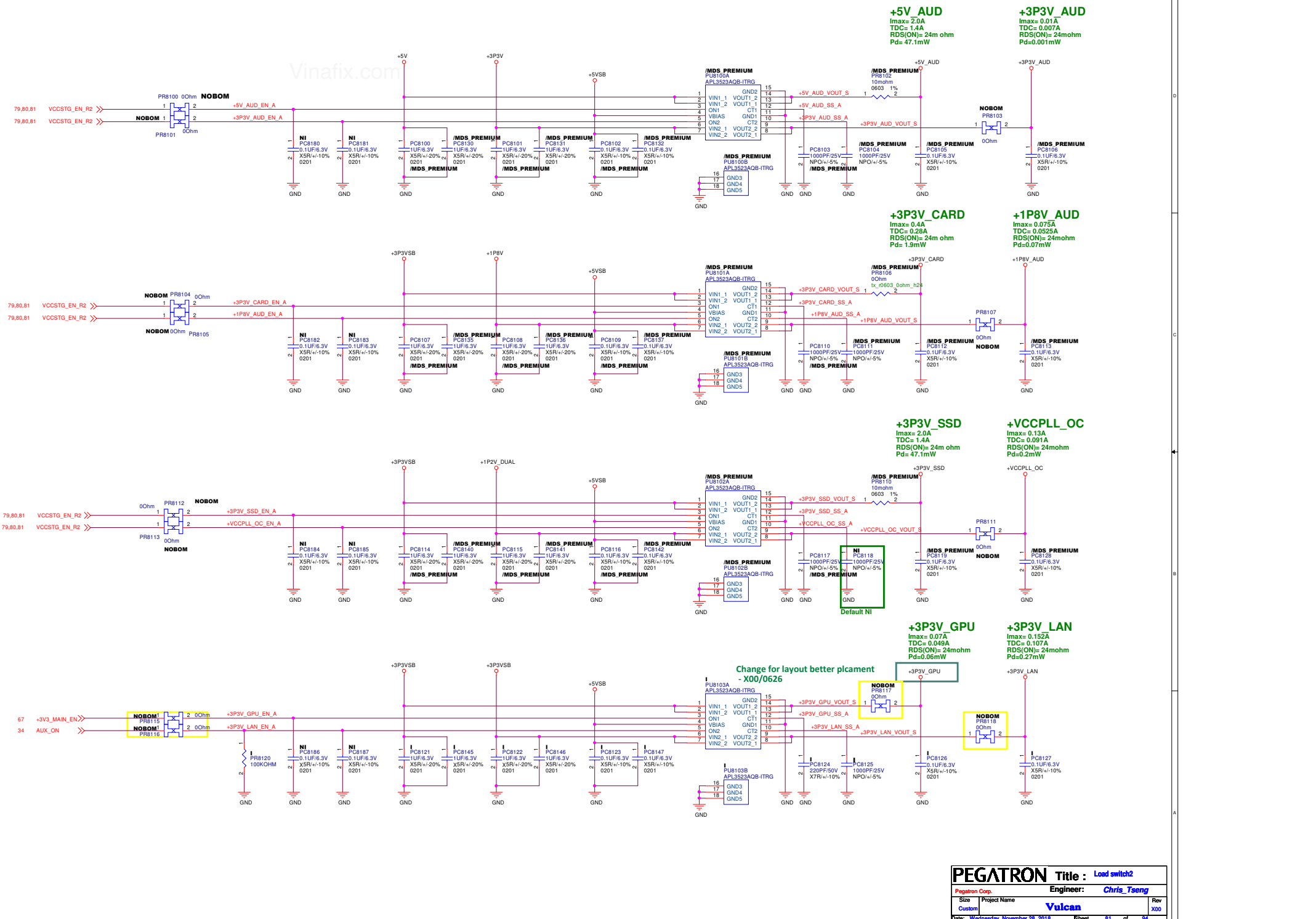
+5V_AUD
Imax= 2.0A
TDC= 1.4A
RDS(ON)= 24m ohm
Pd= 47.1mW
+3P3V_AUD
Imax= 0.01A
TDC= 0.007A
RDS(ON)= 24mohm
Pd=0.001mW
+3P3V_CARD
Imax= 0.4A
TDC= 0.28A
RDS(ON)= 24m ohm
Pd= 1.9mW
+1P8V_AUD
Imax= 0.075A
TDC= 0.0525A
RDS(ON)= 24mohm
Pd=0.07mW
+3P3V_SSD
Imax= 2.0A
TDC= 1.4A
RDS(ON)= 24m ohm
Pd= 47.1mW
+VCCPLL_OC
Imax= 0.13A
TDC= 0.091A
RDS(ON)= 24mohm
Pd=0.2mW
+3P3V_GPU
Imax= 0.07A
TDC= 0.049A
RDS(ON)= 24mohm
Pd=0.06mW
+3P3V_LAN
Imax= 0.152A
TDC= 0.107A
RDS(ON)= 24mohm
Pd=0.27mW
Change for layout better plcament
- X00/0626
Default NI
PEGATRON
Title : Load switch2
Pegatron Corp.
Engineer: Chris_Tseng
Size: Custom
Project Name: Vulcan
Rev: X00
Date: Wednesday, November 28, 2018
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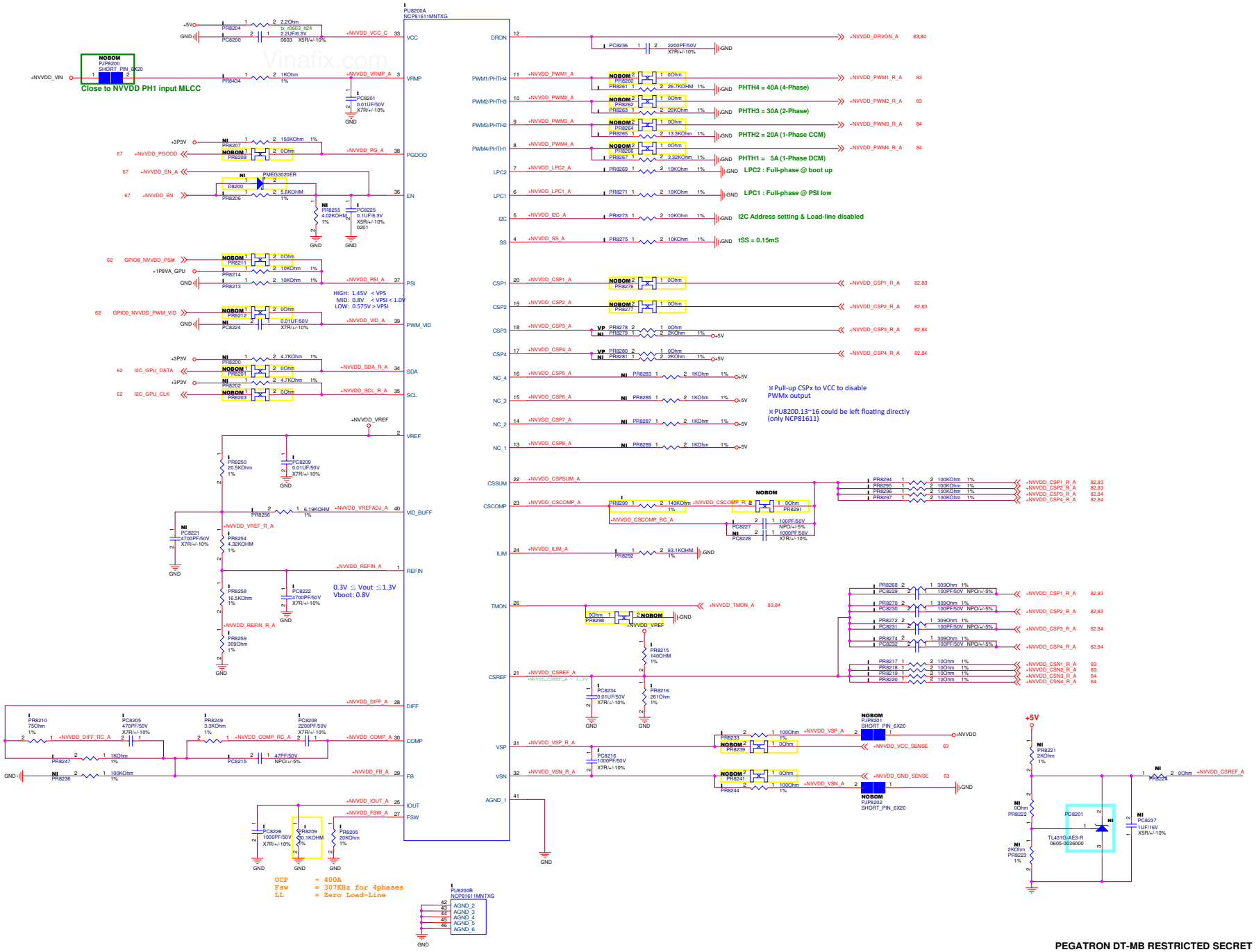
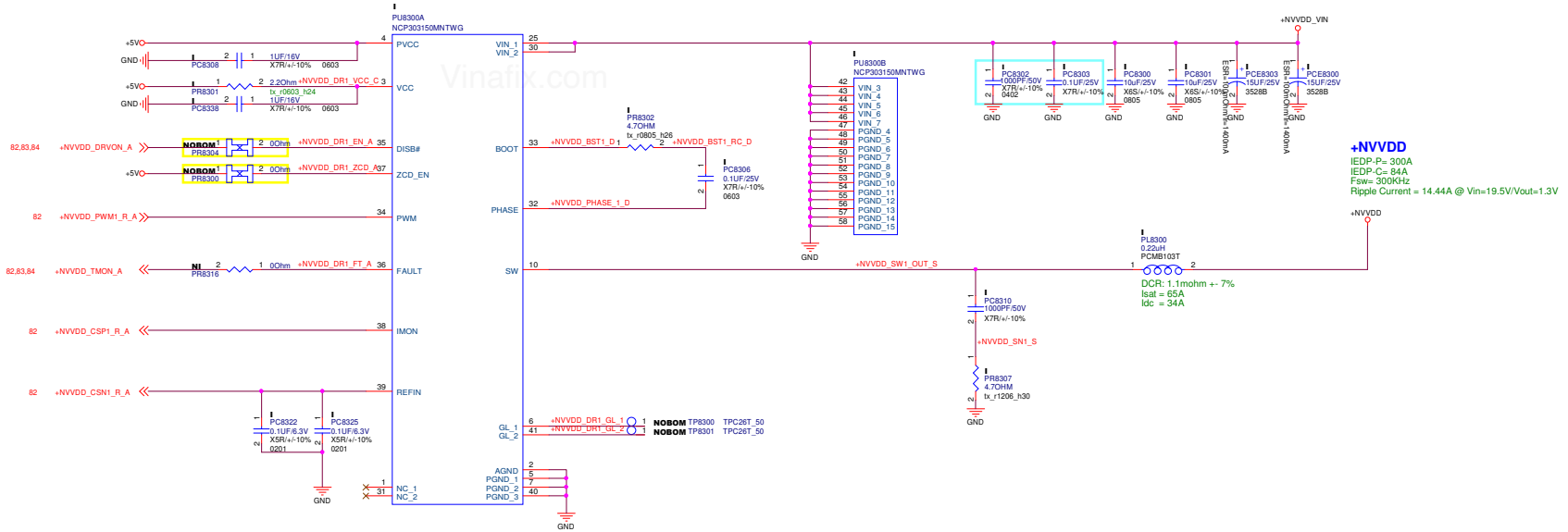
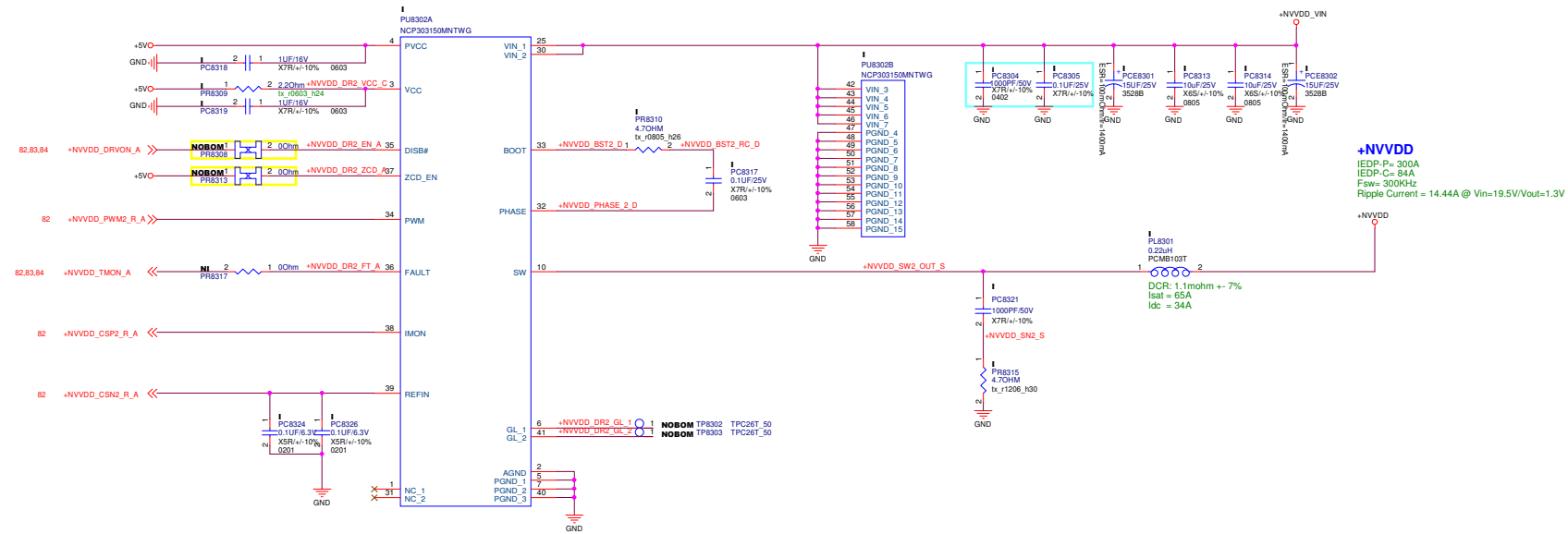

PU8200A
NCP81611MNTXG
Close to NVVDD PH1 input MLCC
Vinafix.com
HIGH: 1.45V < VPS
MID: 0.8V < VPSI < 1.0V
LOW: 0.575V > VPSI
0.3V ≤ Vout ≤1.3V
Vboot: 0.8V
※ Pull-up CSPx to VCC to disable PWMx output
※ PU8200.13~16 could be left floating directly (only NCP81611)
PHTH4 = 40A (4-Phase)
PHTH3 = 30A (2-Phase)
PHTH2 = 20A (1-Phase CCM)
PHTH1 = 5A (1-Phase DCM)
LPC2 : Full-phase @ boot up
LPC1 : Full-phase @ PSI low
I2C Address setting & Load-line disabled
tSS = 0.15mS
OCP ~ 400A
Fsw = 307KHz for 4phases
LL = Zero Load-Line
PU8200B
NCP81611MNTXG
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : +NVVDD Controller
Engineer: Chris_Tseng
Vulcan
Wednesday, November 28, 2018





PEGATRON DT-MB RESTRICTED SECRET

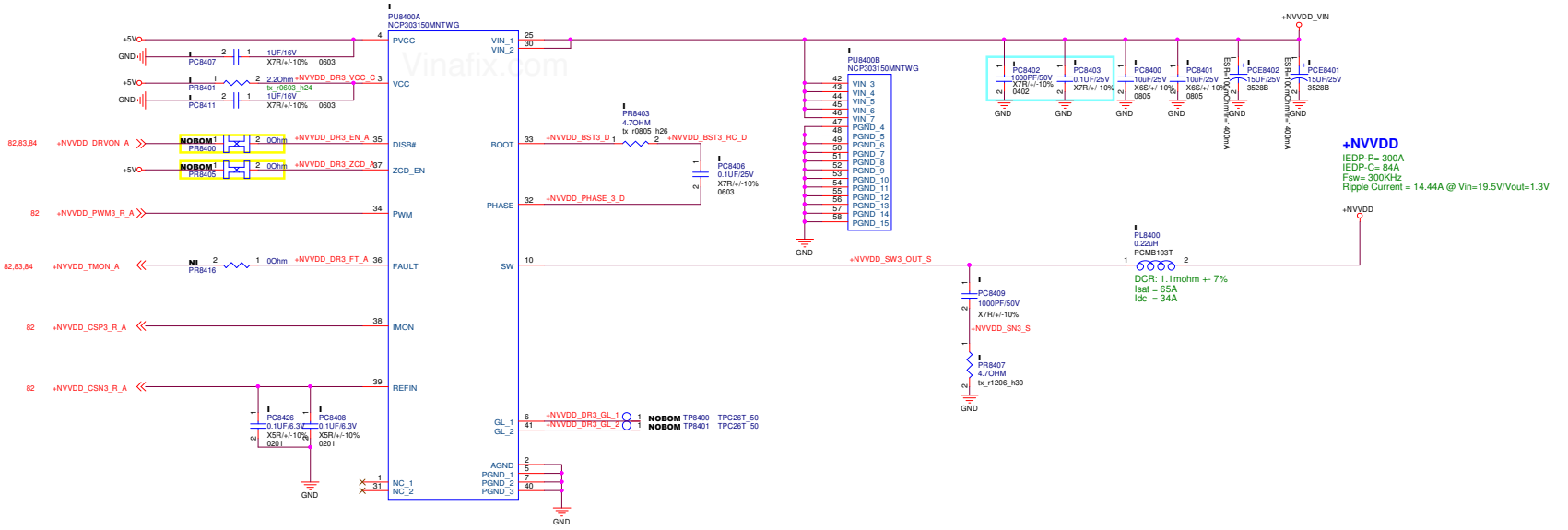
<Core Design>

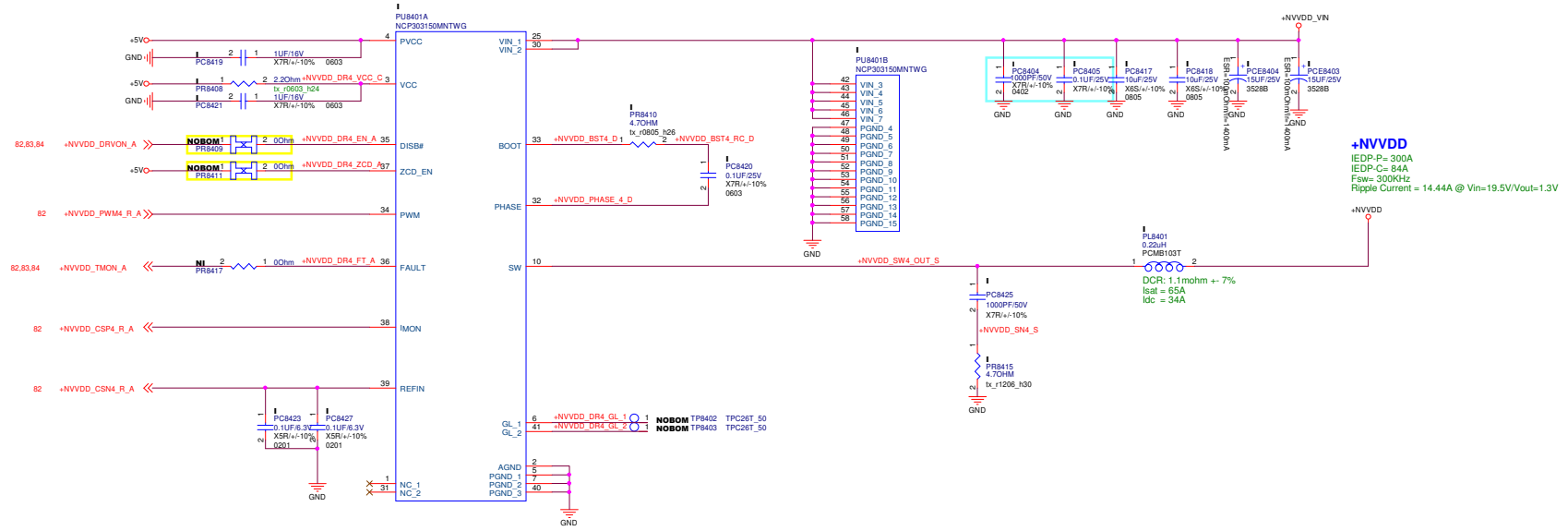
PEGATRON Title : +NVDD Driver /Cap

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 83 of 94





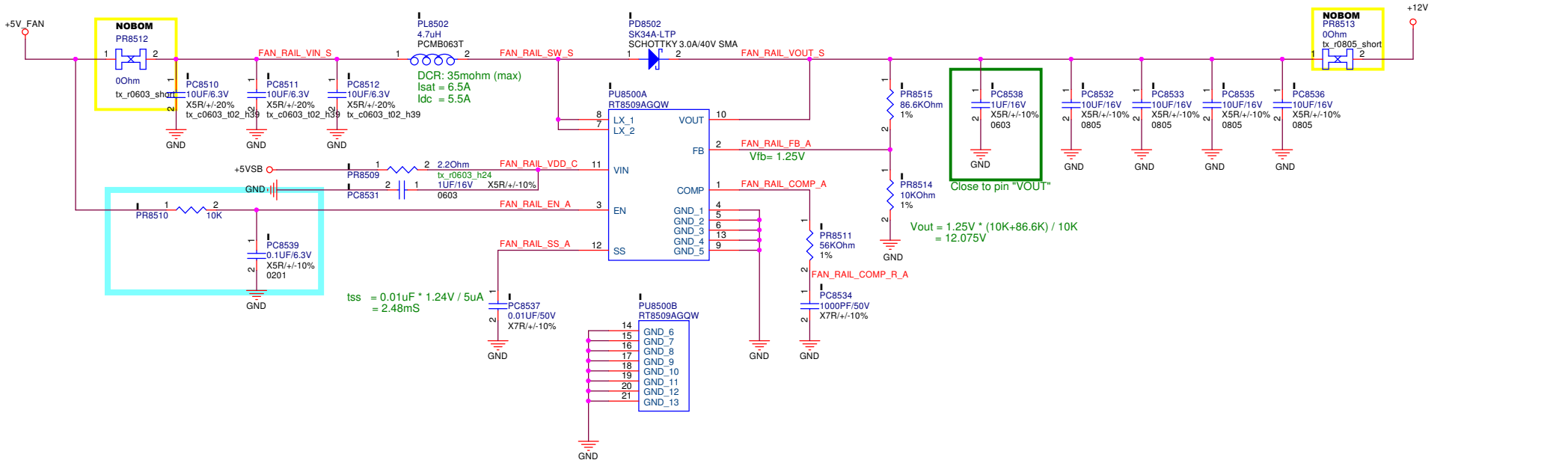
<Core Design>

PEGATRON Title : +NVVDD Driver-2

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 84 of 94



Owner	+12V OC point	Low Limit	High limit
	4.5A(Min)/5.0A(Typ.)	N/A	3.25uH @ 8A
	4.5A(Min)/5.0A(Typ.)	N/A	3.25uH @ 8A

※ OC point is based on peak inductor current

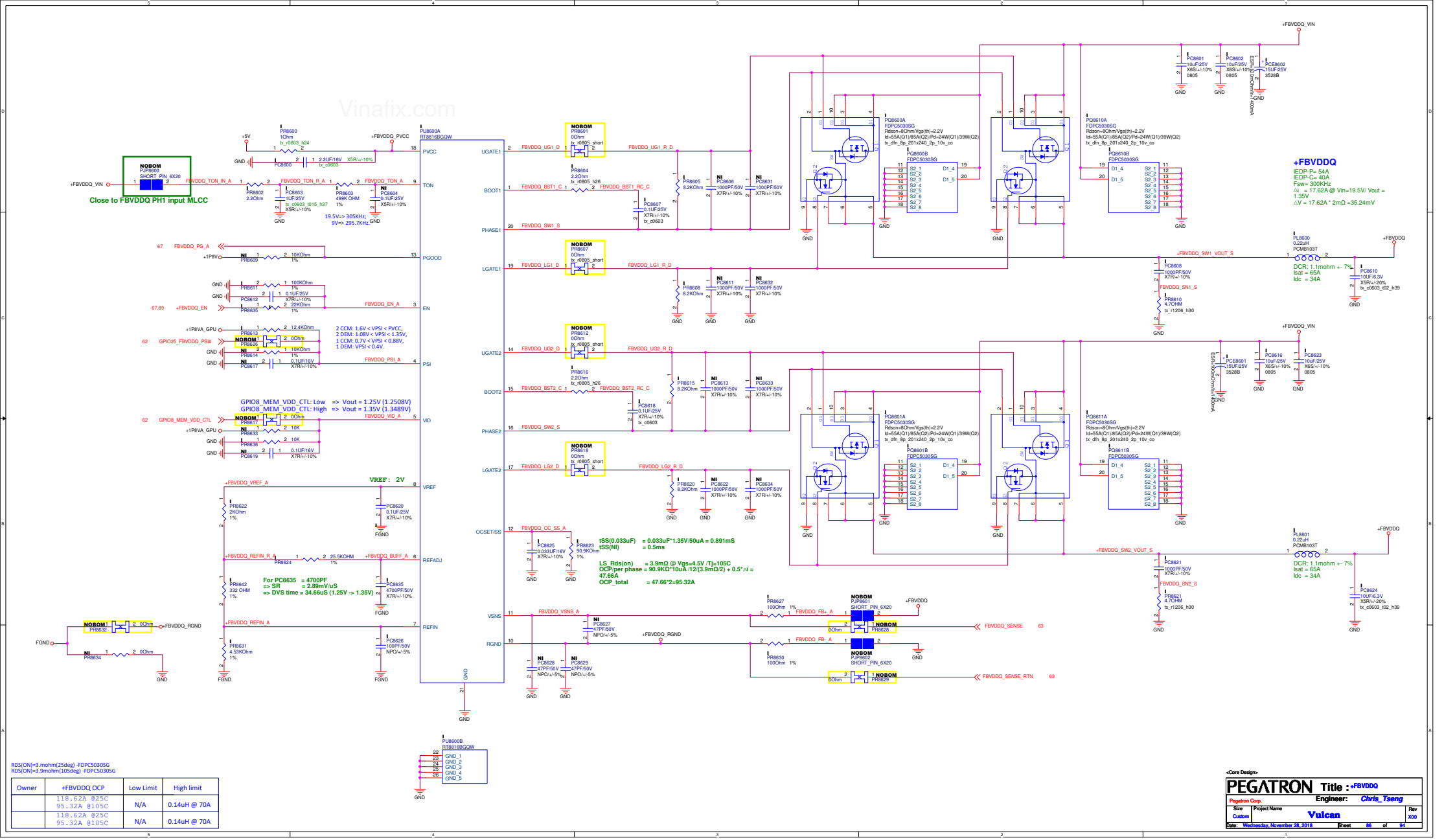
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +12V

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 85 of 94



RDS(ON)=3.mohm(25deg) -FDPC5030SG
RDS(ON)=3.9mohm(105deg) -FDPC5030SG

Owner	+FBVDDQ OCP	Low Limit	High limit
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A

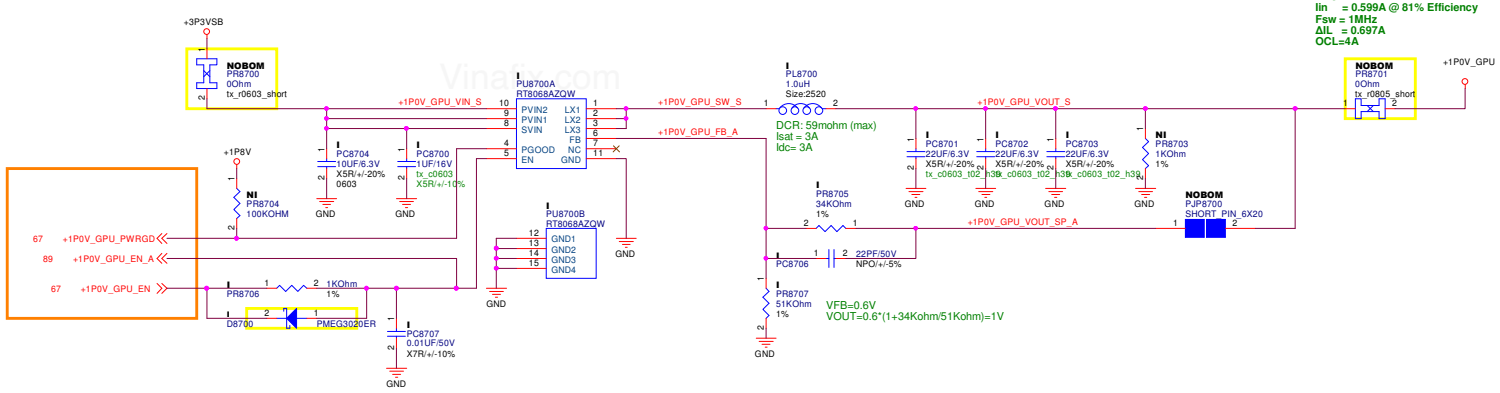
<Core Design>

PEGATRON Title : +FBVDDQ

Pegatron Corp. Engineer: Chris_Tseng

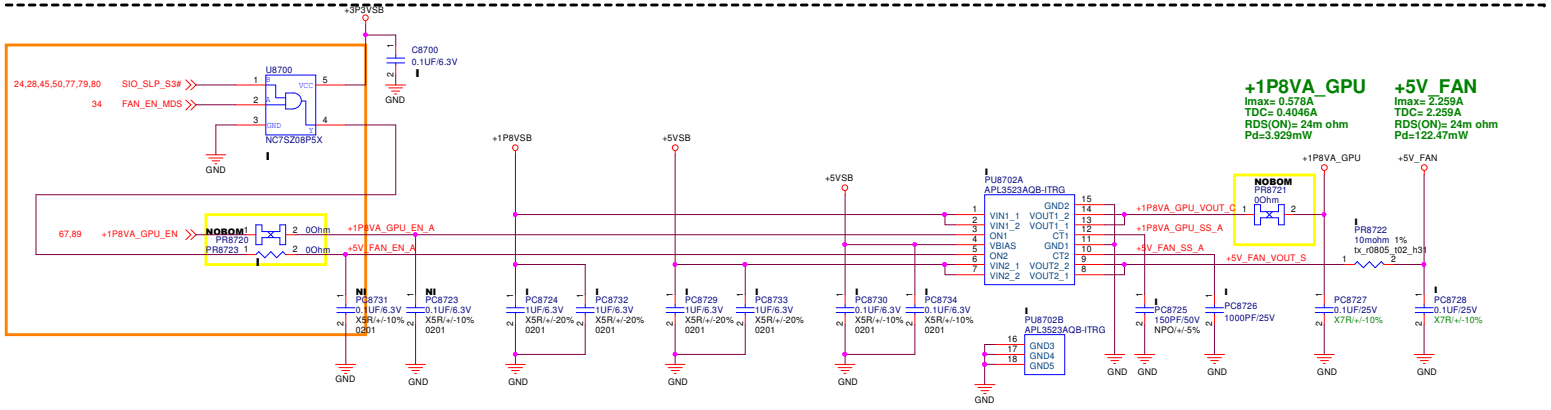
Size	Project Name	Rev
Custom	Vulcan	X00

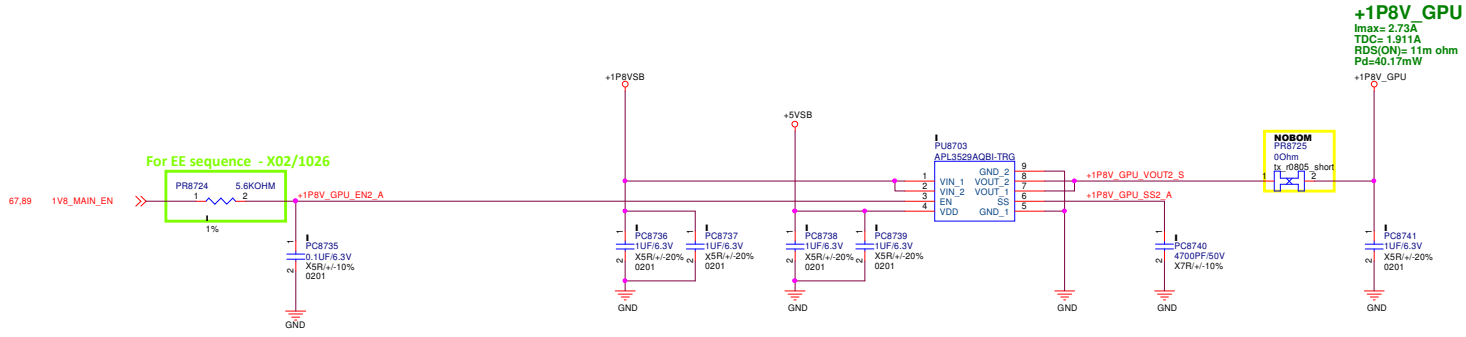
Date: Wednesday, November 28, 2018 Sheet 86 of 94



Owner	+1P0V_GPU	Low Limit	High limit
Atticus	4.0A	N/A	0.44uH @ 6A
Terry	4.0A	N/A	0.44uH @ 6A

※ OC point is based on peak inductor current





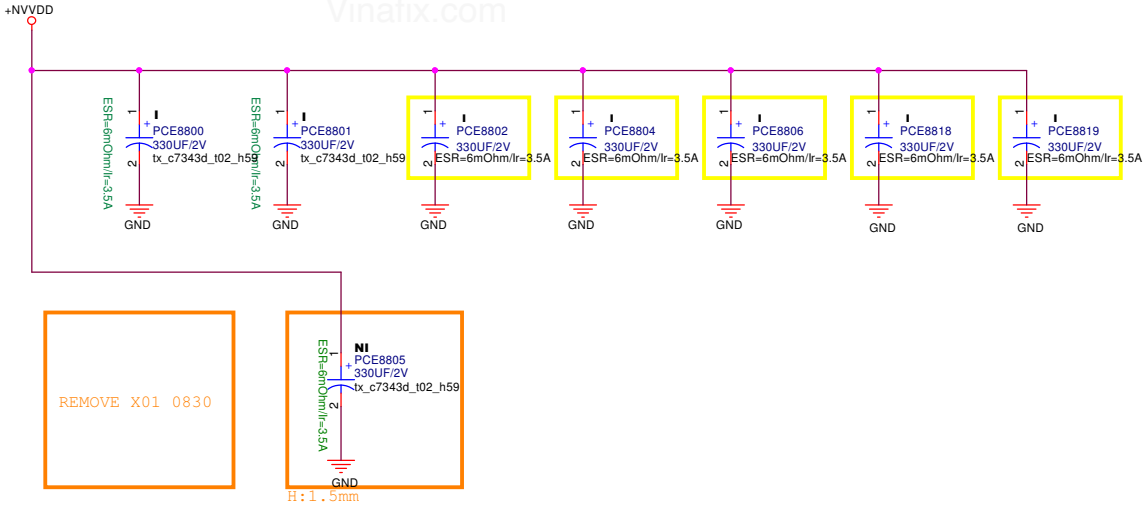
<Core Design>

PEGATRON Title : +1P0V_GPU/+1P8V_GPU & LDO

Pegatron Corp. Engineer: Chris_Tseng

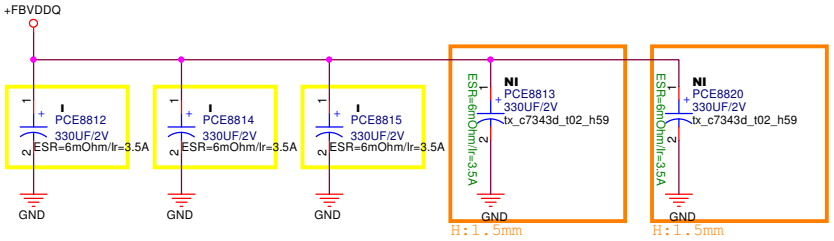
Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 87 of 94



+NVVDD Output CAP(w/ +NVVDDS)

330uF/2V/H=2mm * 7 (I)
330uF/2V/H=1.5mm * 2(NI)



+FBVDDQ Output CAP

330uF/2V/H=2mm * 3 (I)
330uF/2V/H=1.5mm * 2(NI)

<Core Design>

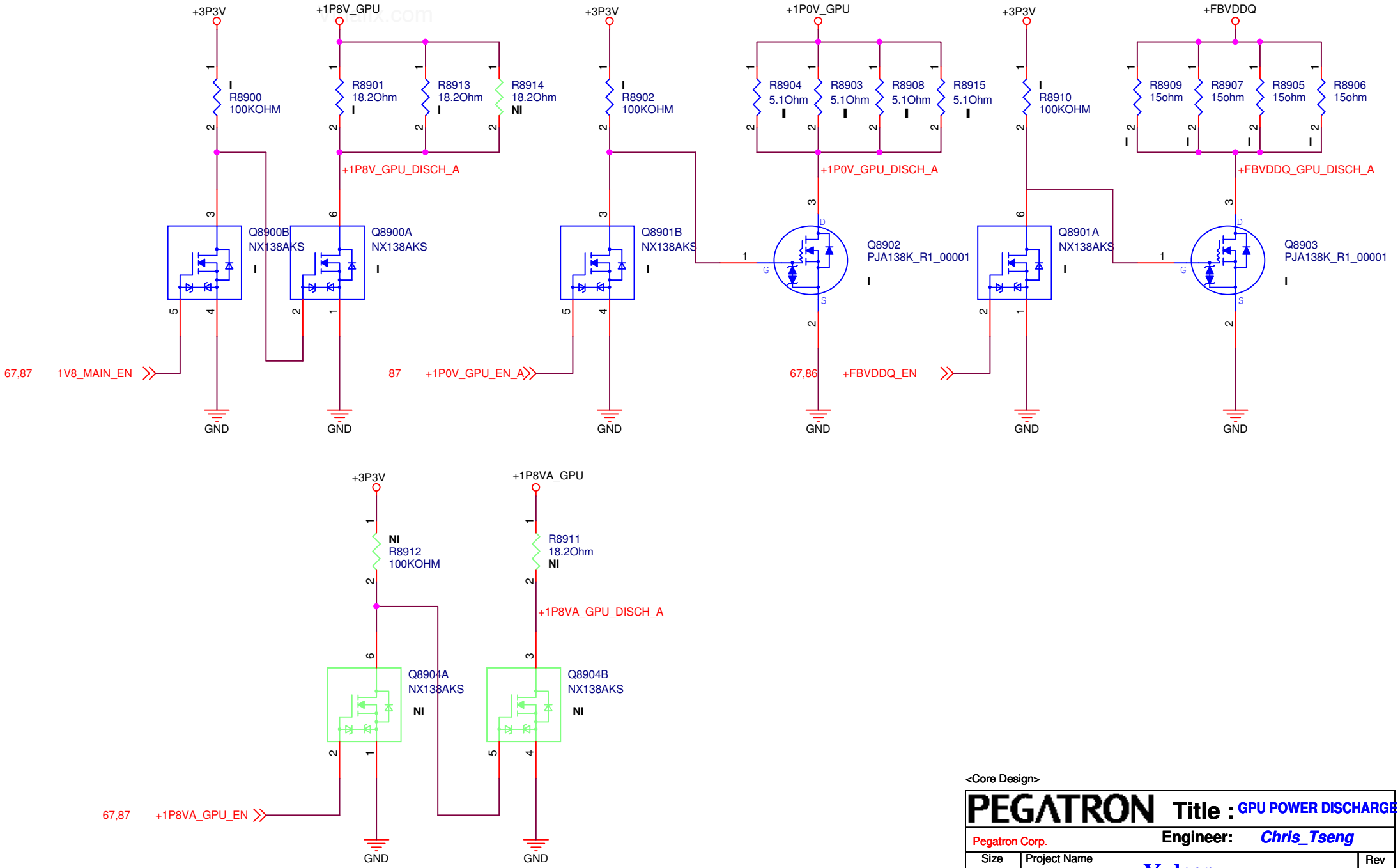
PEGATRON Title : GPU_POWER_CAP

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A3	Vulcan	X00

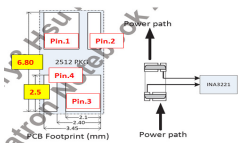
Date: Wednesday, November 28, 2018 Sheet 88 of 94

GPU POWER DISCHARGE



<Core Design>

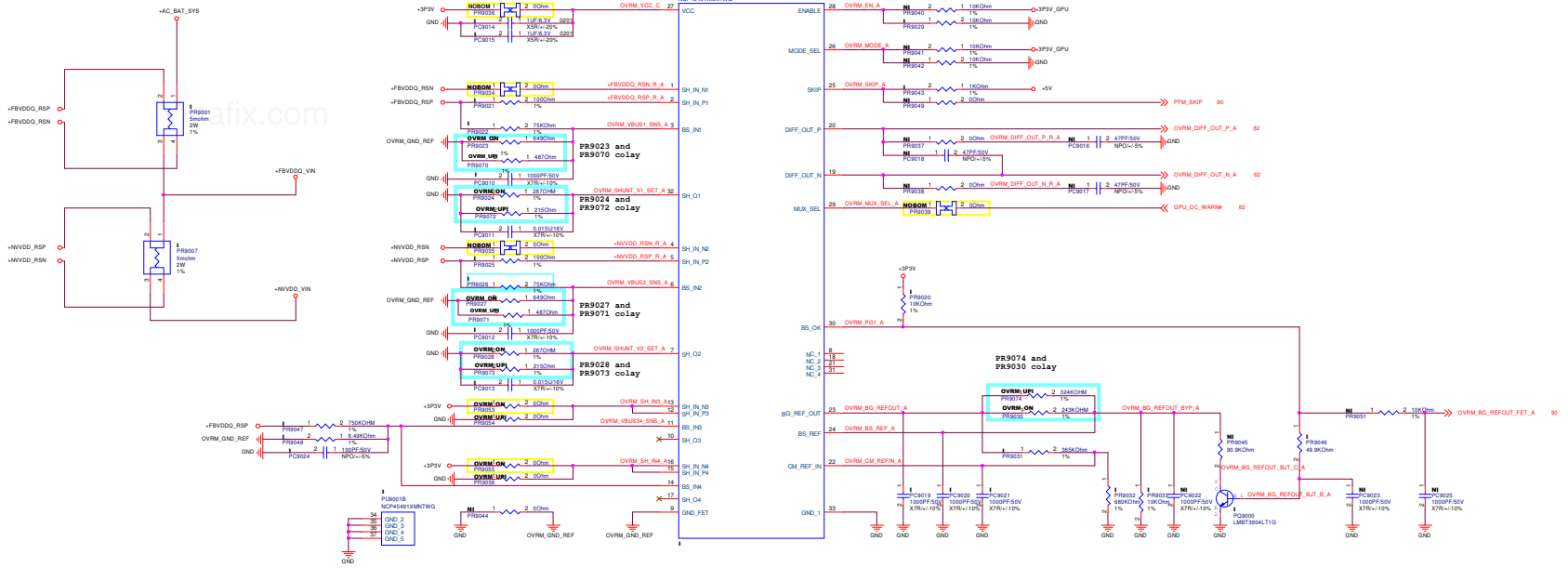
PEGATRON	Title : GPU POWER DISCHARGE	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: A4	Project Name: Vulcan	Rev: B00
Date: Wednesday, November 28, 2018	Sheet 89 of 94	



+AC_BAT_SYS (GPU power only)

Input Current: 12A @19V (1ms moving average)
Input Current: 10A @19V (5ms moving average)
Input Current : 4.21A @19V (1s movingi average)

Input Current: 25.33A @9V (1ms moving average)
Input Current: 21.11A @9V (5ms moving average)
Input Current : 8.89A @9V (1s movingi average)



Only change part number to
On-semi (06T89V004N00)

OnSemi		R954	R924	R977	R923	R950	R953	R952	C841	C836
		PR9023	PR9027	PR9024	PR9028	PR9030	PR9022	PR9026	PC9010	PC9012
N18E-G3 MAX-Q	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G2 MAX-Q	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G1 MAX-P	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G0 MAX-P	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF

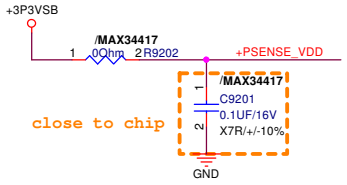
uPI		R954	R924	R977	R923	R950	R953	R952	C841	C836
		PR9070	PR9071	PR9072	PR9073	PR9074	PR9022	PR9026	PC9010	PC9012
N18E-G3 MAX-Q	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G2 MAX-Q	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G1 MAX-P	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G0 MAX-P	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF

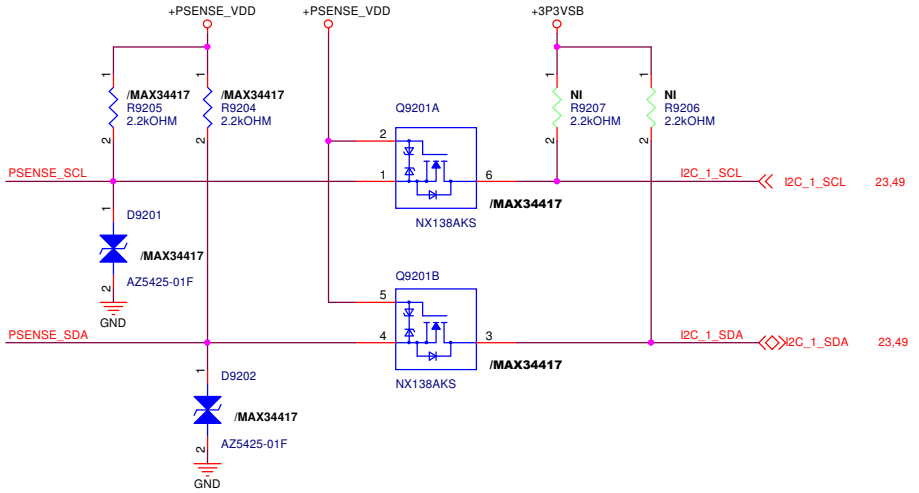
<Core Design>
PEGATRON Title : Power sense
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 60 of 98

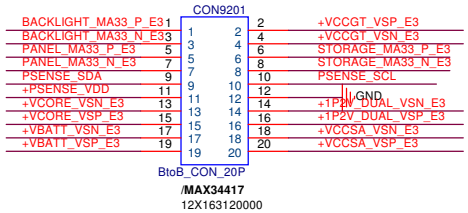
<Core Design>

PEGATRON	Title : RESERVE	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: A2	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 91 of 94	

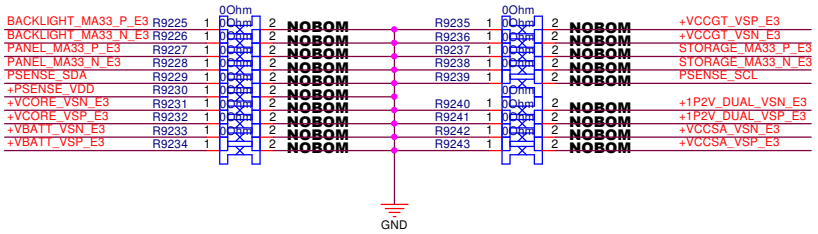
POWER SENSE







VCCGT		SSD/HDD				VDDQ		VCCSA	
2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19
PANEL Backlight		PANEL Logic				VCORE		Battery	



	Chip Channel	Connector pin	Item	Location	Sense Resistor	Note
Sensor 1 [10h]	1	P1+/-	CPU_VCCGT	PR7307 (10m ohm) PR7308 (10m ohm)	5m ohm (0x05)	VCCGT
	2	P2+/-	STORAGE	R3109 (10m ohm)	10m ohm (0x0A)	SSD
				R3216 (10m ohm)		HDD(SATA)
	3	P3+/-	DISPLAY_CTLR	R4852 (10m ohm)	10m ohm (0x0A)	Panel Logic
	4	P4+/-	DISPLAY_BACKLIGHT	R4800 (10m ohm)	10m ohm (0x0A)	Panel Backlight
Sensor 2 [1Eh]	1	P5+/-	STYSTEM	R6811 (5m ohm)	5m ohm (0x05)	Battery
	2	P6+/-	CPU_VCORE	PR7100 (10m ohm) PR7101 (10m ohm)	5m ohm (0x05)	VCORE
	3	P7+/-	CPU_VDDQ	PR7700 (10m ohm)	10m ohm (0x0A)	VDDQ
	4	P8+/-	CPU_VCCSA	PR7407 (10m ohm)	10m ohm (0x0A)	VCCSA

<Core Design>

PEGATRON Title : POWER SENSE MAX34417

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 92 of 94

<Core Design>

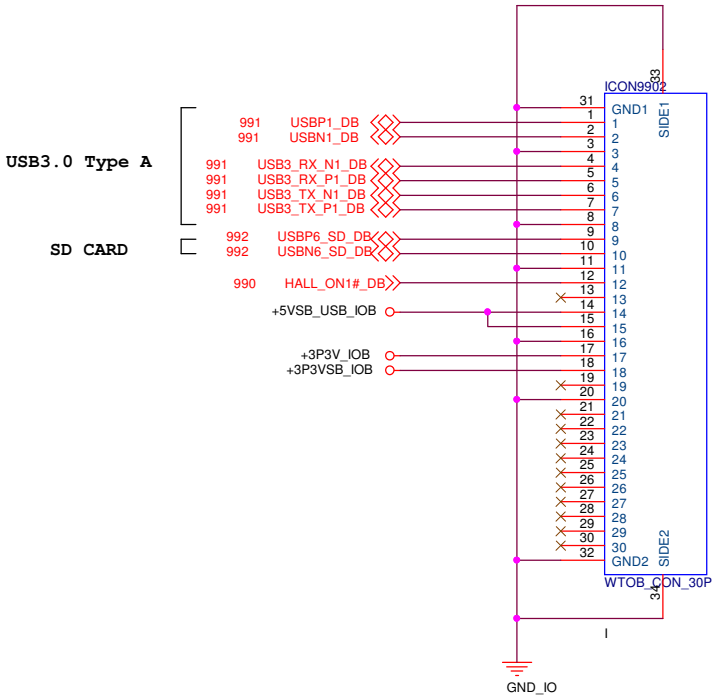
PEGATRON Title : RESERVE

Pegatron Corp. Engineer: Chris_Tseng

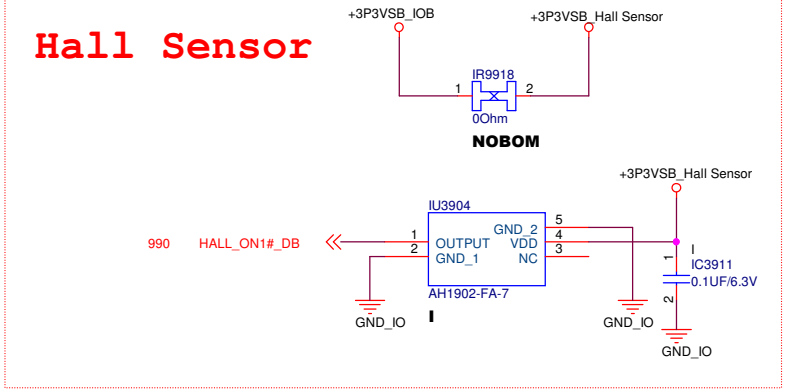
Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 94 of 94

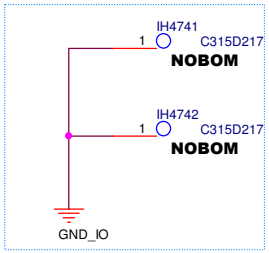
990.IO port/Hall sensor



Hall Sensor



Screw Hole



<Core Design>

PEGATRON Title : IO port/Hall sensor

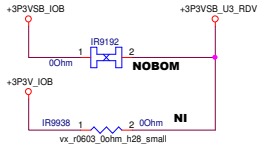
Pegatron Corp. Engineer: Alex_Tsai

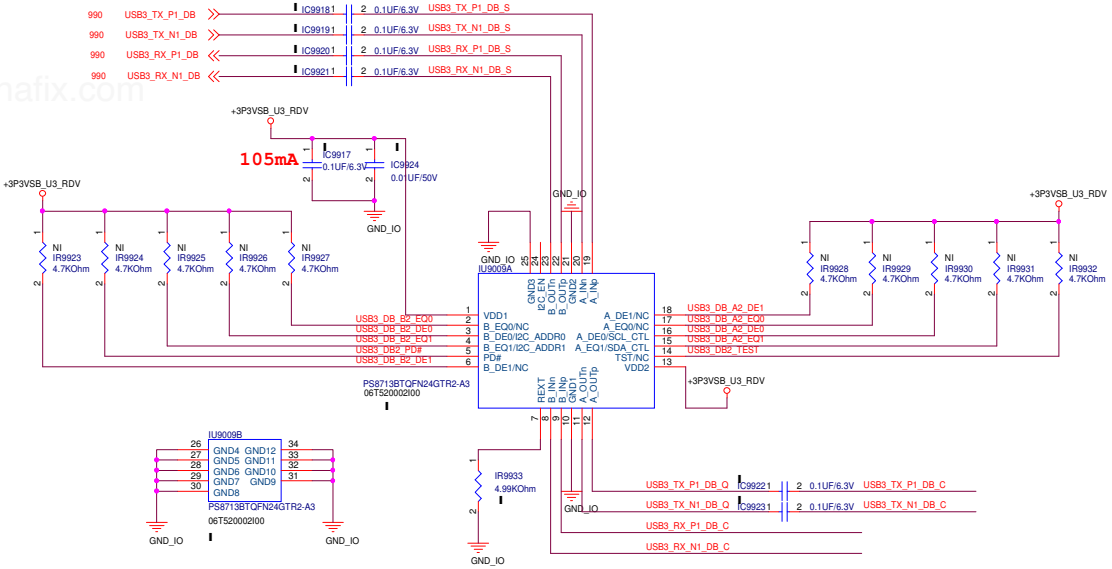
Size	Project Name	Rev
B	Vulcan	X00

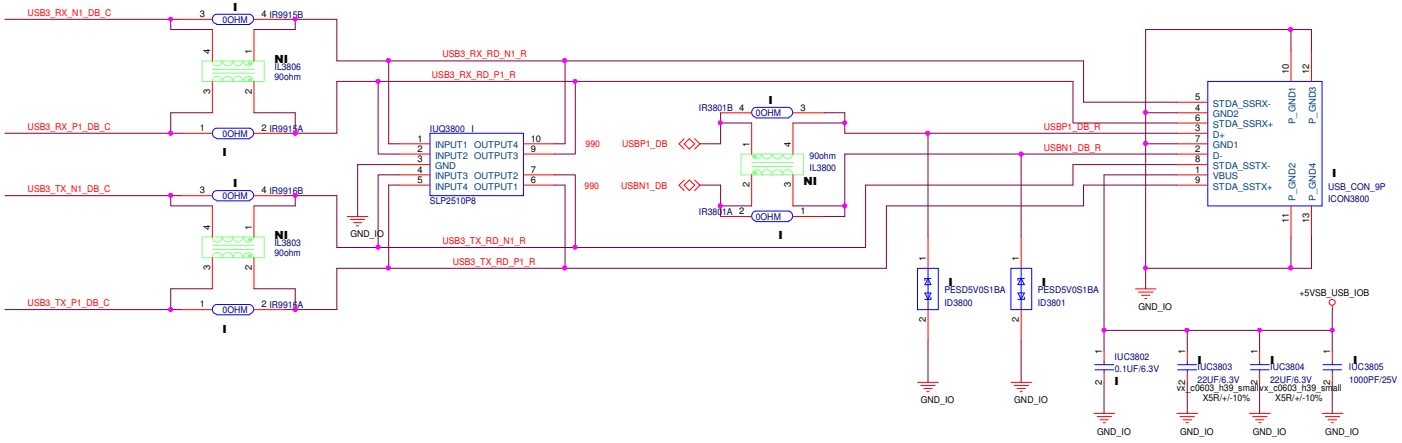
Date: Wednesday, November 28, 2018 Sheet 990 of 94

991.USB PORT

Imax: 105mA







<Core Design>

PEGATRON Title : USB DB PORT

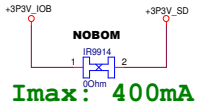
Pegatron Corp. Engineer: Alex_Tsai

Size	Project Name	Rev
C	Vulcan	X00

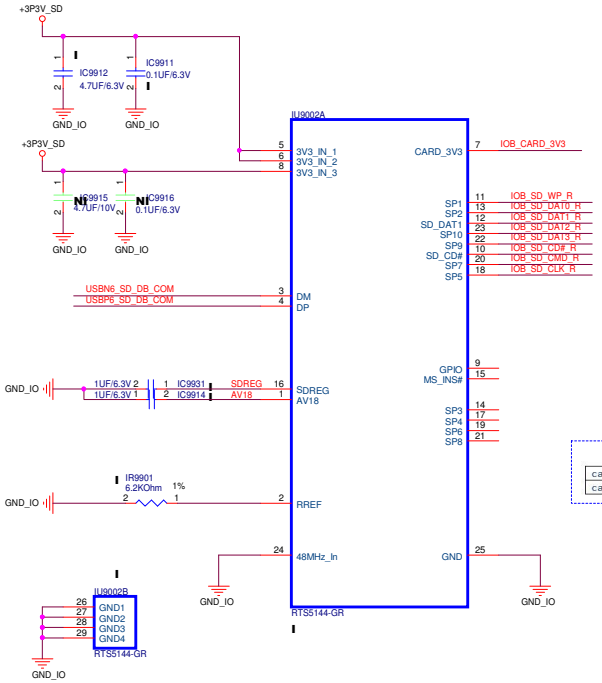
Date: Wednesday, November 28, 2018 Sheet 991 of 94

992.Card_reader_RTS5144-GR

POWER

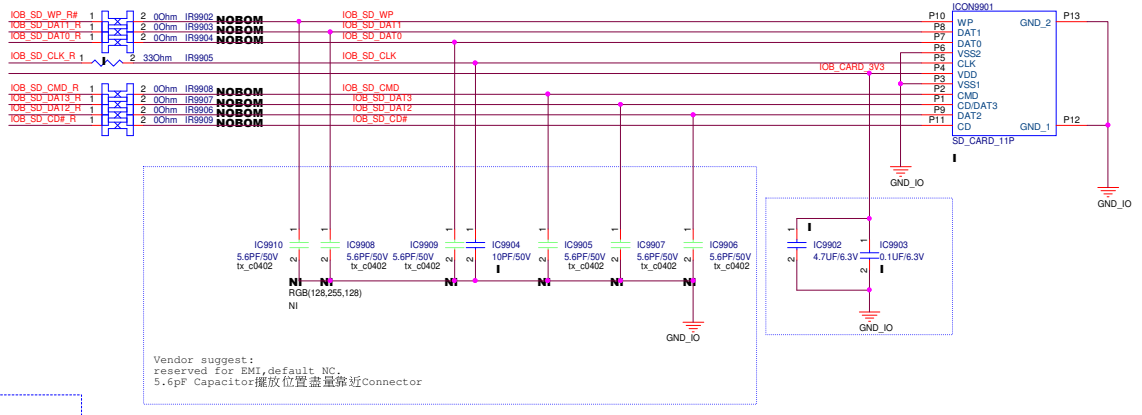


Imax: 400mA

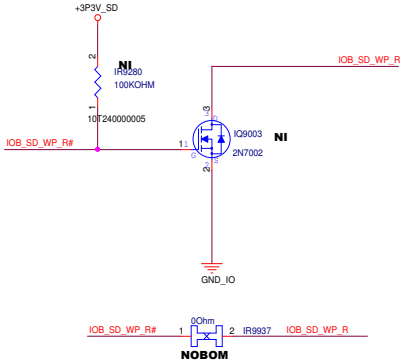


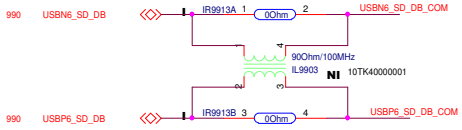
WITHOUT CARD	CARD INSERTED:LOCK	CARD INSERTED:UNLOCK
W/P GND	W/P GND	W/P GND
C/D VSS1 P3	C/D VSS1 P3	C/D VSS1 P3

card lock	SD_WP pin high
card unlock	SD_WP pin low



Vendor suggest:
reserved for EMI,default NC.
5.6pF Capacitor擺放位置盡量靠近Connector





<Core Design>

PEGATRON Title : Card_reader_RTS5144GR

Pegatron Corp. Engineer: Alex_Tsai

Size	Project Name	Rev
C	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 992 of 94