COMPAL CONFIDENTIAL

MODEL NAME : Loki 15/17

PCB NO : DA8001BS000

BOM P/N : 431A7Y31L01

KBL-U+MEC1416 board

2017-07-18

REV : 1.0 (A00)

PCB R1

ZZZ

DA8001BS000

PCB@

PCB 21C LA-F115P REV0 M/B 3

PCB R3

ZZZ

DAZ21C00101

PCB_R3@

PCB CAL50 LA-F115P LS-F111P GOLD A31 !

KBL R1

UC1

SA0000AWC0L

i7KBLR_1.8G_QS@

S IC A31 FJ8067703281816 QNBF Y0 1.8G

UC1

SA0000A370L

i5KBLU_2.5G_R1@

S IC FJ8067702739739 SR2ZU H0 2.5G A31!

UC1

SA0000AWB1L

i5KBLR_1.6G_QS@

S IC A31 FJ8067703282221 QNEG Y0 1.6G

UC1

SA0000AQZ0L

i7KBLR_1.8G_ES@

S IC A31 FJ8067703281813 QN5C Y0 1.8G

UC1

SA0000A344L

i7KBLU_2.7G@

S IC FJ8067702739740 SR2ZV H0 2.7G A31!

UC1

SA0000ACL0L

i3SKL_2.0G_SMB0@

S IC FJ8066201931106 SR2UW D1 2G A31!

KBL R3

UC1

SA0000AWC2L

i7KBLR_R3@

S IC FJ8067703281816 SR3LC Y0 1.8G A31!

UC1

SA0000AWB3L

i5KBLR_R3@

S IC FJ8067703282221 SR3LB Y0 1.6G A31!

UC1

SA0000B2Y1L

i3KBLU_R3@

S IC FJ8067702739765 SR3JY H0 2.7G A31!

UC1

SA0000ADV3L

KBLU_Pentium_R3@

S IC FJ8067702739932 SR348 H0 2.3G A31!

UC1

SA0000ADL3L

KBLU_Celeron_R3@

S IC FJ8067702739933 SR349 H0 1.8G A31!

UC1

SA0000ACL1L

i3SKL_SMB0_R3@

S IC FJ8066201931106 SR2UW D1 2G A31!

UC1

SA0000B2Y0L

i3KBLU_R1@

UC1

SA0000A374L

i5KBLU_R3@

UC1

SA0000AWS0L

i5KNLR_R1@

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
U22@/U42@ : KBL U/KBL U-R
SKL@/KBL@:SKL/KBL
EC@ : EC
JP@/PJP@ : JUMP
EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
TYPEC@EMI@/TYPEC@ESD@/TYPEC@RF@:EMI, ESD ,RFTYPEC Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
MMC@ : eMMC
FFS@ : Free Fall Sensor
TYPEC@ : typeC
DSX@ : Deep sleep
FP@:Finger Printer
M2_50@ : GPU R17M_2_50
2G@/2G_H@/2G_S@/2G_M@ : VRAM type
4G@/4G_H@/4G_S@/4G_M@ : VRAM type

LOKI@:Loki only
LOKI@EMI@/LOKI@ESD@:EMI/ESD LOKI Component
ODD@:ODD Component
LOKI@TYPEC@ : typeC
GEN8@:RTC GEN8
FTPM@:SW TPM

MAD@:LokiL only
MAD@RF@:RF MAD Component
GEN9@:RTC GEN9
TPM@:HW TPM

PCB R1

ZZZ

DA8001FO000

PCB_R1_X32@

PCB 21C LA-F116P REV0 M/B 3

UC1

SA0000BVB0L

i3KBLU_23e@

S IC A31 FH8067703037315 QNMU J1 2.3G

UC1

SA0000BVB1L

i3KBLU_23e_R3@

S IC FH8067703037315 SR3N6 J1 2.3G A31!

Layout Dell logo

REV: X00
PWB: 9HTP8

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Issued Date	2016/12/01	Deciphered Date	2017/12/01

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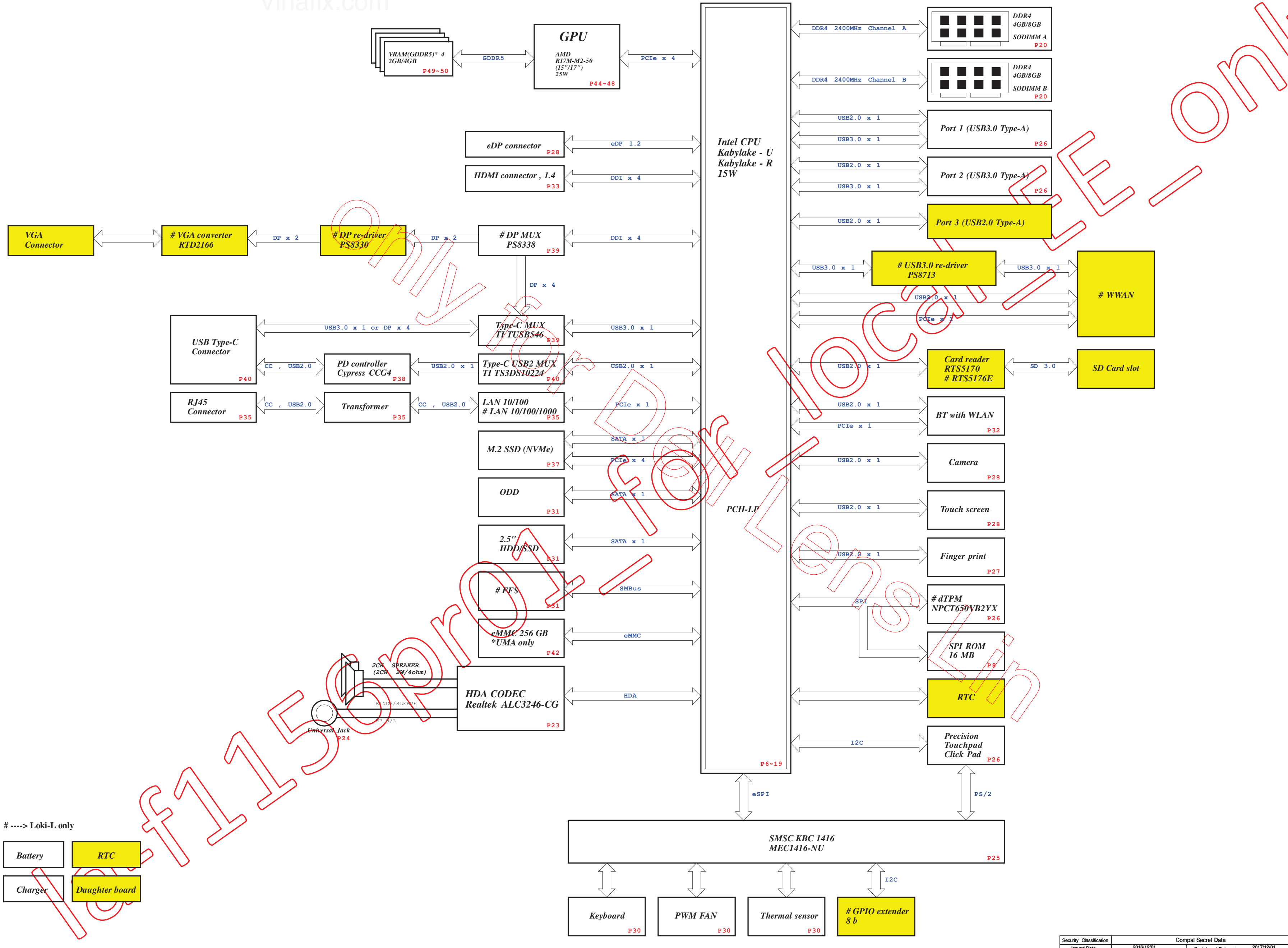
Title: Cover Page

Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 1 of 65

Loki/Loki-L Block Diagram



VRAM(GDDR5)* 4 2GB/4GB P49~50
GDDR5
GPU AMD R17M-M2-50 (15"/17") 25W P44~48
PCIe x 4
DDR4 2400MHz Channel A
DDR4 4GB/8GB SODIMM A P20
DDR4 2400MHz Channel B
DDR4 4GB/8GB SODIMM B P20
eDP connector P28
eDP 1.2
HDMI connector , 1.4 P33
DDI x 4
Intel CPU Kabylake - U Kabylake - R 15W
USB2.0 x 1
USB3.0 x 1
Port 1 (USB3.0 Type-A) P26
Port 2 (USB3.0 Type-A) P26
Port 3 (USB2.0 Type-A)
VGA Connector
VGA converter RTD2166
DP x 2
DP re-driver PS8330
DP MUX PS8338 P39
DP x 4
USB3.0 re-driver PS8713
WWAN
PCIe x 1
USB Type-C Connector P40
USB3.0 x 1 or DP x 4
Type-C MUX TI TUSB546 P39
CC , USB2.0
PD controller Cypress CCG4 P38
Type-C USB2 MUX TI TS3DS10224 P40
Card reader RTS5170 # RTS5176E
SD 3.0
SD Card slot
RJ45 Connector P35
Transformer P35
LAN 10/100 # LAN 10/100/1000 P35
BT with WLAN P32
M.2 SSD (NVMe) P37
SATA x 1
PCIe x 4
Camera P28
ODD P31
PCH-LP
Touch screen P28
2.5" HDD/SSD P31
Finger print P27
FFS P31
SMBus
SPI
dTPM NPCT650VB2YX P26
eMMC 256 GB *UMA only P42
eMMC
SPI ROM 16 MB P8
2CH SPEAKER (2CH 2W/4ohm)
HDA CODEC Realtek ALC3246-CG P23
HDA
RTC
Universal Jack P24
I2C
Precision Touchpad Click Pad P26
P6~19
eSPI
PS/2
SMSC KBC 1416 MEC1416-NU P25
Keyboard P30
PWM FAN P30
Thermal sensor P30
GPIO extender 8 b
----> Loki-L only
Battery
RTC
Charger
Daughter board

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Issued Date 2016/12/01	Deciphered Date 2017/12/01		Title: Block Diagram
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			Date: Friday, March 02, 2018 Sheet 2 of 65

POWER STATES

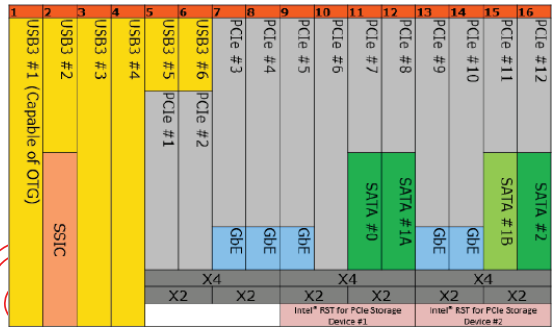
Signal / State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	LOW	HIGH	HIGH	ON	ON	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	DS3	S4/S5	M3
+SDC_IN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+1.0V_PRIM	System +1.0V power rail	ON	ON	OFF	ON*	ON
+1.0VS_VCCIO	+1.0VS IO power rail	ON	OFF	OFF	OFF	OFF
+1.0V_MPHYPLL	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	OFF	ON/OFF	ON
+0.95VSDGPU	+0.9VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.35V_MEM_GFX	+1.35VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF	ON
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	OFF	ON*	ON
+1.8VS	System +1.8VS power rail	ON	OFF	OFF	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3.3V_ALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	OFF	ON*	ON
+3VS	System +3VS power rail	ON	OFF	OFF	OFF	ON
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	OFF	OFF	OFF	ON
+RTC_CELL	RTC power	ON	ON	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

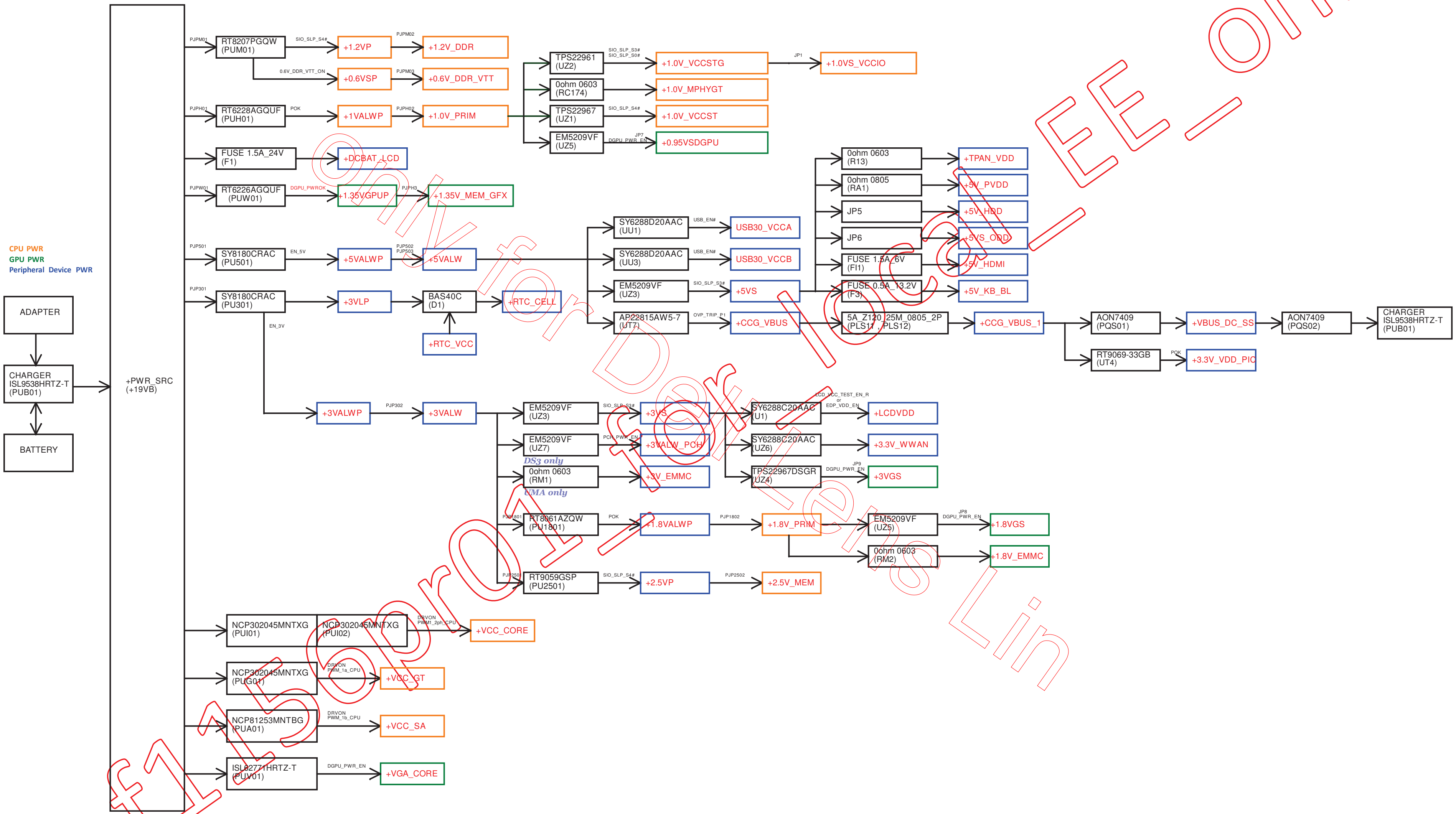


USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 port3 , IO/B
3	USB2.0 Port2
4	TypeC
5	Camera
6	Card reader , IO/B
7	BT
8	Touch screen
9	Finger printer
10	WWAN , IO/B

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 port1
USB3.0-2			WWAN , IO/B
USB3.0-3			USB3.0 port2
USB3.0-4			TypeC
USB3.0-5	PCIE-1		GPU
USB3.0-6	PCIE-2		GPU
	PCIE-3		GPU
	PCIE-4		GPU
	PCIE-5		10/100 LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

Board ID & Model ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT
2	100	13.7	2.902	
3	100	17.8	2.801	DVT1
4	100	22.1	2.703	
5	100	27.0	2.598	DVT2
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	Pilot
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	


CPU PWR
GPU PWR
Peripheral Device PWR
ADAPTER
CHARGER ISL9538HRTZ-T (PUB01)
BATTERY
+PWR_SRC (+19VB)
RT8207PGQW (PUM01)
SIO_SLP_S4#
+1.2VP
PJPM02
+1.2V_DDR
0.6V_DDR_VTT_ON
+0.6VSP
PJPM03
+0.6V_DDR_VTT
RT6228AGQUF (PUH01)
POK
+1VALWP
PJPH02
+1.0V_PRIM
TPS22961 (UZ2)
SIO_SLP_S3#
SIO_SLP_S0#
+1.0V_VCCSTG
JP1
+1.0VS_VCCIO
0ohm 0603 (RC174)
+1.0V_MPHYGT
TPS22967 (UZ1)
SIO_SLP_S4#
+1.0V_VCCST
EM5209VF (UZ5)
JP7
DGPU_PWR_EN
+0.95VSDGPU
FUSE 1.5A_24V (F1)
+DCBAT_LCD
RT6226AGQUF (PUW01)
DGPU_PWROK
+1.35VGPUP
PJPH3
+1.35V_MEM_GFX
SY8180CRAC (PU501)
EN_5V
+5VALWP
PJP502
PJP503
+5VALW
SY6288D20AAC (UU1)
USB_EN#
USB30_VCCA
SY6288D20AAC (UU3)
USB_EN#
USB30_VCCB
EM5209VF (UZ3)
SIO_SLP_S3#
+5VS
AP22815AW5-7 (UT7)
OVP_TRIP_P1
+CCG_VBUS
0ohm 0603 (R13)
+TPAN_VDD
0ohm 0805 (RA1)
+5V_PVDD
JP5
+5V_HDD
JP6
+5VS_ODD
FUSE 1.5A_6V (FI1)
+5V_HDMI
FUSE 0.5A_13.2V (F3)
+5V_KB_BL
5A_Z120_25M_0805_2P (PLS11, PLS12)
+CCG_VBUS_1
AON7409 (PQS01)
+VBUS_DC_SS
AON7409 (PQS02)
CHARGER ISL9538HRTZ-T (PUB01)
RT9069-33GB (UT4)
POK
+3.3V_VDD_PIC
SY8180CRAC (PU301)
+3VLP
BAS40C (D1)
+RTC_CELL
+RTC_VCC
EN_3V
+3VALWP
PJP302
+3VALW
EM5209VF (UZ3)
SIO_SLP_S3#
+3VS
SY6288C20AAC (U1)
LCD_VCC_TEST_EN_R or EDP_VDD_EN
+LCDVDD
EM5209VF (UZ7)
PCH_PWR_EN
+3VALW_PCH
SY6288C20AAC (U6)
+3.3V_WWAN
DS3 only
0ohm 0603 (RM1)
+3V_EMMC
UMA only
TPS22967DSGR (UZ4)
JP9
DGPU_PWR_EN
+3VGS
RT8061AZQW (PU1801)
POK
+1.8VALWP
PJP1802
+1.8V_PRIM
EM5209VF (UZ5)
JP8
DGPU_PWR_EN
+1.8VGS
0ohm 0603 (RM2)
+1.8V_EMMC
RT9059GSP (PU2501)
SIO_SLP_S4#
+2.5VP
PJP2502
+2.5V_MEM
NCP302045MNTXG (PUI01)
NCP302045MNTXG (PUI02)
DRVON
PWM_2ph_CPU
+VCC_CORE
NCP302045MNTXG (PUG01)
DRVON
PWM_1a_CPU
+VCC_GT
NCP81253MNTBG (PUA01)
DRVON
PWM_1b_CPU
+VCC_SA
ISL62771HRTZ-T (PUV01)
DGPU_PWR_EN
+VGA_CORE

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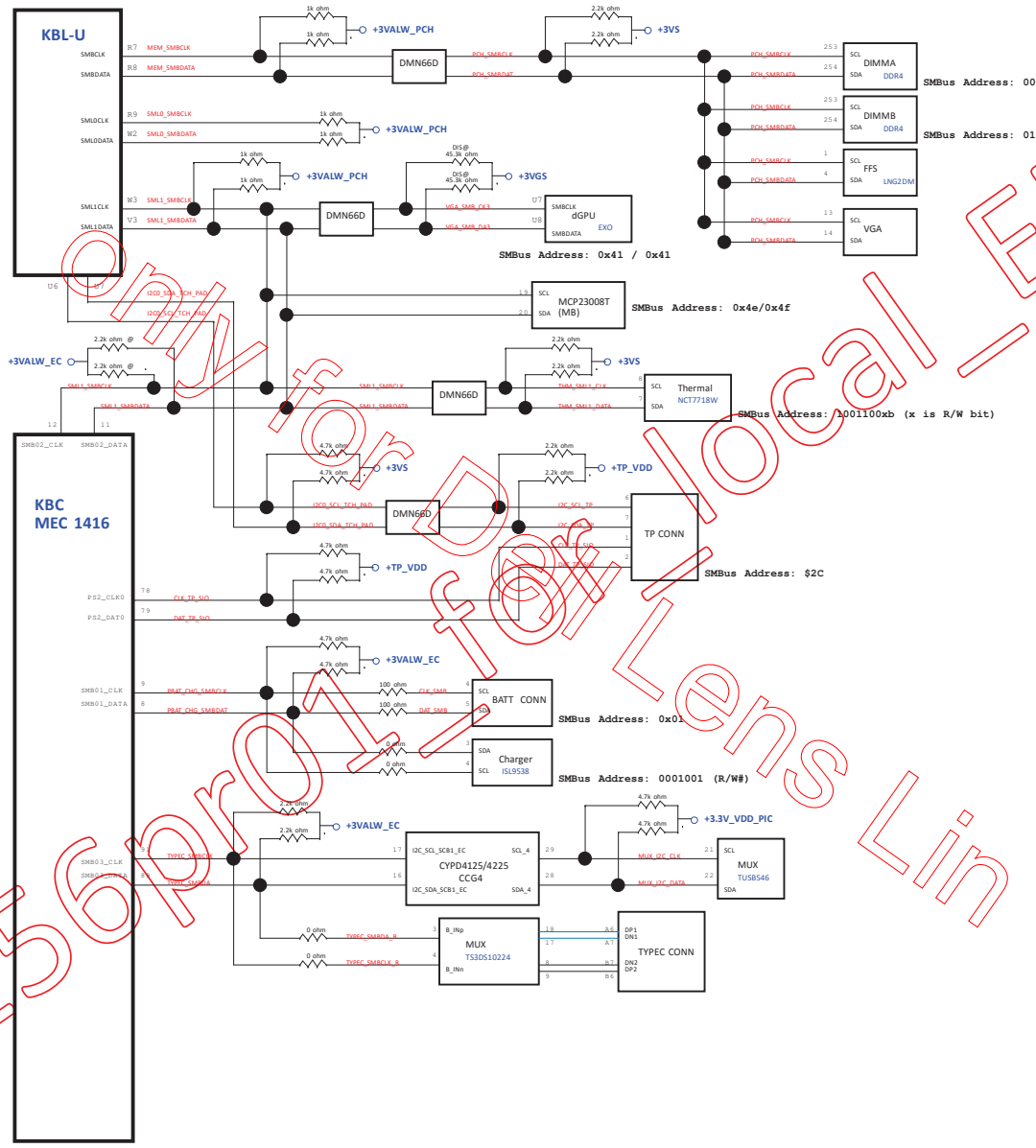
Title: Power Rail

Size | Document Number: LA-F115P | Rev 0.1



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.	
Title	SMBus Block Diagram
Size	Document Number: LA-F115P
Rev	0.1
Date: Friday, March 02, 2018	Sheet 5 of 85

Main Func = CPU

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

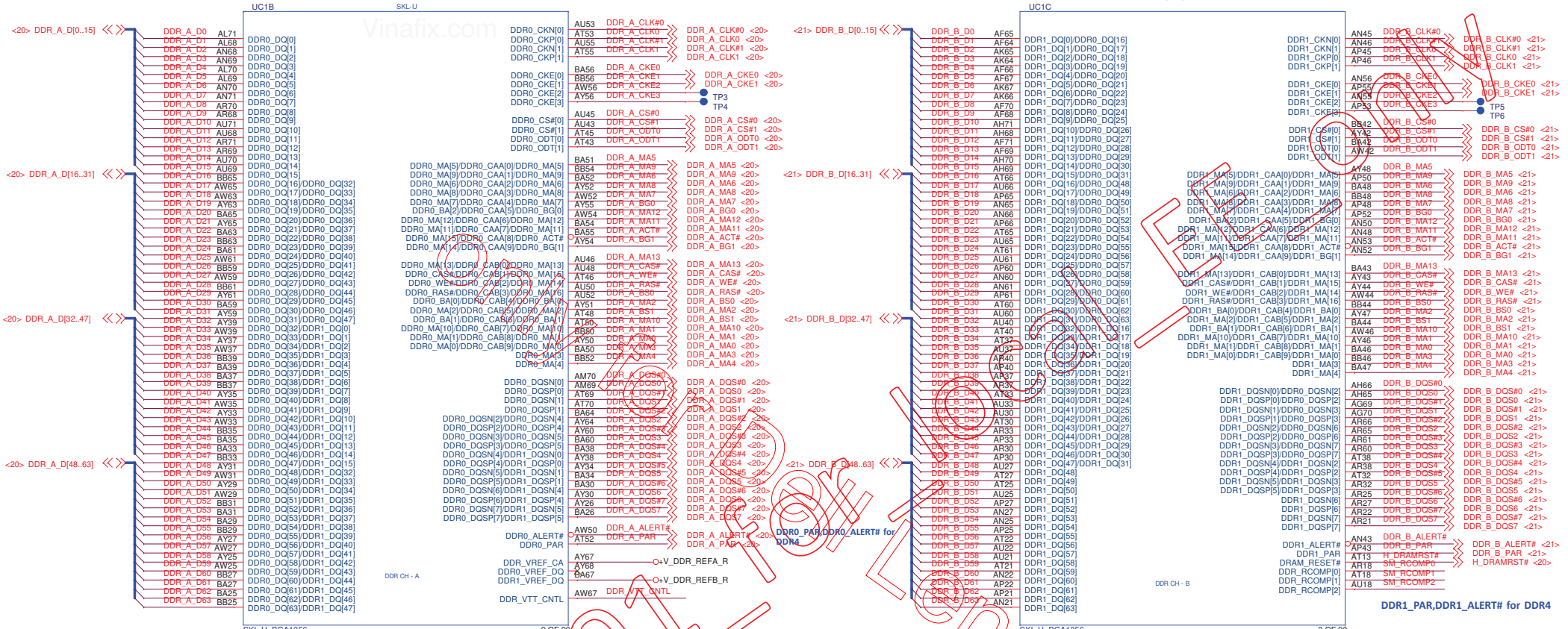
Title: MCP(1/14)DDI,EDP,CSI2,EMMC

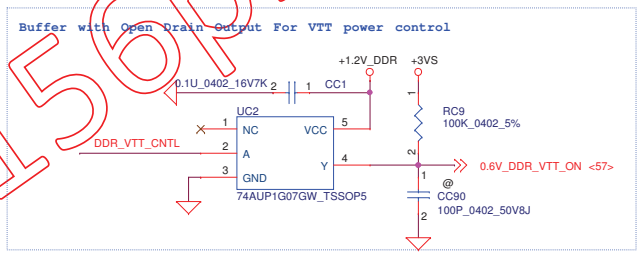
Size	Document Number	Rev
	LA-F115P	0.1

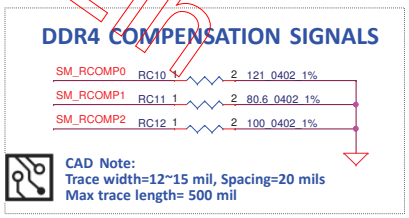
Date: Friday, March 02, 2018 Sheet 6 of 65

Main Func = CPU

DDR4 Interleaved Memory



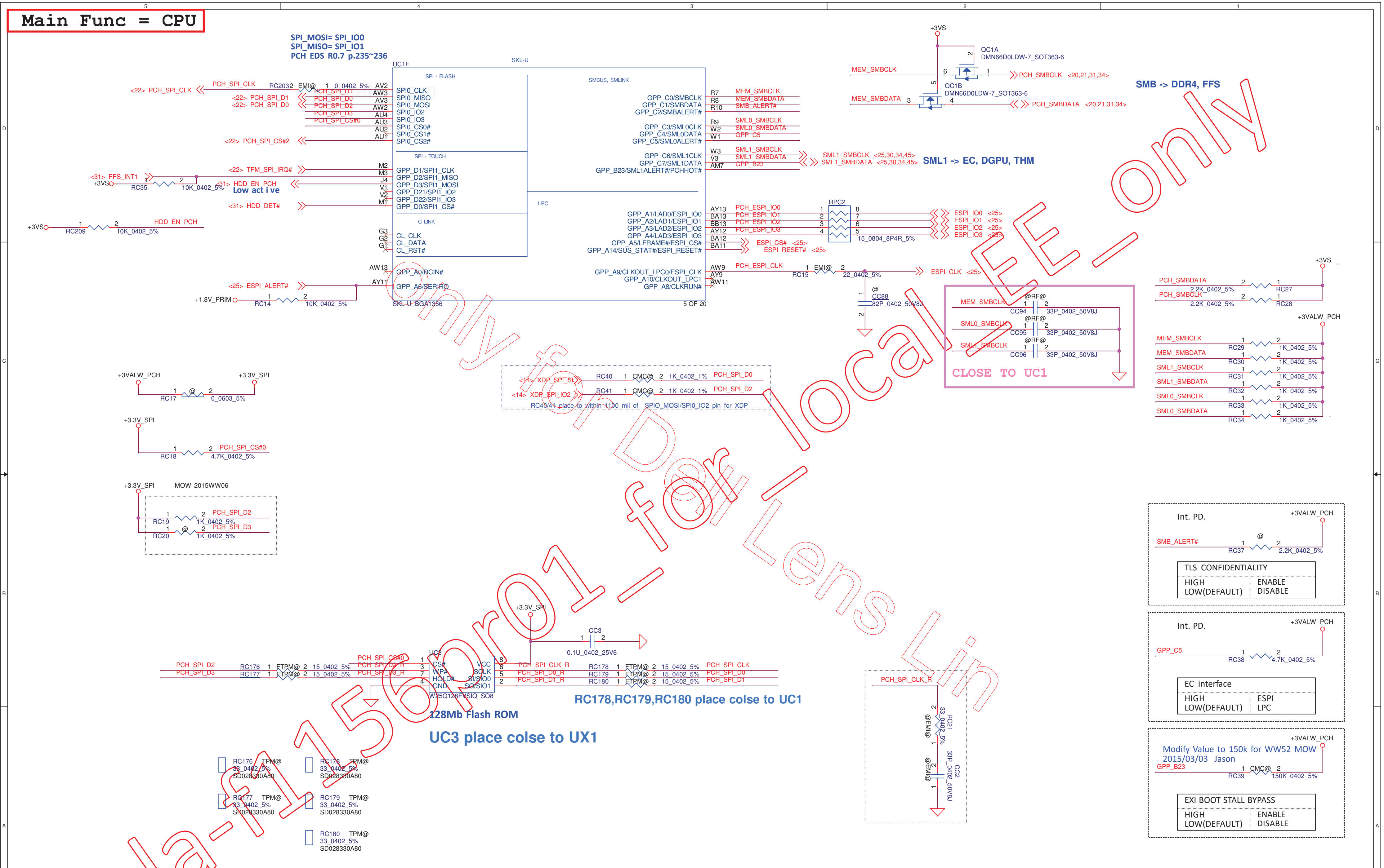




Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MCP(2/14)DDR4		
Size	Document Number	LA-F115P	Rev 0.1
Date:	Friday, March 02, 2018	Sheet 7 of 65	

Main Func = CPU



SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236
UC1E
SKL-U
SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#
C LINK
CL_CLK
CL_DATA
CL_RST#
GPP_A0/RCIN#
GPP_A6/SERIRQ
SKL-U_BGA1356
5 OF 20
SMBUS, SMLINK
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
LPC
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#
<22> PCH_SPI_CLK
<22> PCH_SPI_D1
<22> PCH_SPI_D0
<22> PCH_SPI_CS#2
<22> TPM_SPI_IRQ#
<31> FFS_INT1
<31> HDD_EN_PCH
Low active
<31> HDD_DET#
<25> ESPI_ALERT#
HDD_EN_PCH
RC2032 EMI@ 0_0402_5%
RC35 10K_0402_5%
RC209 10K_0402_5%
RC14 10K_0402_5%
+3VS
+1.8V_PRIM
QC1A DMN66D0LDW-7_SOT363-6
QC1B DMN66D0LDW-7_SOT363-6
MEM_SMBCLK
MEM_SMBDATA
PCH_SMBCLK <20,21,31,34>
PCH_SMBDATA <20,21,31,34>
SMB -> DDR4, FFS
SML1_SMBCLK <25,30,34,45>
SML1_SMBDATA <25,30,34,45>
SML1 -> EC, DGPU, THM
RPC2 15_0804_8P4R_5%
ESPI_IO0 <25>
ESPI_IO1 <25>
ESPI_IO2 <25>
ESPI_IO3 <25>
ESPI_CS# <25>
ESPI_RESET# <25>
RC15 EMI@ 22_0402_5%
ESPI_CLK <25>
CC88 82P_0402_50V8J
CC94 @RF@ 33P_0402_50V8J
CC95 @RF@ 33P_0402_50V8J
CC96 @RF@ 33P_0402_50V8J
CLOSE TO UC1
RC27 2.2K_0402_5%
RC28 2.2K_0402_5%
+3VALW_PCH
RC29 1K_0402_5%
RC30 1K_0402_5%
RC31 1K_0402_5%
RC32 1K_0402_5%
RC33 1K_0402_5%
RC34 1K_0402_5%
<14> XDP_SPI_SI
<14> XDP_SPI_IO2
RC40 CMC@ 1K_0402_1% PCH_SPI_D0
RC41 CMC@ 1K_0402_1% PCH_SPI_D2
RC40/41 place to within 1100 mil of SPIO_MOSI/SPI0_IO2 pin for XDP
+3VALW_PCH
+3.3V_SPI
RC17 @ 0_0603_5%
RC18 4.7K_0402_5% PCH_SPI_CS#0
MOW 2015WW06
RC19 1K_0402_5% PCH_SPI_D2
RC20 @ 1K_0402_5% PCH_SPI_D3
CC3 0.1U_0402_25V6
UC3 W25Q128FVSIQ_SO8
CS# VCC WP# SCLK HOLD# SI/SIO0 GND SO/SIO1
RC176 ETPM@ 15_0402_5%
RC177 ETPM@ 15_0402_5%
RC178 ETPM@ 15_0402_5%
RC179 ETPM@ 15_0402_5%
RC180 ETPM@ 15_0402_5%
128Mb Flash ROM
UC3 place colse to UX1
RC178,RC179,RC180 place colse to UC1
RC176 TPM@ 33_0402_5% SD028330A80
RC177 TPM@ 33_0402_5% SD028330A80
RC178 TPM@ 33_0402_5% SD028330A80
RC179 TPM@ 33_0402_5% SD028330A80
RC180 TPM@ 33_0402_5% SD028330A80
PCH_SPI_CLK_R
RC21 @EMI@ 33_0402_5%
CC2 @EMI@ 33P_0402_50V8J
Int. PD.
SMB_ALERT#
RC37 @ 2.2K_0402_5%
TLS CONFIDENTIALITY
HIGH ENABLE
LOW(DEFAULT) DISABLE
Int. PD.
GPP_C5
RC38 4.7K_0402_5%
EC interface
HIGH ESPI
LOW(DEFAULT) LPC
Modify Value to 150k for WW52 MOW
2015/03/03 Jason
GPP_B23
RC39 CMC@ 150K_0402_5%
EXI BOOT STALL BYPASS
HIGH ENABLE
LOW(DEFAULT) DISABLE

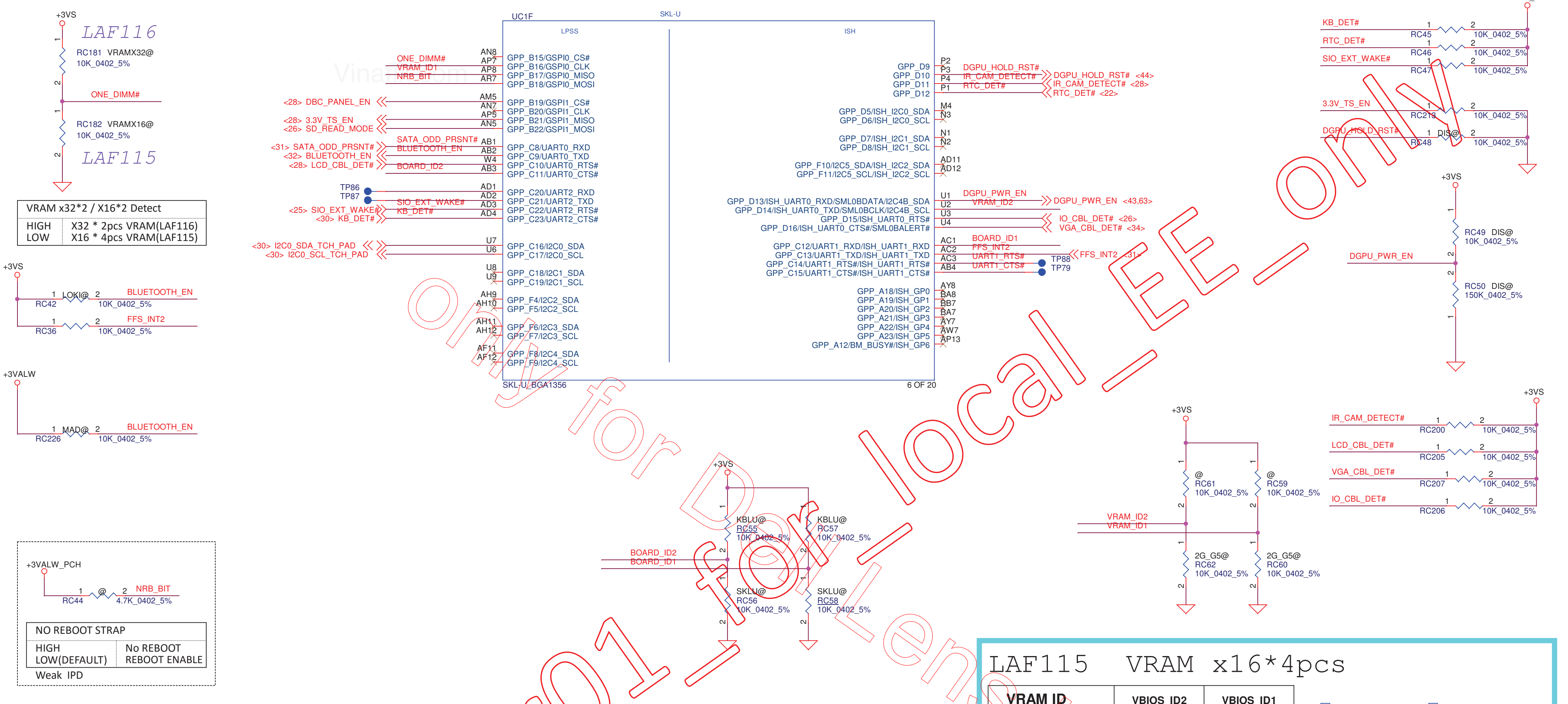
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **MCP(3/14)SPI,SMB,LPC**

Size | Document Number: **LA-F115P** | Rev 0.1

Main Func = CPU



+3VS
LAF116
RC181 VRAMX32@ 10K_0402_5%
ONE_DIMM#
RC182 VRAMX16@ 10K_0402_5%
LAF115
UC1F
SKL-U
LPSS
ISH
GPP_B15/GSPI0_CS#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_F4/I2C2_SDA
GPP_F5/I2C2_SCL
GPP_F6/I2C3_SDA
GPP_F7/I2C3_SCL
GPP_F8/I2C4_SDA
GPP_F9/I2C4_SCL
SKL-U_BGA1356
6 OF 20
GPP_D9
GPP_D10
GPP_D11
GPP_D12
GPP_D5/ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL
GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL
GPP_F10/I2C5_SDA/ISH_I2C2_SDA
GPP_F11/I2C5_SCL/ISH_I2C2_SCL
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
GPP_D15/ISH_UART0_RTS#
GPP_D16/ISH_UART0_CTS#/SML0BALERT#
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
GPP_A12/BM_BUSY#/ISH_GP6
ONE_DIMM#
VRAM_ID1
NRB_BIT
<28> DBC_PANEL_EN
<28> 3.3V_TS_EN
<26> SD_READ_MODE
<31> SATA_ODD_PRSNT#
<32> BLUETOOTH_EN
<28> LCD_CBL_DET#
BOARD_ID2
TP86
TP87
SIO_EXT_WAKE#
KB_DET#
<25> SIO_EXT_WAKE#
<30> KB_DET#
<30> I2C0_SDA_TCH_PAD
<30> I2C0_SCL_TCH_PAD
DGPU_HOLD_RST#
IR_CAM_DETECT#
RTC_DET#
DGPU_HOLD_RST# <44>
IR_CAM_DETECT# <28>
RTC_DET# <22>
DGPU_PWR_EN
VRAM_ID2
DGPU_PWR_EN <43,63>
IO_CBL_DET# <26>
VGA_CBL_DET# <34>
BOARD_ID1
FFS_INT2
UART1_RTS#
UART1_CTS#
FFS_INT2 <31>
TP88
TP79
+3VS
RC42 LOKI@ 10K_0402_5% BLUETOOTH_EN
RC36 10K_0402_5% FFS_INT2
+3VALW
RC226 MAD@ 10K_0402_5% BLUETOOTH_EN
+3VALW_PCH
KB_DET# RC45 10K_0402_5%
RTC_DET# RC46 10K_0402_5%
SIO_EXT_WAKE# RC47 10K_0402_5%
3.3V_TS_EN RC213 10K_0402_5%
DGPU_HOLD_RST# RC48 DIS@ 10K_0402_5%
+3VS
RC49 DIS@ 10K_0402_5%
DGPU_PWR_EN
RC50 DIS@ 150K_0402_5%
+3VS
IR_CAM_DETECT# RC200 10K_0402_5%
LCD_CBL_DET# RC205 10K_0402_5%
VGA_CBL_DET# RC207 10K_0402_5%
IO_CBL_DET# RC206 10K_0402_5%
+3VS
RC61 @ 10K_0402_5%
RC59 @ 10K_0402_5%
VRAM_ID2
VRAM_ID1
RC62 2G_G5@ 10K_0402_5%
RC60 2G_G5@ 10K_0402_5%
+3VS
RC55 KBLU@ 10K_0402_5%
RC57 KBLU@ 10K_0402_5%
BOARD_ID2
BOARD_ID1
RC56 SKLU@ 10K_0402_5%
RC58 SKLU@ 10K_0402_5%
+3VALW_PCH
RC44 @ 4.7K_0402_5% NRB_BIT

VRAM x32*2 / X16*2 Detect	
HIGH	X32 * 2pcs VRAM(LAF116)
LOW	X16 * 4pcs VRAM(LAF115)

NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Weak IPD

CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

RC55 KBLR@ 10K_0402_5% SD028100280

RC58 KBLR@ 10K_0402_5% SD028100280

LAF115 VRAM x16*4pcs

VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_D14)	VBIOS_ID1 (GPP_B17)
2G GDDR5	0	0
4G GDDR5	0	1
New 2G GDDR5	1	0
Reserved	1	1

RC62 4G_G5@ 10K_0402_5% SD028100280

RC61 New_2G_G5@ 10K_0402_5% SD028100280

RC59 4G_G5@ 10K_0402_5% SD028100280

RC60 New_2G_G5@ 10K_0402_5% SD028100280

LAF116 VRAM x32*2pcs

VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_D14)	VBIOS_ID1 (GPP_B17)
2G GDDR5_1	0	0
2G GDDR5_2	0	1
Reserved	1	0
Reserved	1	1

RC62 X32_1@ 10K_0402_5% SD028100280

RC62 X32_2@ 10K_0402_5% SD028100280

RC60 X32_1@ 10K_0402_5% SD028100280

RC59 X32_2@ 10K_0402_5% SD028100280

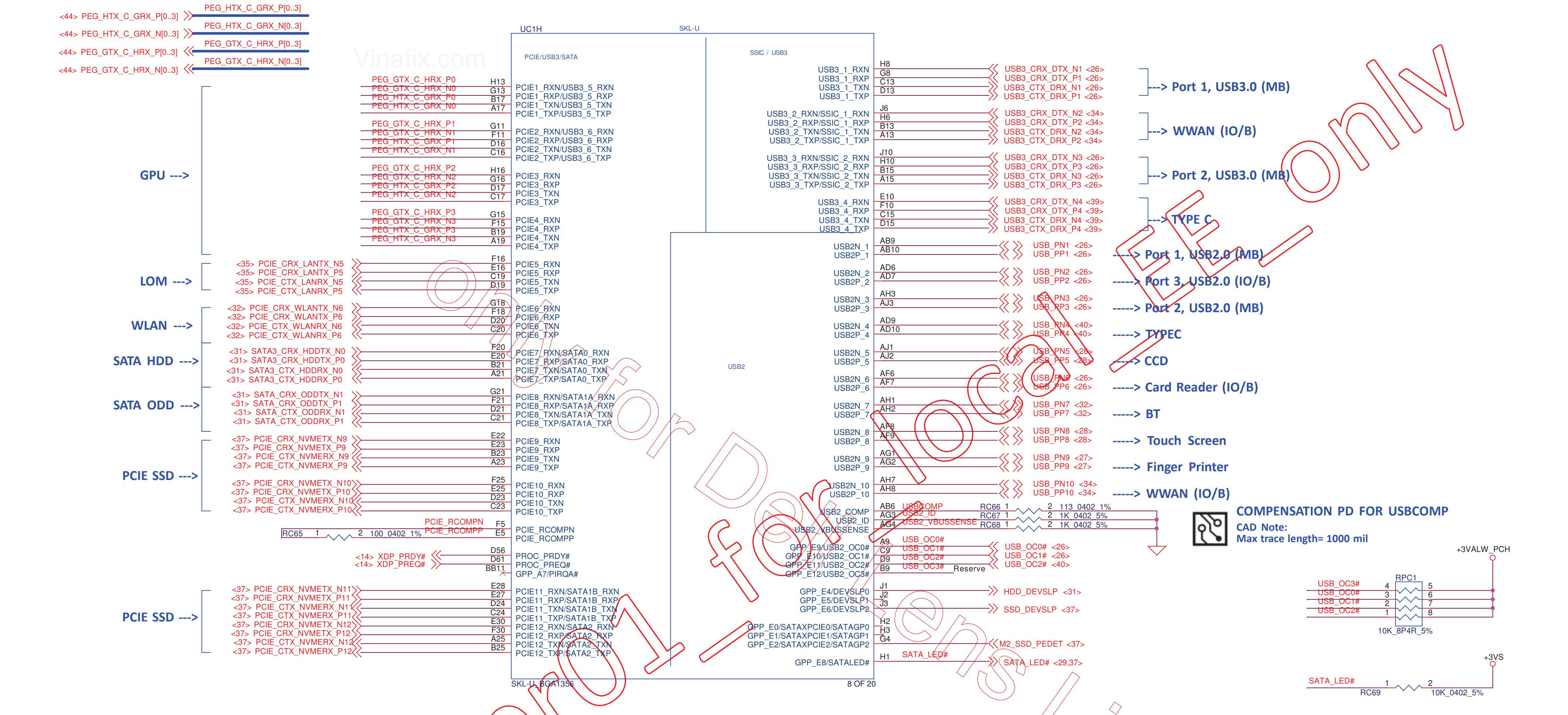
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **MCP(4/14)GSPI,I2C,UART,ISH**

Size | Document Number: **LA-F115P** | Rev 0.1

Main Func = CPU



<44> PEG_HTX_C_GRX_P[0..3]
<44> PEG_HTX_C_GRX_N[0..3]
<44> PEG_GTX_C_HRX_P[0..3]
<44> PEG_GTX_C_HRX_N[0..3]
UC1H
SKL-U
PCIE/USB3/SATA
SSIC / USB3
USB2
GPU --->
LOM --->
WLAN --->
SATA HDD --->
SATA ODD --->
PCIE SSD --->
PCIE SSD --->
PCIE1_RXN/USB3_5_RXN
PCIE1_RXP/USB3_5_RXP
PCIE1_TXN/USB3_5_TXN
PCIE1_TXP/USB3_5_TXP
PCIE2_RXN/USB3_6_RXN
PCIE2_RXP/USB3_6_RXP
PCIE2_TXN/USB3_6_TXN
PCIE2_TXP/USB3_6_TXP
PCIE7_RXN/SATA0_RXN
PCIE7_RXP/SATA0_RXP
PCIE7_TXN/SATA0_TXN
PCIE7_TXP/SATA0_TXP
PCIE8_RXN/SATA1A_RXN
PCIE8_RXP/SATA1A_RXP
PCIE8_TXN/SATA1A_TXN
PCIE8_TXP/SATA1A_TXP
PCIE_RCOMPN
PCIE_RCOMPP
PROC_PRDY#
PROC_PREQ#
GPP_A7/PIRQA#
PCIE11_RXN/SATA1B_RXN
PCIE11_RXP/SATA1B_RXP
PCIE11_TXN/SATA1B_TXN
PCIE11_TXP/SATA1B_TXP
PCIE12_RXN/SATA2_RXN
PCIE12_RXP/SATA2_RXP
PCIE12_TXN/SATA2_TXN
PCIE12_TXP/SATA2_TXP
SKL-U_BGA1356
8 OF 20
RC65 100_0402_1%
---> Port 1, USB3.0 (MB)
---> WWAN (IO/B)
---> Port 2, USB3.0 (MB)
---> TYPE C
-----> Port 1, USB2.0 (MB)
-----> Port 3, USB2.0 (IO/B)
-----> Port 2, USB2.0 (MB)
-----> TYPEC
-----> CCD
-----> Card Reader (IO/B)
-----> BT
-----> Touch Screen
-----> Finger Printer
-----> WWAN (IO/B)
USB2_COMP
USB2_ID
USB2_VBUSSENSE
RC66 113_0402_1%
RC67 1K_0402_5%
RC68 1K_0402_5%
COMPENSATION PD FOR USBCOMP
CAD Note:
Max trace length= 1000 mil
GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
Reserve
GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2
HDD_DEVSLP <31>
SSD_DEVSLP <37>
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E8/SATALED#
M2_SSD_PEDET <37>
SATA_LED# <29,37>
+3VALW_PCH
RPC1
10K_8P4R_5%
+3VS
RC69
10K_0402_5%

GPIO	Device Control
USB_OC0#	USB Port 1
USB_OC1#	WWAN
USB_OC2#	USB Port 4 (Type-C)
USB_OC3#	NA

Security Classification	Compal Secret Data	
Issued Date	2016/12/01	Deciphered Date 2017/12/01

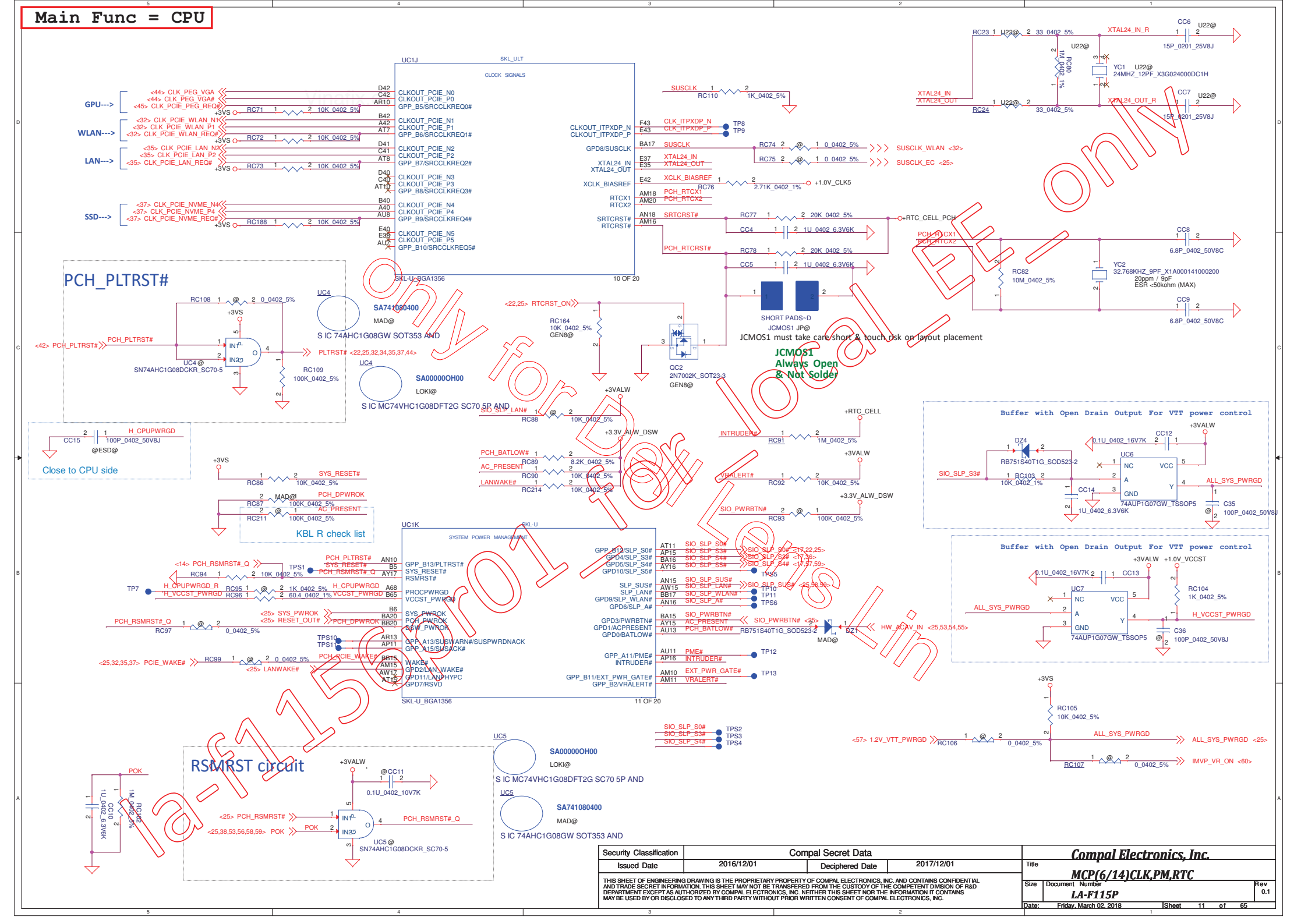
Compal Electronics, Inc.

Title: **MCP(5/14)PCIE,USB,SATA**

Size | Document Number: **LA-F115P** | Rev 0.1

Date: Friday, March 02, 2018

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

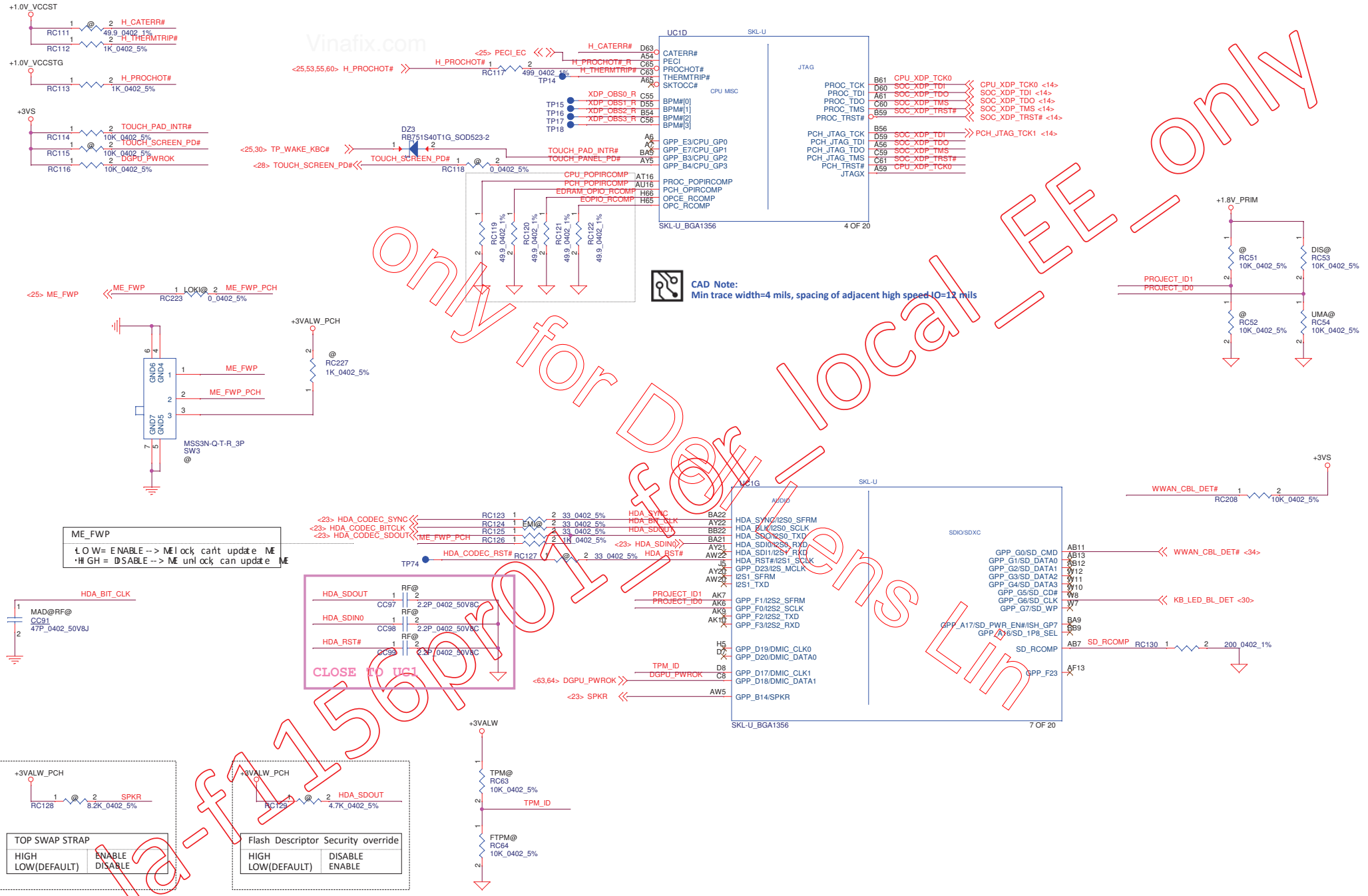
Compal Electronics, Inc.

Title: MCP(6/14)CLK,PM,RTC

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 11 of 65

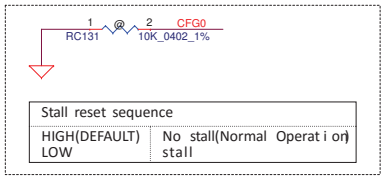
Main Func = CPU

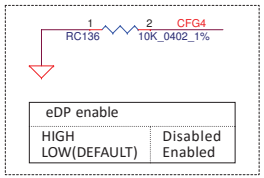


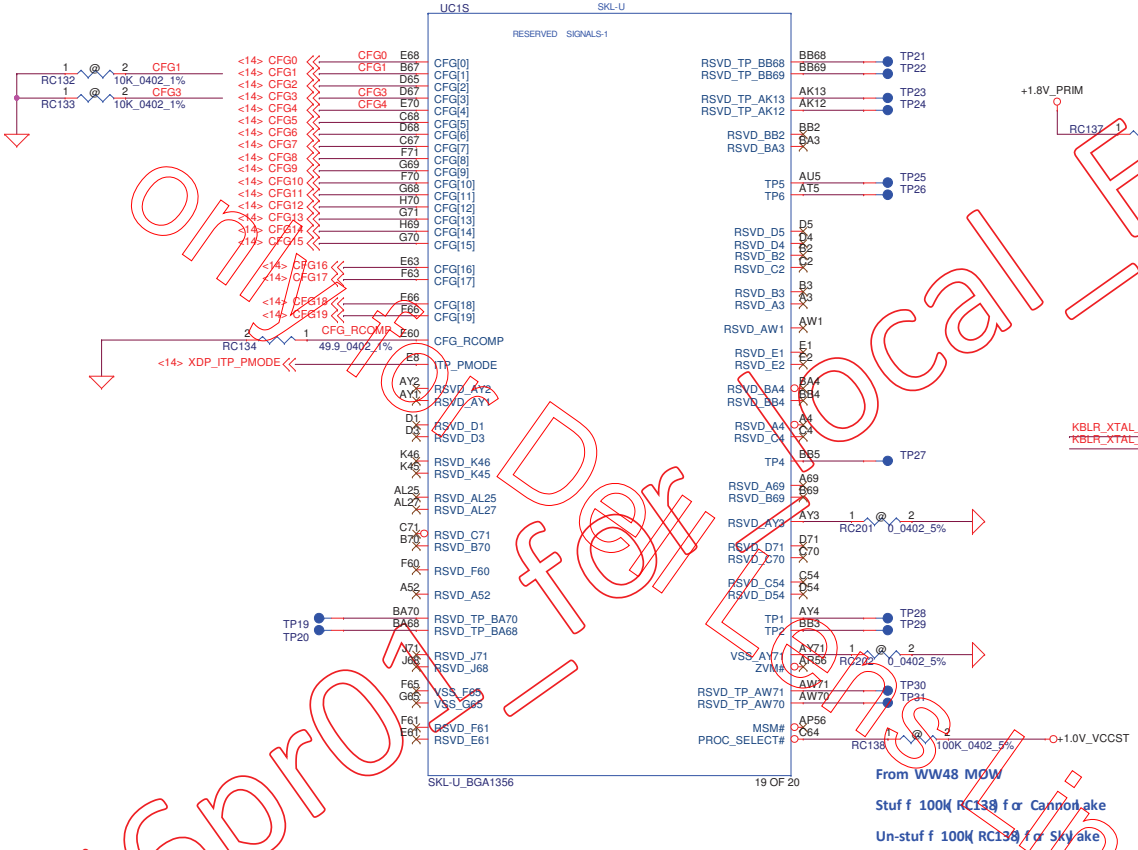
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

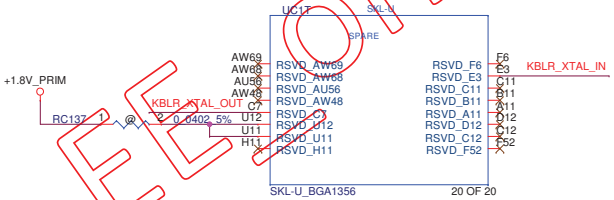
Compal Electronics, Inc.	
Title	MCP(7/14)MISC,JTAG,HDA,SDIO
Size	Document Number: LA-F115P
Rev	0.1
Date: Friday, March 02, 2018	Sheet 12 of 65

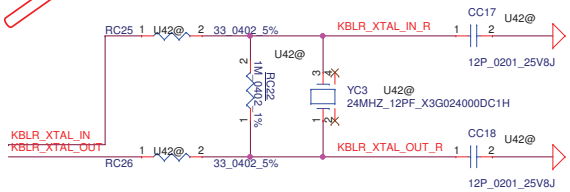
Main Func = CPU











From WW48 MOW

Stuf f 100K RC138 f or Cannon Lake

Un-stuf f 100K RC138 f or Sky Lake

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(8/14)CFG,RSVD

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 13 of 65

Main Func = CPU

Connector Less Routing Topology

DCI Link
RC142 need POP
RC146 need POP

+3.3V_SPI
RC139 1 CMC@ 2 1K_0402_5% XDP_SPI_SI

+1.0V_VCCSTG
Place to CPU side
RC140 2 CMC@ 1 51_0402_5% SOC_XDP_TMS
RC141 2 CMC@ 1 51_0402_5% SOC_XDP_TDI
RC142 2 CMC@ 1 51_0402_5% SOC_XDP_TDO

+1.0V_XDP
RC143 1 CMC@ 2 1K_0402_5% XDP_ITP_PMODE
RC144 2 @ 1 0_0402_5% XDP_PRSENT_CPU
RC145 2 @ 1 0_0402_5% XDP_SPI_IO2
Place to CPU side
RC146 2 CMC@ 1 51_0402_1% CPU_XDP_TCK0
RC147 2 @ 1 51_0402_5% PCH_JTAG_TCK1

<12> SOC_XDP_TDO → TPC1
<12> CPU_XDP_TCK0 → TPC2
<12> PCH_JTAG_TCK1 → TPC3
<12> SOC_XDP_TMS → TPC4

<12> SOC_XDP_TDI → TPC5
<12> SOC_XDP_TRST# → TPC6
<13> XDP_ITP_PMODE → TPC7

<8> XDP_SPI_SI → TPC8
<8> XDP_SPI_IO2 → TPC9

CFG3 RC175 1 CMC@ 2 0_0402_5% XDP_PRSENT_CPU

<11> PCH_RSMRST#_O PCH_RSMRST#_Q RC148 1 CMC@ 2 1K_0402_5% XDP_HOOK0

PRIMARY CMC CONN

+1.0V_PRIM RC149 1 CMC@ 2 0_0603_5% +1.0V_XDP

<13> CFG0 → TPC10
<13> CFG1 → TPC11
<13> CFG2 → TPC12
<13> CFG3 → TPC13
<13> CFG4 → TPC14
<13> CFG5 → TPC15
<13> CFG6 → TPC16
<13> CFG7 → TPC17

<13> CFG17 → TPC18
<13> CFG16 → TPC19

<13> CFG8 → TPC20
<13> CFG9 → TPC21
<13> CFG10 → TPC22
<13> CFG11 → TPC23
<13> CFG12 → TPC24
<13> CFG13 → TPC25
<13> CFG14 → TPC26
<13> CFG15 → TPC27

<13> CFG19 → TPC28
<13> CFG18 → TPC29

TPC30 → XDP_PREQ# <10>
TPC31 → XDP_PRDY# <10>
TPC32 → XDP_HOOK0
TPC33 → XDP_PRSENT_CPU

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(9/14)XDP

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 14 of 65

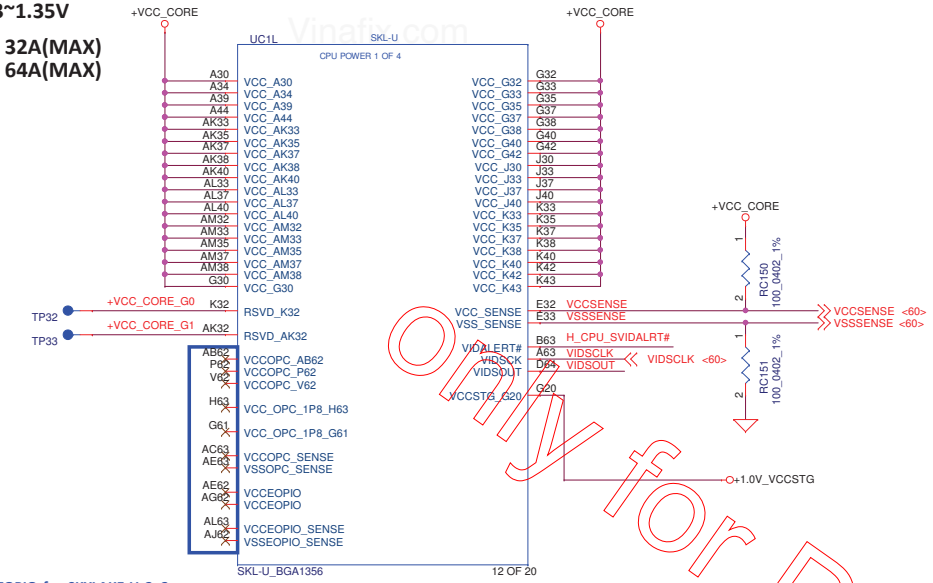
Main Func = CPU

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

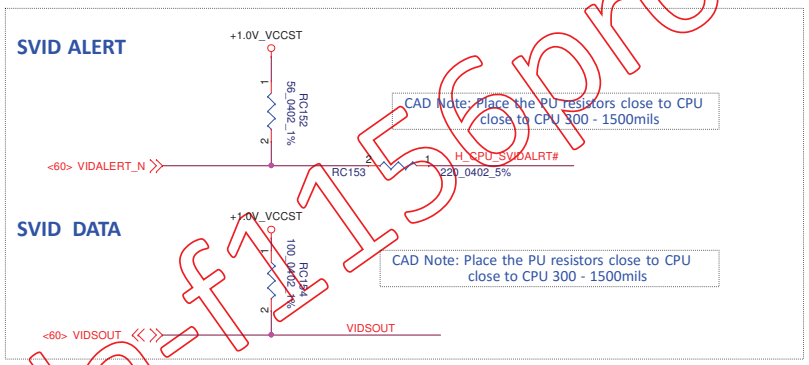
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

+VCC_CORE: 0.3~1.35V

+VCC_CORE(U22): 32A(MAX)
+VCC_CORE(U42): 64A(MAX)



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(10/14)PWR-VCC CORE

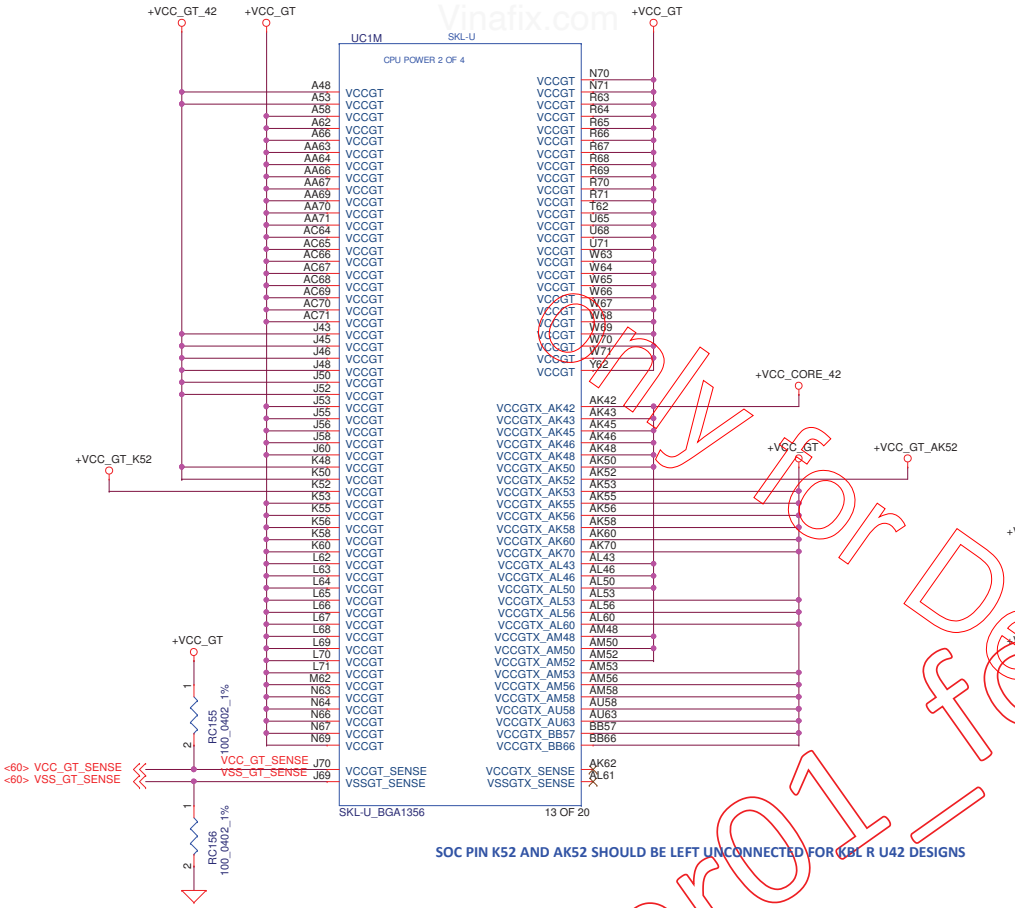
Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 15 of 65

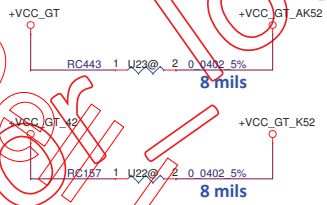
Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)



SOC PIN K52 AND AK52 SHOULD BE LEFT UNCONNECTED FOR KBL R U42 DESIGNS



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(11/14)PWR-VCCGT

Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 16 of 65

Main Func = CPU

Annotat i on
1.35V in DDR3L
1.2V in LPDDR3 and DDR4

+1.2V_DDR

BSC PSC

CC26 10U_0402_6.3V6M
CC27 10U_0402_6.3V6M
CC28 10U_0402_6.3V6M
CC29 10U_0402_6.3V6M
CC30 10U_0402_6.3V6M
CC31 10U_0402_6.3V6M

CC32 1U_0402_6.3V6K
CC33 1U_0402_6.3V6K
CC34 1U_0402_6.3V6K
CC35 1U_0402_6.3V6K
CC36 22U_0603_6.3V6M
CC37 22U_0603_6.3V6M
CC38 22U_0603_6.3V6M

CC39 10U_0402_6.3V6M
CC40 1U_0402_6.3V6K

UC1N SKL-U
CPU POWER 3 OF 4
SKL-U_BGA1356
14 OF 20

VDDQ_AU23 AU23
VDDQ_AU28 AU28
VDDQ_AU35 AU35
VDDQ_AU42 AU42
VDDQ_BB23 BB23
VDDQ_BB32 BB32
VDDQ_BB41 BB41
VDDQ_BB47 BB47
VDDQ_BB51 BB51
VDDQC AM40
VCCST A18
VCCSTG_A22 A22
VCCPLL_OC AL23
VCCPLL_K20 K20
VCCPLL_K21 K21

+1.0VS_VCCIO
VCCIO AK28 AK30 AL30 AL42 AM28 AM30 AM42
+VCC_SA
VCCSA AK23 AK25 G23 G25 G27 G28 J22 J23 J27 K23 K25 K27 K28 K30
VCCIO_SENSE AM23
VSSIO_SENSE AM22
TP38 TP39
VSSSA_SENSE H21
VCCSA_SENSE H20
RC160 100_0402_1%
RC159 100_0402_1%

+1.0V_VCCST
PSC
CC41 1U_0402_6.3V6K

+1.0V_VCCSTG
BSC
CC42 1U_0402_6.3V6K

+1.2V_VCCSFR_OC
CC43 1U_0402_6.3V6K

+1.0V_VCCST
PSC
CC44 1U_0402_6.3V6K

VSA_SEN- <60>
VSA_SEN+ <60>

+1.0VS_VCCIO
BSC
CC45 1U_0402_6.3V6K
CC46 1U_0402_6.3V6K
CC47 1U_0402_6.3V6K
CC48 1U_0402_6.3V6K
CC49 10U_0402_6.3V6M
CC50 10U_0402_6.3V6M

PSC
CC51 1U_0402_6.3V6K
CC52 1U_0402_6.3V6K
CC53 1U_0402_6.3V6K
CC54 1U_0402_6.3V6K

JP1
Always Short
+1.0V_VCCSTG +1.0VS_VCCIO
JP1 PJP@
JUMP_43X79
CZ8 0.1U_0402_25V6 @
Imax : 3.4 A
POP option with Volume

+1.0V_VCCST source

Imax : 0.24 A
JP2
Always Short

DZ5 RB751S40T1G_SOD523-2
CZ21 1U_0402_6.3V6K
+1.0V_PRIM
RZ1 22.1K_0402_1%
<11,57,59> SIO_SLP_S4#
1.0V_VCCST_EN
CZ1 0.1U_0402_10V7K
+5VALW
UZ1
VIN VOUT ON CT VBIAS GND
TPS22967DSGR_SON8_2X2
+1.0V_VCCST_C
JP2 PJP@
PAD-OPEN1x1m
CZ2 0.1U_0402_10V7K
CZ3 470P_0402_50V7K
CZ22 1U_0402_6.3V6K
+1.0V_VCCST

UC9 SA00000OH00
LOKI@
S IC MC74VHC1G08DFT2G SC70 5P AND

UC9 SA741080400
MAD@
S IC 74AHC1G08GW SOT353 AND

+1.0V_VCCSTG source

Imax : 3.4 A + 0.04A

+1.0V_PRIM
UZ2
VIN1 VIN2 VIN thermal VBIAS ON VOUT GND
TPS22961DNYR_WSON8
4.4mohm/6A
TR=12.5us@Vin=1.05V
+5VALW
CZ24 1U_0402_6.3V6K
CZ25 0.1U_0402_10V7K
+1.0V_VCCSTG
CZ6 0.1U_0402_10V7K

RZ2 0_0402_5%
+3VALW
<11,36> SIO_SLP_S3#
<11,22,25> SIO_SLP_S0#
UC9@ SN74AHC1G08DCKR_SC70-5
VCCSTG_EN
RZ3 49.9K_0402_1%
VCCSTG_EN_R
DZ2 RB751S40T1G_SOD523-2
CZ7 0.1U_0402_10V7K

+1.0V_VCCSTG +1.0V_VCCST
RZ4 0_0603_5%
pop option with UZ1

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

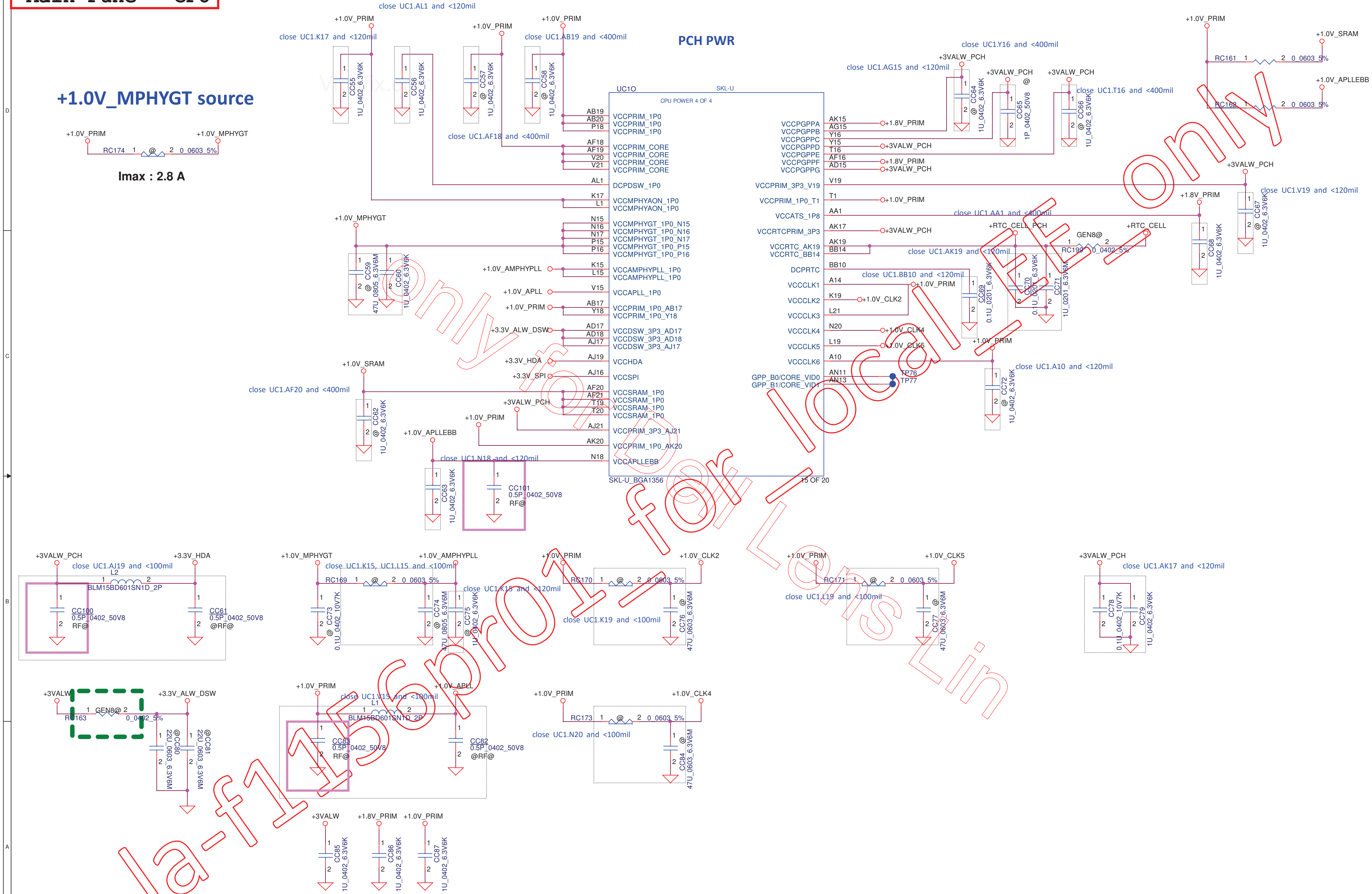
Compal Electronics, Inc.

Title: MCP(12/14)PWR-VCCIO,MEM

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 17 of 65

Main Func = CPU



PCH PWR
+1.0V_MPHYGT source
Imax : 2.8 A
UC1O
SKL-U
CPU POWER 4 OF 4
SKL-U_BGA1356
15 OF 20
VCCPRIM_1P0
VCCPRIM_CORE
DCPDSW_1P0
VCCMPHYAON_1P0
VCCMPHYGT_1P0_N15
VCCMPHYGT_1P0_N16
VCCMPHYGT_1P0_N17
VCCMPHYGT_1P0_P15
VCCMPHYGT_1P0_P16
VCCAMPHYPLL_1P0
VCCAPLL_1P0
VCCPRIM_1P0_AB17
VCCPRIM_1P0_Y18
VCCDSW_3P3_AD17
VCCDSW_3P3_AD18
VCCDSW_3P3_AJ17
VCCHDA
VCCSPI
VCCSRAM_1P0
VCCPRIM_3P3_AJ21
VCCPRIM_1P0_AK20
VCCAPLLEBB
VCCPGPPA
VCCPGPPB
VCCPGPPC
VCCPGPPD
VCCPGPPE
VCCPGPPF
VCCPGPPG
VCCPRIM_3P3_V19
VCCPRIM_1P0_T1
VCCATS_1P8
VCCRTCPRIM_3P3
VCCRTC_AK19
VCCRTC_BB14
DCPRTC
VCCCLK1
VCCCLK2
VCCCLK3
VCCCLK4
VCCCLK5
VCCCLK6
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
+1.0V_PRIM
+1.0V_MPHYGT
+1.0V_SRAM
+1.0V_APLLEBB
+3VALW_PCH
+1.8V_PRIM
+1.0V_AMPHYPLL
+1.0V_APLL
+3.3V_ALW_DSW
+3.3V_HDA
+3.3V_SPI
+RTC_CELL_PCH
+RTC_CELL
+1.0V_CLK2
+1.0V_CLK4
+1.0V_CLK5
+3VALW
close UC1.AL1 and <120mil
close UC1.K17 and <120mil
close UC1.AB19 and <400mil
close UC1.AF18 and <400mil
close UC1.Y16 and <400mil
close UC1.AG15 and <120mil
close UC1.T16 and <400mil
close UC1.V19 and <120mil
close UC1.AA1 and <400mil
close UC1.AK19 and <120mil
close UC1.BB10 and <120mil
close UC1.A10 and <120mil
close UC1.AF20 and <400mil
close UC1.N18 and <120mil
close UC1.AJ19 and <100mil
close UC1.K15, UC1.L15 and <100mil
close UC1.K15 and <120mil
close UC1.K19 and <100mil
close UC1.L19 and <100mil
close UC1.AK17 and <120mil
close UC1.V15 and <100mil
close UC1.N20 and <100mil
RC174 0_0603_5%
RC161 0_0603_5%
RC162 0_0603_5%
RC199 0_0402_5%
RC169 0_0603_5%
RC170 0_0603_5%
RC171 0_0603_5%
RC163 0_0402_5%
RC173 0_0603_5%
L2 BLM15BD601SN1D_2P
L1 BLM15BD601SN1D_2P
GEN8@
RF@
TP76
TP77

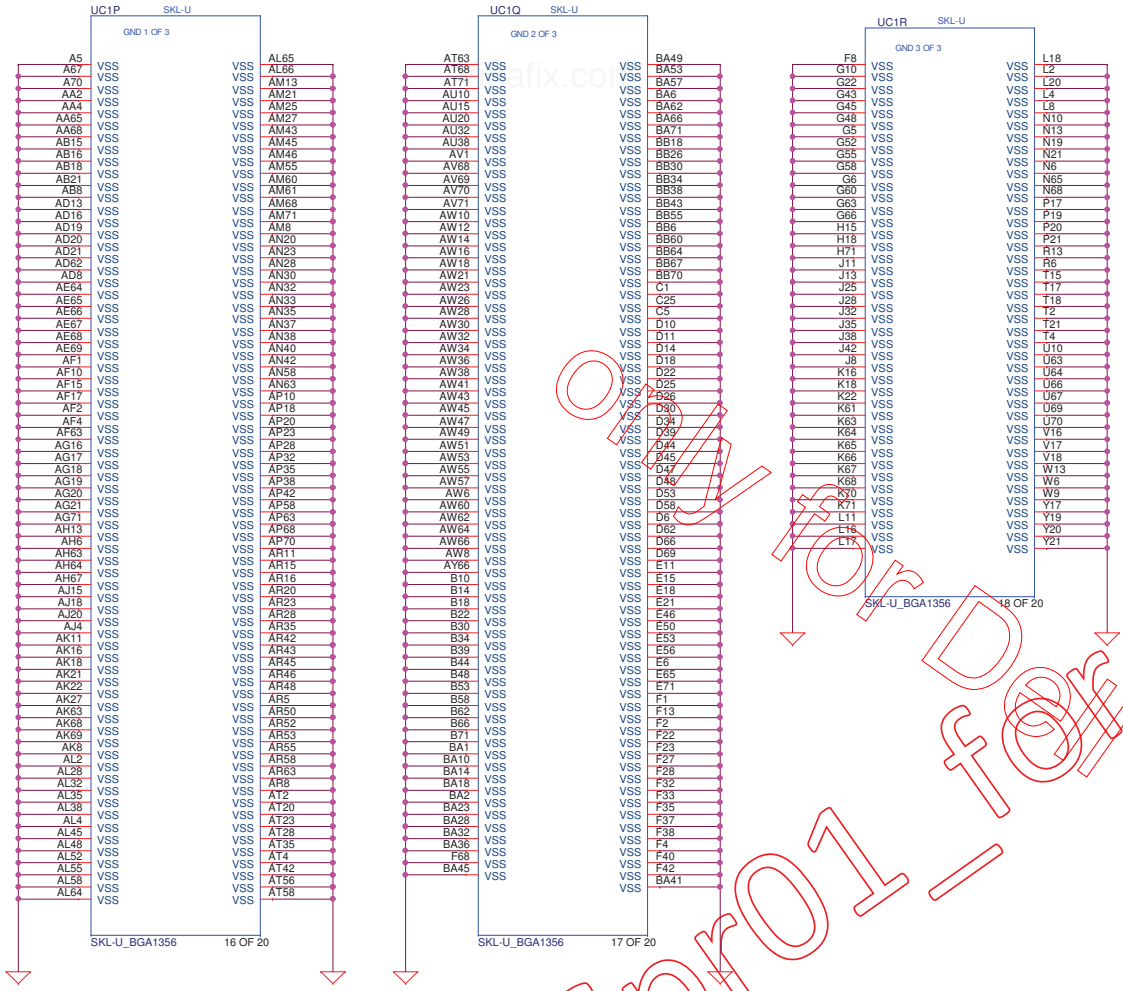
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(13/14)PCH PWR

Size | Document Number: LA-F115P | Rev 0.1

Main Func = CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

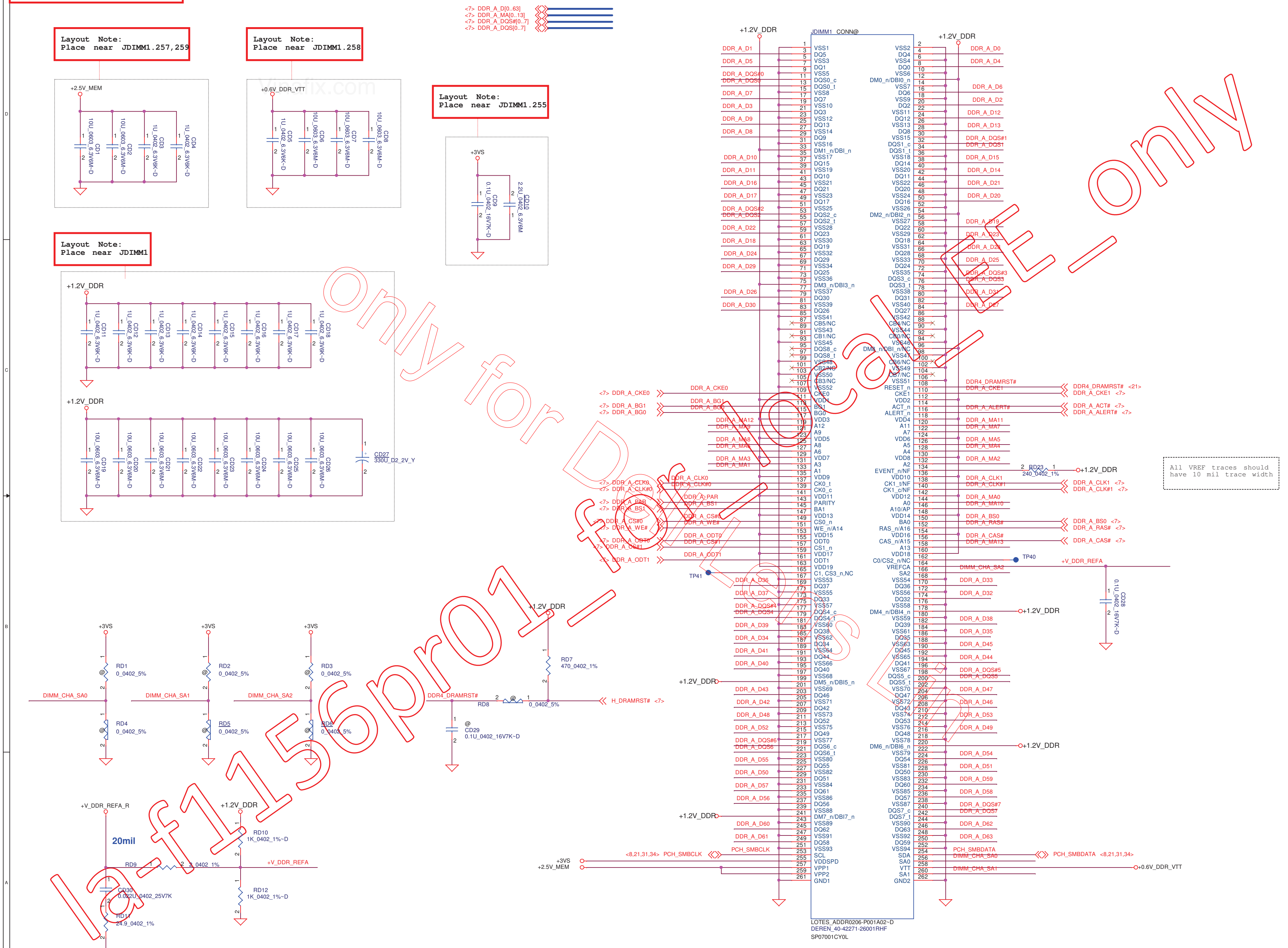
Compal Electronics, Inc.

Title: MCP(14/14)VSS

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 19 of 65

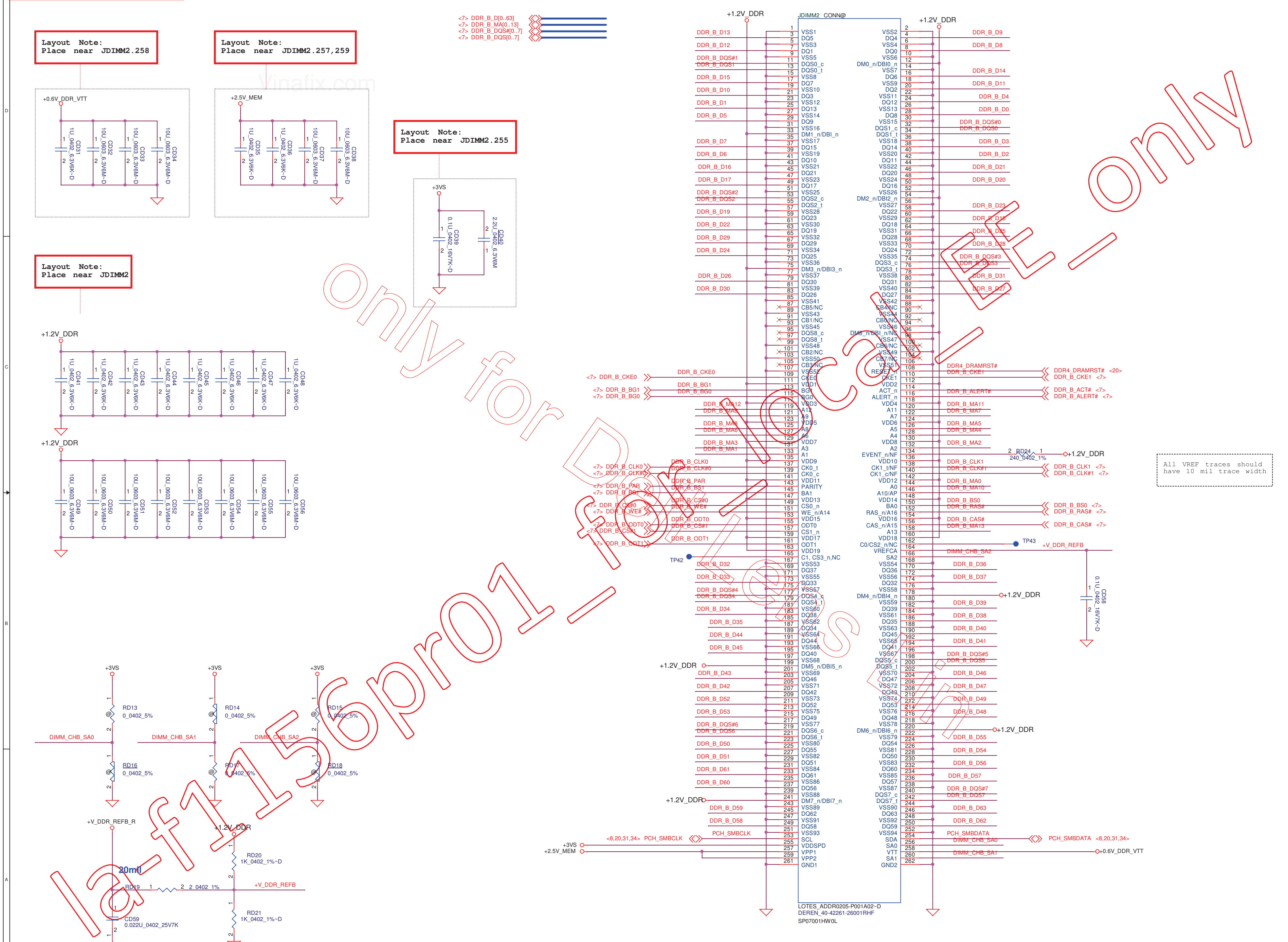
Main Func = DDR



Layout Note: Place near JDIMM1.257,259
Layout Note: Place near JDIMM1.258
Layout Note: Place near JDIMM1.255
Layout Note: Place near JDIMM1
+2.5V_MEM
+0.6V_DDR_VTT
+3VS
+1.2V_DDR
<7> DDR_A_D[0..63]
<7> DDR_A_MA[0..13]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_DQS[0..7]
JDIMM1 CONN@
CD27 330U_D2_2V_Y
CD28 0.1U_0402_16V7K~D
CD29 0.1U_0402_16V7K~D
CD30 0.022U_0402_25V7K
RD1 0_0402_5%
RD2 0_0402_5%
RD3 0_0402_5%
RD4 0_0402_5%
RD5 0_0402_5%
RD6 0_0402_5%
RD7 470_0402_1%
RD8 0_0402_5%
RD9 2_0402_1%
RD10 1K_0402_1%~D
RD11 24.9_0402_1%
RD12 1K_0402_1%~D
RD23 240_0402_1%
DIMM_CHA_SA0
DIMM_CHA_SA1
DIMM_CHA_SA2
DDR4_DRAMRST#
H_DRAMRST# <7>
DDR4_DRAMRST# <21>
+V_DDR_REFA_R
+V_DDR_REFA
20mil
TP40
TP41
<8,21,31,34> PCH_SMBCLK
PCH_SMBDATA <8,21,31,34>
All VREF traces should have 10 mil trace width
LOTES_ADDR0206-P001A02~D
DEREN_40-42271-26001RHF
SP07001CY0L

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date 2017/12/01	Title: DDR4 DIMMA_RVS
			Size / Document Number: LA-F111P / Rev 0.1
			Date: Friday, March 02, 2018 / Sheet 20 of 65

Main Func = DDR



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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Compal Electronics, Inc.

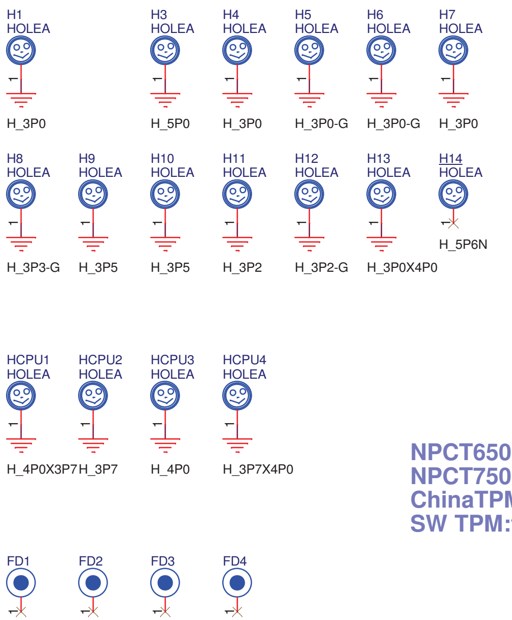
Title: **DDR4 DIMMB STD**

Size | Document Number: **LA-F115P** | Rev 0.1

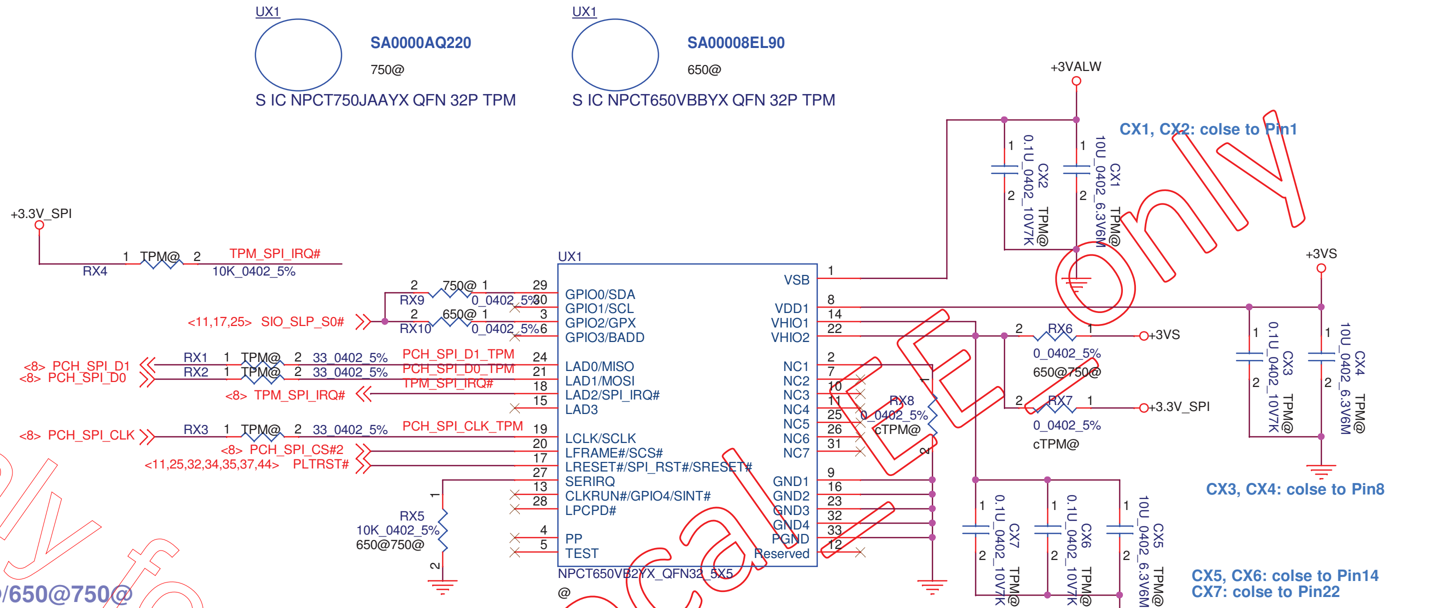
Date: Friday, March 02, 2018 | Sheet 21 of 65

Main Func = TPM

Screw hole/FD



H1 HOLEA H_3P0
H3 HOLEA H_5P0
H4 HOLEA H_3P0
H5 HOLEA H_3P0-G
H6 HOLEA H_3P0-G
H7 HOLEA H_3P0
H8 HOLEA H_3P3-G
H9 HOLEA H_3P5
H10 HOLEA H_3P5
H11 HOLEA H_3P2
H12 HOLEA H_3P2-G
H13 HOLEA H_3P0X4P0
H14 HOLEA H_5P6N
HCPU1 HOLEA H_4P0X3P7
HCPU2 HOLEA H_3P7
HCPU3 HOLEA H_4P0
HCPU4 HOLEA H_3P7X4P0
FD1
FD2
FD3
FD4

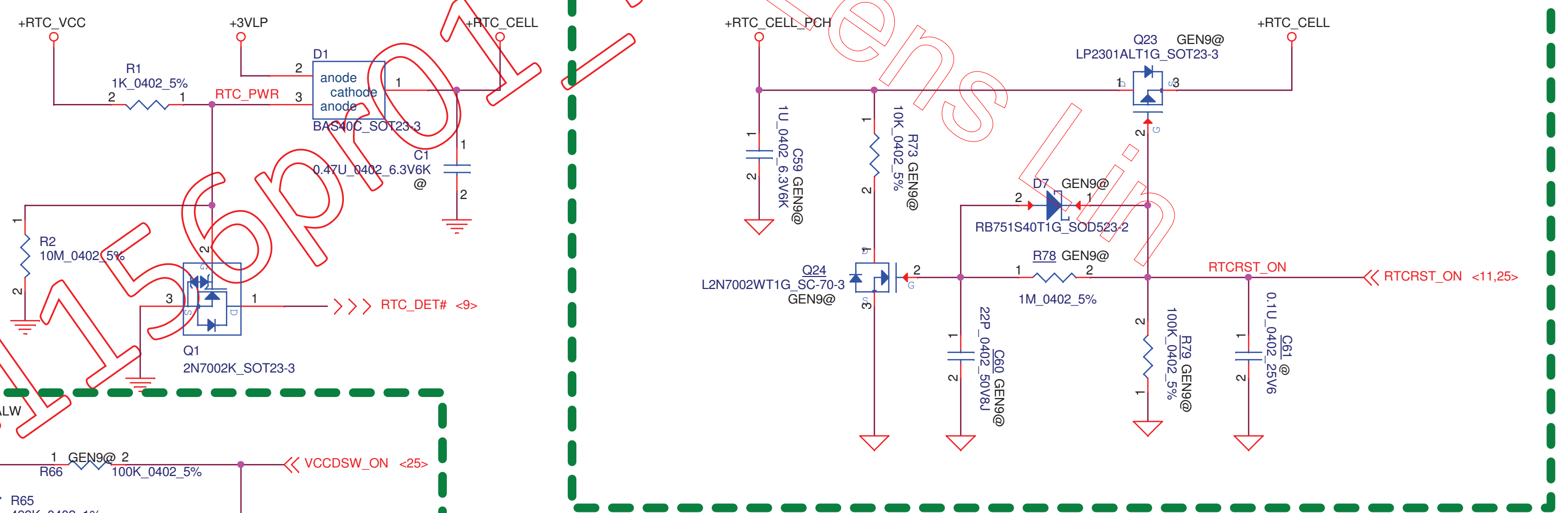


UX1 SA0000AQ220 750@
S IC NPCT750JAAYX QFN 32P TPM
UX1 SA00008EL90 650@
S IC NPCT650VBBYX QFN 32P TPM
+3.3V_SPI
RX4 TPM@ 10K_0402_5%
TPM_SPI_IRQ#
<11,17,25> SIO_SLP_S0#
RX9 750@ 0_0402_5%
RX10 650@ 0_0402_5%
<8> PCH_SPI_D1
<8> PCH_SPI_D0
RX1 TPM@ 33_0402_5%
RX2 TPM@ 33_0402_5%
PCH_SPI_D1_TPM
PCH_SPI_D0_TPM
<8> TPM_SPI_IRQ#
<8> PCH_SPI_CLK
RX3 TPM@ 33_0402_5%
PCH_SPI_CLK_TPM
<8> PCH_SPI_CS#2
<11,25,32,34,35,37,44> PLTRST#
RX5 10K_0402_5% 650@750@
UX1
GPIO0/SDA
GPIO1/SCL
GPIO2/GPX
GPIO3/BADD
LAD0/MISO
LAD1/MOSI
LAD2/SPI_IRQ#
LAD3
LCLK/SCLK
LFRAME#/SCS#
LRESET#/SPI_RST#/SRESET#
SERIRQ
CLKRUN#/GPIO4/SINT#
LPCPD#
PP
TEST
VSB
VDD1
VHIO1
VHIO2
NC1
NC2
NC3
NC4
NC5
NC6
NC7
GND1
GND2
GND3
GND4
PGND
Reserved
NPCT650VB2YX_QFN32_5X5
@
+3VALW
CX1 10U_0402_6.3V6M TPM@
CX2 0.1U_0402_10V7K TPM@
CX1, CX2: colse to Pin1
+3VS
RX6 0_0402_5% 650@750@
RX7 0_0402_5% cTPM@
RX8 0_0402_5% cTPM@
+3.3V_SPI
CX3 0.1U_0402_10V7K TPM@
CX4 10U_0402_6.3V6M TPM@
CX3, CX4: colse to Pin8
CX7 0.1U_0402_10V7K TPM@
CX6 0.1U_0402_10V7K TPM@
CX5 10U_0402_6.3V6M TPM@
CX5, CX6: colse to Pin14
CX7: colse to Pin22

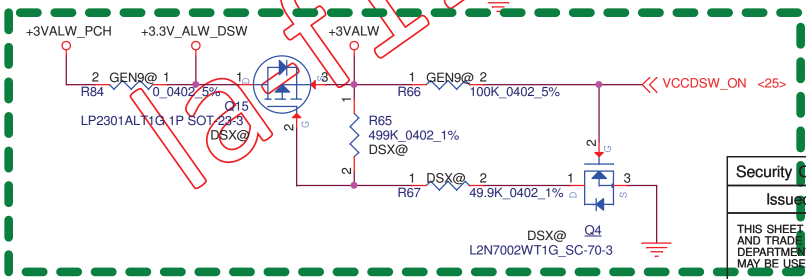
NPCT650:TPM@/650@/650@750@
NPCT750:TPM@/750@/650@750@
ChinaTPM:TPM@/cTPM@
SW TPM:fTPM@

UX1 place colse to UC3

Main Func = RTC

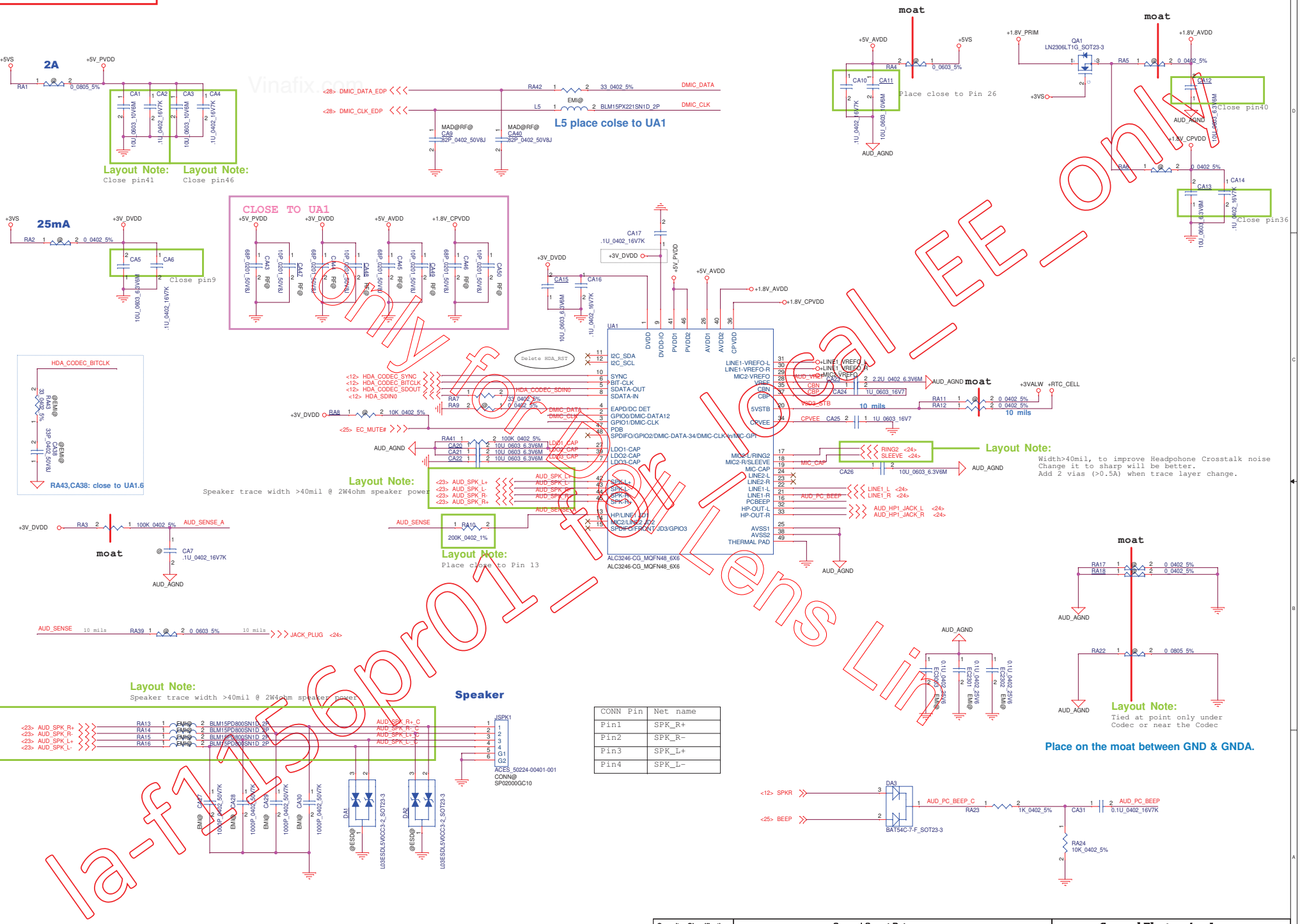


+RTC_VCC
+3VLP
+RTC_CELL
R1 1K_0402_5%
RTC_PWR
D1 anode cathode anode BAS40C_SOT23-3
C1 0.47U_0402_6.3V6K @
R2 10M_0402_5%
Q1 2N7002K_SOT23-3
RTC_DET# <9>
+RTC_CELL_PCH
+RTC_CELL
Q23 GEN9@ LP2301ALT1G_SOT23-3
C59 1U_0402_6.3V6K GEN9@
R73 10K_0402_5% GEN9@
D7 GEN9@ RB751S40T1G_SOD523-2
Q24 L2N7002WT1G_SC-70-3 GEN9@
R78 GEN9@ 1M_0402_5%
RTCRST_ON
RTCRST_ON <11,25>
C60 22P_0402_50V8J GEN9@
R79 100K_0402_5% GEN9@
C61 0.1U_0402_25V6 @



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title: TPM/RTC/Screw hole
				Size / Document Number: LA-F115P / Rev 0.1
				Date: Friday, March 02, 2018 / Sheet 22 of 65

Main Func = Audio



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

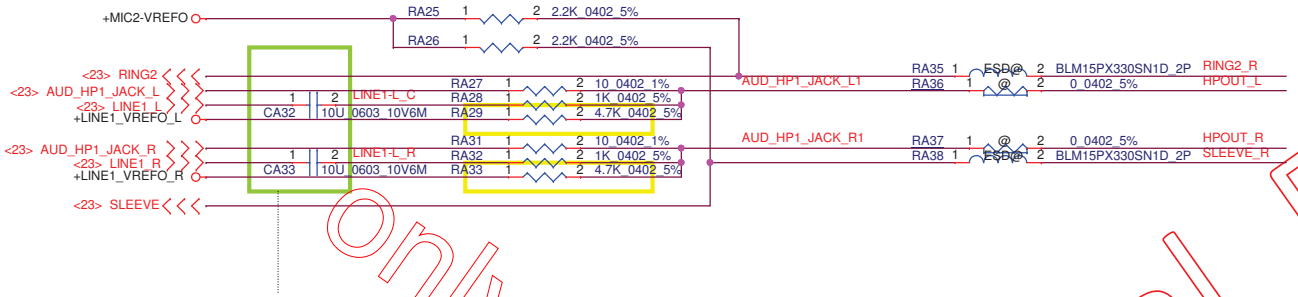
Compal Electronics, Inc.

Title: Audio Codec ALC3246

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 23 of 65

Main Func = Audio Jack

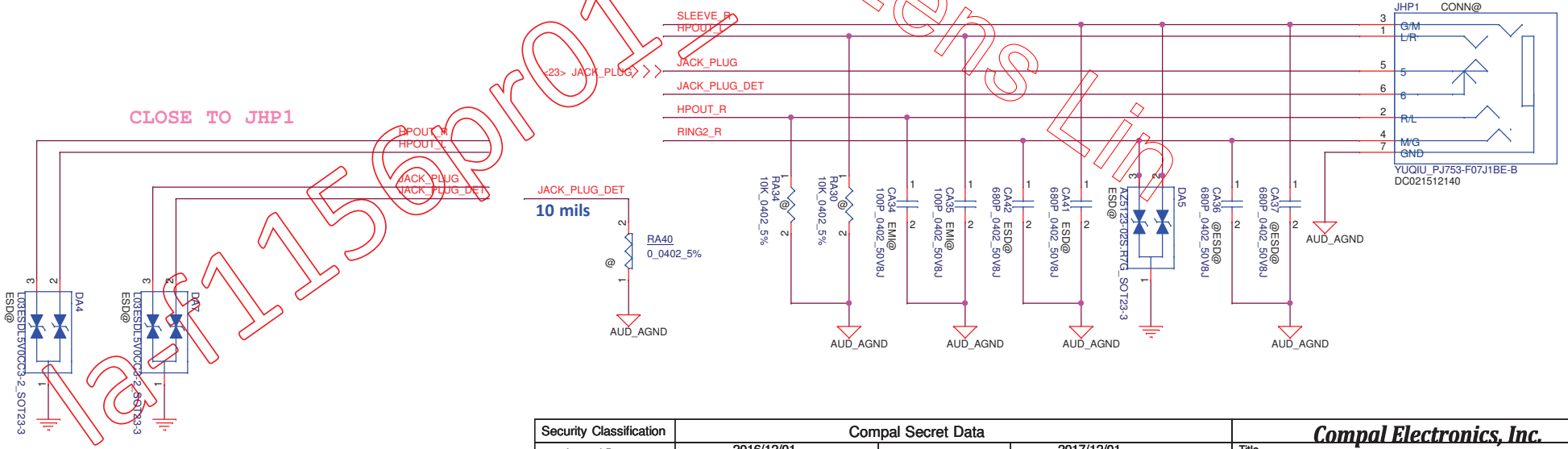


Layout Note:
Close to UA1

Universal Jack
(Global Headset Jack + mic phone in + line in support)

Main Func = Audio Jack

Universal Jack
(Global Headset Jack + mic phone in + line in support)

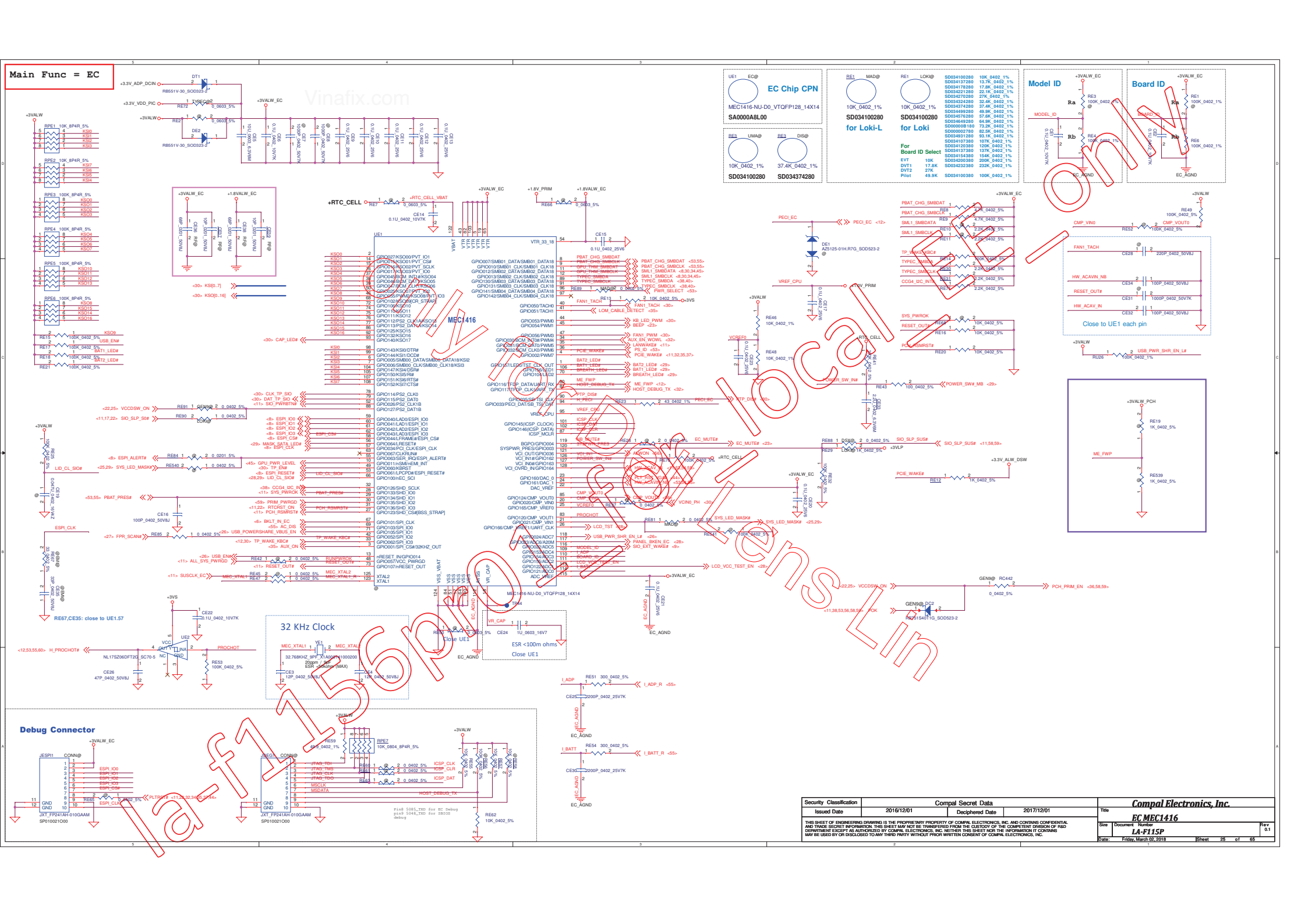


Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title	Audio JACK	
Size	Document Number LA-F115P	Rev 0.1
Date: Friday, March 02, 2018	Sheet 24 of 65	

Main Func = EC


EC Chip CPN
MEC1416-NU-D0_VTQFP128_14X14
SA0000A8L00
for Loki-L
SD034100280
for Loki
SD034374280
Model ID
Board ID
Close to UE1 each pin
32 KHz Clock
Debug Connector
ESR <100m ohms
Close UE1
RE67,CE35: close to UE1.57
MEC1416
Compal Secret Data
Issued Date
2016/12/01
Deciphered Date
2017/12/01
Compal Electronics, Inc.
EC MEC1416
LA-F115P
Friday, March 02, 2018
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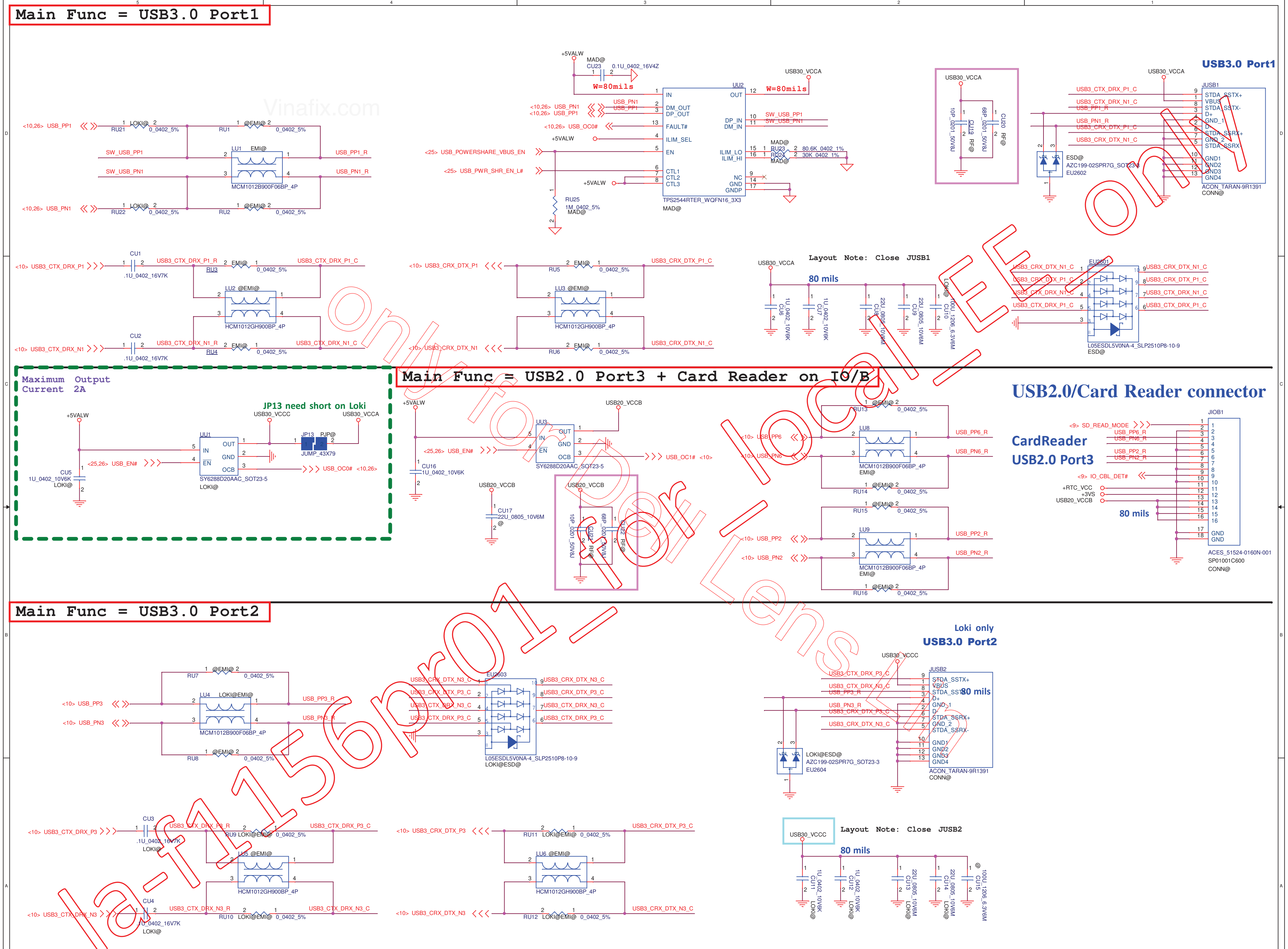


Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

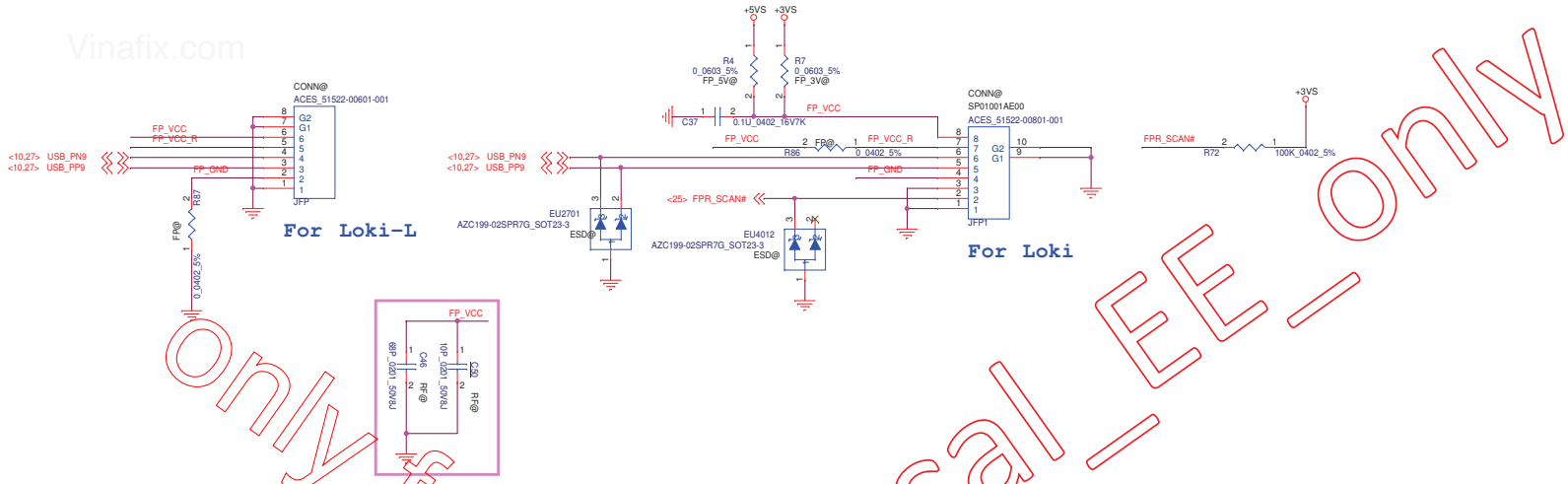
Compal Electronics, Inc.

Title: *USB3.0 & I/O*

Size | Document Number: *LA-F115P* | Rev 0.1

Date: Friday, March 02, 2018 | Sheet 26 of 65

Main Func = Finger Printer



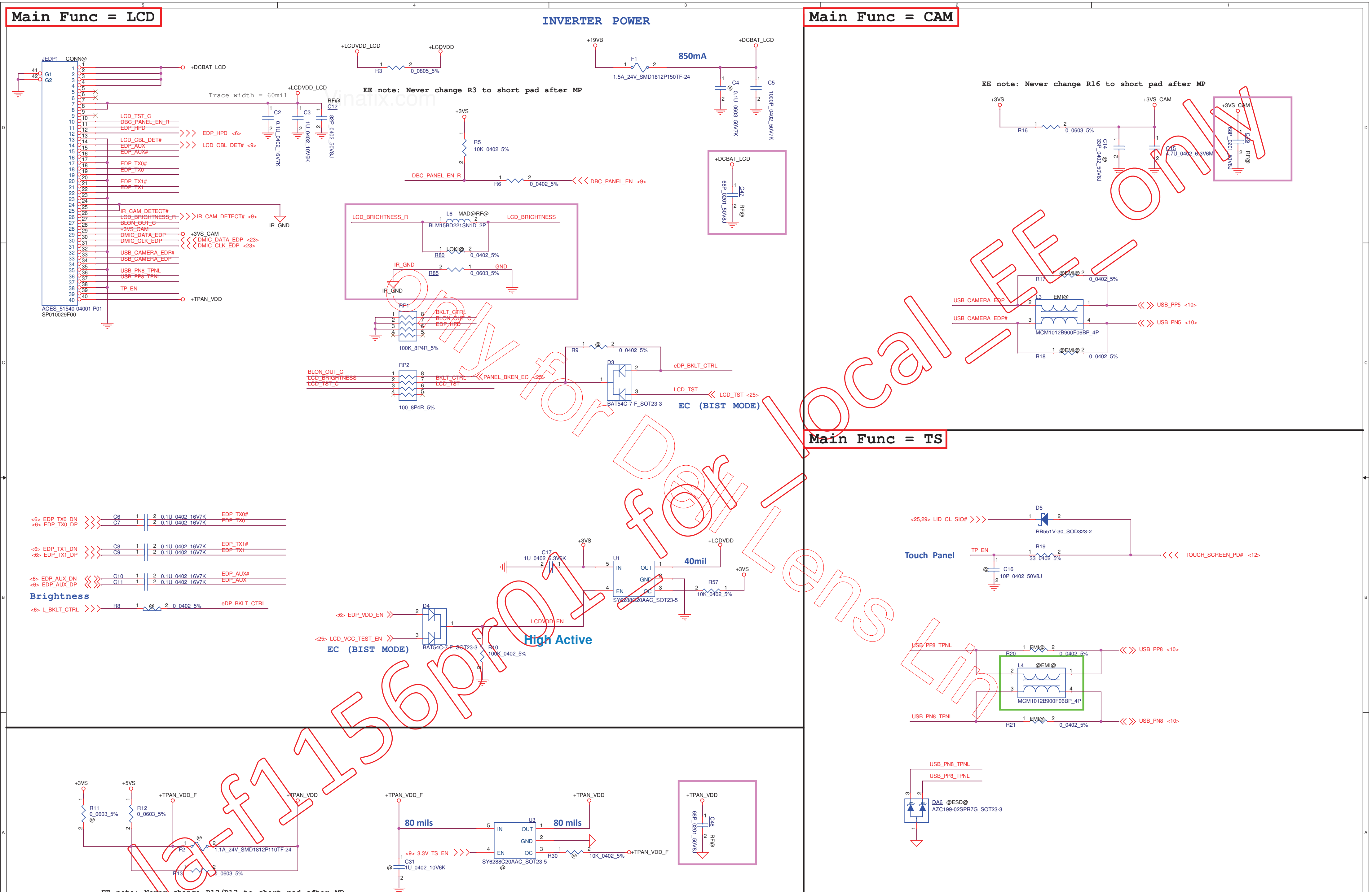
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **Finger Print**

Size	Document Number	Rev
	LA-F115P	0.1

Date: Friday, March 02, 2018 Sheet 27 of 65


Main Func = LCD
INVERTER POWER
Main Func = CAM
Main Func = TS
EE note: Never change R3 to short pad after MP
EE note: Never change R16 to short pad after MP
EE note: Never change R12/R13 to short pad after MP
Trace width = 60mil
850mA
40mil
80 mils
EC (BIST MODE)
High Active
Brightness
Touch Panel
JEDP1 CONN@
ACES_51540-04001-P01
SP010029F00
+DCBAT_LCD
+LCDVDD_LCD
+LCDVDD
+19VB
+3VS
+5VS
+3VS_CAM
+TPAN_VDD
+TPAN_VDD_F
1.5A_24V_SMD1812P150TF-24
1.1A_24V_SMD1812P110TF-24
BLM15BD221SN1D_2P
MCM1012B900F06BP_4P
BAT54C-7-F_SOT23-3
SY6288C20AAC_SOT23-5
RB551V-30_SOD323-2
AZC199-02SPR7G_SOT23-3
TOUCH_SCREEN_PD# <12>
USB_PP5 <10>
USB_PN5 <10>
USB_PP8 <10>
USB_PN8 <10>
DBC_PANEL_EN <9>
LCD_TST <25>
PANEL_BKEN_EC <25>

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

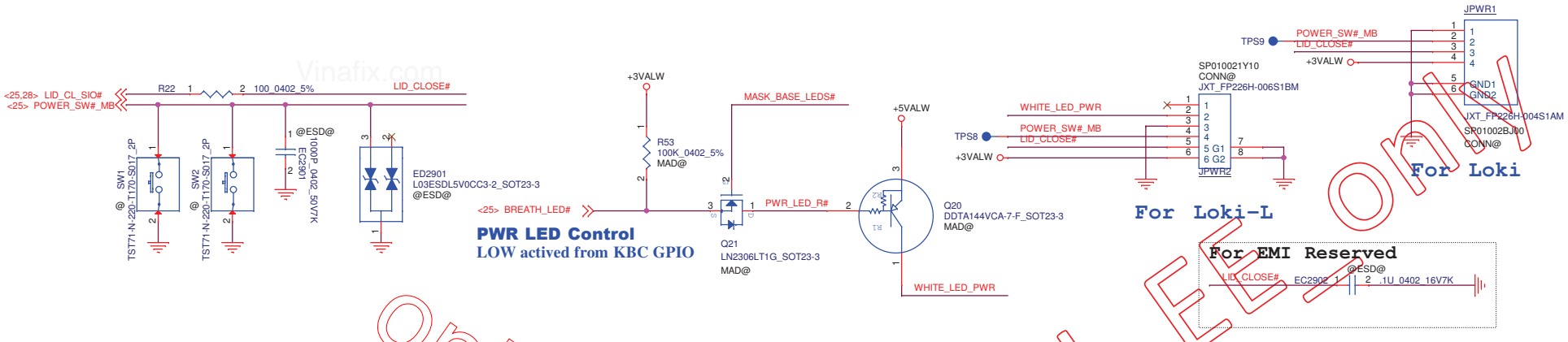
Title: **LCD/Cam/MIC/T.Panel**

Size | Document Number: **LA-F115P** | Rev 0.1

Main Func = Power BTN

Main Func = PWR LED

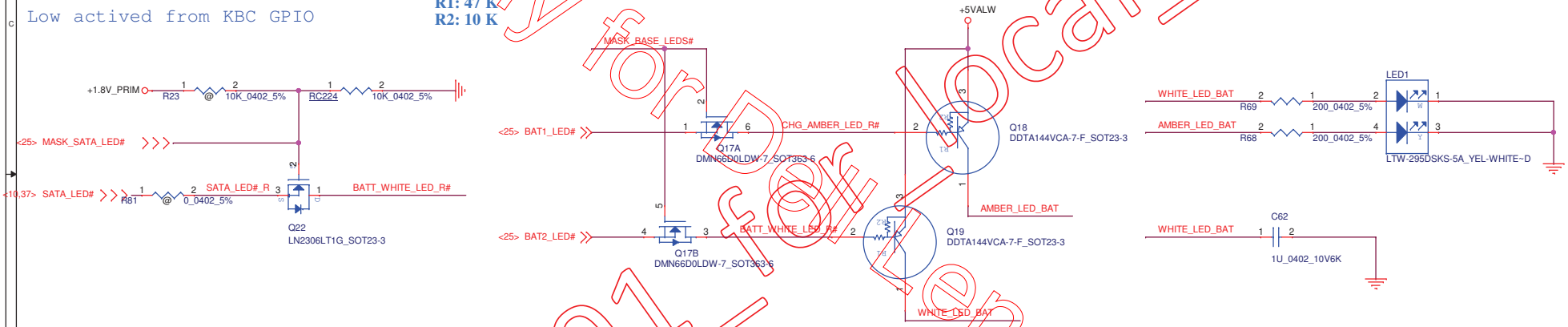
Low actived from KBC GPIO



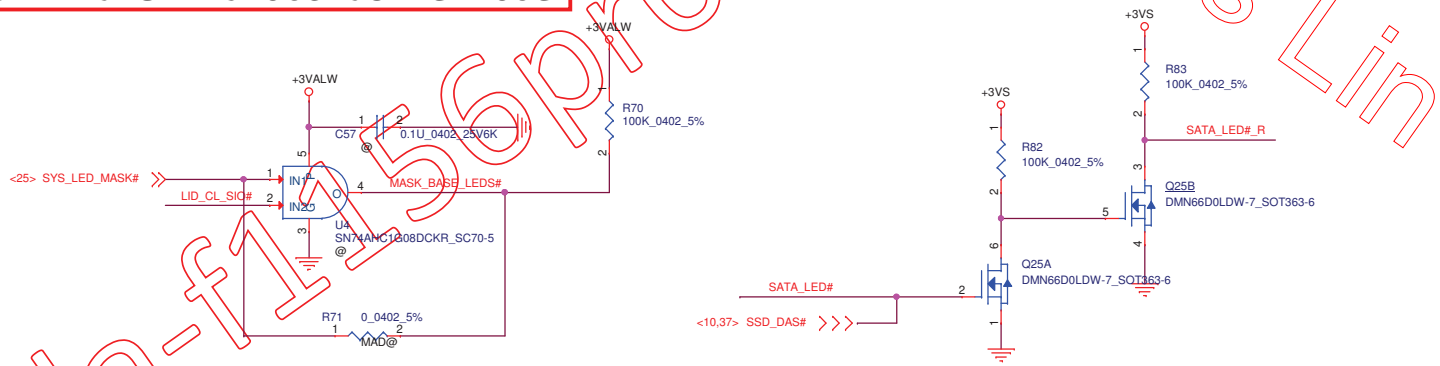
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Func = Unobtrusive Mode



VIH	2.1V
VIL	0.9V

07/28 change note: "SYS_LED_MASK#" from GPIO063 change to GPIO021

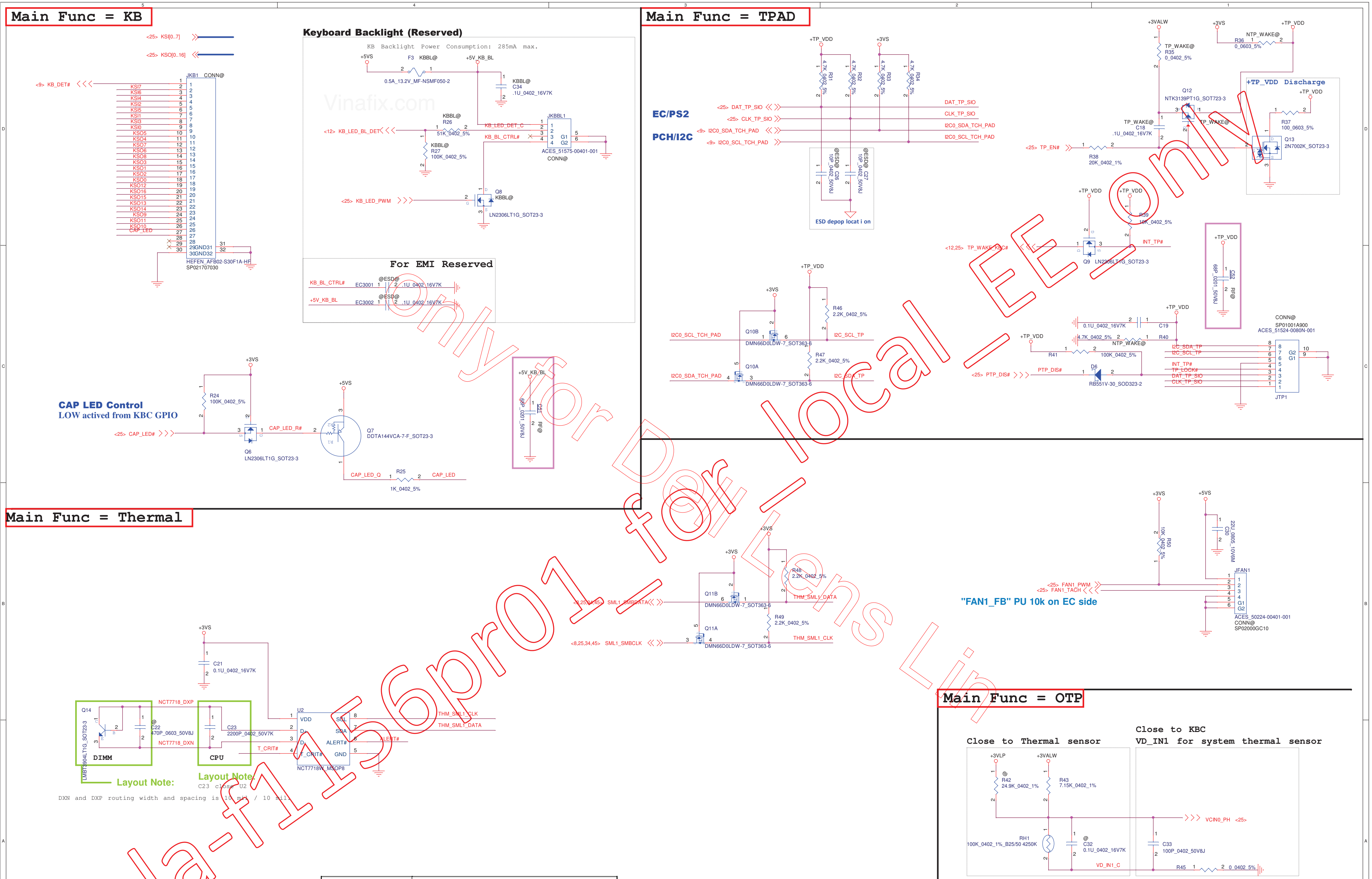
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

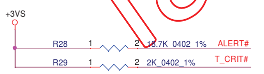
Compal Electronics, Inc.

Title: LED Board/Power Button

Size	Document Number	Rev
	LA-F115P	0.1

Date: Friday, March 02, 2018 Sheet 29 of 65





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

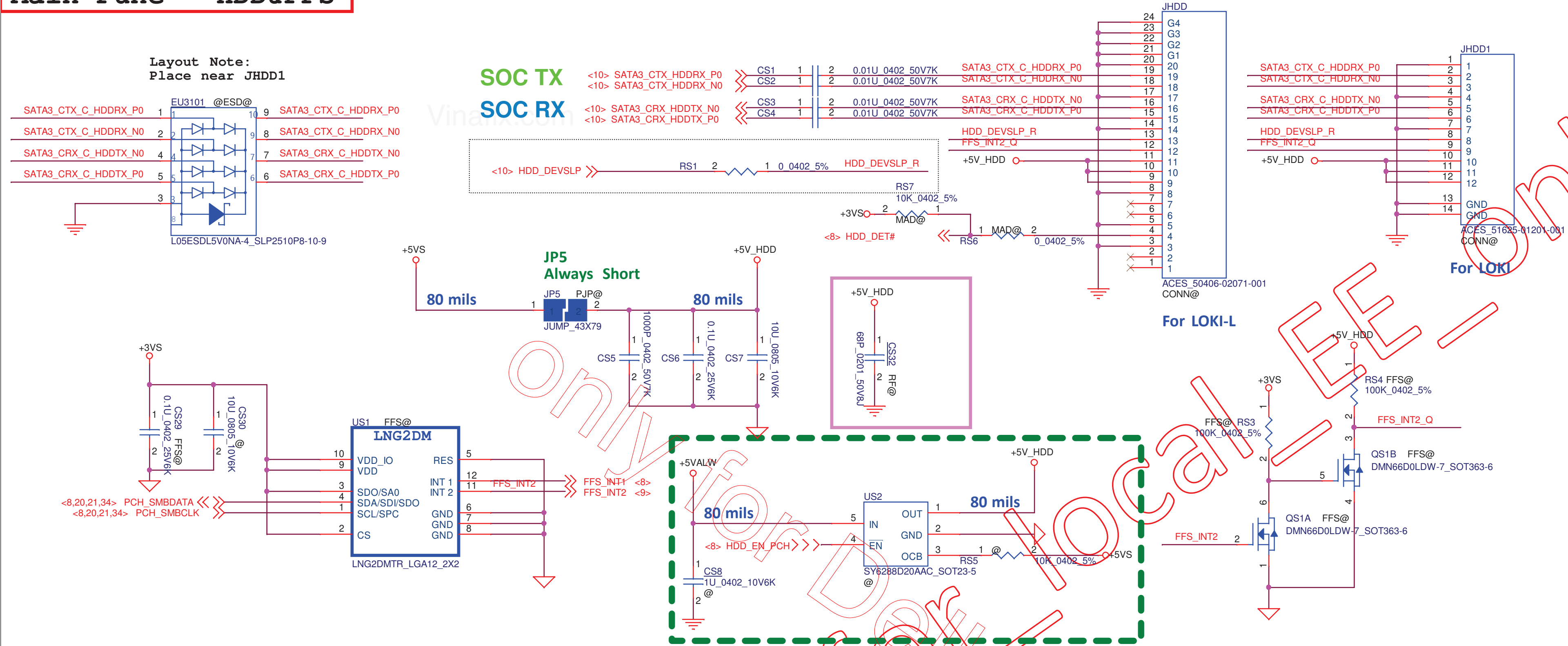
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **Keyboard/Touch Pad/Thermal/FAN**

Size | Document Number: **LA-F115P** | Rev 0.1

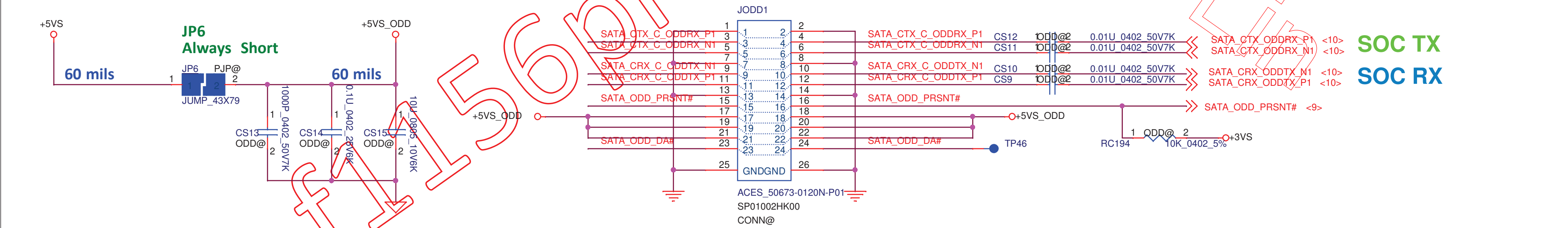
Main Func = HDD&FFS



Layout Note:
Place near JHDD1
EU3101 @ESD@
L05ESDL5V0NA-4_SLP2510P8-10-9
SATA3_CTX_C_HDDRX_P0
SATA3_CTX_C_HDDRX_N0
SATA3_CRX_C_HDDTX_N0
SATA3_CRX_C_HDDTX_P0
SOC TX
SOC RX
<10> SATA3_CTX_HDDRX_P0
<10> SATA3_CTX_HDDRX_N0
<10> SATA3_CRX_HDDTX_N0
<10> SATA3_CRX_HDDTX_P0
CS1 CS2 CS3 CS4
0.01U_0402_50V7K
<10> HDD_DEVSLP
RS1 0_0402_5%
HDD_DEVSLP_R
FFS_INT2_Q
+5V_HDD
RS7 10K_0402_5%
+3VS
MAD@
<8> HDD_DET#
RS6 MAD@ 0_0402_5%
JHDD
ACES_50406-02071-001
CONN@
For LOKI-L
JHDD1
ACES_51625-01201-001
CONN@
For LOKI
+5VS
JP5
Always Short
PJP@
JUMP_43X79
80 mils
+5V_HDD
CS5 1000P_0402_50V7K
CS6 0.1U_0402_25V6K
CS7 10U_0805_10V6K
CS32 68P_0201_50V8J RF@
+3VS
CS29 0.1U_0402_25V6K FFS@
CS30 10U_0805_10V6K @
US1 FFS@
LNG2DM
VDD_IO VDD SDO/SA0 SDA/SDI/SDO SCL/SPC CS RES INT 1 INT 2 GND
LNG2DMTR_LGA12_2X2
<8,20,21,34> PCH_SMBDATA
<8,20,21,34> PCH_SMBCLK
FFS_INT1 <8>
FFS_INT2 <9>
+5VALW
US2
IN EN OUT GND OCB
SY6288D20AAC_SOT23-5
<8> HDD_EN_PCH
CS8 1U_0402_10V6K
RS5 10K_0402_5%
RS4 FFS@ 100K_0402_5%
FFS@ RS3 100K_0402_5%
FFS_INT2_Q
QS1B FFS@ DMN66D0LDW-7_SOT363-6
QS1A FFS@ DMN66D0LDW-7_SOT363-6
FFS_INT2

CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

Main Func = ODD



+5VS
JP6
Always Short
PJP@
JUMP_43X79
60 mils
+5VS_ODD
CS13 ODD@ 1000P_0402_50V7K
CS14 ODD@ 0.1U_0402_25V6K
CS15 ODD@ 10U_0805_10V6K
JODD1
ACES_50673-0120N-P01
SP01002HK00
CONN@
SATA_CTX_C_ODDRX_P1
SATA_CTX_C_ODDRX_N1
SATA_CRX_C_ODDTX_N1
SATA_CRX_C_ODDTX_P1
SATA_ODD_PRSNT#
SATA_ODD_DA#
TP46
CS12 CS11 CS10 CS9 ODD@
0.01U_0402_50V7K
<10> SATA_CTX_ODDRX_P1
<10> SATA_CTX_ODDRX_N1
<10> SATA_CRX_ODDTX_N1
<10> SATA_CRX_ODDTX_P1
SATA_ODD_PRSNT# <9>
RC194 ODD@ 10K_0402_5%
+3VS
SOC TX
SOC RX

CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSNT	P1	8
5V	P2	9
5V	P3	10 11
Attention	P4	12
GND	P5	
GND	P6	

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

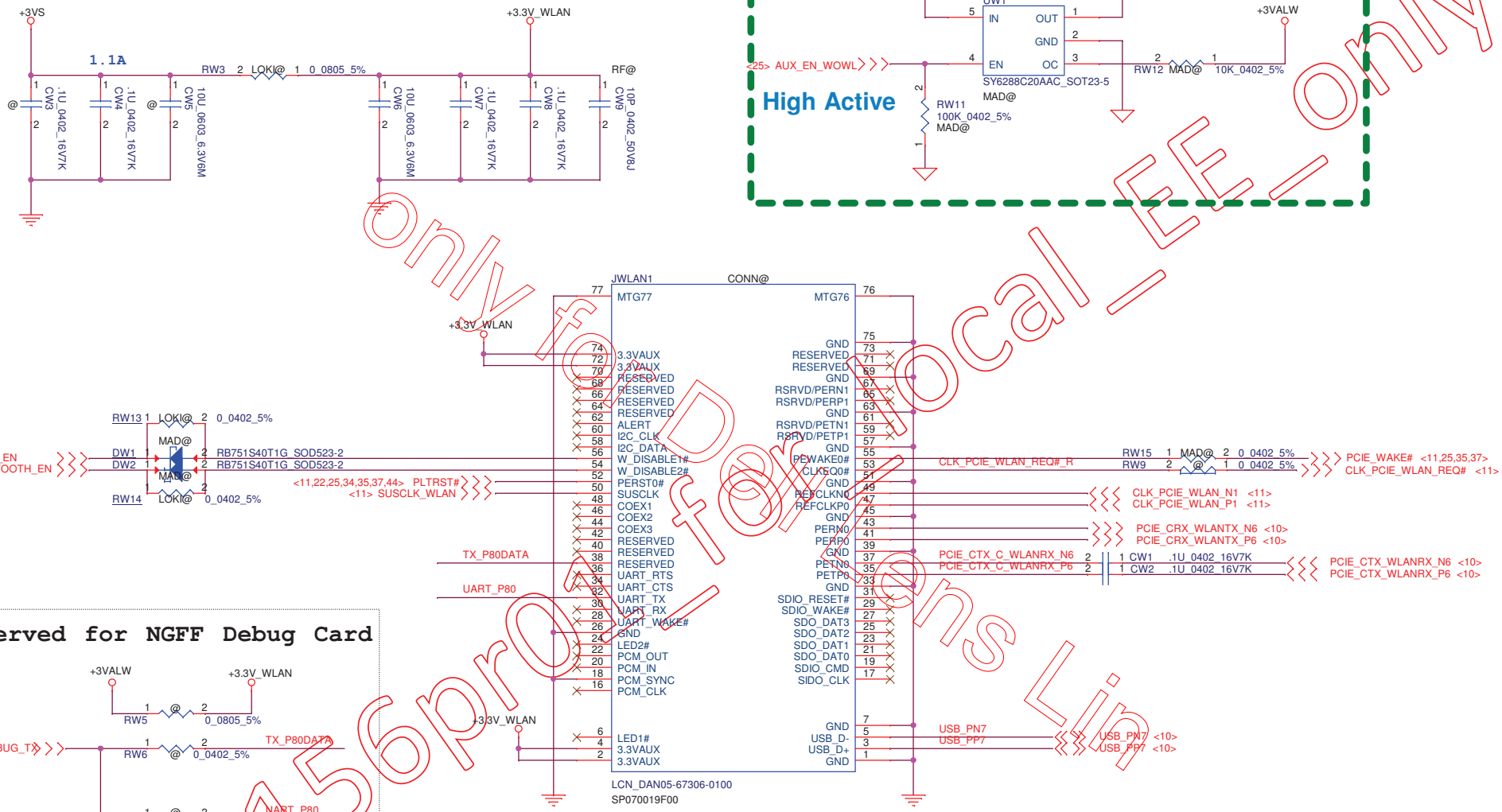
Compal Electronics, Inc.

Title: **HDD/FFS/ODD**

Size: Custom | Document Number: **LA-F115P** | Rev: 0.1

Main Func = WLAN

A Key CONN



Reserved for NGFF Debug Card

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

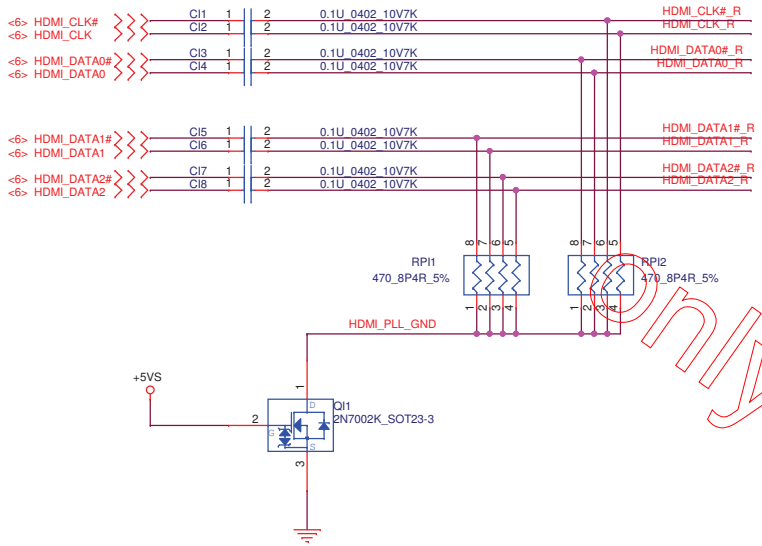
Compal Electronics, Inc.

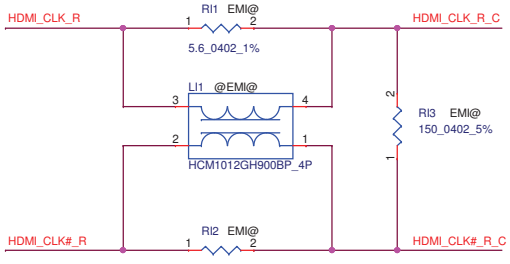
Title: NGFF WLAN CONN

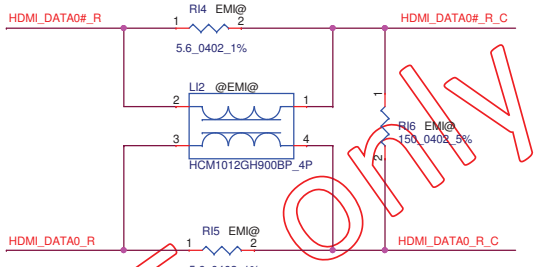
Size | Document Number: LA-F115P | Rev: 0.1

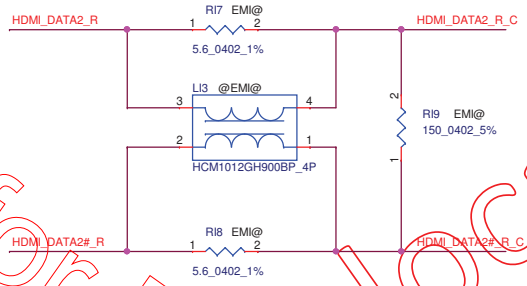
Date: Friday, March 02, 2018 | Sheet 32 of 65

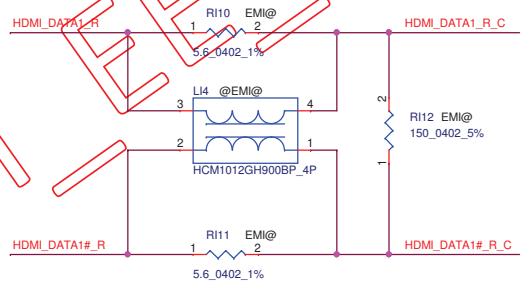
Main Func = HDMI

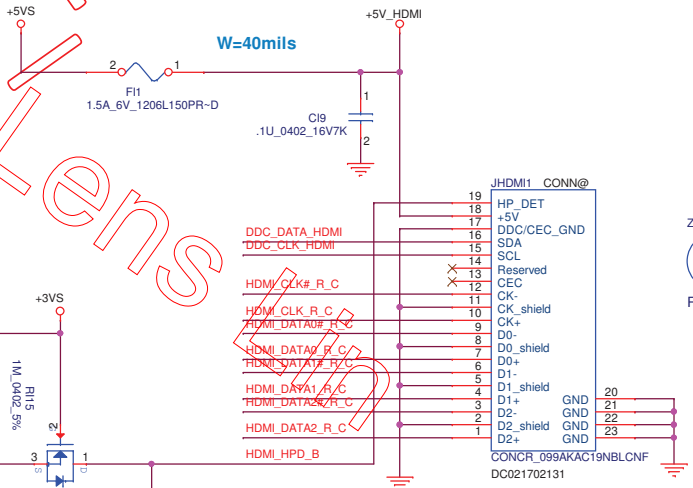


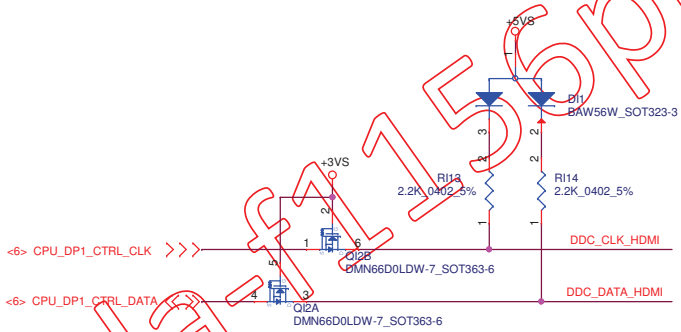












Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

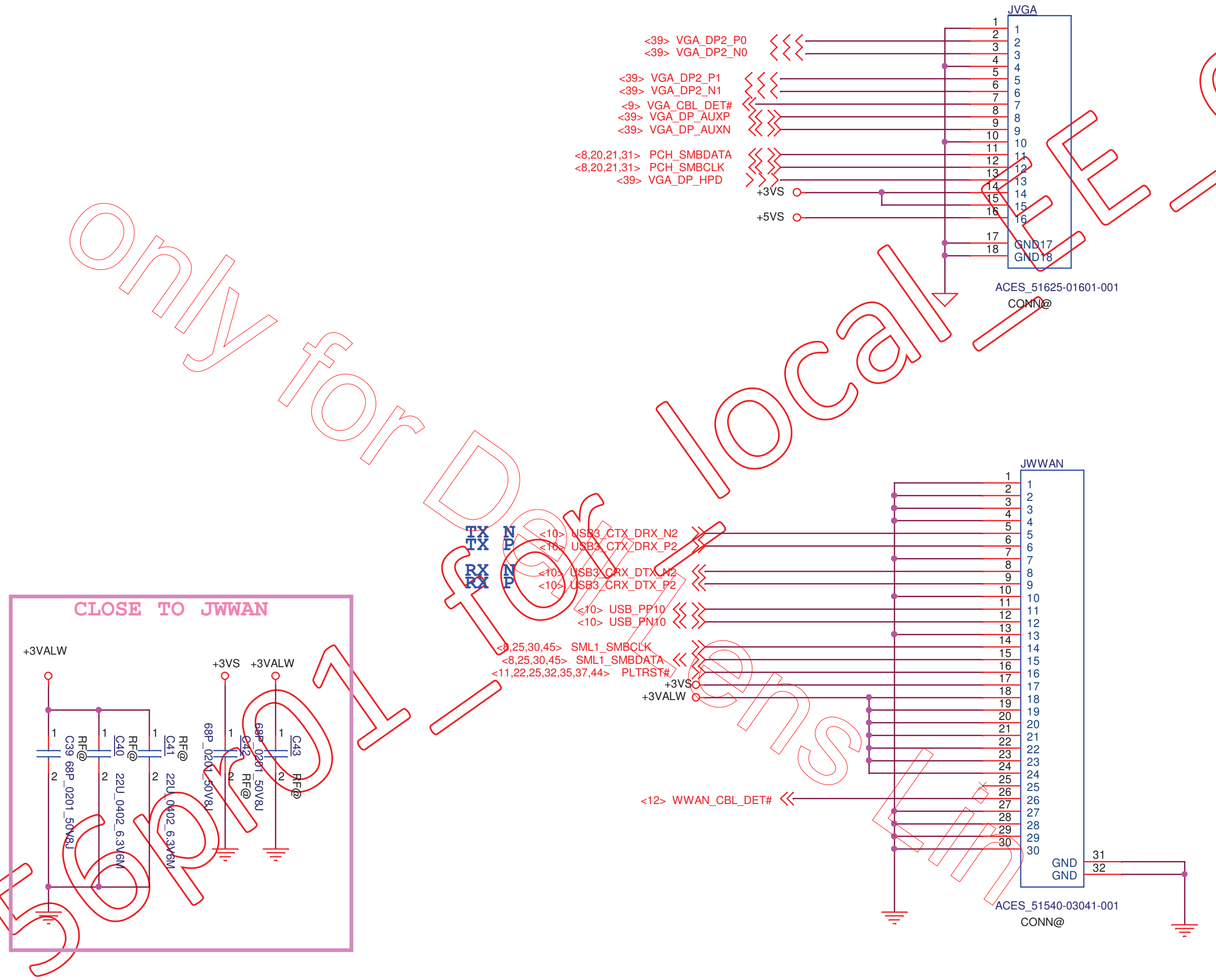
Compal Electronics, Inc.

Title: **HDMI L.Shifter/Conn**

Size	Document Number	Rev
	LA-F115P	0.1

Date: Friday, March 02, 2018 | Sheet 33 of 65

Main Func = WWAN/B & VGA/B



JVGA
<39> VGA_DP2_P0
<39> VGA_DP2_N0
<39> VGA_DP2_P1
<39> VGA_DP2_N1
<9> VGA_CBL_DET#
<39> VGA_DP_AUXP
<39> VGA_DP_AUXN
<8,20,21,31> PCH_SMBDATA
<8,20,21,31> PCH_SMBCLK
<39> VGA_DP_HPD
+3VS
+5VS
GND17
GND18
ACES_51625-01601-001
CONN@
JWWAN
TX N
TX P
RX N
RX P
<10> USB3_CTX_DRX_N2
<10> USB3_CTX_DRX_P2
<10> USB3_CRX_DTX_N2
<10> USB3_CRX_DTX_P2
<10> USB_PP10
<10> USB_PN10
<8,25,30,45> SML1_SMBCLK
<8,25,30,45> SML1_SMBDATA
<11,22,25,32,35,37,44> PLTRST#
+3VS
+3VALW
<12> WWAN_CBL_DET#
GND
GND
ACES_51540-03041-001
CONN@
CLOSE TO JWWAN
+3VALW
+3VS
+3VALW
C39 68P_0201_50V8J RF@
C40 22U_0402_6.3V6M RF@
C41 22U_0402_6.3V6M RF@
C42 68P_0201_50V8J RF@
C43 68P_0201_50V8J RF@

RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.08106.0003): 10/100M <70mW.

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

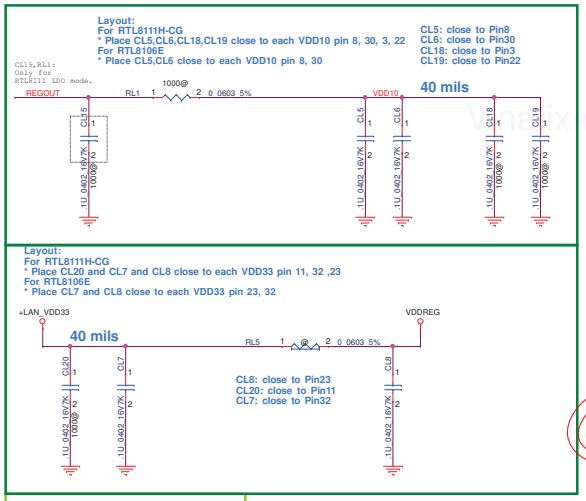
Title: IO DB(WWAN/VGA)

Size / Document Number: LA-F115P — Rev 0.1

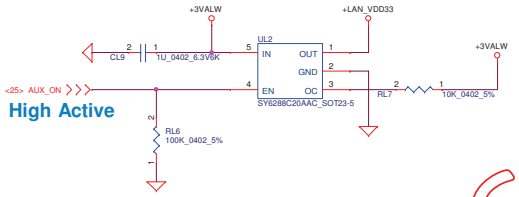
Date: Friday, March 02, 2018 —

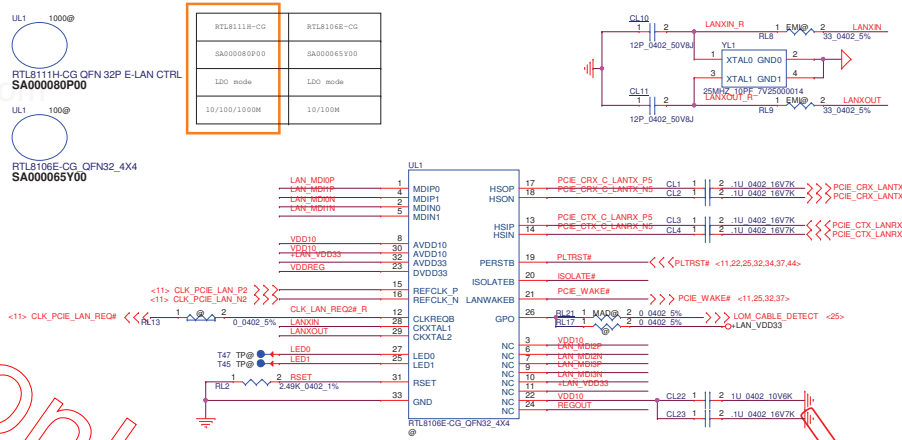
Main Func = LAN

LAN Chip (10/100/1000M & 10/100M co-layout)

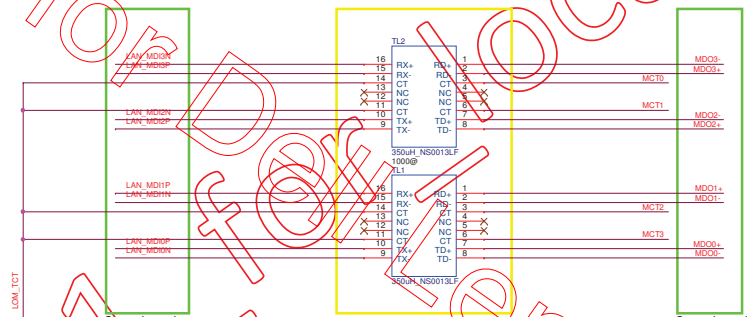


+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.





LAN TransFormer (10/100/1000M & 10/100M co-layout)



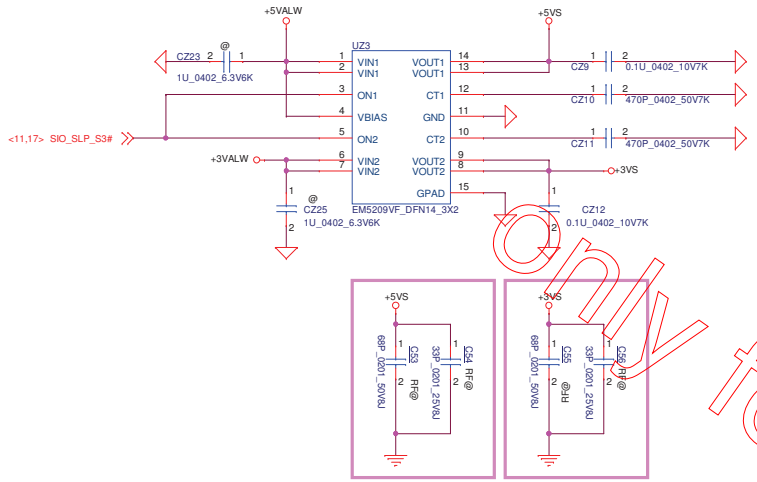
	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

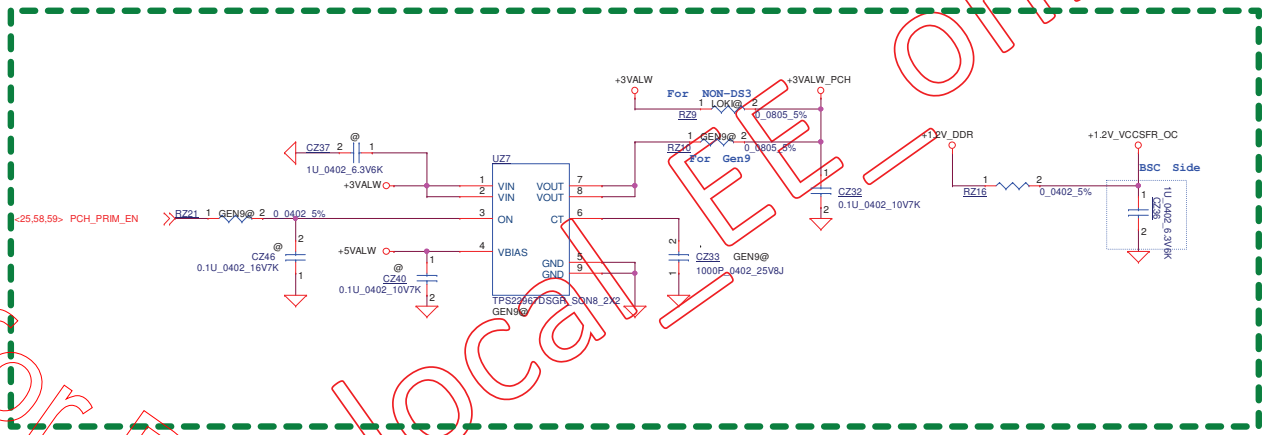
Compal Electronics, Inc.			
Title	P35-LAN RTL8111/RTL8106		
Size	Document Number	Rev	
	LA-F115P	0.1	
Date:	Friday, March 02, 2018	Sheet	35 of 65

Main Func = DC/DC

+5VS/+3VS for System



+3VALW_PCH for System
+1.2V_DDR TO +1.2V_VCCSFR_OC



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: DC/DC

Size | Document Number: LA-F115P | Rev: 0.1

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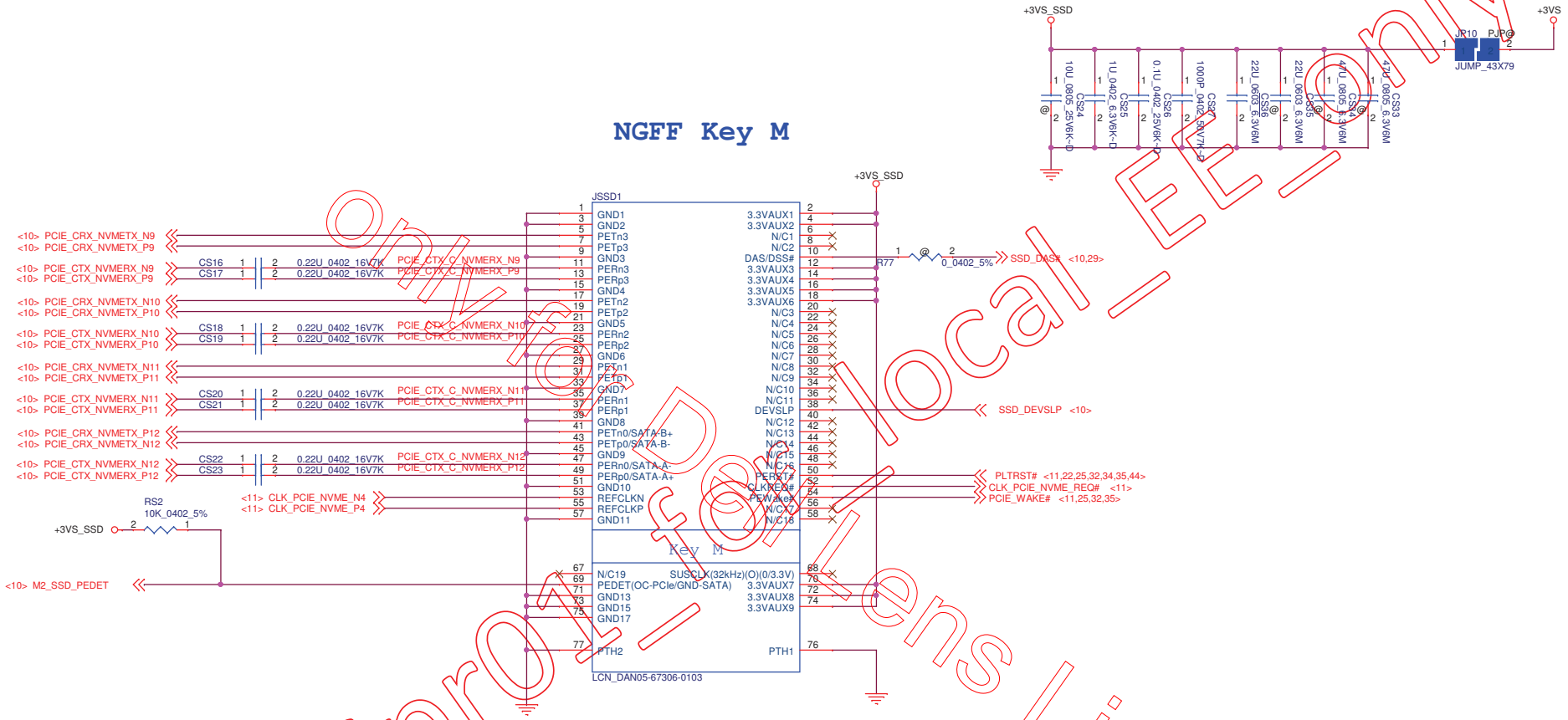
Main Func = SSD

M Key CONN

NGFF Key M

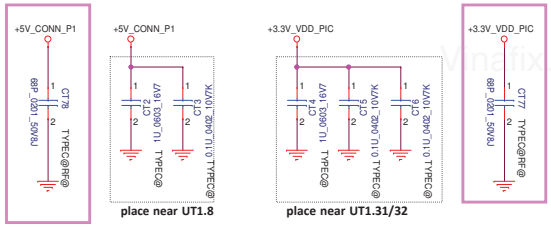


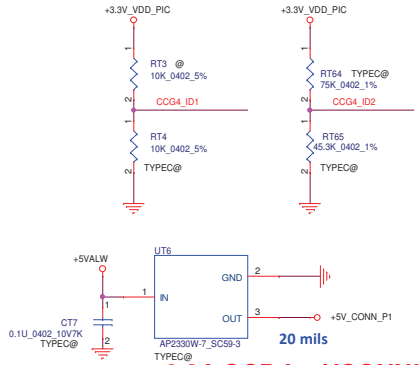
PEDET	Module Type
0	SATA
1	PCIE

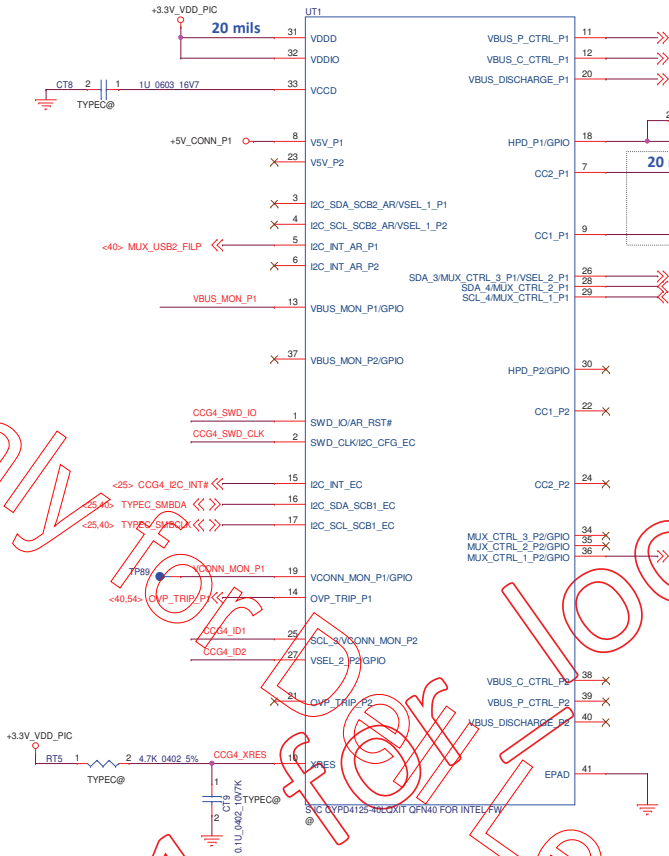
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

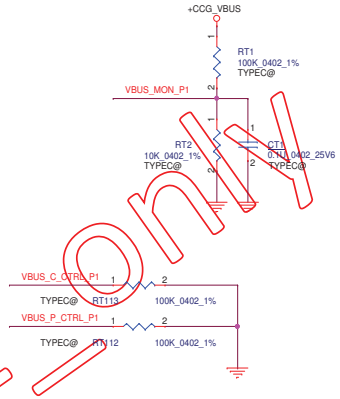
Compal Electronics, Inc.			
Title: NVME SSD			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, March 02, 2018	Sheet 37 of 65		

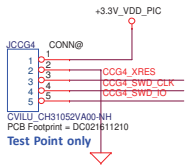
Main Func = CCG4

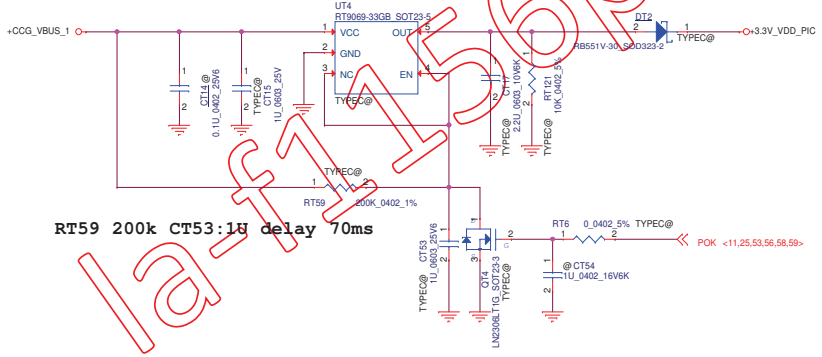












Voltages for various platform on "CCG4_ID_1" pin and "CCG4_ID_2" pin

#	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1	Single Port - Intel - DDM support - Armani 13" & 14"	L0	L7
2	Single Port - Intel - DDM support - Kyloren	L0	L6
3	Single Port - Intel - DDM support - Miyake	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - StarLord KBL - R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

Voltage level	Voltage value
L0	0V
L1	3.3V
L2	3.3V/2
L3	3.3V/3
L4	3.3V/4
L5	3.3V/5
L6	3.3V/6
L7	3.3V/7

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: Cypress PD Control

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018 | Sheet 38 of 65

Main Func = typec MUX & DP MUX

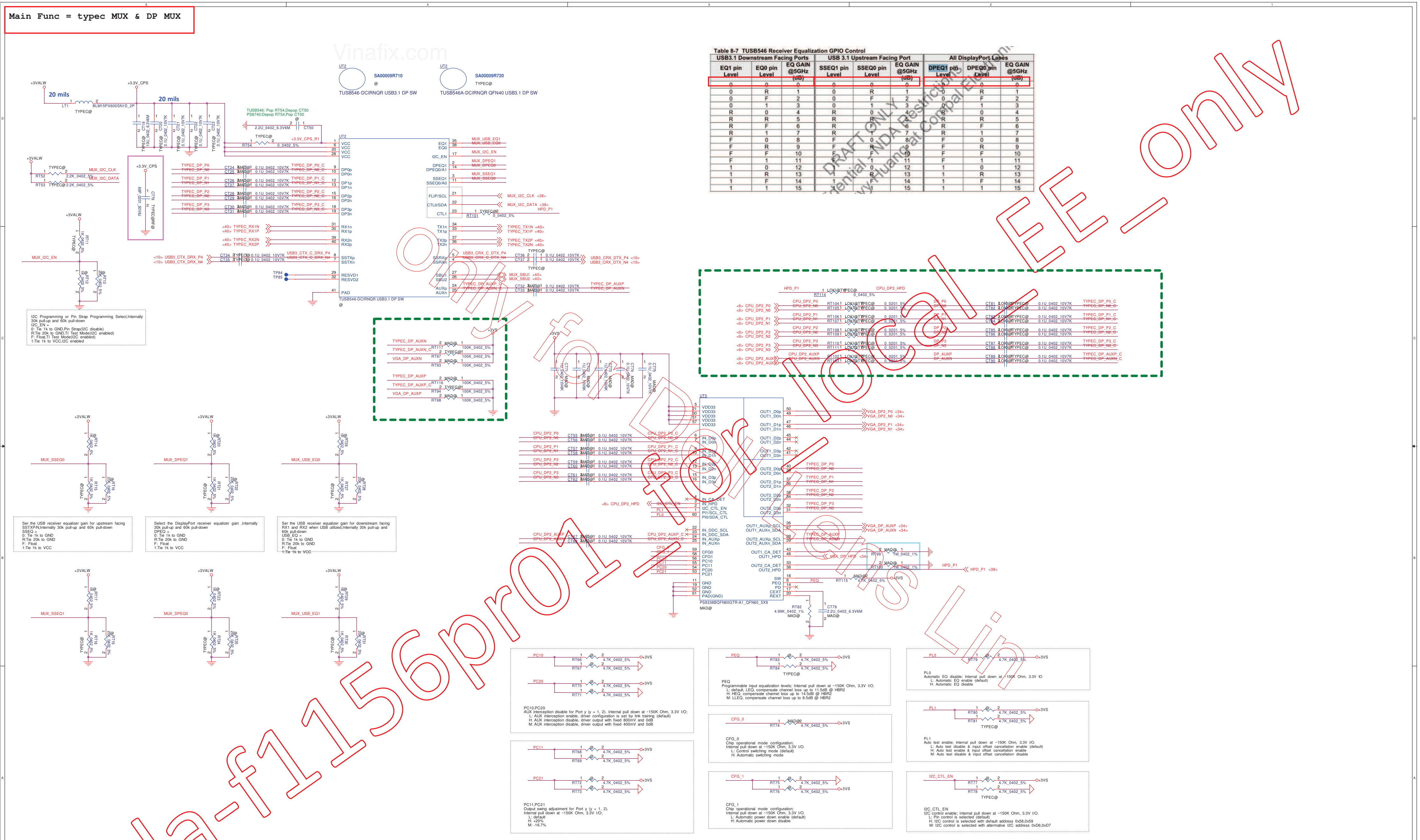


Table 8-7 TUSB546 Receiver Equalization GPIO Control

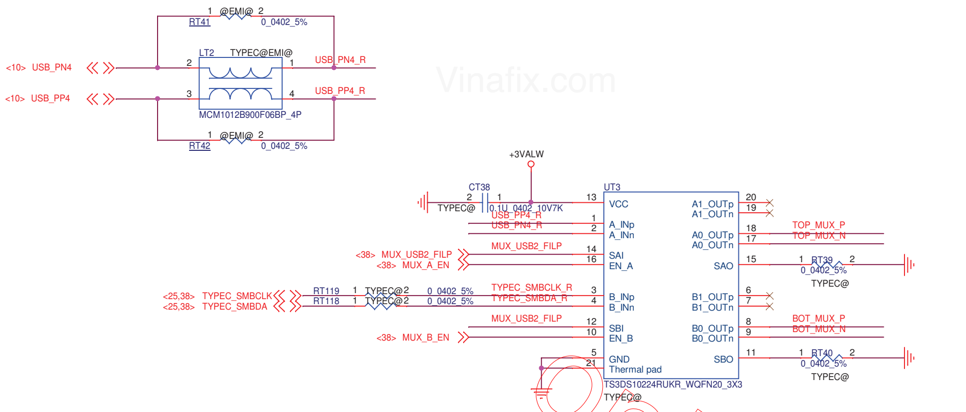
USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title: Dual Role Mux

Size | Document Number: LA-F115P | Rev 0.1

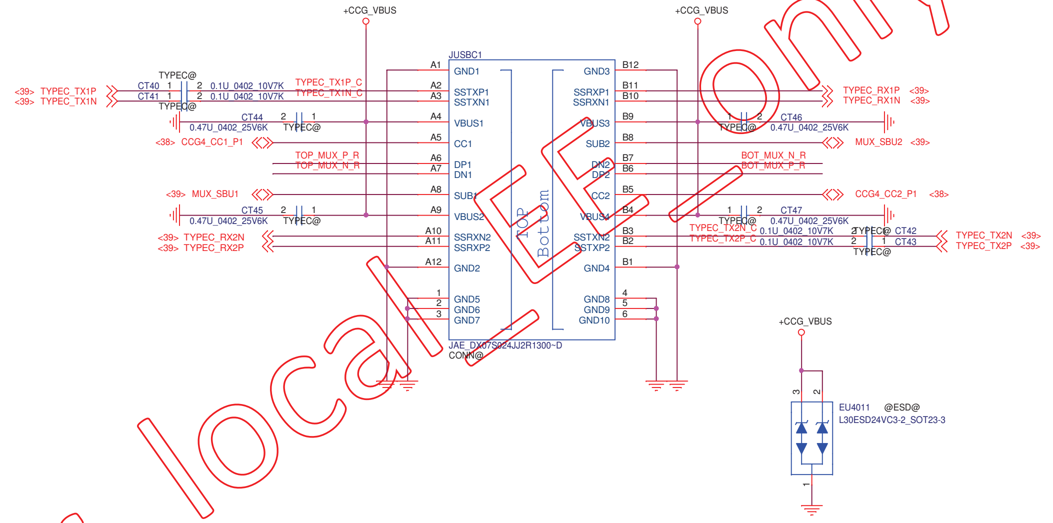
Main Func = USB2/I2C Mux

Close to JUSBC1 <500mil



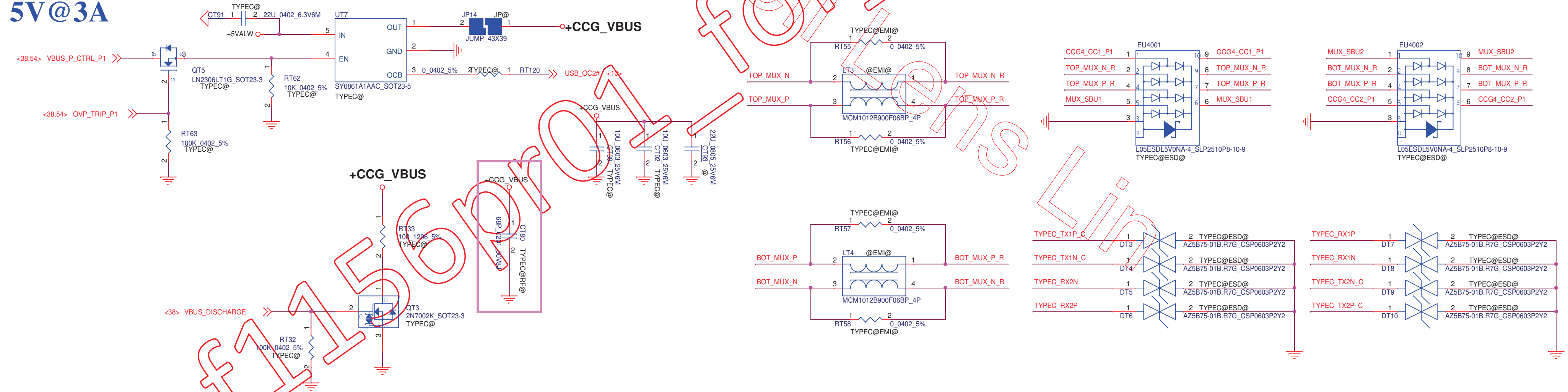
USB_PN4
USB_PP4
USB_PN4_R
USB_PP4_R
RT41
RT42
LT2
TYPEC@EMI@
MCM1012B900F06BP_4P
+3VALW
CT38
UT3
VCC
A_INp
A_INn
SAI
EN_A
SAO
B_INp
B_INn
SBI
EN_B
SBO
GND
Thermal pad
A1_OUTp
A1_OUTn
A0_OUTp
A0_OUTn
B1_OUTp
B1_OUTn
B0_OUTp
B0_OUTn
MUX_USB2_FILP
MUX_A_EN
MUX_B_EN
TYPEC_SMBCLK
TYPEC_SMBDA
TYPEC_SMBCLK_R
TYPEC_SMBDA_R
RT119
RT118
TOP_MUX_P
TOP_MUX_N
BOT_MUX_P
BOT_MUX_N
RT39
RT40
TS3DS10224RUKR_WQFN20_3X3
TYPEC@

MUX_USB2_FILP	MUX_A_EN	MUX_B_EN	A0_OUT	B0_OUT
0	0	1	--	USB2
0	1	1	I2C	USB2
1	1	0	USB2	--
1	1	1	USB2	I2C



+CCG_VBUS
JUSBC1
GND1
SSTXP1
SSTXN1
VBUS1
CC1
DP1
DN1
SUB1
VBUS2
SSRXN2
SSRXP2
GND2
GND3
SSRXP1
SSRXN1
VBUS3
SUB2
DN2
DP2
CC2
VBUS4
SSTXN2
SSTXP2
GND4
TYPEC_TX1P
TYPEC_TX1N
TYPEC_RX1P
TYPEC_RX1N
TYPEC_RX2N
TYPEC_RX2P
TYPEC_TX2N
TYPEC_TX2P
CCG4_CC1_P1
CCG4_CC2_P1
MUX_SBU1
MUX_SBU2
TOP_MUX_P_R
TOP_MUX_N_R
BOT_MUX_N_R
BOT_MUX_P_R
JAE_DX07S024JJ2R1300~D
CONN@
EU4011
@ESD@
L30ESD24VC3-2_SOT23-3

5V@3A



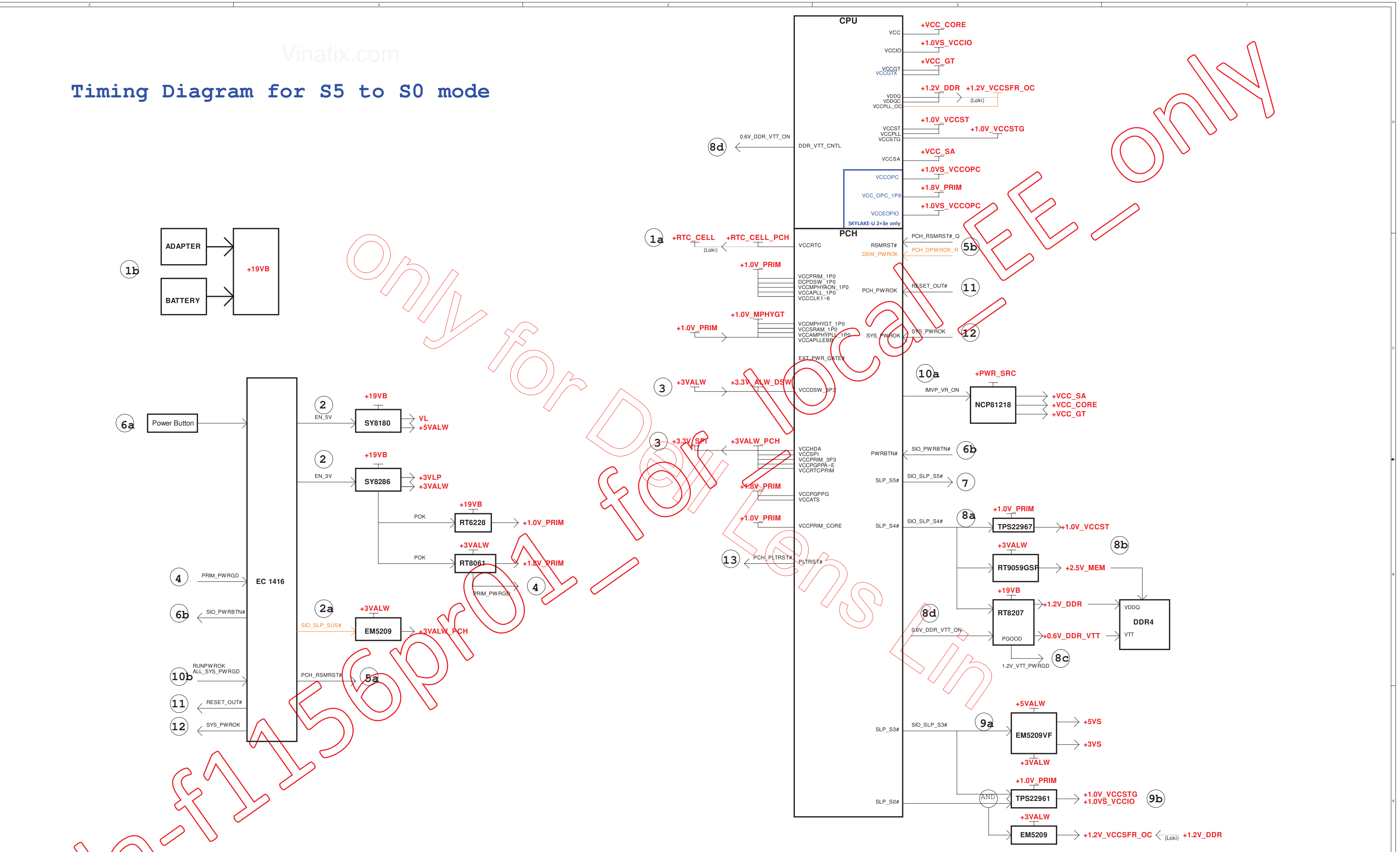
CT91
22U_0402_6.3V6M
+5VALW
UT7
IN
EN
OUT
GND
OCB
SY6861A1AAC_SOT23-5
JP14
JUMP_43X39
+CCG_VBUS
VBUS_P_CTRL_P1
OVP_TRIP_P1
QT5
LN2306LT1G_SOT23-3
RT62
RT63
RT120
USB_OC2#
VBUS_DISCHARGE
QT3
2N7002K_SOT23-3
RT33
RT32
CT80
EU4001
EU4002
L05ESDL5V0NA-4_SLP2510P8-10-9
TYPEC@ESD@
LT3
LT4
RT55
RT56
RT57
RT58
MCM1012B900F06BP_4P
DT3
DT4
DT5
DT6
DT7
DT8
DT9
DT10
AZ5B75-01B.R7G_CSP0603P2Y2

Type-C 5V Provide Path Control

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.
Title: TYPE-C
Size / Document Number: LA-F115P
Rev 0.1
Date: Friday, March 02, 2018

Timing Diagram for S5 to S0 mode

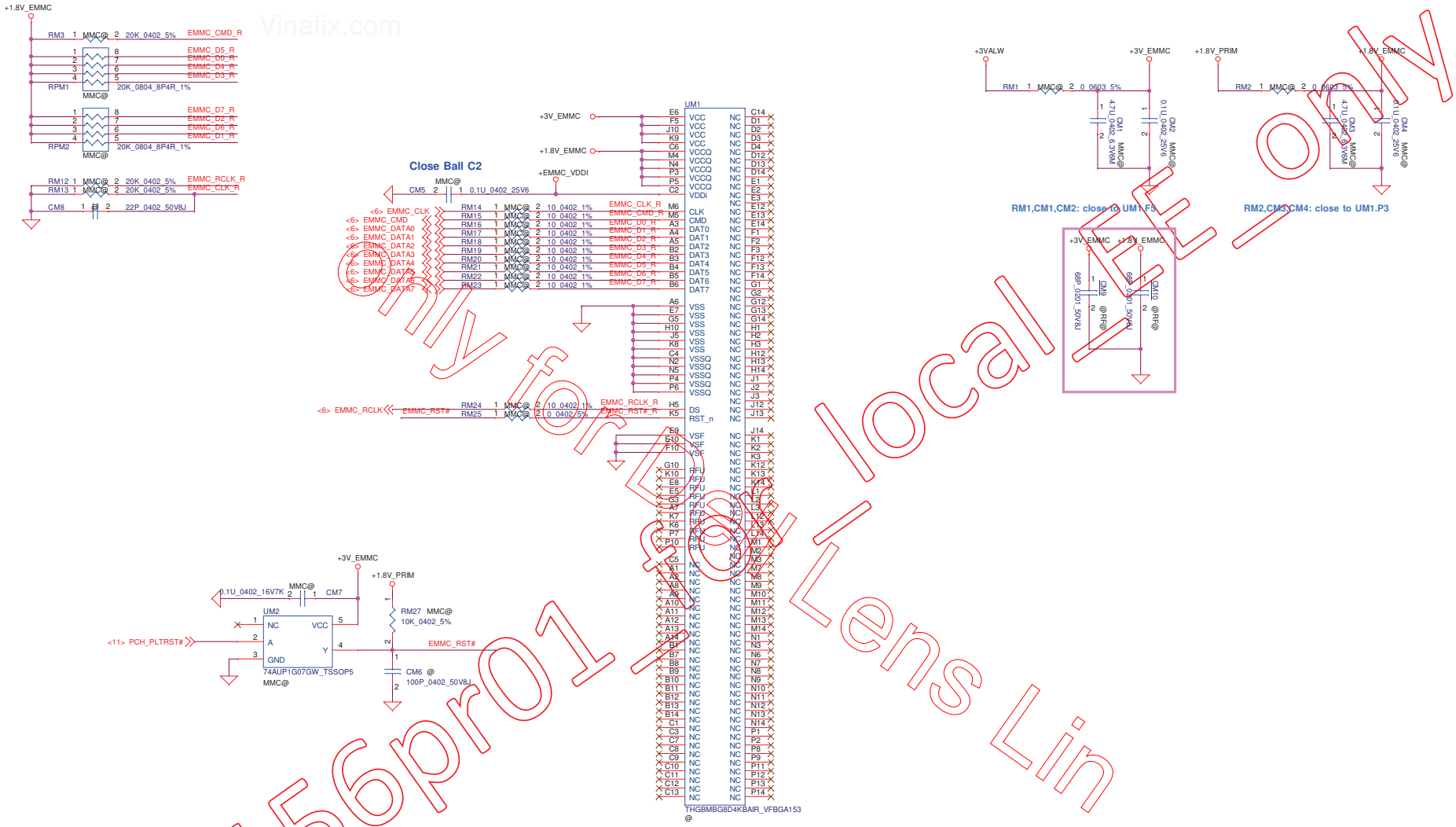


Compal Electronics, Inc.

Title: Platform Power Sequence

Document Number: LA-F115P   Rev 0.1

Main Func = eMMC

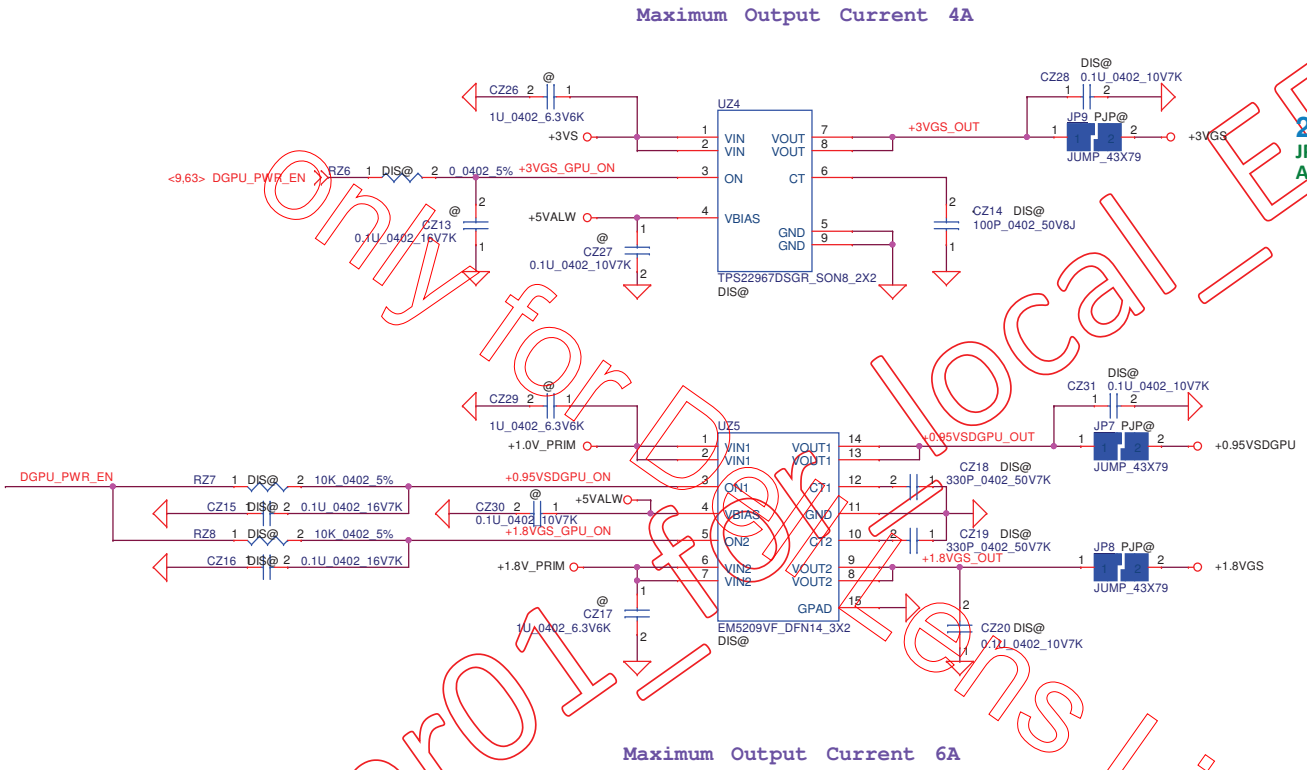


Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	RAV for eMMC		
Size	Document Number	LA-F115P	Rev 0.1
Date: Friday, March 02, 2018	Sheet 42 of 65		

Main Func = GPU

+3V/+0.95V/+1.8V for GPU



250mA
JP9
Always Short

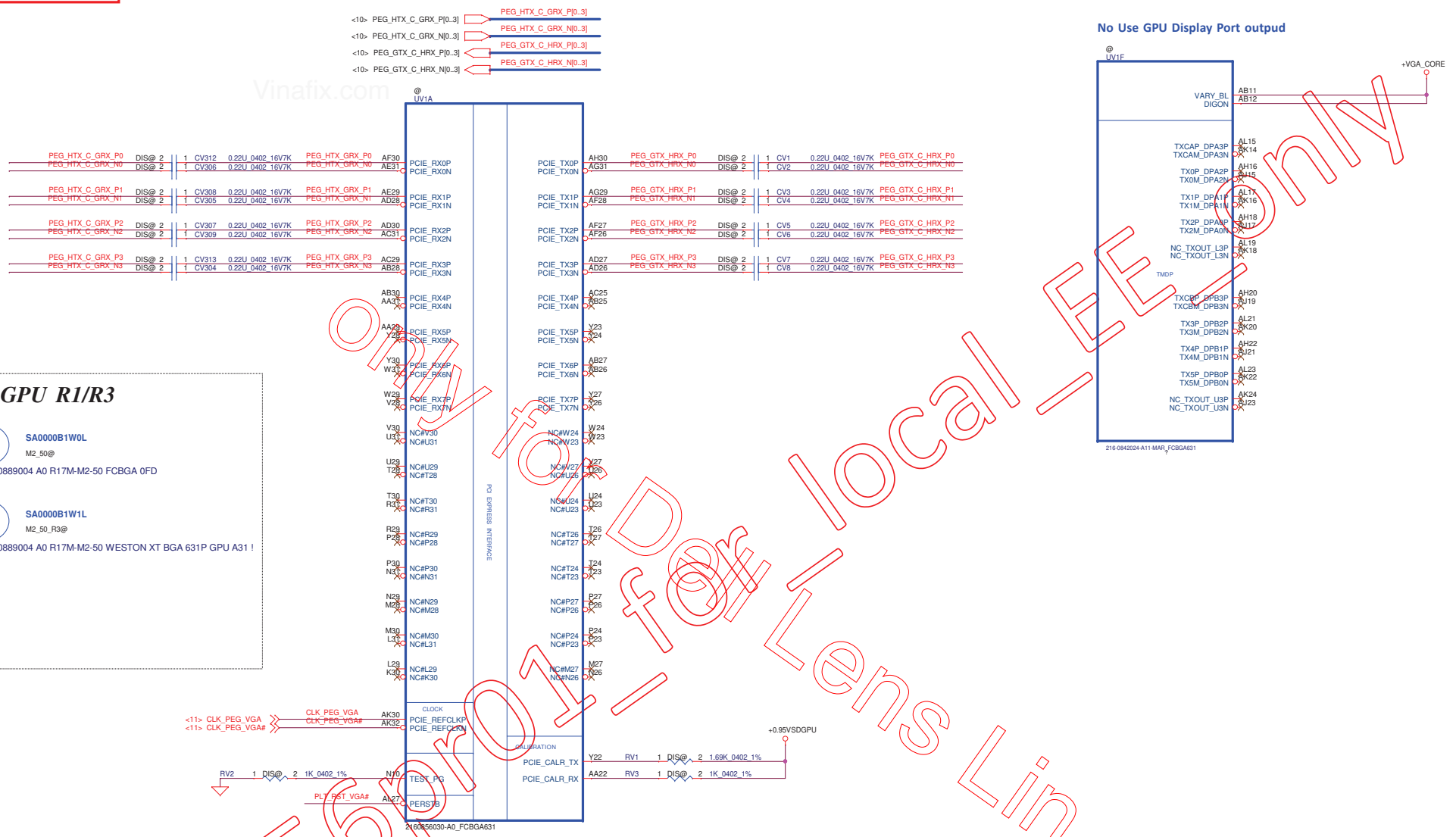
2300mA
JP7
Always Short

500mA
JP8
Always Short

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.		
Title: GPU Power		
Size	Document Number: LA-F115P	Rev: 0.1
Date: Friday, March 02, 2018	Sheet 43 of 65	

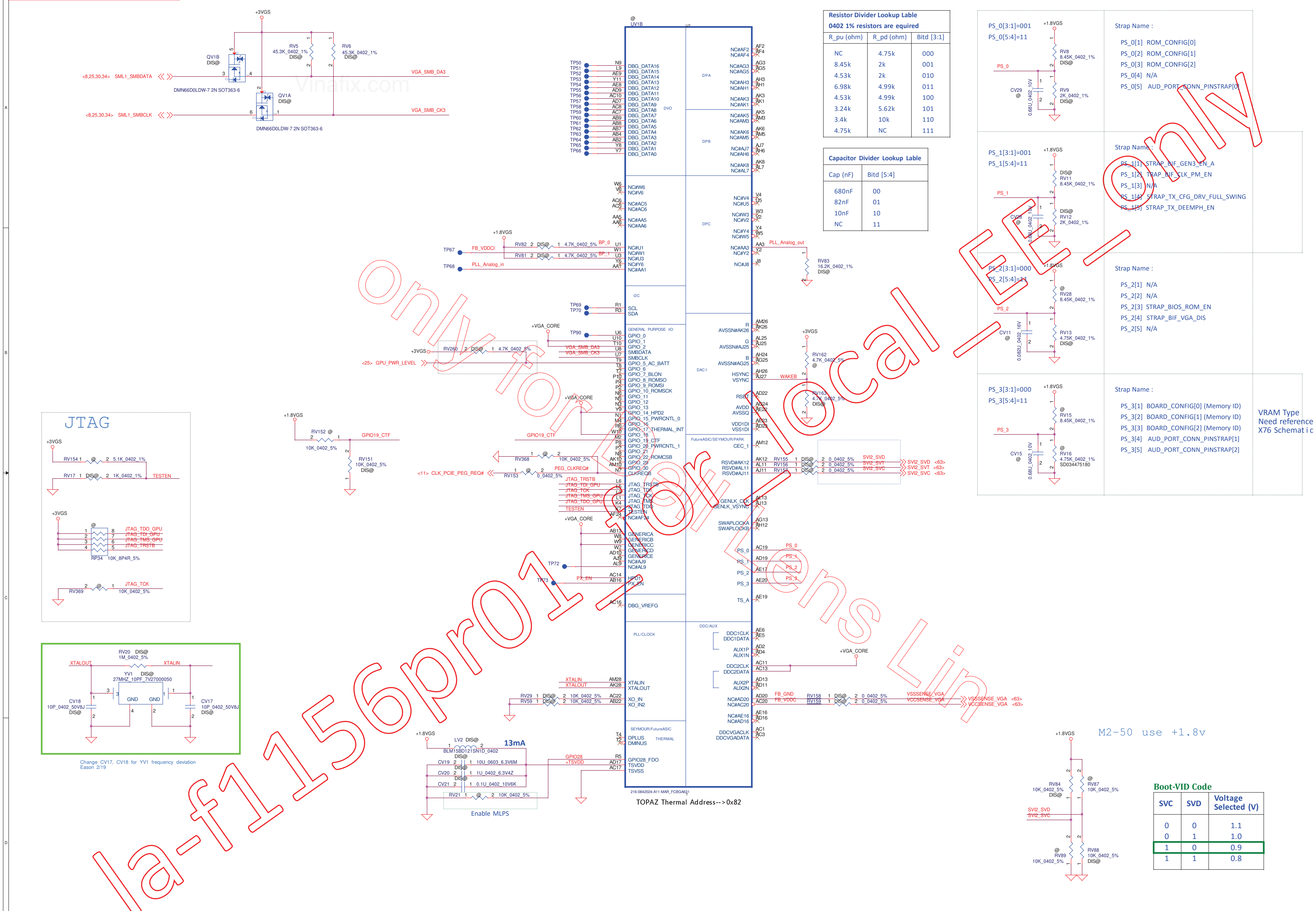
Main Func = GPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MESO_(1/5)_PCIE/DP		
Size	Document Number		Rev
	LA-F115P		0.1
Date:	Friday, March 02, 2018	Sheet	44 of 65

Main Func = GPU



UV1B
DBG_DATA16 … DBG_DATA0
GENERAL PURPOSE I/O
JTAG
XTALIN
XTALOUT
TOPAZ Thermal Address-->0x82
Enable MLPS
13mA
Change CV17, CV18 for YV1 frequency deviation Eason 2/19
VRAM Type Need reference X76 Schematic
M2-50 use +1.8v
PS_0[3:1]=001
PS_0[5:4]=11
PS_1[3:1]=001
PS_1[5:4]=11
PS_2[3:1]=000
PS_2[5:4]=11
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Resistor Divider Lookup Lable

0402 1% resistors are equired

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

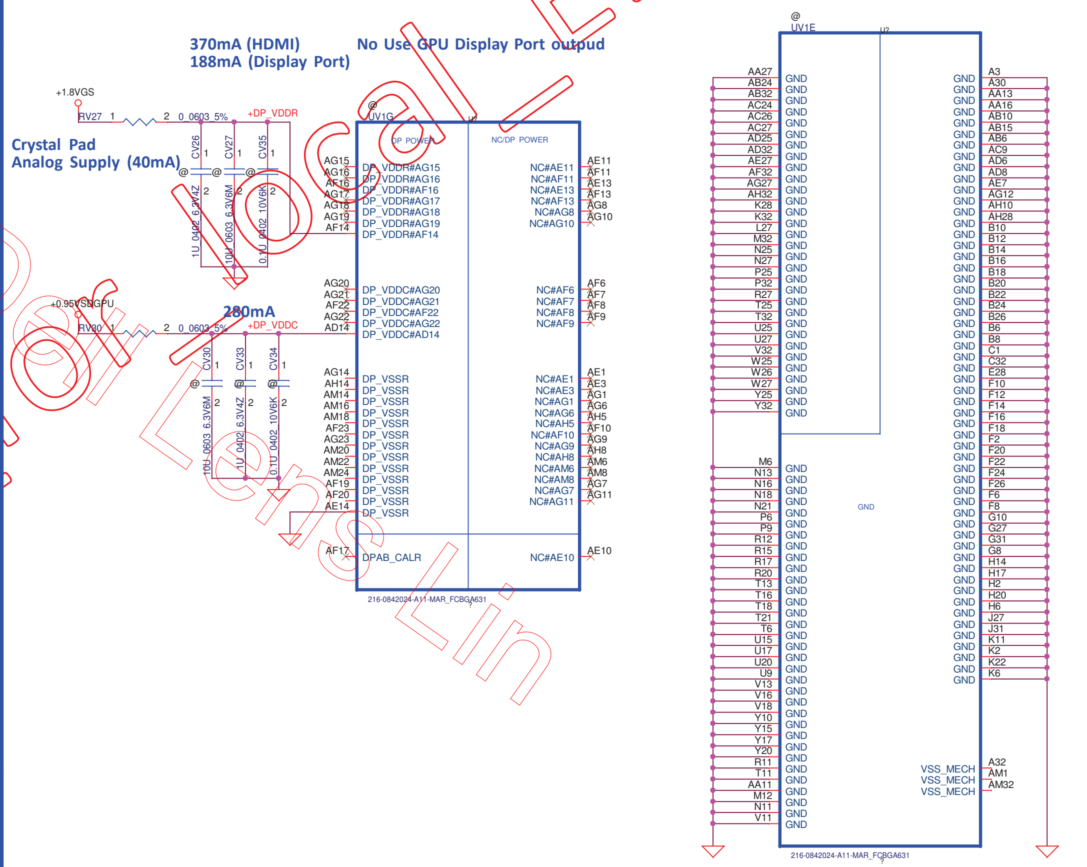
Compal Electronics, Inc.

Title: MESO_(2/5)_MSIC

Size / Document Number: LA-F115P — Rev 0.1

Date: Friday, March 02, 2018 — Sheet 45 of 65

Main Func = GPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **MESO_(3/5)_Power/GND**

Size | Document Number: **LA-F115P** | Rev 0.1

Main Func = GPU

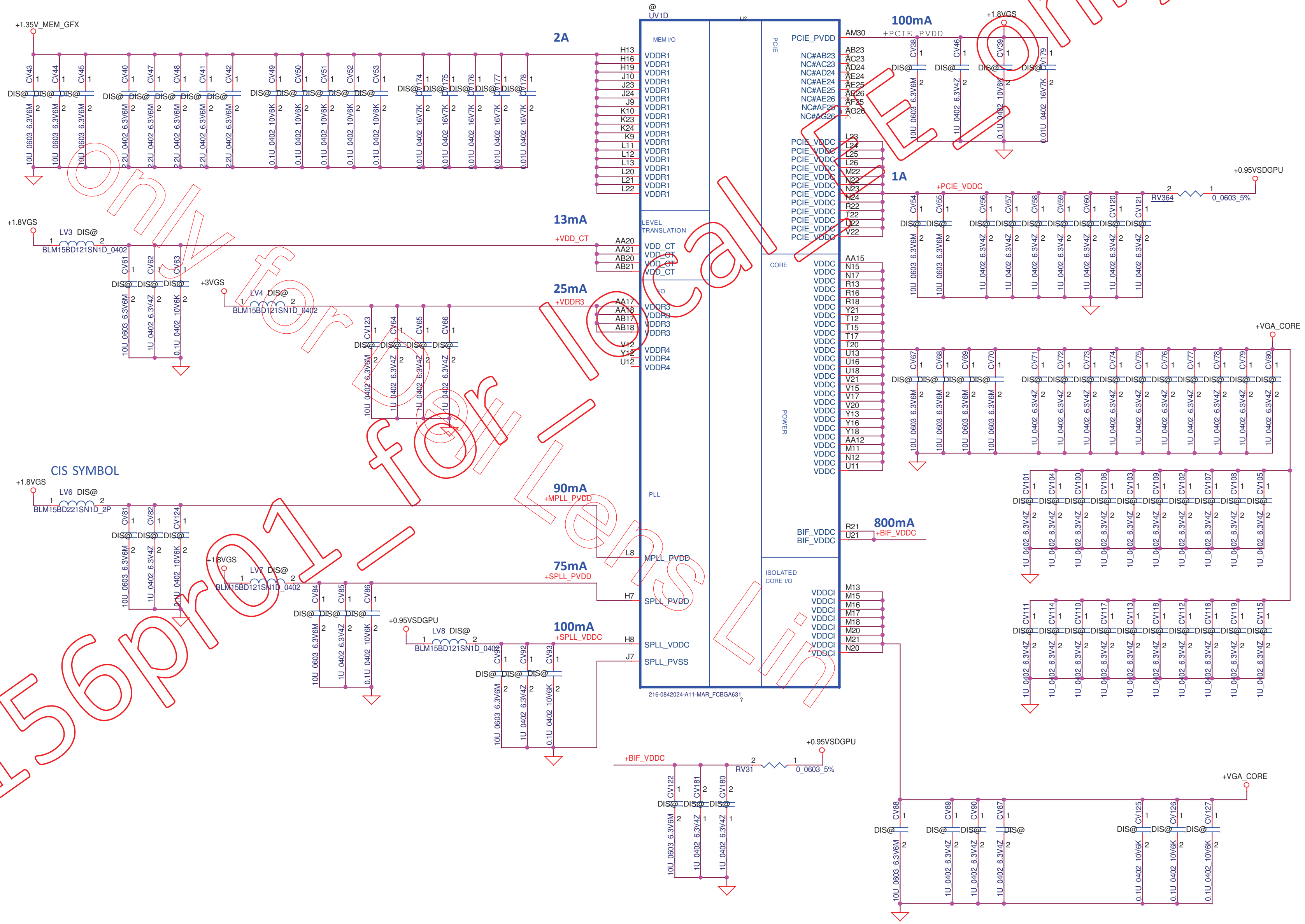
+VGA_CORE	10uF	1uF	0.1uF
VDDC	4	30	0
VDDCI	1	3	3

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	2	7	0
BIF_VDDC	1	2	0
SPLL_VDDC	1	1	1
+DP_VDDC	0	0	0

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1	3	5	5	5

+1.8VGS	10uF	1uF	0.1uF
PCIE_PVDD	1	1	1
MPLL_PVDD	1	1	1
SPLL_PVDD	1	1	1
VDDR4 (NC)	0	0	0
VDD_CT	1	1	1
+TSVDD	1	1	1
+DP_VDDR	0	0	0

+3VGS	10uF	1uF	0.1uF
VDDR3	1	3	0



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

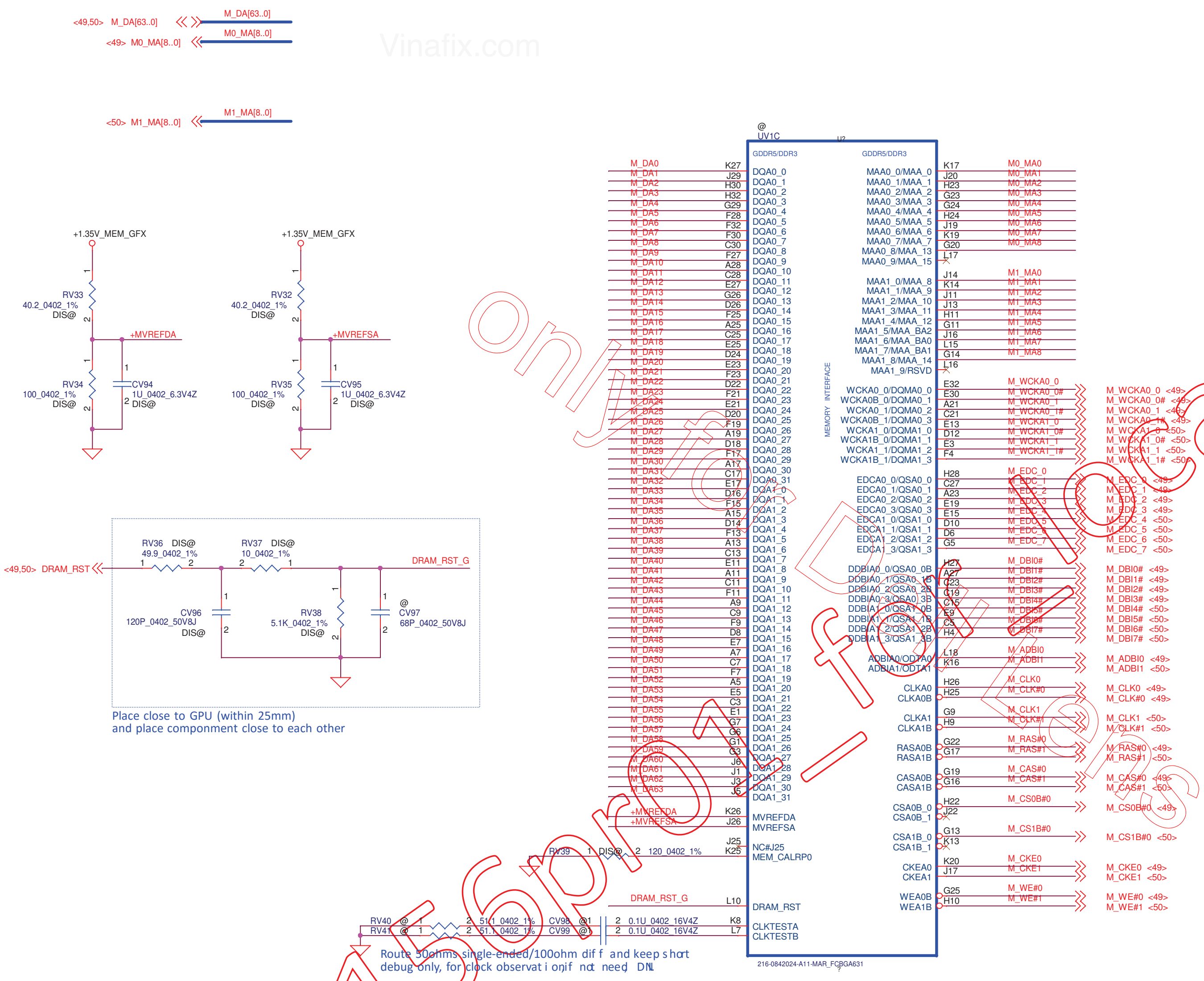
Compal Electronics, Inc.

Title: MESO_(4/5)_Power

Size: Custom | Document Number: LA-F115P | Rev: 0.1

Date: Friday, March 02, 2018

Main Func = GPU



<49,50> M_DA[63..0]
M_DA[63..0]
<49> M0_MA[8..0]
M0_MA[8..0]
<50> M1_MA[8..0]
M1_MA[8..0]
+1.35V_MEM_GFX
RV33 40.2_0402_1% DIS@
RV32 40.2_0402_1% DIS@
+MVREFDA
+MVREFSA
RV34 100_0402_1% DIS@
CV94 1U_0402_6.3V4Z DIS@
RV35 100_0402_1% DIS@
CV95 1U_0402_6.3V4Z DIS@
RV36 DIS@ 49.9_0402_1%
RV37 DIS@ 10_0402_1%
<49,50> DRAM_RST
DRAM_RST_G
CV96 120P_0402_50V8J DIS@
RV38 5.1K_0402_1% DIS@
CV97 68P_0402_50V8J
Place close to GPU (within 25mm)
and place compponment close to each other
UV1C
GDDR5/DDR3
MEMORY INTERFACE
DQA0_0 … DQA0_31
DQA1_0 … DQA1_31
MVREFDA
MVREFSA
NC#J25
MEM_CALRP0
RV39 DIS@ 120_0402_1%
DRAM_RST
CLKTESTA
CLKTESTB
RV40 @ 51.1_0402_1%
RV41 @ 51.1_0402_1%
CV98 @ 0.1U_0402_16V4Z
CV99 @ 0.1U_0402_16V4Z
Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI
MAA0_0/MAA_0 … MAA0_9/MAA_15
MAA1_0/MAA_8 … MAA1_9/RSVD
WCKA0_0/DQMA0_0
WCKA0B_0/DQMA0_1
WCKA0_1/DQMA0_2
WCKA0B_1/DQMA0_3
WCKA1_0/DQMA1_0
WCKA1B_0/DQMA1_1
WCKA1_1/DQMA1_2
WCKA1B_1/DQMA1_3
EDCA0_0/QSA0_0 … EDCA1_3/QSA1_3
DDBIA0_0/QSA0_0B … DDBIA1_3/QSA1_3B
ADBIA0/ODTA0
ADBIA1/ODTA1
CLKA0
CLKA0B
CLKA1
CLKA1B
RASA0B
RASA1B
CASA0B
CASA1B
CSA0B_0
CSA0B_1
CSA1B_0
CSA1B_1
CKEA0
CKEA1
WEA0B
WEA1B
216-0842024-A11-MAR_FCBGA631
M_WCKA0_0 <49>
M_WCKA0_0# <49>
M_WCKA0_1 <49>
M_WCKA0_1# <49>
M_WCKA1_0 <50>
M_WCKA1_0# <50>
M_WCKA1_1 <50>
M_WCKA1_1# <50>
M_EDC_0 <49>
M_EDC_1 <49>
M_EDC_2 <49>
M_EDC_3 <49>
M_EDC_4 <50>
M_EDC_5 <50>
M_EDC_6 <50>
M_EDC_7 <50>
M_DBI0# <49>
M_DBI1# <49>
M_DBI2# <49>
M_DBI3# <49>
M_DBI4# <50>
M_DBI5# <50>
M_DBI6# <50>
M_DBI7# <50>
M_ADBI0 <49>
M_ADBI1 <50>
M_CLK0 <49>
M_CLK#0 <49>
M_CLK1 <50>
M_CLK#1 <50>
M_RAS#0 <49>
M_RAS#1 <50>
M_CAS#0 <49>
M_CAS#1 <50>
M_CS0B#0 <49>
M_CS1B#0 <50>
M_CKE0 <49>
M_CKE1 <50>
M_WE#0 <49>
M_WE#1 <50>

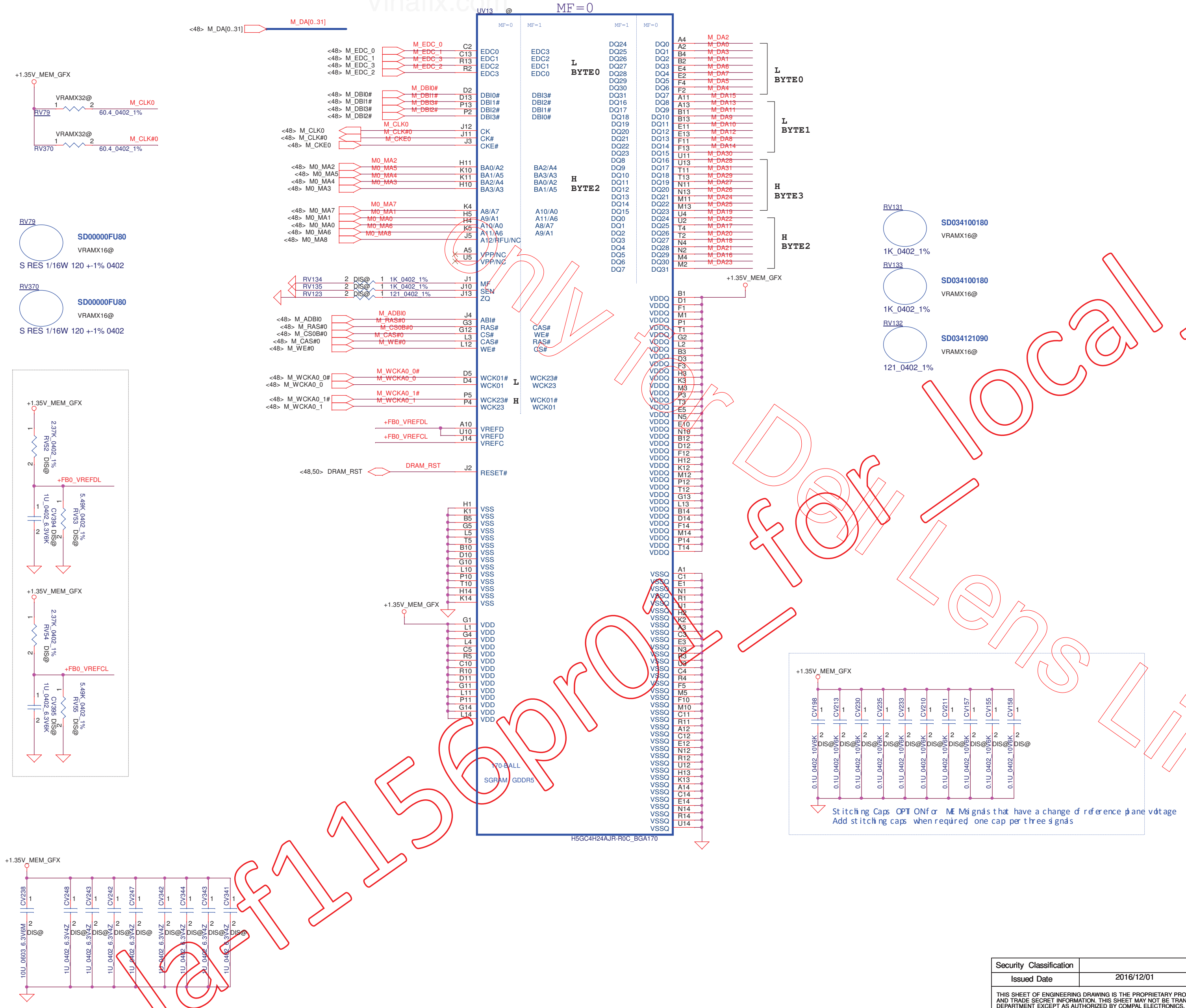
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MESO_(5/5)_MEM

Size | Document Number: LA-F115P | Rev 0.1

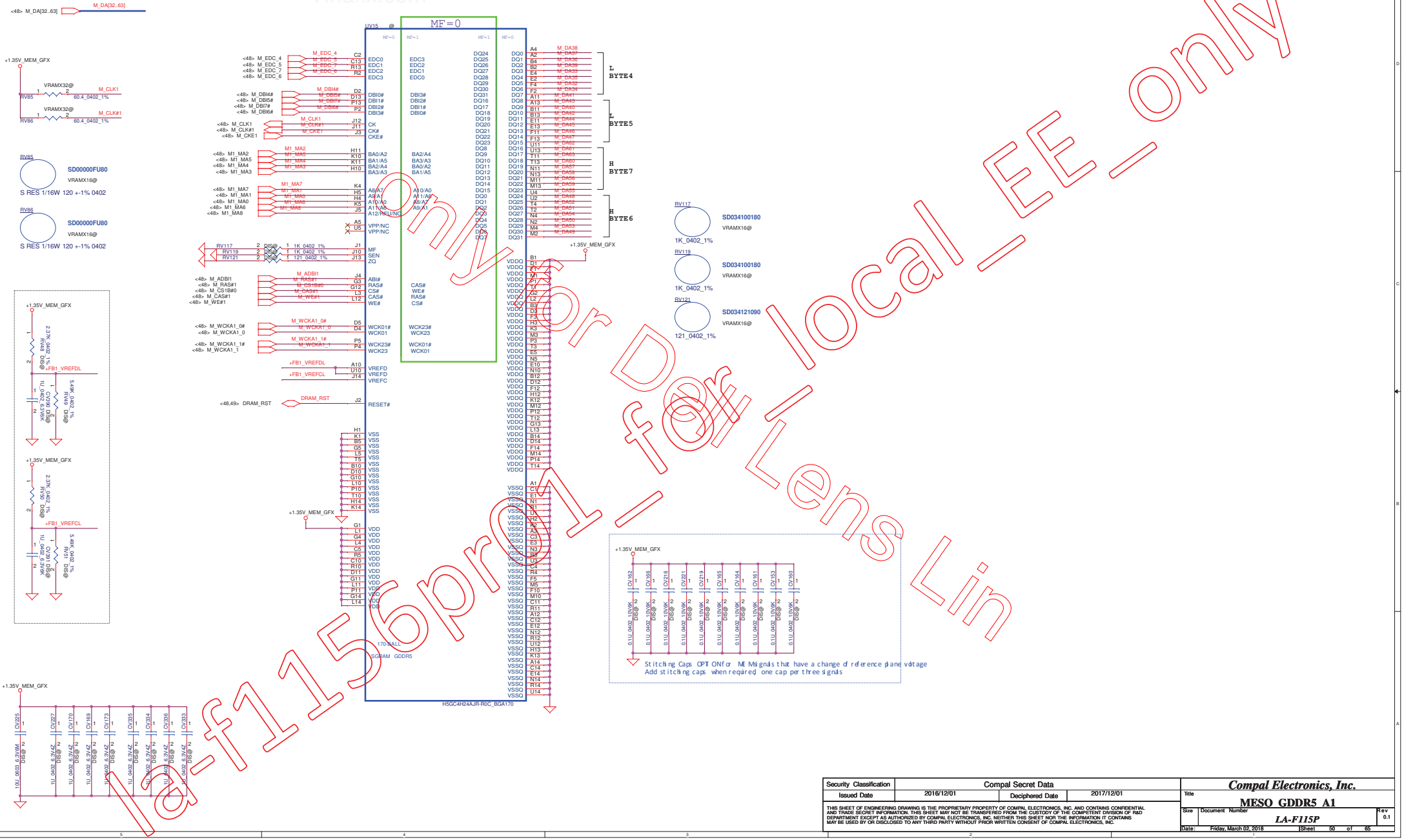
Main Func = GDDR5



UV13
MF=0
M_DA[0..31]
+1.35V_MEM_GFX
VRAMX32@
RV79
RV370
60.4_0402_1%
M_CLK0
M_CLK#0
SD00000FU80
VRAMX16@
S RES 1/16W 120 +-1% 0402
EDC0
EDC1
EDC2
EDC3
DBI0#
DBI1#
DBI2#
DBI3#
CK
CK#
CKE#
BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
A12/RFU/NC
VPP/NC
MF
SEN
ZQ
ABI#
RAS#
CS#
CAS#
WE#
WCK01#
WCK01
WCK23#
WCK23
VREFD
VREFC
RESET#
VSS
VDD
VDDQ
VSSQ
L BYTE0
L BYTE1
H BYTE2
H BYTE3
RV134
RV135
RV123
1K_0402_1%
121_0402_1%
RV131
RV133
RV132
SD034100180
SD034121090
+FB0_VREFDL
+FB0_VREFCL
DRAM_RST
2.37K_0402_1%
5.49K_0402_1%
1U_0402_6.3V6K
DIS@
170-BALL
SGRAM GDDR5
H5GC4H24AJR-R0C_BGA170
0.1U_0402_10V6K
10U_0603_6.3V6M
1U_0402_6.3V4Z
Stitching Caps OPTION for MEM signals that have a change of reference plane voltage
Add stitching caps when required, one cap per three signals

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title: MESO_GDDR5_A0
				Size / Document Number: LA-F115P / Rev 0.1
				Date: Friday, March 02, 2018 / Sheet 49 of 65

Main Func = GDDR5



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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Compal Electronics, Inc.

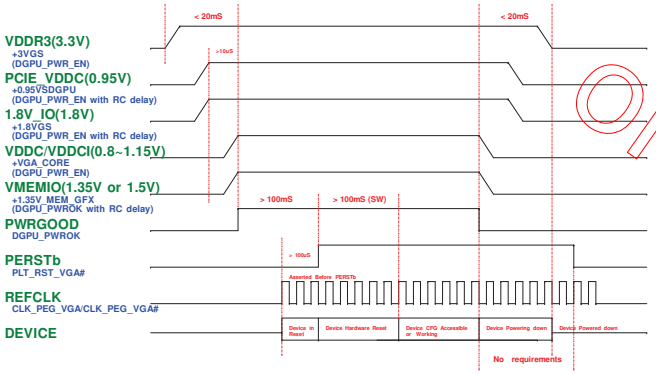
Title: **MESO GDDR5 A1**

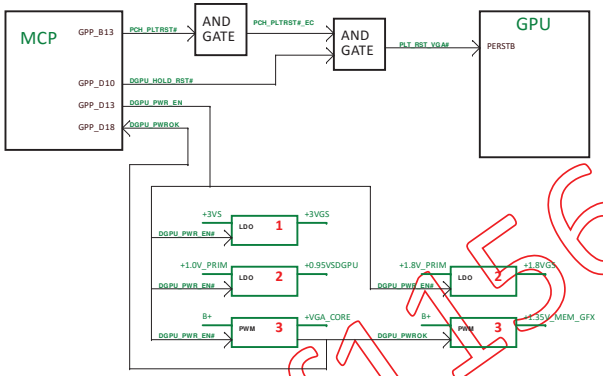
Size	Document Number	Rev
	LA-F115P	0.1

Date: Friday, March 02, 2018 Sheet 50 of 85

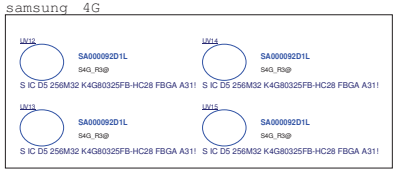
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µ s).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.

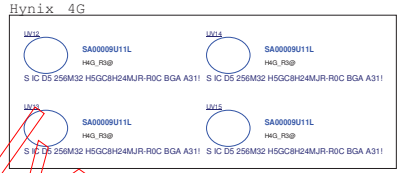




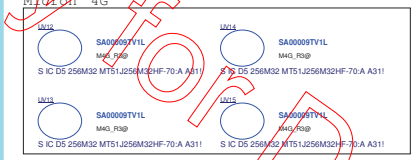
samsung 4G



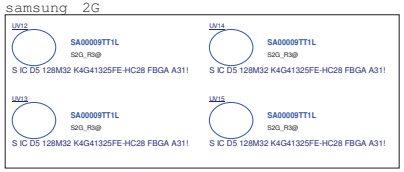
Hynix 4G



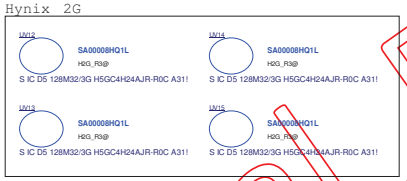
Micron 4G



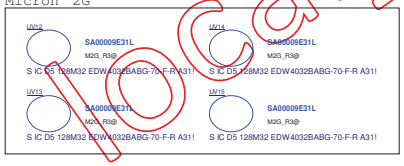
samsung 2G



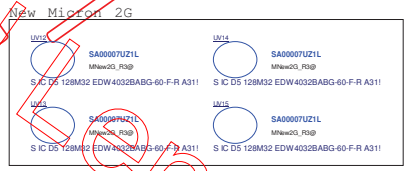
Hynix 2G



Micron 2G

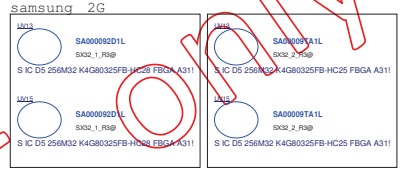


New Micron 2G

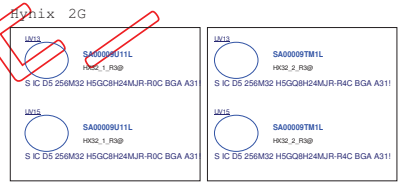


LAF115 VRAM x16*4pcs

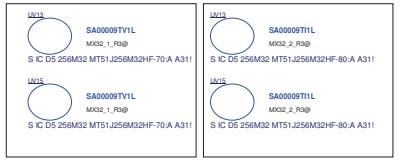
samsung 2G



Hynix 2G



Micron 2G



LAF116 VRAM x32*2pcs

Table 3–21 Resistor Divider Lookup T

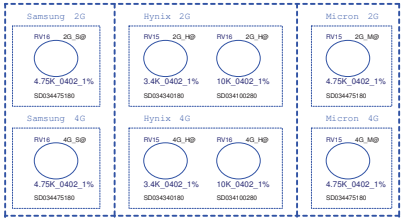
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R17M-M2-50 VRAM Only

Memory ID	4Gb R3 P/N	Vendor	Configuratio	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BABG-70-F-R A31!	2GB

Memory ID	8Gb R3 P/N	Vendor	Configuratio	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70:A A31!	4GB



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01
Title	MESO_Note		
Size	Document Number		Rev 0.1
	LA-F115P		
Date:	Friday, March 02, 2018	Sheet	51 of 65

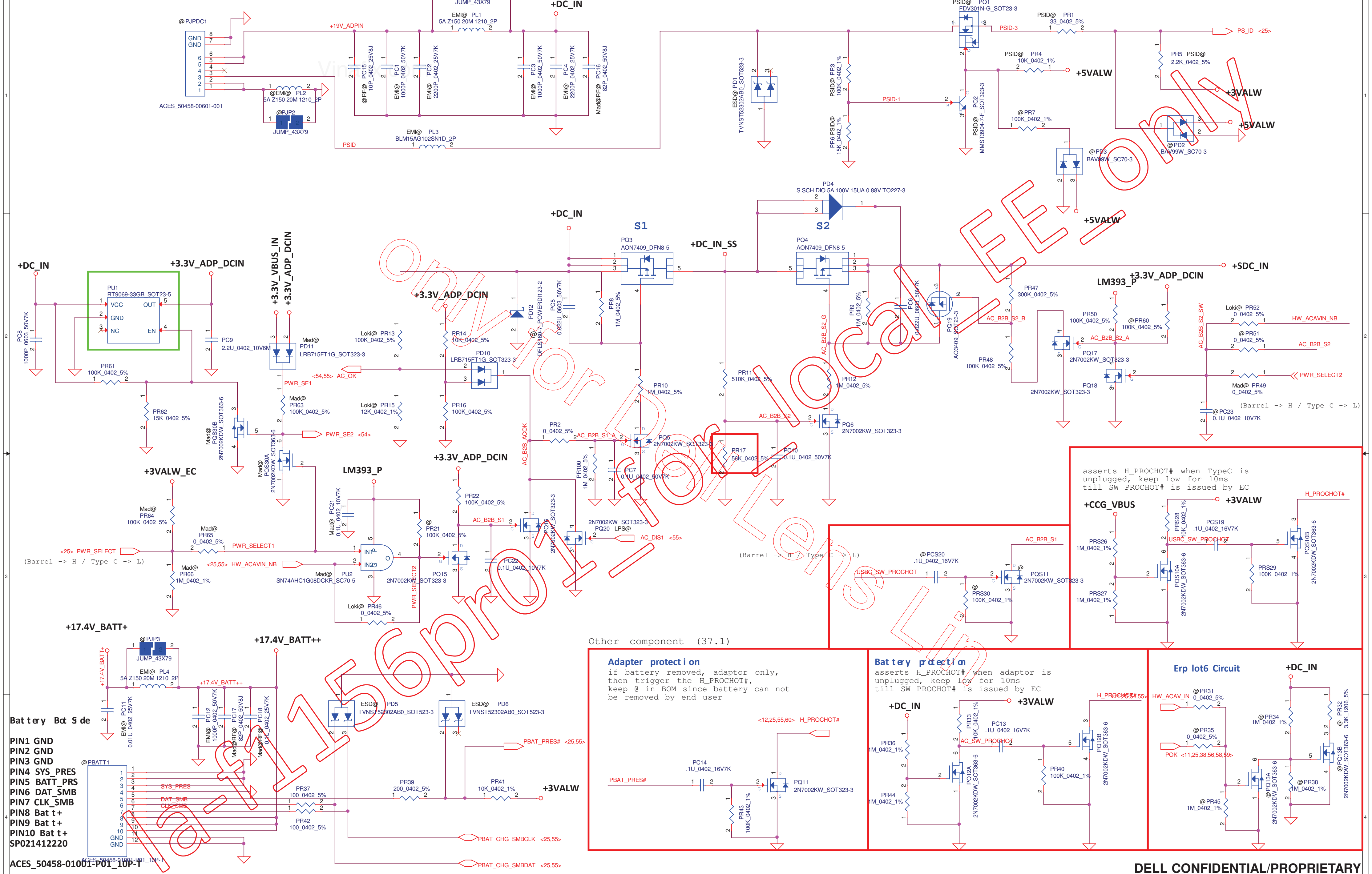
Version Change List (P. I. R. List)

Page	Part reference	Change description	Reason
32	RW15	add RW15	[BITS325553] Some units auto power on when plug AC
29	RC224	add RC224	[BITS325233] LED light twice when plug AC on SUT
27	R72	add R72 for FPR_SCAN# Pull +3VALW	[BITS327066] Can't turn off when press power button once on BIOS/BootMenu/ePSA(KBL-R)
26	EU2601	"DU1" change location to "EU2601"	Compal naming rule.
29	SW2	add SW2	debug, for NPI debug purpose.
25	DT1	DT1.1 from "+3.3V_VDD_PIC" change to "+3VALW"	Fixed can't charge in S3, AC IN after battery plug.
38	DT1	DT1.2 from "+3valw" change to +3.3V_ADP_DCIN	Fixed can't charge in S3, AC IN after battery plug.
38	QT4	SWAP QT4 S&D	Fixed Loki can't power on with TypeC adapter.
39	RT117,RT116	add RT117,RT116	Loki-L, Fixed TypeC DP no display issue.
9	UC1	add RC213 for 3.3V_TS_EN PD	Loki-L, for MS touch disable for PCH reset.
25	UE1	EC pin94 change net name to H_PECI	GPIO table update.
9	UC1	net name from "BT_RADIO_DIS#" change to "BLUETOOTH_EN"	GPIO table update.
11,22,25	UE1	"RTC_ENABLE" rename to "RTCRST_ON"	GPIO table update.
8,25	UE1	netname from "ESPI_IO0_EC" change to "ESPI_IO0"	GPIO table update.
8,25	UE1	netname from "ESPI_IO1_EC" change to "ESPI_IO1"	GPIO table update.
8,25	UE1	netname from "ESPI_IO2_EC" change to "ESPI_IO2"	GPIO table update.
8,25	UE1	netname from "ESPI_IO3_EC" change to "ESPI_IO3"	GPIO table update.
8,25	UE1	netname from "ESPI_CLK_EC" change to "ESPI_CLK"	GPIO table update.
25	UE1	UE1.68 & UE1.88 change net	GPIO table update.
25	UE1	netname from "VCCDSW_EN" change to "VCCDSW_OFF#"	GPIO table update.
22	R59,R60,R61,R62,R63,R64,Q2,Q3,Q5	remove R59,R60,R61,R62,R63,R64,Q2,Q3,Q5	Loki-L, GEN9
22	R73,R78,R79,C59,C60,C61,D7,Q23,Q24	add R73,R78,R79,C59,C60,C61,D7,Q23,Q24	Loki-L, GEN9
34	JWWAN	change JWWAN pin define	Loki-L Move IO extend to WWAN/B
25	UE3,CE40,CE41,RE83,RE77,RE76,RE75,RE78,RE79,RE80,CE42,CE41,CE40,RE13,RE14,RE15,UZ6,RZ18,RZ17,CZ41	del UE3,CE40,CE41,RE83,RE77,RE76,RE75,RE78,RE79,RE80,CE42,CE41,CE40,RE13,RE14,RE15,UZ6,RZ18,RZ17,CZ41	Loki-L Move IO extendor to WWAN/B
25	RE12	RE12.2 from "+3valw" change to "+3.3V_ALW_DSW"	Loki-L, Deep SX follow PDG.
39	UT5	del UT5.18 connect to UT5.38	Loki-L, Fixed DP mux HPD switch issue.
39	RT115	add RT115	Loki-L, Fixed DP mux HPD switch issue.
25	UE7,CE505,CE504,RE34,RE536,RE537,QE13,CE503,RE530	add UE7,CE505,CE504,RE34,RE536,RE537,QE13,CE503,RE530	Loki-L, For WDT issue, Deep SX support.
37	CS28,CS33,CS34,CS35,CS36	del CS28,add CS33,CS34,CS35,CS36	Power Change CAP value
39	RT97	RT97.2 form "TYPEC_DP_AUXN" change to "TYPEC_DP_AUXN_C"	Spec, Change to meet TI TUSB546 spec
39	RT94	RT94.2 form "TYPEC_DP_AUXP" change to "TYPEC_DP_AUXP_C"	Spec, Change to meet TI TUSB546 spec
39	UT2	netname from "VGA_DP_AUXN_C" change to "VGA_DP_AUXN"	Spec, Change to meet TI TUSB546 spec
39	UT2	netname from "VGA_DP_AUXP_C" change to "VGA_DP_AUXP"	Spec, Change to meet TI TUSB546 spec
39	CT69,CT70	del CT69,CT70	Vender recommand, VGA/B already have CAP
38	RT60,RT61	del RT60,RT61	Vender recommand.
22	RX9	reserve RX9	Vender recommand.
23	RA8	from 100K change to 10K	Vender recommand.
40	RT37,RT38	remove RT37,RT38	EC request
12	SW3,RC223	add SW3,RC223	for LOKIL NPI BIOS request
37,29	R81,R77	add R81,R77,R82,R83,Q25	for LED issue
	RA1,RA22	Change Footprint from "R_0805" to "R0805_0ohm"	Change to Short PAD
	RA4,RA39,RL5,RC17,RC169,RC170,RC171,RC173,RC174,RE7,RE50,RE66	Change Footprint from "R_0603" to "R0603_0ohm"	
	RA2,RA5,RA17,RA18,RA6,RA36,RA37,RA40,RL13,RW9,RW10,RC99,RC106,RC107,RC97,R8,RL13	Change Footprint from "R_0402" to "R0402_0ohm"	
	RD4,RD5,RD6,RD8,RD14,RD16,RD18,RE28,RE37,RE42,RE60,RE61,RE63	Change Footprint from "R_0402" to "R0402_0ohm"	
	L4	Change Footprint from "INPAQ_MCM1012B900F06BP_4P" to "INPAQ_MCM1012B900F06BP_4P-NPM"	Close solder mask
	LU2,LU3,LU5,LU6	Change Footprint from "INPAQ_HCM1012GH900BP_4P" to "INPAQ_HCM1012GH900BP_4P-NPM"	Close solder mask
	RU1,RU2,RU7,RU9,RU13,RU14,RU15,RU16,RU17,R18	Change Footprint from "R_0402" to "R0402-NPM"	Close solder mask
	LI1,LI2,LI3,LI4	Change Footprint from "INPAQ_HCM1012GH900BP_4P" to "INPAQ_HCM1012GH900BP_4P-NPM"	Close solder mask
	RT41,RT42	Change Footprint from "R_0402" to "R0402-NPM"	Close solder mask
	LT3,LT4	Change Footprint from "INPAQ_HCM1012GH900BP_4P" to "INPAQ_HCM1012GH900BP_4P-NPM"	Close solder mask
34	JVGA	change JVGA pin define	
28	R85	add R85,IR_GND/GND	for LOKIL RF request
38	UT4	UT4.pin3&pin4 short	main&2nd have different pin define
38	RT121	CT18 change to RT121	for UT4 discharge

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: EE Change list			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, March 02, 2018		Sheet 52 of 65	

Main Func = DCIN/BATT CONN


+DC_IN
+5VALW
+3VALW
+SDC_IN
+DC_IN_SS
S1
S2
+3.3V_ADP_DCIN
+3.3V_VBUS_IN
+3VALW_EC
LM393_P
+17.4V_BATT+
+17.4V_BATT++
+CCG_VBUS
PS_ID <25>
HW_ACAVIN_NB
AC_B2B_S2
PWR_SELECT2
PWR_SE1
PWR_SE2 <54>
<54,55> AC_OK
<25> PWR_SELECT
<25,55> HW_ACAVIN_NB
AC_DIS1 <55>
(Barrel -> H / Type C -> L)
asserts H_PROCHOT# when TypeC is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC
H_PROCHOT#
USBC_SW_PROCHOT
Other component (37.1)
Adapter protection
if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user
Battery protection
asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC
Erp lot6 Circuit
PBAT_PRES# <25,55>
PBAT_CHG_SMBCLK <25,55>
PBAT_CHG_SMBDAT <25,55>
Battery Bot Side
PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220
ACES_50458-01001-P01_10P-T
ACES_50458-00601-001
RT9069-33GB_SOT23-5
AON7409_DFN8-5
SN74AHC1G08DCKR_SC70-5
S SCH DIO 5A 100V 15UA 0.88V TO227-3

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Issued Date	2016/12/01	Deciphered Date	2017/12/01

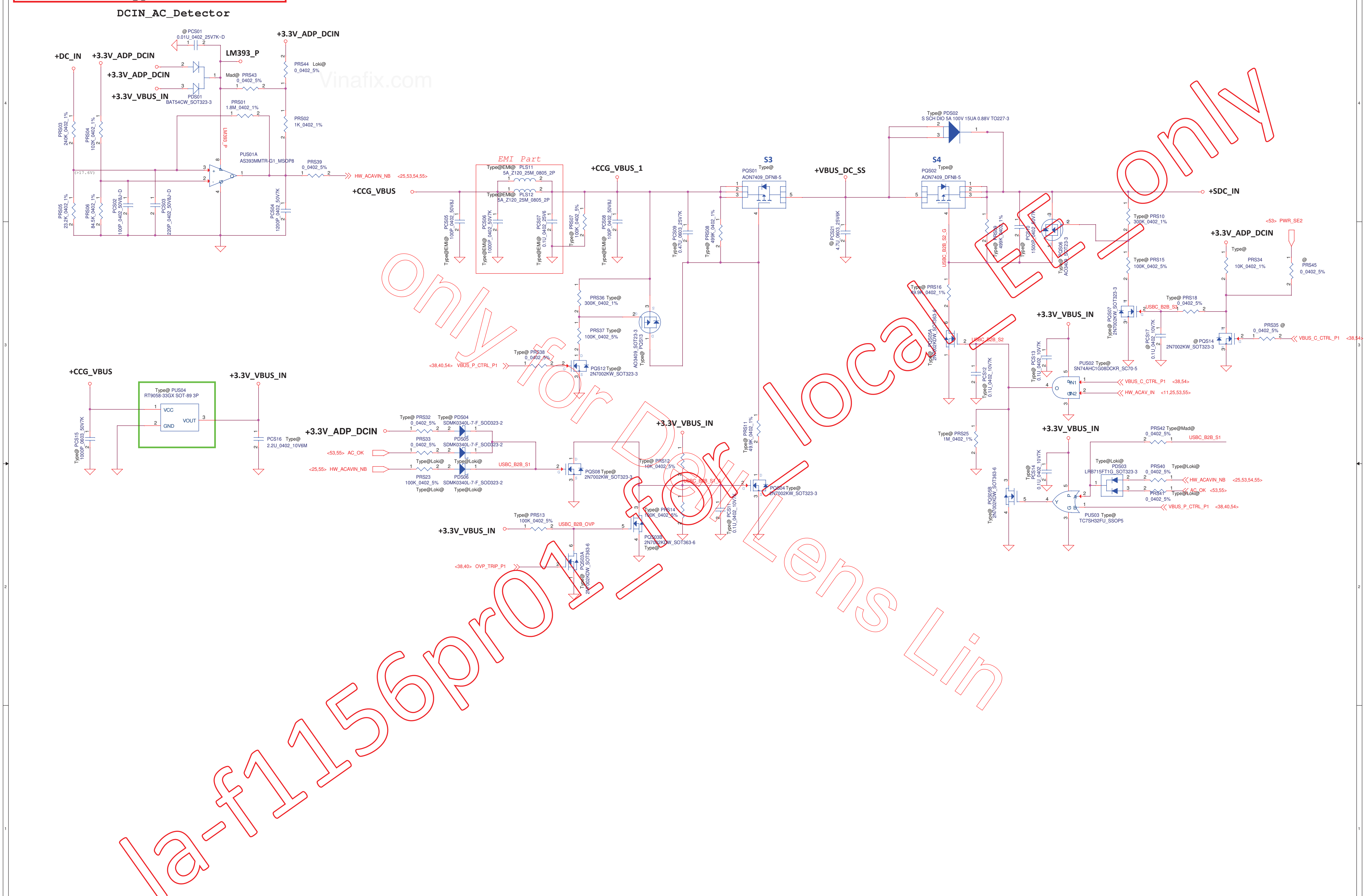
Compal Electronics, Inc.

Title: *PWR_DCIN/BATT CONN*

Size | Document Number | Rev X00

Date: Friday, March 02, 2018 | Sheet 53 of 65

Main Func = Type-C PD Selector



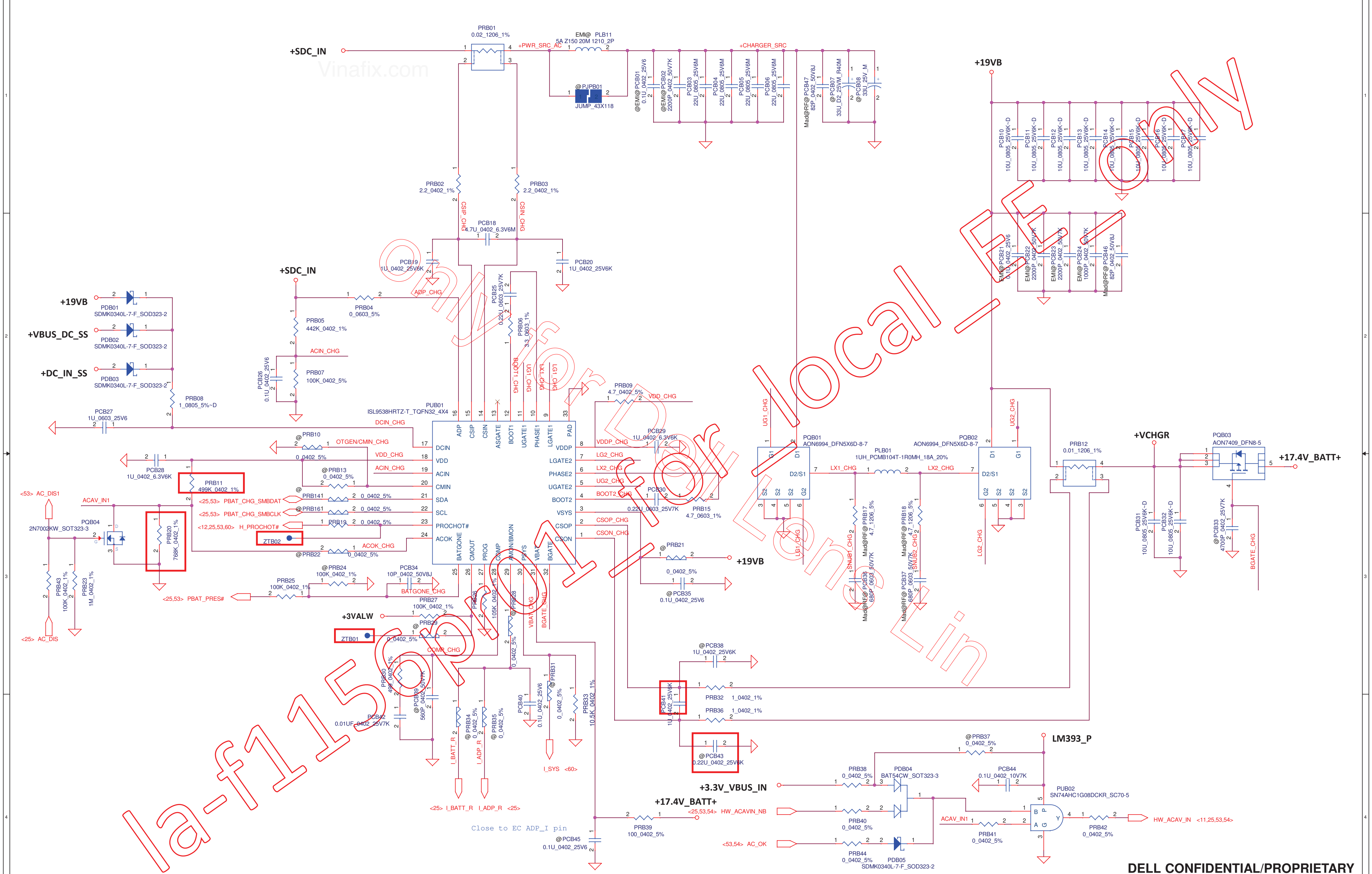
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: *PWR_Type-C PD Selector*

Size | Document Number | Rev X00

Main Func = CHARGER



+SDC_IN
PRB01
0.02_1206_1%
+PWR_SRC_AC
EMI@ PLB11
5A Z150 20M 1210_2P
+CHARGER_SRC
@PJPB01
JUMP_43X118
+19VB
+VBUS_DC_SS
+DC_IN_SS
PDB01
SDMK0340L-7-F_SOD323-2
PDB02
SDMK0340L-7-F_SOD323-2
PDB03
SDMK0340L-7-F_SOD323-2
PRB02
2.2_0402_1%
PRB03
2.2_0402_1%
PCB18
4.7U_0402_6.3V6M
PCB19
1U_0402_25V6K
PCB20
1U_0402_25V6K
PRB04
0_0603_5%
PRB05
442K_0402_1%
PRB07
100K_0402_5%
PRB08
1_0805_5%~D
PCB27
1U_0603_25V6
PUB01
ISL9538HRTZ-T_TQFN32_4X4
DCIN
VDD
ACIN
CMIN
SDA
SCL
PROCHOT#
ACOK
VDDP
LGATE2
PHASE2
UGATE2
BOOT2
VSYS
CSOP
CSON
ADP_CHG
ACIN_CHG
DCIN_CHG
OTGEN/CMIN_CHG
VDD_CHG
PBAT_CHG_SMBDAT
PBAT_CHG_SMBCLK
H_PROCHOT#
ACOK_CHG
PRB11
499K_0402_1%
PRB20
768K_0402_1%
PQB04
2N7002KW_SOT323-3
ACAV_IN1
AC_DIS1
AC_DIS
PBAT_PRES#
ZTB02
ZTB01
+3VALW
PQB01
AON6994_DFN5X6D-8-7
PQB02
AON6994_DFN5X6D-8-7
PLB01
1UH_PCMB104T-1R0MH_18A_20%
LX1_CHG
LX2_CHG
PRB12
0.01_1206_1%
+VCHGR
PQB03
AON7409_DFN8-5
+17.4V_BATT+
BGATE_CHG
PRB32
1_0402_1%
PRB36
1_0402_1%
I_BATT_R
I_ADP_R
I_SYS
Close to EC ADP_I pin
LM393_P
+3.3V_VBUS_IN
PDB04
BAT54CW_SOT323-3
PUB02
SN74AHC1G08DCKR_SC70-5
HW_ACAVIN_NB
AC_OK
HW_ACAV_IN
PDB05
SDMK0340L-7-F_SOD323-2
PRB39
100_0402_5%

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Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

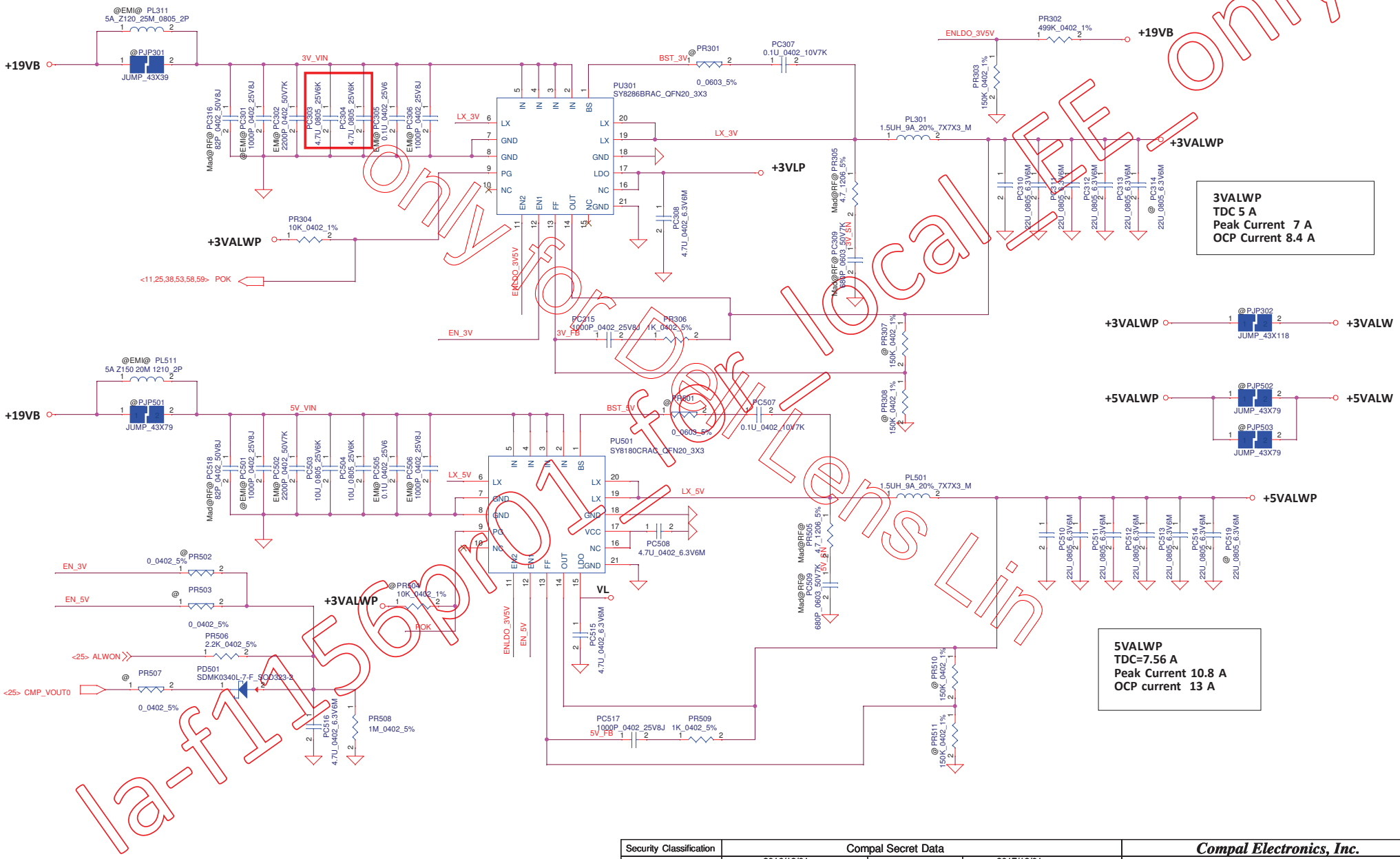
Compal Electronics, Inc.

Title: *PWR_CHARGER*

Size | Document Number | Rev X00

Date: Friday, March 02, 2018 | Sheet 55 of 65

Main Func = 3.3VALWP/5VALWP



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

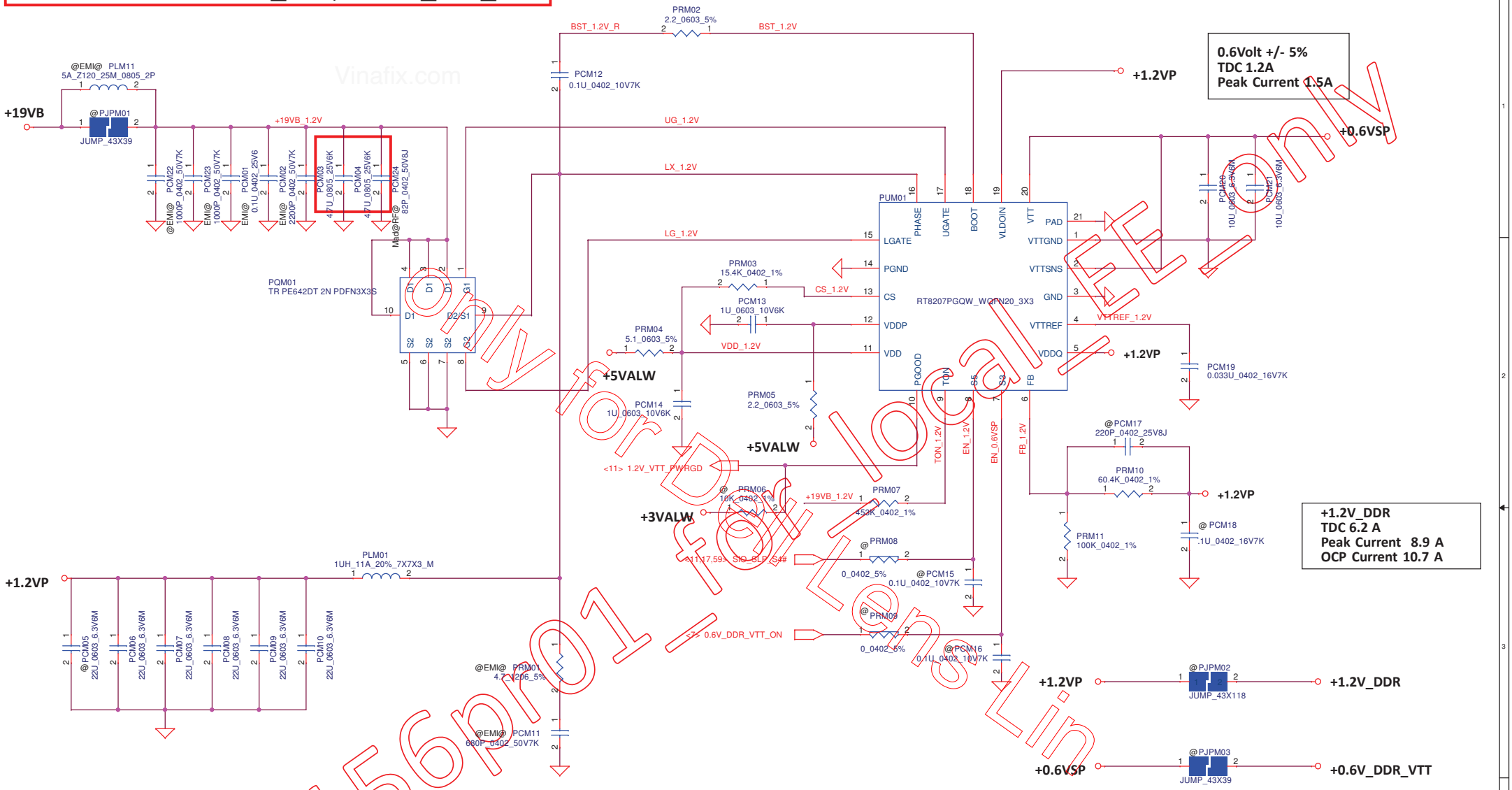
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size	Document Number	Rev
		0.1 (X00)

Date: Friday, March 02, 2018 Sheet 56 of 65

Main Func = +1.2V_DDR/+0.6V_DDR_VTT



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

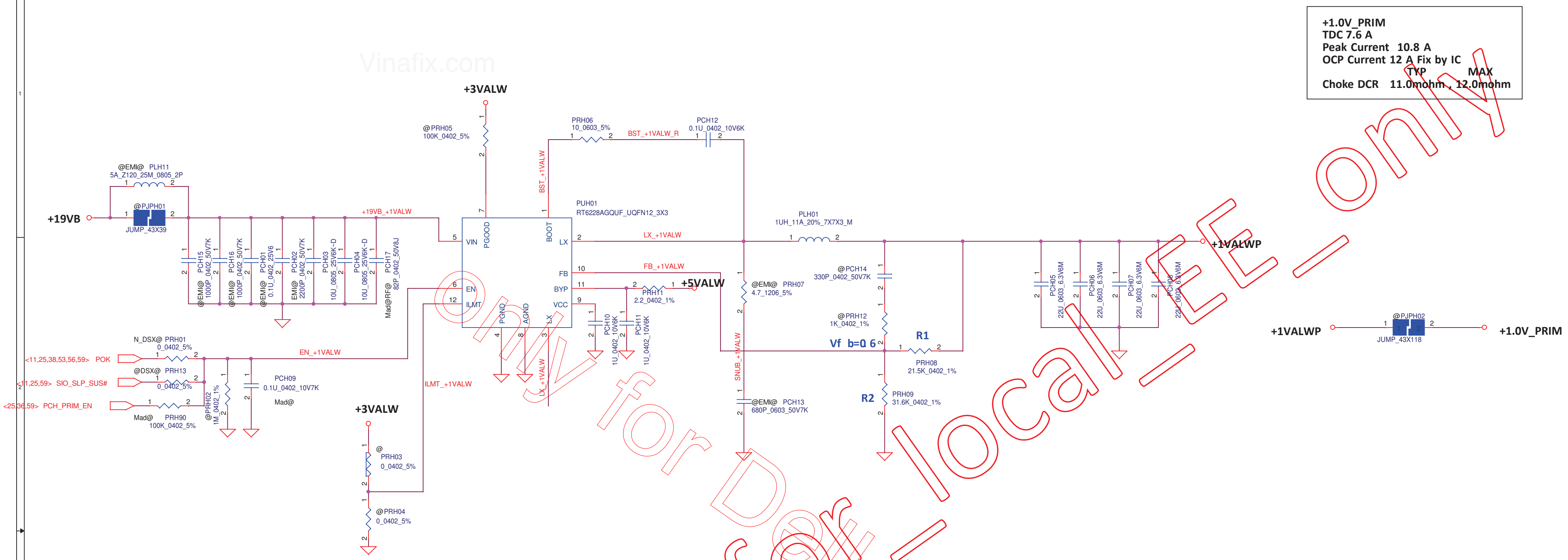
Compal Electronics, Inc.

Title: PWR_+1.2V_MEN/+0.6V_DDR_VTT

Size	Document Number	Rev
Custom		X00

Date: Friday, March 02, 2018 | Sheet 57 of 65

Main Func = +1VALWP


+1.0V_PRIM
TDC 7.6 A
Peak Current 10.8 A
OCP Current 12 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm
+3VALW
@PRH05 100K_0402_5%
PRH06 10_0603_5%
BST_+1VALW_R
PCH12 0.1U_0402_10V6K
BST_+1VALW
@EMI@ PLH11 5A_Z120_25M_0805_2P
@PJPH01 JUMP_43X39
+19VB
+19VB_+1VALW
PUH01 RT6228AGQUF_UQFN12_3X3
VIN PGOOD BOOT LX FB BYP VCC EN ILMT PGND AGND LX
LX_+1VALW
PLH01 1UH_11A_20%_7X7X3_M
+1VALWP
FB_+1VALW
PRH11 2.2_0402_1%
+5VALW
@EMI@ PRH07 4.7_1206_5%
@PCH14 330P_0402_50V7K
@PRH12 1K_0402_1%
Vf b=0 6
R1
PRH08 21.5K_0402_1%
R2
PRH09 31.6K_0402_1%
@EMI@ PCH13 680P_0603_50V7K
SNUB_+1VALW
PCH05 22U_0603_6.3V6M
PCH06 22U_0603_6.3V6M
PCH07 22U_0603_6.3V6M
PCH08 22U_0603_6.3V6M
@PJPH02 JUMP_43X118
+1VALWP
+1.0V_PRIM
@EMI@ PCH15 1000P_0402_50V7K
@EMI@ PCH16 1000P_0402_50V7K
@EMI@ PCH01 0.1U_0402_25V6
EMI@ PCH02 2200P_0402_50V7K
PCH03 10U_0805_25V6K-D
PCH04 10U_0805_25V6K-D
Mad@RF@ PCH17 82P_0402_50V8J
PCH10 1U_0402_10V6K
PCH11 1U_0402_10V6K
N_DSX@ PRH01 0_0402_5%
<11,25,38,53,56,59> POK
EN_+1VALW
@DSX@ PRH13 0_0402_5%
<11,25,59> SIO_SLP_SUS#
<25,36,59> PCH_PRIM_EN
Mad@ PRH90 100K_0402_5%
@PRH02 1M_0402_1%
PCH09 0.1U_0402_10V7K
Mad@
ILMT_+1VALW
+3VALW
@ PRH03 0_0402_5%
@PRH04 0_0402_5%
LX_+1VALW

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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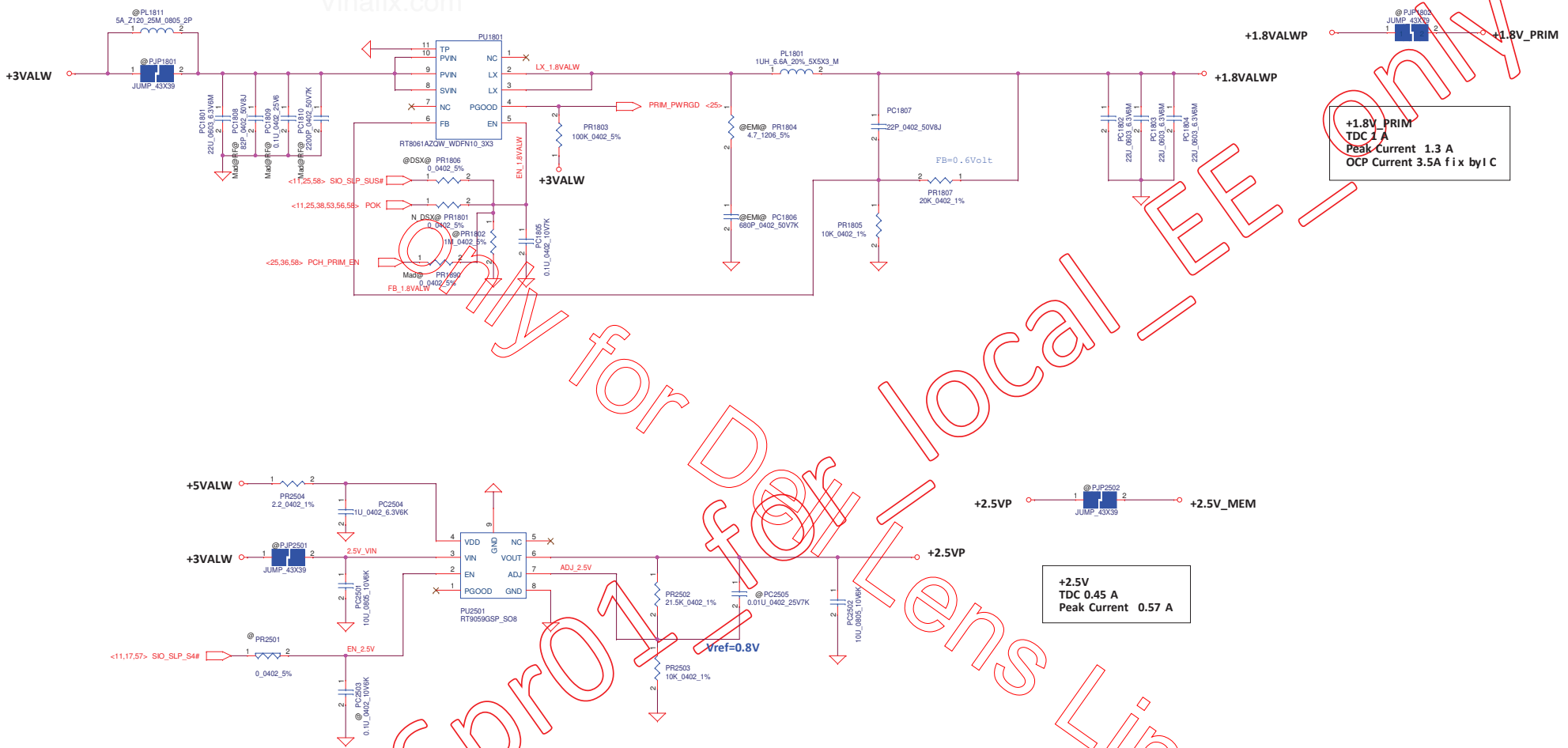
Compal Electronics, Inc.

Title: ***PWR_+1VALWP***

Size: C | Document Number | Rev: X00

Date: Friday, March 02, 2018 | Sheet 58 of 65

Main Func = +1.8VALWP / +2.5VP



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

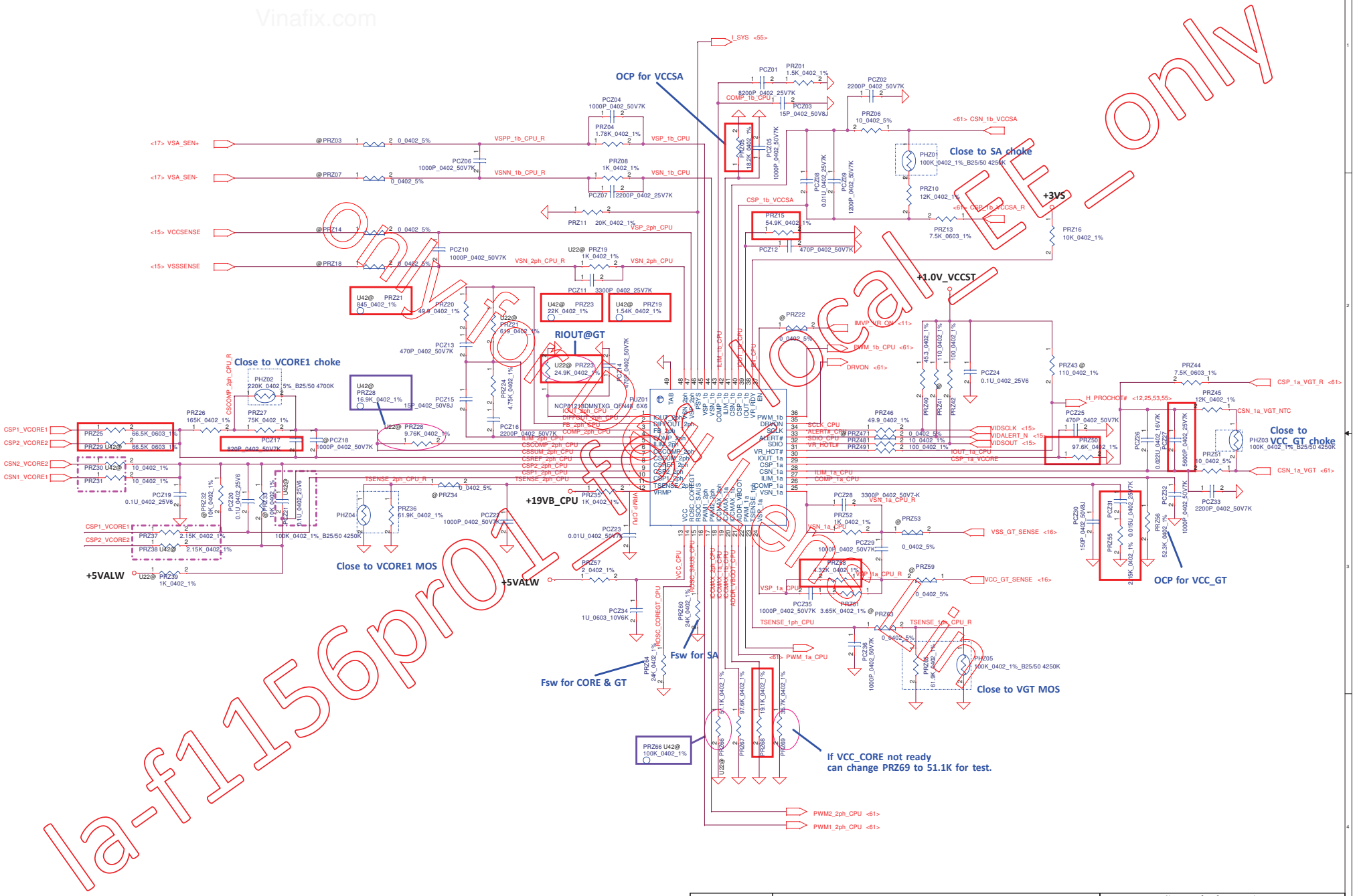
Compal Electronics, Inc.

Title: PWR_+1.8VALWP / +2.5VP

Size	Document Number	Rev
C		X00

Date: Friday, March 02, 2018 | Sheet 59 of 65

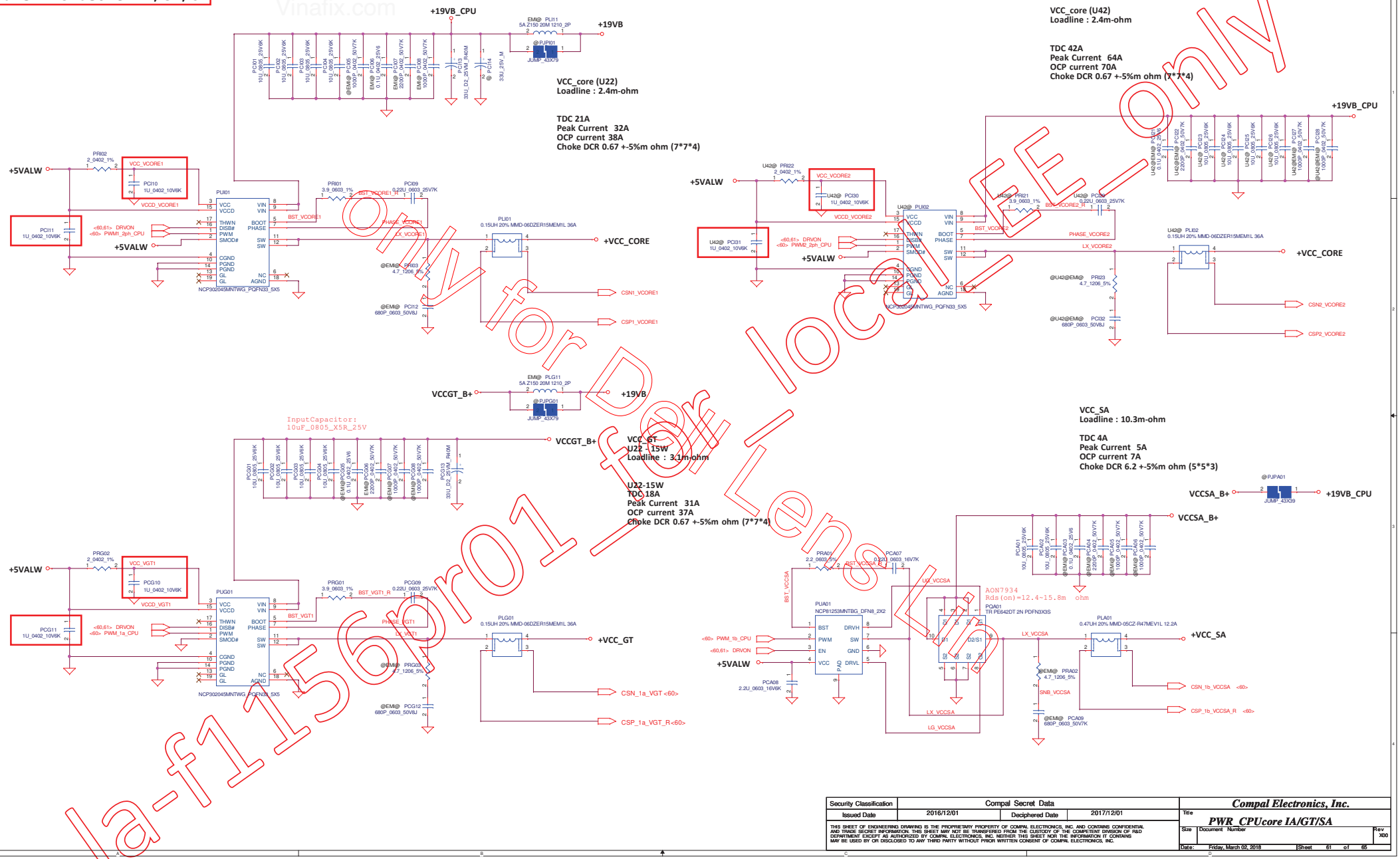
Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.	
Title	PWR_CPU
Size	Document Number / Rev X00
Date: Friday, March 02, 2018	Sheet 60 of 65

Main Func = CPUcore IA/GT/SA



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date 2017/12/01	Title: PWR_CPUcore IA/GT/SA
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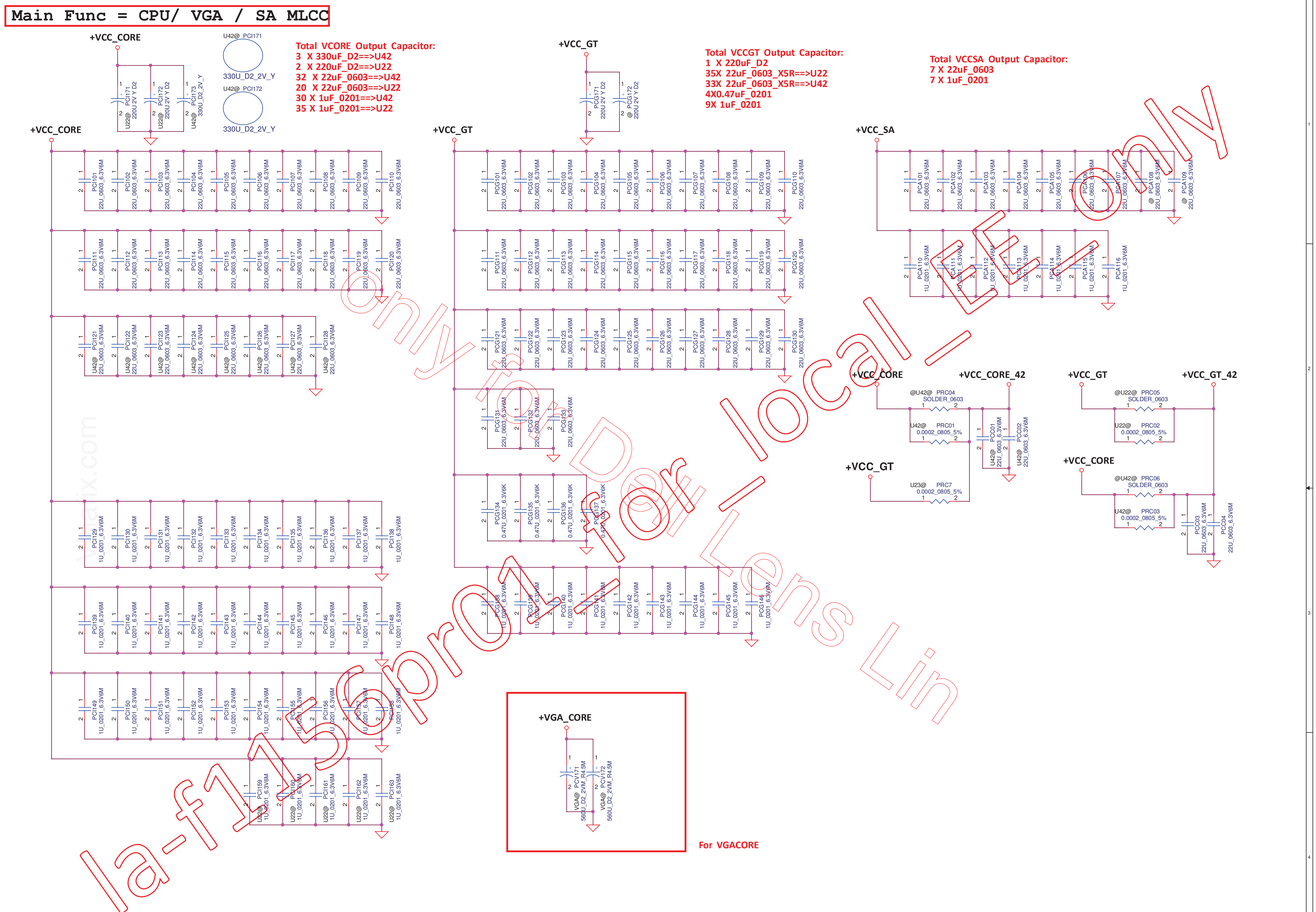
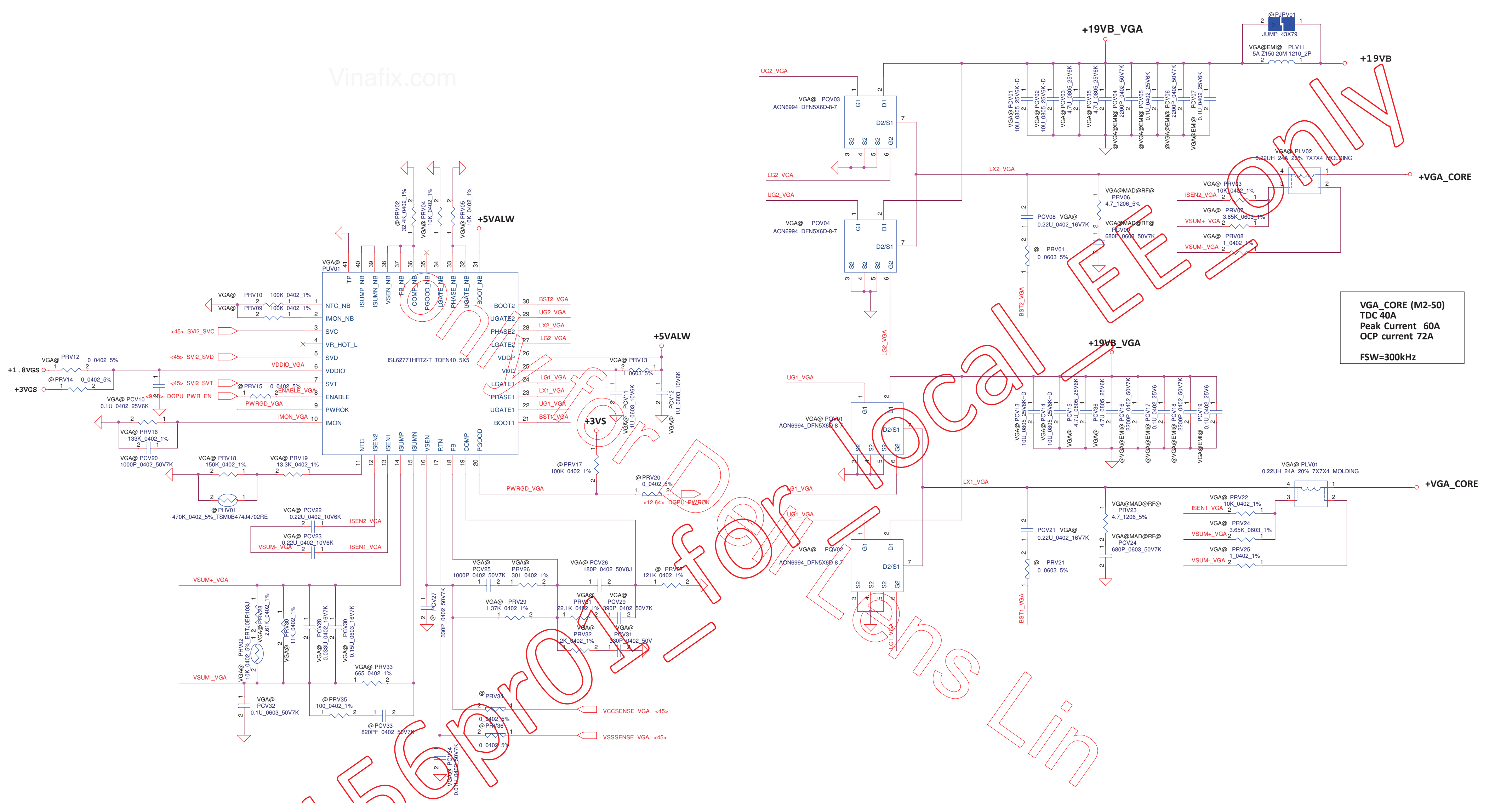
			Date: Friday, March 02, 2018 Sheet 61 of 65



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title: PWR_CPU / VGA / SA MLCC
				Size / Document Number / Rev: X00
				Date: Friday, March 02, 2018 / Sheet 62 of 65

Main Func = VGA CORE

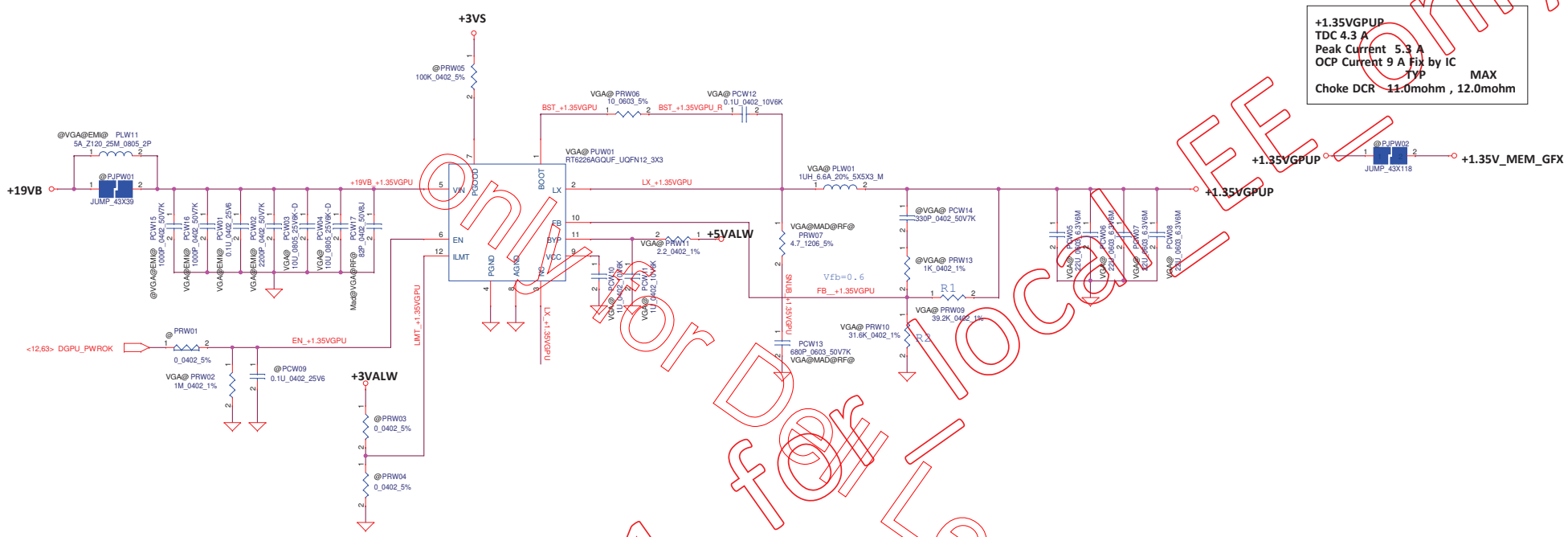


Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title	PWR_VGA_CORE	
Size	Document Number	Rev X00
Date: Friday, March 02, 2018	Sheet 63 of 65	

Main Func = +1.35VGPUP



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: PWR_+1.35VGPUP

Size	Document Number	Rev
		X00

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL			0.1(X00)
2	P56	PWR	20160321	COMPAL			0.1(X00)
3							
4							
5							
6							
7							
8							

Security Classification	Compal Secret Data		
Issued Date	2015/12/22	Deciphered Date	2017/01/31

Compal Electronics, Inc.

Title: Changed-List PWR History

Size | Document Number | Rev X00

Date: Friday, March 02, 2018 | Sheet 65 of 65