LCFC Confidential

SKYWALKER NM-A831 Rev2.0 Schematic

Intel KabyLake Processor with DDR4 + PCH-LP

NVIDIA N16S-GTR GDDR5 2GB
NVIDIA N16P-GT GDDR5 2GB

2016-08-24 Rev2.0

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Title: COVER PAGE			
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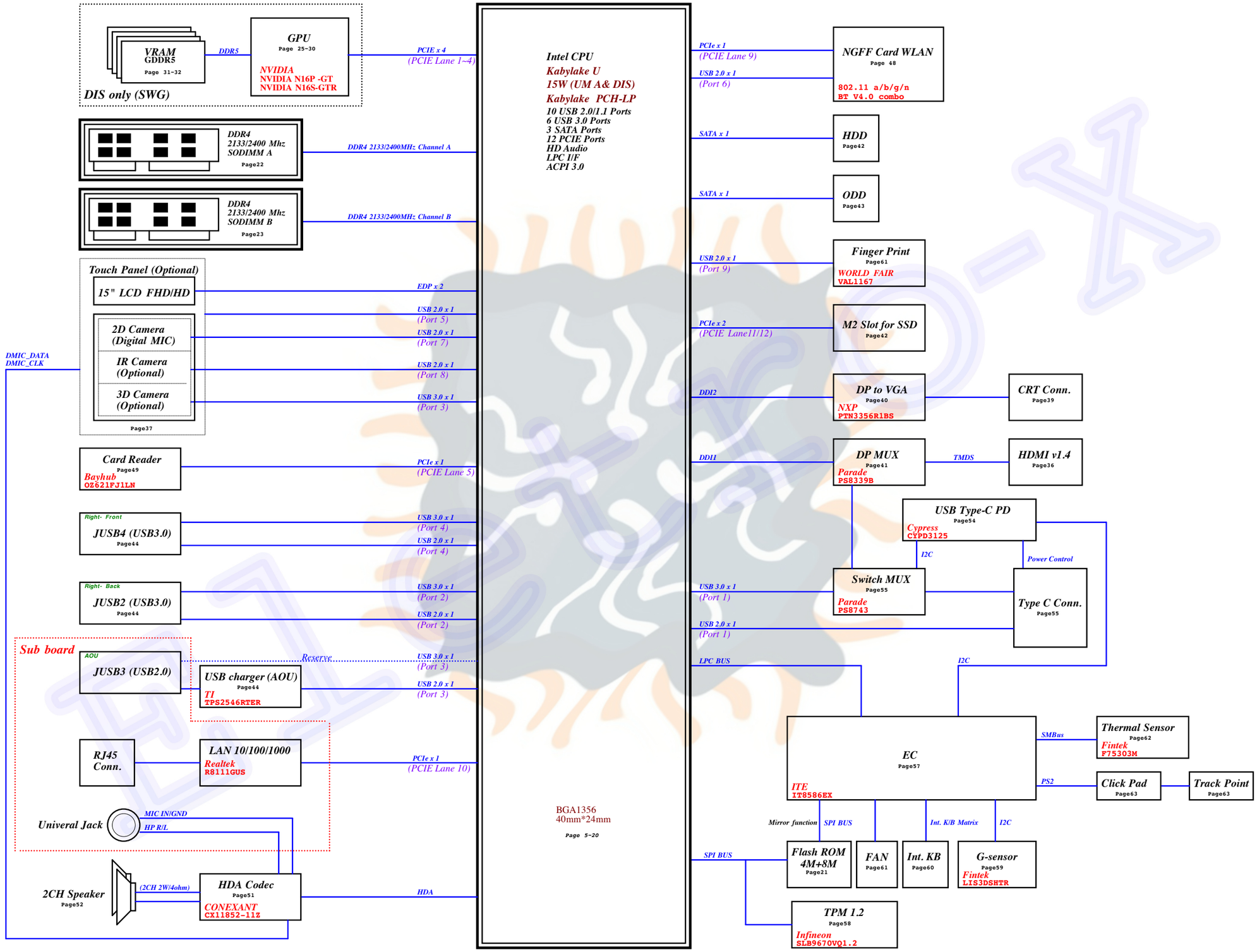
Skywalker KBL U Block Diagram



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Title: BLOCK DIAGRAM

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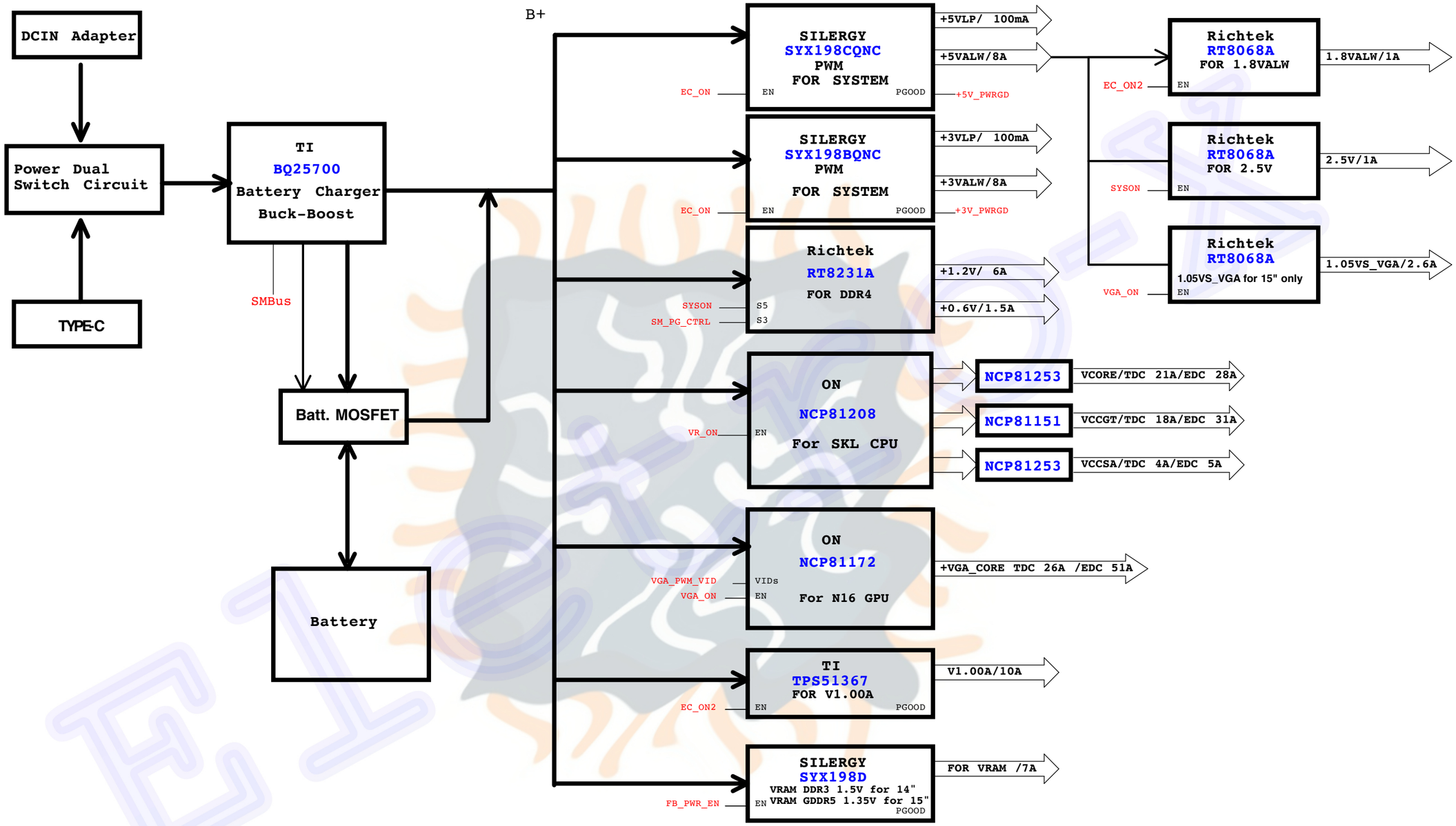

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Title	*Power Block Diagram*	
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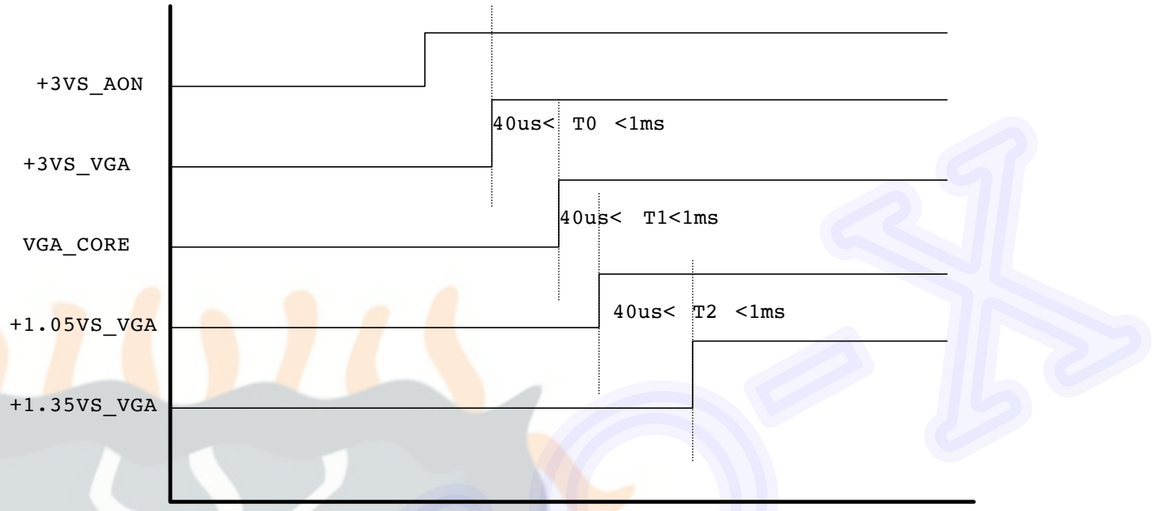
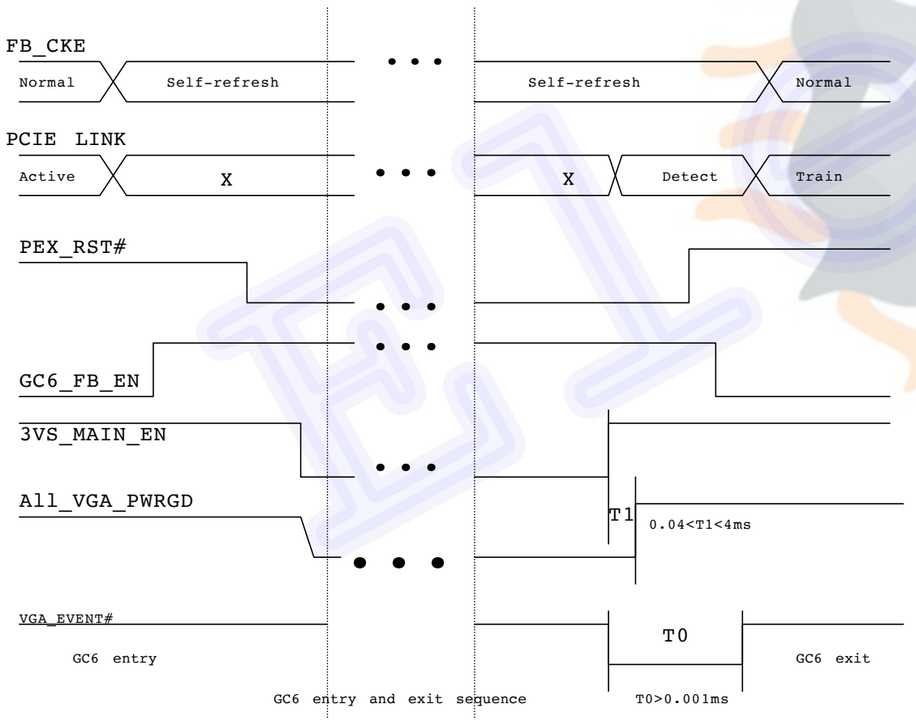
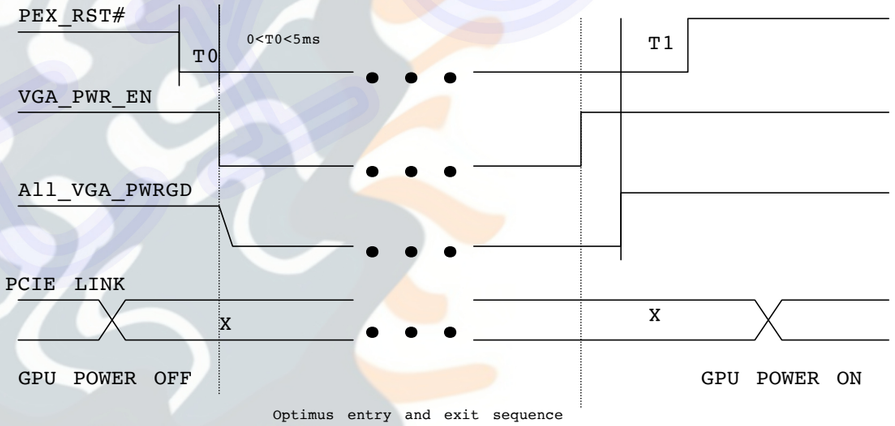
GPIO	I/O	Functional Description	I/O Termination
GPIO0	O	FB Enable for GC6 2.0, Open source	10K pull-down
GPIO1	O	Memory voltage control	Pull-up/pull down to set the FBVDD/Q boot voltage
GPIO2	O	Panel Backlight PWM Brightness Control	100K pull down
GPIO3	O	Panel Power Enable	100K pull down
GPIO4	O	Panel Backlight Enable	100K pull down
GPIO5	O	GPU Power Sequence for GC6 2.0, Open Drain	10k pull-up to 3V3_AON
GPIO6	I	GPU wake signal for GC6 2.0	10k pull-up to 3V3_AON
GPIO7	O	3D Vision L/R signal	100K pull down
GPIO8	O	System side PCIe rest monitor	10k pull-up to 3V3_AON
GPIO9	I/O	Active low thermal alert, open drain	10k pull-up to 3V3_AON
GPIO10	O	Memory VREF Control	100K pull down
GPIO11	O	GPU Core VDD PWM control signal	
GPIO12	I	AC power detect or power supply overdraw input	100k pull-up to 3V3_AON
GPIO13	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase
GPIO14	I	Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI	
GPIO15	I	Hot Plug Detect for IFPC	
GPIO16	I	Active Low Frame Lock, Open Drain	10k pull-up to 3V3_AON
GPIO17	I	Hot Plug Detect for IFPD	
GPIO18	I	Hot Plug Detect for IFPE	
GPIO19	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	
GPIO20	O	Reserved	
GPIO21	O	GPU PCIe self-reset control, Open Drain	10k pull-up to 3V3_AON
OVERT	I/O	Catastrophic Over Temperature	100k pull-up to 3V3_AON







Title: **P35-GPU GPIO table & sequence**

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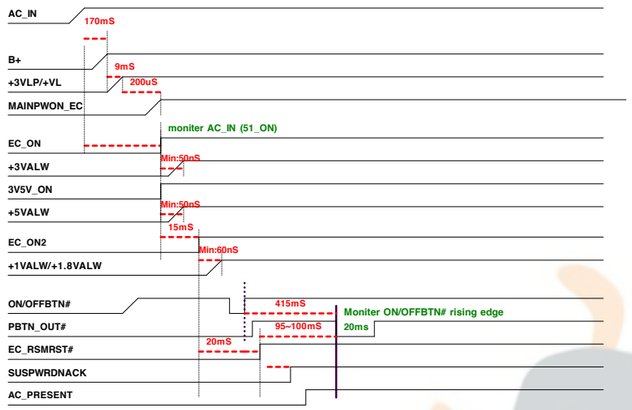
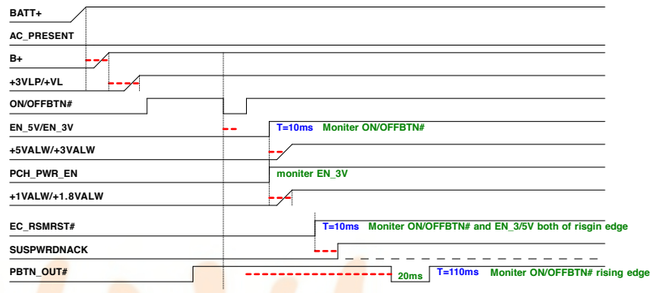
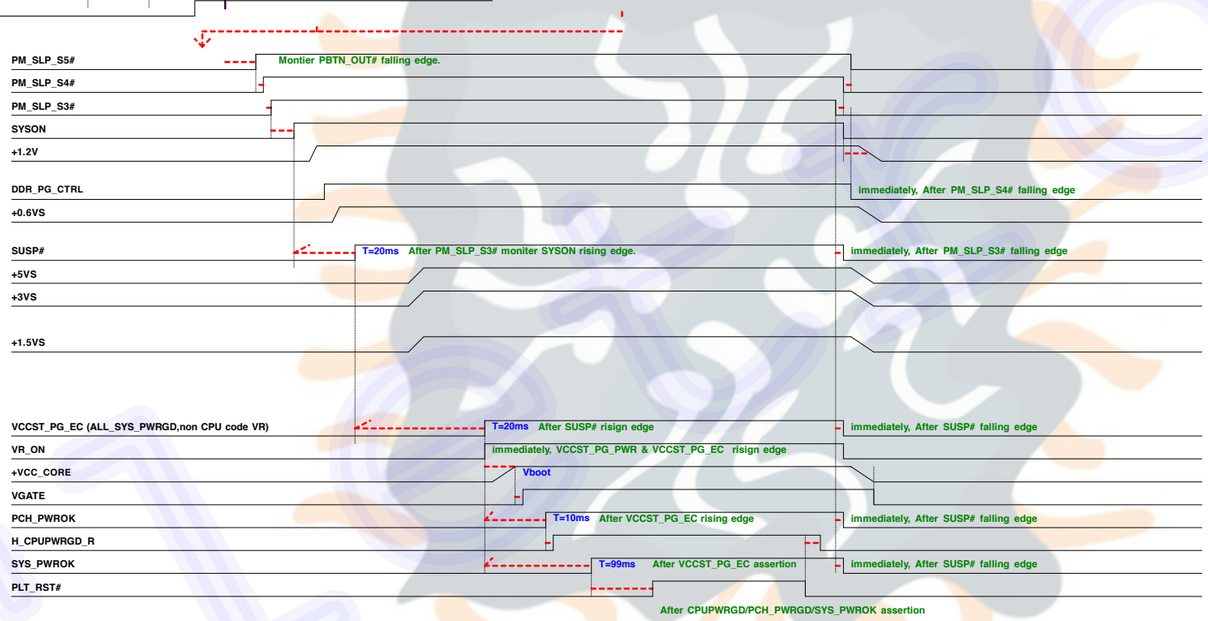
Skywalker PWR Sequence_SKL-U_DDR4_Non-Deep Sx]

[AC Mode]



[DC Mode]





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Title: Power Sequence

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+ +3VL	+3VALW +5VALW +1VALW +1.8VALW	+2.5V +1.2V +VCC_STG	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VGA_CORE +3VS_VGA +1.35VS_VGA +3VS_AON +1VS_VGA +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	Main VGA	BATT (Charger)	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	LAN PHY	G sensor	USB Type-C
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580F +3VL	X	X	X	X	X	X	X	X	X	V +3VPD_VDD
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	V +3VS_GS	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	X	X	X	X	V +5VS	X	X	X
PCH_SML1CLK PCH_SML1DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	X	X

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
DIMM2@	For DIMM2 function
DIMM1@	For DIMM1 function
TYPEC@	For USB Type-C function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
MIRROR@	For mirror function
NGC6@	For VGA Non GC6 function
GC6@	For VGA GC6 function

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#	SYSON
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	HIGH
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF	LOW
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF	LOW

USB2 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3 Sub board
4	JUSB4
5	Touch Panel
6	BT
7	CMOS
8	IR CAMERA
9	FP/Smart

USB3 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	3D CCD
4	JUSB4

PCIE Port

Port	Device
1	GPU
2	GPU
3	GPU
4	GPU
5	CardReader
6	X
7	X
8	X
9	WLAN
10	LAN
11	M.2 SSD
12	M.2 SSD

SATA Port

Port	Device
1	HDD
2	ODD
3	X
4	X

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Title: NOTE LIST

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_AON	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VS_AON	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_AON	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_AON	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VS_AON	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VS_AON				
STRAP3	+3VS_AON				
STRAP4	+3VS_AON				

DEVID_SEL	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

PCIE_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GT	Samsung	K4G41325FE-HC28	PD 45.3K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC4H24AJR-T2C 256X16	PD 34.8K							
	Micron	EDW4032BABG-60-F 256X16	PD 24.9K							

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR	Samsung	K4G80325FB-HC03	PD 4.99K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC8H24MJR-T2C	PD 30.1K							
	Micron	MT51J256M32HF-60:A	PD 10K							

Title			
VGA NOTE			
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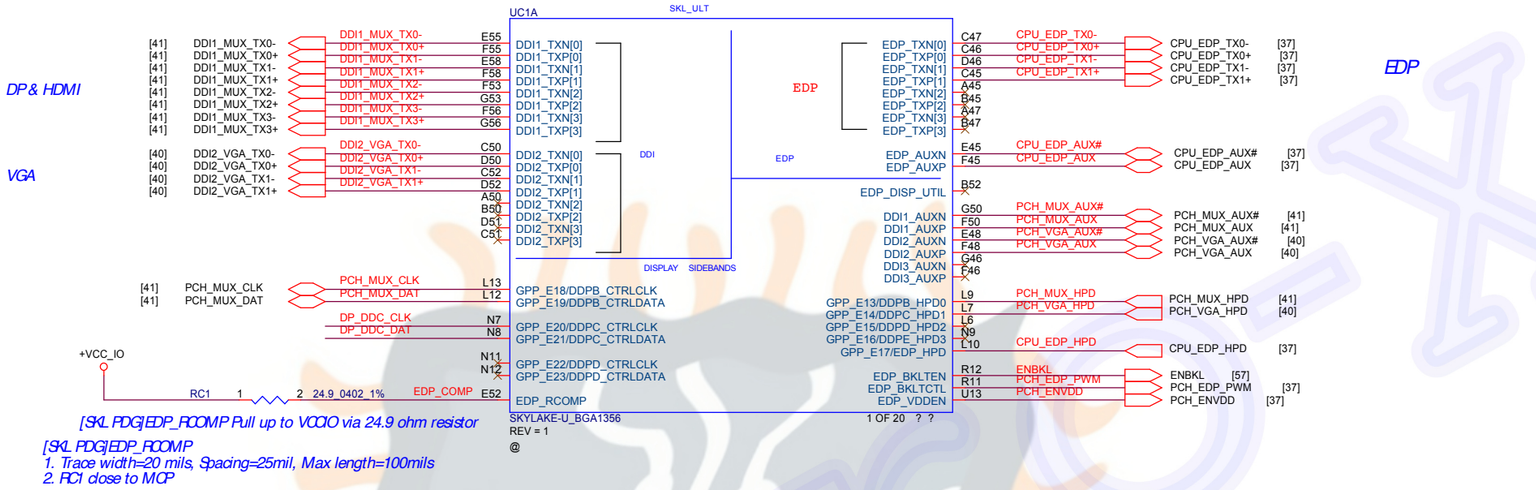
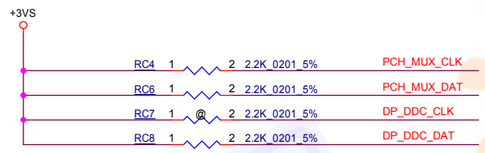
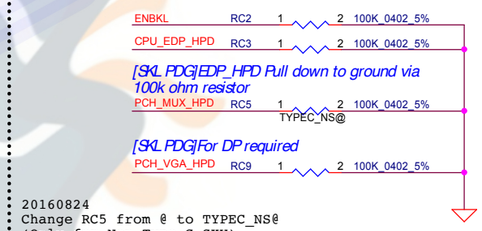


DDPB_CTRLDATA, DDPC_CTRLDATA Internal PD 20K



20160202
Install RC4,RC6 to fix dual display issue



20160824
Change RC5 from @ to TYPEC_NS@
(Only for Non Type-C SKU)

DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.

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Title: **KBL(1/16):DDI/EDP**

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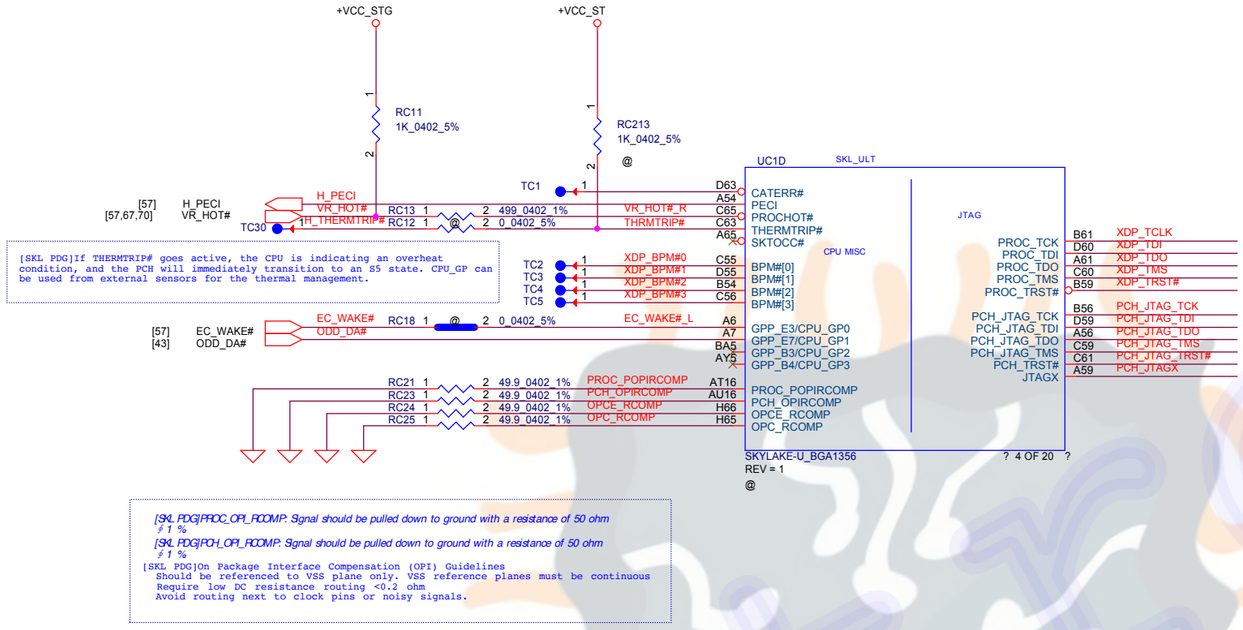

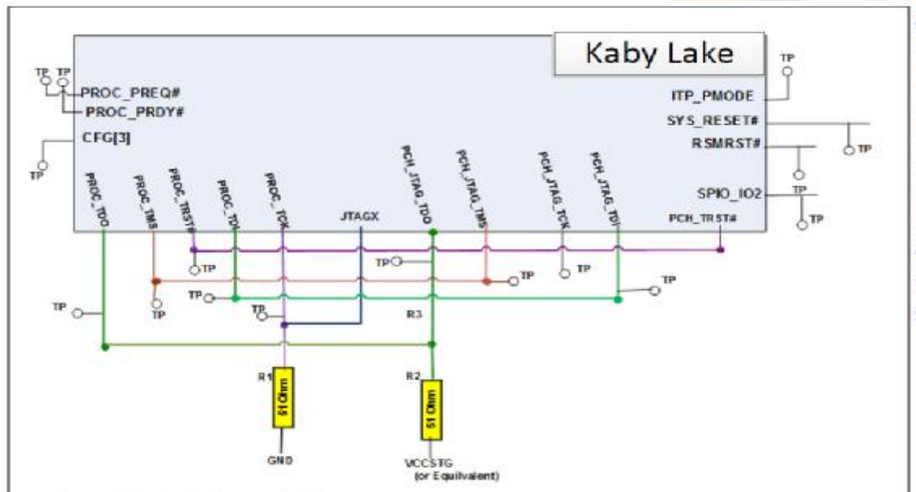

Figure 44-6. Connector Less Routing Topology

– Stubs on JTAG nets should not more than 200ps
– R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
– Place Test point pads on Secondary side
– Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2 VCCOBS_AB (PCH V1.0 A), GND pins (2)
– TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
– TP = Test Point Pad (size – 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

XDP_TCLK RC29 1 DCI@ 2 0_0402_5% PCH_JTAGX
XDP_TDI RC30 1 DCI@ 2 0_0402_5% PCH_JTAG_TDI
XDP_TDO RC31 1 DCI@ 2 0_0402_5% PCH_JTAG_TDO
XDP_TMS RC32 1 DCI@ 2 0_0402_5% PCH_JTAG_TMS
XDP_TRST# RC33 1 DCI@ 2 0_0402_5% PCH_JTAG_TRST#

Close to UC1

Termination option

XDP_TCLK

PROC_TCK Termination:
51 ohm +/- 5% pull down to GNG (Ground)
Placed to within 200ps (1100 mil) or PROC_TCK pin

PCH_JTAG_TDO

PCH_JTAG_TDO Termination:
51ohm +/- 5% pull up to VccSTG or equivalent.
Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin

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Title: KBL(2/16):MISC/JTAG
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TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

[22] DDR_A_D[63..0]

UC1B — SKL_ULT — DDR CH - A

DDR_A_D0	AL71	DDR0_DQ[0]	
DDR_A_D1	AL68	DDR0_DQ[1]	
DDR_A_D2	AN68	DDR0_DQ[2]	
DDR_A_D3	AN69	DDR0_DQ[3]	
DDR_A_D4	AL70	DDR0_DQ[4]	
DDR_A_D5	AL69	DDR0_DQ[5]	
DDR_A_D6	AN70	DDR0_DQ[6]	
DDR_A_D7	AN71	DDR0_DQ[7]	
DDR_A_D8	AR70	DDR0_DQ[8]	
DDR_A_D9	AR68	DDR0_DQ[9]	
DDR_A_D10	AU71	DDR0_DQ[10]	
DDR_A_D11	AU68	DDR0_DQ[11]	
DDR_A_D12	AR71	DDR0_DQ[12]	
DDR_A_D13	AR69	DDR0_DQ[13]	
DDR_A_D14	AU70	DDR0_DQ[14]	
DDR_A_D15	AU69	DDR0_DQ[15]	
DDR_A_D16	BB65	DDR0_DQ[16]/DDR0_DQ[32]	
DDR_A_D17	AW65	DDR0_DQ[17]/DDR0_DQ[33]	
DDR_A_D18	AW63	DDR0_DQ[18]/DDR0_DQ[34]	
DDR_A_D19	AY63	DDR0_DQ[19]/DDR0_DQ[35]	
DDR_A_D20	BA65	DDR0_DQ[20]/DDR0_DQ[36]	
DDR_A_D21	AY65	DDR0_DQ[21]/DDR0_DQ[37]	
DDR_A_D22	BA63	DDR0_DQ[22]/DDR0_DQ[38]	
DDR_A_D23	BB63	DDR0_DQ[23]/DDR0_DQ[39]	
DDR_A_D24	BA61	DDR0_DQ[24]/DDR0_DQ[40]	
DDR_A_D25	AW61	DDR0_DQ[25]/DDR0_DQ[41]	
DDR_A_D26	BB59	DDR0_DQ[26]/DDR0_DQ[42]	
DDR_A_D27	AW59	DDR0_DQ[27]/DDR0_DQ[43]	
DDR_A_D28	BB61	DDR0_DQ[28]/DDR0_DQ[44]	
DDR_A_D29	AY61	DDR0_DQ[29]/DDR0_DQ[45]	
DDR_A_D30	BA59	DDR0_DQ[30]/DDR0_DQ[46]	
DDR_A_D31	AY59	DDR0_DQ[31]/DDR0_DQ[47]	
DDR_A_D32	AY39	DDR0_DQ[32]/DDR1_DQ[0]	
DDR_A_D33	AW39	DDR0_DQ[33]/DDR1_DQ[1]	
DDR_A_D34	AY37	DDR0_DQ[34]/DDR1_DQ[2]	
DDR_A_D35	AW37	DDR0_DQ[35]/DDR1_DQ[3]	
DDR_A_D36	BB39	DDR0_DQ[36]/DDR1_DQ[4]	
DDR_A_D37	BA39	DDR0_DQ[37]/DDR1_DQ[5]	
DDR_A_D38	BA37	DDR0_DQ[38]/DDR1_DQ[6]	
DDR_A_D39	BB37	DDR0_DQ[39]/DDR1_DQ[7]	
DDR_A_D40	AY35	DDR0_DQ[40]/DDR1_DQ[8]	
DDR_A_D41	AW35	DDR0_DQ[41]/DDR1_DQ[9]	
DDR_A_D42	AY33	DDR0_DQ[42]/DDR1_DQ[10]	
DDR_A_D43	AW33	DDR0_DQ[43]/DDR1_DQ[11]	
DDR_A_D44	BB35	DDR0_DQ[44]/DDR1_DQ[12]	
DDR_A_D45	BA35	DDR0_DQ[45]/DDR1_DQ[13]	
DDR_A_D46	BA33	DDR0_DQ[46]/DDR1_DQ[14]	
DDR_A_D47	BB33	DDR0_DQ[47]/DDR1_DQ[15]	
DDR_A_D48	AY31	DDR0_DQ[48]/DDR1_DQ[32]	
DDR_A_D49	AW31	DDR0_DQ[49]/DDR1_DQ[33]	
DDR_A_D50	AY29	DDR0_DQ[50]/DDR1_DQ[34]	
DDR_A_D51	AW29	DDR0_DQ[51]/DDR1_DQ[35]	
DDR_A_D52	BB31	DDR0_DQ[52]/DDR1_DQ[36]	
DDR_A_D53	BA31	DDR0_DQ[53]/DDR1_DQ[37]	
DDR_A_D54	BA29	DDR0_DQ[54]/DDR1_DQ[38]	
DDR_A_D55	BB29	DDR0_DQ[55]/DDR1_DQ[39]	
DDR_A_D56	AY27	DDR0_DQ[56]/DDR1_DQ[40]	
DDR_A_D57	AW27	DDR0_DQ[57]/DDR1_DQ[41]	
DDR_A_D58	AY25	DDR0_DQ[58]/DDR1_DQ[42]	
DDR_A_D59	AW25	DDR0_DQ[59]/DDR1_DQ[43]	
DDR_A_D60	BB27	DDR0_DQ[60]/DDR1_DQ[44]	
DDR_A_D61	BA27	DDR0_DQ[61]/DDR1_DQ[45]	
DDR_A_D62	BA25	DDR0_DQ[62]/DDR1_DQ[46]	
DDR_A_D63	BB25	DDR0_DQ[63]/DDR1_DQ[47]	

SKYLAKE-U_BGA1356
REV = 1
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DDR0_CKN[0]	AU53	DDR_A_DDRCLK0_1866M#	DDR_A_DDRCLK0_1866M# [22]
DDR0_CKP[0]	AT53	DDR_A_DDRCLK0_1866M	DDR_A_DDRCLK0_1866M [22]
DDR0_CKN[1]	AU55	DDR_A_DDRCLK1_1866M#	DDR_A_DDRCLK1_1866M# [22]
DDR0_CKP[1]	AT55	DDR_A_DDRCLK1_1866M	DDR_A_DDRCLK1_1866M [22]
	BA56	DDR_A_CKE0	
DDR0_CKE[0]	BB56	DDR_A_CKE1	DDR_A_CKE0 [22]
DDR0_CKE[1]	AW56		DDR_A_CKE1 [22]
DDR0_CKE[2]	AY56		
DDR0_CKE[3]			
	AU45	DDR_A_CS0#	
DDR0_CS#[0]	AU43	DDR_A_CS1#	DDR_A_CS0# [22]
DDR0_CS#[1]	AT45	DDR_A_ODT0	DDR_A_CS1# [22]
DDR0_ODT[0]	AT43	DDR_A_ODT1	DDR_A_ODT0 [22]
DDR0_ODT[1]			DDR_A_ODT1 [22]
	BA51	DDR_A_MA5	
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BB54	DDR_A_MA9	
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BA52	DDR_A_MA6	
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	AY52	DDR_A_MA8	
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AW52	DDR_A_MA7	
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AY55	DDR_A_BG0	DDR_A_BG0 [22]
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AW54	DDR_A_MA12	
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	BA54	DDR_A_MA11	
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA55	DDR_A_ACT_N	DDR_A_ACT_N [22]
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	AY54	DDR_A_BG1	DDR_A_BG1 [22]
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]			
	AU46	DDR_A_MA13	
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU48	DDR_A_MA15	
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AT46	DDR_A_MA14	
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AU50	DDR_A_MA16	
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU52	DDR_A_BA0	DDR_A_BA0 [22]
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AY51	DDR_A_MA2	
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AT48	DDR_A_BA1	DDR_A_BA1 [22]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT50	DDR_A_MA10	
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	BB50	DDR_A_MA1	
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	AY50	DDR_A_MA0	
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	BA50	DDR_A_MA3	
DDR0_MA[3]	BB52	DDR_A_MA4	
DDR0_MA[4]			
	AM70	DDR_A_DQS#0	
DDR0_DQSN[0]	AM69	DDR_A_DQS0	
DDR0_DQSP[0]	AT69	DDR_A_DQS#1	
DDR0_DQSN[1]	AT70	DDR_A_DQS1	
DDR0_DQSP[1]	BA64	DDR_A_DQS#2	
DDR0_DQSN[2]/DDR0_DQSN[4]	AY64	DDR_A_DQS2	
DDR0_DQSP[2]/DDR0_DQSP[4]	AY60	DDR_A_DQS#3	
DDR0_DQSN[3]/DDR0_DQSN[5]	BA38	DDR_A_DQS3	
DDR0_DQSP[3]/DDR0_DQSP[5]	AY38	DDR_A_DQS#4	
DDR0_DQSN[4]/DDR1_DQSN[0]	AY34	DDR_A_DQS4	
DDR0_DQSP[4]/DDR1_DQSP[0]	BA34	DDR_A_DQS#5	
DDR0_DQSN[5]/DDR1_DQSN[1]	BA30	DDR_A_DQS5	
DDR0_DQSP[5]/DDR1_DQSP[1]	AY30	DDR_A_DQS#6	
DDR0_DQSN[6]/DDR1_DQSN[4]	AY26	DDR_A_DQS6	
DDR0_DQSP[6]/DDR1_DQSP[4]	BA26	DDR_A_DQS#7	
DDR0_DQSN[7]/DDR1_DQSN[5]		DDR_A_DQS7	
DDR0_DQSP[7]/DDR1_DQSP[5]			
	AW50	DDR_A_ALERT_N	DDR_A_ALERT_N [22]
DDR0_ALERT#	AT52	DDR_A_PARITY	DDR_A_PARITY [22]
DDR0_PAR			
	AY67	DDR4_VREF_CA_CPU_A	DDR4_VREF_CA_CPU_A [22]
DDR_VREF_CA	AY68	DDR4_VREF_DQ_CPU_A	TC31
DDR0_VREF_DQ	BA67	DDR4_VREF_DQ_CPU_B	DDR4_VREF_DQ_CPU_B [23]
DDR1_VREF_DQ			
	AW67	DDR_PG_CTRL	
DDR_VTT_CNTL			

DDR_A_MA0 … DDR_A_MA16 → DDR_A_MA[0..16] [22]

DDR_A_DQS#0 … DDR_A_DQS#7 → DDR_A_DQS#[0..7] [22]

DDR_A_DQS0 … DDR_A_DQS7 → DDR_A_DQS[0..7] [22]

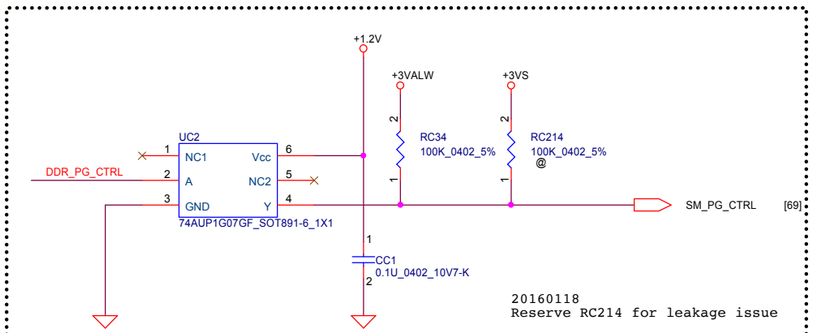

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TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF85	DDR1_DQ[0]	DDR0_DQ[16]
	AF84	DDR1_DQ[1]	DDR0_DQ[17]
	AK85	DDR1_DQ[2]	DDR0_DQ[18]
	AK84	DDR1_DQ[3]	DDR0_DQ[19]
	AF86	DDR1_DQ[4]	DDR0_DQ[20]
	AF87	DDR1_DQ[6]	DDR0_DQ[21]
	AK87	DDR1_DQ[6]	DDR0_DQ[22]
	AK86	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF88	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH88	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF89	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH89	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT86	DDR1_DQ[16]	DDR0_DQ[48]
	AU86	DDR1_DQ[17]	DDR0_DQ[49]
	AP85	DDR1_DQ[18]	DDR0_DQ[50]
	AN85	DDR1_DQ[19]	DDR0_DQ[51]
	AN86	DDR1_DQ[20]	DDR0_DQ[52]
	AP86	DDR1_DQ[21]	DDR0_DQ[53]
	AT85	DDR1_DQ[22]	DDR0_DQ[54]
	AU85	DDR1_DQ[23]	DDR0_DQ[55]
	AT81	DDR1_DQ[24]	DDR0_DQ[56]
	AU81	DDR1_DQ[25]	DDR0_DQ[57]
	AP80	DDR1_DQ[26]	DDR0_DQ[58]
	AN80	DDR1_DQ[27]	DDR0_DQ[59]
	AN81	DDR1_DQ[28]	DDR0_DQ[60]
	AP81	DDR1_DQ[29]	DDR0_DQ[61]
	AT80	DDR1_DQ[30]	DDR0_DQ[62]
	AU80	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AT38	DDR1_DQ[39]	DDR1_DQ[23]
	AR37	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AT33	DDR1_DQ[42]	DDR1_DQ[26]
	AR33	DDR1_DQ[43]	DDR1_DQ[27]
	AP33	DDR1_DQ[44]	DDR1_DQ[28]
	AR30	DDR1_DQ[45]	DDR1_DQ[29]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY45	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

[23] DDR_B_D[0..63]

UC1C — SKL_ULT

DDR_B_D0 AF65
DDR_B_D1 AF64
DDR_B_D2 AK65
DDR_B_D3 AK64
DDR_B_D4 AF66
DDR_B_D5 AF67
DDR_B_D6 AK67
DDR_B_D7 AK66
DDR_B_D8 AF70
DDR_B_D9 AF68
DDR_B_D10 AH71
DDR_B_D11 AH68
DDR_B_D12 AF71
DDR_B_D13 AF69
DDR_B_D14 AH70
DDR_B_D15 AH69
DDR_B_D16 AT66
DDR_B_D17 AU66
DDR_B_D18 AP65
DDR_B_D19 AN65
DDR_B_D20 AN66
DDR_B_D21 AP66
DDR_B_D22 AT65
DDR_B_D23 AU65
DDR_B_D24 AT61
DDR_B_D25 AU61
DDR_B_D26 AP60
DDR_B_D27 AN60
DDR_B_D28 AN61
DDR_B_D29 AP61
DDR_B_D30 AT60
DDR_B_D31 AU60
DDR_B_D32 AU40
DDR_B_D33 AT40
DDR_B_D34 AT37
DDR_B_D35 AU37
DDR_B_D36 AR40
DDR_B_D37 AP40
DDR_B_D38 AP37
DDR_B_D39 AR37
DDR_B_D40 AT33
DDR_B_D41 AU33
DDR_B_D42 AU30
DDR_B_D43 AT30
DDR_B_D44 AR33
DDR_B_D45 AP33
DDR_B_D46 AR30
DDR_B_D47 AP30
DDR_B_D48 AU27
DDR_B_D49 AT27
DDR_B_D50 AT25
DDR_B_D51 AU25
DDR_B_D52 AP27
DDR_B_D53 AN27
DDR_B_D54 AN25
DDR_B_D55 AP25
DDR_B_D56 AT22
DDR_B_D57 AU22
DDR_B_D58 AU21
DDR_B_D59 AT21
DDR_B_D60 AN22
DDR_B_D61 AP22
DDR_B_D62 AP21
DDR_B_D63 AN21

DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
DDR1_DQ[30]/DDR0_DQ[62]
DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
DDR1_DQ[33]/DDR1_DQ[17]
DDR1_DQ[34]/DDR1_DQ[18]
DDR1_DQ[35]/DDR1_DQ[19]
DDR1_DQ[36]/DDR1_DQ[20]
DDR1_DQ[37]/DDR1_DQ[21]
DDR1_DQ[38]/DDR1_DQ[22]
DDR1_DQ[39]/DDR1_DQ[23]
DDR1_DQ[40]/DDR1_DQ[24]
DDR1_DQ[41]/DDR1_DQ[25]
DDR1_DQ[42]/DDR1_DQ[26]
DDR1_DQ[43]/DDR1_DQ[27]
DDR1_DQ[44]/DDR1_DQ[28]
DDR1_DQ[45]/DDR1_DQ[29]
DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
DDR1_DQ[49]
DDR1_DQ[50]
DDR1_DQ[51]
DDR1_DQ[52]
DDR1_DQ[53]
DDR1_DQ[54]
DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]

DDR1_CKN[0] AN45
DDR1_CKN[1] AN46
DDR1_CKP[0] AP45
DDR1_CKP[1] AP46
DDR1_CKE[0] AN56
DDR1_CKE[1] AP55
DDR1_CKE[2] AN55
DDR1_CKE[3] AP53
DDR1_CS#[0] BB42
DDR1_CS#[1] AY42
DDR1_ODT[0] BA42
DDR1_ODT[1] AW42

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AY48
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AP50
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] BA48
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] BB48
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AP48
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AP52
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AN50
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AN48
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AN53
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AN52

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] BA43
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AY43
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AY44
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AW44
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] BB44
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AY47
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] BA44
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AW46
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AY46
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] BA46
DDR1_MA[3] BB46
DDR1_MA[4] BA47

DDR1_DQSN[0]/DDR0_DQSN[2] AH66
DDR1_DQSP[0]/DDR0_DQSP[2] AH65
DDR1_DQSN[1]/DDR0_DQSN[3] AG69
DDR1_DQSP[1]/DDR0_DQSP[3] AG70
DDR1_DQSN[2]/DDR0_DQSN[6] AR66
DDR1_DQSP[2]/DDR0_DQSP[6] AR65
DDR1_DQSN[3]/DDR0_DQSN[7] AR61
DDR1_DQSP[3]/DDR0_DQSP[7] AR60
DDR1_DQSN[4]/DDR1_DQSN[2] AT38
DDR1_DQSP[4]/DDR1_DQSP[2] AR38
DDR1_DQSN[5]/DDR1_DQSN[3] AT32
DDR1_DQSP[5]/DDR1_DQSP[3] AR32
DDR1_DQSN[6] AR25
DDR1_DQSP[6] AR27
DDR1_DQSN[7] AR22
DDR1_DQSP[7] AR21

DDR1_ALERT# AN43
DDR1_PAR AP43
DRAM_RESET# AT13
DDR_RCOMP[0] AR18
DDR_RCOMP[1] AT18
DDR_RCOMP[2] AU18

DDR CH - B

SKYLAKE-U_BGA1356
REV = 1
@

3 OF 20 ?

DDR_B_DDRCLK0_1866M# AN45 → DDR_B_DDRCLK0_1866M# [23]
DDR_B_DDRCLK1_1866M# AN46 → DDR_B_DDRCLK1_1866M# [23]
DDR_B_DDRCLK0_1866M AP45 → DDR_B_DDRCLK0_1866M [23]
DDR_B_DDRCLK1_1866M AP46 → DDR_B_DDRCLK1_1866M [23]
DDR_B_CKE0 AN56 → DDR_B_CKE0 [23]
DDR_B_CKE1 AP55 → DDR_B_CKE1 [23]
DDR_B_CS0# BB42 → DDR_B_CS0# [23]
DDR_B_CS1# AY42 → DDR_B_CS1# [23]
DDR_B_ODT0 BA42 → DDR_B_ODT0 [23]
DDR_B_ODT1 AW42 → DDR_B_ODT1 [23]
DDR_B_BG0 AP52 → DDR_B_BG0 [23]
DDR_B_ACT_N AN53 → DDR_B_ACT_N [23]
DDR_B_BG1 AN52 → DDR_B_BG1 [23]
DDR_B_BA0 BB44 → DDR_B_BA0 [23]
DDR_B_BA1 BA44 → DDR_B_BA1 [23]
DDR_B_ALERT_N AN43 → DDR_B_ALERT_N [23]
DDR_B_PARITY AP43 → DDR_B_PARITY [23]
DDR4_DRAMRST_N AT13 → DDR4_DRAMRST_N [22,23]

SM_RCOMP0 AR18 — RC36 1 — 2 121_0402_1%
SM_RCOMP1 AT18 — RC38 1 — 2 80.6_0402_1%
SM_RCOMP2 AU18 — RC39 1 — 2 100_0402_1%

[KBL PDG]for DDR4 COMPENSATION
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

DDR_B_MA0 … DDR_B_MA16 → DDR_B_MA[0..16] [23]

DDR_B_DQS#0 … DDR_B_DQS#7 → DDR_B_DQS#[0..7] [23]

DDR_B_DQS0 … DDR_B_DQS7 → DDR_B_DQS[0..7] [23]

+1.2V
RC35 2 1 470_0402_5%
DDR4_DRAMRST_N — RC37 1 @ 2 0_0402_5% — DDR4_DRAMRST# [22,23]

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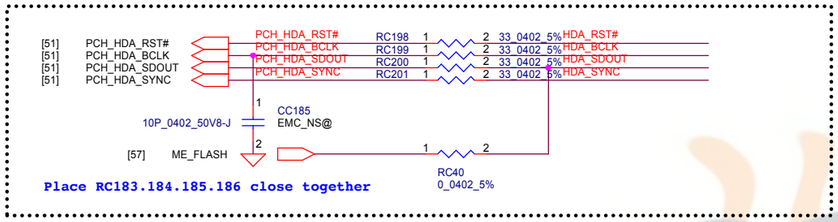
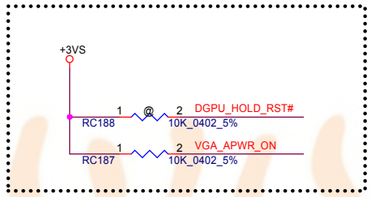
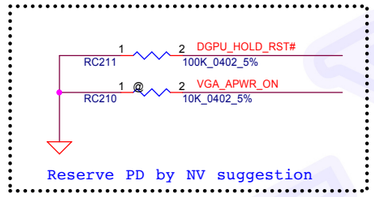
Title: KBL(4/16):DDR4 CH.B
Size: Custom | Document Number: SKYWALKER | Rev: 2.0
Date: Thursday, August 25, 2016 | Sheet 8 of 82

[KBL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in
the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.

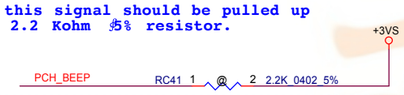




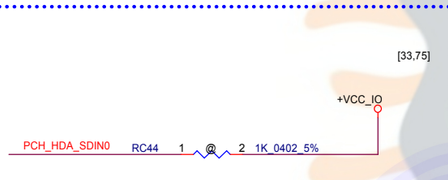


Note:
SPKR (PC_BEEP) has an integrated weak pull-down resistor (20 K ohm nominal) to disable Top-Block Sway by default.

To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 Kohm ±5% resistor.

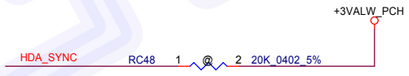


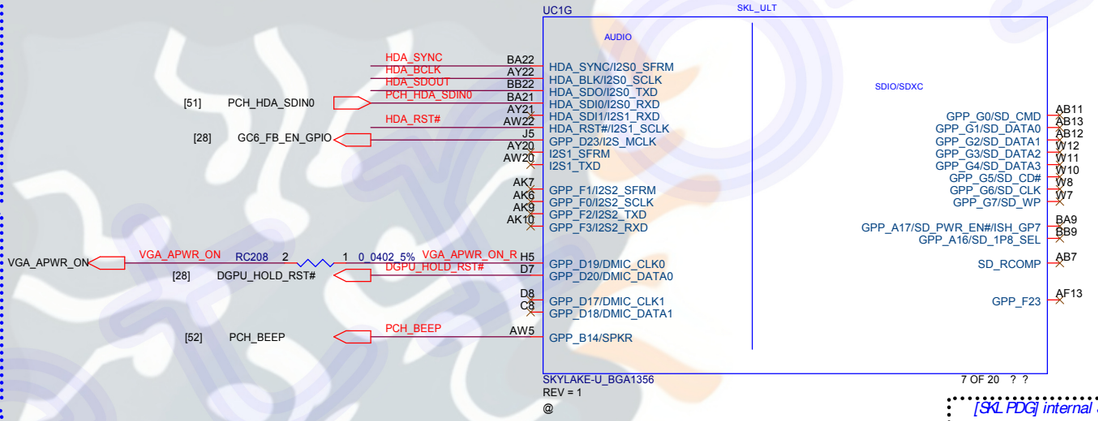
Note:
Internal PD 20K



Note:
HDA_SDO should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.

Note:
Internal PD 20K





[SKL PDG] internal SD Card

Not support internal SD card. Remove SD_RCOMP

Security Classification	LC Future Center Secret Data		
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Title: **KBL(5/16):HDA/SDIO**

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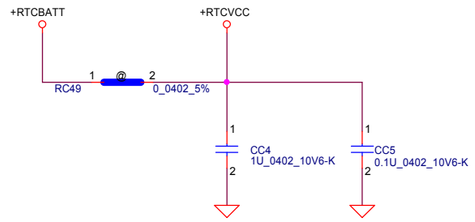
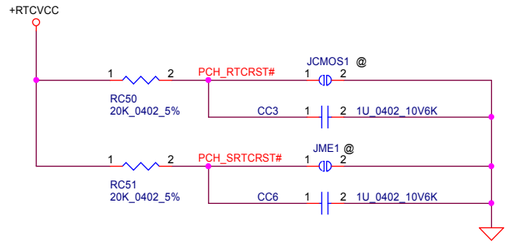
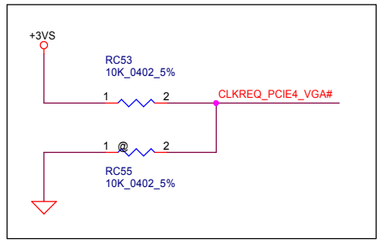
RTC External Circuit

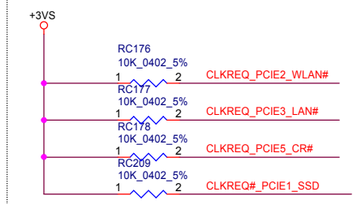
+RTCBATT, +RTCVCC
Trace width = 20mils



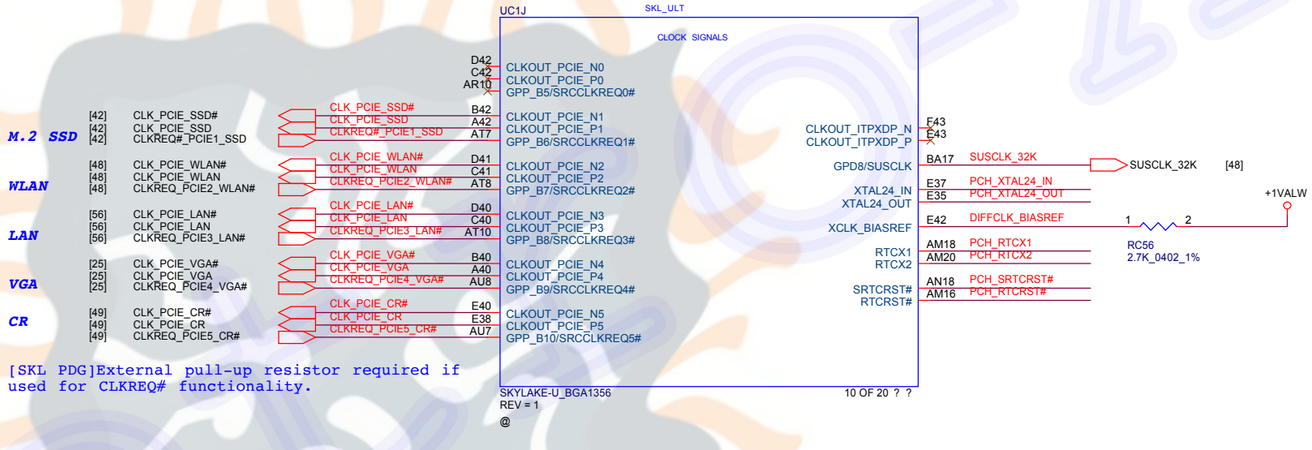
JCMOS, JME Setting, Need Under DDR Door





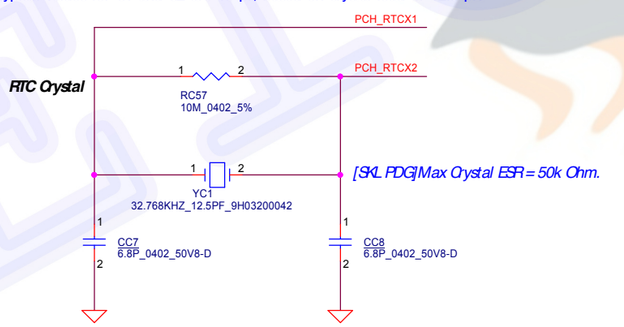


Place RC176,177,178,209 close together



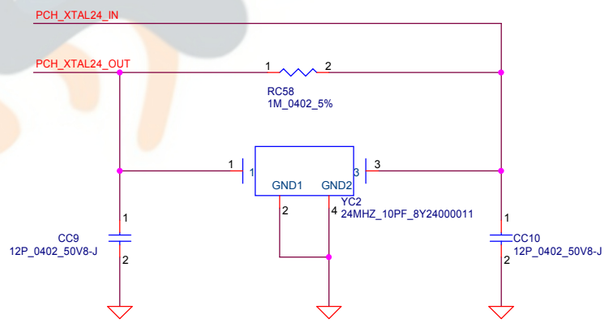
[SKL PDG]External pull-up resistor required if used for CLKREQ# functionality.

[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.



20160127
Change CC7/CC8 to 6.8p by vender suggestion

[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(6/16):CLOCK SIGNALS**

Size: Custom | Document Number: **SKYWALKER** | Rev: 2.0

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Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

+3VALW_PCH
SMBALERT# — RC59 1 — 2 — 1K_0402_5%

GPP_C2, Internal PD 20K

JTAG ODT

SPI0_MOSI

+3VALW_PCH
SPI_SI — RC62 1 @ 2 — 8.2K_0402_5%

+3VALW_PCH
SPI_SO — RC65 1 @ 2 — 8.2K_0402_5%

GPP_C5, Internal PD 20K

*L: LPC
H: eSPI

+3VALW_PCH
SML0ALERT# — RC67 1 @ 2 — 1K_0402_5%

+3VS
Place RC179,180,181 close together

RC1791 2 10K_0402_5% SERIRQ
RC1801 2 10K_0402_5% EC_SCI#
RC1811 2 10K_0402_5% KBRST#
RC72 1 2 4.7K_0402_5% CP_SMB_CLK
RC76 1 2 4.7K_0402_5% CP_SMB_DAT
RC2121 2 10K_0402_5% GPU_EVENT#

PCH_SMB_CLK — RC71 1 2 2.2K_0402_1%
PCH_SMB_DATA — RC73 1 2 2.2K_0402_1%
PCH_SML1CLK — RC74 1 2 2.2K_0402_1%
PCH_SML1DATA — RC75 1 2 2.2K_0402_1%

Add RC212 PU by NV suggestion

SML1ALERT# — RC77 1 @ 2 1K_0402_5%

close to CPU

UC1E — SKL_ULT

SPI - FLASH
[21,58] SPI_CLK — AV2 SPI0_CLK
[21,58] SPI_SO — AW3 SPI0_MISO
[21,58] SPI_SI — AV3 SPI0_MOSI
[21] SPI_IO2 — AW2 SPI0_IO2
[21] SPI_IO3 — AU4 SPI0_IO3
[21] SPI_CS0#_8MB — AU3 SPI0_CS0#
[21] SPI_CS1#_4MB — AU2 SPI0_CS1#
[58] SPI_CS2#_TPM — AU1 SPI0_CS2#

SPI - TOUCH
M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C LINK
[48] CL_CLK_WLAN — G3 CL_CLK
[48] CL_DATA_WLAN — G2 CL_DATA
[48] CL_RST_WLAN# — G1 CL_RST#

[25] All_GPU_PWRGD — RC107 1 2 0_0402_5% — All_GPU_PWRGD_R
[28] GPU_EVENT# — GPU_EVENT#
[57] EC_SCI# — EC_SCI#

[57] KBRST# — KBRST# — AW13 GPP_A0/RCIN#
CC183 10P_0402_50V8-J — [57,58] SERIRQ — SERIRQ — AY11 GPP_A6/SERIRQ
CC183 EMC_NS@

SKYLAKE-U_BGA1356
REV = 1
@

SMBUS, SMLINK
R7 GPP_C0/SMBCLK — PCH_SMB_CLK
R8 GPP_C1/SMBDATA — PCH_SMB_DATA
R10 GPP_C2/SMBALERT# — SMBALERT#
R9 GPP_C3/SML0CLK
W2 GPP_C4/SML0DATA
W1 GPP_C5/SML0ALERT# — SML0ALERT#
W3 GPP_C6/SML1CLK — PCH_SML1CLK
V3 GPP_C7/SML1DATA — PCH_SML1DATA
AM7 GPP_B23/SML1ALERT#/PCHHOT# — SML1ALERT#

LPC
AY13 GPP_A1/LAD0/ESPI_IO0 — LPC_AD0 [57]
BA13 GPP_A2/LAD1/ESPI_IO1 — LPC_AD1 [57]
BB13 GPP_A3/LAD2/ESPI_IO2 — LPC_AD2 [57]
AY12 GPP_A4/LAD3/ESPI_IO3 — LPC_AD3 [57]
BA12 GPP_A5/LFRAME#/ESPI_CS# — LPC_FRAME# [57]
BA11 GPP_A14/SUS_STAT#/ESPI_RESET# — SUS_STAT#

AW9 GPP_A9/CLKOUT_LPC0/ESPI_CLK — PCH_PCI_CLK_R — RC63 0_0402_5% — TC7
AY9 GPP_A10/CLKOUT_LPC1
AW11 GPP_A8/CLKRUN# — CLKRUN# — RC66 8.2K_0402_5% — +3VS
RC64 22_0402_5% — CLK_PCI_EC [57]
CC184 10P_0402_50V8-J — EMC_NS@

5 OF 20 ? ?

Close to UC1

DIMM1, DIMM2, Security EEPROM, Click Pad

EC,dGPU,Thermal Sensor

SB00000YS00
2N7002KDWH_SOT363-6
QC1A

PCH_SMB_CLK — CP_SMB_CLK [22,23,63]
+3VS
Plan to remove QC1 after SDV
PCH_SMB_DATA — CP_SMB_DAT [22,23,63]

QC1B
2N7002KDWH_SOT363-6
SB00000YS00

SB00000YS00
2N7002KDWH_SOT363-6
QC2A

+3VS — PCH_SML1CLK — EC_SMB_CK3 [28,57,59,62]
PCH_SML1DATA — EC_SMB_DA3 [28,57,59,62]

QC2B
2N7002KDWH_SOT363-6
SB00000YS00

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Title: KBL(7/16):LPC/SPI/SMBUS/CL
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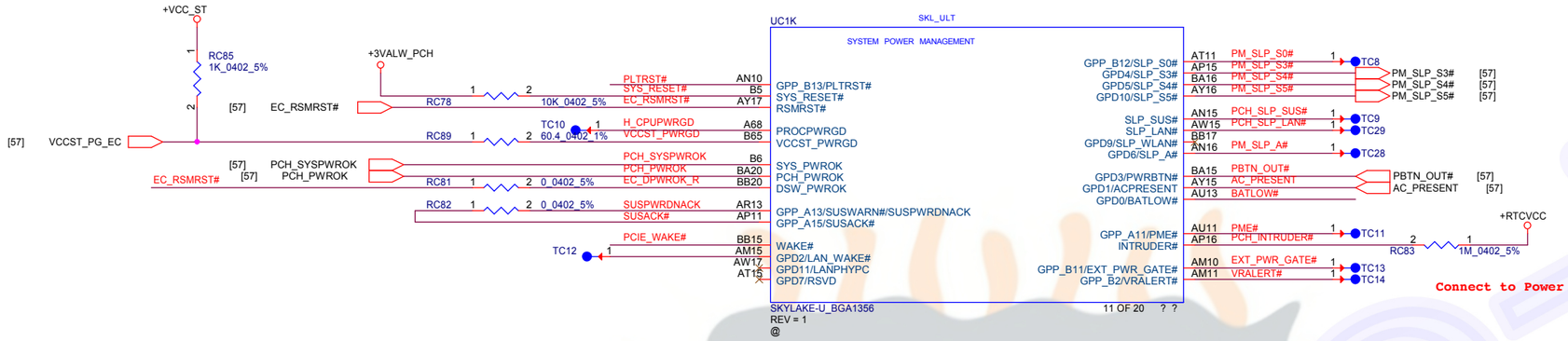
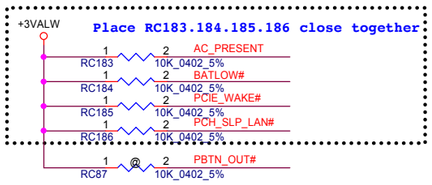
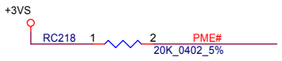
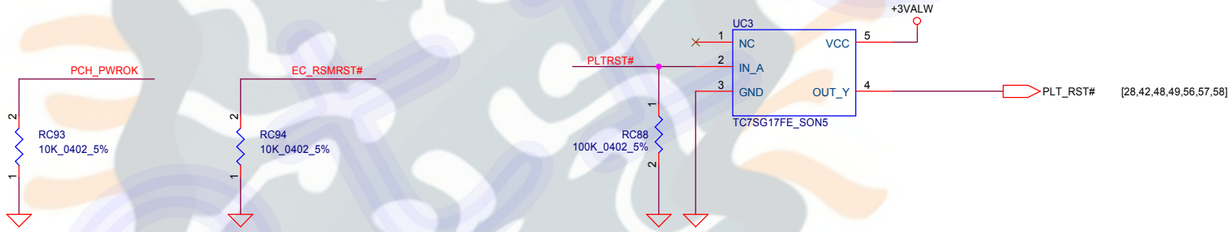






20160408
1.Add RC218 for PME# by BIOS request



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(8/16):SYSTEM PM

Size	Document Number	Rev
Custom	SKYWALKER	2.0

Date: Thursday, August 25, 2016 Sheet 12 of 82

3D_DET# RC215 2 1 10K_0402_5% +3VS

20160201
Add 3D_DET# pull up resistor

GPP_B22, Internal PD 20K

*L: SPI
H: LPC

GSPI1_MOSI 2 RC95 @ 1 1K_0402_5% +3VS

To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 K ±5 % resistor

GPP_B18, Internal PD 20K

*L: Disable "No Reboot" mode
H: Enable "No Reboot" mode

GSPI0_MOSI 2 RC102 @ 1 1K_0402_5% +3VS

To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 K ±5 % resistor

Project ID

	PLANARID0 (GPP_C8)	PLANARID1 (GPP_C9)	PLANARID2 (GPP_C10)	
L	14"	UMA	Skylake	
H	15"	DIS	Kabylake	

+3VS
RC96 10K_0402_5% KBL@
RC52 10K_0402_5% DIS@
RC99 10K_0402_5%
PLANARID0
PLANARID1
PLANARID2
RC101 10K_0402_5% SKL@
RC54 10K_0402_5% UMA@
RC104 10K_0402_5%

UC1F ?SKL_ULT
SKYLAKE-U_BGA1356
REV = 1
6 OF 20

LPSS
[48] RF_OFF# — RF_OFF# — AN8 GPP_B15/GSPI0_CS#
AP7 GPP_B16/GSPI0_CLK
AP8 GPP_B17/GSPI0_MISO
GSPI0_MOSI — AR7 GPP_B18/GSPI0_MOSI
[37] PCH_CMOS_ON — PCH_CMOS_ON — AM5 GPP_B19/GSPI1_CS#
AN7 GPP_B20/GSPI1_CLK
[48] BT_ON — BT_ON — AP5 GPP_B21/GSPI1_MISO
GSPI1_MOSI — AN5 GPP_B22/GSPI1_MOSI
PLANARID0 — AB1 GPP_C8/UART0_RXD
PLANARID1 — AB2 GPP_C9/UART0_TXD
PLANARID2 — W4 GPP_C10/UART0_RTS#
AB3 GPP_C11/UART0_CTS#
[48] UART2_RX — UART2_RX — AD1 GPP_C20/UART2_RXD
[48] UART2_TX — UART2_TX — AD2 GPP_C21/UART2_TXD
[60] F4_LED# — F4_LED# — AD3 GPP_C22/UART2_RTS#
[37] PCH_TSOFF# — PCH_TSOFF# — AD4 GPP_C23/UART2_CTS#
U7 GPP_C16/I2C0_SDA
U6 GPP_C17/I2C0_SCL
U8 GPP_C18/I2C1_SDA
U9 GPP_C19/I2C1_SCL
AH9 GPP_F4/I2C2_SDA
AH10 GPP_F5/I2C2_SCL
MIC_HW_EN — AH11 GPP_F6/I2C3_SDA
AH12 GPP_F7/I2C3_SCL
RC108 0_0402_5%
AF11 GPP_F8/I2C4_SDA
AF12 GPP_F9/I2C4_SCL

ISH
GPP_D9 P2
GPP_D10 P3
GPP_D11 P4 — DCI_CLK — DCI_CLK [55]
GPP_D12 P1 — DCI_DATA — DCI_DATA [55]
GPP_D5/ISH_I2C0_SDA M4
GPP_D6/ISH_I2C0_SCL N3
GPP_D7/ISH_I2C1_SDA N1
GPP_D8/ISH_I2C1_SCL N2
GPP_F10/I2C5_SDA/ISH_I2C2_SDA AD11
GPP_F11/I2C5_SCL/ISH_I2C2_SCL AD12
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA U1
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL U2
GPP_D15/ISH_UART0_RTS# U3
GPP_D16/ISH_UART0_CTS#/SML0BALERT# U4
GPP_C12/UART1_RXD/ISH_UART1_RXD AC1
GPP_C13/UART1_TXD/ISH_UART1_TXD AC2 — MUX_SW_PCH — MUX_SW_PCH [41]
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AC3
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB4
GPP_A18/ISH_GP0 AY8
GPP_A19/ISH_GP1 BA8
GPP_A20/ISH_GP2 BB7 — 3D_FW_GPIO — 3D_FW_GPIO [37]
GPP_A21/ISH_GP3 BA7 — 3D_DET# — 3D_DET# [37]
GPP_A22/ISH_GP4 AY7
GPP_A23/ISH_GP5 AW7
? GPP_A12/BM_BUSY#/ISH_GP6 AP13 — 1 — TC17

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Title: KBL(10/16):GPIO/CPU/MISC
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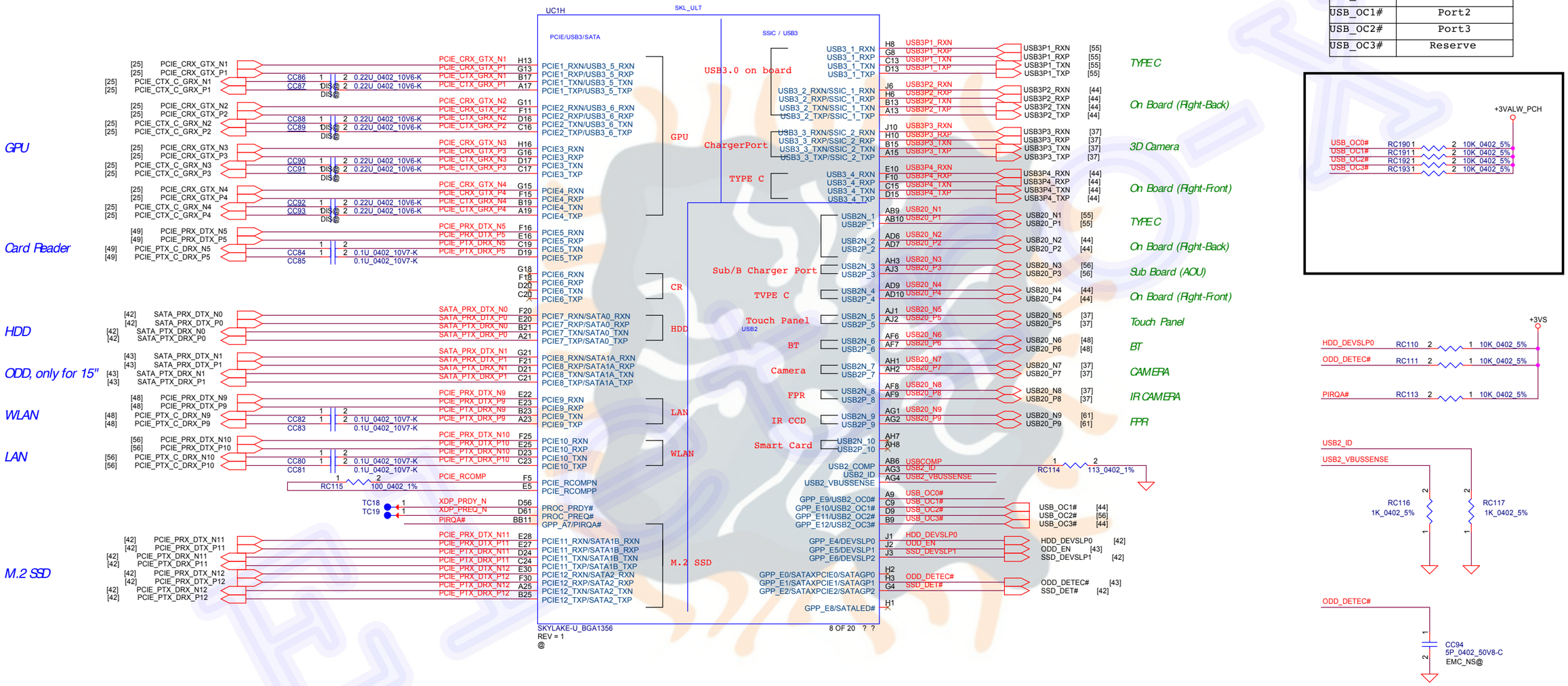

	USB Port Number
USB_OC0#	Port1
USB_OC1#	Port2
USB_OC2#	Port3
USB_OC3#	Reserve

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(11/16):PCIE/USB/SATA

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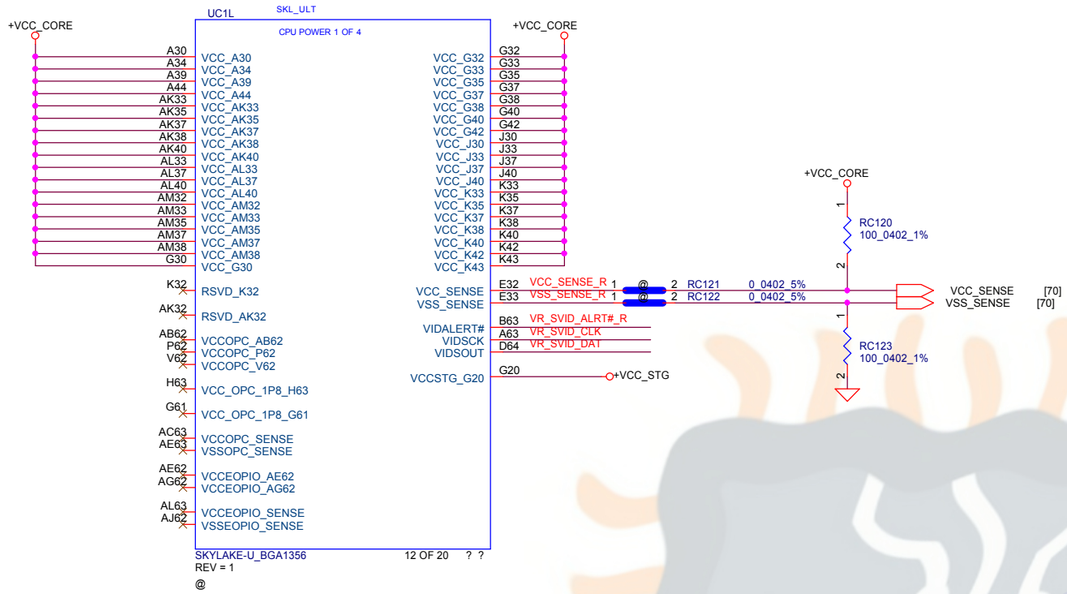
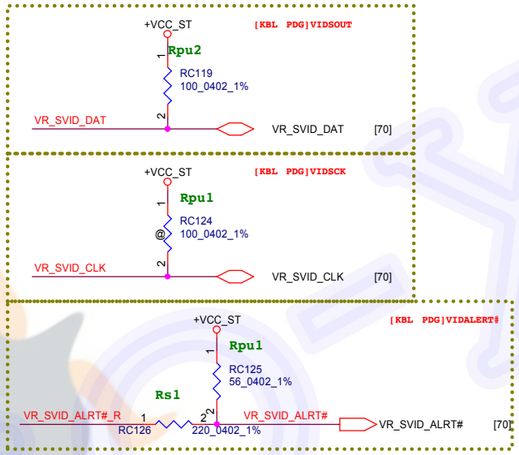
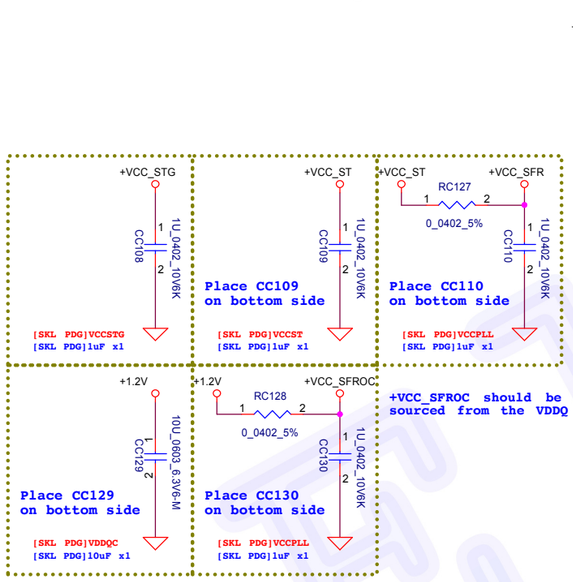
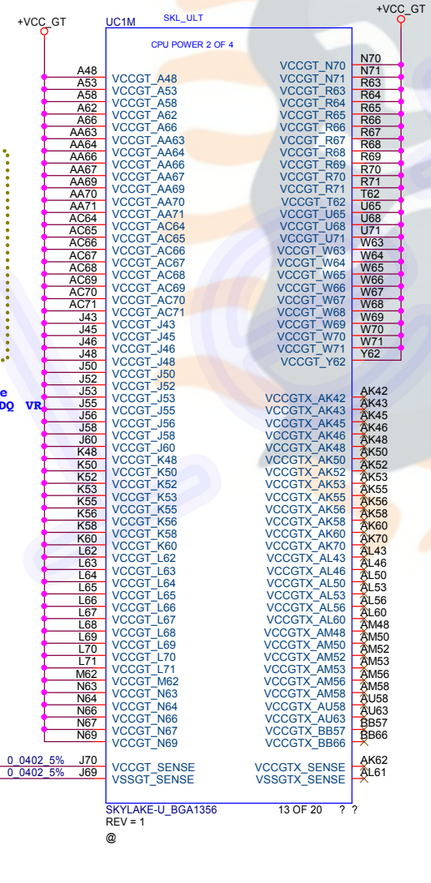
Table 10-10. SVID Bus Routing Guidelines

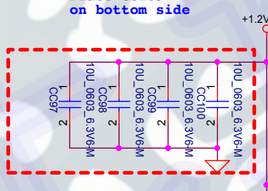
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

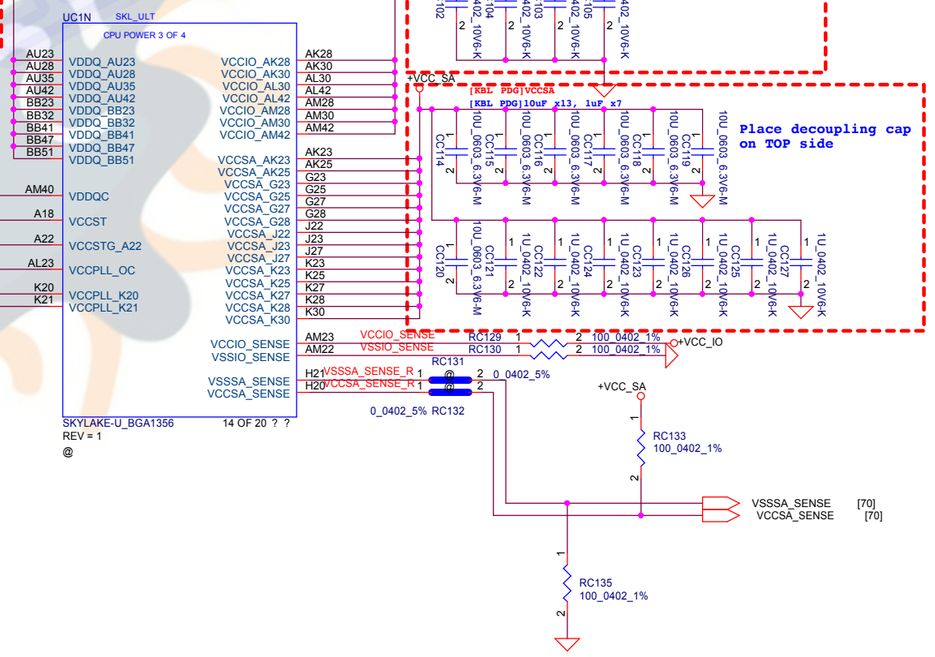












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Reserve for Sense Resistor

+1.8VALW — RC139 1 — 2 0_0603_5% — +1.8VALW_PCH

+3VALW — RC140 1 — 2 0_0805_5% — +3VALW_PCH

+1VALW — RC141 1 — 2 0_0805_5% — +1VALW_PCH

+1VALW — RC202 1 — 2 0_0805_5% — +VCC_MPHYGT

+VCC_MPHYGT — RC1451 2 0_0402_5% — +VCC_AMPHYPLL

+1VALW_PCH — RC1461 2 0_0402_5% — +1VALW_PLL

CC132 please close to N18

+VCC_MPHYGT — CC132 1U_0402_10V6K

[SKL PDG]VccAPLLEBB
[SKL PDG]1uF x1
[SKL PDG]Close N18,
Placement type:Edge<3mm(118mil)

SRAM Primary Well 1.0 V. Dedicated SRAM rail and can have on board power down gate control.

CC136 please close to AF20

+VCC_MPHYGT — @CC136 1U_0402_10V6K

[SKL PDG]VccSRAM
[SKL PDG]1uF x1
[SKL PDG]Close AF20,
Placement type:Edge<10mm(394mil)

VccMPHYGT(Mod PHY Externally Gated Primary 1.0 V: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.)

CC133 & CC134 please close to N15

+VCC_MPHYGT — CC133 1U_0402_10V6K — CC134 47U_0805_6.3V6-M

[SKL PDG]VccMPHYGT
[SKL PDG]1uF x1
[SKL PDG]Close N15,
Placement type:Edge<3mm(118mil)
[SKL PDG]47uF x1
[SKL PDG]Close N15,
Placement type:Edge<10mm(394mil)

Mod PHY Always On Primary 1.0 V: Always on primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic

CC137 please close to K17

+1VALW_PCH — CC137 1U_0402_10V6K

[SKL PDG]VccMPHYAON
[SKL PDG]1uF x1
[SKL PDG]Close K17,
Placement type:Edge<3mm(118mil)

Primary Well 1.0 V: For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.

please close to AG15 , Y16 & T16

+3VALW_PCH — CC140 1U_0402_10V6K — CC141 1U_0402_10V6K — CC142 1U_0402_10V6K

CC143 close to AB19

+1VALW_PCH — CC143 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]1uF x1
[SKL PDG]Close AB19,
Placement type:Edge<10mm(394mil)

+1VALW_PCH — CC181 22U_0603_6.3V6-M — CC131 22U_0603_6.3V6-M

+1VALW_PCH — CC182 22U_0603_6.3V6-M — CC135 22U_0603_6.3V6-M

UC1O — SKL_ULT — CPU POWER 4 OF 4

AB19, AB20, P18	VCCPRIM_1P0_AB19, VCCPRIM_1P0_AB20, VCCPRIM_1P0_P18	1100mA
AF18, AF19, V20, V21	VCCPRIM_CORE_AF18, VCCPRIM_CORE_AF19, VCCPRIM_CORE_V20, VCCPRIM_CORE_V21	500mA
AL1	DCPDSW_1P0	22mA
K17, L1	VCCMPHYAON_1P0_K17, VCCMPHYAON_1P0_L1	
N15, N16, N17, P15, P16	VCCMPHYGT_1P0_N15, VCCMPHYGT_1P0_N16, VCCMPHYGT_1P0_N17, VCCMPHYGT_1P0_P15, VCCMPHYGT_1P0_P16	1500mA
K15, L15	VCCAMPHYPLL_1P0_K15, VCCAMPHYPLL_1P0_L15	88mA
V15	VCCAPLL_1P0	26mA
AB17, Y18	VCCPRIM_1P0_AB17, VCCPRIM_1P0_Y18	
AD17, AD18, AJ17	VCCDSW_3P3_AD17, VCCDSW_3P3_AD18, VCCDSW_3P3_AJ17	118mA
AJ19	VCCHDA	68mA
AJ16	VCCSPI	
AF20, AF21, T19, T20	VCCSRAM_1P0_AF20, VCCSRAM_1P0_AF21, VCCSRAM_1P0_T19, VCCSRAM_1P0_T20	565mA
AJ21	VCCPRIM_3P3_AJ21	75mA
AK20	VCCPRIM_1P0_AK20	33mA
N18	VCCAPLLEBB	33mA

+PCH_CORE, +DCPDSW, +VCC_MPHYGT, +VCC_AMPHYPLL, +1VALW_PLL, +VCC_DSW3P3, +VCC_HDA, +3V_SPI0, +3VALW_PRIM

SKYLAKE-U_BGA1356
REV = 1
@

15 OF 20 ? ?

AK15, AG15, Y16, Y15, T16, AF16, AD15	VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPF, VCCPGPPG	85mA
V19	VCCPRIM_3P3_V19	161mA
T1	VCCPRIM_1P0_T1	135mA
AA1	VCCATS_1P8	
AK17	VCCRTCPRIM_3P3	
AK19, BB14	VCCRTC_AK19, VCCRTC_BB14	
BB10	DCPRTC	
A14	VCCCLK1	
K19	VCCCLK2	
L21	VCCCLK3	
N20	VCCCLK4	
L19	VCCCLK5	
A10	VCCCLK6	
AN11, AN13	GPP_B0/CORE_VID0, GPP_B1/CORE_VID1	T1, T2

+1VALW_PCH, +3VALW_PCH, +1.8VALW_PCH, +3VALW_PRIM, +1VALW_PCH, +1.8VALW_PCH, +3VALW_RTCPRIM, +RTCVCC

Primary Well 3.3 V

+3VALW_PCH — RC147 1 — 2 0_0402_5% — +3VALW_PRIM

[SKL PDG]VCCPRIM
[SKL PDG]1uF x1
[SKL PDG]Close V19,
Placement type:Edge<3mm(118mil)

+3VALW_PRIM — CC145 1U_0402_10V6K

HD Audio Power 3.3 V, 1.8 V, 1.5 V. For Intel High Definition Audio.

+3VALW_PCH — RC148 1 — 2 0_0402_5% — +VCC_HDA

[SKL PDG]VccHDA
[SKL PDG]1uF x1
[SKL PDG]Close AJ19,
Placement type:Edge<10mm(394mil)

+VCC_HDA — CC147 1U_0402_10V6K

Thermal Sensor Primary Well 1.8 V

[SKL PDG]VccATS
[SKL PDG]1uF x1
[SKL PDG]Close AA1,
Placement type:Edge<10mm(394mil)

+1.8VALW_PCH — CC144 1U_0402_10V6K

Deep Sx Well 1.0 V: This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.

[SKL PDG]DcpDSW
[SKL PDG]1uF x1
[SKL PDG]Close AL1,
Placement type:Edge<3mm(118mil)

+DCPDSW — CC148 1U_0402_10V6K

RTC de-coupling capacitor only. This rail should NOT be driven.

[SKL PDG]DcpRTC
[SKL PDG]0.1uF x1
[SKL PDG]Close BB10,
Placement type:Edge<3mm(118mil)

+DCPRTC — CC146 0.1U_0402_10V6-K

+VCC_AMPHYPLL — @CC149 1U_0402_10V6K

Core Logic Primary Well: This rail scales from 0.85 V to 1.0 V.

+1VALW — RC151 1 — 2 0_0805_5% — +PCH_CORE

[SKL PDG]VccPRIM_Core
[SKL PDG]1uF x1
[SKL PDG]Close AF18,
Placement type:Edge<10mm(394mil)

+PCH_CORE — CC150 1U_0402_10V6K

Deep Sx Well for GPD GPIOs and USB2

+3VALW_PCH — RC152 1 — 2 0_0402_5% — +VCC_DSW3P3

[SKL PDG]VccDSW

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+3VALW_PCH — RC150 1 — 2 0_0402_5% — +3VALW_RTCPRIM

[SKL PDG]VccRTCPRIM
[SKL PDG]1uF x1,0.1uF x2
[SKL PDG]Close AK17,
Placement type:Edge<3mm(118mil)

+3VALW_RTCPRIM — CC151 1U_0402_10V6K — CC152 0.1U_0402_10V6K — CC153 0.1U_0402_10V6K

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

[SKL PDG]VccRTC
[SKL PDG]1uF x1
[SKL PDG]Close AK19,
Placement type:Edge<3mm(118mil)

+RTCVCC — CC154 1U_0402_10V6K

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Title: **KBL(13/16):POWER**

Size: A2 | Document Number: **SKYWALKER** | Rev: 1.0

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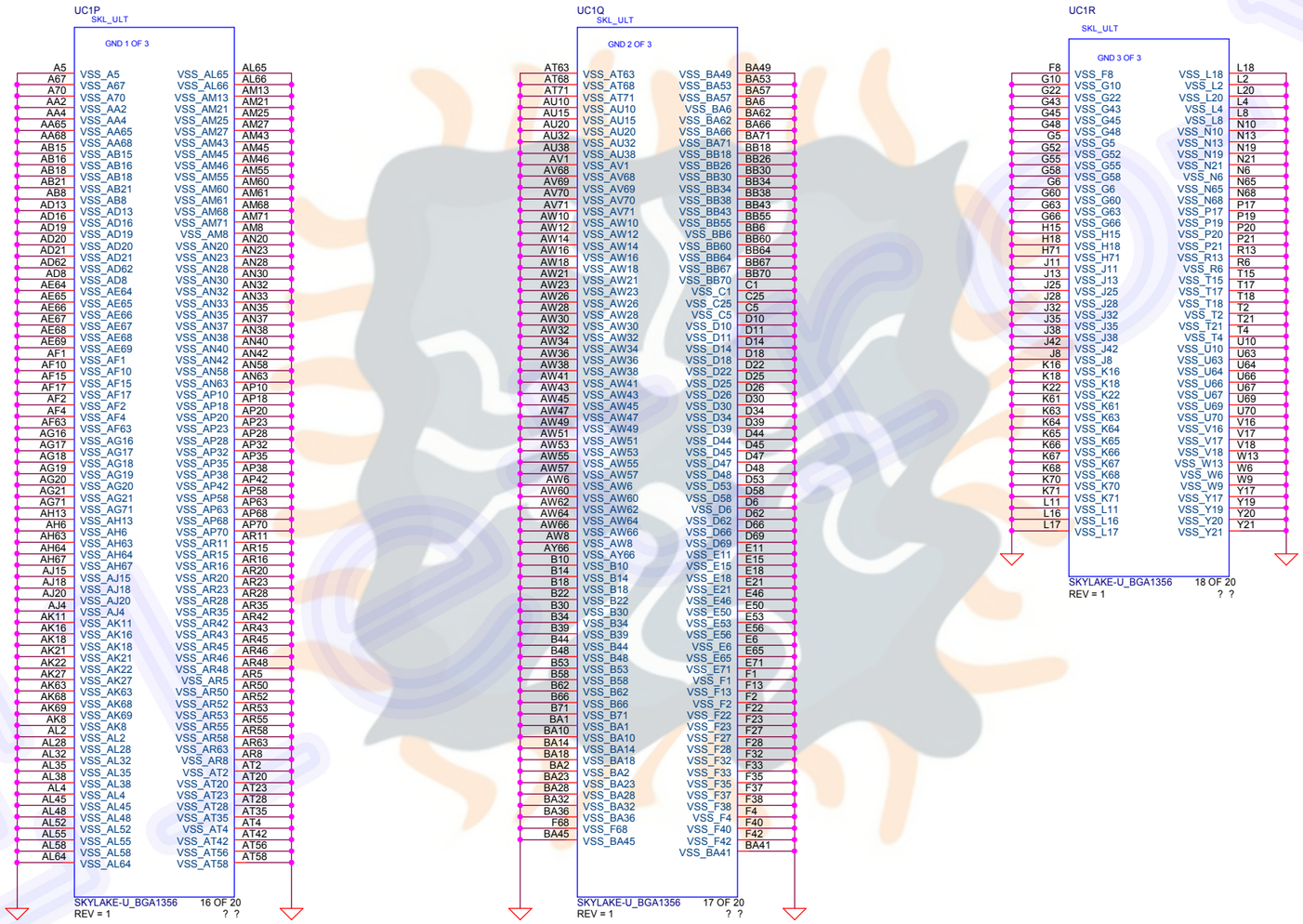

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(14/16):GND

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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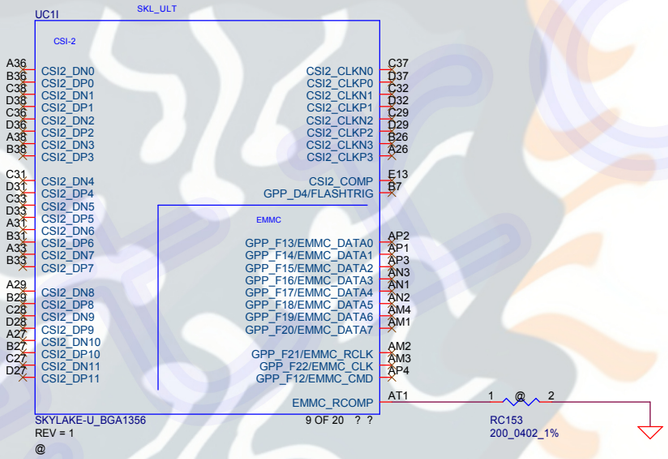

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Title: KBL(15/16):CSI-2/EMMC

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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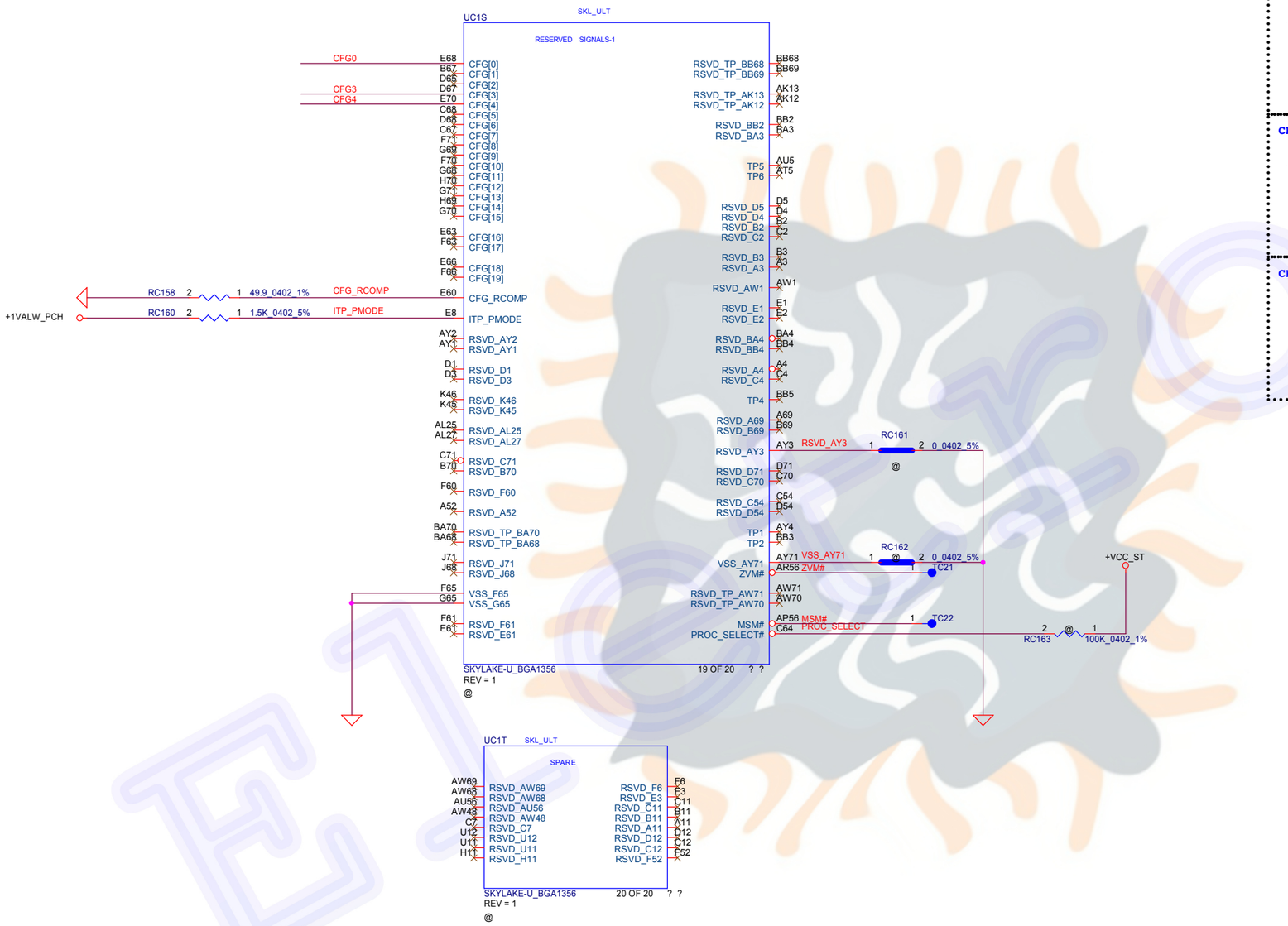

[SKL EDS]

CFG0

+VCC_IO

CFG0 — RC154 2 @ 1 1K_0402_5%

RC155 2 @ 1 1K_0402_1%

L:Stall.
*H:(Default) Normal Operation; No stall.

CFG4

+VCC_IO

CFG4 — RC156 2 @ 1 1K_0402_5%

RC157 2 1 1K_0402_1%

*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

CFG3

CFG3 — RC159 1 @ 2 1K_0402_5%

CFG3 require >= 0.5"
CPU Debug Consent Strap

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

Title	KBL(16/16):CFG/RESERVED
Size	Custom
Document Number	SKYWALKER
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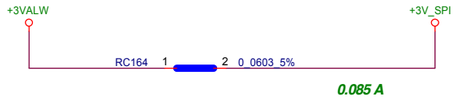
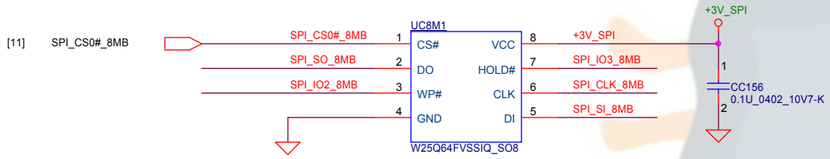
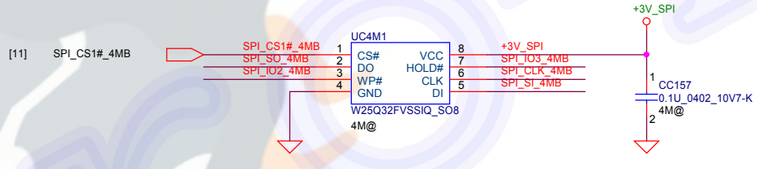


8MB(64Mb)

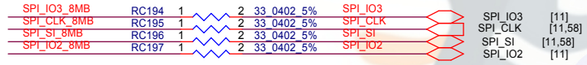
[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM



4MB(32Mb) Reserve



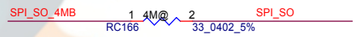
Place RC194,195,196,197 close together



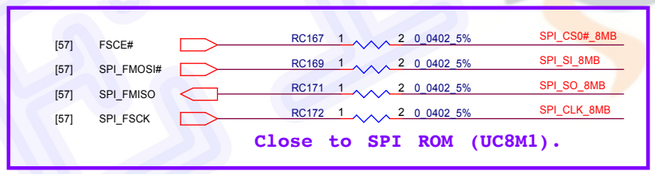
Place RC203,204,205,206 close together

Near SPI ROM

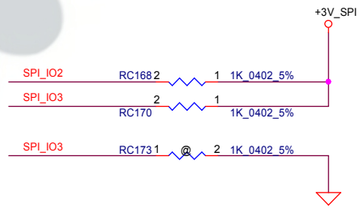
Near SPI ROM



Mirror Code



Close to SPI ROM (UC8M1).



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Title: **SPI ROM**

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V

CD1 10U_0603_6.3V6-M
CD2 10U_0603_6.3V6-M
CD3 10U_0603_6.3V6-M
CD4 10U_0603_6.3V6-M
CD5 10U_0603_6.3V6-M
CD6 10U_0603_6.3V6-M
CD7 10U_0603_6.3V6-M
CD8 10U_0603_6.3V6-M

+1.2V

CD14 1U_0402_6.3V6-K
CD15 1U_0402_6.3V6-K
CD16 1U_0402_6.3V6-K
CD17 1U_0402_6.3V6-K
CD18 1U_0402_6.3V6-K
CD19 1U_0402_6.3V6-K
CD20 1U_0402_6.3V6-K
CD21 1U_0402_6.3V6-K
CD26 @ 330U_D2_2VM_R9M

Place decoupling cap on DRAM side.

[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+2.5V

CD9 10U_0603_6.3V6-M
CD10 10U_0603_6.3V6-M
CD11 1U_0402_6.3V6-K
CD12 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM

[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+0.6VS

CD22 10U_0603_6.3V6-M
CD23 10U_0603_6.3V6-M
CD24 1U_0402_6.3V6-K
CD63 1U_0402_6.3V6-K
CD64 1U_0402_6.3V6-K
CD65 1U_0402_6.3V6-K

DDR_A_D[0..63] [7]
DDR_A_MA[0..16] [7]
DDR_A_DQS#[0..7] [7]
DDR_A_DQS[0..7] [7]

JDIMM1A ME@

+1.2V

DDR_A_D5 DDR_A_D1 DDR_A_DQS#0 DDR_A_DQS0 DDR_A_D2 DDR_A_D7 DDR_A_D9 DDR_A_D12 DDR_A_D10 DDR_A_D15 DDR_A_D16 DDR_A_D20 DDR_A_DQS#2 DDR_A_DQS2 DDR_A_D23 DDR_A_D18 DDR_A_D25 DDR_A_D24 DDR_A_D30 DDR_A_D26 DDR_A_DQS#8 DDR_A_DQS8

DDR_A_D0 DDR_A_D4 DDR_A_D6 DDR_A_D3 DDR_A_D8 DDR_A_D13 DDR_A_DQS#1 DDR_A_DQS1 DDR_A_D11 DDR_A_D14 DDR_A_D17 DDR_A_D21 DDR_A_D22 DDR_A_D19 DDR_A_D29 DDR_A_D28 DDR_A_DQS#3 DDR_A_DQS3 DDR_A_D31 DDR_A_D27

[7] DDR_A_CKE0 DDR_A_CKE0
[7] DDR_A_BG1 DDR_A_BG1
[7] DDR_A_BG0 DDR_A_BG0
DDR_A_MA12 DDR_A_MA9 DDR_A_MA8 DDR_A_MA6

DDR4_DRAMRST# [8,23]
DDR_A_CKE1 [7]
DDR_A_ACT_N DDR_A_ALERT_N
DDR_A_ACT_N [7]
DDR_A_ALERT_N [7]
DDR_A_MA11 DDR_A_MA7 DDR_A_MA5 DDR_A_MA4

FOX_AS0A826-H4RB-7H

+3VS

RD6 10K_0402_5% @ SA0_CHA_P
RD7 10K_0402_5% @ SA1_CHA_P
RD8 10K_0402_5% @ SA2_CHA_P
RD9 0_0402_5%
RD10 0_0402_5%
RD11 0_0402_5%

SPD Address = 0H

JDIMM1B ME@

+2.5V +1.2V +0.6VS

DDR_A_MA3 DDR_A_MA1 DDR_A_DDRCLK0_1866M DDR_A_DDRCLK0_1866M# DDR_A_PARITY DDR_A_BA1 DDR_A_CS0# DDR_A_MA14 DDR_A_ODT0 DDR_A_CS1# DDR_A_ODT1 DDR_A_D37 DDR_A_D32 DDR_A_DQS#4 DDR_A_DQS4 DDR_A_D38 DDR_A_D39 DDR_A_D40 DDR_A_D44 DDR_A_D43 DDR_A_D46 DDR_A_D49 DDR_A_D52 DDR_A_DQS#6 DDR_A_DQS6 DDR_A_D50 DDR_A_D55 DDR_A_D56 DDR_A_D60 DDR_A_D59 DDR_A_D58 CP_SMB_CLK VDDSPD_1

[7] DDR_A_DDRCLK0_1866M
[7] DDR_A_DDRCLK0_1866M#
[7] DDR_A_PARITY
[7] DDR_A_BA1
[7] DDR_A_CS0#
[7] DDR_A_ODT0
[7] DDR_A_CS1#
[7] DDR_A_ODT1

DDR_A_MA2 EVENT_n_1 DDR_A_MA0 DDR_A_MA10 DDR_A_BA0 DDR_A_MA16 DDR_A_MA15 DDR_A_MA13 M_VREF_CA_DIMMA SA2_CHA_P DDR_A_D33 DDR_A_D36 DDR_A_D35 DDR_A_D34 DDR_A_D41 DDR_A_D45 DDR_A_DQS#5 DDR_A_DQS5 DDR_A_D42 DDR_A_D47 DDR_A_D48 DDR_A_D53 DDR_A_D54 DDR_A_D51 DDR_A_D57 DDR_A_D61 DDR_A_DQS#7 DDR_A_DQS7 DDR_A_D63 DDR_A_D62 CP_SMB_DAT SA0_CHA_P SA1_CHA_P

DDR_A_DDRCLK1_1866M [7]
DDR_A_DDRCLK1_1866M# [7]
DDR_A_BA0 [7]

RD5 240_0402_1%

+3VS

RD12 0_0402_5%

[11,23,63] CP_SMB_CLK
CP_SMB_DAT [11,23,63]

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.

CD29 0.1U_0402_10V7-K
CD30 2.2U_0402_6.3V6-M

Place decoupling cap close to DIMM

FOX_AS0A826-H4RB-7H

+1.2V

2.2U_0402_6.3V6-M CD27 @
0.1U_0402_10V7-K CD28 @

RF

+1.2V

RD1 1K_0402_1%
RD2 2_0402_1%
RD3 1K_0402_1%
RD4 24.9_0402_1%
CD13 0.022U_0402_25V7-K
CD25 0.1U_0402_16V7-K @

[7] DDR4_VREF_CA_CPU_A
M_VREF_CA_DIMMA

+1.2V

RD13 240_0402_1%
RD14 240_0402_1%

DDR_A_DQS#8
DDR_A_DQS8

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Title: DDR4 CH-A PRIMARY

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V

CD34 10U_0603_6.3V6-M
CD35 10U_0603_6.3V6-M
CD36 10U_0603_6.3V6-M
CD37 10U_0603_6.3V6-M
CD38 10U_0603_6.3V6-M
CD39 10U_0603_6.3V6-M
CD40 10U_0603_6.3V6-M
CD41 10U_0603_6.3V6-M

CD49 1U_0402_6.3V6-K
CD50 1U_0402_6.3V6-K
CD51 1U_0402_6.3V6-K
CD52 1U_0402_6.3V6-K
CD53 1U_0402_6.3V6-K
CD54 1U_0402_6.3V6-K
CD55 1U_0402_6.3V6-K
CD56 1U_0402_6.3V6-K
CD57 330U_D2_2VM_R9M

Place decoupling cap on DRAM side.

[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+0.6VS

CD32 10U_0603_6.3V6-M
CD33 10U_0603_6.3V6-M
CD42 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM

[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+2.5V

CD45 10U_0603_6.3V6-M
CD46 10U_0603_6.3V6-M
CD47 1U_0402_6.3V6-K
CD48 1U_0402_6.3V6-K
CD68 1U_0402_6.3V6-K
CD66 1U_0402_6.3V6-K
CD67 1U_0402_6.3V6-K

Layout Node:
Place Close DIMMs

DDR_B_D[0..63] [8]
DDR_B_MA[0..16] [8]
DDR_B_DQS#[0..7] [8]
DDR_B_DQS[0..7] [8]

JDIMM2A ME@

		1	VSS_1	VSS_2	2	
DDR_B_D13		3	DQ5	DQ4	4	DDR_B_D8
DDR_B_D12		5	VSS_3	VSS_4	6	DDR_B_D9
		7	DQ1	DQ0	8	
DDR_B_DQS#1		9	VSS_5	VSS_6	10	
DDR_B_DQS1		11	DQS0_C	DM0_n/DBIO_n	12	
DDR_B_D10		13	DQS0_t	VSS_7	14	DDR_B_D15
		15	VSS_8	DQ6	16	
DDR_B_D14		17	DQ7	VSS_9	18	DDR_B_D11
DDR_B_D4		19	VSS_10	DQ2	20	
		21	DQ3	VSS_11	22	DDR_B_D1
DDR_B_D0		23	VSS_12	DQ12	24	
		25	DQ13	VSS_13	26	DDR_B_D5
		27	VSS_14	DQ8	28	
		29	DQ9	VSS_15	30	DDR_B_DQS#0
		31	VSS_16	DQS1_c	32	DDR_B_DQS0
DDR_B_D6		33	DM1_n/DBI1_n	DQS1_t	34	
		35	VSS_17	VSS_18	36	DDR_B_D3
DDR_B_D2		37	DQ15	DQ14	38	
		39	VSS_19	VSS_20	40	DDR_B_D7
DDR_B_D21		41	DQ10	DQ11	42	
		43	VSS_21	VSS_22	44	DDR_B_D20
DDR_B_D16		45	DQ21	DQ20	46	
		47	VSS_23	VSS_24	48	DDR_B_D17
DDR_B_DQS#2		49	DQ17	DQ16	50	
DDR_B_DQS2		51	VSS_25	VSS_26	52	
		53	DQS2_c	DM2_n/DBI2_n	54	
DDR_B_D18		55	DQS2_t	VSS_27	56	DDR_B_D23
		57	VSS_28	DQ22	58	
DDR_B_D22		59	DQ23	VSS_29	60	DDR_B_D19
		61	VSS_30	DQ18	62	
DDR_B_D29		63	DQ19	VSS_31	64	DDR_B_D28
		65	VSS_32	DQ28	66	
DDR_B_D25		67	DQ29	VSS_33	68	DDR_B_D24
		69	VSS_34	DQ24	70	
		71	DQ25	VSS_35	72	DDR_B_DQS#3
		73	VSS_36	DQS3_c	74	DDR_B_DQS3
		75	DM3_n/DBI3_n	DQS3_t	76	
DDR_B_D30		77	VSS_37	VSS_38	78	DDR_B_D31
		79	DQ30	DQ31	80	
DDR_B_D26		81	VSS_39	VSS_40	82	DDR_B_D27
		83	DQ26	DQ27	84	
		85	VSS_41	VSS_42	86	
		87	CB5/NC	CB4/NC	88	
		89	VSS_43	VSS_44	90	
		91	CB1/NC	CB0/NC	92	
DDR_B_DQS#8		93	VSS_45	VSS_46	94	
DDR_B_DQS8		95	DQS8_c	DBI8_n	96	
		97	DQS8_t	VSS_47	98	
		99	VSS_48	CB6/NC	100	
		101	CB2/NC	VSS_49	102	
		103	VSS_50	CB7/NC	104	
		105	CB3/NC	VSS_51	106	
		107	VSS_52	RESET_n	108	DDR4_DRAMRST# [8,22]
		109	CKE0	CKE1	110	DDR_B_CKE1 [8]
DDR_B_CKE0	[8]	111	VDD_1	VDD_2	112	
DDR_B_BG1	[8]	113	BG1	ACT_n	114	DDR_B_ACT_N [8]
DDR_B_BG0	[8]	115	BG0	ALERT_n	116	DDR_B_ALERT_N [8]
		117	VDD_3	VDD_4	118	
DDR_B_MA12		119	A12	A11	120	DDR_B_MA11
DDR_B_MA9		121	A9	A7	122	DDR_B_MA7
		123	VDD_5	VDD_6	124	
DDR_B_MA8		125	A8	A5	126	DDR_B_MA5
DDR_B_MA6		127	A6	A4	128	DDR_B_MA4
		129	VDD_7	VDD_8	130	

FOX_AS0A826-H4SB-7H
SP071407011

SPD Address = 2H

RD20 10K_0402_5% @ SA0_CHB_P
RD21 10K_0402_5% @ SA1_CHB_P
RD22 10K_0402_5% @ SA2_CHB_P
RD23 0_0402_5%
RD24 0_0402_5% @
RD25 0_0402_5%

RD26 0_0402_5% @ [11,22,63] CP_SMB_CLK

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.

CD60 0.1U_0402_10V7-K
CD61 2.2U_0402_6.3V6-M

Place decoupling cap close to DIMM

JDIMM2B ME@

		131	A3	A2	132	DDR_B_MA2
DDR_B_MA3		133	A1	EVENT_n	134	EVENT_n_Z
		135	VDD_9	VDD_10	136	
DDR_B_DDRCLK0_1866M	[8] DDR_B_DDRCLK0_1866M	137	CK0_t	CK1_t	138	DDR_B_DDRCLK1_1866M
DDR_B_DDRCLK0_1866M#	[8] DDR_B_DDRCLK0_1866M#	139	CK0_c	CK1_c	140	DDR_B_DDRCLK1_1866M#
		141	VDD_11	VDD_12	142	
DDR_B_PARITY	[8] DDR_B_PARITY	143	Parity	A0	144	DDR_B_MA0
		145		A10/AP	146	DDR_B_MA10
DDR_B_BA1	[8] DDR_B_BA1	147	BA1	VDD_14	148	DDR_B_BA0
DDR_B_CS0#	[8] DDR_B_CS0#	149	VDD_13	BA0	150	DDR_B_MA16
DDR_B_MA14		151	CS0_n	RAS_n/A16	152	
		153	WE_n/A14	VDD_16	154	DDR_B_MA15
DDR_B_ODT0	[8] DDR_B_ODT0	155	VDD_15	CAS_n/A15	156	DDR_B_MA13
DDR_B_CS1#	[8] DDR_B_CS1#	157	ODT0	A13	158	
		159	CS1_n	VDD_18	160	
DDR_B_ODT1	[8] DDR_B_ODT1	161	VDD_17	C0/CS2_n/NC	162	M_VREF_CA_DIMMB
		163	ODT1	VREFCA	164	SA2_CHB_P
		165	VDD_19	RFU	166	
		167	C1/CS3_n/NC	VSS_54	168	
DDR_B_D37		169	VSS_53	DQ36	170	DDR_B_D36
DDR_B_D33		171	DQ37	VSS_56	172	DDR_B_D32
		173	VSS_55	DQ32	174	
DDR_B_DQS#4		175	DQ33	VSS_58	176	
DDR_B_DQS4		177	VSS_57	DM4_n/DBI4_n	178	
		179	DQS4_c	VSS_59	180	
DDR_B_D34		181	DQS4_t	DQ39	182	DDR_B_D35
		183	VSS_60	VSS_61	184	
DDR_B_D38		185	DQ38	DQ35	186	DDR_B_D39
		187	VSS_62	VSS_63	188	
DDR_B_D41		189	DQ34	DQ45	190	DDR_B_D45
		191	DQ44	VSS_65	192	
DDR_B_D40		193	VSS_64	DQ41	194	DDR_B_D44
		195	VSS_66	VSS_67	196	
		197	DQ40	DQS5_c	198	DDR_B_DQS#5
		199	VSS_68	DQS5_t	200	DDR_B_DQS5
		201	DM5_n/DBI5_n	VSS_70	202	
DDR_B_D43		203	VSS_69	DQ47	204	DDR_B_D42
		205	DQ46	VSS_72	206	
DDR_B_D47		207	VSS_71	DQ43	208	DDR_B_D46
		209	DQ42	VSS_74	210	
DDR_B_D53		211	VSS_73	DQ53	212	DDR_B_D52
		213	DQ52	VSS_76	214	
DDR_B_D48		215	VSS_75	DQ49	216	DDR_B_D49
		217	DQ48	VSS_78	218	
DDR_B_DQS#6		219	VSS_77	DM6_n/DBI6_n	220	
DDR_B_DQS6		221	DQS6_c	VSS_79	222	
		223	DQS6_t	DQ54	224	DDR_B_D51
DDR_B_D50		225	VSS_80	VSS_81	226	
		227	DQ55	DQ50	228	DDR_B_D54
DDR_B_D55		229	VSS_82	VSS_83	230	
		231	DQ51	DQ60	232	DDR_B_D56
DDR_B_D60		233	VSS_84	DQ61	234	
		235	DQ61	VSS_85	236	DDR_B_D57
DDR_B_D61		237	VSS_86	DQS7_c	238	
		239	DQ56	VSS_87	240	DDR_B_DQS#7
		241	VSS_88	DQS7_t	242	DDR_B_DQS7
		243	DM7_n/DBI7_n	VSS_90	244	
DDR_B_D59		245	VSS_89	DQ63	246	DDR_B_D62
		247	DQ62	VSS_92	248	
DDR_B_D58		249	VSS_91	DQ59	250	DDR_B_D63
		251	DQ58	VSS_94	252	
CP_SMB_CLK		253	VSS_93	SDA	254	CP_SMB_DAT [11,22,63]
VDDSPD_2		255	SCL	SA0	256	SA0_CHB_P
		257	VDDSPD	SA2	258	
		259	VPP_1	Vtt	260	SA1_CHB_P
		261	VPP_2	SA1	262	
			GND_1	GND_2		

FOX_AS0A826-H4SB-7H
SP071407011

RD19 240_0402_1%

CD58 2.2U_0402_6.3V6-M @
CD59 0.1U_0402_10V7-K @

[7] DDR4_VREF_DQ_CPU_B
RD16 2_0402_1% M_VREF_CA_DIMMB
RD15 1K_0402_1%
RD17 1K_0402_1%
RD18 24.9_0402_1%
CD43 0.022U_0402_25V7-K
CD44 0.1U_0402_16V7-K

RD27 240_0402_1%
RD28 240_0402_1% DDR_B_DQS#8 DDR_B_DQS8

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Title: **DDR4 CH-B PRIMARY**
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[15] PCIE_CTX_C_GRX_N[1..4]
[15] PCIE_CTX_C_GRX_P[1..4]
PCIE_CTX_C_GRX_N[1..4]
PCIE_CTX_C_GRX_P[1..4]
[15] PCIE_CRX_GTX_N[1..4]
[15] PCIE_CRX_GTX_P[1..4]
PCIE_CRX_GTX_N[1..4]
PCIE_CRX_GTX_P[1..4]

+3VS_AON
RV1 @ 10K_0402_5%
UV1A
1/18 PCI_EXPRESS
GM107/GM108 GK107/GK208 GF117
PEX_WAKE_N AJ11 — NC
[28] VGA_PEX_RST# — VGA_PEX_RST# — RV11 DIS@ 0_0402_5% — PEX_RST_N AJ12
CLKREQ_VGA# — PEX_CLKREQ_N AK12
[10] CLK_PCIE_VGA — CLK_PCIE_VGA — PEX_REFCLK AL13
[10] CLK_PCIE_VGA# — CLK_PCIE_VGA# — PEX_REFCLK_N AK13
PCIE_CRX_GTX_P1 — CV8 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P1 — PEX_TX0 AK14
PCIE_CRX_GTX_N1 — CV9 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N1 — PEX_TX0_N AJ14
PCIE_CTX_C_GRX_P1 — PEX_RX0 AN12
PCIE_CTX_C_GRX_N1 — PEX_RX0_N AM12
PCIE_CRX_GTX_P2 — CV10 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P2 — PEX_TX1 AH14
PCIE_CRX_GTX_N2 — CV11 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N2 — PEX_TX1_N AG14
PCIE_CTX_C_GRX_P2 — PEX_RX1 AN14
PCIE_CTX_C_GRX_N2 — PEX_RX1_N AM14
PCIE_CRX_GTX_P3 — CV12 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P3 — PEX_TX2 AK15
PCIE_CRX_GTX_N3 — CV13 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N3 — PEX_TX2_N AJ15
PCIE_CTX_C_GRX_P3 — PEX_RX2 AP14
PCIE_CTX_C_GRX_N3 — PEX_RX2_N AP15
PCIE_CRX_GTX_P4 — CV21 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P4 — PEX_TX3 AL16
PCIE_CRX_GTX_N4 — CV22 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N4 — PEX_TX3_N AK16
PCIE_CTX_C_GRX_P4 — PEX_RX3 AN15
PCIE_CTX_C_GRX_N4 — PEX_RX3_N AM15

PEX_TX4 AK17 / PEX_TX4_N AJ17
PEX_RX4 AN17 / PEX_RX4_N AM17
PEX_TX5 AH17 / PEX_TX5_N AG17
PEX_RX5 AP17 / PEX_RX5_N AP18
PEX_TX6 AK18 / PEX_TX6_N AJ18
PEX_RX6 AN18 / PEX_RX6_N AM18
PEX_TX7 AL19 / PEX_TX7_N AK19
PEX_RX7 AN20 / PEX_RX7_N AM20
PEX_TX8 AK20 / PEX_TX8_N AJ20
PEX_RX8 AP20 / PEX_RX8_N AP21
PEX_TX9 AH20 / PEX_TX9_N AG20
PEX_RX9 AN21 / PEX_RX9_N AM21
PEX_TX10 AK21 / PEX_TX10_N AJ21
PEX_RX10 AN23 / PEX_RX10_N AM23
PEX_TX11 AL22 / PEX_TX11_N AK22
PEX_RX11 AP23 / PEX_RX11_N AP22
PEX_TX12 AK23 / PEX_TX12_N AJ23
PEX_RX12 AN24 / PEX_RX12_N AM24
PEX_TX13 AH23 / PEX_TX13_N AG23
PEX_RX13 AN26 / PEX_RX13_N AM26
PEX_TX14 AK24 / PEX_TX14_N AJ24
PEX_RX14 AP26 / PEX_RX14_N AP27
PEX_TX15 AL25 / PEX_TX15_N AK25
PEX_RX15 AN27 / PEX_RX15_N AM27
PEX LANES 4 TO 15 NC FOR GM108
PEX LANES 8 TO 15 NC FOR GK208/GF117
N16P-GX_BGA908

PEX_IOVDD_1 AG19
PEX_IOVDD_2 AG21
PEX_IOVDD_3 AG22
PEX_IOVDD_4 AG24
PEX_IOVDD_5 AH21
PEX_IOVDD_6 AH25
+1.05VS_VGA
Under GPU: 1UF_0402_6.3V6-K CV54 DIS@; 1UF_0402_6.3V6-K CV55 DIS@
Near GPU: 4.7U_0603_6.3V6AK CV3 DIS@
Midway between GPU and power supply: 10U_0603_6.3V6M CV4 DIS@; 10U_0603_6.3V6M CV67 DIS@; 22U_0603_6.3V6-M CV64 DIS@; 22U_0603_6.3V6-M CV7 DIS@

PEX_IOVDDQ_01 AG13
PEX_IOVDDQ_02 AG15
PEX_IOVDDQ_03 AG16
PEX_IOVDDQ_04 AG18
PEX_IOVDDQ_05 AG25
PEX_IOVDDQ_06 AH15
PEX_IOVDDQ_07 AH18
PEX_IOVDDQ_08 AH26
PEX_IOVDDQ_09 AH27
PEX_IOVDDQ_10 AJ27
PEX_IOVDDQ_11 AK27
PEX_IOVDDQ_12 AL27
PEX_IOVDDQ_13 AM28
PEX_IOVDDQ_14 AN28
Under GPU: 1UF_0402_6.3V6-K CV56 DIS@; 1UF_0402_6.3V6-K CV57 DIS@
Near GPU: 4.7U_0603_6.3V6AK CV16 DIS@
Midway between GPU and power supply: 10U_0603_6.3V6M CV17 DIS@; 10U_0603_6.3V6M CV61 DIS@; 22U_0603_6.3V6-M CV58 DIS@; 22U_0603_6.3V6-M CV20 DIS@

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
+3VS_AON
0.1U_0402_10V7-K CV23 DIS@; 4.7U_0402_6.3V6M CV24 DIS@; 4.7U_0402_6.3V6M CV25 DIS@

+VGA_CORE
RV2 100_0402_1% DIS@
VDD_SENSE L4 — GFXCORE_VDD_SENSE_D [75]
GND_SENSE L5 — GFXCORE_GND_SENSE_D [75]
RV3 100_0402_1% DIS@
3V3AUX_NC P8

+3VS_AON
[80] dgpu_pwrgd — dgpu_pwrgd
[79] VDDQPWRGD — VDDQPWRGD
DV1 BAT54AW_SOT323-3 DIS@
RV13 10K_0402_5% DIS@
All_GPU_PWRGD — All_GPU_PWRGD [11]
+3VS
RV9212 DIS@ 10K_0402_5% dgpu_pwrgd
RV9222 DIS@ 10K_0402_5% VDDQPWRGD

PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT_N AK26
RV6 @1 2 200_0402_1%
+1.05VS_VGA
RV7 DIS@ 0_0402_5%
PEX_PLLVDD AG26
Under GPU: CV26 DIS@ 0.1U_0402_25V7K
Near GPU: CV27 DIS@ 1UF_0402_6.3V6-K; CV28 DIS@ 4.7U_0402_6.3V6M
TESTMODE AK11
PEX_TERMP AP29
RV10 DIS@ 2.49K_0402_1%
RV8 DIS@ 10K_0402_5%

+3VS_AON
+3VS_AON
RV5 10K_0402_5% DIS@
QV1 2N7002KW_SOT323-3 DIS@
[10] CLKREQ_PCIE4_VGA#
CLKREQ_VGA#
RV9 10K_0402_5% @
RV14 0_0402_5% @

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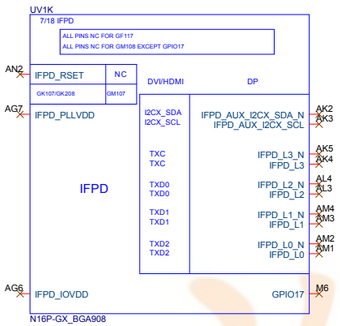
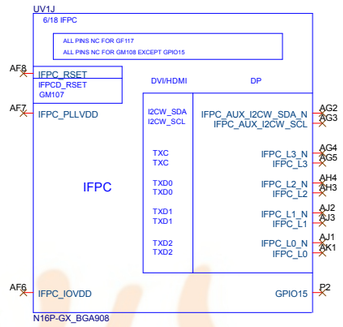
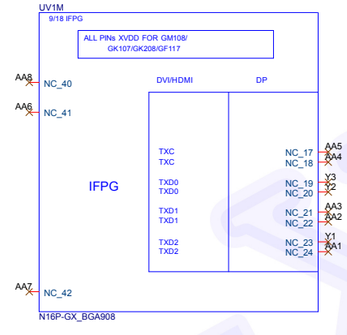
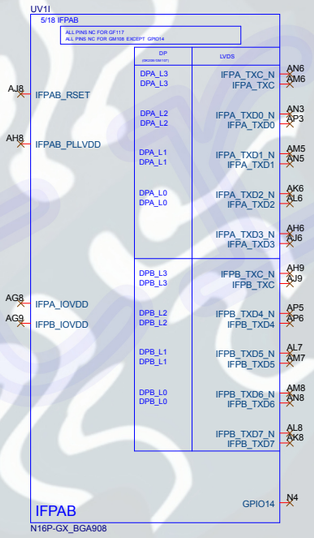
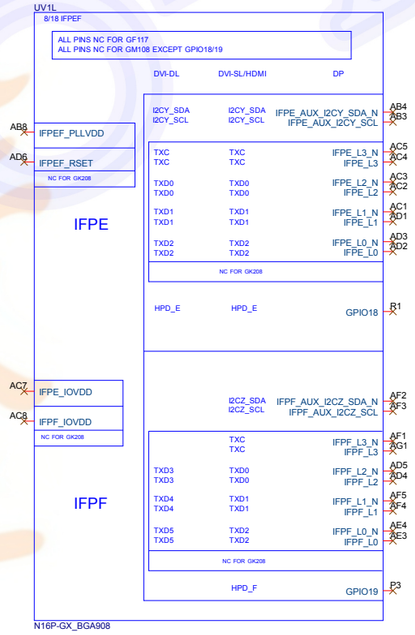
Title: N16P-Q1/Q3(1/6): PEG I/F
Size C | Document Number: SKYWALKER | Rev 2.0
Date: Thursday, August 25, 2016 | Sheet 25 of 82











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Title: **N16P-Q1/Q3(2/6): DIGITAL OU**

Size	Document Number	Rev
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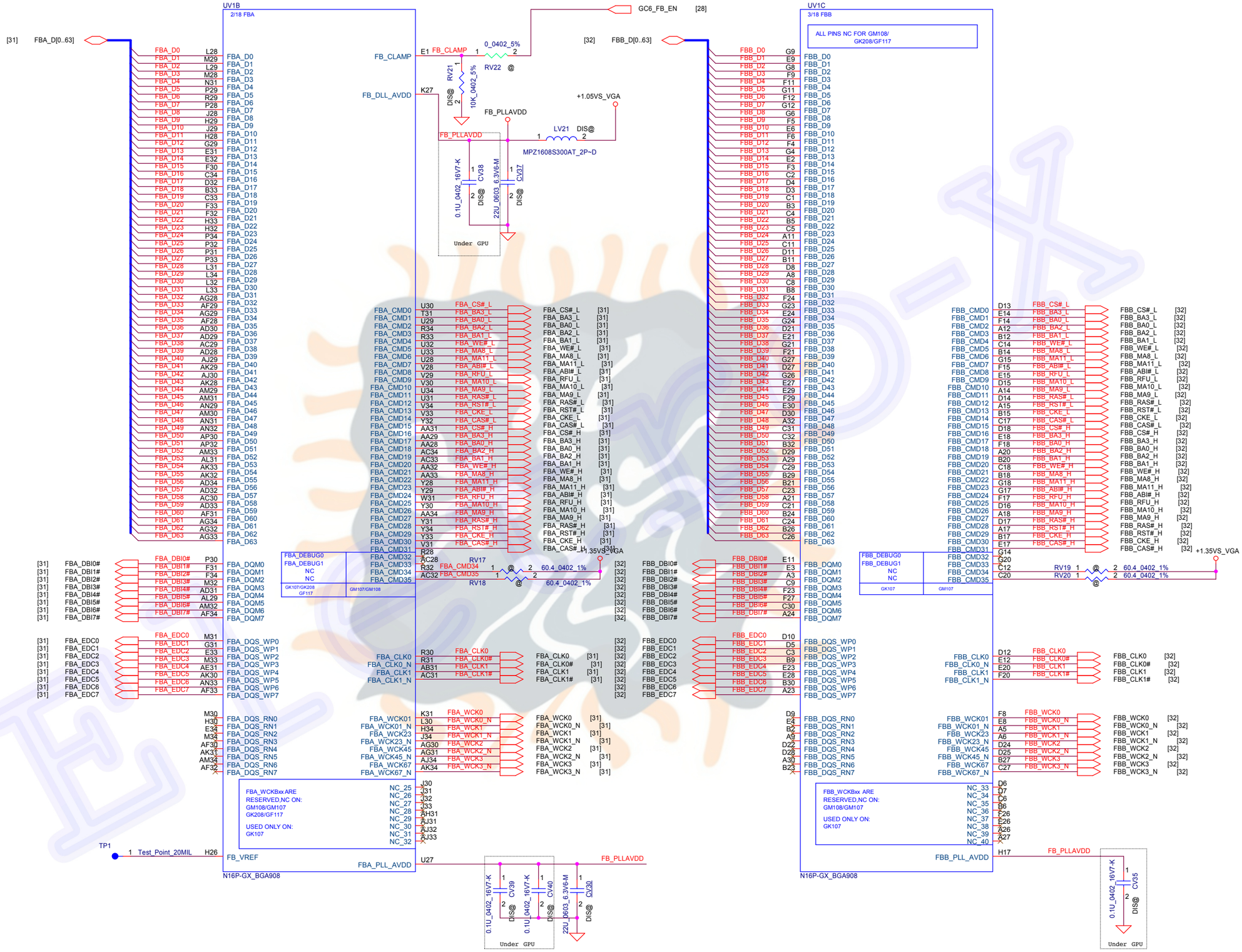

FBx_PLL_AVDD		
Capactior Type	GB4B-128/GDDR5 NV_DG	Actual
0.1uF_0402	3	3
22uF_0805	1	1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: 033_N16P-Q1/Q3(3/6): MEM[illegible]F

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30ohm@100MHz ESR=0.01

+1.05VS_VGA

LV1 DIS@ MPZ1608S300AT_2P~D NEAR BALL

CV107 22U_0603_6.3V6-M DIS@

CV108 0.1U_0402_25V7K DIS@

112mA

LV2 PBY160808T-301Y-N_2P DIS@

CV101 22U_0603_6.3V6-M DIS@

CV102 10U_0603_6.3V6-M DIS@

CV103 0.1U_0402_25V7K DIS@

CV104 0.1U_0402_25V7K DIS@ UNDER GPU

RV104 DIS@ 0_0402_5%

UV1P 12/18 XTAL_PLL

AD8 PLLVDD
AE8 SP_PLLVDD
AD7 VID_PLLVDD

NC
GM107 / GK107/GK208 — GM108 / GF117

VIDEO_CLK_XTAL_SS 50-ohm TRACE

H1 XTAL_SSIN
H3 XTAL_IN
J4 XTAL_OUTBUFF
H2 XTAL_OUT

N16P-GX_BGA908

XTAL_OUTBUFF_GPU

RV108 10K_0402_5% DIS@

RV125 10K_0402_5% @

RV109 10K_0402_5% DIS@

+3VS_AON

RV110 @ 1M_0402_5% 27MHZ_OUT

RV970 0_0201_5% DIS@

Crystal YV1 27MHZ_7PF_8Y27000005 DIS@ GND2 OUT IN GND1

27MHZ_IN GPU_XTAL_OUT_R

CV105 6.8P_0402_50V8-D DIS@

CV106 6.8P_0402_50V8-D DIS@

20160419
Add RV970 to reduce crystal driving level

+3VS_AON

RV129 RV111 RV112 RV113 RV114 10K_0402_1% @ DIS@

RV114 493K_0402_1%

Strap0 = H
GC6 enable

STRAP0 STRAP1 STRAP2 STRAP3 STRAP4

RV115 RV116 RV117 RV118 RV119 10K_0402_1% @

UV1Q 13/18 MISC2

ROM_CS_N H6
ROM_SI H5
ROM_SO H7
ROM_SCLK H4
BUFRST_N L2

STRAP0 J2
STRAP1 J7
STRAP2 J6
STRAP3 J5
STRAP4 J3

NC	NC	NC	NC	NC
GK107/GK208	GF117	GM107	GM108	

+3VS_AON

RV920 10K_0402_1% @

MULTI_STRAP_REF0_GND_GPU J1

MULTI_STRAP_REF0_GND

RV124 DIS@ 40.2K_0402_1%

N16P-GX_BGA908

+3VS_VGA

RV101 RV102 RV106 4.99K_0402_1% 10K_0402_5% @

RV105 RV103 RV107 4.99K_0402_1% X76@ DIS@

+3VS_VGA

RV127 @ 10K_0402_1%

[75] DGFX_PWRGD — DGFX_PWRGD — RV925 @ 0_0402_5%

[33,75,80] VGA_ON — VGA_ON — RV143 DIS@ 0_0402_5%

GC6_FB_EN — RV138 GC6@ 0_0402_5%

RV200 NGC6@ 0_0402_5%

DV101 GC6@ DAN222MGT2L_VMD3

FB_PWR_EN — FB_PWR_EN [79]

RV926 200K_0402_5% @

GC6_FB_EN_GPIO — GC6_FB_EN_GPIO [9]

Connect to EC or PCH to indicate the GC6 status of GPU to the system

+3VS_AON

CV109 @ 0.1U_0402_10V6-K

QV102 @ 2N7002KW_SOT323-3

GC6_FB_EN — GC6_FB_EN_D — RV141 DIS@ 0_0402_5% — GC6_FB_EN_GPIO

VGA_PEX_RST#

GPU Thermal shut down pin, sent to EC to control SLP_S3#

[57] WRST# — WRST#

QV22 @ 2N7002W-T/R7_SOT323-3

VGA_OVERT# — CV112 @ 0.01U_0402_25V7-K

20160303
Correct VGA_OVERT# netname and unstuff QV22

+3VS_AON

RV120 2.2K_0402_5% DIS@

RV121 2.2K_0402_5% DIS@

UV1R 11/18 MISC1

VGA_OVERT# — M1 OVERT (GM107/GM108/GK208: GK107/GF117 — GPIO8)

THERMDN K4
THERMDP K3

I2CS_SCL T4 — I2CS_SCL
I2CS_SDA T3 — I2CS_SDA
I2CC_SCL R2 — I2CC_SCL
I2CC_SDA R3 — I2CC_SDA
I2CB_SCL R7 — I2CB_SCL
I2CB_SDA R6 — I2CB_SDA

NC	NC	I2CB_SCL	I2CB_SDA
GF117		GM107/GM108 / GK107/GK208	

Test_Point_20MIL TP2 1 AM10 — JTAG_TCK
Test_Point_20MIL TP3 1 AP11 — JTAG_TMS
Test_Point_20MIL TP4 1 AM11 — JTAG_TDI
Test_Point_20MIL TP5 1 AP12 — JTAG_TDO
AN11 — JTAG_TRST_N

RV144 DIS@ 10K_0402_5%

GPIO0 P6 — GC6_FB_EN — GC6_FB_EN [27]
GPIO1 M3
GPIO2 D6
GPIO3 P5
GPIO4 P7
GPIO5 L7 — VGA_MPWR_ON — VGA_MPWR_ON [33]
GPIO6 M7 — VGA_EVENT#
GPIO7 N8 — SYS_PEX_RST_MON
GPIO8 L5 — VGA_ALERT#
GPIO9 M2 — MEM_VREF — MEM_VREF [31,32]
GPIO10 L1 — VGA_PWM_VID — VGA_PWM_VID [75]
GPIO11 M5 — VGA_PWR_LIM_D — VGA_PWR_LIM_D [67]
GPIO12 N3 — VGA_PSI — VGA_PSI [75]
GPIO13 M4
GPIO16 R8
GPIO20 P4
GPIO21 P3 — GPU_PEX_RST_HOLD

GPIO16	NC	GPIO16	GM107/GM108
GPIO20	NC	NC	
GPIO8	NC	NC	
GK208	GF117	GK107	

N16P-GX_BGA908

2N7002KDWH_SOT363-6

QV21B DIS@ — EC_SMB_CK3 — EC_SMB_CK3 [11,57,59,62]

QV21A DIS@ — EC_SMB_DA3 — EC_SMB_DA3 [11,57,59,62]

SMBUS to EC for Thermal

+3VS_AON

VGA_MPWR_ON — RV130 DIS@ 10K_0402_1%
SYS_PEX_RST_MON — RV123 @ 10K_0402_1%
VGA_OVERT# — RV122 DIS@ 10K_0402_1%
VGA_ALERT# — RV131 DIS@ 10K_0402_1%
VGA_PWR_LIM_D — RV132 DIS@ 100K_0402_5%
VGA_PSI — RV133 DIS@ 10K_0402_1%
GPU_PEX_RST_HOLD — RV134 DIS@ 10K_0402_1%
VGA_EVENT# — RV135 DIS@ 10K_0402_1%

GC6_FB_EN — RV146 DIS@ 10K_0402_1%
MEM_VREF — RV136 DIS@ 100K_0402_5%

+3VS_AON

UV101 GC6@ 74LVC1G08GW_SOT353-1-5

SYS_PEX_RST_MON — RV128 GC6@ 0_0402_5%

VGA_PEX_RST# — VGA_PEX_RST# [25]

RV140 1 NGC6@ 2 0_0402_5% SYS_PEX_RST_MON_R

+3VS_AON

UV102 DIS@ 74LVC1G08GW_SOT353-1-5

DGPU_HOLD_RST# — DGPU_HOLD_RST# [9]

PLT_RST# — PLT_RST# [12,42,48,49,56,57,58]

GPIO from PCH

+3VS_AON

CV110 DIS@ 0.1U_0402_10V6-K

QV101 DIS@ 2N7002KW_SOT323-3

VGA_EVENT# — RV145 @ 0_0402_5% — GPU_EVENT#_R — RV147 DIS@ 0_0402_5% — GPU_EVENT#

GPU_EVENT# [11]

PCH GPIO Pin to wake up GPU from GC6

+3VS_AON

RV926 200K_0402_5%

FB_PWR_EN [79]

VGA_PWR_LIM_D — DV102 — RB751V-40_SOD323-2 — VGA_PWR_LIM — VGA_PWR_LIM [57]

VGA_ALERT# — DV103 — RB751V-40_SOD323-2

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GT	Samsung	K4G41325FE-HC28	PD 45.3K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC4H24AJR-T2C 256X16	PD 34.8K							
	Micron	EDW4032BABG-60-F 256X16	PD 24.9K							

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR	Samsung	K4G80325FB-HC03	PD 4.99K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC8H24MJR-T2C	PD 30.1K							
	Micron	MT51J256M32HF-60:A	PD 10K							

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Title: 034_N16P-Q1/Q3(4/6): GPIO

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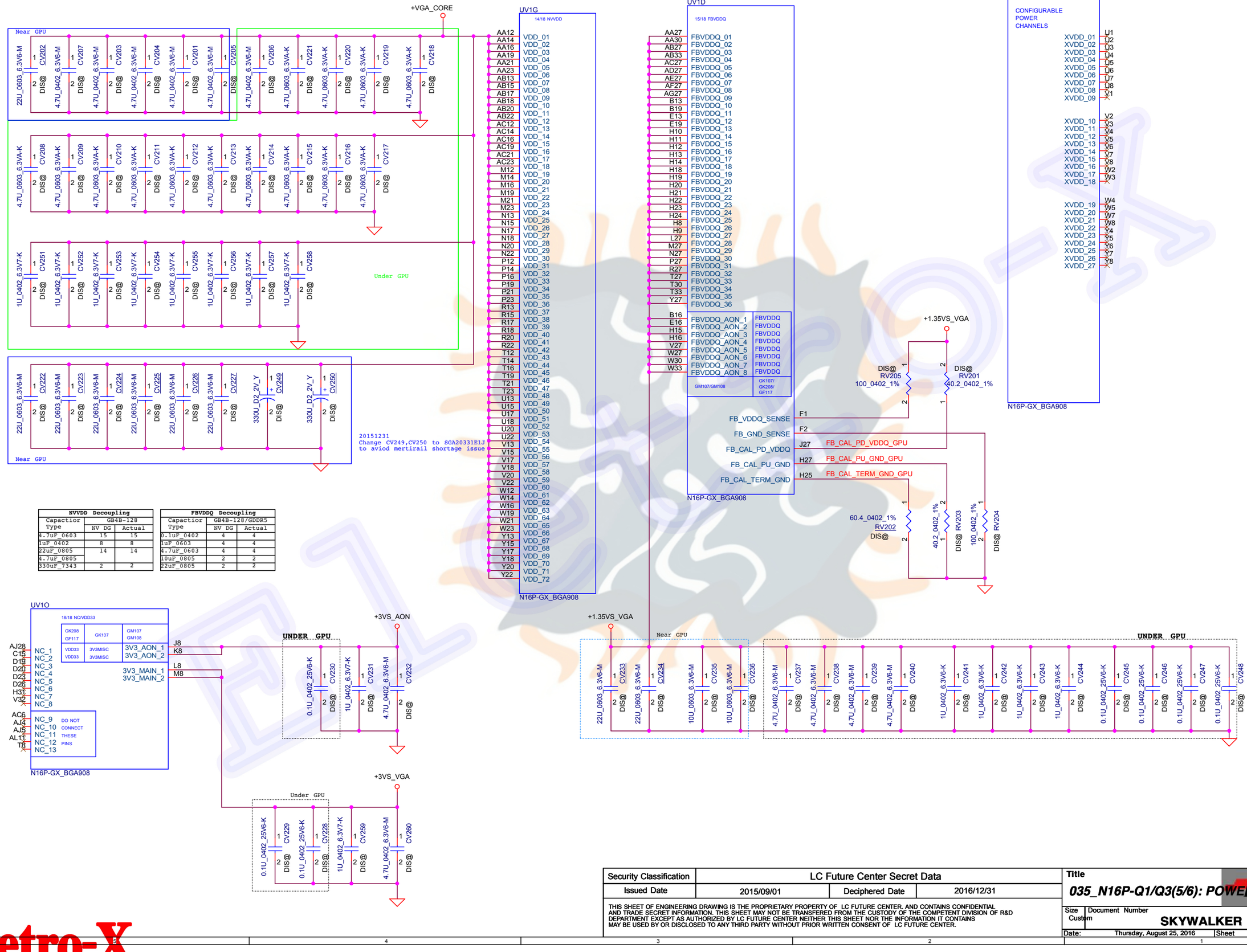

NVVDD Decoupling		
Capactior Type	GB4B-128	
	NV DG	Actual
4.7uF_0603	15	15
1uF_0402	8	8
22uF_0805	14	14
4.7uF_0805		
330uF_7343	2	2

FBVDDQ Decoupling		
Capactior Type	GB4B-128/GDDR5	
	NV DG	Actual
0.1uF_0402	4	4
1uF_0603	4	4
4.7uF_0603	4	4
10uF_0805	2	2
22uF_0805	2	2

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Title: 035_N16P-Q1/Q3(5/6): POWE

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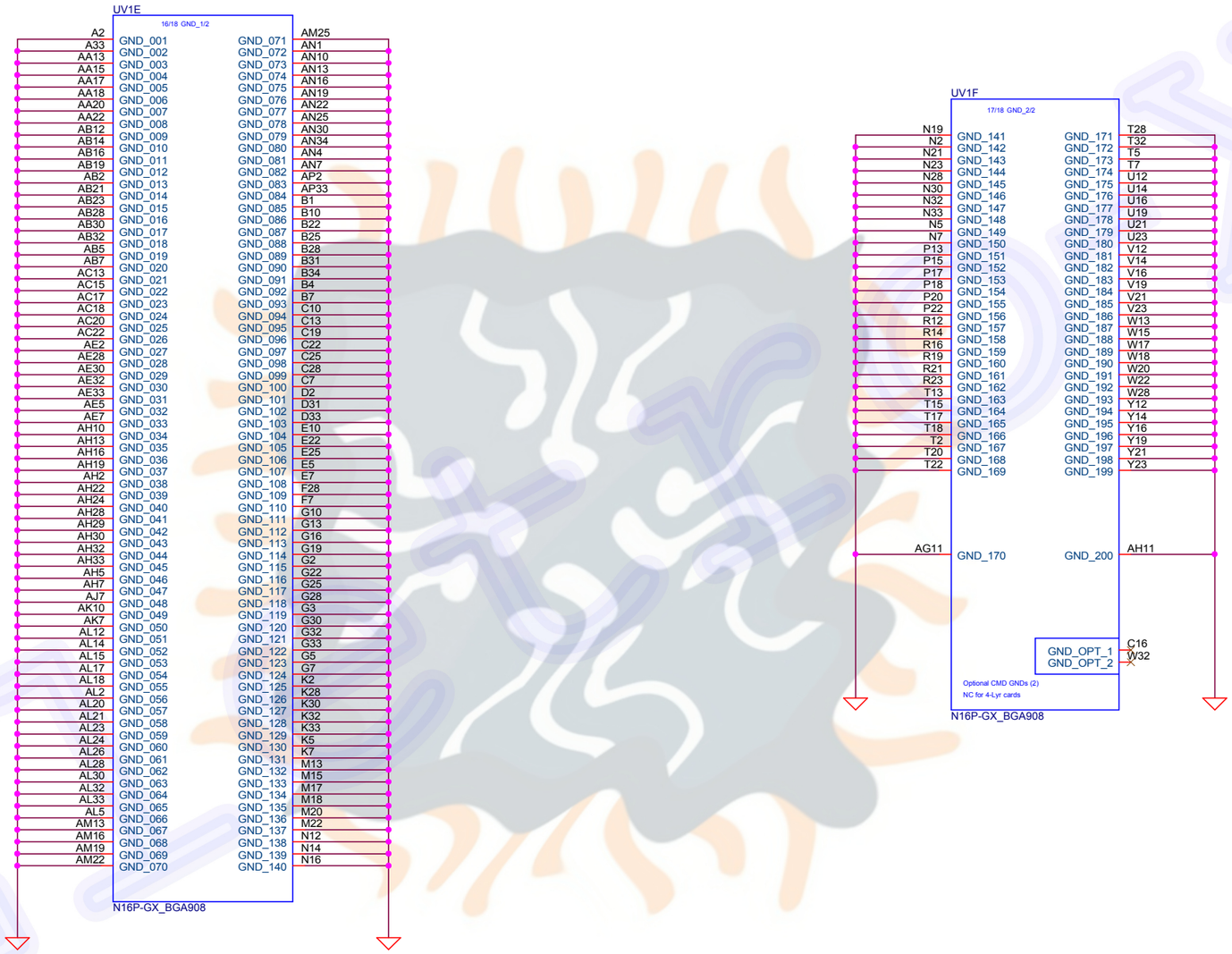

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: *036_N16P-Q1/Q3(6/6): GND*

Size	Document Number	Rev
Custom	SKYWALKER	2.1

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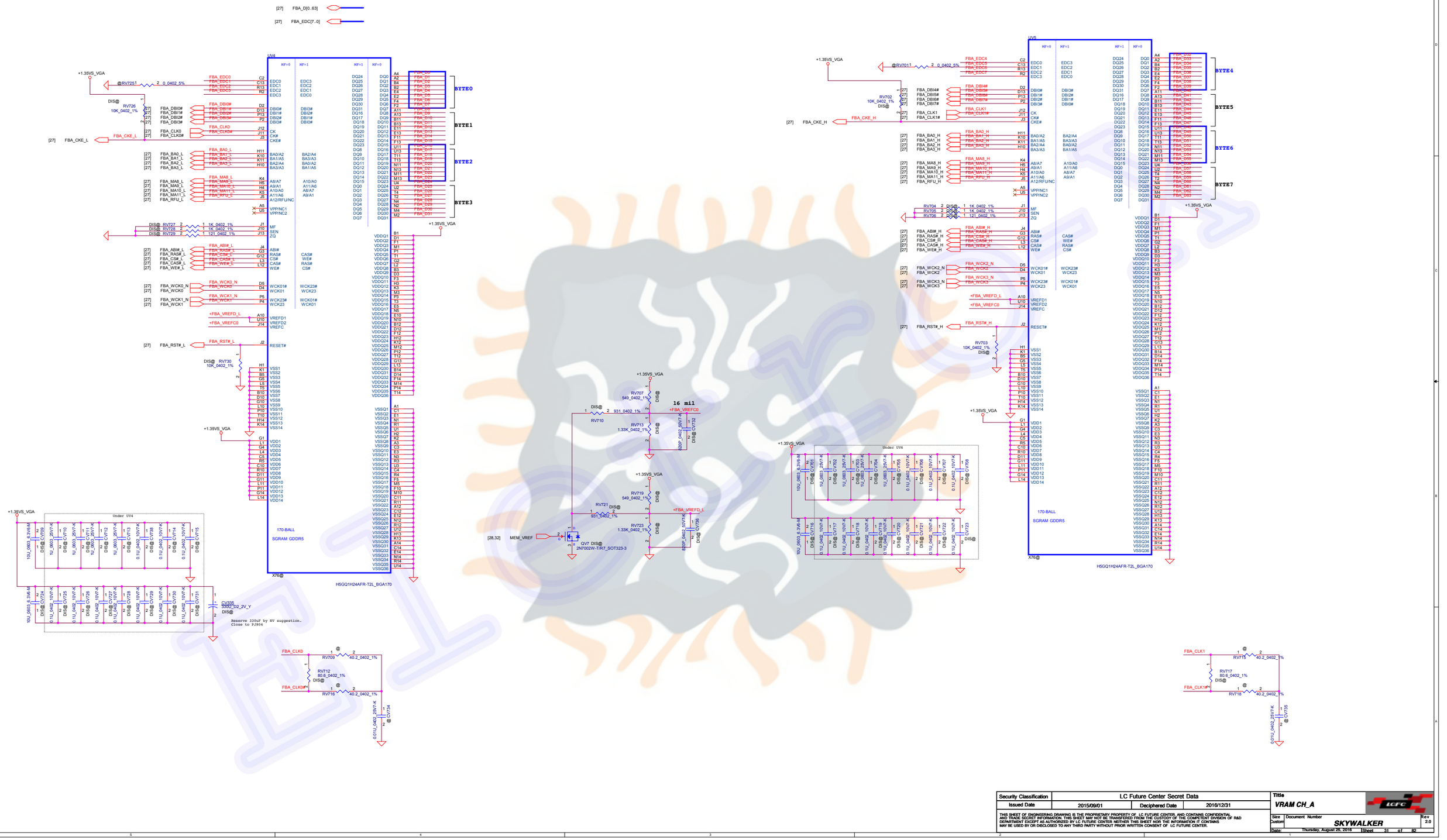

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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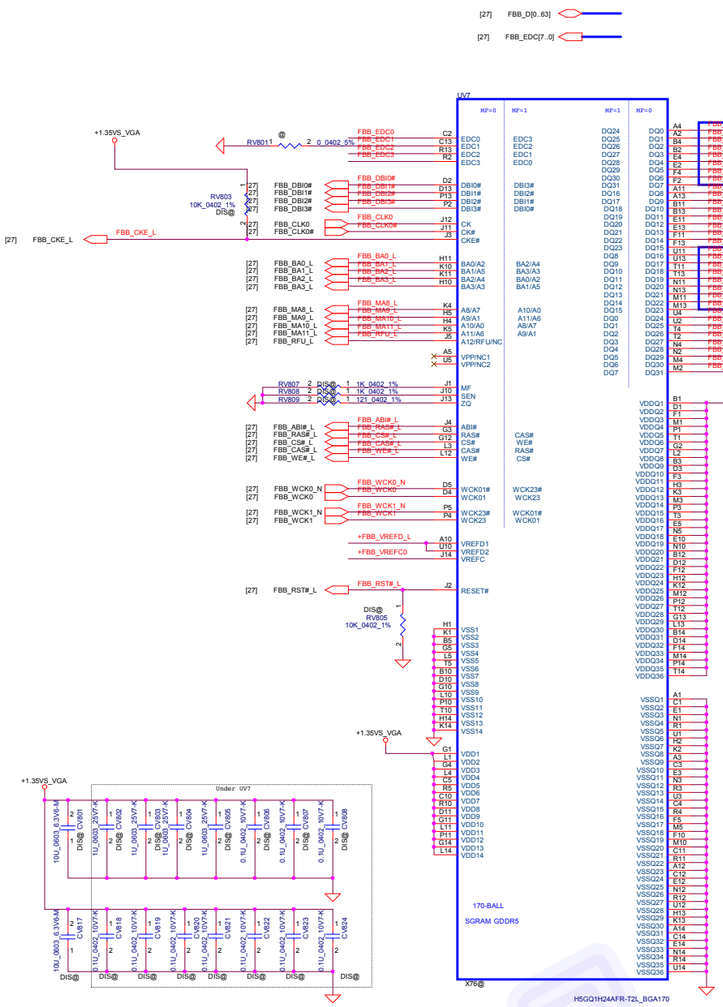
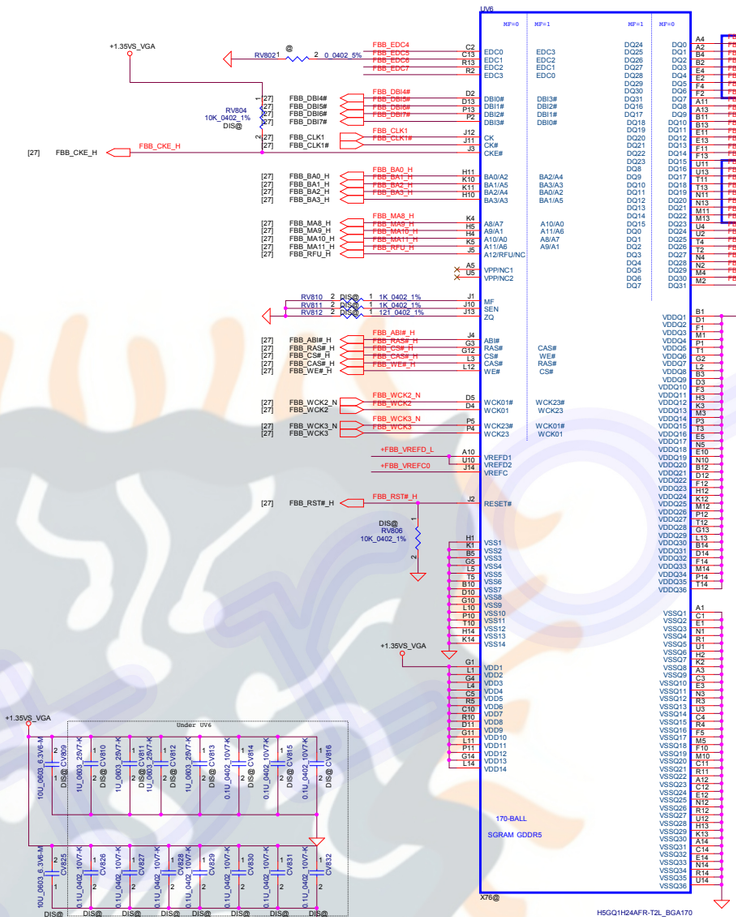
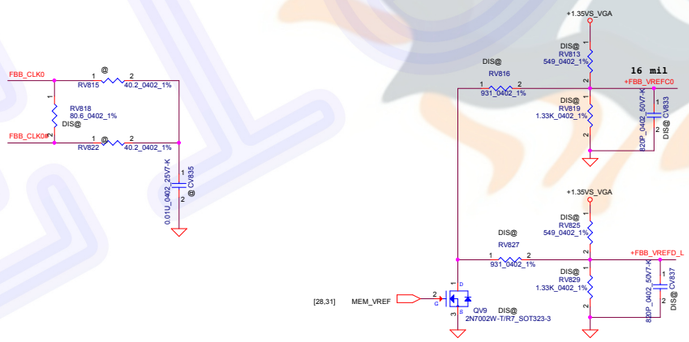
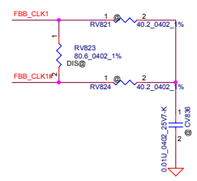
Title	VRAM CH_A		
Size	Document Number		Rev
Custom	SKYWALKER		2.0
Date:	Thursday, August 25, 2016	Sheet 31 of 82	









Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: VRAM CH_B

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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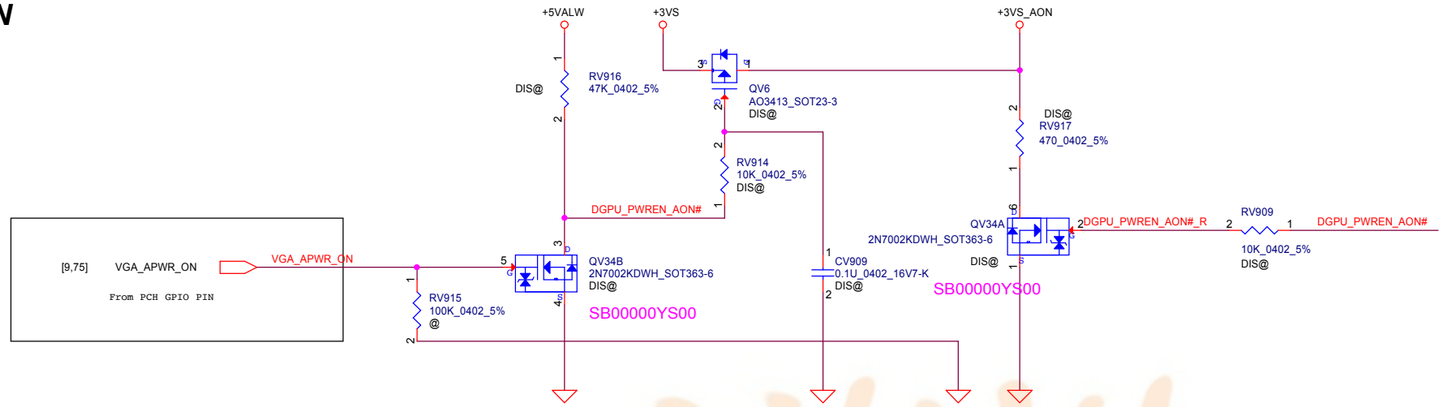
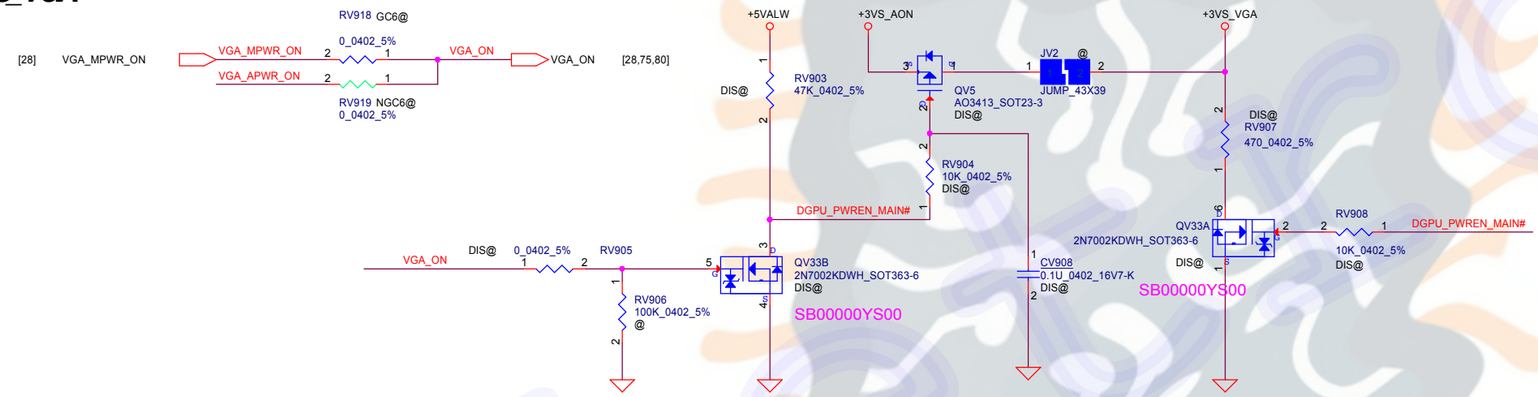
+3VS to +3VS_AON

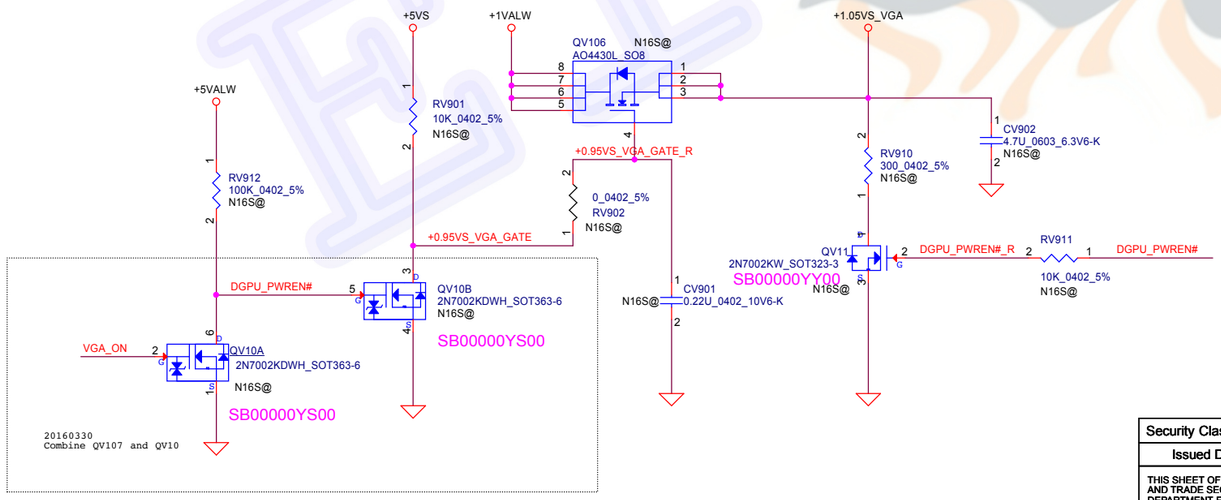


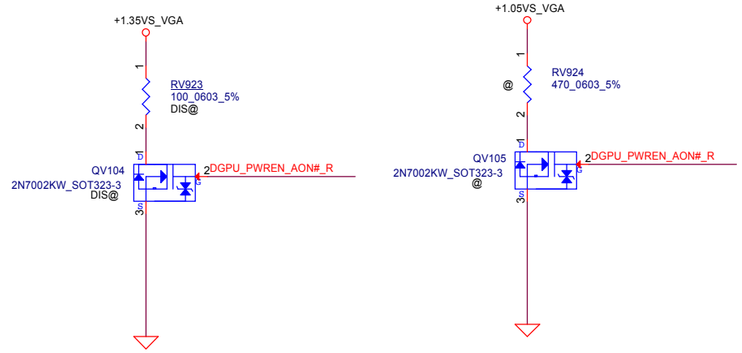
+3VS_VGA



20160310
Add 1.05VS_VGA circuit for N16S GPU

+1VALW to +1.05VS_VGA





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Title: *N16S-GT swich power*

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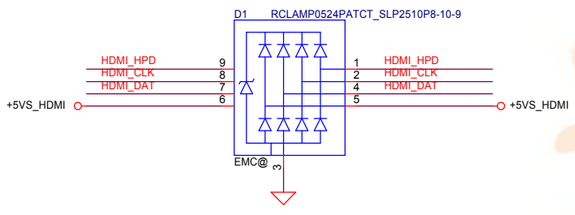
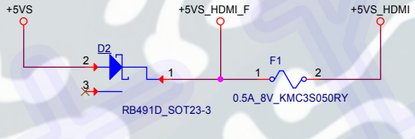
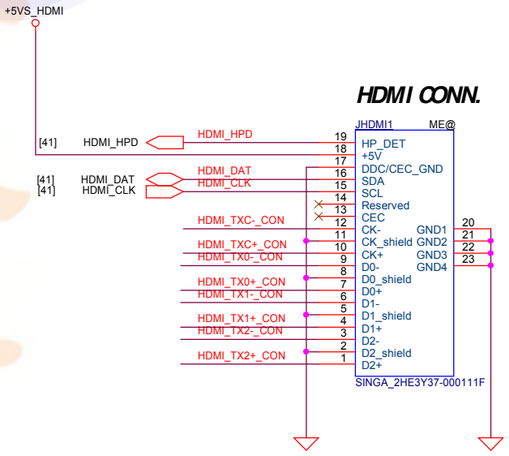
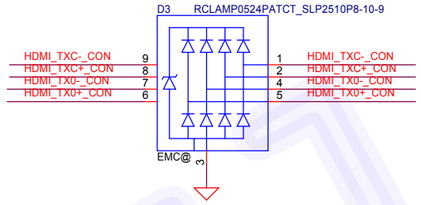
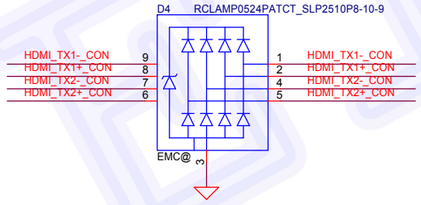






HDMI CONN.





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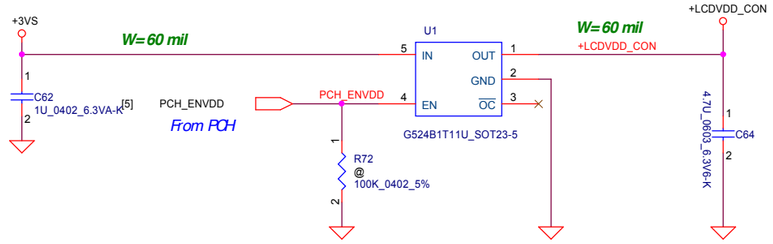
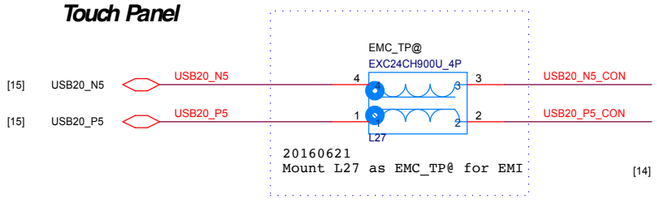
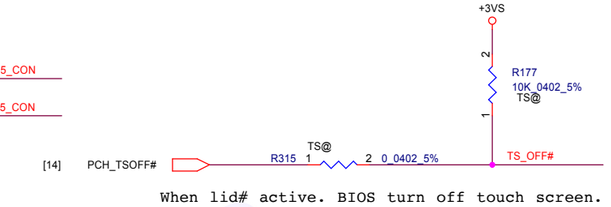
LCDVDD Circuit



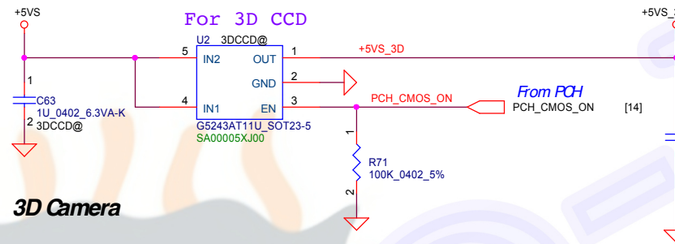
Touch Panel



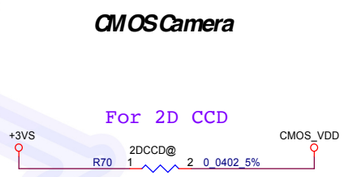


When lid# active. BIOS turn off touch screen.

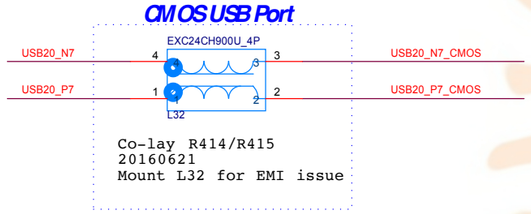
3D Camera



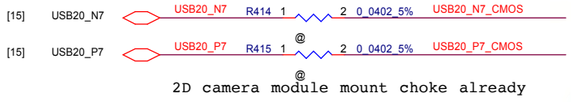
CMOS Camera



CMOS USB Port

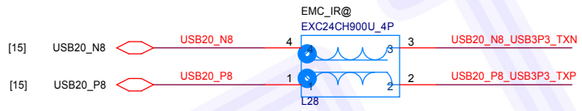


Co-lay R414/R415
20160621
Mount L32 for EMI issue

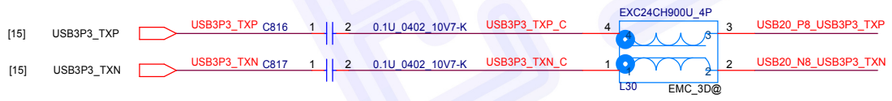


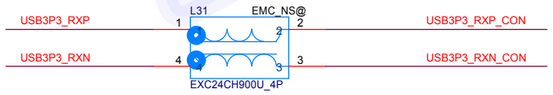
2D camera module mount choke already

IR camera USB Port



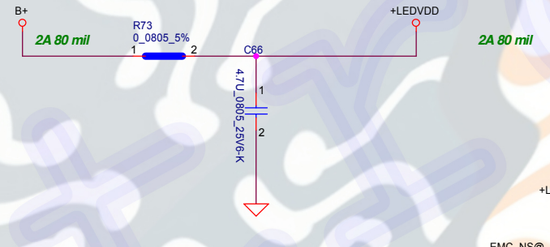
3D CCD USB Port

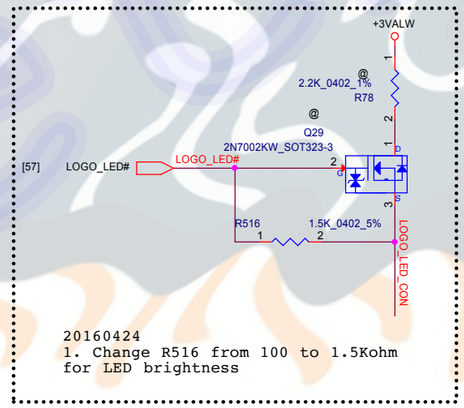




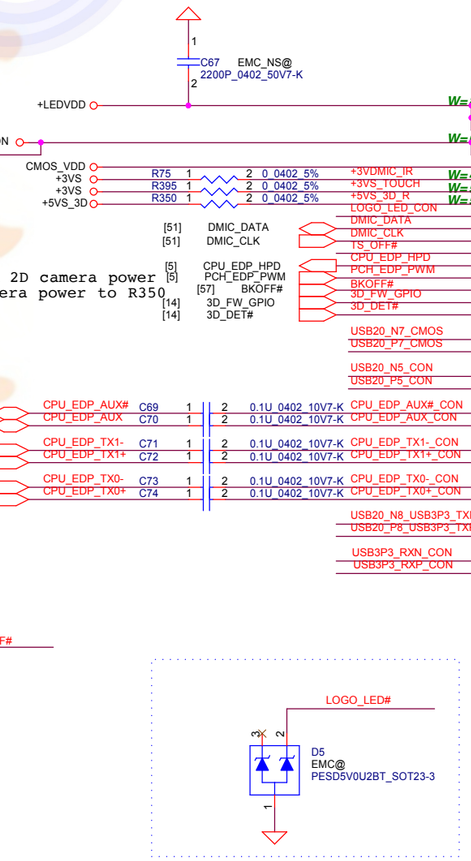
Co-lay L31 and R412/R413

3D camera module mount choke on RX already

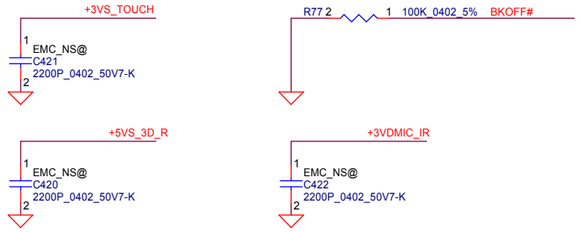




20160424
1. Change R516 from 100 to 1.5Kohm
for LED brightness



20160421
1. Spreate 3D and 2D camera power
2. Connect 3D camera power to R350



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Title: **eDP CONN**

LCFC

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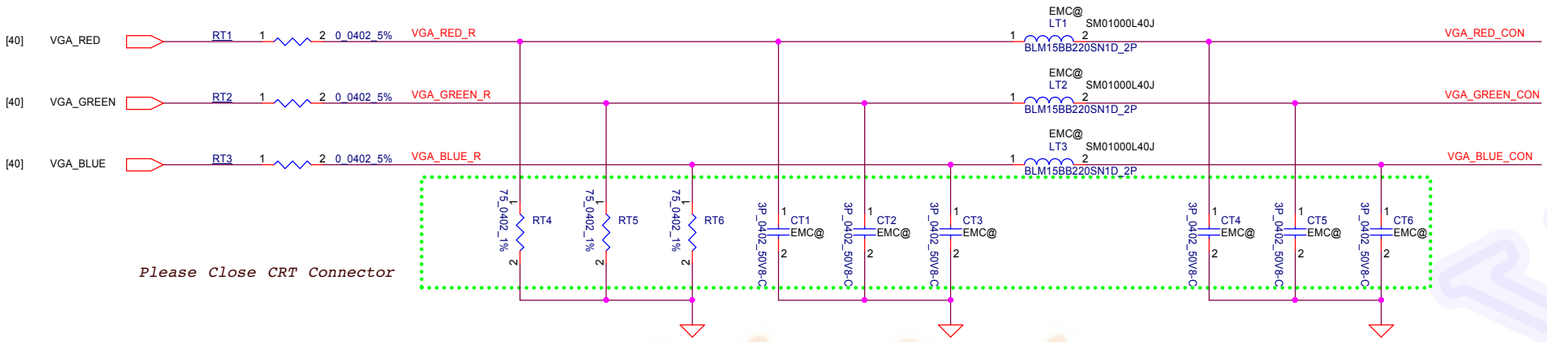
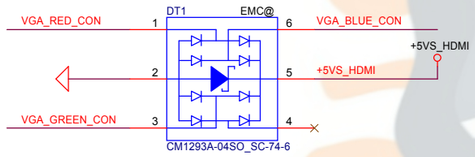
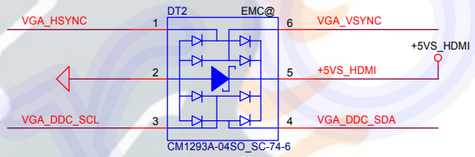
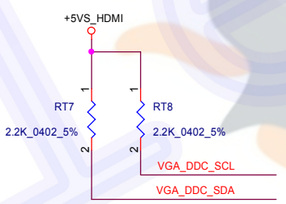


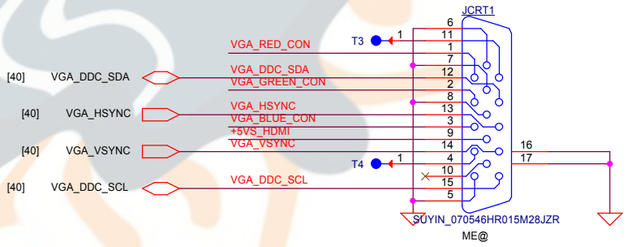






Only for 15'

CRT Connector



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Title: CRT CONN

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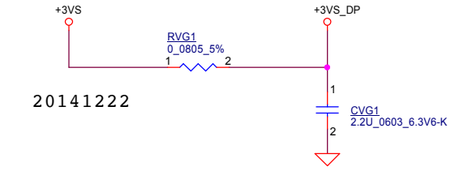
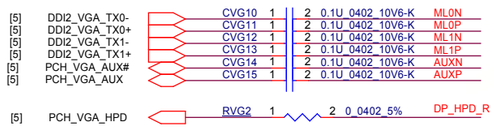
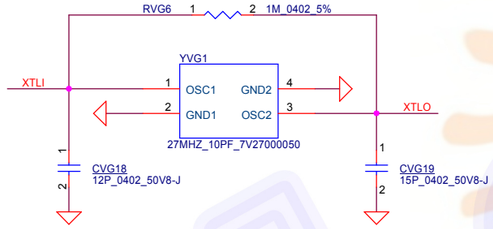
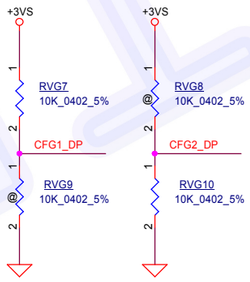






20160127
Change CVG19 to 15p by vender suggestion



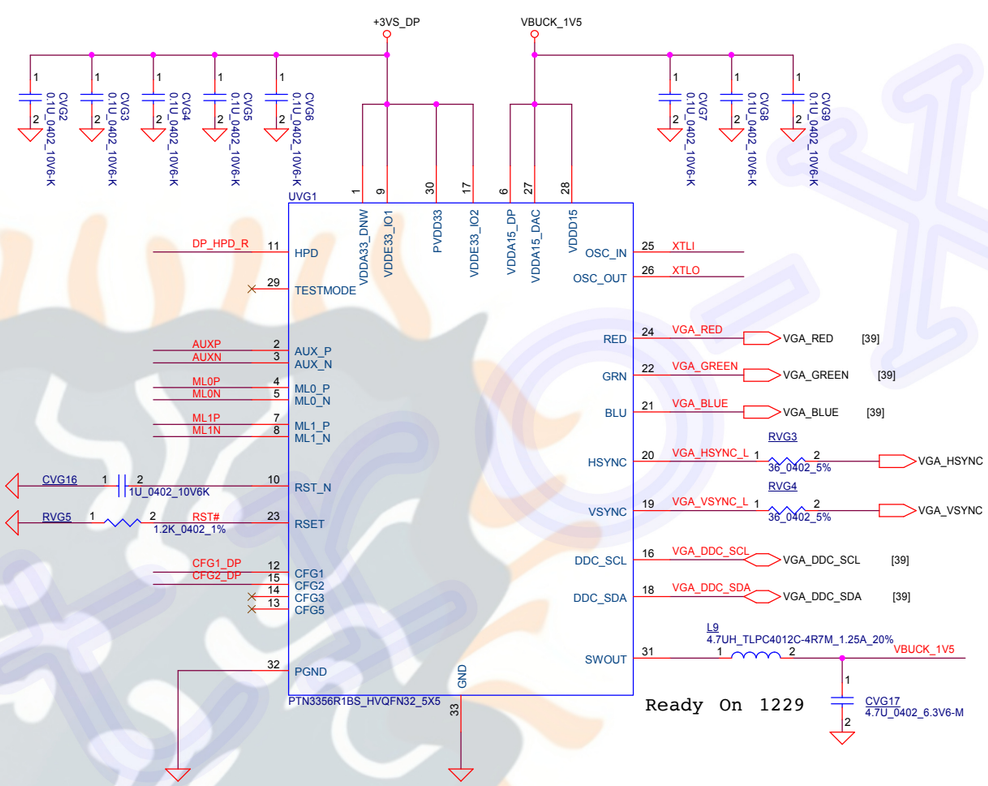


Table 7. CFG1/CFG2 pin definitions

Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior

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Title: *DP to VGA*

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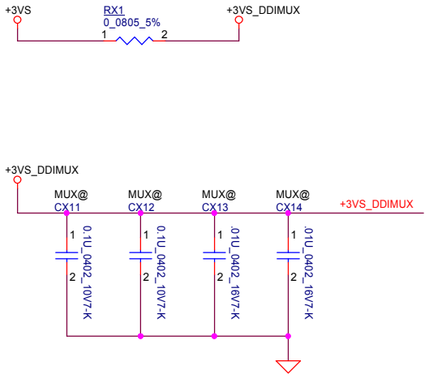

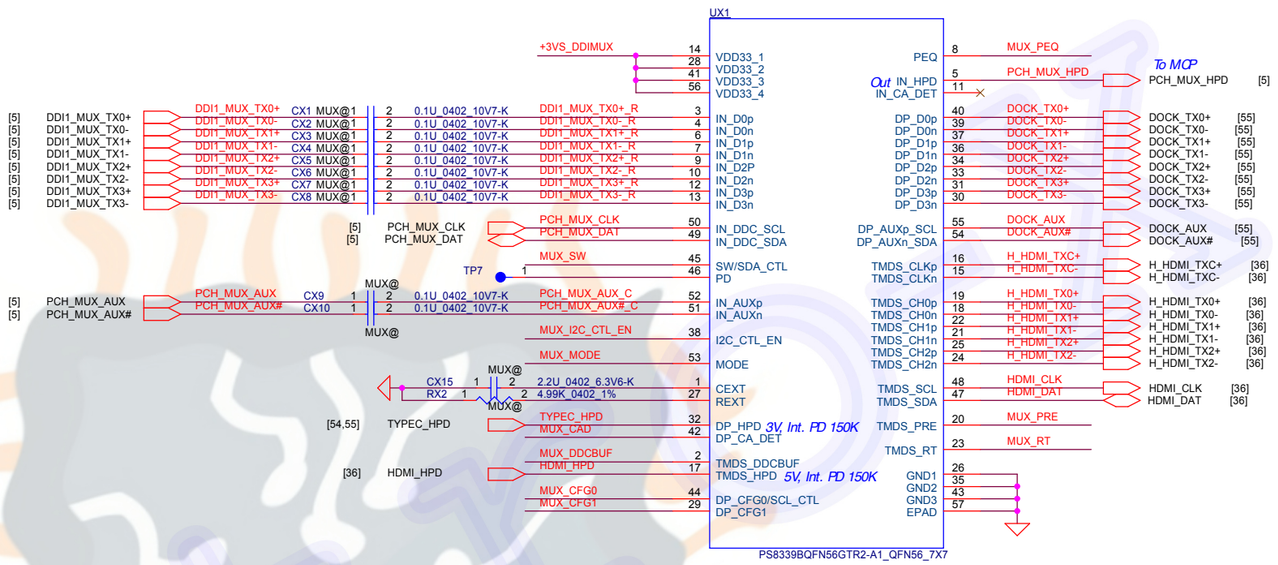

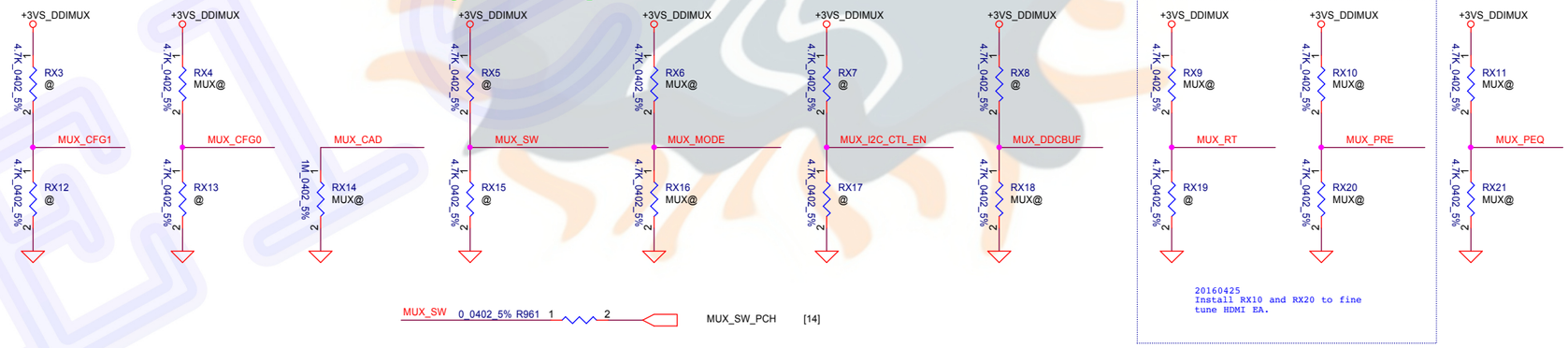

20160419
1. Connect MUX_SW to PCH, display priolity control by BIOS
2. Add R961 0 ohm and unstaff RX15.

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Title: **Mux IC**

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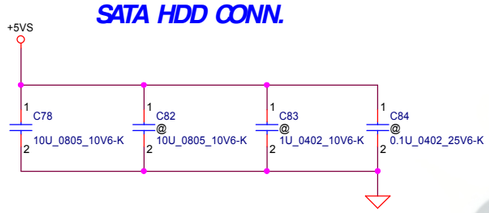

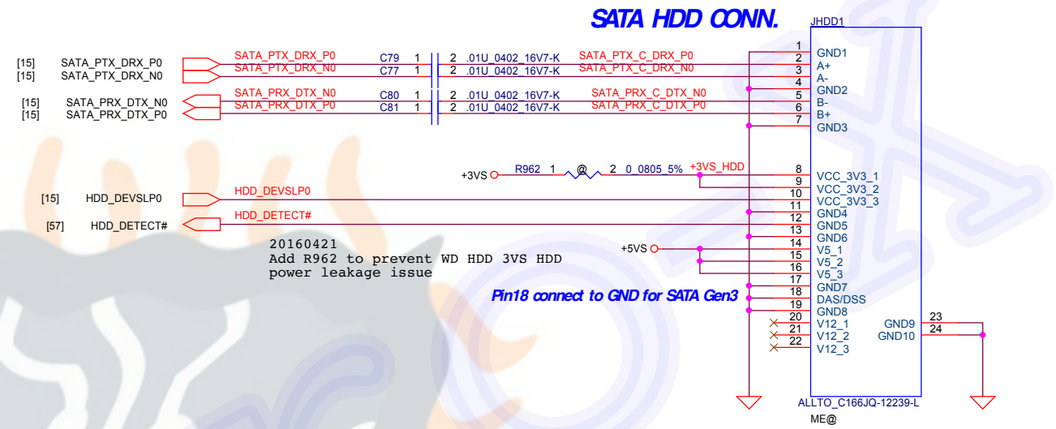

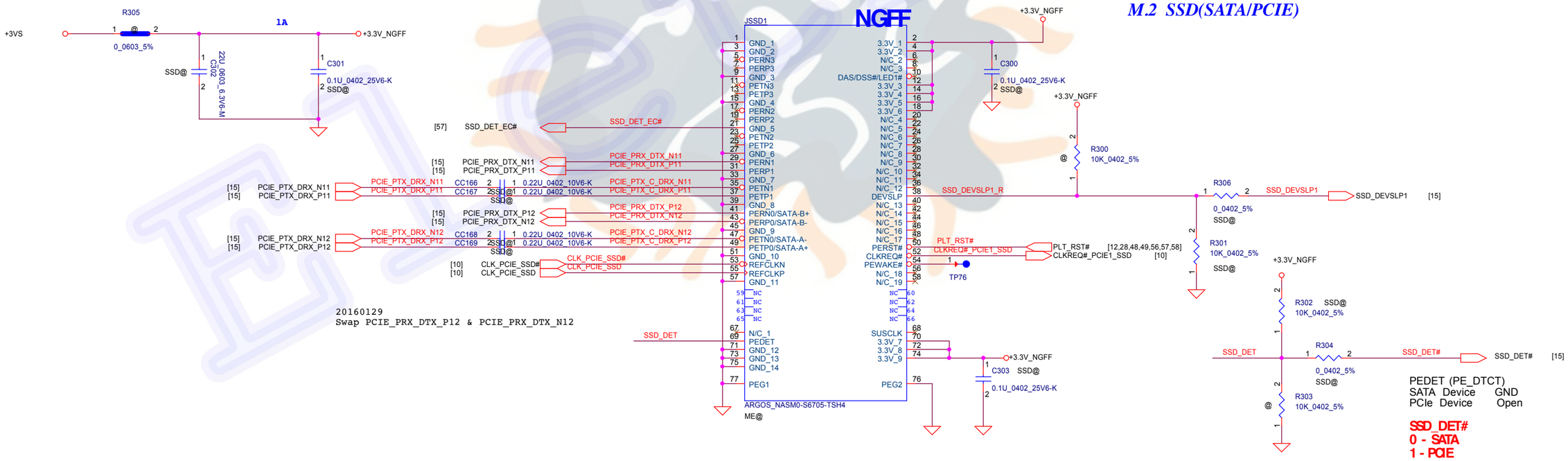

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Title: SATA HDD

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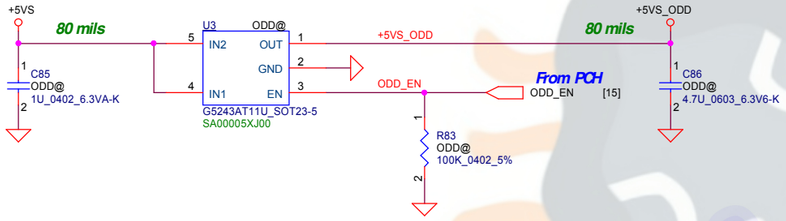
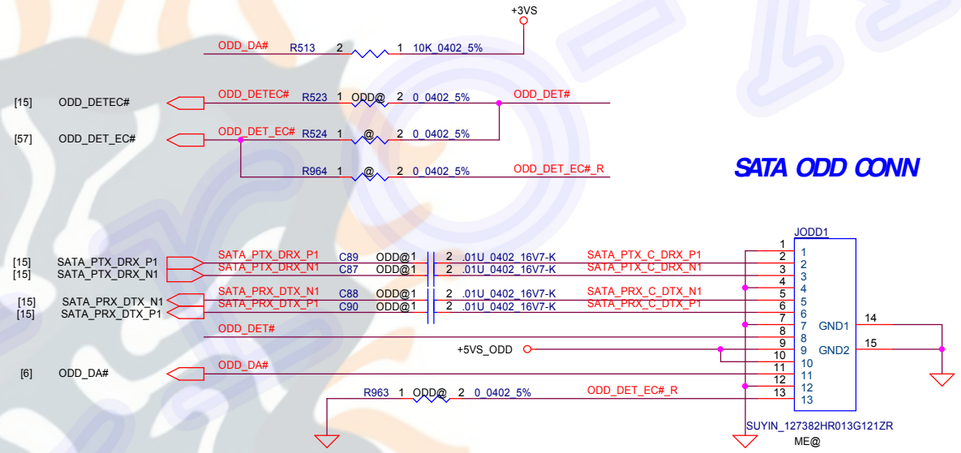
+5VSTO+5VS_ODD



SATA ODD CONN



20160421
Add R963 and reserve R964 for tember function

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Title: ODD

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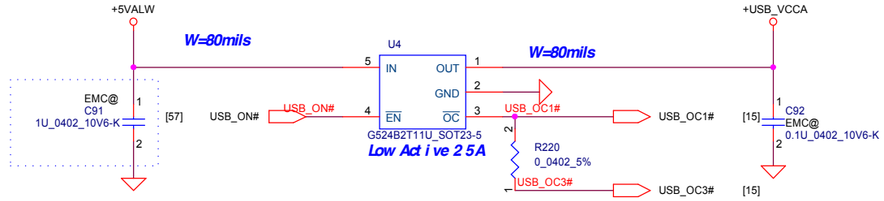
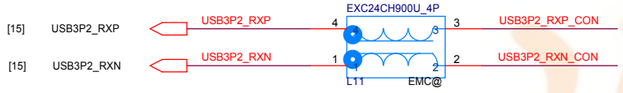
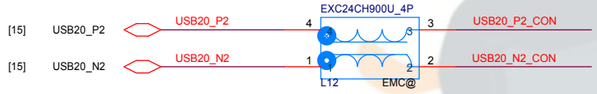
USB3 PORT2

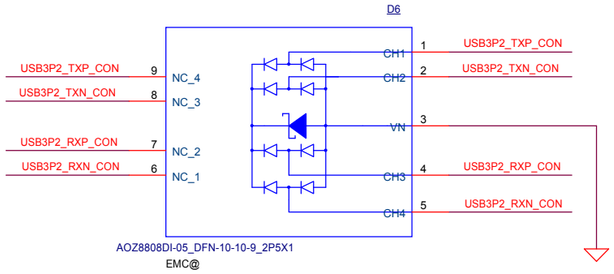
POWER SWITCH

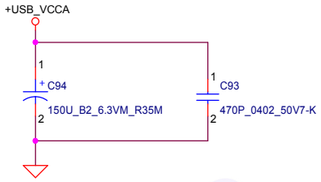


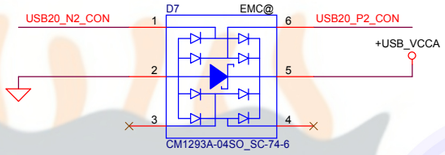
20160616
Change C91 for 0.1U_0402_10V6-K to 1U_0402_10V6-K EMC@

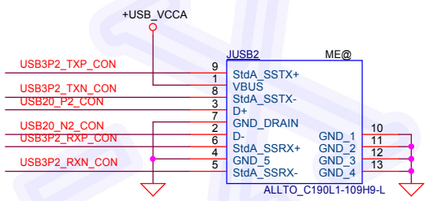




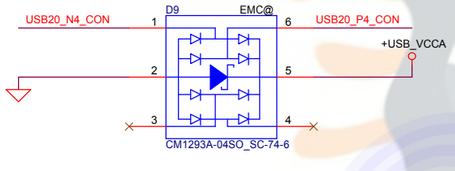


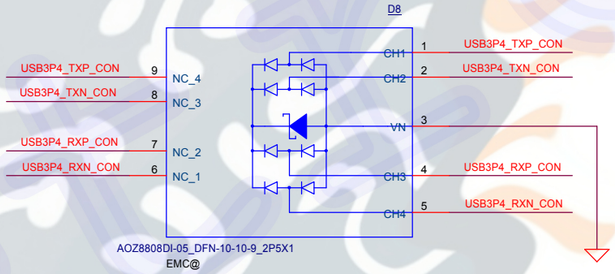


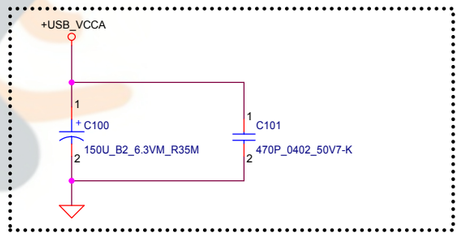


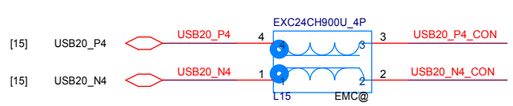


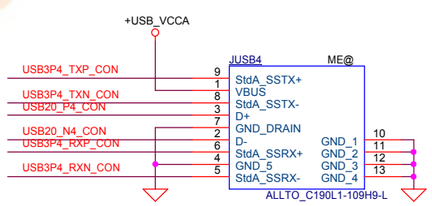
PORT4











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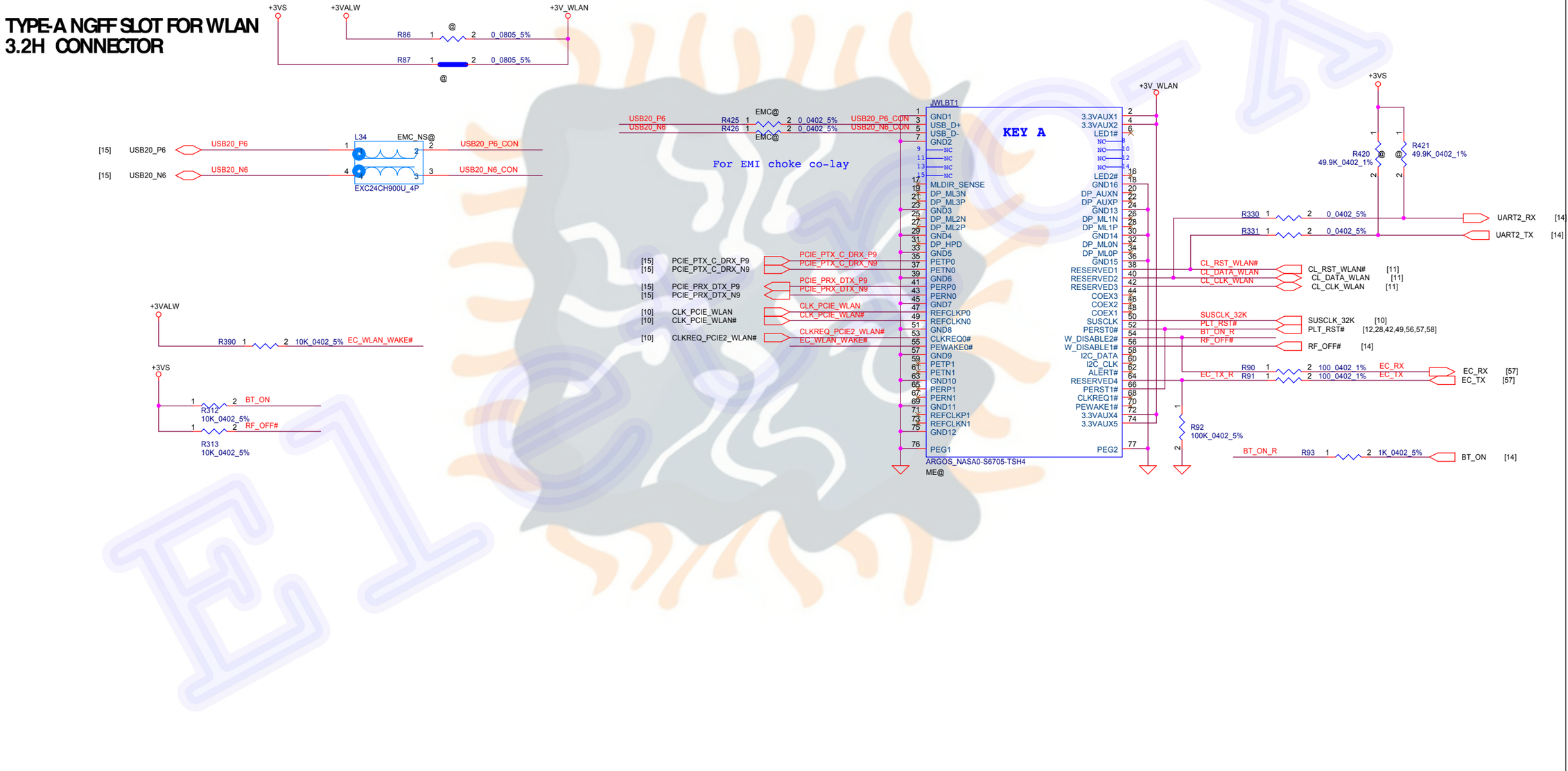
TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR



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Title: **WWAN/WLAN NGFF CONN.**

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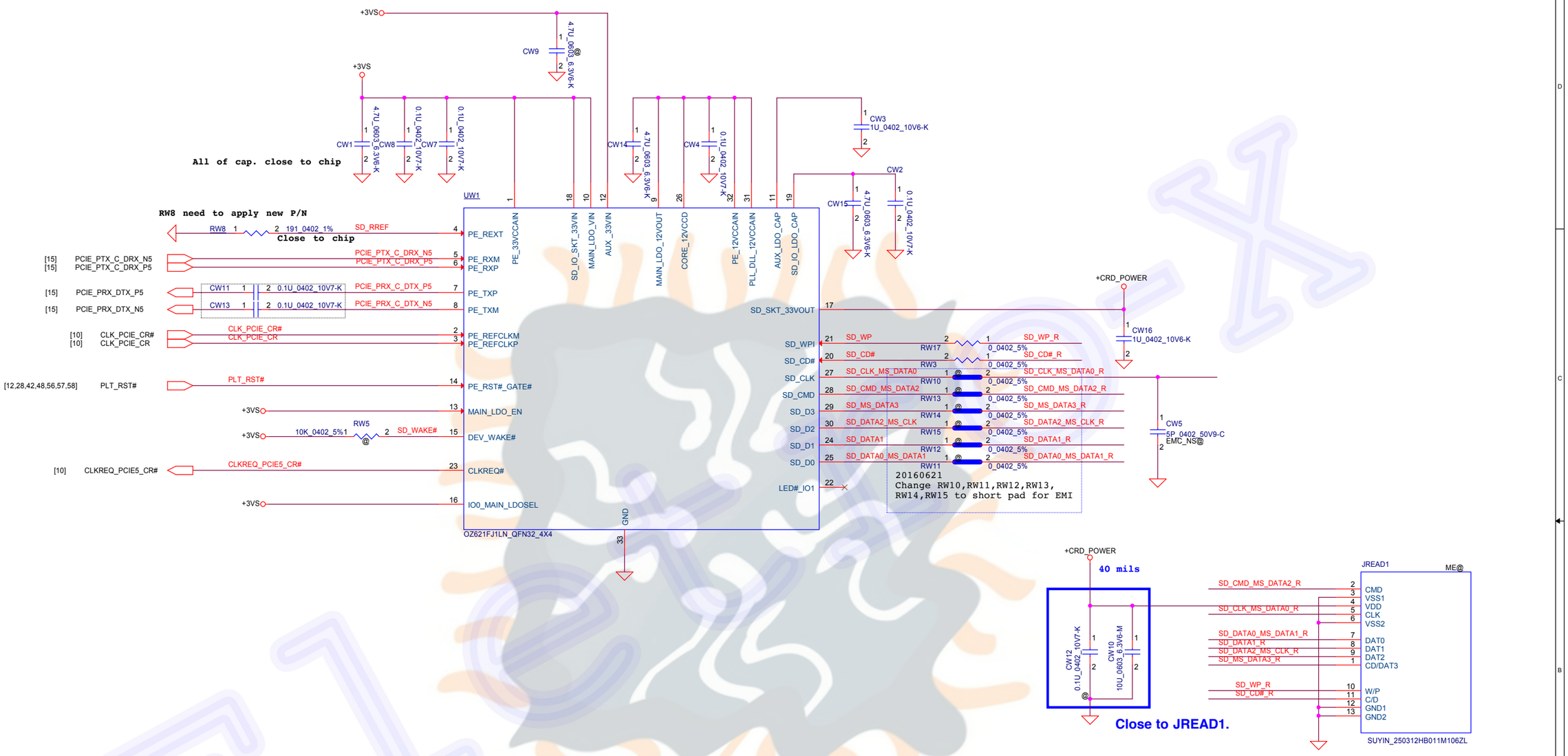

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Title: **Card Reader**

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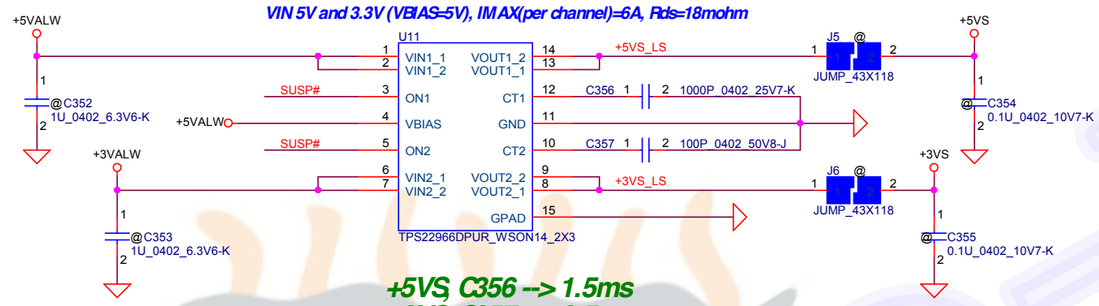
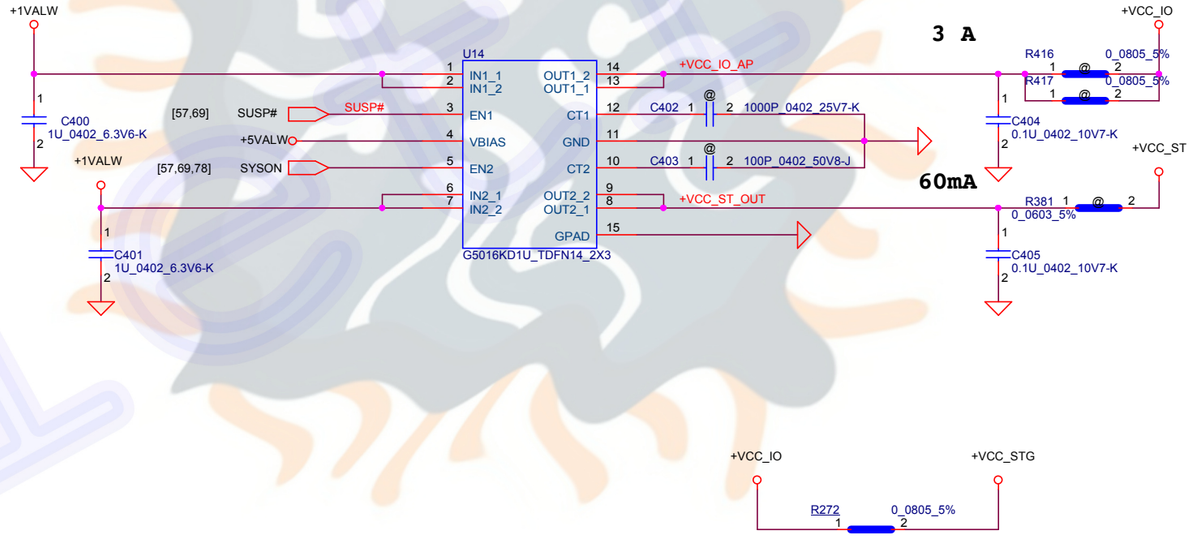
Load Switch
+5VALW To +5VS
+3VALW To +3VS



+1VALW to +VCC_IO_AP & +VCC_ST

Unstaff C402 and C403 for the fastest sequence.



Slew Rate=10uS<TR<65us

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: DC V TO VS/ V-PCH/VM

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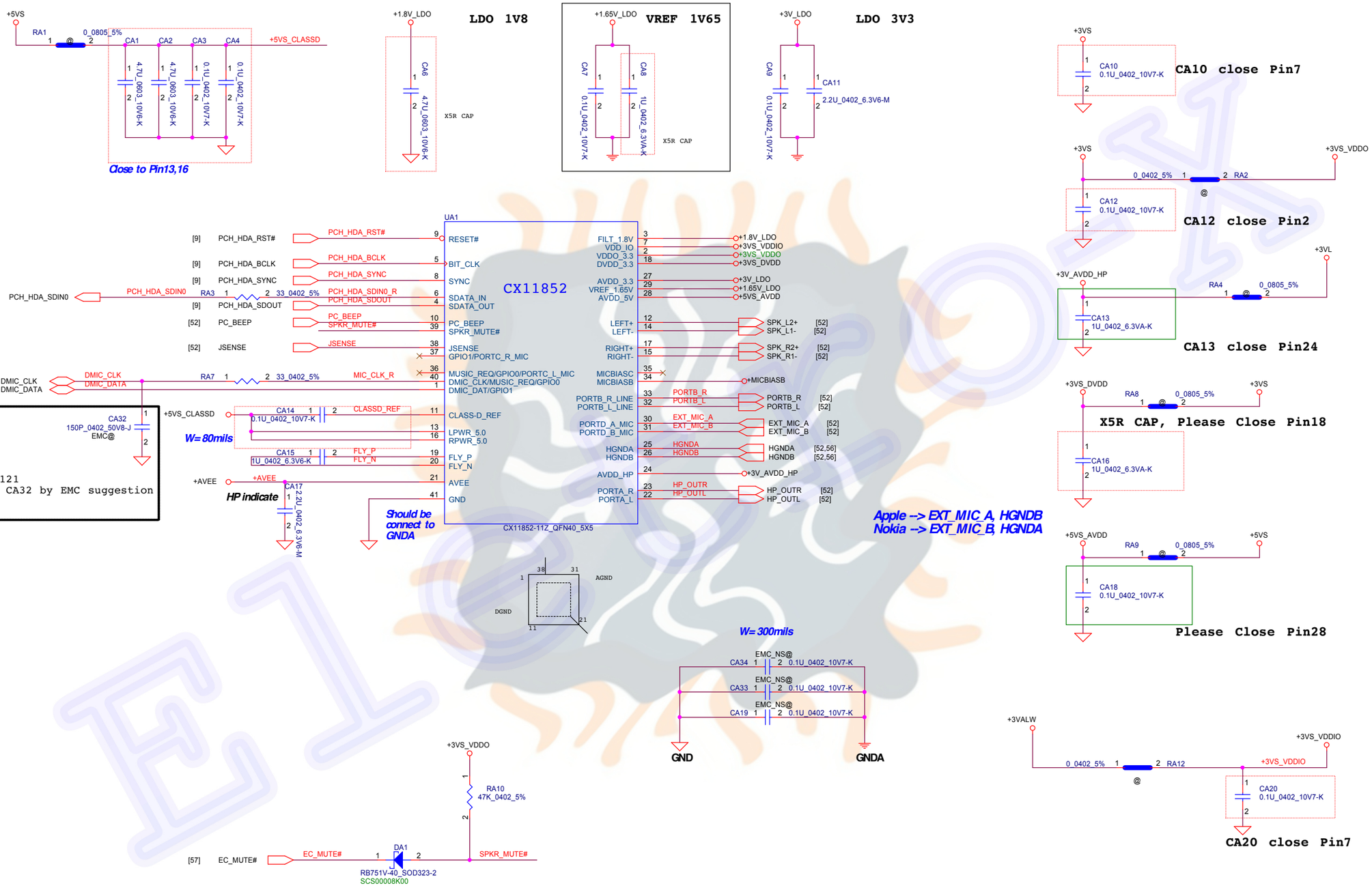

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Title: **Audio Codec**

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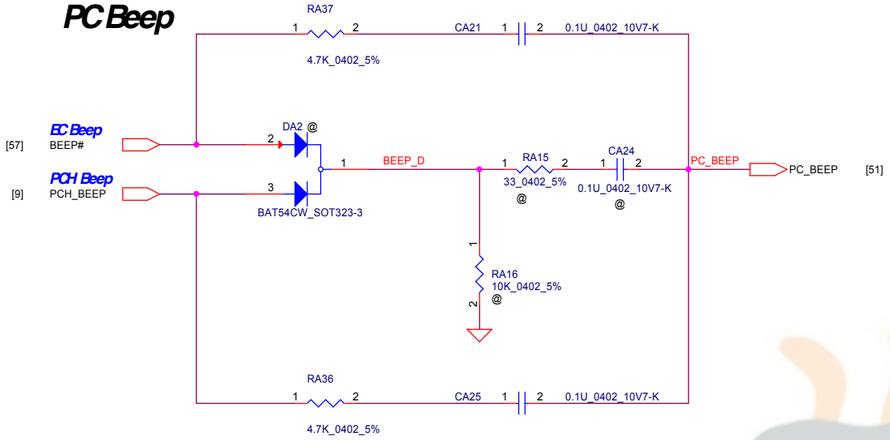
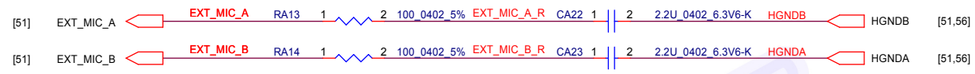
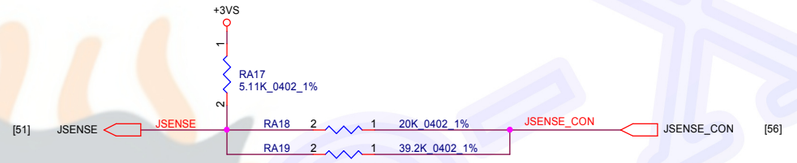
PC Beep



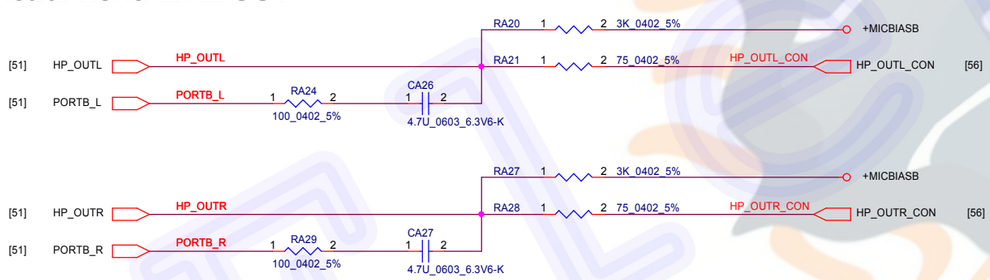
EXT. MIC/ LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



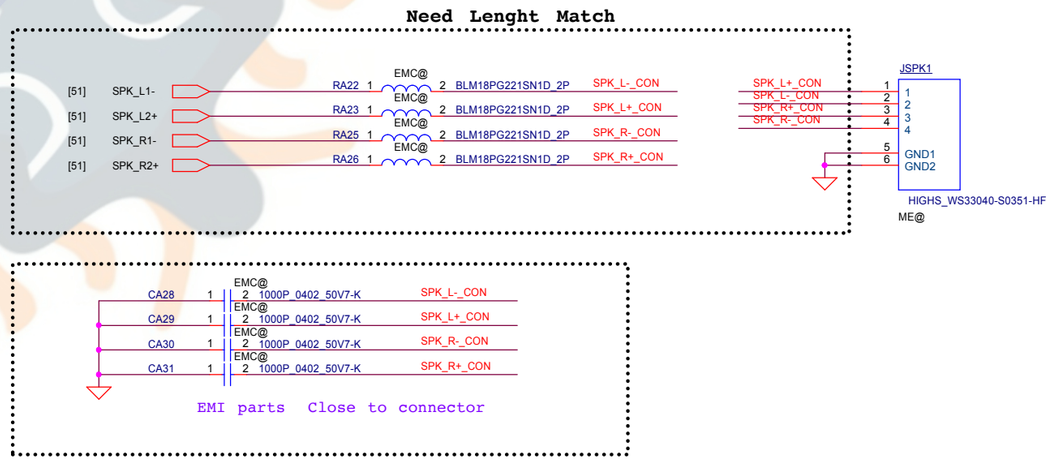


HeadPhone/ LINE OUT



Speaker OUT

SPK CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: HP/MIC JACK/Speaker

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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20160624
Change R99 Pin1 to +3VPD_VDD

20160426
1.Change C108,C109 to 150P
by vender suggestion

20160505
Change C108,109 to 390P
due to U20 material shortage

20160624
Change pull up from +3VPD to +3VALW

20160627
Change pull up from +3VALW to +3VPD_VDDIO

20160414
1.Change pull up from +3VPD to +3VALW
by vender suggestion.

20160615
Add VBUS_C_CTRL0 due to Type-C
Add R961 0_0402_5%

20160414
1.Change net name from +3VPD_VDDIO
to +3VPD_VDD

20160616
Add soft stop

VBUS_P_CTRL = 1 (Consumer Path ON)
VBUS_P_CTRL = 0/Z (Consumer Path OFF)

FROM SYSTEM

20160309
1. Reserve R896 for discharge circuit.

20160624
Type-C solution for inrush current
Change R536/R537 to 10M_0201_5% TYPEC@ for layout place
Change R974/R975 to 100K_0201_5% TYPEC@ for layout place
Change C8622/C8623 to 0.0.1U_0201_25V6-K TYPEC@ for layout place

20160627
Change R974/R975 to 10K_0201_5% TYPEC@

20160824
Due to EMI fail with Acbel typeC adapter
EMI suggest add -filter

20160624
Change F10 connect to VCCPD_VBUS

20160616
Change +3VAWL to +3V_MUX

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Title: TYPE-C_Controller

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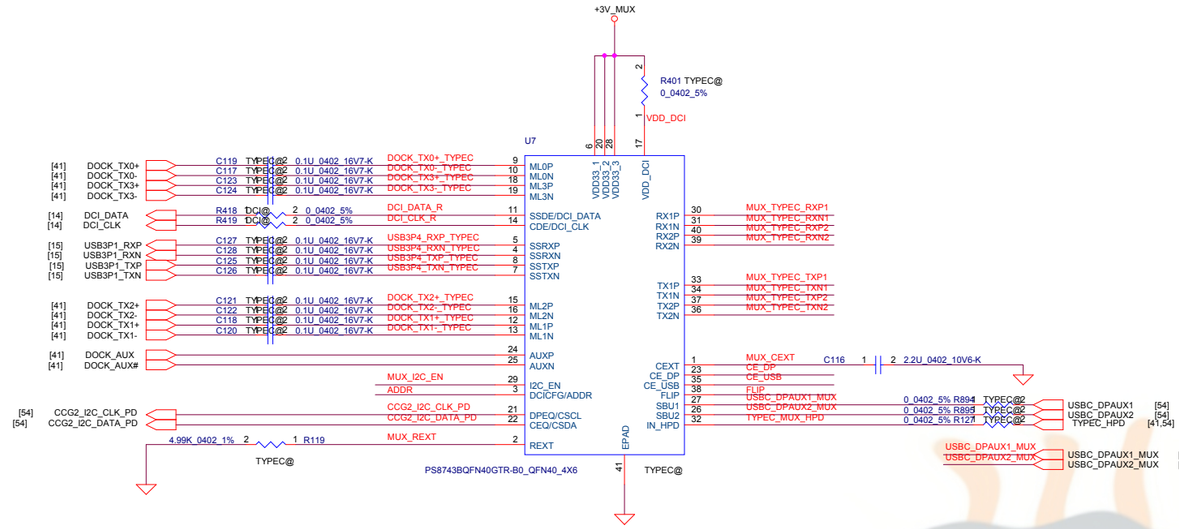
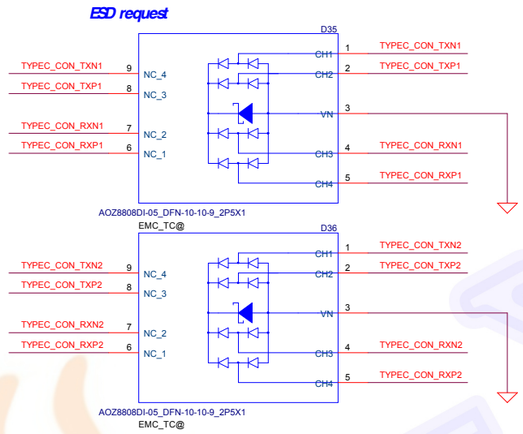
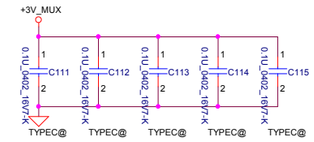
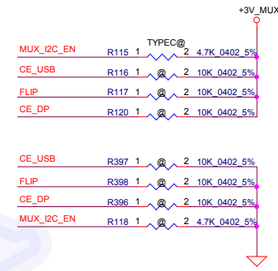
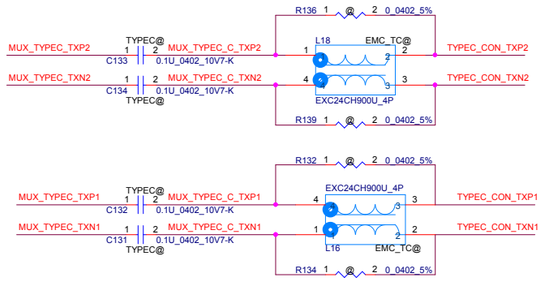
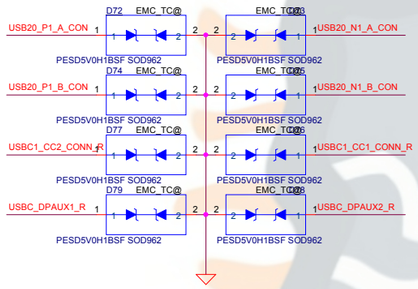


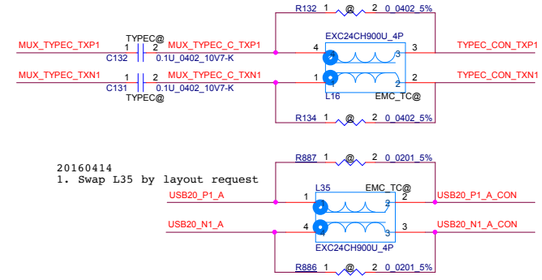




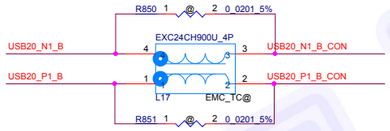


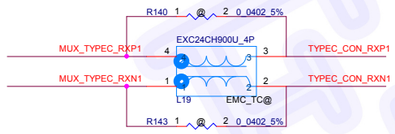


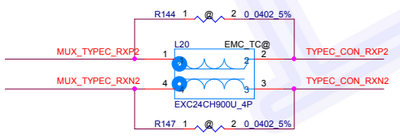




20160414
1. Swap L35 by layout request





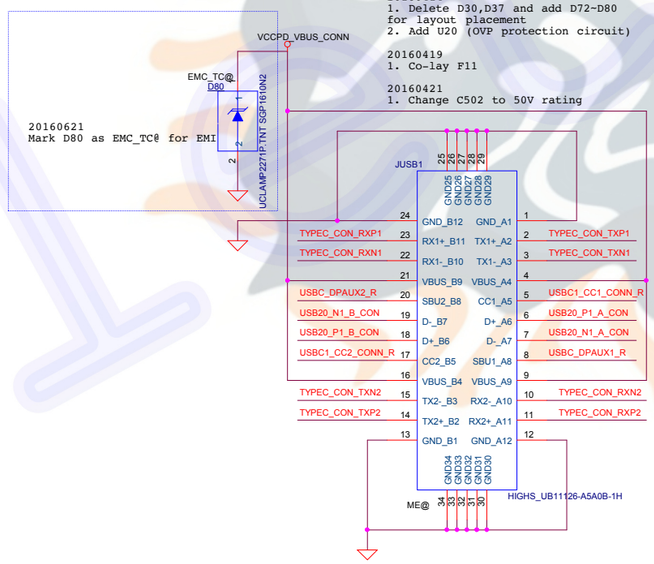


20160414
1. Delete D30,D37 and add D72~D80
for layout placement
2. Add U20 (OVP protection circuit)

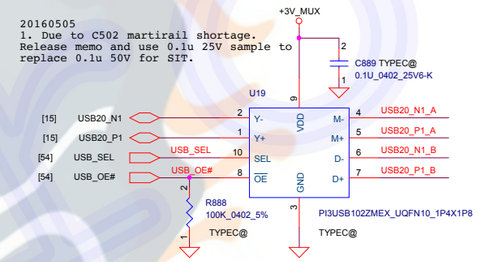
20160419
1. Co-lay F11

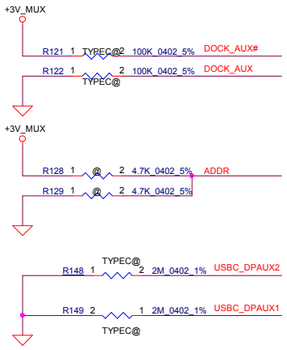
20160421
1. Change C502 to 50V rating

20160621
Mark D80 as EMC_TC@ for EMI



20160505
1. Due to C502 martirail shortage.
Release memo and use 0.1u 25V sample to
replace 0.1u 50V for SIT.





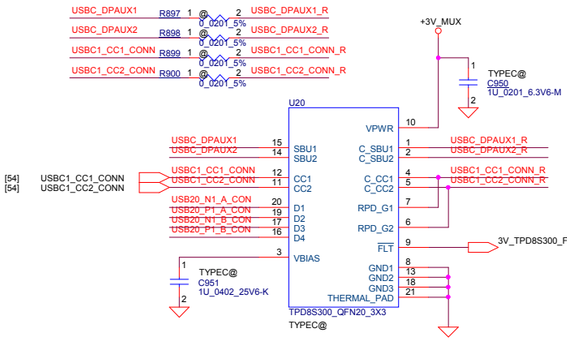
20160330
1.Add CC/SBU
protection solution

20160505
1. Unstaff U20 and staff
R897,R898,R899,R900
due to U20 martirail shortage.

201616
FLT pin into U5 pin30

20160624
1. Change VPER to +3V_MUX

20160719
1. U20 martirail prepare ready.



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Title: TYPE-C_MUX

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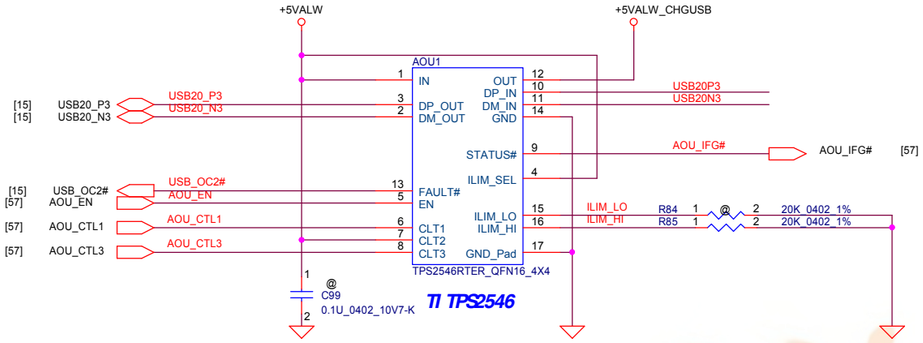
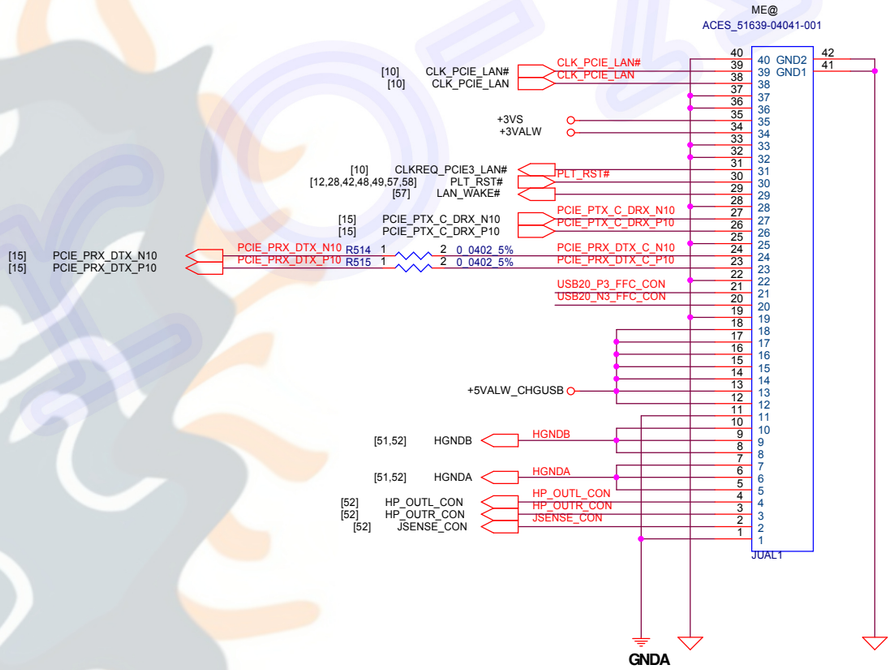


	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
	0	0	0	X	**DCH**	OUT held low
*	1	1	1	1	**CDP**	Data Connected and Port Power Mgt. Function Active
*	1	1	1	0	**SDP2**	Data Connected
*	1	1	0	X	**SDP1**	Data Connected
*	0	1	0	X	**SDP1**	Data Connected
	1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	**DCP_Auto**	Data Disconnected and Port Power Mgt. Function Active
	0	0	1	X	**DCP_Auto**	Data Disconnected and Power Wake Function Active



1. AC Capacitor place on Sub/B

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Title: **DOCKING/ DCIN CONN**

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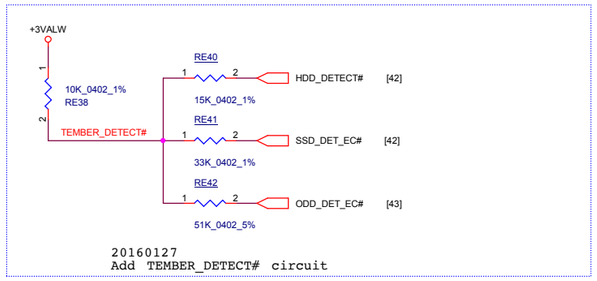
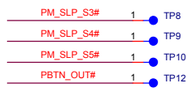
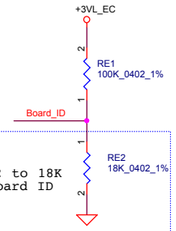
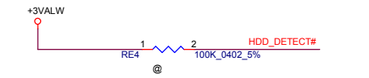
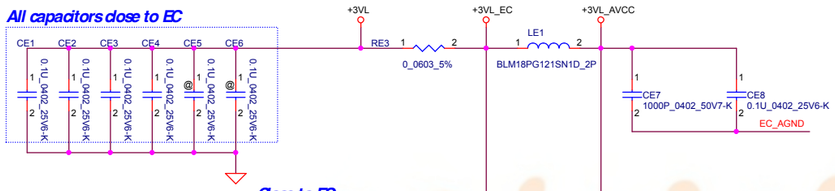


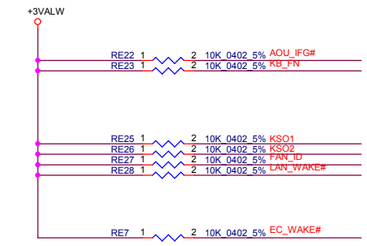


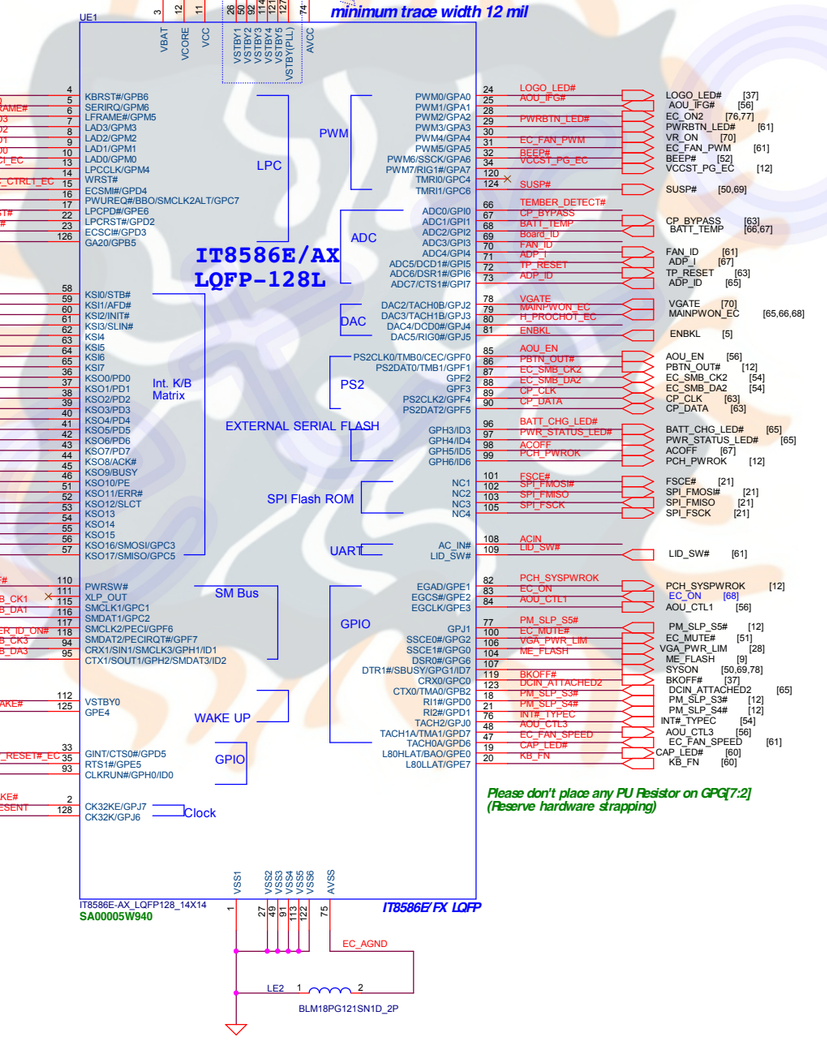


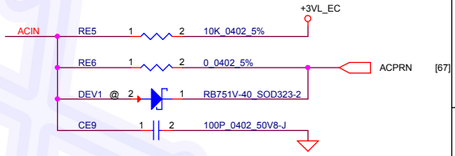
Vcc	3.3V +/- 5%				
RE1	100K +/- 1%				
Board ID	RE2	VAD_BID min	VAD_BID typ	VAD_BID max	Phase
0	OK +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

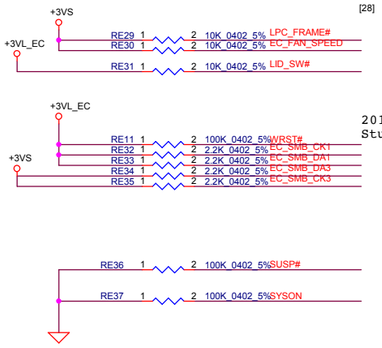


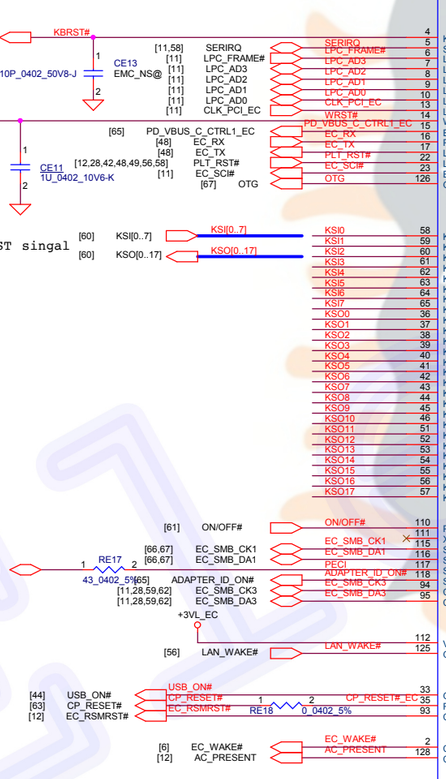


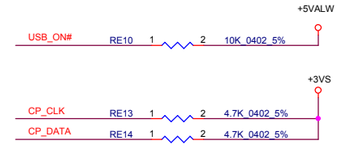




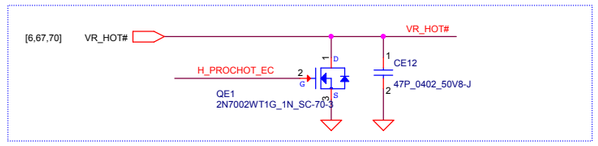


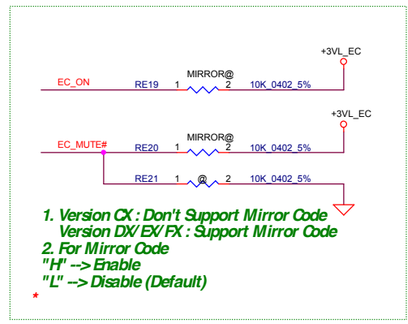






Un-stuff if not necessary.





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Title: EC

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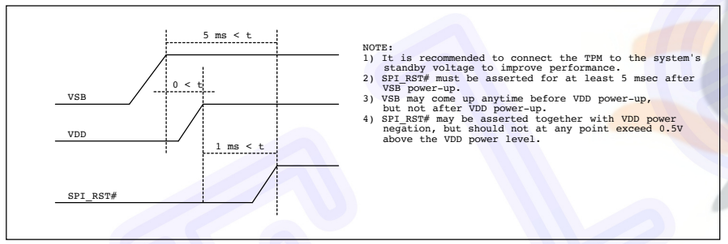
TPM IC

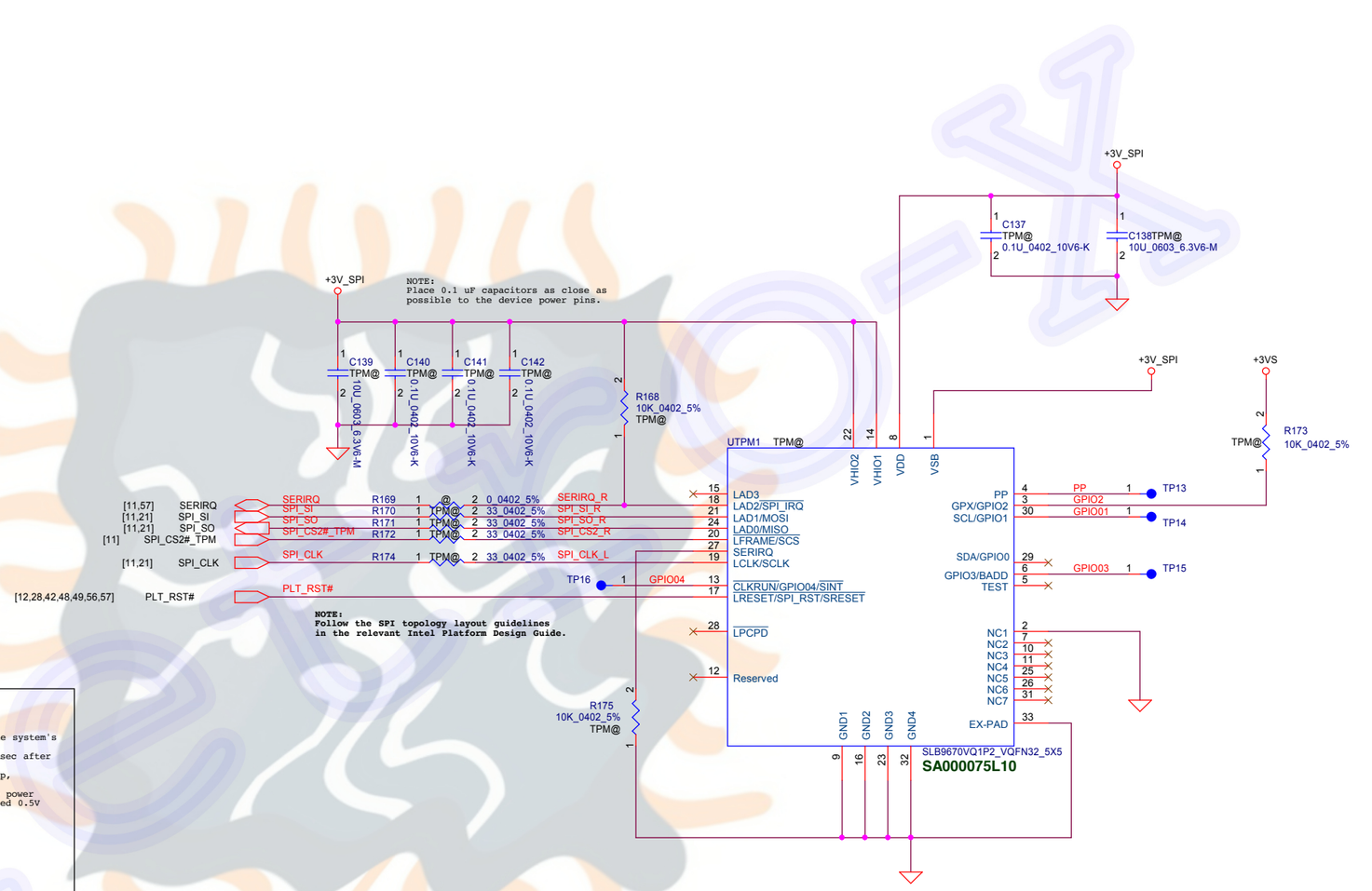
TABLE

Pin No	TCG PTP Spec (x38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table

NOTE:
Check timing sequence in SDV phase.





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: TPM

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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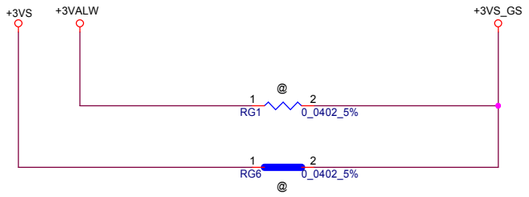


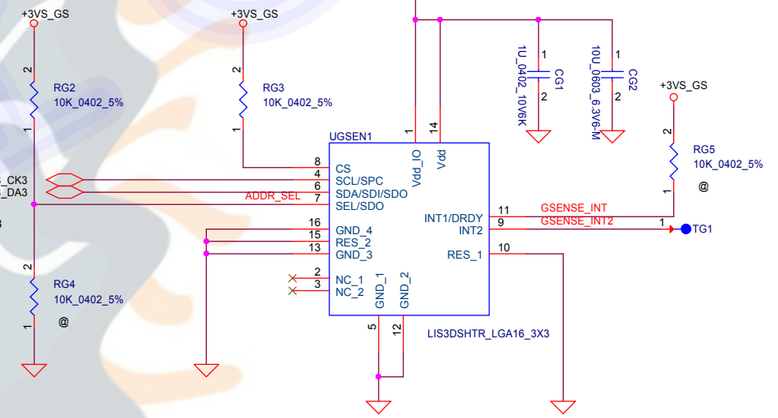
APS G-Sensor

TABLE

P/N	ADDR_SEL	Address
LIS3DSHTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: G SENSOR

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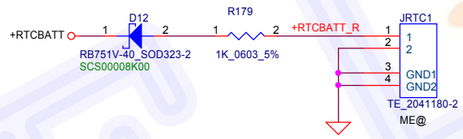
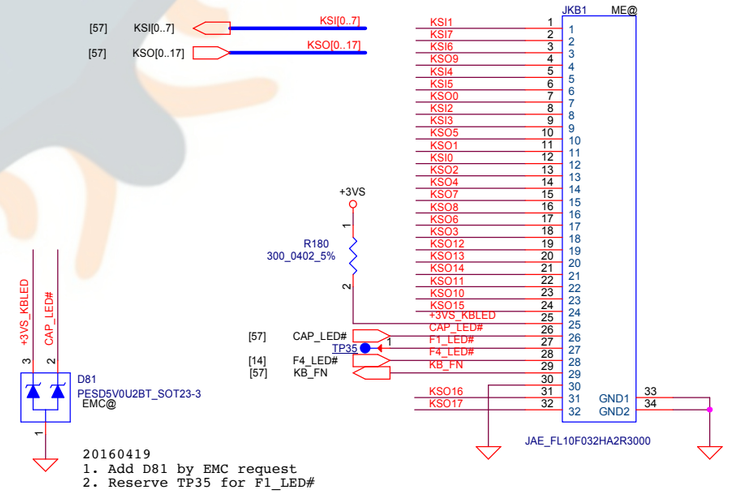
RTC CONN.



KB CONN



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KB/RTC/TOUCH PAN CONN.**

Size	Document Number	Rev
Custom	SKYWALKER	2.0
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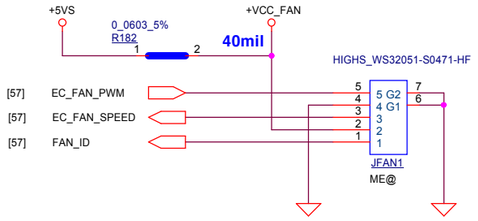
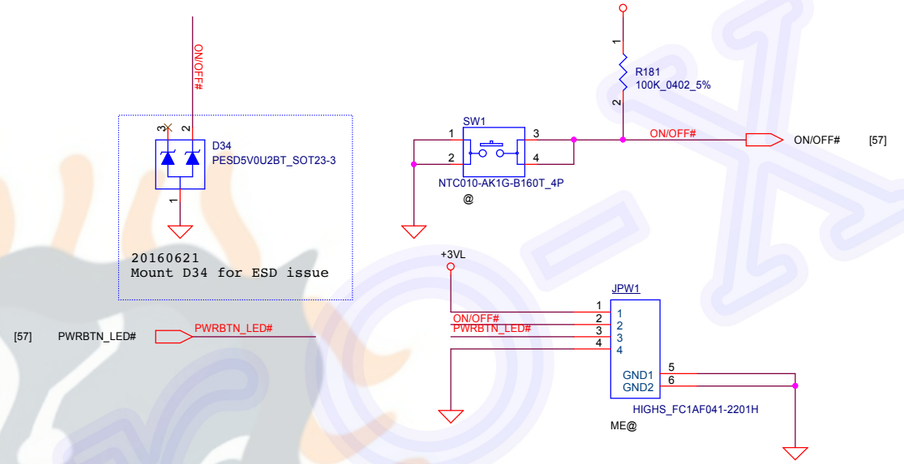
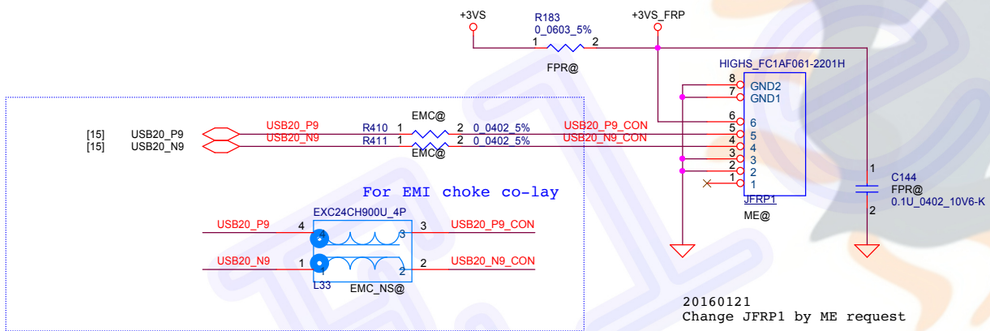
FAN CONN.



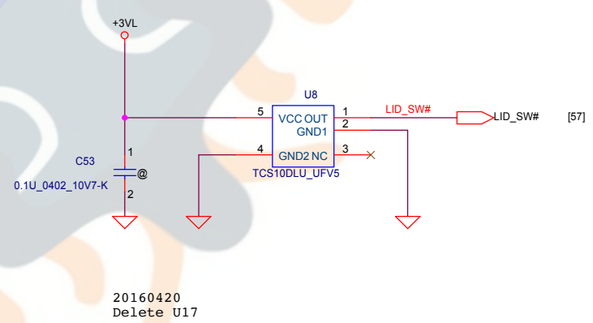
PWR BTN



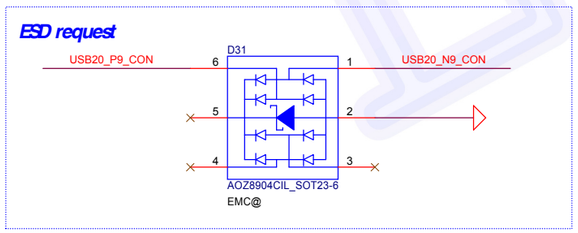
FingerPrint CONN.



Lid Switch



ESD request



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: PBTN/LID/FP/FAN CONN.

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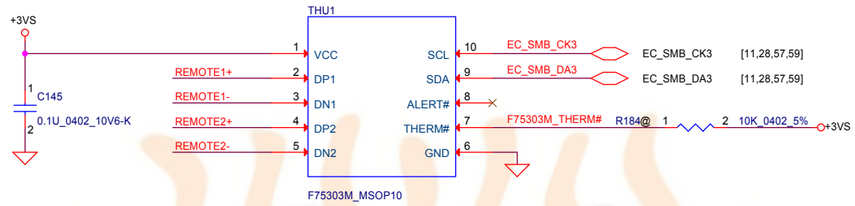
Thermal Sensor placed near by VRAM

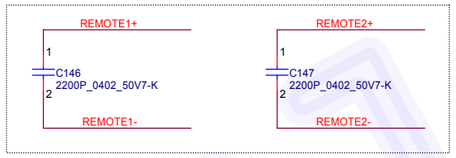


Address 1001_101xb

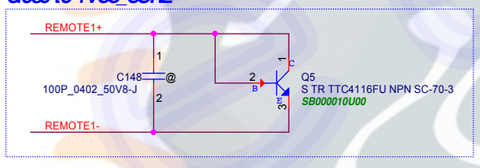
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

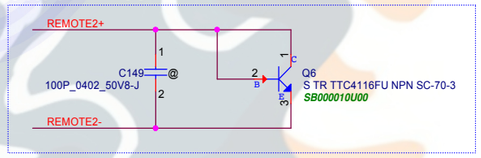
Close to U1

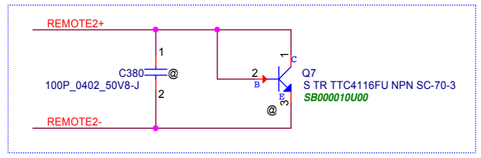


Close to +VCC_CORE



Close JDIMM1&JDIMM2





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: *Thermal Sensor*

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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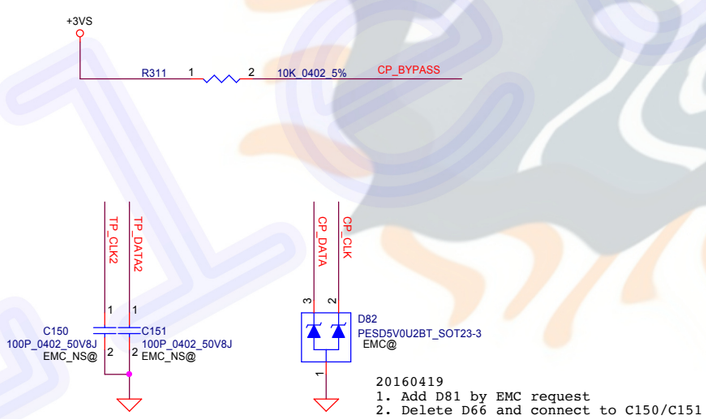
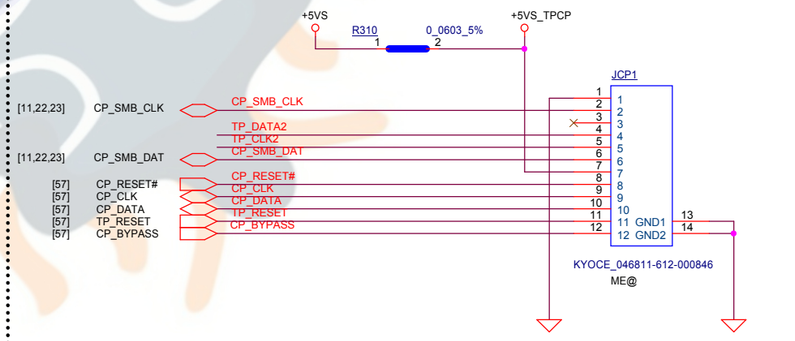
Track point



20160419
1. Add D81 by EMC request
2. Delete D66 and connect to C150/C151

Click Pad



20160417
Change JCP1 to KYOCE_046811-612-000846

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: CP/TPOINTCONN.

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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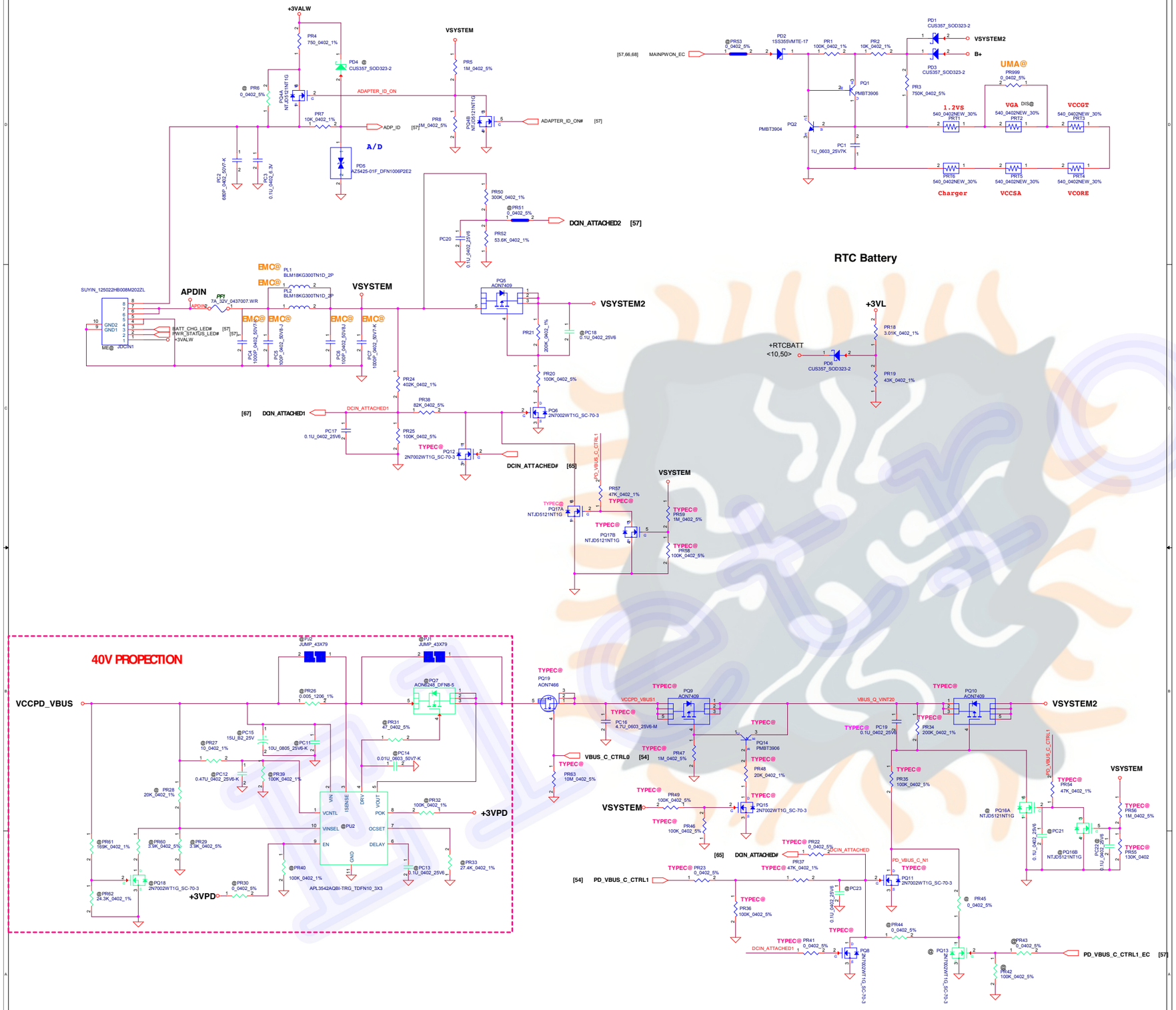

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

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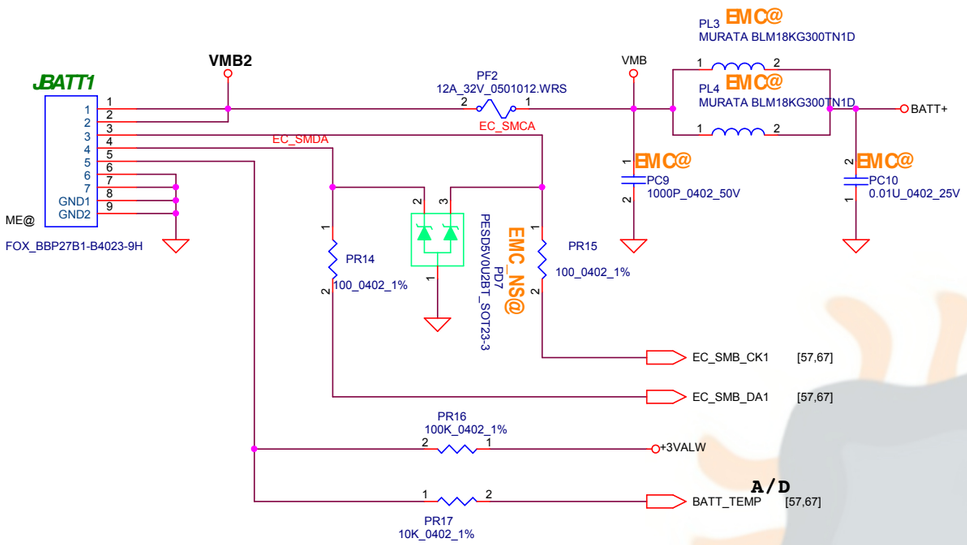
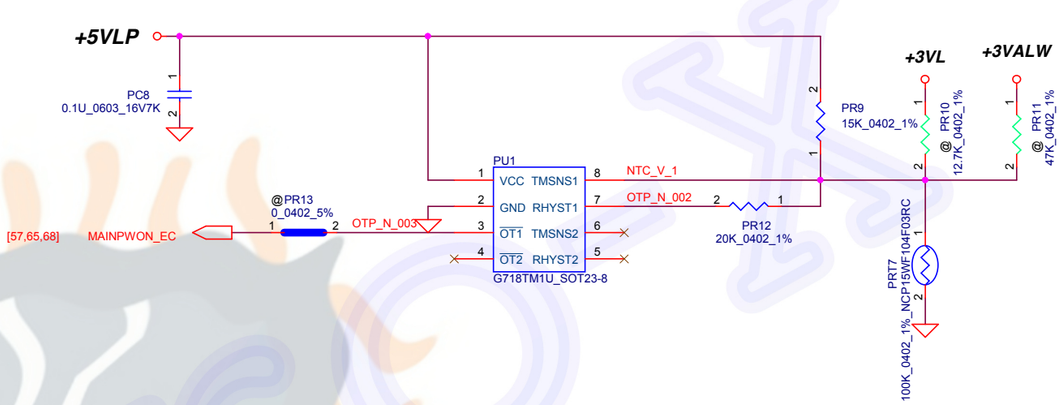
Title: *DCIN / VIN Detector*

Size: Custom | Document Number: **KENOBI** | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 65 of 82



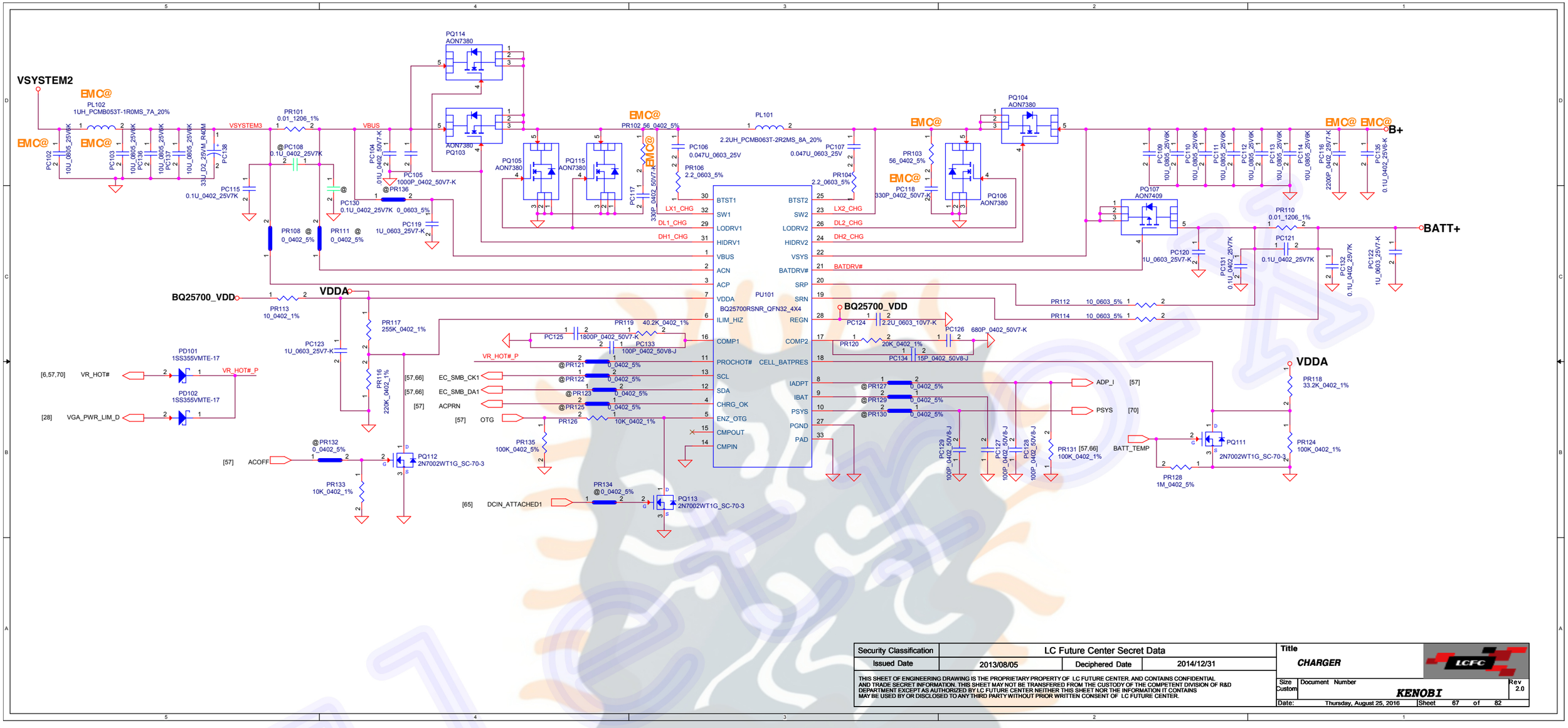
PRT7 under CPU bottom side for CPU thermal protection
This is fot thermal team request



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: ***BATTERY CONN/OTP***

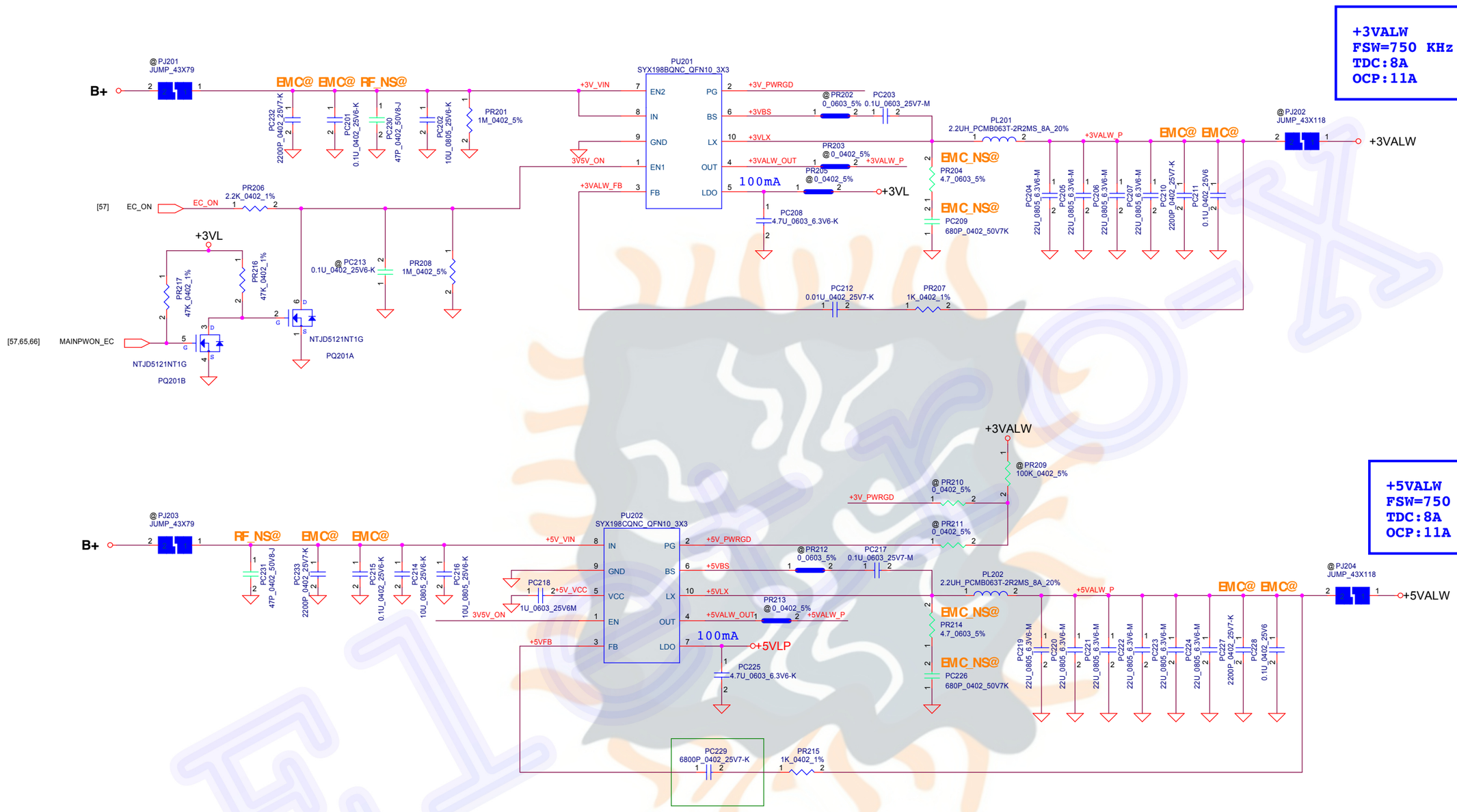
Size: Custom	Document Number: ***Skywalker***	Rev: 2.0
Date: Thursday, August 25, 2016	Sheet 66 of 83	



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: CHARGER

Size: Custom	Document Number: KENOBI	Rev: 2.0
Date: Thursday, August 25, 2016	Sheet 67 of 82	



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	Skywalker	2.0

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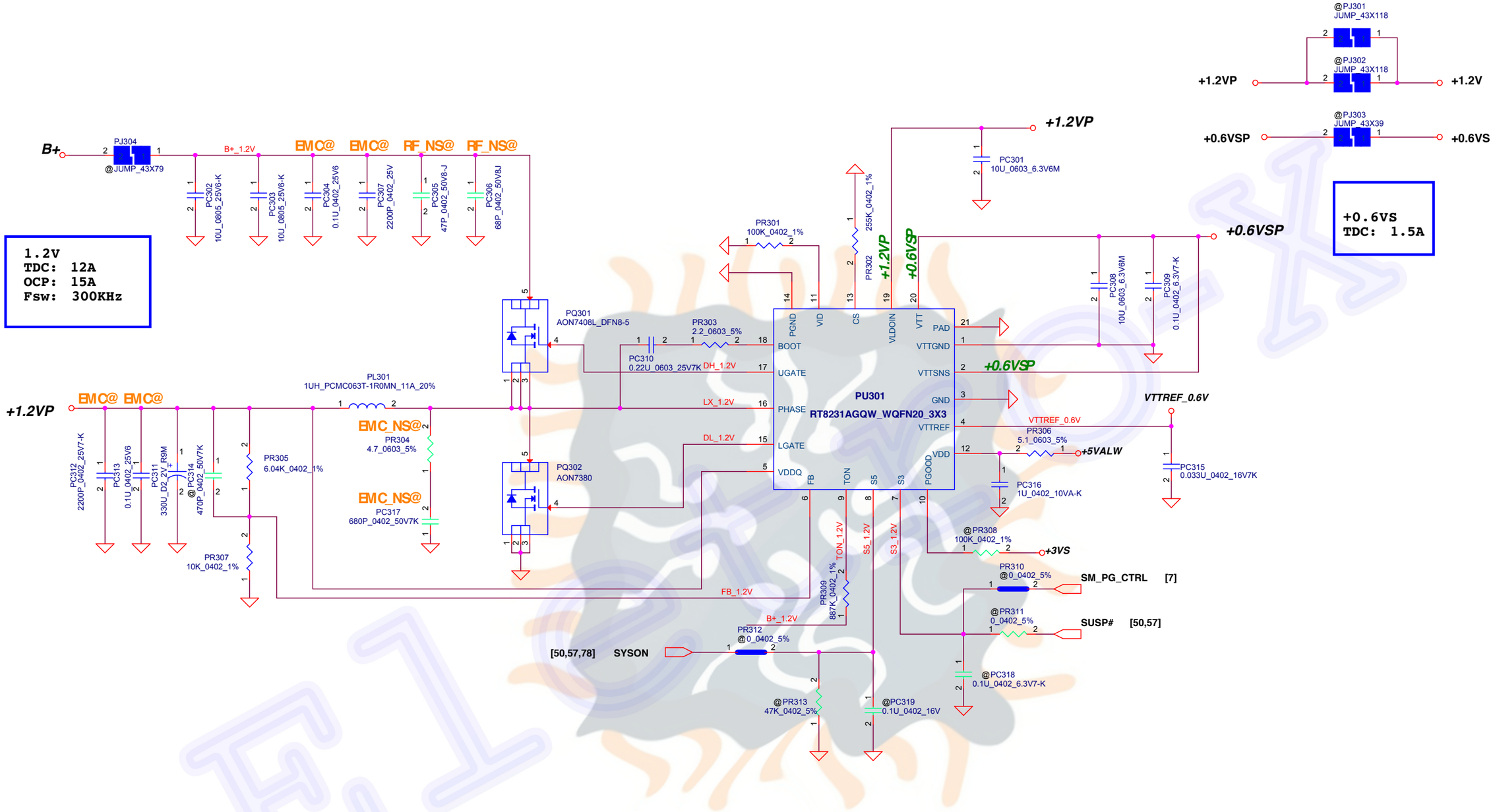
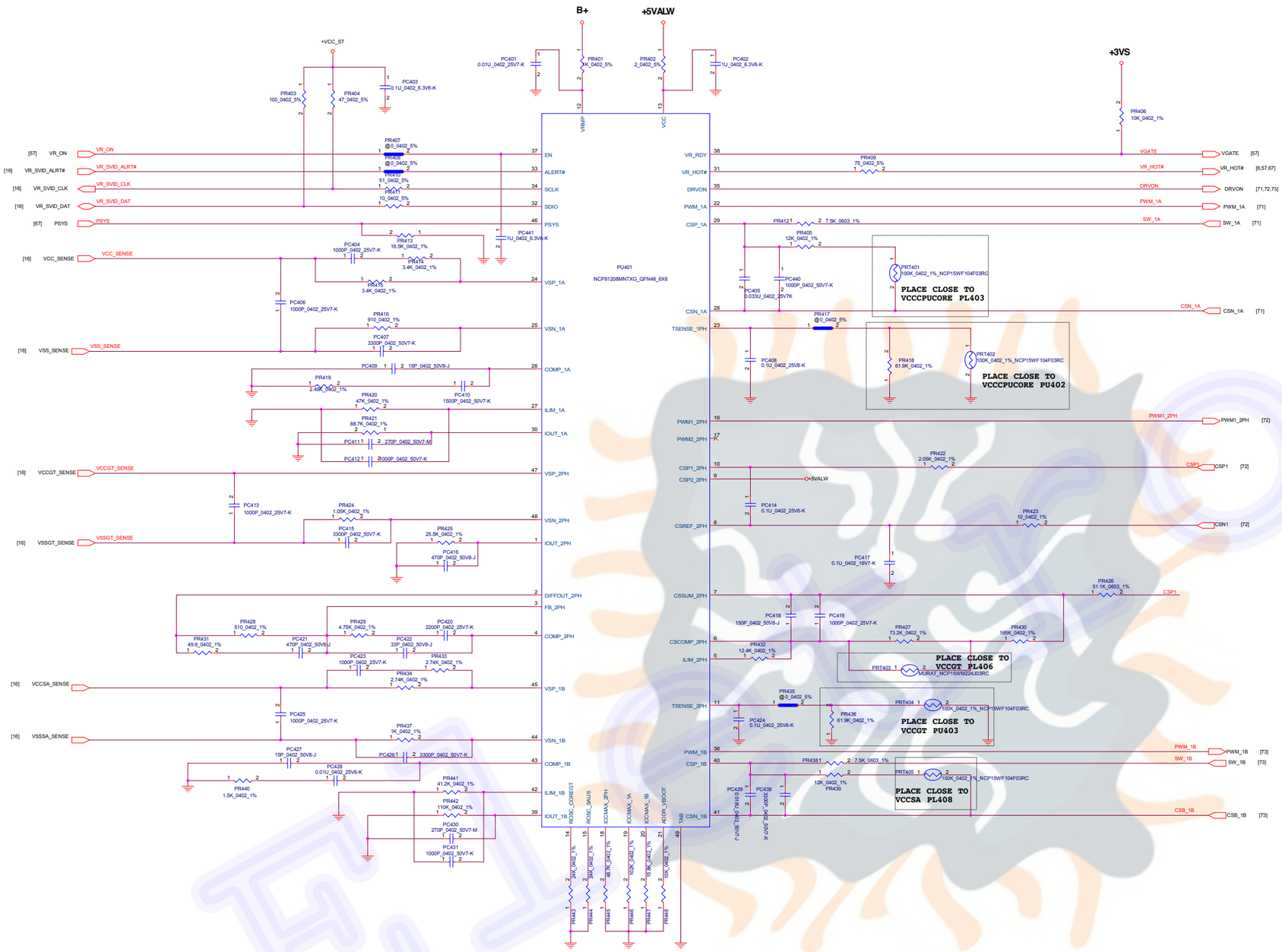


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.2V/+0.6VS

Size: Custom | Document Number: Skywalker | Rev: 1.0

Date: Thursday, August 25, 2016 | Sheet 69 of 88



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

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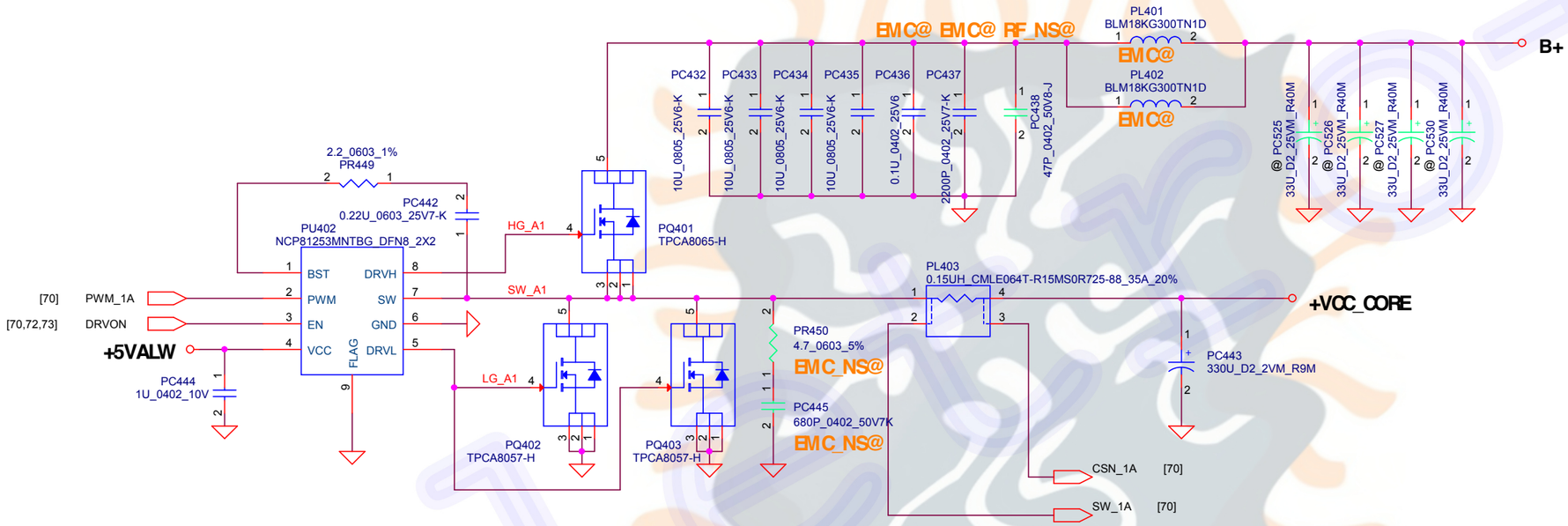
Title	IMVP8		
Size	Document Number		Rev
D	Skywalker		2.0
Date:	Thursday, August 28, 2014	Sheet	70 of 83



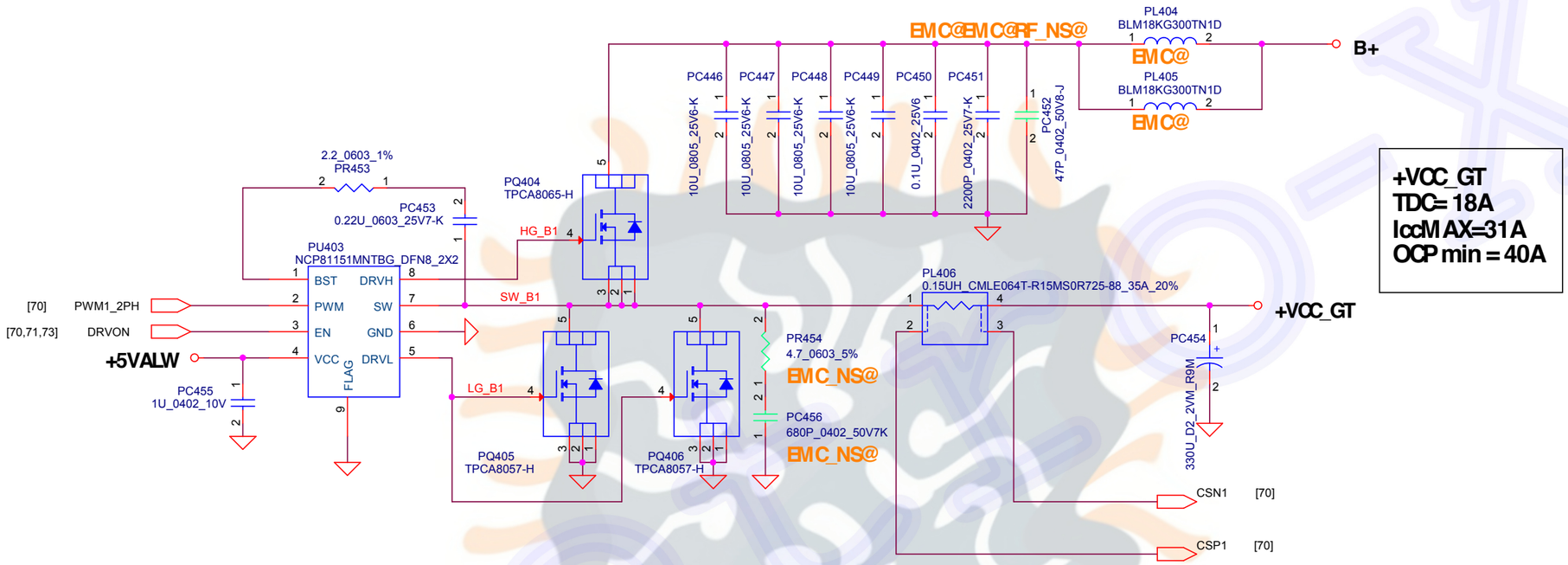
+VCC_CORE
TDC=21A
IccMAX=31A
OCP=36A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_CORE

Size	Document Number	Rev
Custom	Skywalker	2.0

Date: Thursday, August 25, 2016 Sheet 71 of 83



+VCC_GT
TDC= 18A
IccMAX=31A
OCP min = 40A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_GT*

Size	Document Number	Rev
Custom	*Skywalker*	2.0

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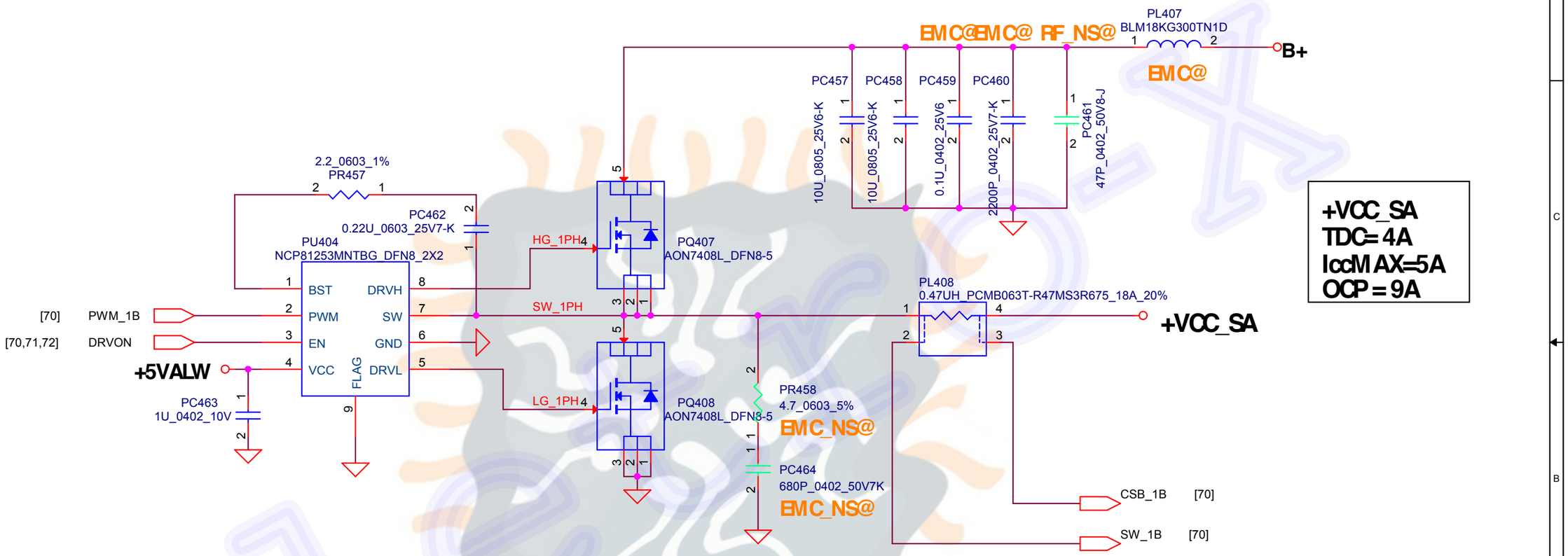

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+VCC_SA		
Size: Custom	Document Number: Skywalker		Rev: 2.0
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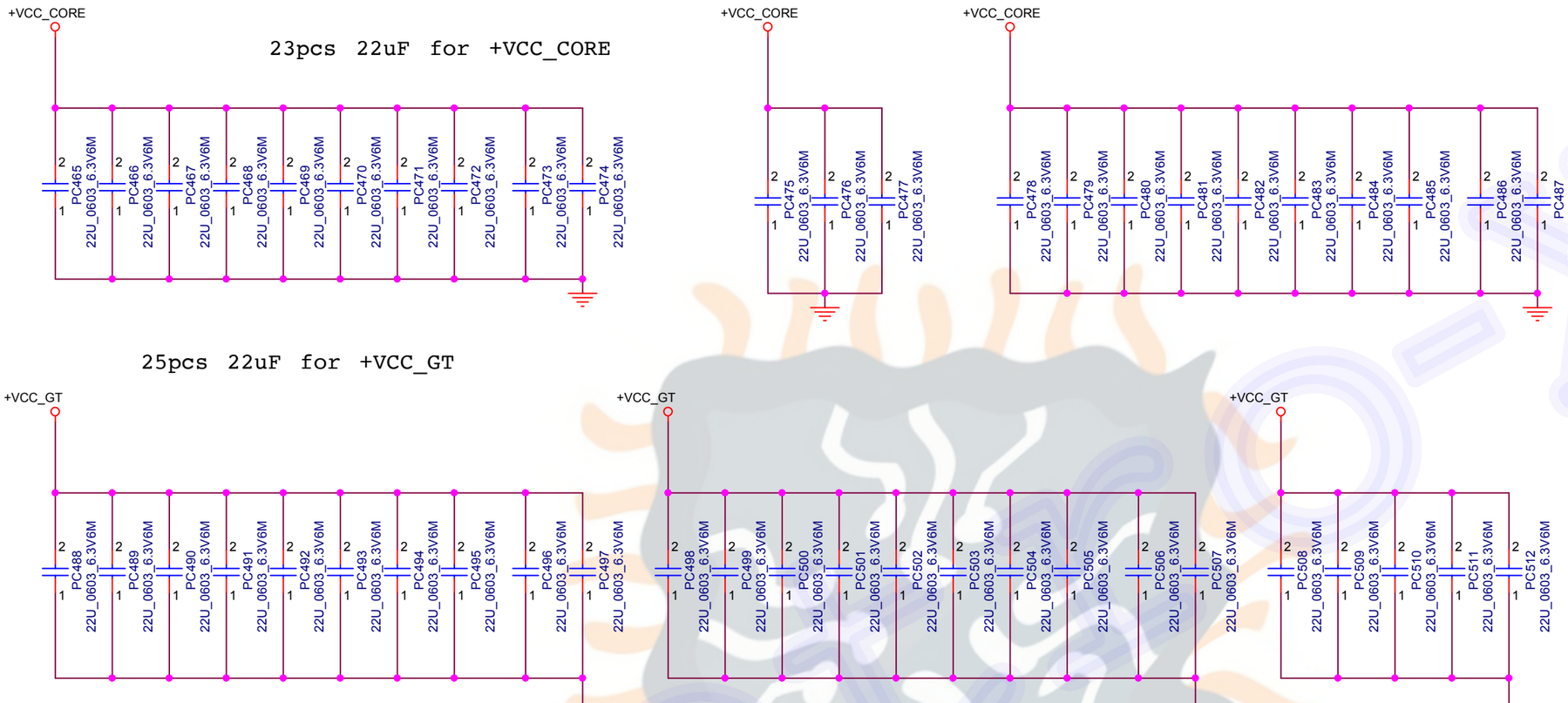
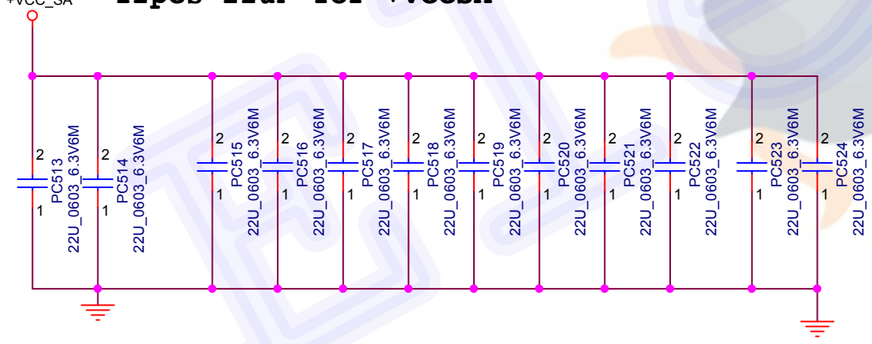
Based on PDDG rev 0.7 Table 5-1.

23pcs 22uF for +VCC_CORE



25pcs 22uF for +VCC_GT

12pcs 22uF for +VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
B	Skywalker	2.0

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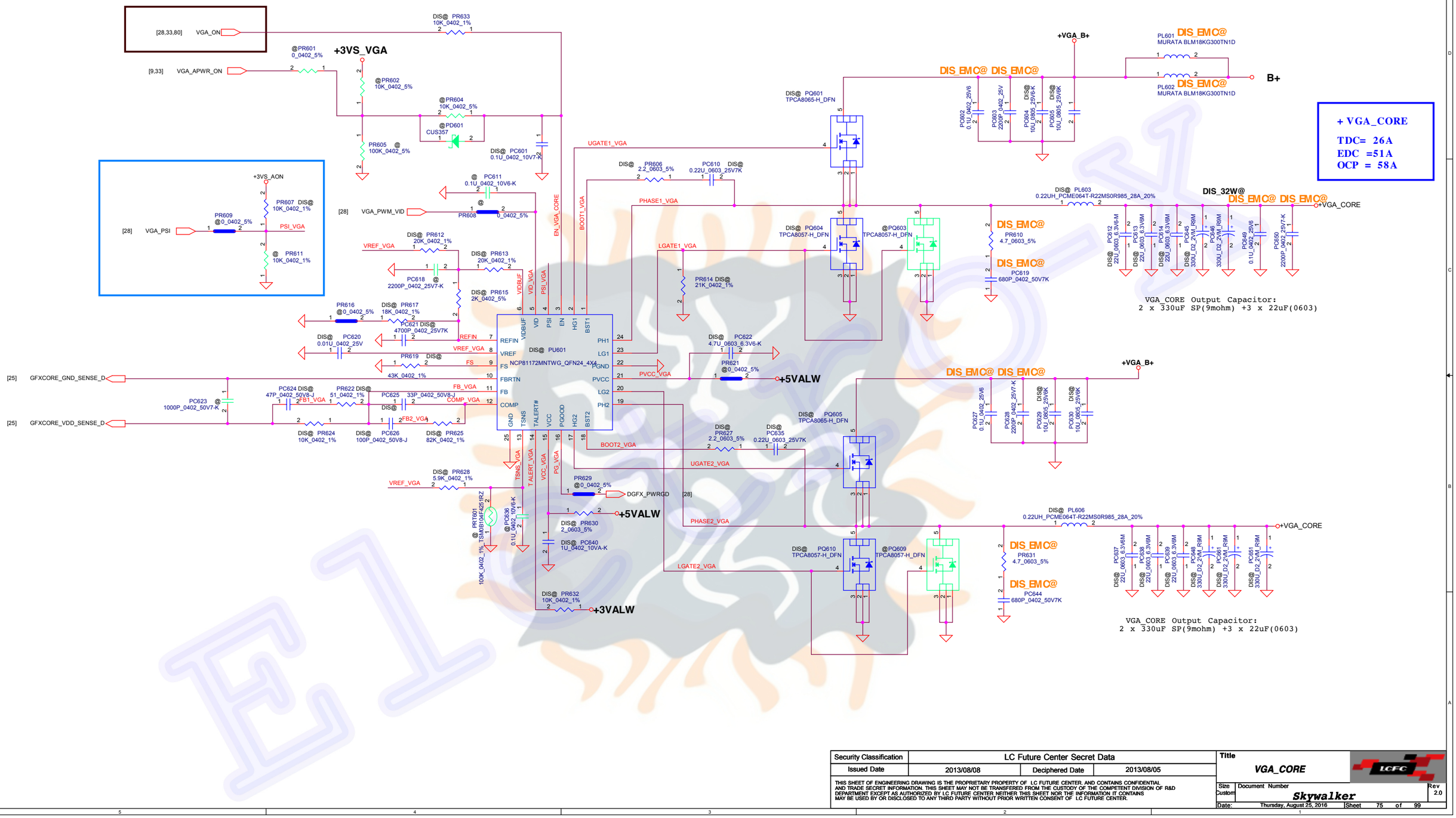
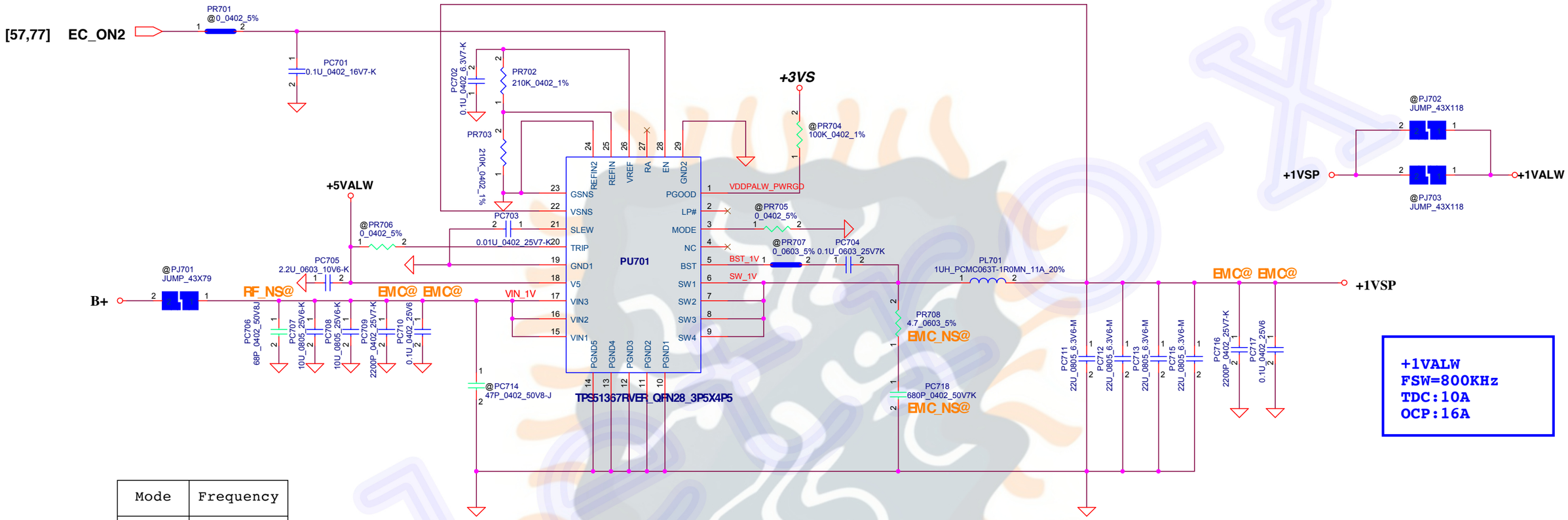


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	VGA_CORE		
Size	Document Number		Rev
Custom	Skywalker		2.0
Date:	Thursday, August 25, 2016	Sheet	75 of 99

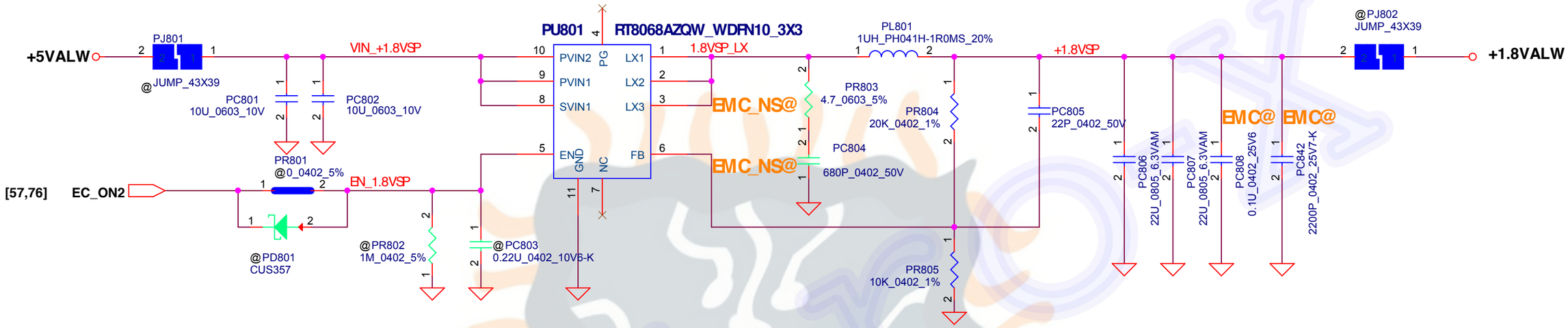


Mode	Frequency
GND	400KHz
Float	800KHz

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/08/01

Title	+1VALW		
Size	Custom	Document Number	Skywalker
Rev	2.0		
Date:	Thursday, August 25, 2016	Sheet	76 of 83

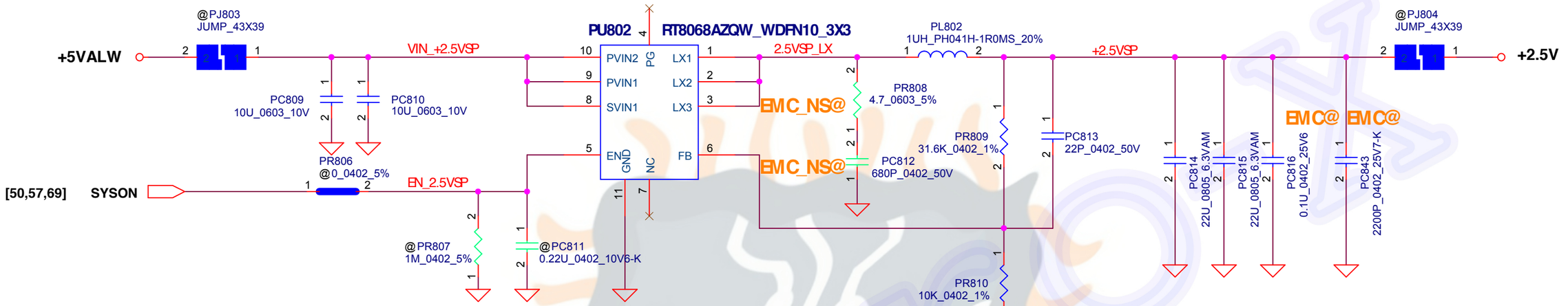
+1.8VALW
TDC: 1A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.8VALW		
Size	Document Number		Rev
Custom	Skywalker		2.0
Date:	Thursday, August 25, 2016	Sheet 77 of 83	

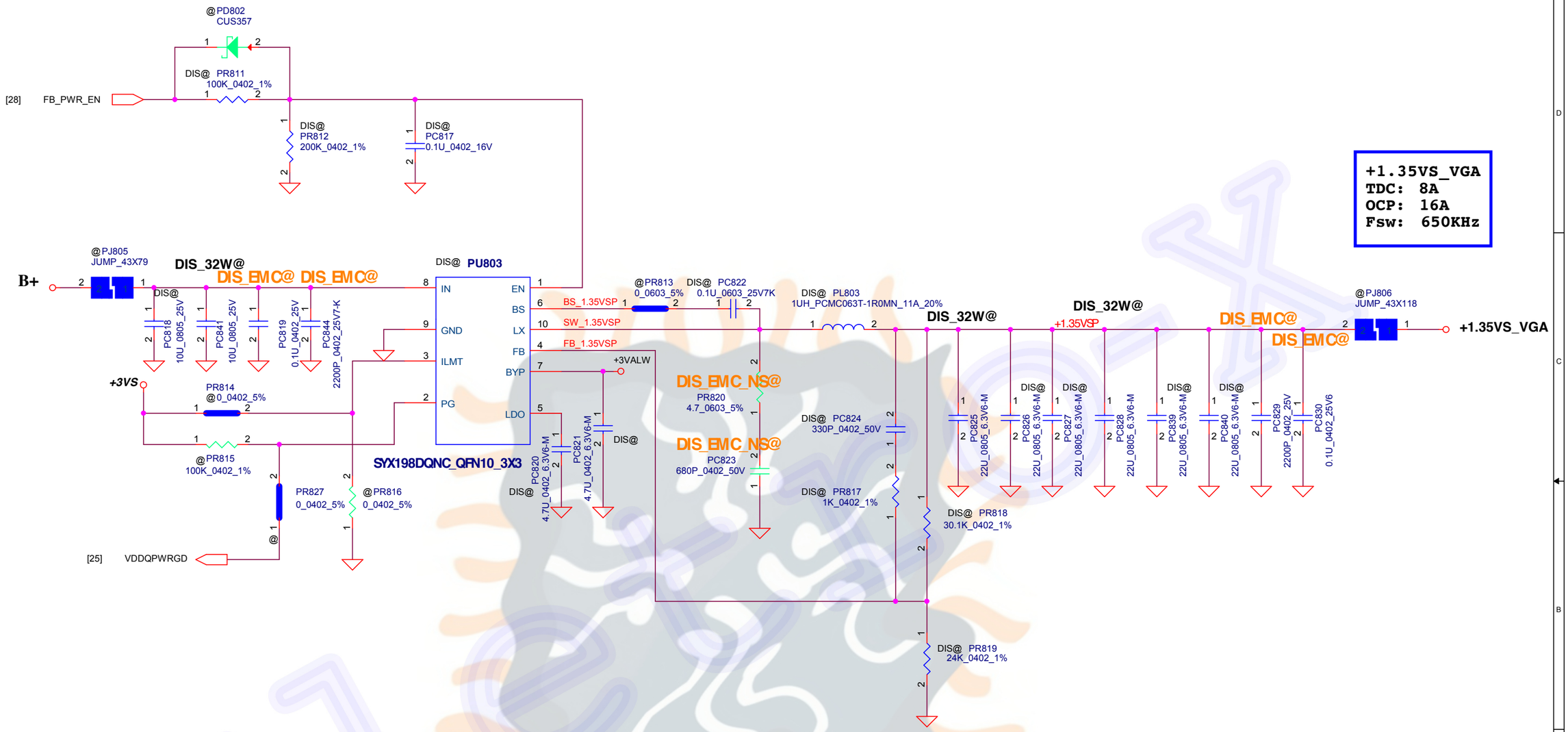
+2.5V
TDC: 2A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

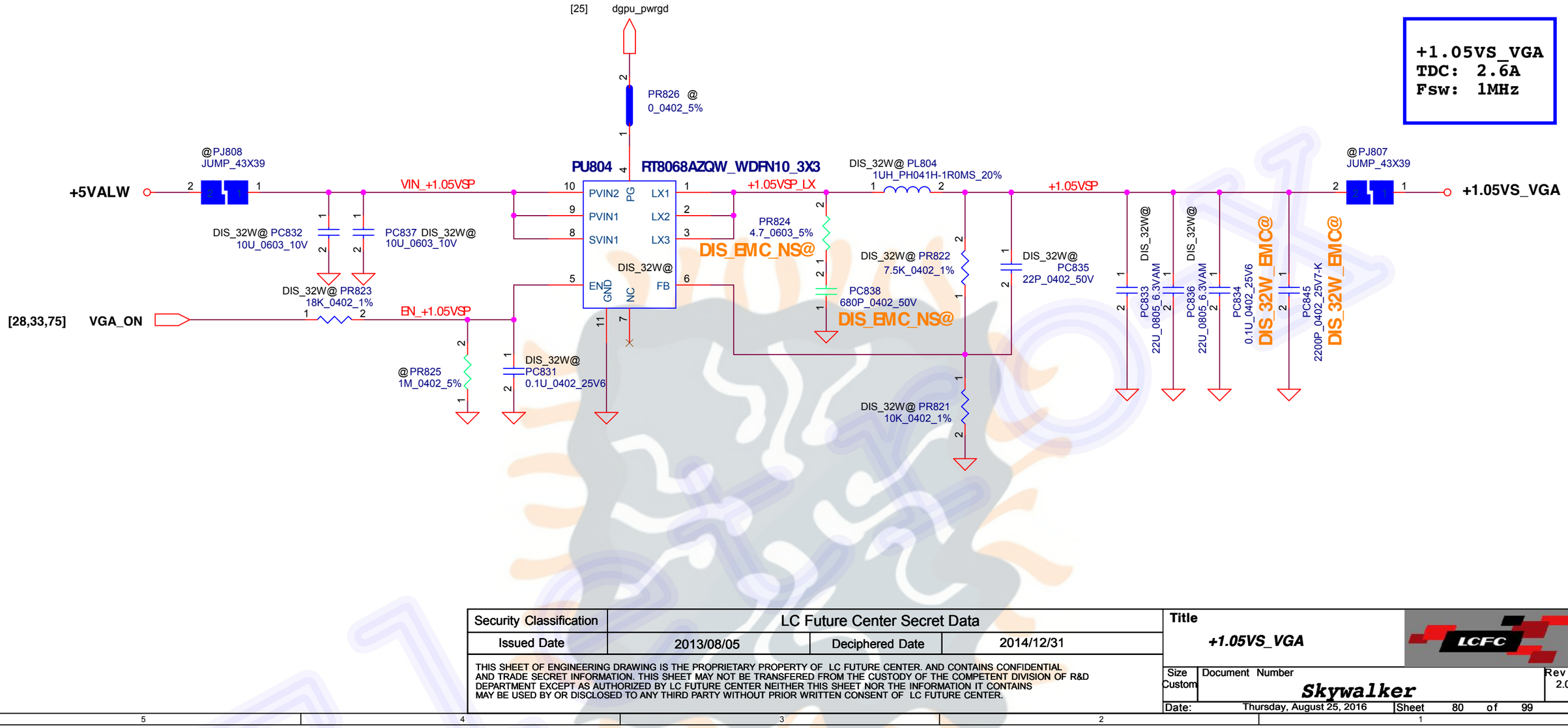
Title: +2.5V

Size: Custom	Document Number: Skywalker	Rev: 2.0
Date: Thursday, August 25, 2016	Sheet 78 of 83	



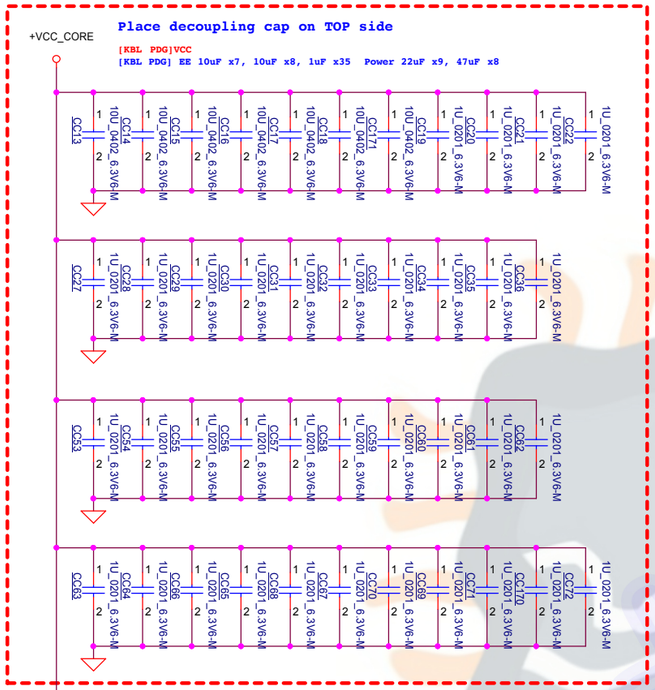
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

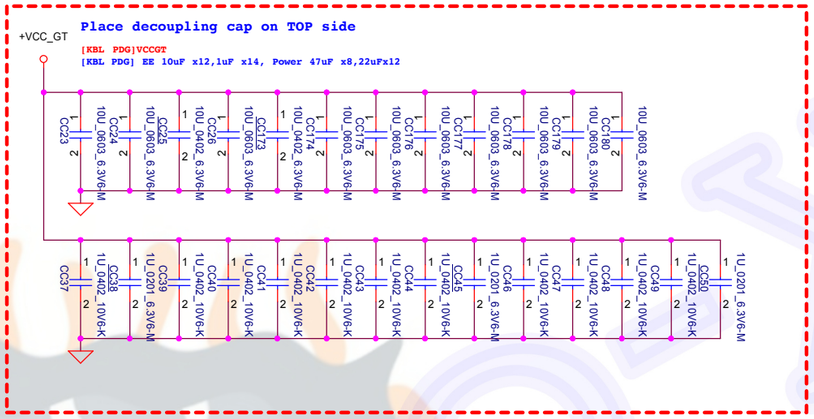
Title	+1.35VS_VGA		
Size	Custom	Document Number	Skywalker
Rev	2.0		
Date:	Thursday, August 25, 2016	Sheet	79 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.05VS_VGA		
Size: Custom	Document Number: Skywalker		Rev: 2.0
Date: Thursday, August 25, 2016	Sheet 80 of 99		





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(9/16):Decoupling

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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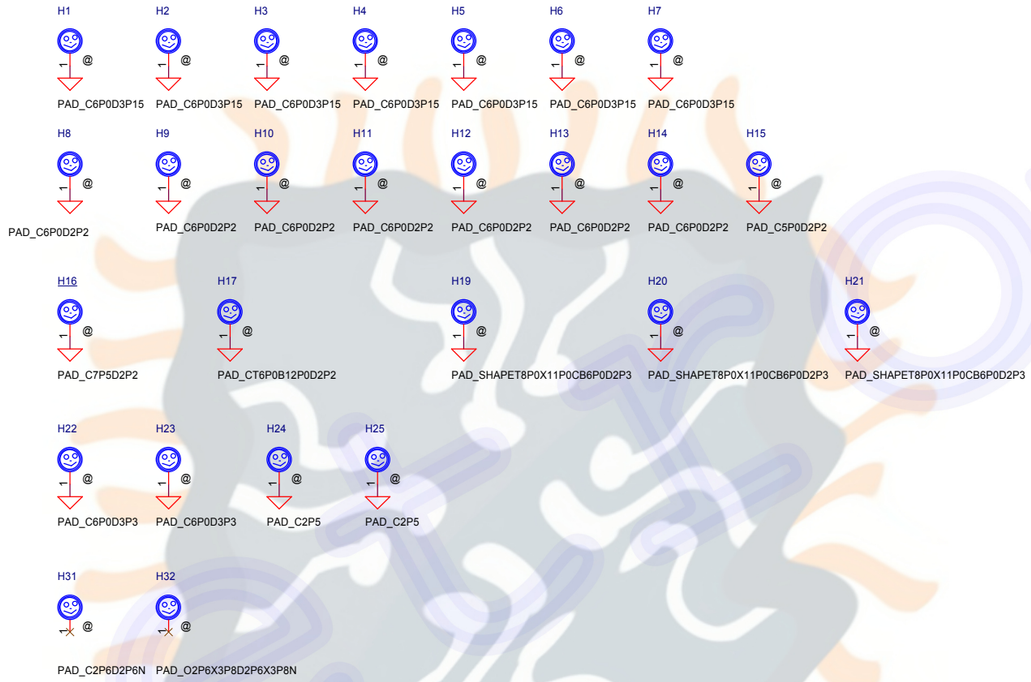
Screw Hole



Center Zero

PCB Fedical Mark PAD

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: P68-PLM/SCREW HOLE

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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