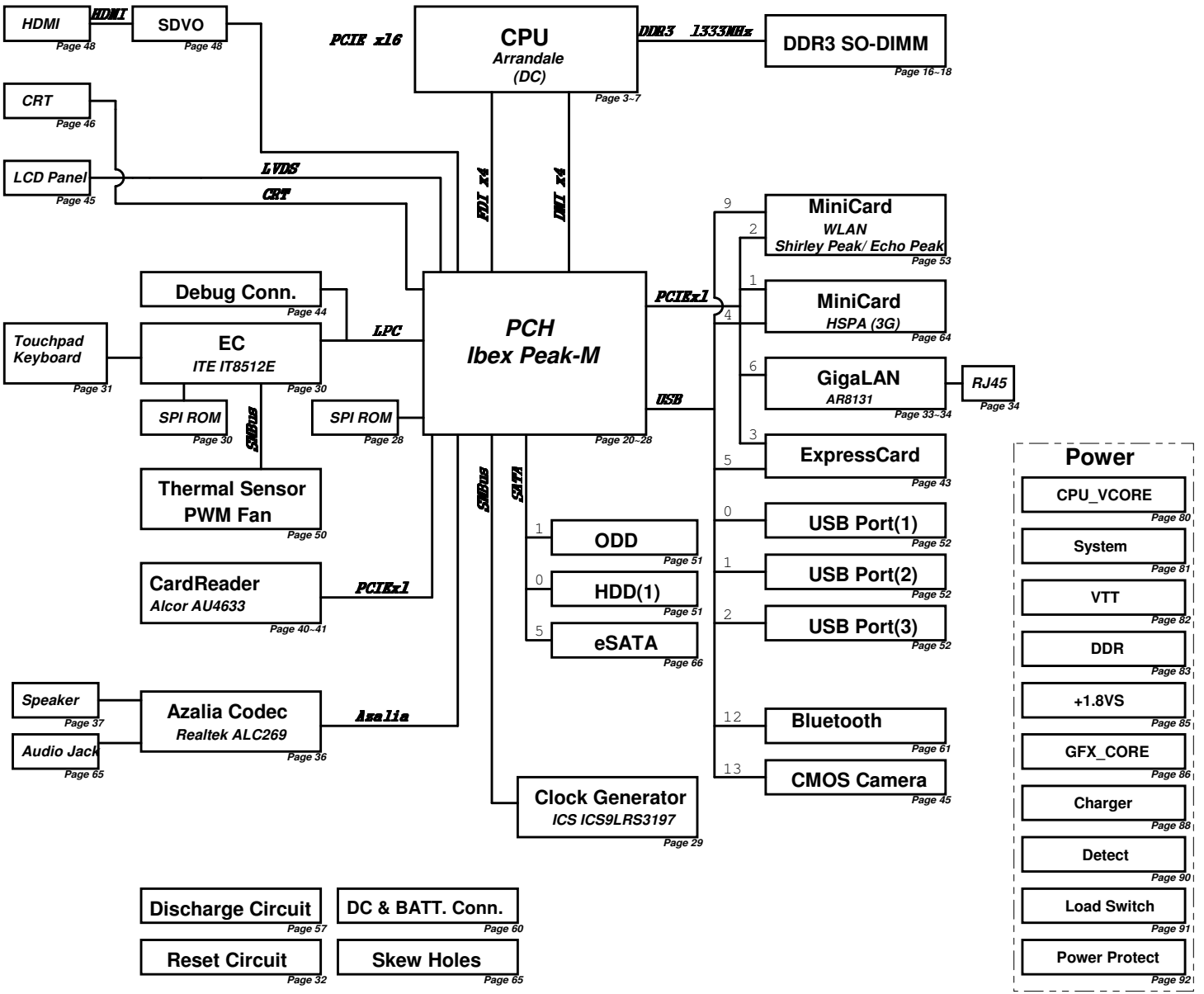
SYSTEM PAGE REF.

H36Y Schematics for Calpella Platform Rev. 2.2

BLOCK DIAGRAM



PEGATRON Title : Block Diagram

BG1VHW1 Engineer: Kuansheng Yang

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 1 of 99

PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	-	GPIO0	-	+3VS
GPIO 01	-	DOCKING_DET#	EXT PU	+3VS
GPIO [2:5]	Native	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	-	DGPU_PWR_EN	EXT PU	+3VS
GPIO 07	-	XIDE_BAY_IN#	EXT PU	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	-	PM_LANPHY_EN	EXT PU	+3VSUS
GPIO 13	-	DGPU_PWR_EN_R	-	+3VSUS
GPIO 14	Native	USB_OC7#	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	-	DGPU_HOLD_RST#	-	+3VS
GPIO 17	-	DGPU_PWR_OK	EXT PD & INT TBD	+3VS
GPIO 18	-	CLK_REQ1#	EXT PU(DNI)/PD	+3VS
GPIO 19	Native	SATA1GP	-	+3VS
GPIO 20	Native	CLKREQ2_WLAN#	EXT PU(DNI)/PD	+3VS
GPIO 21	Native	SATA0GP	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	-	LPC_DRQ#1	-	+3VS
GPIO 24	-	OC_LAN_RST#	EXT PU	+3VSUS
GPIO 25	Native	CLKREQ3_NEWCARD#	EXT PU(DNI)/PD	+3VSUS
GPIO 26	-	CLK_REQ4#	EXT PU(Not used)	+3VSUS
GPIO 27	-	VRM_EN	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_SUSPWRDNACK	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	Native	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	STP_PCI#	EXT PU	+3VS
GPIO 35	GPO	CAP_RST#_ICH	EXT PU/PD(DNI)	+3VS
GPIO 36	-	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	-	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5_LAN#	EXT PU (Not used)	+3VSUS
GPIO 45	-	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	-	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	-	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	-	EMAIL_LED	-	+3VS
GPIO 49	GPO	PCH_TEMP_ALERT#	-	+3VS
GPIO 50	-	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	-	PCI_GNT1#	INT PU	+3VS
GPIO 52	-	PCI_REQ2#	EXT PU	+5VS
GPIO 53	-	PCI_GNT2#	INT PU	+3VS
GPIO 54	-	PCI_REQ3#	INT PU	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#_R	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	-	RTLAN_DSM_EN	EXT PU	+3VSUS
GPIO 61	-	PM_SUS_STAT#	-	+3VSUS
GPIO 62	-	SUS_CLK	-	+3VSUS
GPIO 63	-	SLP_S5#	-	+3VSUS
GPIO 64	-	CLK_OUT0	INT TBD	+3VS
GPIO 65	-	CLK_OUT1	INT TBD	+3VS
GPIO 66	-	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_USB48_CR	INT TBD	+3VS
GPIO 72	-	PM_BATLOW#	EXT PU (Not used)	+3VSUS
GPIO 73	-	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	-	SML1ALERT#	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DAT	EXT PU	+3VSUS

EC IT8512

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		-
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN_PWM
GPA6		-
GPA7		-
GPB0		-
GPB1		-
GPB2		-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0		-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		-
GPE0	O	VSUS_ON
GPE1	O	SUSC_EC#
GPE2	O	SUSB_EC#
GPE3	O	CPU_VRON
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPF0		-
GPF1		-
GPF2		-
GPF3	I	DISTP#
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	ME_AC_PRESENT
GPG0	O	KB_ID0
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	I	3G_ON
GPH2	O	GFX_VR_ON
GPH3		-
GPH4		-
GPH5		-
GPH6	O	CAP_LED#
GPI0	I	PCH_TEMP_ALERT#
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	ME_PM_SLP_LAN#
GPI5		-
GPI6	I	ME_PM_SLP_M#
GPI7	I	ME_SUSPWRDNACK
GPJ0	O	CAP_RST#_EC
GPJ1	O	PM_PWROK
GPJ2	O	KB_ID1
GPJ3		-
GPJ4	O	TP_LED
GPJ5	I	GFX_VR

EC IT8301

EC GPIO	Use As	Signal Name
GPIO0		-
GPIO1		-
GPIO2		-
GPIO3		-
GPIO4		-
GPIO5		-
GPIO6		-
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		-
GPIO11		-
GPIO12		-
GPIO13		-
GPIO14		-
GPIO15		-
GPIO16		-
GPIO17		-
GPIO18		-
GPIO19		-
GPIO20		-
GPIO21		-
GPIO22		-
GPIO23		-
GPIO24		-
GPIO25		-
GPIO26		-
GPIO27		-
GPIO28		-
GPIO29		-
GPIO30		-
GPIO31		-
GPIO32		-
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		-
GPIO37		-

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2h)
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
CPU Thermal IC(G780)	1001100x (98h)
VGA Thermal IC(G781-1)	1001101x (9Ah)
VGA Thermal Sensor(NB9E-GE1)	1001111x (9Eh)
VID Controller ASM8272	0011011x (36h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	N/A
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	N/A
SATA5	eSATA

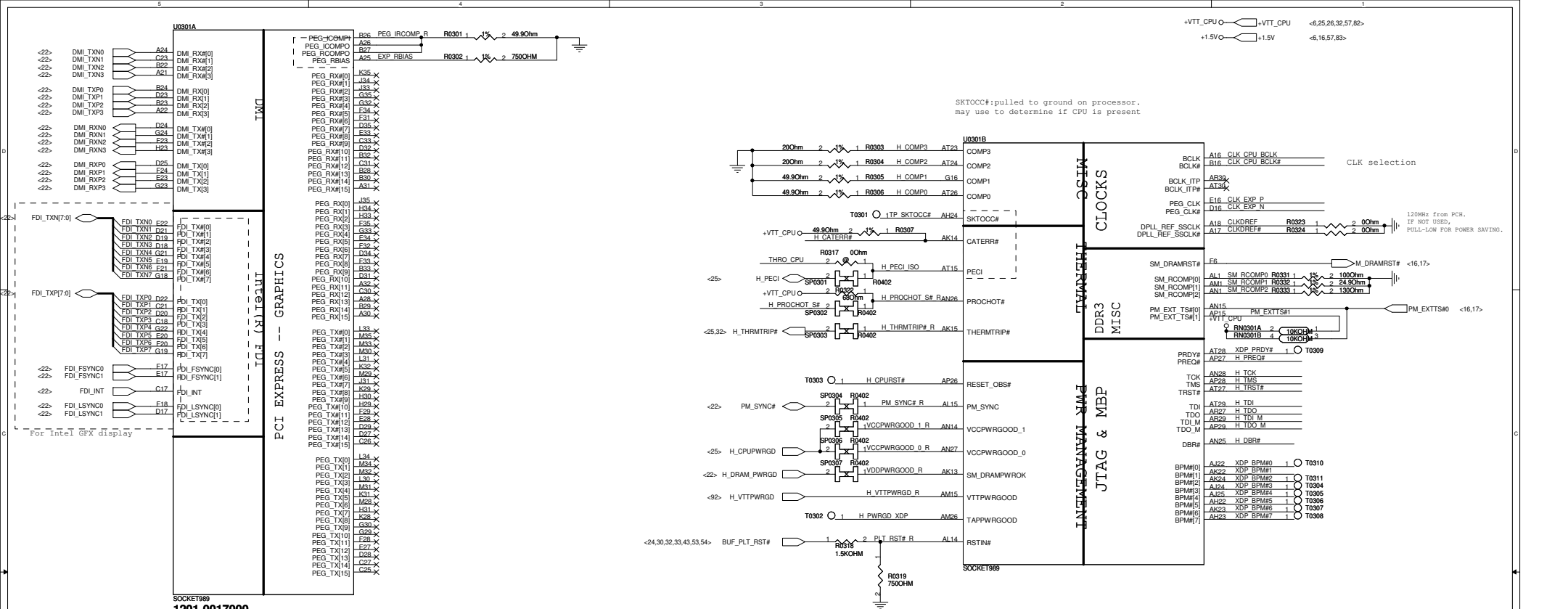
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	N/A
USB 4	N/A
USB 5	Newcard
USB 6	Card Reader
USB 7	3G
USB 8	N/A
USB 9	WLAN
USB 10	N/A
USB 11	N/A
USB 12	Bluetooth
USB 13	CMOS Camera

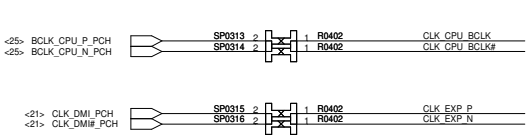
PEGATRON Title : System Setting

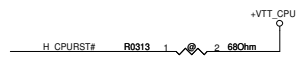
BG1VHW1 Engineer: *Kuansheng Yang*

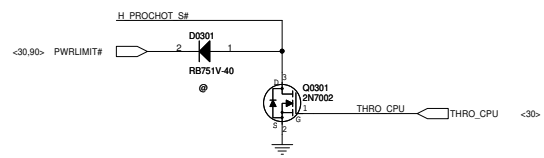
Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 2 of 99









FDI disable: (For discrete graphic)

1. NC:

FDI_TX#[0:7],FDI_TX[0:7],FDI_RX#[0:7],FDI_RX[0:7]

VCC_AXGSENSE,VSS_AXGSENSE

2. Pull-down to GND via 1KΩ ± 5% resistor:

FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON

~15mW power saving.(DG R0.8 P.70)

3. Connected to GND:

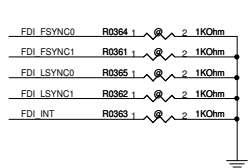
VCCAXG,DPLL_REF_CLK,DPLL_REF_CLK#

4. Can be connected to GND directly:

DPLL_REF_CLK,DPLL_REF_CLK#

5. Connect to +V1.05S rail:

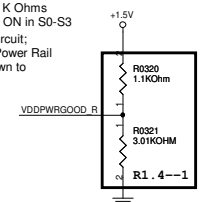
VCCFDIPLL



DRAMPWROK: (WW35 MoW)

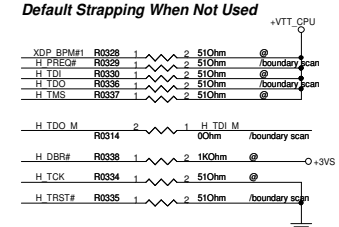
Choose either one solution: -->Choose solution 2

1. This pin should have an external pull-up of 1K Ohms to 10K Ohms to a rail of 1.05/1.1V which is ON in S0-S3
2. Connect this pin through a voltage divider circuit; recommend 4.75K Ohms pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12K Ohms pull-down to ground to convert to processor's VTT level.



WW14_2009_WOM

Default Strapping When Not Used



Adding layout test point
for boundary scan
Jervis 2009/11/09

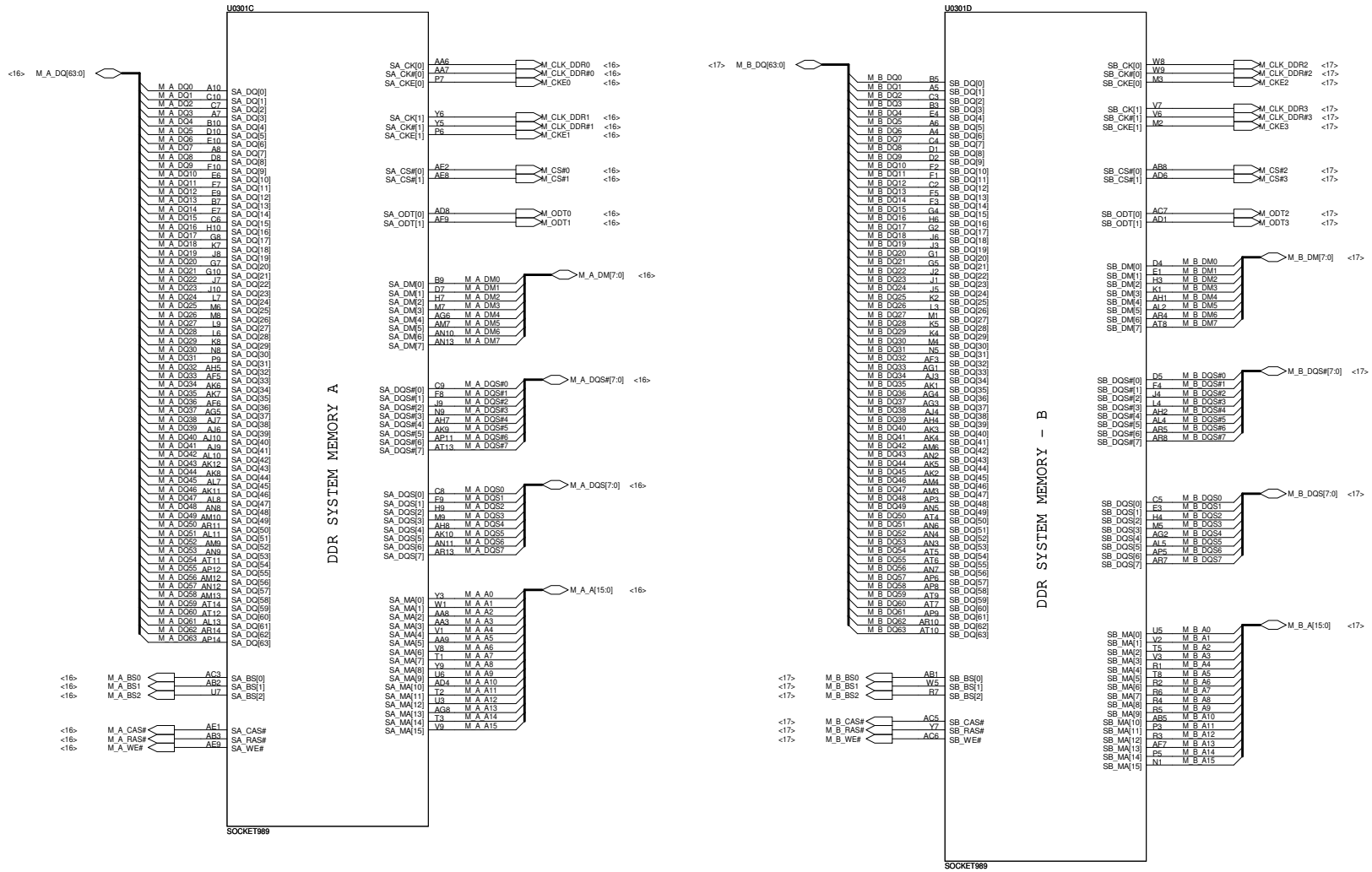
CLK_CPU_BCLK	1	T0312
H_VTTPWRGD_R	1	T0313
VCCPWRGOOD_0_R	1	T0314
VCCPWRGOOD_1_R	1	T0315
PLT_RST#_R	1	T0316
H_TRST#	1	T0317
H_TCK	1	T0318
H_TMS	1	T0319
H_TDI	1	T0320
H_TDO	1	T0321
H_TDI_M	1	T0322
H_TDO_M	1	T0323

PEGATRON Title : CPU(1)_DMI,PEG,FDI,CLK,MISC

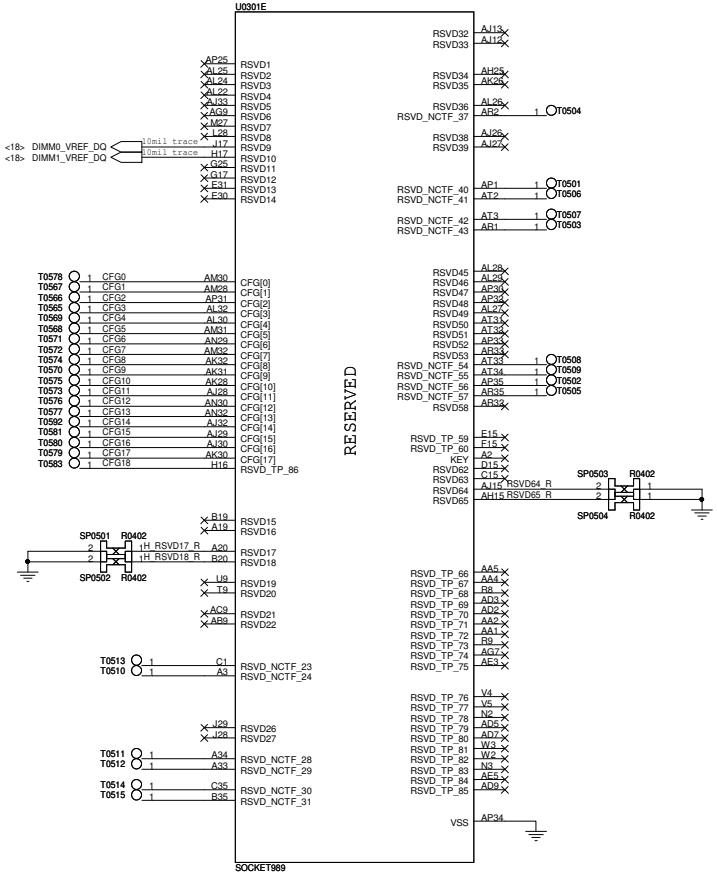
BG1\HW1 Engineer: *Kuansheng Yang*

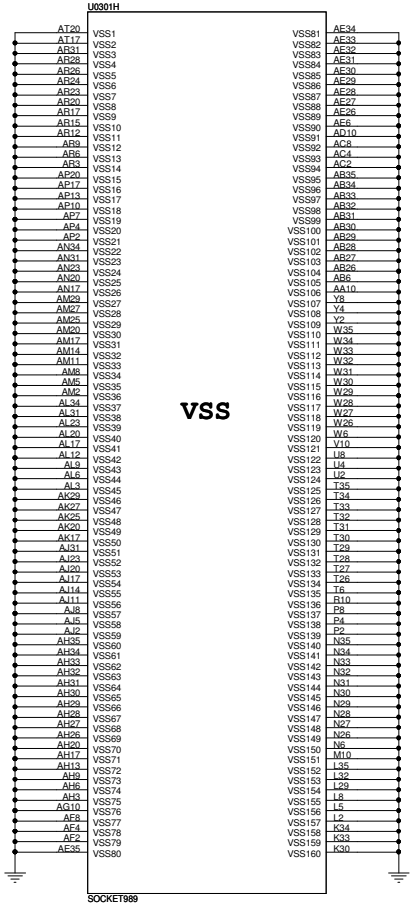
Size	Project Name	Rev
C	H36Y_U30X10	1.0

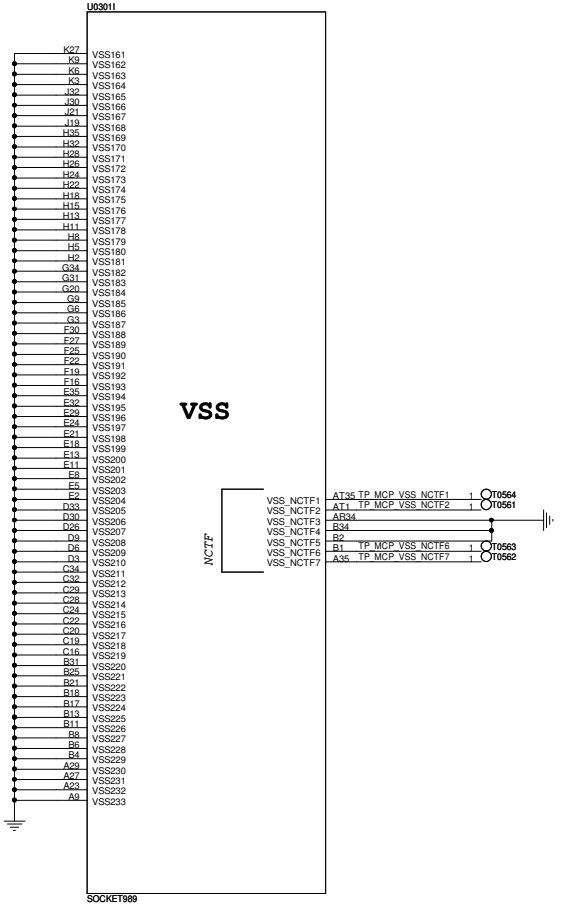
Date: Monday, May 10, 2010 Sheet 3 of 99



PEGATRON	Title : CPU(2)_DDR3		
BG1VHW1	Engineer: Kuansheng Yang		
Size: C	Project Name: H36Y_U30X10		Rev: 1.0
Date: Monday, May 10, 2010	Sheet 4 of 99		







CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal.(Auburndale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

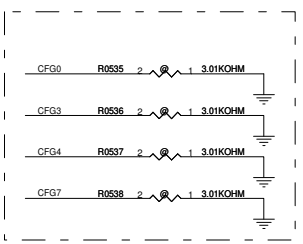
CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact AUB functionality.

Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.

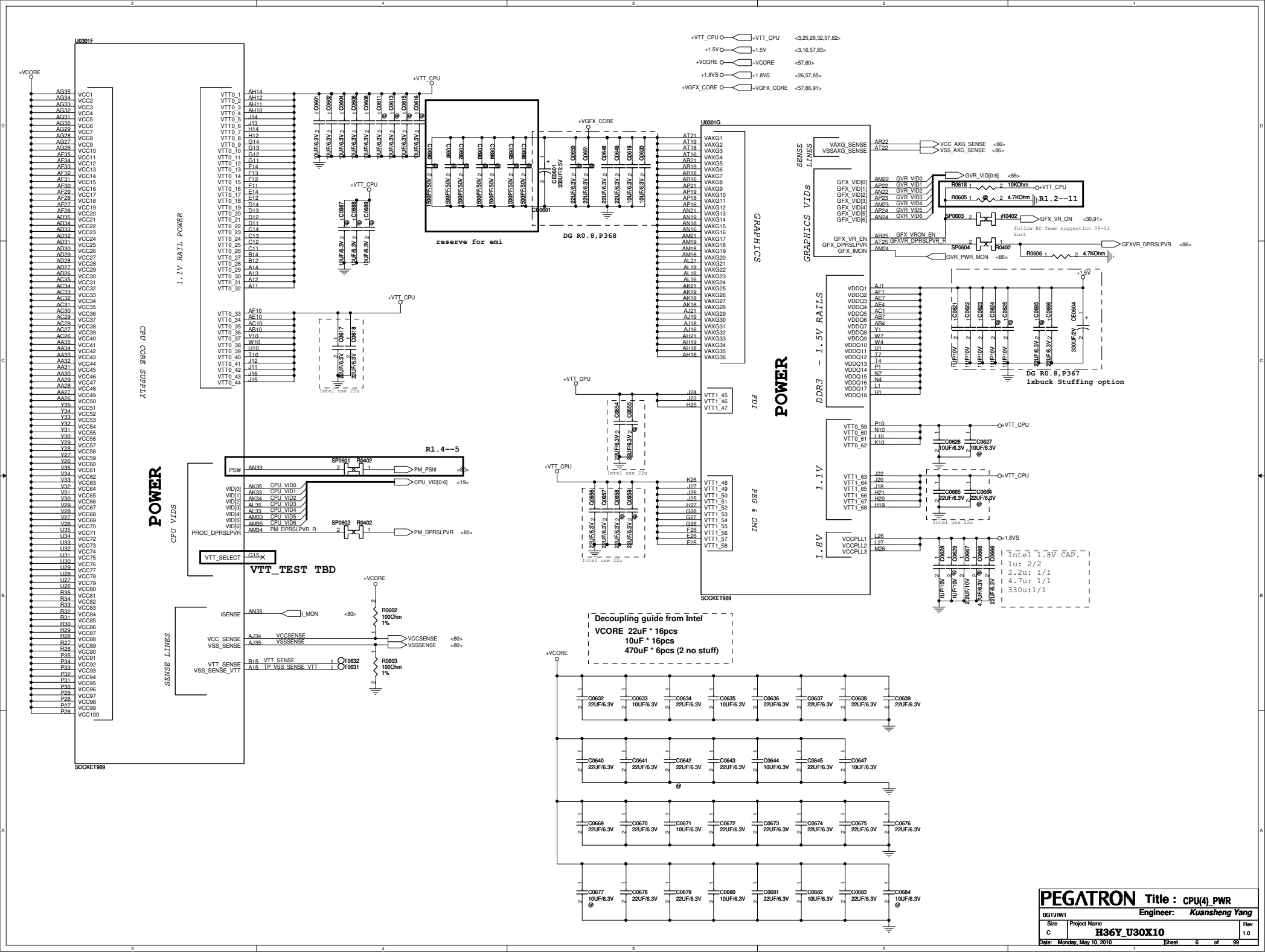


PEGATRON Title : CPU(3)_CFG,RSVD,GND

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 5 of 99



PEGATRON Title : CPU(4)_PWR

BG1VHW1 Engineer: Kuansheng Yang

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 6 of 99

PEGATRON	Title : CPU(5)_XDP		
BG1VHW1	Engineer: *Kuansheng Yang*		
Size: C	Project Name: H36Y_U30X10		Rev: 1.0
Date: Monday, May 10, 2010	Sheet 7 of 99		

PEGATRON	Title : NB(1)_****			
BG1\HW1	Engineer: *Kuansheng Yang*			
Size: Custom	Project Name: H36Y_U30X10			Rev: 1.0
Date: Monday, May 10, 2010	Sheet 8 of 99			

PEGATRON Title : NB(2)_****

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
Custom	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 9 of 99

PEGATRON Title : NB(3)_****

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
Custom	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 10 of 99

PEGATRON	Title : NB(4)_****			
BG1\HW1	Engineer: *Kuansheng Yang*			
Size: Custom	Project Name: H36Y_U30X10			Rev: 1.0
Date: Monday, May 10, 2010	Sheet 11 of 99			

PEGATRON	Title : NB(5)_****			
BG1\HW1	Engineer: *Kuansheng Yang*			
Size: Custom	Project Name: H36Y_U30X10			Rev: 1.0
Date: Monday, May 10, 2010	Sheet 12 of 99			

PEGATRON	Title : NB(6)_****	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: Custom	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 13 of 99	

PEGATRON	Title : NB(7)_****	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: A	Project Name: **H36Y_U30X10**	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 14 of 99	

PEGATRON

Title : NB(8)_****

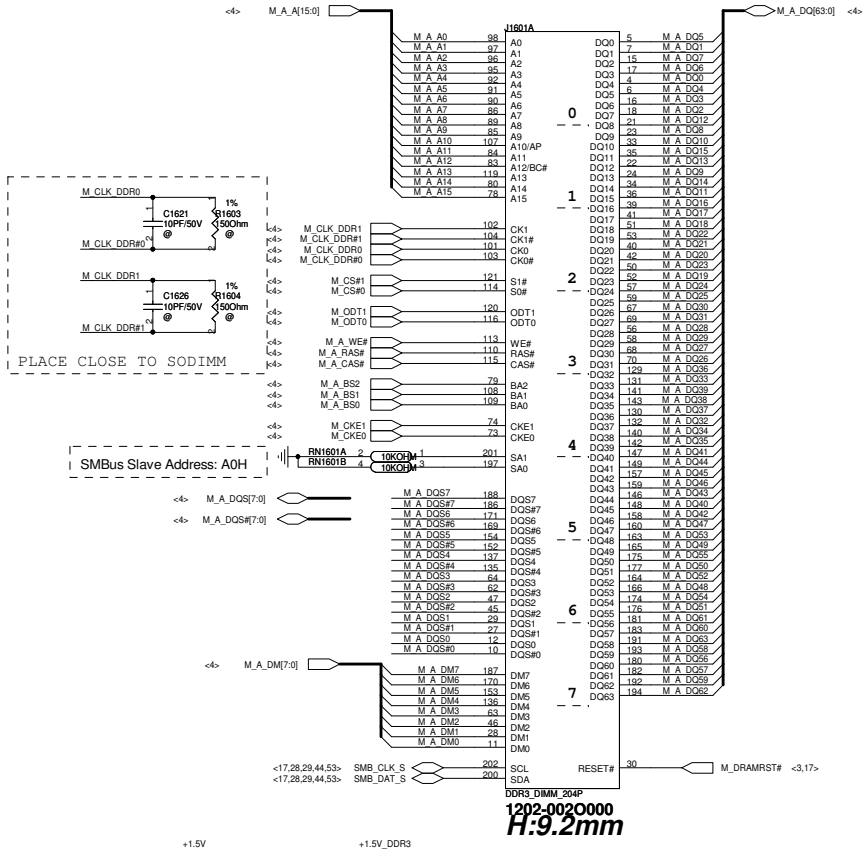
BG1\HW1

Engineer: *Kuansheng Yang*

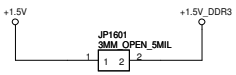
Size	Project Name	Rev
A	**H36Y_U30X10**	1.0

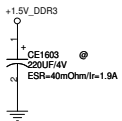
Date: Monday, May 10, 2010 Sheet 15 of 99

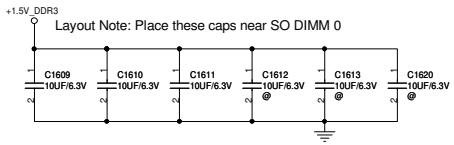
+1.5V <3,6,57,83>
+1.5V_DDR3 <17,18>
+0.75VS <17,57,83>
+3VS <3,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
M_VREFCA_DIMM0 <18>
M_VREFDQ_DIMM0 <18>

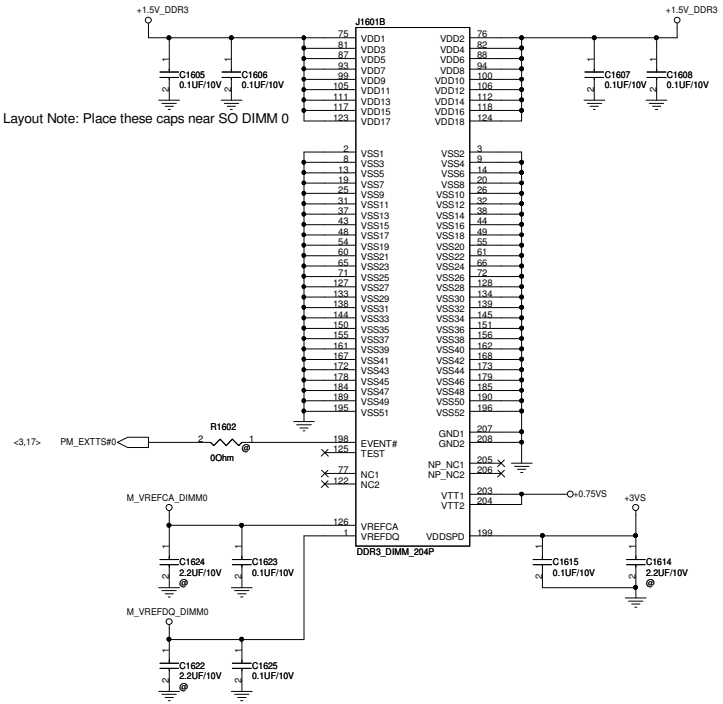


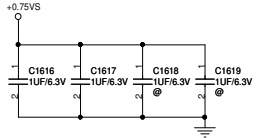
1202-002O000
H:9.2mm



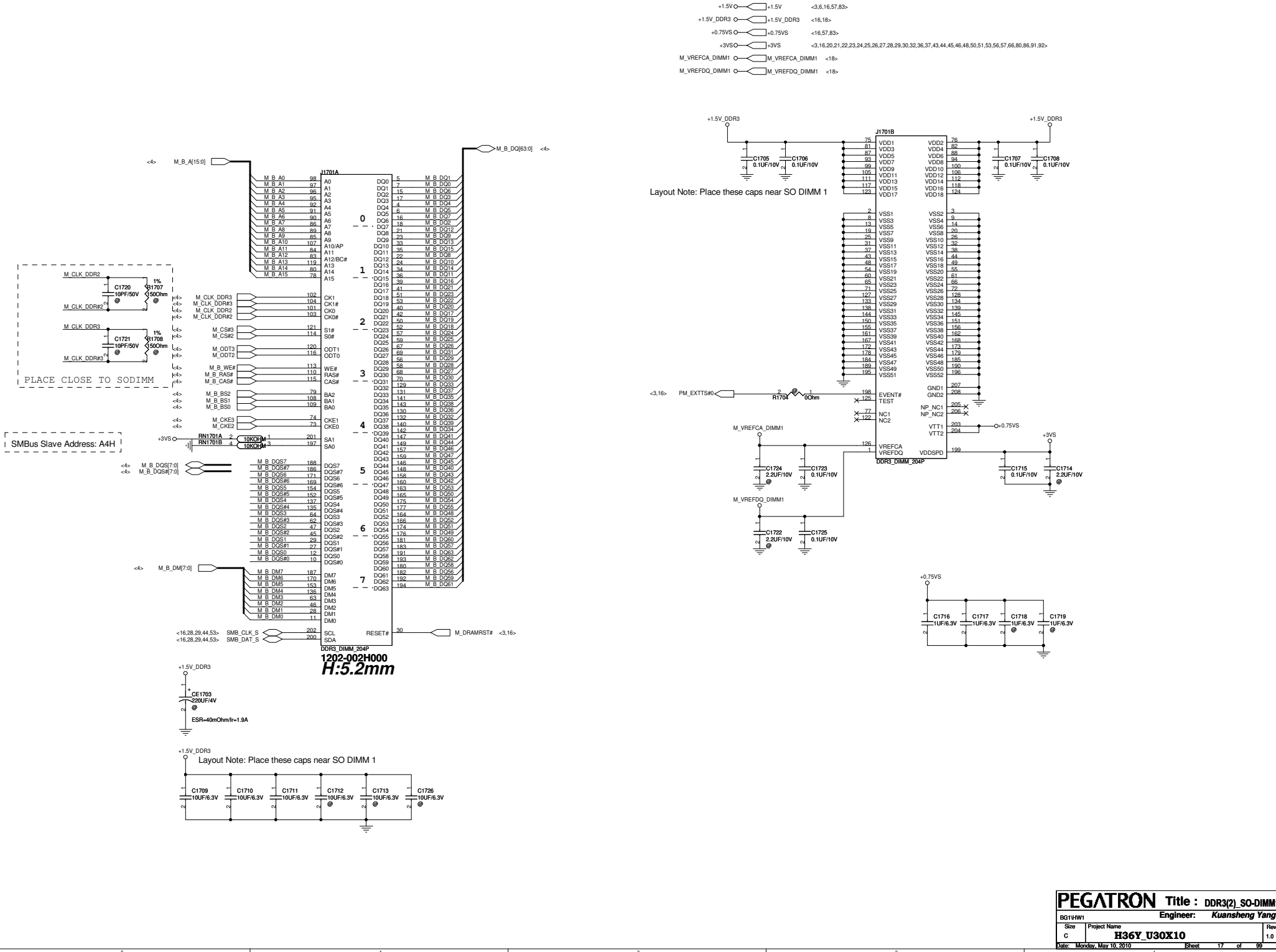








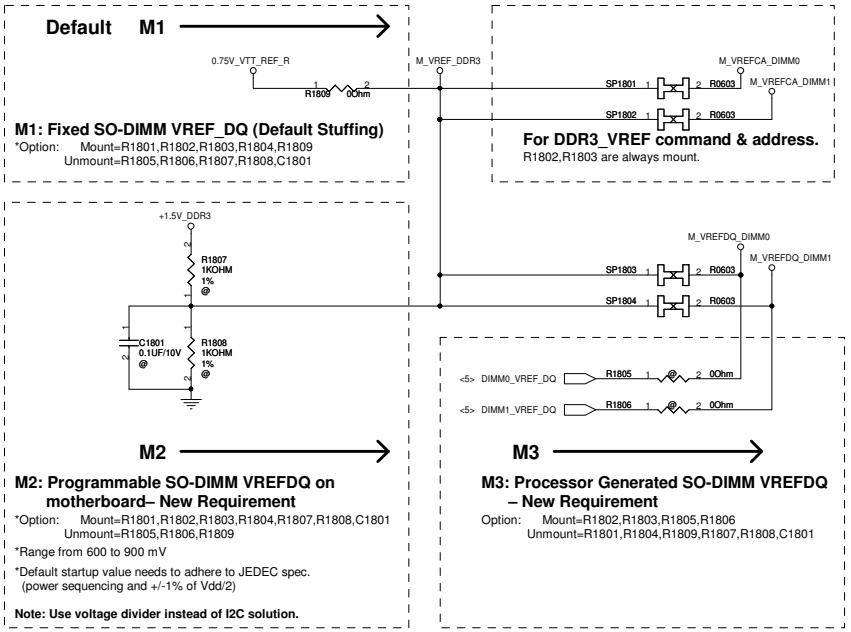
PEGATRON	Title : DDR3(1)_SO-DIMM0	
BG1VHW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 16 of 99	



PEGATRON	Title : DDR3(2)_SO-DIMM1	
BG1VHW1	Engineer: Kuansheng Yang	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 17 of 99	

DDR3 Vref

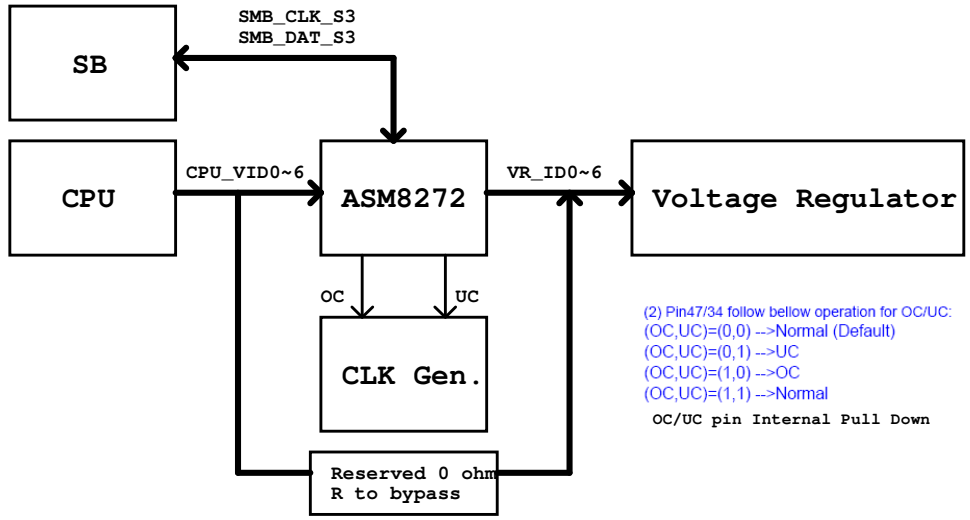
Intel Document Number: 400755
Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details



+1.5V_DDR3 — +1.5V_DDR3 <16,17>
M_VREFCA_DIMM0 — M_VREFCA_DIMM0 <16>
M_VREFDQ_DIMM0 — M_VREFDQ_DIMM0 <16>
M_VREFCA_DIMM1 — M_VREFCA_DIMM1 <17>
M_VREFDQ_DIMM1 — M_VREFDQ_DIMM1 <17>
+3V — +3V <24,33,40,43,45,53,54,56,57,61,91>
0.75V_VTT_REF_R — 0.75V_VTT_REF_R <83>

PEGATRON Title : DDR3(3)_CA/DQ Voltage
BG1\HW1 Engineer: *Kuansheng Yang*
Size C | Project Name H36Y_U30X10 | Rev 1.0
Date: Monday, May 10, 2010 Sheet 18 of 99

Block Diagram

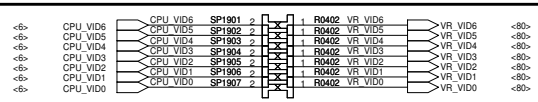


(2) Pin47/34 follow bellow operation for OC/UC:
(OC,UC)=(0,0) -->Normal (Default)
(OC,UC)=(0,1) -->UC
(OC,UC)=(1,0) -->OC
(OC,UC)=(1,1) -->Normal

OC/UC pin Internal Pull Down

+VTT_CPU ⟶ +VTT_CPU <3,6,25,26,32,57,82>

+3VS ⟶ +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>



R1.4--2

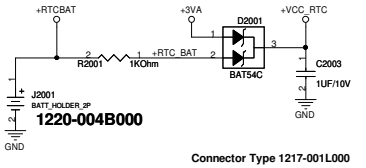
PEGATRON Title : VID Controller

BG1VHW1 Engineer: Kuansheng Yang

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 19 of 99

RTC battery



Connector Type 1217-001L000

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

RTCRST# RC delay should be 18ms~25ms

R2003 20KOhm, C2004 1UF/10V, JRST2001 SGL_JUMP@

R2004 20KOhm, R2005 1MOhm, C2005 1UF/10V, JRST2002 SGL_JUMP@

Adding layout test point for boundary scan Jervis 2009/11/09

HDA_SYNC: Select VCCVRM 1.5V or 1.8V

EDS 1.0: SATA port2,port3 may not be available in all PCH SKUs.

+1.05VS <26,27,29,57,80,82>
+VCC_RTC <27>
+3VS <3,16,17,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+1.05VM_ORG <27>
+VTT_PCH_VCCIO <26,27>
+3VM_SPI <28,44>

C2001 18PF/50V, C2002 18PF/50V, X2001 32.768Khz, R2002 10MOhm

R2006 330KOhm, R2020 1KOhm@

U2001A

X1_RTC	B13	RTCX1	RTC
X2_RTC	D13	RTCX2	
RTCRST#	C14	RTCRST#	
SRTCRST#	D17	SRTCRST#	
SM_INTRUDER#	A16	INTRUDER#	
SM_INTVRMEN	A14	INTVRMEN	
ACZ_BCLK	A30	HDA_BCLK	IHDA
ACZ_SYNC	D29	HDA_SYNC	
SB_SPKR	P1	SPKR	
ACZ_RST#	C30	HDA_RST#	
ACZ_SDIN0_AUD	G30	HDA_SDIN0	
	F30	HDA_SDIN1	
	F32	HDA_SDIN2	
	F32	HDA_SDIN3	
ACZ_SDOUT	B29	HDA_SDO	
HDA_DOCK_EN#	H32	HDA_DOCK_EN#/GPIO33	SATA
DGPU_PWR_EN_R	J30	HDA_DOCK_RST#/GPIO13	
PCH_JTAG_TCK_BUF	M3	JTAG_TCK	JTAG
	K3	JTAG_TMS	
	K1	JTAG_TDI	
	J2	JTAG_TDO	
	J4	TRST#	
SB_SPICLK	BA2	SPI_CLK	SPI
SB_SPICS0#	AV3	SPI_CS0#	
SB_SPICS1#	AY3	SPI_CS1#	
SPI_MOSI	AY1	SPI_MOSI	
SPI_SO	AV1	SPI_MISO	

IBEXPEAK-M

FWH0/LAD0	D33	LPC_AD0	<30,44>
FWH1/LAD1	B33	LPC_AD1	<30,44>
FWH2/LAD2	C32	LPC_AD2	<30,44>
FWH3/LAD3	A32	LPC_AD3	<30,44>
FWH4/LFRAME#	C34	LPC_FRAME#	<30,44>
LDRQ0#	A34	PCH_DRQ#0	T2005
LDRQ1#/GPIO23	F34	LPC_DRQ#1	T2006
SERIRQ	AB9	INT_SERIRQ	<30,44>
SATA0RXN	AK7	SATA_RXN0	<51>
SATA0RXP	AK6	SATA_RXP0	<51>
SATA0TXN	AK11	SATA_TXN0	<51>
SATA0TXP	AK9	SATA_TXP0	<51>
			HDD1
SATA1RXN	AH6	SATA_RXN1	<51>
SATA1RXP	AH5	SATA_RXP1	<51>
SATA1TXN	AH9	SATA_TXN1	<51>
SATA1TXP	AH8	SATA_TXP1	<51>
			ODD
SATA2RXN	AF11		
SATA2RXP	AF9		
SATA2TXN	AF7		
SATA2TXP	AF6		
SATA3RXN	AH3		
SATA3RXP	AH1		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	AD9		
SATA4RXP	AD8		
SATA4TXN	AD6		
SATA4TXP	AD5		
SATA5RXN	AD3	SATA_RXN5	<66>
SATA5RXP	AD1	SATA_RXP5	<66>
SATA5TXN	AB3	SATA_TXN5	<66>
SATA5TXP	AB1	SATA_TXP5	<66>
			ESATA
SATAICOMPO	AF16		
SATAICOMPI	AF15	SATA_COMP	R2007 37.4Ohm
SATALED#	T3	SATA_LED#	<56>
SATA0GP/GPIO21	Y9	SATA0GP	
SATA1GP/GPIO19	V1	SATA1GP	

+VTT_PCH_VCCIO, +3VS

R2025 10KOhm

<36> ACZ_BCLK_AUD, <36> ACZ_SYNC_AUD, <36,37> ACZ_RST#_AUD, <36> ACZ_SDOUT_AUD
RN2001A 33OHM ACZ_BCLK
RN2001B 33OHM ACZ_SYNC
RN2001C 33OHM ACZ_RST#
RN2001D 33OHM ACZ_SDOUT

+3VS, R3037 10KOhm@, Q2001 2N7002ET1G, <30,44> PCH_SPI_OV, HDA_DOCK_EN#, R2029 100KOHM

<28,44> SPI_CLK, SP2001, R0402 SB_SPICLK
<28,44> SPI_CS#0, SP2001, R0402 SB_SPICS0#
<28,44> SPI_CS#1, SP2002, R0402 SB_SPICS1#
<28,44> SPI_SI
<28,44> SPI_SO
+3VM_SPI, R2015 1KOhm@

INT_SERIRQ R2026 10KOhm
SATA0GP R2027 10KOhm
SATA1GP R2028 10KOhm@
+3VS

Pull up to +3VS per 395136_Checklist V1.6

Strap information:

HDA_SPKR: No reboot strap
Low: Disable.
High:Enable

HDA_DOCK_EN#:
1.Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2.GPIO33 low on the rising edge of PWROK, Will also disable Intel ME.

SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)

PEGATRON Title : PCH(1)_SATA,IHDA,RTC,LPC
BG1\HW1 Engineer: Kuansheng Yang
Size C | Project Name H36Y_U30X10 | Rev 1.0
Date: Monday, May 10, 2010 Sheet 20 of 99

PCIE5: PCIE-->CB

+3VSUS <27,30,33,34,81,92>
+3VS <3,16,17,20,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+VTT_PCH_ORG <22,26,27>
+3VSUS_ORG <22,24,25,27>

U2001B

PCI-E*
PERn1 BG30
PERp1 BJ30
PETn1 BF29
PETp1 BH29
PERn2 AW30
PERp2 BA30
PETn2 BC30
PETp2 BD30
PERn3 AU30
PERp3 AT30
PETn3 AU32
PETp3 AV32
PERn4 BA32
PERp4 BB32
PETn4 BD32
PETp4 BE32
PERn5 BF33
PERp5 BH33
PETn5 BG32
PETp5 BJ32
PERn6 BA34
PERp6 AW34
PETn6 BC34
PETp6 BD34
PERn7 AT34
PERp7 AU34
PETn7 AU36
PETp7 AV36
PERn8 BG34
PERp8 BJ34
PETn8 BG36
PETp8 BJ36

<53> PCIE_RXN2_WLAN
<53> PCIE_RXP2_WLAN
<53> PCIE_TXN2_WLAN
<53> PCIE_TXP2_WLAN
C2103 0.1UF/16V PCIE_TXN2_WLAN_C
C2104 0.1UF/16V PCIE_TXP2_WLAN_C

<43> PCIE_RXN3_NEWCARD
<43> PCIE_RXP3_NEWCARD
<43> PCIE_TXN3_NEWCARD
<43> PCIE_TXP3_NEWCARD
C2105 0.1UF/16V PCIE_TXN3_NEWCARD_C
C2106 0.1UF/16V PCIE_TXP3_NEWCARD_C

<54> PCIE_RXN4_USB30
<54> PCIE_RXP4_USB30
<54> PCIE_TXN4_USB30
<54> PCIE_TXP4_USB30
C2110 0.1UF/16V PCIE_TXN4_USB30_C
C2111 0.1UF/16V PCIE_TXP4_USB30_C

Ken 0318

<33> PCIE_RXN6_GLAN
<33> PCIE_RXP6_GLAN
<33> PCIE_TXN6_GLAN
<33> PCIE_TXP6_GLAN
C2108 0.1UF/16V PCIE_TXN6_GLAN_C
C2109 0.1UF/16V PCIE_TXP6_GLAN_C

EDS 1.0:
PCIE7,8 may not be availiable in all PCH SKUs.

CLKOUT_PCIE0N AK48
CLKOUT_PCIE0P AK47
PCIECLKRQ0#/GPIO73 P9
CLKOUT_PCIE1N AM43
CLKOUT_PCIE1P AM45
PCIECLKRQ1#/GPIO18 U4
CLKOUT_PCIE2N AM47
CLKOUT_PCIE2P AM48
PCIECLKRQ2#/GPIO20 N4
CLKOUT_PCIE3N AH42
CLKOUT_PCIE3P AH41
PCIECLKRQ3#/GPIO25 A8
CLKOUT_PCIE4N AM51
CLKOUT_PCIE4P AM53
PCIECLKRQ4#/GPIO26 M9
CLKOUT_PCIE5N AJ50
CLKOUT_PCIE5P AJ52
PCIECLKRQ5#/GPIO44 H6
CLKOUT_PEG_B_N AK53
CLKOUT_PEG_B_P AK51
PEG_B_CLKRQ#/GPIO56 P13

T2101 CLK_REQ0# P9
T2102 CLK_REQ1# U4
T2104 CLKREQ_GLAN#_R P13

<53> CLK_PCIE_WLAN#_PCH
<53> CLK_PCIE_WLAN_PCH
SP2101 SP2102 R0402 CLK_PCH_SRC2_N CLK_PCH_SRC2_P
<53> CLKREQ2_WLAN#
SP2103 R0402 N4

<43> CLK_PCIE_NEWCARD#_PCH
<43> CLK_PCIE_NEWCARD_PCH
SP2104 SP2105 R0402 CLK_PCH_SRC3_N CLK_PCH_SRC3_P
<43,44> CLKREQ3_NEWCARD#
SP2106 R0402 A8

<54> CLK_PCIE_USB30#_PCH
<54> CLK_PCIE_USB30_PCH
SP2112 SP2111 R0402 CLK_PCH_SRC4_N CLK_PCH_SRC4_P
<54> CLK_REQ4_USB30#
SP2113 R0402 CLK_REQ4# M9

Ken 0318

<33> CLK_PCIE_LAN#
<33> CLK_PCIE_LAN
SP2107 SP2108 R0402 CLK_PCH_SRC5_N CLK_PCH_SRC5_P
<33> CLK_REQ5_LAN#

SMBus
SMBALERT#/GPIO11 B9 EXT_SCI# → EXT_SCI# <30>
SMBCLK H14 SCL_3A → SCL_3A <28>
SMBDATA C8 SDA_3A → SDA_3A <28>
SML0ALERT#/GPIO60 J14 RTLAN_DSM_EN T2106
SML0CLK C6 SML0_CLK T2107
SML0DATA G8 SML0_DAT T2108
SML1ALERT#/GPIO74 M14 SML1ALERT# T2105
SML1CLK/GPIO58 E10 SML1_CLK → SML1_CLK <28,56>
SML1DATA/GPIO75 G12 SML1_DAT → SML1_DAT <28,56>
TO EC

C-Link
CL_CLK1 T13 → CL_CLK <53>
CL_DATA1 T11 → CL_DATA <53>
CL_RST1# T9 → CL_RST# <53>

PEG
PEG_A_CLKRQ#/GPIO47 H1 CLKREQ_PEG# T2110
CLKOUT_PEG_A_N AD43 CLK_PCIE_PEG# PCH_L
CLKOUT_PEG_A_P AD45 CLK_PCIE_PEG_PCH_L
SP2109 SP2110 R0402 R0402 T2113 T2114
CLKOUT_DMI_N AN4 → CLK_DMI#_PCH <3>
CLKOUT_DMI_P AN2 → CLK_DMI_PCH <3>
CLKOUT_DP_N/CLKOUT_BCLK1_N AT1 T2115
CLKOUT_DP_P/CLKOUT_BCLK1_P AT3 T2116

Clock Inputs from CLK BUFFER
CLKIN_DMI_N AW24 → CLK_DMI# <29>
CLKIN_DMI_P BA24 → CLK_DMI <29>
CLKIN_BCLK_N AP3 → CLK_PCH_BCLK# <29>
CLKIN_BCLK_P AP1 → CLK_PCH_BCLK <29>
CLKIN_DOT_96N F18 → CLK_DOT96# <29>
CLKIN_DOT_96P E18 → CLK_DOT96 <29>
CLKIN_SATA_N/CKSSCD_N AH13 → CLK_SATA# <29>
CLKIN_SATA_P/CKSSCD_P AH12 → CLK_SATA <29>
REFCLK14IN P41 → CLK_ICH14 <29>
Adding layout test point for boundary scan Jervis 2009/11/09
CLKIN_PCILOOPBACK J42 → CLK_PCI_FB <24>
T2117
XTAL25_IN AH51
XTAL25_OUT AH53
XCLK_RCOMP AF38 XCLK_COMP R2117 90.9Ohm → VTT_PCH_ORG

Clock Flex
CLKOUTFLEX0/GPIO64 T45 CLK_OUT0 T2111
CLKOUTFLEX1/GPIO65 P43 CLK_OUT1 T2112
CLKOUTFLEX2/GPIO66 T42 CLK_OUT2 T2109
CLKOUTFLEX3/GPIO67 N50 CLK_OUT3 R2118 22Ohm → CLK_USB48_CR <40>
C2107 10PF/50V
GND

IBEXPEAK-M

R2120 0Ohm GND
C2101 27PF/50V
R2151 1MOhm
X2102 25Mhz
X2101 25Mhz
C2102 27PF/50V
GND

05061930 KEN xtal co-lay

+3VSUS_ORG
EXT_SCI# R2130 10KOhm
SCL_3A R2132 2.2KOhm
SDA_3A R2133 2.2KOhm
RTLAN_DSM_EN R2131 10KOhm
SML0_CLK R2140 2.2KOhm
SML0_DAT R2138 2.2KOhm
SML1_CLK R2136 4.7KOhm
SML1_DAT R2137 4.7KOhm
SML1ALERT# R2142 10KOhm

PCH CLKREQ Setting:

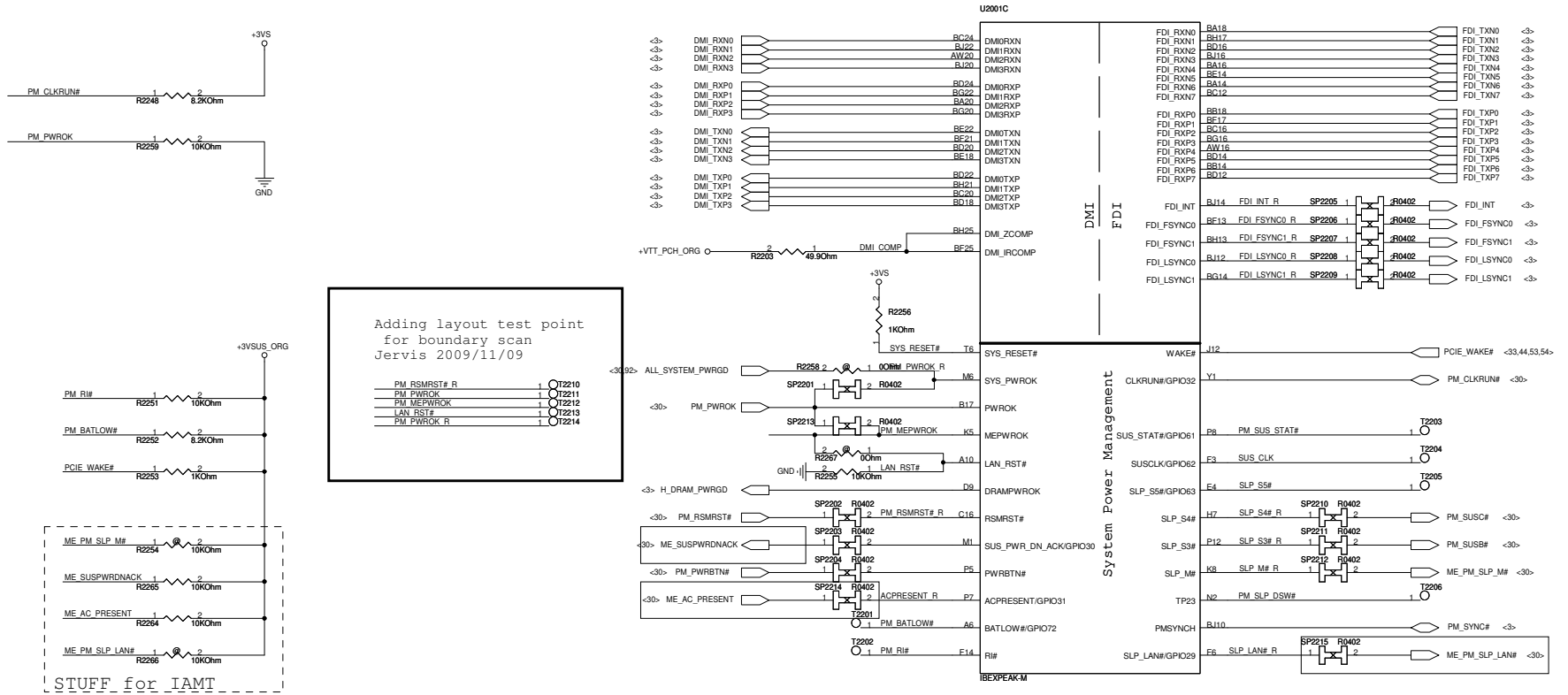
Not connected to device.
+3VSUS_ORG
CLK_REQ0# R2126 10KOhm
CLK_REQ4_USB30# R2135 10KOhm

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
+3VS
CLK_REQ1# R2125 10KOhm
CLKREQ2_WLAN# R2123 10KOhm
+3VSUS_ORG
CLKREQ3_NEWCARD# R2124 10KOhm
CLKREQ_GLAN#_R R2129 10KOhm
CLK_REQ5_LAN# R2128 10KOhm
CLK_REQ5_LAN# R2134 10KOhm
CLKREQ2_WLAN# R2144 10KOhm
CLKREQ3_NEWCARD# R2143 10KOhm
CLKREQ_PEG# R2139 10KOhm
CLK_REQ4_USB30# R2127 10KOhm
GND

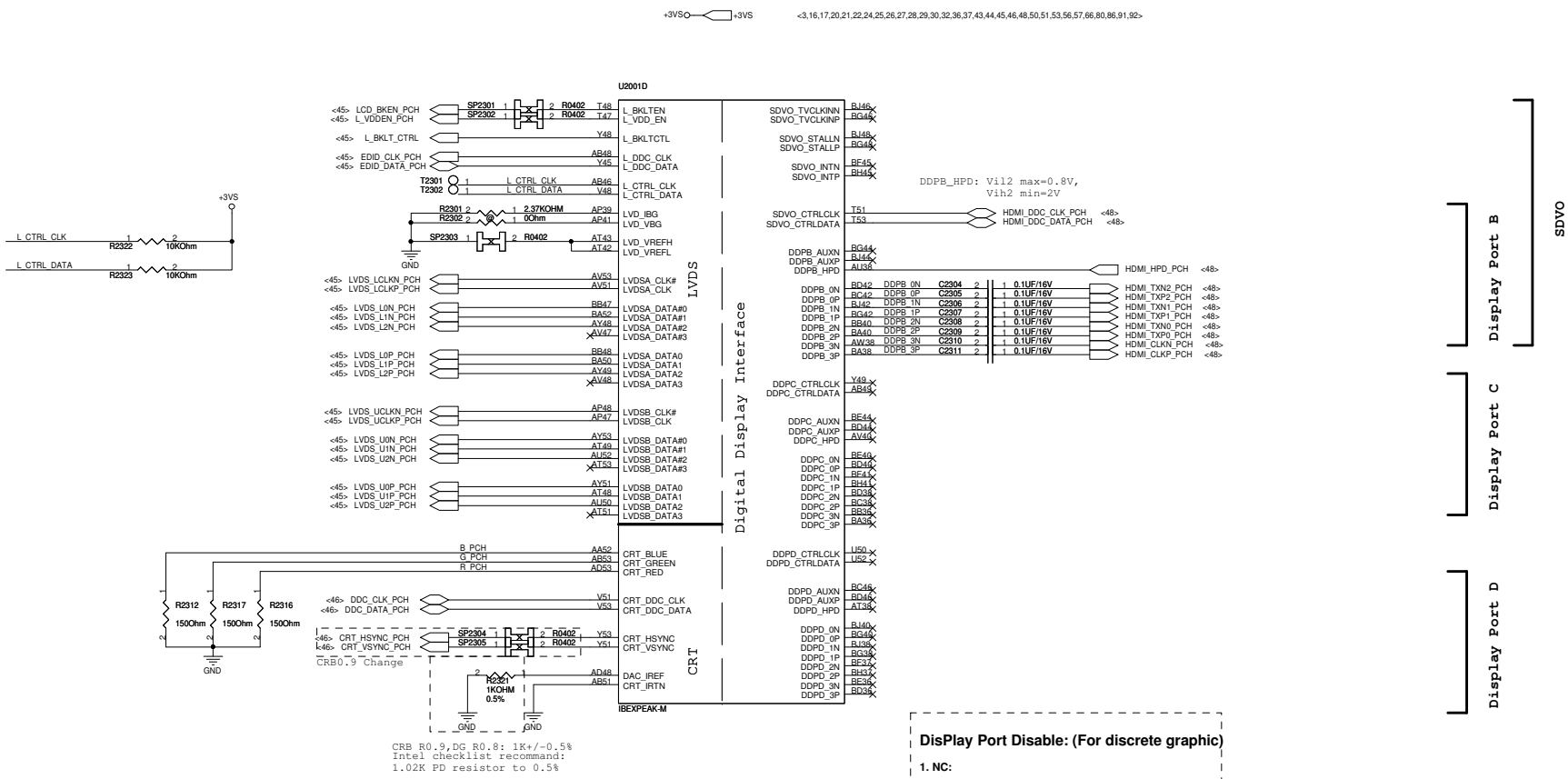
05052100 KEN
05052100 KEN

PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG
BG1\HW1 Engineer: Kuansheng Yang
Size C | Project Name H36Y_U30X10 | Rev 1.0
Date: Monday, May 10, 2010 Sheet 21 of 99

pre-ES1 not support
Reversal Feature



PEGATRON	Title : PCH(3)_FDI,DMI,SYS PWR		
BG1\HW1	Engineer: *Kuansheng Yang*		
Size: C	Project Name: H36Y_U30X10		Rev: 1.0
Date: Monday, May 10, 2010	Sheet 22 of 99		



DisPlay Port Disable: (For discrete graphic)

1. NC:

ALL

LVDS Disable: (For discrete graphic)

1. NC:

LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:

VccALVDS,VccTX_LVDS

CRT Disable: (For discrete graphic)

1. NC:

CRT_RED,CRT_GREEN,CRT_BLUE
CRT_HSYCN,CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:

DAC_IREF

3. Connected to GND:

CRT_ITRN

4. Connect to +V3.3:

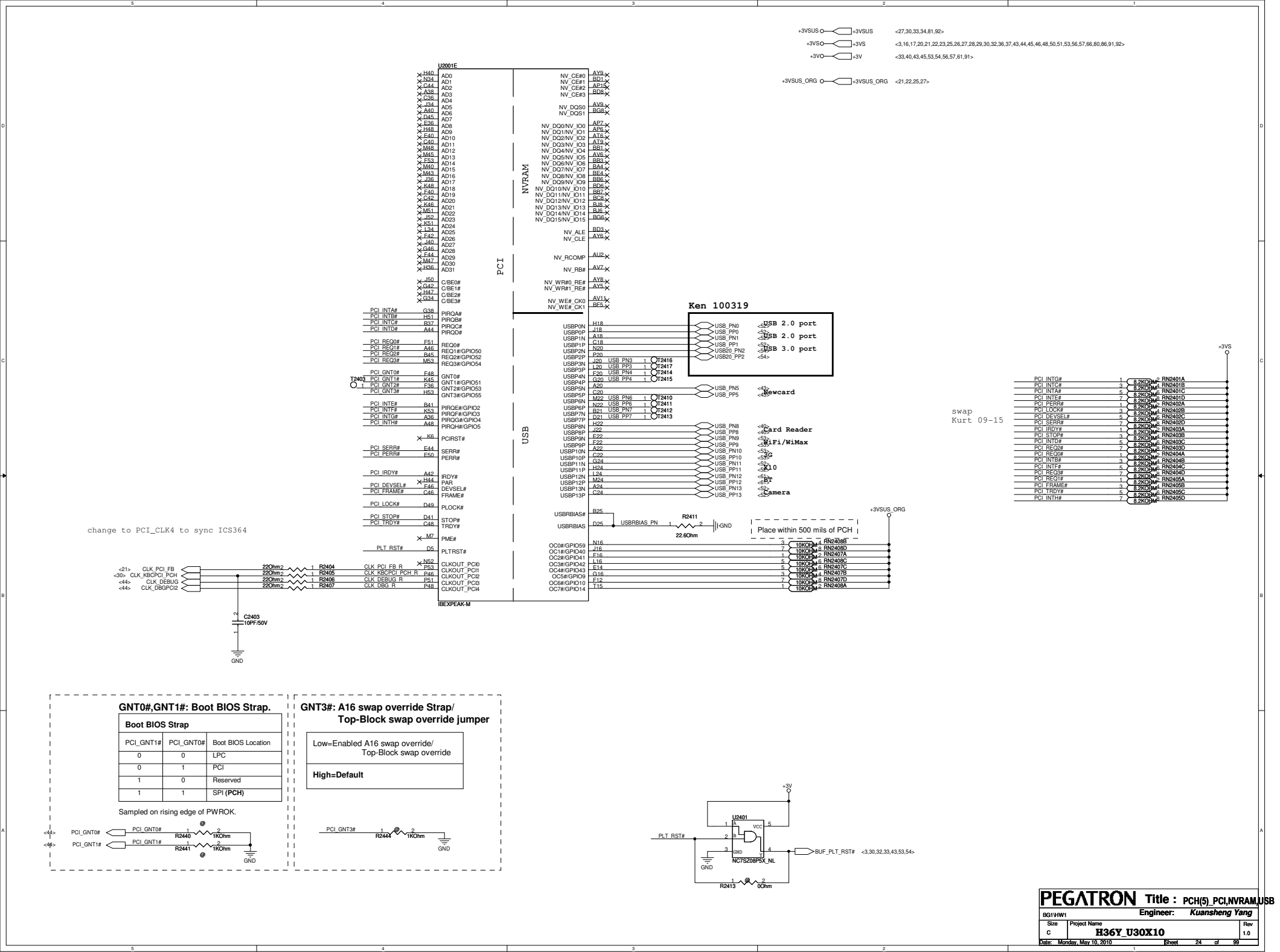
VCCADAC

PEGATRON **Title : PCH(4)_DP,LVDS,CRT**

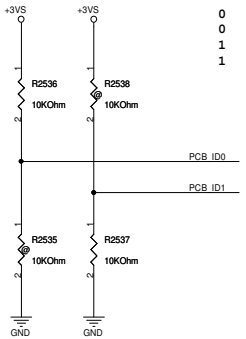
BG1VHW1 **Engineer: *Kuansheng Yang***

Size	Project Name	Rev
C	**H36Y_U30X10**	1.0

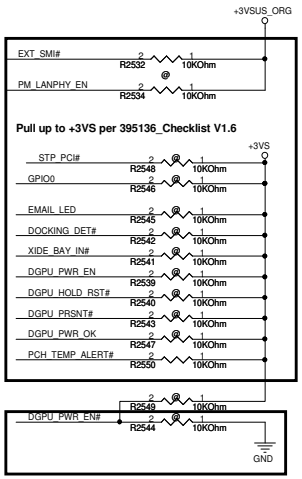
Date: Monday, May 10, 2010 Sheet 23 of 99


+3VSUS +3VSUS <27,30,33,34,81,92>
+3VS +3VS <3,16,17,20,21,22,23,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+3V +3V <33,40,43,45,53,54,56,57,61,91>
+3VSUS_ORG +3VSUS_ORG <21,22,25,27>
U2001E
PCI
NVRAM
USB
IBEXPEAK-M
Ken 100319
USB 2.0 port
USB 2.0 port
USB 3.0 port
Newcard
Card Reader
WiFi/WiMax
3G
BT
Camera
Place within 500 mils of PCH
change to PCI_CLK4 to sync ICS364
swap
Kurt 09-15
GNT0#,GNT1#: Boot BIOS Strap.
Boot BIOS Strap
PCI_GNT1# PCI_GNT0# Boot BIOS Location
0 0 LPC
0 1 PCI
1 0 Reserved
1 1 SPI (PCH)
Sampled on rising edge of PWROK.
GNT3#: A16 swap override Strap/ Top-Block swap override jumper
Low=Enabled A16 swap override/ Top-Block swap override
High=Default
U2401
NC7SZ08P5X_NL
BUF_PLT_RST# <3,30,32,33,43,53,54>
PEGATRON Title : PCH(5)_PCI,NVRAM,USB
BG1/HW1 Engineer: Kuansheng Yang
Size C Project Name H36Y_U30X10 Rev 1.0
Date: Monday, May 10, 2010 Sheet 24 of 99

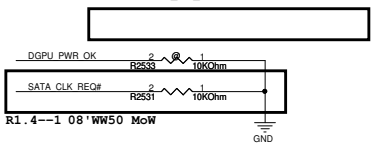
ID0	ID1	SKU
0	0	CFD_Non-IAMT
0	1	CFD_IAMT
1	0	AUB_Non-IAMT
1	1	AUB_IAMT



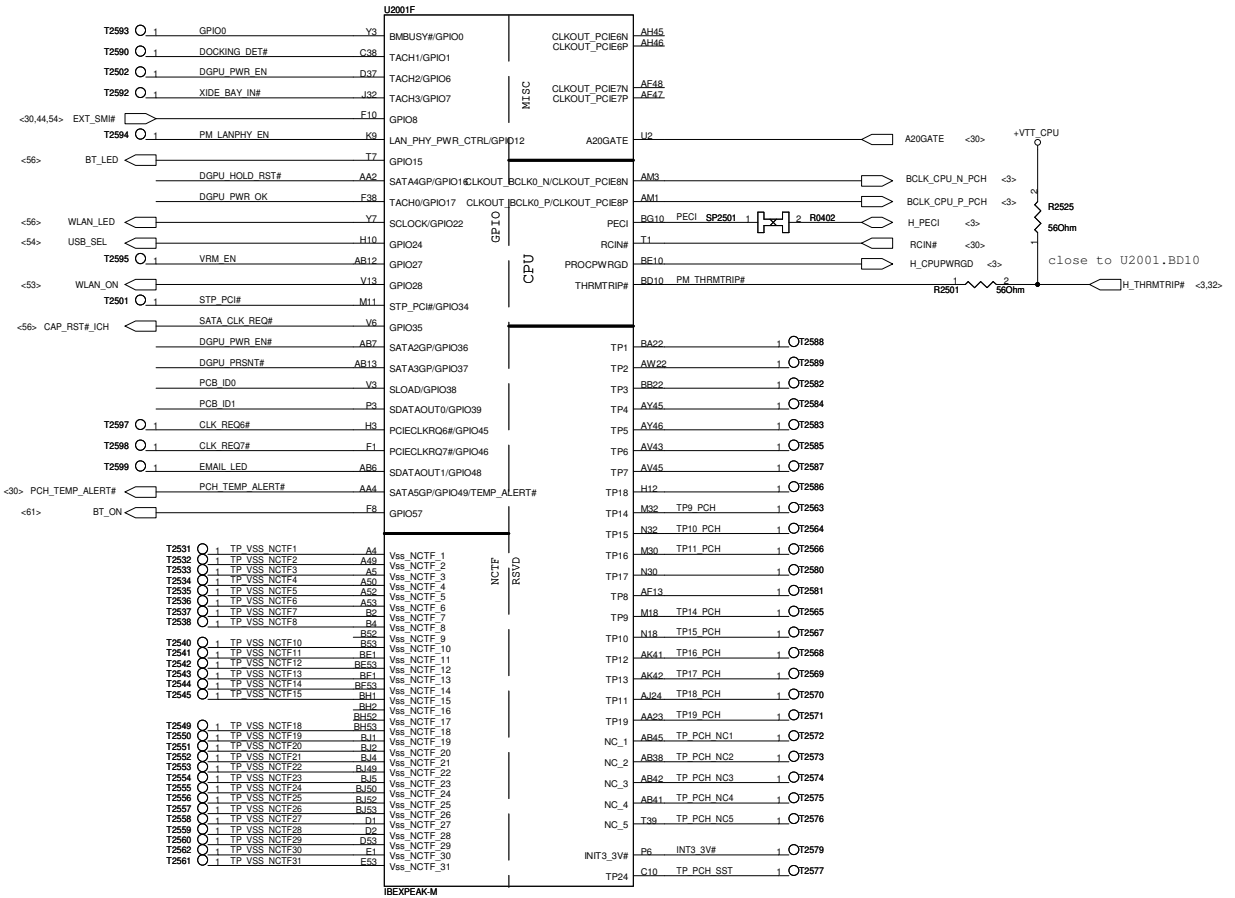
GPIO 27:Enable VCCVRM,Low=disable.
Default internal pull up.



Remove PWR_OK_VGA net



R1.4--1 08'WW50 MoW

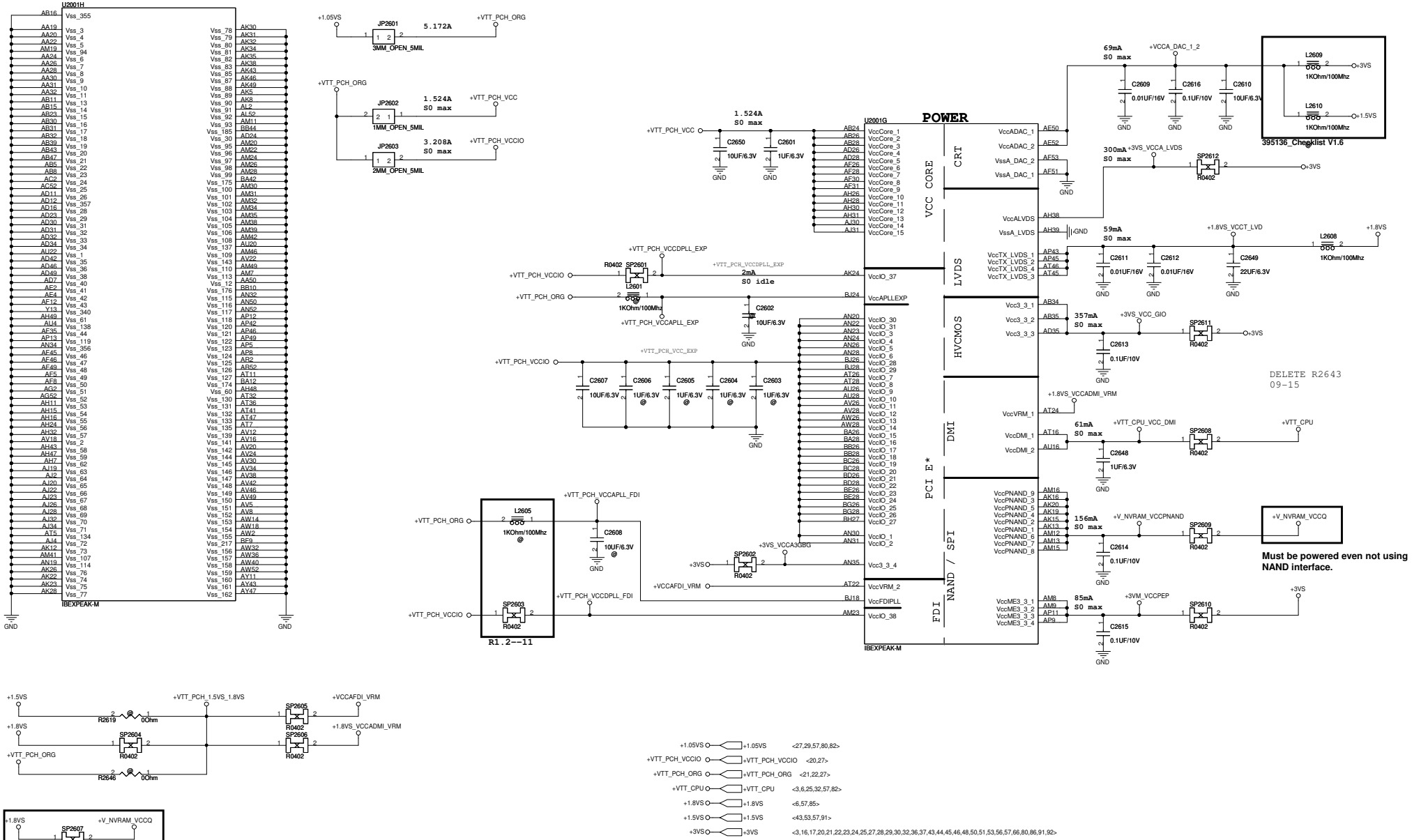


+3VS	+3VS	<3,16,17,20,21,22,23,24,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+3VSUS	+3VSUS	<27,30,33,34,81,92>
+VTT_CPU	+VTT_CPU	<3,6,26,32,57,82>
+3VSUS_ORG	+3VSUS_ORG	<21,22,24,27>

PEGATRON Title : PCH(6)_CPU,GPIO,MISC
BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 25 of 99



+1.05VS <27,29,57,80,82>

+VTT_PCH_VCCIO <20,27>

+VTT_PCH_ORG <21,22,27>

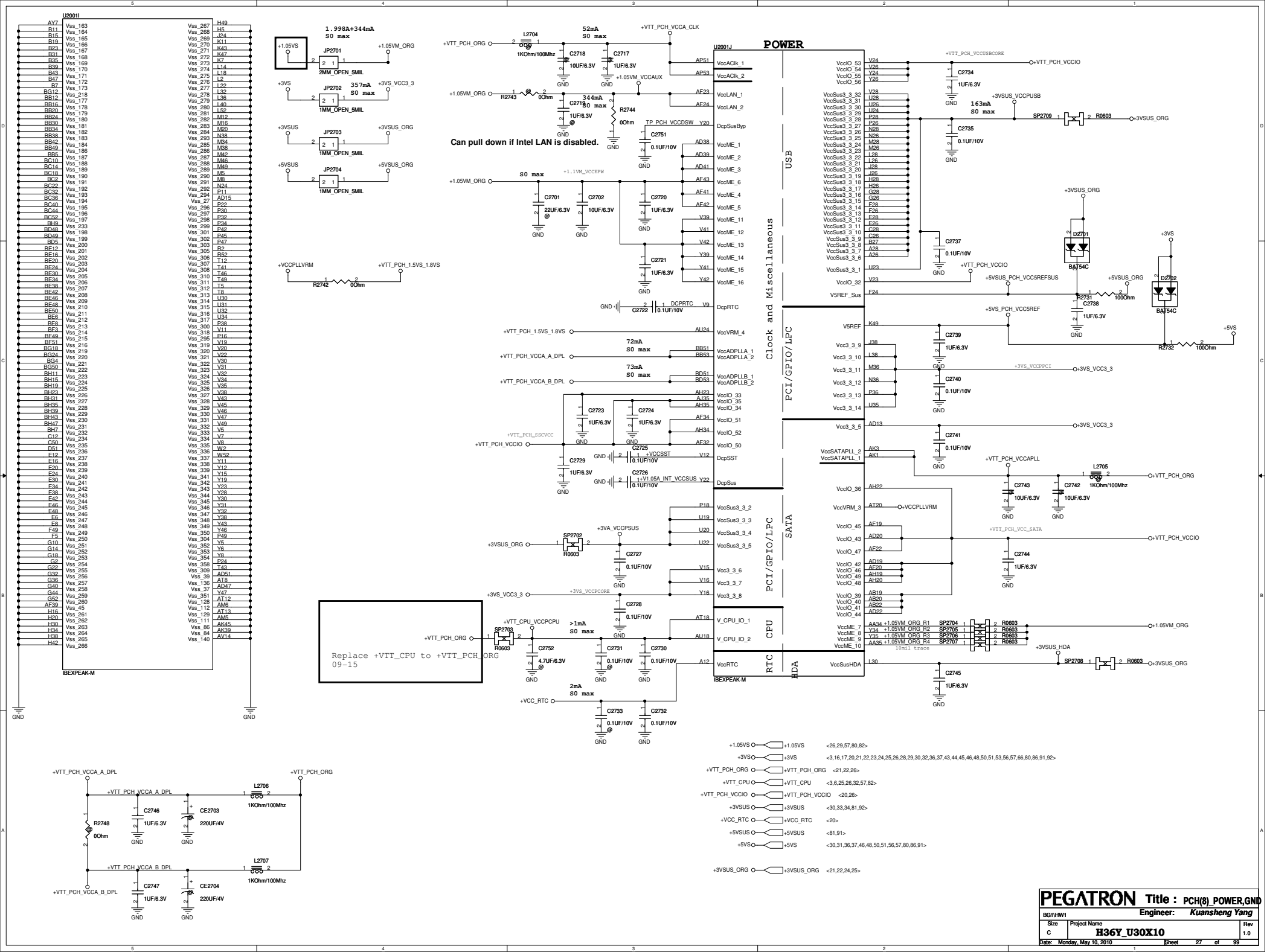
+VTT_CPU <3,6,25,32,57,82>

+1.8VS <6,57,85>

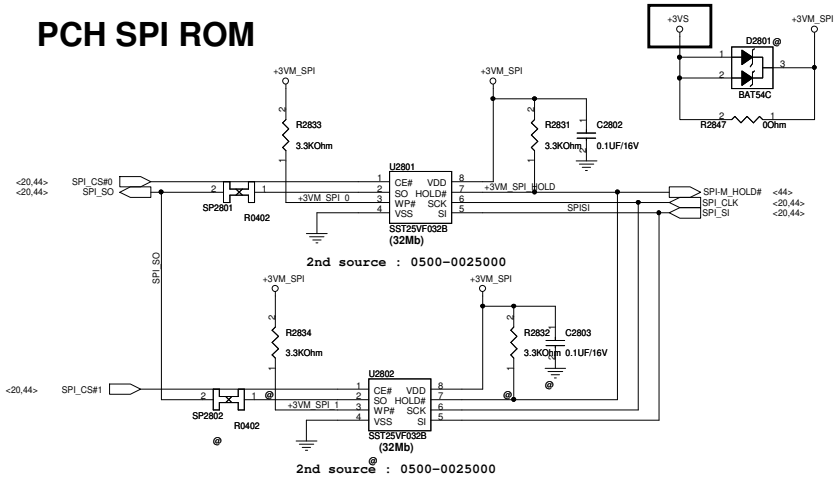
+1.5VS <43,53,57,91>

+3VS <3,16,17,20,21,22,23,24,25,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

PEGATRON	Title : PCH(7)_POWER,GND		
BG1\HW1	Engineer: Kuansheng Yang		
Size: C	Project Name: H36Y_U30X10		Rev: 1.0
Date: Monday, May 10, 2010	Sheet 26 of 99		


POWER
U2001I
U2001J
iBEXPEAK-M
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
1.998A+344mA
S0 max
JP2701
2MM_OPEN_5MIL
JP2702
357mA
S0 max
1MM_OPEN_5MIL
JP2703
1MM_OPEN_5MIL
JP2704
1MM_OPEN_5MIL
Can pull down if Intel LAN is disabled.
52mA
S0 max
344mA
S0 max
163mA
S0 max
72mA
S0 max
73mA
S0 max
>1mA
S0 max
2mA
S0 max
Replace +VTT_CPU to +VTT_PCH_ORG
09-15
PEGATRON
Title : PCH(8)_POWER,GND
Engineer: Kuansheng Yang
BG1\HW1
Size C
Project Name H36Y_U30X10
Rev 1.0
Date: Monday, May 10, 2010
Sheet 27 of 99

PCH SPI ROM

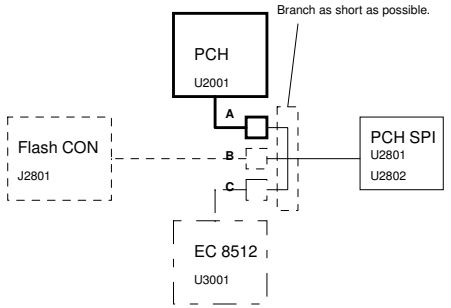


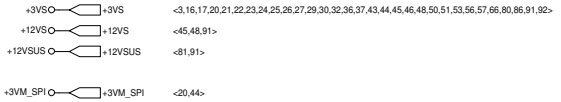
SPI FROM EC

For EC request.

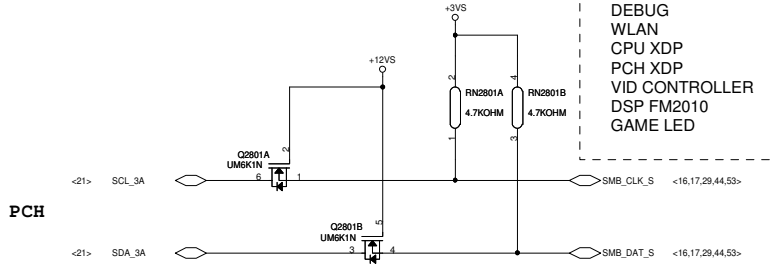
SPI FLASH CON

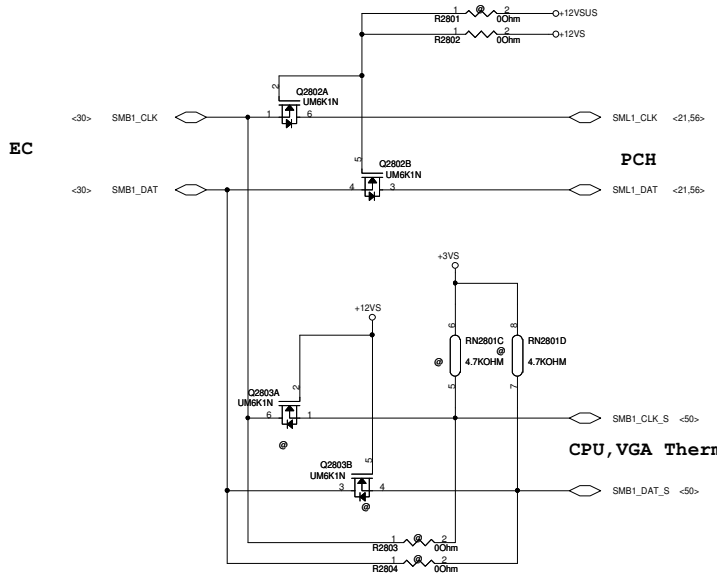
SPI Setting for layout:



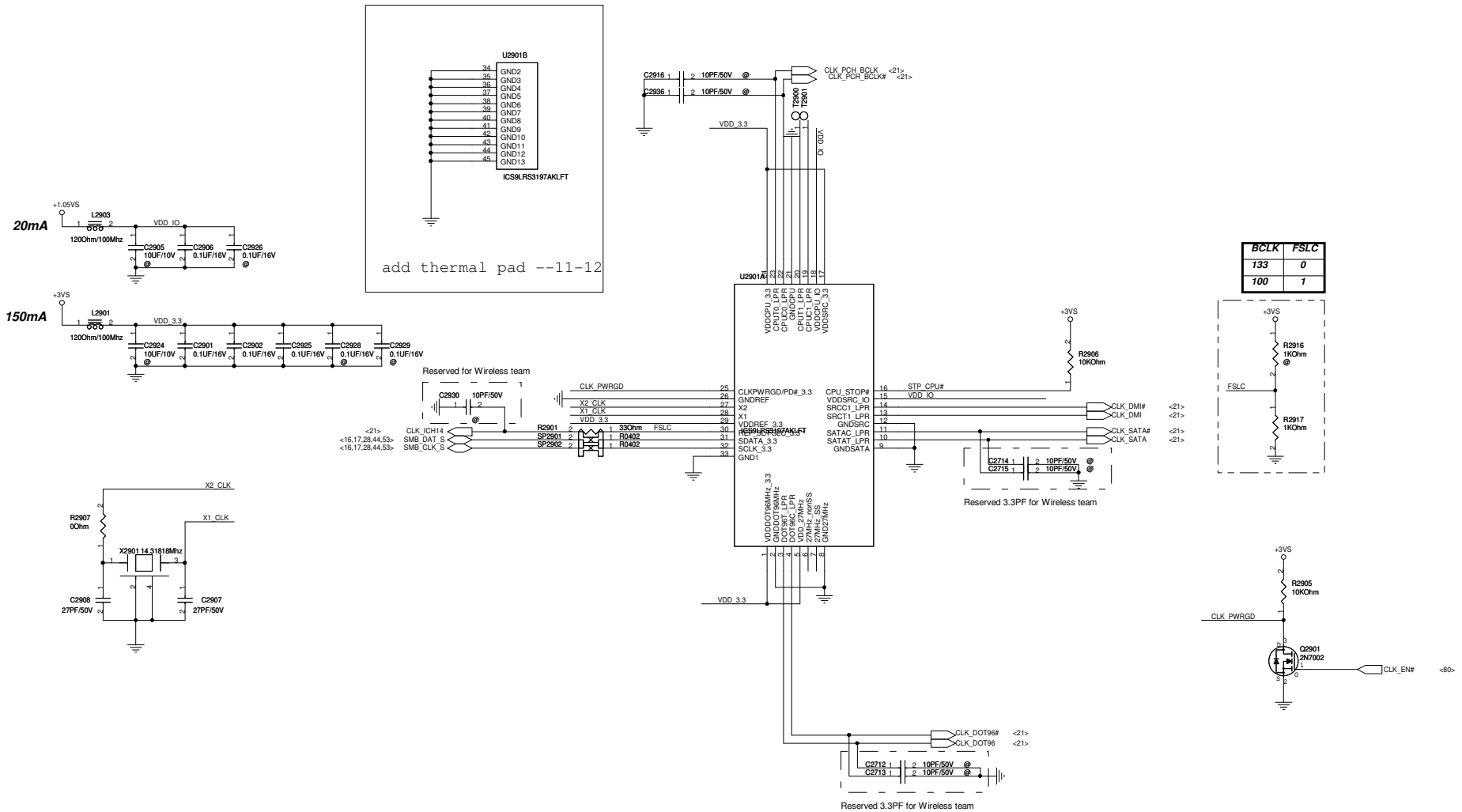


SMBUS Link device
- SPD
- CLKGEN
- DEBUG
- WLAN
- CPU XDP
- PCH XDP
- VID CONTROLLER
- DSP FM2010
- GAME LED



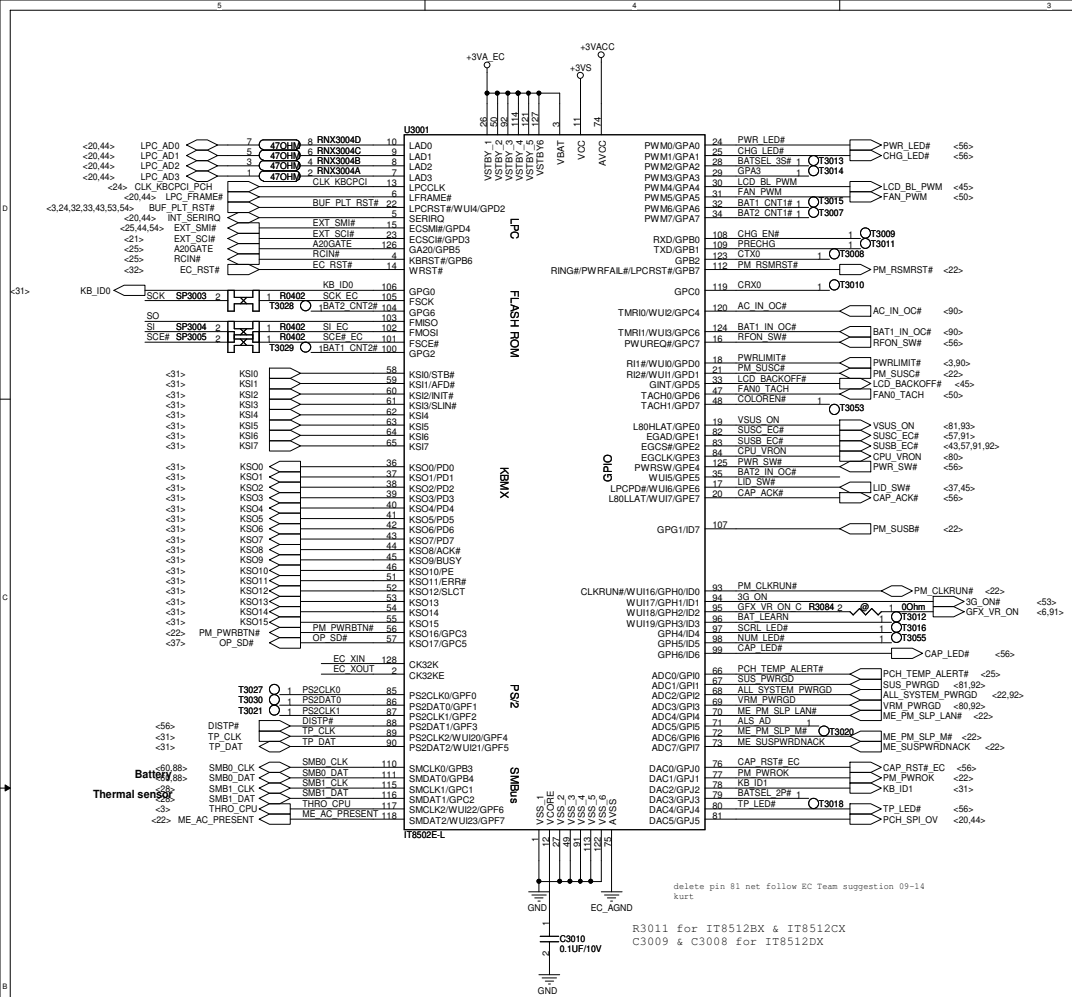


PEGATRON	Title : PCH(9)_SPI,SMB	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 28 of 99	

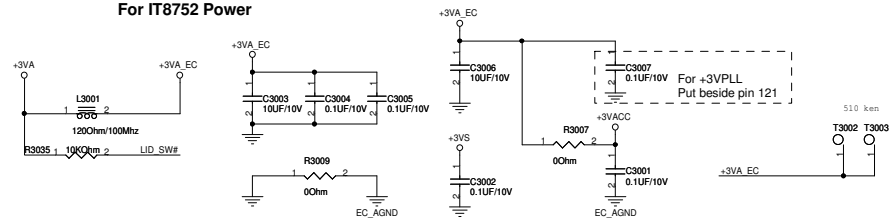


R1.4--3

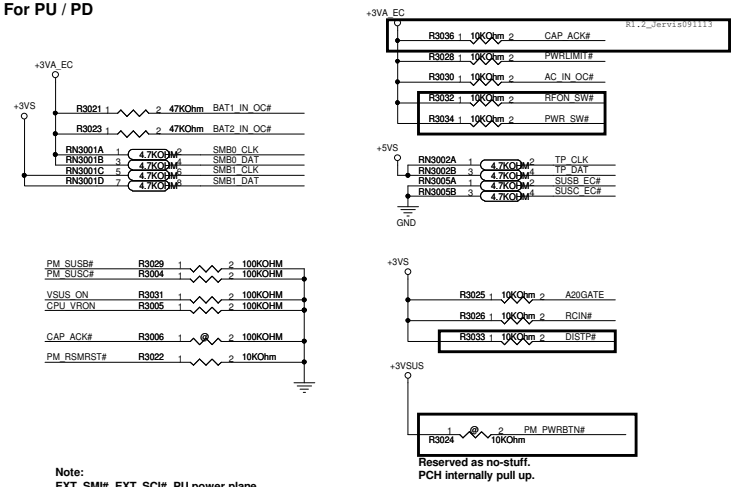
PEGATRON	Title : CLK_ICS9LRS3197	
BG1VHW1	Engineer: Kuansheng Yang	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 29 of 99	



For IT8752 Power



For PU / PD

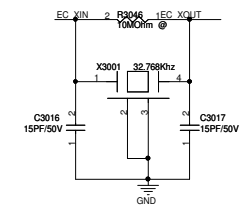


Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

Reserved as no-stuff.
PCH internally pull up.

iAMT EC strapping need to check

For X'tal



Note:
Cload=12.5PF place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

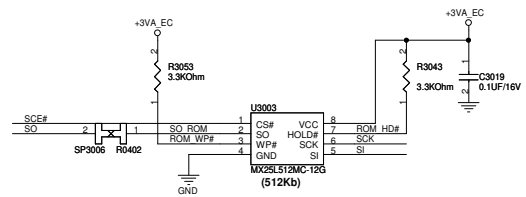
Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

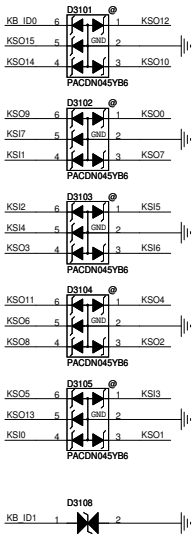
For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

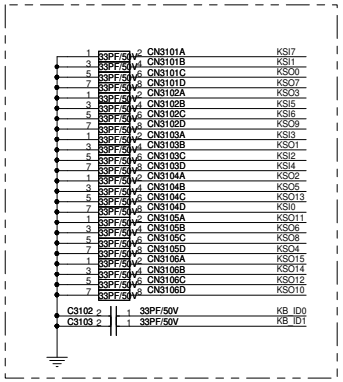


2nd source : 0500-001L000

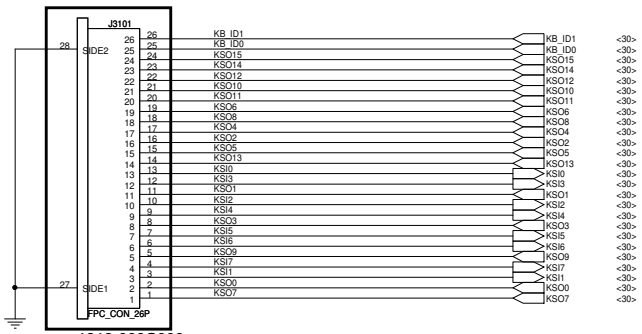
PEGATRON	Title : EC_IT8512(1)		
BG1VHW1	Engineer: Kuansheng Yang		
Size: C	Project Name: H36Y_U30X10		Rev: 1.0
Date: Monday, May 10, 2010	Sheet 30 of 99		



EMI

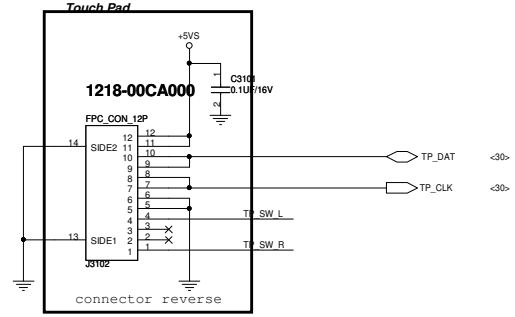


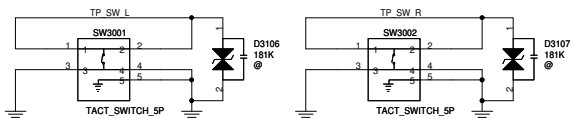
Keyboard



1218-009C000

Touch Pad





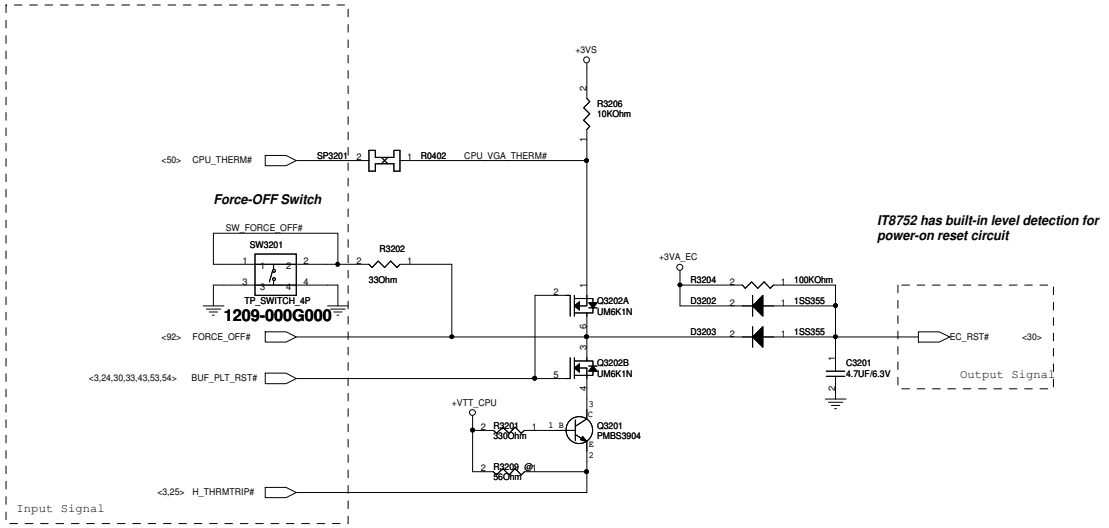
1209-000Q000

1st source: 1209-000P000
2nd source: 1209-000Q000

+3VA_EC +3VA_EC <30,32>
+3V +3V <24,33,40,43,45,53,54,56,57,61,91>
+3VS +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+5VA +5VA <56,81,82,88>
+5V +5V <44,52,54,56,57,85,91>
+5VS +5VS <27,30,36,37,46,48,50,51,56,57,80,86,91>

PEGATRON	Title : EC_IT8512(2)KB, TP,FP		
BG1\HW1	Engineer: *Kuansheng Yang*		
Size C	Project Name H36Y_U30X10		Rev 1.0
Date: Monday, May 10, 2010	Sheet 31 of 99		

Thermal Policy



+VTT_CPU	+VTT_CPU	<3,6,25,26,57,82>
+3VA_EC	+3VA_EC	<30>
+3VS	+3VS	<3,16,17,20,21,22,23,24,25,26,27,28,29,30,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

PEGATRON Title : RST_Reset Circuit

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 32 of 99

+3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

+3VSUS <27,30,34,81,92>

AR8131:Remove R3301,C3318,C3319

AR8121:Remove L3302,C3317,R3302,C3336

R3301 @ 0Ohm

C3318 close to Pin 1

L3302 4.7UH

+1.7_Pin1

C3316 0.1UF/16V

C3317 10UF/6.3V

C3318 1UF/10V @

+AVDD_CEN_LAN

+1.7_Pin6

R3302 0Ohm

C3319 1UF/10V @

C3336 0.1UF/16V

GND

AR8131 with overclock: Remove R3315

AR8121:Remove R3315

ground pad要打散熱孔

R3315 5.4KOHM @

PCIE_TXN6_GLAN <21>

PCIE_TXP6_GLAN <21>

CLK_PCIE_LAN <21>

CLK_PCIE_LAN# <21>

C3335 0.1UF/16V

C3334 0.1UF/16V

PCIE_RXP6_GLAN <21>

PCIE_RXN6_GLAN <21>

U3301A

AR8131:Remove C3322,C3321,L3303,L3304

AR8121:Remove C3337,R3324

R3303 @ 0Ohm

R3304 0Ohm

+AVDDL

+AVDD_VCO1

C3337 0.1UF/16V

R3324 0Ohm

+AVDD_VCO2

C3323 0.1UF/16V

With overclock:Remove R3303

Not overclock:Remove R3304

For AR8131: Remove R3305,R3306,C3324,C3325,C3326,Q3301

For AR8121: Remove C3327 R3308

Q3301 close to Pin8

R3305 0Ohm

+3V_LAN

C3324 0.1UF/16V

BC807-25 Q3301 @

R3306 10KOhm @

+2.5_Pin5

C3327 0.1UF/16V

+AVDDL

C3325 0.1UF/16V

C3326 10UF/6.3V @

R3308 0Ohm

VDD_+2.5V

GND

+3V_LAN

+1.7_Pin1

<22,44,53,54> PCIE_WAKE#

pin#5的pin name應爲 2.5V

+2.5_Pin5

+1.7_Pin6

SEL_25M

R3310 4.7KOhm @

C3333 1000PF/50V @

C3332 1UF/10V

C3331 0.1UF/16V

AR8121:Remove R3310

AR8131/25MHz:Remove R3310 C3333

R3311 2.37KOHM

AR8121: Remove R3313

AR8131: Remove R3314

R3313 0Ohm

CLK_REQ5_LAN# <21>

R3314 0Ohm @

AR8131-AL1E

SP3301

R0402

Q3302 2N7002 @

<3,24,30,32,43,53,54> BUF_PLT_RST#

+3V

<34> L_TRDP0

<34> L_TRDN0

<34> L_TRDP1

<34> L_TRDN1

<34> L_TRDP2

<34> L_TRDN2

<34> L_TRDP3

<34> L_TRDN3

RN3301A 49.9OHM

RN3301B 49.9OHM

RN3302A 49.9OHM

RN3302B 49.9OHM

RN3303A 49.9OHM

RN3303B 49.9OHM

RN3304A 49.9OHM

RN3304B 49.9OHM

CX3301D 0.1UF/25V

CX3301C 0.1UF/25V

CX3301B 0.1UF/25V

CX3301A 0.1UF/25V

1AV0-000LF00

SWAP

Kurt 09-15

swap 09-17

+3VSUS L3301 80Ohm/100Mhz +3V_LAN

C3301 10UF/6.3V

C3302 10UF/6.3V

C3303 1UF/10V

C3304 0.1UF/16V

C3301 C3302 C3303 C3304 close to pin2

VDD_+2.5V

C3305 1UF/10V

C3306 0.1UF/16V

C3307 0.1UF/16V

C3305 close to pin15

+DVDDL

C3308 1UF/10V

C3309 0.1UF/16V

C3310 0.1UF/16V

C3311 0.1UF/16V @

C3308 close to pin45/46

+AVDDL

C3312 0.1UF/16V

C3313 0.1UF/16V

C3314 0.1UF/16V

C3315 0.1UF/16V

05061930 KEN xtal co-lay

X2_LAN

X1_LAN

X3302 25Mhz

X3301 25Mhz

C3328 10PF/50V @

1EXT_25/48

T3300 TPC26T

C3329 27PF/50V @

C3330 27PF/50V

For AR8131 : Remove R3309

+1.7_Pin6

R3309 0Ohm @

VDD_+2.5V

AR8121:Remove C3328

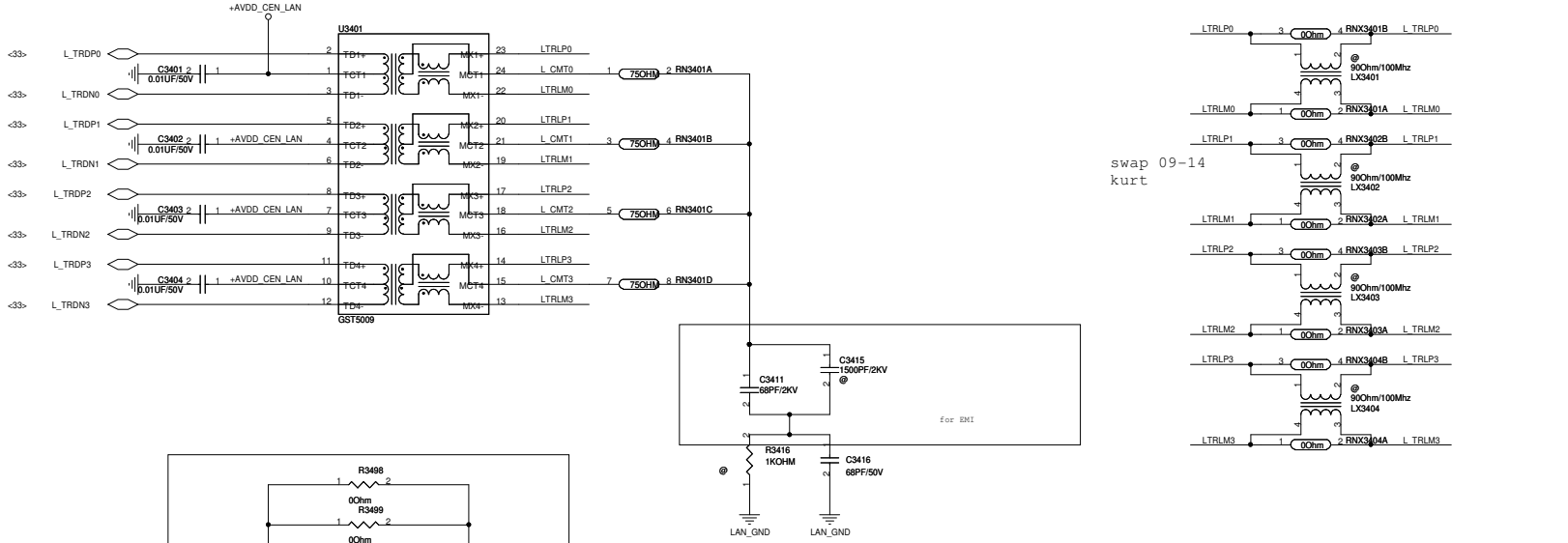
AR8131/25MHz: Remove C3328

U3301B

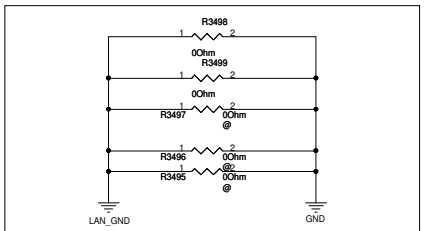
AR8131-AL1E

R1.4--6

PEGATRON	Title : LAN_AR8131		
BG1VHW1	Engineer: *Kuansheng Yang*		
Size: C	Project Name: H36Y_U30X10		Rev: 1.0
Date: Monday, May 10, 2010	Sheet 33 of 99		

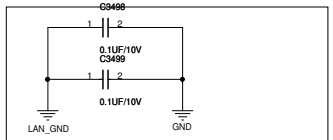


swap 09-14
kurt

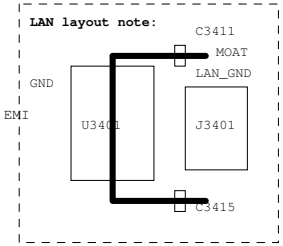


09-17
Add R3495,R3496,R3497,R3498,R3499 for EMI

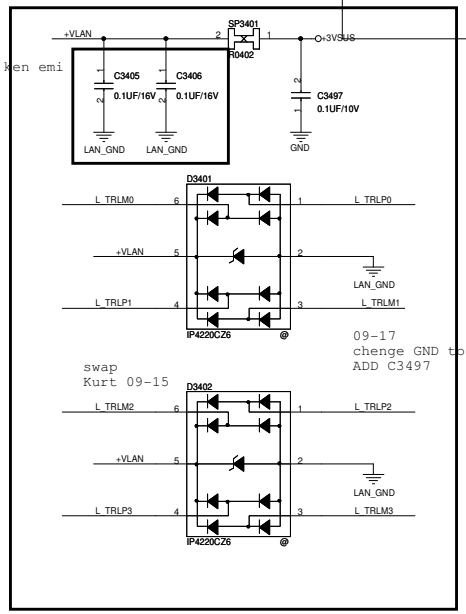
R1.4-2



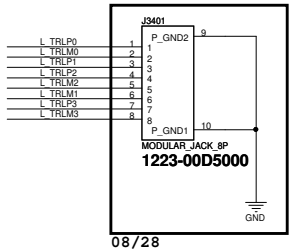
add c3498& c3499 for EMI
09-16



105101000 ken emi



09-17
chenge GND to LAN_GND
ADD C3497



08/28

PEGATRON	Title : RJ45/ RJ11	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 34 of 99	

PEGATRON Title : MDC CONN

BG1\HW1 Engineer: *Kuansheng Yang*

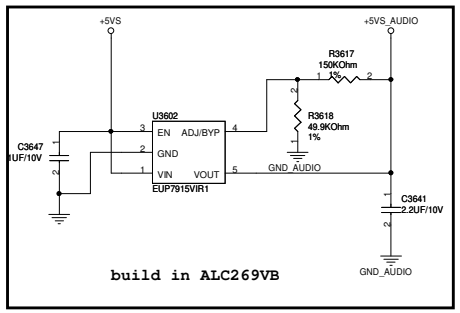
Size	Project Name	Rev
C	H36Y_U30X10	1.0

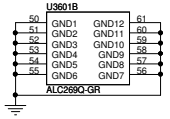
Date: Monday, May 10, 2010 Sheet 35 of 99

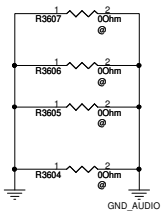
Audio Codec

DIGITAL ANALOG

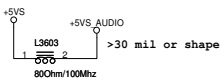
Vout=1.215*(1+(150K/49.9K)= 4.86V

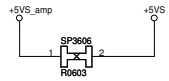


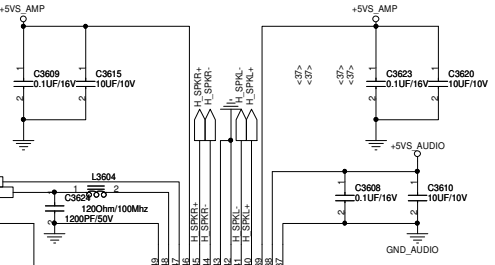




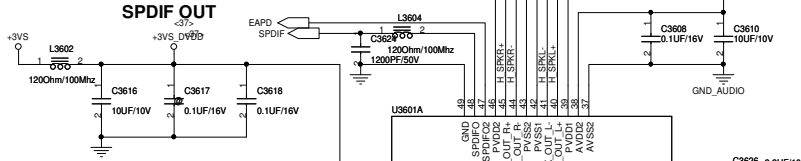
add R3607&R3606&R3605 c3499 for EMI 09-16

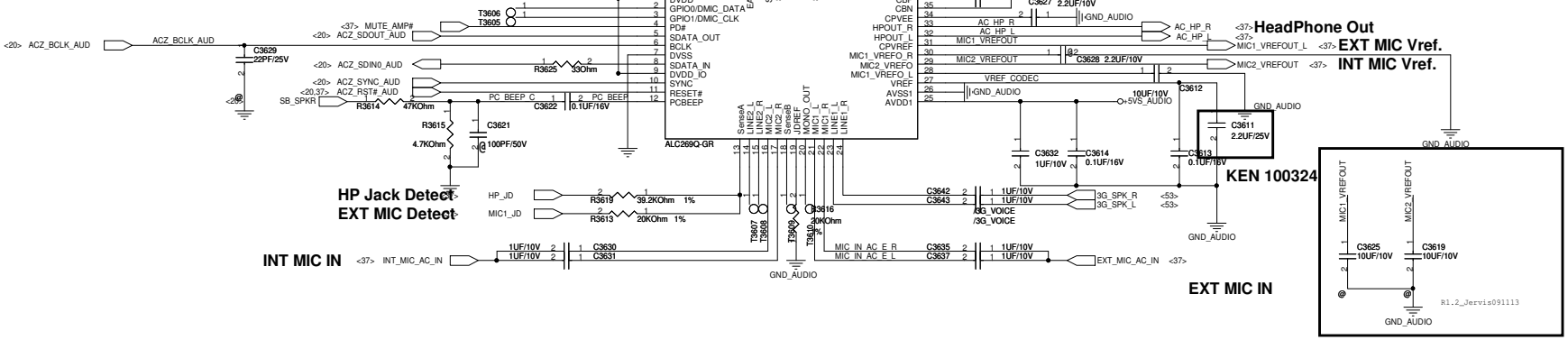






SPDIF OUT





HeadPhone Out

EXT MIC Vref.

INT MIC Vref.

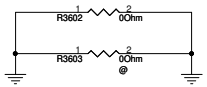
KEN 100324

HP Jack Detect

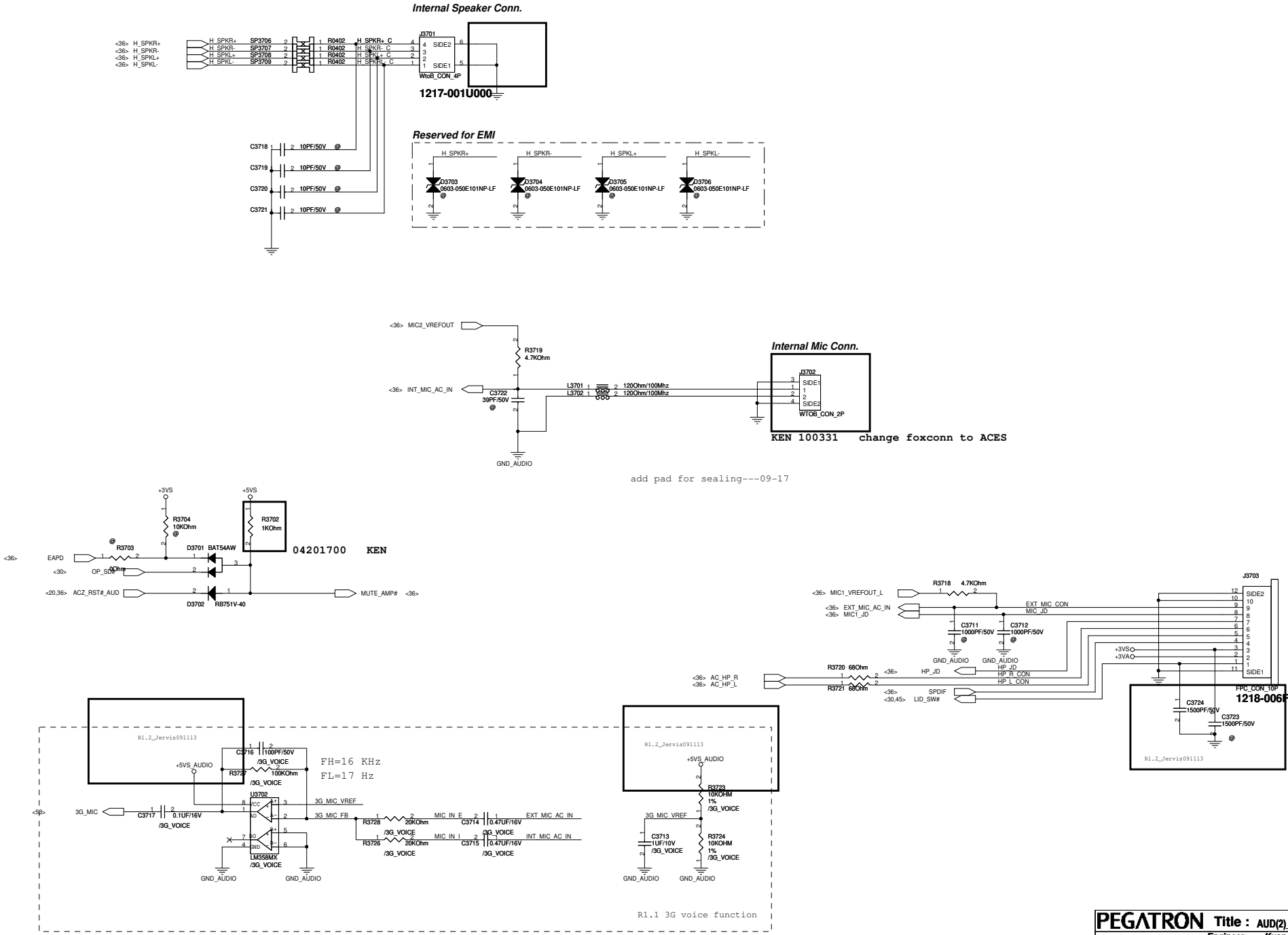
EXT MIC Detect

INT MIC IN

EXT MIC IN



PEGATRON	Title : AUD(1)_ALC269	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 36 of 99	



PEGATRON	Title : AUD(2)_AMP,JACK	
BG1VHW1	Engineer: Kuansheng Yang	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 37 of 99	

PEGATRON Title : AUD(3)_FM2010

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

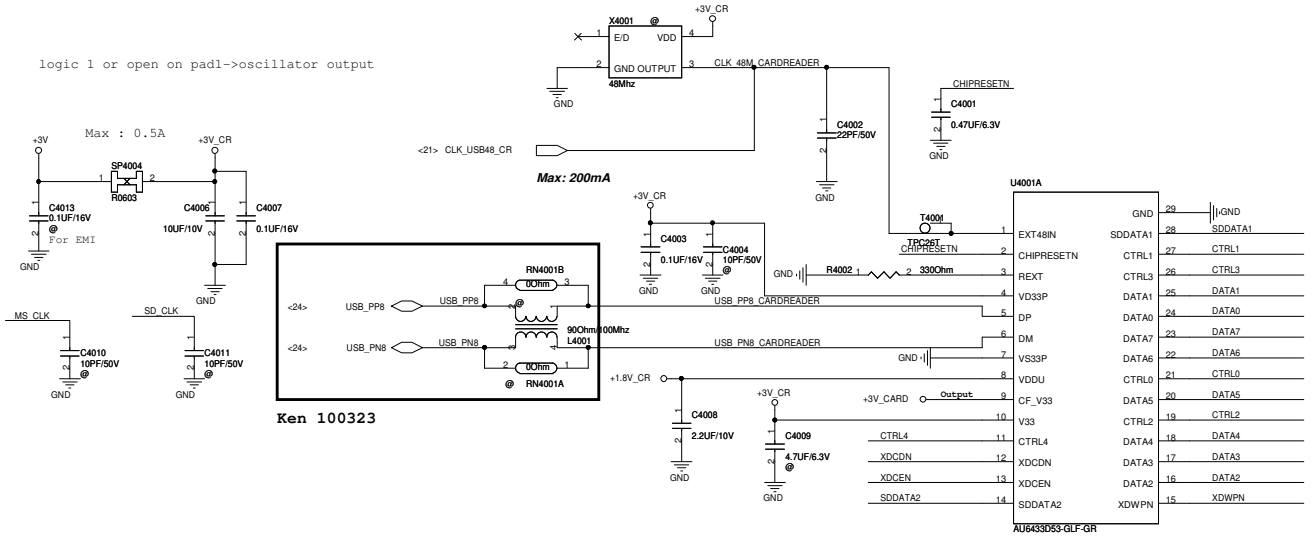
Date: Monday, May 10, 2010 Sheet 38 of 99

PEGATRON Title : AUD(4)_****

BG1\HW1 Engineer: *Kuansheng Yang*

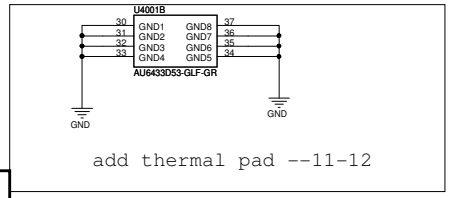
Size	Project Name	Rev
Custom	H36Y_U30X10	1.0

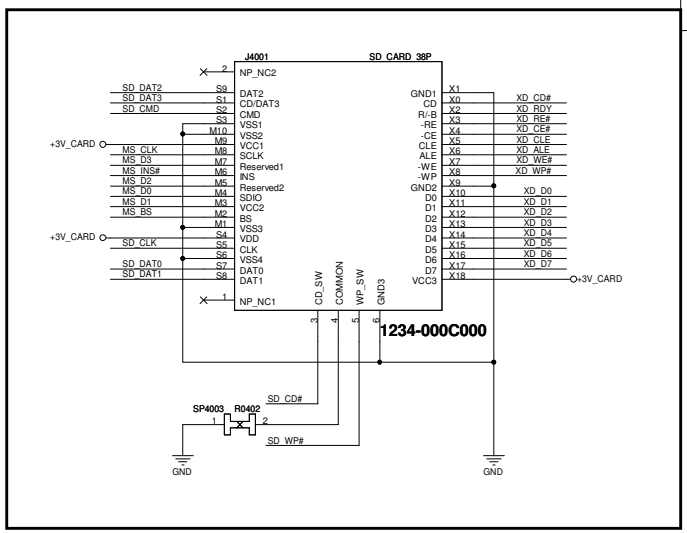
Date: Monday, May 10, 2010 Sheet 39 of 99

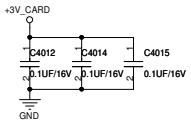


Pin Name	Description
CTRL4	XDRDN/ MSINS
XDCDN	XDCDN
XDCEN	XDCEN
SDDATA2	SDDATA2
XDWPN	XDWPN
DATA2	XDDATA2/ MSDATA2
DATA3	SDDATA3/ XDDATA3/ MSDATA3
DATA4	SDDATA4/ XDDATA4/ MSDATA4
CTRL2	SDCMD/ XDRBN
DATA5	SDDATA5/ XDDATA5/ MSDATA5
CTRL0	SDCLK/ XDALE/ MSBS
DATA6	SDDATA6/ XDDATA6/ MSDATA6
DATA7	SDDATA7/ XDDATA7/ MSDATA7
DATA0	SDDATA0/ XDDATA0/ MSDATA0
DATA1	XDDATA1/ MSDATA1
CTRL3	SDCDN/ XDWRN
CTRL1	SDWP/ XDCLE/ MSCLK
SDDATA1	SDDATA1

CTRL4		XD_RE#	MS_INS#
XDCDN		XD_CD#	
XDCEN		XD_CE#	
SDDATA2	SD_DAT2		
XDWPN		XD_WP#	
DATA2		XD_D2	MS_D2
DATA3	SD_DAT3	XD_D3	MS_D3
DATA4	SD_DAT4	XD_D4	MS_D4
CTRL2	SD_CMD	XD_RDY	
DATA5	SD_DAT5	XD_D5	MS_D5
CTRL0	SD_CLK	XD_ALE	MS_BS
DATA6	SD_DAT6	XD_D6	MS_D6
DATA7	SD_DAT7	XD_D7	MS_D7
DATA0	SD_DAT0	XD_D0	MS_D0
DATA1		XD_D1	MS_D1
CTRL3	SD_CD#	XD_WE#	
CTRL1	SD_WP#	XD_CLE	MS_CLK
SDDATA1	SD_DAT1		







PEGATRON	Title : ALCOR AU6433
BG1\HW1	Engineer: Kuansheng Yang
Size: C	Project Name: H36Y_U30X10
Rev: 1.0	
Date: Monday, May 10, 2010	Sheet 40 of 99

+3VS +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

PEGATRON Title : CB(2)_R5C833

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 41 of 99

+3VSO +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

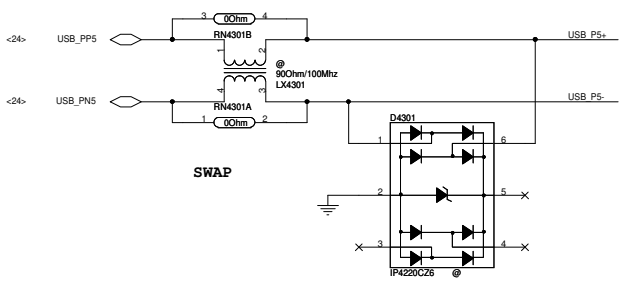
+12VO +12V <91>

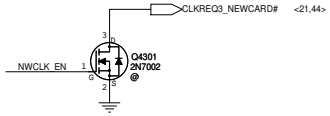
PEGATRON Title : CB(3)_4in1 CardReader

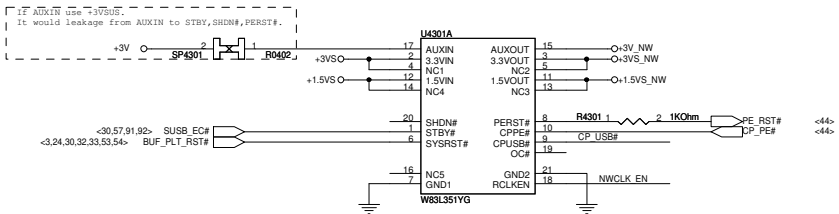
BG1VHW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

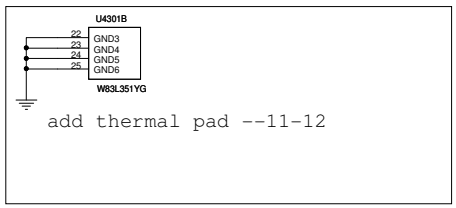
Date: Monday, May 10, 2010 Sheet 42 of 99

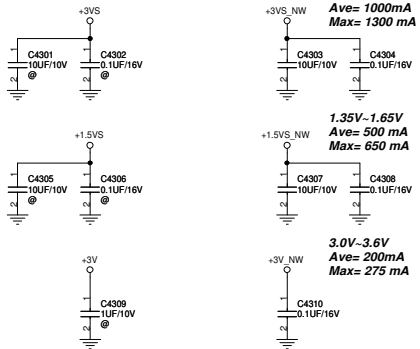


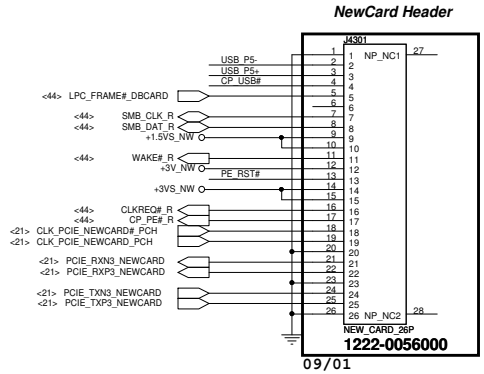




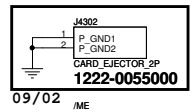
0629-000F000 WINBOND W83L351YG
0629-000U000 GMT G577CSR91U
0629-000A000 RICOH R5538D001





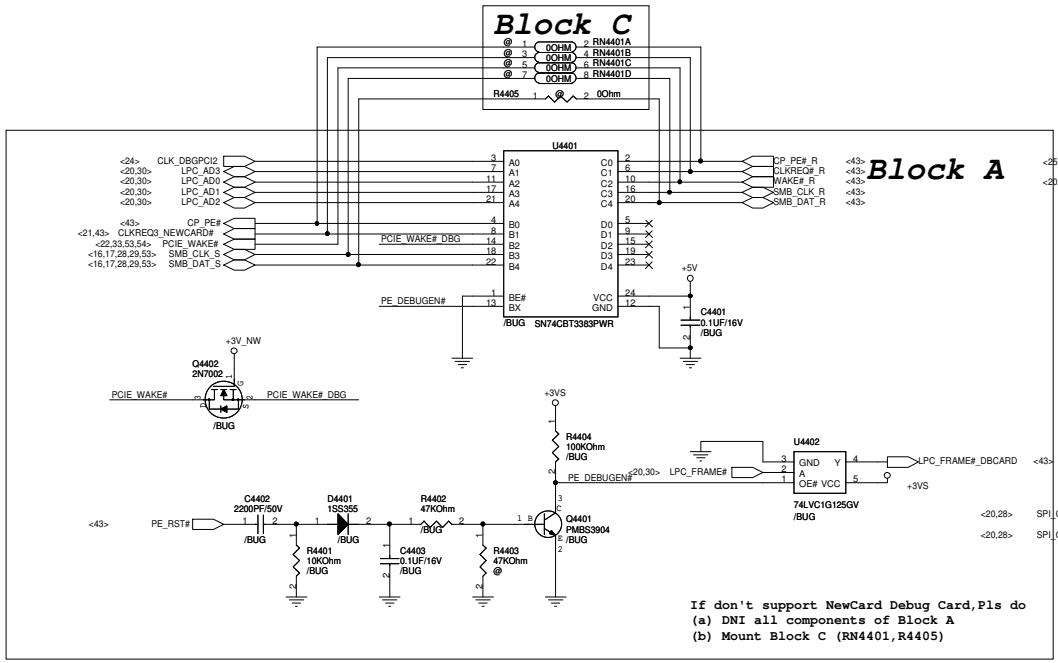


delete pin 27,28 net 09-14
kurt

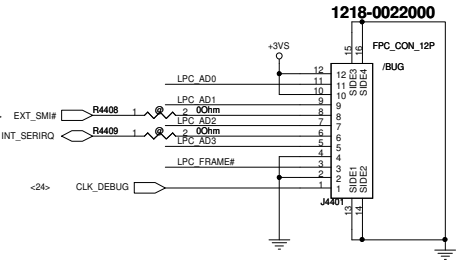


PEGATRON	Title : CB(4)_NewCard	
BG1VHW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 43 of 99	

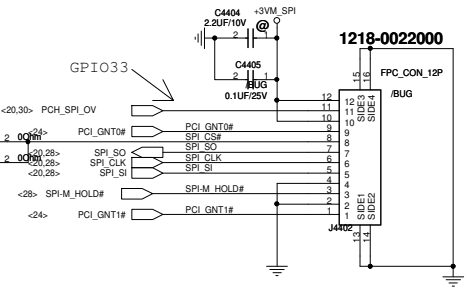
For NewCard Debug Card



LPC Debug Port



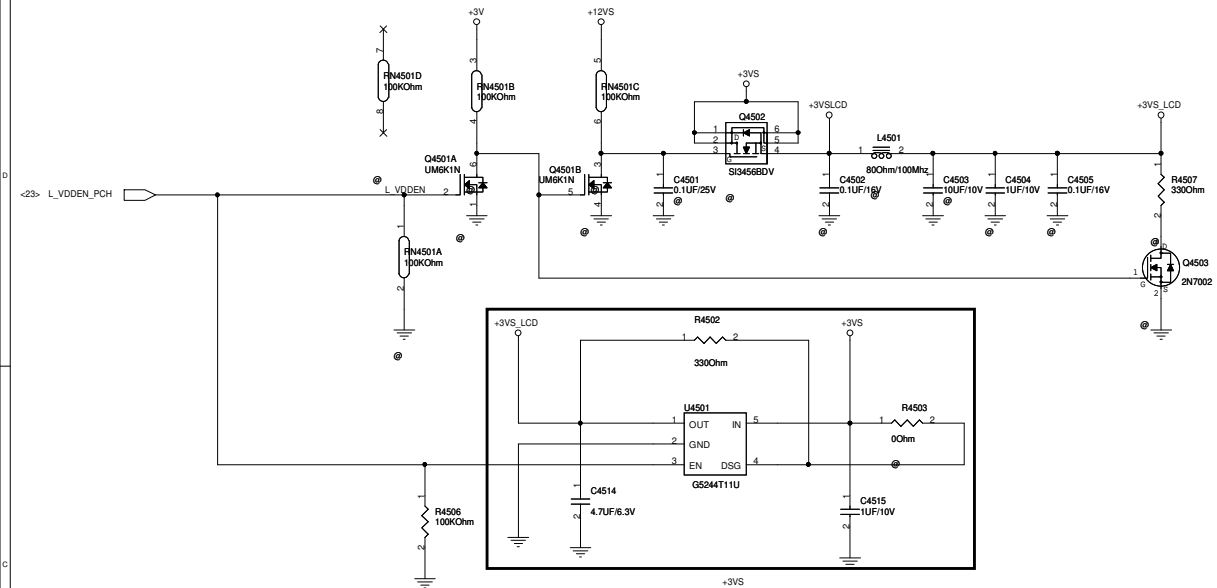
SPI Connecter Debug Connector

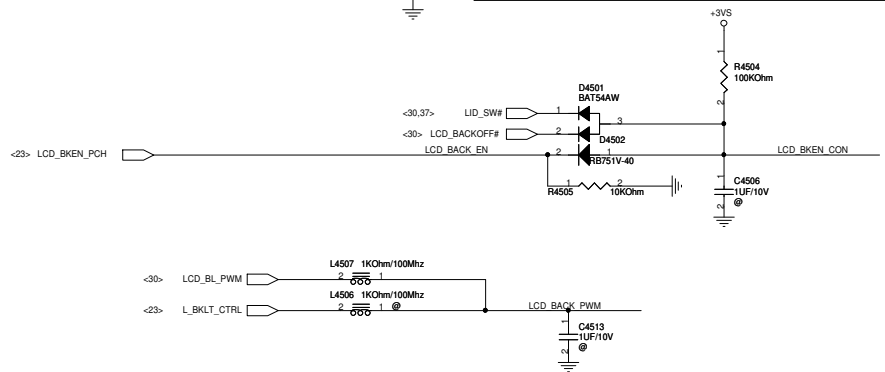


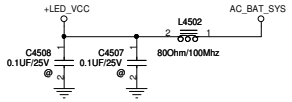
+5V +5V <52,54,56,57,85,91>

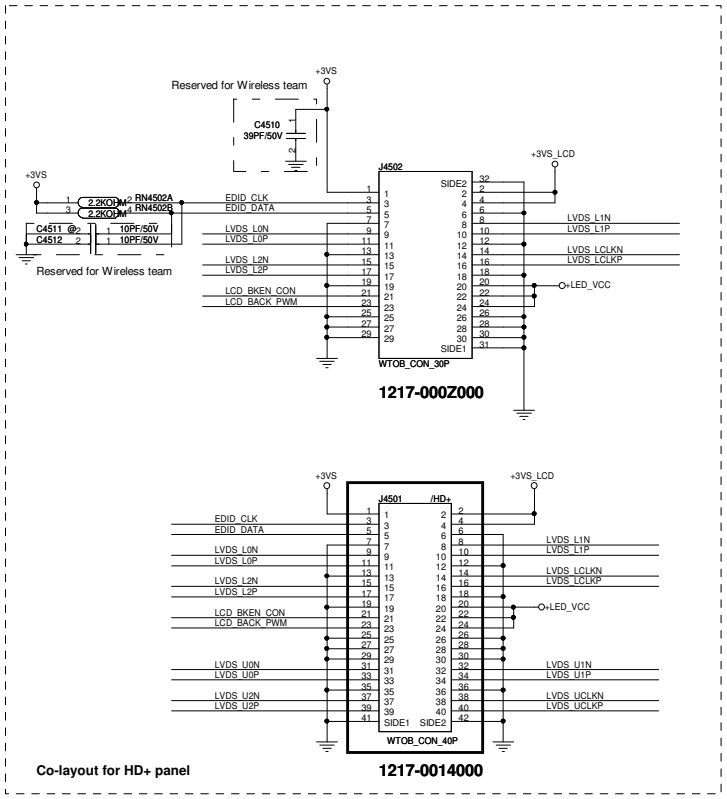
+3VS +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,45,46,48,50,51,53,56,57,66,80,86,91,92>

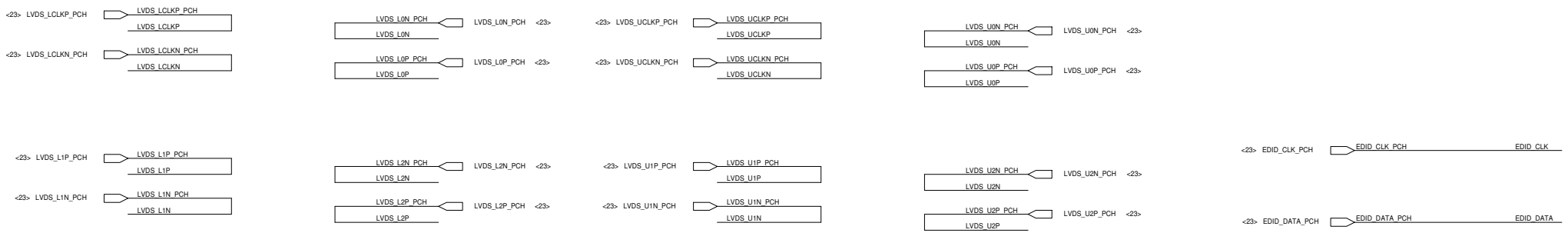
PEGATRON	Title : BUG_Debug	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 44 of 99	











IN=1 for VGA output
IN=0 for PCH output

2'nd source:0615-0002000

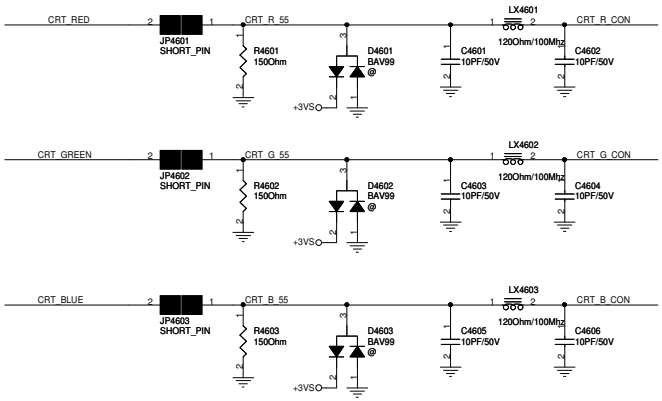
Default LVDS signal swing is 300mV.
For switchable graphics, 320mV is required.

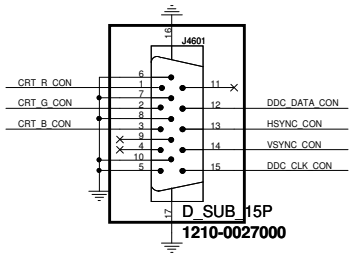
PEGATRON **Title : CRT(1)_LVDS**

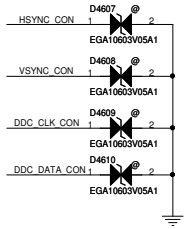
BG1\HW1 **Engineer: *Kuansheng Yang***

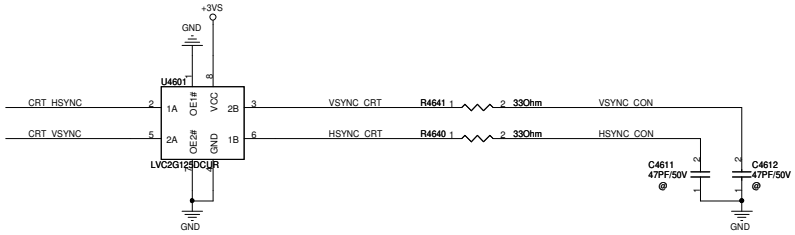
Size	Project Name	Rev
C	H36Y_U30X10	1.0

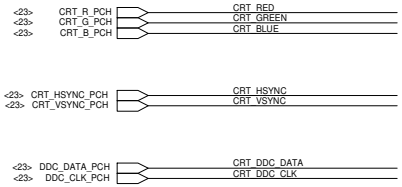
Date: Monday, May 10, 2010 Sheet 45 of 99

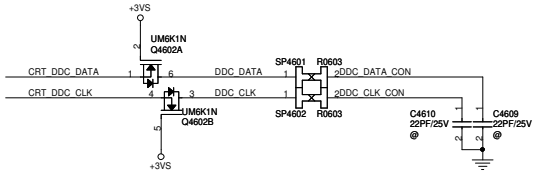


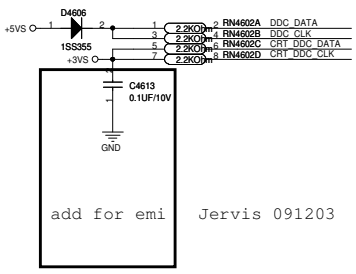












+3VS — +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,48,50,51,53,56,57,66,80,86,91,92>

+5V — +5V <44,52,54,56,57,85,91>

+5VS — +5VS <27,30,31,36,37,48,50,51,56,57,80,86,91>

PEGATRON Title : CRT(2)_D-Sub

BG1VHW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 46 of 99

R2.0

+3VS +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

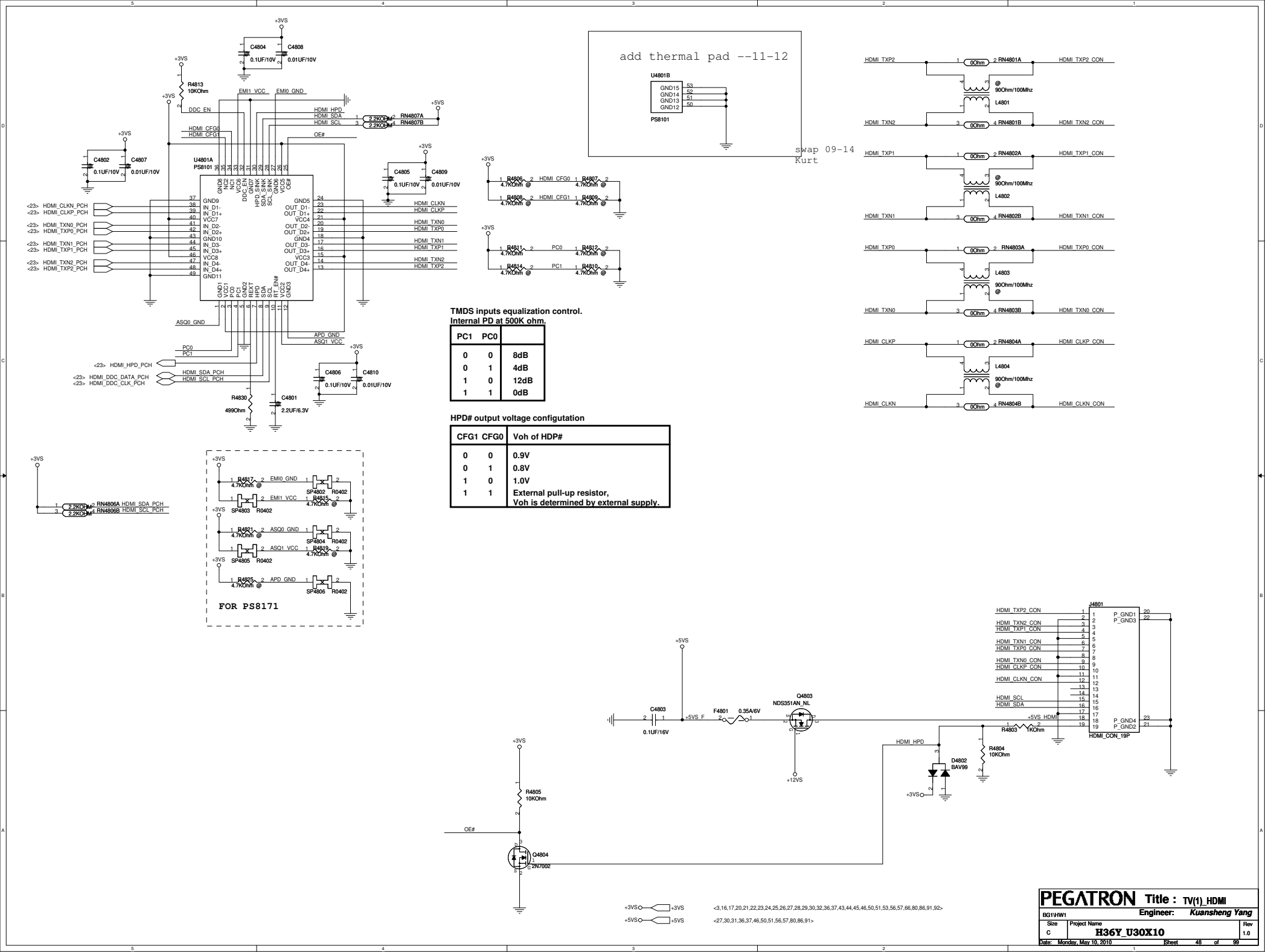
+5VS +5VS <27,30,31,36,37,46,48,50,51,56,57,80,86,91>

PEGATRON Title : CRT(3)_Display Port

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 47 of 99

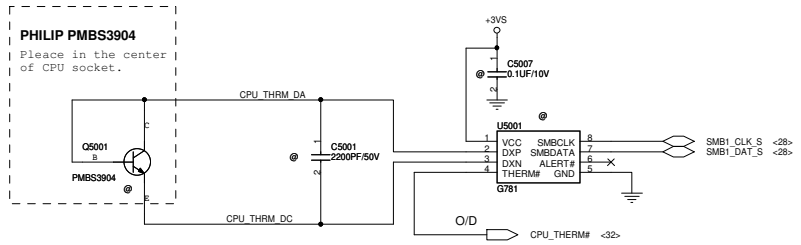

add thermal pad --11-12
swap 09-14
Kurt
U4801B
PS8101
U4801A
PS8101
TMDS inputs equalization control.
Internal PD at 500K ohm.
PC1 PC0
0 0 8dB
0 1 4dB
1 0 12dB
1 1 0dB
HPD# output voltage configutation
CFG1 CFG0 Voh of HDP#
0 0 0.9V
0 1 0.8V
1 0 1.0V
1 1 External pull-up resistor, Voh is determined by external supply.
FOR PS8171
J4801
HDMI_CON_19P
Q4803
NDS351AN_NL
Q4804
2N7002
D4802
BAV99
F4801 0.35A/6V
PEGATRON Title : TV(1)_HDMI
Engineer: Kuansheng Yang
BG1\HW1
Size C
Project Name H36Y_U30X10
Rev 1.0
Date: Monday, May 10, 2010
Sheet 48 of 99

PEGATRON	Title : TV(2)_****	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 49 of 99	

+3VSO +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,51,53,56,57,66,80,86,91,92>

+5VSO +5VS <27,30,31,36,37,46,48,51,56,57,80,86,91>

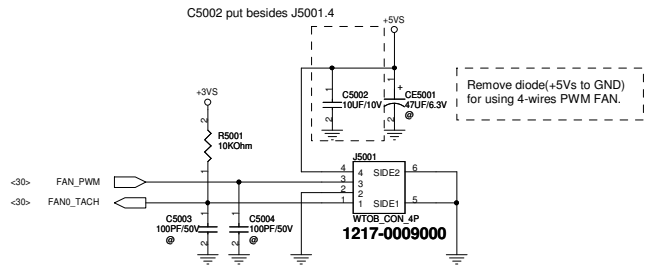
CPU Thermal Sensor



SMBUS addr=1001100x (98)

U5001: Remote(Local) thermal sensor,use remote mode.

PWM Fan



PEGATRON Title : FAN_Fan,Sensor

BG1\HW1 Engineer: *Kuansheng Yang*

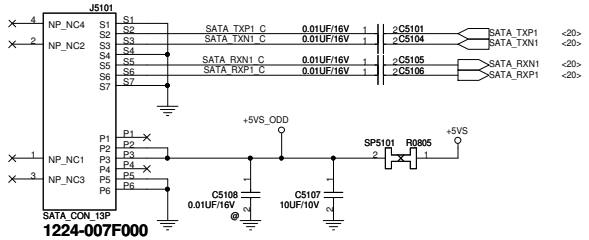
Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 50 of 99

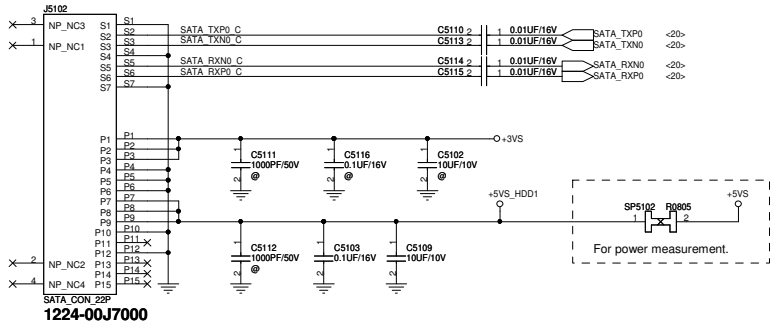
ODD

+3VS → +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,53,56,57,66,80,86,91,92>

+5VS → +5VS <27,30,31,36,37,46,48,50,56,57,80,86,91>

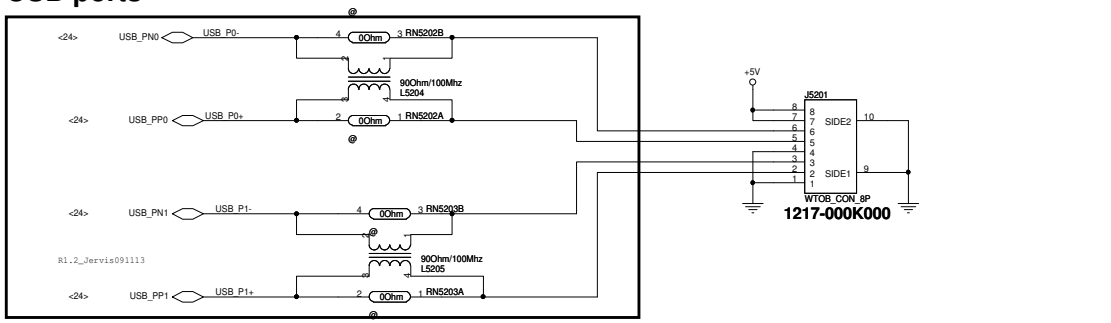


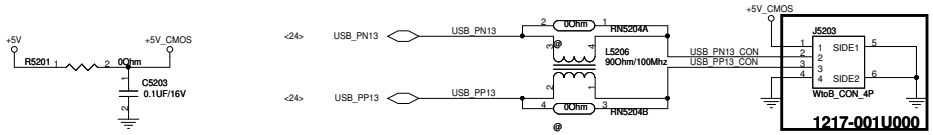
HDD

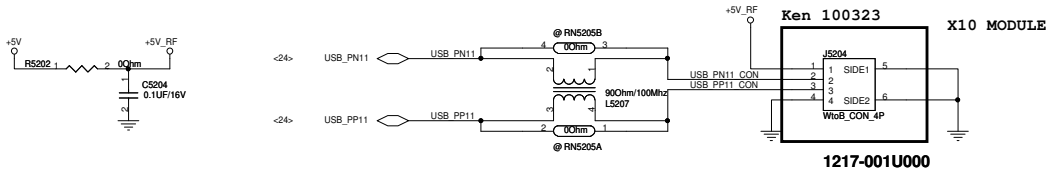


PEGATRON	Title : XDD_HDD,ODD	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 51 of 99	

USB ports

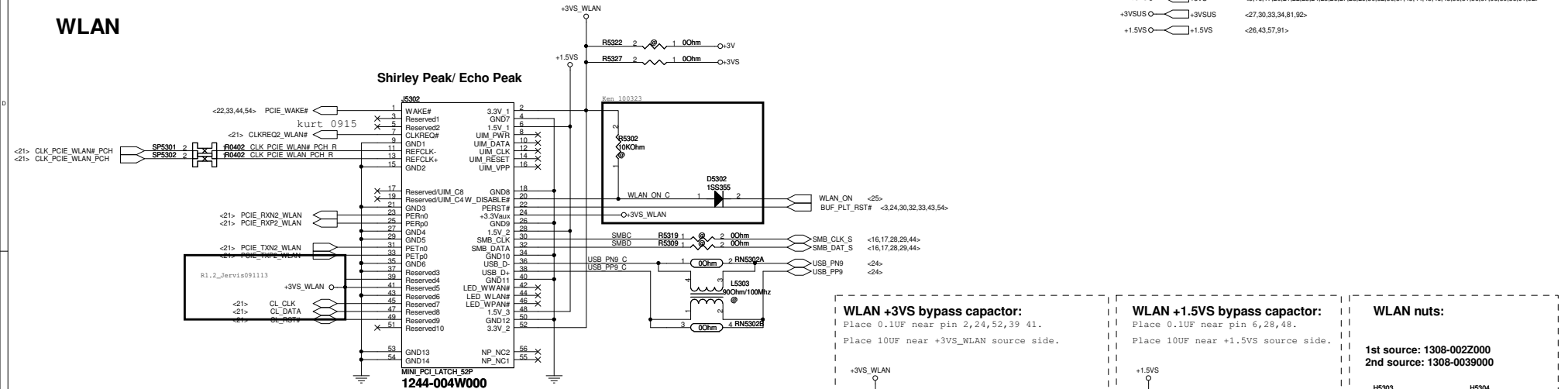






PEGATRON	Title : USB_USB Port	
BG1\HW1	Engineer: *Kuansheng Yang*	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 52 of 99	

WLAN



+3VS +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,56,57,66,80,86,91,92>

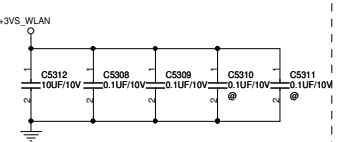
+3VSUS +3VSUS <27,30,33,34,81,92>

+1.5VS +1.5VS <26,43,57,91>

WLAN +3VS bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

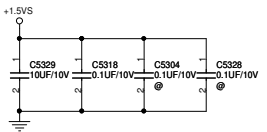
Place 10UF near +3VS_WLAN source side.



WLAN +1.5VS bypass capactor:

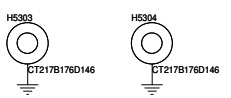
Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.



WLAN nuts:

1st source: 1308-002Z000
2nd source: 1308-0039000



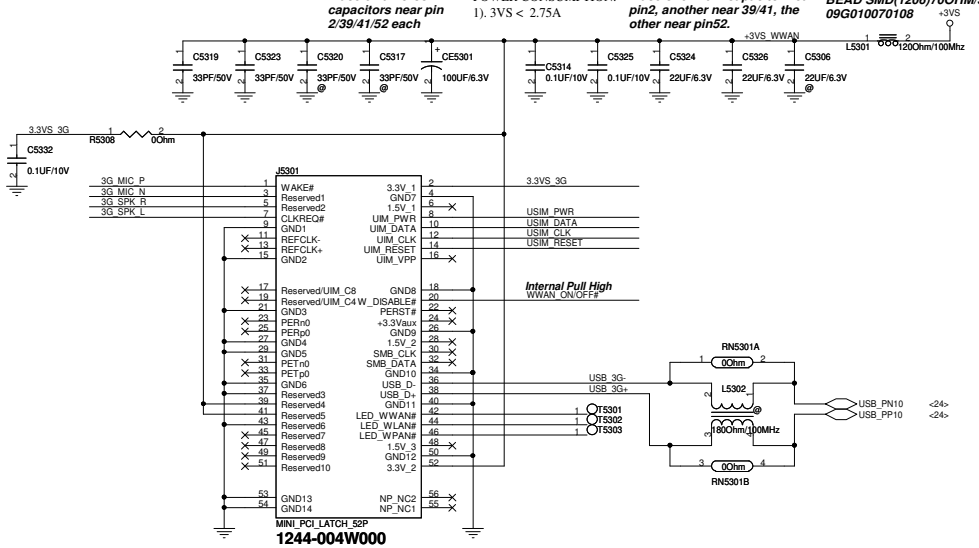
3G

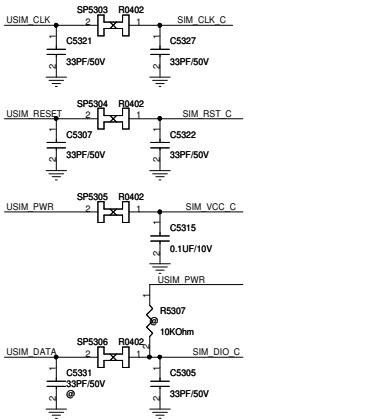
Place 0.1uF & 33PF capacitors near pin 2/39/41/52 each

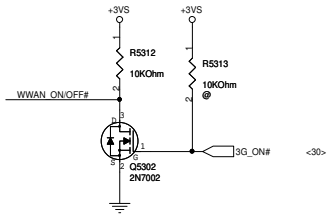
POWER CONSUMPTION:
1). 3VS < 2.75A

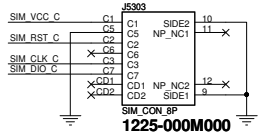
Place one 22uF capacitor near pin2, another near 39/41, the other near pin52.

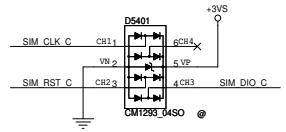
Option : BEAD SMD(1206)70OHM/3A 09G010070108

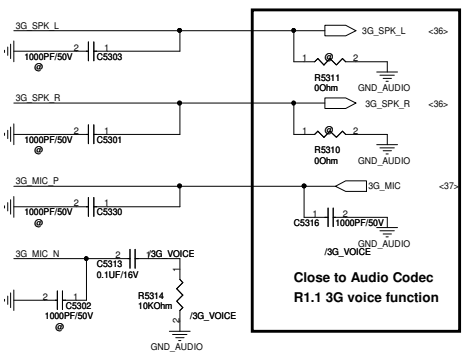




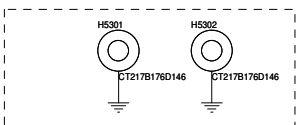




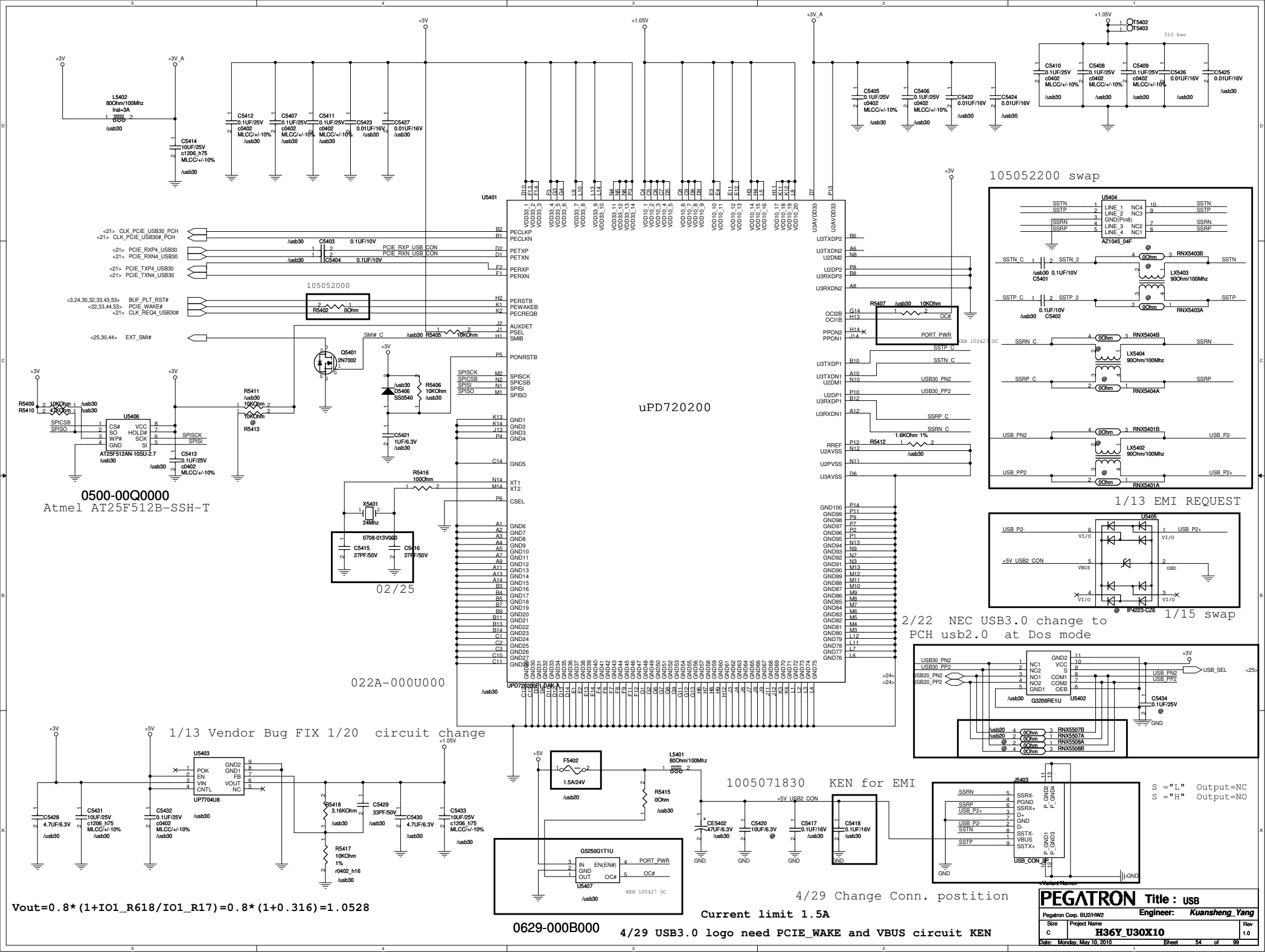




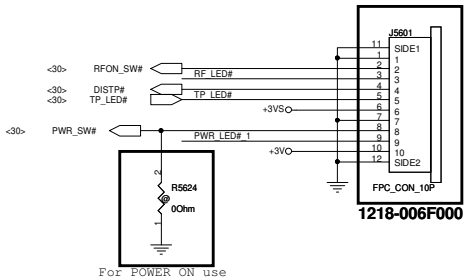
50-100 Ohm
For SE Mode



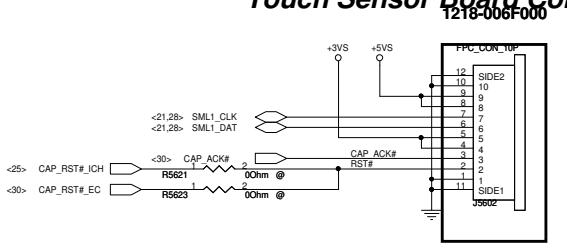
PEGATRON	Title : WLAN/ 3G	
BG1VHW1	Engineer: Kuansheng Yang	
Size: C	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 53 of 99	

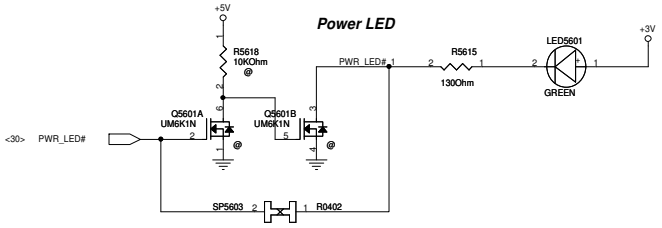

105052200 swap
105052000
uPD720200
0500-00Q0000
Atmel AT25F512B-SSH-T
022A-000U000
02/25
1/13 EMI REQUEST
1/15 swap
2/22 NEC USB3.0 change to
PCH usb2.0 at Dos mode
1/13 Vendor Bug FIX 1/20 circuit change
1005071830 KEN for EMI
S ="L" Output=NC
S ="H" Output=NO
Vout=0.8*(1+IO1_R618/IO1_R17)=0.8*(1+0.316)=1.0528
0629-000B000
Current limit 1.5A
4/29 Change Conn. postition
4/29 USB3.0 logo need PCIE_WAKE and VBUS circuit KEN
PEGATRON
Title : USB
Engineer: Kuansheng_Yang
Pegatron Corp. BU2/HW2
Size C
Project Name H36Y_U30X10
Rev 1.0
Date: Monday, May 10, 2010
Sheet 54 of 99

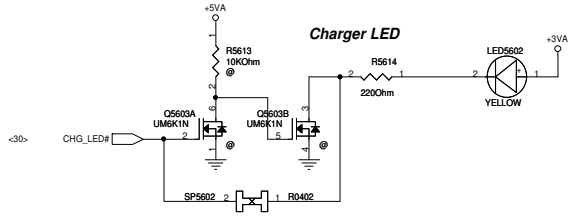
Power Switch Board Conn

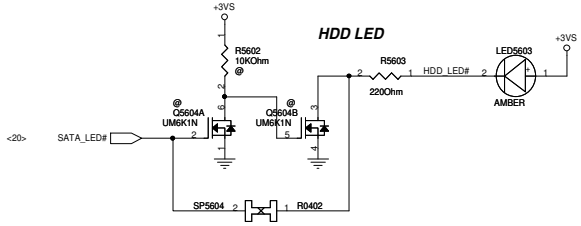


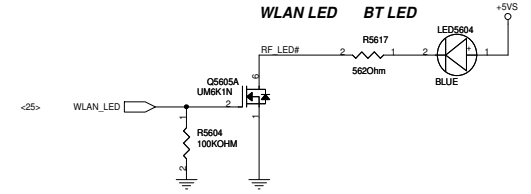
Touch Sensor Board Conn

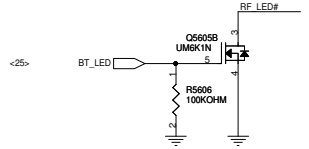


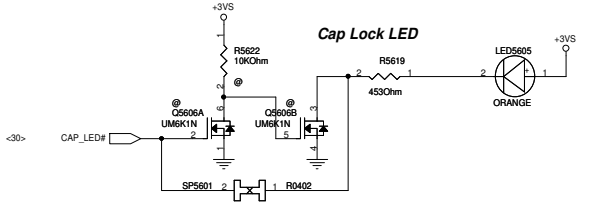












+3VA	+3VA	<20,30,37,57,81,93>
+3VS	+3VS	<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,57,66,80,86,91,92>
+5VSUS	+5VSUS	<27,81,91>
+5VA	+5VA	<81,82,88>
+5V	+5V	<44,52,54,57,85,91>
+5VS	+5VS	<27,30,31,36,37,46,48,50,51,57,80,86,91>
AC_BAT_SYS	AC_BAT_SYS	<45,80,81,82,83,86,88>

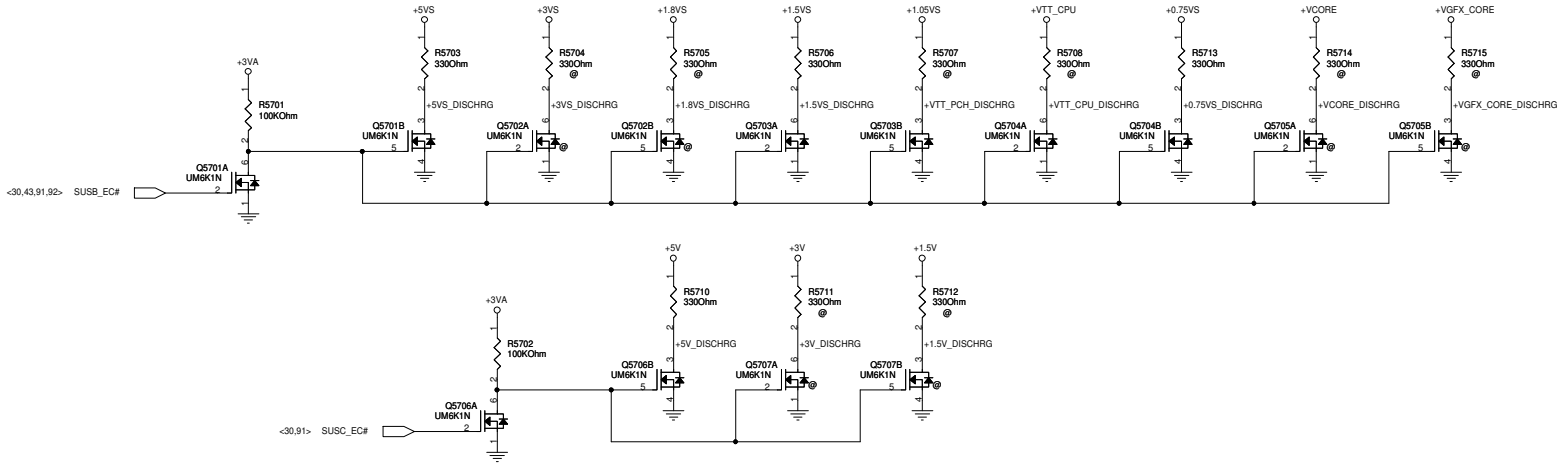
PEGATRON **Title : LED_Indicator**

BG1VHW1 **Engineer: *Kuansheng Yang***

Size	Project Name	Rev
C	**H36Y_U30X10**	1.0

Date: Monday, May 10, 2010 Sheet 56 of 99

+3VA	+3VA	<20,30,37,56,81,93>
+VCORE	+VCORE	<6,80>
+VGFX_CORE	+VGFX_CORE	<6,86,91>
+VTT_CPU	+VTT_CPU	<3,6,25,26,32,82>
+0.75VS	+0.75VS	<16,17,83>
+1.05VS	+1.05VS	<26,27,29,80,82>
+1.5VS	+1.5VS	<26,43,53,91>
+1.8VS	+1.8VS	<6,26,85>
+3VS	+3VS	<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,66,80,86,91,92>
+5VS	+5VS	<27,30,31,36,37,46,48,50,51,56,80,86,91>
+1.5V	+1.5V	<3,6,16,83>
+3V	+3V	<24,33,40,43,45,53,54,56,61,91>
+5V	+5V	<44,52,54,56,85,91>



PEGATRON **Title : DSG_Discharge**

BG1\HW1 **Engineer: *Kuansheng Yang***

Size	Project Name	Rev
C	**H36Y_U30X10**	1.0

Date: Monday, May 10, 2010 Sheet 57 of 99

PEGATRON Title : PCI_****

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 58 of 99

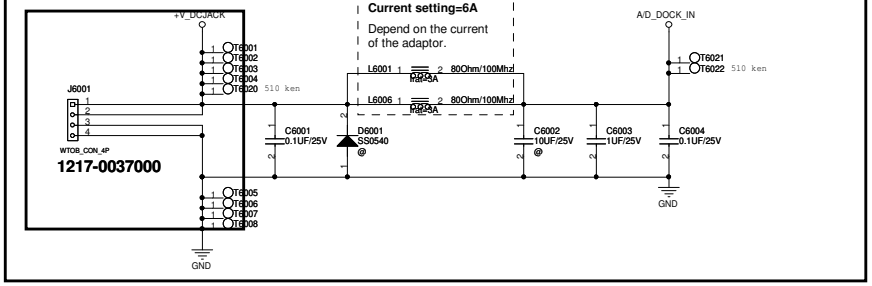
PEGATRON Title : DJ_****

BG1\HW1 Engineer: *Kuansheng Yang*

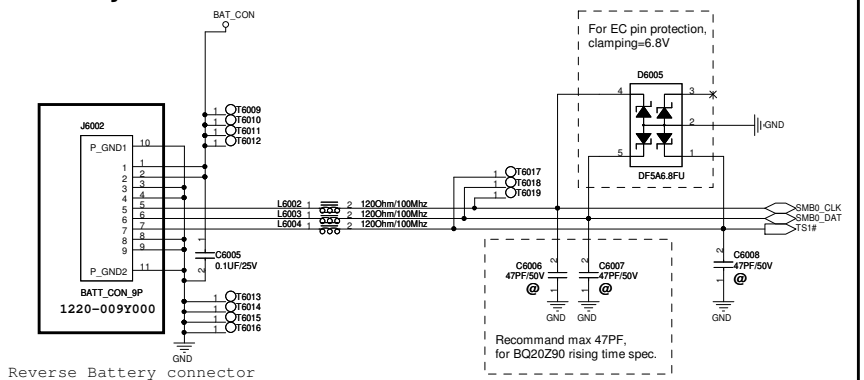
Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 59 of 99

DC Jack WtoB CONN



Battery Connector



Reverse Battery connector

Jervis-R1.1

+VCC_RTC	+VCC_RTC	<20,27>
+3VA_EC	+3VA_EC	<30,32>
+3VA	+3VA	<20,30,37,56,57,81,93>
+5VA	+5VA	<56,81,82,88>
+3VSUS	+3VSUS	<27,30,33,34,81,92>
+5VSUS	+5VSUS	<27,81,91>
+12VSUS	+12VSUS	<28,81,91>
+1.5V	+1.5V	<3,6,16,57,83>
+3V	+3V	<24,33,40,43,45,53,54,56,57,61,91>
+5V	+5V	<44,52,54,56,57,85,91>
+12V	+12V	<91>
+0.75VS	+0.75VS	<16,17,57,83>
+1.05VS	+1.05VS	<26,27,29,57,80,82>
+1.5VS	+1.5VS	<26,43,53,57,91>
+1.8VS	+1.8VS	<6,26,57,85>
+3VS	+3VS	<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+5VS	+5VS	<27,30,31,36,37,46,48,50,51,56,57,80,86,91>
+12VS	+12VS	<28,45,48,91>

AC_BAT_SYS	AC_BAT_SYS	<45,80,81,82,83,86,88>
A/D_DOCK_IN	A/D_DOCK_IN	<88>
BAT_CON	BAT_CON	<88>
+1.5V_DDR3	+1.5V_DDR3	<16,17,18>
+VTT_CPU	+VTT_CPU	<3,6,25,26,32,57,82>
+VCORE	+VCORE	<6,57,80>
+VGFX_CORE	+VGFX_CORE	<6,57,86,91>
+VTT_PCH_ORG	+VTT_PCH_ORG	<21,22,26,27>
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	<20,26,27>
+1.05VM_ORG	+1.05VM_ORG	<27>
+V_NVRAM_VCCQ	+V_NVRAM_VCCQ	<26>
M_VREFCA_DIMM0	M_VREFCA_DIMM0	<16,18>
M_VREFDQ_DIMM0	M_VREFDQ_DIMM0	<16,18>
M_VREFCA_DIMM1	M_VREFCA_DIMM1	<17,18>
M_VREFDQ_DIMM1	M_VREFDQ_DIMM1	<17,18>

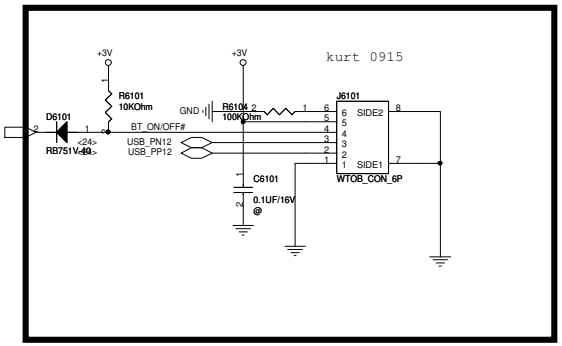
PEGATRON Title : DC_DC/BAT CONN

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 60 of 99

+3V +3V <24,33,40,43,45,53,54,56,57,91>



PEGATRON Title : BT_Bluetooth

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 61 of 99

PEGATRON Title : TPM_****

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 62 of 99

PEGATRON Title : N/A

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 63 of 99

PEGATRON Title : TUN_TV Tuner

BG1\HW1 Engineer: *Kuansheng Yang*

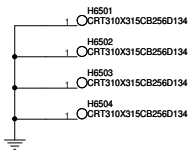
Size	Project Name	Rev
C	H36Y_U30X10	1.0

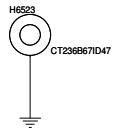
Date: Monday, May 10, 2010 Sheet 64 of 99

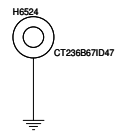
Change H6509 PARTNUMBER TO s04498

R1.1_Jervis091023

CPU Bracket Hole



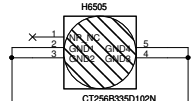


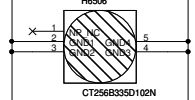


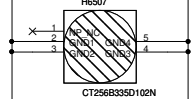
add nut h6523,h6524 for sb heat

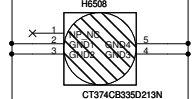
R1.1_Jervis091023

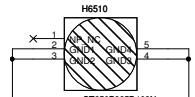
Screw Hole
Drill 2.6mm
Top Ring 6.5mm
Bot Ring 8.5mm

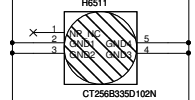


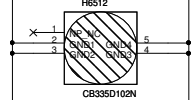


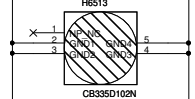


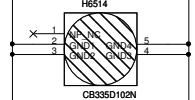


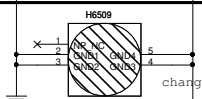








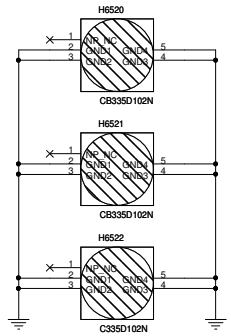




change H6509 partnumber to s04545

R1.2_Jervis091116

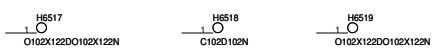
Screw Hole
Drill 2.6mm
Top Ring 8.5mm
Bot Ring 8.5mm



change H6512,H6513,H6514,H6520,H6521 partnumber to s04545

R1.1_Jervis091023

Tooling Hole



PEGATRON **Title : ME_CONN,Skew Hole**

BG1\HW1 **Engineer:** ***Kuansheng Yang***

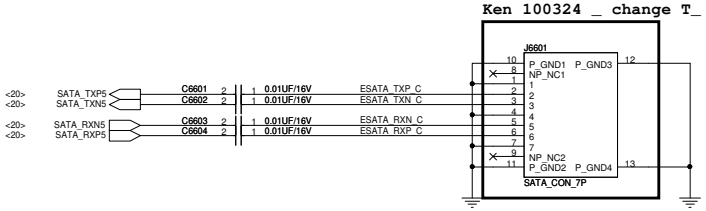
Size	Project Name	Rev
C	**H36Y_U30X10**	1.0

Date: Monday, May 10, 2010 Sheet 65 of 99

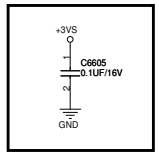
+3VS +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,80,86,91,92>

+1.8VS +1.8VS <6,26,57,85>

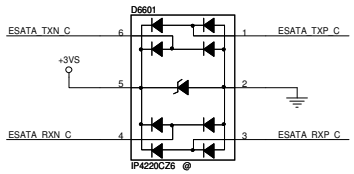
Ken 100324 _ change T_



Ken 1005071830 for EMI



for EMI request,delete ESATA_GND
09-17



PEGATRON Title : ESA_ESATA

BG1\HW1 Engineer: Kuansheng Yang

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 66 of 99

PEGATRON Title : ONFI

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 67 of 99

PEGATRON Title : N/A

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 68 of 99

PEGATRON Title : OTH

BG1\HW1 Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 69 of 99

PEGATRON Title : VGA Main (1)

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 70 of 99

PEGATRON Title : <Title>

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 71 of 99

PEGATRON Title : VRAM Channel A

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 72 of 99

PEGATRON Title : <Title>

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 73 of 99

PEGATRON Title : MEMORY INTERFACE

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 74 of 99

PEGATRON	Title : POWER (1)	
PEGATRON	Engineer: *Kuansheng Yang*	
Size: Custom	Project Name: H36Y_U30X10	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 75 of 99	

PEGATRON Title : POWER (2)

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 76 of 99

PEGATRON Title : <Title>

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 77 of 99

PEGATRON Title : STRAP

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

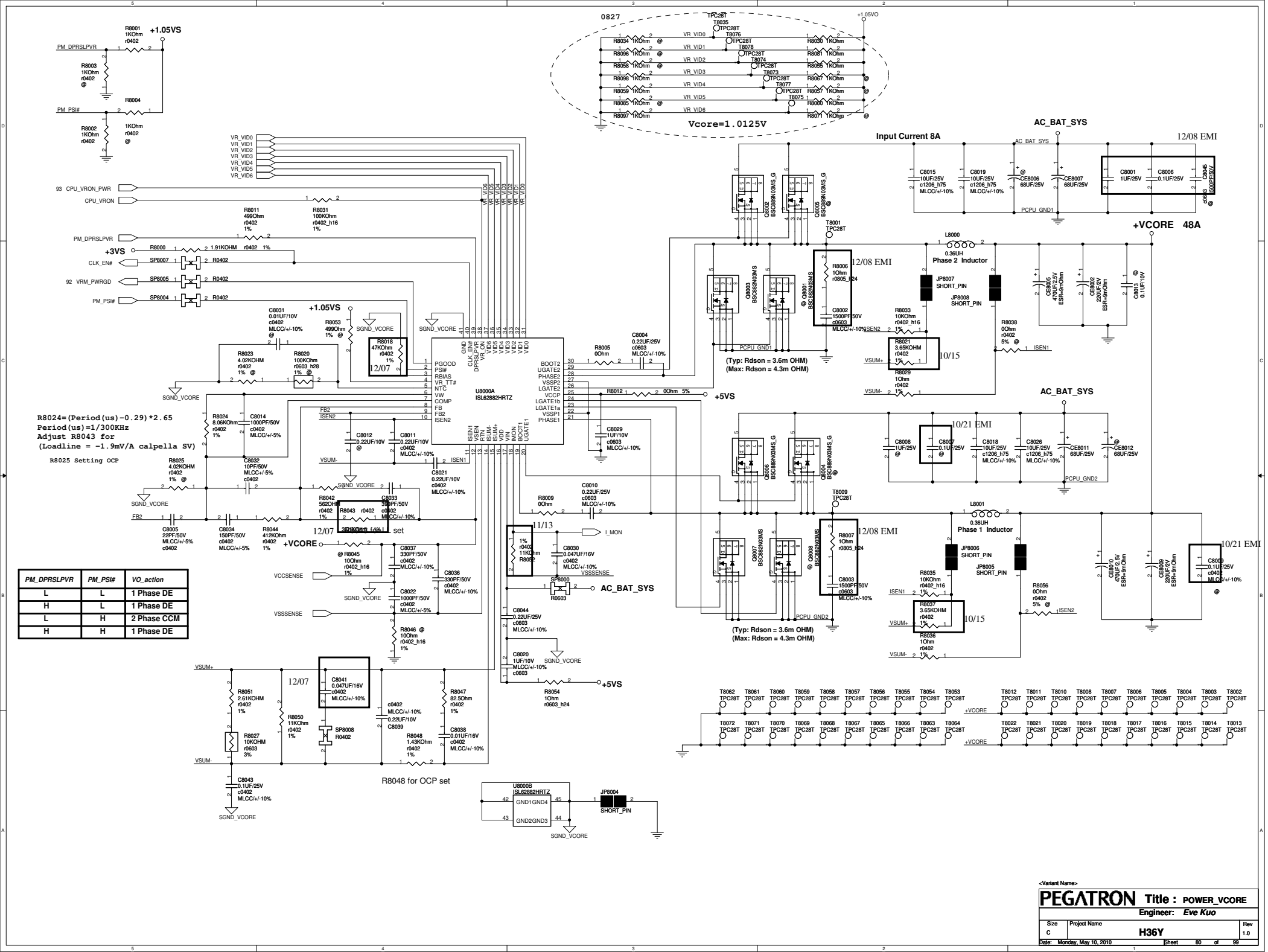
Date: Monday, May 10, 2010 Sheet 78 of 99

PEGATRON Title : <Title>

<OrgName> Engineer: *Kuansheng Yang*

Size	Project Name	Rev
C	H36Y_U30X10	1.0

Date: Monday, May 10, 2010 Sheet 79 of 99



PM_DPRSLPVR	PM_PSI#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

SKIP:
GND : DEM operation;
REF : Ultrasonic Mode operation;
VCC : PWM operation.

VENLDO:
Rising Edge:Max:2V;Typ:1.6V;Min:1.2V
Falling Edge:Max:1.06V;Typ:1V;Min:0.94V

TON:(5V/3.3V)
VCC:(200kHz/250kHz)
REF:(300kHz/375kHz)
GND:(400kHz/500kHz)

82,83,85,91,93 SUSB#_PWR

R8106 0Ohm r0402_h16
R8129 REF 0Ohm @ SKIP#
R8105 0Ohm r0402_h16 @

AC_BAT_SYS

U8101B RT8206AGQW
34 GND3
35 GND4
36 GND5
37 GND6
SGND_3V_5V

Input Current 3A

C8101 0.1UF/25V @
C8118 10UF/25V c1206_h75 MLCC/+/-10%
C8112 0.1UF/25V c0603
R8146 150KOHM 1% @
C8108 4.7UF/6.3V c0603
SP8106 R0603
R8102 0Ohm @
C8115 1UF/10V @
R8125 220KOhm r0402 1% Separate
R8124 316KOhm 1%
C8109 0.22UF/25V c0603 MLCC/+/-10%
R8107 0Ohm
R8101 0Ohm @
R8141 0Ohm @
C8113 1UF/10V c0603 MLCC/+/-10%
R8100 0Ohm @
R8128 10Ohm r0603_h24 5%
+5VAO
10/14
10/06

U8101A RT8206AGQW
BYP, VOUT1, FB1, ILIM1, PGOOD1, EN1, UGATE1, PHASE1
GND2, FB2, ILIM2, VOUT2, SKIP#, PGOOD2, EN2, UGATE2, PHASE2
BOOT1, UGATE1, VCC, SECFB, GND, LGATE2, BOOT2
+3VO_FB, SKIP# SP8105 R0603, ENBL, DL1

VOUT:Typ.=5.09V;Max.=5.217V;Min.=4.966V;T=2.5%
OCP setting 5.5A (5V:300kHz)

+5VO (Max:5.39A)
+5VSUS 0.01A
JP8102 @ 1MM_OPEN_5MIL
L8101 3.3UH DCR:Typ=28mOhm;Max=30mOhm
R8115 2.2Ohm r0805_h24 @ 5%
Q8101 SI4134DY-T1-GE3
C8103 1UF/10V @
CE8101 100UF/6.3V
JP8105 SHORT_PIN
JP8111 SHORT_PIN
JP8109 SHORT_PIN
C8125 1500PF/50V c0603 MLCC/+/-10% @
R8103 2.2Ohm
R8104 4.7OHM
C8110 0.1UF/25V MLCC/+/-10% c0603
C8111 0.1UF/25V c0603 MLCC/+/-10%
C8137 47PF/50V c0402 MLCC/+/-5%
C8114 1UF/10V c0603 MLCC/+/-10%
R8127 200KOhm r0402 1%
R8132 39KOHM r0402 1%
SECFB
+15VO
*SECFB:2V(T=4%)
JP8110 SHORT_PIN
92 SUS_PWRGD
SGND_3V_5V

JP8108 @ 1MM_OPEN_5MIL
+5VAO
+5VA
C8134 39PF/50V c0402 MLCC/+/-5% @
R8108 30.9KOhm r0402 1%
C8136 0.1UF/25V c0402 MLCC/+/-10% @
R8109 20KOhm r0402_h16 1%

(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)
FB1=2V(T=1.25%)

Input Current 3.3A

C8102 10UF/25V c1206_h75 MLCC/+/-10%
C8117 10UF/25V @
C8127 0.1UF/25V
C8139 1500PF/50V c0603 @
12/08 EMI
Q8102 SI4134DY-T1-GE3
10/15

VOUT:Typ.=3.32V;Max.=3.388V;Min.=3.253V;T=2.05%
OCP setting 12.4A (3.3V:375kHz)

+3VO (Max:8.894A)
L8100 4.7UH DCR:Typ=10.8mOhm;Max=11.8mOhm
10/28
JP8101 @ 1MM_OPEN_5MIL
+3VA (Max:0.12A)
R8116 1Ohm r0805_h24 @
10/21 EMI
Q8103 SI4134DY-T1-GE3
C8126 1500PF/50V c0603 MLCC/+/-10% @
C8100 1UF/10V @
CE8103 100UF/6.3V
JP8112 SHORT_PIN
JP8104 SHORT_PIN

(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)
FB1=2V(T=1.25%)

R8112 13.3KOHM r0402 1%
C8135 39PF/50V c0402 MLCC/+/-5% @
C8138 0.1UF/25V c0402 MLCC/+/-10% @
R8111 20KOhm r0402_h16 1%

+3VSUS

JP8107 close to Q8104
JP8107 SHORT_PIN
AC_BAT_SYS
+3VO
Q8104 SI3456CDV-T1-E3
10/06
+3VSUS 0.919A
R8130 84.5KOhm r0402 1%
R8131 560KOhm r0402_h16 5%
R8135 100KOhm r0402 5%
Q8106A UM6K1N
Q8106B UM6K1N
+5VAO
T8127 TPC26T
93 VSUS_ON
R8136 470KOhm r0402 5%
C8104 1000PF/50V c0402 MLCC/+/-5%
C8119 0.1UF/25V MLCC/+/-10% c0603 @

+12VSUS

+5VO
C8121 0.1UF/25V
C8120 0.1UF/25V
C8122 1UF/25V @
C8123 0.1UF/25V
+10VO
D8104 BAT54S
D8103 BAT54S
DL1
+15VO
C8124 1UF/25V
JP8106 @ 1MM_OPEN_5MIL
(Max:0.02A)
+12VSUS
VOUT:Typ.=12.256V;Max.=12.962V;Min.=11.571V;T=5.76%

TOTAL COUNT : 38 PCS

TPC26 T8160 T8158 T8159 +12VSUS
TPC26 T8154 T8152 T8153 +5VSUS
TPC26 T8147 T8148 T8142 +3VSUS
TPC26 T8129 T8106 T8115 +3VA
TPC26 T8139 T8141 T8138 +5VA
TPC26 T8110 T8103 T8114 T8120 +5VO
TPC26 T8134 T8132 T8135 T8121 +5VO
TPC26 T8117 T8107 T8109 T8122 +3VO
TPC26 T8123 T8128 T8136 T8124 +3VO
TPC26 T8104 T8108 T8116 T8126
TPC26 T8112 T8119 T8101 T8130
TPC26 T8105 T8111 T8118 T8137
TPC26 T8113 T8131 T8102 T8133

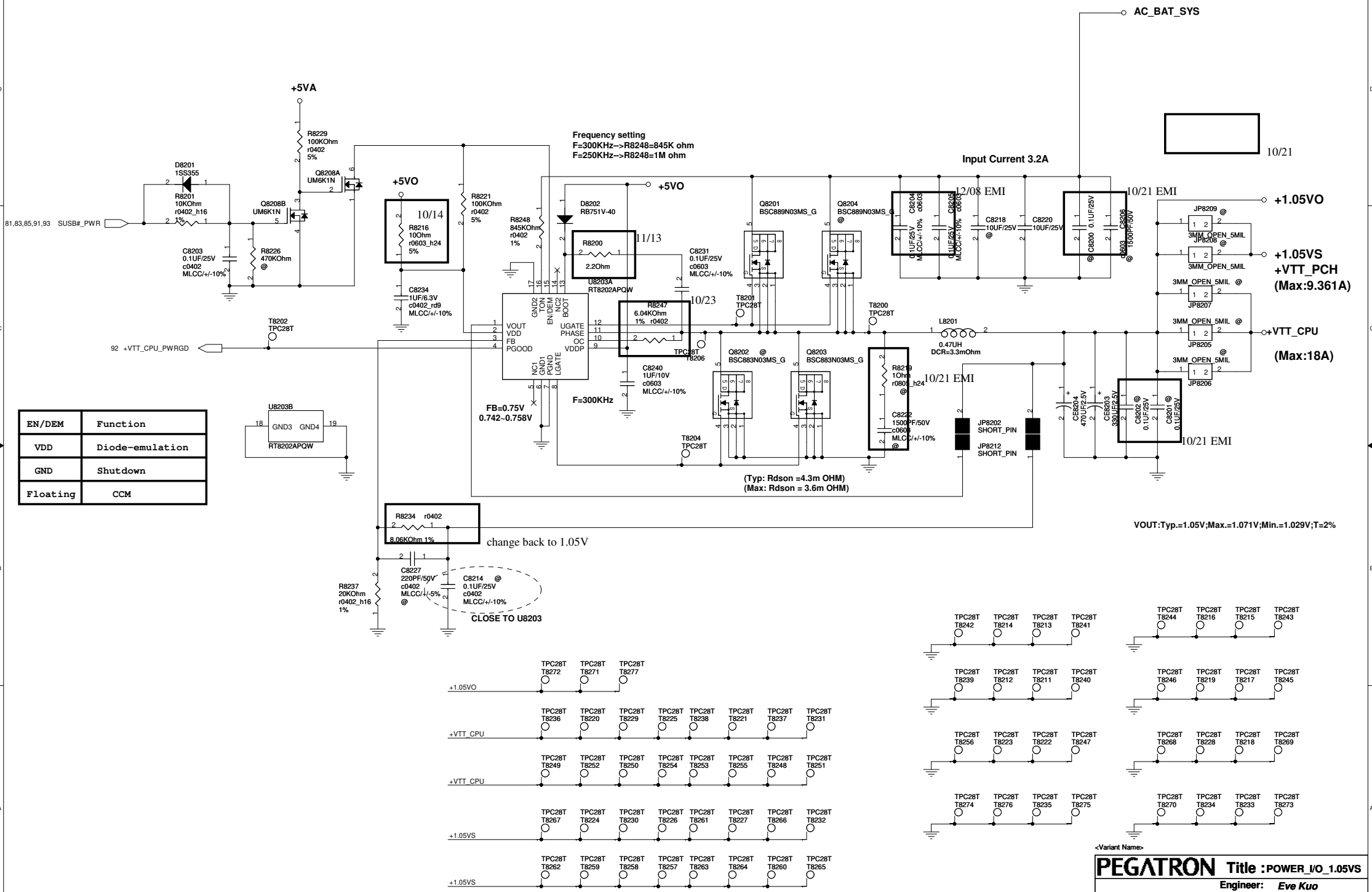
TPC26 T8150 T8149 T8151
TPC26 T8143 T8145 T8125
TPC26 T8163 T8161 T8162
TPC26 T8157 T8155 T8156
TPC26 T8146 T8140 T8144

<Variant Name>

PEGATRON Title :POWER_SYSTEM
Engineer: Eve Kuo

Size	Project Name	Rev
Custom	H36Y	1.0

Date: Monday, May 10, 2010 Sheet 81 of 99



EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM

+1.05VO: T8272 T8271 T8277

+VTT_CPU: T8236 T8220 T8229 T8225 T8238 T8221 T8237 T8231

+VTT_CPU: T8249 T8252 T8250 T8254 T8253 T8255 T8248 T8251

+1.05VS: T8267 T8224 T8230 T8226 T8261 T8227 T8266 T8232

+1.05VS: T8262 T8259 T8258 T8257 T8263 T8264 T8260 T8265

T8242 T8214 T8213 T8241

T8239 T8212 T8211 T8240

T8256 T8223 T8222 T8247

T8274 T8276 T8235 T8275

T8244 T8216 T8215 T8243

T8246 T8219 T8217 T8245

T8268 T8228 T8218 T8269

T8270 T8234 T8233 T8273

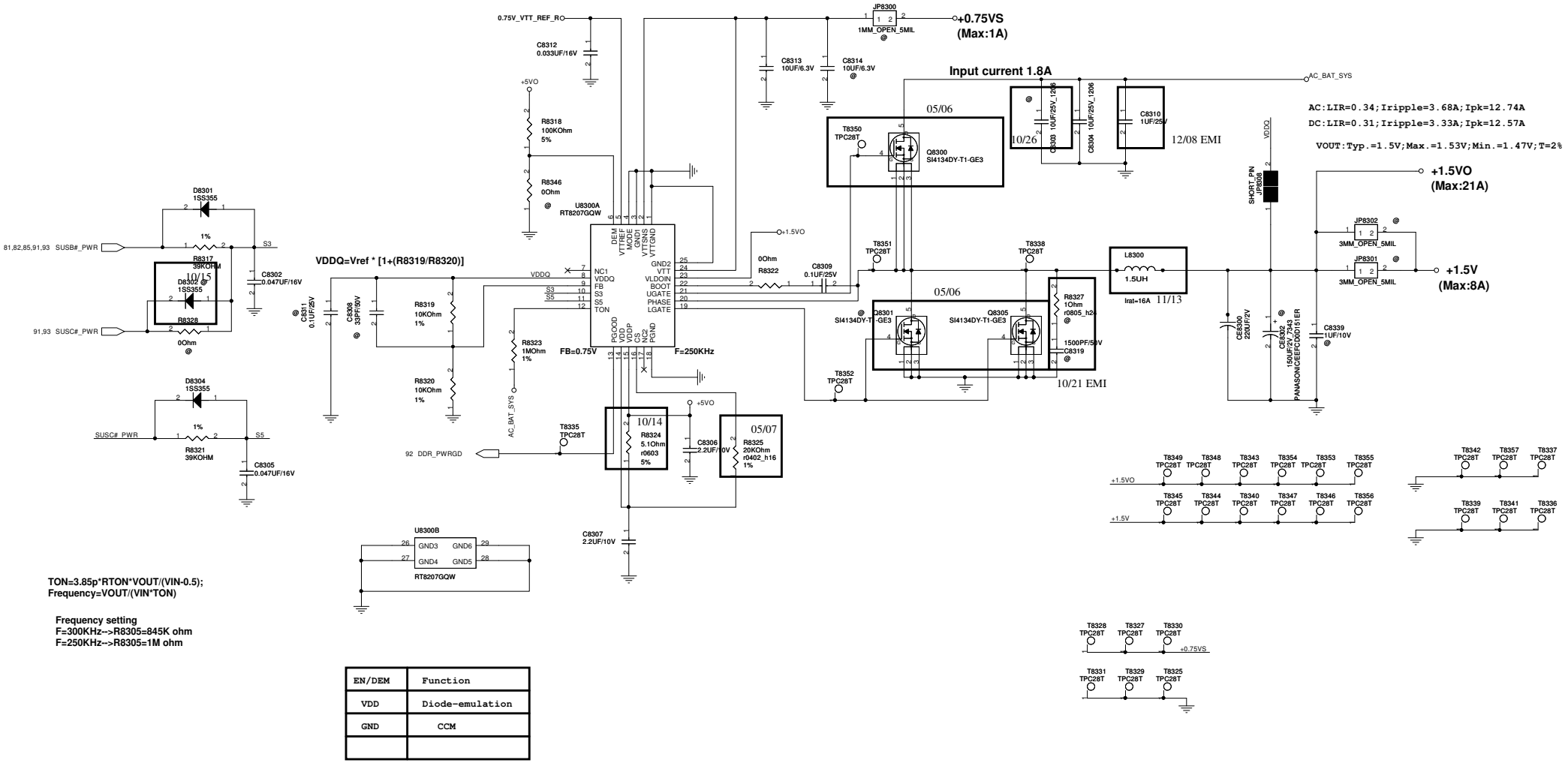
<Variant Name>

PEGATRON Title : POWER_I/O_1.05VS

Engineer: Eve Kuo

Size	Project Name	Rev
Custom	H36Y	1.0

Date: Monday, May 10, 2010 Sheet 82 of 99



TON=3.85p*RTON*VOUT/(VIN-0.5);
Frequency=VOUT/(VIN*TON)

Frequency setting
F=300KHz-->R8305=845K ohm
F=250KHz-->R8305=1M ohm

EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

PEGATRON **Title :** POWER_I/O_DDR & VTT

Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	H36Y	0.3

Date: Monday, May 10, 2010 Sheet 83 of 99

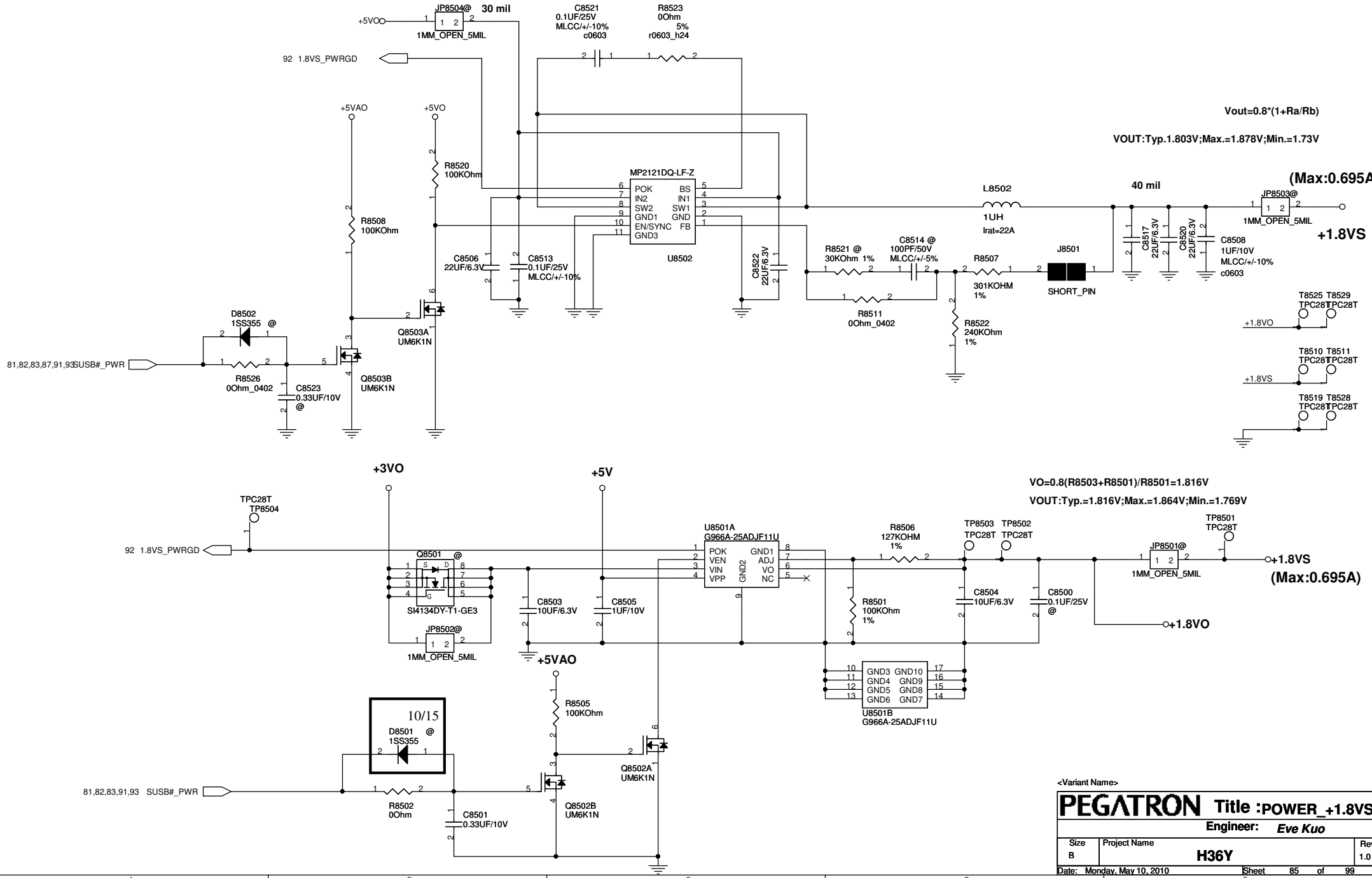
<Variant Name>

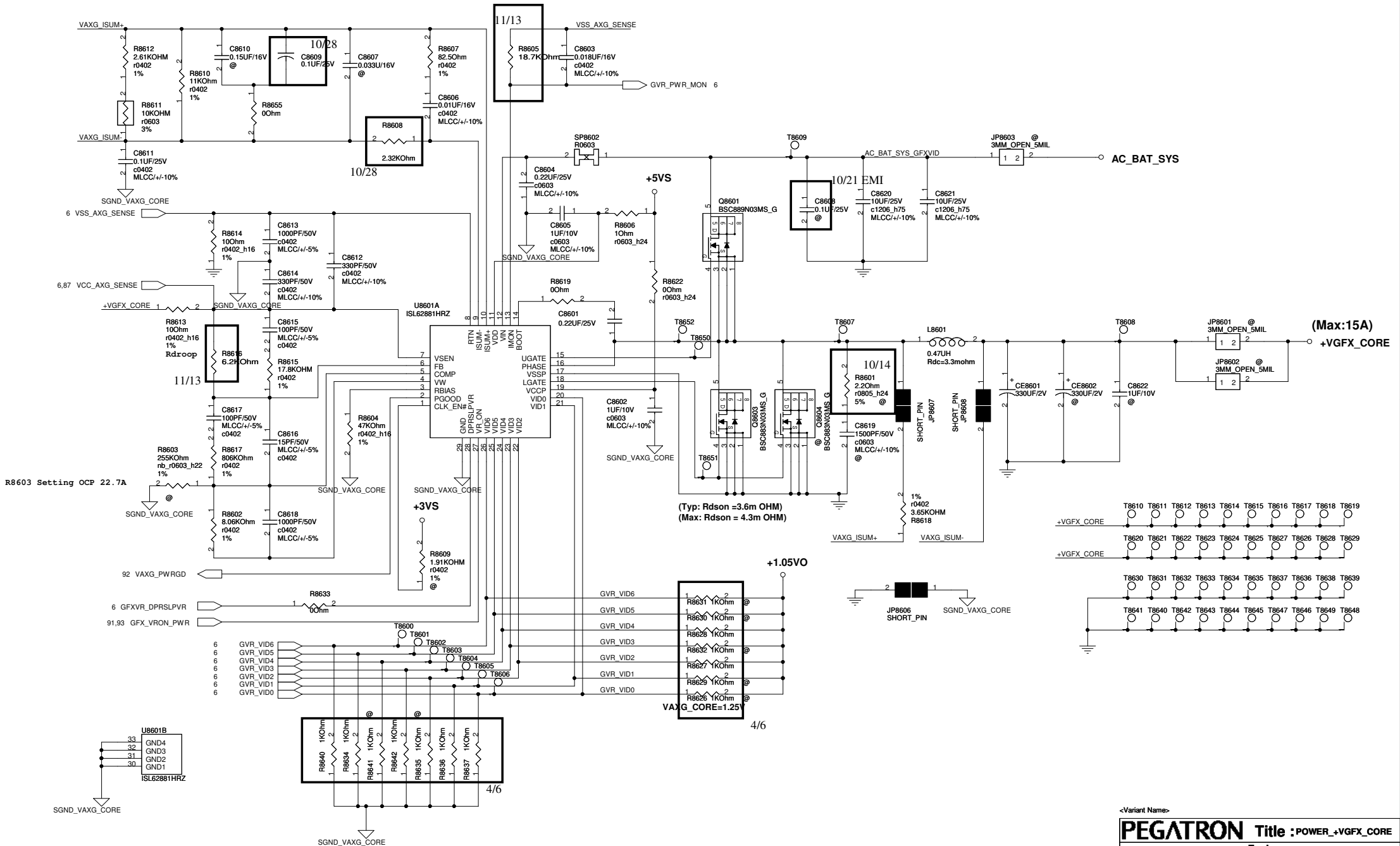
PEGATRON Title : POWER_I/O_1.05VS

Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	H36Y	1.0

Date: Monday, May 10, 2010 Sheet 84 of 99


JP8504@ 30 mil
1MM_OPEN_5MIL
+5VO
C8521
0.1UF/25V
MLCC/+/-10%
c0603
R8523
0Ohm
5%
r0603_h24
92 1.8VS_PWRGD
+5VAO
+5VO
R8520
100KOhm
R8508
100KOhm
MP2121DQ-LF-Z
POK
IN2
SW2
GND1
EN/SYNC
GND3
BS
IN1
SW1
GND
FB
U8502
C8506
22UF/6.3V
C8513
0.1UF/25V
MLCC/+/-10%
C8522
22UF/6.3V
L8502
1UH
Irat=22A
40 mil
JP8503@
1MM_OPEN_5MIL
+1.8VS
(Max:0.695A)
Vout=0.8*(1+Ra/Rb)
VOUT:Typ.1.803V;Max.=1.878V;Min.=1.73V
R8521 @
30KOhm 1%
C8514 @
100PF/50V
MLCC/+/-5%
R8507
301KOHM
1%
J8501
SHORT_PIN
R8511
0Ohm_0402
R8522
240KOhm
1%
C8517
22UF/6.3V
C8520
22UF/6.3V
C8508
1UF/10V
MLCC/+/-10%
c0603
D8502
1SS355 @
Q8503A
UM6K1N
81,82,83,87,91,93SUSB#_PWR
R8526
0Ohm_0402
C8523
0.33UF/10V
@
Q8503B
UM6K1N
T8525 T8529
TPC28T TPC28T
+1.8VO
T8510 T8511
TPC28T TPC28T
+1.8VS
T8519 T8528
TPC28T TPC28T
+3VO
+5V
TPC28T
TP8504
92 1.8VS_PWRGD
Q8501 @
SI4134DY-T1-GE3
JP8502@
1MM_OPEN_5MIL
C8503
10UF/6.3V
C8505
1UF/10V
+5VAO
U8501A
G966A-25ADJF11U
POK
VEN
VIN
VPP
GND1
ADJ
VO
NC
GND2
R8506
127KOHM
1%
TP8503 TP8502
TPC28T TPC28T
TP8501
TPC28T
JP8501@
1MM_OPEN_5MIL
+1.8VS
(Max:0.695A)
VO=0.8(R8503+R8501)/R8501=1.816V
VOUT:Typ.=1.816V;Max.=1.864V;Min.=1.769V
R8501
100KOhm
1%
C8504
10UF/6.3V
C8500
0.1UF/25V
@
+1.8VO
GND3 GND10
GND4 GND9
GND5 GND8
GND6 GND7
U8501B
G966A-25ADJF11U
10/15
D8501 @
1SS355
R8505
100KOhm
Q8502A
UM6K1N
81,82,83,91,93 SUSB#_PWR
R8502
0Ohm
C8501
0.33UF/10V
Q8502B
UM6K1N
<Variant Name>
PEGATRON
Title :POWER_+1.8VS
Engineer: Eve Kuo
Size
B
Project Name
H36Y
Rev
1.0
Date: Monday, May 10, 2010
Sheet 85 of 99



<Variant Name>

PEGATRON **Title : POWER_+VGFX_CORE**

Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	**H36Y**	1.0

Date: Monday, May 10, 2010 Sheet 86 of 99

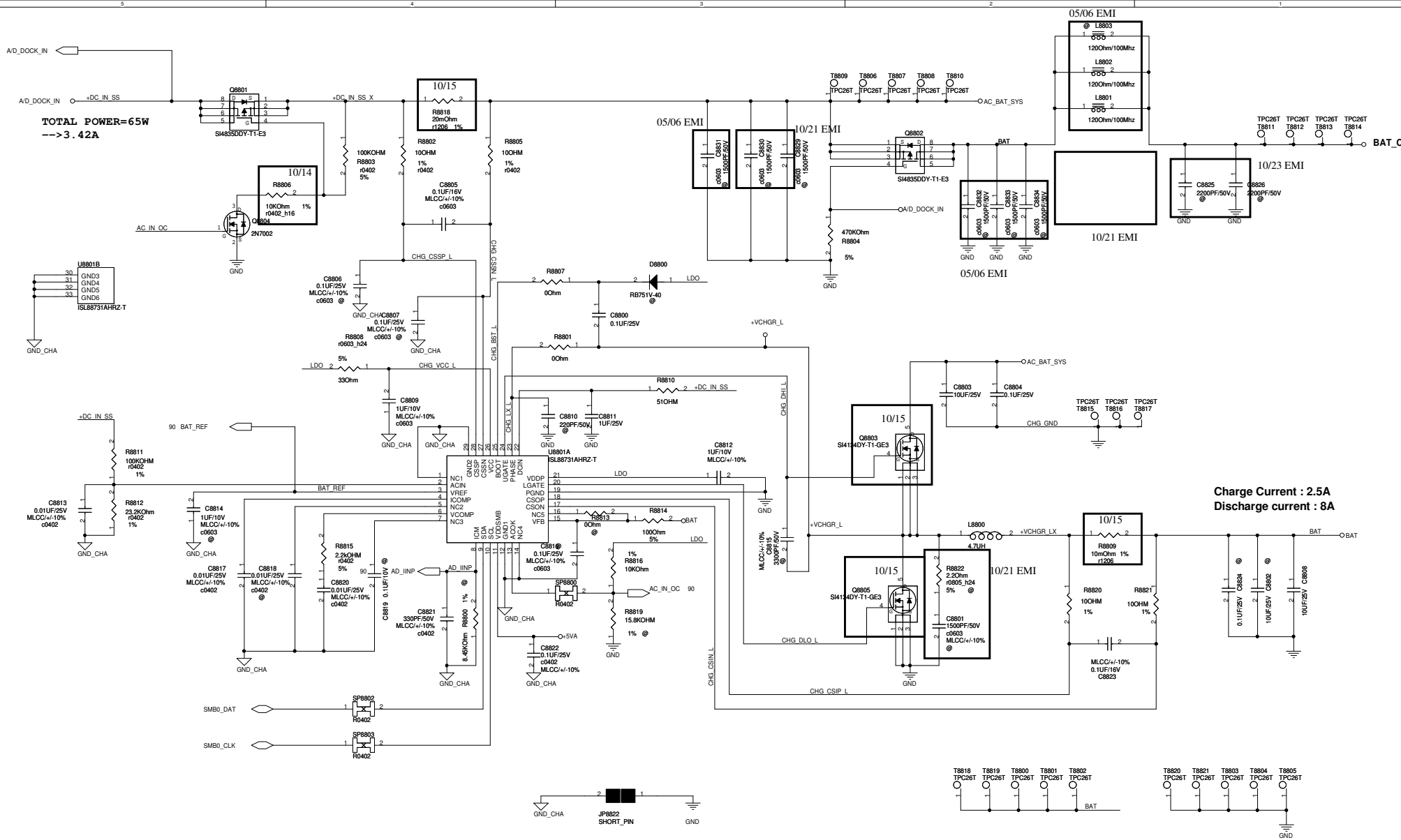
<Variant Name>

PEGATRON Title : POWER_+VGA_VCORE

Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	H36Y	1.0

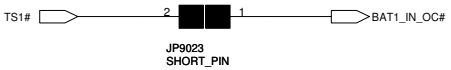
Date: Monday, May 10, 2010 Sheet 87 of 99


TOTAL POWER=65W
-->3.42A
Charge Current : 2.5A
Discharge current : 8A
Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202
Charger ISL6251 => EC CODE : 203
PEGATRON Title : POWER CHARGER
Engineer: Eve Kuo
H36Y
Size C
Project Name
Rev 1.0
Date: Monday, May 10, 2010
Sheet 88 of 99

<Variant Name>

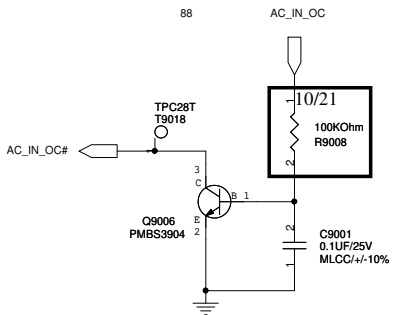
PEGATRON	Title : POWER_N/A	
	Engineer: *Jeff_Du*	
Size: A	Project Name: **N83**	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 89 of 99	

BATTERY IN DETECT



ADAPTER IN DETECT

Use MAX17015 IC function to Cost down component



POWER LIMIT CIRCUIT

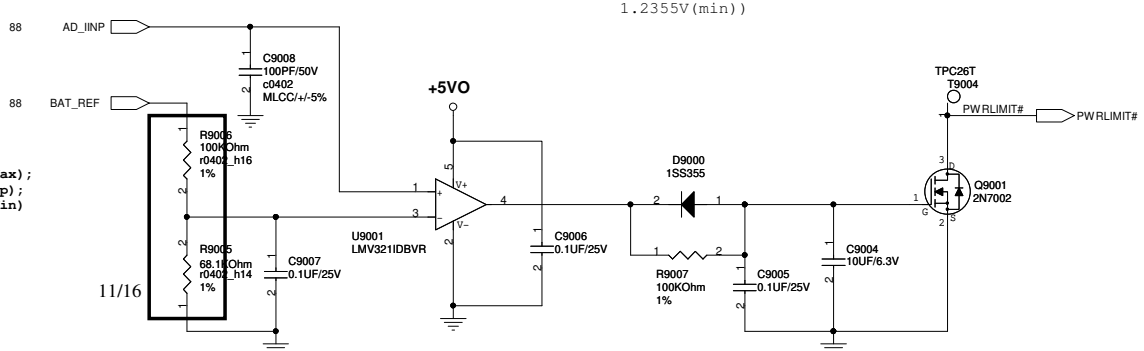
Pinput=65W----->Iinput=3.25A R2=20 mohm

Vicm=20*Iinput*R2 ==> Vicm=1.3655V(max)
1.3V(typ)
1.2355V(min))

+2.5Vref delete

Vref=3.2V;T=1%

Viinp=1.2335V(Max);
1.206V(Typ);
1.1793V(Min)



11/16

<Variant Name>

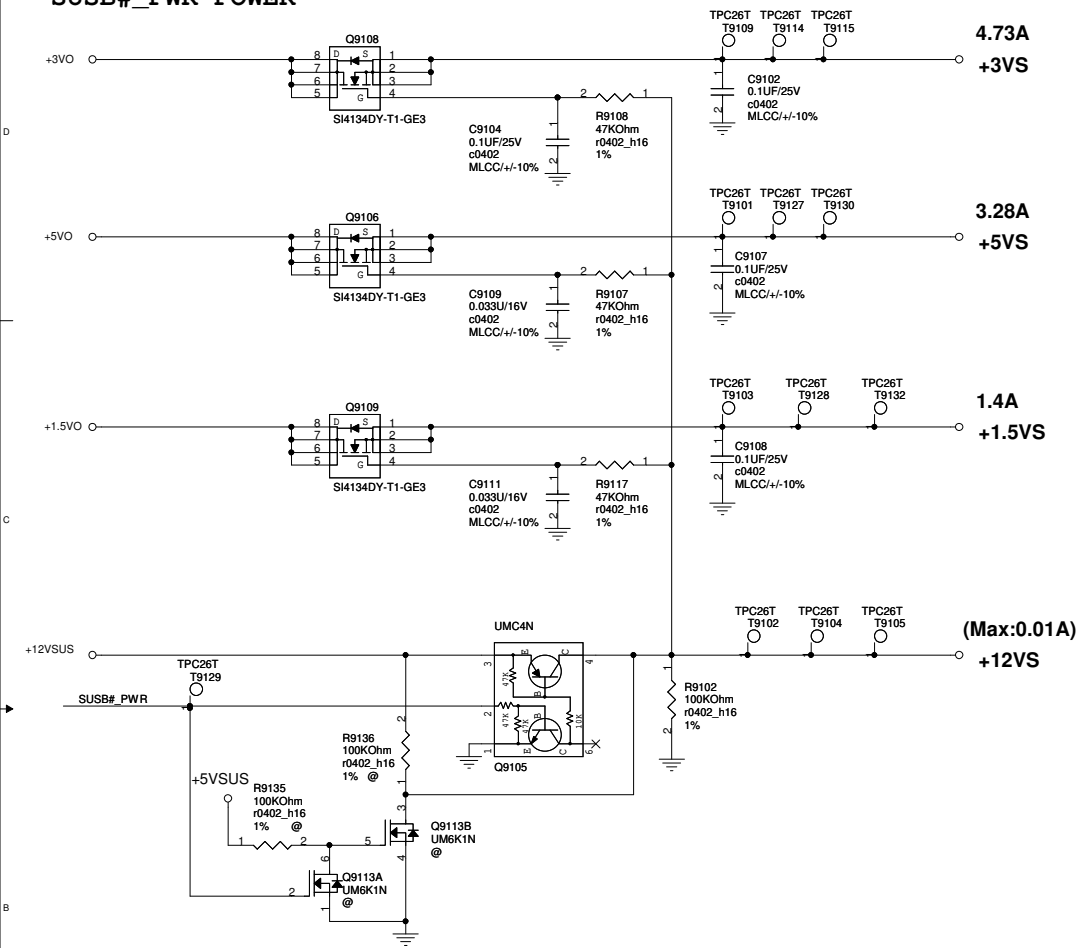
PEGATRON Title : POWER_DETECT

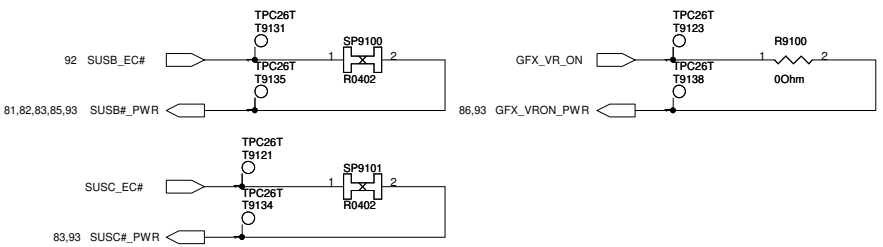
Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	H36Y	1.0

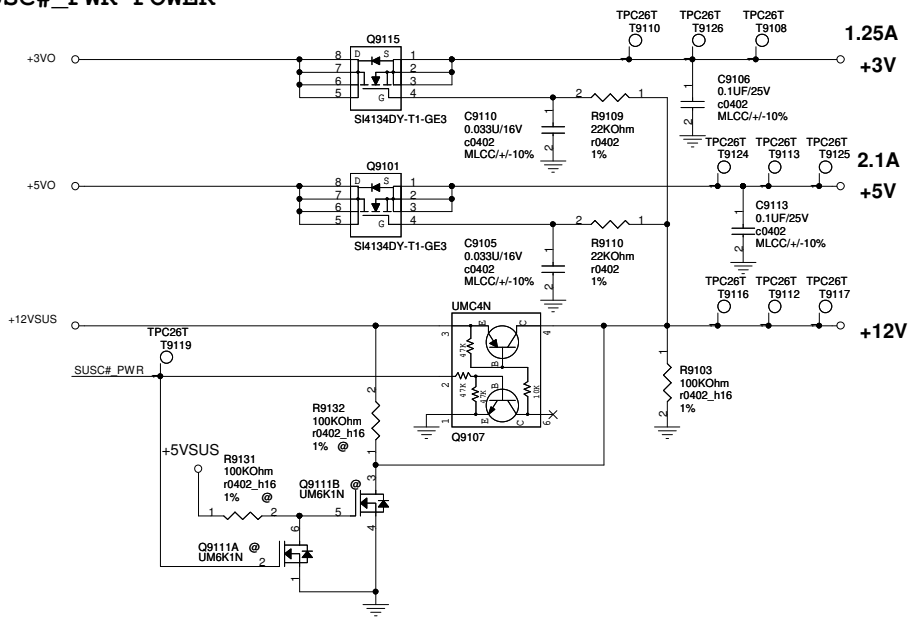
Date: Monday, May 10, 2010 Sheet 90 of 99

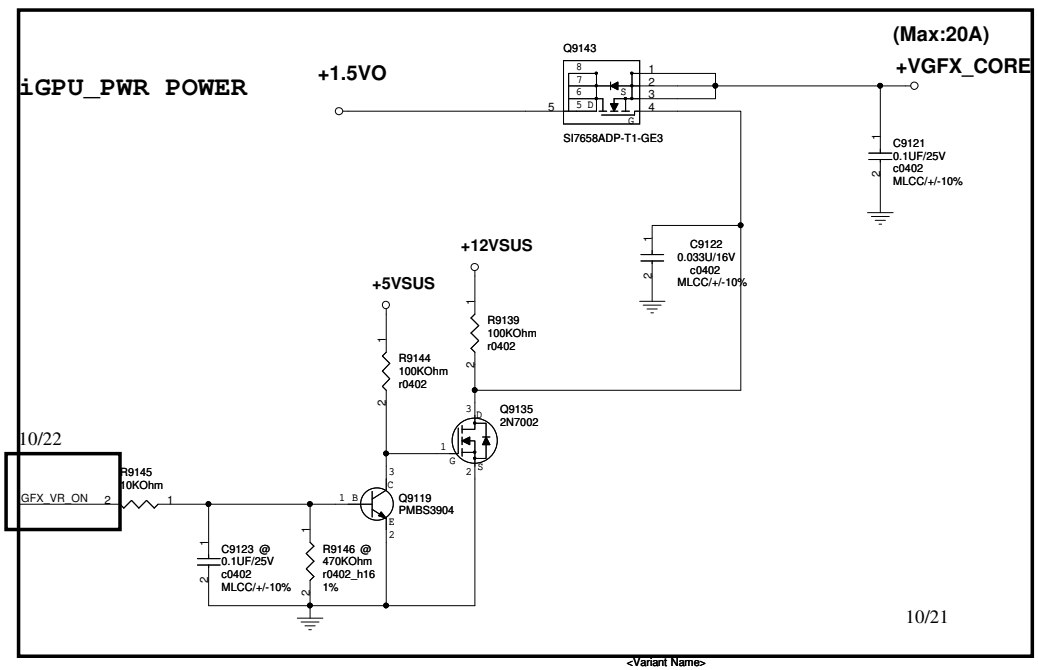
SUSB#_PWR POWER





SUSC#_PWR POWER





<Variant Name>

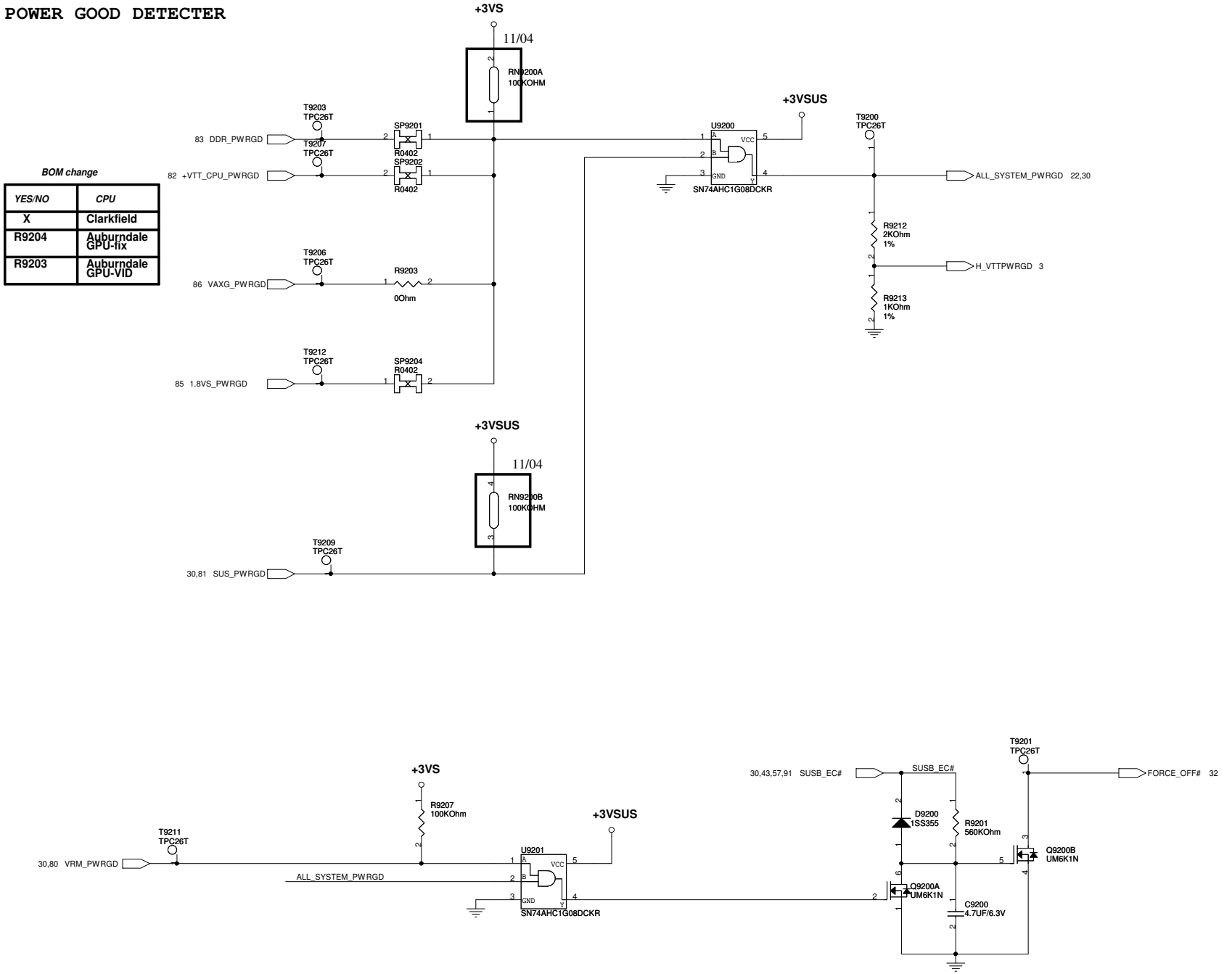
PEGATRON **Title : POWER_LOAD SWITCH**

Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	H36Y	1.0

Date: Monday, May 10, 2010 Sheet 91 of 99

POWER GOOD DETECTER



BOM change

YES/NO	*CPU*
X	Clarkfield
R9204	Auburndale GPU-fix
R9203	Auburndale GPU-VID

<Variant Name>

PEGATRON **Title :POWER_PROTECT**

Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	**H36Y**	1.0

Date: Monday, May 10, 2010 Sheet 92 of 99

AC_BAT_SYS — AC_BAT_SYS 80,81,82,83,86,88

BAT — BAT 88

BAT_CON — BAT_CON 88

+3VA — +3VA 81

+5VAO — +5VAO 81,85

+5VA — +5VA 81,82,88

+5VO — +5VO 81,82,83,90,91

+3VO — +3VO 81,85,91

+1.8VO — +1.8VO 85

+1.05VO — +1.05VO 80,82,86,91

+0.75VS — +0.75VS 83

+1.5VO — +1.5VO 83,91

+5VSUS — +5VSUS 81,91

+3VSUS — +3VSUS 81,92

+12VSUS — +12VSUS 81,91

+5V — +5V 85,91

+3V — +3V 91

+12V — +12V 91

+3VS — +3VS 80,86,91,92

+1.5V — +1.5V 83

+5VS — +5VS 80,86,91

+12VS — +12VS 91

+1.05VS — +1.05VS 80,82

+VTT_CPU — +VTT_CPU 82

+1.5VS — +1.5VS 91

+1.8VS — +1.8VS 85

+VCORE — +VCORE 80

+VGFX_CORE — +VGFX_CORE 82,86,91

FOR POWER TEST

+3VA — JP9300 (SGL_JUMP) — TPC26T T9301 — CPU_VRON_PWR 80

+3VA — JP9301 (SGL_JUMP) — TPC26T T9302 — SUSB#_PWR 81,82,83,85,91

+3VA — JP9302 (SGL_JUMP) — TPC26T T9303 — SUSC#_PWR 83,91

+3VA — JP9303 (SGL_JUMP) — TPC26T T9304 — VSUS_ON 81

10/06

+1.05VO — JP9306 (SGL_JUMP) — TPC26T T9307 — GFX_VRON_PWR 86,91

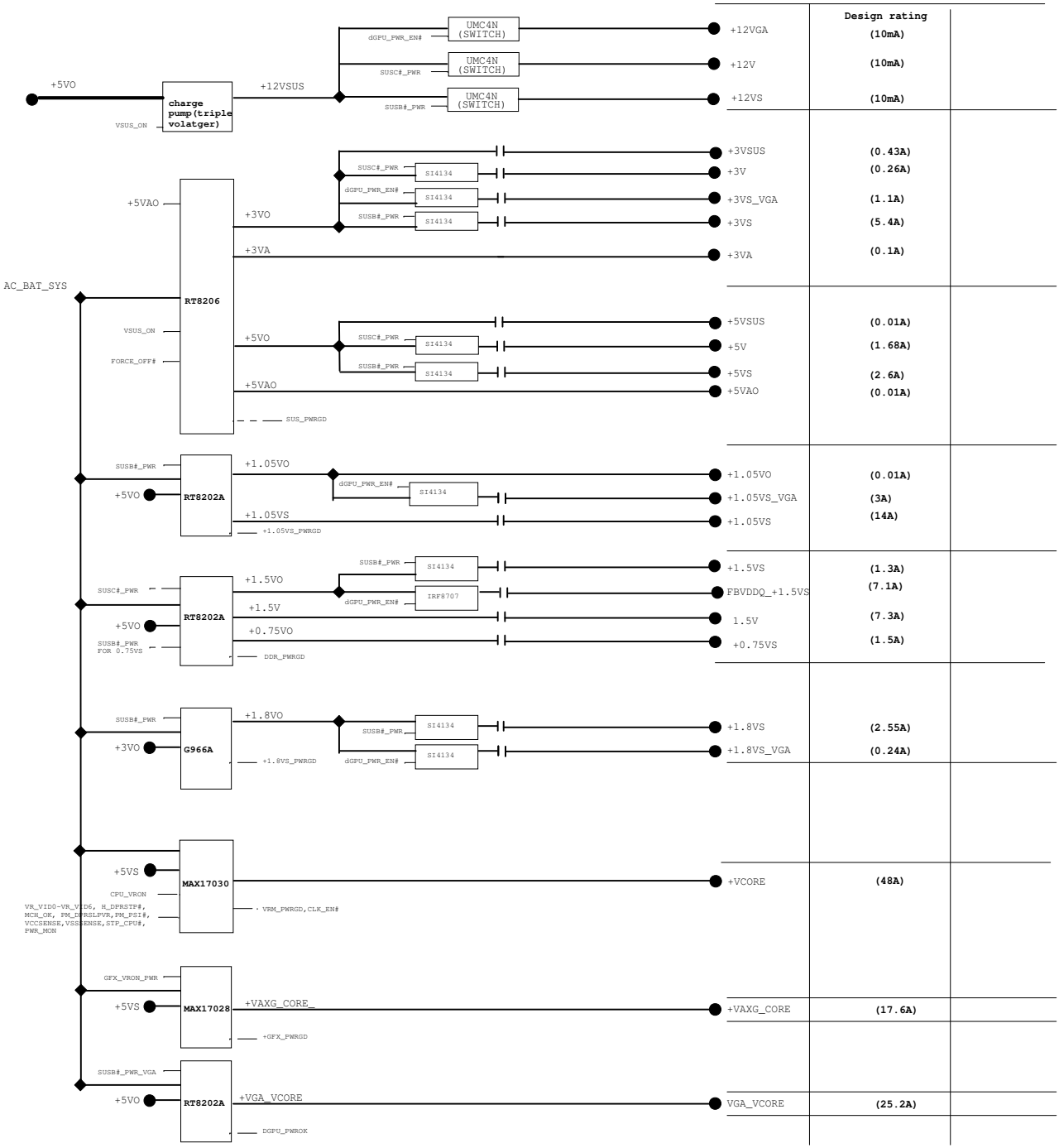
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: *Eve Kuo*

Size	Project Name	Rev
Custom	H36Y	1.0

Date: Monday, May 10, 2010 Sheet 93 of 99


Design rating
+5VO
charge pump(triple volatger)
VSUS_ON
+12VSUS
dGPU_PWR_EN#
UMC4N (SWITCH)
SUSC#_PWR
UMC4N (SWITCH)
SUSB#_PWR
UMC4N (SWITCH)
+12VGA
(10mA)
+12V
(10mA)
+12VS
(10mA)
+5VAO
RT8206
AC_BAT_SYS
+3VO
+3VA
SUSC#_PWR
SUSB#_PWR
dGPU_PWR_EN#
SI4134
+3VSUS
(0.43A)
+3V
(0.26A)
+3VS_VGA
(1.1A)
+3VS
(5.4A)
+3VA
(0.1A)
VSUS_ON
FORCE_OFF#
+5VO
+5VAO
SUS_PWRGD
+5VSUS
(0.01A)
+5V
(1.68A)
+5VS
(2.6A)
+5VAO
(0.01A)
SUSB#_PWR
+5VO
RT8202A
+1.05VO
+1.05VS
+1.05VS_PWRGD
dGPU_PWR_EN#
SI4134
+1.05VO
(0.01A)
+1.05VS_VGA
(3A)
+1.05VS
(14A)
SUSC#_PWR
RT8202A
+1.5VO
+1.5V
+0.75VO
SUSB#_PWR FOR 0.75VS
DDR_PWRGD
SUSB#_PWR
SI4134
IRF8707
+1.5VS
(1.3A)
FBVDDQ_+1.5VS
(7.1A)
1.5V
(7.3A)
+0.75VS
(1.5A)
SUSB#_PWR
+3VO
G966A
+1.8VO
+1.8VS_PWRGD
SUSB#_PWR
dGPU_PWR_EN#
SI4134
+1.8VS
(2.55A)
+1.8VS_VGA
(0.24A)
+5VS
MAX17030
CPU_VRON
VR_VID0-VR_VID6, H_DPRSTP#, MCH_OK, PM_DPRSLPVR,PM_PSI#, VCCSENSE,VSSSENSE,STP_CPU#, PWR_MON
VRM_PWRGD,CLK_EN#
+VCORE
(48A)
GFX_VRON_PWR
+5VS
MAX17028
+VAXG_CORE_
+GFX_PWRGD
+VAXG_CORE
(17.6A)
SUSB#_PWR_VGA
+5VO
RT8202A
+VGA_VCORE
DGPU_PWROK
VGA_VCORE
(25.2A)

modify notice

Version	Date	Description
1.0	090619	1. page88 alter solution that form MAX17015 change into ISL6251A. 2. page86 alter solution that form MAX17028 change into ISL62881.
	090622	1.Vcore form 3 Phase change into 2Phase 2.Q8100 Q8101 form SI4134DY change to SI7326 Q8102 form SI4134DY change to SI7716ADN Q8103 from SI4134DY change to SI7114ADN 3.Del CE8104 CE8105 Q8202 Q8305 Q8602 ADD CE8712
	090623	1.Del Q8008 Q8009 Q8203 Q8304 Q8604 ADD C8005 2.CE8103 From 150uf/4v change to 220uf/4v CE8101 From 100uf/6.3v change to 150uf/6.3v 3.Q8201 From IRF8707 change to SIR474DP Q8202 From IRF8707 change to SI7170DP L8201 From 0.56uH change 1uH CE8203 CE8204 From 470uf/2.5V change to 330uf/2.5V 4.Q8302 From IRF8707 change to SIR474DP Q8303 From IRF8707 change to SI7658ADP L8300 From 0.56uH change 1uH CE8302 CE8300 From 470uf/2.5V change to 330uf/2.5V 5.Q8603 From SI7170DP change to SI7658ADP
	090626	Modify R& C SIZE
	090629	Modify R& C SIZE UPDATE JP8801 JP8802 JP8803 JP8804 JP8805 JP8806 Part Number Change CE8005 CE8010 From NEC change to PANASONIC Modify OCP Resister R8125 R8124 R8247 R8308 R8706
	100330	Page 85 +1.8VS add co-layout PWM circuit.

PEGATRON Title : Power History

<OrgName> Engineer: Eve Kuo

Size: Custom | Project Name: H36Y | Rev: 1.0

Date: Monday, May 10, 2010 | Sheet 95 of 99

PEGATRON Title : N/A

BG1\HW1 Engineer: *George Chen*

Size	Project Name	Rev
Custom	H26	1.0

Date: Monday, May 10, 2010 Sheet 96 of 99

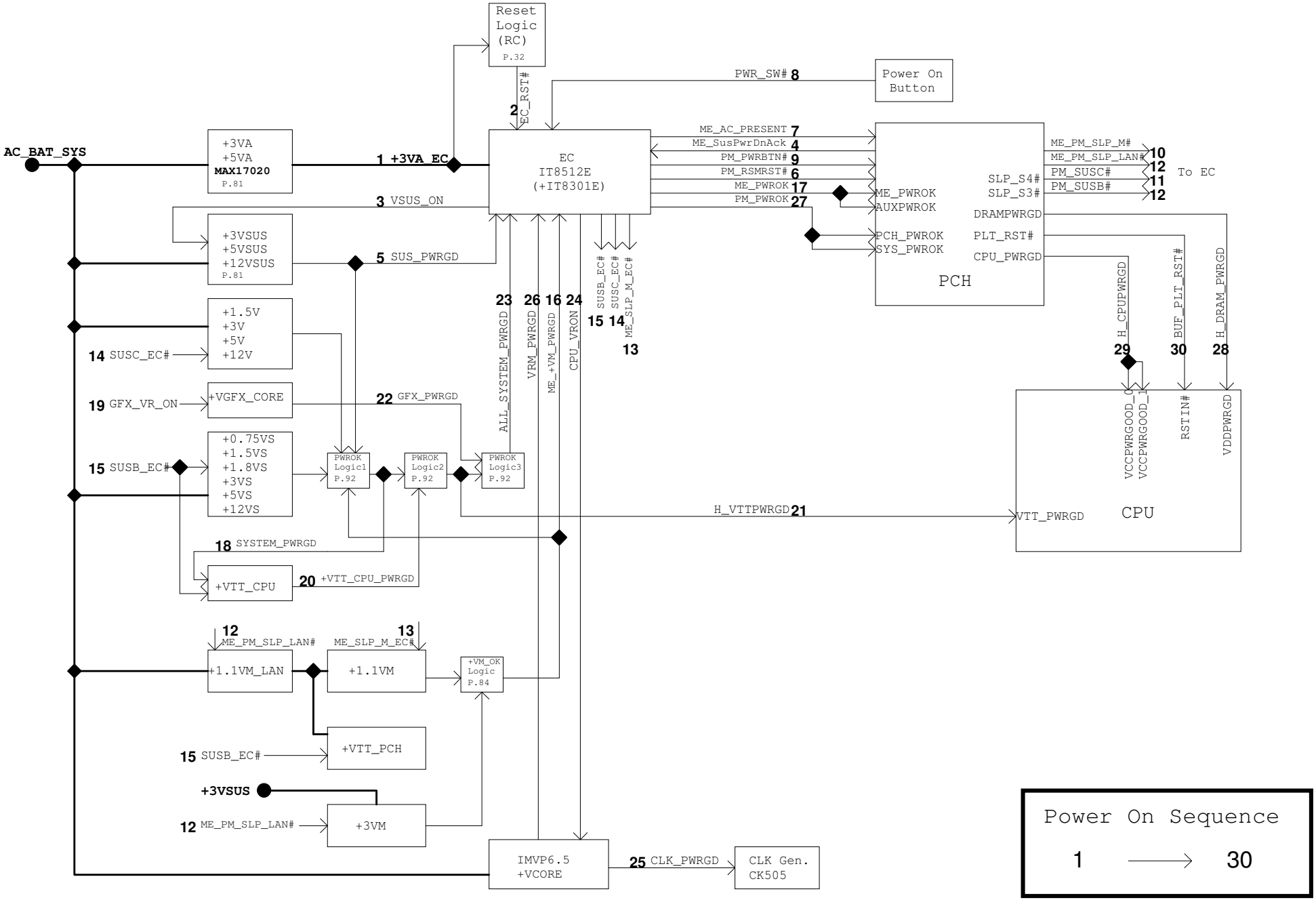
PEGATRON Title : ****

BG1\HW1 Engineer: *George Chen*

Size	Project Name	Rev
Custom	H26	1.0

Date: Monday, May 10, 2010 Sheet 97 of 99

Power On Sequence Diagram Rev. 0.2



Power On Sequence

1 → 30

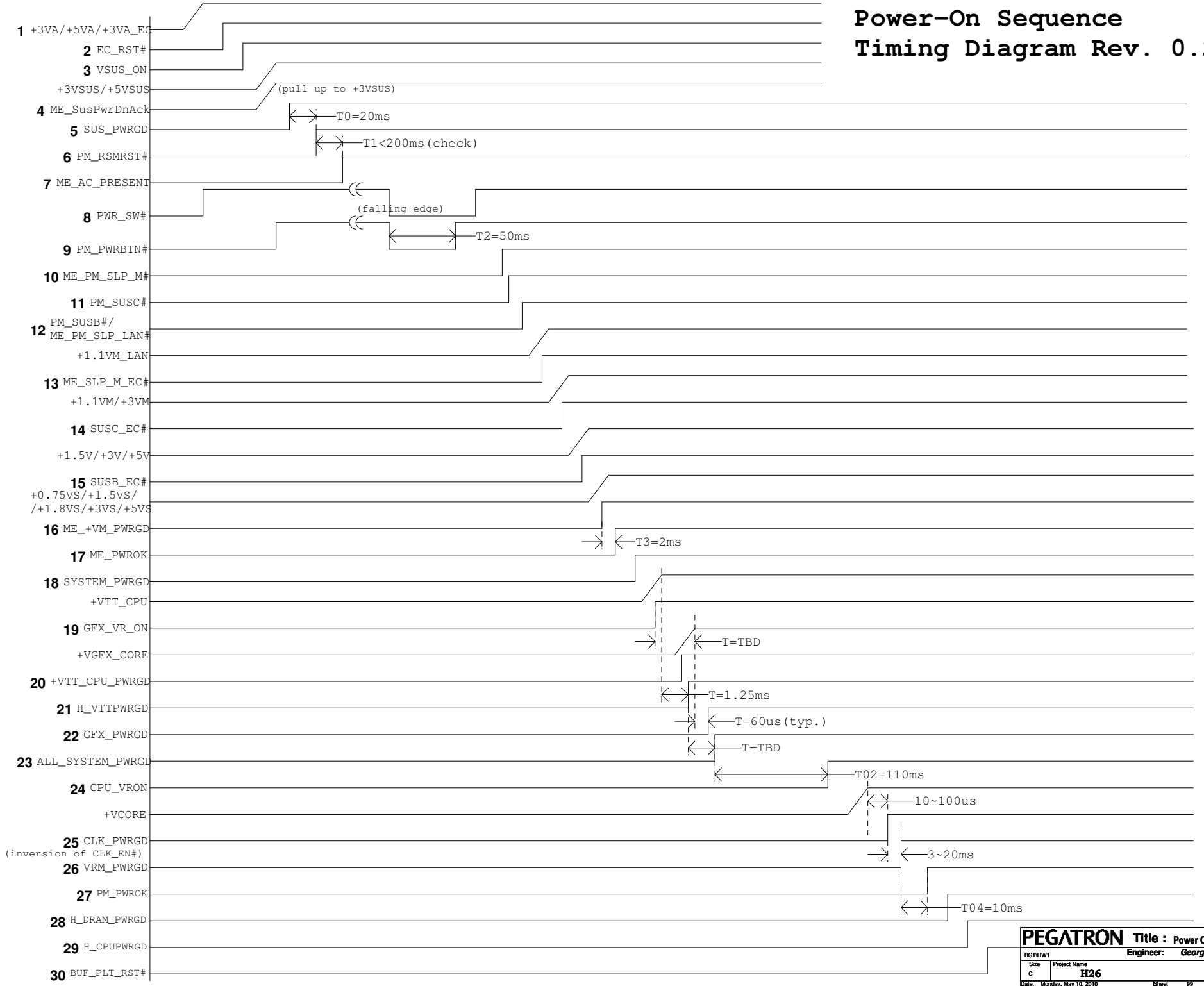
PEGATRON Title : Power On Sequence

BG1VHW1 Engineer: George Chen

Size	Project Name	Rev
C	H26	1.0

Date: Monday, May 10, 2010 Sheet 98 of 99

Power-On Sequence Timing Diagram Rev. 0.2



PEGATRON	Title : Power On Timing	
BG1VHW1	Engineer: George Chen	
Size: C	Project Name: H26	Rev: 1.0
Date: Monday, May 10, 2010	Sheet 99 of 99	