Model Name: GA-P55M-UD2 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1156-A
05	CPU_LGA1156-B
06	CPU_LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCI EXPRESS*16 SLOT
11	PCH_FDI,DMI,USB,PCIE,NVRAM
12	PCH_DP,CLK BUFFER
13	PCH_HOST,SATA,PCI
14	PCH_GPIO,CTRL,AUDIO
15	PCH_PWR,GND
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOTs X3
18	PCI SLOT X2
19	ITE 8720 LPC IO
20	COM, -PROHOT , DYNAMIC OC , LPT
21	Dual BIOS
22	ALC888/889A
23	REAR AUDIO JACK
24	CLOCK GEN ICS9LPRS914
25	VCORE PWM ISL6334CR-1
26	VCORE PWM ISL6334CR-2
27	DISCRETE POWER I

SHEET	TITLE
28	DDR_15V & VCC1_05_PCH PWM_ISL6545CBZ
29	CPU_VAXG PWM_ISL6314CRZ
30	CPU_VTT PWM ISL6322G
31	F_PANEL , F_USB , FDD
32	ATX POWER
33	Marvell 88SE9123
34	REALTEK RTL8111DL
35	REALTEK RTL8111DL_1
36	TI TSB43AB23 1394
37	HWM,KB/MS , FAN CTRL
38	TPM SLB9635TT
39	ESATA JMB362
40	TABLE LIST
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Title: Cover Sheet

Size: Custom | Document Number: GA-P55M-UD2 | Rev: 1.0

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GA-P55M-UD2 Version: 1.0

Component value change history

Data	Change Item	Reason
0.1	1. 9ME55QD3R-00-01	
EP55A-UD3P 0.1	1. Add R687,BC241 For ISL8014 VDD PIN	
	2. IDE Conn. change 直立式	
	3. ADD CPU RM	
	4. CPU_VAXG R153 --> R151 68K/4/1 , R127 20K/4/1 --> 42K/4/1 , BC60 0.1u --> 1n/4	
	5. DIMM & LPT COLOR --> BLUE	
	6. REMOVE 7474 , CHANGE TO ITE8720/JX	
	7. CLK阻值調整	
	8. PCIEX16 CHANGE TO RIGHT EJECTOR	
	9. 0.5uH --> 1.0uH 含阻值修改	
EP55A-UD3P 0.2	1. CHECK +12V SHORT PAD FOR 10mil	
	2. F1_1394加蓋(包材階)	
	3. ADD DR86=124K/4/1 , DR88=249K/4/1	
	4. U12~U15 upi6262M --> upi6267M	
	5. DRAM_PWROK R490=1K/4/1 , R491=3K/4/1	
	6. REMOVE DR138=0/4 , ADD DR139,DR141=0/4	
	7. RU2指定料號:10HP4-112540-11R	
	8. 排阻指定廠牌用WALSIN	
	9. LU1,LU4 RTL8111D --> RTL8111C	
	10. PCB "育富"移除	
	11. ONFI指定用11SM1-600078-02R	
	12. R376 2.26K/4/1 --> 2.55K/4/1	
	13. 確認上哪種upi6262 10%/upi6267?	
	14. FB7~FB10 REMOVE	
	15. PCH BUFFER 25MHz REMOVE "X2,C93,C94,R420"	
	16. BIOS 16M --> 32M (FOR ONFI ONBOARD)	
P55M-UD4	1. RTL8111C --> RTC8111D (是否上新板VB?)	
P55M-UD2 0.2	1. ADD PACKAGE F1_1394 2. P55 REV.B1 --> REV.B2 3. VCC1_05_PCH --> OP+MOS	
P55M-UD2 1.0	1. CHECK POWER SEQUENCY FOR VCC1_05_PCH 3. REMOVE PLL, 22U 2. PROCHOT阻值修改 4. Q73,Q74 UPA2724 --> UPA2726	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
EP55-UD3R 0.1	1. 9ME55QD3R-00-01	
EP55A-UD3P 0.1	1. PWR_LED GPIO46 --> GPIO20	
	2. CHECK DDR3 LAYER RULE UPDATE (DDR3 LIBRARY UPDATE)	
	3. ADD F_PANEL RESET & BOTTOM ESD PROTECT	
	4. CPU ISENSE & IOUT ADD CONTROL CIRCUIT	
	5. RESET 7474 COST DOWN CHECK	
	6. SRCCLK_CKG TRACE CHANGE TO TOP	
	7. USBP12 , USBP13 +- SWAP NET	
	8. +12V PROTECT Q91 ADD Damping Resistor "R748"	
	9. 零件位置BAT移出至BAT外框	
	10. X3與CLR_CMOS距離不足5mm	
	11. Remove 0 ohm	
	12. CPU_VTT ADD背面電容SBC9,SBC10	
	13. CPU_VTT ADD VTT_SENSE , VTT_VSS	
	14. MODIFY PCIEX4 & PCIEX1 SELECT "-4X_EN"	
	15. ADD ESATA JMB362	
	16. ITE8275 PATCH -SYS_RST 漏電	
	17. DRAM_PWROK 留Damping 電阻	
	18. DRIVER的PIN5 GND走線與GATE同粗	
	19. LAN CTRL18爲PHASE須在第二層做隔離	
EP55A-UD3P 0.2	1. REMOVE AUDIO ESD	
	2. REMOVE CPU_VAXG	
	3. PCH_CLK 改 SHORT PAD (0 ohm維持10pcs以下)	
	4. ITE8275 GPIO11,GPIO13 TO TURBO0/TURBO1	
	5. F_PANEL UPDATE H2X10PANEL-1	
	6. ONFI 改 ON BOARD	
	7. 1394 "IEC1" NET SWAP & SHORT PROTECT	
	8. PIN HEATER CHECK	
	9. ITE8275 SYS_RST PATCH	
	10. BC118,BC119 --> TBC29,TBC30	
	11. BC5靠近M_BIOS PIN8 , BC6靠近M_BIOS PIN8	
	12. U2 7474 REMOVE	

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Title: BOM & PCB MODIFY HISTORY

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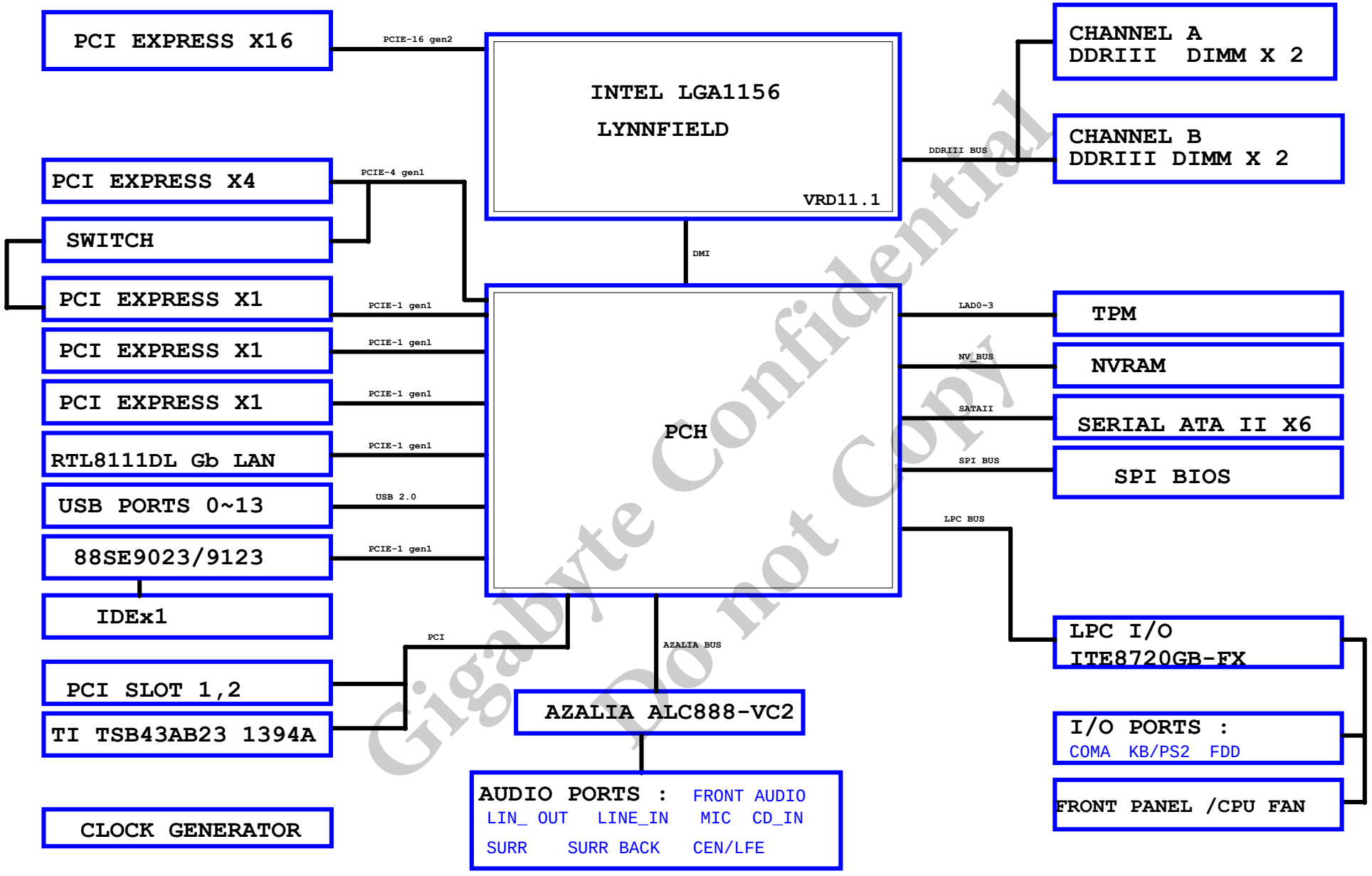
BLOCK DIAGRAM



Gigabyte Technology		
Title: BLOCK DIAGRAM		
Size: C	Document Number: GA-P55M-UD2	Rev: 1.0
Date: Thursday, July 09, 2009	Sheet 3 of 33	

FDI : 16/5/5/5/16(breakout min 8/4/5/4/8)
Impedance=80 +- 17.5%

PCIEX16:16/5/5/5/16(breakout min 8/4/5/4/8)
Impedance=80 +- 17.5%

DMI:12/5/5/5/12
Impedance=80 +- 17.5%

CFG0=1: 1X16 PEG
CFG0=0: 2X8 PEG

For PCIE2.0 issue
Must remove after
fixed issue

Rev 0.2 modefy

Rev 0.2 modefy

Rev 0.2 modefy

Check Trace length/ width

CFG	H	L	NOTE
0			H:1X16 , L:2X8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		
7	RSVD		ENGINEERING EXPERIMENT
15	RSVD		ENGINEERING EXPERIMENT

CFG 0-5 all internal PULL-UP

POWER ON CONFIG TABLE (Default=1.2250V)

	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CFG0	1
VID4	IMON CFG1	1
VID5	IMON CFG2	1
VID6	RSVD	
VID7	VRD SEL	LOW
PSI#	RSVD	LOW

Title	CPU LGA1156-A
Size	Custom
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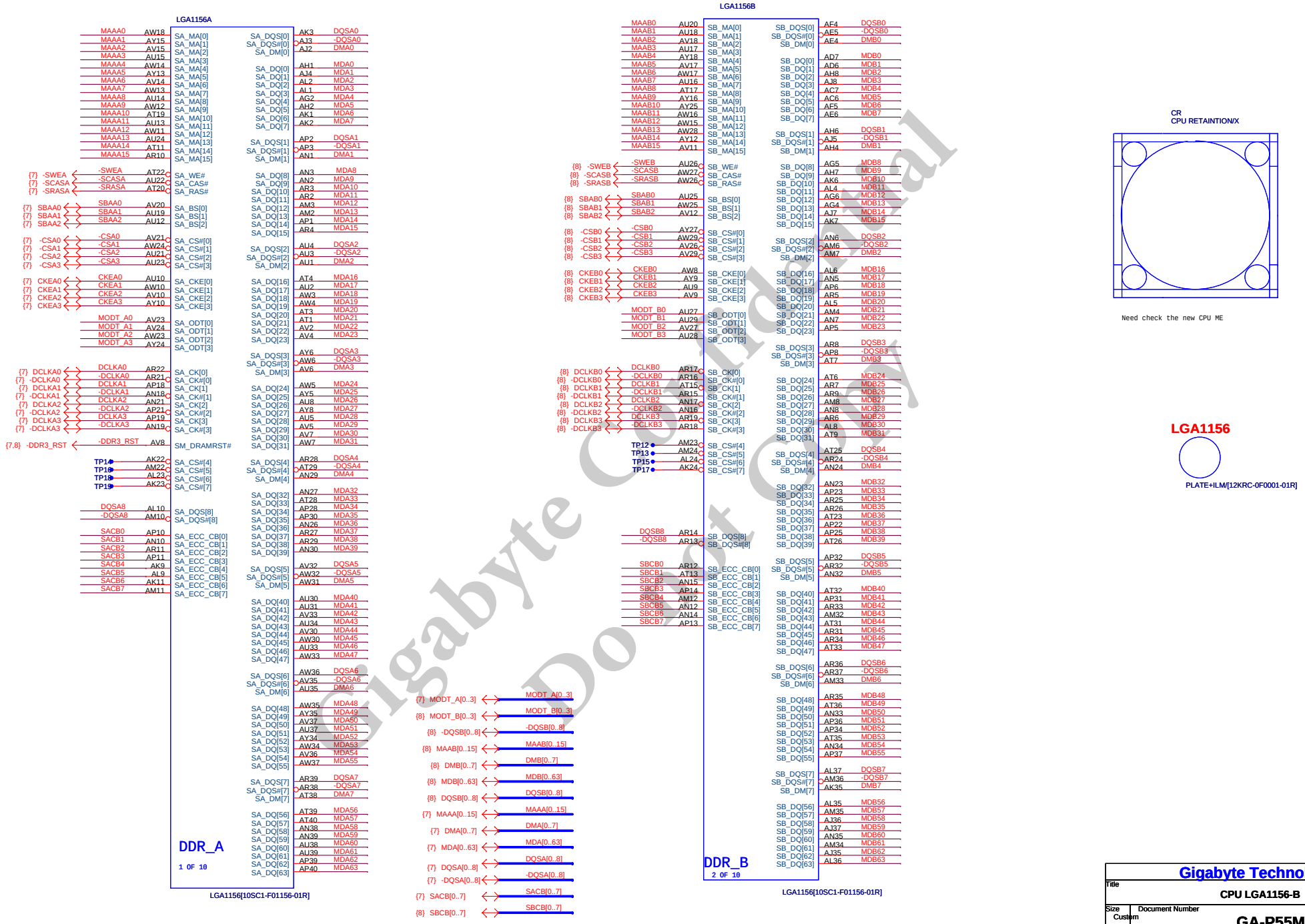
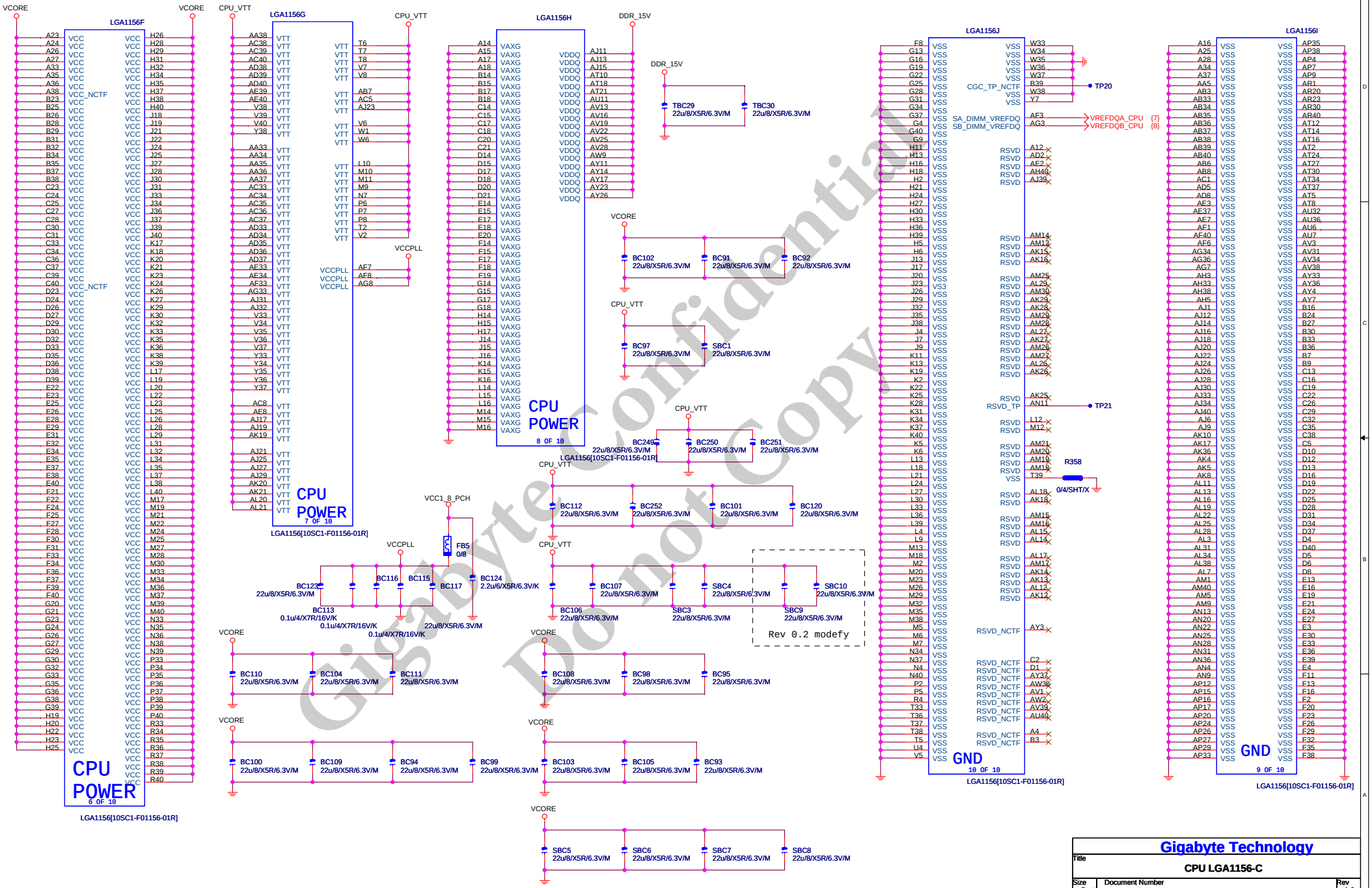
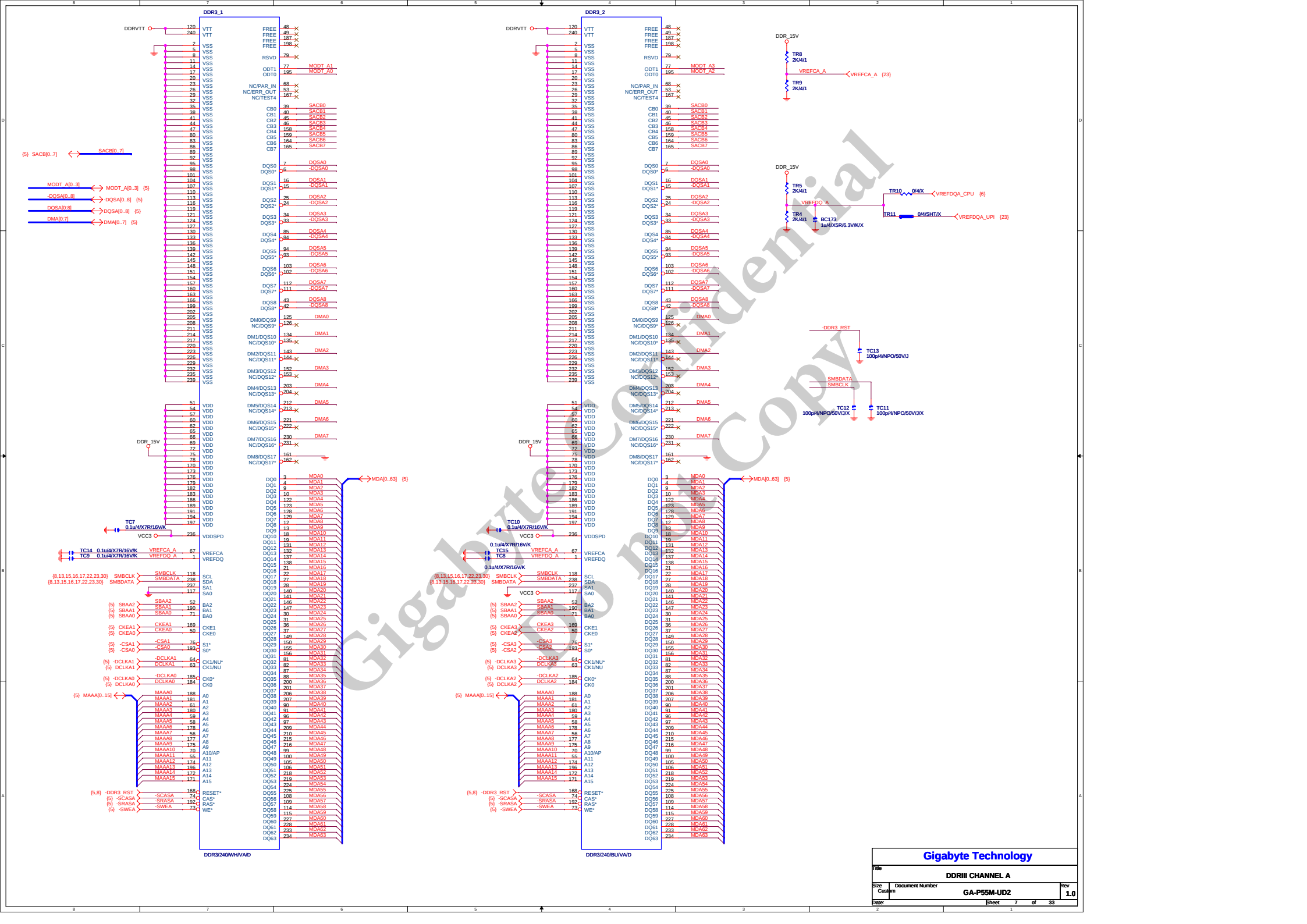


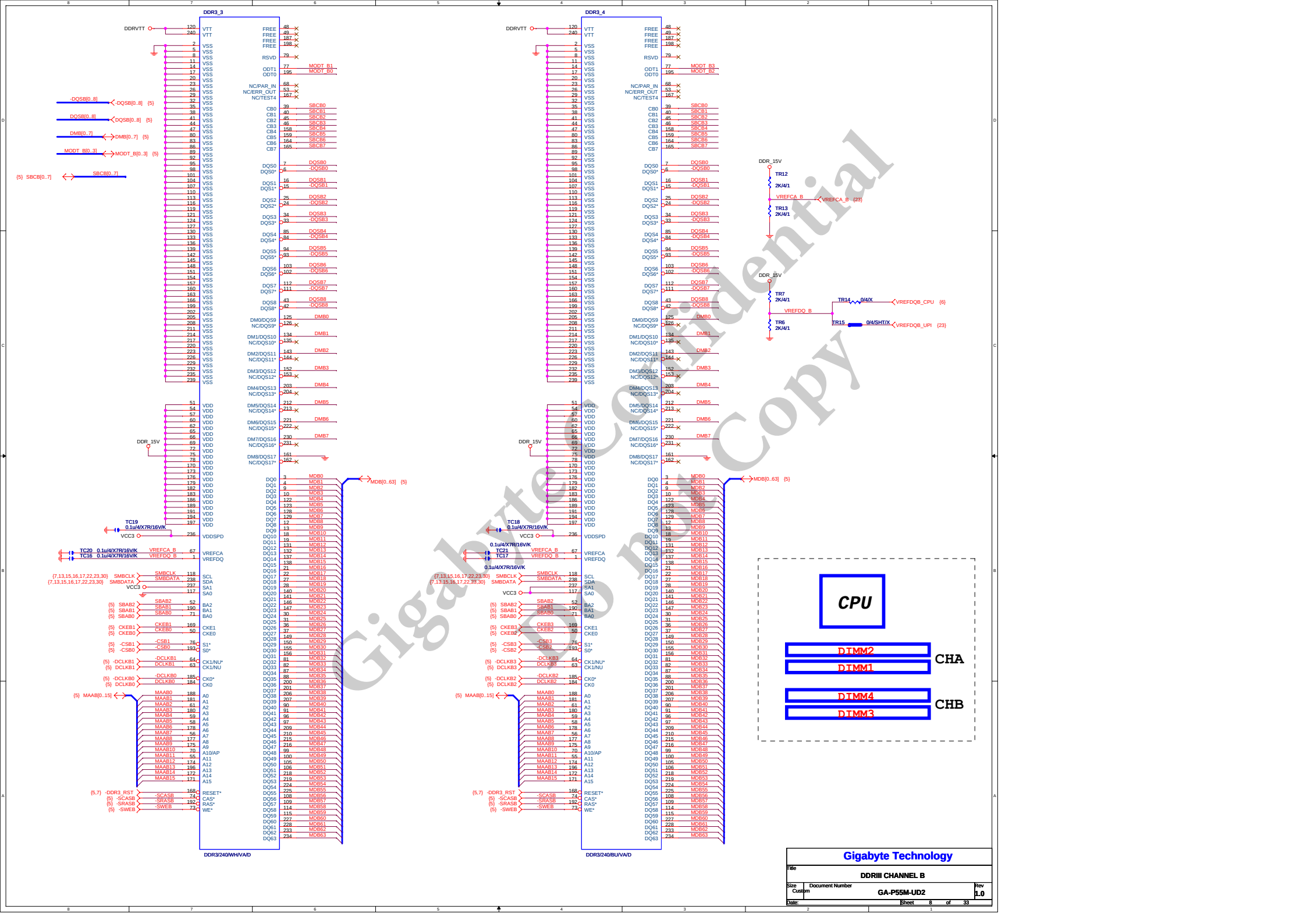
Gigabyte Technology		
Title: CPU LGA1156-B		
Size: Custom	Document Number: GA-P55M-UD2	Rev: 1.0
Date: Thursday, July 09, 2009	Sheet 5 of 33	



Gigabyte Technology		
Title: CPU LGA1156-C		
Size: Custom	Document Number: GA-P55M-UD2	Rev: 1.0
Date: Thursday, July 09, 2009	Sheet 6 of 33	



Gigabyte Technology		
Title: DDRIII CHANNEL A		
Size: Custom	Document Number: GA-P55M-UD2	Rev: 1.0
Date:	Sheet 7 of 33	



Gigabyte Technology	
Title	DDRIII CHANNEL B
Size: Custom	Document Number: GA-P55M-UD2
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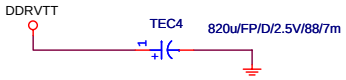
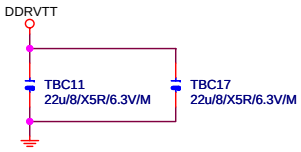
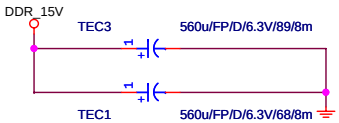
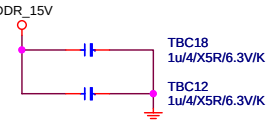
DDR TERMINATION CHANNEL A/B

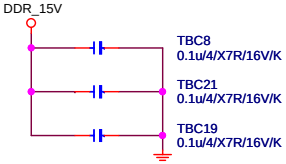




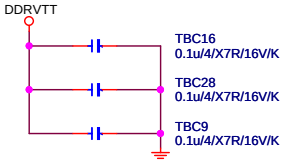


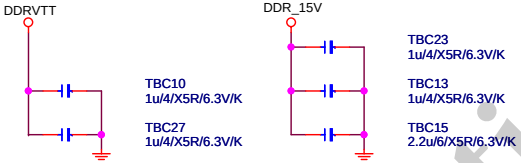


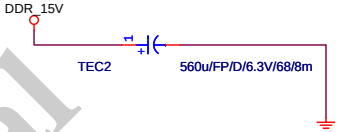
DDR15V Decouple

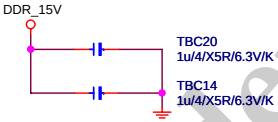


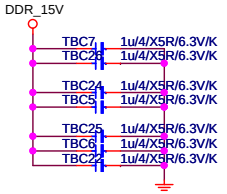
DDRVTT Decouple

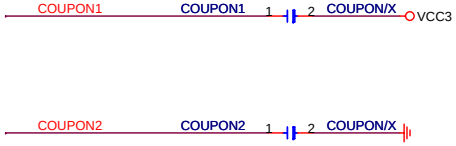












Gigabyte Technology		
Title: DDRIII POWER CAP		
Size: B	Document Number: GA-P55M-UD2	Rev: 1.0
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DMI:12/5/5/5/12
Impedance=80 +- 17.5%

PCHB

USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%

DMI Terminator voltage
HI : AC COUP : TX/RX TO VCC
LO : DC COUP : HALF SWING

Rev 0.2 modefy

OC[3:0]# for Device 29 (ports 0-7)

OC[7:4]# for Device 26 (ports 8-13)

Impedance=50+- 15%
ONFI: NV_DQ 4/5
NV_DQS 4/10
NV_CTRL 4/10
NV_CK 4/15

PCIE X1 :15/5/5/5/15
Impedance=80 +- 17.5%

電容要靠近 slot 端

PCH_HS

PCH_HS[12SP2-030030-C1R]

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5_6#	USB10~13
OC7#	

NV_ALE	
Hi	Enable Danbury
Lo	Disable Danbury

Intel anti theft techonlogy

Title	PCH FDI,DMI,USB ,PCIE,NVRAM
Size	B
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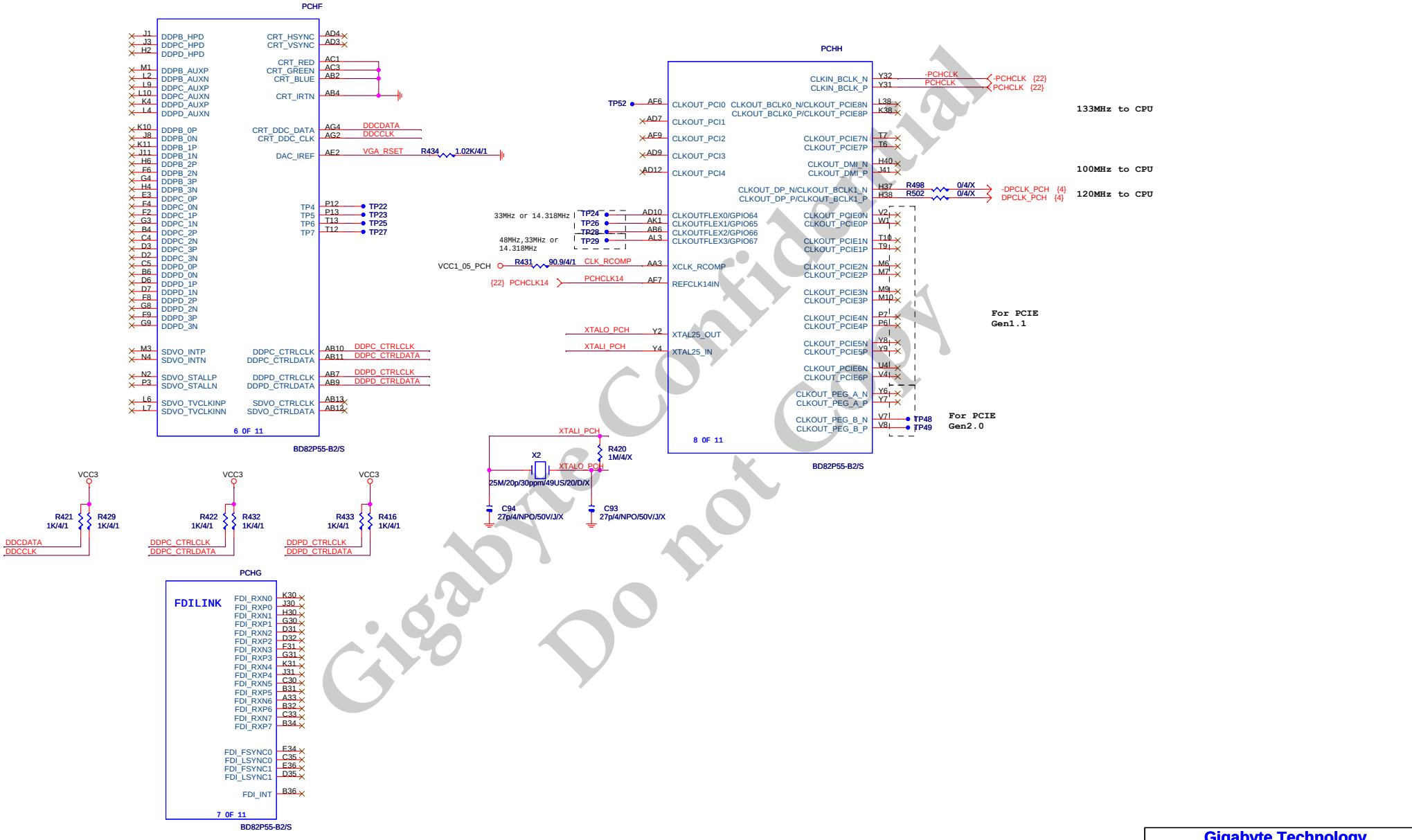
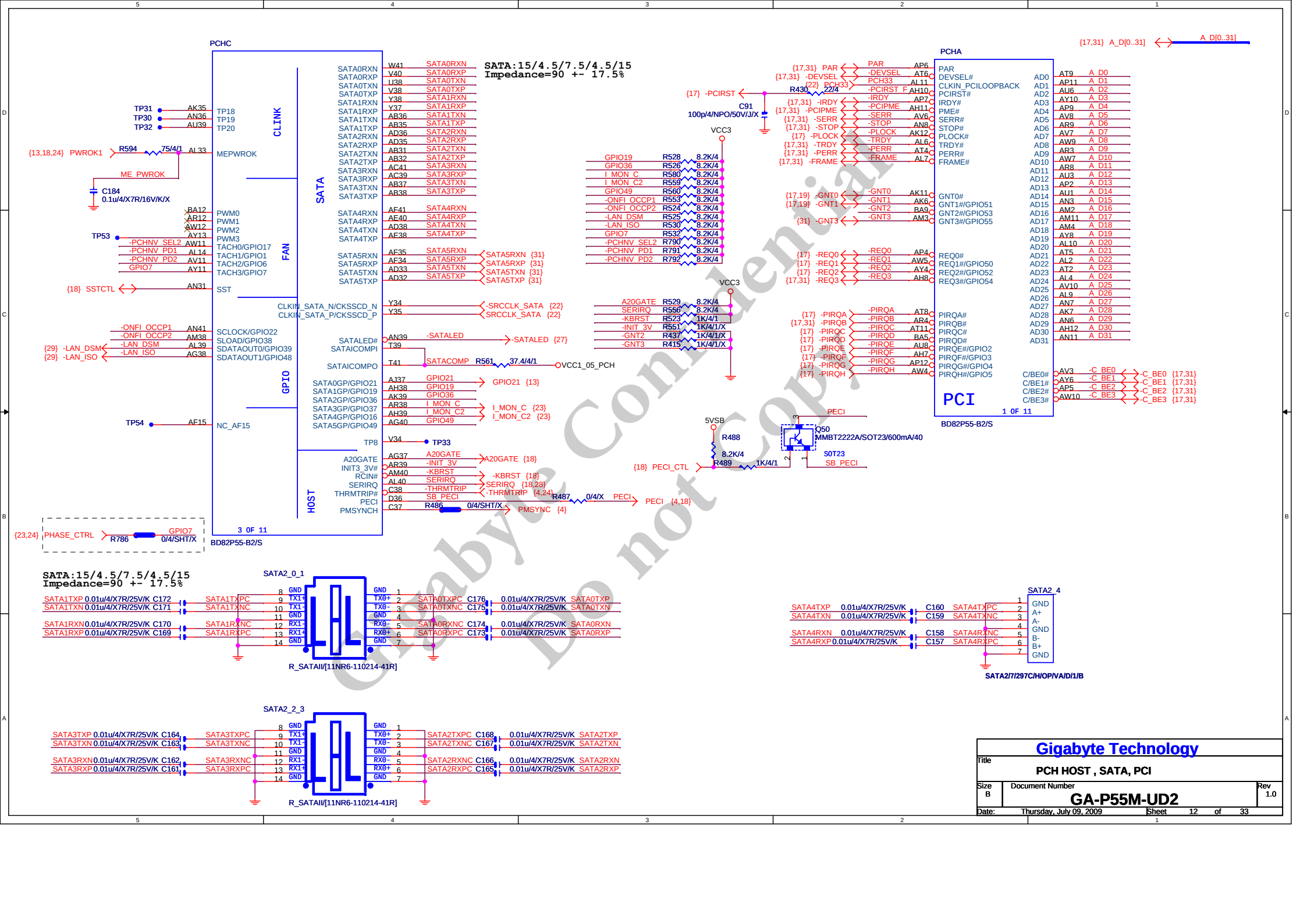
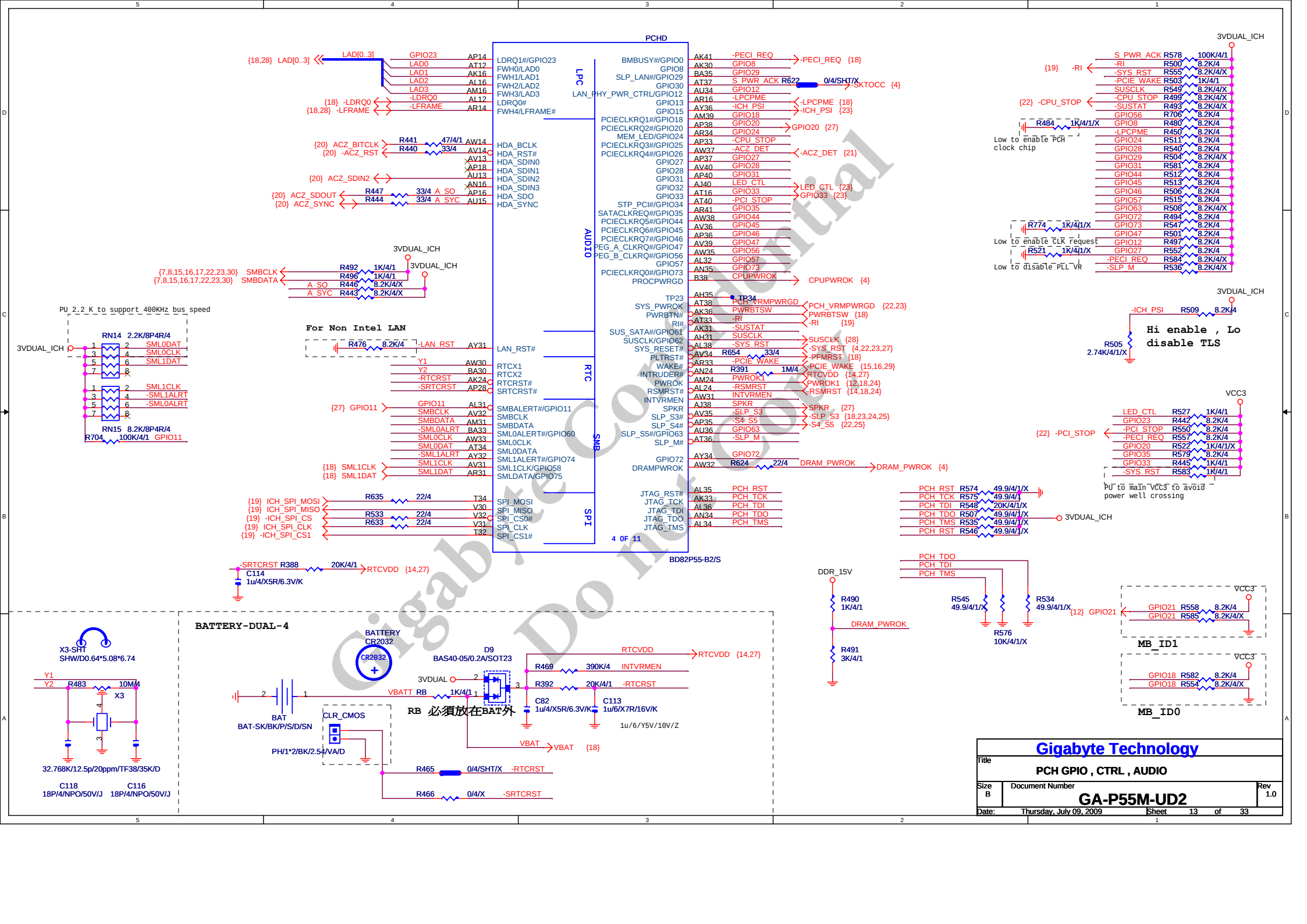
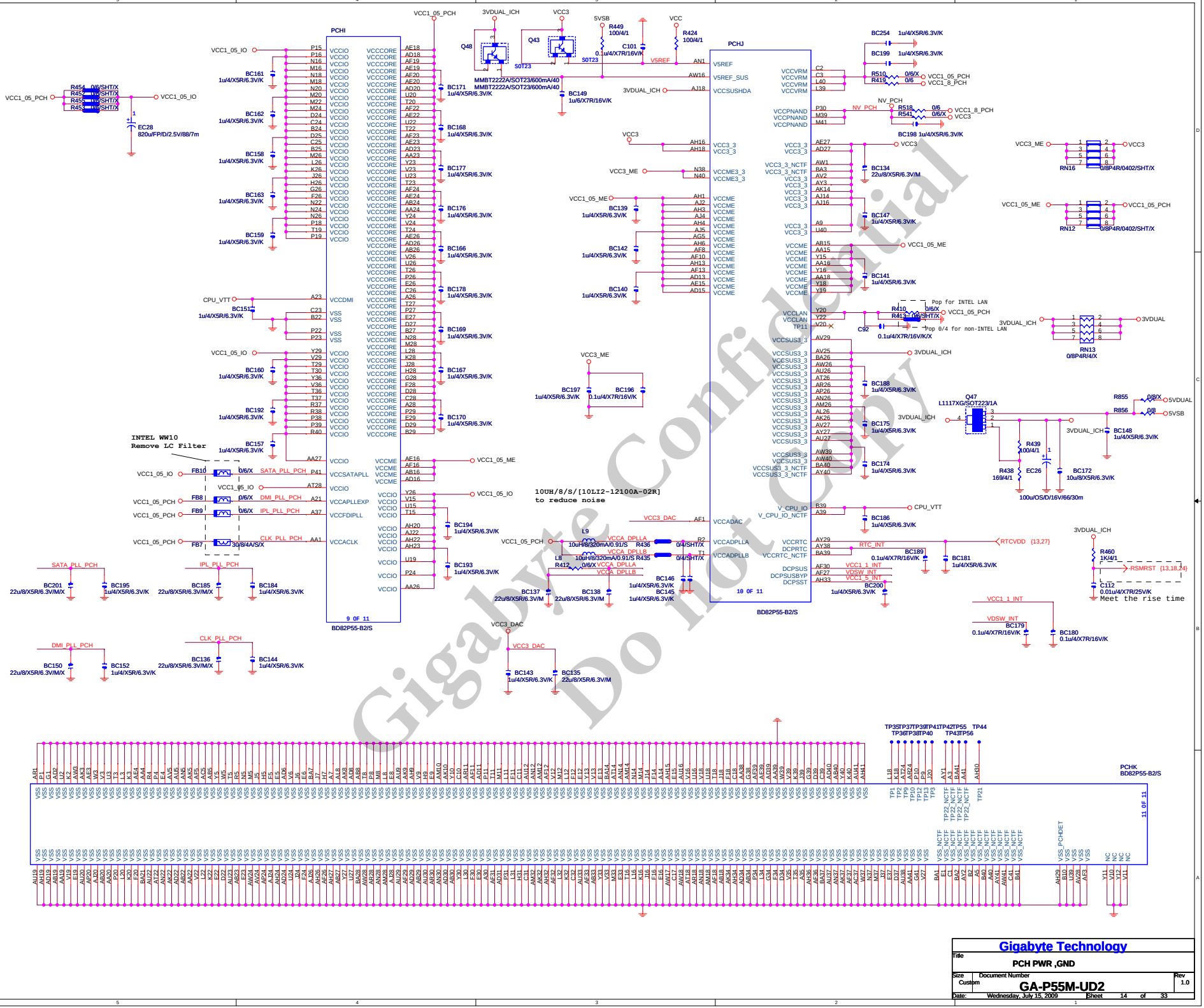
Gigabyte Technology



Gigabyte Technology		
Title: PCH DISPLAY ,CLK BUFFER		
Size: Custom	Document Number: GA-P55M-UD2	Rev: 1.0
Date: Thursday, July 09, 2009	Sheet 11 of 33	






PCHI
PCHJ
PCHK
BD82P55-B2/S
9 OF 11
10 OF 11
11 OF 11
INTEL WW10
Remove LC Filter
10UH/8/S/[10LI2-12100A-02R]
to reduce noise
Pop for INTEL LAN
Pop 0/4 for non-INTEL LAN
Meet the rise time
Gigabyte Confidential
Do not Copy
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PCH PWR ,GND
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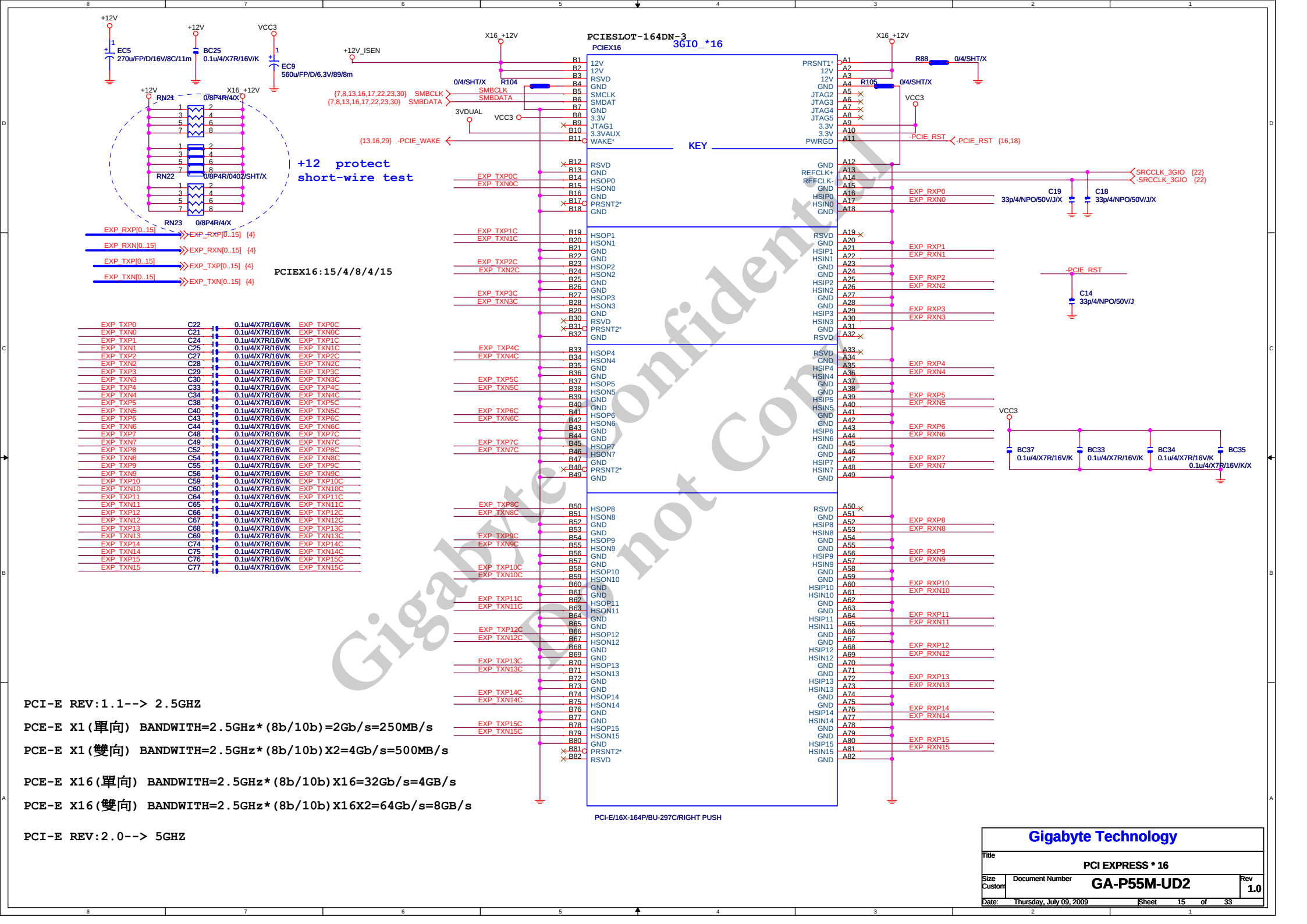
PCIESLOT-164DN-3
3GIO_*16
PCIEX16
KEY
+12 protect
short-wire test
PCIEX16:15/4/8/4/15
PCI-E/16X-164P/BU-297C/RIGHT PUSH
PCI-E REV:1.1--> 2.5GHZ
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s
PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s
PCI-E REV:2.0--> 5GHZ
Gigabyte Technology
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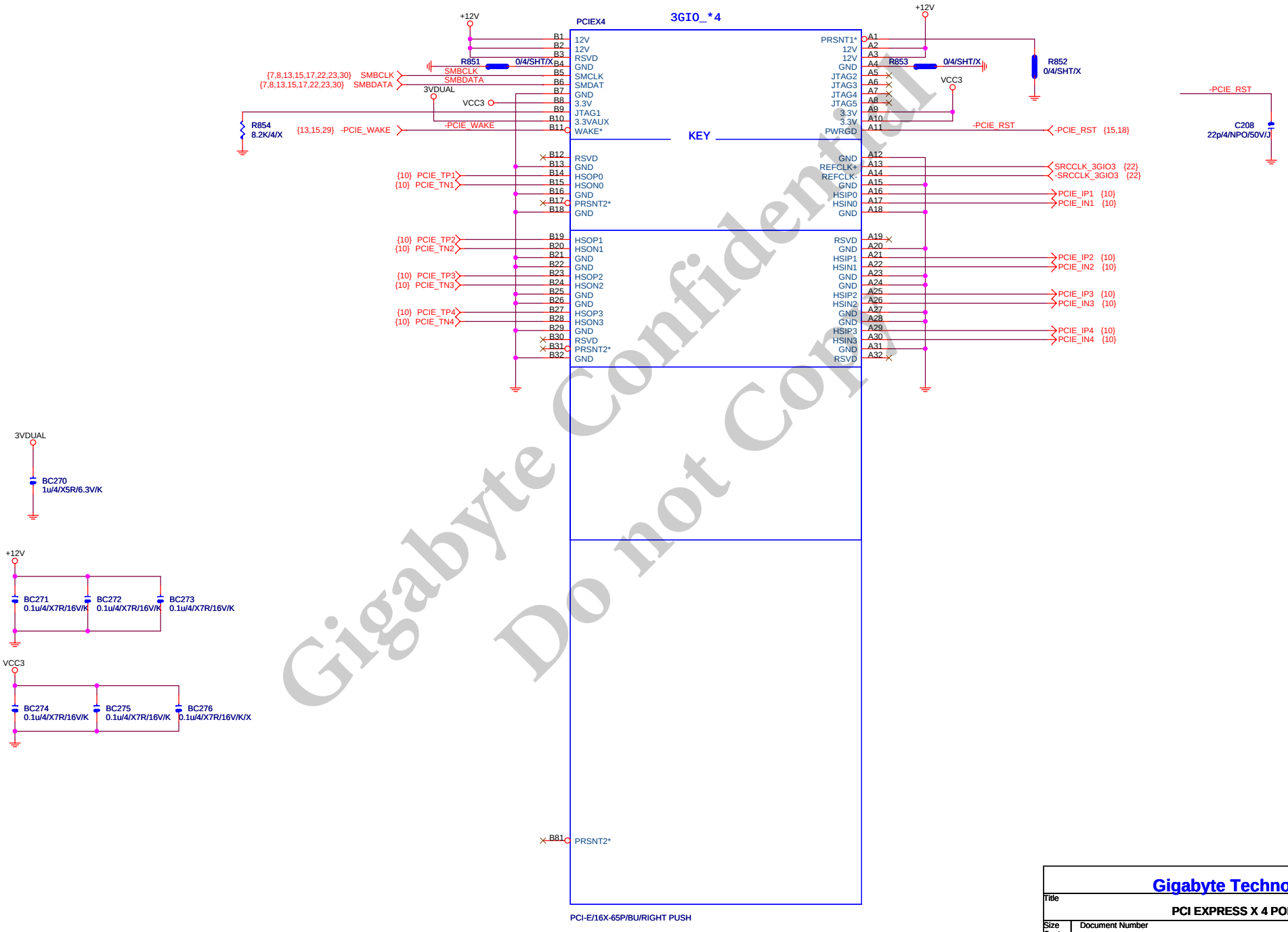

Gigabyte Technology		
Title: PCI EXPRESS X 4 PORT		
Size: Custom	Document Number: GA-P55M-UD2	Rev: 1.0
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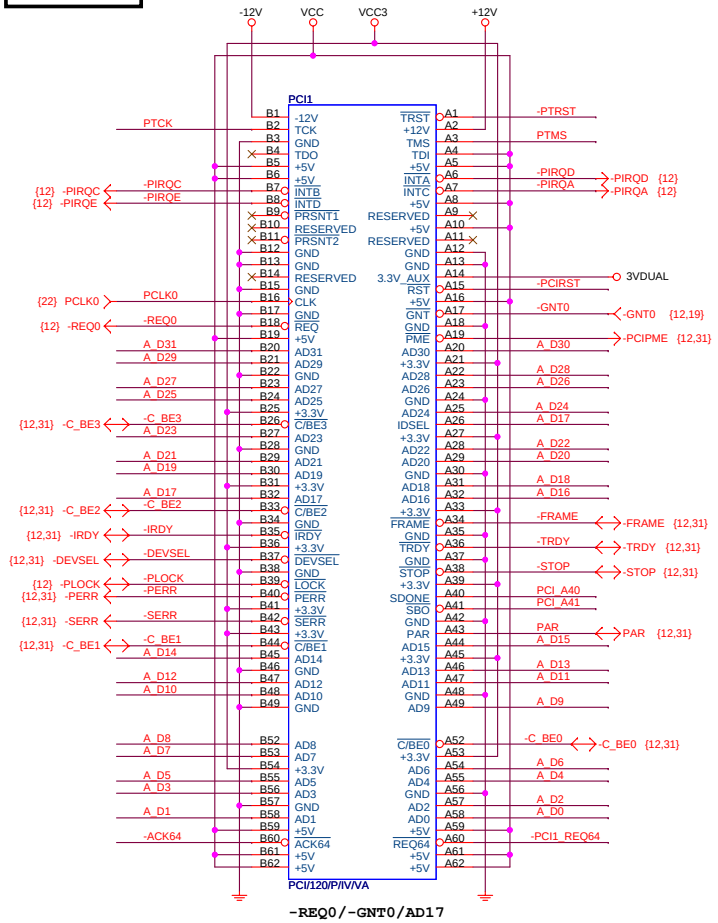
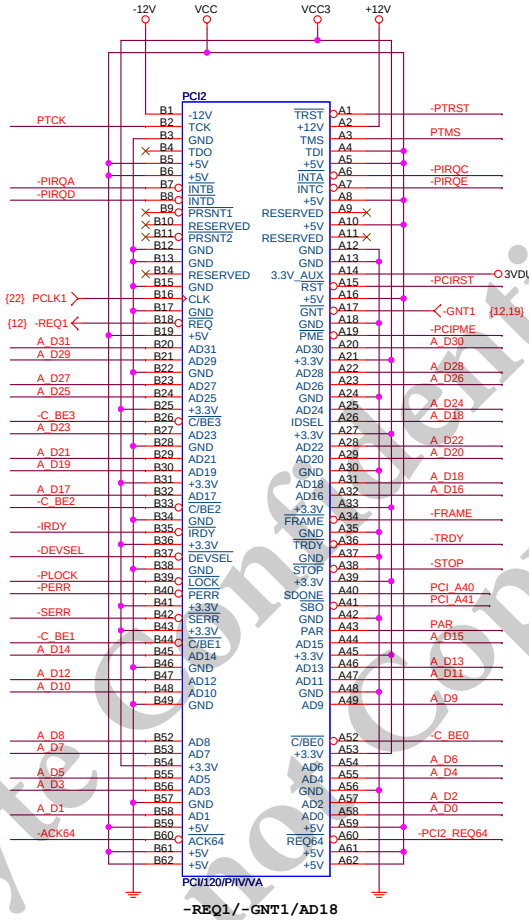
PCI1,2 SLOT





{12,31} A_D[0..31] — A_D[0..31]

-PCIRST {12} — C20 27p/4/NPO/50V/J/X

Place close to PCI1

{7,8,13,15,16,22,23,30} SMBCLK — R242 0/6/SHT/X — PCI_A40
{8,13,15,16,22,23,30} SMBDATA — R238 0/6/SHT/X — PCI_A41

RN4 8.2K/8P4R/4: -PTRST, PTCK, PTMS, VCC

RN11 2.2K/8P4R/4: {12} -REQ1, {12} -REQ2, {12,31} -REQ3, {12} -REQ0, VCC

RN8 2.2K/8P4R/4: VCC, -ACK64, -PCI1_REQ64, PAR, -PCI2_REQ64, PAR {12,31}

3VDUAL — BC40 1u/4/X5R/6.3V/K

RN6 2.2K/8P4R/4: -FRAME, -IRDY, -TRDY, -DEVSEL, VCC

RN7 2.2K/8P4R/4: -PLOCK, -STOP, -PERR, -SERR

RN5 8.2K/8P4R/4: {12} -PIRQD, {12} -PIRQC, {12,31} -PIRQB, {12} -PIRQA, VCC3

RN10 8.2K/8P4R/4: {12} -PIRQG, {12} -PIRQH, {12} -PIRQE, {12} -PIRQF

VCC3 — BC255 0.1u/4/X7R/16V/K — BC256 1u/4/X5R/6.3V/K — BC257 0.1u/4/X7R/16V/K — BC258 1u/4/X5R/6.3V/K

VCC — BC114 0.1u/4/X7R/16V/K/X — EC6 560u/FP/D/6.3V/89/8m

Gigabyte Technology			
Title: PCI SLOT 1, 2			
Size: Custom	Document Number: GA-P55M-UD2		Rev: 1.0
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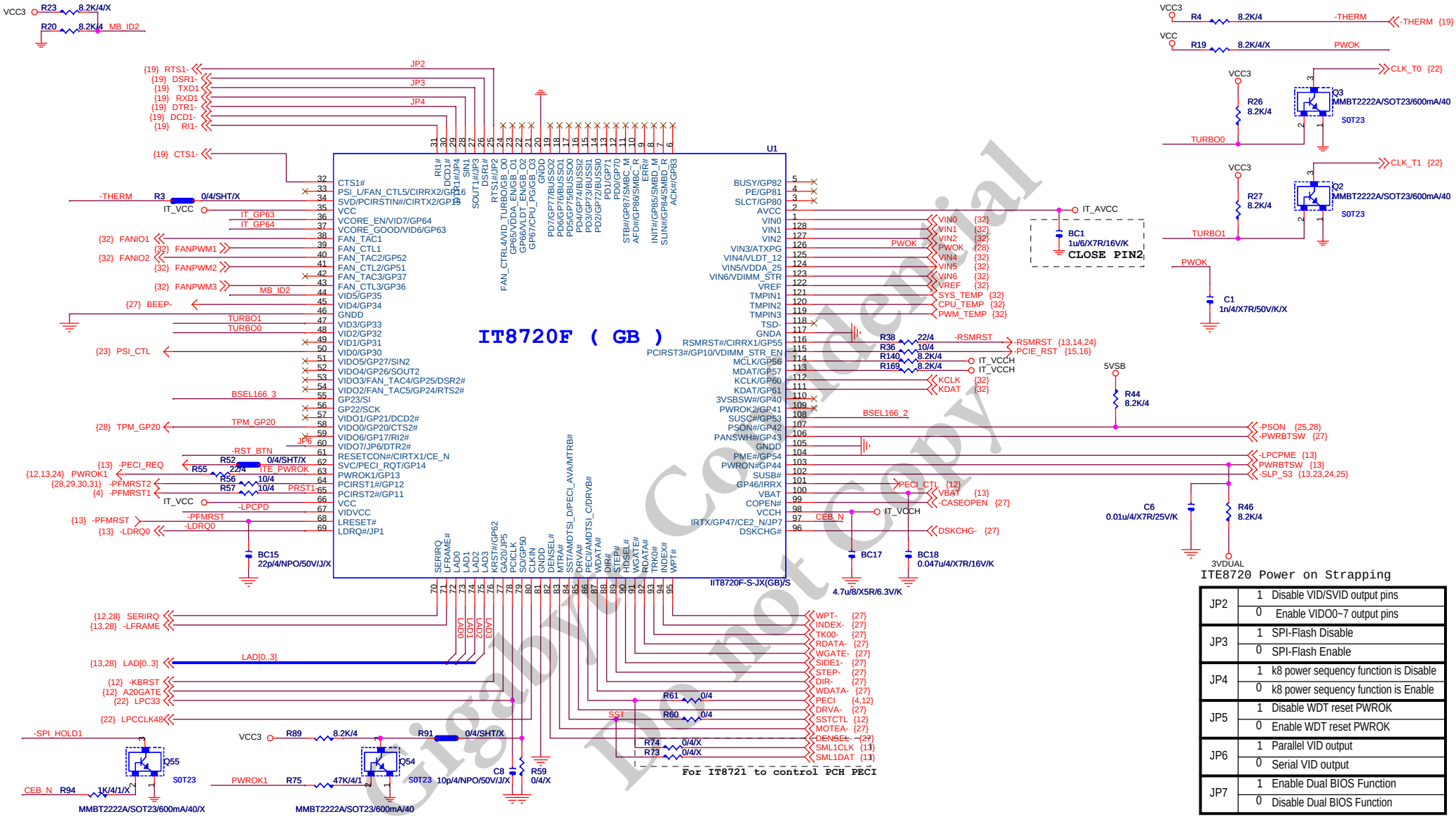
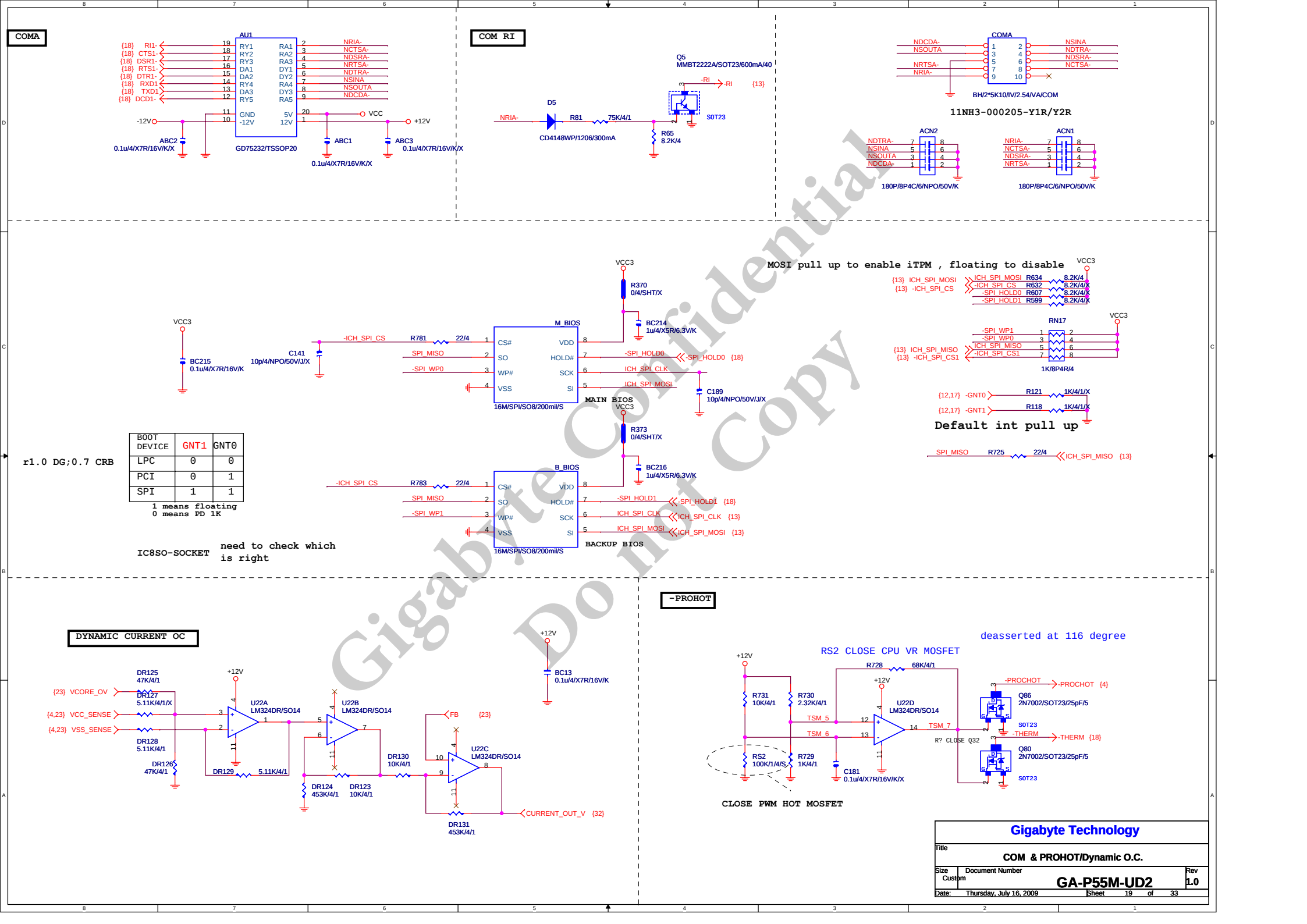


ITE8720 Power on Strapping

JP2	1	Disable VID/SVID output pins
	0	Enable VIDO0~7 output pins
JP3	1	SPI-Flash Disable
	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP5	1	Disable WDT reset PWROK
	0	Enable WDT reset PWROK
JP6	1	Parallel VID output
	0	Serial VID output
JP7	1	Enable Dual BIOS Function
	0	Disable Dual BIOS Function

Gigabyte Technology

Title	ITE 8720 LPC IO	
Size B	Document Number GA-P55M-UD2	Rev 1.0
Date: Thursday, July 09, 2009	Sheet 18 of 33	



AZALIA CODEC

ALC889A+/ALC889A/ALC888Vx Colay

	ALC888-VA ALC888-VC2	ALC888B	ALC889A	ALC889A+
CR49	O	X	O	O
CR46	X	X	O	X
CR57	X	X	O	X
CR47	X	X	X	O
CR48	O	O	O	X
CR26	20K/1%	20K/0.1%	20K/1%	20K/1%

CR2: 20K/4/0.1% @ALC889A
CR2: 20K/4/1% @ALC889A+/ALC888Vx

CR26 20K/4/0.1

{21} CEN
{21} LFE
{21} S_SURR_L
{21} S_SURR_R
{21} SPDIFI
CBC31 470p/4/X7R/50V/K
{21} SPDIFI_I
{21} SPDIF

SURR_R {21}
SURR_L {21}

AVDD
CBC12 0.1u/4/X7R/16V/K

CR40 5.11K/4/1 S_SURR_JD {21}
CR39 10K/4/1 CEN_JD {21}
CR65 47/4/1 FAUDIO_JD {21}
CBC39 1n/4/X7R/50V/K

JD resistors close to pin34 of CODEC

VCC3
CR53 2.2/8
CBC37 22u/8/X5R/6.3V/M

co-layout

CU1

ALC889A+

{21} SPDIFO2_HDMI

CR46 8.2K/4/X
CR57 8.2K/4/X
CR49 0/4/X

{13} ACZ_SDOUT
{13} ACZ_BITCLK
CR58 22/4
{13} ACZ_SDIN2
CR59 22/4
VCC3
{13} ACZ_SYNC
{13} -ACZ_RST

50歐姆:4/5

CR14/CBC4 close to SouthBridge

CBC34 22p/4/NPO/50V/J/X
CBC35 0.1u/4/X7R/16V/K
CBC33 0.1u/4/X7R/16V/K

1 DVDD1
2 GPIO0/XTALI
3 GPIO1/XTALO
4 DVS1
5 SDATA_OUT
6 BIT_CLK
7 DVSS2
8 SDATA-IN
9 DVDD2
10 SYNC
11 RESET#
12 PC_BEEP

48 SPDIFO
47 SPDIFI/EAPD
46 SURBACK-R/XTALSEL
45 SURBACK-L/JD0 GPIO0
44 LFE
43 CEN
42 AVSS2
41 SURR-R
40 JDREF (NC)/JD3
39 SURR-L
38 AVDD2
37 LINE1-VREFOR/VREFO3

36 FRONT-R
35 FRONT-L
34 SENSE B (JD2)/FMIC1
33 DCVOL/VREFVOUT2
32 MIC1-VREFO-R/FMIC2
31 LINE2-VREFO/JD4
30 MIC2-VREFO/AFILT2
29 LINE1-VREFO-L/AFILT1
28 MIC1-VREFO-L/VREFOUT
27 VREF
26 AVSS1
25 AVDD1

LINE_O_R {21}
LINE_O_L {21}

Can Support Amp Out

CR20 8.2K/4/X AVDD
VODR CR14 8.2K/4
MIC1_VREFO_R {21}
LINE2_VREFO {21}
MIC2_VREFO {21}
VOCR {21}
VOBR CR17 8.2K/4
MIC1_VREFO_L {21}

AVDD
22u/8/X5R/6.3V/M

13 SENSE A(JD1)/PHONE JD
14 LINE2-L/AUX-L
15 LINE2-R/AUX-R
16 MIC2-L/JD2
17 MIC2-R/JD1 GPIO1
18 CD_L
19 CD_GND
20 CD_R
21 MIC1-L/MIC1
22 MIC1-R/MIC2
23 LINE1-L
24 LINE1-R

ALC888B-GR/LQFP48

CBC8 0.1u/4/X7R/16V/K
CBC7

Digital Area
Analog Area

CBC2 4.7u/8/X5R/6.3V/K LINE_IN_R {21}
CBC4 4.7u/8/X5R/6.3V/K LINE_IN_L {21}
CBC10 4.7u/8/X5R/6.3V/K MIC1_R {21}
CBC11 4.7u/8/X5R/6.3V/K MIC1_L {21}

50歐姆:4/10

CBC15 0.1u/4/X7R/16V/K CD_R {21}
CBC14 0.1u/4/X7R/16V/K CDGND {21}
CBC13 0.1u/4/X7R/16V/K CD_L {21}

{21} FRONT_JD
{21} LINE1_JD
{21} MIC1_JD
{21} SURR_JD
CR32 5.11K/4/1
CR33 10K/4/1
CR31 20K/4/1
CR38 39.2K/4/1

JD resistors close to pin13 of CODEC

{21} LINE2_L
{21} LINE2_R
{21} MIC2_L
{21} MIC2_R

Can Support Amp Out

CD_RR {21}
CDGND_G {21}
CD_LL {21}

Gigabyte Technology

Title: HD AUDIO ALC889A

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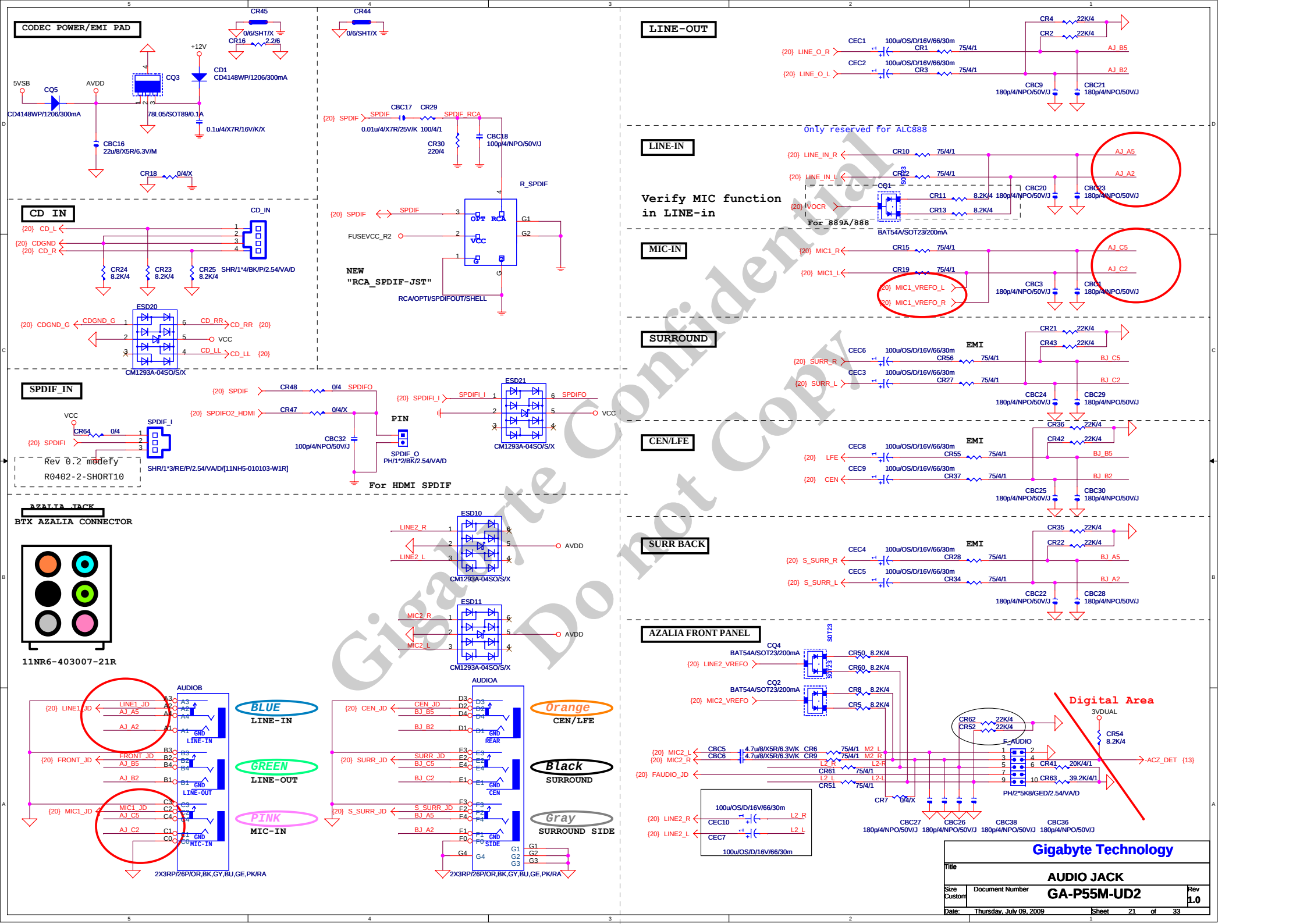
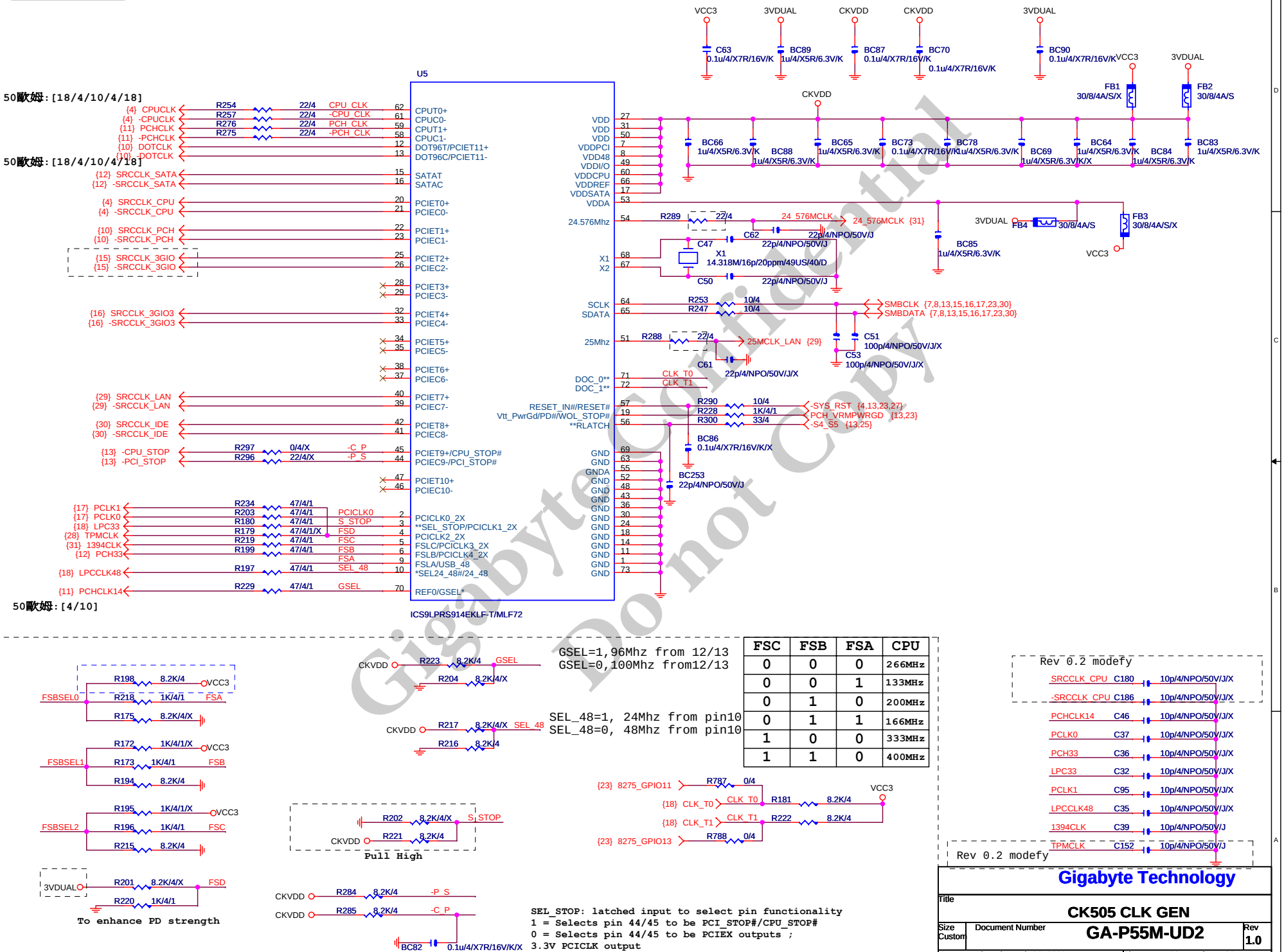


CLK GEN CK505



FSC	FSB	FSA	CPU
0	0	0	266MHz
0	0	1	133MHz
0	1	0	200MHz
0	1	1	166MHz
1	0	0	333MHz
1	1	0	400MHz

Gigabyte Technology

Title: CK505 CLK GEN

Size: Custom | Document Number: GA-P55M-UD2 | Rev: 1.0

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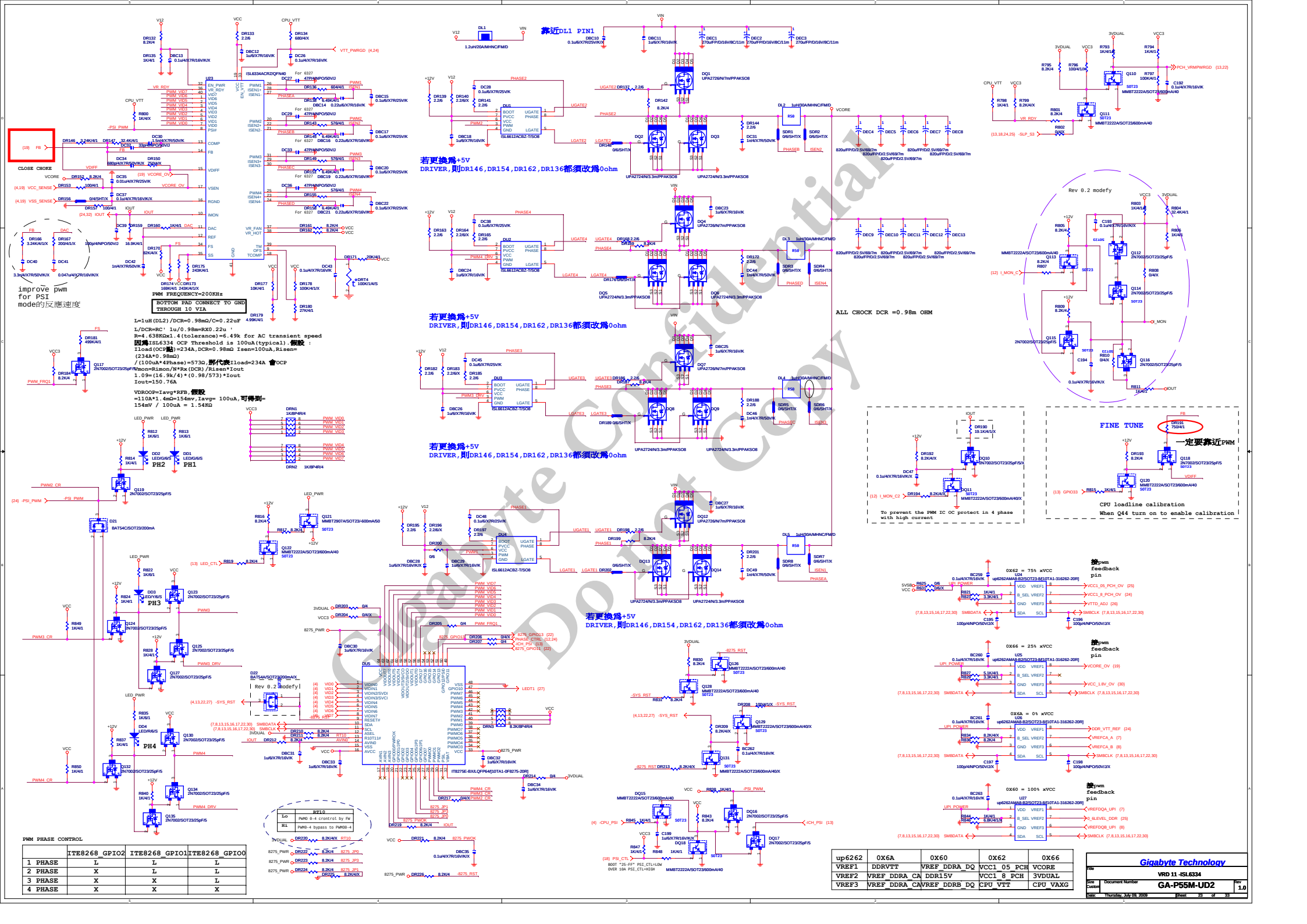

	ITE8268_GPIO2	ITE8268_GPIO1	ITE8268_GPIO0
1 PHASE	L	L	L
2 PHASE	X	L	L
3 PHASE	X	X	L
4 PHASE	X	X	X

up6262	0X6A	0X60	0X62	0X66
VREF1	DDRVTT	VREF_DDRA_DQ	VCC1_05_PCH	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	3VDUAL
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	CPU_VTT	CPU_VAXG

R10	
Lo	PWM0 0-4 crontrol by FW
Hi	PWM0-4 bypass to PWM09-4

Gigabyte Technology	
File	VRD 11 -ISL6334
Size / Custom	Document Number: GA-P55M-UD2
Rev	1.0
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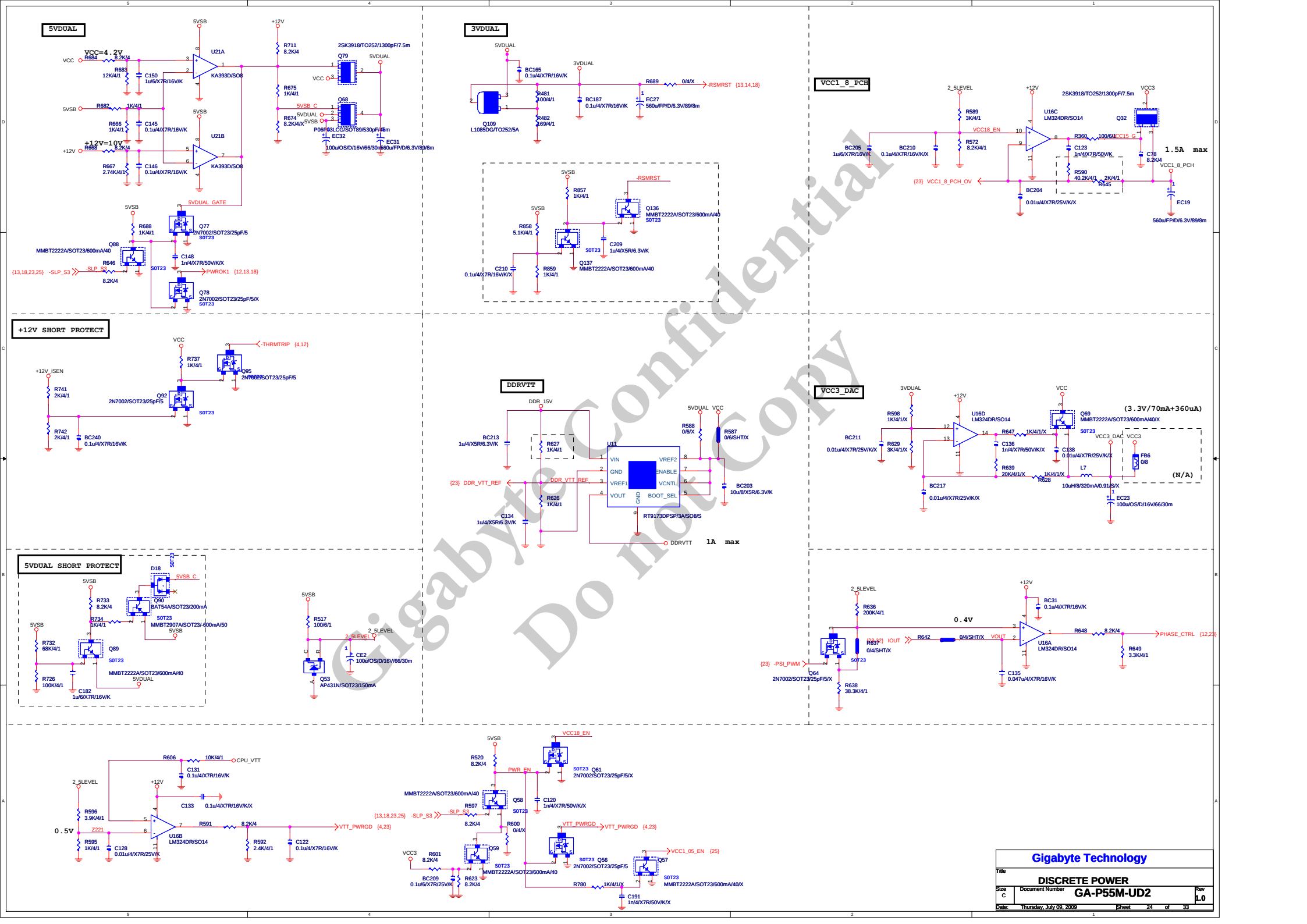

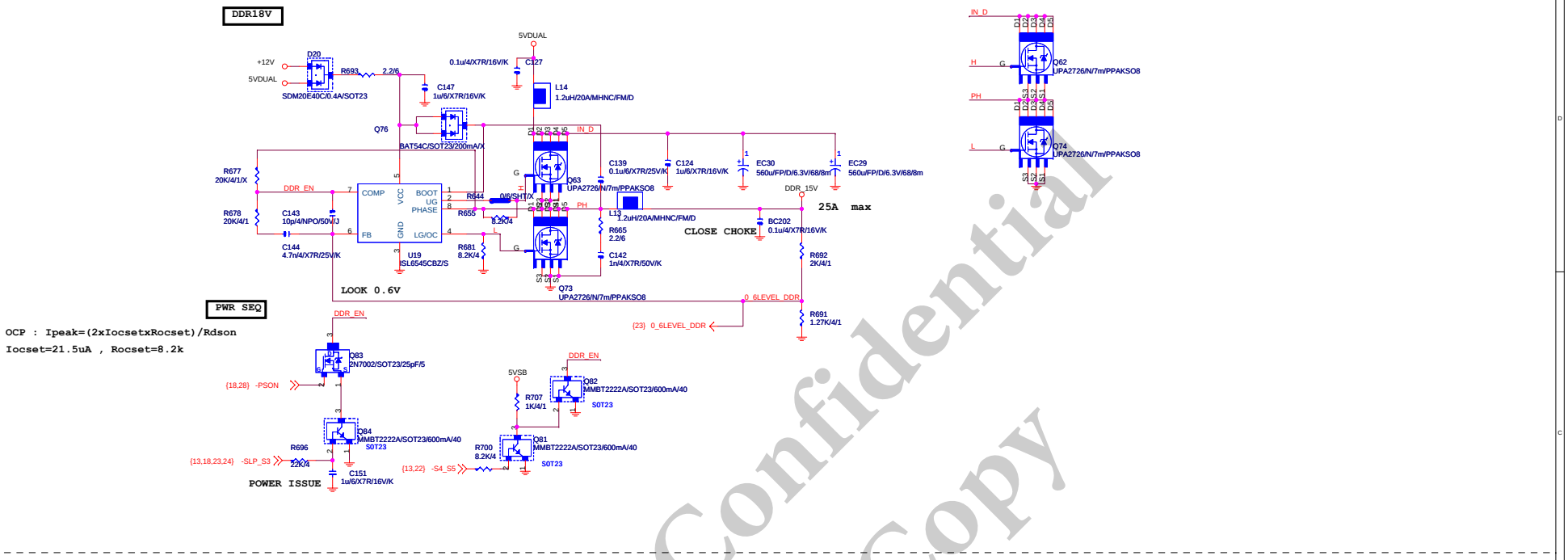

Gigabyte Technology		
Title: DDR_15V		
Size: C	Document Number: GA-P55M-UD2	Rev: 1.0
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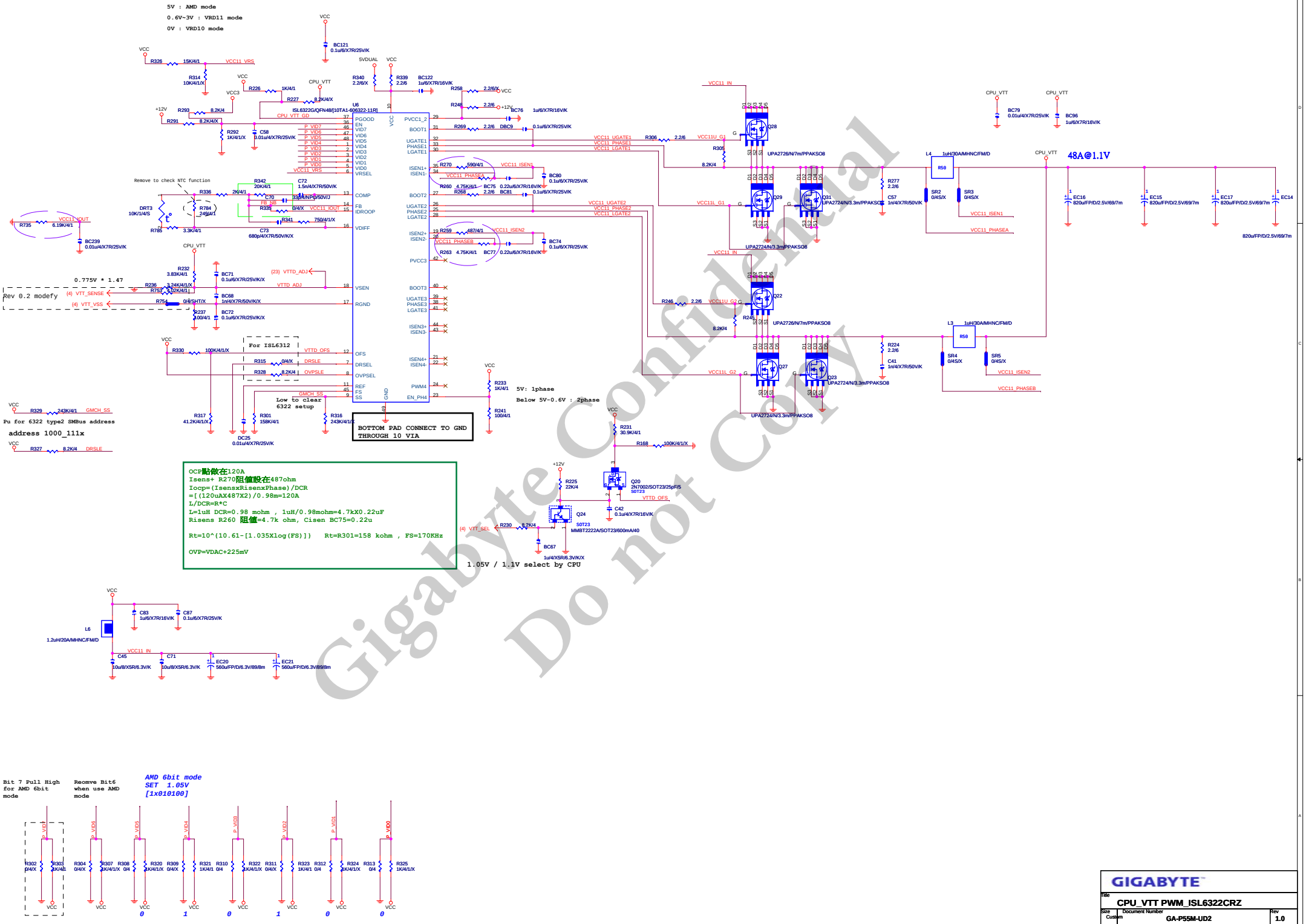

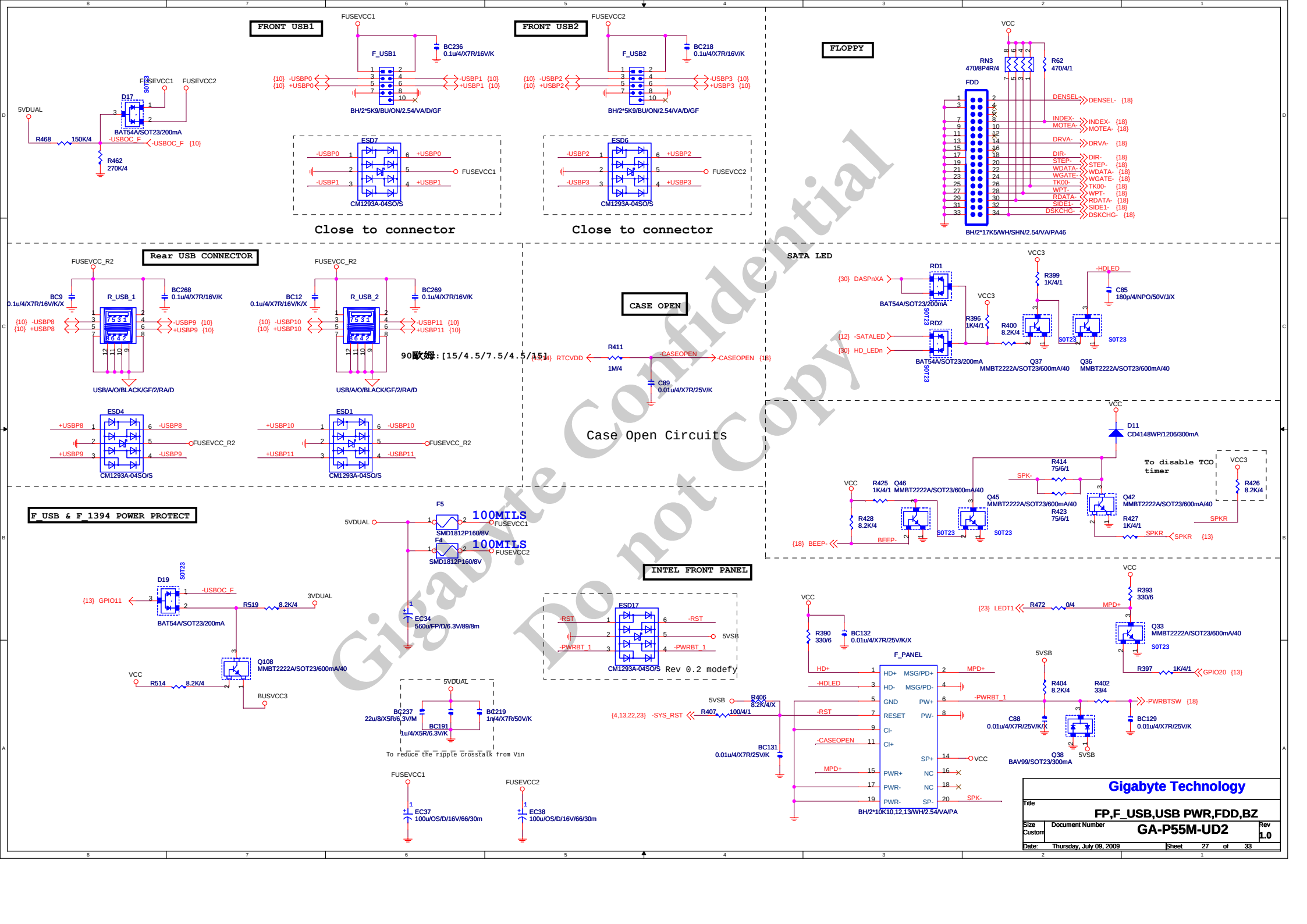
FRONT USB1
FRONT USB2
FLOPPY
Close to connector
Close to connector
Rear USB CONNECTOR
CASE OPEN
SATA LED
Case Open Circuits
F_USB & F_1394 POWER PROTECT
INTEL FRONT PANEL
To disable TCO timer
To reduce the ripple crosstalk from Vin
Rev 0.2 modefy
Gigabyte Technology
FP,F_USB,USB PWR,FDD,BZ
GA-P55M-UD2
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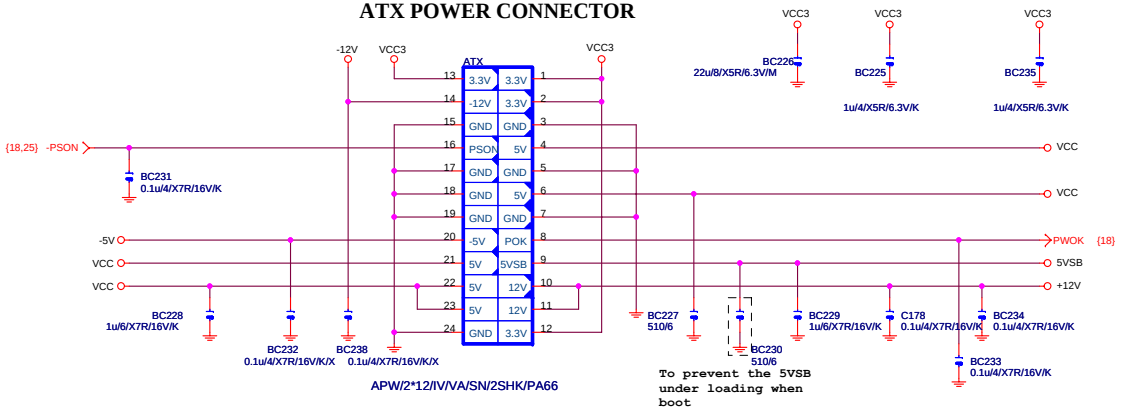
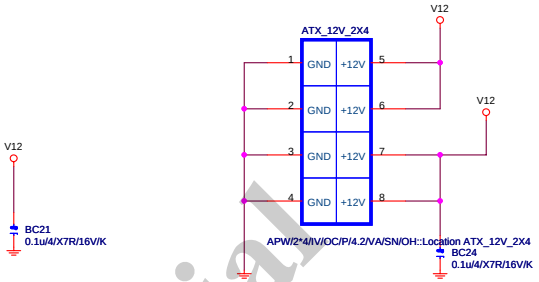
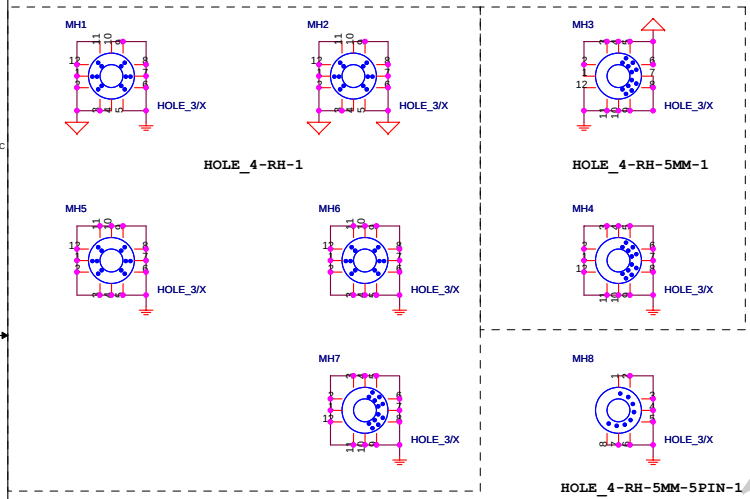
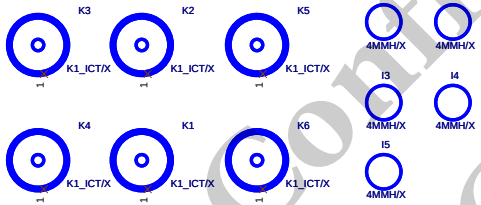
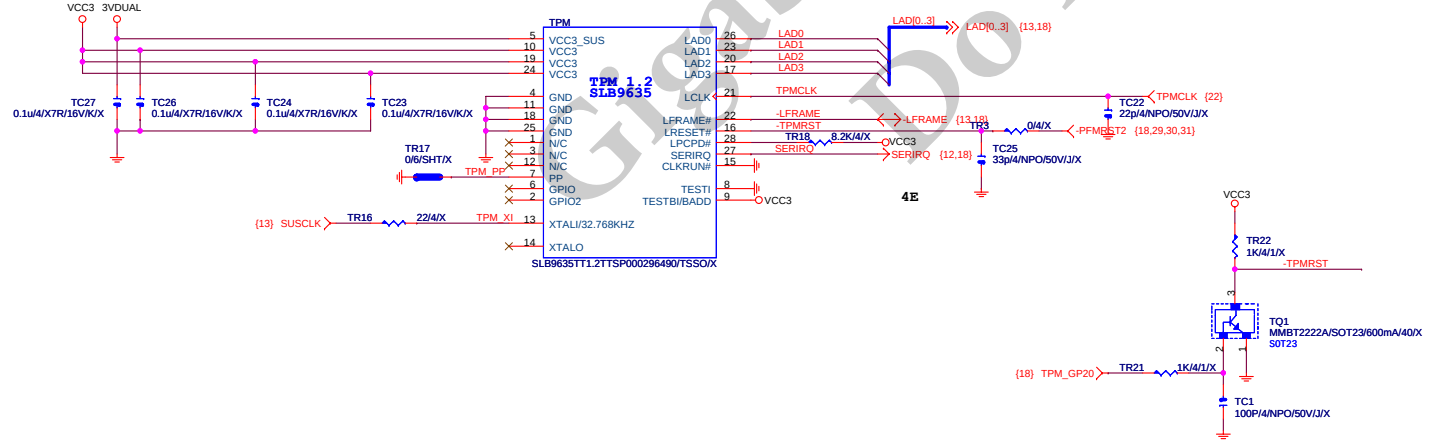
ATX POWER CONNECTOR











Gigabyte Technology			
Title: ATX POWER CONNECTOR			
Size: Custom	Document Number: GA-P55M-UD2		Rev: 1.0
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PCIE-1G LAN

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
VDD15	1.5V	1.2V

for RT8111B N/C
for RT8111C 0 ohm
(Internal Regulator)
for RT8111C N/C
(external Regulator)

離 PIN63 0.5cm以內
For RT8111C
LR16離IC越近越好

RTL8111D-GR/QFN64/[10HP2-408111-70R]

For RTL8111C

80歐姆:[15/5/5/5/15]

SRCCLK 50歐姆:[18/4/10/4/18]

離IC近越好

Dual Color LED
Green
Orange

Single Color LED
Yellow

P35-152-19W9

for RT8111C Mount

FOR CLOSE
PIN1,29,37,40

距離pin1 在0.5cm以內

距離LL2 在0.5cm以內

USB_LAN CONNECTOR

Close to connector

FOR EMI

USB_LAN

UP
DOWN

USB+LAN/1G/GO,Y/OS/RA/D/1

90歐姆:[20/4/8/4/20]

90歐姆:[15/4.5/7.5/4.5/15]

400MILS 240MILS

SMD1812P260/6V

RTL8111DL -->N/A

Gigabyte Technology

Title: REALTEK RTL8111C

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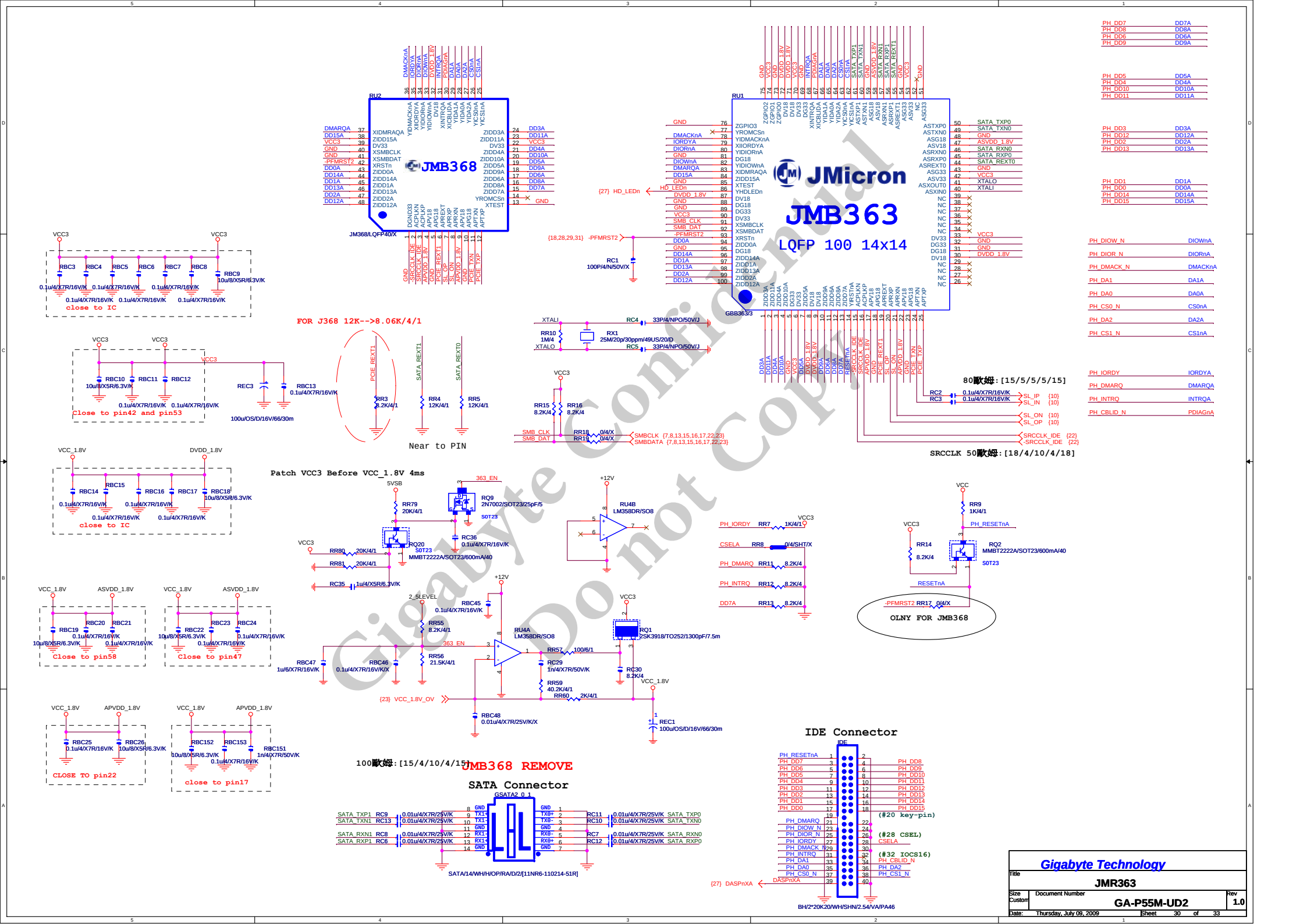

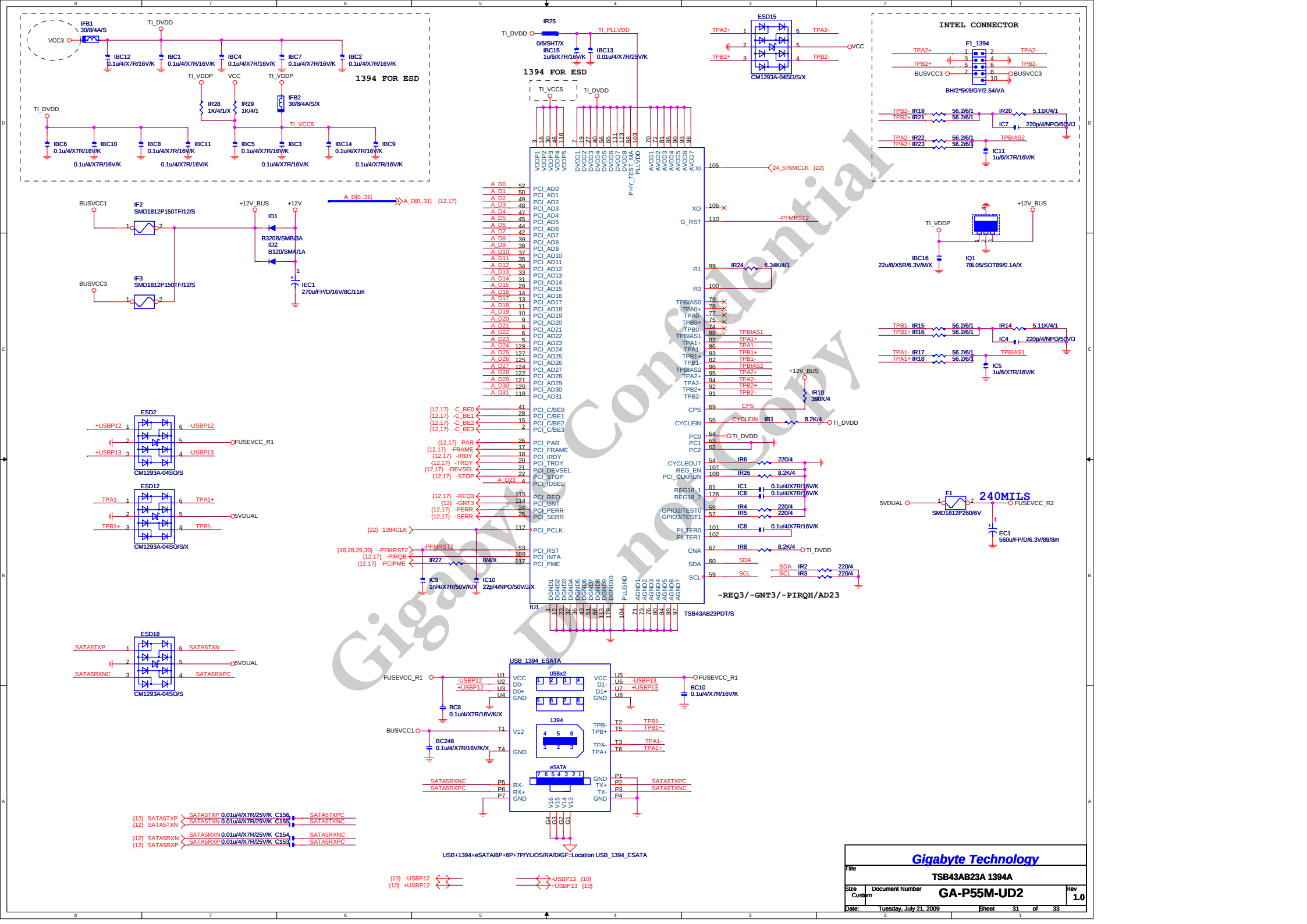
1394 FOR ESD
INTEL CONNECTOR
F1_1394
BH/2*5K9/GY/2.54/VA
TSB43AB23PDT/S
USB_1394_ESATA
USB+1394+eSATA/8P+6P+7P/YL/OS/RA/D/GF::Location USB_1394_ESATA
-REQ3/-GNT3/-PIRQH/AD23
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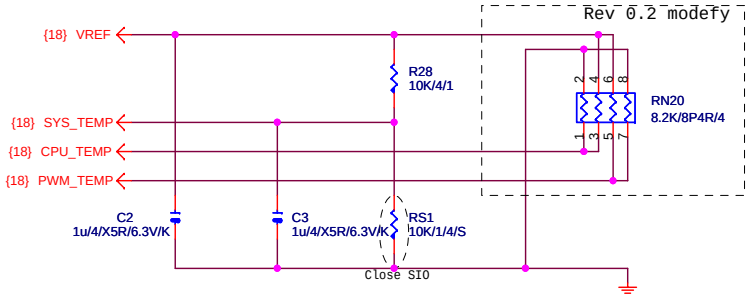
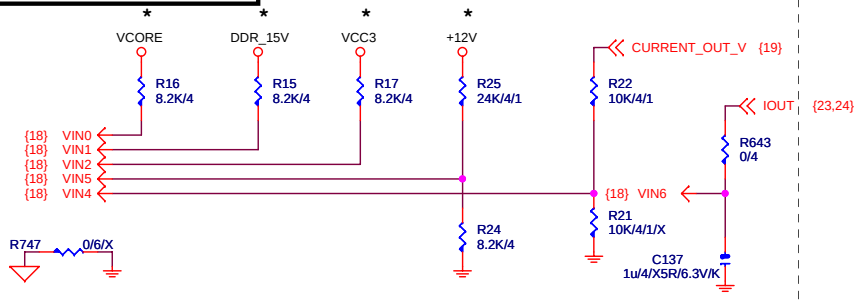
TSB43AB23A 1394A
GA-P55M-UD2
1.0
Tuesday, July 21, 2009

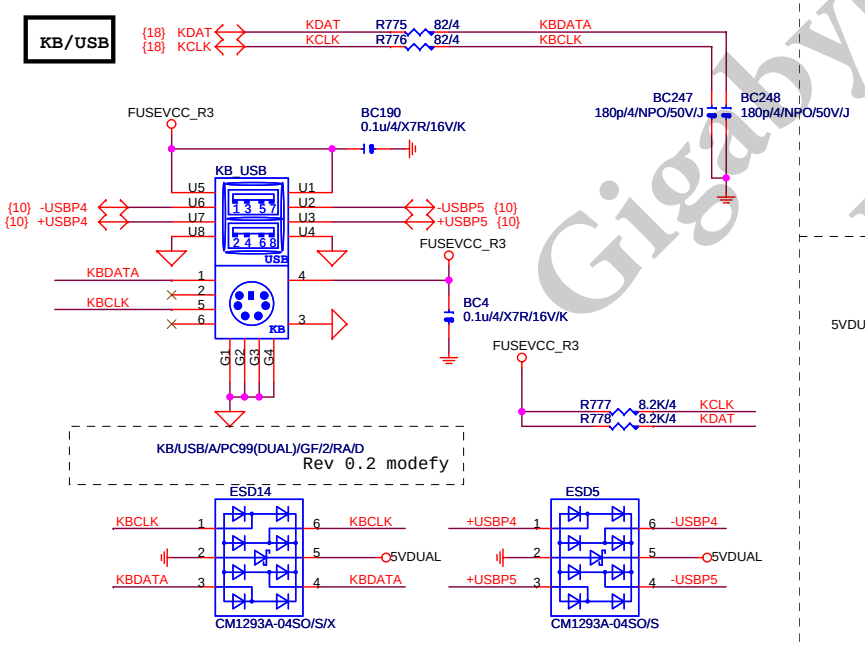
TEMP H/W MONITOR



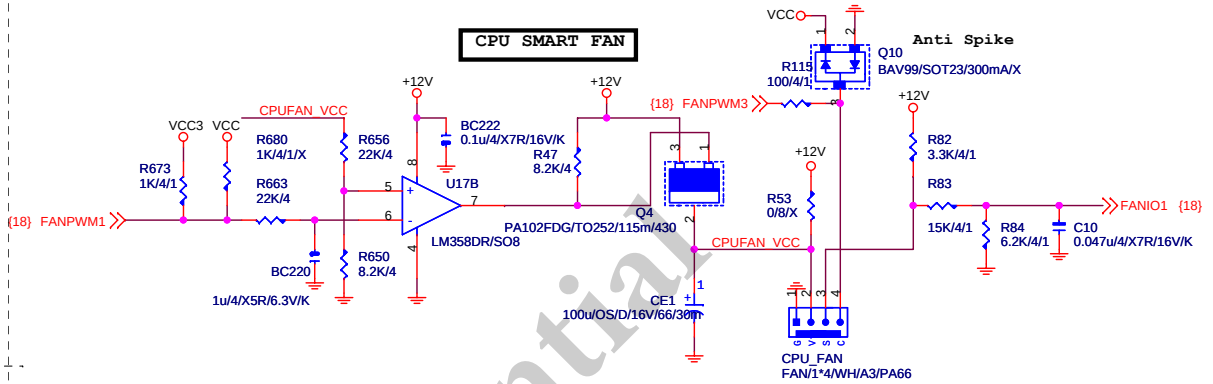
VOLTAGE-- H/W MONITOR



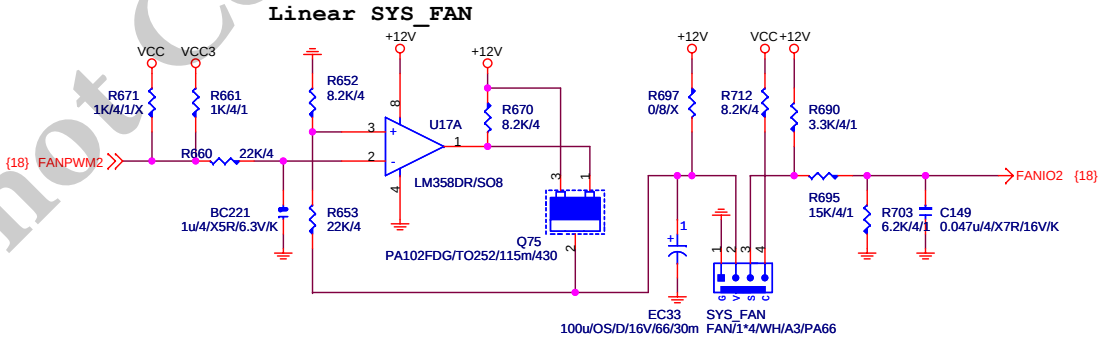
KB/USB

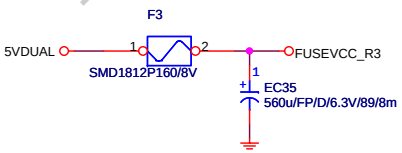


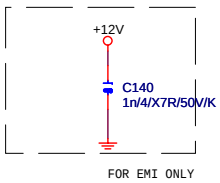
CPU SMART FAN



SYS FAN







Gigabyte Technology		
Title: HWM,KB/MS, FAN CTRL		
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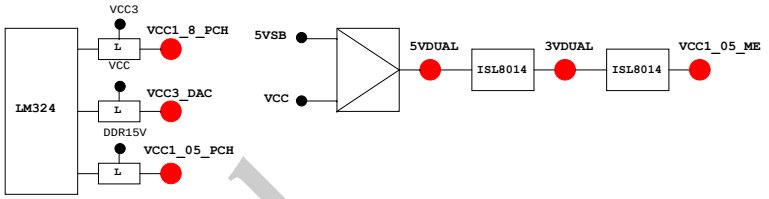
PCH GPIO LIST TABLE

PIN NAME	PWR	AFTER/PLTRST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

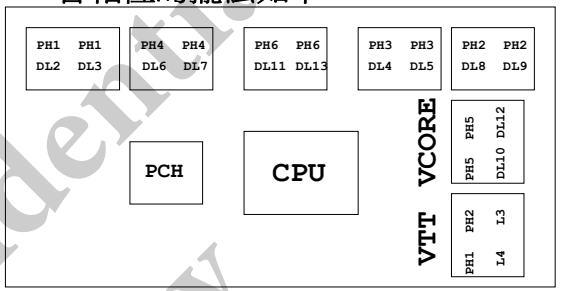
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	空 PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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