Model Name: GA-P55A-UD3 *1.0*

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1156-A
05	CPU_LGA1156-B
06	CPU_LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCH_FDI,DMI,USB,PCIE,NVRAM
11	PCH_DP,CLK BUFFER
12	PCH_HOST,SATA,PCI
13	PCH_GPIO,CTRL,AUDIO
14	PCH_PWR,GND
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOT
18	PCI SLOT 1,2,3
19	ITE 8720 LPC IO
20	COM, -PROHOT , DYNAMIC OC , LPT
21	Dual BIOS
22	ALC888
23	REAR AUDIO JACK
24	CLOCK GEN ICS9LPRS914
25	VCORE PWM ISL6334ACR
26	CPU_VTT PWM_ISL6322G
27	DDR_15V & VCC1_05_PCH PWM_ISL6545CBZ

SHEET	TITLE
28	DISCRETE POWER
29	F_PANEL , F_USB , FDD
30	ATX POWER
31	Marvell 9128
32	REALTEK RTL8111D
33	TPM SLB9635TT
34	HWM,KB/MS , FAN CTRL
35	ESATA JMB362
36	IT8213-1 PATA
37	UP72022
38	TABLE LIST
39	
40	
41	
42	
43	
44	
45	
46	

Gigabyte Technology

Title	Cover Sheet	
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
Date: Friday, November 13, 2009	Sheet 1 of 38	

GA-P55A-UD3 Version: 1.0

Component value change history

Data	Change Item	Reason
EP55A-UD3P 0.2	1. CHECK +12V SHORT PAD FOR 10mil	9. LU1,LU4 RTL8111D --> RTL8111C
	2. F1_1394加蓋(包材階)	10. PCB "育富"移除
	3. ADD DR86=124K/4/1 , DR88=249K/4/1	11. ONFI指定用11SM1-600078-02R
	4. U12~U15 upi6262M --> upi6267M	12. R376 2.26K/4/1 --> 2.55K/4/1
	5. DRAM_PWROK R490=1K/4/1 , R491=3K/4/1	13. 確認上哪種upi6262 10%/upi6267?
	6. REMOVE DR138=0/4 , ADD DR139,DR141=0/4	14. FB7~FB10 REMOVE
	7. RU2指定料號:10HP4-112540-11R	15. PCH BUFFER 25MHz REMOVE "X2,C93,C94,X420"
	8. 排阻指定廠牌用WALSIN	16. BIOS 16M --> 32M (FOR ONFI ONBOARD)
2009/06/10 PBOM:0.1	1.NEW MODEL: P55-UD3P-0.1	
2009/06/24 EBOM:10A	1.ADD -RSMRST PATCH CIRCUIT R866~R868,C192,C193,Q112,Q113,3UDUAL_ICH ADD 5VSB R864,R865	
	2.CHANGE Marvel9123 gpio pin,del RR39,R10,RR67,RR65,ADD RR62	
	3.CHANGE IT8275 料號,DR84 100--->0	
	4.MARVELL 9123----->JMB363	
	5.J363/J632 PATCH POWER SEQUENCE;Q50 MOS--->BJT	
2009/07/7 PBOM:10B	1.P-BOM	
2009/07/10 PBOM:10C	1.RBC53 0.1UF----->1UF	
2009/07/16 PBOM:10D	1.移除PLL電容,BC136,BC150,BC185,BC201	
2009/07/22 PBOM:10E	1(CE2,EC32,EC37,EC38,EC23,EC36,REC3)100uf cap 6*6改成6.3*10.5mm ,因缺料	
	2.VCC3_DAC直接由VCC3經0 ohm提供	
2009/07/29 PBOM:10F	1.ADD R190 1K/4/1 FOR PCIE OVERCLOCK	
2009/08/24 EBOM:29T	1.P55-UD3P-3.0 FOR 9123/USB3.0/8213	
2009/09/9 EBOM:29A	1.CHANGE 9123;USB3.0 MP料號	
2009/10/01 EBOM:02	1.E-BOM	
2009/10/01 PBOM:10A	1.P-BOM	
2009/11/04 PBOM:10B	1.MOS HEATSINK加替料,DEL ESD3	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
EP55A-UD3P 0.2	1. REMOVE AUDIO ESD	7. 1394 "IEC1" NET SWAP & SHORT PROTECT
	2. REMOVE CPU_VAXG	8. PIN HEATER CHECK
	3. PCH_CLK 改 SHORT PAD (0 ohm維持10pcs以下)	9. ITE8275 SYS_RST PATCH
	4. ITE8275 GPIO11,GPIO13 TO TURBO0/TURBO1	10. BC118,BC119 --> TBC29,TBC30
	5. F_PANEL UPDATE H2X10PANEL-1	11. BC5靠近M_BIOS PIN8 , BC6靠近M_BIOS PIN8
	6. ONFI 改 ON BOARD	12. U2 7474 REMOVE
EP55-UD4P 0.2	1.ONFI作塞孔	
2009/05/20 PCB:0.1	1.NEW MODEL: P55-UD3P-0.1由EP55A-UD3P-0.2修改	
2009/06/10 PCB:0.1	1.NEW MODEL: P55-UD3LP-0.1由P55-UD3P-0.1修改	
2009/06/24 PCB:1.0	1.P55-UD3P-1.0 2.修改文字面	
	3.ADD -RSMRST PATCH CIRCUIT,3UDUAL_ICH ADD 5VSB	
	4.ADD J362 POWER SEQUENCE PATCH CIRCUIT,VCC3&362_1.8V	
	5.MARVELL 9123--->J363(SPEC 變動)	
2009/07/07 PCB:1.01	1.修改文字面,加入crossFire X(PM-SALES REQUEST)	
	2.連帶更改FB5,CR64,RN21 short-wire----->電阻;ESD17 5VDUAL--->5VSB	
2009/08/21 PCB:2.9T	1.P55-UD3P-3.0 FOR 9123/USB3.0	
	2.實驗4層板及6層板(不同內層切割)	
2009/09/08 PCB:2.91	1.ADD PCIEX1 SLOT DETECT PIN FOR BIOS	
	2.EACH USB PORT USE ONE POLYFUSE	
	3.修正X16/X8 TURBO MODE 線路	
	4.調整PCICLK,USB_SEL GPIO GP40 TO GP23	
2009/09/18 PCB:1.0	1.修正X16 lane9接至switch for 9128/usb3.0 GNE2時可以斷開x16 slot端	
	2.版本改0.1,ALC888--->ALC889	
2009/09/21 PCB:0.1	1.由P55A-UD3P-1.0修正.SPEC 12相CPU爲8相	
	2.DEL ESATA,NEC SWITCH	
2009/10/01 PCB:0.2	1.add NEC switch,USB 2.0 switch	
2009/10/02 PCB:1.0	1.由0.2改爲1.0版	

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Title: BOM & PCB MODIFY HISTORY

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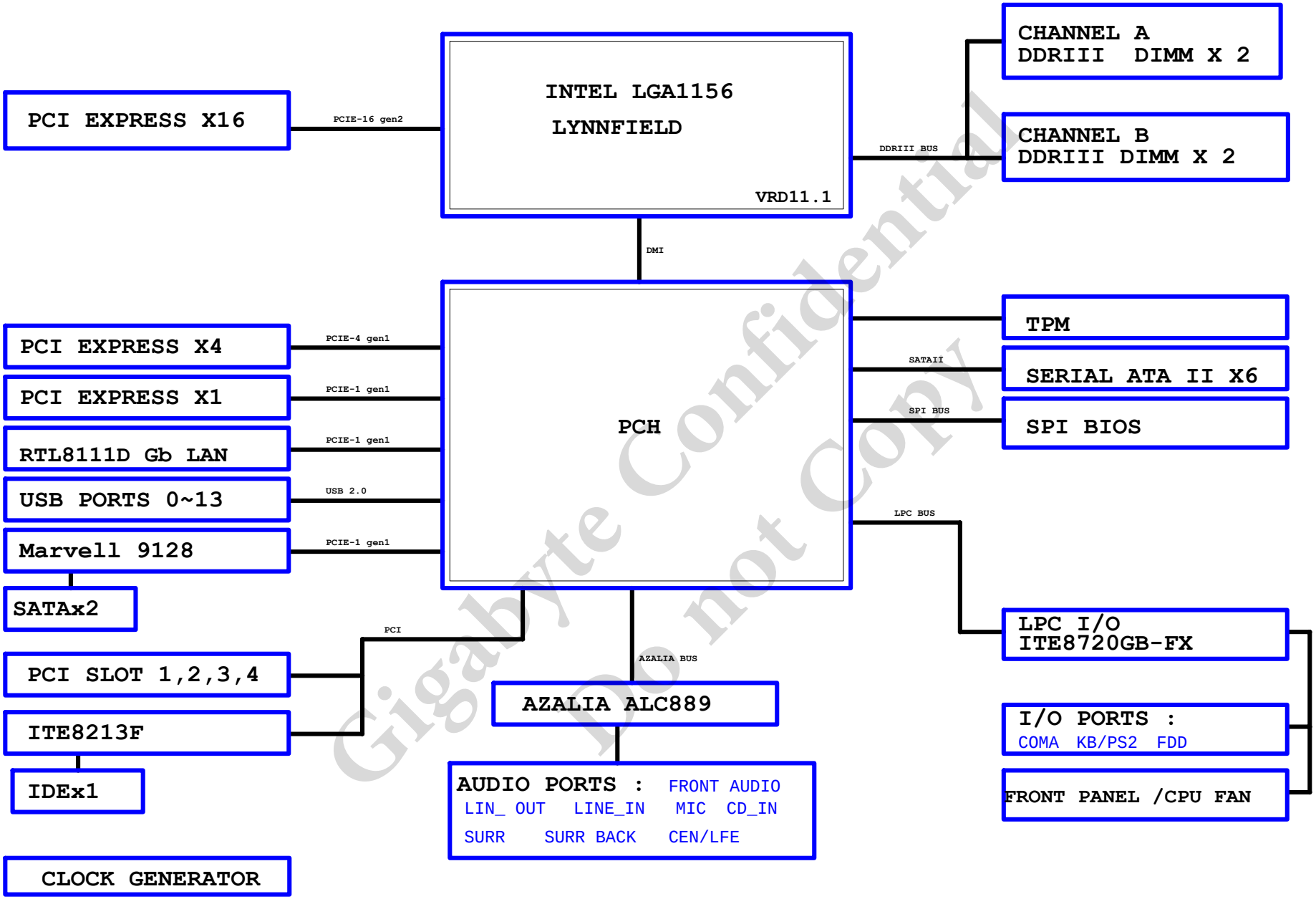
BLOCK DIAGRAM



Gigabyte Technology		
Title: BLOCK DIAGRAM		
Size: C	Document Number: GA-P55A-UD3	Rev: 1.0
Date: Friday, November 13, 2009	Sheet 3 of 38	

FDI : 16/5/5/5/16(breakout min 8/4/5/4/8)
Impedance=80 +- 17.5%

PCIEX16:16/5/5/5/16(breakout min 8/4/5/4/8)
Impedance=80 +- 17.5%

DMI:12/5/5/5/12
Impedance=80 +- 17.5%

CFG0=1: 1X16 PEG
CFG0=0: 2X8 PEG

LGA1156E

LGA1156D

LGA1156C

MISC

5 OF 10

CPU-SK/1156/S/15

DISPLAY LINK

4 OF 10

PEG

3 OF 10

DMI

EUP

3VDUAL_ICH

CPU_VTT

Rev 0.2 modefy

Check Trace length/ width

For PCIE2.0 issue
Must remove after
fixed issue

CFG 0-5 all internal PULL-UP

CFG	H	L	NOTE
0			H:1X16 , L:2X8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		
7	RSVD		ENGINEERING EXPERIMENT
15	RSVD		ENGINEERING EXPERIMENT

POWER ON CONFIG TABLE (Default=1.2250V)

	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CFG0	1
VID4	IMON CFG1	1
VID5	IMON CFG2	1
VID6	RSVD	
VID7	VRD SEL	LOW
PSI#	RSVD	LOW

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Title: CPU LGA1156-A

Size: Custom | Document Number: GA-P55A-UD3 | Rev: 1.0

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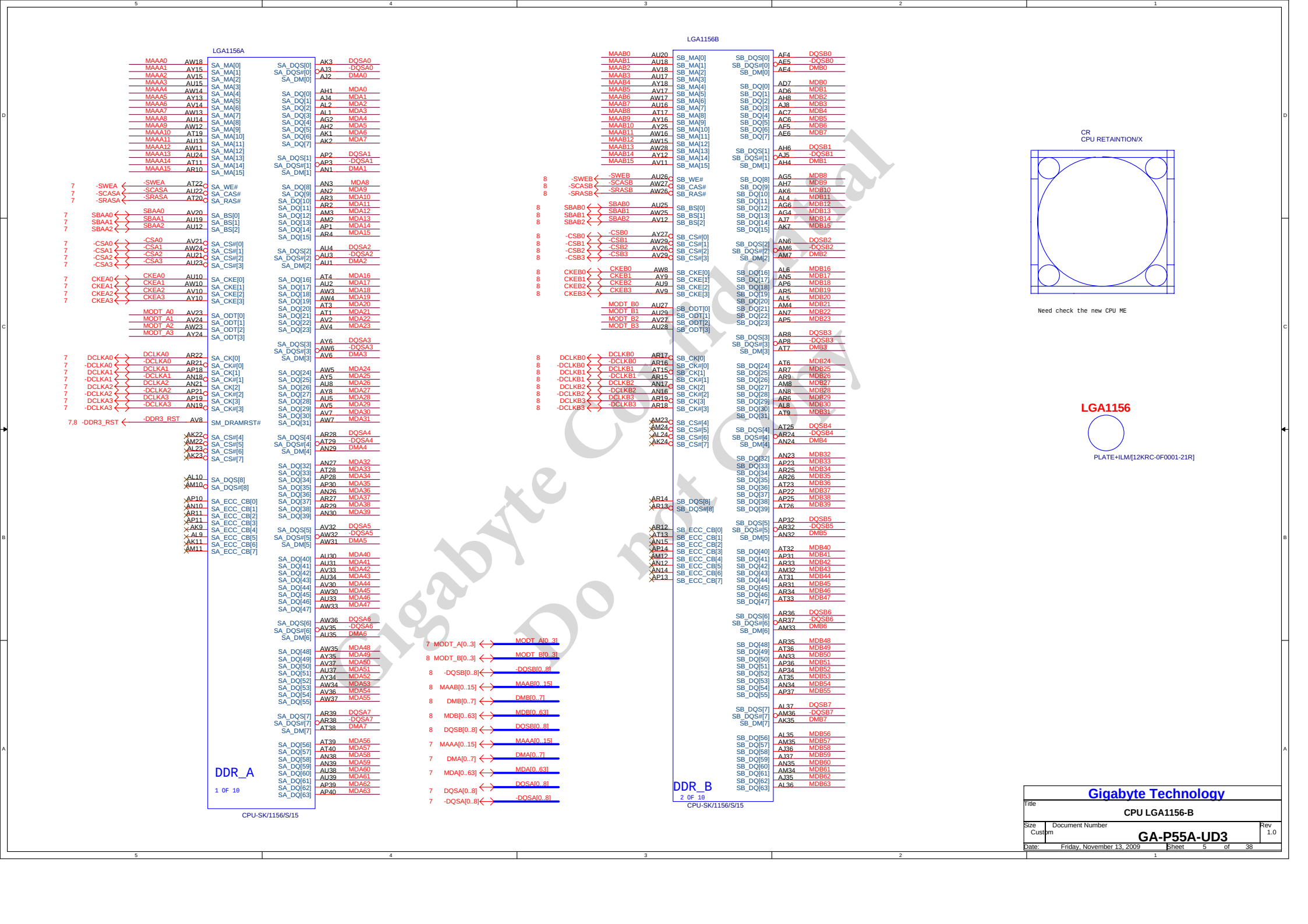

Title	CPU LGA1156-B
Size	Custom
Document Number	GA-P55A-UD3
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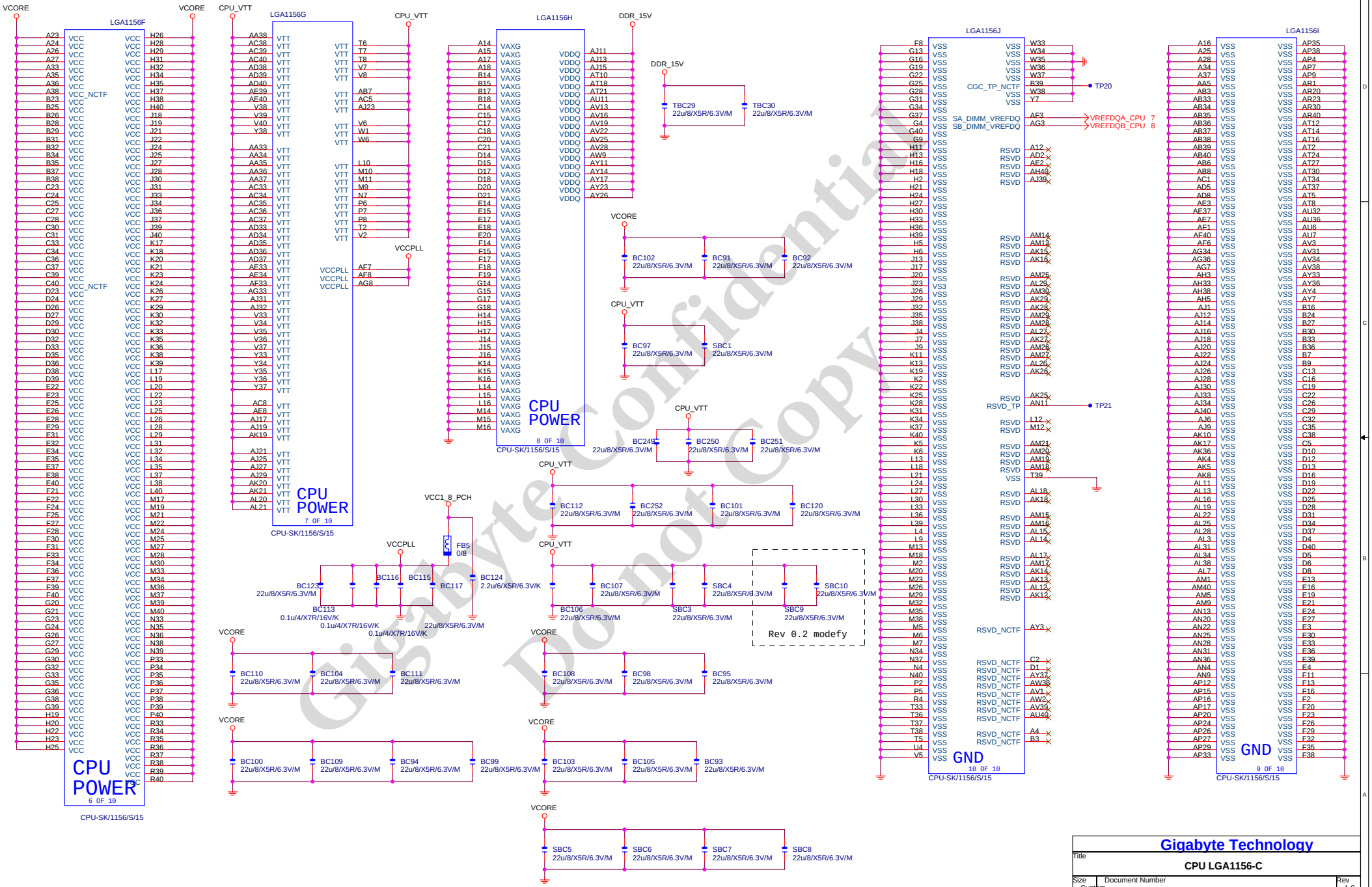
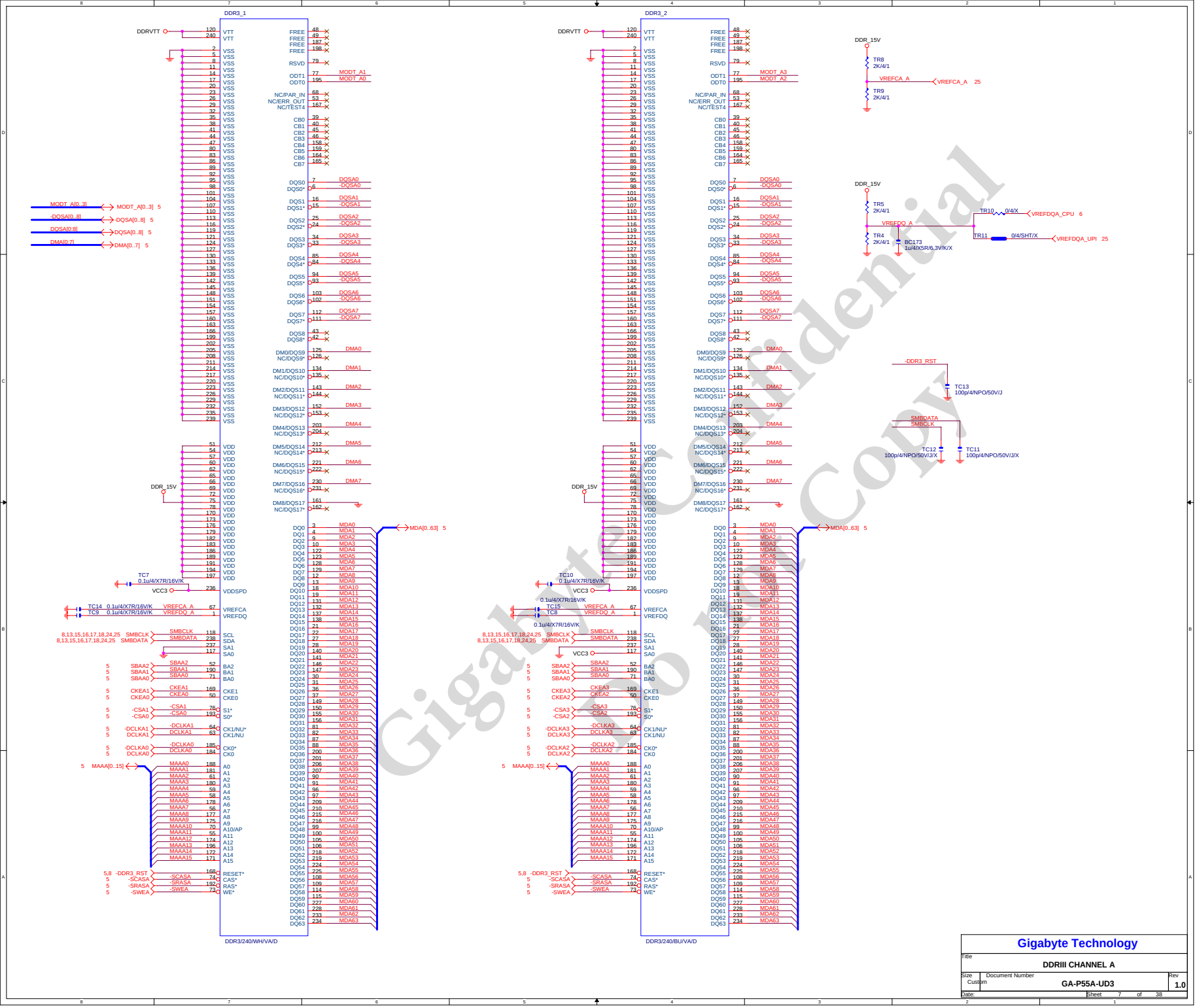
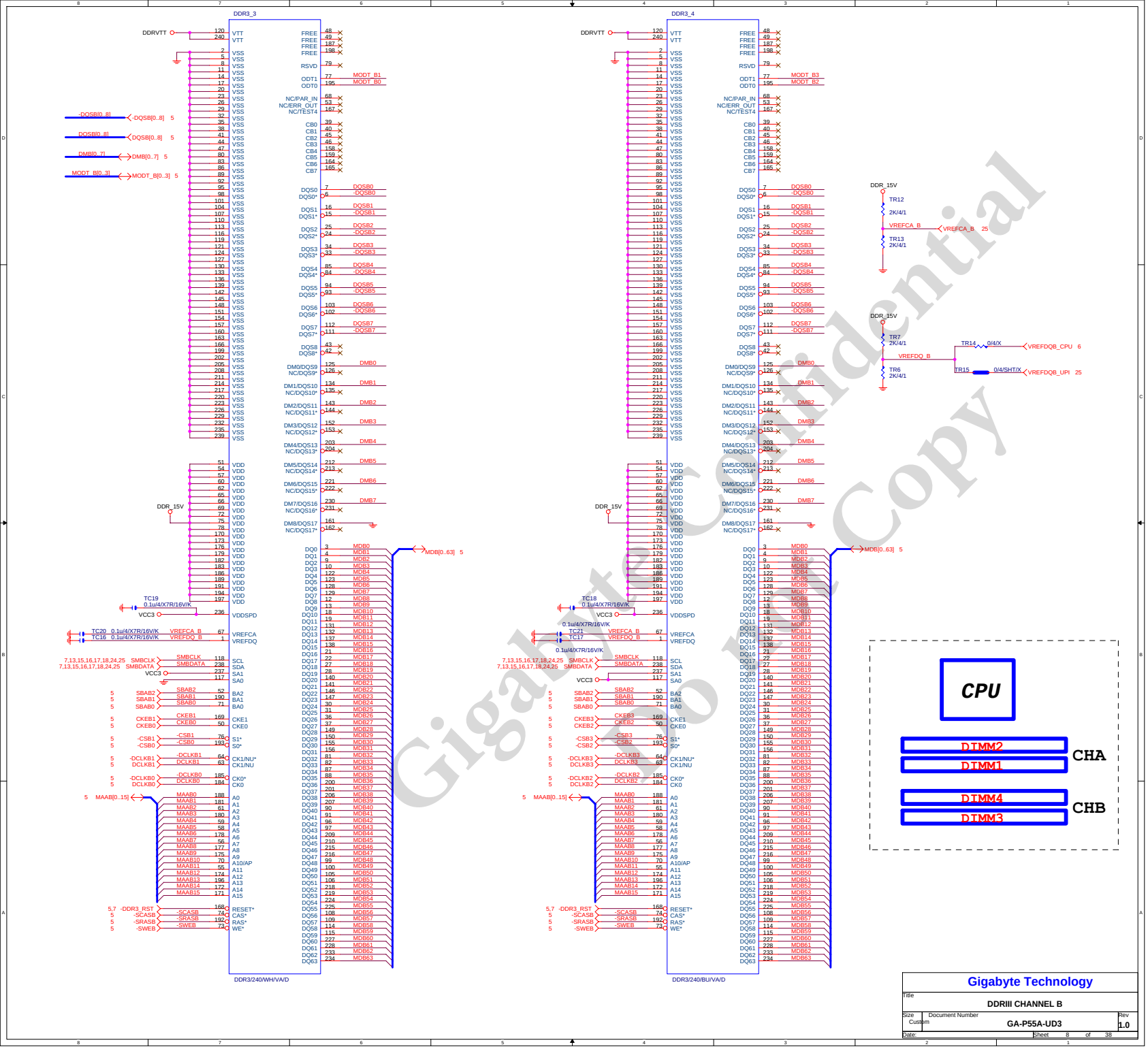
Gigabyte Technology



Gigabyte Technology		
Title: CPU LGA1156-C		
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
Date: Friday, November 13, 2009	Sheet 6 of 38	

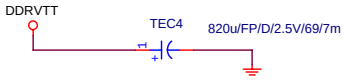


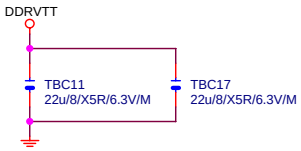
Gigabyte Technology		
Title: DDRIII CHANNEL A		
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
Date:	Sheet 7 of 38	

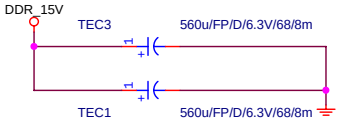


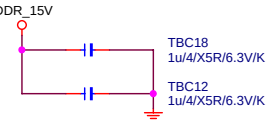
Gigabyte Technology		
Title: DDRIII CHANNEL B		
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
Date:	Sheet 8 of 38	

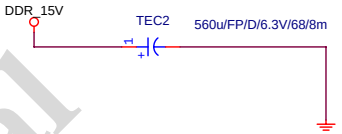
DDR TERMINATION CHANNEL A/B



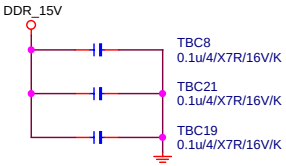




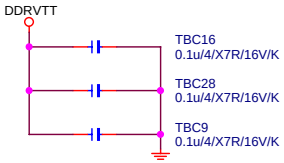


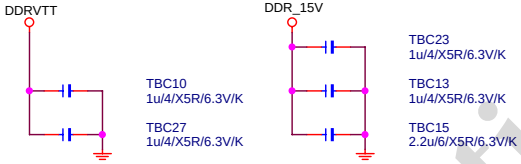


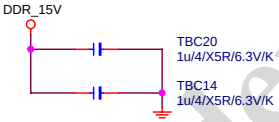
DDR15V Decouple

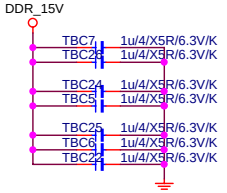


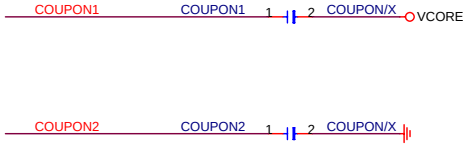
DDRVTT Decouple











Gigabyte Technology		
Title: DDRIII POWER CAP		
Size: B	Document Number: GA-P55A-UD3	Rev: 1.0
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DMI:12/5/5/5/12
Impedance=80 +- 17.5%

PCIE X1 :15/5/5/5/15
Impedance=80 +- 17.5%

電容要靠近 slot 端

PCHB

BD82P55-B2/S/[10HB1-038255-20R]

USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%

Rev 0.2 modefy

OC[3:0]# for Device 29 (ports 0-7)

OC[7:4]# for Device 26 (ports 8-13)

PCHE

NVRAM

BD82P55-B2/S/[10HB1-038255-20R]

Impedance=50+- 15%
ONFI: NV_DQ 4/5
NV_DQS 4/10
NV_CTRL 4/10
NV_CK 4/15

NB_HEATSIN

HEAT SINK/EP55-UD4P/PIN/ZHIHAN/[12SP2-060010-12R]

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5_6#	USB10~13
OC7#	

NV_ALE	
Hi	Enable Danbury
Lo	Disable Danbury

Intel anti theft techonlogy

DMI Terminator voltage
LO : DC COUP : HALF SWING
HI : AC COUP : TX/RX TO VCC

Title	PCH FDI,DMI,USB ,PCIE,NVRAM
Size	B
Document Number	GA-P55A-UD3
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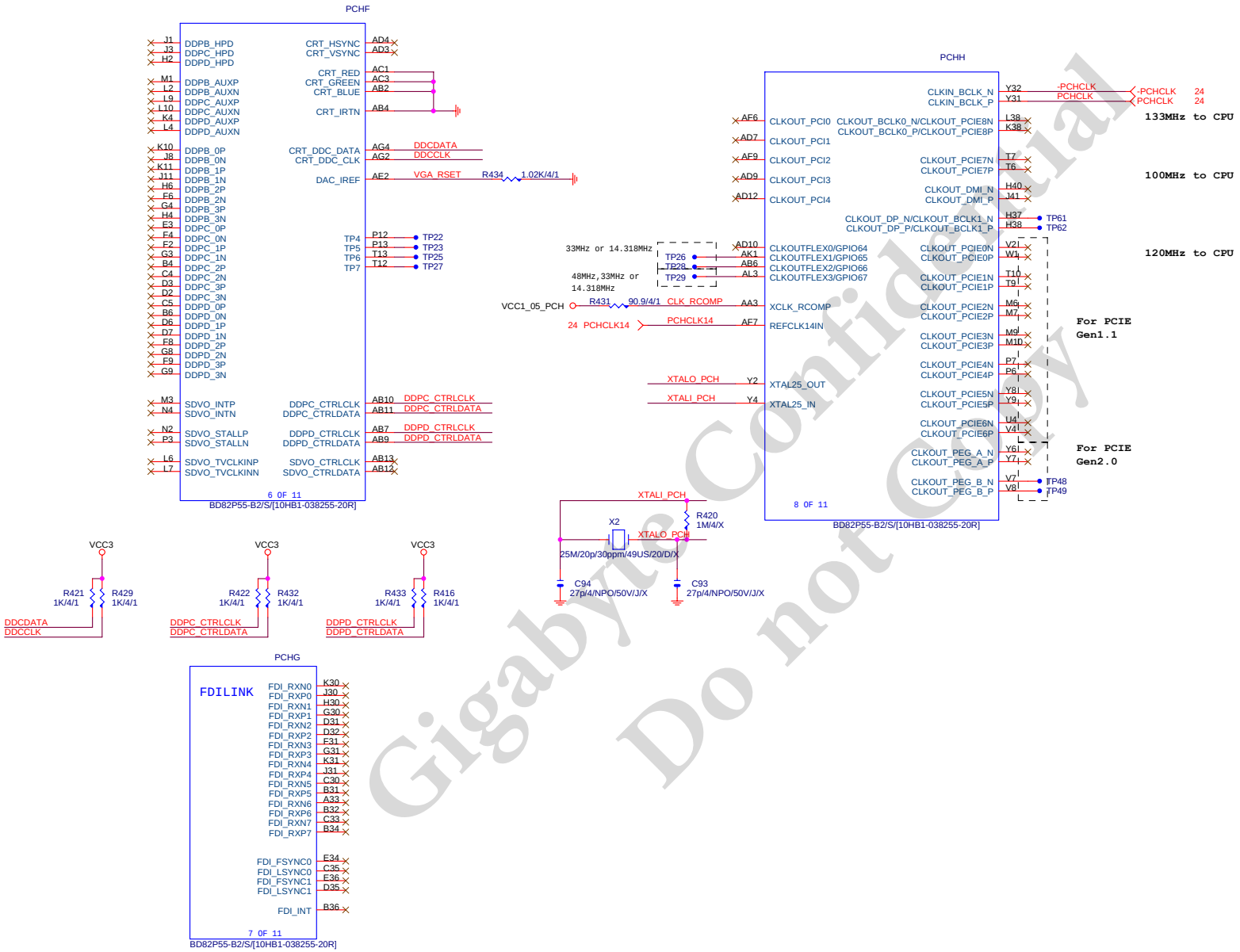
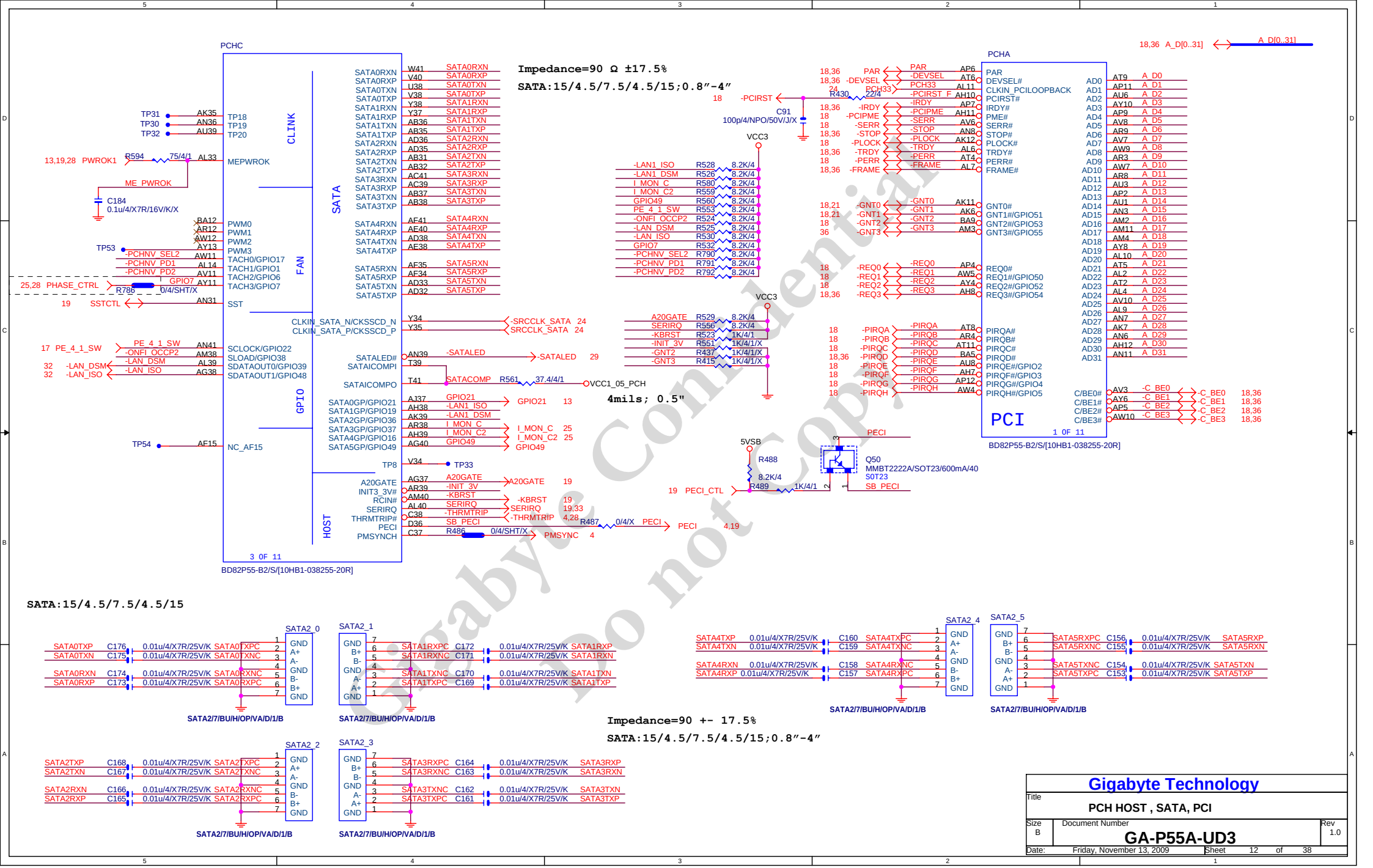
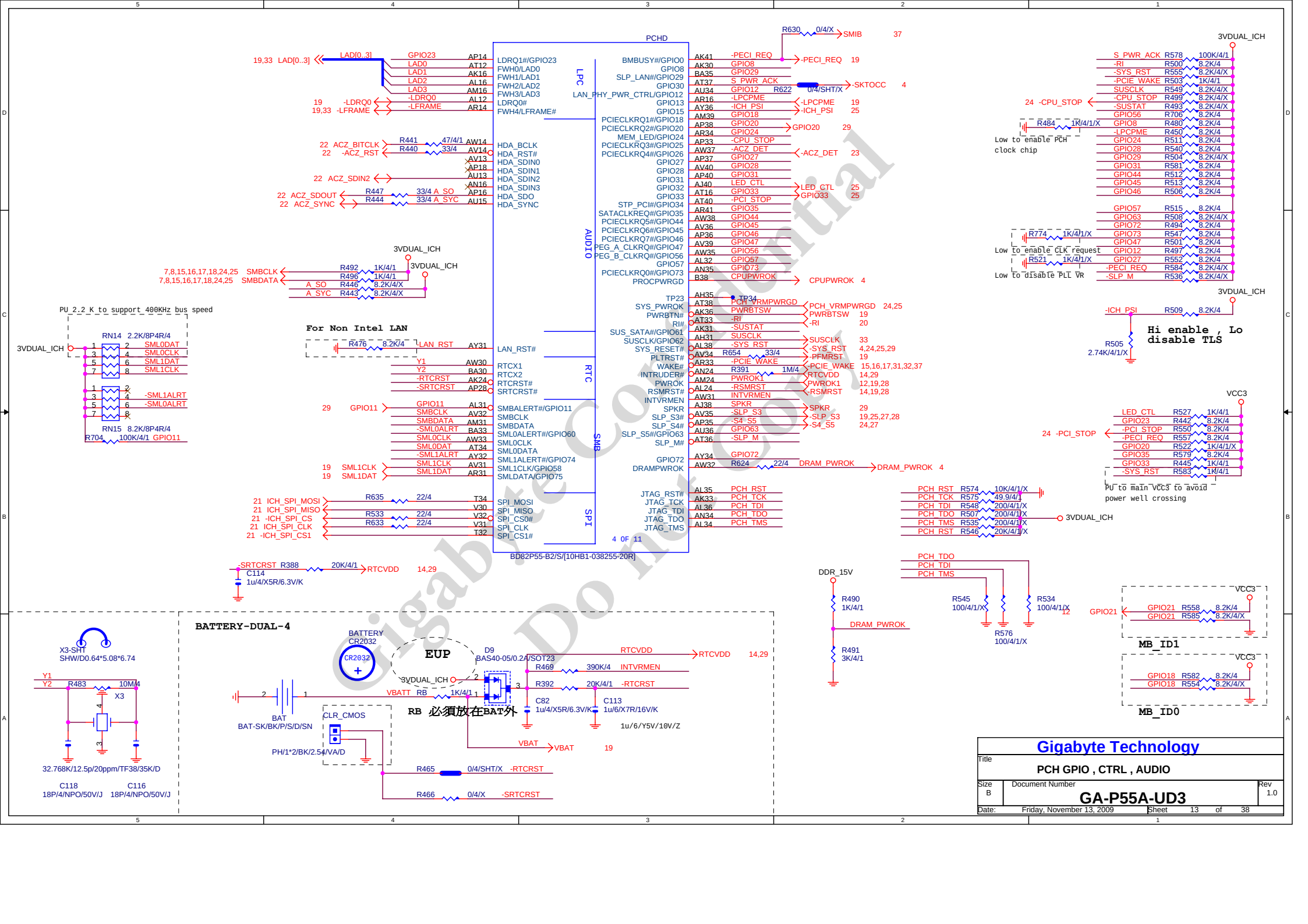
Gigabyte Technology



Gigabyte Technology		
Title: PCH DISPLAY ,CLK BUFFER		
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
Date: Friday, November 13, 2009	Sheet 11 of 38	



Gigabyte Technology			
Title: PCH HOST , SATA, PCI			
Size: B	Document Number: GA-P55A-UD3		Rev: 1.0
Date: Friday, November 13, 2009	Sheet 12 of 38		


PCHD
LPC
AUDIO
RTC
SMB
SPI
BD82P55-B2/S/[10HB1-038255-20R]
4 OF 11
For Non Intel LAN
PU 2.2 K to support 400KHz bus speed
RN14 2.2K/8P4R/4
RN15 8.2K/8P4R/4
BATTERY-DUAL-4
EUP
CR2032
RB 必須放在BAT外
Low to enable PCH clock chip
Low to enable CLK request
Low to disable PLL VR
Hi enable , Lo disable TLS
PU to main VCC3 to avoid power well crossing
MB_ID1
MB_ID0
Gigabyte Technology
PCH GPIO , CTRL , AUDIO
GA-P55A-UD3
Rev 1.0
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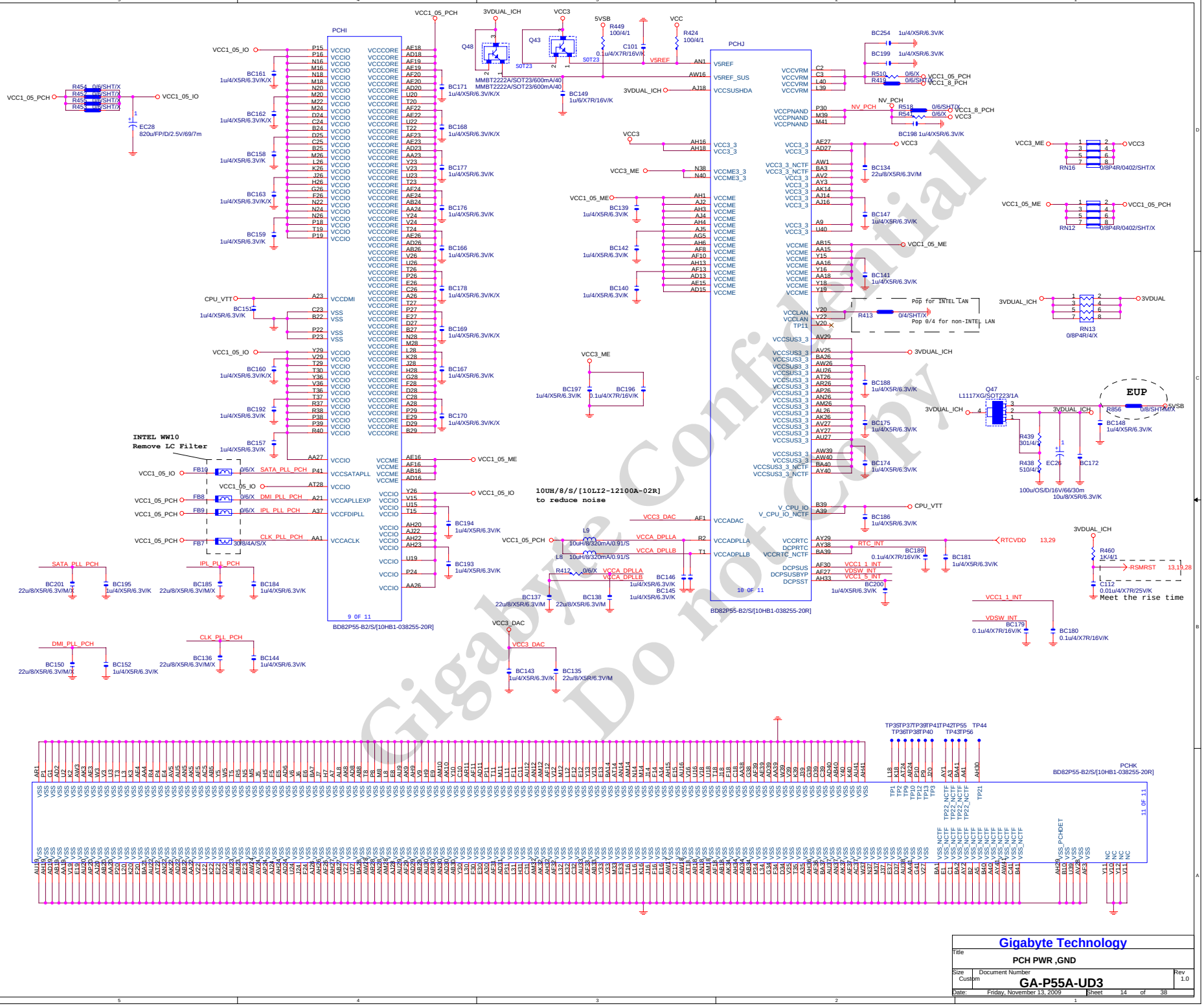
Confidential
Do not Copy


PCHI
PCHJ
PCHK
BD82P55-B2/S/[10HB1-038255-20R]
INTEL WW10
Remove LC Filter
10UH/8/S/[10LI2-12100A-02R]
to reduce noise
EUP
Pop for INTEL LAN
Pop 0/4 for non-INTEL LAN
Meet the rise time
Gigabyte Confidential
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Gigabyte Technology
PCH PWR ,GND
GA-P55A-UD3
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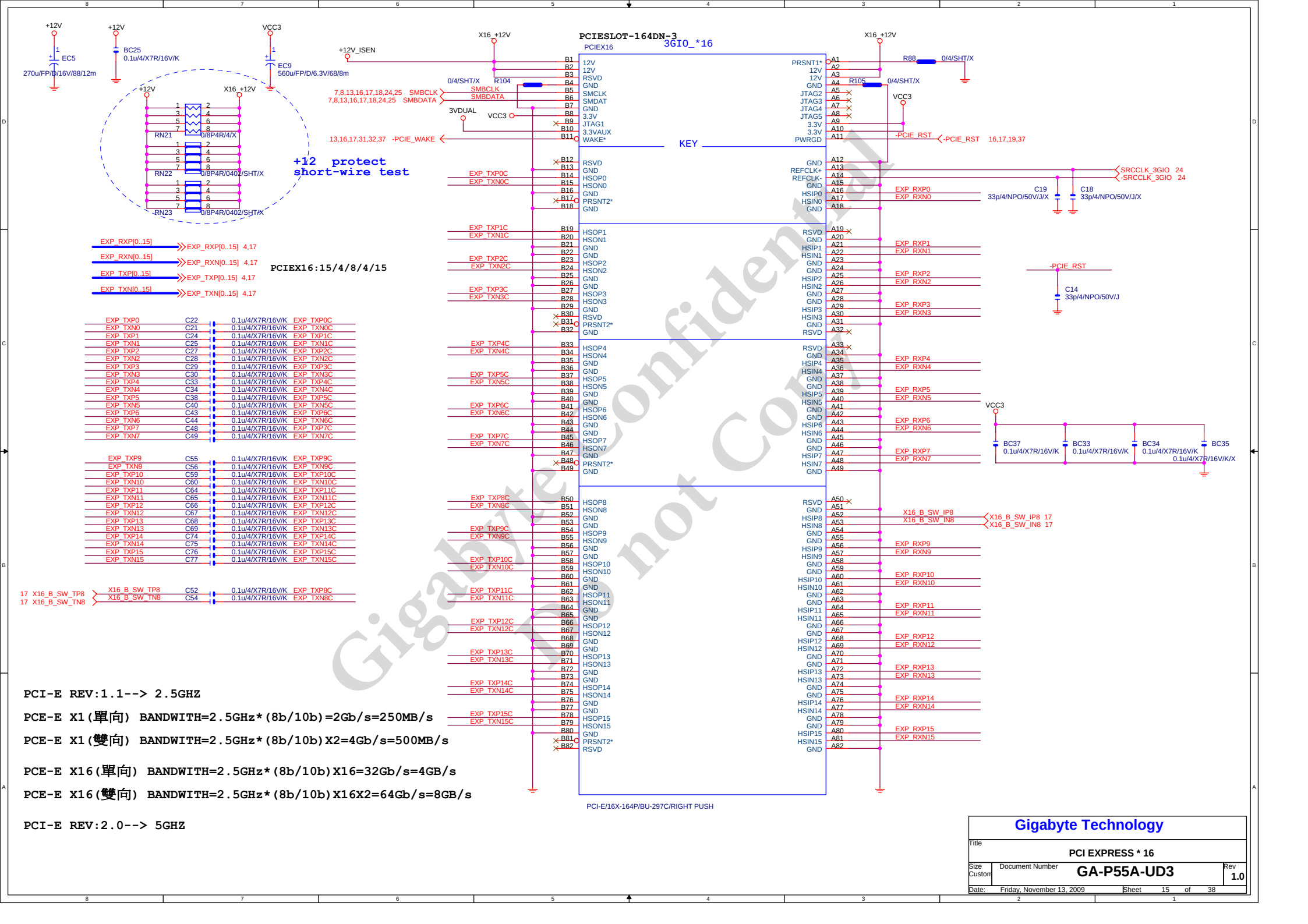
PCIESLOT-164DN-3
PCIEX16
3GIO_*16
KEY
+12 protect
short-wire test
PCIEX16:15/4/8/4/15
PCI-E REV:1.1--> 2.5GHZ
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s
PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s
PCI-E REV:2.0--> 5GHZ
PCI-E/16X-164P/BU-297C/RIGHT PUSH
Gigabyte Technology
PCI EXPRESS * 16
GA-P55A-UD3
1.0
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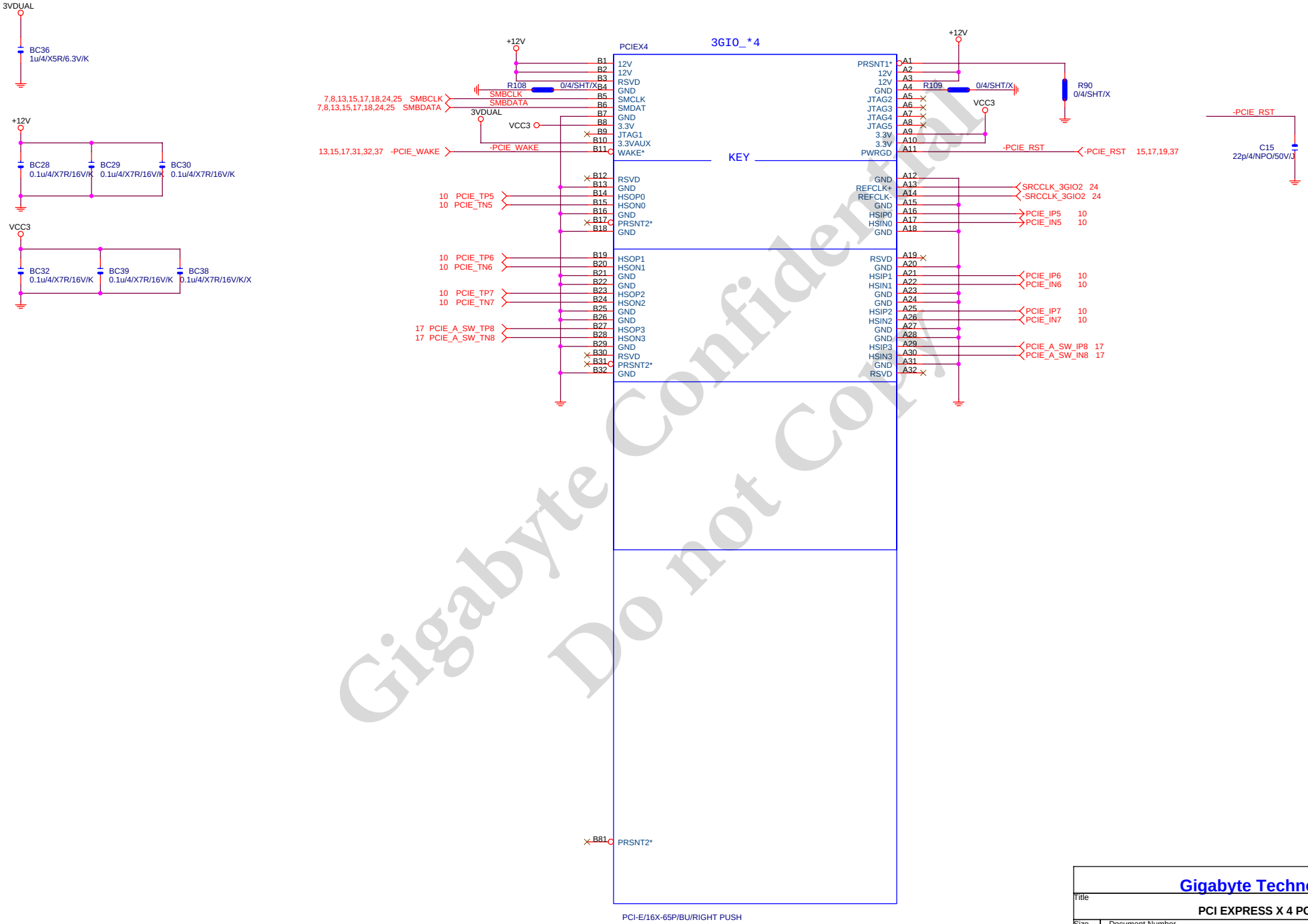

Gigabyte Technology	
Title	PCI EXPRESS X 4 PORT
Size: Custom	Document Number: GA-P55A-UD3
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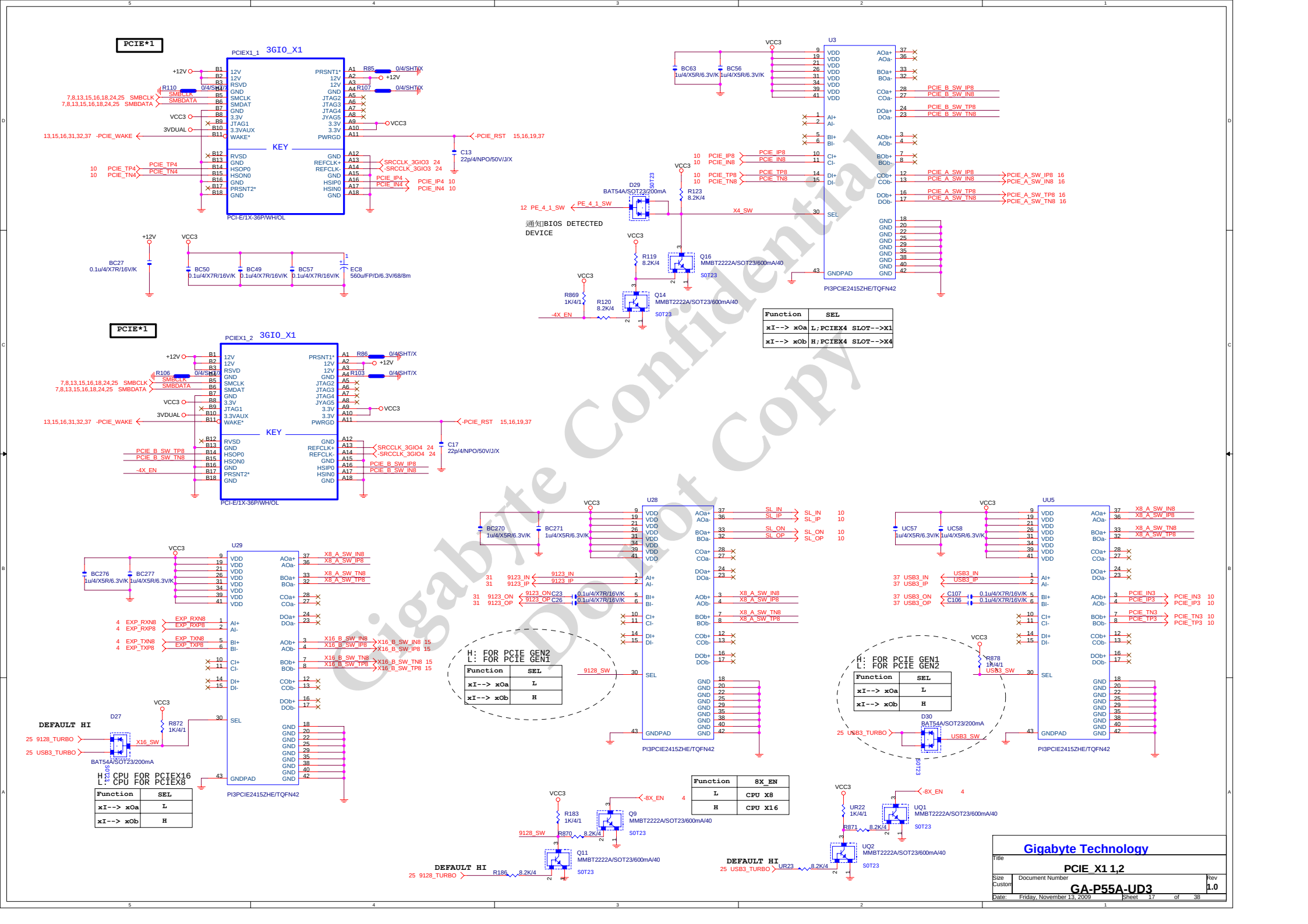

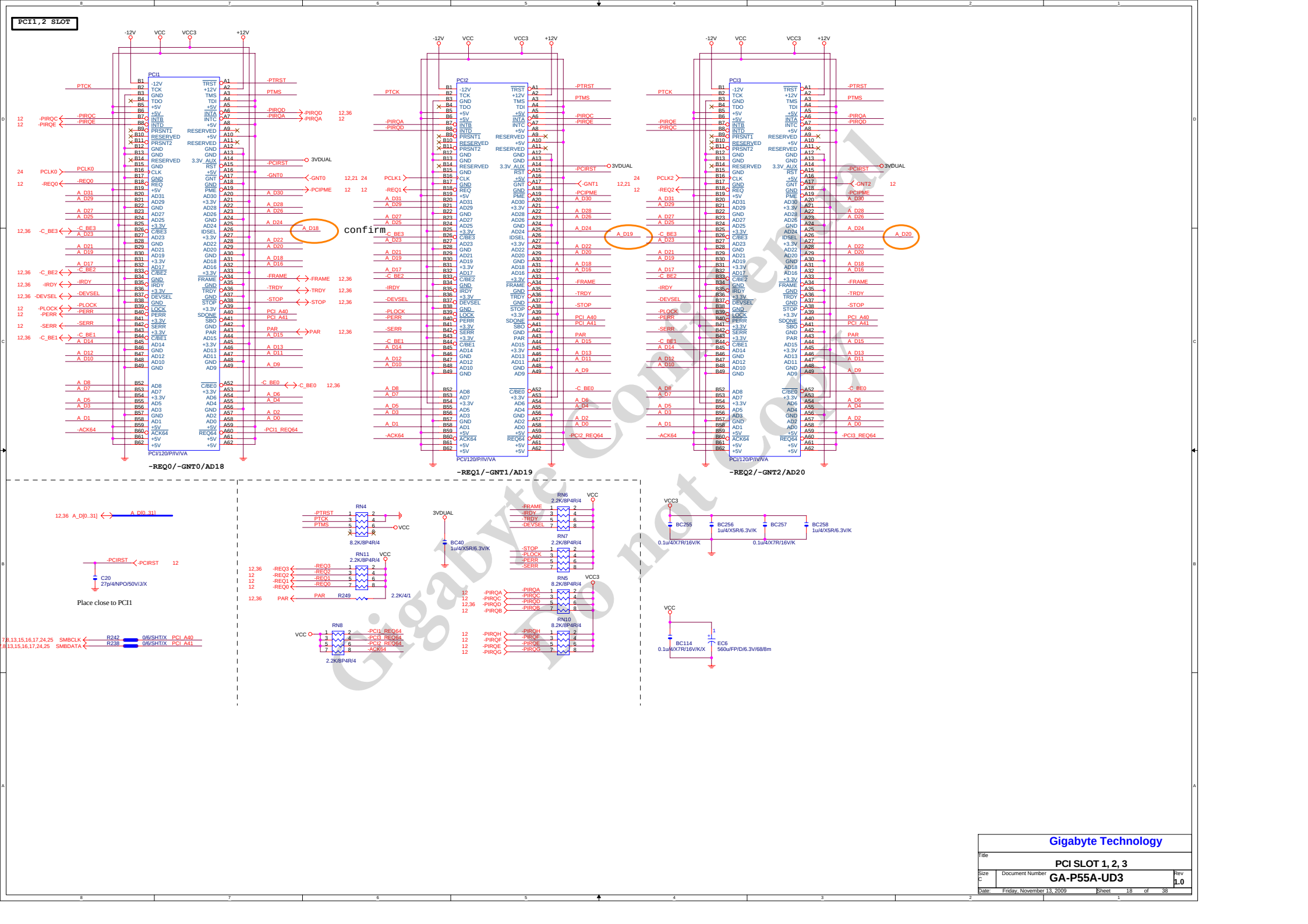
PCI1,2 SLOT
PCI1
PCI2
PCI3
PCI/120/P/IV/VA
-REQ0/-GNT0/AD18
-REQ1/-GNT1/AD19
-REQ2/-GNT2/AD20
confirm
A_D18
A_D19
A_D20
Place close to PCI1
C20
27p/4/NPO/50V/J/X
RN4
RN5
RN6
RN7
RN8
RN10
RN11
R242
R238
R249
BC40
1u/4/X5R/6.3V/K
BC114
BC255
BC256
BC257
BC258
EC6
560u/FP/D/6.3V/68/8m
Gigabyte Technology
PCI SLOT 1, 2, 3
GA-P55A-UD3
1.0
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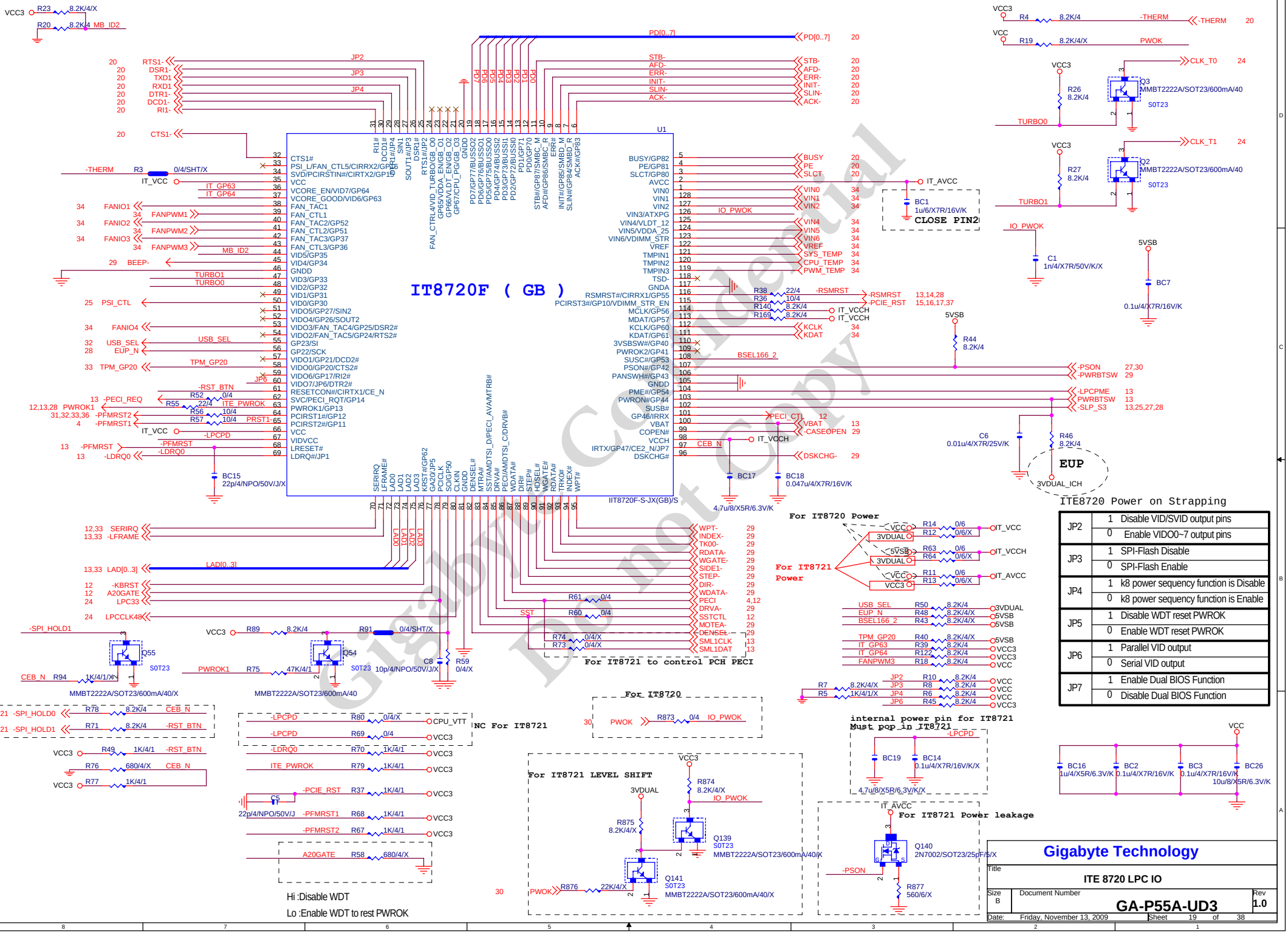
IT8720F (GB)
U1
IIT8720F-S-JX(GB)/S
ITE8720 Power on Strapping
JP2
1 Disable VID/SVID output pins
0 Enable VIDO0~7 output pins
JP3
1 SPI-Flash Disable
0 SPI-Flash Enable
JP4
1 k8 power sequency function is Disable
0 k8 power sequency function is Enable
JP5
1 Disable WDT reset PWROK
0 Enable WDT reset PWROK
JP6
1 Parallel VID output
0 Serial VID output
JP7
1 Enable Dual BIOS Function
0 Disable Dual BIOS Function
For IT8720 Power
For IT8721 Power
For IT8721 to control PCH PECI
For IT8720
NC For IT8721
For IT8721 LEVEL SHIFT
For IT8721 Power leakage
internal power pin for IT8721 Must pop in IT8721
EUP
Hi :Disable WDT
Lo :Enable WDT to rest PWROK
Gigabyte Technology
ITE 8720 LPC IO
GA-P55A-UD3
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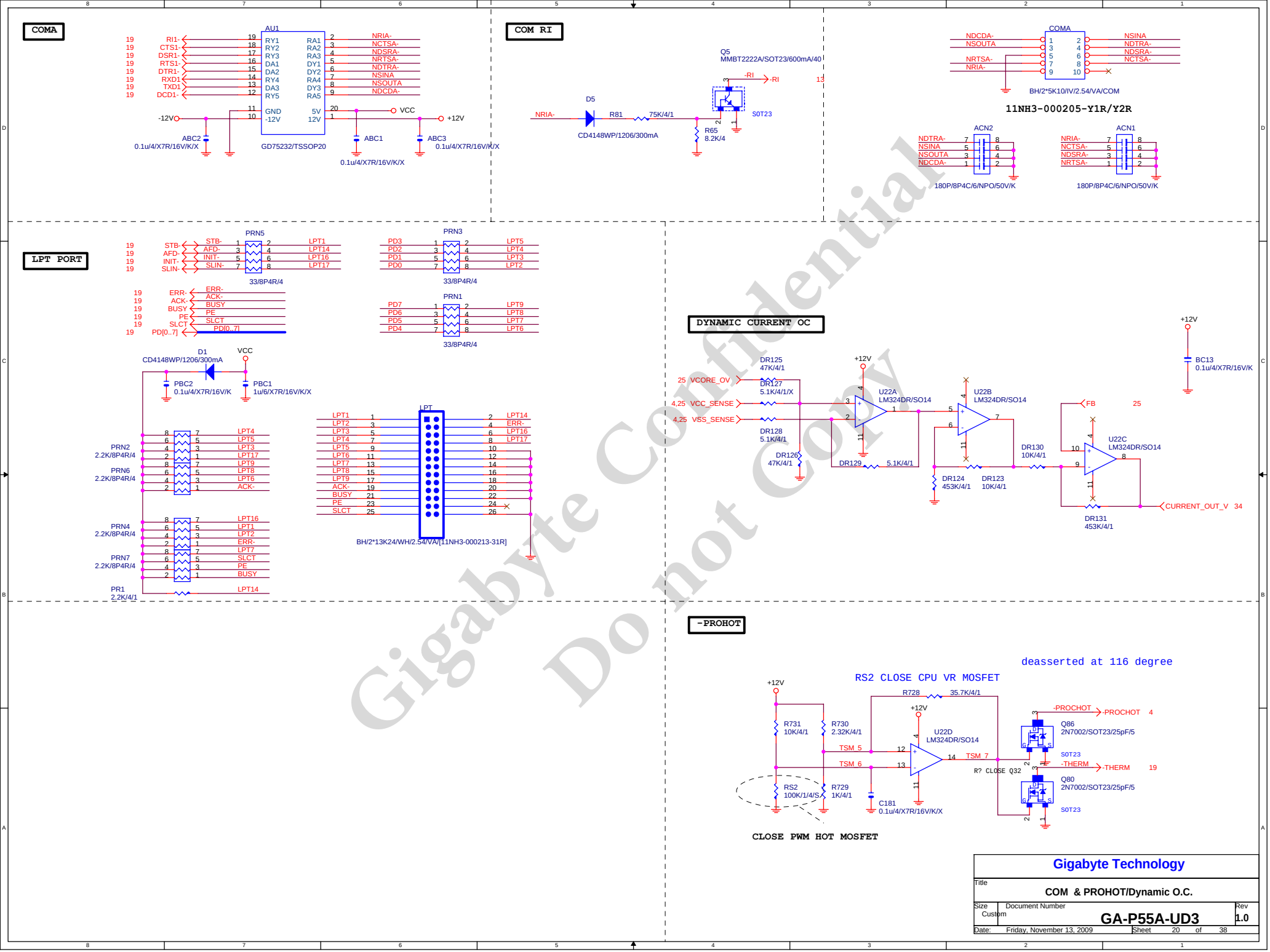

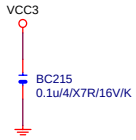

r1.0 DG;0.7 CRB

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

IC8SO-SOCKET

Gigabyte Technology

Title: BIOS

Size: Custom | Document Number: GA-P55A-UD3 | Rev: 1.0

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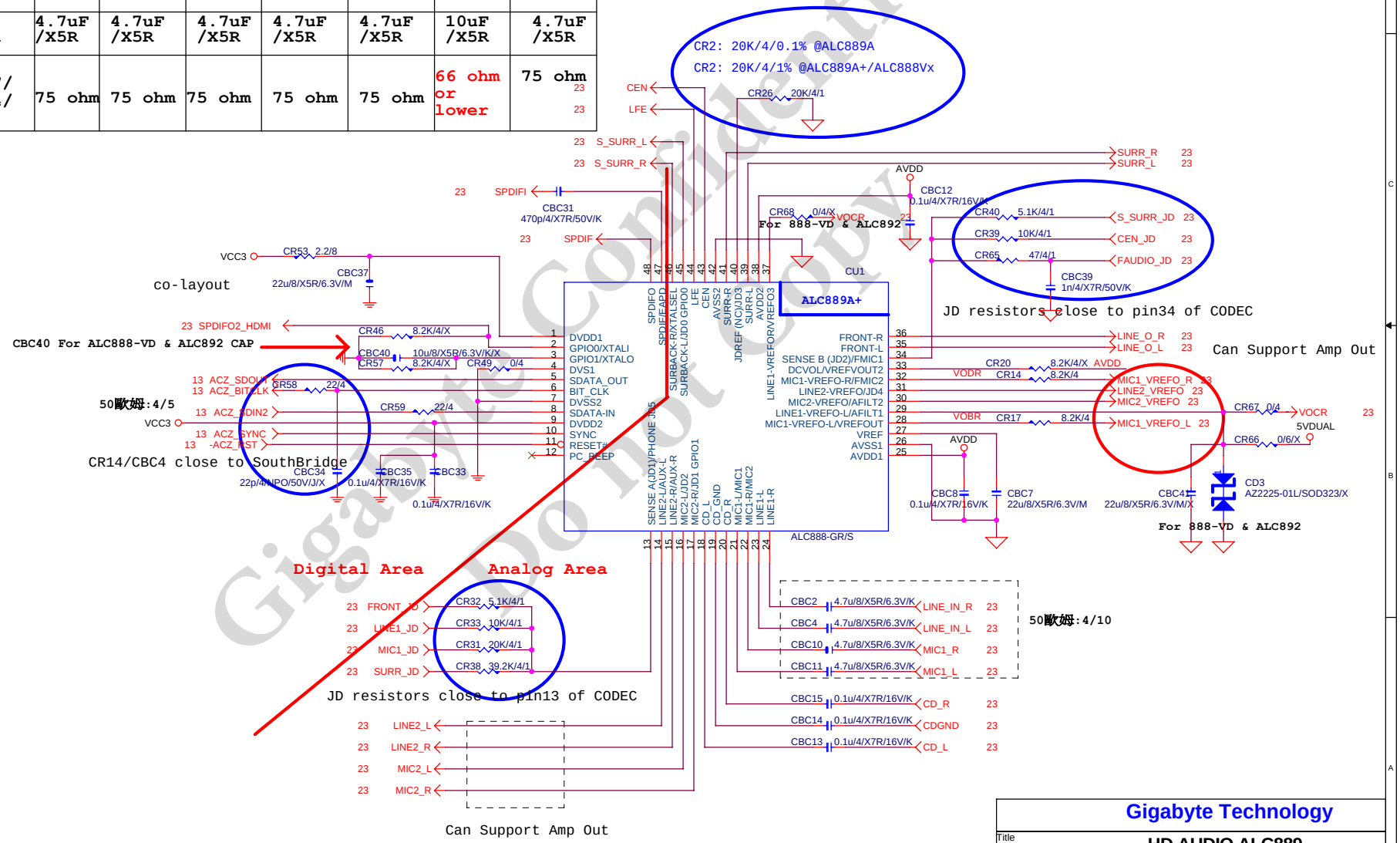
AZALIA CODEC *ALC889A+/ALC889A/ALC888Vx Colay*

	ALC883	ALC888-VA	ALC888B	ALC888-VD	ALC892	ALC889	ALC889A
CR46	X	X	X	X	X	X	O
CR57	X	X	X	X	X	X	O
CR49	O	O	X	X	X	O	O
CBC40	X	X	X	10uF/X5R	10uF/X5R	X	X
CR20	O	X	X	X	X	X	X
CR26	20K/1%	20K/1%	20K/1%	20K/1%	20K/1%	20K/1%	20K/0.1%
CR47	X	X	X	X	O	O	X
CR48	O	O	O	O	X	X	O
CBC2/CBC4/CBC5/ CBC6/CBC10/CBC11	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR1/CR3/CR10/CR12/ CR15/CR19/CR56/CR27/ CR55/CR37/CR28/CR34/ CR6/CR9/CR51/CR61	75 ohm	75 ohm	75 ohm	75 ohm	75 ohm	66 ohm or lower	75 ohm



Gigabyte Technology		
Title	HD AUDIO ALC889	
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
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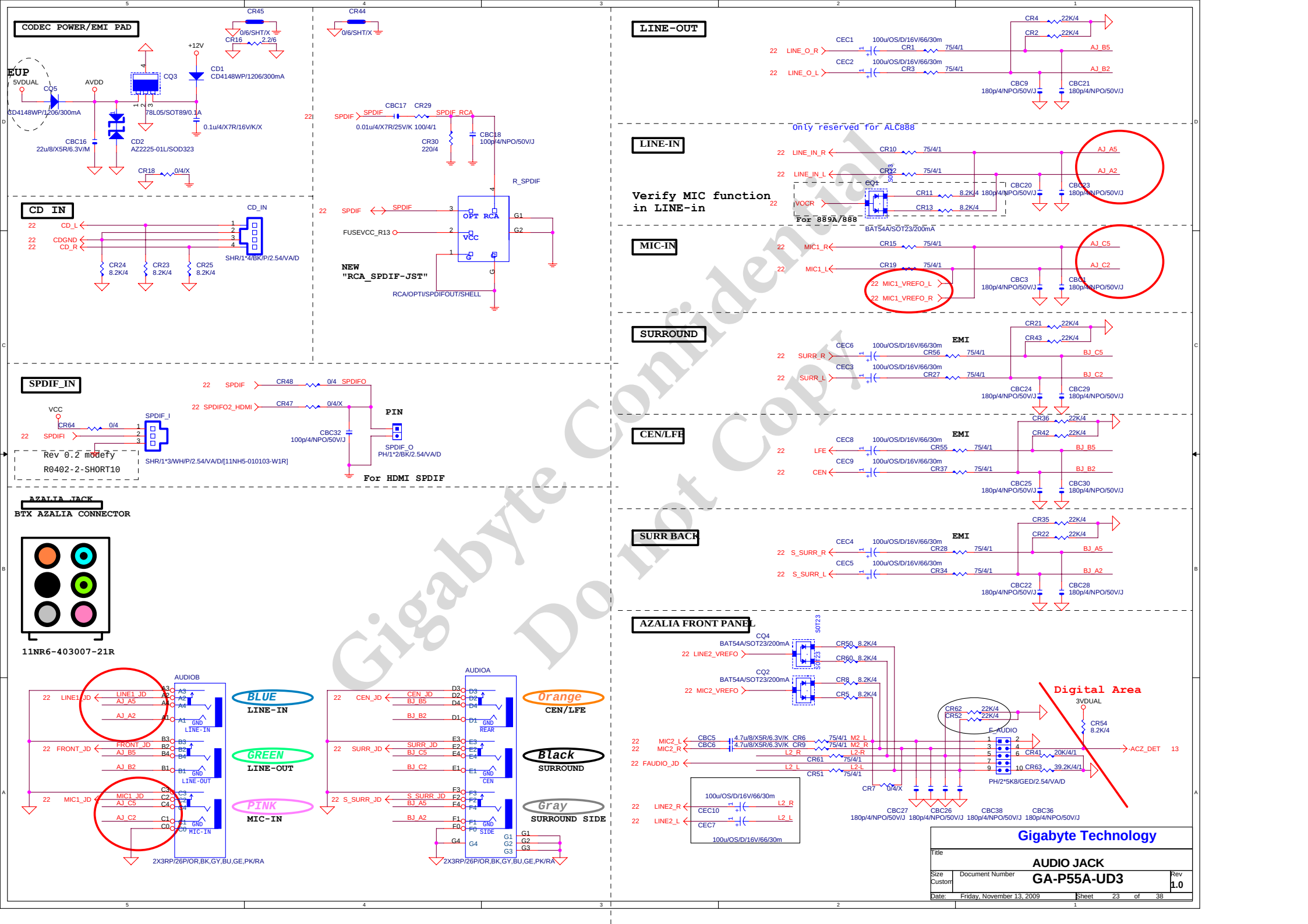
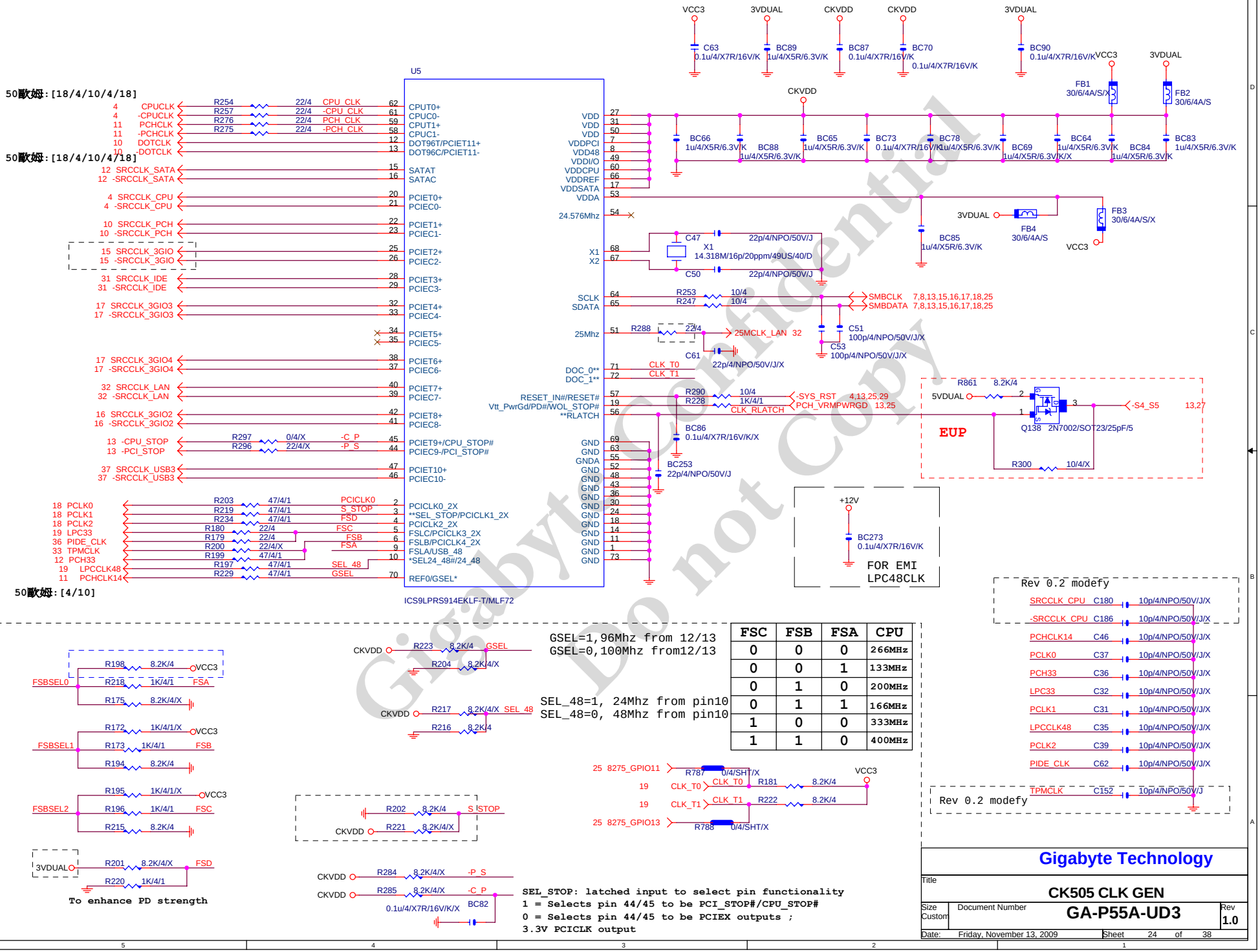


CLK GEN CK505



FSC	FSB	FSA	CPU
0	0	0	266MHz
0	0	1	133MHz
0	1	0	200MHz
0	1	1	166MHz
1	0	0	333MHz
1	1	0	400MHz

GSEL=1,96Mhz from 12/13
GSEL=0,100Mhz from12/13

SEL_48=1, 24Mhz from pin10
SEL_48=0, 48Mhz from pin10

Gigabyte Technology

Title	CK505 CLK GEN	
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
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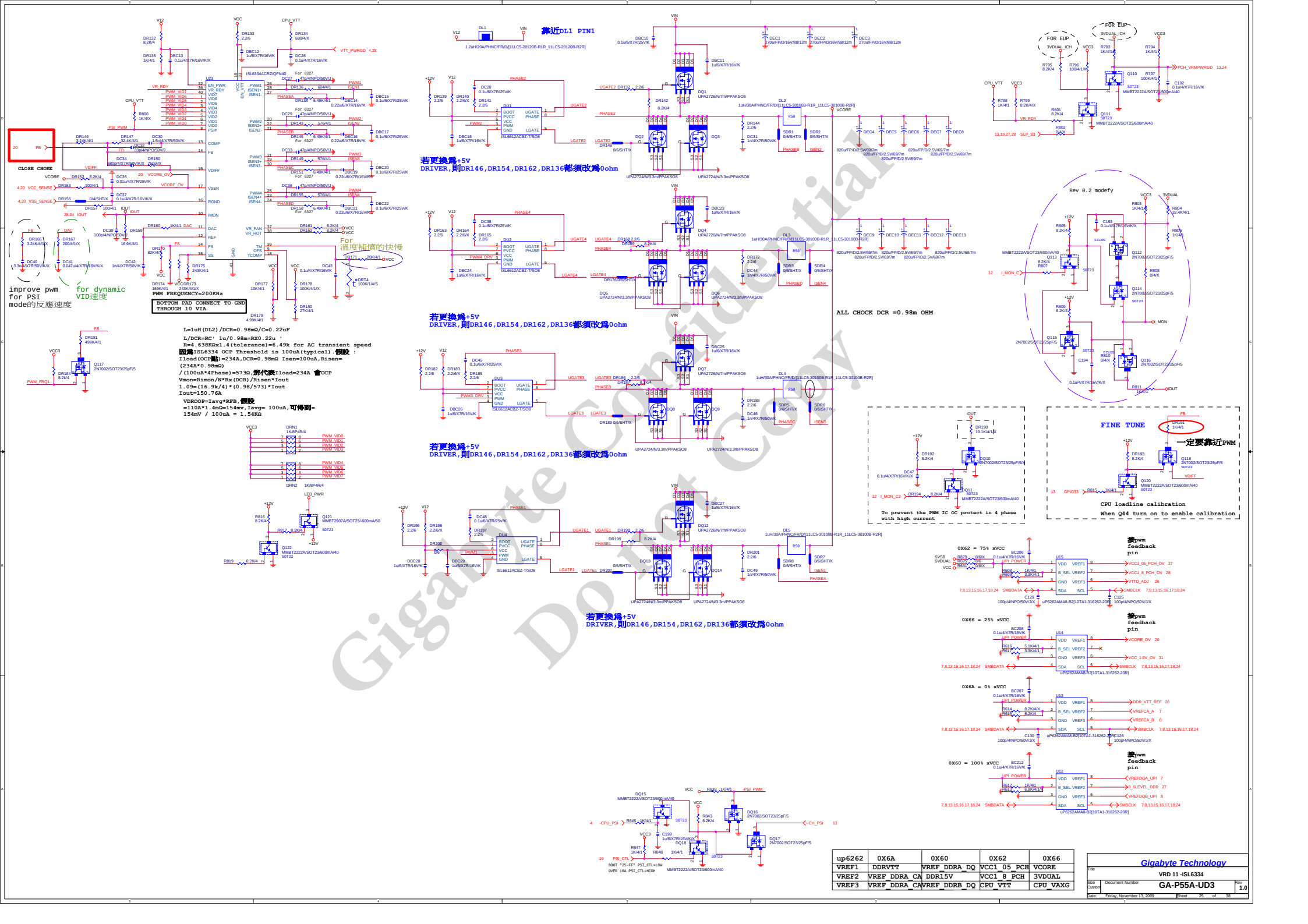

up6262	0X6A	0X60	0X62	0X66
VREF1	DDRVTT	VREF_DDRA_DQ	VCC1_05_PCH	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	3VDUAL
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	CPU_VTT	CPU_VAXG

Gigabyte Technology

Title: VRD 11 -ISL6334

Size: Custom | Document Number: GA-P55A-UD3 | Rev: 1.0

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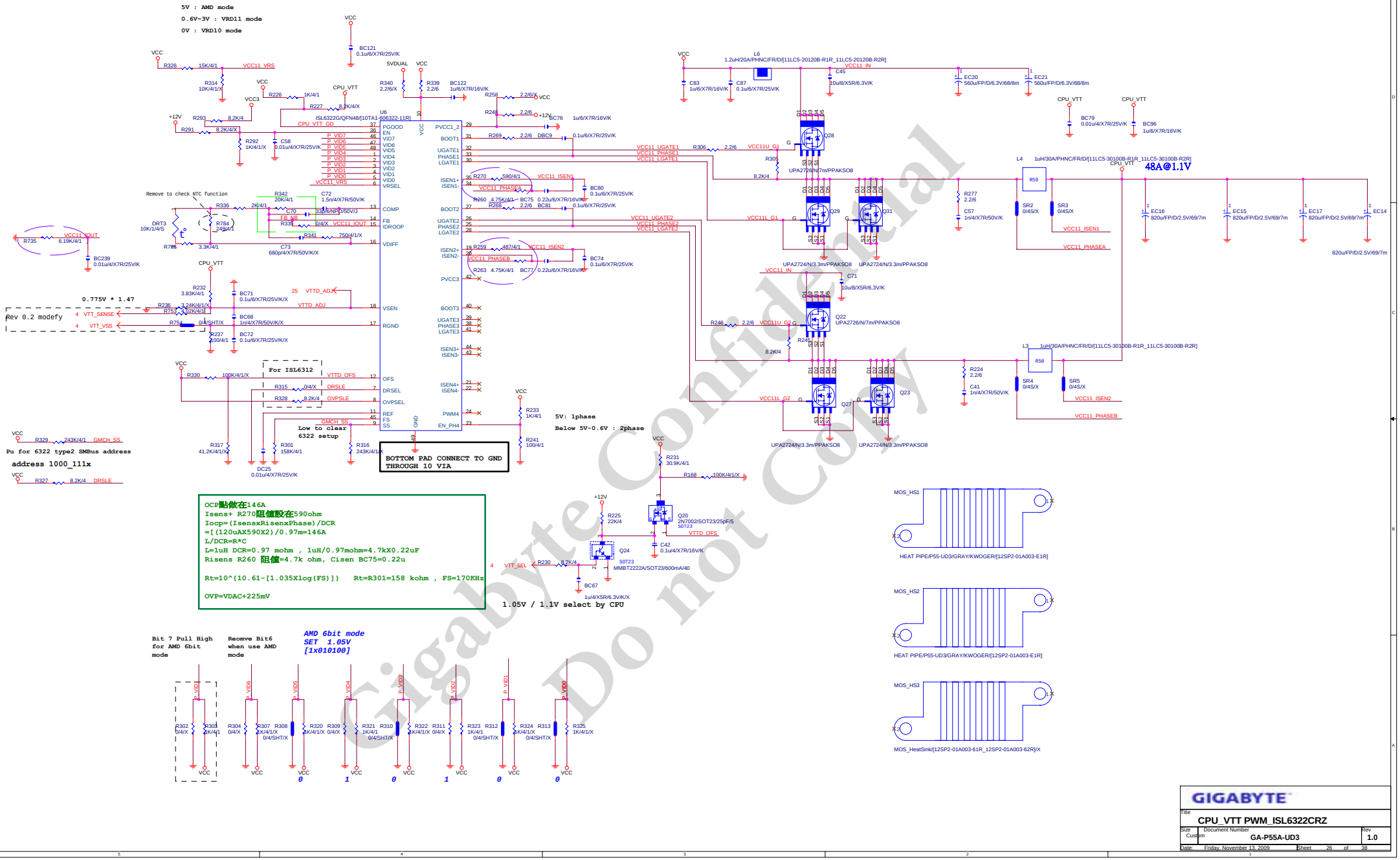

Title	CPU_VTT PWM_ISL6322CRZ
Size	Custom
Document Number	GA-P55A-UD3
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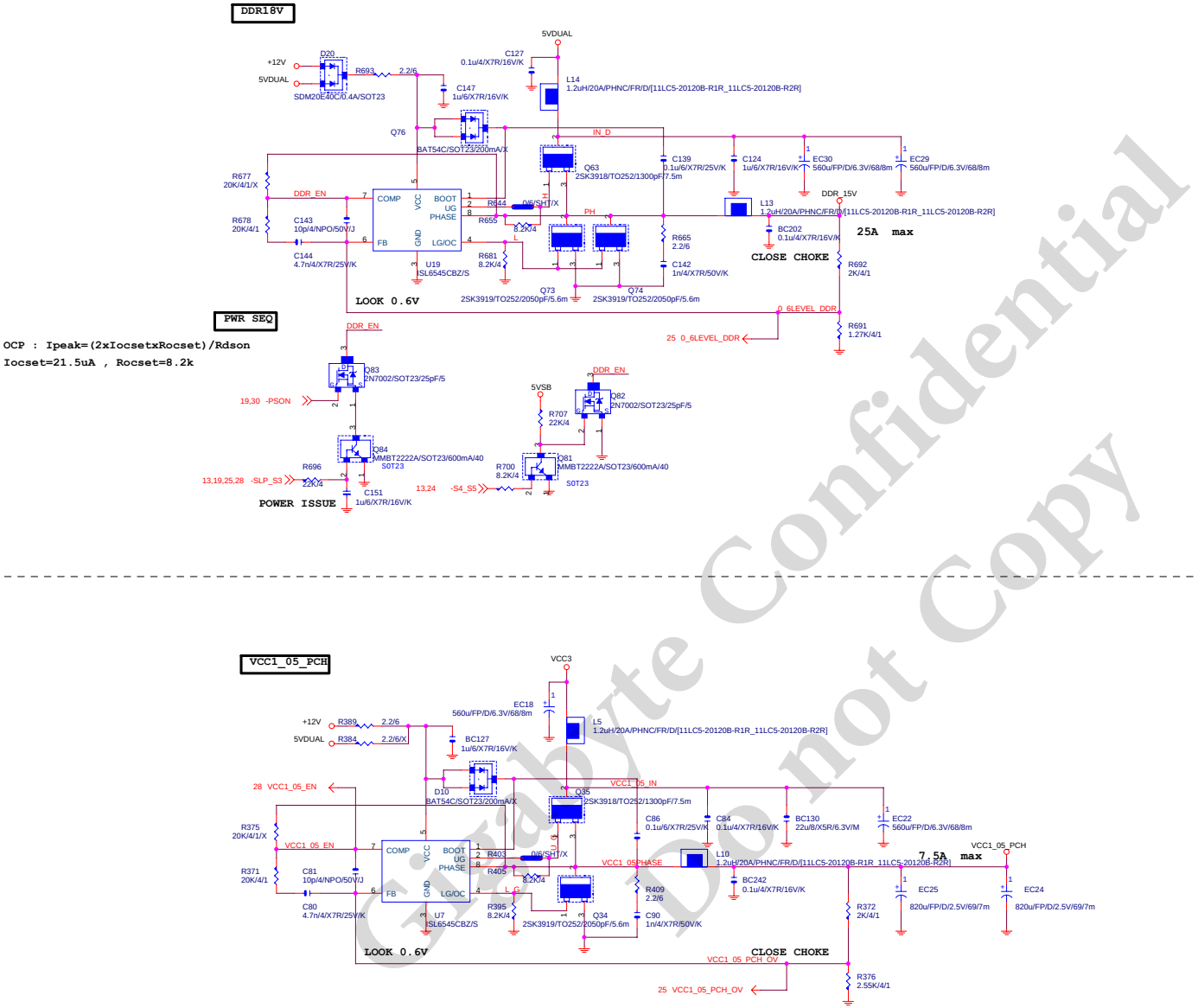

Gigabyte Technology		
Title: DDR_15V		
Size: C	Document Number: GA-P55A-UD3	Rev: 1.0
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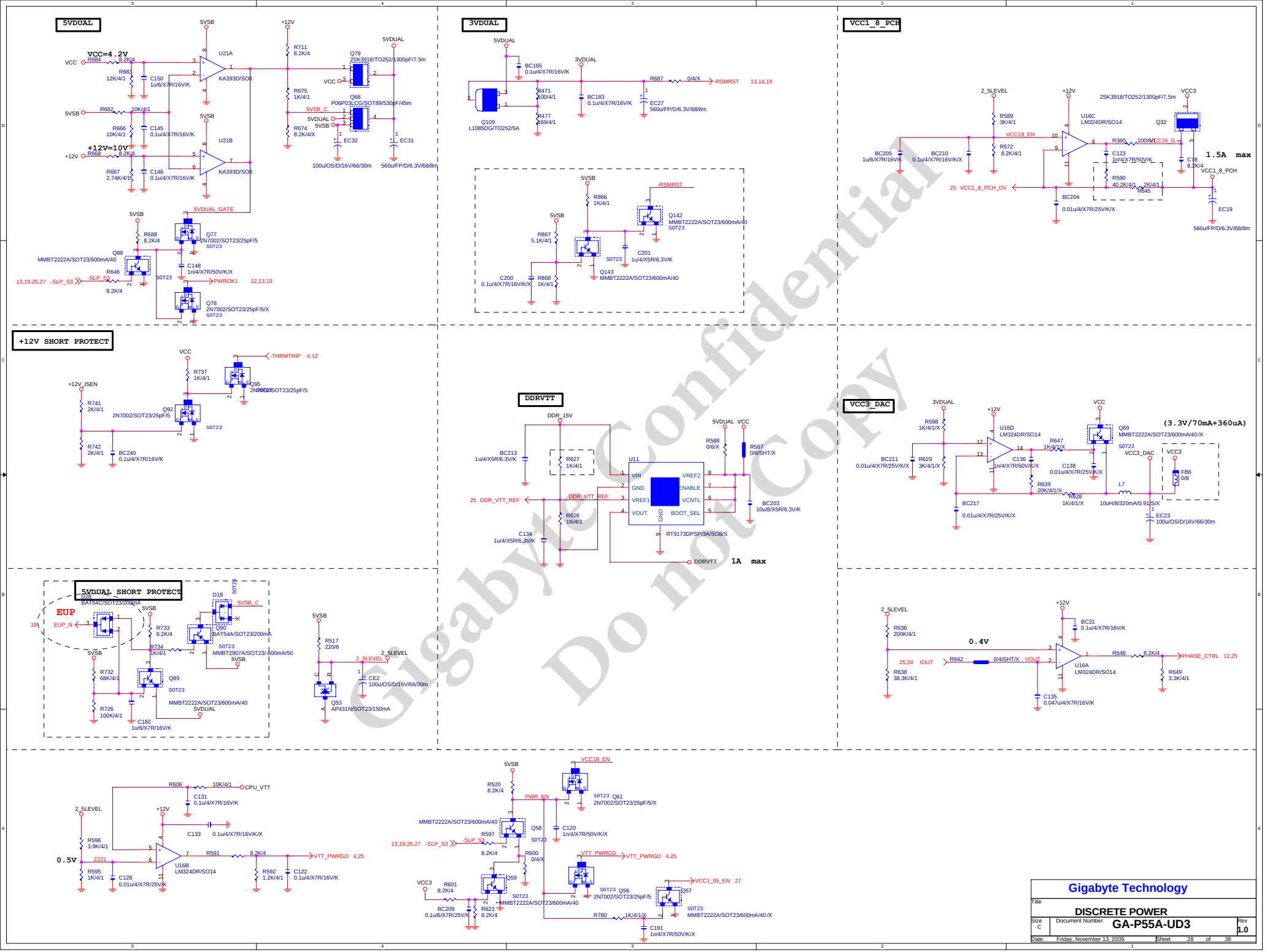

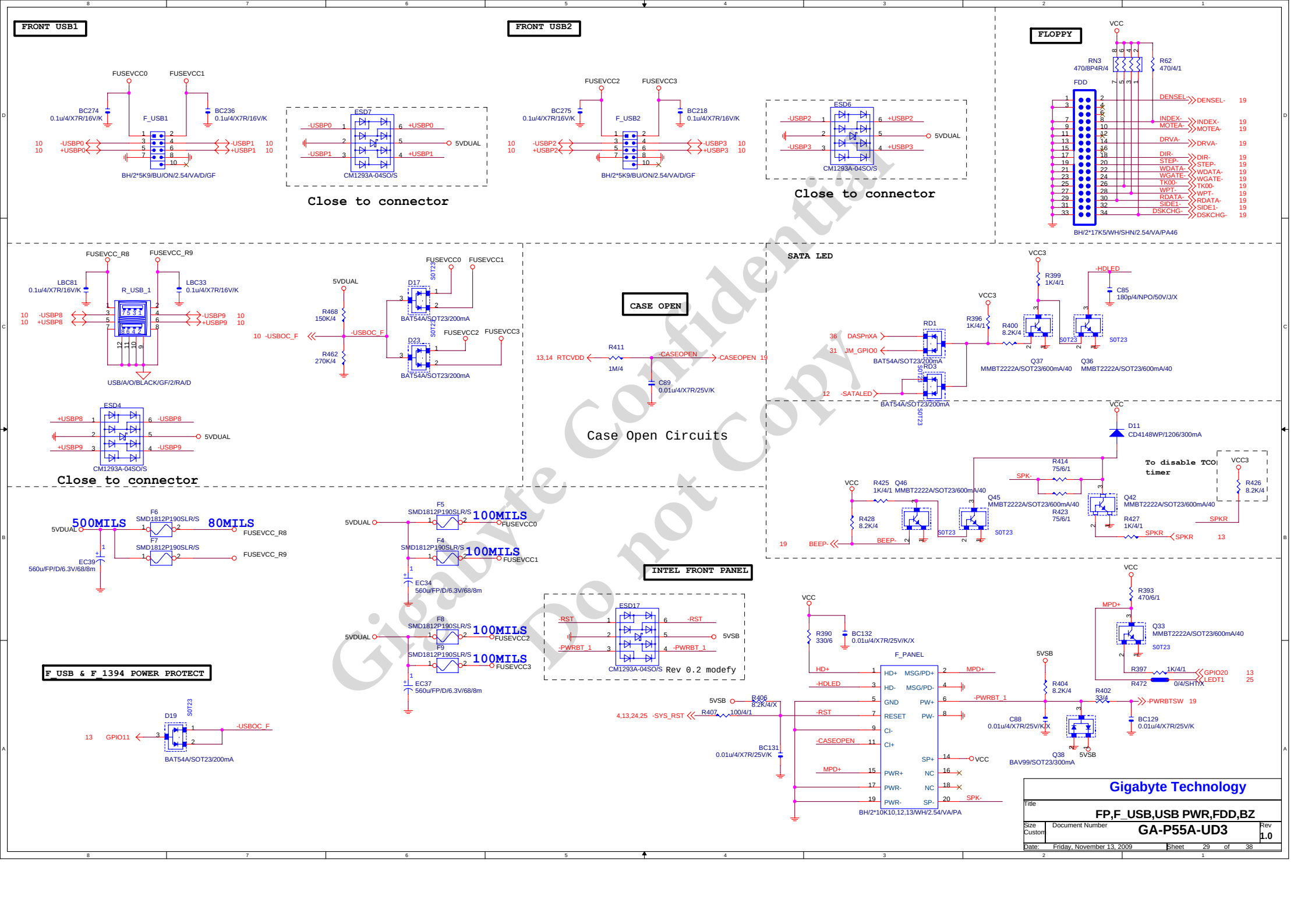
FRONT USB1
FUSEVCC0
FUSEVCC1
BC274
0.1u/4/X7R/16V/K
F_USB1
BC236
0.1u/4/X7R/16V/K
-USBP0
+USBP0
-USBP1
+USBP1
BH/2*5K9/BU/ON/2.54/VA/D/GF
ESD7
5VDUAL
CM1293A-04SO/S
Close to connector
FRONT USB2
FUSEVCC2
FUSEVCC3
BC275
0.1u/4/X7R/16V/K
F_USB2
BC218
0.1u/4/X7R/16V/K
-USBP2
+USBP2
-USBP3
+USBP3
BH/2*5K9/BU/ON/2.54/VA/D/GF
ESD6
5VDUAL
CM1293A-04SO/S
Close to connector
FLOPPY
VCC
RN3
470/8P4R/4
R62
470/4/1
FDD
DENSEL-
INDEX-
MOTEA-
DRVA-
DIR-
STEP-
WDATA-
WGATE-
TK00-
WPT-
RDATA-
SIDE1-
DSKCHG-
BH/2*17K5/WH/SHN/2.54/VA/PA46
FUSEVCC_R8
FUSEVCC_R9
LBC81
0.1u/4/X7R/16V/K
R_USB_1
LBC33
0.1u/4/X7R/16V/K
-USBP8
+USBP8
-USBP9
+USBP9
USB/A/O/BLACK/GF/2/RA/D
ESD4
5VDUAL
CM1293A-04SO/S
Close to connector
5VDUAL
R468
150K/4
-USBOC_F
R462
270K/4
FUSEVCC0
FUSEVCC1
D17
BAT54A/SOT23/200mA
FUSEVCC2
FUSEVCC3
D23
BAT54A/SOT23/200mA
CASE OPEN
R411
1M/4
-CASEOPEN
C89
0.01u/4/X7R/25V/K
Case Open Circuits
SATA LED
VCC3
R399
1K/4/1
-HDLED
C85
180p/4/NPO/50V/J/X
RD1
RD3
BAT54A/SOT23/200mA
R396
1K/4/1
R400
8.2K/4
Q37
MMBT2222A/SOT23/600mA/40
Q36
MMBT2222A/SOT23/600mA/40
DASPnXA
JM_GPIO0
-SATALED
D11
CD4148WP/1206/300mA
To disable TCO timer
R414
75/6/1
R425
1K/4/1
Q46
MMBT2222A/SOT23/600mA/40
R428
8.2K/4
Q45
MMBT2222A/SOT23/600mA/40
R423
75/6/1
Q42
MMBT2222A/SOT23/600mA/40
R427
1K/4/1
R426
8.2K/4
SPK-
SPKR
BEEP-
500MILS
80MILS
F6
F7
SMD1812P190SLR/S
EC39
560u/FP/D/6.3V/68/8m
F5
F4
F8
F9
100MILS
EC34
EC37
INTEL FRONT PANEL
ESD17
-RST
-PWRBT_1
CM1293A-04SO/S Rev 0.2 modefy
F_PANEL
R390
330/6
BC132
0.01u/4/X7R/25V/K/X
HD+
-HDLED
-RST
-CASEOPEN
MPD+
BC131
0.01u/4/X7R/25V/K
R406
8.2K/4/X
R407
100/4/1
4,13,24,25 -SYS_RST
R393
470/6/1
Q33
MMBT2222A/SOT23/600mA/40
R397
1K/4/1
R472
0/4/SHT/X
GPIO20
LEDT1
R404
8.2K/4
R402
33/4
C88
0.01u/4/X7R/25V/K/X
Q38
BAV99/SOT23/300mA
BC129
0.01u/4/X7R/25V/K
-PWRBTSW
F_USB & F_1394 POWER PROTECT
D19
BAT54A/SOT23/200mA
GPIO11
-USBOC_F
Gigabyte Technology
FP,F_USB,USB PWR,FDD,BZ
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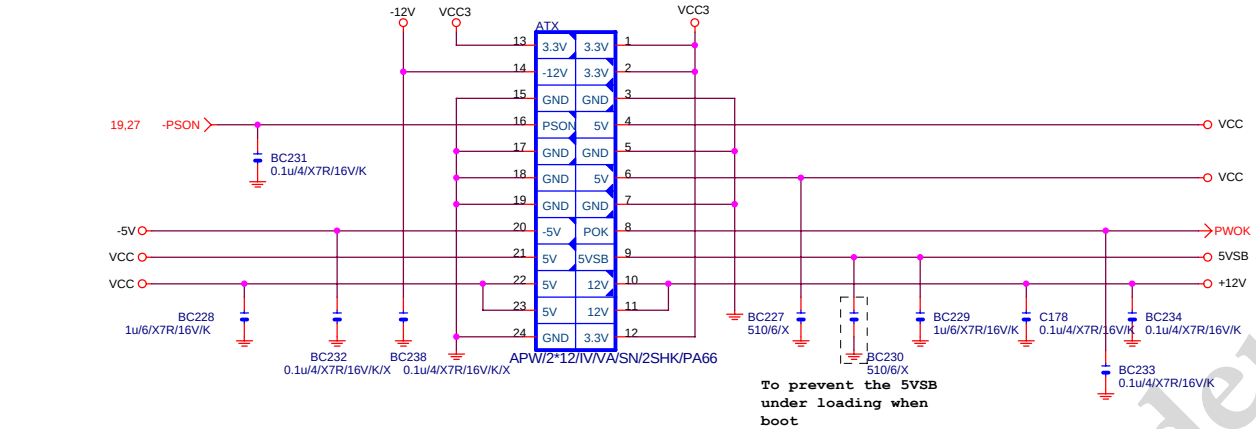
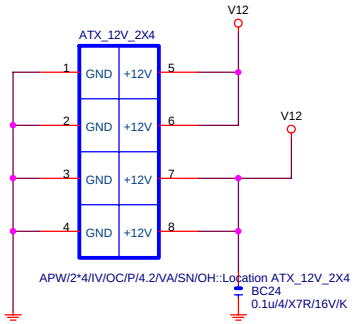
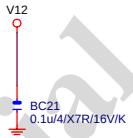
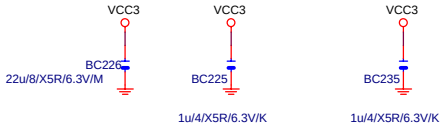
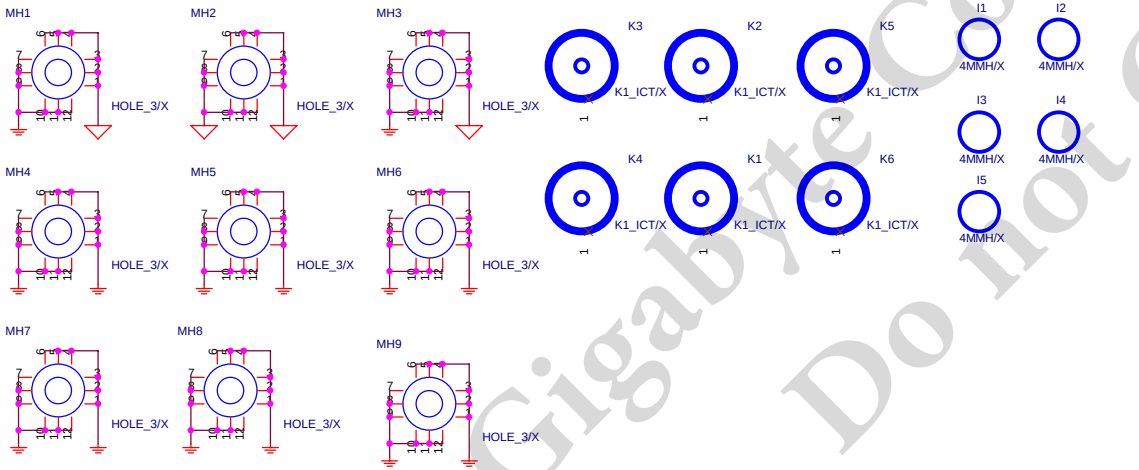
ATX POWER CONNECTOR



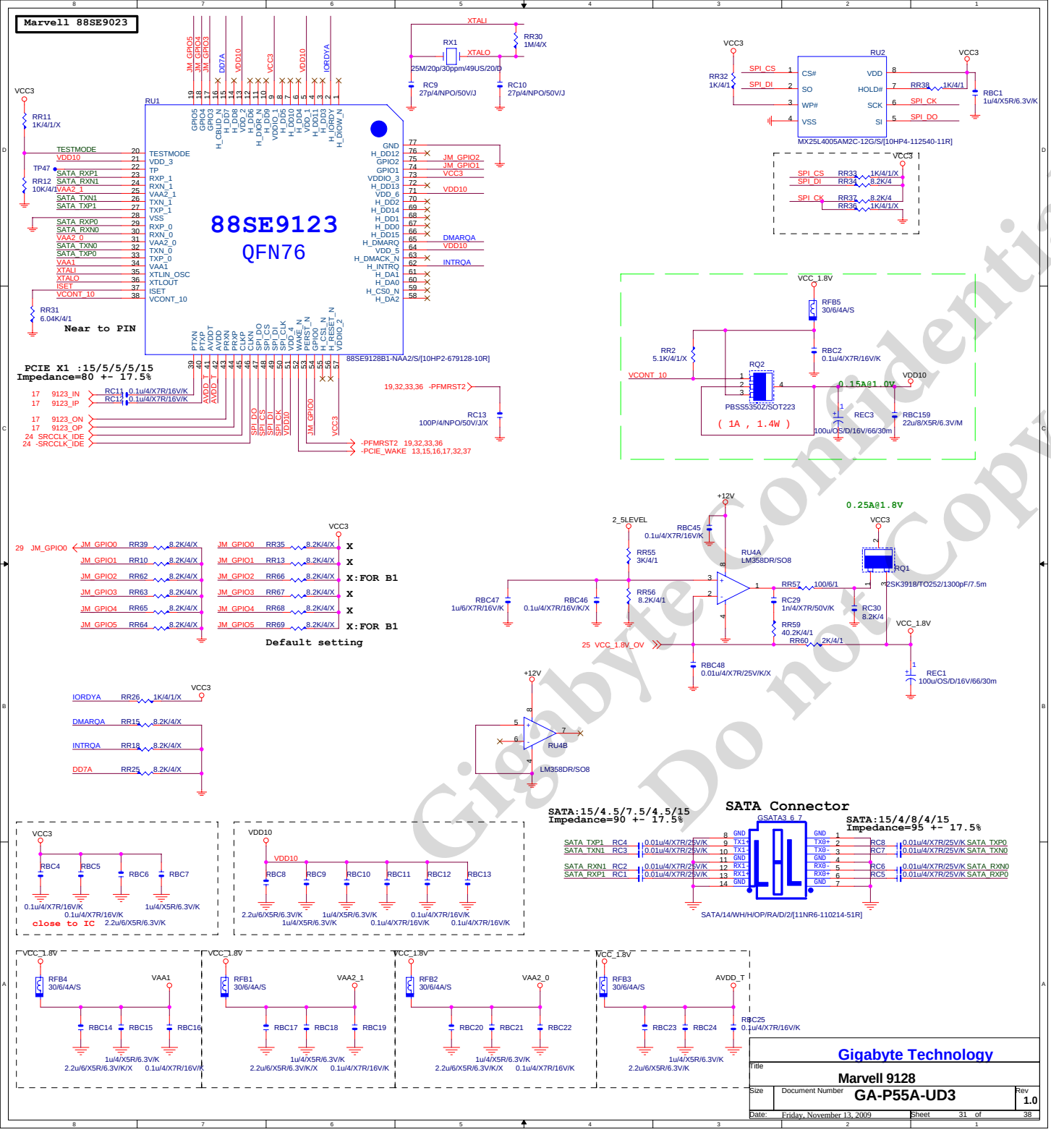








Gigabyte Technology		
Title: ATX POWER CONNECTOR		
Size: B	Document Number: GA-P55A-UD3	Rev: 1.0
Date: Friday, November 13, 2009	Sheet 30 of 38	



PCIE-1G LAN

Power domain chart

For RT8111C/D

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
VDD15	1.5V	1.2V

for RT8111B N/C
for RT8111C 0 ohm (Internal Regulator)
for RT8111C N/C (external Regulator)

LU4
RTL8111D-VB-GR/S/[10HP2-408111-70R]

80歐姆:[15/5/5/5/15]

SRCCLK 50歐姆:[18/4/10/4/18]

離 PIN63 0.5cm以內

LR27離IC越近越好

離IC近越好

For RTL8111C

Dual Color LED

Single Color LED

P35-152-19W9

FOR CLOSE PIN1,29,37,40

距離pin1 在0.5cm以內

距離LL2 在0.5cm以內

放靠近後窗

放靠近後窗

USB30_LAN CONNECTOR

USB30_LAN
R-A USB+LAN/W TF/1G/USB3.0 UDE/[11NR6-702009-K1R]

Close to USB30_LAN

Close to USB30_LAN

400MILS

240MILS

SEL	OE	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

NEC

PCH

Gigabyte Technology

Title	REALTEK RTL8111D	
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.0
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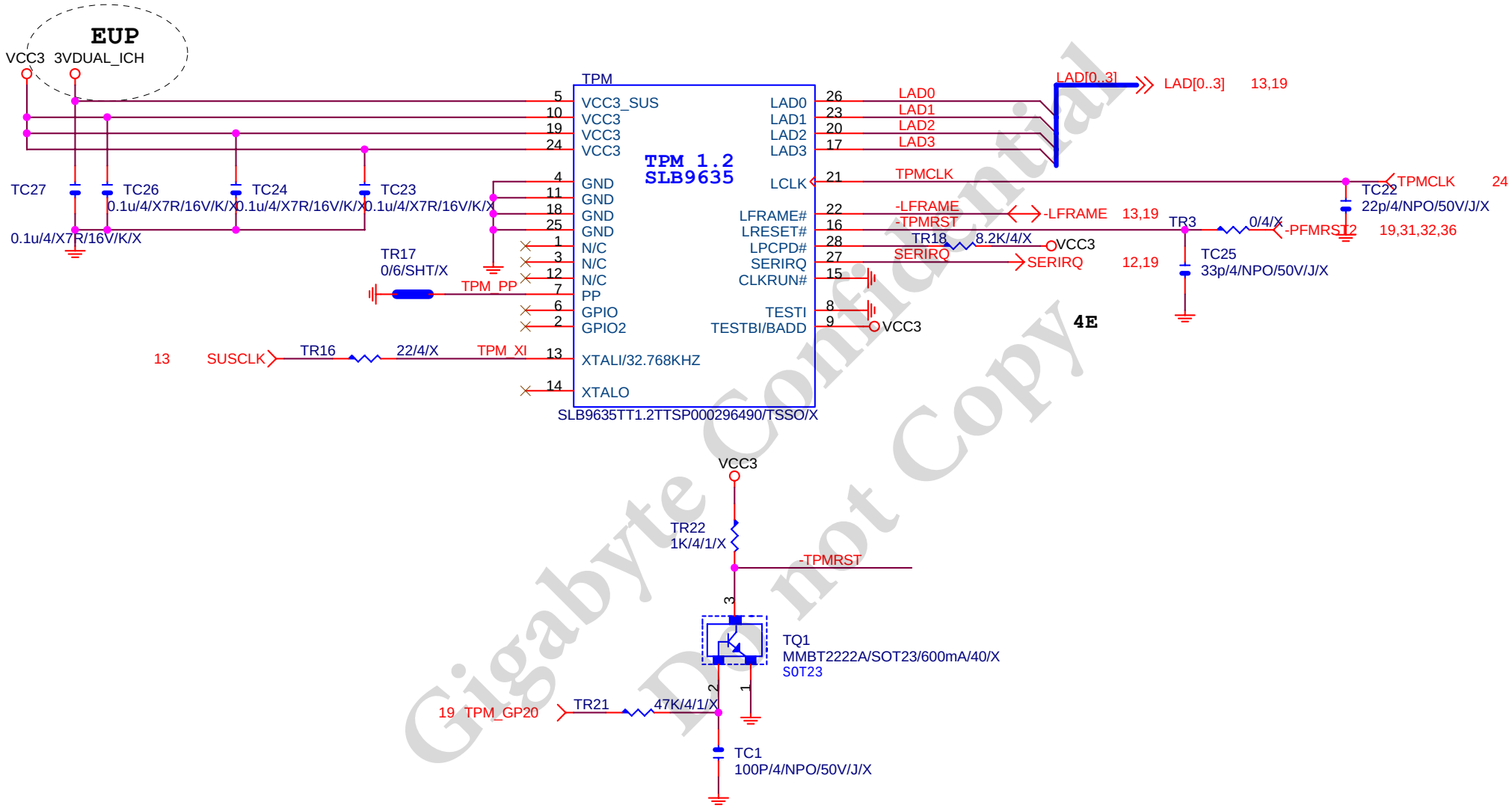
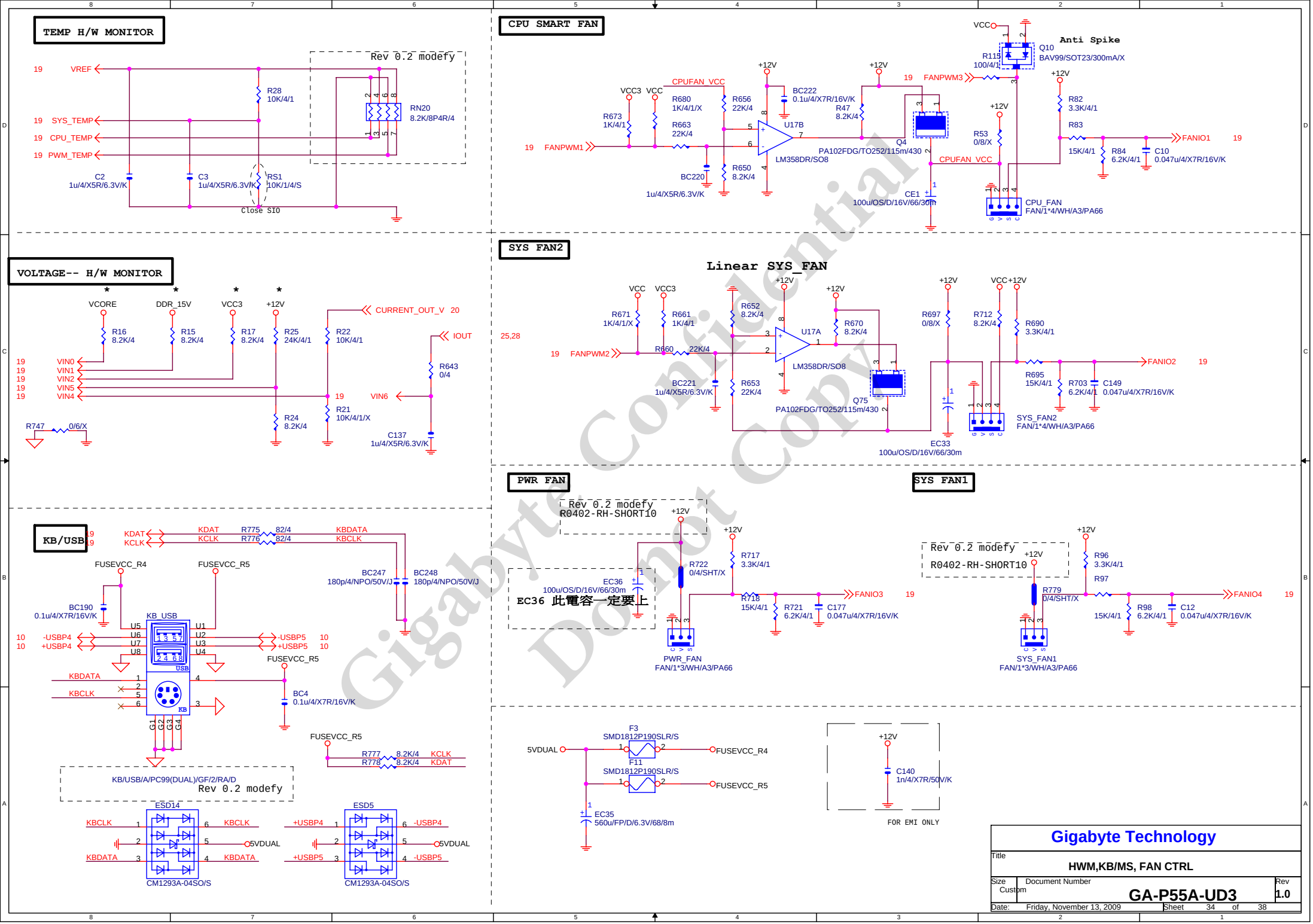
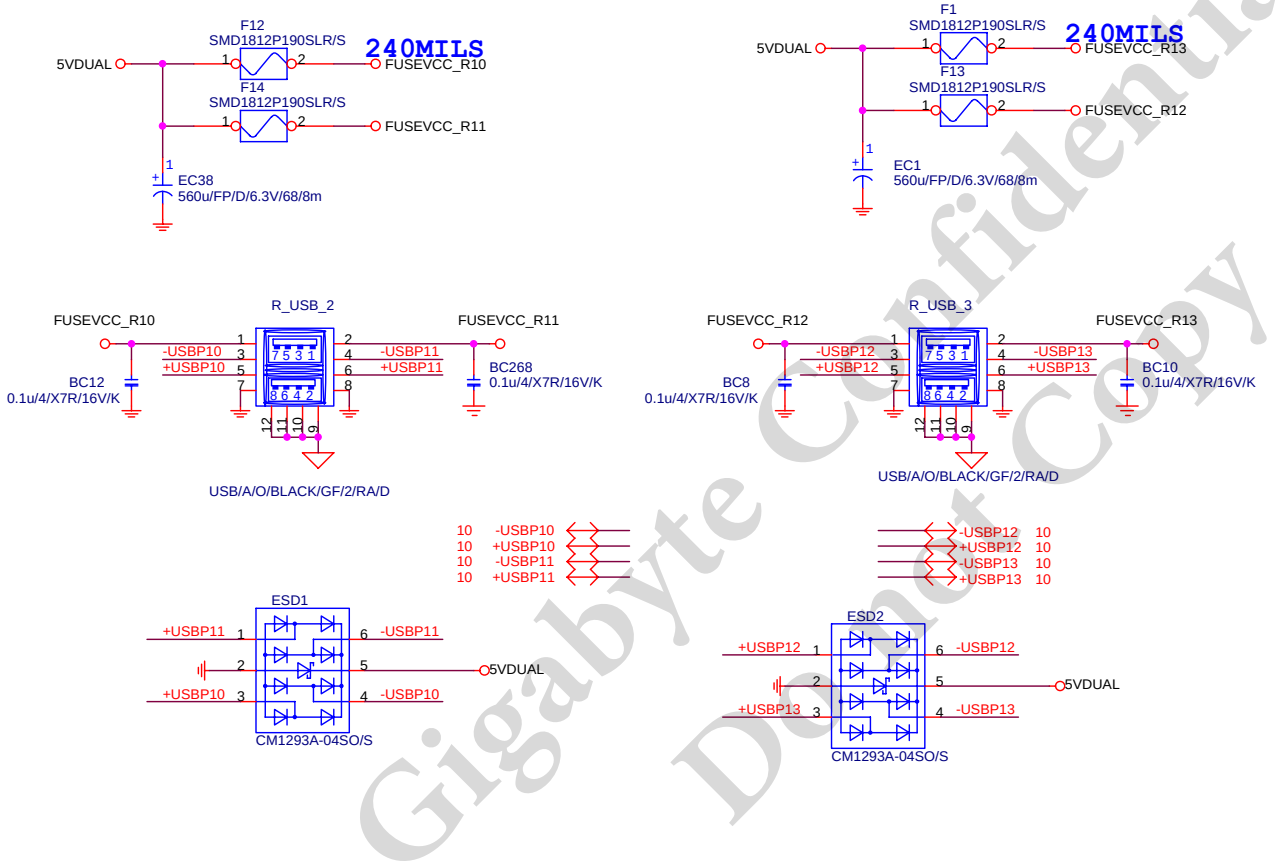


Gigabyte Technology		
Title: TPM I/F-SLB 9635 TT 1.2		
Size: A	Document Number: GA-P55A-UD3	Rev: 1.0
Date: Friday, November 13, 2009	Sheet 33 of 38	





GIGABYTE™

Title
R_USB

Size	Document Number	Rev
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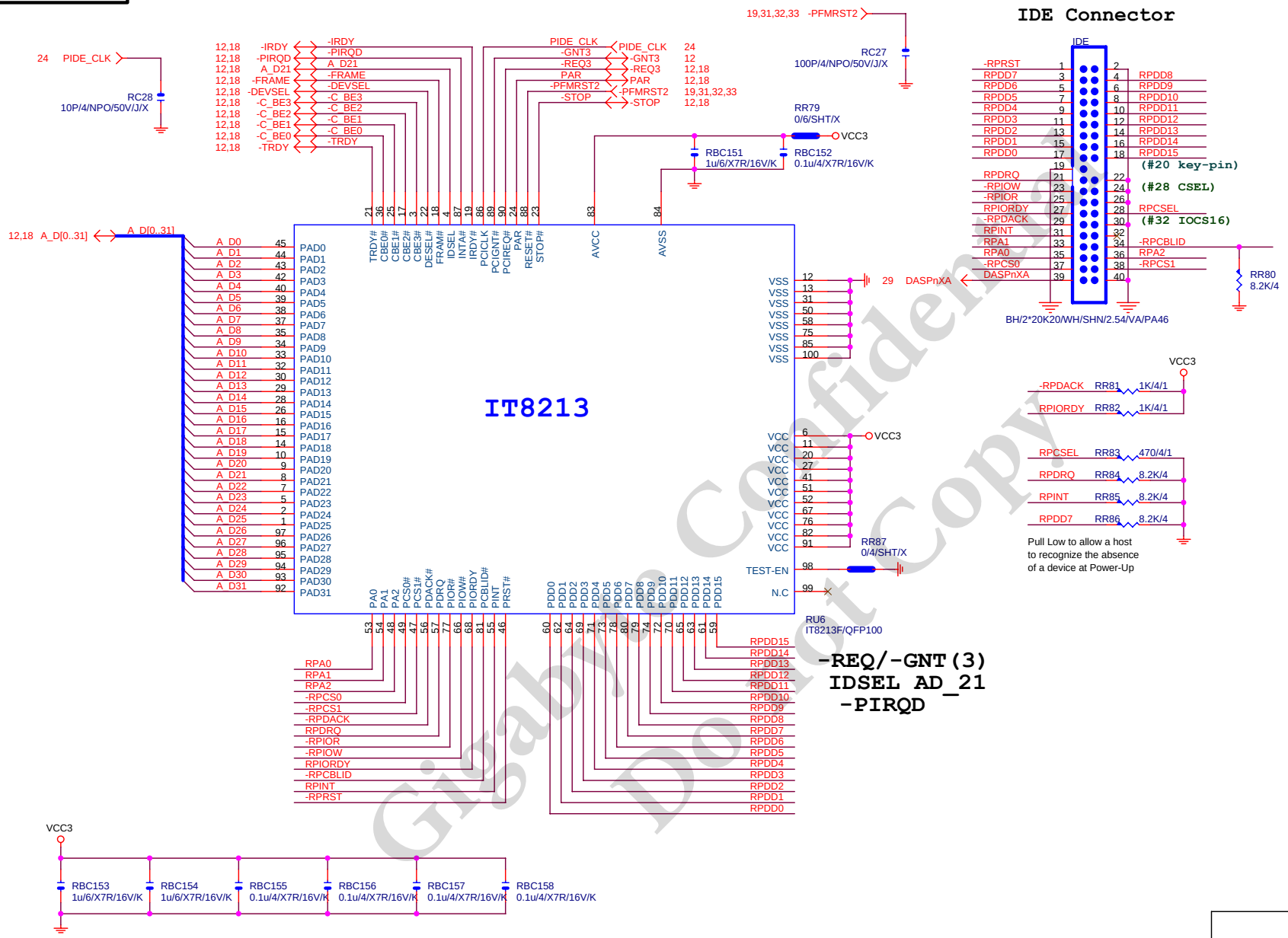
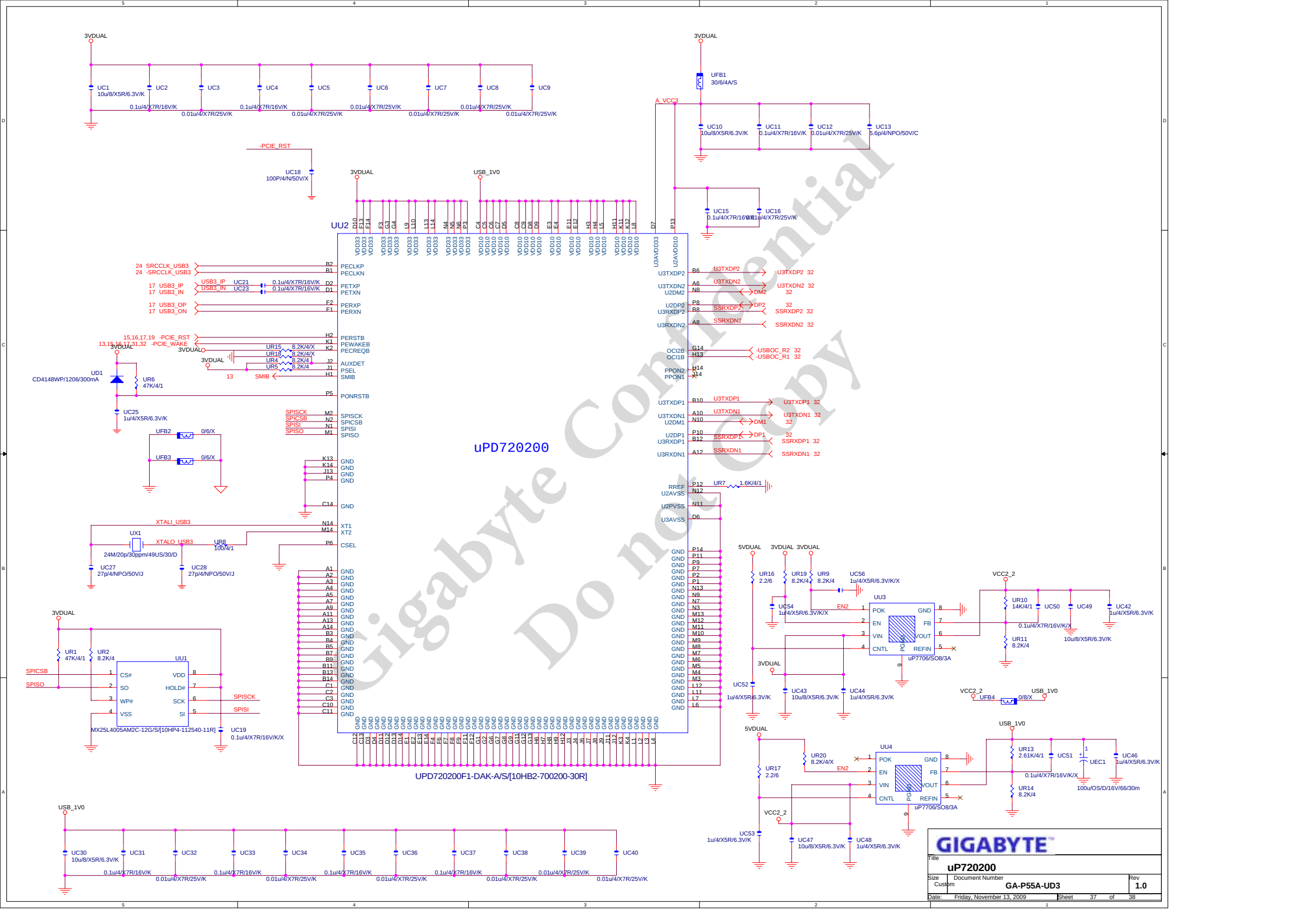
IT8213 1P PATA



Gigabyte Technology			
Title	IT8213 1P PATA		
Size	Document Number GA-P55A-UD3		Rev 1.0
Date: Friday, November 13, 2009	Sheet 36 of 38		


uPD720200
UU2
UPD720200F1-DAK-A/S/[10HB2-700200-30R]
UU1
MX25L4005AM2C-12G/S/[10HP4-112540-11R]
UU3
UU4
uP7706/SO8/3A
3VDUAL
5VDUAL
USB_1V0
VCC2_2
A_VCC3
-PCIE_RST
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GIGABYTE
Title
uP720200
Size
Custom
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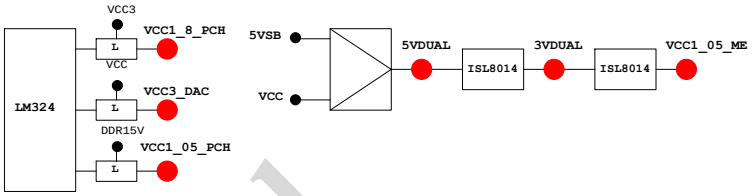
PCH GPIO LIST TABLE

PIN NAME	PWR	AFTER/ PLTRST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

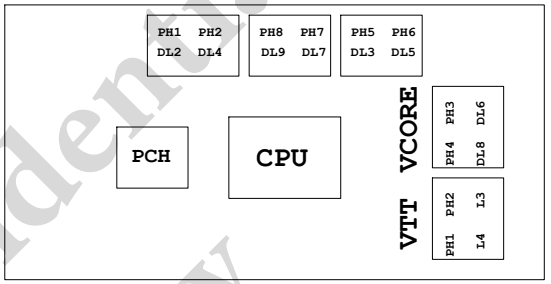
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	空 PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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