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PAGANI M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point

Date : 2011/11/22
Version 0.1

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title	Block Diagrams	
Size: Custom	Document Number: LA-8711	Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 1 of 57	

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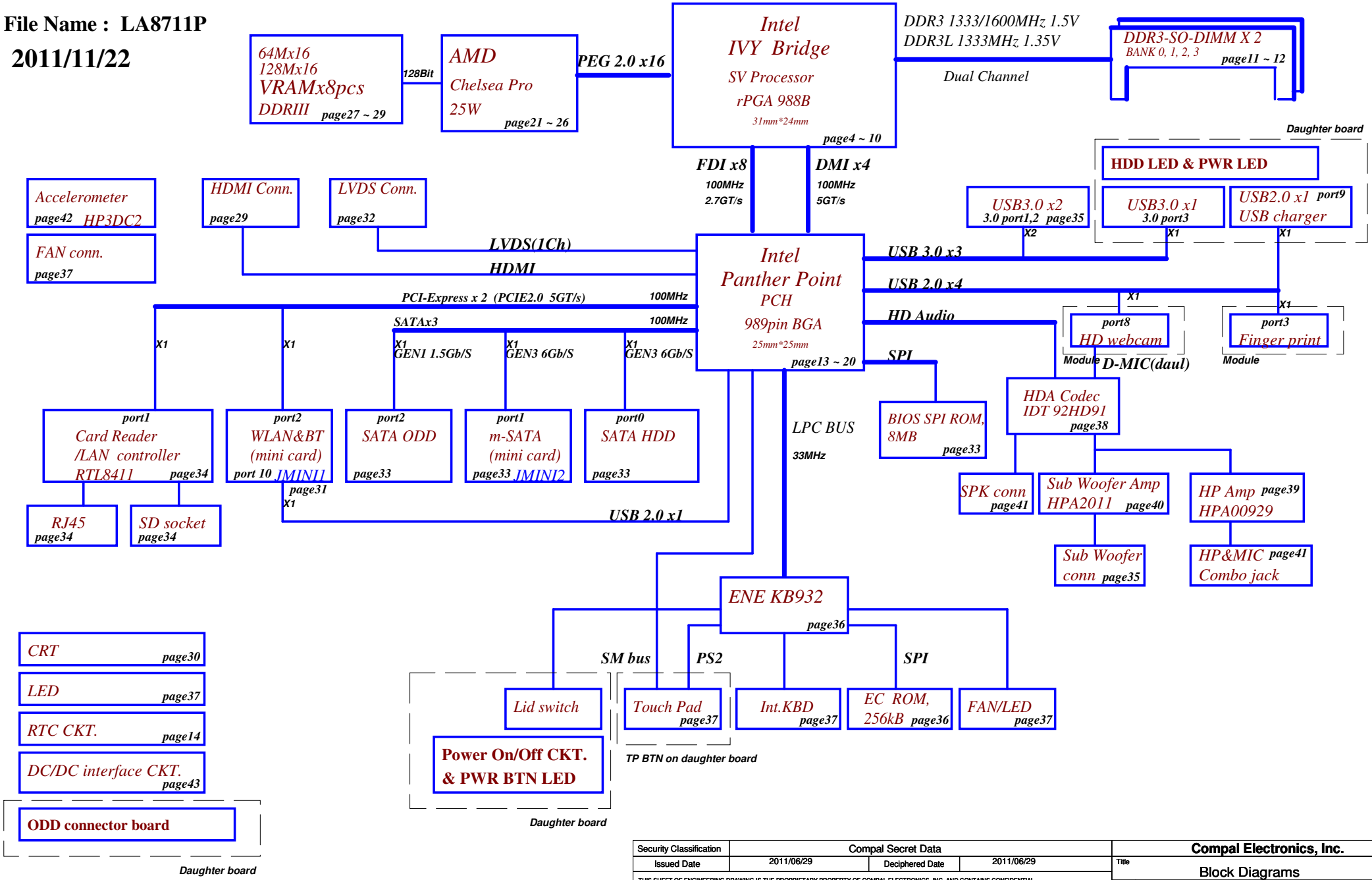
Model Name : Zonda

File Name : LA8711P

2011/11/22



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH				V	V					V
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

SATA	DESTINATION
SATA0	HDD,JHDD1
SATA1	m-SATA,JMINI2
SATA2	ODD, JODD1
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	USB3.0
		1	USB3.0
	UHCI1	2	USB3.0
		3	USB2.0 FRP
	UHCI2	4	X
		5	m-SATA
	UHCI3	6	X
		7	X
EHCI2	UHCI4	8	Camera
		9	USB2.0 and sleep charger
	UHCI5	10	minPCIE-WLAN/BT
		11	X
	UHCI6	12	X
		13	X

USB 3.0	Port	3 External USB Port
	0	USB3.0
	1	USB3.0
	2	USB3.0(SB)

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	CR+ Giga LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Option	@	CONN@	PX@	
UMA	X	X	X	
DIS	X	X	V	

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: Notes List

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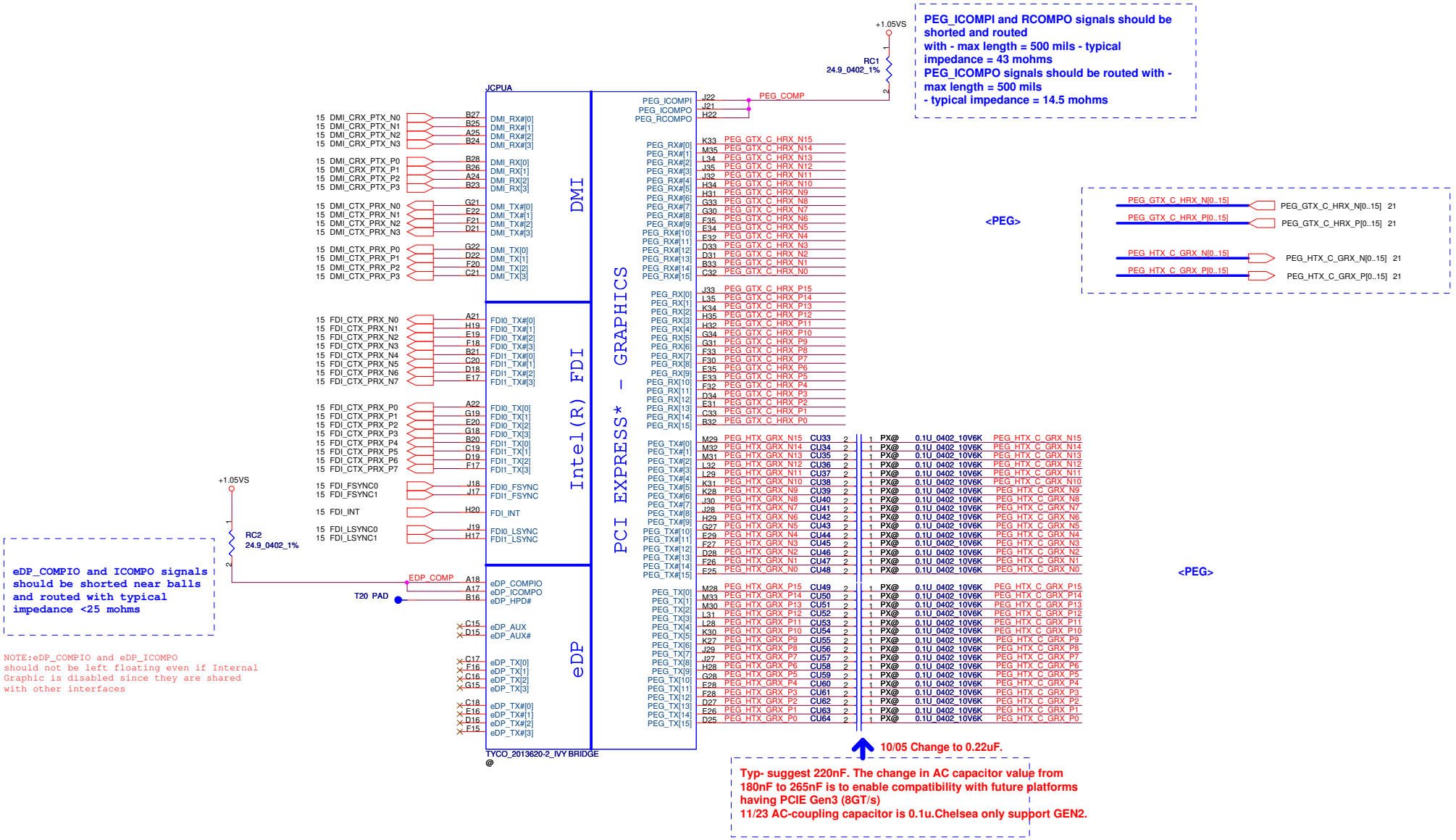

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Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
Custom	LA-8551P	0.1

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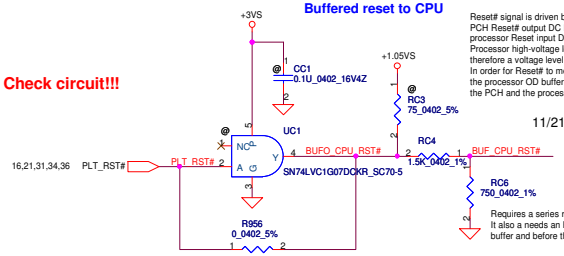
Buffered reset to CPU

Check circuit!!!



Reset# signal is driven by the PCH to multiple agents on the platform. PCH Reset# output DC levels are 0-V and 3.3 V, processor Reset input DC levels are 0V and 1.0 V. Processor high-voltage level is lower than PCH high voltage level, therefore a voltage level shifter is required on the Reset# signal. In order for Reset# to meet the signal quality requirement at the input to the processor OD buffer must be placed on the motherboard between the PCH and the processor.

11/21 follow QAZ60 cost down CPU_RST#

Requires a series resistor of 43±5% between processor and PCH. It also a needs an Rtt of 75±5% to VCCP after the OD buffer and before the series resistor.

JCPU

This pin is for compability with future platforms. A pull up resistor to VCCIO is required if connected to the DF_TVS strap on the PCH.

PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

MISC
- 17 H_SNB_IVB# → C26 PROC_SELECT#
- RC7 10K_0402_5% → AN34 SKTOCC#
- PAD T5 @ → AL33 CATERR#

THERMAL
- 17,36 H_PECI → RC9 0_0402_5% H_PECI_ISO → AN33 PECI
- 36,47 H_PROCHOT# → RC10 56_0402_5% H_PROCHOT#_R → AL32 PROCHOT#
- 17 H_THEMTRIP# → RC12 0_0402_5% H_THEMTRIP#_R → AN32 THERMTRIP#

PWR MANAGEMENT
- 15 H_PM_SYNC → RC13 0_0402_5% H_PM_SYNC_R → AM34 PM_SYNC
- 17 H_CPUPWRGD → RC16 0_0402_5% H_CPUPWRGD_R → AP33 UNCOREPWRGOOD
- UNCOREPWRGOOD:非CORE外的電OK
- PM_SYS_PWRGD_BUF → RC18 130_0402_5% PM_DRAM_PWRGD_R → V8 SM_DRAMPWROK
- SM_DRAMPWROK:DRAM power ok
- BUF_CPU_RST# → AR33 RESET#

CLOCKS
- 100MHz
- BCLK A28, BCLK# A27 → CLK_CPU_DMI 14, CLK_CPU_DMI# 14
- DPLL_REF_CLK A16, DPLL_REF_CLK# A15 → RC84 1K_0402_5%, RC85 1K_0402_5%
- ITP CLK change to part E.

DDR3 MISC
- SM_DRAMRST# → R8 H_DRAMRST# → H_DRAMRST# 6
- SM_RCOMP[0] AK1 → SM_RCOMP0
- SM_RCOMP[1] A5 → SM_RCOMP1
- SM_RCOMP[2] A4 → SM_RCOMP2

JTAG & BPM
- PRDY# AP29, PREQ# AP27
- TCK AR26 XDP_TCK, TMS AR27 XDP_TMS, TRST# AP30 XDP_TRST#
- TDI AR28 XDP_TDI, TDO AP26 XDP_TDO
- DBR# AL35 XDP_DBRESET#_R → RC17 0_0402_5% XDP_DBRESET# → XDP_DBRESET# 15
- BPM#[0] AT28, BPM#[1] AR29, BPM#[2] AR30, BPM#[3] AT30, BPM#[4] AP32 XDP_BPM#4_R, BPM#[5] AR31 XDP_BPM#5_R, BPM#[6] AT31 XDP_BPM#6_R, BPM#[7] AR32 XDP_BPM#7_R
- T60 @ PAD, T61 @ PAD, T62 @ PAD, T63 @ PAD

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6/27 Add ESD solution

SI# 8/16 Reserve RC81~RC85 by ESD request

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

XDP_DBRESET# RC5 2 1K_0402_5% +3VS
circuit check 10k

Processor Pullups

+1.05VS
- RC8 2 62_0402_5% H_PROCHOT#
- RC11 2 10K_0402_5% H_CPUPWRGD_R

H_PROCHOT#
C4680 47P_0402_50V8J

SI# 10/02 Change to Pull High +3VS

+3VS
RC81 10K_0402_5%
+3VALW
CC2 0.1U_0402_16V4Z
UC2 74AHC1G09GW_TSSOP5
@ RC27 0_0402_5%
15 SYS_PWROK
15 PM_DRAM_PWRGD
@ RC28
+3VS
200_0402_5%
Part Number = SA00003Y000
+1.5V_CPU_VDDQ
RC25 200_0402_5%
3V_PCH
RC30 200_0402_5%

Sharing add for module desige

Remove mos for layout

DDR3 Compensation Signals

- SM_RCOMP0 RC23 140_0402_1%
- SM_RCOMP1 RC24 25.5_0402_1%
- SM_RCOMP2 RC26 200_0402_1%

PU/PD for JTAG signals

- XDP_TMS T40 @PAD
- XDP_TDI T41 @PAD
- XDP_TDO T42 @PAD
- XDP_TCK T43 @PAD
- XDP_TRST# T46 @PAD

C263 0.1U_0402_16V7K
- XDP_TRST#
- C264 220P_0402_50V7K
- PLT_RST#
- C265 @ 100P_0402_50V8J
- PM_SYS_PWRGD_BUF
- C266 220P_0402_50V7K
- BUF_CPU_RST#

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

XDP_DBRESET#_R CC4 0.1U_0402_16V7K <BOM Structure>
H_CPUPWRGD_R C118 220P_0402_50V7K

6/27 Add ESD solution

SI# 8/19 BOM
C118 220P
C266 220P
C264 220P
C263 0.1u
CC4 0.1u ok

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Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
C	LA-8041P	0.1

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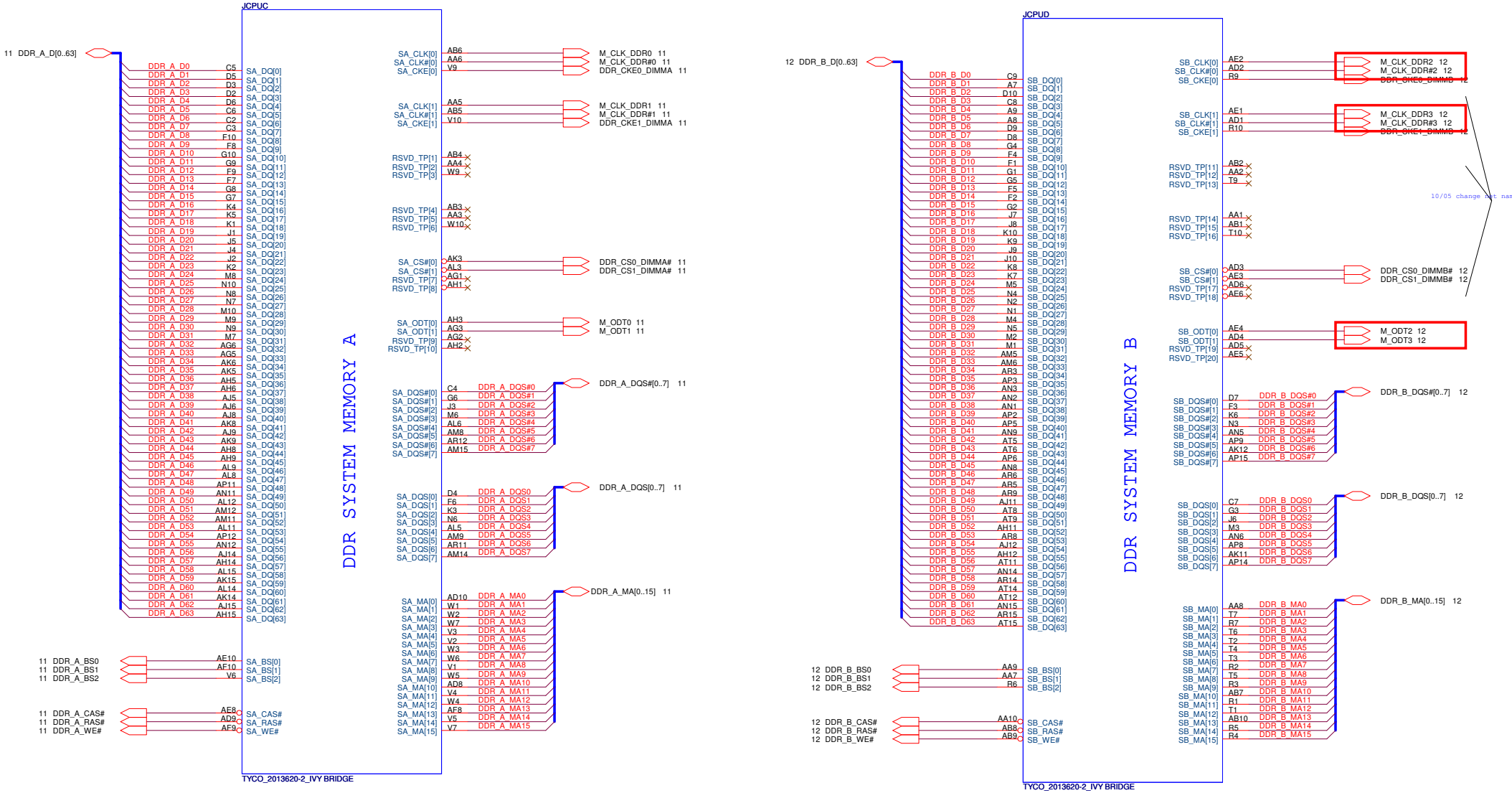

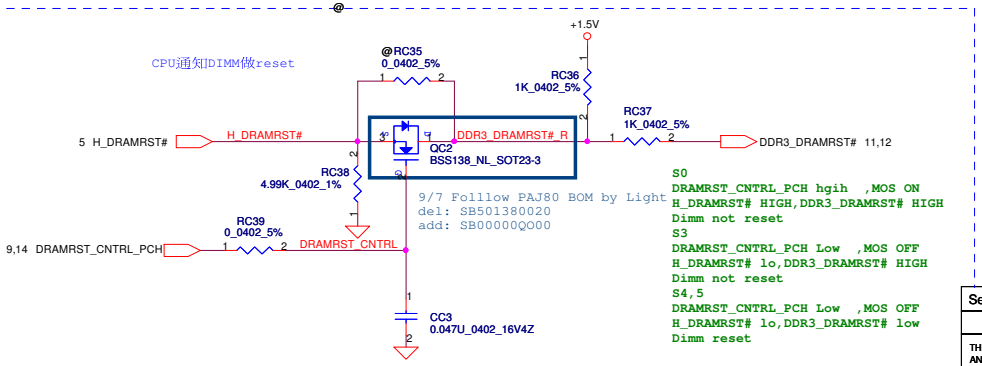

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Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-8041P	0.1

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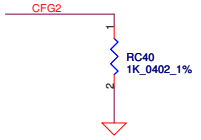
CFG Straps for Processor

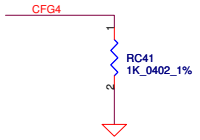
Change to part G.

change to install

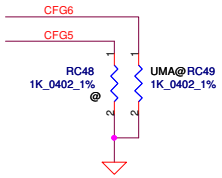


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

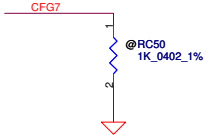
change to install



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



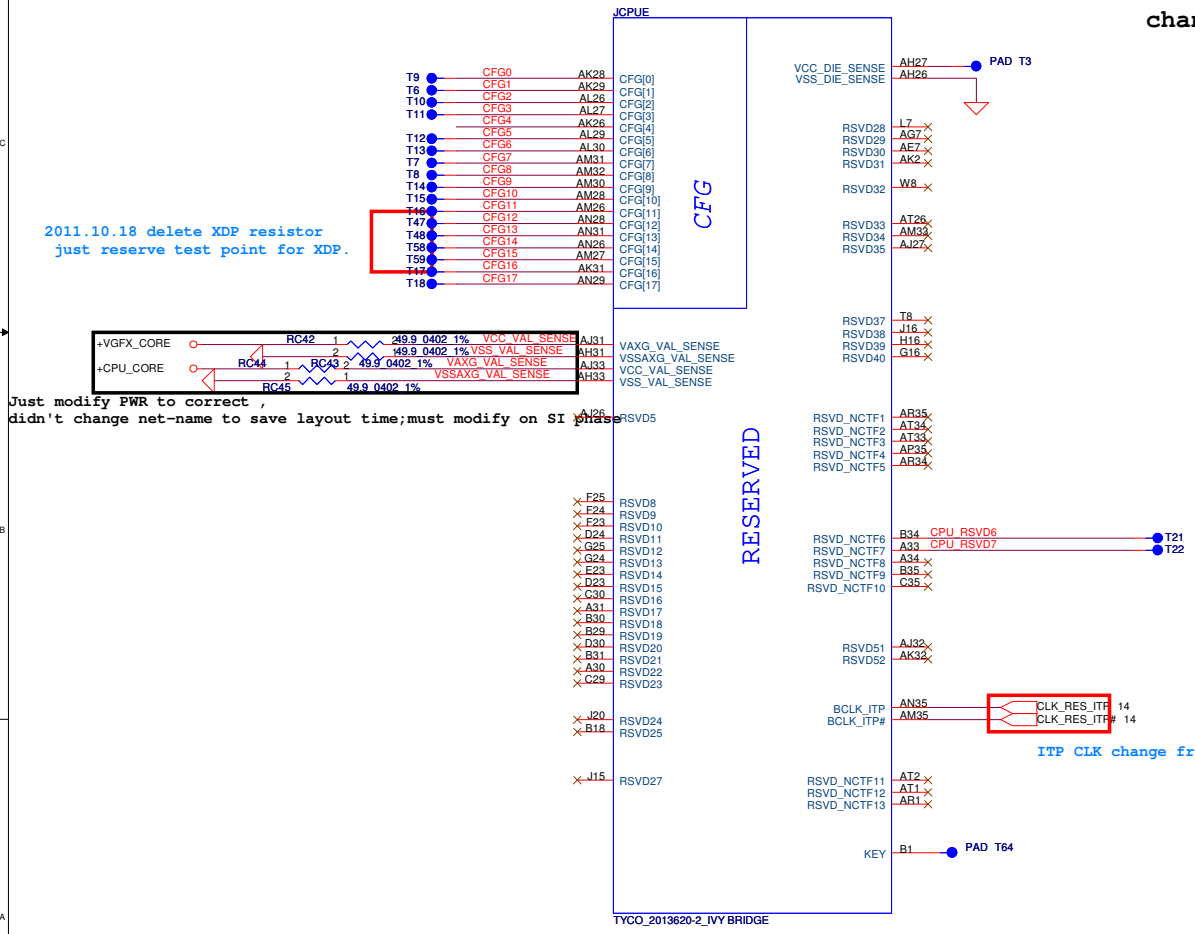
PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled *01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

2011.10.18 delete XDP resistor
just reserve test point for XDP.

Just modify PWR to correct ,
didn't change net-name to save layout time;must modify on SI phase



ITP CLK change from part C.

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Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
Custom	LA-8041P	0.1

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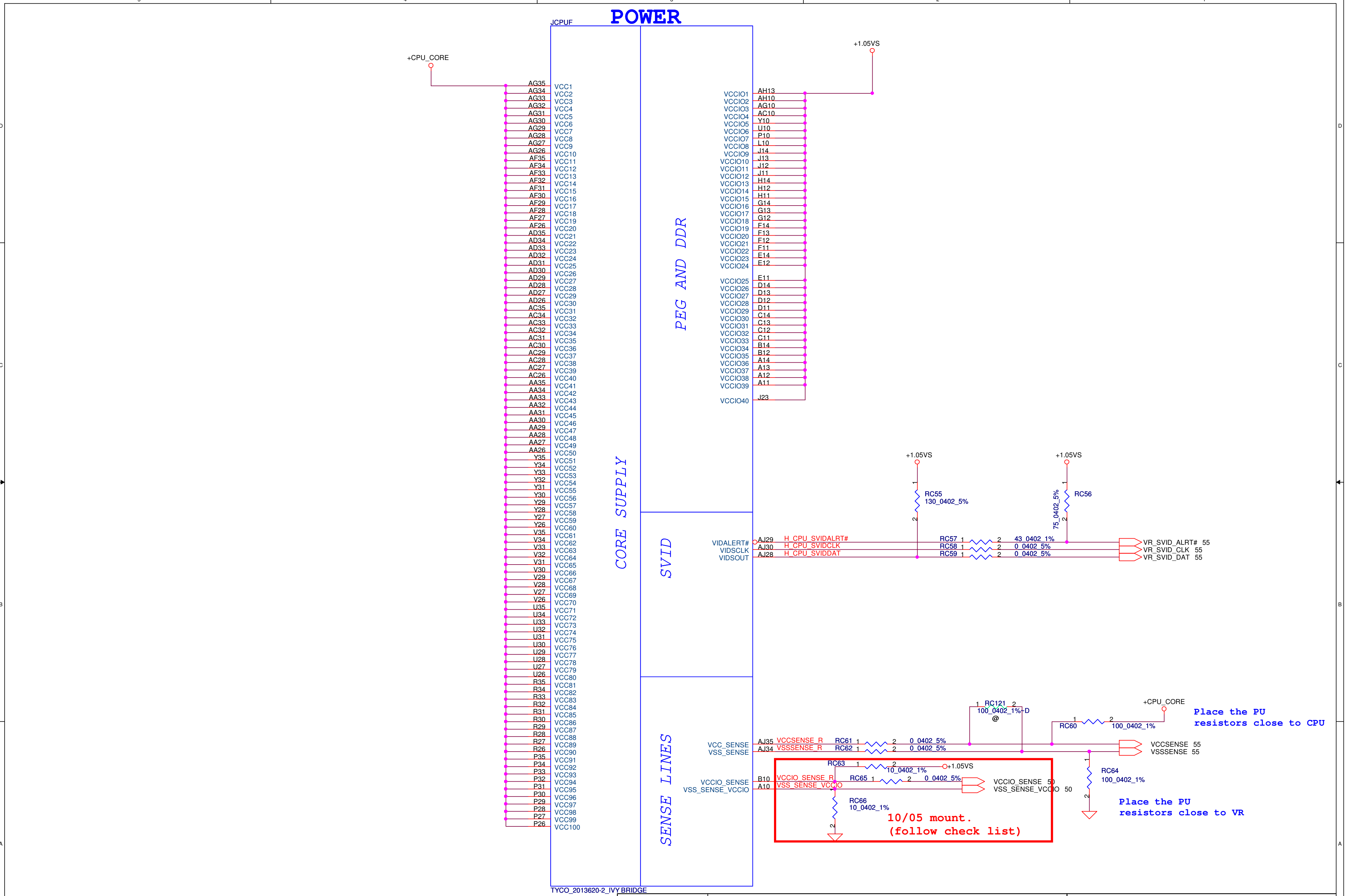
POWER



JCPUF
+CPU_CORE
+1.05VS
AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
VCC1 … VCC100
CORE SUPPLY
PEG AND DDR
VCCIO1 … VCCIO40
AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23
SVID
VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT
RC55 130_0402_5%
RC56 75_0402_5%
RC57 43_0402_1%
RC58 0_0402_5%
RC59 0_0402_5%
VR_SVID_ALRT# 55
VR_SVID_CLK 55
VR_SVID_DAT 55
SENSE LINES
VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R
RC61 0_0402_5%
RC62 0_0402_5%
RC121 100_0402_1% @
RC60 100_0402_1%
VCCSENSE 55
VSSSENSE 55
Place the PU resistors close to CPU
VCCIO_SENSE B10 VCCIO_SENSE_R
VSS_SENSE_VCCIO A10 VSS_SENSE_VCCIO
RC63 10_0402_1%
RC65 0_0402_5%
RC66 10_0402_1%
VCCIO_SENSE 50
VSS_SENSE_VCCIO 50
RC64 100_0402_1%
Place the PU resistors close to VR
10/05 mount. (follow check list)
TYCO_2013620-2_IVY BRIDGE
@

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Title: **PROCESSOR(5/7) PWR,BYPASS**

Size: Custom | Document Number: LA-8041P | Rev: 0.1

POWER

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

+1.5V_CPU_VDDQ
CC74 2 1 0.1U_0402_10V7K
CC75 2 1 0.1U_0402_10V7K
+1.5V

+VGFX_CORE

JCPUG

SENSE LINES
VAXG_SENSE AK35
VSSAXG_SENSE AK34
RC157 1 @ 2 100_0402_1%~D
100±5% pull-up to VCC;
100±5% pull-down to GND.
VCC_AXG_SENSE 55
VSS_AXG_SENSE 55
+V_SM_VREF should have 20 mil trace width

VREF
SM_VREF AL1
+V_SM_VREF_CNT
CC79 0.1U_0402_16V4Z
SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1
+V_DDR_REFA_R
+V_DDR_REFB_R

DDR3 -1.5V RAILS
VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SA RAIL
VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

MISC
VCCSA_SENSE H23
VCCSA_SENSE
VCCSA_SENSE 52
@RC78 0_0402_5%
VCCSA_VID[0] C22
VCCSA_VID[1] C24
RC79 2 VCCSA_VID0
RC80 0_0402_5%
VCCSA_VID1
VCCSA_VID0 52
VCCSA_VID1 52
RC52 @ 75_0402_5%
VCCIO_SEL A19
VCCP_PWRCTRL_R
10K_0402_5%
@RC53

1.8V RAIL
VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

TYCO_2013620-2_IVY BRIDGE

GRAPHICS
AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

+1.5V_CPU_VDDQ
RC68 1K_0402_1%
RC69 1K_0402_1%
11/21 follow PBL22 design remove 10u*2, 1U*8; keep 10U*5
CC100 330U_D2_2V_Y
+1.5V_CPU_VDDQ Source

QC4 Change to SA0000JA00 for small package 1016
+VCCSA
CC22 10U_0603_6.3V6M
CC21 10U_0603_6.3V6M
CC24 10U_0603_6.3V6M
Delete CC25 330U cap 10.19 (after check with power)
11/21 follow PBL22 design remove 10u*2, 1U*5

For Chief River only

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

QC7 SB000002X00 BSS138W-7-F_SOT323-3
DRAMRST_CNTRL_PCH
DRAMRST_CNTRL_PCH 6,14
+V_DDR_REFA
RC15 @ 0_0402_5%
+V_DDR_REFA_R
RC14 @ 1K_0402_1%
QC8 SB000002X00 BSS138W-7-F_SOT323-3
DRAMRST_CNTRL_PCH
+V_DDR_REFB
RC82 @ 0_0402_5%
+V_DDR_REFB_R
RC83 @ 1K_0402_1%

10/03 add +V_DDR_REFB

+1.8VS
RC77 0_0805_5%
+1.8VS_VCCPLL
CC29 10U_0603_6.3V6M
CC120 @ 330U_D2_2VM_R6M
CC121 1U_0402_6.3V6K
CC122 1U_0402_6.3V6K
SI# 7/29 Add CC26 10uF and reserve 330U on 1.8V power Rail

@

+3VALW
+VSB
+1.5V
QC4 AON6718L_DFN8-5
+1.5V_CPU_VDDQ
RC70 100K_0402_5%
RC71 470_0603_5%
RC72 100K_0402_5%
RUN_ON_CPU1.5VS3
R78 @ 20K_0402_5%
RC74 0_0402_5%
36 CPU1.5V_S3_GATE
@RC75 0_0402_5%
36,43,50,51,52,53 SUSP#
RUN_ON_CPU1.5VS3_SUSP
2N7002DWH_SOT363-6 QC5B
2N7002DWH_SOT363-6 QC5A
RC73 330K_0402_5%
CC118 0.1U_0402_25V6
RUN_ON_CPU1.5VS3#
Q10A 2N7002DWH_SOT363-6
SI# BOM Change CC118 0.1u 25V form 0.1u 16V

CPU EDS descript as follow:
For Chief River platforms this pin should not be used.

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

Follow DG 0.71 page 6

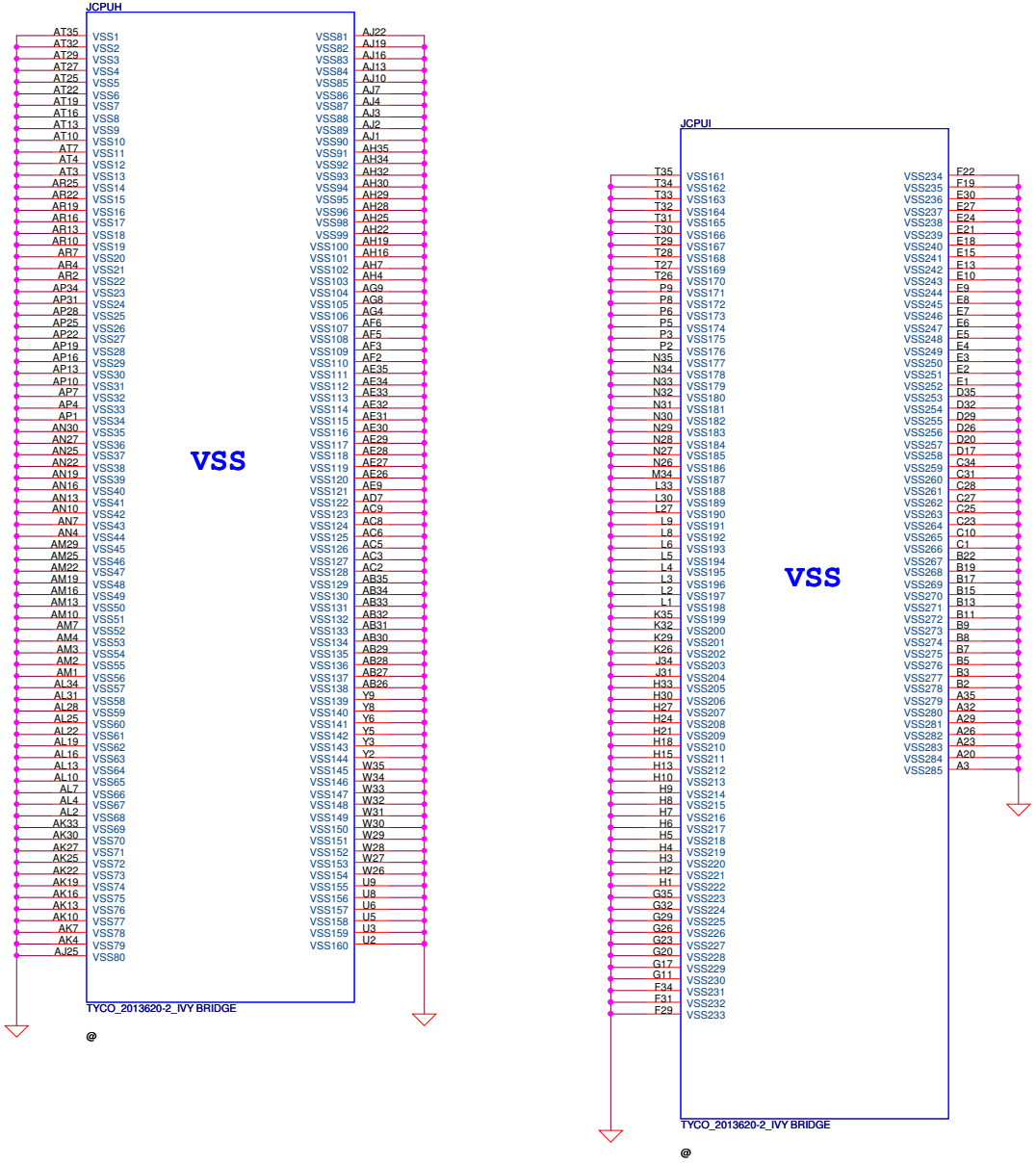
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Sunday, November 27, 2011 Sheet 9 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Sunday, November 27, 2011 Sheet 10 of 57

DDR3 SO-DIMM A

6 DDR_A_D[0..63]
6 DDR_A_DQS[0..7]
6 DDR_A_DQS#[0..7]
6 DDR_A_MA[0..15]

Delete DDR_A_DM[0..7]

All VREF traces should have 20 mil trace width

+V_DDR_REFA

CD1 0.1U_0402_16V7K
CD2 2.2U_0603_6.3V6K

+1.5V 3.56A@+1.5V

JDDRL1
LCN_DAN06-K4806-0102
CONIN@

	VREF_DQ	1	2	VSS1			
DDR_A_D0	VSS2	3	4	DQ4	DDR_A_D4		
DDR_A_D1	DQ0	5	6	DQ5	DDR_A_D5		
	DQ1	7	8	VSS3			
	VSS4	9	10	DQS#0	DDR_A_DQS#0		
	DM0	11	12	DQS0	DDR_A_DQS0		
	VSS5	13	14	VSS6			
DDR_A_D2	DQ2	15	16	DQ6	DDR_A_D6		
DDR_A_D3	DQ3	17	18	DQ7	DDR_A_D7		
	VSS7	19	20	VSS8			
DDR_A_D8	DQ8	21	22	DQ12	DDR_A_D12		
DDR_A_D9	DQ9	23	24	DQ13	DDR_A_D13		
	VSS9	25	26	VSS10			
DDR_A_DQS#1	DQS#1	27	28	DM1			
DDR_A_DQS1	DQS1	29	30	RESET#	DDR3_DRAMRST#	DDR3_DRAMRST#	6,12
	VSS11	31	32	VSS12			
DDR_A_D10	DQ10	33	34	DQ14	DDR_A_D14		
DDR_A_D11	DQ11	35	36	DQ15	DDR_A_D15		
	VSS13	37	38	VSS14			
DDR_A_D16	DQ16	39	40	DQ20	DDR_A_D20		
DDR_A_D17	DQ17	41	42	DQ21	DDR_A_D21		
	VSS15	43	44	VSS16			
DDR_A_DQS#2	DQS#2	45	46	DM2			
DDR_A_DQS2	DQS2	47	48	VSS17			
	VSS18	49	50	DQ22	DDR_A_D22		
DDR_A_D18	DQ18	51	52	DQ23	DDR_A_D23		
DDR_A_D19	DQ19	53	54	VSS19			
	VSS20	55	56	DQ28	DDR_A_D28		
DDR_A_D24	DQ24	57	58	DQ29	DDR_A_D29		
DDR_A_D25	DQ25	59	60	VSS21			
	VSS22	61	62	DQS#3	DDR_A_DQS#3		
	DM3	63	64	DQS3	DDR_A_DQS3		
	VSS23	65	66	VSS24			
DDR_A_D26	DQ26	67	68	DQ30	DDR_A_D30		
DDR_A_D27	DQ27	69	70	DQ31	DDR_A_D31		
	VSS25	71	72	VSS26			
6 DDR_CKE0_DIMMA	DDR_CKE0_DIMMA	73	74	CKE1	DDR_CKE1_DIMMA	DDR_CKE1_DIMMA	6
	CKE0	75	76	VDD2			
	VDD1	77	78	A15	DDR_A_MA15		
	NC1	79	80	A14	DDR_A_MA14		
6 DDR_A_BS2	BA2	81	82	VDD4			
	VDD3	83	84	A11	DDR_A_MA11		
DDR_A_MA12	A12/BC#	85	86	A7	DDR_A_MA7		
DDR_A_MA9	A9	87	88	VDD6			
	VDD5	89	90	A6	DDR_A_MA6		
DDR_A_MA8	A8	91	92	A4	DDR_A_MA4		
DDR_A_MA5	A5	93	94	VDD8			
	VDD7	95	96	A2	DDR_A_MA2		
DDR_A_MA3	A3	97	98	A0	DDR_A_MA0		
DDR_A_MA1	A1	99	100	VDD10			
	VDD9	101	102	CK1	M_CLK_DDR1	M_CLK_DDR1	6
6 M_CLK_DDR0	CK0	103	104	CK1#	M_CLK_DDR#1	M_CLK_DDR#1	6
6 M_CLK_DDR#0	CK0#	105	106	VDD12			
	VDD11	107	108	BA1	DDR_A_BS1		
DDR_A_MA10	A10/AP	109	110	RAS#	DDR_A_RAS#	DDR_A_BS1 6 DDR_A_RAS# 6	
DDR_A_BS0	BA0	111	112	VDD14			
	VDD13	113	114	S0#	DDR_CS0_DIMMA#		
6 DDR_A_WE#	WE#	115	116	ODT0	M_ODT0	DDR_CS0_DIMMA# 6 M_ODT0 6	
6 DDR_A_CAS#	CAS#	117	118	VDD16			
	VDD15	119	120	ODT1	M_ODT1	M_ODT1 6	
DDR_A_MA13	A13	121	122	NC2			
6 DDR_CS1_DIMMA#	S1#	123	124	VDD18			
	VDD17	125	126	VREF_CA	+VREF_CA		
	NCTEST	127	128	VSS28			
DDR_A_D32	VSS27	129	130	DQ36	DDR_A_D36		
DDR_A_D33	DQ32	131	132	DQ37	DDR_A_D37		
	DQ33	133	134	VSS30			
DDR_A_DQS#4	VSS29	135	136	DM4			
DDR_A_DQS4	DQS4	137	138	VSS31			
	VSS32	139	140	DQ38	DDR_A_D38		
DDR_A_D34	DQ34	141	142	DQ39	DDR_A_D39		
DDR_A_D35	DQ35	143	144	VSS33			
	VSS34	145	146	DQ44	DDR_A_D44		
DDR_A_D40	DQ40	147	148	DQ45	DDR_A_D45		
DDR_A_D41	DQ41	149	150	VSS35			
	VSS36	151	152	DQS#5	DDR_A_DQS#5		
	DM5	153	154	DQS5	DDR_A_DQS5		
	VSS37	155	156	VSS38			
DDR_A_D42	DQ42	157	158	DQ46	DDR_A_D46		
DDR_A_D43	DQ43	159	160	DQ47	DDR_A_D47		
	VSS39	161	162	VSS40			
DDR_A_D48	DQ48	163	164	DQ52	DDR_A_D52		
DDR_A_D49	DQ49	165	166	DQ53	DDR_A_D53		
	VSS41	167	168	VSS42			
DDR_A_DQS#6	DQS#6	169	170	DM6			
DDR_A_DQS6	DQS6	171	172	VSS43			
	VSS44	173	174	DQ54	DDR_A_D54		
DDR_A_D50	DQ50	175	176	DQ55	DDR_A_D55		
DDR_A_D51	DQ51	177	178	VSS45			
	VSS46	179	180	DQ60	DDR_A_D60		
DDR_A_D56	DQ56	181	182	DQ61	DDR_A_D61		
DDR_A_D57	DQ57	183	184	VSS47			
	VSS48	185	186	DQS#7	DDR_A_DQS#7		
	DM7	187	188	DQS7	DDR_A_DQS7		
	VSS49	189	190	VSS50			
DDR_A_D58	DQ58	191	192	DQ62	DDR_A_D62		
DDR_A_D59	DQ59	193	194	DQ63	DDR_A_D63		
	VSS51	195	196	VSS52			
RD51 2 10K_0402_5%	SA0	197	198	EVENT#			
+3VS	VDDSPD	199	200	SDA	PCH_SMBDATA	PCH_SMBDATA	12,14,37,40
	SA1	201	202	SCL	PCH_SMBCLK	PCH_SMBCLK	12,14,37,40
	VTT1	203	204	VTT2	+0.75VS		
	G1	205	206	G2		0.6A@+0.75VS	

CD23 2.2U_0603_6.3V6K
CD24 0.1U_0402_16V7K
RD6 10K_0402_5%

RD1 1K_0402_1%
RD2 1K_0402_1%
RD3 1K_0402_1%
RD4 1K_0402_1%

CD10 0.1U_0402_16V7K
CD11 2.2U_0603_6.3V6K

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

11/18 for layout spacing: remove CD5/CD6/CD9
11/21 1U*4 only

CD3 1U_0402_6.3V6K
CD4 1U_0402_6.3V6K
CD5 1U_0402_6.3V6K
CD6 1U_0402_6.3V6K

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

CD12 10U_0603_6.3V6M
CD13 10U_0603_6.3V6M
CD14 10U_0603_6.3V6M
CD15 10U_0603_6.3V6M
CD16 10U_0603_6.3V6M
CD17 10U_0603_6.3V6M
CD18 0.1U_0402_16V7K
CD19 0.1U_0402_16V7K
CD20 0.1U_0402_16V7K
CD21 0.1U_0402_16V7K
CD22 330U_B2_2.5VM_R15M
SGA00004400

DDR3 SO-DIMM A

CD26 0.1U_0402_16V7K
CD27 0.1U_0402_16V7K
CD28 0.1U_0402_16V7K
CD25 0.1U_0402_16V7K

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

Standard
<Address(SA1,SA0):00>

LA-8711 Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Title	DDRIII DIMM		
Size C	Document Number LA-8041P		Rev 0.1
Date: Sunday, November 27, 2011	Sheet 11 of 61		

DDR3 SO-DIMM B

10/03 change to +V_DDR_REFB

All VREF traces should have 20 mil trace width

3.56A@+1.5V

6 DDR_B_D[0..63]
6 DDR_B_DQS[0..7]
6 DDR_B_DQS#[0..7]
6 DDR_B_MA[0..15]

Delete DDR_B_DM[0..7]

10/03 change to +V_DDR_REFB

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

11/18 for layout spacing: remove CD51/CD54/CD53
11/21 keep 1u*4 only -Kenny

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

SGA00004400

10/03 change to +VREF_CB

10/05 change to PH.

Standard
<Address(SA1,SA0):10>

0.6A@+0.75VS

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

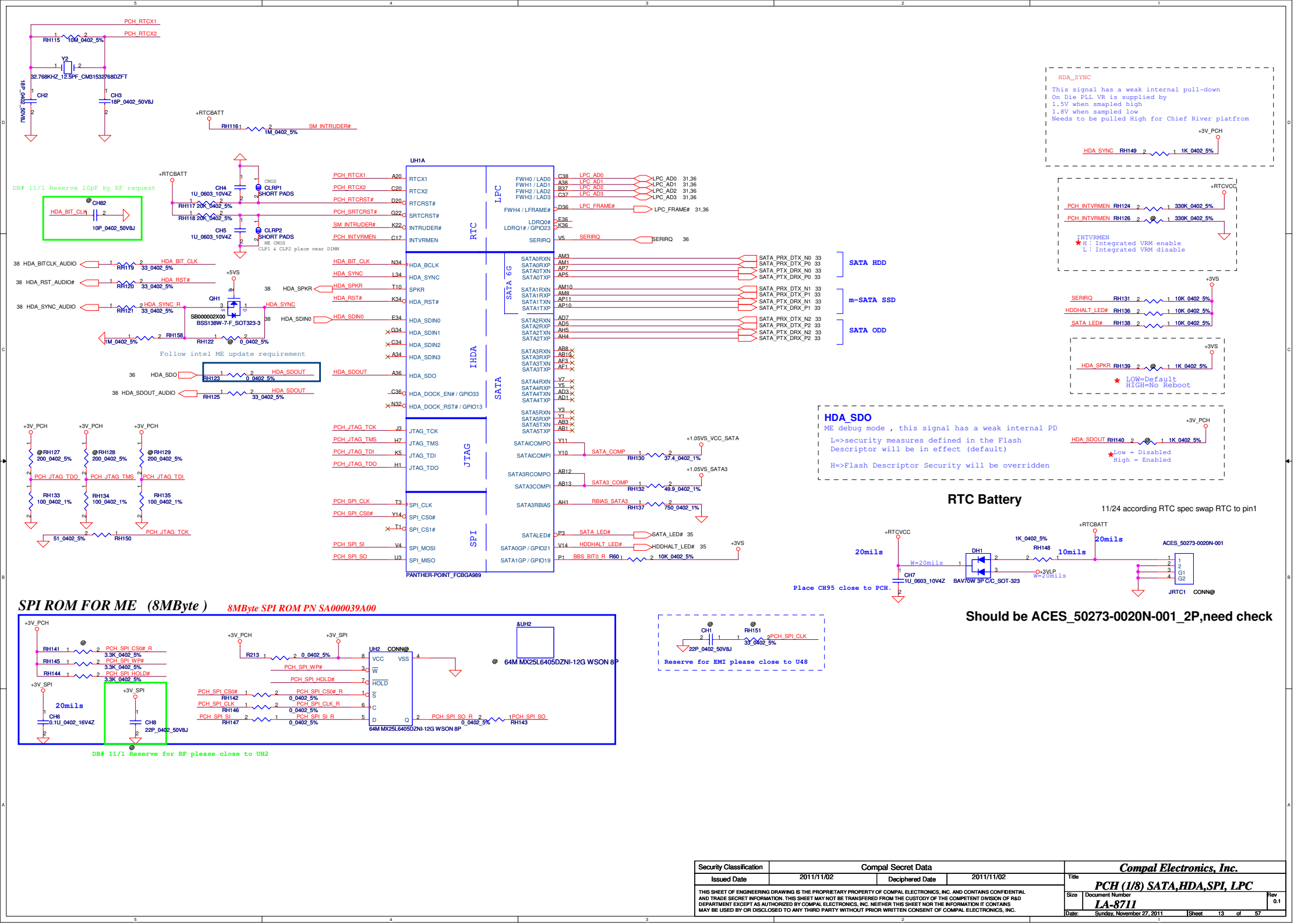
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: DDRIII-DDRH

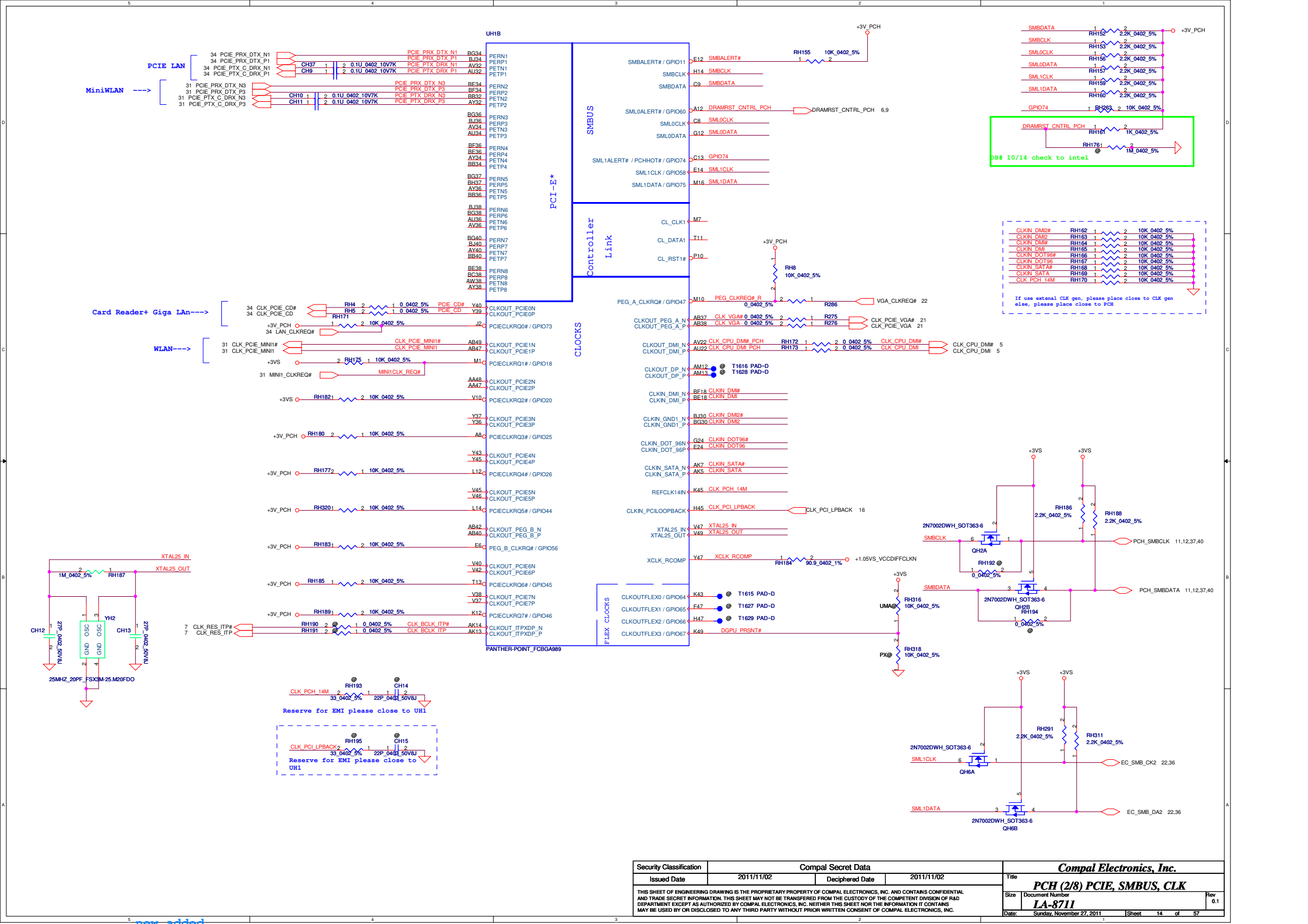
Size	Document Number	Rev
		0.1

Date: Sunday, November 27, 2011 | Sheet 12 of 61



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.	
Title	PCH (1/8) SATA,HDA,SPI, LPC
Size	Document Number: LA-8711
Rev	0.1
Date:	Sunday, November 27, 2011
Sheet	13 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

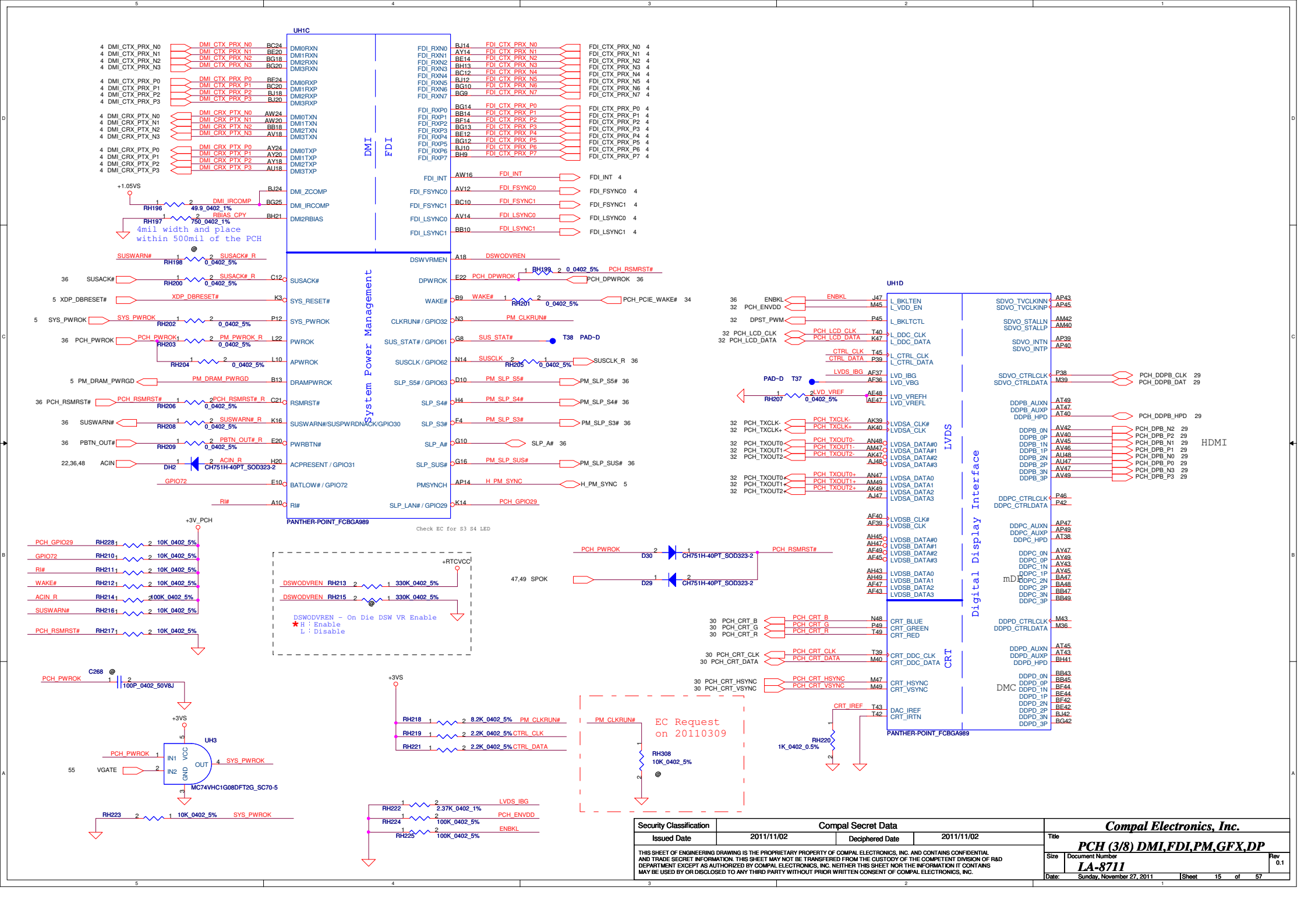
Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 14 of 57

new added



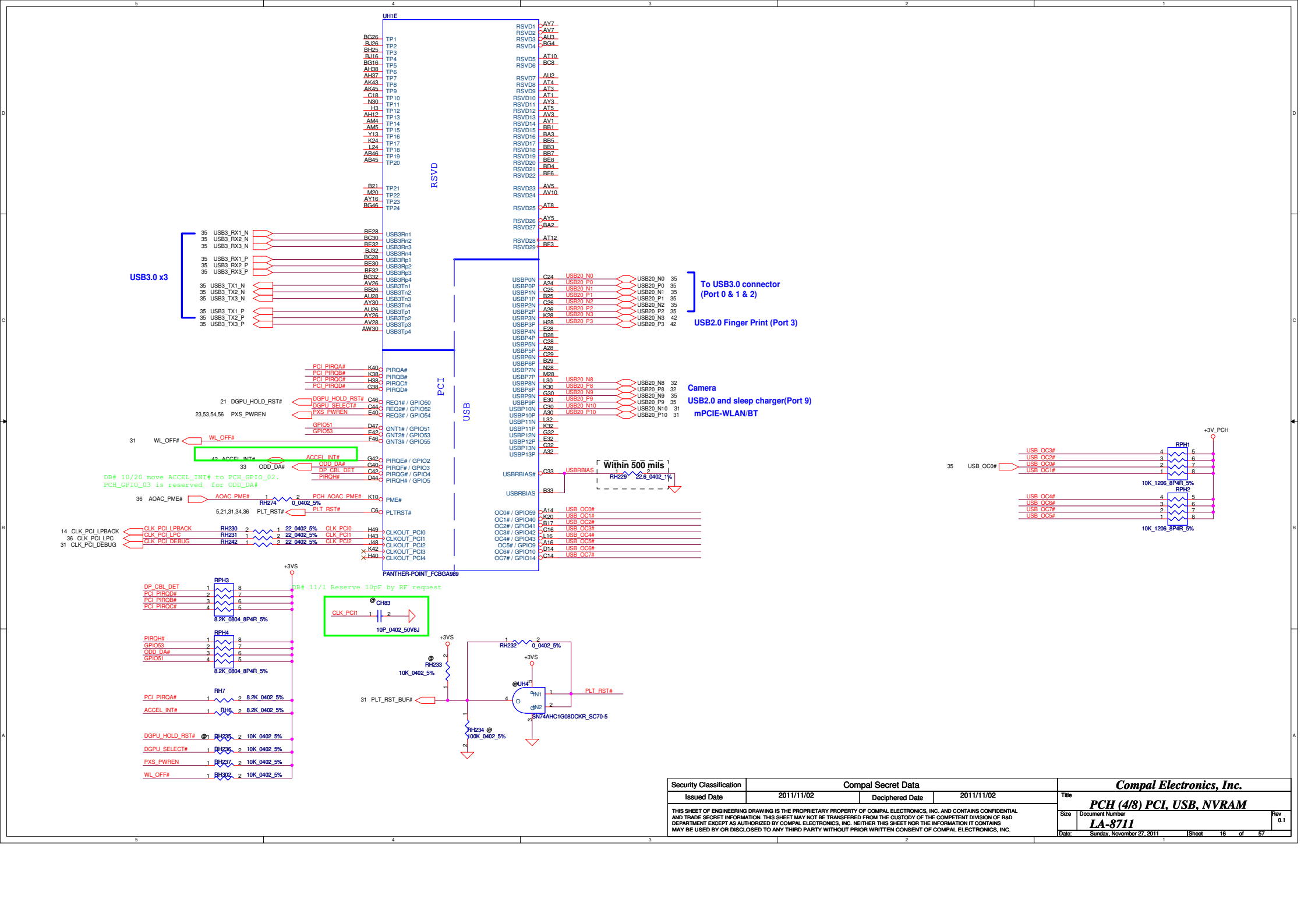
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 15 of 57


UH1E
PANTHER-POINT_FCBGA989
RSVD
PCI
USB
USB3.0 x3
To USB3.0 connector
(Port 0 & 1 & 2)
USB2.0 Finger Print (Port 3)
Camera
USB2.0 and sleep charger(Port 9)
mPCIE-WLAN/BT
Within 500 mils
DB# 10/20 move ACCEL_INT# to PCH_GPIO_02.
PCH_GPIO_03 is reserved for ODD_DA#
DB# 11/1 Reserve 10pF by RF request
SN74AHC1G08DCKR_SC70-5
10K_1206_8P4R_5%
8.2K_0804_8P4R_5%
Security Classification
Compal Secret Data
Issued Date
2011/11/02
Deciphered Date
2011/11/02
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Compal Electronics, Inc.
Title
PCH (4/8) PCI, USB, NVRAM
Size
Document Number
LA-8711
Rev
0.1
Date: Sunday, November 27, 2011
Sheet 16 of 57

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3V_PCH
RH267 1 2 SLP_ME_CSW_DEV# 10K_0402_5%
RH241 1 2 SLP_ME_CSW_DEV# 1K_0402_5% @

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

+3VS
RH245 2 @ 1 1K_0402_5% PCH_GPIO37
RH246 2 1 PCH_GPIO37 100K_0402_5%

GPIO27
PCH_GPIO27 (Have internal Pull-High)
★High: VCCVRM VR Enable
Low: VCCVRM VR Disable
@RH250 1 2 PCH_GPIO27 10K_0402_5%

DB# 10/20 Reserve GPIO 36 pull up resistor and add pull down resistor
DB# 11/23 pull up +3VS for ODD_detect#

+3VS
10K_0402_5% 2 RH301 1 ODD_DETECT#
10K_0402_5% 2 @RH255 1 ODD_DETECT#

DB# 10/20 Common BT_ON is GPIO 34 (Rout to GPIO 38 currently), GPIO 38 pull high 10K to 3VS only

UH1F

36 GPIO0	GPIO0	T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40
	GPIO1	A42	TACH1 / GPIO1	TACH5 / GPIO69	B41
	GPIO6	H36	TACH2 / GPIO6	TACH6 / GPIO70	C41
36 EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7	TACH7 / GPIO71	A40
36 EC_SMI#	EC_SMI#	C10	GPIO8		
	DMC_DET#	C4	LAN_PHY_PWR_CTRL / GPIO12		
36 EC_LID_OUT#	RH154 2 1 0_0402_5% EC_LID_OUT#_R	G2	GPIO15	A20GATE	P4
	PCH_GPIO16	U2	SATA4GP / GPIO16	PECI	AU16
56 VGA_PWRGD	VGA_PWRGD	D40	TACH0 / GPIO17	RCIN#	P5
	PCH_GPIO22	T5	SCLOCK / GPIO22	PROCPWRGD	AY11
51 DDR3L_EN	DDR3L_EN	E8	GPIO24	THRMTRIP#	AY10
	PCH_GPIO27	E16	GPIO27	INIT3_3V#	T14
36 SLP_ME_CSW_DEV#	SLP_ME_CSW_DEV#	P8	GPIO28	DF_TVS	AY1
31 BT_ON#	BT_ON#	K1	STP_PCI# / GPIO34	TS_VSS1	AH8
	PCH_GPIO35	K4	GPIO35	TS_VSS2	AK11
33 ODD_DETECT#	ODD_DETECT#	V8	SATA2GP / GPIO36	TS_VSS3	AH10
	PCH_GPIO37	M5	SATA3GP / GPIO37	TS_VSS4	AK10
	PCH_GPIO38	N2	SLOAD / GPIO38	NC_1	P37
	PCH_GPIO39	M3	SDATAOUT0 / GPIO39		
	PCH_GPIO48	V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2
	GPIO49	V3	SATA5GP / GPIO49 / TEMP_ALERT#	VSS_NCTF_16	BG48
33 HDD_DETECT#	HDD_DETECT#	D6	GPIO57	VSS_NCTF_17	BH3
				VSS_NCTF_18	BH47
	VSS_NCTF_1	A4		VSS_NCTF_19	BJ4
	VSS_NCTF_2	A44		VSS_NCTF_20	BJ44
	VSS_NCTF_3	A45		VSS_NCTF_21	BJ45
	VSS_NCTF_4	A46		VSS_NCTF_22	BJ46
	VSS_NCTF_5	A5		VSS_NCTF_23	BJ5
	VSS_NCTF_6	A6		VSS_NCTF_24	BJ6
	VSS_NCTF_7	B3		VSS_NCTF_25	C2
	VSS_NCTF_8	B47		VSS_NCTF_26	C48
	VSS_NCTF_9	BD1		VSS_NCTF_27	D1
	VSS_NCTF_10	BD49		VSS_NCTF_28	D49
	VSS_NCTF_11	BE1		VSS_NCTF_29	E1
	VSS_NCTF_12	BE49		VSS_NCTF_30	E49
	VSS_NCTF_13	BF1		VSS_NCTF_31	F1
	VSS_NCTF_14	BF49		VSS_NCTF_32	F49

GPIO
CPU/MISC
NCTF
PANTHER-POINT_FCBGA989

11/24 Kirk review need pu +3VS; but not in check list.

+3VS
RH280 10K_0402_5%
ODD_EN# 33

+3VS
RH238 10K_0402_5%
GATEA20 36

PCH_PECI_R 0_0402_5% @ RH239 H_PECI 5,36
EC_KBRST# 36
H_CPUPWRGD 5
H_THERMTRIP# 390_0402_5% RH240 H_THEMTRIP# 5

+1.8VS
RH226 2.2K_0402_5%
NV_CLE RH227 1K_0402_5% H_SNB_IVB# 5
Layout note: CLOSE TO THE BRANCHING POINT

+3VS
ODD_EN# RH310 10K_0402_5%
GPIO6 RH243 10K_0402_5%
GPIO1 RH244 10K_0402_5%
EC_KBRST# RH295 10K_0402_5%
PCH_GPIO35 RH273 10K_0402_5%
PCH_GPIO16 RH247 10K_0402_5%

+3V_PCH
DDR3L_EN @RH248 10K_0402_5%
HDD_DETECT# RH249 10K_0402_5%
DMC_DET# RH251 10K_0402_5%
EC_LID_OUT#_R RH252 1K_0402_5%
EC_SMI# @RH253 10K_0402_5%

+3VS
GPIO0 RH254 10K_0402_5%
PCH_GPIO38 RH256 10K_0402_5%
PCH_GPIO48 RH257 10K_0402_5%
PCH_GPIO22 RH258 10K_0402_5%
BT_ON# RH259 10K_0402_5%
PCH_GPIO39 RH260 10K_0402_5%
VGA_PWRGD RH261 10K_0402_5%
GPIO49 RH262 10K_0402_5%

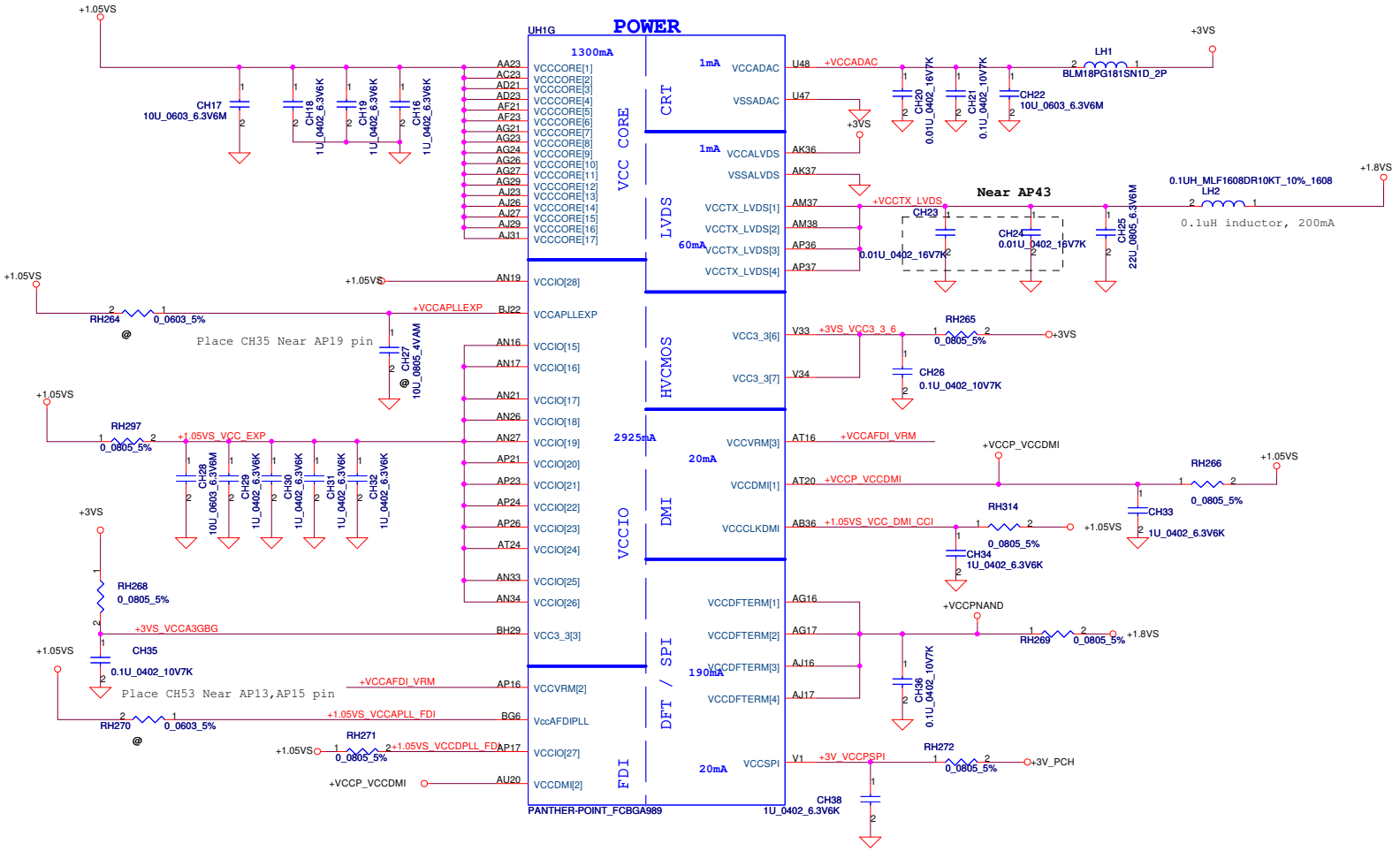
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

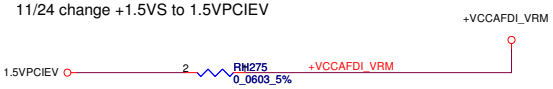
Size	Document Number	Rev
	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 17 of 57



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

11/24 change +1.5VS to 1.5VPCIEV



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.		
Title: PCH (6/8) PWR		
Size	Document Number: LA-8711	Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 18 of 57	

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

UH1J

PANTHER-POINT_FCBGA989

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA

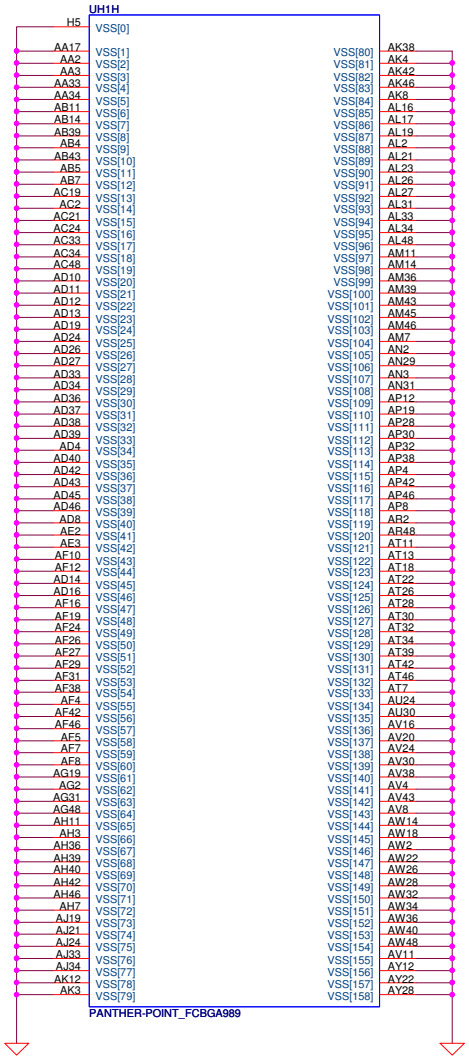
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

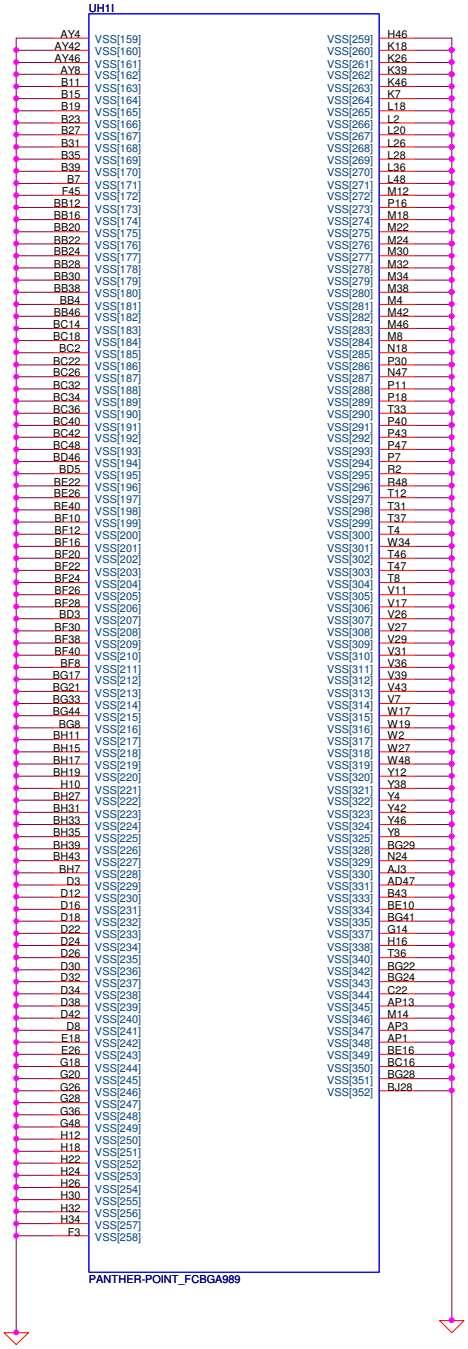
Compal Electronics, Inc.

Title: PCH (7/8) PWR

Size: | Document Number: LA-8711 | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 19 of 57





Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

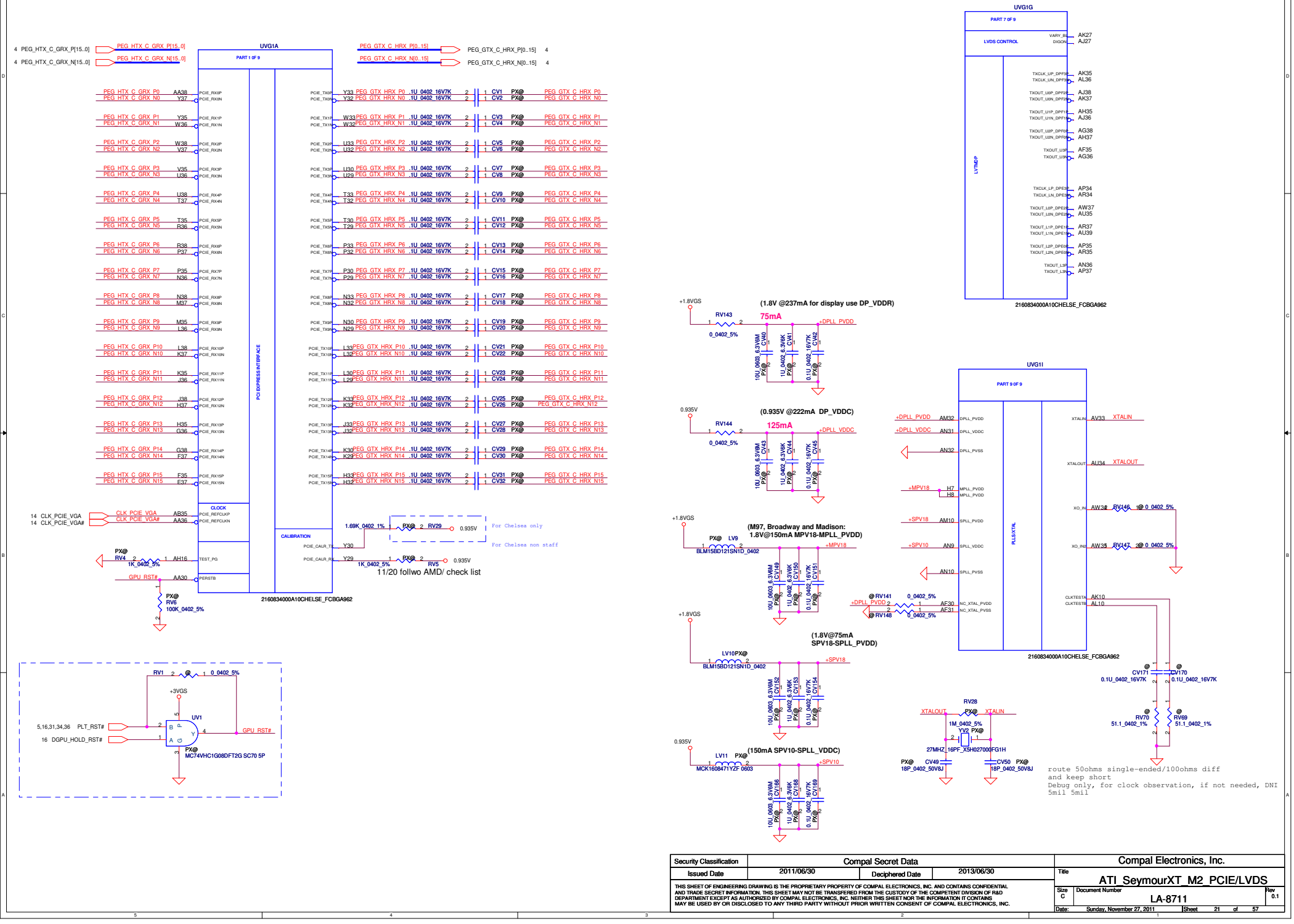
Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 20 of 57

LVDS Interface



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.			
Title: ATI_SeymourXT_M2_PCIE/LVDS			
Size: C	Document Number: LA-8711		Rev: 0.1
Date: Sunday, November 27, 2011		Sheet 21 of 57	

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS <all internal PD>	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE TRANSMITTER Power Saving Enable 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	Internal use only.This Pad has an internal PD and Must be 0V at reset. The pad may be left unconnected.	0
RSVD	H2SYNC		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT GPIO13,12,11(config 2,1,0): internal PD. a)If BIOS_ROM_EN=1,the config[2:0] defines the ROM type. b)If BIOS_ROM_EN=0,the config[2:0] defines the primary aperture size Memory apertures config[3:0] 128MB 000 256MB 001 64MB 010	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defalit setting for desktop)

STRAPS

RV9 SMT-->@

Update net name

Internal VGA Thermal Sensor

Use Internal Thermal Sensor

External VGA Thermal Sensor: No stuff

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

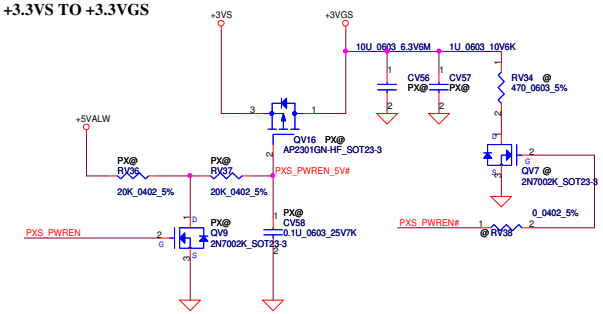
Compal Electronics, Inc.			
Title	ATI_SeymourXT_M2_Main_MSIC		
Size C	Document Number LA-8711		Rev 0.1
Date: Sunday, November 27, 2011		Sheet 22 of 57	

Name	FCH Pin Assignments
	Hudson-2 / Hudson-3
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192
PE_PWRGD	GPIO28

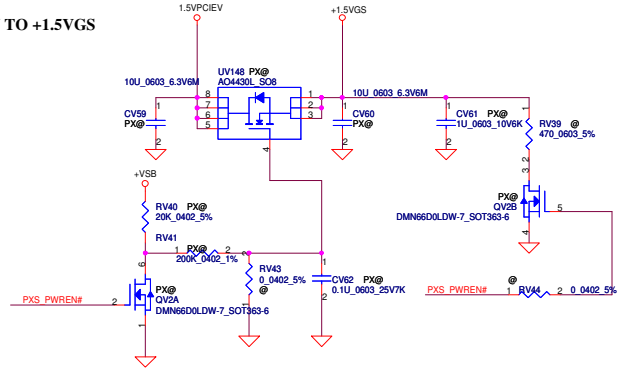
Chelsea Power Up

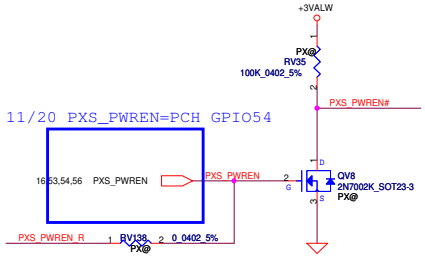
- +3VGS/+VGA_CORE
- 0,935V(VDDC)
- VDDCI
- +1.5VGS(VDDR1/MVDDQ)
- +1.8VS

+3.3VS TO +3.3VGS

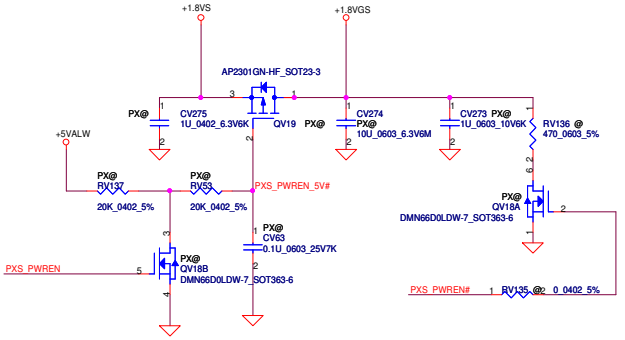


+1.5V TO +1.5VGS





+1.8VS TO +1.8VGS



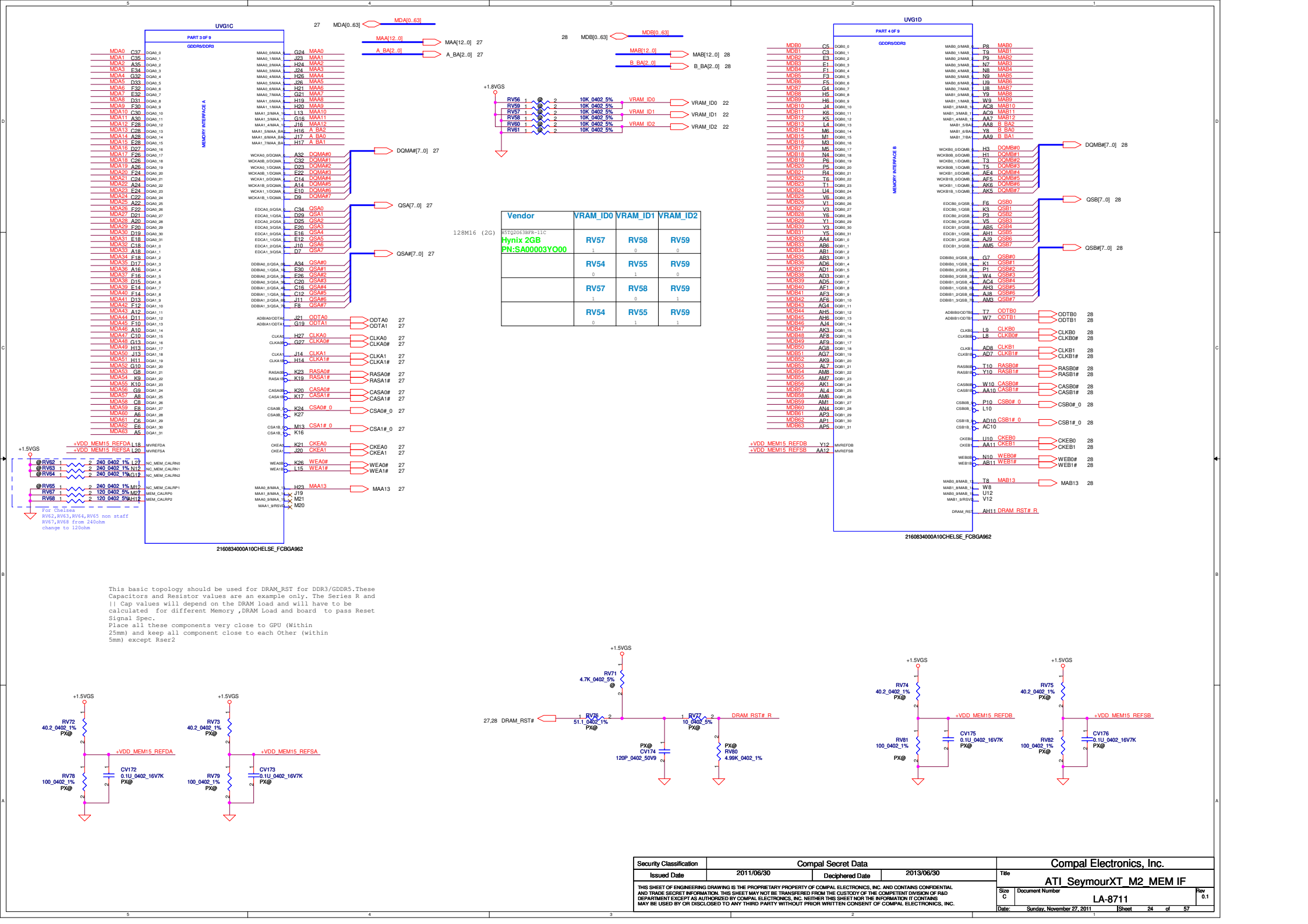
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_BACO POWER

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 23 of 57



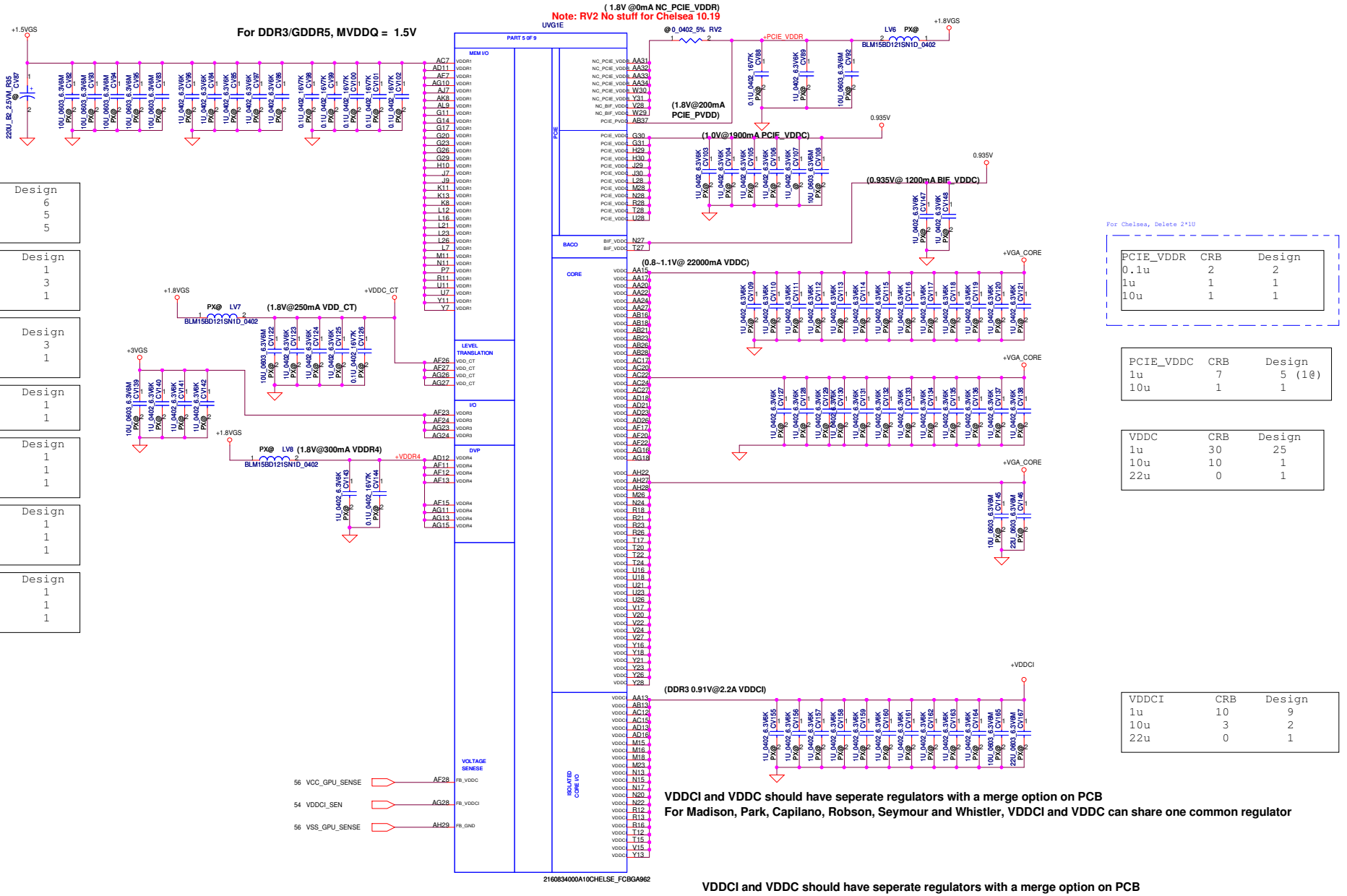
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 24 of 57



VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

For Chelsea, Delete 2*1U

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	1	1
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

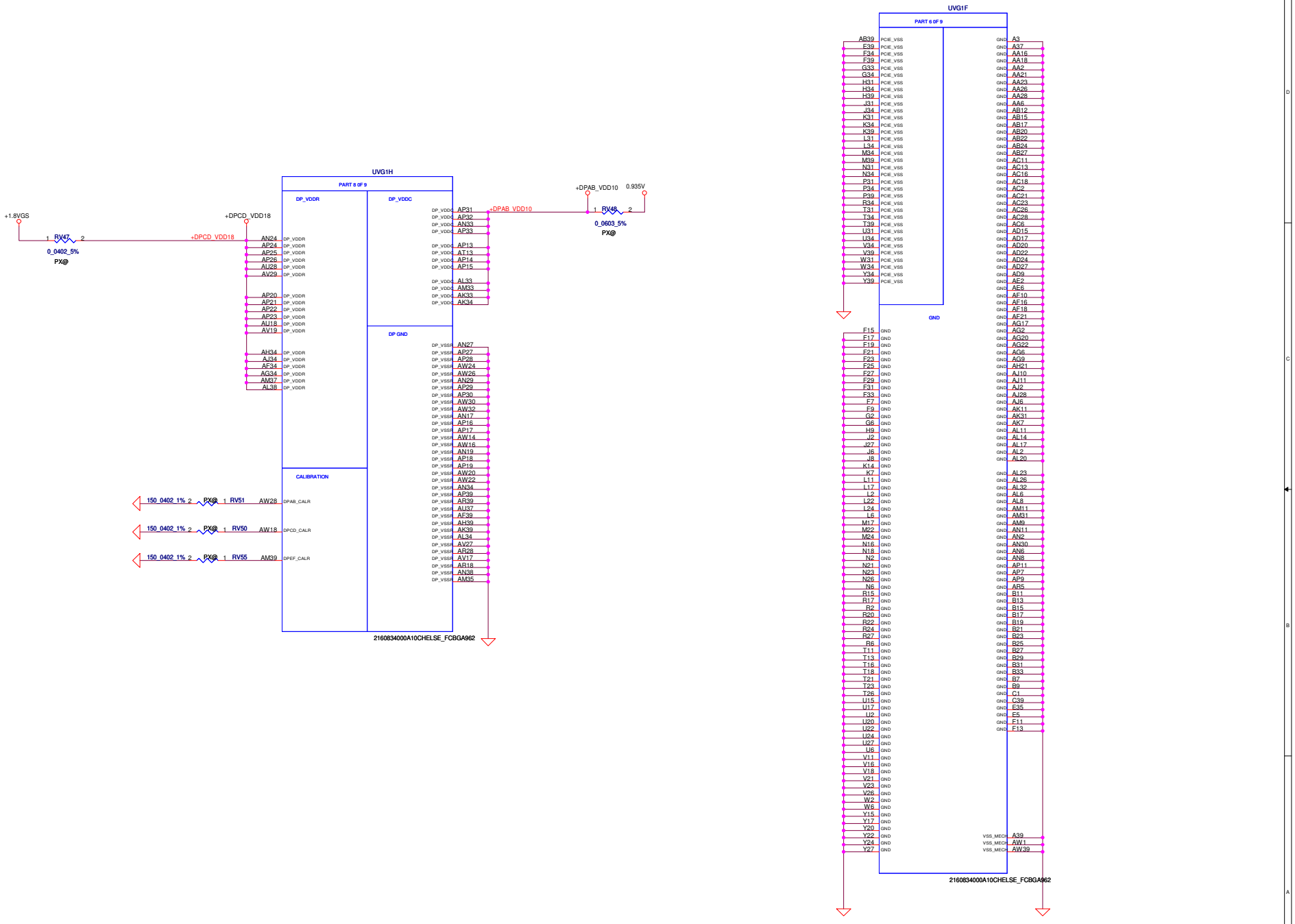
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 25 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SetmourXT_M2_PWR_GND

Size	Document Number	Rev
C	LA-8711	0.1

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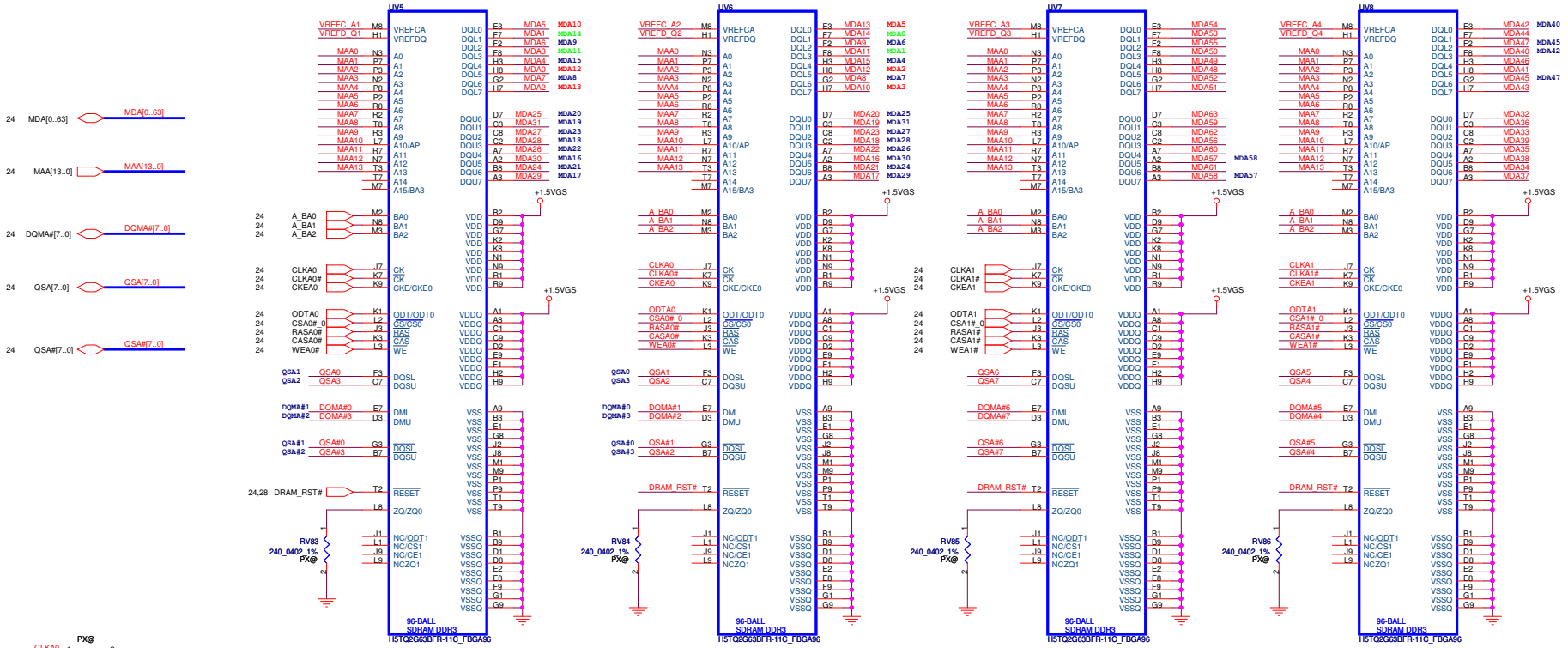
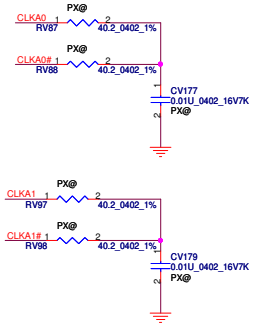
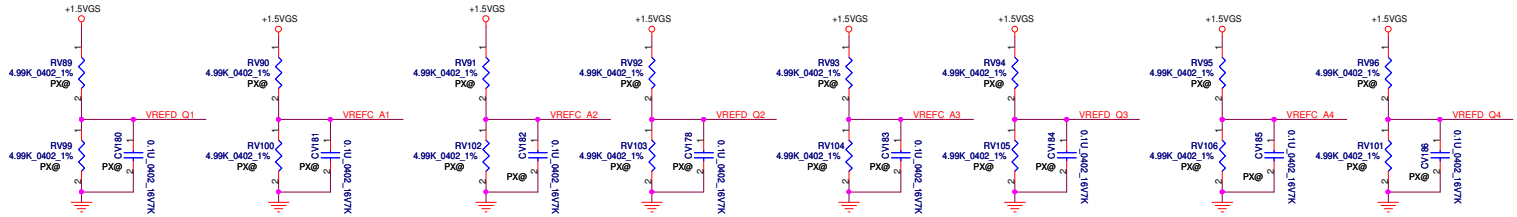
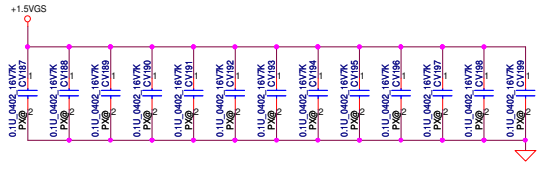
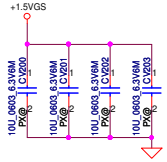
11/25 swap UV5.F8/ UV5.H8 =>MDA3/MDA0

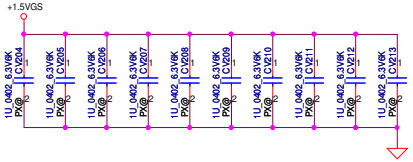


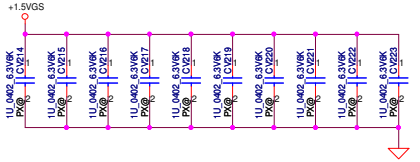












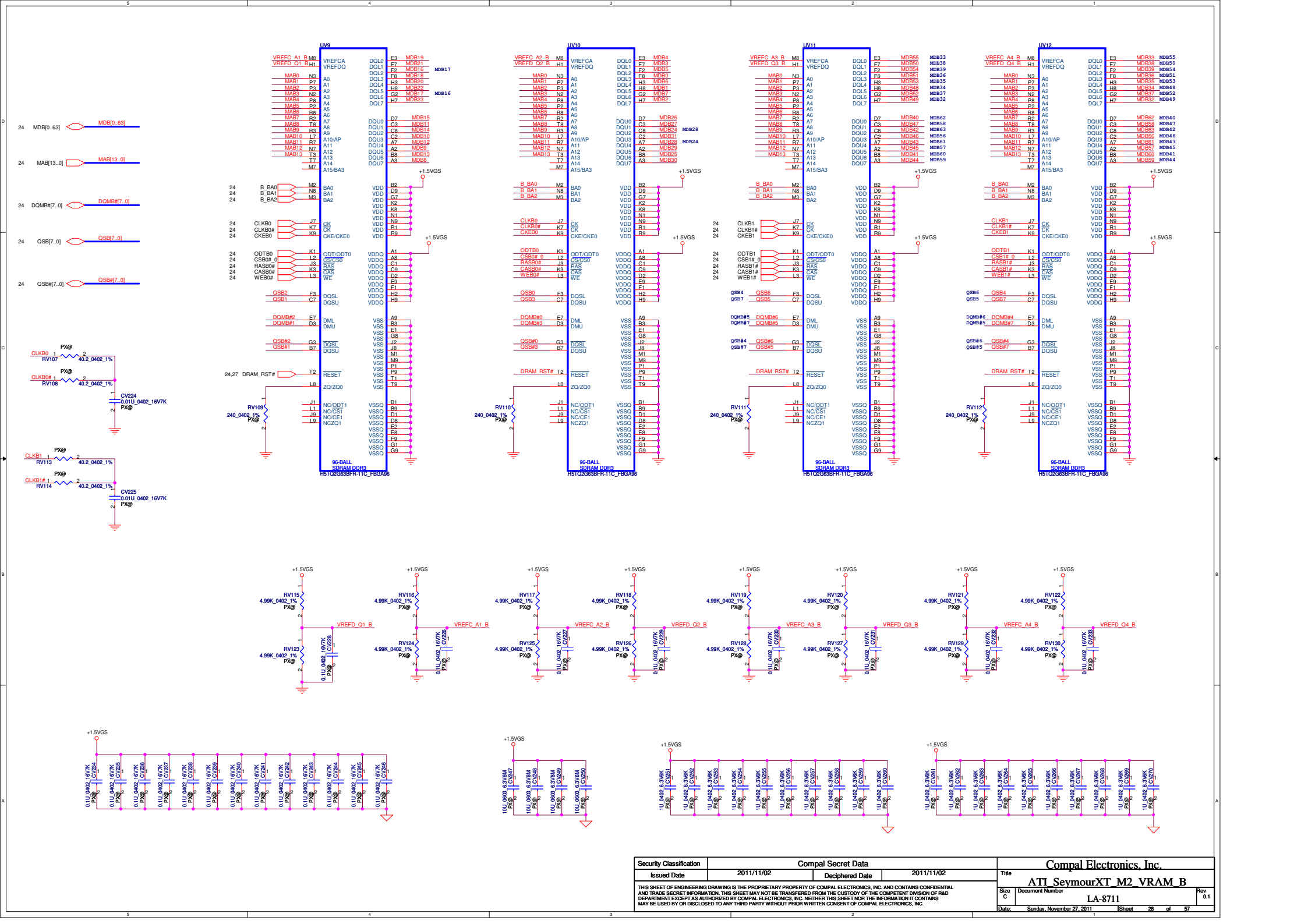
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 27 of 57



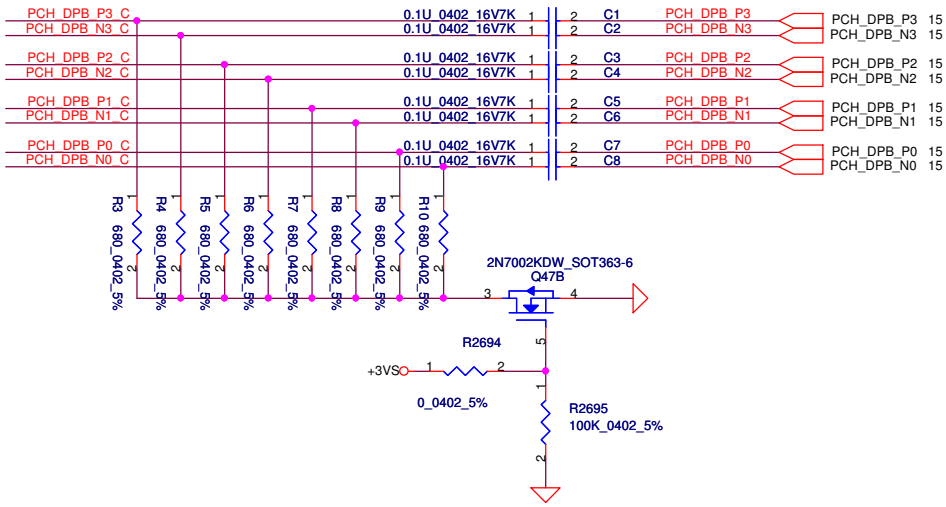
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

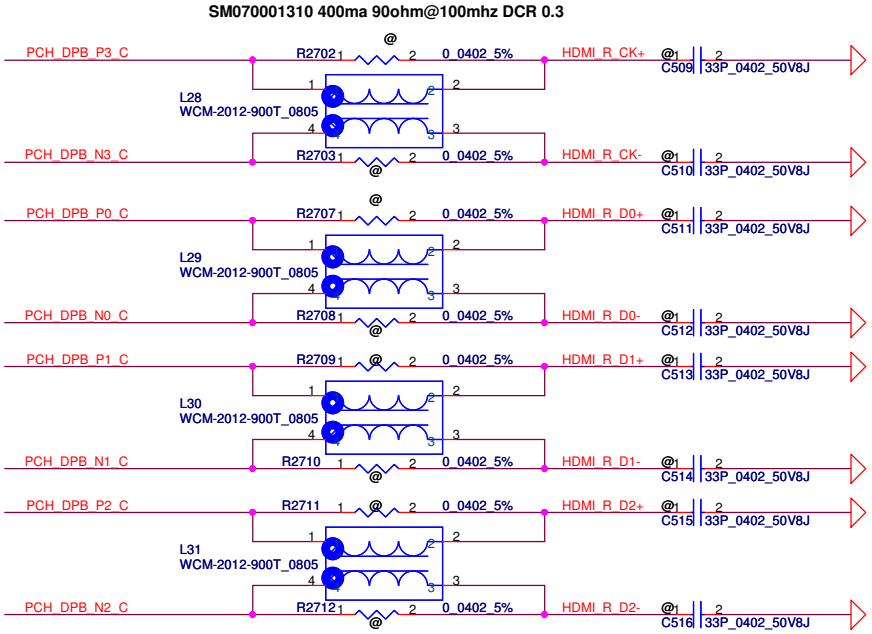
Compal Electronics, Inc.

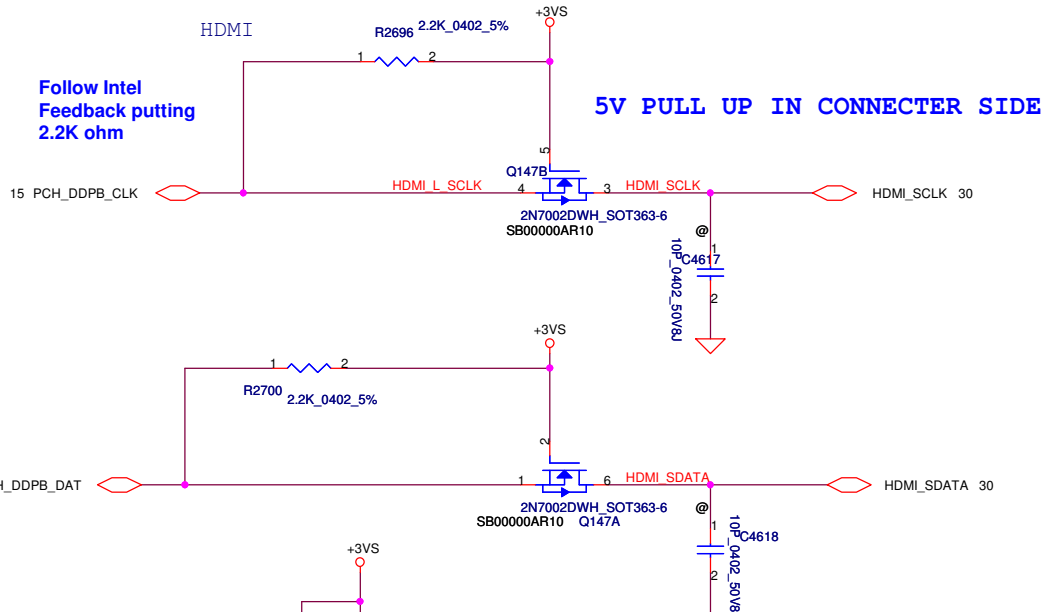
Title: ATI_SeymourXT_M2_VRAM_B

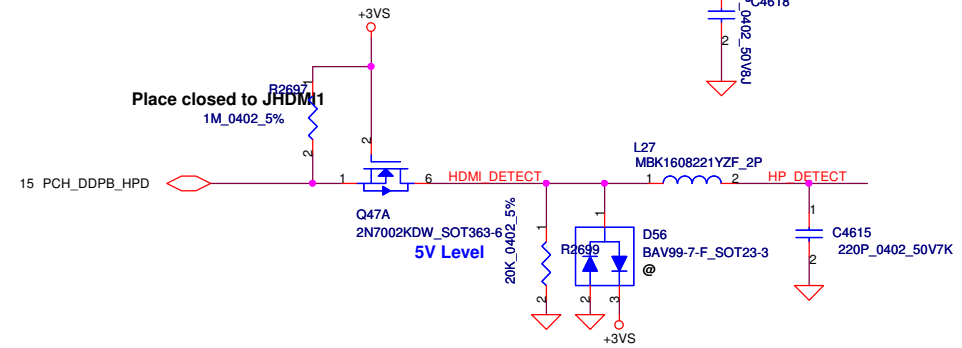
Size	Document Number	Rev
C	LA-8711	0.1

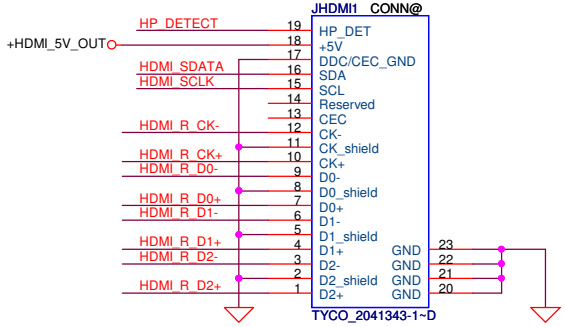
Date: Sunday, November 27, 2011 | Sheet 28 of 57







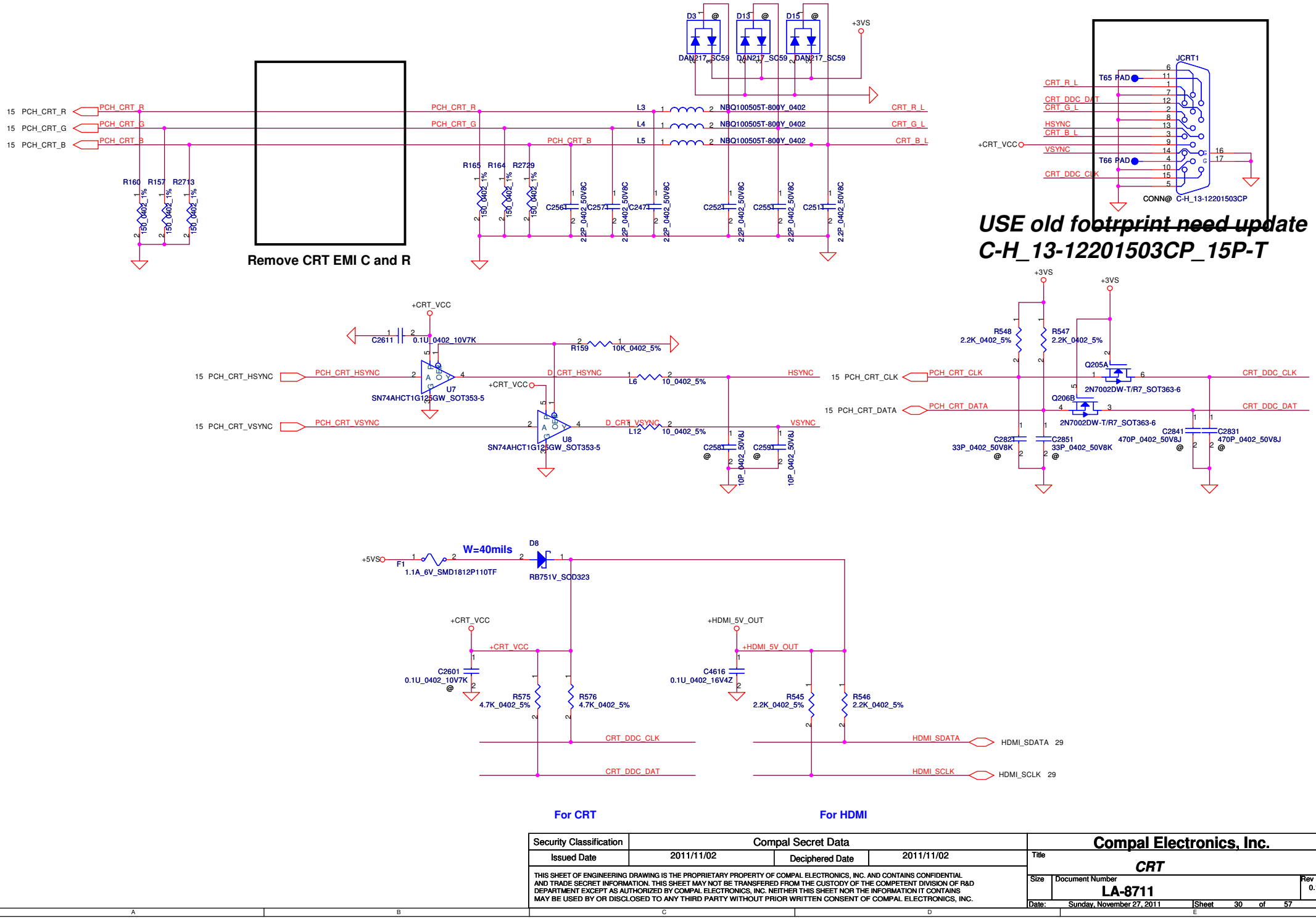




Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.			
Title: HDMI Conn			
Size	Document Number: LA-8711		Rev: 0.1
Date: Sunday, November 27, 2011		Sheet 29 of 57	

CRT CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: **CRT**

Size	Document Number	Rev
	LA-8711	0.1

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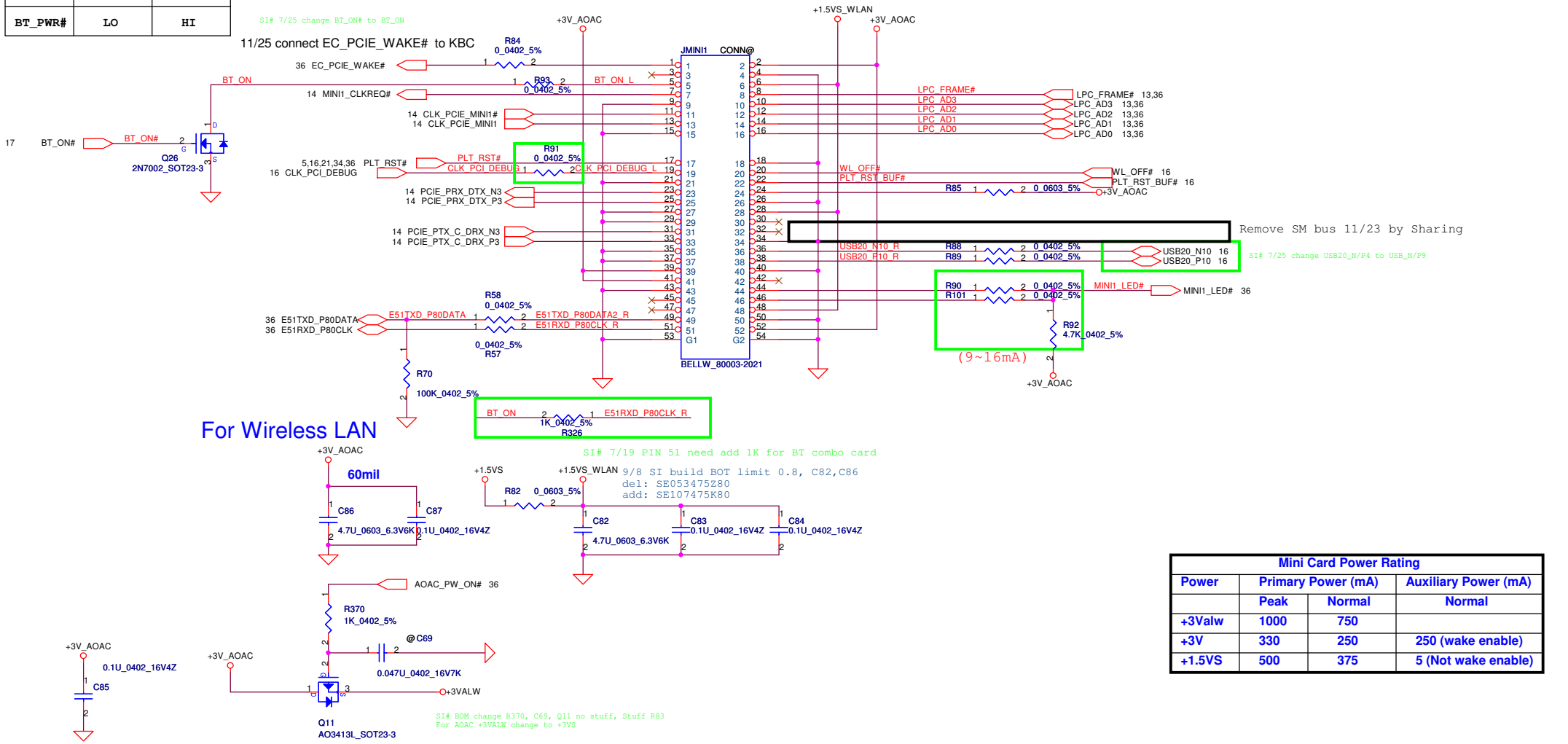
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

WLAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3Valw	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.	
Title	MiniCard & WLan
Size	Document Number: LA-8711
Rev	0.1
Date:	Sunday, November 27, 2011
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SI# 8/15 R62 change to +3VALW, R61change to 10 ohm, R63 change to 200K ohm

LCD POWER CIRCUIT

+LCDVDD
R61 30_0603_5%
+3VALW
R62 100K_0402_5%
R63 200K_0402_5%
0.1U_0402_16V7K
C55
+3VS
W=60mils
Q7 AO3413L_SOT23-3
Q6A DMN66D0LDW-7_SOT363-6
0.01U_0402_25V7K C61
+LCDVDD
W=60mils
C62 4.7U_0603_6.3V6K
C63 0.1U_0402_16V4Z
15 PCH_ENVDD
PCH_ENVDD
Q6B DMN66D0LDW-7_SOT363-6

9/8 SI build BOT limit 0.8, C62
del: SE053475Z80
add: SE107475K80

Place closed to JLVDS1
+3VS
+LCDVDD
C56 0.1U_0402_16V4Z
C57 10U_0603_6.3V6M
C58 0.1U_0402_16V4Z

+3VS
R64 2.2K_0402_5% LCD_CLK
R65 2.2K_0402_5% LCD_DATA
@C64 10P_0402_50V8J
@C65 10P_0402_50V8J
C66 220P_0402_50V7K INVTPWM
C67 220P_0402_50V7K DISPOFF#

INVPWR_B+
W=60mils
L7 FBMA-L11-201209-221LMA30T_0805
L8 FBMA-L11-201209-221LMA30T_0805
B+
C59 680P_0402_50V7K
C60 68P_0402_50V8J
SM010014520 3000ma
220ohm@100mhz
DCR 0.04

LCD/LED PANEL Conn.

W=60mils W=60mils

Check pin definition.

11/23 remove INVT_PWM

15 DPST_PWM
R197 0_0402_5%
INVTPWM
@ R72 10K_0402_5%

36 BKOFF#
BKOFF# R76 33_0402_5% DISPOFF#
R74 10K_0402_5%

15 PCH_LCD_CLK
PCH_LCD_CLK R193 0_0402_5% LCD_CLK
15 PCH_LCD_DATA
R194 0_0402_5% LCD_DATA

@
R156 0_0402_5%
L11
16 USB20_P8
USB20_P8_R
16 USB20_N8
USB20_N8_R
WCM-2012-900T_4P
@ R229 0_0402_5%
8/19 change stuff L26 by EMI request

D55
D_MIC_CLK
D_MIC_DATA
PESD5V0U2BT
@
6/27 Add ESD solution

+LCDVDD
JLVDS1
LCD_CLK
LCD_DATA
15 PCH_TXOUT0+
15 PCH_TXOUT0-
15 PCH_TXOUT1+
15 PCH_TXOUT1-
15 PCH_TXOUT2+
15 PCH_TXOUT2-
15 PCH_TXCLK+
15 PCH_TXCLK-
USB20_N8_R
USB20_P8_R
DISPOFF#
INVTPWM
INVPWR_B+
+3VS
D_MIC_CLK
D_MIC_DATA
GND
STARC_111H30-000000-G4-R
CONN@

38 D_MIC_CLK_L_C
38 D_MIC_DATA_C
D_MIC_CLK_L_C
D_MIC_DATA_C
100_0402_5%
RA13
D_MIC_CLK_L
LA19 FBMA-L10-160808-301LMT_2P
D_MIC_CLK
LA20 FBMA-L10-160808-301LMT_2P
D_MIC_DATA

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

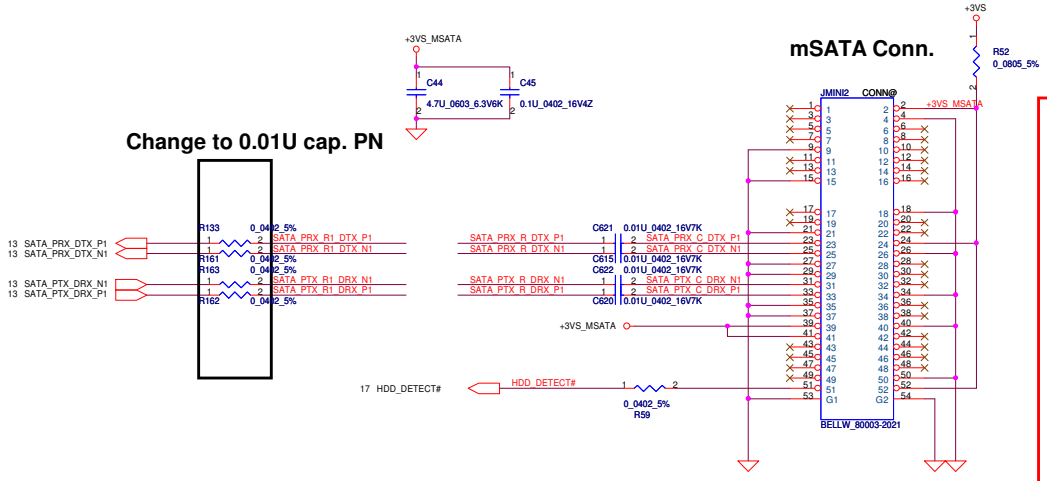
Title: LVDS Connector

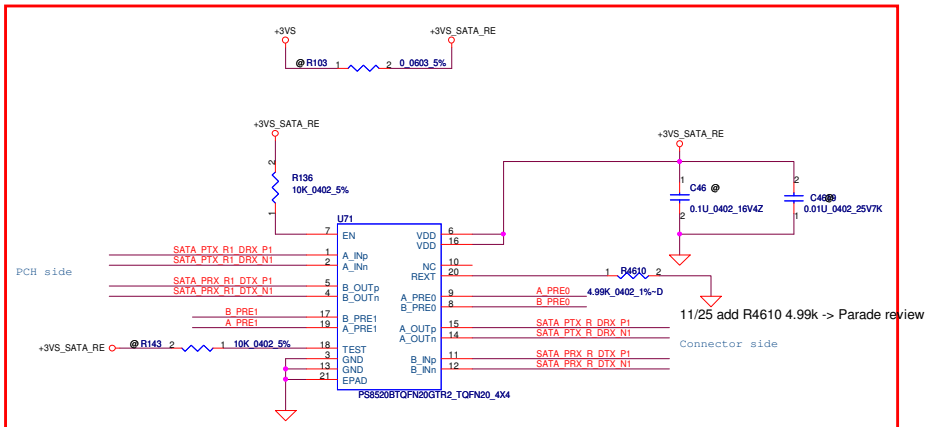
Size	Document Number	Rev
	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 32 of 57

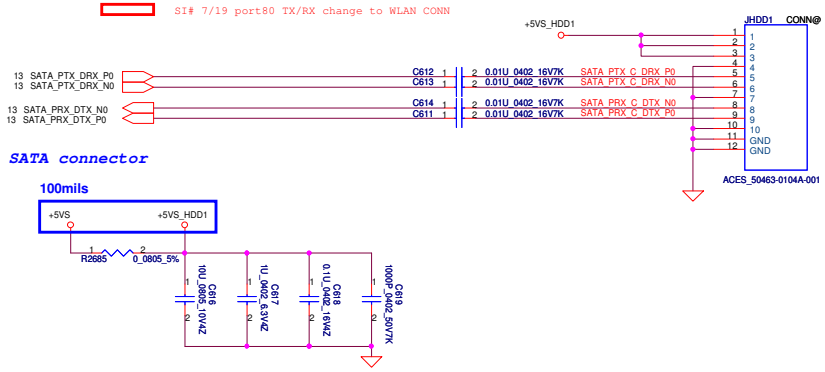
PV# 9/17 JMINI2/JMINI3 change footprint follow ME connector list

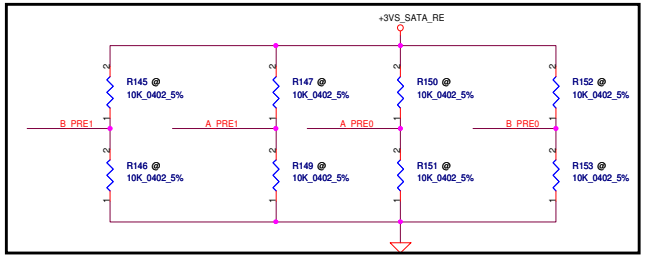
mSATA Conn.





SI# 7/19 port80 TX/RX change to WLAN CONN

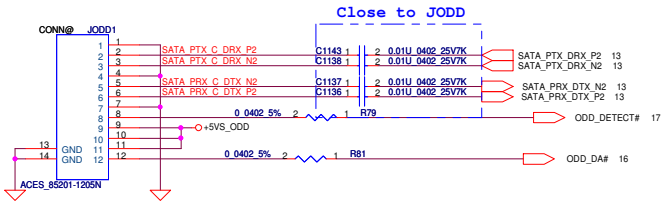




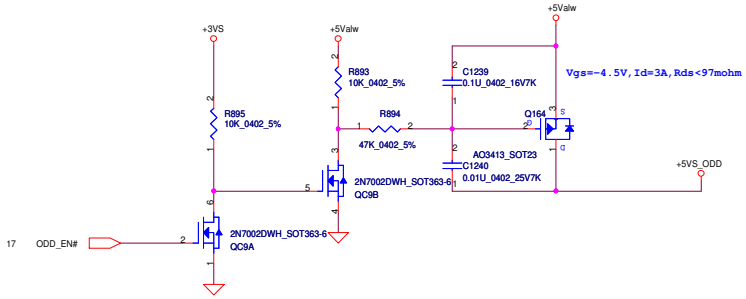
Need Vendor check value

Reserve SATA Redriver

SATA ODD Conn



Place components closely ODD CONN.
11/24 remove 22uF to sub board



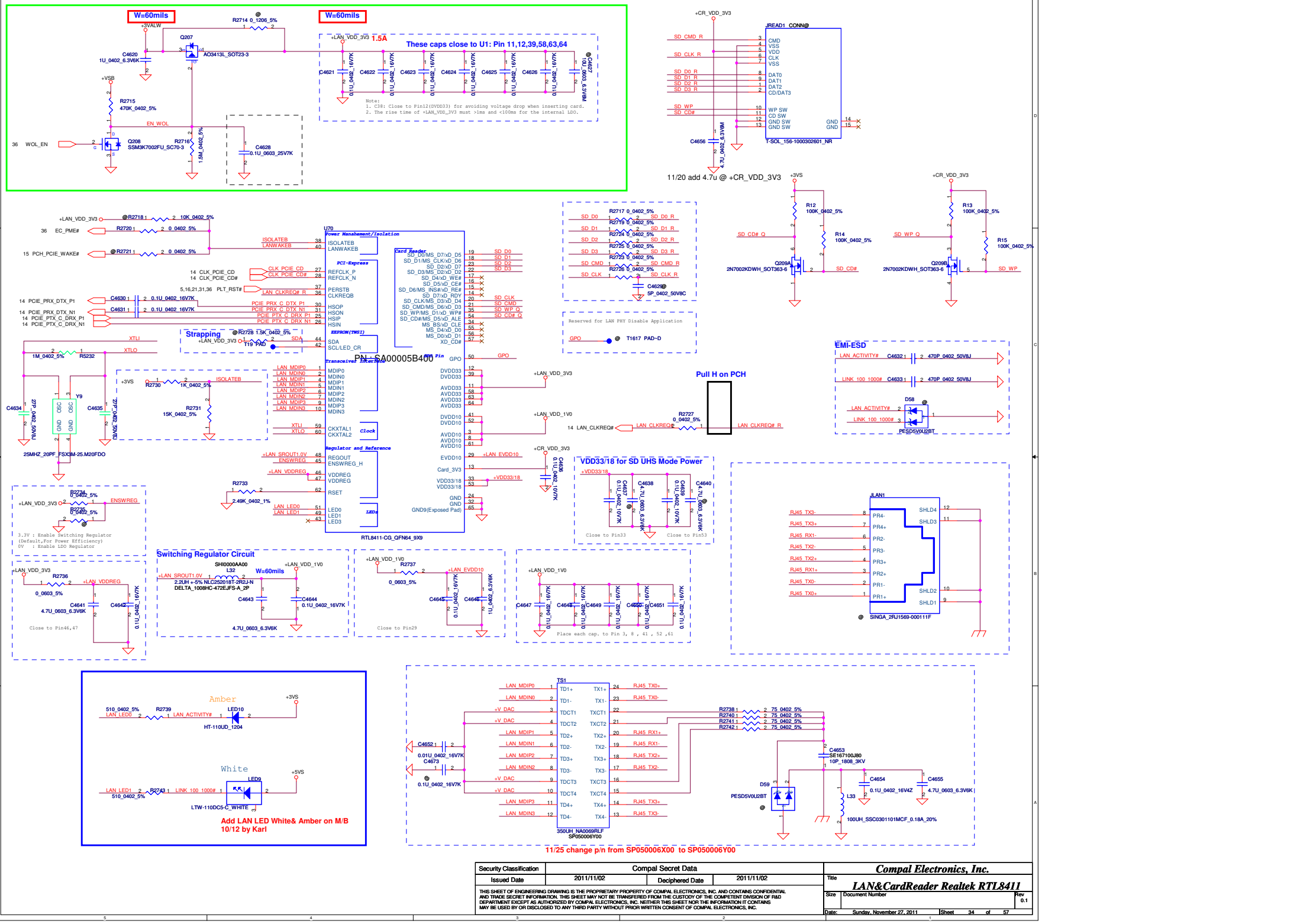
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: mSATA Connector

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 33 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

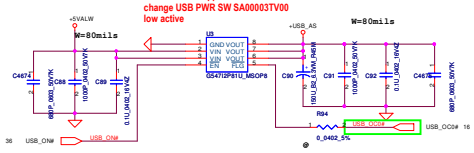
Title: LAN&CardReader Realtek RTL8411

Size	Document Number	Rev
		0.1

Date: Sunday, November 27, 2011 Sheet 34 of 57

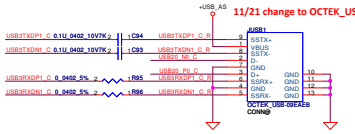
USB3.0

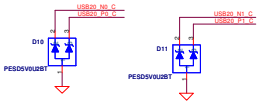
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active



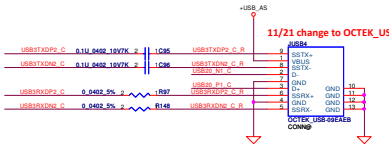
SI# 8/8 change USB_OC0# to USB30_OC#

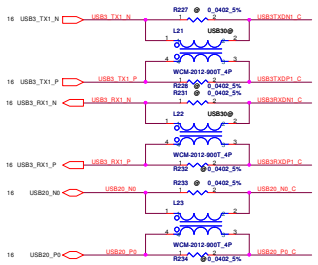
11/21 change to OCTEK_USB-09EAEB

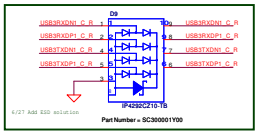


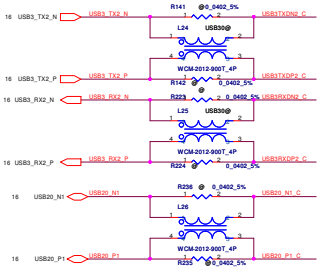


11/21 change to OCTEK_USB-09EAEB



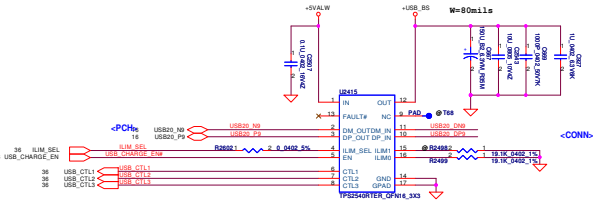




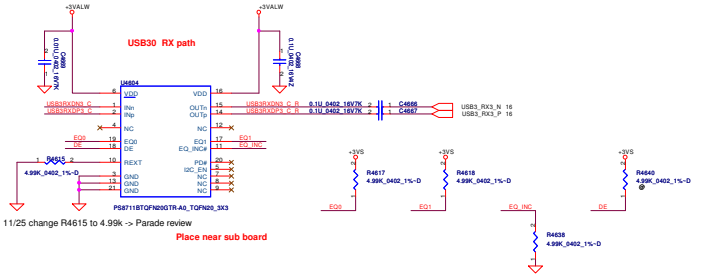


USB2.0 charger

USB charger footprint need change to TPS2543



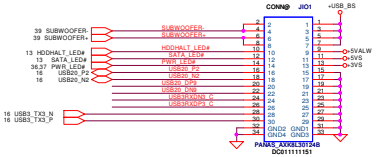
State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	X	1	0	0	1	1



11/25 change R4615 to 4.99k -> Parade review

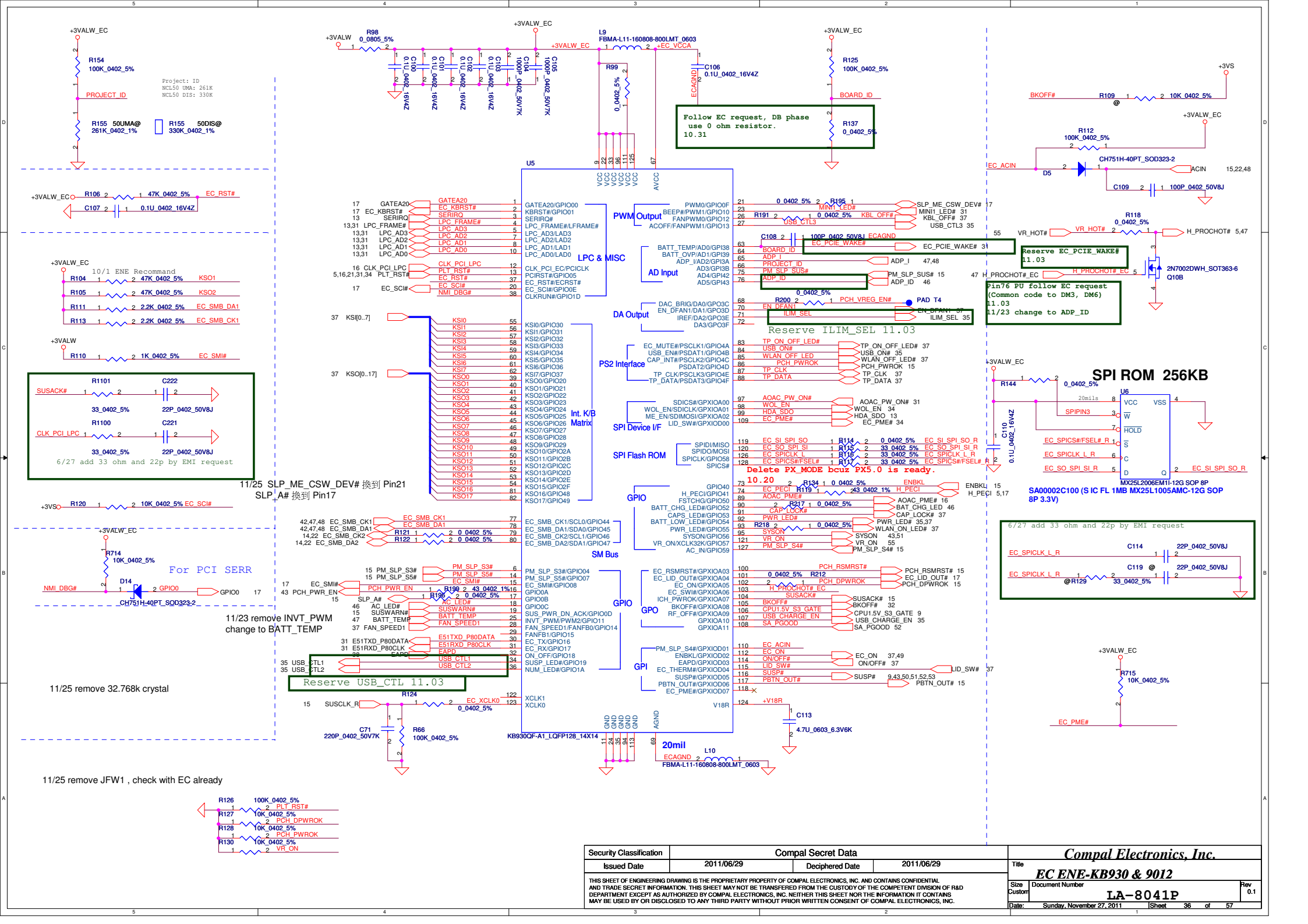
Place near sub board

11/21 follow AMD change to 30 pin



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.			
Title: USB Con & Daughter Con			
Size: D	Document Number: LA-8041P		Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 35 of 57		


U5
KB930QF-A1_LQFP128_14X14
Project: ID
NCL50 UMA: 261K
NCL50 DIS: 330K
Follow EC request, DB phase use 0 ohm resistor. 10.31
Reserve ILIM_SEL 11.03
Reserve USB_CTL 11.03
Reserve EC_PCIE_WAKE# 11.03
Pin76 PU follow EC request (Common code to DM3, DM6) 11.03 11/23 change to ADP_ID
Delete PX_MODE bcuz PX5.0 is ready. 10.20
SPI ROM 256KB
SA00002C100 (S IC FL 1MB MX25L1005AMC-12G SOP 8P 3.3V)
MX25L2006EM1I-12G SOP 8P
10/1 ENE Recommand
6/27 add 33 ohm and 22p by EMI request
11/25 SLP_ME_CSW_DEV# 換到 Pin21
SLP_A# 換到 Pin17
11/23 remove INVT_PWM change to BATT_TEMP
11/25 remove 32.768k crystal
11/25 remove JFW1 , check with EC already
PWM Output
LPC & MISC
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device I/F
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Security Classification
Compal Secret Data
Issued Date
2011/06/29
Deciphered Date
2011/06/29
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Title
EC ENE-KB930 & 9012
Size
Custom
Document Number
LA-8041P
Rev
0.1
Date:
Sunday, November 27, 2011
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36
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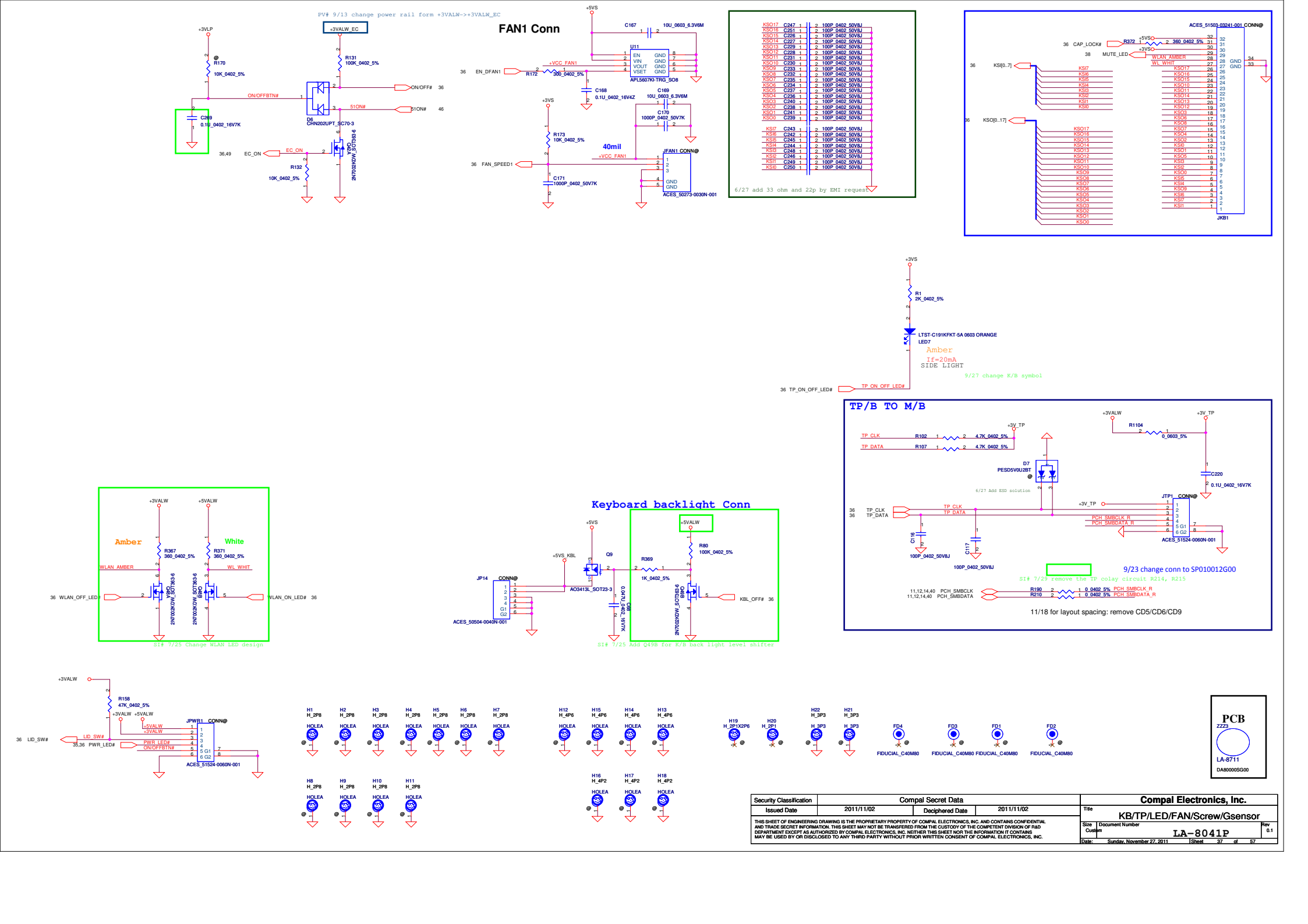
57



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: KB/TP/LED/FAN/Screw/Gsensor

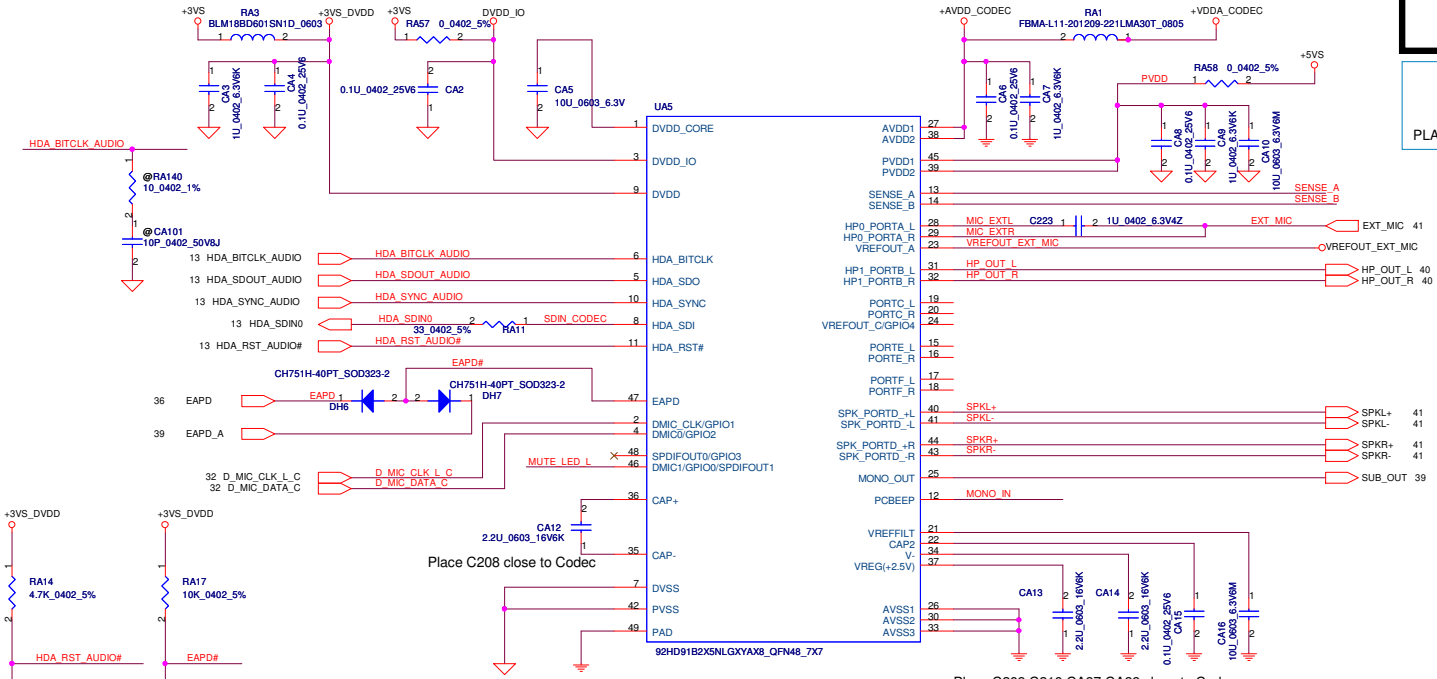
Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Sunday, November 27, 2011 | Sheet 37 of 57

DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Place AVDD ,PVDD,and DVDD capacitor close to Codec

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

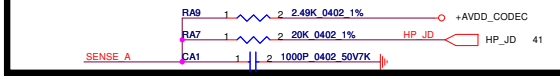


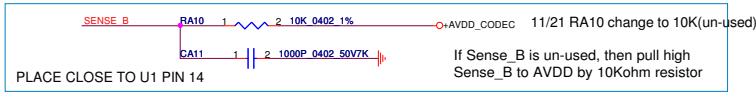
Place C208 close to Codec

Place C209,C210,CA87,CA89 close to Codec

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF





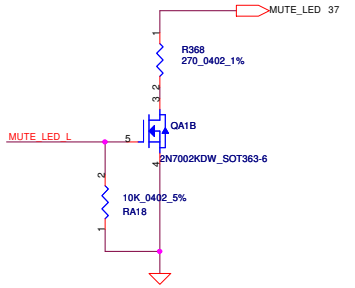
11/21 RA10 change to 10K(un-used)

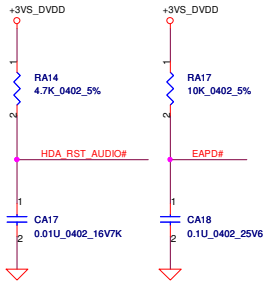
If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

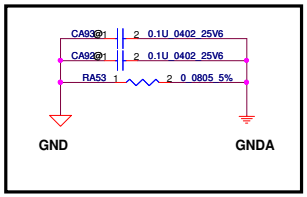
PLACE CLOSE TO U1 PIN 14

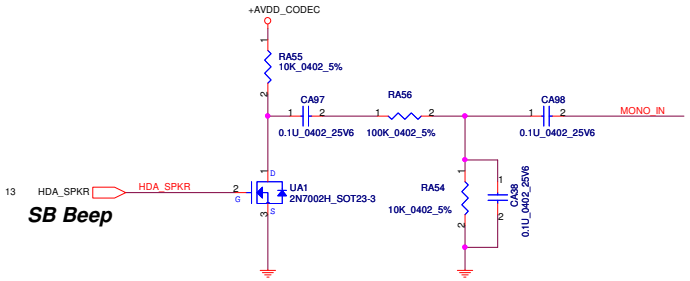
HP Jack
Ext MIC

Internal SPKR
(front stereo speaker)



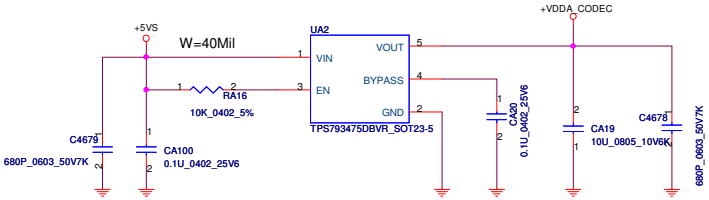






SB Beep

9/27 LDO TPS793475DBVR for audio power



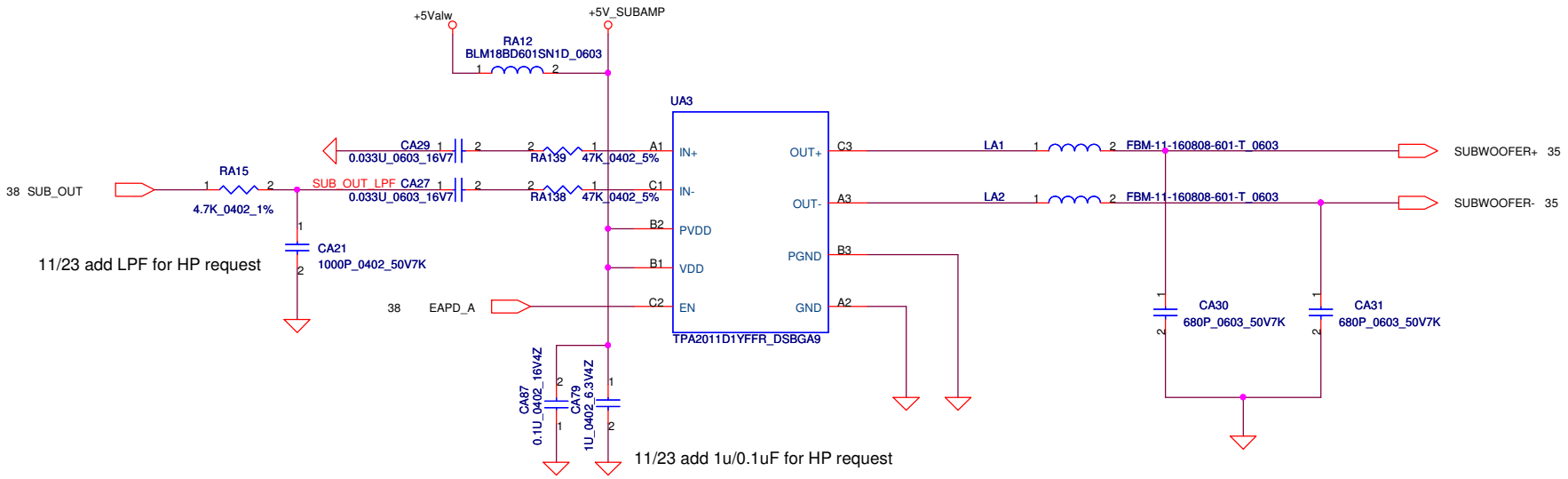
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: Audio IDT 92HD91

Size: Custom | Document Number | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 38 of 57



2011.10.28 Change Sub-woofer Amp to TPA2011D1

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

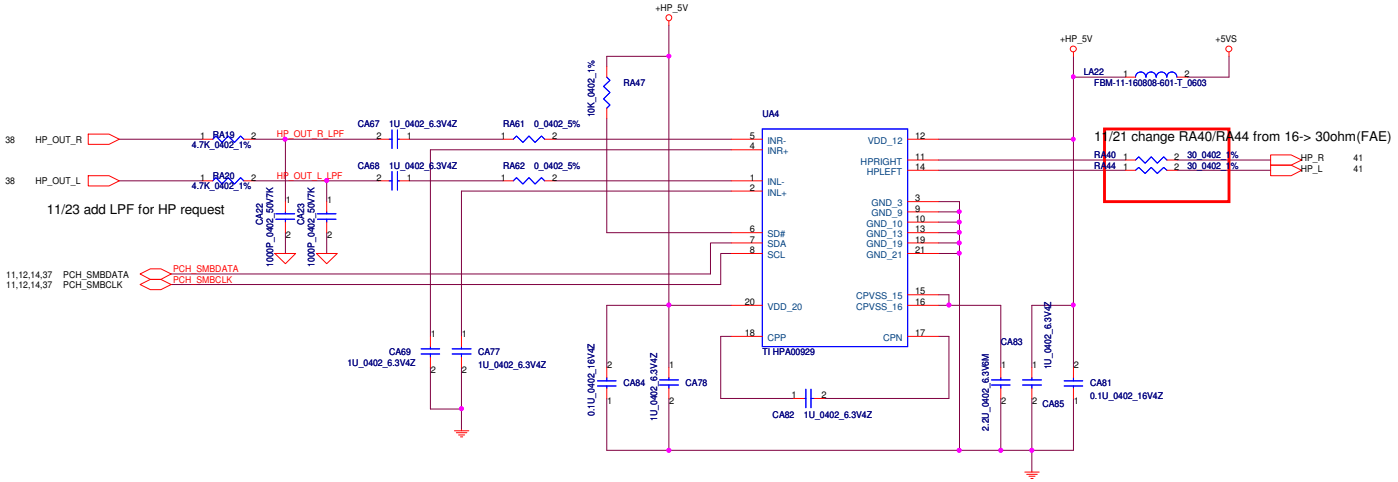
Compal Electronics, Inc.

Title: Audio Woofer Amplifier

Size	Document Number	Rev
B		0.1

Date: Sunday, November 27, 2011 Sheet 39 of 57

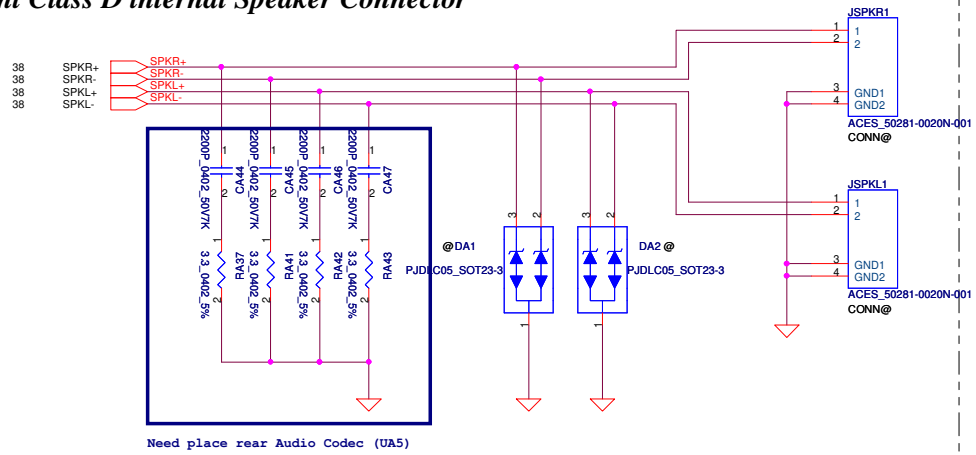
Headphone Amp

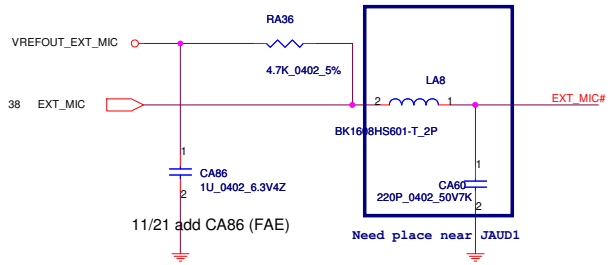


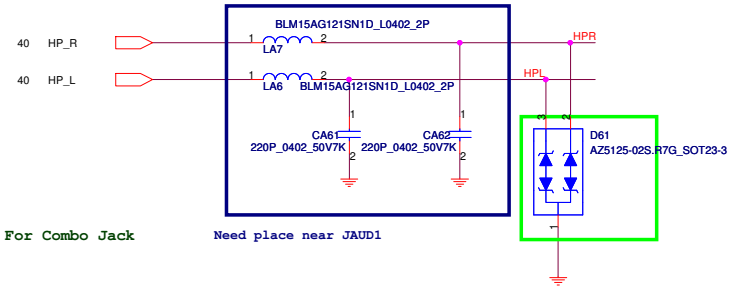
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/02	Deciphered Date 2011/11/02	Title: Audio SPK/HP Amplifier
Size: Custom	Document Number		Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 40 of 57		

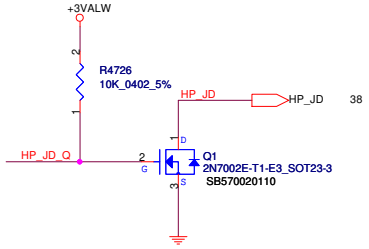
Front Class D internal Speaker Connector

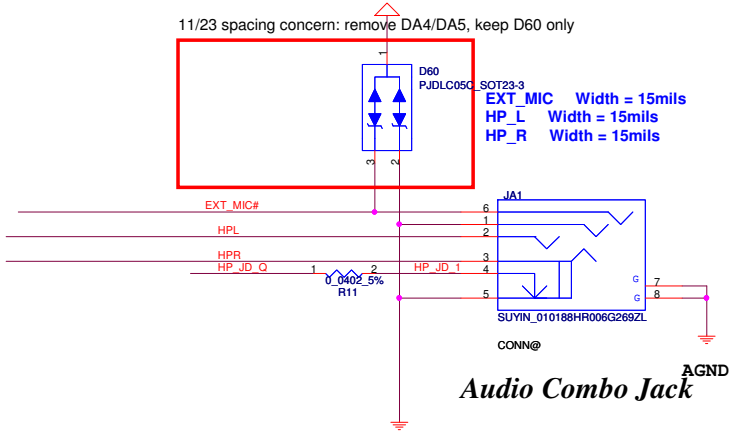
11/25 change SPKR connector follw AMD











Audio Combo Jack

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: Audio SPK Conn/Jack/MIC

Size	Document Number	Rev
Custom	LA-8711	0.1

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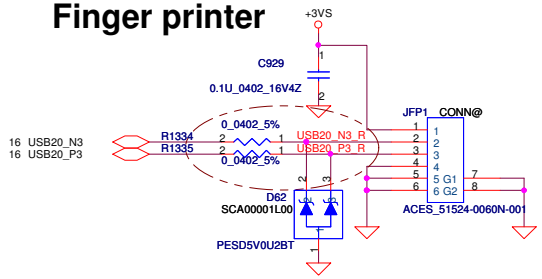
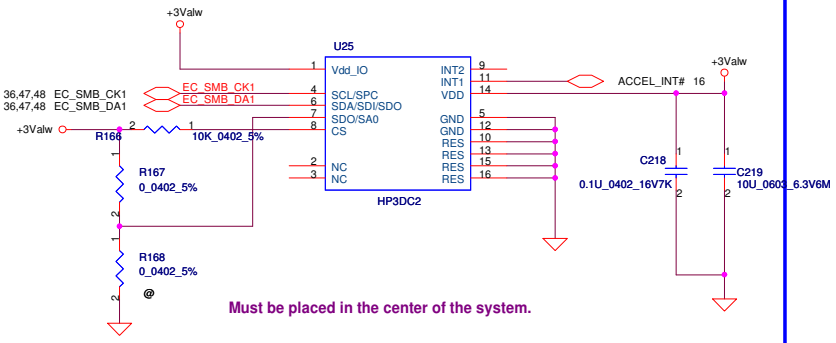
Finger printer



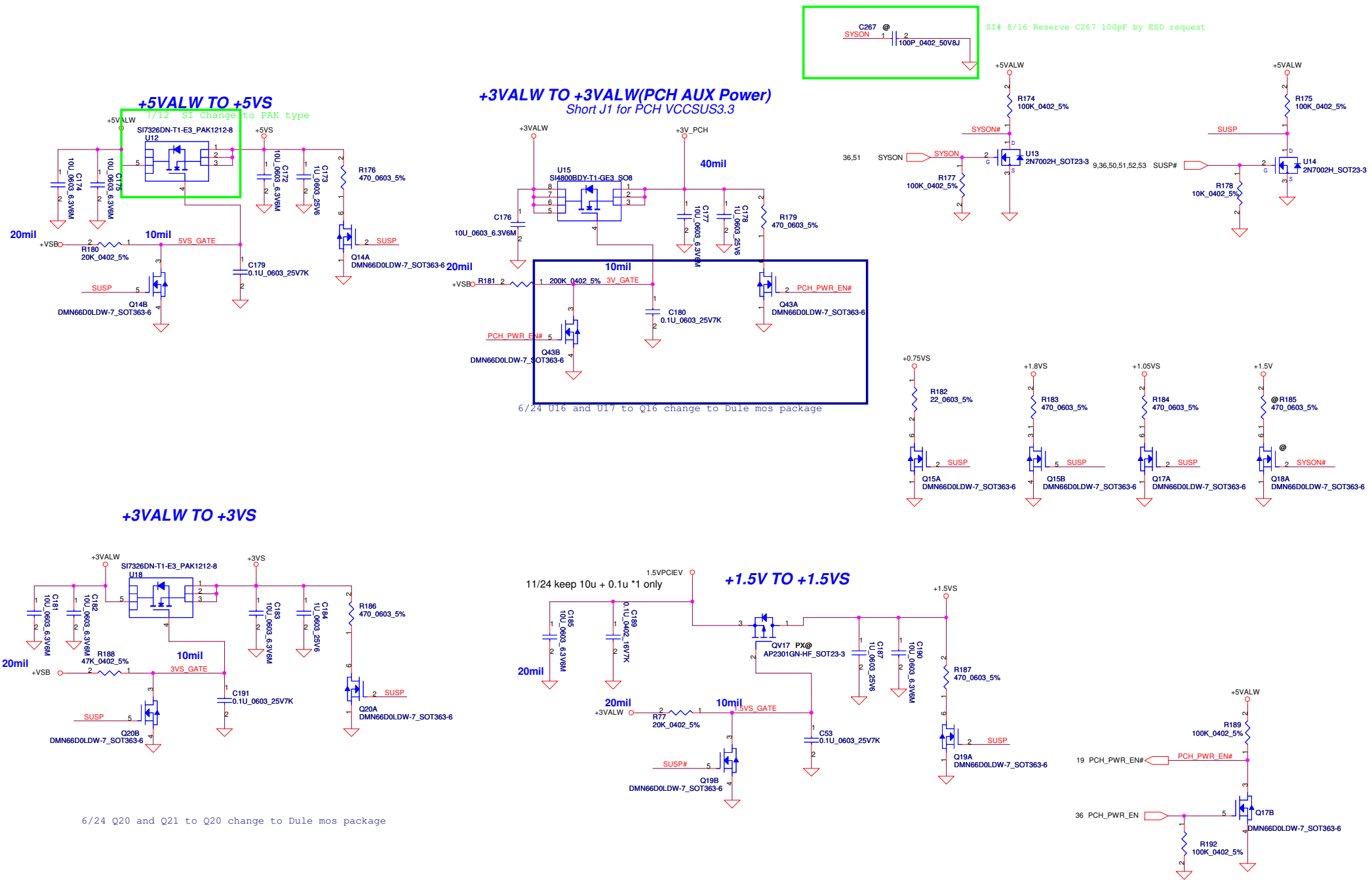
ACCELEROMETER



Must be placed in the center of the system.

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.			
Title: TCG/BIOS ROM/PS2/LED/SW			
Size	Document Number: LA-8711		Rev: 0.1
Date: Sunday, November 27, 2011		Sheet 42 of 57	



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title	DC Interface		
Size Custom	Document Number LA-8041P		Rev 0.1
Date: Sunday, November 27, 2011	Sheet 43 of 57		

QC11 (LA-8551P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	mSATA MINI2	TP	SODIMM	EC_SMB_CK2 PCH_SMBDATA	PCH_SMBCLK PCH_SMBDATA	G-Sensor	GPU	AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V							V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					V
PCH_SMLCLK PCH_SMLDATA	PCH						V			V	

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JMINI2
SATA1	m-SATA,JMINI1
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	
		1	USB/B (Right Side)
	UHCI1	2	
		3	
	UHCI2	4	
		5	m-SATA
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	

USB 3.0	Port	1 External USB Port
	0	
	1	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	USB3.0 FL1009-2Q0		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Option	@	CONN@	USB3.0@	
UMA	X	X	V	

Symbol Note :

: means Digital Ground

: means Analog Ground

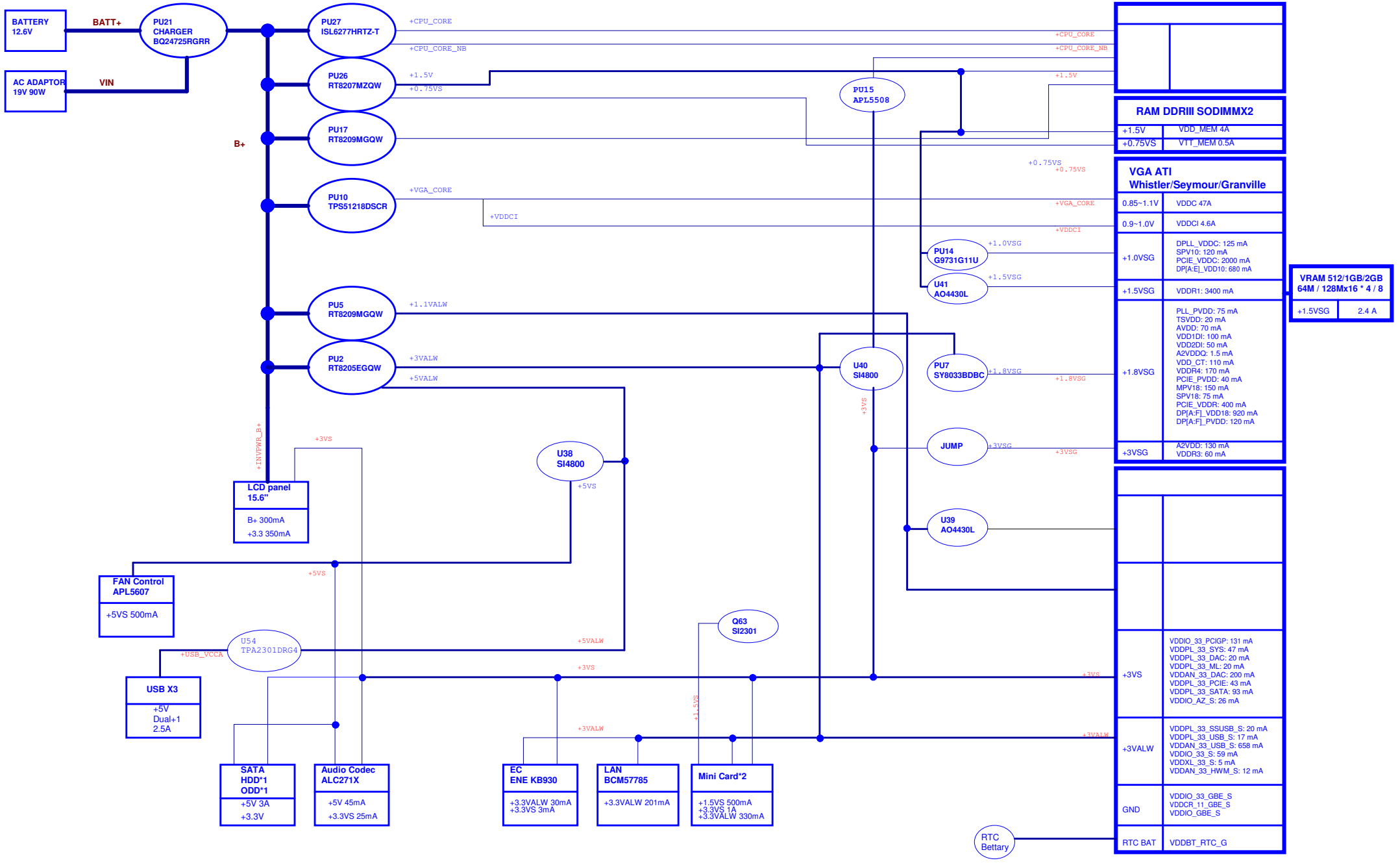
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: Notes List

Size: C | Document Number: LA-8711 | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 44 of 57

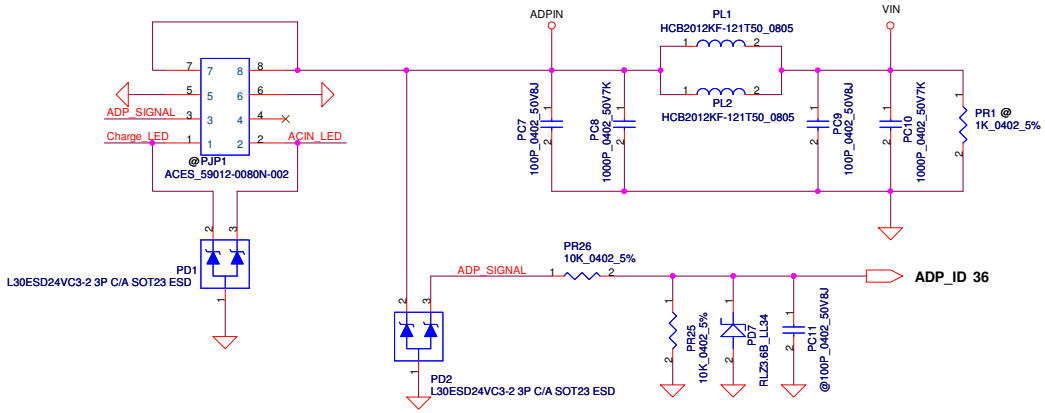


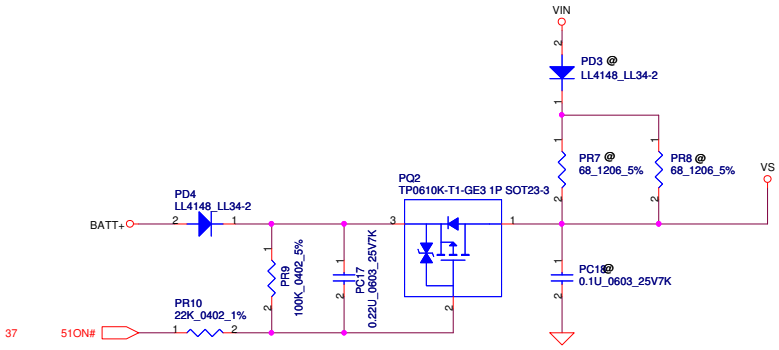
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

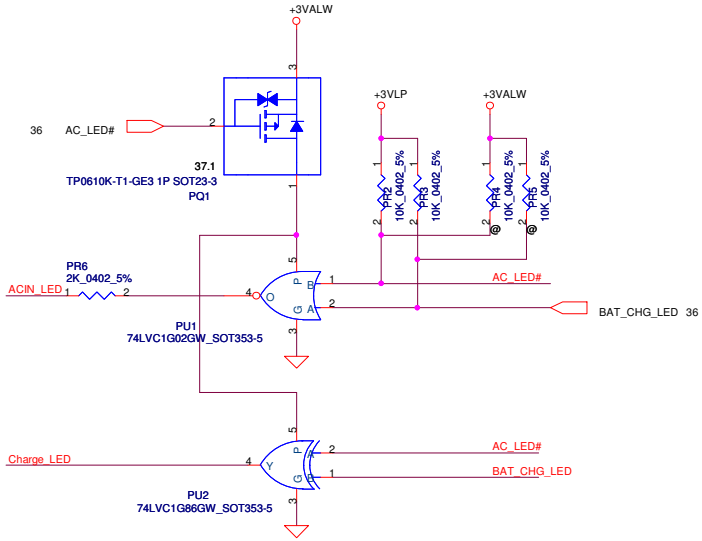
Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 45 of 57







Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR- DCIN / Vin Detector		
Size: Custom	Document Number: LA8711P		Rev: 0.1
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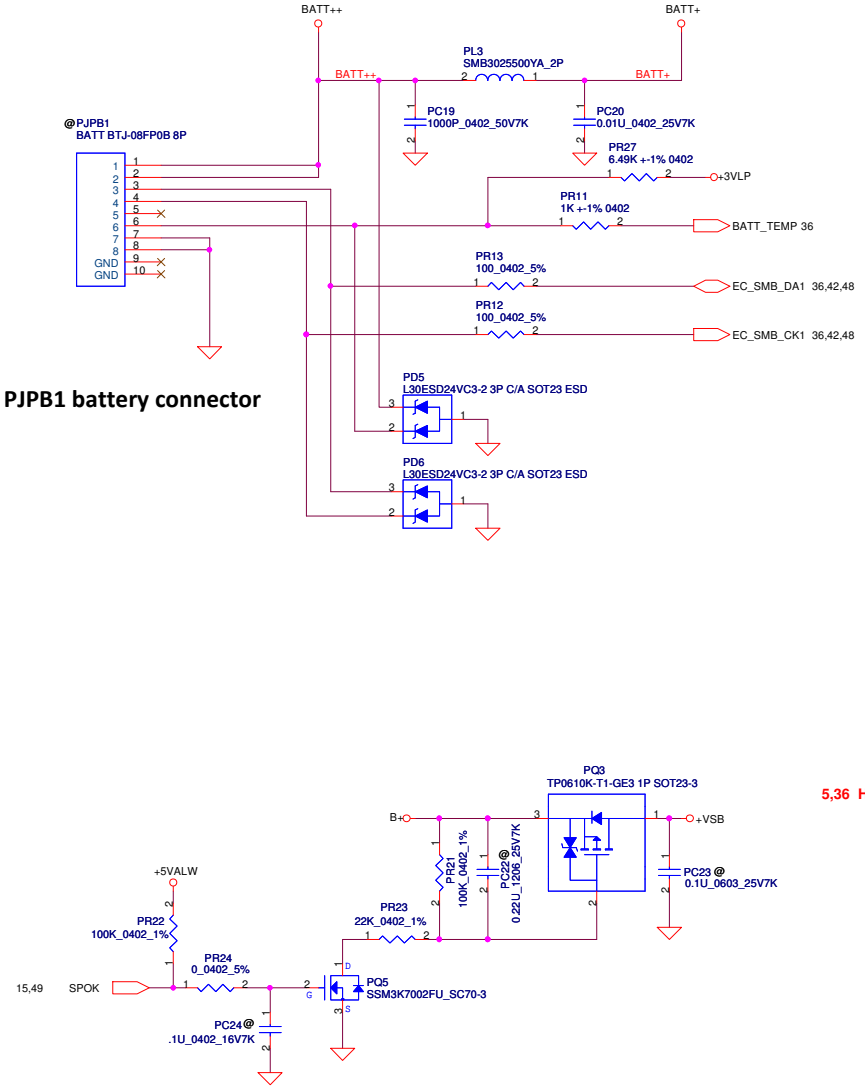


PJPB1 battery connector

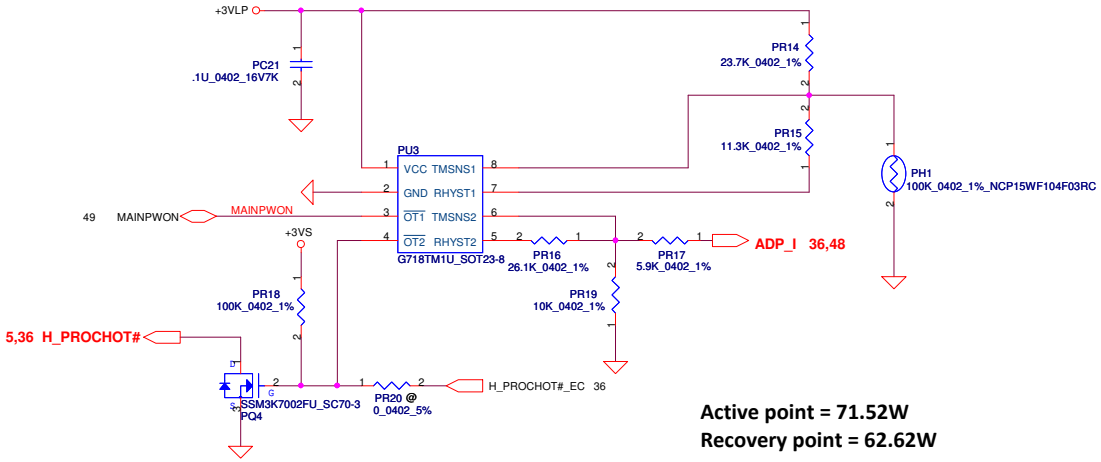
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 --> Remove PU1 circuit, but keep PR25
PH1, PR15, PQ3, PR17,PR18, PR16
VCIN0_PH-->NTC_V
VCIN1_PH-->Turbo_V

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 56 +-3 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



Active point = 71.52W
Recovery point = 62.62W

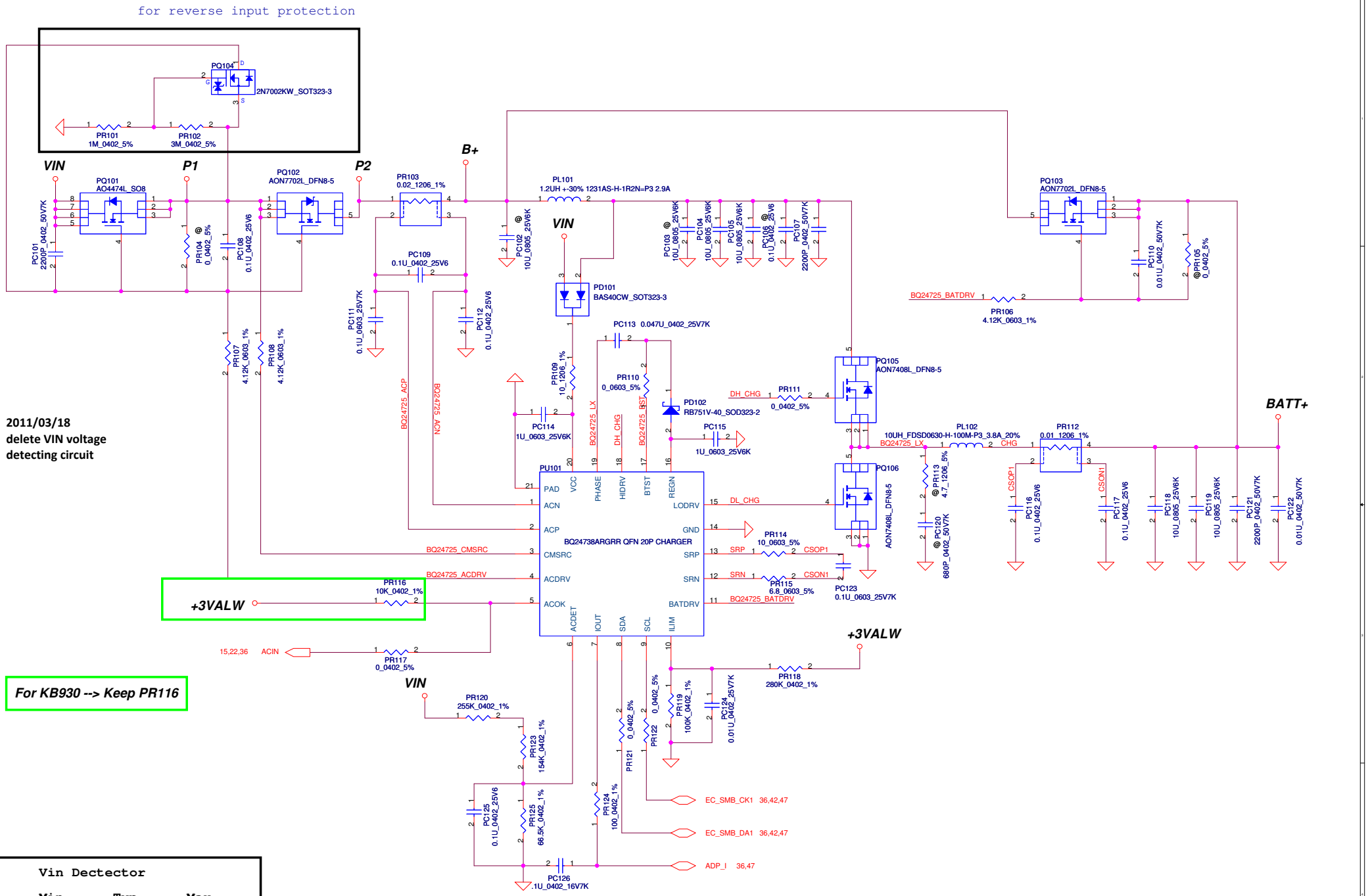
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- BATTERY CONN

Size: Custom | Document Number: LA8711P | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 47 of 57



2011/03/18
delete VIN voltage
detecting circuit

For KB930 --> Keep PR116

Vin Dectector

	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

ILIM and external DPM
4.36A

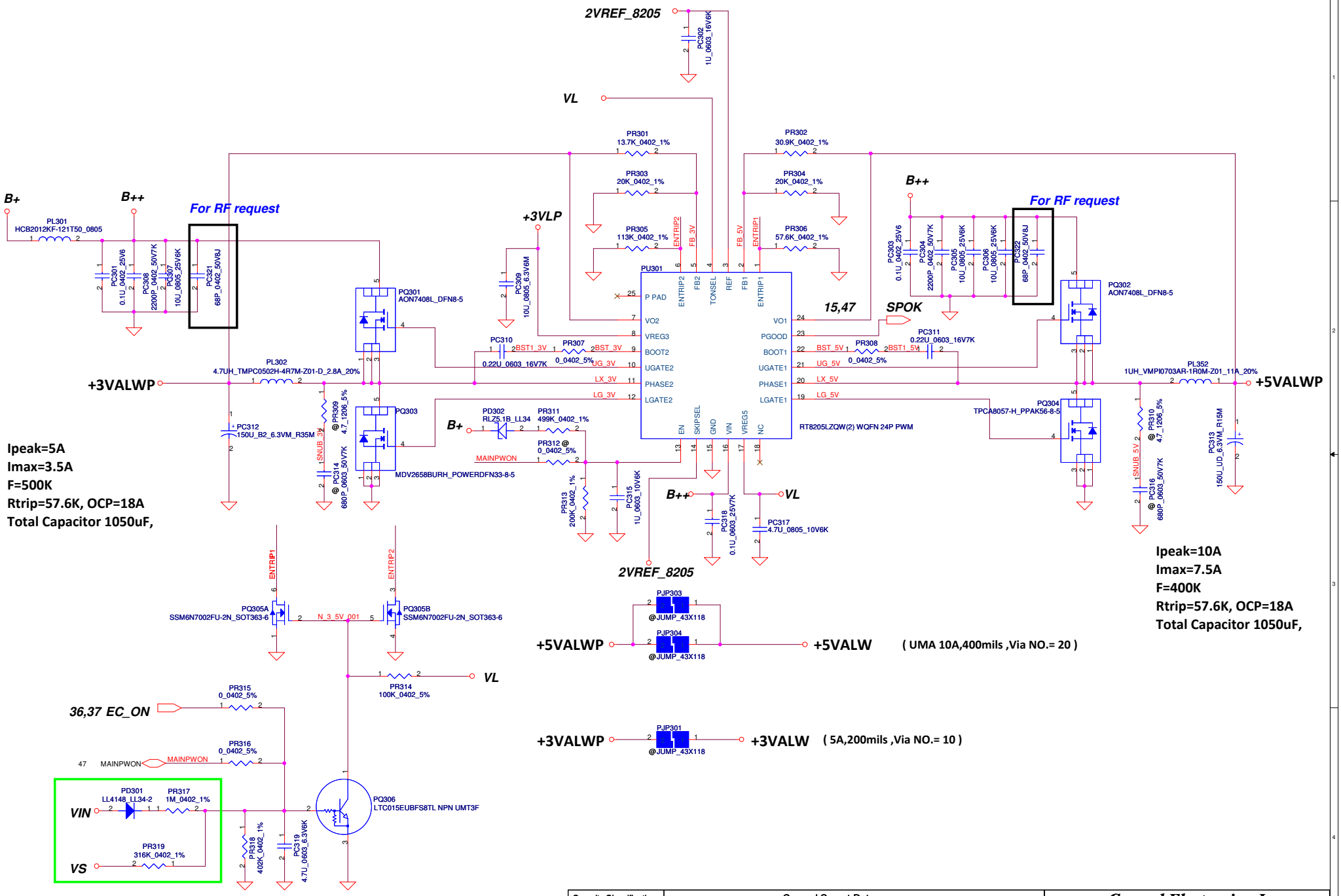
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- CHARGER

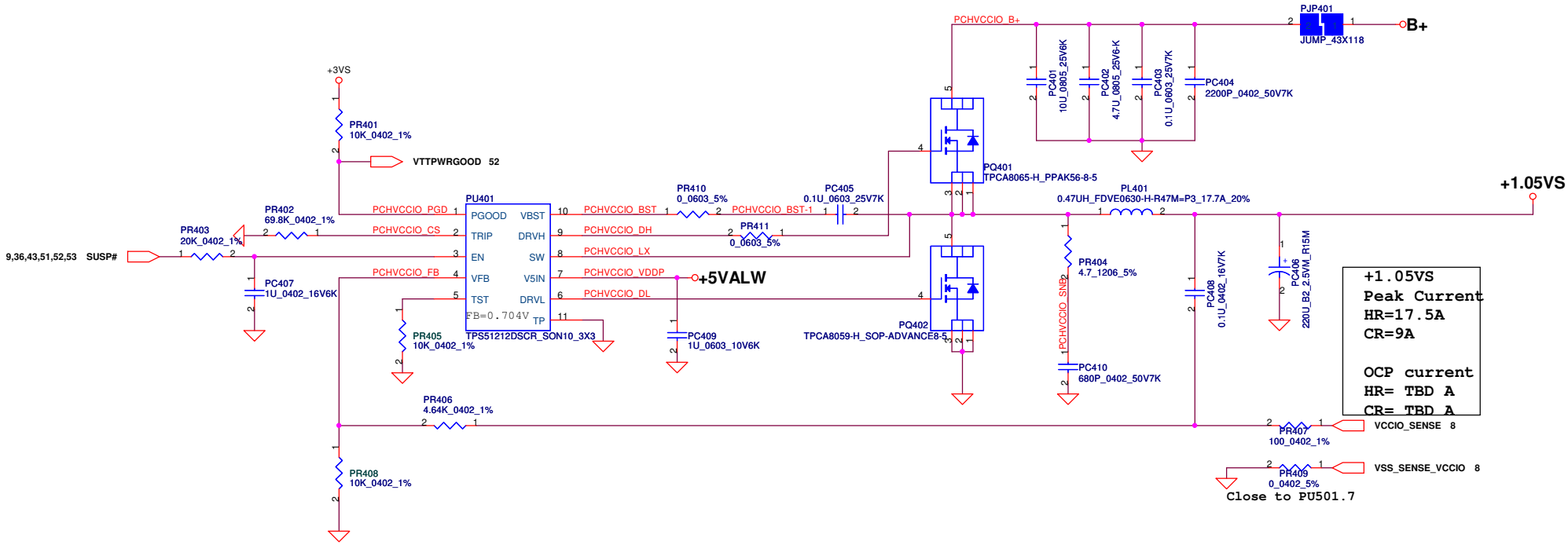
Size | Document Number: LA-8712P | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 48 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR- 3VALWP/5VALWP		
Size: Custom	Document Number: LA8711P		Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 49 of 57		



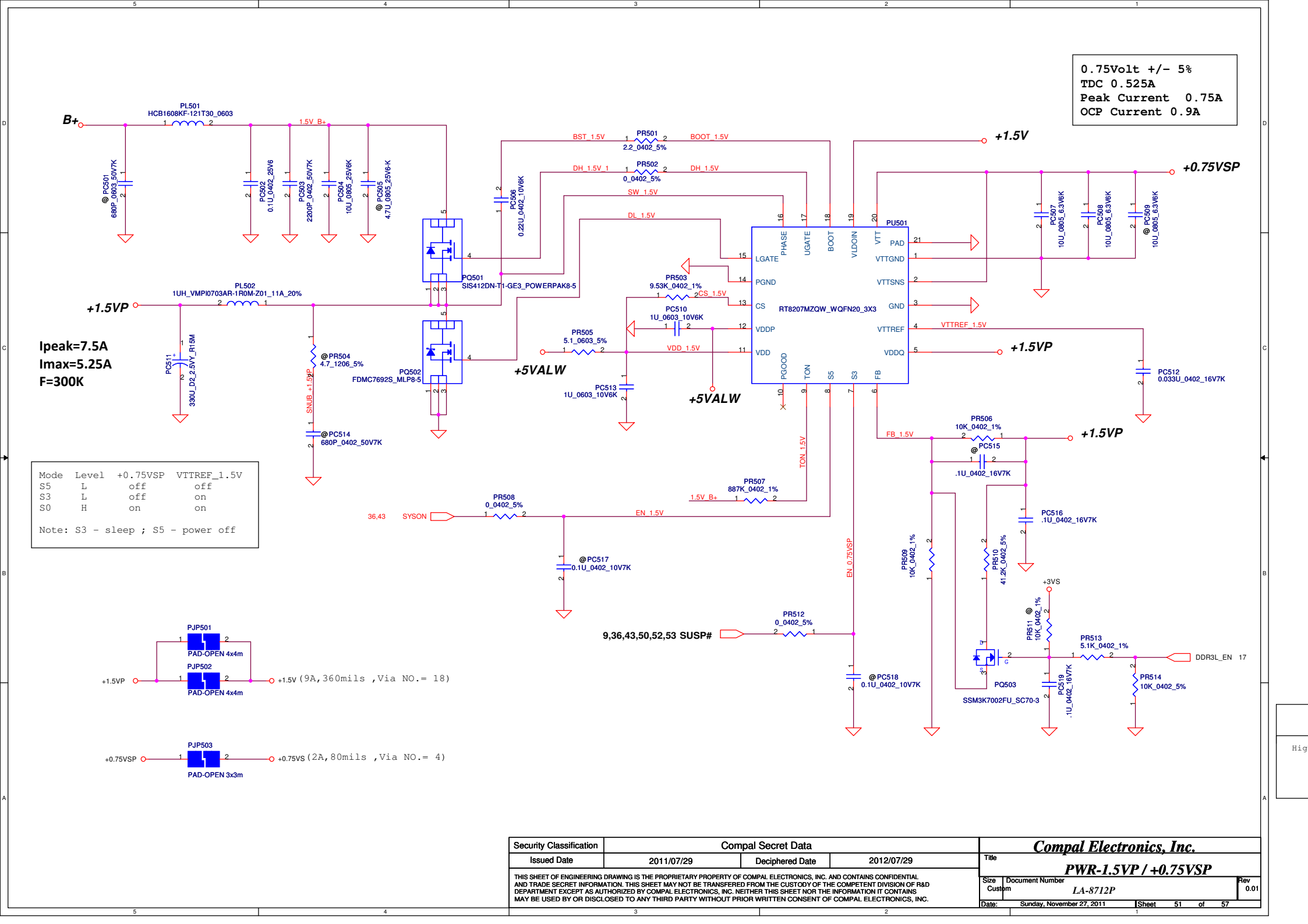
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PWR-1.05VS

Size: Custom | Document Number: LA8711P | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 50 of 57



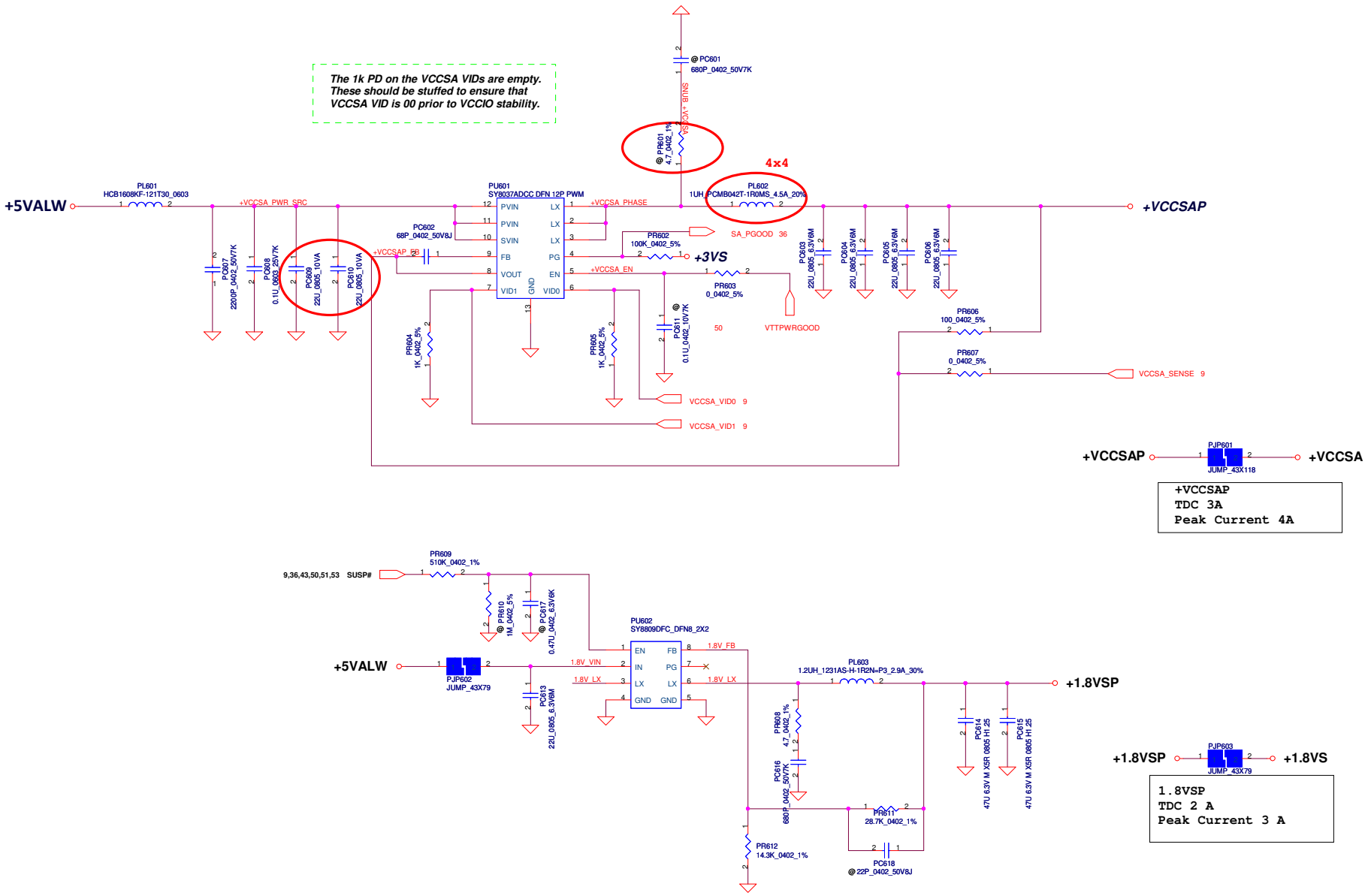
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

Size	Document Number	Rev
Custom	LA-8712P	0.01

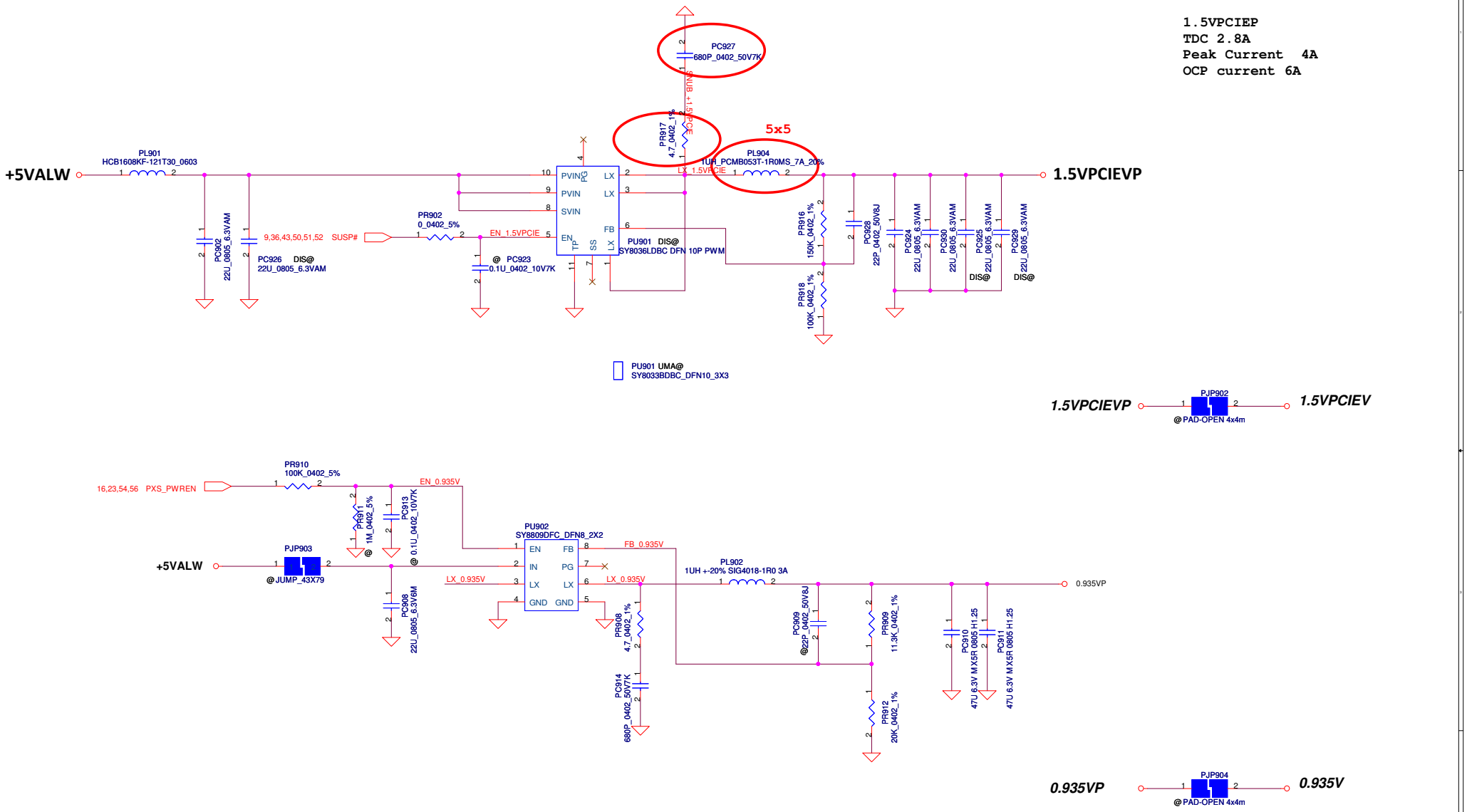
Date: Sunday, November 27, 2011 Sheet 51 of 57



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title	PWR-VCCPP/1.8VSP	
Size: Custom	Document Number: LA8711P	Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 52 of 57	



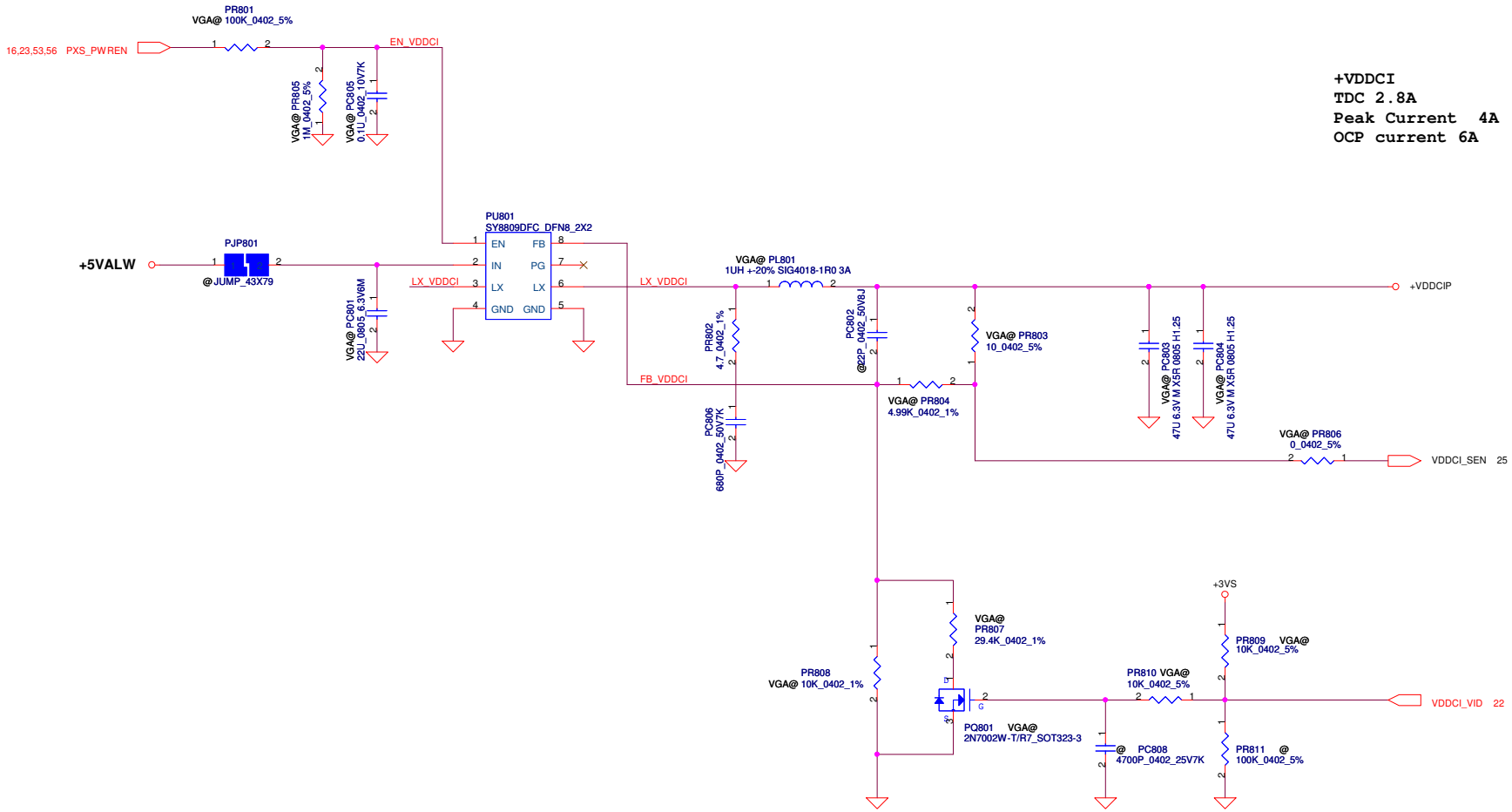
Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: **+1.5VPCIE/0.935V**

Size	Document Number	Rev
	LA8711P	0.2

Date: Sunday, November 27, 2011 | Sheet 53 of 57



+VDDCI
TDC 2.8A
Peak Current 4A
OCP current 6A

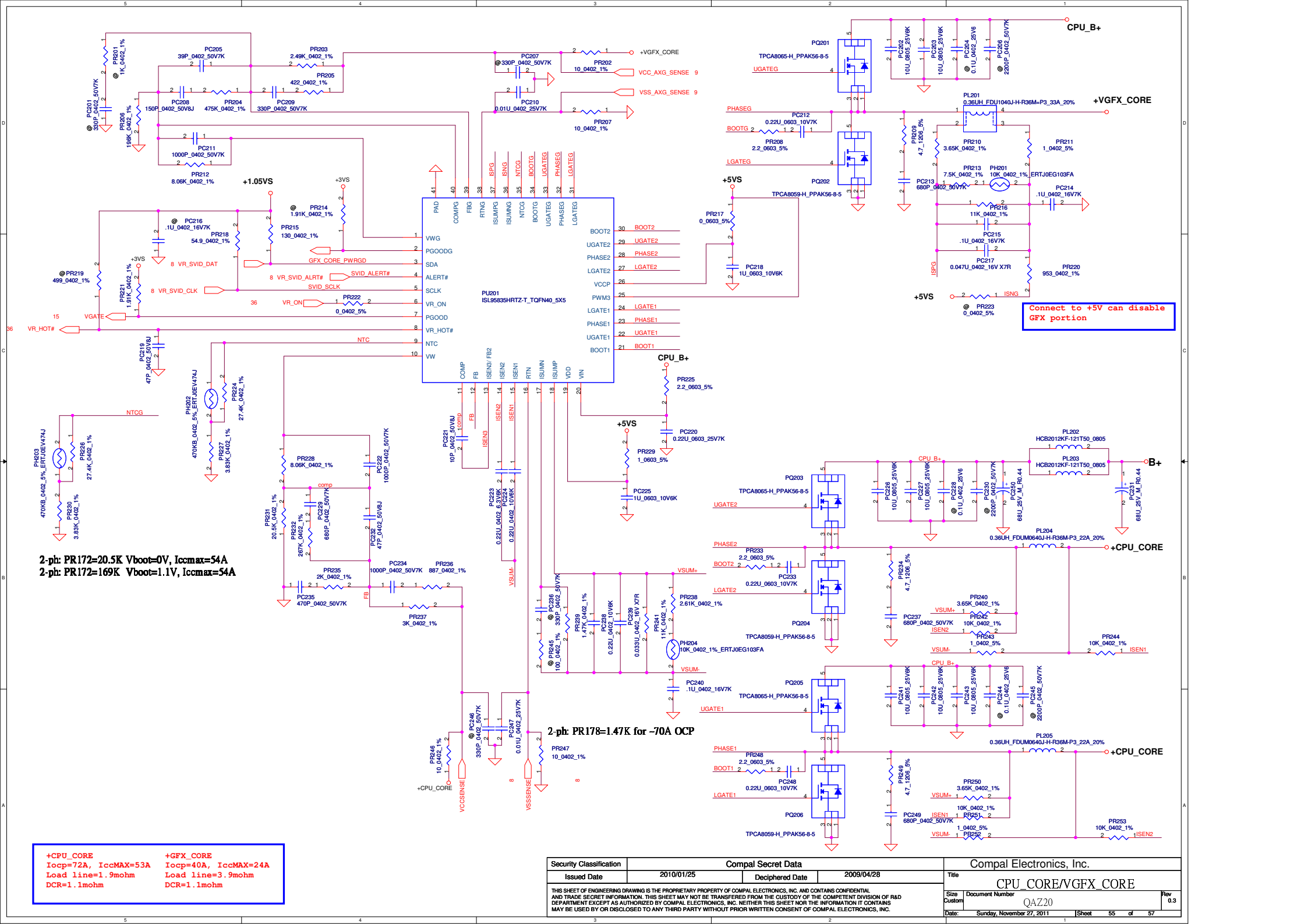
	VDDCI_VID
High	1V
Low	0.9V

Compal Electronics, Inc.

Title: +VDDCIP

Size | Document Number: LA8711P | Rev: 0.2

Date: Sunday, November 27, 2011 | Sheet 54 of 57


PU201
ISL9583HRTZ-T_TQFN40_5X5
CPU_B+
+VGFX_CORE
+5VS
+1.05VS
+3VS
+CPU_CORE
B+
Connect to +5V can disable GFX portion
2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
2-ph: PR172=169K Vboot=1.1V, Iccmax=54A
2-ph: PR178=1.47K for -70A OCP
+CPU_CORE
Iocp=72A, IccMAX=53A
Load line=1.9mohm
DCR=1.1mohm
+GFX_CORE
Iocp=40A, IccMAX=24A
Load line=3.9mohm
DCR=1.1mohm
Security Classification
Compal Secret Data
Issued Date
2010/01/25
Deciphered Date
2009/04/28
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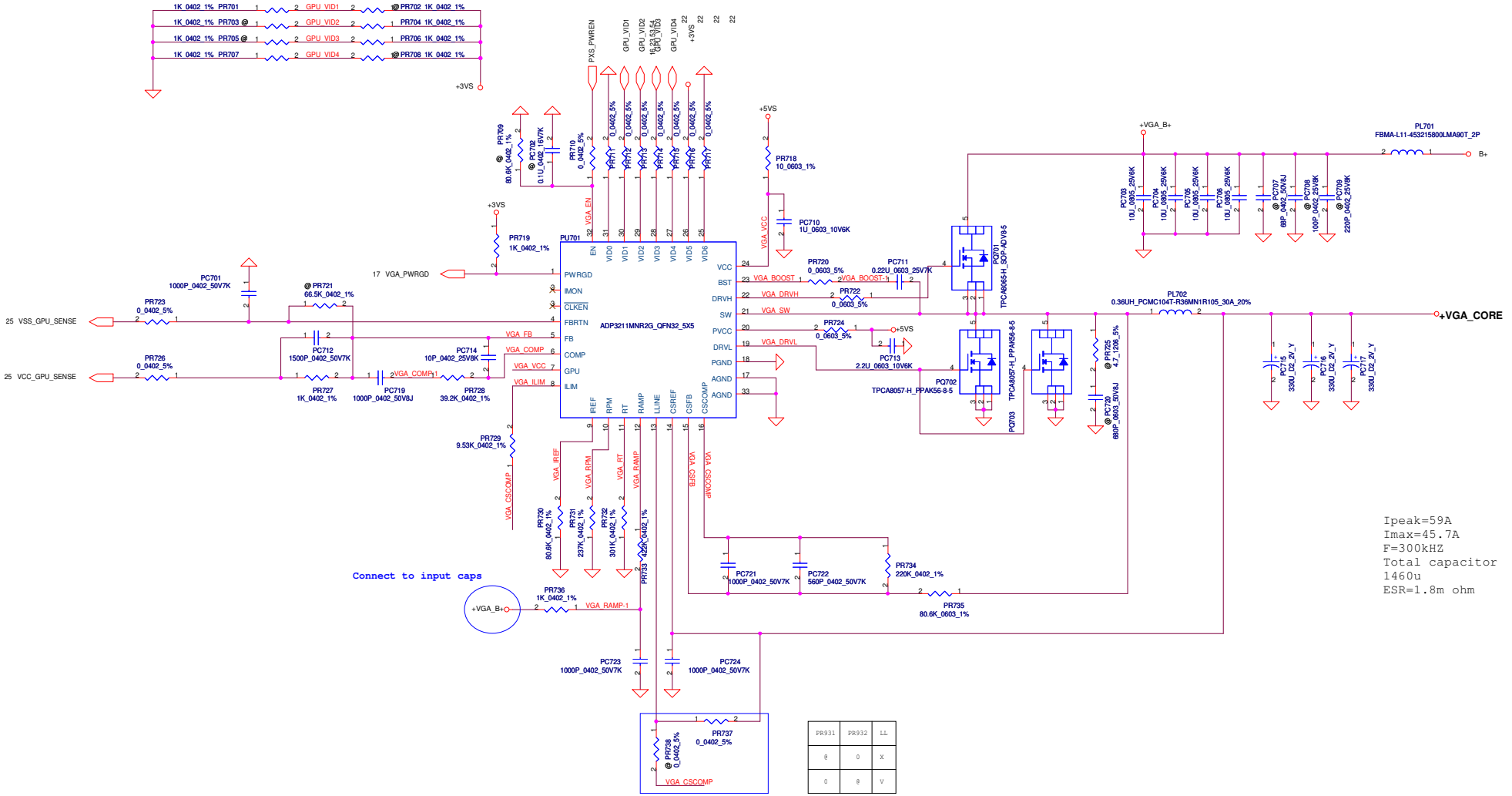
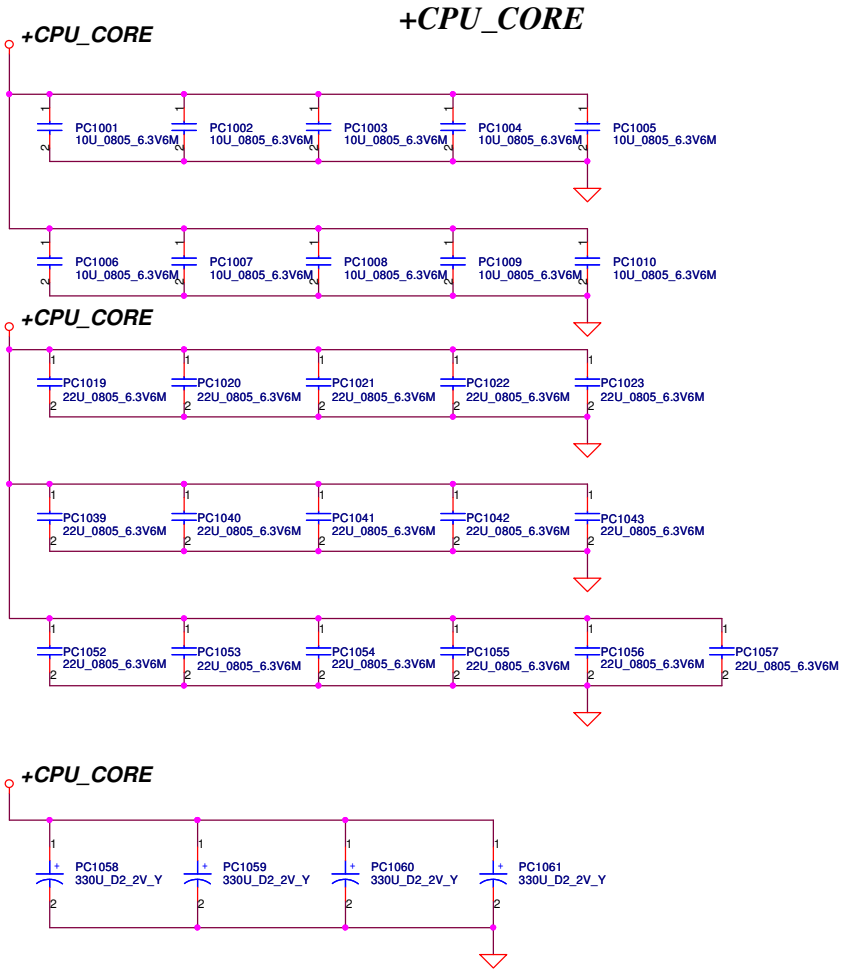
Title
CPU_CORE/VGFX_CORE
Size
Custom
Document Number
QAZ20
Rev
0.3
Date:
Sunday, November 27, 2011
Sheet
55
of
57



PR931	PR932	LL
@	0	X
0	@	V

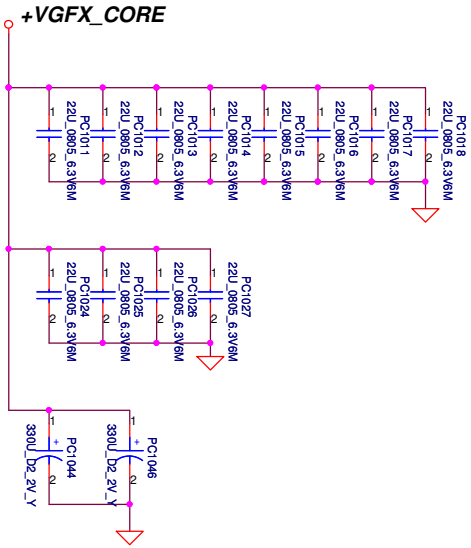
Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size	Document Number	LA-8712P	Rev 0.3
Date: Sunday, November 27, 2011	Sheet 56 of 57		



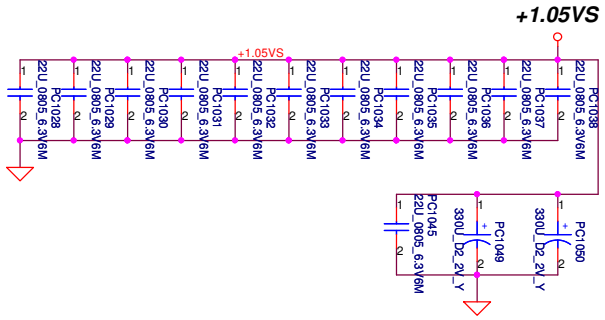
+CPU_CORE

+VGFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA8711P	0.1

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