Table of Contents

MTP	MTE	bottom side, 22mil
TP	EE/SW debug	top side, 22mil
XDP_TP	Intel requested	don't care, 22mil
GTP	Unused IO and GPIO/ Possible for Future Removal	don't care, 22mil
PTP	Current Sensing	top side (as close to resistor as possible), 22mil
MTP_BF	MTE big pads for FW, OS load, and RF.	bottom side, 31mil
MTTP_BF	MTE big pads for RF	top side, 31mil (if RF connector at the bottom side of the board)

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

Title: 01. Table of Contents

Microsoft Confidential — Engineer: Surface

Size	Project Name	Rev
A3	A	1.0.0.1

Date: Thursday, April 26, 2018 — Sheet 1 of 79

Schematics Change History

Schematics Change is maintained in spreadsheet, and would not fit on this page.

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors

Property: BUILD-OPT

DNP = Not Installed Part.

S = Short after design fixed

Title: 02. CHANGE HISTORY			
Microsoft Confidential	Engineer:	Surface	
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 2 of 79		

Architectural Diagram I-Core

Rev 2.5

Front IR (OV7251)

Illuminator

Debug UART, external connector

Power Monitor Components (DEBUG)

MIPI CSIx1 (1Gbps)

I2C

MIPI CSIx1

Front RGB (720p – OV9734)

Analog audio combo jack (3.5mm)

HD Audio

I2C

Audio Codec

R

L

AMP ALC1304

Right

Left

2 Mic

3.3V@0.8A OUT

Memory/ Storage

SSD2 BGA chip 128GB, 256GB 512GB, 1TB

SSD BGA chip 128GB, 256GB 512GB, 1TB

LPDDR3 x32 16,8,4 GB (4x)

2/4 x PCIe

2/4 x PCIe

128-bit (32b x 4) – 2 Chl -64 bit each

ALS

I2C

I2C1 UART2 CSI2x2 CSI2x2 I2C2

HDA I2C4

I2C3

PCIe 11/12

PCIe 7/8

DDR0x64, DD1x64

DMIC

DDI1

DDI1_AUX

DDPB_CTRL

DDI2_AUX

DDPC_CTRL

USB3p2

USB2p2

DDI2

16MB SPI ROM

Quad SPI

SPI0 GPIOs

Backlight Controller

I2C5

LCD 13.5"

TCON

NTRIG G5

eDP

eDP 1.4a

SPI

SPI1

I2C

I2C0

INT

SKL-U 15W 2+2/2+3E

DDI2_AUX

DDPC_CTRL

USB3p1

USB2p1

PCIe9

USB2p5 LPC

UART

UART1

DPG

PDX

TrackPad

KeyBoard

UART

INT

SC Freescale K22

UART

SL UART

MUX

PWM/Tach

Fan/Fan Connection

Temp

I2C

I2C

SC Debug

Hall Effect

XDP

Debug XDP

LPC

1XPCIe

USB2

Wifi abgn+ac Marvell 88W8897 BT

Antennas

Power path updates Separate Block Diagram

POR CHANGES

TPM Infineon Nuvaton NationZ

IMVP8 PMIC ISL95857 W/2+3E support

Power/PMIC BD9992GW (sep Block Dia)

7.4V

Battery 45WH w/Fuel G

7.4V

Battery Charger ISL9237

SC,K22

Greenpak

Surflink

SD FLUSH

POR CHANGES

2xTPS62134 VCCEDRAM/VCCEOPIO

MUX

AUX/DDPC

CMC + ESD

mDP

POWER IN/OUT

MUX

AUX/DDPC

Debug Signals

Debug MUX

CMC + ESD

CMC + ESD

5V@1.78A OUT

CMC + ESD

USB2

POR CHANGES

LEGEND

Mostly same as P

Changed Feature/Implementation

New Feature/Implementation

Title: 03. BLOCK DIAGRAM

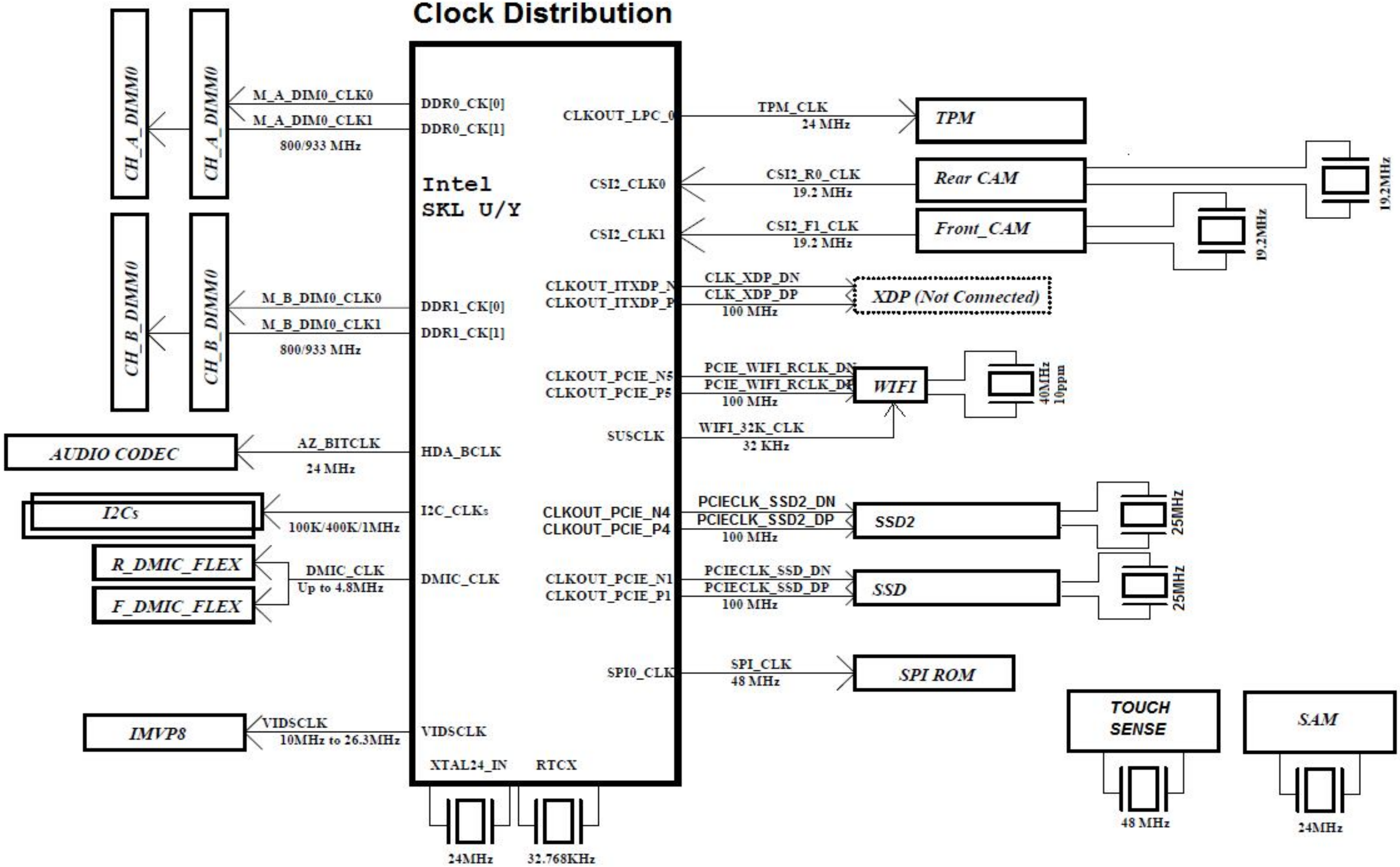
Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 3 of 79

Clock Distribution



Title: 04. CLOCK DISTRIBUTION			
Microsoft Confidential	Engineer: Surface		
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 4 of 79		

System Power State Diagram

Microsoft Confidential

3P3VA ON
3P3V_SAMON
S0 RAILS ON

3P3VA ON
3P3V_SAMON
S0 RAILS OFF

3P3VA ON
3P3V_SAMOFF
S0 RAILS OFF

3P3VA OFF
3P3V_SAMOFF
ALL S0 RAILS OFF

S5
S5 PWR:ON / S0 OFF
SAM: Active
GP/RTC: ON

S0
S5/S0 Pwr: ON
SAM: Active
GP/RTC: ON

Pre-S5
S5/S0 PWR:OFF
SAM: Active
GP/RTC: ON

Connected Standby
S5/S0 Pwr: Low Power
SAM: Low Power
GP/RTC: ON

DeepSlp
S5/S0 PWR: OFF
SAM: OFF
PMIC/CHGR: OFF
GP/RTC: ON

Any State
(except EMER Shutdown)

EMER Shutdown
S5/S0 PWR: OFF
SAM: OFF
PMIC/CHGR OFF
GP/RTC: OFF
BATTERY:OFF

G3
S5/S0 PWR: OFF
SAM: OFF
PMIC/CHGR OFF
GP/RTC: OFF

Hard Reset
S5/S0 PWR: OFF
SAM: Pwr Cycle
PMIC/CHGR:Pwr Cycle
GP/RTC: ON

HW Debug
S5/S0 PWR: OFF
SAM: Pwr Cycle
PMIC/CHGR:Pwr Cycle
GP/RTC: ON

Battery/System Critical Temp (SAM)

OS Shut Dowm

SB_PWRBTN Asserted (debounced PWR_SW_N)

PMIC_EN de-asserted

PMIC_EN AND (PWR_SW_N OR PWR_BTN_STATE) asserted)

SB_PWRBTN asserted OR Keyboard Lid Closed OR Sleep Selected OR OS Timeout

SB_PWRBTN asserted OR OS Wake Event

Battery/System Critical Temp (SAM)

SAM_GP_DEEPSLP Asserted (no PSU & 30s timeout)

PWR_SW_N asserted >30msec OR SL_PG asserted

GP_DBACC asserted AND Hard Reset Done

Surflink PWR applied

Surflink PWR applied

Hard Reset Done (PWR_BTN_STATE asserted)

VDD_BAT PWR applied

System Temp Critical (HW GP_TSYS>Tcrit OR Bat temp>60C)

SAM_RST asserted OR PWR_SW_N >15s

PWR_SW_N >30sec

NOTE: HW Debug state only available during development

Vinafix.com

Title:	05. SIGNAL & RESET MAP		
Microsoft Confidential	Engineer:	Surface	
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 5 of 79		

J47001
SurfLink Connector
PWR_SL1

PWR_SL1

Q63008 / Q63009
Back to Back FETS

PWR_SL1_R

R63001
20mΩ

U63001
ISL9237
Buck/Boost Charger

VSYS_R

R63042
10mΩ

R63009
10mΩ

VDD_BAT

J70001 /70002 / 70003
Battery Connector

2S
Battery
7.6V typ

VDD_BAT

PWR_SL1_F

3P3VA
Imax = .5A

U56002
TPS 62177
3P3VA
Always On

R56007
100mΩ

U56005
NX3P1108
3P3VA_SW_EN

R56033
100mΩ

3P3VA_SW
Imax = .3A

R36016
100mΩ

3P3VA_TEMP

R36023
100mΩ

3P3V_PMI_DBG

R28001
100mΩ

3P3VA_SAM

R31023
0mΩ

3P3V_DEBUG

VCC_RTC
Imax=100 uA

IMVP 8

R67007
20mΩ

VCORE

VCORE

R68001
20mΩ

VCCGT/GTx

VCCGT

R67028
50mΩ

VCCSA

VCCSA

SKL
VCORE
Imax = 28A
VCCGT/VCCK
Imax = 30A
VCCSA
Imax = 7A

Platform PMIC
U58001

R58034
10mΩ

V3P3_DSW
V6

V3P3_DSW

R58039
20mΩ

R26004
10mΩ

3VSUS_ORG

R68001
100mΩ

3P3V_TPM

U65003
TPS22920
3P3V_SSD_EN

R6501010mΩ

3P3V_SSD

R43017
25mΩ

U43005
TPS 62085
1P8V_SSD

1P8V_SSD

R43016
25mΩ

U43006
TPS 62085
1P2V_SSD

1P2V_SSD

U65001
TPS22920
EDP_VDD_EN

R65002
50mΩ

3P3V_PANEL

R53037
0Ω

U53005
NCP380
nDP_PWR_EN

ML_V3P3_PWR

J53001
mDP
Connector

R54035
100mΩ

3P3V_CAM

R58019
5mΩ

V5A
V5

V5A

R58024
10mΩ

R45033
5mΩ

U45004
AP2553
SKL_SLP_S4_N

5V_USBPWR_A

J45001
USB 3.0 A
Connector

R48022
100mΩ

U48002
SLG59M1448V
PCH_TPANEL_PWR_EN

5V0_OFFBOARD
(keyboard)

R64019
10mΩ

5V_SWPWR

R64006
50mΩ

U64002
SLG59M1448 V
PCH_TPANEL_PWR_EN

5V_TS

R64016
20mΩ

U64004
SLG59M1448V
PCH_AUD_5V_EN

5V_AUDIO

R64020
20mΩ

U64006
SLG59M1448V
SAM_FAN_PWR_EN

5V_FAN (i-core only)

Vsys

R58012
20mΩ

V1P8A
V8

V1P8A

R58016
20mΩ

R28003
10mΩ

1P8VSUS_ORG

U62001
SLG59M1448 V
PCH_AUD_1V8_EN

R62002
20mΩ

1P8V_AUDIO

R40005
20mΩ

1P8V_AUDIO_DVDD

U62003
NX3P1108
PCH_TPANEL_PWR_EN

R62007
20mΩ

1P8V_TS

R58002
10mΩ

V3P3A_PCH
V7

V3P3A_PCH

R58008
50mΩ

U65004
TPS 22920
WWAN_PWREN

R65012
40mΩ

3P3V_WWAN

R59023
25mΩ

V0P85A
V12

V0P85A

R59027
10mΩ

V0P85A

R59003
25mΩ

V1P00A
V11

V1P00A

R59007
10mΩ

V1P00A

R61007
20mΩ

1V_MODPHY

U61002
SLG5NT1477
VCCSTG_EN

R61003
10mΩ

VCCSTG

U61003
SLG5NT1477
SKL_SLP_S4_N +
XDP_PRESENT_LOGIC

R61006
10mΩ

VCCST_CPU

R18031
0mΩ

V1P00A_XDP

R58023
10mΩ

V1P8U_2P5U
V9

V1P8U_2P5U

R58026
50mΩ

V1P8U_2P5U

R58032
25mΩ

V1P2U
V10

V1P2U

R58037
5mΩ

R59032
10mΩ

U61001
SLG5NT1477
SOIX_EN

R61005
10mΩ

VCCPLL_OC

V0P6DX_LPDDR3
V13

R59035
20mΩ

V0P6DX_LPDDR3

R58004
25mΩ

VCCIO
V4

VCCIO

R58030
10mΩ

VCCIO

R72001
20mΩ

U72001
RT8555
L_BKLTEN

VCC_EDP_BKLT_OUT

DeepSleep Rail

S4/S5 Rail

S0 Rail

Power Monitor Input

R99999
20mΩ

Load switch
Control Signal

DC-DC
Regulator

External
Regulator/Load
Switch

Linear
Regulator

DVT/U70850x16x512cCRetail

Title: 06. POWER DISTRIBUTION

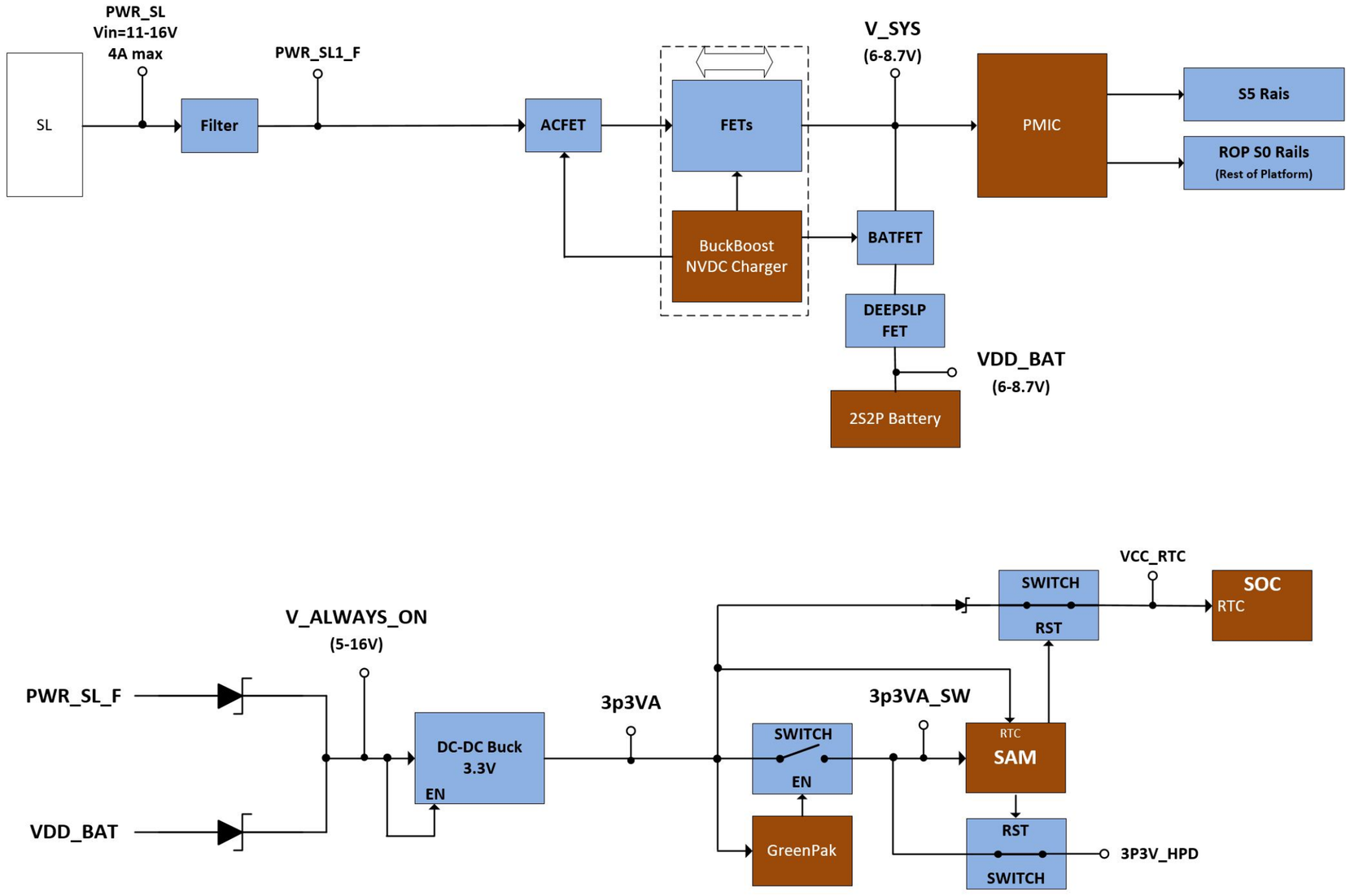
Microsoft Confidential

Surface

Size: D
Project Name:
Engineer:
Rev: 1.0.0.1

Date: Thursday, April 26, 2018
Sheet 6 of 79

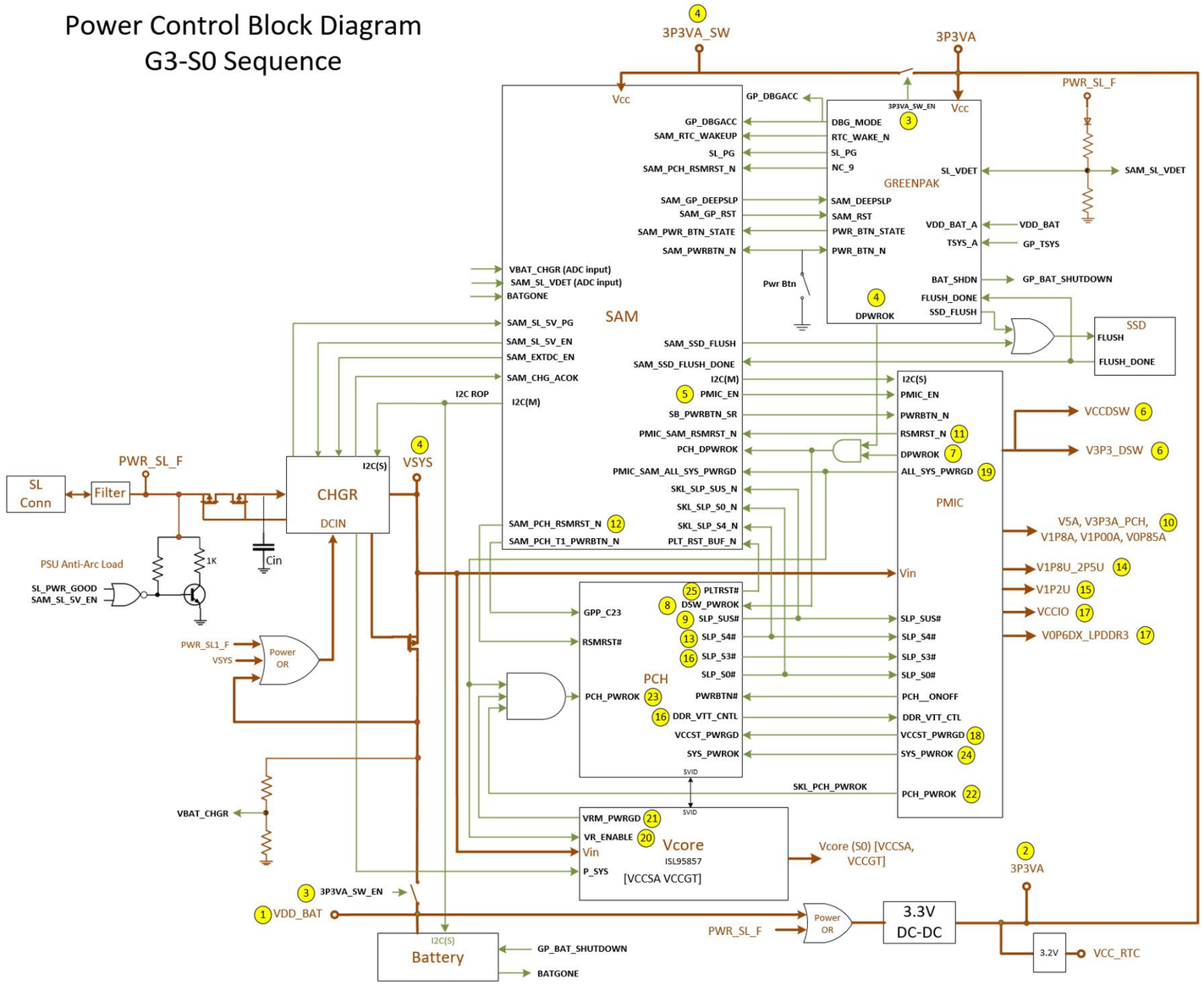
Lynx SL INPUT POWER DIAGRAM



DVI7U7660s16s512x2Retail

Microsoft Confidential	Title: 07. POWER SEQUENCE 1		
	Engineer: Surface		
Size: D	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 7 of 79		

Power Control Block Diagram
G3-S0 Sequence



DVI7U7660s16s512x2Retail

Title: 08. POWER SEQUENCE

Microsoft Confidential | Engineer: Surface

Size	Project Name	Rev
D	A	1.0.0.1

Date: Thursday, April 26, 2018 | Sheet 8 of 79

I2C Map

7-bit slave addresses
September 28, 2016

DEBUG: Power Monitors

U36002 PMI1 MAX34407 0x12 S
U36004 PMI3 MAX34407 0x18 S
U36006 PMI5 MAX34407 0x1C S
U36008 PMI6 INA231 0x41 S
U36001 PMI0 MAX34407 0x1E S
U36003 PMI2 MAX34407 0x10 S
U36005 PMI4 MAX34407 0x1A S
U36007 PMIBATT INA231 0x40 S

PMI_I2C_Sxx
3P3V_PMI_DBG
2.2k?
To EE Power Debug Connector
Option to connect to I2C_ROP_Sxx

Debug Connector
EE Power Debug Connector
Debug Muxes
Removed in Retail
DEBUG_OSG in Retail
DNP in Non-Retail/Retail

Cameras

EEPROM GT24C08S 0x50, 0x51, 0x52, 0x53 S
Front RGB OV9734 0x36 S
IR Cam OV07251 0x60 S

1P8VSUS_ORG
2k?
I2C_Sxx_CAM
To EE Power Debug Connector

Light Sensor and BKLT Controller

ALS ISL29033 0x44 S
Backlight Drvr RT8555 0x31 S

I2C_Sxx_ALS
I2C_Sxx_BKLT
1P8VSUS_ORG
2k?
Display_VDD18
3P3V_PANEL
4.7k?
To Debug Connector

Display

TCON MLTS152000 0x28 S
I2C_DISPLAY_Sxx (DNP)
To Debug Connector

SOC/PCH
U10001
0x4D

M I2C2
M I2C1
M I2C3
I2C5 M
I2C_Sxx_ALS (DNP)
1P8VSUS_ORG
2k?
Option to Connect to ALS Sensor at J54001

I2C4 M
I2C0 M
I2C_Sxx_TP
5VA -> P3V3_TP
TP_PWR_EN
2.2k?

Trackpad

Trackpad IC S9101B 0x20 S
To Debug Muxes
To Debug Connector

Wifi/BT

Wifi 88W8897 U50001 M
1P8V_WIFI_INT_OUT
10k?
SER_Sxx
EEPROM AT24C16D 0x50 -0x57 S

Power Management

PMIC BD99992GW 0x30 S
3P3VA_SW
2k?
I2C_Sxx_MCU

Charger BQ24770 0x09 S
Fuel Gauge BQ40x50 0x0B S
CHG_Sxx
BATT_I2C_xxx
3P3VA_SW
2.2k?
I2C_ROP_Sxx
To Debug Muxes
To EE Power Debug Connector

M I2C2
SAM
K22P121M120SF5
U27001
0x28
M I2C1
I2C0 M
Option to Connect I2Cs

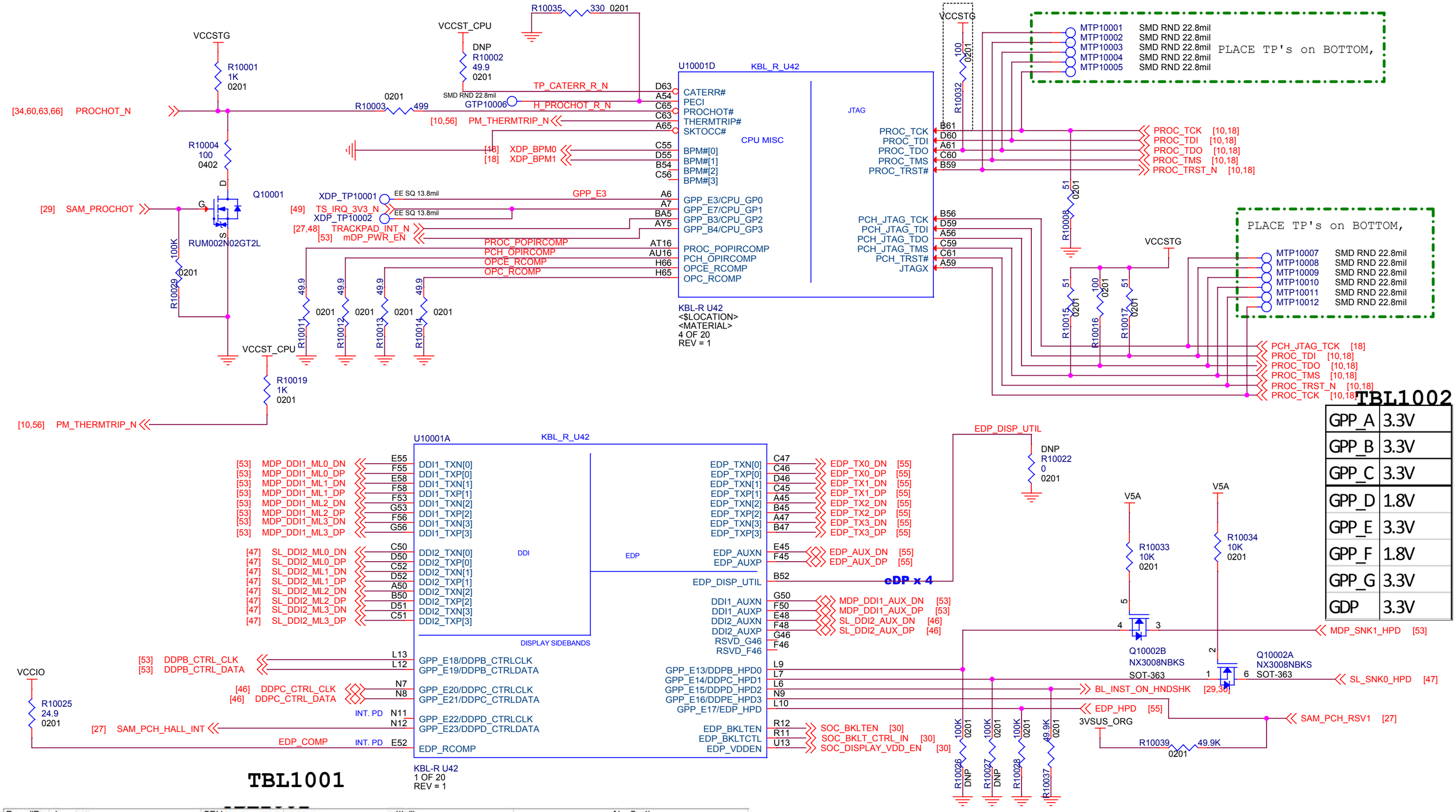
I2C_Sxx_MCU
To EE Power Debug Connector

Temp Sensors

Critical Temp SN1511004 0x48 S
Temp Sensor STTS751 0x3B S
IR Temp TMP007 0x40 S
Temp Sensor STTS751 0x3A S
Temp Sensor STTS751 0x4A S

DVi7U7660s16s512x2Retail

Title:	09. I2C MAP		
Microsoft Confidential	Engineer:	Surface	
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018		Sheet 9 of 79	



TBL1001

BoardID	description	CPU	stuff(all)	No-Stuff
000	reserved		R23040, R23042, R23044	R23041, R23043, R23045, R28091, R28092, R28093
001	reserved		R23041, R23042, R23044, R28091	R23040, R23043, R23045, R28093, R28092
010	KBL U42 i5-8250U	M1086844-00	R23040, R23043, R23044, R28092	R23041, R23042, R23045, R28093, R28091
011	reserved		R23041, R23043, R23044, R28091, R28092	R23040, R23042, R23045, R28093
100	KBL U42 i5-8350U	M1029639-001	R23040, R23042, R23045, R28093	R23041, R23043, R23044, R28091, R28092
101	reserved		R23041, R23042, R23045, R28093, R28091	R23040, R23043, R23044, R28092
110	KBL U42 i7-8650U	M1020597-001	R23040, R23043, R23045, R28093, R28092	R23041, R23042, R23044, R28091
111	reserved		R23041, R23043, R23045, R28091, R28092, R28093	R23040, R23042, R23044

U SPECIFIC

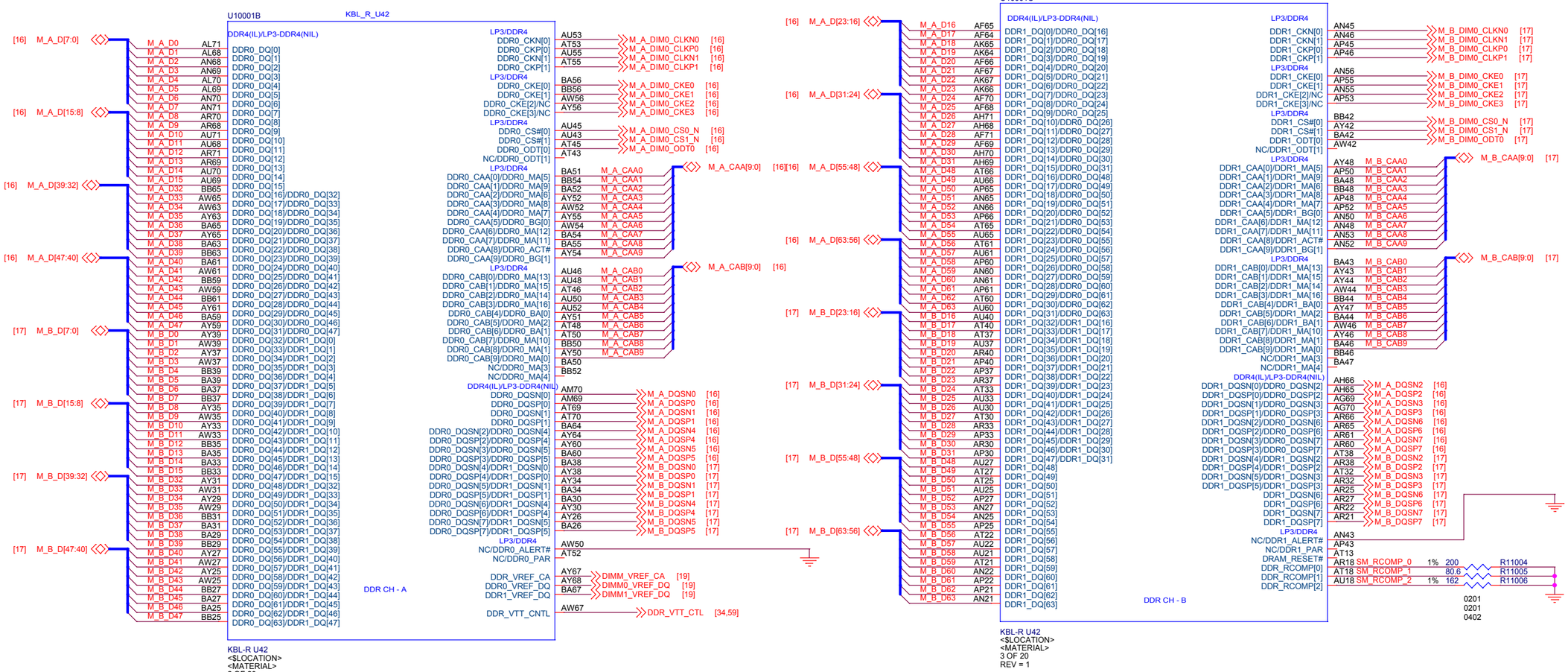
Title: 10. CPU(1)_MISC,JTAG,DDI.EDP

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Friday, April 27, 2018 Sheet 10 of 79



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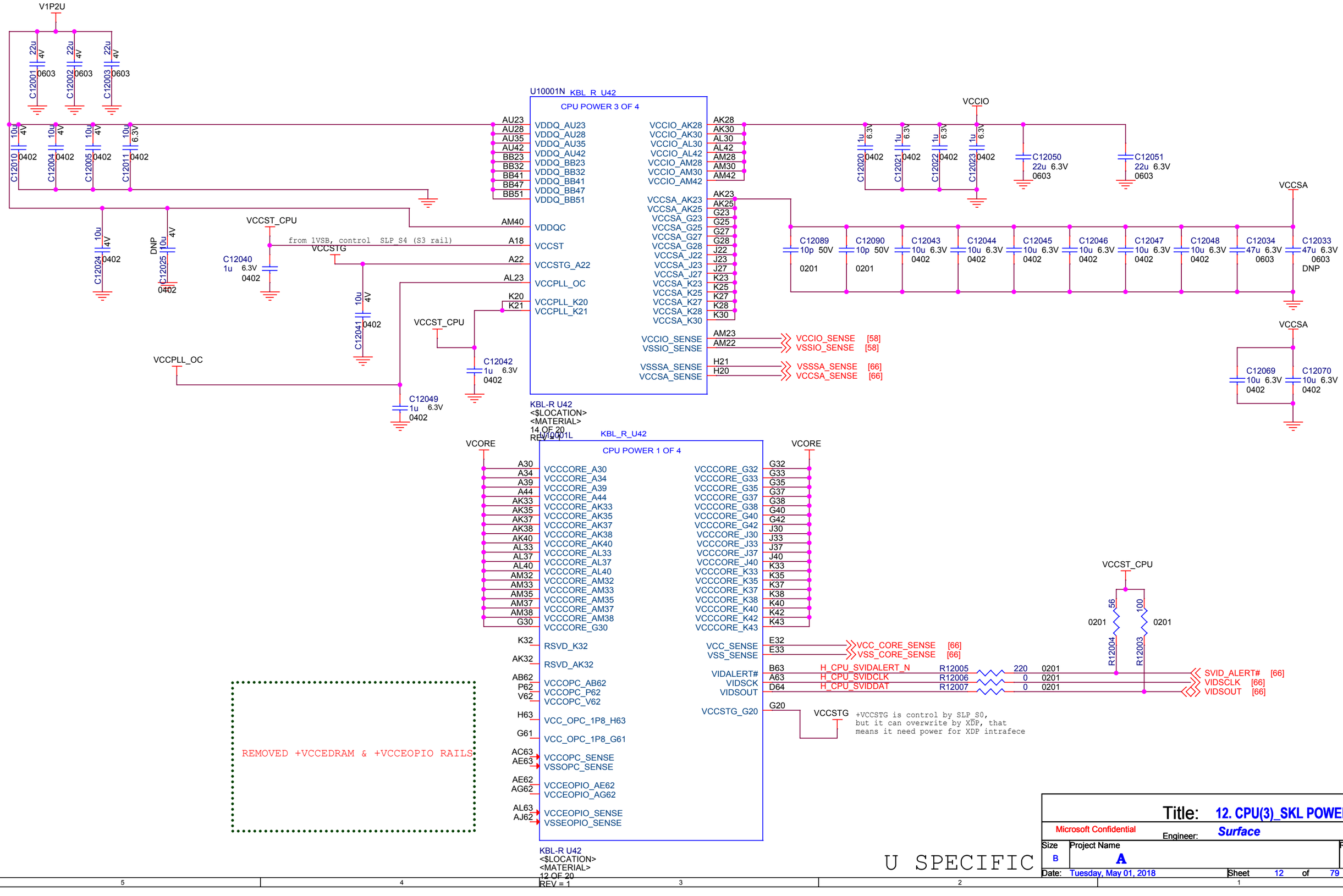
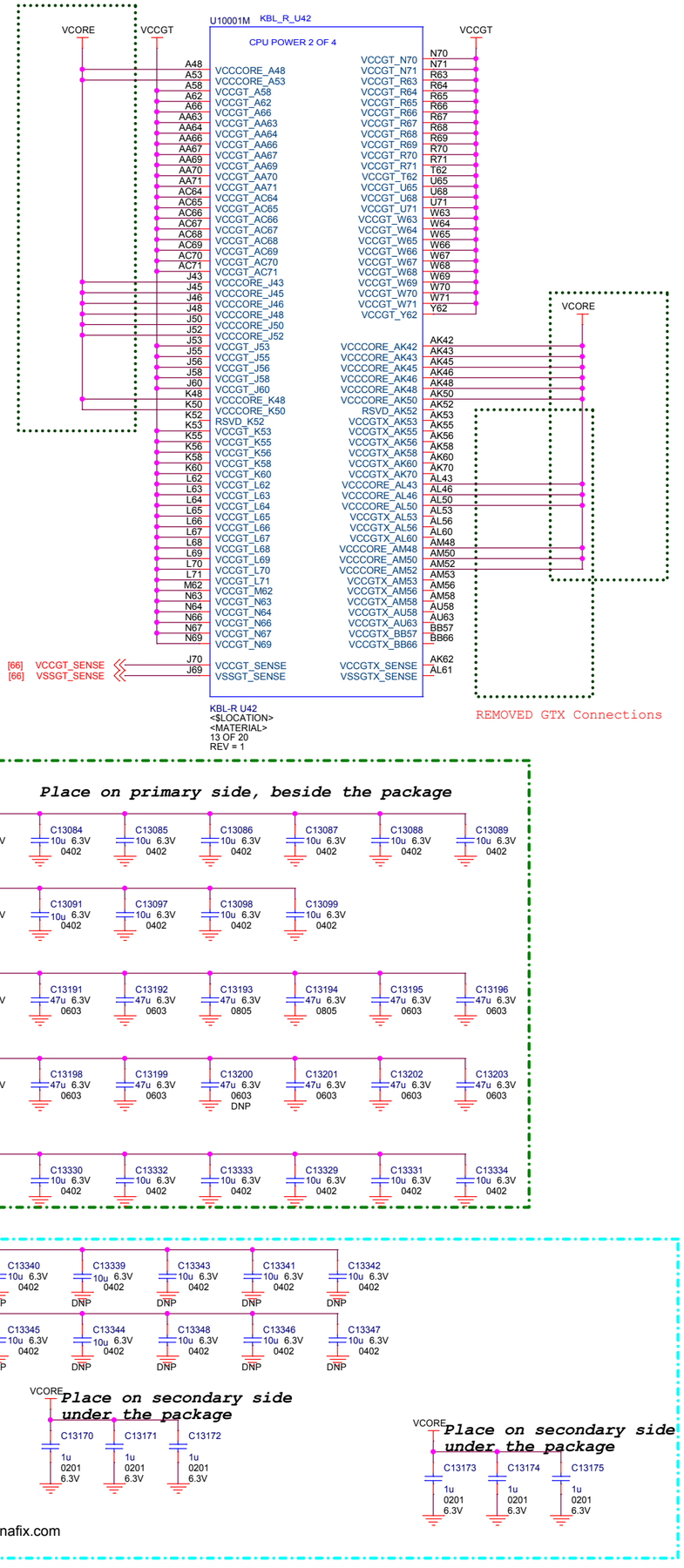
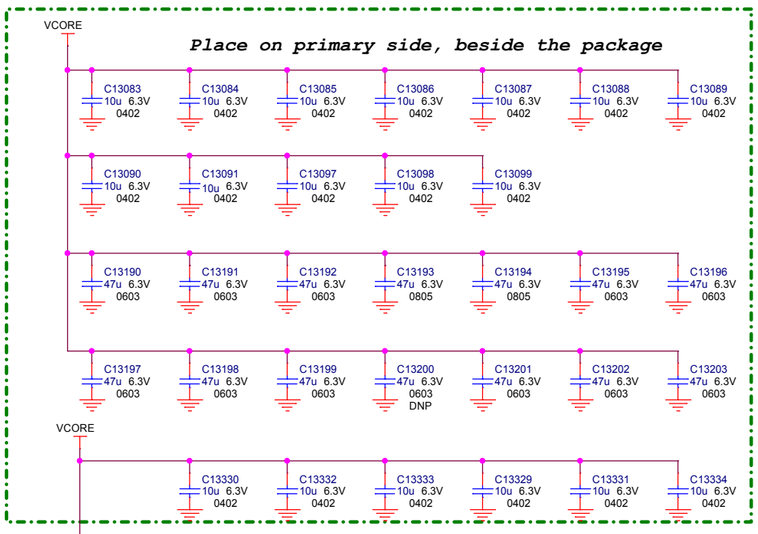
U SPECIFIC

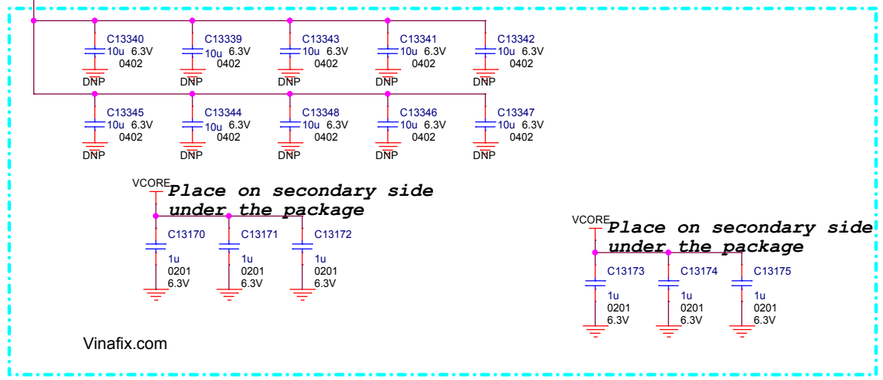
Title:	11. CPU(2)_LPDDR3
Microsoft Confidential	Engineer: Surface
Size: C	Project Name: A
Rev: 1.0.0.1	
Date: Friday, April 27, 2018	Sheet 11 of 79

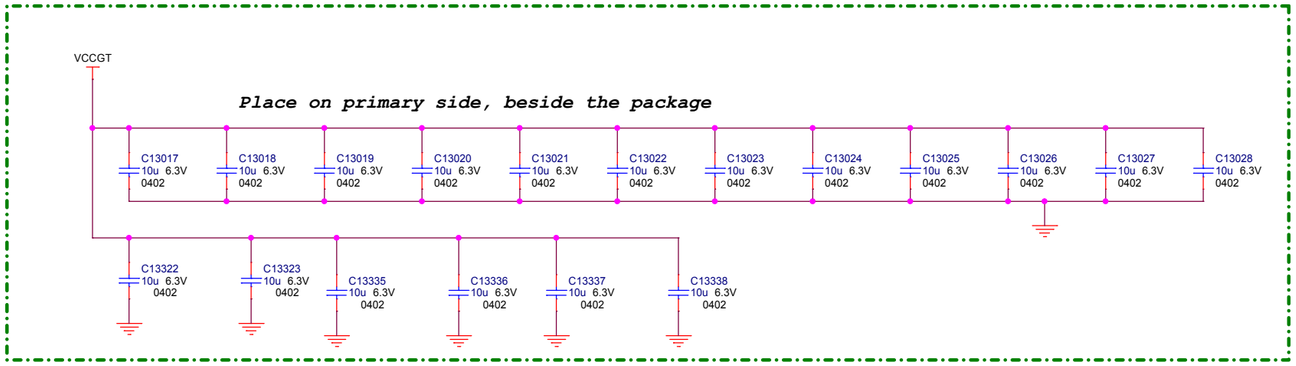

V1P2U
C12001 22u 4V 0603
C12002 22u 4V 0603
C12003 22u 4V 0603
C12010 10u 4V 0402
C12004 10u 4V 0402
C12005 10u 4V 0402
C12011 10u 6.3V 0402
C12024 10u 4V 0402
DNP C12025 10u 4V 0402
C12040 1u 6.3V 0402
VCCST_CPU
from 1VSB, control SLP_S4 (S3 rail)
VCCSTG
C12041 10u 4V 0402
VCCPLL_OC
C12049 1u 6.3V 0402
C12042 1u 6.3V 0402
U10001N KBL_R_U42
CPU POWER 3 OF 4
AU23 AU28 AU35 AU42 BB23 BB32 BB41 BB47 BB51 VDDQ_AU23 VDDQ_AU28 VDDQ_AU35 VDDQ_AU42 VDDQ_BB23 VDDQ_BB32 VDDQ_BB41 VDDQ_BB47 VDDQ_BB51
AM40 VDDQC
A18 VCCST
A22 VCCSTG_A22
AL23 VCCPLL_OC
K20 K21 VCCPLL_K20 VCCPLL_K21
VCCIO_AK28 VCCIO_AK30 VCCIO_AL30 VCCIO_AL42 VCCIO_AM28 VCCIO_AM30 VCCIO_AM42 AK28 AK30 AL30 AL42 AM28 AM30 AM42
VCCSA_AK23 VCCSA_AK25 VCCSA_G23 VCCSA_G25 VCCSA_G27 VCCSA_G28 VCCSA_J22 VCCSA_J23 VCCSA_J27 VCCSA_K23 VCCSA_K25 VCCSA_K27 VCCSA_K28 VCCSA_K30 AK23 AK25 G23 G25 G27 G28 J22 J23 J27 K23 K25 K27 K28 K30
VCCIO_SENSE VSSIO_SENSE AM23 AM22
VCCIO_SENSE [58]
VSSIO_SENSE [58]
VSSSA_SENSE VCCSA_SENSE H21 H20
VSSSA_SENSE [66]
VCCSA_SENSE [66]
VCCIO
C12020 1u 6.3V 0402
C12021 1u 6.3V 0402
C12022 1u 6.3V 0402
C12023 1u 6.3V 0402
C12050 22u 6.3V 0603
C12051 22u 6.3V 0603
VCCSA
C12089 10p 50V 0201
C12090 10p 50V 0201
C12043 10u 6.3V 0402
C12044 10u 6.3V 0402
C12045 10u 6.3V 0402
C12046 10u 6.3V 0402
C12047 10u 6.3V 0402
C12048 10u 6.3V 0402
C12034 47u 6.3V 0603
C12033 47u 6.3V 0603 DNP
VCCSA
C12069 10u 6.3V 0402
C12070 10u 6.3V 0402
KBL-R U42
<$LOCATION>
<MATERIAL>
14 OF 20
REV = 1
U10001L KBL_R_U42
CPU POWER 1 OF 4
VCORE
A30 A34 A39 A44 AK33 AK35 AK37 AK38 AK40 AL33 AL37 AL40 AM32 AM33 AM35 AM37 AM38 G30 VCCCORE_A30 VCCCORE_A34 VCCCORE_A39 VCCCORE_A44 VCCCORE_AK33 VCCCORE_AK35 VCCCORE_AK37 VCCCORE_AK38 VCCCORE_AK40 VCCCORE_AL33 VCCCORE_AL37 VCCCORE_AL40 VCCCORE_AM32 VCCCORE_AM33 VCCCORE_AM35 VCCCORE_AM37 VCCCORE_AM38 VCCCORE_G30
K32 RSVD_K32
AK32 RSVD_AK32
AB62 P62 V62 VCCOPC_AB62 VCCOPC_P62 VCCOPC_V62
H63 VCC_OPC_1P8_H63
G61 VCC_OPC_1P8_G61
AC63 AE63 VCCOPC_SENSE VSSOPC_SENSE
AE62 AG62 VCCEOPIO_AE62 VCCEOPIO_AG62
AL63 AJ62 VCCEOPIO_SENSE VSSEOPIO_SENSE
VCCCORE_G32 VCCCORE_G33 VCCCORE_G35 VCCCORE_G37 VCCCORE_G38 VCCCORE_G40 VCCCORE_G42 VCCCORE_J30 VCCCORE_J33 VCCCORE_J37 VCCCORE_J40 VCCCORE_K33 VCCCORE_K35 VCCCORE_K37 VCCCORE_K38 VCCCORE_K40 VCCCORE_K42 VCCCORE_K43 G32 G33 G35 G37 G38 G40 G42 J30 J33 J37 J40 K33 K35 K37 K38 K40 K42 K43
VCC_SENSE VSS_SENSE E32 E33
VCC_CORE_SENSE [66]
VSS_CORE_SENSE [66]
VIDALERT# VIDSCK VIDSOUT B63 A63 D64
H_CPU_SVIDALERT_N R12005 220 0201
H_CPU_SVIDCLK R12006 0 0201
H_CPU_SVIDDAT R12007 0 0201
VCCSTG_G20 G20
VCCSTG
+VCCSTG is control by SLP_S0, but it can overwrite by XDP, that means it need power for XDP intrafece
VCCST_CPU
R12004 56 0201
R12003 100 0201
SVID_ALERT# [66]
VIDSCLK [66]
VIDSOUT [66]
REMOVED +VCCEDRAM & +VCCEOPIO RAILS
KBL-R U42
<$LOCATION>
<MATERIAL>
12 OF 20
REV = 1
U SPECIFIC
Title: 12. CPU(3)_SKL POWER1
Microsoft Confidential
Engineer: Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Tuesday, May 01, 2018
Sheet 12 of 79

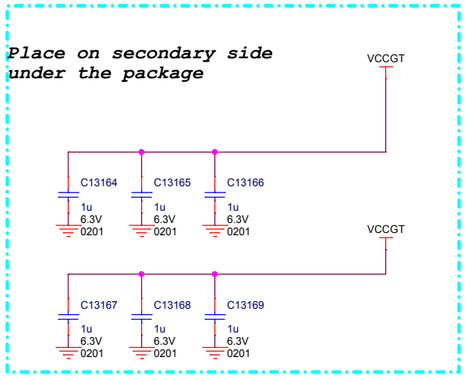


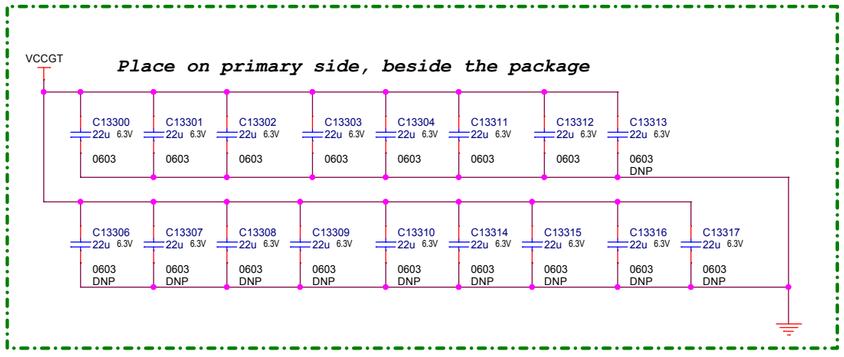
REMOVED GTX Connections

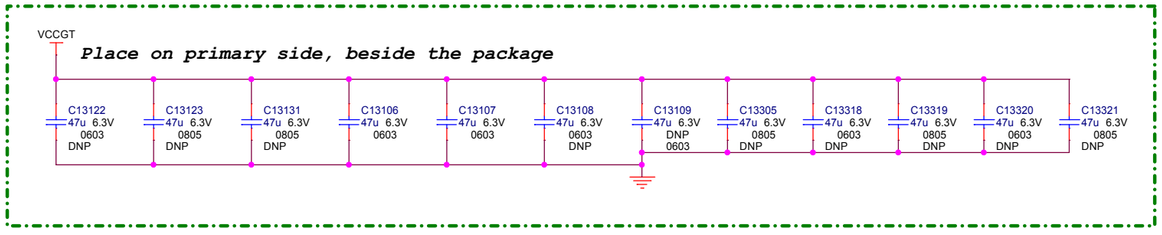












U SPECIFIC

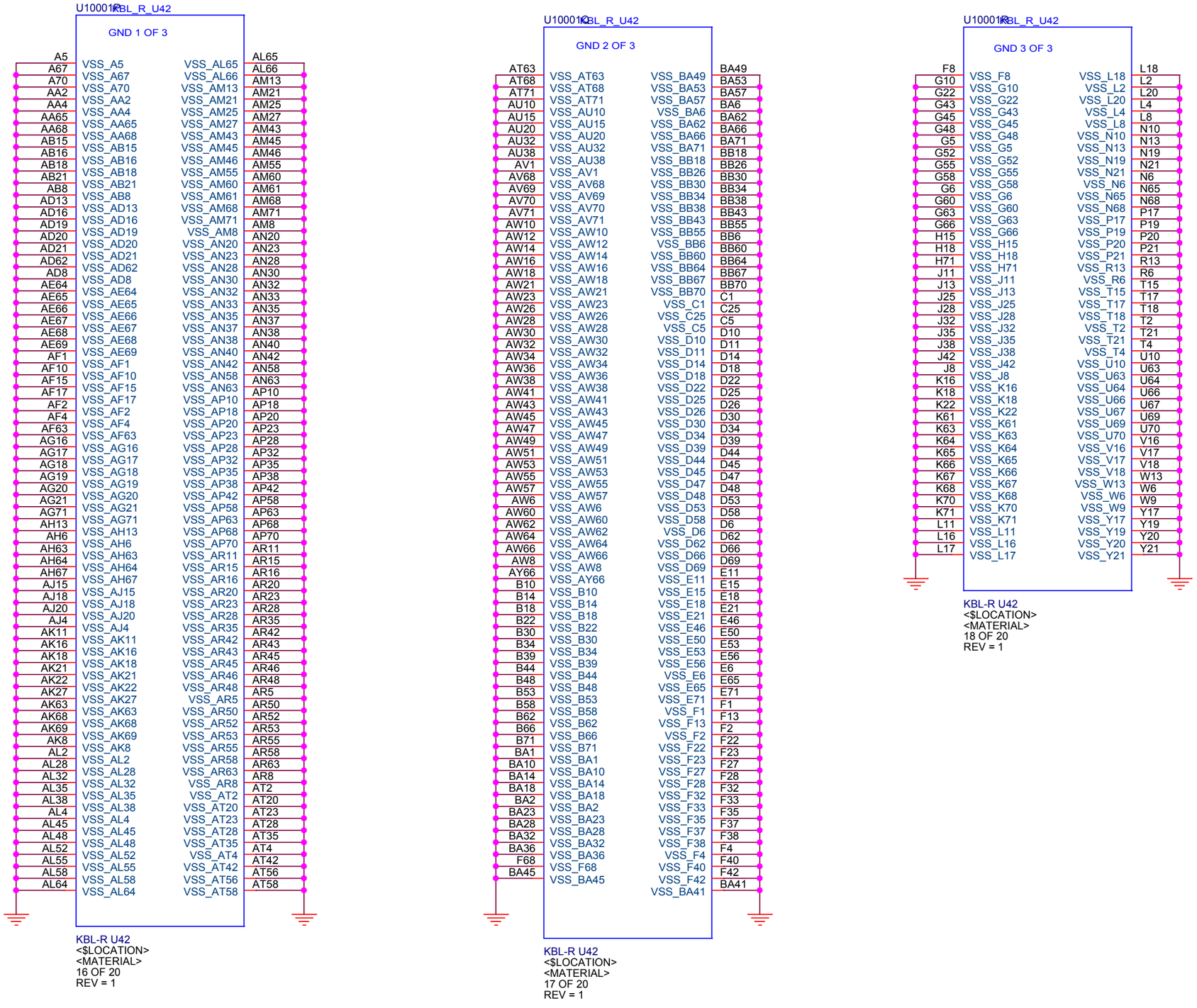
Microsoft Confidential

Title: 13. CPU(4)_SKL_POWER2

Engineer: Surface

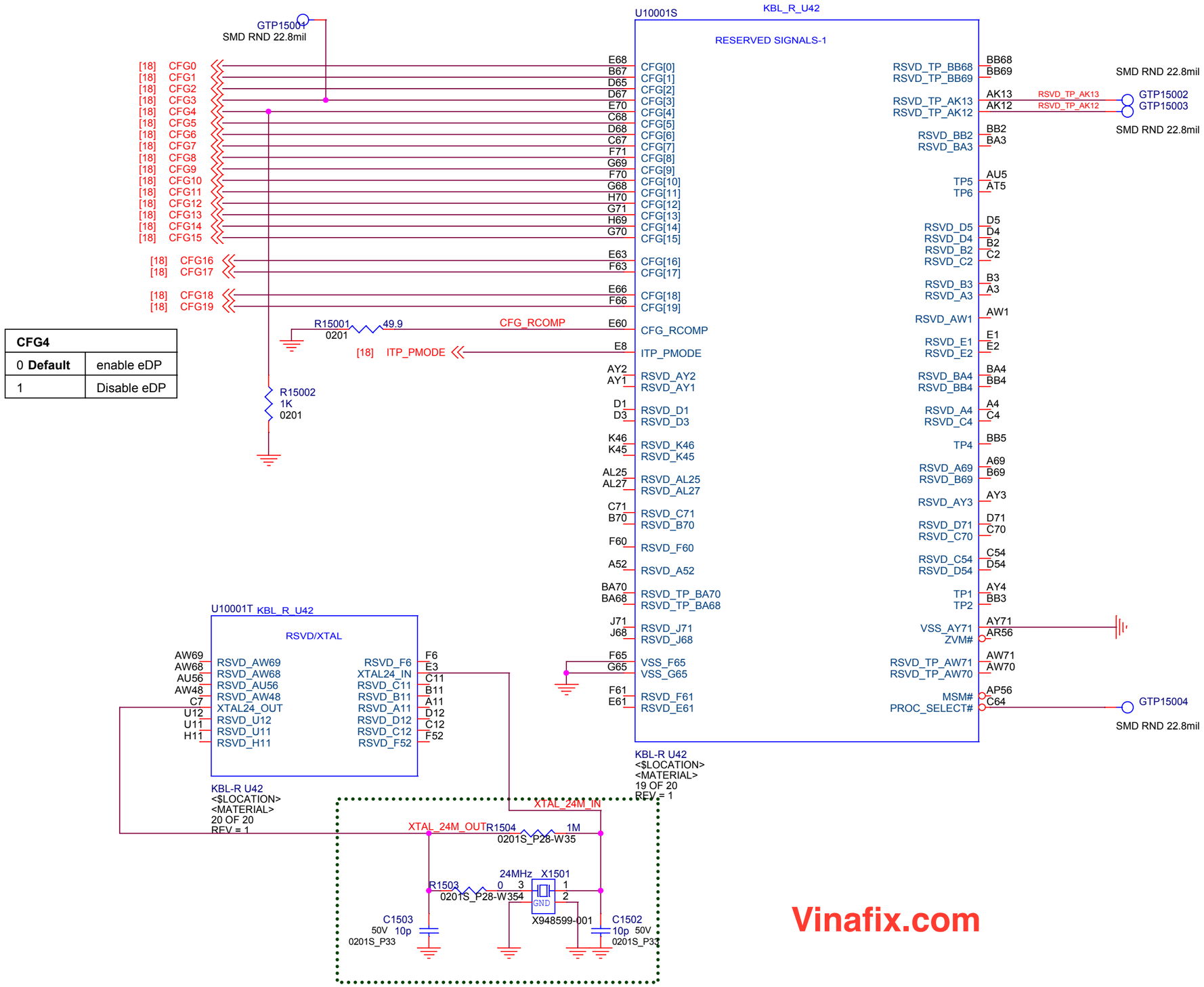
Size	Project Name	Rev
C	A	1.0.0.1

Date: Tuesday, May 01, 2018 Sheet 13 of 79



U SPECIFIC

Title:	14. CPU(5)_GND		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Friday, April 27, 2018	Sheet 14 of 79		


U10001S
KBL_R_U42
RESERVED SIGNALS-1
GTP15001
SMD RND 22.8mil
[18] CFG0
[18] CFG1
[18] CFG2
[18] CFG3
[18] CFG4
[18] CFG5
[18] CFG6
[18] CFG7
[18] CFG8
[18] CFG9
[18] CFG10
[18] CFG11
[18] CFG12
[18] CFG13
[18] CFG14
[18] CFG15
[18] CFG16
[18] CFG17
[18] CFG18
[18] CFG19
R15001 49.9 0201
CFG_RCOMP
[18] ITP_PMODE
R15002 1K 0201
CFG[0]
CFG[1]
CFG[2]
CFG[3]
CFG[4]
CFG[5]
CFG[6]
CFG[7]
CFG[8]
CFG[9]
CFG[10]
CFG[11]
CFG[12]
CFG[13]
CFG[14]
CFG[15]
CFG[16]
CFG[17]
CFG[18]
CFG[19]
CFG_RCOMP
ITP_PMODE
RSVD_AY2
RSVD_AY1
RSVD_D1
RSVD_D3
RSVD_K46
RSVD_K45
RSVD_AL25
RSVD_AL27
RSVD_C71
RSVD_B70
RSVD_F60
RSVD_A52
RSVD_TP_BA70
RSVD_TP_BA68
RSVD_J71
RSVD_J68
VSS_F65
VSS_G65
RSVD_F61
RSVD_E61
RSVD_TP_BB68
RSVD_TP_BB69
RSVD_TP_AK13
RSVD_TP_AK12
RSVD_BB2
RSVD_BA3
TP5
TP6
RSVD_D5
RSVD_D4
RSVD_B2
RSVD_C2
RSVD_B3
RSVD_A3
RSVD_AW1
RSVD_E1
RSVD_E2
RSVD_BA4
RSVD_BB4
RSVD_A4
RSVD_C4
TP4
RSVD_A69
RSVD_B69
RSVD_AY3
RSVD_D71
RSVD_C70
RSVD_C54
RSVD_D54
TP1
TP2
VSS_AY71
ZVM#
RSVD_TP_AW71
RSVD_TP_AW70
MSM#
PROC_SELECT#
SMD RND 22.8mil
GTP15002
GTP15003
SMD RND 22.8mil
GTP15004
SMD RND 22.8mil
ZVM# and MSM# may need to
control the VCCOPC and VCCEOPIO
U10001T KBL_R_U42
RSVD/XTAL
AW69 RSVD_AW69
AW68 RSVD_AW68
AU56 RSVD_AU56
AW48 RSVD_AW48
C7 XTAL24_OUT
U12 RSVD_U12
U11 RSVD_U11
H11 RSVD_H11
RSVD_F6 F6
XTAL24_IN E3
RSVD_C11 C11
RSVD_B11 B11
RSVD_A11 A11
RSVD_D12 D12
RSVD_C12 C12
RSVD_F52 F52
KBL-R U42
<$LOCATION>
<MATERIAL>
20 OF 20
REV = 1
KBL-R U42
<$LOCATION>
<MATERIAL>
19 OF 20
REV = 1
XTAL_24M_IN
XTAL_24M_OUT
R1504 1M 0201S_P28-W35
R1503 0201S_P28-W354
24MHz X1501
X948599-001
C1503 50V 10p 0201S_P33
C1502 10p 50V 0201S_P33
CFG4
0 Default enable eDP
1 Disable eDP
Vinafix.com
U SPECIFIC
Title: 15. CPU(6)_CFG_RESERVED
Microsoft Confidential
Engineer: Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Friday, April 27, 2018
Sheet 15 of 79

U16001
H9CCNNNBLTBLAR-NUD

U16002
H9CCNNNBLTBLAR-NUD

V0P6DX_LPDDR3

V_VREF_CA_DIMM

V_VREF_DQ_DIMM0

V1P8U_2P5U

V1P2U

GND

TBL1601

TBL1601, SEE PAGE 23

For 1.8V sensing

For 1.2V sensing

5 distributed. the Figure 4-56 at PDG2.0 the pink circle.

2 near each DRAM. Look the Figure 4-55 at PDG2.0 the pink circle.

5 distributed. Look the Figure 4-56 at PDG2.0 the blue circle.

3 near each DRAM. Look the Figure 4-55 at PDG2.0 the blue circle.

2 near each DRAM. Look the Figure 4-55 at PDG2.0 the red circle.

4 near each DRAM. Look the Figure 4-55 at PDG2.0 the red circle (big one).

5 distributed. Look the Figure 4-56 at PDG2.0 the red circle (VDDQ).

2 near each DRAM. Look the Figure 4-55 at PDG2.0 the yellow circle.

3 distributed. Look the Figure 4-56 at PDG2.0 the yellow circle.

DNP For 4GB System Memory: R16035, R16036

distributed along terminations. Shown in blue Figure 4-57 in PDG2.0

Edge of vtt island. Caps shown in green Figure 4-57 in PDG2.0

Vinafix.com

U SPECIFIC

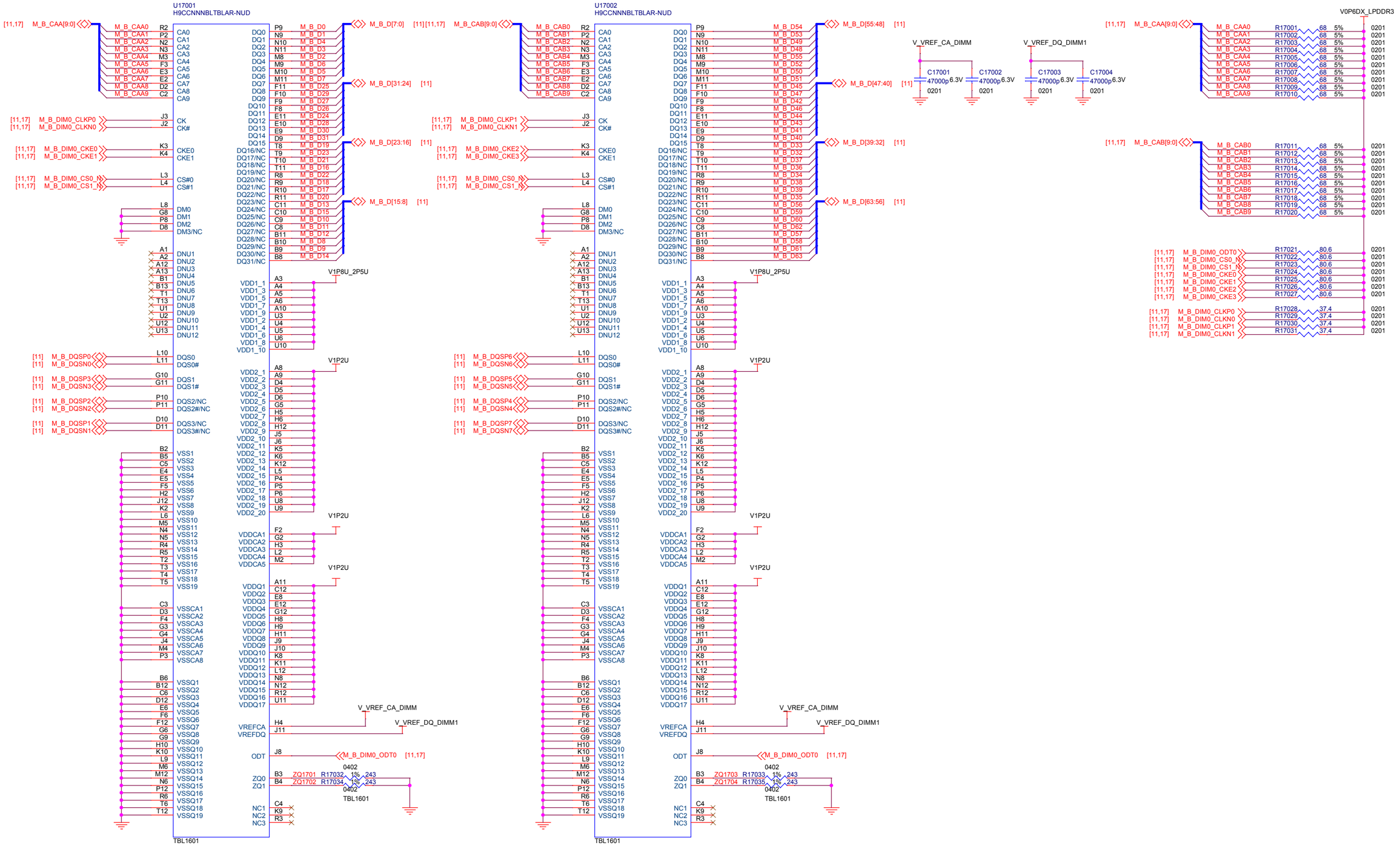
Title: 16. LPDDR3(1)_MEMORY DOWN

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
C	A	1.0.0.1

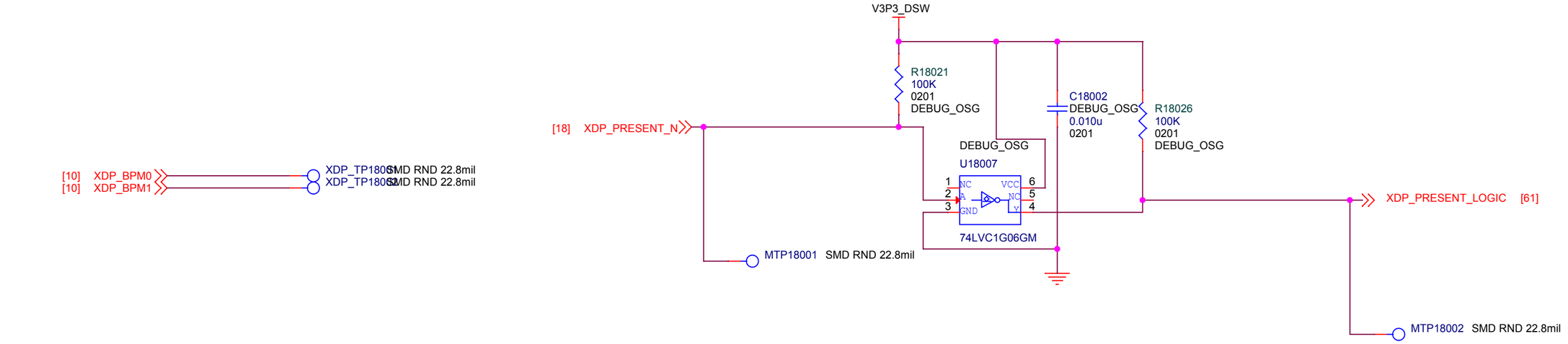
Date: Thursday, April 26, 2018 Sheet 16 of 79

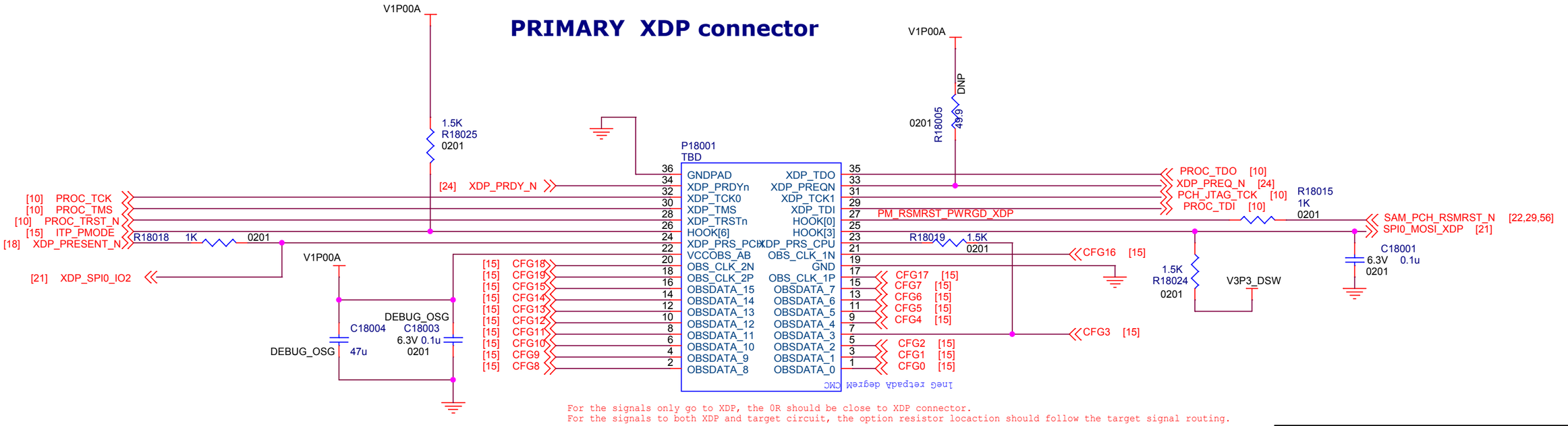


Vinafix.com

U SPECIFIC

Title:	17. LPDDR3(2)_MEMORY DOWN		
Microsoft Confidential	Engineer: Surface		
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 17 of 79		

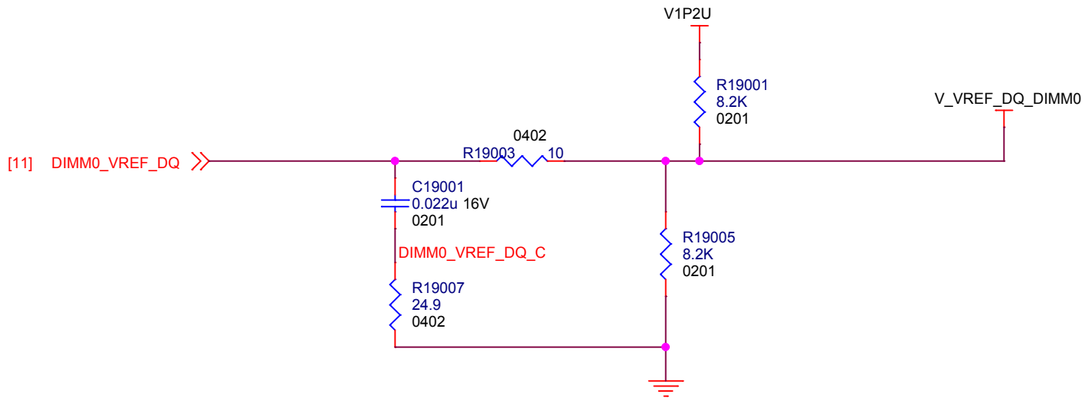


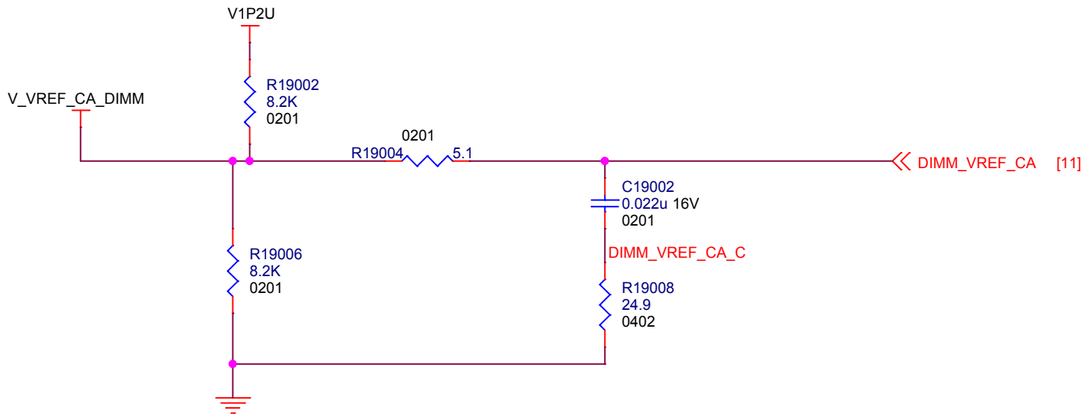


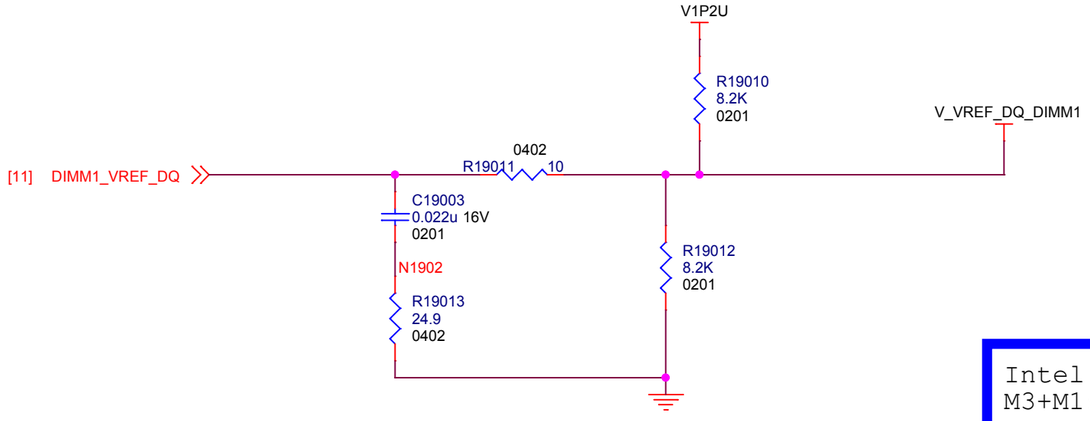
Title:	18. XDP		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 18 of 79		

LPDDR3 Vref

M3: CPU driven VREF path is stuffed by default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

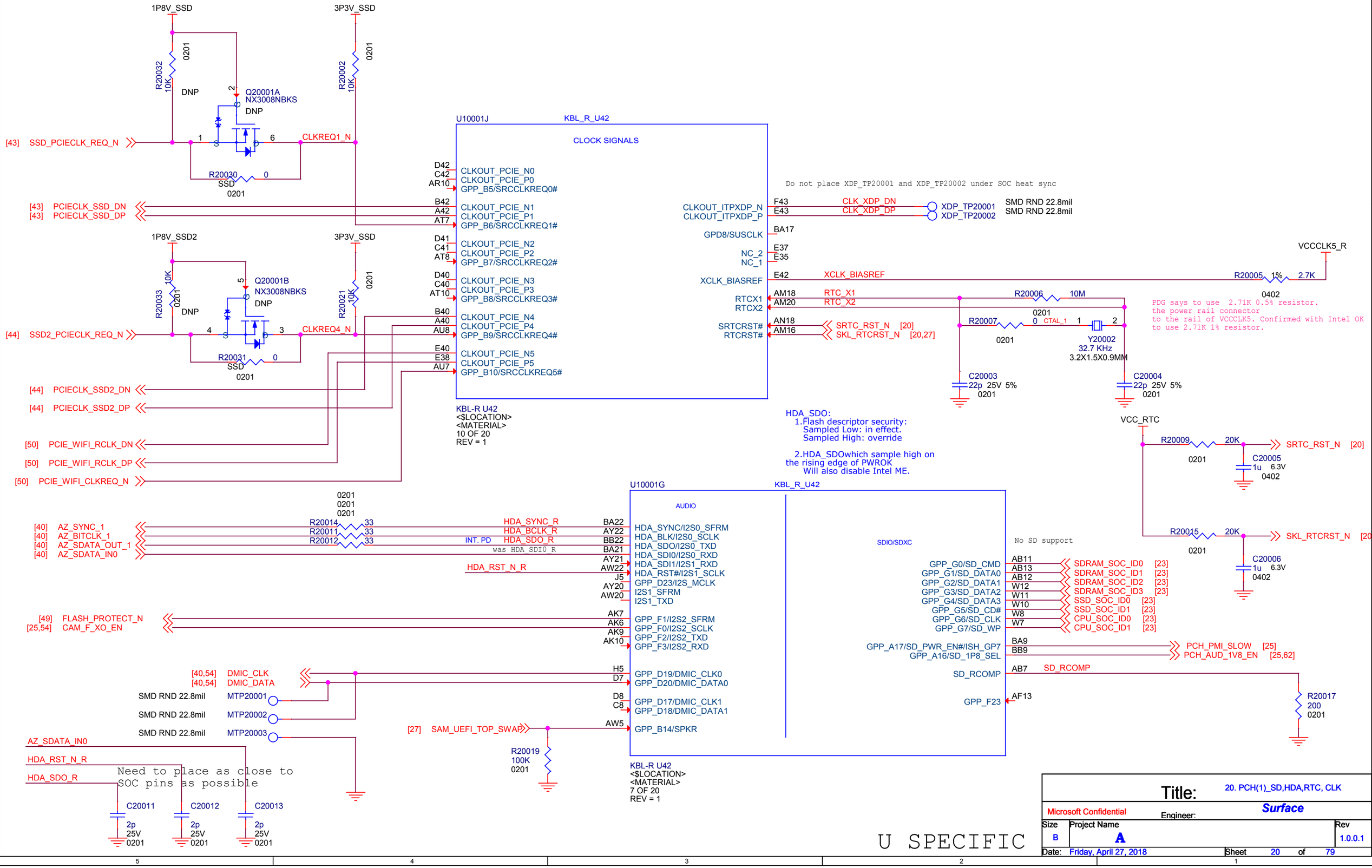






Intel 0203
M3+M1: Default Recommendation

Title:	19. LPDDR3(3)_CA/DQ Voltage	
Microsoft Confidential	Engineer: Surface	
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 19 of 79	


1P8V_SSD
3P3V_SSD
R20032 10K 0201
R20002 10K 0201
DNP
Q20001A NX3008NBKS
DNP
[43] SSD_PCIECLK_REQ_N
CLKREQ1_N
R20030 0 SSD 0201
[43] PCIECLK_SSD_DN
[43] PCIECLK_SSD_P
1P8V_SSD2
3P3V_SSD
R20033 10K 0201
R20021 10K 0201
Q20001B NX3008NBKS
DNP
[44] SSD2_PCIECLK_REQ_N
CLKREQ4_N
R20031 0 SSD 0201
[44] PCIECLK_SSD2_DN
[44] PCIECLK_SSD2_DP
[50] PCIE_WIFI_RCLK_DN
[50] PCIE_WIFI_RCLK_DP
[50] PCIE_WIFI_CLKREQ_N
U10001J
KBL_R_U42
CLOCK SIGNALS
D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5
E38 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#
KBL-R U42
<$LOCATION>
<MATERIAL>
10 OF 20
REV = 1
Do not place XDP_TP20001 and XDP_TP20002 under SOC heat sync
CLKOUT_ITPXDP_N F43 CLK_XDP_DN XDP_TP20001 SMD RND 22.8mil
CLKOUT_ITPXDP_P E43 CLK_XDP_DP XDP_TP20002 SMD RND 22.8mil
GPD8/SUSCLK BA17
NC_2 E37
NC_1 E35
XCLK_BIASREF E42 XCLK_BIASREF
R20005 1% 2.7K 0402
VCCCLK5_R
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2
R20006 10M 0201
R20007 0 CTAL_1 0201
Y20002 32.7 KHz 3.2X1.5X0.9MM
C20003 22p 25V 5% 0201
C20004 22p 25V 5% 0201
SRTCRST# AN18 SRTC_RST_N [20]
RTCRST# AM16 SKL_RTCRST_N [20,27]
PDG says to use 2.71K 0.5% resistor.
the power rail connector
to the rail of VCCCLK5. Confirmed with Intel OK
to use 2.71K 1% resistor.
HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.HDA_SDOwhich sample high on
the rising edge of PWROK
Will also disable Intel ME.
VCC_RTC
R20009 20K 0201
C20005 1u 6.3V 0402
SRTC_RST_N [20]
R20015 20K 0201
C20006 1u 6.3V 0402
SKL_RTCRST_N [20,27]
U10001G
KBL_R_U42
AUDIO
SDIO/SDXC
No SD support
[40] AZ_SYNC_1
[40] AZ_BITCLK_1
[40] AZ_SDATA_OUT_1
[40] AZ_SDATA_IN0
R20014 33
R20011 33
R20012 33
HDA_SYNC_R
HDA_BCLK_R
INT. PD HDA_SDO_R
was HDA_SDI0_R
BA22 HDA_SYNC/I2S0_SFRM
AY22 HDA_BLK/I2S0_SCLK
BB22 HDA_SDO/I2S0_TXD
BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
HDA_RST_N_R AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD
[49] FLASH_PROTECT_N
[25,54] CAM_F_XO_EN
AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD
[40,54] DMIC_CLK
[40,54] DMIC_DATA
H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1
SMD RND 22.8mil MTP20001
SMD RND 22.8mil MTP20002
SMD RND 22.8mil MTP20003
[27] SAM_UEFI_TOP_SWAP
AW5 GPP_B14/SPKR
R20019 100K 0201
KBL-R U42
<$LOCATION>
<MATERIAL>
7 OF 20
REV = 1
GPP_G0/SD_CMD AB11
GPP_G1/SD_DATA0 AB13
GPP_G2/SD_DATA1 AB12
GPP_G3/SD_DATA2 W12
GPP_G4/SD_DATA3 W11
GPP_G5/SD_CD# W10
GPP_G6/SD_CLK W8
GPP_G7/SD_WP W7
SDRAM_SOC_ID0 [23]
SDRAM_SOC_ID1 [23]
SDRAM_SOC_ID2 [23]
SDRAM_SOC_ID3 [23]
SSD_SOC_ID0 [23]
SSD_SOC_ID1 [23]
CPU_SOC_ID0 [23]
CPU_SOC_ID1 [23]
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9
GPP_A16/SD_1P8_SEL BB9
PCH_PMI_SLOW [25]
PCH_AUD_1V8_EN [25,62]
SD_RCOMP AB7
SD_RCOMP
R20017 200 0201
GPP_F23 AF13
AZ_SDATA_IN0
HDA_RST_N_R
HDA_SDO_R
Need to place as close to
SOC pins as possible
C20011 2p 25V 0201
C20012 2p 25V 0201
C20013 2p 25V 0201
U SPECIFIC
Title: 20. PCH(1)_SD,HDA,RTC, CLK
Microsoft Confidential
Engineer:
Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Friday, April 27, 2018
Sheet 20 of 79

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

[18] XDP_SPI0_IO2
[18] SPI0_MOSI_XDP

R21007 1K 0201
R21008 1K 0201

Close to PCH

[37] SPI_CLK
[37] SPI_SO
[37] SPI_SI
[37] SPI_WP_IO2
[37] SPI_HOLD_IO3_N
[37] SPI_CS0_N

R21011 15 0201 SPI_CLK_R
R21012 15 0201 SPI_SO_R
R21013 15 0201 SPI_SI_R
R21009 15 0201 SPI_WP_IO2_R
R21010 15 0201 SPI_HOLD_IO3_R_N
R21023 15 0201

[49] TS_SPI_CLK
[49] TS_SPI_MISO
[49] TS_SPI_MOSI

R21014 15 0201 TS_SPI_CLK_R
R21015 15 0201 TS_SPI_MISO_R
R21016 15 0201 TS_SPI_MOSI_R

[49] TS_SPI_CS_N

R21019 15 0201 TS_SPI_CS_N_R

3VSUS_ORG

R21029 10K 1% 0201

[38] TPM_SERIRQ — Serial Interrupt Request

U10001E

KBL_R_U42

SPI - FLASH

SPI0_CLK	AV2
SPI0_MISO	AW3
SPI0_MOSI	AV3
SPI0_IO2	AW2
SPI0_IO3	AU4
SPI0_CS0#	AU3
SPI0_CS1#	AU2
SPI0_CS2#	AU1

SPI_TOUCH

GPP_D1/SPI1_CLK	M2
GPP_D2/SPI1_MISO	M3
GPP_D3/SPI1_MOSI	J4
GPP_D21/SPI1_IO2	V1
GPP_D22/SPI1_IO3	V2
GPP_D0/SPI1_CS#	M1

C LINK

CL_CLK	G3
CL_DATA	G2
CL_RST#	G1

GPP_A0/RCIN#	AW13
GPP_A6/SERIRQ	AY11

SMBUS, SMLINK 1

GPP_C0/SMBCLK	R7
GPP_C1/SMBDATA	R8
GPP_C2/SMBALERT#	R10 INT. PD
GPP_C3/SML0CLK	R9
GPP_C4/SML0DATA	W2
GPP_C5/SML0ALERT#	W1 INT. PD was SMB0ALERT#
GPP_C6/SML1CLK	W3
GPP_C7/SML1DATA	V3
GPP_B23/SML1ALERT#/PCHHOT#	AM7 INT. PD

LPC

GPP_A1/LAD0/ESPI_IO0	AY13
GPP_A2/LAD1/ESPI_IO1	BA13
GPP_A3/LAD2/ESPI_IO2	BB13
GPP_A4/LAD3/ESPI_IO3	AY12
GPP_A5/LFRAME#/ESPI_CS#	BA12
GPP_A14/SUS_STAT#/ESPI_RESET#	BA11
GPP_A9/CLKOUT_LPC0/ESPI_CLK	AW9
GPP_A10/CLKOUT_LPC1	AY9
GPP_A8/CLKRUN#	AW11

KBL-R U42
<$LOCATION>
<MATERIAL>
5 OF 20
REV = 1

GPP_C5 - LPC boot mode selection - needs to be 0

R21004 10K 1% 0201
R21031 100K 1% 0201
GTP21013 SMD RND 22.8mil

TPM_LPC0 [38]
TPM_LPC1 [38]
TPM_LPC2 [38]
TPM_LPC3 [38]
TPM_LFRAME [38]
TPM_DEEPSLP_N [38]

CK_24M_EC_R — R21020 22 0201 — TPM_CLK [38]

C21002 10p 50V 0201 DNP

3VSUS_ORG
R21021 8.2K 0201
TPM_CLKRUN [38]

Need into improve LPC signals - P had in their latest design

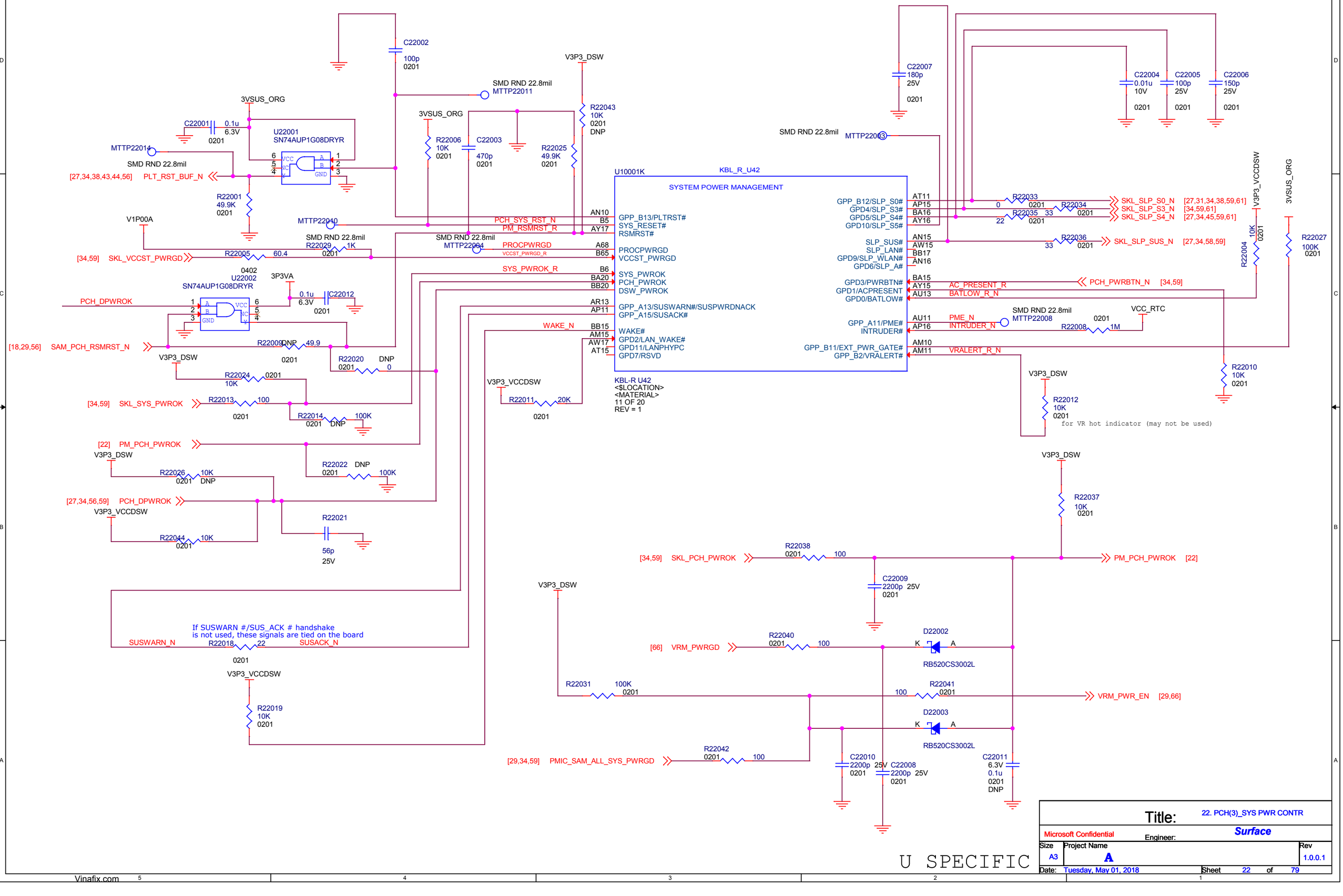
R21024 LAD0_SKL_TERM	R21027 LAD1_SKL_TERM	R21025 LAD2_SKL_TERM	R21026 LAD3_SKL_TERM	49.9 0201
C21003	C21006	C21004	C21005	56p 25V 0201

GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

Needs to be left open or low for booting

U SPECIFIC

Title:	21. PCH(2)_CLK,SMB,LPC, SPI		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Friday, April 27, 2018	Sheet 21 of 79		


C22002
100p
0201
V3P3_DSW
SMD RND 22.8mil
MTTP22011
3VSUS_ORG
C22001
0.1u
6.3V
0201
U22001
SN74AUP1G08DRYR
MTTP22014
SMD RND 22.8mil
[27,34,38,43,44,56] PLT_RST_BUF_N
R22001
49.9K
0201
3VSUS_ORG
R22006
10K
0201
C22003
470p
0201
R22025
49.9K
0201
R22043
10K
0201
DNP
V1P00A
MTTP22010
PCH_SYS_RST_N
PM_RSMRST_R
SMD RND 22.8mil
R22029
1K
0201
SMD RND 22.8mil
MTTP22004
PROCPWRGD
VCCST_PWRGD_R
[34,59] SKL_VCCST_PWRGD
R22005
60.4
0402
U22002
SN74AUP1G08DRYR
3P3VA
0.1u
6.3V
C22012
0201
PCH_DPWROK
SYS_PWROK_R
[18,29,56] SAM_PCH_RSMRST_N
R22009DNP
49.9
0201
V3P3_DSW
R22020
DNP
0
0201
R22024
10K
0201
[34,59] SKL_SYS_PWROK
R22013
100
0201
R22014
100K
0201
DNP
[22] PM_PCH_PWROK
V3P3_DSW
R22026
10K
0201
DNP
R22022
DNP
0201
100K
[27,34,56,59] PCH_DPWROK
V3P3_VCCDSW
R22021
56p
25V
R22044
10K
0201
If SUSWARN #/SUS_ACK # handshake
is not used, these signals are tied on the board
SUSWARN_N
R22018
22
SUSACK_N
0201
V3P3_VCCDSW
R22019
10K
0201
U10001K
KBL_R_U42
SYSTEM POWER MANAGEMENT
AN10
B5
AY17
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
A68
B65
PROCPWRGD
VCCST_PWRGD
B6
BA20
BB20
SYS_PWROK
PCH_PWROK
DSW_PWROK
AR13
AP11
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE_N
BB15
AM15
AW17
AT15
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD
KBL-R U42
<$LOCATION>
<MATERIAL>
11 OF 20
REV = 1
V3P3_VCCDSW
R22011
20K
0201
C22007
180p
25V
0201
SMD RND 22.8mil
MTTP22003
C22004
0.01u
10V
0201
C22005
100p
25V
0201
C22006
150p
25V
0201
AT11
AP15
BA16
AY16
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
R22033
0
0201
R22034
33
0201
R22035
22
0201
SKL_SLP_S0_N [27,31,34,38,59,61]
SKL_SLP_S3_N [34,59,61]
SKL_SLP_S4_N [27,34,45,59,61]
AN15
AW15
BB17
AN16
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
R22036
33
0201
SKL_SLP_SUS_N [27,34,58,59]
BA15
AY15
AU13
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
PCH_PWRBTN_N [34,59]
AC_PRESENT_R
BATLOW_R_N
AU11
AP16
GPP_A11/PME#
INTRUDER#
PME_N
INTRUDER_N
SMD RND 22.8mil
MTTP22008
R22008
1M
0201
VCC_RTC
AM10
AM11
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
VRALERT_R_N
V3P3_VCCDSW
3VSUS_ORG
R22004
10K
0201
R22027
100K
0201
R22010
10K
0201
V3P3_DSW
R22012
10K
0201
for VR hot indicator (may not be used)
V3P3_DSW
R22037
10K
0201
[34,59] SKL_PCH_PWROK
R22038
0201
100
PM_PCH_PWROK [22]
C22009
2200p 25V
0201
V3P3_DSW
[66] VRM_PWRGD
R22040
0201
100
D22002
K A
RB520CS3002L
R22031
100K
0201
100
R22041
0201
VRM_PWR_EN [29,66]
D22003
K A
RB520CS3002L
[29,34,59] PMIC_SAM_ALL_SYS_PWRGD
R22042
0201
100
C22010
2200p 25V
0201
C22008
2200p 25V
0201
C22011
6.3V
0.1u
0201
DNP
U SPECIFIC
Title: 22. PCH(3)_SYS PWR CONTR
Microsoft Confidential
Engineer:
Surface
Size A3
Project Name A
Rev 1.0.0.1
Date: Tuesday, May 01, 2018
Sheet 22 of 79
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TBL2301B

R23016, R28013 LOAD FOR DEBUG, ELSE NO-STUFF

R23023, R28024 LOAD FOR RETAIL, ELSE NO-STUFF

TBL2301A

R23015, R28014 NEW BOARDID SYSTEM, ELSE NO-STUFF

R23022, R28025 OLD BOARDID SYSTEM, ELSE NO-STUFF

TBL2301 PCBA vendor and revision

R23010, R23020, R23024	Revision EV2P5
R23005, R23013, R23017, R28051, R28052, R28053	NO-STUFF FOR REVISION
R23005, R23020, R23024, R28051	Revision EV2P51
R23010, R23013, R23017, R28052, R28053	NO-STUFF FOR REVISION
R23010, R23013, R23024, R28052	Revision DV
R23005, R23020, R23017, R28051, R28053	NO-STUFF FOR REVISION
R23005, R23013, R23024, R28051, R28052	Revision DV1.01
R23010, R23020, R23017, R28053	NO-STUFF FOR REVISION
R23010, R23020, R23017, R28053	Revision DV1.1, DV1.2, PV
R23005, R23013, R23024, R28051, R28052	NO-STUFF FOR REVISION
R23005, R23020, R23017, R28051, R28053	Lacey EV1
R23010, R23013, R23024, R28052	NO-STUFF FOR REVISION
R23010, R23013, R23017, R28052, R28053	Reserved
R23005, R23020, R23024, R28051	NO-STUFF FOR REVISION
R23005, R23013, R23017, R28051, R28052, R28053	Reserved
R23010, R23020, R23024	NO-STUFF FOR REVISION

TBL_SSD_2302

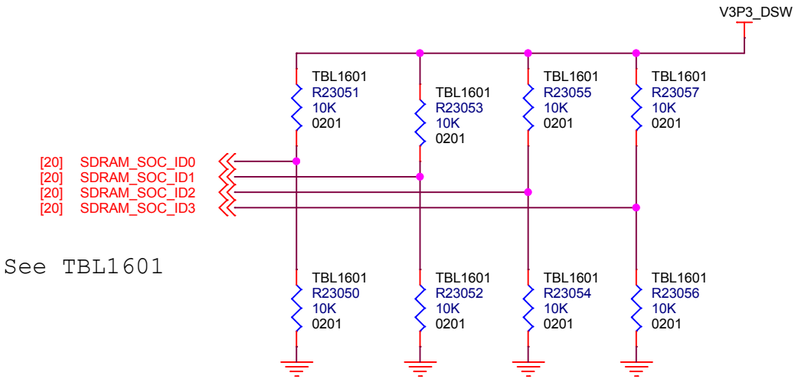
BoardID	SSD vendor	stuff	No-Stuff
00	Toshiba SSD	R23030, R23032	R23031, R23033, R28081, R28082
01	SAMSUNG SSD	R23031, R23032, R28081	R23030, R23033, R28082
10	INTEL PS SSD	R23030, R23033, R28082	R23031, R23032, R28081
11	Hynix SSD	R23031, R23033, R28081, R28082	R23030, R23032

TBL2304

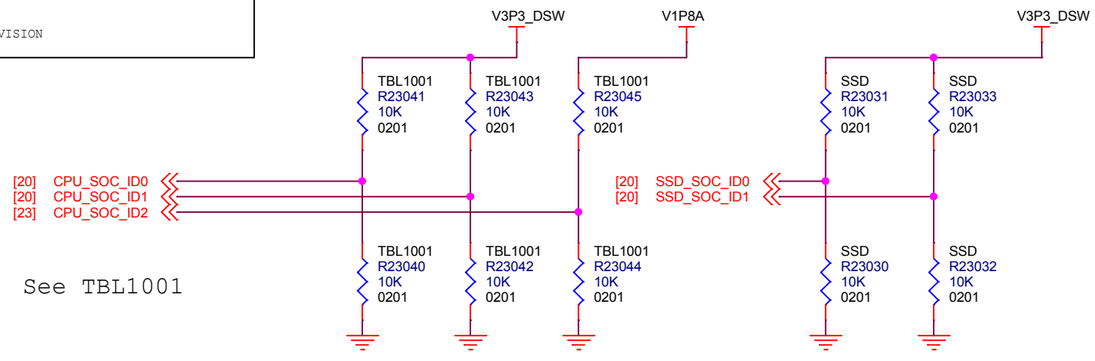
BoardID	GreenPak Revision	stuff	No-Stuff
00	Initial release, Mxxxxxx-001	R23008, R23009	R23003, R23004, R28061, R28062
01	1st new revision	R23003, R23009, R28061	R23008, R23004, R28062
10	2nd new revision	R23008, R23004, R28062	R23003, R23009, R28061
11	3rd new revision	R23003, R23004, R28061, R28062	R23008, R23009

TBL1601

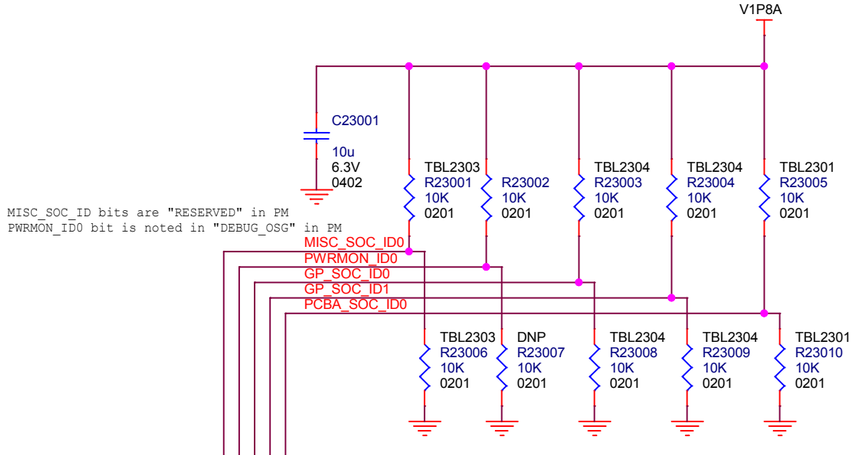
BoardID	sdram vendor and revision	Size	stuff	No-Stuff
0000	Hynix: H9CCNNN8JTBLAR-NUD, 8Gb LPDDR3	4GB	R23050, R23052, R23054, R2305	R23051, R23053, R23055, R23057
0001	Samsung: K4E8E324EB-EGCF000, 8Gb LPDDR3	4GB	R23051, R23052, R23054, R2305	R23050, R23053, R23055, R23057
0010	Hynix: H9CCNNN8GTALAR-NUD, 8gB LPDDR3	4GB	R23050, R23053, R23054, R2305	R23051, R23052, R23055, R23057
0011	Reserved	4GB	R23051, R23053, R23054, R2305	R23050, R23052, R23055, R23057
0100	Hynix: H9CCNNNBLTBLAR-NUD, 16Gb LPDDR3	8GB	R23050, R23052, R23055, R2305	R23051, R23053, R23054, R23057
0101	Samsung: K4E6E304EB-EGCF000, 16Gb LPDDR3	8GB	R23051, R23052, R23055, R2305	R23050, R23053, R23054, R23057
0110	Hynix: H9CCNNNBJTALAR-NUD, 16Gb LPDDR3	8GB	R23050, R23053, R23055, R2305	R23051, R23052, R23054, R23057
0111	Reserved	8GB	R23051, R23053, R23055, R2305	R23050, R23052, R23054, R23057
1000	Hynix: H9CCNNNCLTMLBR-NUD, 32Gb LPDDR3	16GB	R23050, R23052, R23054, R2305	R23051, R23053, R23055, R23056
1001	Samsung: K4EBE304EB-EGCF000, 32Gb LPDDR3	16GB	R23051, R23052, R23054, R2305	R23050, R23053, R23055, R23056
1010	Hynix: H9CCNNNCLGALAR-NUD, 32Gb LPDDR3	16GB	R23050, R23053, R23054, R2305	R23051, R23052, R23055, R23056
1011	Reserved	16GB	R23051, R23053, R23054, R2305	R23050, R23052, R23055, R23056
1100	Reserved	Reserved	R23050, R23052, R23055, R2305	R23051, R23053, R23054, R23056
1101	Reserved	Reserved	R23051, R23052, R23055, R2305	R23050, R23053, R23054, R23056
1110	Reserved	Reserved	R23050, R23053, R23055, R2305	R23051, R23052, R23054, R23056
1111	Reserved	Reserved	R23051, R23053, R23055, R2305	R23050, R23052, R23054, R23056

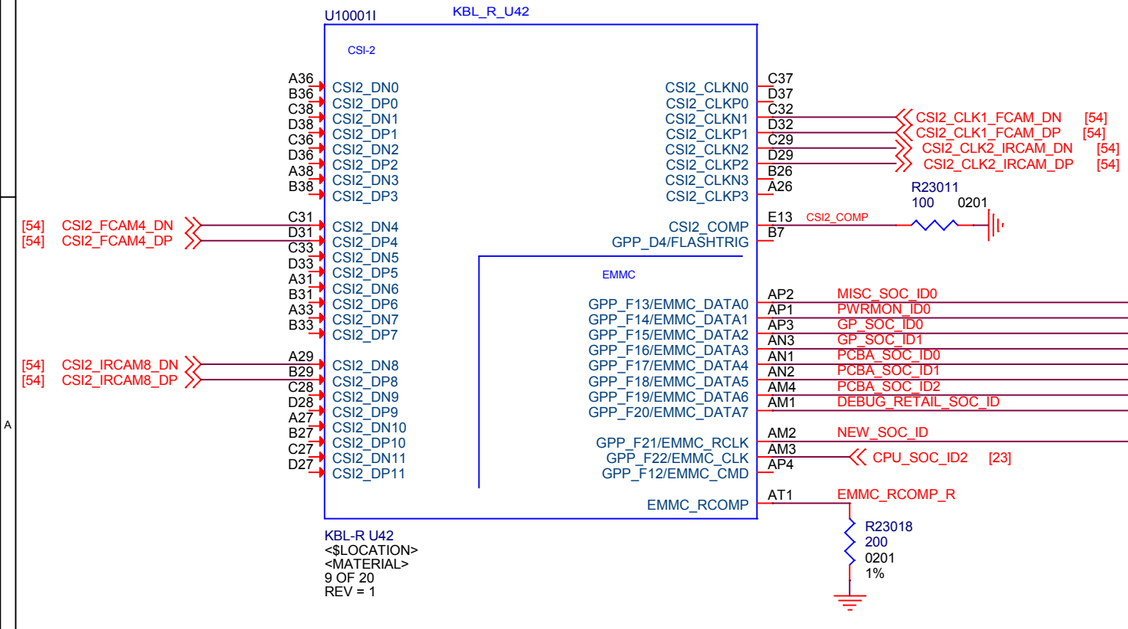


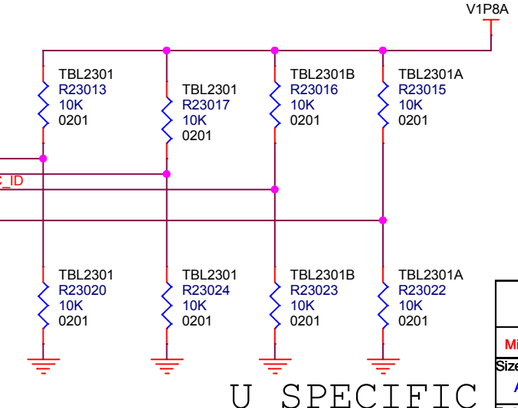
See TBL1601



See TBL1001







POWER MONITORS

R23007 POWER MONITORS, ELSE NO-STUFF

R23002 NO POWER MONITORS, ELSE NO-STUFF

DV HAS NO POWER MONITORS

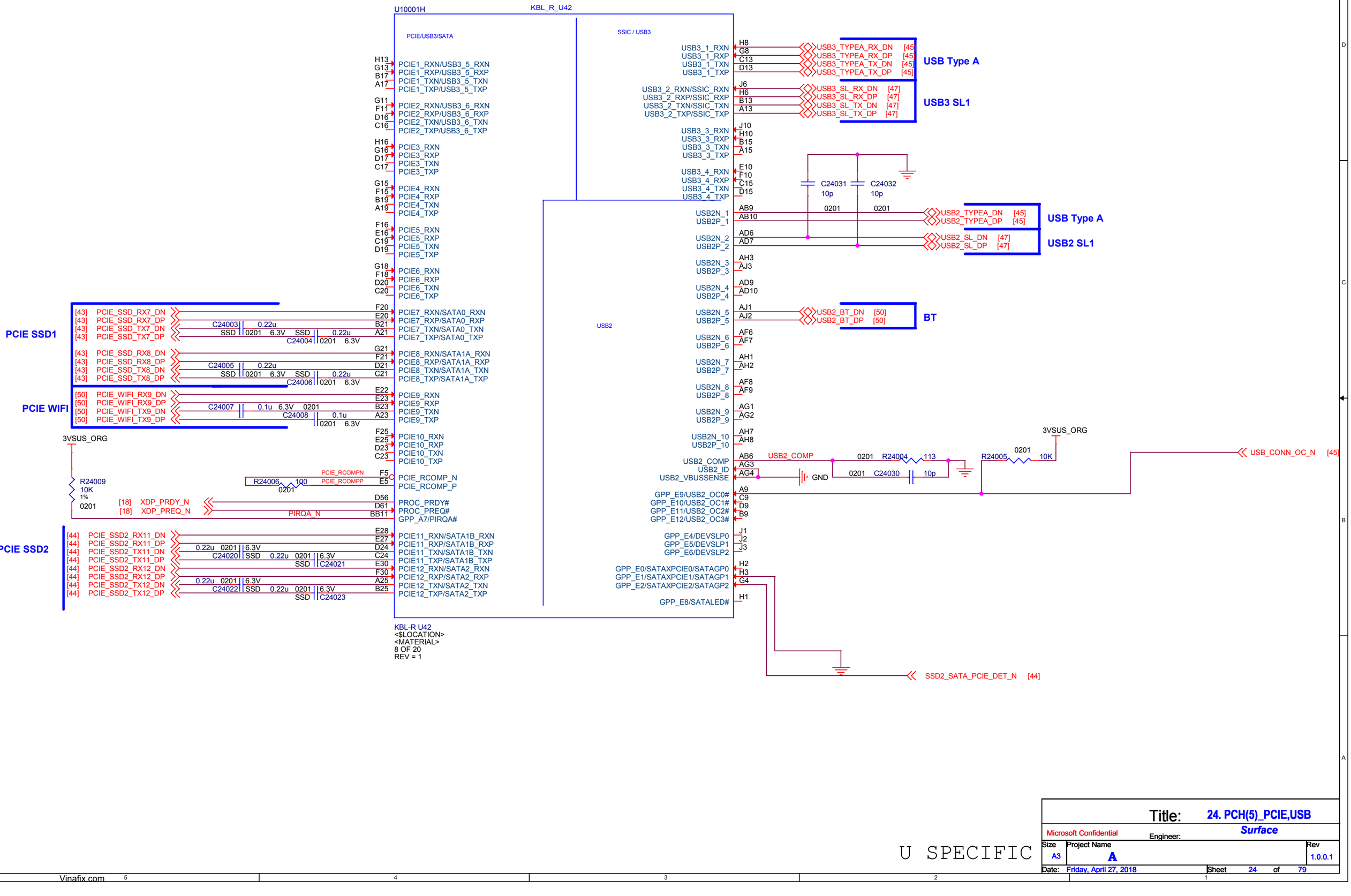
U SPECIFIC

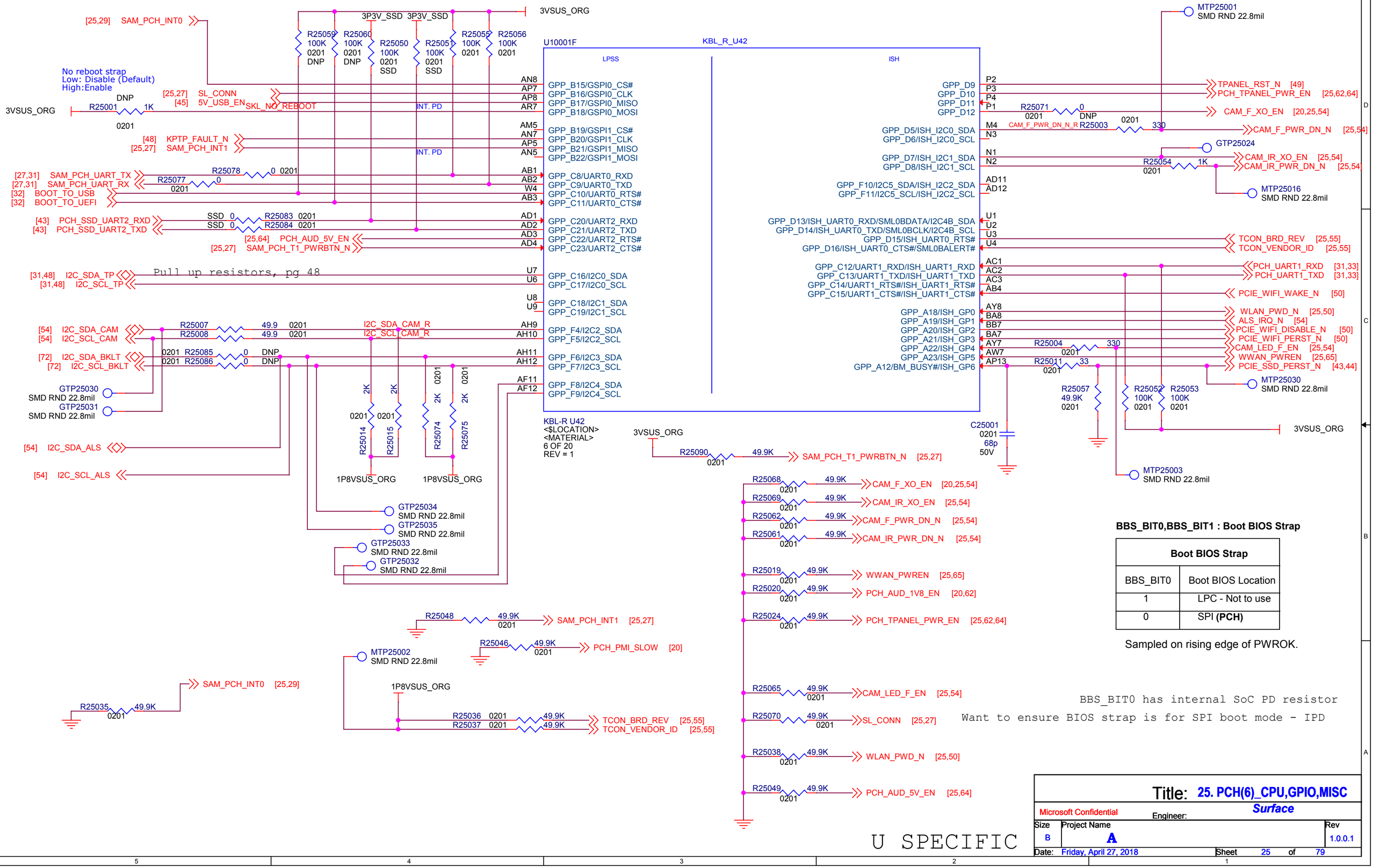
Title: 23. PCH(4)_CCI, HWID

Microsoft Confidential Engineer: Surface

Size	Project Name	Rev
A3	A	1.0.0.1

Date: Friday, April 27, 2018 Sheet 23 of 79


U10001H
KBL_R_U42
PCIE/USB3/SATA
SSIC / USB3
USB2
H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP
G11 PCIE2_RXN/USB3_6_RXN
F11 PCIE2_RXP/USB3_6_RXP
D16 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP
H16 PCIE3_RXN
G16 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP
G15 PCIE4_RXN
F15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP
F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP
G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP
F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP
G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP
E22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP
F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP
F5 PCIE_RCOMP_N
E5 PCIE_RCOMP_P
D56 PROC_PRDY#
D61 PROC_PREQ#
BB11 GPP_A7/PIRQA#
E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP
E30 PCIE12_RXN/SATA2_RXN
F30 PCIE12_RXP/SATA2_RXP
A25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP
PCIE_RCOMPN
PCIE_RCOMPP
R24006 100 0201
PCIE SSD1
[43] PCIE_SSD_RX7_DN
[43] PCIE_SSD_RX7_DP
[43] PCIE_SSD_TX7_DN
[43] PCIE_SSD_TX7_DP
C24003 0.22u SSD 0201 6.3V
C24004 SSD 0.22u 0201 6.3V
[43] PCIE_SSD_RX8_DN
[43] PCIE_SSD_RX8_DP
[43] PCIE_SSD_TX8_DN
[43] PCIE_SSD_TX8_DP
C24005 0.22u SSD 0201 6.3V
C24006 SSD 0.22u 0201 6.3V
PCIE WIFI
[50] PCIE_WIFI_RX9_DN
[50] PCIE_WIFI_RX9_DP
[50] PCIE_WIFI_TX9_DN
[50] PCIE_WIFI_TX9_DP
C24007 0.1u 6.3V 0201
C24008 0.1u 0201 6.3V
3VSUS_ORG
R24009 10K 1% 0201
[18] XDP_PRDY_N
[18] XDP_PREQ_N
PIRQA_N
PCIE SSD2
[44] PCIE_SSD2_RX11_DN
[44] PCIE_SSD2_RX11_DP
[44] PCIE_SSD2_TX11_DN
[44] PCIE_SSD2_TX11_DP
[44] PCIE_SSD2_RX12_DN
[44] PCIE_SSD2_RX12_DP
[44] PCIE_SSD2_TX12_DN
[44] PCIE_SSD2_TX12_DP
0.22u 0201 6.3V C24020 SSD 0.22u 0201 6.3V SSD C24021
0.22u 0201 6.3V C24022 SSD 0.22u 0201 6.3V SSD C24023
KBL-R U42
<$LOCATION>
<MATERIAL>
8 OF 20
REV = 1
USB3_1_RXN H8
USB3_1_RXP G8
USB3_1_TXN C13
USB3_1_TXP D13
USB3_TYPEA_RX_DN [45]
USB3_TYPEA_RX_DP [45]
USB3_TYPEA_TX_DN [45]
USB3_TYPEA_TX_DP [45]
USB Type A
USB3_2_RXN/SSIC_RXN J6
USB3_2_RXP/SSIC_RXP H6
USB3_2_TXN/SSIC_TXN B13
USB3_2_TXP/SSIC_TXP A13
USB3_SL_RX_DN [47]
USB3_SL_RX_DP [47]
USB3_SL_TX_DN [47]
USB3_SL_TX_DP [47]
USB3 SL1
USB3_3_RXN J10
USB3_3_RXP H10
USB3_3_TXN B15
USB3_3_TXP A15
USB3_4_RXN E10
USB3_4_RXP F10
USB3_4_TXN C15
USB3_4_TXP D15
C24031 10p 0201
C24032 10p 0201
USB2N_1 AB9
USB2P_1 AB10
USB2_TYPEA_DN [45]
USB2_TYPEA_DP [45]
USB Type A
USB2N_2 AD6
USB2P_2 AD7
USB2_SL_DN [47]
USB2_SL_DP [47]
USB2 SL1
USB2N_3 AH3
USB2P_3 AJ3
USB2N_4 AD9
USB2P_4 AD10
USB2N_5 AJ1
USB2P_5 AJ2
USB2_BT_DN [50]
USB2_BT_DP [50]
BT
USB2N_6 AF6
USB2P_6 AF7
USB2N_7 AH1
USB2P_7 AH2
USB2N_8 AF8
USB2P_8 AF9
USB2N_9 AG1
USB2P_9 AG2
USB2N_10 AH7
USB2P_10 AH8
USB2_COMP AB6
USB2_ID AG3
USB2_VBUSSENSE AG4
USB2_COMP 0201 R24004 113
GND 0201 C24030 10p
3VSUS_ORG
R24005 0201 10K
USB_CONN_OC_N [45]
GPP_E9/USB2_OC0# A9
GPP_E10/USB2_OC1# C9
GPP_E11/USB2_OC2# D9
GPP_E12/USB2_OC3# B9
GPP_E4/DEVSLP0 J1
GPP_E5/DEVSLP1 J2
GPP_E6/DEVSLP2 J3
GPP_E0/SATAXPCIE0/SATAGP0 H2
GPP_E1/SATAXPCIE1/SATAGP1 H3
GPP_E2/SATAXPCIE2/SATAGP2 G4
GPP_E8/SATALED# H1
SSD2_SATA_PCIE_DET_N [44]
U SPECIFIC
Title: 24. PCH(5)_PCIE,USB
Microsoft Confidential
Engineer:
Surface
Size A3
Project Name A
Rev 1.0.0.1
Date: Friday, April 27, 2018
Sheet 24 of 79
Vinafix.com


3VSUS_ORG
3P3V_SSD 3P3V_SSD
[25,29] SAM_PCH_INT0
R25059 100K 0201 DNP
R25060 100K 0201 DNP
R25050 100K 0201 SSD
R25051 100K 0201 SSD
R25055 100K 0201
R25056 100K 0201
U10001F
KBL_R_U42
LPSS
ISH
No reboot strap
Low: Disable (Default)
High:Enable
DNP
3VSUS_ORG R25001 1K 0201
[25,27] SL_CONN
[45] 5V_USB_EN
SKL_NO_REBOOT
INT. PD
[48] KPTP_FAULT_N
[25,27] SAM_PCH_INT1
INT. PD
[27,31] SAM_PCH_UART_TX
[27,31] SAM_PCH_UART_RX
[32] BOOT_TO_USB
[32] BOOT_TO_UEFI
R25078 0 0201
R25077 0 0201
[43] PCH_SSD_UART2_RXD
[43] PCH_SSD_UART2_TXD
SSD 0 R25083 0201
SSD 0 R25084 0201
[25,64] PCH_AUD_5V_EN
[25,27] SAM_PCH_T1_PWRBTN_N
[31,48] I2C_SDA_TP
[31,48] I2C_SCL_TP
Pull up resistors, pg 48
[54] I2C_SDA_CAM
[54] I2C_SCL_CAM
R25007 49.9 0201
R25008 49.9 0201
I2C_SDA_CAM_R
I2C_SCL_CAM_R
[72] I2C_SDA_BKLT
[72] I2C_SCL_BKLT
0201 R25085 0 DNP
0201 R25086 0 DNP
GTP25030 SMD RND 22.8mil
GTP25031 SMD RND 22.8mil
[54] I2C_SDA_ALS
[54] I2C_SCL_ALS
2K 0201
R25014
R25015
1P8VSUS_ORG
R25074
R25075
GTP25034 SMD RND 22.8mil
GTP25035 SMD RND 22.8mil
GTP25033 SMD RND 22.8mil
GTP25032 SMD RND 22.8mil
KBL-R U42
<$LOCATION>
<MATERIAL>
6 OF 20
REV = 1
GPP_B15/GSPI0_CS#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_F4/I2C2_SDA
GPP_F5/I2C2_SCL
GPP_F6/I2C3_SDA
GPP_F7/I2C3_SCL
GPP_F8/I2C4_SDA
GPP_F9/I2C4_SCL
AN8 AP7 AP8 AR7 AM5 AN7 AP5 AN5 AB1 AB2 W4 AB3 AD1 AD2 AD3 AD4 U7 U6 U8 U9 AH9 AH10 AH11 AH12 AF11 AF12
GPP_D9 GPP_D10 GPP_D11 GPP_D12
GPP_D5/ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL
GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL
GPP_F10/I2C5_SDA/ISH_I2C2_SDA
GPP_F11/I2C5_SCL/ISH_I2C2_SCL
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
GPP_D15/ISH_UART0_RTS#
GPP_D16/ISH_UART0_CTS#/SML0BALERT#
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
GPP_A12/BM_BUSY#/ISH_GP6
P2 P3 P4 P1 M4 N3 N1 N2 AD11 AD12 U1 U2 U3 U4 AC1 AC2 AC3 AB4 AY8 BA8 BB7 BA7 AY7 AW7 AP13
MTP25001 SMD RND 22.8mil
TPANEL_RST_N [49]
PCH_TPANEL_PWR_EN [25,62,64]
CAM_F_XO_EN [20,25,54]
R25071 0 0201 DNP
CAM_F_PWR_DN_N_R R25003 330 0201
CAM_F_PWR_DN_N [25,54]
GTP25024
R25054 1K 0201
CAM_IR_XO_EN [25,54]
CAM_IR_PWR_DN_N [25,54]
MTP25016 SMD RND 22.8mil
TCON_BRD_REV [25,55]
TCON_VENDOR_ID [25,55]
PCH_UART1_RXD [31,33]
PCH_UART1_TXD [31,33]
PCIE_WIFI_WAKE_N [50]
WLAN_PWD_N [25,50]
ALS_IRQ_N [54]
PCIE_WIFI_DISABLE_N [50]
PCIE_WIFI_PERST_N [50]
CAM_LED_F_EN [25,54]
WWAN_PWREN [25,65]
PCIE_SSD_PERST_N [43,44]
R25004 330 0201
R25011 33 0201
R25057 49.9K 0201
R25052 100K 0201
R25053 100K 0201
MTP25030 SMD RND 22.8mil
3VSUS_ORG
C25001 0201 68p 50V
MTP25003 SMD RND 22.8mil
3VSUS_ORG
R25090 49.9K 0201
SAM_PCH_T1_PWRBTN_N [25,27]
R25068 49.9K 0201
CAM_F_XO_EN [20,25,54]
R25069 49.9K 0201
CAM_IR_XO_EN [25,54]
R25062 49.9K 0201
CAM_F_PWR_DN_N [25,54]
R25061 49.9K 0201
CAM_IR_PWR_DN_N [25,54]
R25019 49.9K 0201
WWAN_PWREN [25,65]
R25020 49.9K 0201
PCH_AUD_1V8_EN [20,62]
R25024 49.9K 0201
PCH_TPANEL_PWR_EN [25,62,64]
R25048 49.9K 0201
SAM_PCH_INT1 [25,27]
R25046 49.9K 0201
PCH_PMI_SLOW [20]
MTP25002 SMD RND 22.8mil
1P8VSUS_ORG
R25036 0201 49.9K
R25037 0201 49.9K
TCON_BRD_REV [25,55]
TCON_VENDOR_ID [25,55]
R25035 49.9K 0201
SAM_PCH_INT0 [25,29]
R25065 49.9K 0201
CAM_LED_F_EN [25,54]
R25070 49.9K 0201
SL_CONN [25,27]
R25038 49.9K 0201
WLAN_PWD_N [25,50]
R25049 49.9K 0201
PCH_AUD_5V_EN [25,64]
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT0 | Boot BIOS Location
1 | LPC - Not to use
0 | SPI (PCH)
Sampled on rising edge of PWROK.
BBS_BIT0 has internal SoC PD resistor
Want to ensure BIOS strap is for SPI boot mode - IPD
U SPECIFIC
Title: 25. PCH(6)_CPU,GPIO,MISC
Microsoft Confidential
Engineer:
Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Friday, April 27, 2018
Sheet 25 of 79

Put this logic at near SOC VCCPRIM.

U10001O KBL_R_U42

CPU POWER 4 OF 4

KBL-R U42
<$LOCATION>
<MATERIAL>
15 OF 20
REV = 1

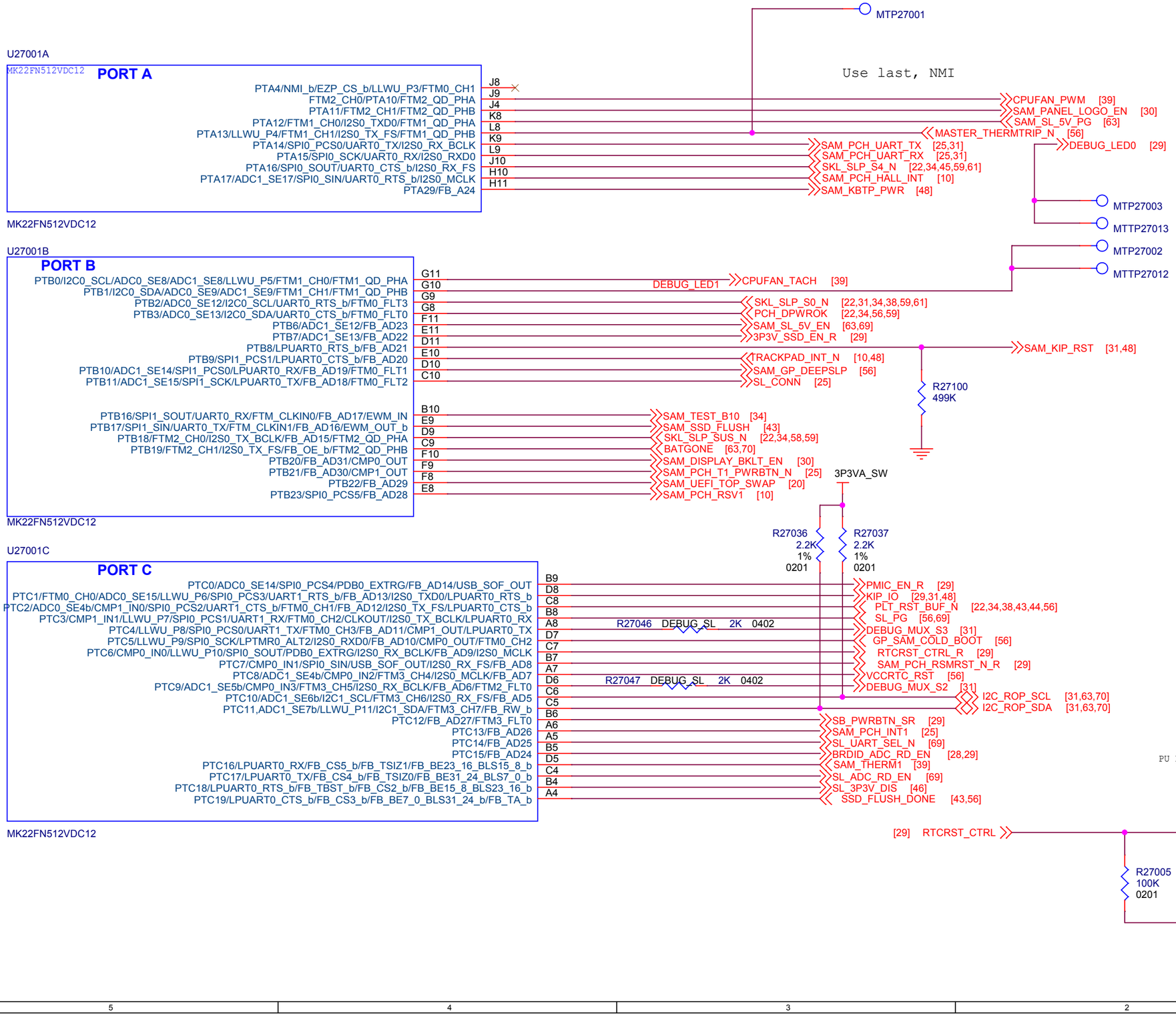
VCCPLL(VCCSFR)=0.12A

V0P85A 2.57A

2pF caps need to be place as close to SOC pins as possible

U SPECIFIC

Title:	26. PCH(7)_POWER
Microsoft Confidential	Surface
Engineer:	
Size: A3	Project Name: A
Rev: 1.0.0.1	
Date: Friday, April 27, 2018	Sheet 26 of 79


U27001A
MK22FN512VDC12
PORT A
PTA4/NMI_b/EZP_CS_b/LLWU_P3/FTM0_CH1
FTM2_CH0/PTA10/FTM2_QD_PHA
PTA11/FTM2_CH1/FTM2_QD_PHB
PTA12/FTM1_CH0/I2S0_TXD0/FTM1_QD_PHA
PTA13/LLWU_P4/FTM1_CH1/I2S0_TX_FS/FTM1_QD_PHB
PTA14/SPI0_PCS0/UART0_TX/I2S0_RX_BCLK
PTA15/SPI0_SCK/UART0_RX/I2S0_RXD0
PTA16/SPI0_SOUT/UART0_CTS_b/I2S0_RX_FS
PTA17/ADC1_SE17/SPI0_SIN/UART0_RTS_b/I2S0_MCLK
PTA29/FB_A24
J8
J9
J4
K8
L8
K9
L9
J10
H10
H11
MTP27001
Use last, NMI
CPUFAN_PWM [39]
SAM_PANEL_LOGO_EN [30]
SAM_SL_5V_PG [63]
MASTER_THERMTRIP_N [56]
SAM_PCH_UART_TX [25,31]
SAM_PCH_UART_RX [25,31]
SKL_SLP_S4_N [22,34,45,59,61]
SAM_PCH_HALL_INT [10]
SAM_KBTP_PWR [48]
DEBUG_LED0 [29]
MTP27003
MTTP27013
MK22FN512VDC12
U27001B
PORT B
PTB0/I2C0_SCL/ADC0_SE8/ADC1_SE8/LLWU_P5/FTM1_CH0/FTM1_QD_PHA
PTB1/I2C0_SDA/ADC0_SE9/ADC1_SE9/FTM1_CH1/FTM1_QD_PHB
PTB2/ADC0_SE12/I2C0_SCL/UART0_RTS_b/FTM0_FLT3
PTB3/ADC0_SE13/I2C0_SDA/UART0_CTS_b/FTM0_FLT0
PTB6/ADC1_SE12/FB_AD23
PTB7/ADC1_SE13/FB_AD22
PTB8/LPUART0_RTS_b/FB_AD21
PTB9/SPI1_PCS1/LPUART0_CTS_b/FB_AD20
PTB10/ADC1_SE14/SPI1_PCS0/LPUART0_RX/FB_AD19/FTM0_FLT1
PTB11/ADC1_SE15/SPI1_SCK/LPUART0_TX/FB_AD18/FTM0_FLT2
PTB16/SPI1_SOUT/UART0_RX/FTM_CLKIN0/FB_AD17/EWM_IN
PTB17/SPI1_SIN/UART0_TX/FTM_CLKIN1/FB_AD16/EWM_OUT_b
PTB18/FTM2_CH0/I2S0_TX_BCLK/FB_AD15/FTM2_QD_PHA
PTB19/FTM2_CH1/I2S0_TX_FS/FB_OE_b/FTM2_QD_PHB
PTB20/FB_AD31/CMP0_OUT
PTB21/FB_AD30/CMP1_OUT
PTB22/FB_AD29
PTB23/SPI0_PCS5/FB_AD28
G11
G10
G9
G8
F11
E11
D11
E10
D10
C10
B10
E9
D9
C9
F10
F9
F8
E8
DEBUG_LED1
CPUFAN_TACH [39]
MTP27002
MTTP27012
SKL_SLP_S0_N [22,31,34,38,59,61]
PCH_DPWROK [22,34,56,59]
SAM_SL_5V_EN [63,69]
3P3V_SSD_EN_R [29]
TRACKPAD_INT_N [10,48]
SAM_GP_DEEPSLP [56]
SL_CONN [25]
SAM_KIP_RST [31,48]
R27100
499K
SAM_TEST_B10 [34]
SAM_SSD_FLUSH [43]
SKL_SLP_SUS_N [22,34,58,59]
BATGONE [63,70]
SAM_DISPLAY_BKLT_EN [30]
SAM_PCH_T1_PWRBTN_N [25]
SAM_UEFI_TOP_SWAP [20]
SAM_PCH_RSV1 [10]
3P3VA_SW
R27036
2.2K
1%
0201
R27037
2.2K
1%
0201
MK22FN512VDC12
U27001C
PORT C
PTC0/ADC0_SE14/SPI0_PCS4/PDB0_EXTRG/FB_AD14/USB_SOF_OUT
PTC1/FTM0_CH0/ADC0_SE15/LLWU_P6/SPI0_PCS3/UART1_RTS_b/FB_AD13/I2S0_TXD0/LPUART0_RTS_b
PTC2/ADC0_SE4b/CMP1_IN0/SPI0_PCS2/UART1_CTS_b/FTM0_CH1/FB_AD12/I2S0_TX_FS/LPUART0_CTS_b
PTC3/CMP1_IN1/LLWU_P7/SPI0_PCS1/UART1_RX/FTM0_CH2/CLKOUT/I2S0_TX_BCLK/LPUART0_RX
PTC4/LLWU_P8/SPI0_PCS0/UART1_TX/FTM0_CH3/FB_AD11/CMP1_OUT/LPUART0_TX
PTC5/LLWU_P9/SPI0_SCK/LPTMR0_ALT2/I2S0_RXD0/FB_AD10/CMP0_OUT/FTM0_CH2
PTC6/CMP0_IN0/LLWU_P10/SPI0_SOUT/PDB0_EXTRG/I2S0_RX_BCLK/FB_AD9/I2S0_MCLK
PTC7/CMP0_IN1/SPI0_SIN/USB_SOF_OUT/I2S0_RX_FS/FB_AD8
PTC8/ADC1_SE4b/CMP0_IN2/FTM3_CH4/I2S0_MCLK/FB_AD7
PTC9/ADC1_SE5b/CMP0_IN3/FTM3_CH5/I2S0_RX_BCLK/FB_AD6/FTM2_FLT0
PTC10/ADC1_SE6b/I2C1_SCL/FTM3_CH6/I2S0_RX_FS/FB_AD5
PTC11,ADC1_SE7b/LLWU_P11/I2C1_SDA/FTM3_CH7/FB_RW_b
PTC12/FB_AD27/FTM3_FLT0
PTC13/FB_AD26
PTC14/FB_AD25
PTC15/FB_AD24
PTC16/LPUART0_RX/FB_CS5_b/FB_TSIZ1/FB_BE23_16_BLS15_8_b
PTC17/LPUART0_TX/FB_CS4_b/FB_TSIZ0/FB_BE31_24_BLS7_0_b
PTC18/LPUART0_RTS_b/FB_TBST_b/FB_CS2_b/FB_BE15_8_BLS23_16_b
PTC19/LPUART0_CTS_b/FB_CS3_b/FB_BE7_0_BLS31_24_b/FB_TA_b
B9
D8
C8
B8
A8
D7
C7
B7
A7
D6
C6
C5
B6
A6
A5
B5
D5
C4
B4
A4
R27046 DEBUG_SL 2K 0402
R27047 DEBUG_SL 2K 0402
PMIC_EN_R [29]
KIP_IO [29,31,48]
PLT_RST_BUF_N [22,34,38,43,44,56]
SL_PG [56,69]
DEBUG_MUX_S3 [31]
GP_SAM_COLD_BOOT [56]
RTCRST_CTRL_R [29]
SAM_PCH_RSMRST_N_R [29]
VCCRTC_RST [56]
DEBUG_MUX_S2 [31]
I2C_ROP_SCL [31,63,70]
I2C_ROP_SDA [31,63,70]
SB_PWRBTN_SR [29]
SAM_PCH_INT1 [25]
SL_UART_SEL_N [69]
BRDID_ADC_RD_EN [28,29]
SAM_THERM1 [39]
SL_ADC_RD_EN [69]
SL_3P3V_DIS [46]
SSD_FLUSH_DONE [43,56]
MK22FN512VDC12
PU Resistors are on PCH side
SKL_RTCRST_N [20]
Q27001
RUM002N02GT2L
G
D
S
[29] RTCRST_CTRL
R27005
100K
0201
Title: 27. SAM_1, K22
Microsoft Confidential
Engineer:
Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
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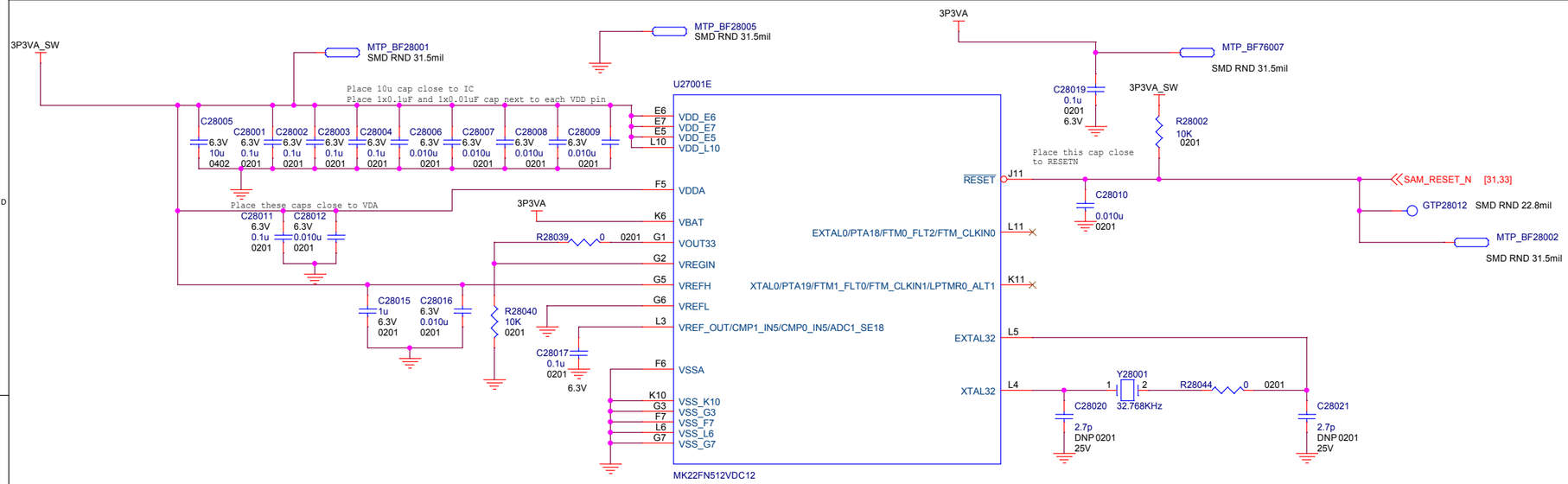

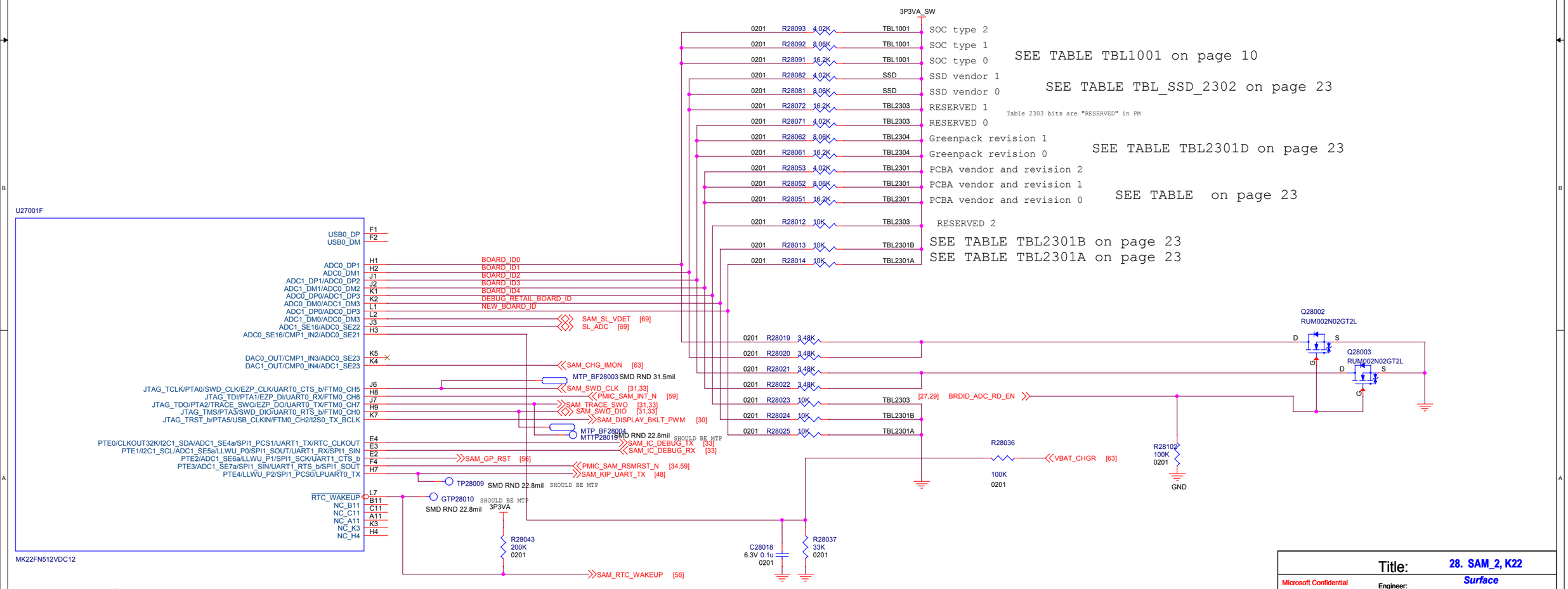

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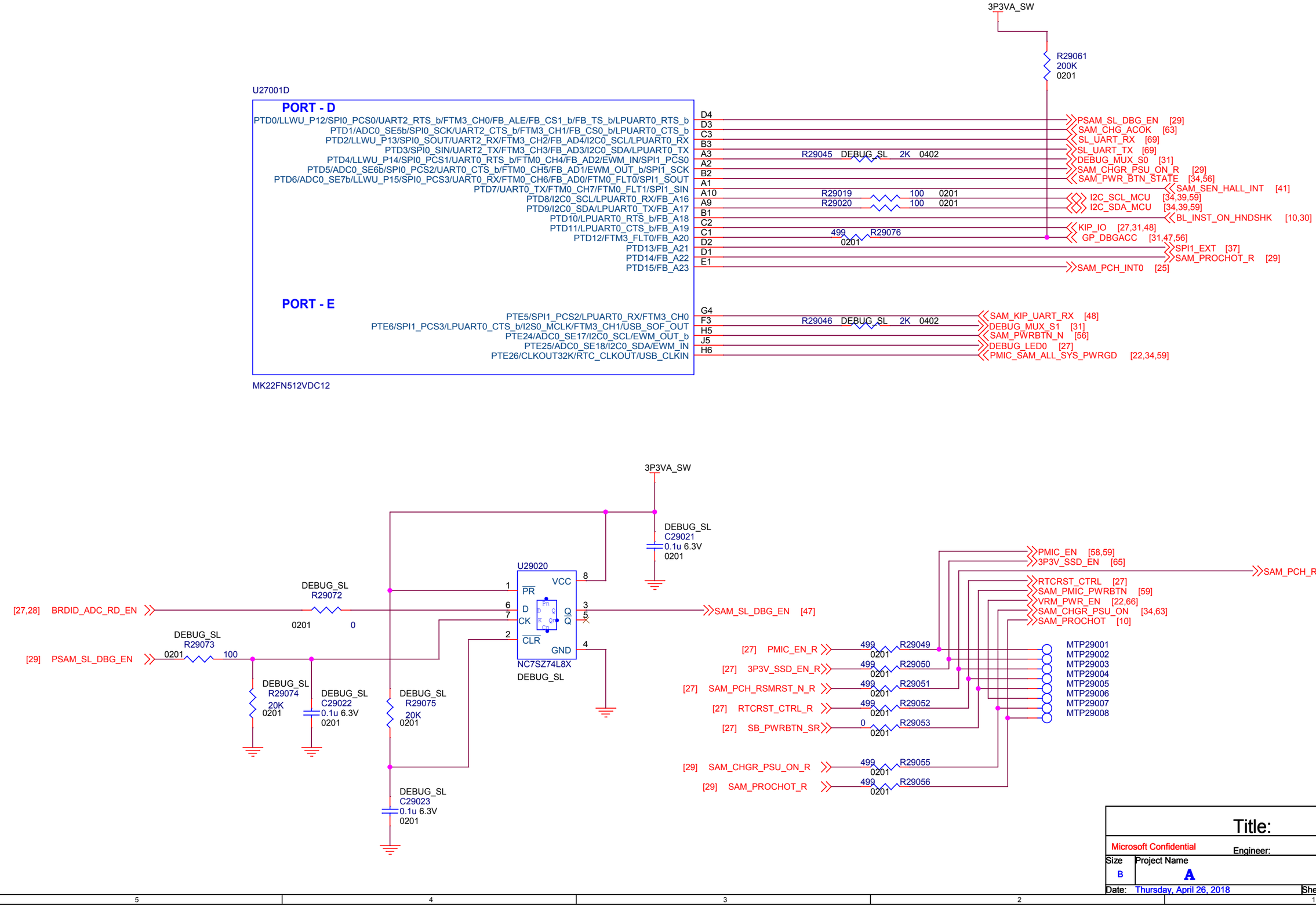
Title:	28. SAM_2, K22		
Microsoft Confidential	Engineer:	Surface	
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 28 of 79		


3P3VA_SW
R29061
200K
0201
U27001D
PORT - D
PTD0/LLWU_P12/SPI0_PCS0/UART2_RTS_b/FTM3_CH0/FB_ALE/FB_CS1_b/FB_TS_b/LPUART0_RTS_b
PTD1/ADC0_SE5b/SPI0_SCK/UART2_CTS_b/FTM3_CH1/FB_CS0_b/LPUART0_CTS_b
PTD2/LLWU_P13/SPI0_SOUT/UART2_RX/FTM3_CH2/FB_AD4/I2C0_SCL/LPUART0_RX
PTD3/SPI0_SIN/UART2_TX/FTM3_CH3/FB_AD3/I2C0_SDA/LPUART0_TX
PTD4/LLWU_P14/SPI0_PCS1/UART0_RTS_b/FTM0_CH4/FB_AD2/EWM_IN/SPI1_PCS0
PTD5/ADC0_SE6b/SPI0_PCS2/UART0_CTS_b/FTM0_CH5/FB_AD1/EWM_OUT_b/SPI1_SCK
PTD6/ADC0_SE7b/LLWU_P15/SPI0_PCS3/UART0_RX/FTM0_CH6/FB_AD0/FTM0_FLT0/SPI1_SOUT
PTD7/UART0_TX/FTM0_CH7/FTM0_FLT1/SPI1_SIN
PTD8/I2C0_SCL/LPUART0_RX/FB_A16
PTD9/I2C0_SDA/LPUART0_TX/FB_A17
PTD10/LPUART0_RTS_b/FB_A18
PTD11/LPUART0_CTS_b/FB_A19
PTD12/FTM3_FLT0/FB_A20
PTD13/FB_A21
PTD14/FB_A22
PTD15/FB_A23
D4
D3
C3
B3
A3
A2
B2
A1
A10
A9
B1
C2
C1
D2
D1
E1
R29045 DEBUG_SL 2K 0402
R29019 100 0201
R29020 100 0201
499 R29076 0201
PSAM_SL_DBG_EN [29]
SAM_CHG_ACOK [63]
SL_UART_RX [69]
SL_UART_TX [69]
DEBUG_MUX_S0 [31]
SAM_CHGR_PSU_ON_R [29]
SAM_PWR_BTN_STATE [34,56]
SAM_SEN_HALL_INT [41]
I2C_SCL_MCU [34,39,59]
I2C_SDA_MCU [34,39,59]
BL_INST_ON_HNDSHK [10,30]
KIP_IO [27,31,48]
GP_DBGACC [31,47,56]
SPI1_EXT [37]
SAM_PROCHOT_R [29]
SAM_PCH_INT0 [25]
PORT - E
PTE5/SPI1_PCS2/LPUART0_RX/FTM3_CH0
PTE6/SPI1_PCS3/LPUART0_CTS_b/I2S0_MCLK/FTM3_CH1/USB_SOF_OUT
PTE24/ADC0_SE17/I2C0_SCL/EWM_OUT_b
PTE25/ADC0_SE18/I2C0_SDA/EWM_IN
PTE26/CLKOUT32K/RTC_CLKOUT/USB_CLKIN
G4
F3
H5
J5
H6
R29046 DEBUG_SL 2K 0402
SAM_KIP_UART_RX [48]
DEBUG_MUX_S1 [31]
SAM_PWRBTN_N [56]
DEBUG_LED0 [27]
PMIC_SAM_ALL_SYS_PWRGD [22,34,59]
MK22FN512VDC12
3P3VA_SW
DEBUG_SL
C29021
0.1u 6.3V
0201
U29020
VCC
PR
D
CK
CLR
GND
Q
Q
NC7SZ74L8X
DEBUG_SL
1
2
3
4
5
6
7
8
DEBUG_SL
R29072
0201
0
[27,28] BRDID_ADC_RD_EN
DEBUG_SL
R29073
0201
100
[29] PSAM_SL_DBG_EN
DEBUG_SL
R29074
20K
0201
DEBUG_SL
C29022
0.1u 6.3V
0201
DEBUG_SL
R29075
20K
0201
DEBUG_SL
C29023
0.1u 6.3V
0201
SAM_SL_DBG_EN [47]
PMIC_EN [58,59]
3P3V_SSD_EN [65]
SAM_PCH_RSMRST_N [18,22,56]
RTCRST_CTRL [27]
SAM_PMIC_PWRBTN [59]
VRM_PWR_EN [22,66]
SAM_CHGR_PSU_ON [34,63]
SAM_PROCHOT [10]
[27] PMIC_EN_R
[27] 3P3V_SSD_EN_R
[27] SAM_PCH_RSMRST_N_R
[27] RTCRST_CTRL_R
[27] SB_PWRBTN_SR
[29] SAM_CHGR_PSU_ON_R
[29] SAM_PROCHOT_R
499 R29049 0201
499 R29050 0201
499 R29051 0201
499 R29052 0201
0 R29053 0201
499 R29055 0201
499 R29056 0201
MTP29001
MTP29002
MTP29003
MTP29004
MTP29005
MTP29006
MTP29007
MTP29008
Title: 29. SAM_3, K22
Microsoft Confidential
Engineer:
Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
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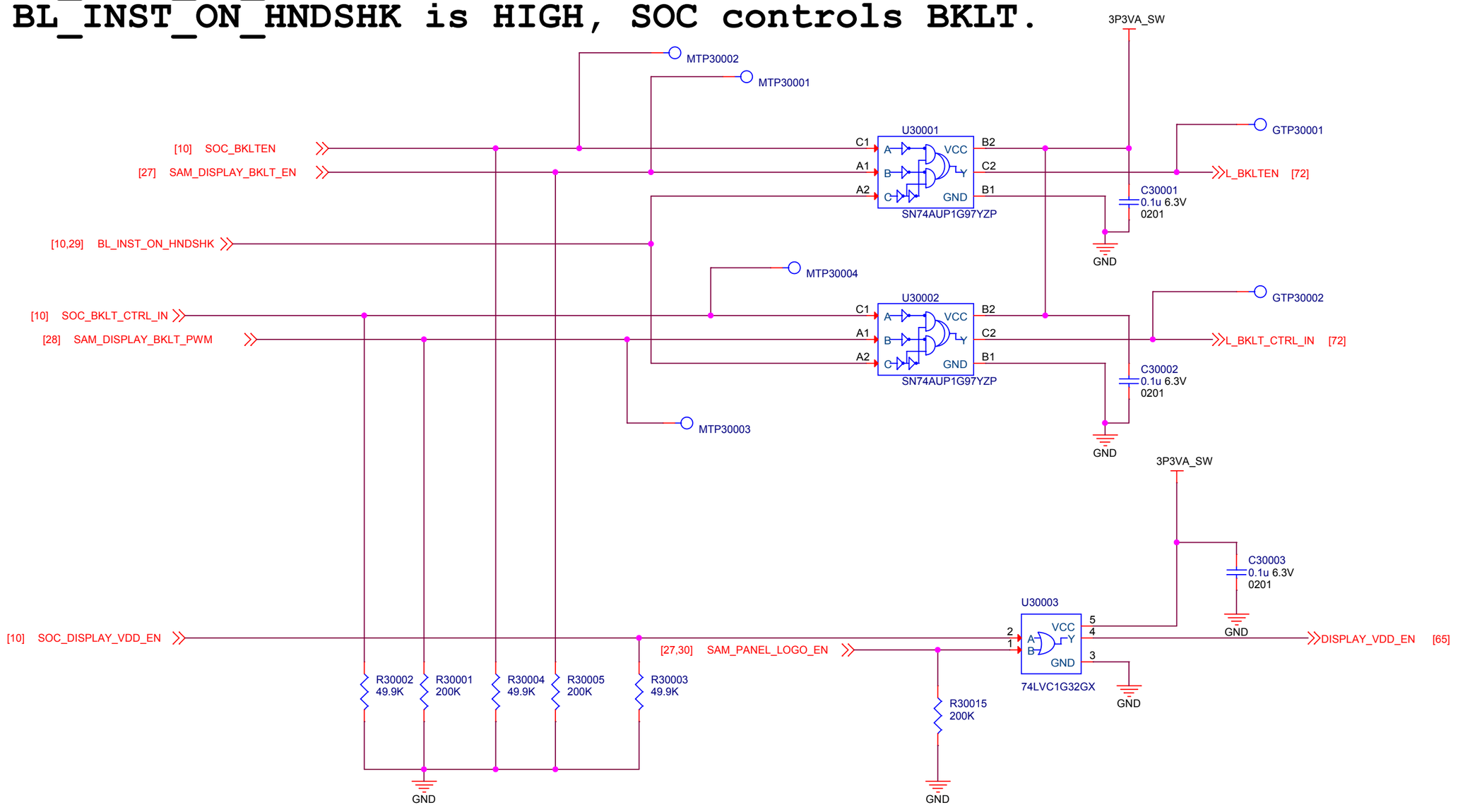
When BL_INST_ON_HNDSHK is LOW, SAM controls BKLT.
When BL_INST_ON_HNDSHK is HIGH, SOC controls BKLT.

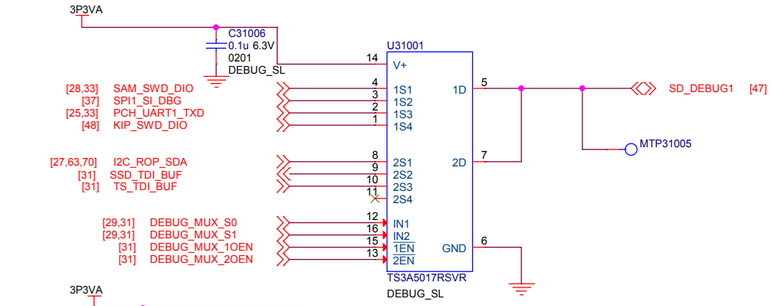


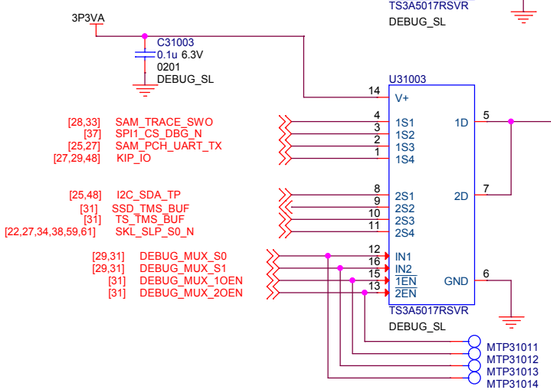
PANEL_LOGO [55]

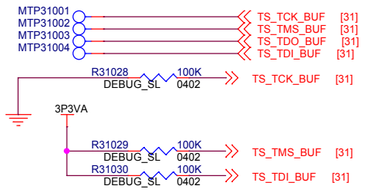
35kohms-287kohms pulldown at TDM
PANEL_LOGO Input is 3.3V tolerant

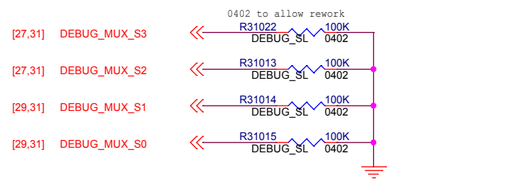
[27,30] SAM_PANEL_LOGO_EN — R30014 — 100 0201

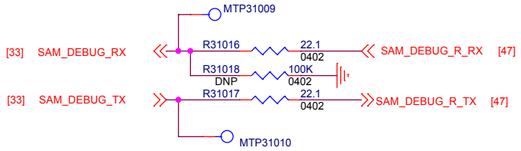
Title:	30. INSTANT_ON	
Microsoft Confidential	Engineer:	Surface
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 30 of 79	

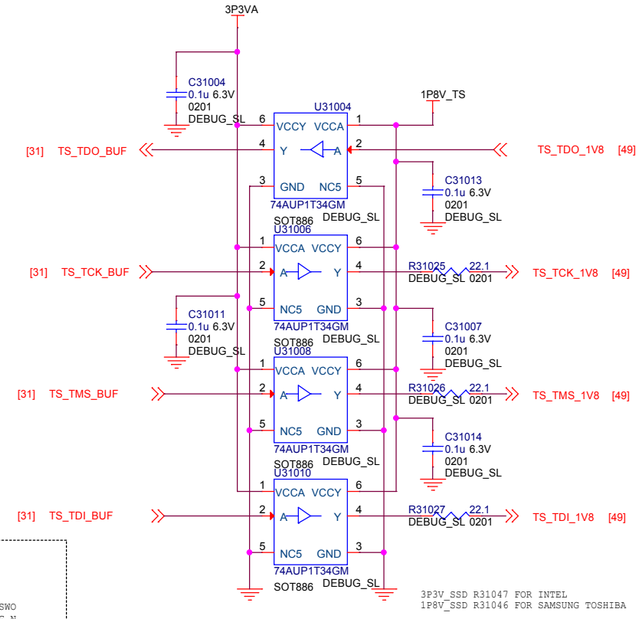


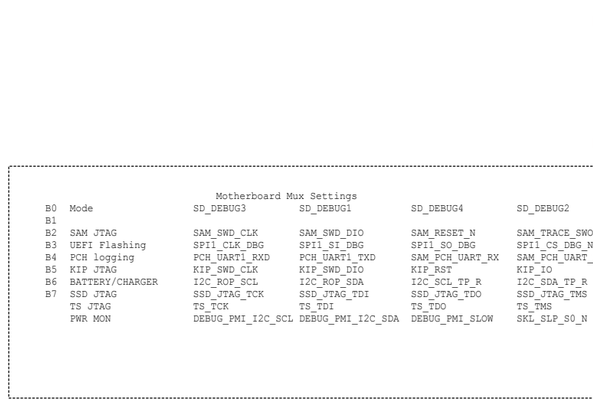


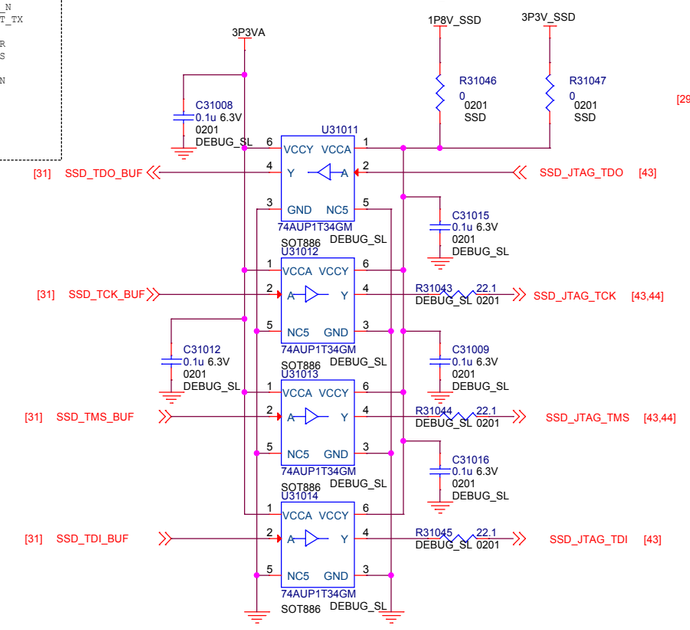


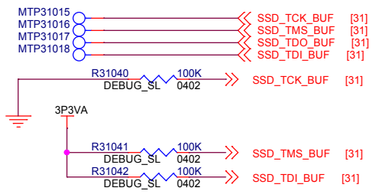


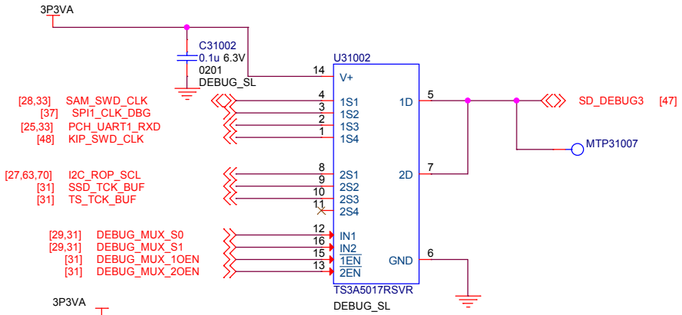


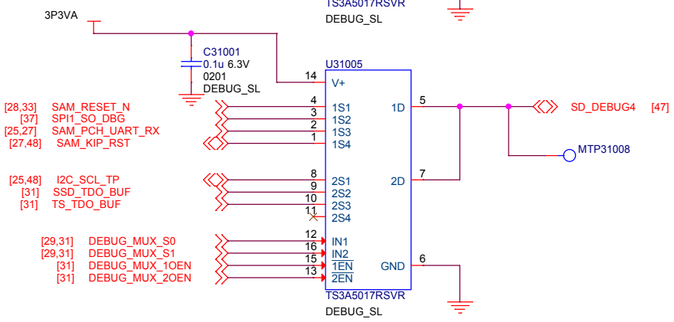


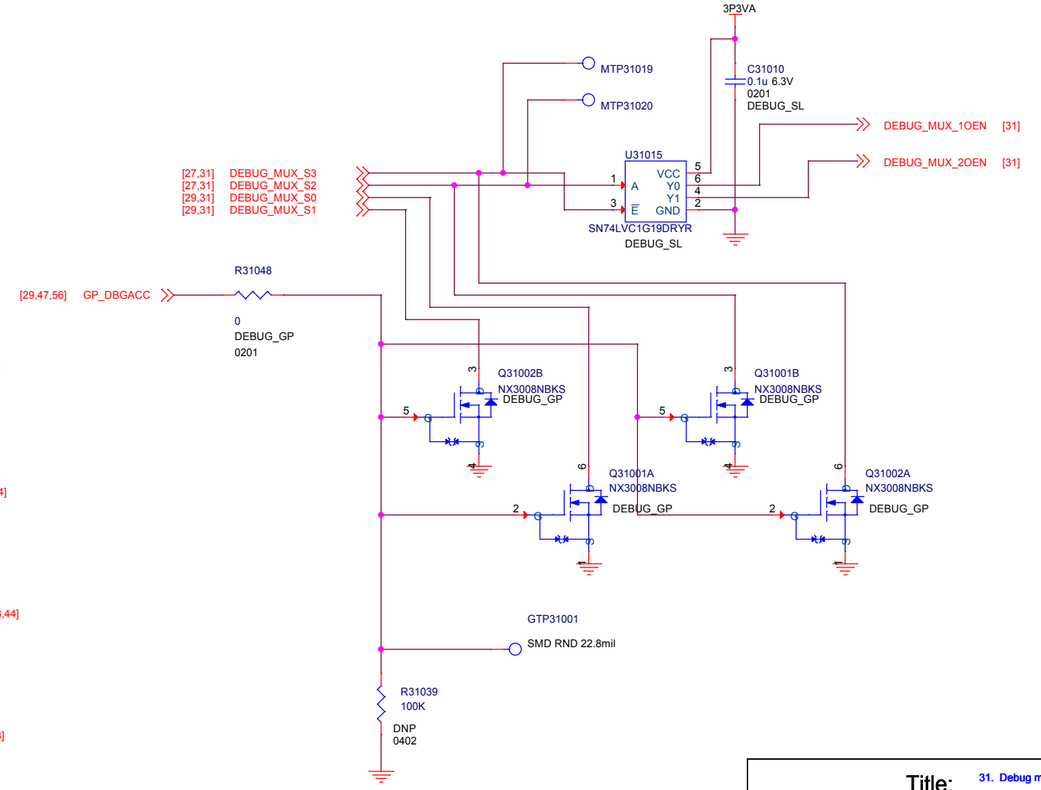








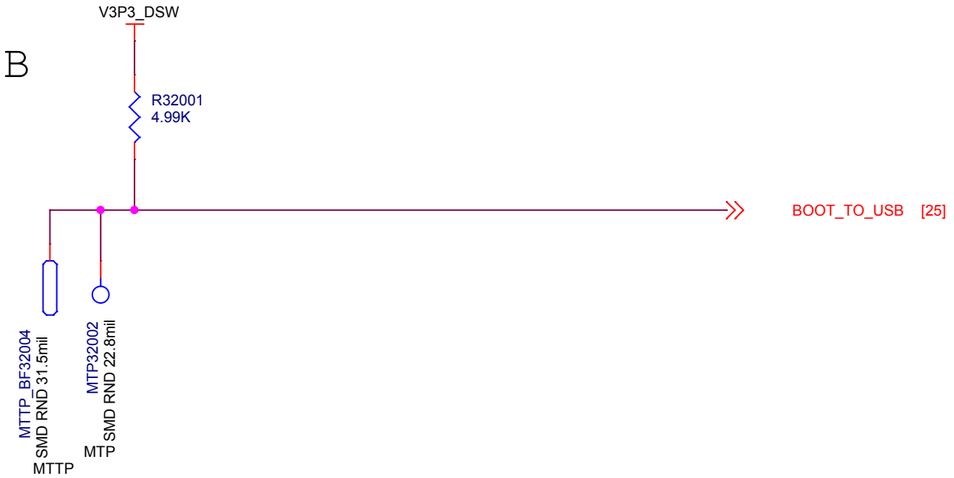


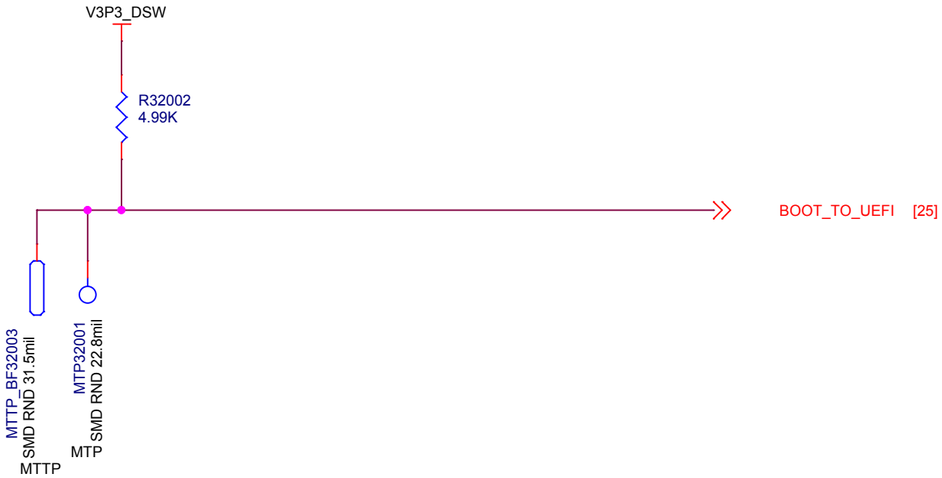


Vinafix.com

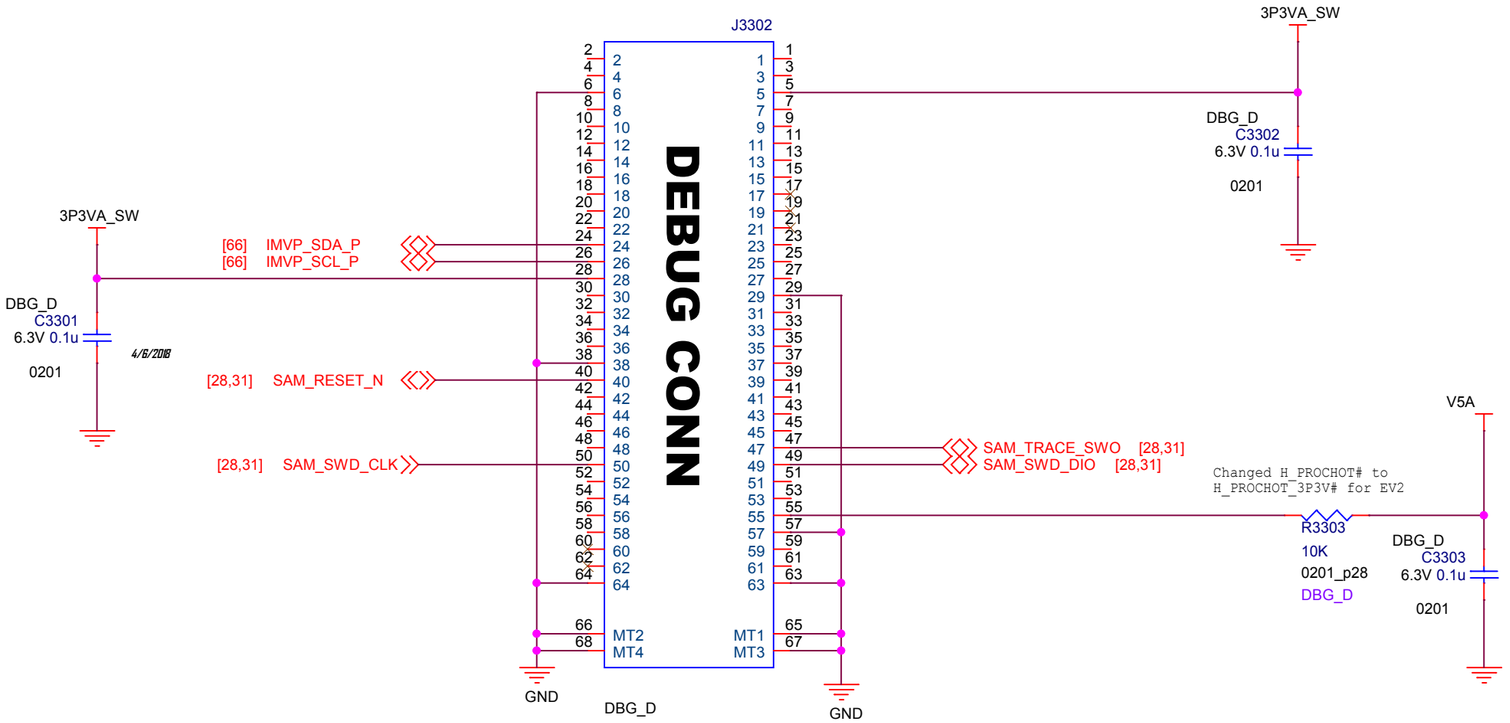
Title:	31. Debug mux		
Microsoft Confidential	Engineer:	Surface	
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 31 of 79		

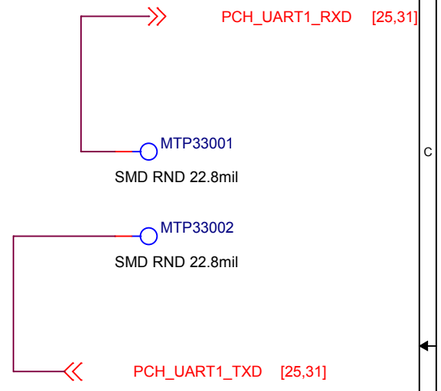
BOOT_TO_USB

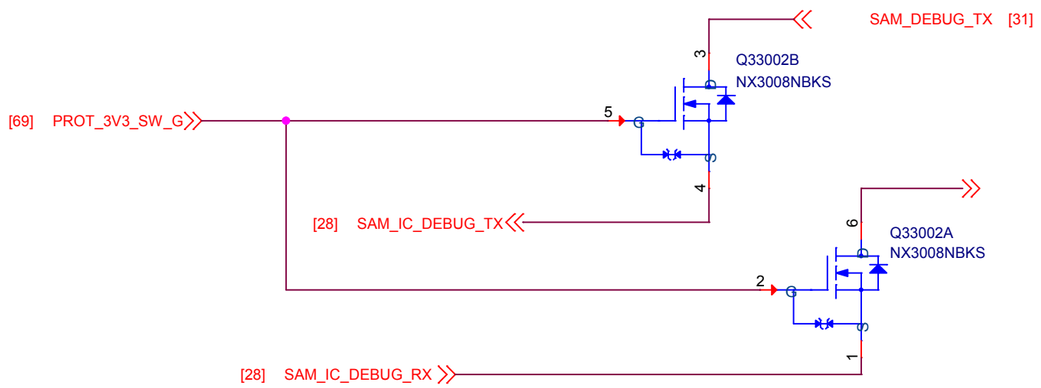




Title:	32. Debug Buttons	
Microsoft Confidential	Engineer:	Surface
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 32 of 79	







DVi7U7660s16s512x2Retail

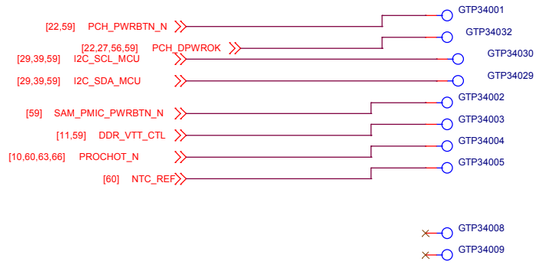
Title: 33. SW Debug Conn

Microsoft Confidential

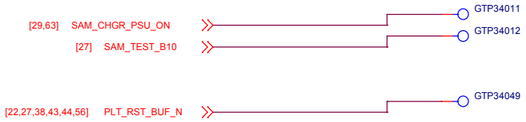
Engineer: Surface

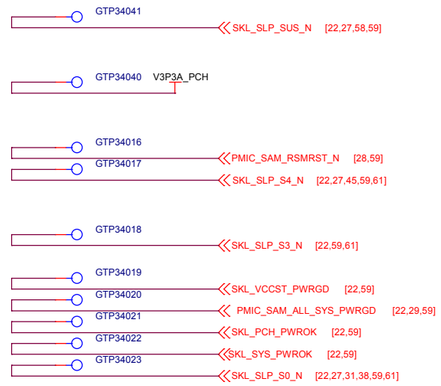
Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 33 of 79



I2C testpoints are shown on page 25





DVI7U7660s16s512x2Retail

Title: 34. EE Debug Connector		
Size: A2	Document Number: A	Rev: <RevCode>
Date: Thursday, April 26, 2018	Sheet 34 of 76	

Title:	35. EMPTY	
Microsoft Confidential	Engineer:	*Surface*
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 35 of 79	

MTP36003
SMD RND 22.8mil

SMD RND 22.8mil
MTP36001

MTP36002
SMD RND 22.8mil

No Power Monitors in this SKU

```
Resistor Address for MAX3440
20.5K    =>  0x3C/0x3D
11.0K    =>  0x38/0x39
5.90K    =>  0x34/0x35
3.16K    =>  0x30/0x31
1.74K    =>  0x2C/0x2D
931K     =>  2x28/2x29
499      =>  2x24/2x25
GND      =>  2x20/2x21
```

Title: 36. Power Monitor

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
Custom	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 36 of 79

UEFI SPI ROM

3VSUS_ORG

1K
0201
R37001

(128Mb=16MB @104MHz)

Needs to >= 66MHz

U37001
W25Q128JVPIQ

SPI1_CS0_N	1	CS#	
SPI1_SO	2	DO(IO1)	VCC 8
SPI1_WP_N	3	WP#(IO2)	HOLD#(IO3) 7 SPI1_HOLD_N
	4	GND1	CLK 6 SPI1_CLK
	9	GND2	DI(IO0) 5 SPI1_SI

3VSUS_ORG

C37001
0.1u 6.3V
0201

3VSUS_ORG

C37002
0.1u 6.3V
0201
DEBUG_SL

DEBUG_SL
U37002
TS3A27518EZQSR

SPI1_CLK	A1	COM1	V+ C2
SPI1_SI	B1	COM2	
SPI1_SO	C1	COM3	EN# C4
SPI1_WP_N	D1	COM4	
SPI1_HOLD_N	E1	COM5	IN1 B4
SPI1_CS0_N	D2	COM6	IN2 D3
			GND C3
	A3	N.C.	
	B3	NC1	NO1 E2
	A2	NC2	NO2 E3
	A4	NC3	NO3 E4
	B5	NC4	NO4 D5 SPI1_WP_DBG_N
	C5	NC5	NO5 D4 SPI1_HOLD_DBG_N
	A5	NC6	NO6 E5

BGA24

DEBUG_SL
R37005 100K 0201

MTTP37001
SMD RND 22.8mil

3VSUS_ORG

1K 0201 DEBUG_SL R37003
1K 0201 DEBUG_SL R37004

SPI1_EXT [29]

SPI_CLK = 20/33/50Mhz

[21] SPI_CLK
[21] SPI_SI
[21] SPI_SO
[21] SPI_WP_IO2
[21] SPI_HOLD_IO3_N
[21] SPI_CS0_N

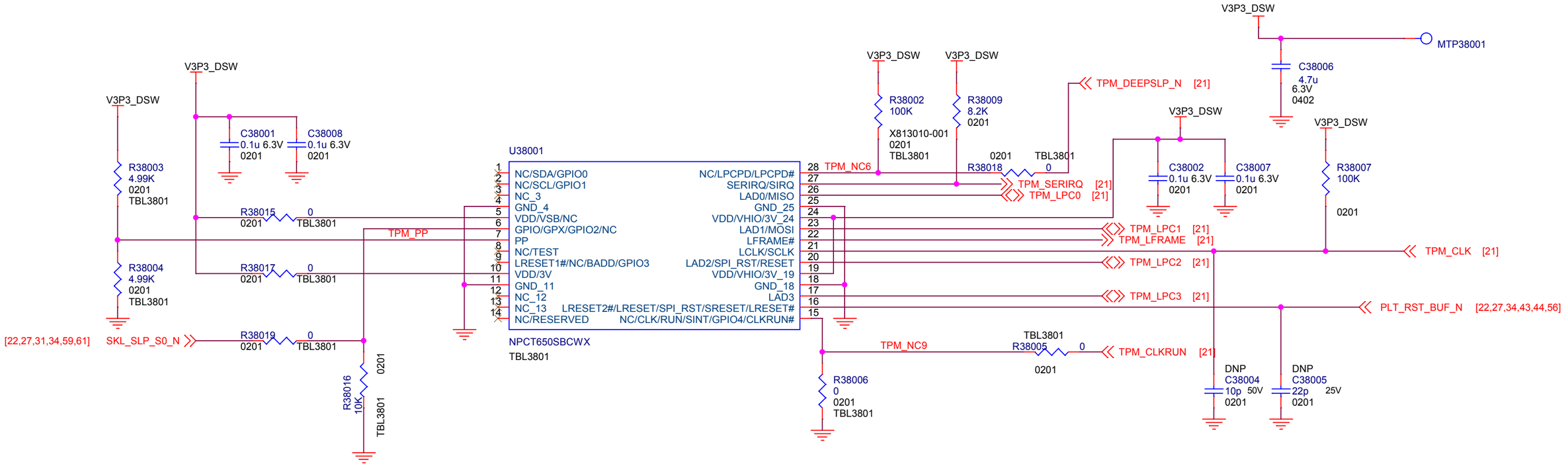
SPI1_CLK_DBG [31]
SPI1_SI_DBG [31]
SPI1_SO_DBG [31]
SPI1_CS_DBG_N [31]

SPI1_CLK	R37006	0	NDEBUG_SL	0201	SPI_CLK MTTP37002 SMD RND 22.8mil
SPI1_SI	R37007	0	NDEBUG_SL	0201	SPI_SI MTTP37003 SMD RND 22.8mil
SPI1_SO	R37008	0	NDEBUG_SL	0201	SPI_SO MTTP37004 SMD RND 22.8mil
SPI1_WP_N	R37009	0	NDEBUG_SL	0201	SPI_WP_IO2 MTTP37005 SMD RND 22.8mil
SPI1_HOLD_N	R37010	0	NDEBUG_SL	0201	SPI_HOLD_IO3_N MTTP37006 SMD RND 22.8mil
SPI1_CS0_N	R37011	0	NDEBUG_SL	0201	SPI_CS0_N MTTP37007 SMD RND 22.8mil

```
IN1/IN2 = L  => COM to NC
IN1/IN2 = H  => NC  to COM
```

Title:	37. SPI ROM UEFI		
Microsoft Confidential	Engineer:	*Surface*	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Tuesday, May 01, 2018	Sheet 37 of 79		

Trusted Platform Module



TBL3801		
Lancelot RefDes	***Nuvuton***	***NationZ***
U38001	M1006791-002	X930840-002
R38002	NO STUFF	X813010-001
R38003	NO STUFF	NO STUFF
R38004	X813007-001	NO STUFF
R38005	X811786-001	NO STUFF
R38006	NO STUFF	X811786-001
R38015	X811786-001	NO STUFF
R38016	NO STUFF	NO STUFF
R38017	X811786-001	X811786-001
R38018	X811786-001	NO STUFF
R38019	X811786-001	NO STUFF

Title: 38. TPM

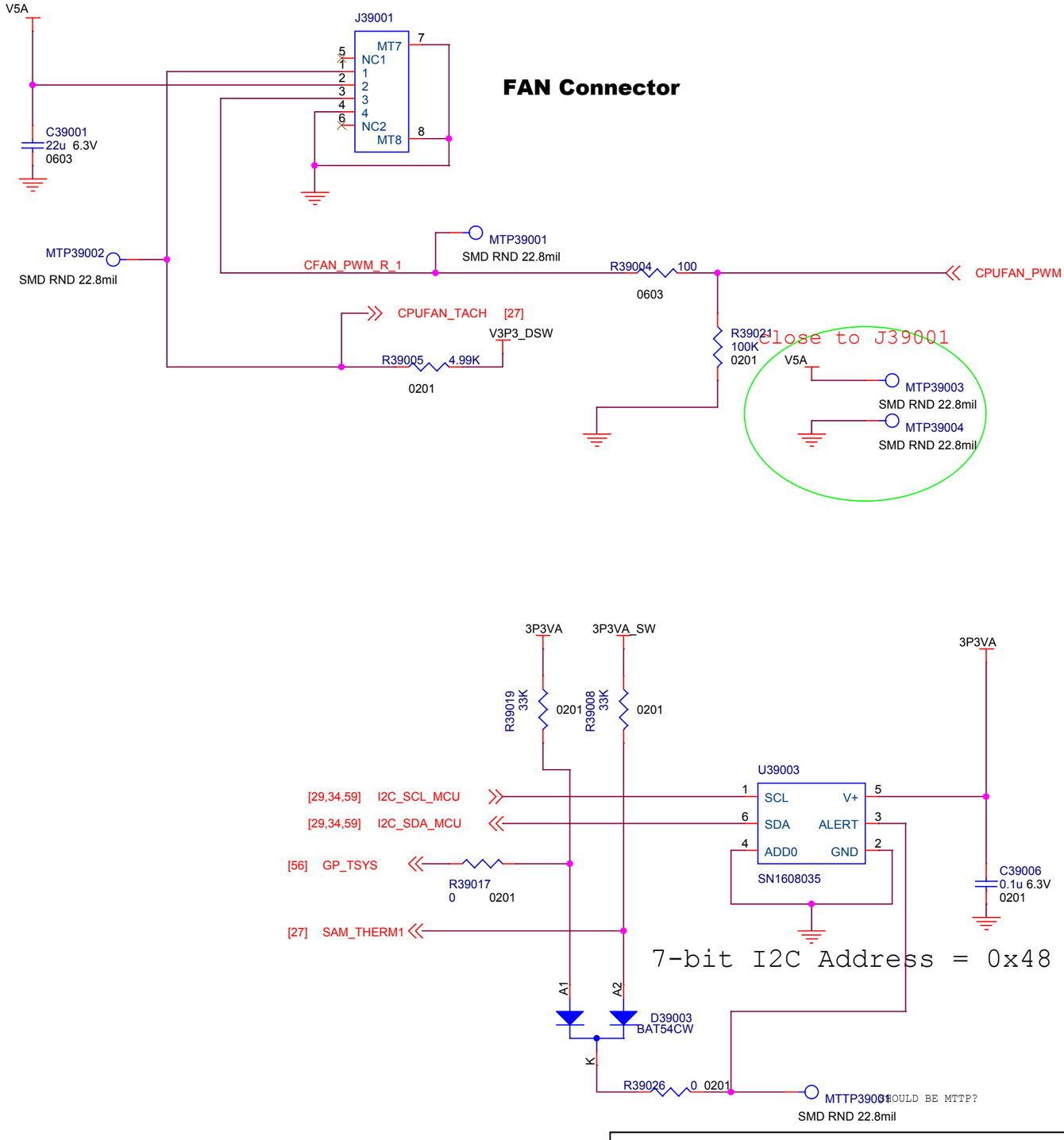
Microsoft Confidential

Engineer: *Surface*

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 38 of 79

FAN Connector



U SPECIFIC

Title:	39. Temp Sensor/System Fan		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Tuesday, May 01, 2018	Sheet 39 of 79		

SPKR Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

C40009 and C40010 can be deleted and L40001 converted to a 0 ohm jumper if smart amp remains.

Place close to J41001

Place under U40001

close to audio

ALC3269C-GRT

Title:	40. REALTEK ALC3269 CODEC		
Microsoft Confidential	Engineer: Surface		
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 40 of 79		

Audio Jack/MIC1 Combo Jack

V3P3_DSW

SMD RND 22.8mil
MTP41011

R41015
499K
0201

SAM_SEN_HALL_INT [29]

C41016
6.3V
0.1u

J41005
PINS MIRRORED
502426-0810

R41001
[40] MIC1_VREFO_L
2.2K 0201

L41001 place close to J41004

C41001
4.7uF
6.3V
0402
[40] MIC1_R

C41015
4.7uF
6.3V
0402
[40] MIC1_L

R41002
1K
0201

L41001
120 OHM,100MHZ
0603
BLM18SG121TN1D

R41003
22K
0201
AGND

C41002
25V 100p
0201
AGND

PCB trace width of MIC1-R/Mic1-L (Sleeve/Ring2) are required at least 40 mil for HP crosstalk consideration and its length should be as short as possible

MIC1_R_CR_F_C

[40] COMBO_JACK

R41004 22K
0201

C41004
10u 6.3V
0402
AGND

SMD RND 22.8mil
MTP41001

HPOUT_JD [40]

D41001
V5.5MLA0402NR
CDS2C05GTA
A2
A1

GND

[40] HPOUT_L
[40] HPOUT_R

R41005 51.1 0603
R41006 51.1 0603

HPOUT_L_F
HPOUT_R_F

L41002 BLM18SG121TN1D 0603
L41003 BLM18SG121TN1D 0603
120 OHM,100MHZ

R41007 10K 0201
R41008 10K 0201
AGND

C41005 100p 25V 0201
C41006 100p 25V 0201
GND

D41002 V5.5MLA0402NR
D41003 V5.5MLA0402NR

HPOUT_L_F_C
HPOUT_R_F_C

MTP41004 SMD RND 22.8mil
MTP41005 SMD RND 22.8mil
MTP41002 SMD RND 22.8mil

DNP
J41004
MIC1_R_CR_F_C
1 MIC
3 RIGHT
4 DET
5 LEFT
2 GND
AGND

D41004
V5.5MLA0402NR

MTP41003 SMD RND 22.8mil
AGND

SPKR

[42] AMP_SPK_RP
[42] AMP_SPK_RN

C41007 1000p 25V 0201
C41008 25V 1000p 0201
GND

SMD RND 22.8mil
MTP41006
MTP41007
SMD RND 22.8mil

J41002
78171-0002
X872411-001
MTG1
MTG2

D41005 V14MLA0603NH
D41006 V14MLA0603NH

[42] AMP_SPK_LP
[42] AMP_SPK_LN

C41009 1000p 25V 0201
C41010 25V 1000p 0201
GND

SMD RND 22.8mil
MTP41008
MTP41009
SMD RND 22.8mil

J41003
78171-0002
X872411-001

D41007 V14MLA0603NH
D41008 V14MLA0603NH

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Title: 41. Audio Jack/Spkr

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
C	A	1.0.0.1

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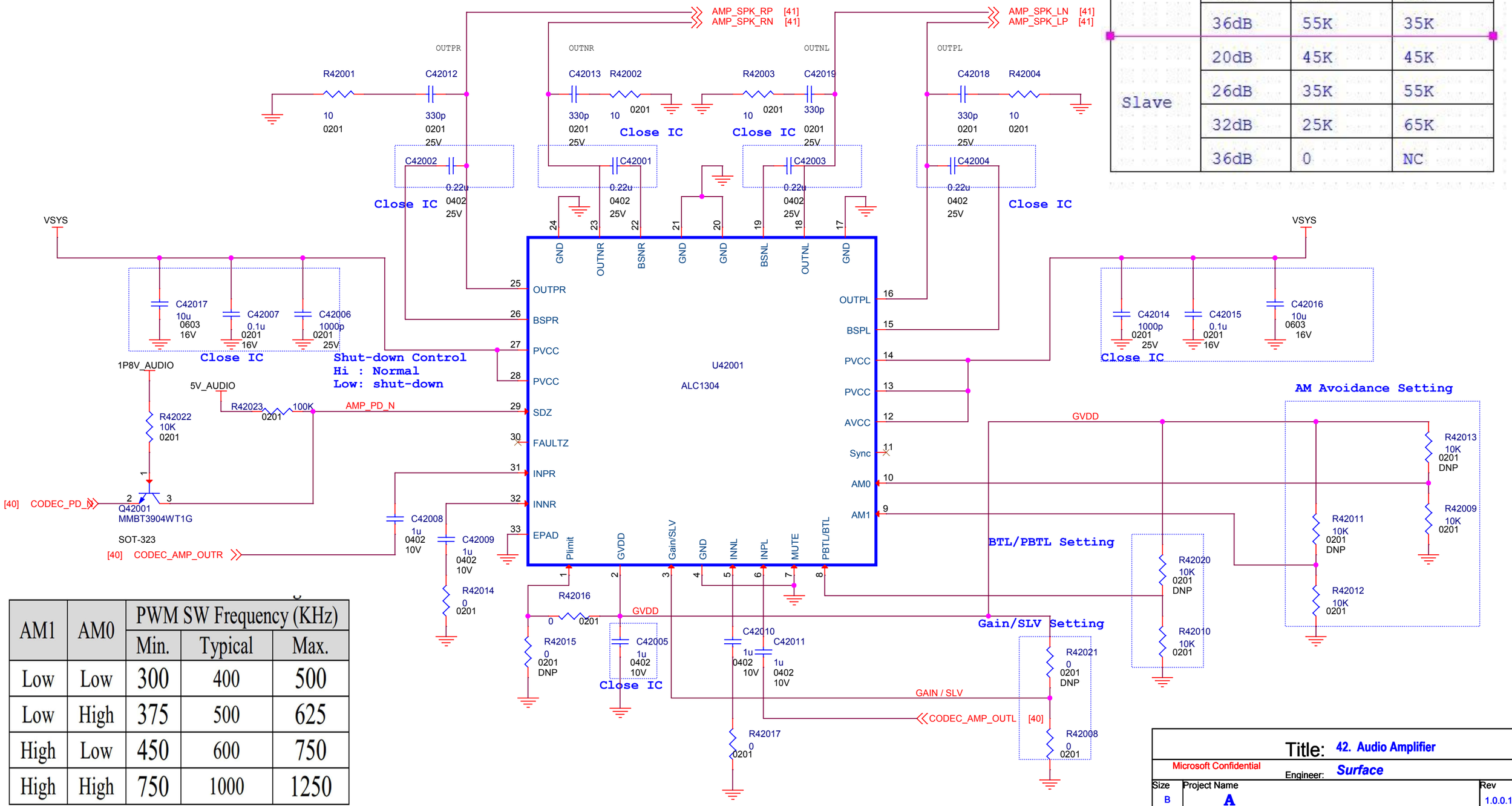
Stereo Input(S.E.)
Stereo Output-BTL

SPKR Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

Mode	Gain	RX(ohm)	RY(ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	36dB	0	NC



AM1	AM0	PWM SW Frequency (KHz)		
		Min.	Typical	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250

Microsoft Confidential

Title: 42. Audio Amplifier

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 42 of 79

For common BGA SSDs

U43001A

[20] PCIECLK_SSD_DP — R43011 0 0402 — D4 REFCLK_P
[20] PCIECLK_SSD_DN — R43012 0 0402 — D5 REFCLK_N

[24] PCIE_SSD_TX7_DP — F4 SATAmAp/PERp0
[24] PCIE_SSD_TX7_DN — F5 SATAmAm/PERn0

[24] PCIE_SSD_RX7_DP — SSD 0.22u 0201 6.3V SSD — H4 SATAmBp/PETp0
[24] PCIE_SSD_RX7_DN — 0.22u 0201 6.3V C43001 — H5 SATAmBm/PETn0
C43002

[24] PCIE_SSD_TX8_DP — K4 PER_P1
[24] PCIE_SSD_TX8_DN — K5 PER_N1

[24] PCIE_SSD_RX8_DP — SSD 0.22u 0201 6.3V SSD — M4 PET_P1
[24] PCIE_SSD_RX8_DN — 0.22u 0201 6.3V C43004 — M5 PET_N1
C43005

P4 PERp2/NC_P4
P5 PERn2/NC_P5
T4 PETp2/NC_T4
T5 PETn2/NC_T5
V4 PERp3/NC_V4
V5 PERn3/NC_V5
Y4 PETp3/NC_Y4
Y5 PETn3/NC_Y5

1P8V_SSD
0201 C43003 0.1u 6.3V SSD — GND
SSD_PERST_N [44]
SMD RND 22.8mil MTP43024
[22,27,34,38,44,56] PLT_RST_BUF_N
[25,44] PCIE_SSD_PERST_N
U43002 SSD SN74AUP1G08DRYR
D7 PERST#
F14 PEDET
R43303 100K 1% SSD 0201 GND
D8 CLKREQ#
D14 SUSCLK/NC_D14
E8 DEVSLP/NC_E8
[20] SSD_PCIECLK_REQ_N
E12 PEWAKE#/NC_E12
GTP43003 SMD RND 22.8mil
W7 LED1#/ DAS

R43098 1M DNP 0402
XRCGB25M000F2P00R0
DNP 0201 C43099 10p 25V
Y43001
C43098 10p 25V 0201 DNP
SSD_XTAL_OUT
SSD_XTAL_IN
B6 CAL_P/NC_B6
C7 XTAL_ OUT/NC_C7
C8 XTAL_IN/NC_C8
C10 RZQ_1/NC_C10

[43] SSD_DIAG1 — SSD_DIAG1 — D13 DIAG1/I2C_DATA
[43,44] SSD_DIAG0 — SSD_DIAG0 — E13 DIAG0/I2C_CLK
L18 JTAG_TRST#/NC_L18
[31,43,44] SSD_JTAG_TCK — N17 JTAG_TCK
[31,43,44] SSD_JTAG_TMS — N18 JTAG_TMS
[31,43] SSD_JTAG_TDI — R17 JTAG_TDI
[43,44] SSD1_JTAG_TDO — R18 JTAG_TDO
U17 SMB_ CLK/NC_U17
U18 SMB_DATA/NC_U18
W18 ALERT#/NC_W18
AA10 RZQ_2/NC_AA10

GTP43014 SMD RND 22.8mil
GTP43013 SMD RND 22.8mil

HFB1M8MO331A0MR

U43001C

C1 GND_C1 — GND_M10 M10
C2 GND_C2 — GND_N1 N1
C3 GND_C3 — GND_N2 N2
C4 GND_C4 — GND_N3 N3
C5 GND_C5 — GND_N4 N4
C15 GND_C15 — GND_N5 N5
D6 GND_D6 — GND_N14 N14
D11 GND_D11 — GND_N15 N15
E1 GND_E1 — GND_P7 P7
E2 GND_E2 — GND_P8 P8
E3 GND_E3 — GND_P9 P9
E4 GND_E4 — GND_P10 P10
E5 GND_E5 — GND_P11 P11
E6 GND_E6 — GND_P12 P12
E7 GND_E7 — GND_R1 R1
E11 GND_E11 — GND_R2 R2
E14 GND_E14 — GND_R3 R3
E15 GND_E15 — GND_R4 R4
F6 GND_F6 — GND_R5 R5
G1 GND_G1 — GND_R9 R9
G2 GND_G2 — GND_R10 R10
G3 GND_G3 — GND_R14 R14
G4 GND_G4 — GND_R15 R15
G5 GND_G5 — GND_T9 T9
G9 GND_G9 — GND_T10 T10
G10 GND_G10 — GND_U1 U1
G14 GND_G14 — GND_U2 U2
G15 GND_G15 — GND_U3 U3
H9 GND_H9 — GND_U4 U4
H10 GND_H10 — GND_U5 U5
J1 GND_J1 — GND_U9 U9
J2 GND_J2 — GND_U10 U10
J3 GND_J3 — GND_U14 U14
J4 GND_J4 — GND_U15 U15
J5 GND_J5 — GND_W1 W1
J9 GND_J9 — GND_W2 W2
J10 GND_J10 — GND_W3 W3
J14 GND_J14 — GND_W4 W4
J15 GND_J15 — GND_W5 W5
K7 GND_K7 — GND_W6 W6
K8 GND_K8 — GND_W11 W11
K9 GND_K9 — GND_W14 W14
K10 GND_K10 — GND_W15 W15
K11 GND_K11 — GND_Y6 Y6
K12 GND_K12 — GND_Y11 Y11
L1 GND_L1 — GND_Y13 Y13
L2 GND_L2 — GND_AA1 AA1
L3 GND_L3 — GND_AA2 AA2
L4 GND_L4 — GND_AA3 AA3
L5 GND_L5 — GND_AA4 AA4
L14 GND_L14 — GND_AA5 AA5
L15 GND_L15 — GND_AA14 AA14
M9 GND_M9 — GND_AA15 AA15

HFB1M8MO331A0MR

U43001D

DNU_A1 A1
DNU_A2 A2
DNU_A4 A4
DNU_A6 A6
DNU_A8 A8 — SMD RND 22.8mil GTP43028
DNU_A11 A11
DNU_A13 A13
DNU_A15 A15
DNU_A17 A17
DNU_A18 A18
DNU_B1 B1
DNU_B2 B2
DNU_B4 B4
DNU_B8 B8 — SMD RND 22.8mil GTP43020
DNU_B11 B11
DNU_B13 B13
DNU_B15 B15
DNU_B17 B17
DNU_B18 B18
DNU_C6 C6
DNU_C9 C9
DNU_C11 C11
DNU_C12 C12
DNU_C16 C16
DNU/DDR_VDDQ C17 — SMD RND 22.8mil GTP43021
DNU_C17 C18 — SMD RND 22.8mil GTP43022
DNU_C18 D12
DNU_D12 E16
DNU_E16 E17
DNU_E17 E18
DNU_E18 G16
DNU_G16 G17
DNU_G17 G18
DNU_G18 J16
DNU_J16 J17
DNU_J17 J18
DNU_J18 L16
DNU_L16 L17
DNU/JTAG_TRST# N16
DNU_N16 R16
DNU_R16 U16
DNU_U16 W16
DNU_W16 W17
DNU_W17 Y7
C13 RFU_C13 — DNU/SSD_FLUSH Y8
C14 RFU_C14 — DNU/SSD_FLUSH_FB Y12
D15 RFU_D15 — DNU_Y12 Y14 — SMD RND 22.8mil GTP43029
F15 RFU_F15 — DNU_Y14 Y15
H14 RFU_H14 — DNU_Y15 AA6
H15 RFU_H15 — DNU_AA6 AA7
K14 RFU_K14 — DNU_AA7 AA8
K15 RFU_K15 — DNU_AA8 AA9
L7 RFU_L7 — DNU_AA9 AA11
L8 RFU_L8 — DNU_AA11 AA12
L9 RFU_L9 — DNU_AA12 AA13
L10 RFU_L10 — DNU_AA13 AA16
L11 RFU_L11 — DNU_AA16 AA17
L12 RFU_L12 — DNU/UART_RX AA18 — SMD RND 22.8mil GTP43024
M7 RFU_M7 — DNU/UART_TX AB1 — SMD RND 22.8mil GTP43025
M8 RFU_M8 — DNU_AB1 AB2
M11 RFU_M11 — DNU_AB2 AB4
M12 RFU_M12 — DNU_AB4 AB6
M14 RFU_M14 — DNU_AB6 AB8
M15 RFU_M15 — DNU_AB8 AB11
N7 RFU_N7 — DNU_AB11 AB13
N8 RFU_N8 — DNU_AB13 AB15
N9 RFU_N9 — DNU/VCCF AB17 — SMD RND 22.8mil GTP43027
N10 RFU_N10 — DNU_AB17 AB18
N11 RFU_N11 — DNU_AB18 AC1
N12 RFU_N12 — DNU_AC1 AC2
P14 RFU_P14 — DNU_AC2 AC4
P15 RFU_P15 — DNU_AC4 AC6
T14 RFU_T14 — DNU_AC6 AC8
T15 RFU_T15 — DNU_AC8 AC11
V14 RFU_V14 — DNU_AC11 AC13
V15 RFU_V15 — DNU_AC13 AC15
W8 RFU_W8 — DNU_AC15 AC17
W12 V_SEL0/RFU_W12 — DNU/VCCFQ AC18 — SMD RND 22.8mil GTP43026
W13 V_SEL1/RFU_W13 — DNU_AC18 — SMD RND 22.8mil GTP43023

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C43101 4.7u 6.3V 0201 SSD

PCH_SSD_UART2_TXD [25]
PCH_SSD_UART2_RXD [25]

PCIE[12:1]_TXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value
PCIE[12:1]_RXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value

Difference between USB3 and PCIe: 1. No Choke, 2. Add cap on PER (p832 at DG v1.2)
RXN/RXP cap value must be different between Gen2 and Gen3
TX (from SOC) caps are at SOC side

Always ON logic, as like Intel RVP5.

GTP43012 SMD RND 22.8mil

U43001B

G7 G8 G11 G12 H7 H8 H11 H12 J7 J8 J11 J12 — 1p2v/1p1v/0p9v/RFU_G7 … 1p2v/1p1v/0p9v/RFU_J12

1P8V_SSD
R7 R8 R11 R12 T7 T8 T11 T12 U7 U8 U11 U12 — V1P8_R7 … V1P8_U12

3P3V_SSD
D9 D10 E9 E10 W9 W10 Y9 Y10 — V3P3_D9 … V3P3_Y10

HFB1M8MO331A0MR

1P2V_SSD

V3P3_DSW
SMD RND 22.8mil GTP43015
R43018 100K 1% 0201 — 3P3V_SSD
C43034 10u 6.3V 0402
U43006 TPS62085RLTR QFN-7 (VIN, SW, EN, VOS, FB, GND, PG)
C43039 0.1u 6.3V — GND
L43002 0.47uH X950133-001 2.5X2.0X1.2
R43025 82.5K 1% 0201 DNP
R43009 82.5K 1% 0201 SSD
C43041 100p 25V 0201 DNP
R43026 215K 1% 0201 DNP
R43010 165K 1% 0201 SSD
C43035 22u 4V 20% 0603 DNP
C43036 22u 4V 20% 0603
C43037 22u 4V 20% 0603
C43038 22u 4V 20% 0603
SMD RND 22.8mil MTP43026
1P2V_SSD
R43150 10K 0201

R43010 is 215K for Samsung, 1P2V_SSD = 1.06V-1.15V + 100mV P-P ripple
R43010 is 165K for Toshiba, 1P2V_SSD = 1.2V +/- 5%
R43010 is 150K for Intel Pleasant Star, 1P2V_SSD = 1.24V+/- 4%
R43010 is 165K and R43009 is 24.9K for Hynix, 1P2V_SSD = 0.92V +/- 0.06V

3P3V_SSD
R43023 0 0201
SMD RND 22.8mil GTP43016
R43019 100K 1% 0201 — V3P3_DSW
R43134 100K 0201 — GND
U43005 TPS62085RLTR QFN-7 (VIN, SW, EN, VOS, FB, GND, PG)
C43029 10u 6.3V 0402
C43080 0.1u 6.3V — GND
L43001 0.47uH X950133-001 2.5X2.0X1.2
C43040 100p 25V 0201 DNP
C43030 22u 4V 20% 0603
C43031 22u 4V 20% 0603
C43032 22u 4V 20% 0603
C43033 22u 4V 20% 0603
SMD RND 22.8mil MTP43027
1P8V_SSD
R43007 82.5K 1% 0201
R43008 33K 1% 0201
R43024 33K 1% 0201

Load R43100 and DNP R43101 for U43001 loaded and U44007 DNP (Single SSD)
DNP R43100 and Load R43101 for both U43001 and U44007 loaded (Dual SSD)

[44] SSD2_JTAG_TDO
[43,44] SSD1_JTAG_TDO
R43100 0 0402 SSD
R43101 0 0402 SSD
SSD_JTAG_TDO [31]
MTP43020 SMD RND 22.8mil
MTP43021 SMD RND 22.8mil
MTP43022 SMD RND 22.8mil
MTP43023 SMD RND 22.8mil
[31,43,44] SSD_JTAG_TMS — SSD_JTAG_TMS
[31,43,44] SSD_JTAG_TCK — SSD_JTAG_TCK
[31,43] SSD_JTAG_TDI — SSD_JTAG_TDI
SSD_JTAG_TDO

GTP43017 SMD RND 22.8mil — SSD_DIAG1 — SSD_DIAG1 [43]
GTP43018 SMD RND 22.8mil — SSD_DIAG0 — SSD_DIAG0 [43,44]

3P3V_SSD
SSD C43006 6.3V 1u 0402
SSD C43007 6.3V 1u 0402
SSD C43008 0.1u 6.3V 0201
SSD C43009 0.1u 6.3V 0201
SSD C43010 6.3V 22u 0603
SSD C43011 6.3V 22u 0603

1P8V_SSD
SSD C43013 6.3V 1u 0402
SSD C43014 6.3V 1u 0402
SSD C43015 0.1u 6.3V 0201
SSD C43016 0.1u 6.3V 0201
SSD C43017 6.3V 22u 0603
SSD C43018 6.3V 22u 0603

1P2V_SSD
SSD C43019 6.3V 1u 0402
SSD C43020 6.3V 1u 0402
SSD C43021 0.1u 6.3V 0201
SSD C43022 0.1u 6.3V 0201
SSD C43023 0.1u 6.3V 0201
SSD C43024 0.1u 6.3V 0201
DNP C43025 6.3V 22u 0603
SSD C43026 6.3V 22u 0603

1P8V_SSD
DNP C43100 0.1u 6.3V 0201
R43120 4.7K 0201 DNP
R43123 4.7K 0201 DNP
[56] GP_SSD_FLUSH — 499 R43113 0201 DNP
U43007 74AUP1G32GX
[27] SAM_SSD_FLUSH
MTP43025 SMD RND 22.8mil
R43108 200K 0201 DNP
R43109 200K 0201 DNP
GTP43019 SMD RND 22.8mil
SSD_DIAG0 [43,44]

1P8V_SSD2
1P8V_SSD
3P3V_SSD
R43124 100K 0201 DNP
R43121 100K 0201 DNP
R43125 4.7K 0201 DNP
R43122 4.7K 0201 DNP
Q43001A
Q43001B
3P3VA_SW
R43107 200K 0201
[43] SSD_DIAG1
[44] SSD2_DIAG1
SSD_FLUSH_DONE [27,56]
R43106 200K 0201 DNP
R43110 200K 0201 DNP

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Title:	43. SSD page 1		
Microsoft Confidential	Engineer:	Surface	
Size: A	Project Name: Custom		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 43 of 79		

For common BGA SSDs

U44007A

[20] PCIECLK_SSD2_DP — R44012 SSD 0 0402 — D4 REFCLK_P
[20] PCIECLK_SSD2_DN — R44013 SSD 0 0402 — D5 REFCLK_N

[24] PCIE_SSD2_TX11_DP — F4 SATAmAp/PERp0
[24] PCIE_SSD2_TX11_DN — F5 SATAmAm/PERn0

[24] PCIE_SSD2_RX11_DP — 0.22u 0201 6.3V SSD C44121 — H4 SATAmBp/PETp0
[24] PCIE_SSD2_RX11_DN — 0.22u 0201 6.3V SSD C44001 — H5 SATAmBm/PETn0

[24] PCIE_SSD2_TX12_DP — K4 PER_P1
[24] PCIE_SSD2_TX12_DN — K5 PER_N1

[24] PCIE_SSD2_RX12_DP — 0.22u 0201 6.3V SSD C44002 — M4 PET_P1
[24] PCIE_SSD2_RX12_DN — 0.22u 0201 6.3V SSD C44003 — M5 PET_N1

[43] SSD_PERST_N — P4 PERp2/NC_P4
P5 PERn2/NC_P5

1P8V_SSD
0201 C44118 0.1u 6.3V DNP GND

T4 PETp2/NC_T4
T5 PETn2/NC_T5

V4 PERp3/NC_V4
V5 PERn3/NC_V5

U44002 SN74AUP1G08DRYR DNP
[22,27,34,38,43,56] PLT_RST_BUF_N
[25,43] PCIE_SSD_PERST_N
R44126 0 0201
Y4 PETp3/NC_Y4
Y5 PETn3/NC_Y5
D7 PERST#
R44010 100K 0201 DNP GND
F14 PEDET
D8 CLKREQ#
D14 SUSCLK/NC_D14
E8 DEVSLP/NC_E8
E12 PEWAKE#/NC_E12
[20] SSD2_PCIECLK_REQ_N — W7 LED1#/ DAS
GTP44001 SMD RND 22.8mil

DNP R44016 1M 0402
XRCGB25M000F2P00R0 Y44001
25V C44120 DNP 10p 0201
C44122 DNP 25V 10p 0201
B6 CAL_P/NC_B6
SSD2_XTAL_OUT — C7 XTAL_ OUT/NC_C7
SSD2_XTAL_IN — C8 XTAL_IN/NC_C8
C10 RZQ_1/NC_C10
[43] SSD2_DIAG1 — SSD2_DIAG1 — D13 DIAG1/I2C_DATA
[43] SSD_DIAG0 — SSD_DIAG0 — E13 DIAG0/I2C_CLK
L18 JTAG_TRST#/NC_L18
[31,43] SSD_JTAG_TCK — SSD_JTAG_TCK — N17 JTAG_TCK
[31,43] SSD_JTAG_TMS — SSD_JTAG_TMS — N18 JTAG_TMS
[43] SSD1_JTAG_TDI — R17 JTAG_TDI
[43] SSD2_JTAG_TDO — SSD2_JTAG_TDO — R18 JTAG_TDO
U17 SMB_CLK/NC_U17
U18 SMB_DATA/NC_U18
W18 ALERT#/NC_W18
AA10 RZQ_2/NC_AA10
GTP44004 SMD RND 22.8mil
GTP44003 SMD RND 22.8mil

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U44007C

GND_C1 C1, GND_C2 C2, GND_C3 C3, GND_C4 C4, GND_C5 C5, GND_C15 C15, GND_D6 D6, GND_D11 D11, GND_E1 E1, GND_E2 E2, GND_E3 E3, GND_E4 E4, GND_E5 E5, GND_E6 E6, GND_E7 E7, GND_E11 E11, GND_E14 E14, GND_E15 E15, GND_F6 F6, GND_G1 G1, GND_G2 G2, GND_G3 G3, GND_G4 G4, GND_G5 G5, GND_G9 G9, GND_G10 G10, GND_G14 G14, GND_G15 G15, GND_H9 H9, GND_H10 H10, GND_J1 J1, GND_J2 J2, GND_J3 J3, GND_J4 J4, GND_J5 J5, GND_J9 J9, GND_J10 J10, GND_J14 J14, GND_J15 J15, GND_K7 K7, GND_K8 K8, GND_K9 K9, GND_K10 K10, GND_K11 K11, GND_K12 K12, GND_L1 L1, GND_L2 L2, GND_L3 L3, GND_L4 L4, GND_L5 L5, GND_L14 L14, GND_L15 L15, GND_M9 M9

GND_M10 M10, GND_N1 N1, GND_N2 N2, GND_N3 N3, GND_N4 N4, GND_N5 N5, GND_N14 N14, GND_N15 N15, GND_P7 P7, GND_P8 P8, GND_P9 P9, GND_P10 P10, GND_P11 P11, GND_P12 P12, GND_R1 R1, GND_R2 R2, GND_R3 R3, GND_R4 R4, GND_R5 R5, GND_R9 R9, GND_R10 R10, GND_R14 R14, GND_R15 R15, GND_T9 T9, GND_T10 T10, GND_U1 U1, GND_U2 U2, GND_U3 U3, GND_U4 U4, GND_U5 U5, GND_U9 U9, GND_U10 U10, GND_U14 U14, GND_U15 U15, GND_W1 W1, GND_W2 W2, GND_W3 W3, GND_W4 W4, GND_W5 W5, GND_W6 W6, GND_W11 W11, GND_W14 W14, GND_W15 W15, GND_Y6 Y6, GND_Y11 Y11, GND_Y13 Y13, GND_AA1 AA1, GND_AA2 AA2, GND_AA3 AA3, GND_AA4 AA4, GND_AA5 AA5, GND_AA14 AA14, GND_AA15 AA15

HFB1M8MO331A0MR

U44007D

DNU_A1 A1, DNU_A2 A2, DNU_A4 A4, DNU_A6 A6, DNU_A8 A8, DNU_A11 A11, DNU_A13 A13, DNU_A15 A15, DNU_A17 A17, DNU_A18 A18, DNU_B1 B1, DNU_B2 B2, DNU_B4 B4, DNU_B8 B8, DNU_B11 B11, DNU_B13 B13, DNU_B15 B15, DNU_B17 B17, DNU_B18 B18, DNU_C6 C6, DNU_C9 C9, DNU_C11 C11, DNU_C12 C12, DNU/DDR_VDDQ C16, DNU_C17 C17, DNU_C18 C18, DNU_D12 D12, DNU_E16 E16, DNU_E17 E17, DNU_E18 E18, DNU_G16 G16, DNU_G17 G17, DNU_G18 G18, DNU_J16 J16, DNU_J17 J17, DNU_J18 J18, DNU_L16 L16, DNU/JTAG_TRST# L17, DNU_N16 N16, DNU_R16 R16, DNU_U16 U16, DNU_W16 W16, DNU_W17 W17, DNU_Y7 Y7, DNU/SSD_FLUSH Y8, DNU/SSD_FLUSH_FB Y12, DNU_D15 Y12, DNU_Y14 Y14, DNU_Y15 Y15, DNU_Y16 AA6, DNU_AA6 AA7, DNU_AA7 AA8, DNU_AA8 AA9, DNU_AA9 AA11, DNU_AA11 AA12, DNU_AA12 AA13, DNU_AA13 AA16, DNU_AA16 AA17, DNU/UART_RX AA18, DNU/UART_TX AB1, DNU_AB1 AB2, DNU_AB2 AB4, DNU_AB4 AB6, DNU_AB6 AB8, DNU_AB8 AB11, DNU_AB11 AB13, DNU_AB13 AB15, DNU/VCCF AB17, DNU_AB17 AB18, DNU_AB18 AC1, DNU_AC1 AC2, DNU_AC2 AC4, DNU_AC4 AC6, DNU_AC6 AC8, DNU_AC8 AC11, DNU_AC11 AC13, DNU_AC13 AC15, DNU_AC15 AC17, DNU/VCCFQ AC18

C13 RFU_C13, C14 RFU_C14, D15 RFU_D15, F15 RFU_F15, H14 RFU_H14, H15 RFU_H15, K14 RFU_K14, K15 RFU_K15, L7 RFU_L7, L8 RFU_L8, L9 RFU_L9, L10 RFU_L10, L11 RFU_L11, L12 RFU_L12, M7 RFU_M7, M8 RFU_M8, M11 RFU_M11, M12 RFU_M12, M14 RFU_M14, M15 RFU_M15, N7 RFU_N7, N8 RFU_N8, N9 RFU_N9, N10 RFU_N10, N11 RFU_N11, N12 RFU_N12, P14 RFU_P14, P15 RFU_P15, T14 RFU_T14, T15 RFU_T15, V14 RFU_V14, V15 RFU_V15, W8 RFU_W8, V_SEL0/RFU_W12, V_SEL1/RFU_W13

SMD RND 22.8mil GTP44020
SMD RND 22.8mil GTP44021
SMD RND 22.8mil GTP44022
C44190 4.7u 6.3V 0201 DNP
SMD RND 22.8mil GTP44024
SMD RND 22.8mil GTP44025
SMD RND 22.8mil GTP44027
SMD RND 22.8mil GTP44026
GTP44002 SMD RND 22.8mil

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PCIE[12:1]_TXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value
PCIE[12:1]_RXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value

Difference between USB3 and PCIe: 1. No Choke, 2. Add cap on PER (p832 at DG v1.2)
RXN/RXP cap value must be different between Gen2 and Gen3
TX (from SOC) caps are at SOC side

Always ON logic, as like Intel RVP5.

V3P3_DSW
SMD RND 22.8mil GTP44015
R44118 100K 1% 0201
3P3V_SSD
U44006 TPS62085RLTR QFN-7
VIN 7, SW 6, EN 1, VOS 4, FB 3, GND 5, PG 2
L44102 0.47uH X950133-001 2.5X2.0X1.2
C44134 10u 6.3V 0402
C44139 0.1u 6.3V 0201
GND
R44018 82.5K 1% 0201 DNP
R44109 24.9K 1% 0201 SSD
C44141 100p 25V 0201 DNP
R44019 215K 1% 0201 DNP
R44110 165K 1% 0201 SSD
TP44007 SMD RND 22.8mil
MTP44026 SMD RND 22.8mil
1P2V_SSD2
C44035 22u 4V 20% 0603
DNP C44136 22u 4V 20% 0603
C44137 22u 4V 20% 0603
C44138 22u 4V 20% 0603
R44150 10K 0201 SSD

R44110 is 215K for Samsung, 1P2V_SSD = 1.06V-1.15V + 100mV P-P ripple
R44110 is 165K for Toshiba, 1P2V_SSD = 1.2V +/- 5%
R44110 is 165K and R44109 is 24.9K for Hynix, 1P2V_SSD = 0.92V +/- 0.08V
only support Hynix 1TB

R44123 0 0201
R44119 100K 1% 0201
V3P3_DSW
U44005 TPS62085RLTR QFN-7
VIN 7, SW 6, EN 1, VOS 4, FB 3, GND 5, PG 2
L44101 0.47uH X950133-001 2.5X2.0X1.2
C44129 10u 6.3V 0402
C44180 0.1u 6.3V 0201
GND
R44134 100K 0201
R44107 82.5K 1% 0201
C44140 100p 25V 0201 DNP
R44108 33K 1% 0201
R44124 33K 1% 0201
TP44006 SMD RND 22.8mil
MTP44027 SMD RND 22.8mil
1P8V_SSD2
C44130 22u 4V 20% 0603
C44131 22u 4V 20% 0603
C44132 22u 4V 20% 0603
C44133 22u 4V 20% 0603

1P2V_SSD2
U44007B HFB1M8MO331A0MR

G7 1p2v/1p1v/0p9v/RFU_G7, G8 1p2v/1p1v/0p9v/RFU_G8, G11 1p2v/1p1v/0p9v/RFU_G11, G12 1p2v/1p1v/0p9v/RFU_G12, H7 1p2v/1p1v/0p9v/RFU_H7, H8 1p2v/1p1v/0p9v/RFU_H8, H11 1p2v/1p1v/0p9v/RFU_H11, H12 1p2v/1p1v/0p9v/RFU_H12, J7 1p2v/1p1v/0p9v/RFU_J7, J8 1p2v/1p1v/0p9v/RFU_J8, J11 1p2v/1p1v/0p9v/RFU_J11, J12 1p2v/1p1v/0p9v/RFU_J12

1P8V_SSD2
R7 V1P8_R7, R8 V1P8_R8, R11 V1P8_R11, R12 V1P8_R12, T7 V1P8_T7, T8 V1P8_T8, T11 V1P8_T11, T12 V1P8_T12, U7 V1P8_U7, U8 V1P8_U8, U11 V1P8_U11, U12 V1P8_U12

3P3V_SSD
D9 V3P3_D9, D10 V3P3_D10, E9 V3P3_E9, E10 V3P3_E10, W9 V3P3_W9, W10 V3P3_W10, Y9 V3P3_Y9, Y10 V3P3_Y10

3VSUS_ORG
R44125 0201 49.9K SSD
R44017 0402 0 SSD
SSD2_SATA_PCIE_DET_N [24]

R44125 is loaded for non-RAID case
R44017 is loaded for the RAID case

3P3V_SSD
SSD C44107 6.3V 1u 0402, SSD C44104 6.3V 1u 0402, SSD C44105 0.1u 6.3V 0201, SSD C44026 0.1u 6.3V 0201, SSD C44108 6.3V 22u 0603, SSD C44030 6.3V 22u 0603

1P8V_SSD2
SSD C44038 6.3V 1u 0402, SSD C44028 6.3V 1u 0402, SSD C44115 0.1u 6.3V 0201, SSD C44109 0.1u 6.3V 0201, SSD C44031 6.3V 22u 0603, SSD C44033 6.3V 22u 0603

1P2V_SSD2
SSD C44025 6.3V 1u 0402, SSD C44103 6.3V 1u 0402, SSD C44024 0.1u 6.3V 0201, SSD C44106 0.1u 6.3V 0201, SSD C44113 0.1u 6.3V 0201, SSD C44112 0.1u 6.3V 0201, DNP C44114 6.3V 22u 0603, SSD C44111 6.3V 22u 0603

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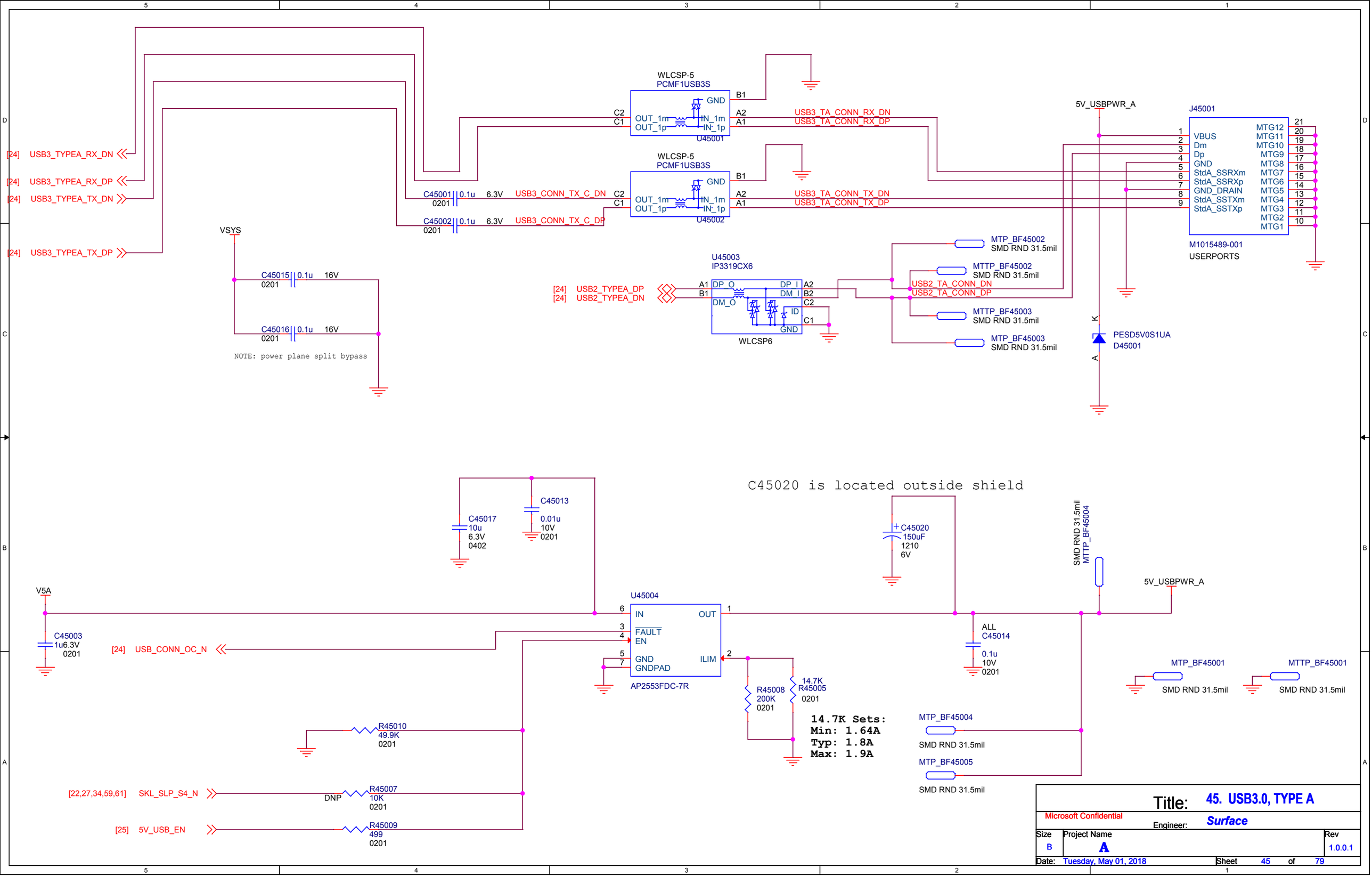
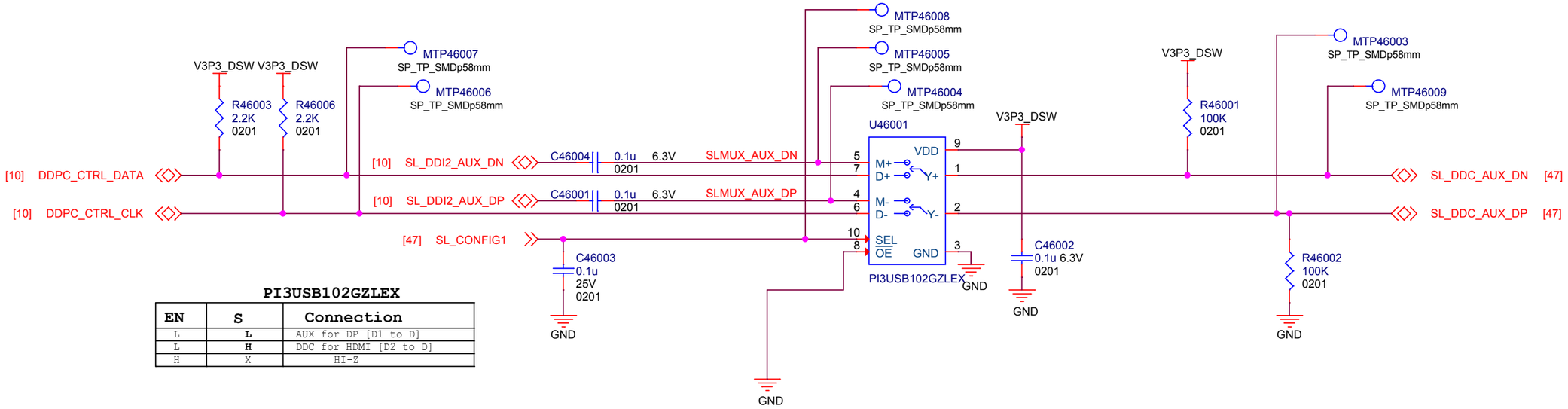
	Engineer: Surface	
Size: Custom	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 44 of 79	


[24] USB3_TYPEA_RX_DN
[24] USB3_TYPEA_RX_DP
[24] USB3_TYPEA_TX_DN
[24] USB3_TYPEA_TX_DP
WLCSP-5
PCMF1USB3S
U45001
U45002
C45001 0.1u 6.3V 0201
C45002 0.1u 6.3V 0201
USB3_CONN_TX_C_DN
USB3_CONN_TX_C_DP
USB3_TA_CONN_RX_DN
USB3_TA_CONN_RX_DP
USB3_TA_CONN_TX_DN
USB3_TA_CONN_TX_DP
5V_USBPWR_A
J45001
M1015489-001
USERPORTS
VSYS
C45015 0.1u 16V 0201
C45016 0.1u 16V 0201
NOTE: power plane split bypass
U45003
IP3319CX6
WLCSP6
[24] USB2_TYPEA_DP
[24] USB2_TYPEA_DN
USB2_TA_CONN_DN
USB2_TA_CONN_DP
MTP_BF45002
SMD RND 31.5mil
MTTP_BF45002
SMD RND 31.5mil
MTTP_BF45003
SMD RND 31.5mil
MTP_BF45003
SMD RND 31.5mil
PESD5V0S1UA
D45001
C45020 is located outside shield
C45017 10u 6.3V 0402
C45013 0.01u 10V 0201
C45020 150uF 1210 6V
SMD RND 31.5mil MTTP_BF45004
V5A
C45003 1u6.3V 0201
[24] USB_CONN_OC_N
U45004
AP2553FDC-7R
ALL C45014 0.1u 10V 0201
MTP_BF45001
SMD RND 31.5mil
MTTP_BF45001
SMD RND 31.5mil
R45010 49.9K 0201
R45008 200K 0201
14.7K R45005 0201
14.7K Sets:
Min: 1.64A
Typ: 1.8A
Max: 1.9A
MTP_BF45004
SMD RND 31.5mil
MTP_BF45005
SMD RND 31.5mil
[22,27,34,59,61] SKL_SLP_S4_N
DNP R45007 10K 0201
[25] 5V_USB_EN
R45009 499 0201
Title: 45. USB3.0, TYPE A
Microsoft Confidential
Engineer: Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Tuesday, May 01, 2018
Sheet 45 of 79

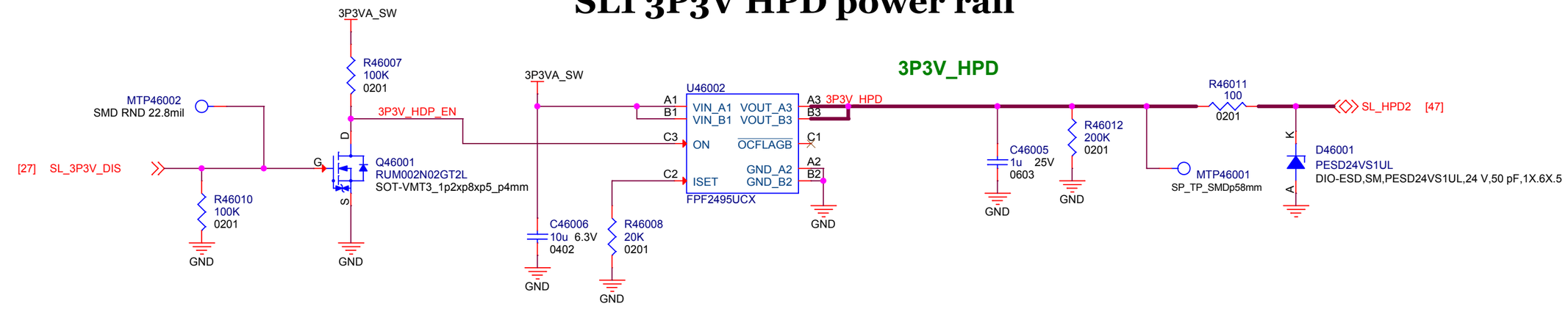
SL1 DP mux to HDMI/DVI Dongle control



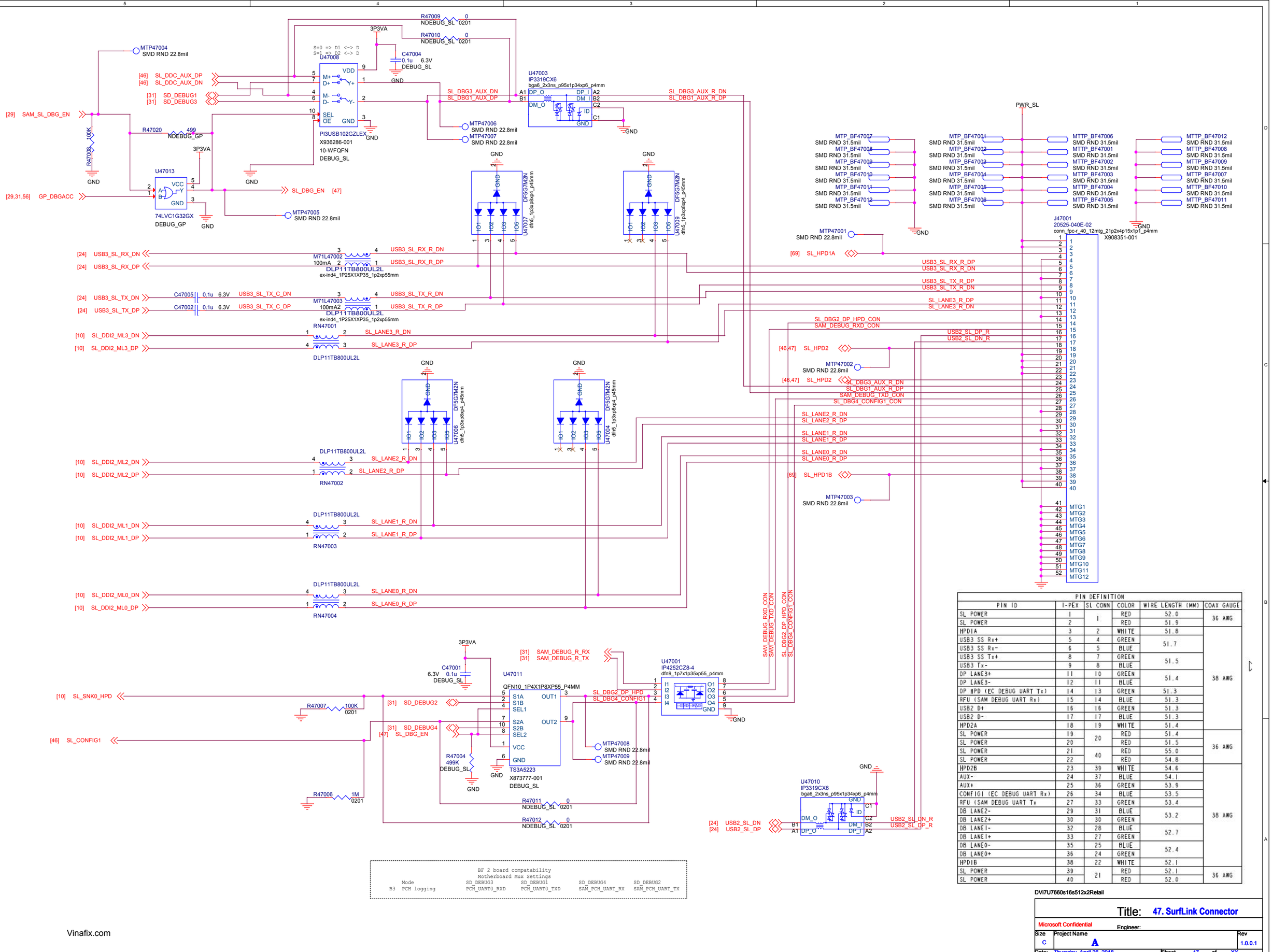
PI3USB102GZLEX

EN	S	Connection
L	**L**	AUX for DP [D1 to D]
L	**H**	DDC for HDMI [D2 to D]
H	X	HI-Z

SL1 3P3V HPD power rail



Title:	46. SL HDMI MUX/3P3V_HPD		
Engineer:	Surface		
Size: B	Project Name: A		Rev: 1.00
Date: Thursday, April 26, 2018		Sheet 46 of 76	



PIN DEFINITION					
PIN ID	I-PEX	SL CONN	COLOR	WIRE LENGTH (MM)	COAX GAUGE
SL POWER	1	1	RED	52.0	36 AWG
SL POWER	2		RED	51.9	
HPD1A	3	2	WHITE	51.8	38 AWG
USB3 SS Rx+	5	4	GREEN	51.7	
USB3 SS Rx-	6	5	BLUE		
USB3 SS Tx+	8	7	GREEN	51.5	
USB3 Tx-	9	8	BLUE		
DP LANE3+	11	10	GREEN	51.4	
DP LANE3-	12	11	BLUE		
DP HPD (EC DEBUG UART Tx)	14	13	GREEN	51.3	
RFU (SAM DEBUG UART Rx)	15	14	BLUE	51.3	
USB2 D+	16	16	GREEN	51.3	
USB2 D-	17	17	BLUE	51.3	
HPD2A	18	19	WHITE	51.4	
SL POWER	19	20	RED	51.4	36 AWG
SL POWER	20		RED	51.5	
SL POWER	21	40	RED	55.0	
SL POWER	22		RED	54.8	
HPD2B	23	39	WHITE	54.6	38 AWG
AUX-	24	37	BLUE	54.1	
AUX+	25	36	GREEN	53.9	
CONFIG1 (EC DEBUG UART Rx)	26	34	BLUE	53.5	
RFU (SAM DEBUG UART Tx	27	33	GREEN	53.4	
DB LANE2-	29	31	BLUE	53.2	
DB LANE2+	30	30	GREEN		
DB LANE1-	32	28	BLUE	52.7	
DB LANE1+	33	27	GREEN		
DB LANE0-	35	25	BLUE	52.4	
DB LANE0+	36	24	GREEN		
HPD1B	38	22	WHITE	52.1	
SL POWER	39	21	RED	52.1	36 AWG
SL POWER	40		RED	52.0	

BF 2 board compatability Motherboard Mux Settings					
Mode	SD_DEBUG3	SD_DEBUG1	SD_DEBUG4	SD_DEBUG2	
B3 PCH logging	PCH_UART0_RXD	PCH_UART0_TXD	SAM_PCH_UART_RX	SAM_PCH_UART_TX	

DVi7U7660s16s512x2Retail

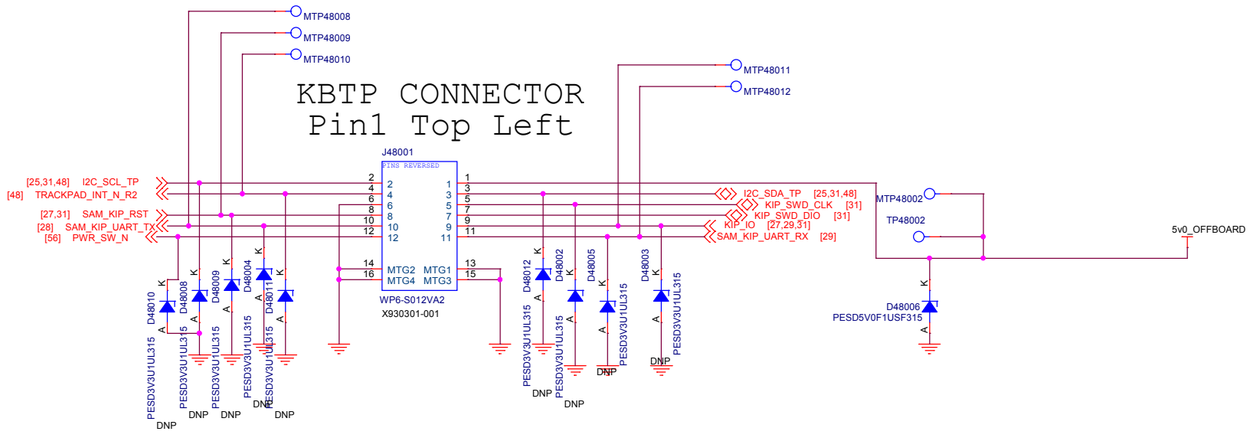
Title: 47. SurfLink Connector

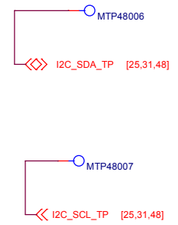
Microsoft Confidential

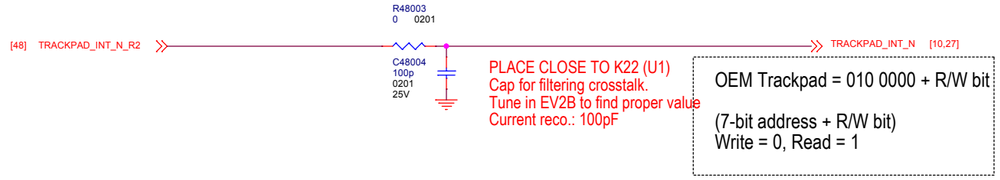
Engineer:

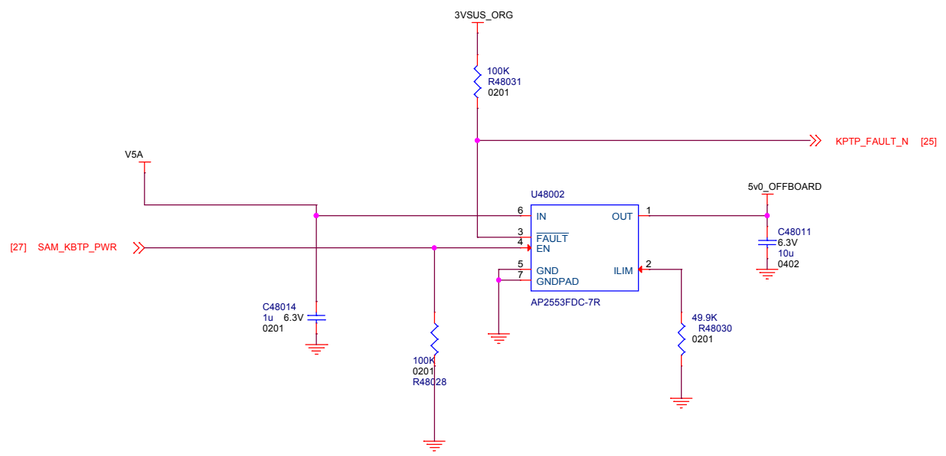
Size	Project Name	Rev
C	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 47 of XX









Vinafix.com

Title:	48. Blade	
Microsoft Confidential	Engineer: Surface	
Size: Custom A	Project Name	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 48 of 79	

[25,49] TPANEL_RST_N

TS_V1P0_TCH_DIG

1P8V_TS

TS_V1P0_TCH_SSI

3VSUS_ORG

[21,49] TS_SPI_CLK

[21,49] TS_SPI_MOSI

[21,49] TS_SPI_MISO

[21,49] TS_SPI_CS_N

[30] TS_IRQ_3V3_N

[20,49] FLASH_PROTECT_N

GPIO signals may toggle during boot (see errata document). Please make sure to implement the workaround described in the errata

[31,49] TS_TCK_1V8

[31,49] TS_TDI_1V8

[31,49] TS_TDO_1V8

[31,49] TS_TMS_1V8

TS_HOST_CLK (If Available)

TS_DLITE_XI

TS_DLITE_XO_R

XTAL-XTAL,SM,48 MHZ,15 PPM,7 PF,2X1.6X0.155MM

Y49001 3_TS_DLITE_XO 48MHz

The crystal and capacitors should be placed as close as possible to the DS, with short and symmetrical traces to the XI and XO pins

TS_FLASH_SCK

TS_FLASH_MISO

TS_FLASH_MOSI

TS_FLASH_CS#

U49003 son9_4x4xp6_p8mm

MX25U1635FZUI

1P8V_TS

DNP

FLASH_PROTECT_N [20,49]

5V_TS

TPANEL_RST_N [25,49]

TS_TCK_1V8 [31,49]

TS_TMS_1V8 [31,49]

TS_TDO_1V8 [31,49]

TS_TDI_1V8 [31,49]

TS_SPI_CLK [21,49]

TS_SPI_MISO [21,49]

TS_SPI_MOSI [21,49]

TS_SPI_CS_N [21,49]

Not to be used for DEBUG build

Use MTP points on pg 31 instead

50 pin Drive Connector

J49002

5024265010

50 pin Flex Breakout

H0 to H47 are the horizontal sensor traces

V0 to V71 are the vertical sensor lines

80 pin Sense Connector

J49003

5024268010

80 pin Flex Breakout

U49001 DS-D5000-B064

Special keepout made to isolate buck and boost ground from system ground

U49002 DS-A5048_82BGA Add underfill

U49004 DS-A5048_82BGA Add underfill

U49005 DS-A5048_82BGA Add underfill

TS_BOOST_HV_IN

TS_HV_IN

PMEG4015EPK315

2.2uH 1.4A L49001 2.0X1.6X1.0MM

4.7uH L49002 0805

X950113-001 L49003 0.47uH 0805

V1P8 Analog

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Microsoft Confidential

Title: 49. Touch

Engineer: Surface

Size: Custom | Project Name: A | Rev: 1.0.0.1

Date: Thursday, April 26, 2018 | Sheet 49 of 76

1P8V_WIFI_INT_OUT
VDD1V8_RF_K9
C50003 1u 6.3V 0201
C50005 3.3p 25V 0201
VDD1V8_RF_K3
C50007 1u 6.3V 0201
C50008 100p 25V 0201
VDD1V8_RF_J1
C50010 100p 25V 0201
VDD1V8_RF_H1
C50013 100p 25V 0201
VDD1V8_RF_G1
C50014 1u 6.3V 0201
VDD1V8_RF_F1
C50023 0.1u 6.3V 0201
VDD1V8_RF_M14
C50029 2.2u 6.3V 0402
C50030 100p 25V 0201
VDD1V8_RF_NFC_E14
C50034 0.1u 6.3V 0201
1P8V_WIFI_INT_OUT
VDD1V8_RF_H16
C50001 100p 25V 0201
VDD1V8_RF_K16
C50002 100p 25V 0201
VDD1V8_RF_G16
C50006 100p 25V 0201
VDD1V8_RF_D2
C50011 100p 25V 0201
VDD1V8_RF_C1
C50012 100p 25V 0201
VDD1V8_RF_PCIE_HSIC_A10
C50016 1u 6.3V 0201
C50017 10p 50V 0201
3P3V_RADIO
VDD3V3_RF_M3
C50026 10u 6.3V 0603
C50027 100p 25V 0201
C50028 3.3p 25V 0201
VDD3V3_RF_M9
C50031 10u 6.3V 0603
C50032 100p 25V 0201
C50033 3.3p 25V 0201
VDD3V3_RF_B11
C50035 1u 6.3V 0201
C50037 0.1u 6.3V 0201
VIO_RF_L12
C50039 0.1u 6.3V 0201
3P3V_RADIO
R50042 10K 0201 PCIE_WIFI_CLKREQ_N [20,50]
R50036 10K 0201 PCIE_WIFI_WAKE_N [25,50]
R50037 DNP 49.9K 0201
3P3V_RADIO
R50038 DNP 10K 0201
R50039 49.9K 0201 PCIE_WIFI_DISABLE_N [25,50]
R50040 DNP 10K 0201
R50041 49.9K 0201 PCIE_WIFI_PERST_N [25,50]
1P8V_WIFI_INT_OUT
U50001A
A10 AVDD18_1
J1 AVDD18_10
K3 AVDD18_11
K9 AVDD18_12
K16 AVDD18_13
M14 AVDD18_14
C1 AVDD18_2
D2 AVDD18_3
E14 AVDD18_4
F1 AVDD18_5
G1 AVDD18_6
G16 AVDD18_7
H1 AVDD18_8
H16 AVDD18_9
B11 AVDD33_1
D16 AVDD33_2
M3 AVDD33_3
M9 AVDD33_4
D15 AVSS1
H10 AVSS10
H15 AVSS11
J15 AVSS12
J16 AVSS13
K1 AVSS14
K15 AVSS15
L2 AVSS16
L3 AVSS17
L5 AVSS18
L7 AVSS19
F2 AVSS2
L9 AVSS20
L10 AVSS21
L13 AVSS22
L16 AVSS23
F3 AVSS3
F16 AVSS4
G2 AVSS5
G15 AVSS6
H2 AVSS7
H3 AVSS8
H9 AVSS9
C3 GPIO[0] WIFI_GPIO0 MTTP50002 SMD RND 22.8mil
D5 GPIO[1] WIFI_GPIO1 MTTP50004 SMD RND 22.8mil
B2 GPIO[2] WIFI_GPIO2 MTTP50003 SMD RND 22.8mil
A3 GPIO[3]
E7 GPIO[4]
E8 GPIO[5]
E9 GPIO[6]
E10 GPIO[7]
K13 GPIO[8]/LED_OUT_WLAN
J13 GPIO[9]/LED_OUT_BT
E6 GPIO[10]/SER_WB
E11 GPIO[11]/LED_OUT_NFC
D8 GPIO[12]/PCIE_PERSTn PCIE_W_PERST_N
B7 GPIO[13]/PCIE_W_DISABLE PCIE_W_DISABLE
B6 GPIO[14]
A5 GPIO[15]
D6 GPIO[16]
B5 GPIO[17]
C6 GPIO[18]
C4 GPIO[19]
C5 GPIO[20]
B3 GPIO[21]
B4 GPIO[22]
C2 GPIO[23]
D4 GPIO[24]
G5 CONFIG_HOST[0] WF_CNFG_HST0 MTTP50005 SMD RND 22.8mil
E5 CONFIG_HOST[1] WF_CNFG_HST1 MTTP50006 SMD RND 22.8mil
F4 CONFIG_HOST[2] WF_CNFG_HST2 MTTP50007 SMD RND 22.8mil
E4 CONFIG_HOST[3] WF_CNFG_HST3 MTTP50008 SMD RND 22.8mil
M15 BRF_ANT BRF_ANT_M15 [50]
B14 BUCK11_SENSE
A15 BUCK11_VOUT WF_BUCK11_VOUT L50002 2.2uH 2.5X2X1.2MM 1.67A
C15 BUCK18_SENSE
B16 BUCK18_VOUT WF_BUCK18_VOUT L50003 2.2uH 2.5X2X1.2MM 1.67A
88W8897-B1-CBK2-T
3P3V_RADIO
MTTP50004 SMD RND 22.8mil
C50009 6.3V 0.1u 0201
VDD3V3_RF_D16
C50070 2p 25V 0201
C50071 2p 25V 0201
DNP C50004 0.1u 6.3V 0201
PCIE_W_PERST_N 220 0201 R50001 PCIE_WIFI_PERST_N [25,50]
PCIE_W_DISABLE 0 0201 R50002 PCIE_WIFI_DISABLE_N [25,50]
1P1V_WIFI_INT 1.1V R50003 0 0201 1P1V_WIFI_INT_OUT
1P8V_WIFI_INT 1.8V R50006 0 0201 1P8V_WIFI_INT_OUT
1P8V_WIFI_INT_OUT
R50005 49.9K 0201
R50007 49.9K 0201
R50008 49.9K 0201
R50009 49.9K 0201
C50015 10u 6.3V 0603
1P8V_WIFI_INT
3P3V_WWAN
L50001 0402 2.2A 30 OHM 30 Ohm
3P3V_RADIO
C50018 0.1u 6.3V 0201
C50020 10u 6.3V 0603
C50021 0.1u 6.3V 0201
OPTION HOST VIO
1P8V_WIFI_INT_OUT
3P3V_RADIO
DNP R50014 0 0201
R50015 0 0201
VIO
VIO
C50036 0.1u 6.3V 0201
WIFI > PCIe3
[20,50] PCIE_WIFI_CLKREQ_N R50021 0 0201 PCIE_WIFI_CLKREQ_N_R
[20] PCIE_WIFI_RCLK_DN R50022 0 0201 PCIE_WIFI_RCLK_R_DN
[20] PCIE_WIFI_RCLK_DP R50023 0 0201 PCIE_WIFI_RCLK_R_DP
[24] PCIE_WIFI_TX9_DN
[24] PCIE_WIFI_TX9_DP
[24] PCIE_WIFI_RX9_DN C50045 0.1u 6.3V 0201 PCIE_WIFI_C_RX9_DN
[24] PCIE_WIFI_RX9_DP C50046 0.1u 6.3V 0201 PCIE_WIFI_C_RX9_DP
[25,50] PCIE_WIFI_WAKE_N R50024 0 0201 PCIE_WAKE_N_R
[25] WLAN_PWD_N R50025 0 0201
SMD RND 31.5mil MTP_BF50001 M_PDN
SMD RND 31.5mil MTP_BF50002 AT0
R50027 49.9K 0201
SMD RND 31.5mil MTP_BF50003
Done: RF_CNTL0_N = 1 for 40MHz auto calibration
U50001B
D10 RES_D10
C10 RES_C10
E15 NFC_ANT_N
E16 NFC_ANT_P
F13 NFC_SWP1_IO
F14 NFC_SWP1_VDDIN
F15 NFC_SWP1_VDDOUT
F12 NFC_SWP2_IO
E13 NFC_SWP2_VDDOUT
G14 NFC_TWSI_CLK
G13 NFC_TWSI_SDA
E12 NFC_VDDANT
G12 NFC_WI_IN
C7 PCIE_CLKREQn
D9 PCIE_RCLK_N
C8 PCIE_RCLK_P
C9 PCIE_RX_N
B9 PCIE_RX_P
B8 PCIE_TX_N
A8 PCIE_TX_P
D7 PCIE_WAKEn
D13 PDn
D14 RES1
H11 RES10
H12 RES11
J12 RES12
K12 RES13
F8 RES2
F9 RES3
F10 RES4
F11 RES5
G4 RES6
G7 RES7
G8 RES8
G11 RES9
G9 RF_CNTL0_N
G10 RF_CNTL1_P
M5 RF_TR_2_A
M10 RF_TR_2_B
M2 RF_TR_5_A
M7 RF_TR_5_B
B12 SD_CLK
C12 SD_CMD
88W8897-B1-CBK2-T
C50038 0.1u 6.3V 0201 NFC_SWP1_VDDIN
J14 TCK
H14 TDI
H13 TDO
L14 TMS
USB_DMNS
USB_DPLS
VBAT_IN
VBLDO33_CNTL
VBLDO33_SENSE
VDD11
VDD12
VIO
VIO_RF
VIO_SD
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
XTAL_IN
XTAL_OUT
SLP_CLK_IN
SER_DAT
SER_CSn
SER_CLK
SD_DAT[0]
SD_DAT[1]
SD_DAT[2]
SD_DAT[3]
MTTP50009 SMD RND 22.8mil PLACE TP's on BOTTOM,
MTTP50010 SMD RND 22.8mil
MTTP50011 SMD RND 22.8mil
MTTP50012 SMD RND 22.8mil
3P3V_RADIO
R50016 49.9K 0201
R50017 49.9K 0201 DNP
BT -> USB2.0(5)
D11 USB_DMNS R50018 0 0201 USB2_BT_DN [24]
C11 USB_DPLS R50019 0 0201 USB2_BT_DP [24]
B15 WF_VBAT_IN_3V3
F7
F6
R50020 0 0201
3P3V_RADIO
1P1V_WIFI_INT_OUT
A7 VDD11
B10 VDD12_B1 C50042 0.1u 6.3V 0201 DNP GND VIO
A2
L12 3P3V_RADIO
A12
C50047 0.1u 6.3V 0201
C50041 1u 6.3V 0201
C50040 10u 6.3V 0603
A6
A9
A11
A14
B1
C14
C16
D1
E1 REF_CLK_IN
E2 REF_CLK_OUT
MTTP50013 SMD RND 22.8mil
A4
E3 SER_DAT
F5 SER_CLK
D3
D12
C13
B13
A13
1P8V_WIFI_INT_OUT
SER_CSN R50028 49.9K 0201
R50029 49.9K 0201 DNP
MTTP50014 SMD RND 22.8mil
MTTP50015 SMD RND 22.8mil
Y50001 FL4000023 3.2X2.5MM
MTTP50016 SMD RND 22.8mil
1P8V_WIFI_INT_OUT
U50003 AT24C16D-MAHM
NC Vcc
NC1 WP WF_EEP_WP
NC2 SCL SER_CLK
GND SDA SER_DAT
PAD
X912618-001
R50031 10K 0201
R50032 10K 0201
C50057 0.1u 6.3V 0201
EEPROM
P50001 SMT
GND 2,3,4
20449-001E
X864717-001
WF_RF_PATH_A_ANT
J50001 MM8030-2610RK0
PROBE
OUT IN
GND3GND4
WF_RF_PATH_COAXX
U50002 LFD182G45MJ6D431
GND1 5G_IN
ANT GND
GND3 2G_IN
RF_TR_5_A_C C50054 5.6p 0201 25V RF_TR_5_A
WIFI_RF_2_A_OUT C50055 10p 0201 50V RF_TR_2_A
DNP C50056 5.6p 0201 25V
DNP C50050 5.6p 0201
L50006 LXES15AAA1-153 X935756-001
Done: 4.7k 0402 for ESD
P50002 SMT
GND 2,3,4
20449-001E
X864717-001
WF_RF_PATH_B_ANT
J50002 MM8030-2610RK0
PROBE
OUT IN
GND3GND4
WF_RF_PATH_B
L50009 LXES15AAA1-153 X935756-001
U50004 LFD182G45MJ6D431
GND1 5G_IN
ANT GND
GND3 2G_IN
GND
C50058 5.6p 0201 25V DNP
RF_TR_5_B_C C50063 5.6p 0201 25V RF_TR_5_B
WIFI_RF_2_B_FIL_IN
3P3V_RADIO
R50030 49.9K 0201
3P3V_RADIO
R50033 0 0201
C50060 10p 50V 0201 <HDL_POWER>
U50005 BGS12SN6
VDD
RFIN RF1
CTRL RF2
GND
C50066 10p 50V 0201 WIFI_RF_2_B_FIL_IN_C
R50034 0 0201
RF_CNTL1_P_R
C50069 10p 50V 0201
RF_TR_2_B_1 C50065 10p 50V 0201 RF_TR_2_B
BRF_ANT_M15_C C50067 10p 50V 0201 BRF_ANT_M15 [50]

Title: 50. Wi-Fi_BT
Microsoft Confidential
Engineer: Surface
Size A2 | Project Name A | Rev 1.0.0.1
Date: Thursday, April 26, 2018 | Sheet 50 of 79

5	4	3	2	1

D

C

B

A

Title: **51. Empty**

Microsoft Confidential

Engineer: ***Surface***

Size	Project Name	Rev
B	**A**	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 51 of 79

Title: 52. Empty

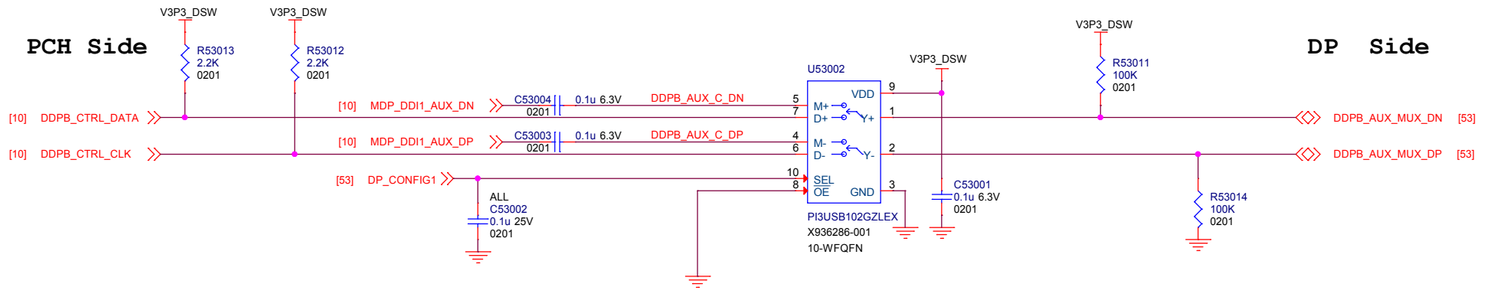
Microsoft Confidential

Engineer: Surface

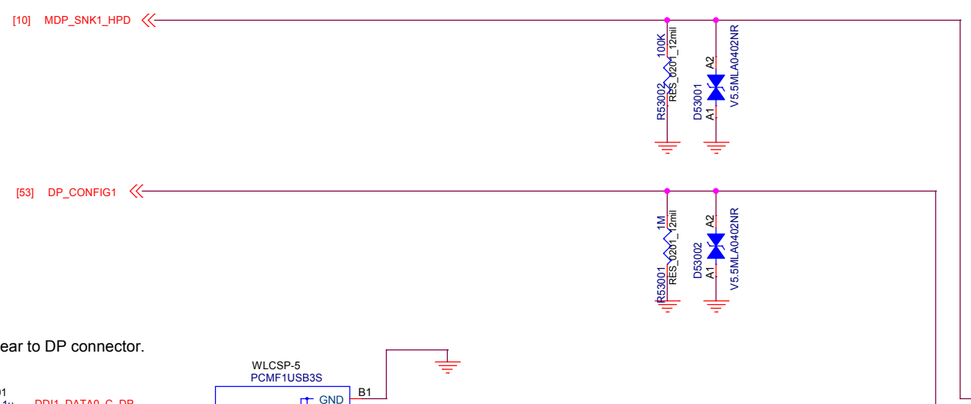
Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 52 of 79

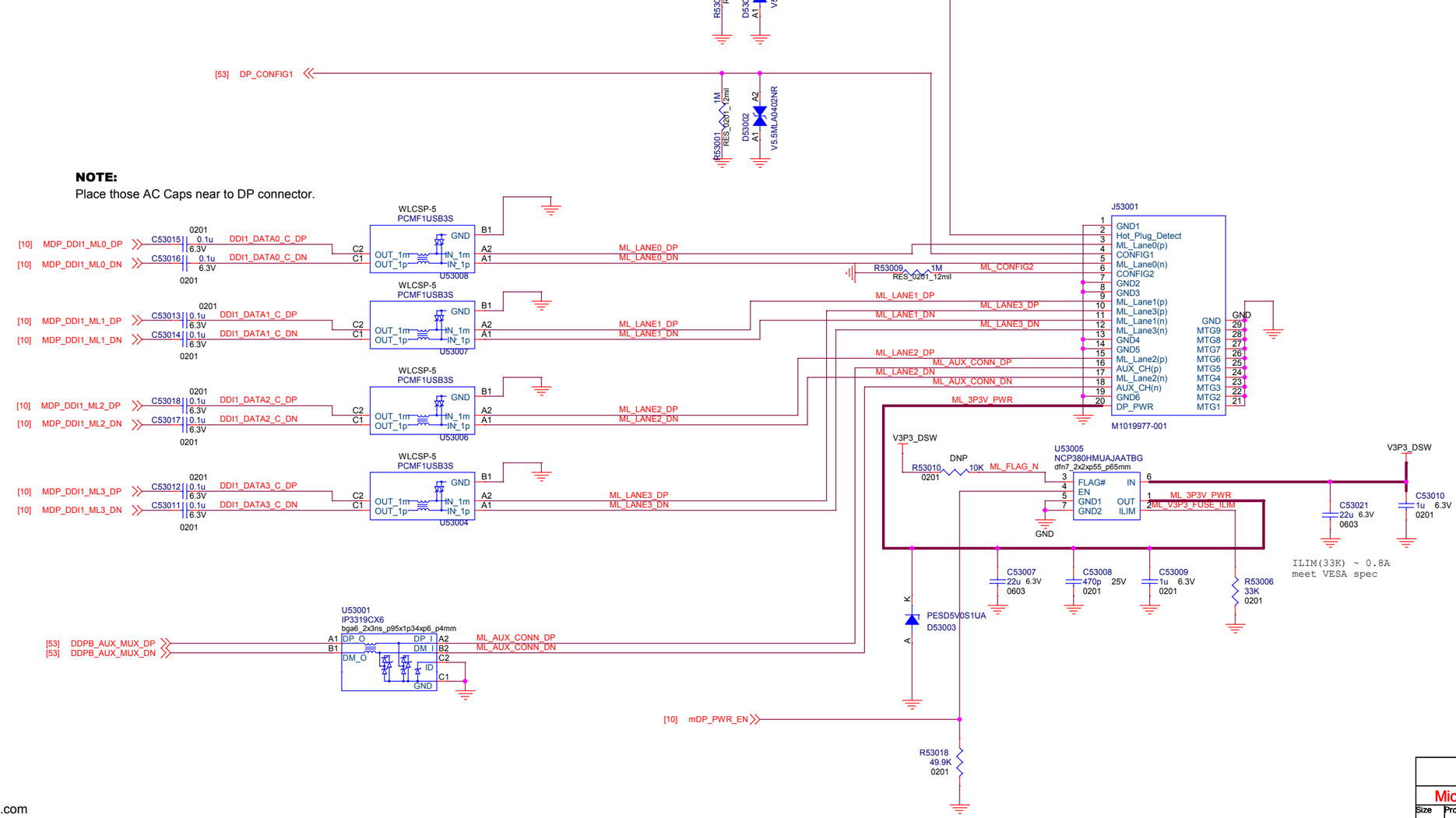
mDP mux to HDMI/DVI Dongle control



NOTE:
Place ESD Diodes close to DP connector



NOTE:
Place those AC Caps near to DP connector.



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Title: mDP			
Microsoft	Engineer: Surface		
Size: C	Project Name: A		Rev: 2.89.6
Date: Thursday, April 26, 2018		Sheet 53 of 76	

Sensor Connector to IR and RGB Cameras, Left and Right Microphones, and ALS Sensor

To IR LED on FPC through J54001

RN54001, RN54002, RN54003, RN54005 need common footprint from DFX and to be stuffed with X869109-001

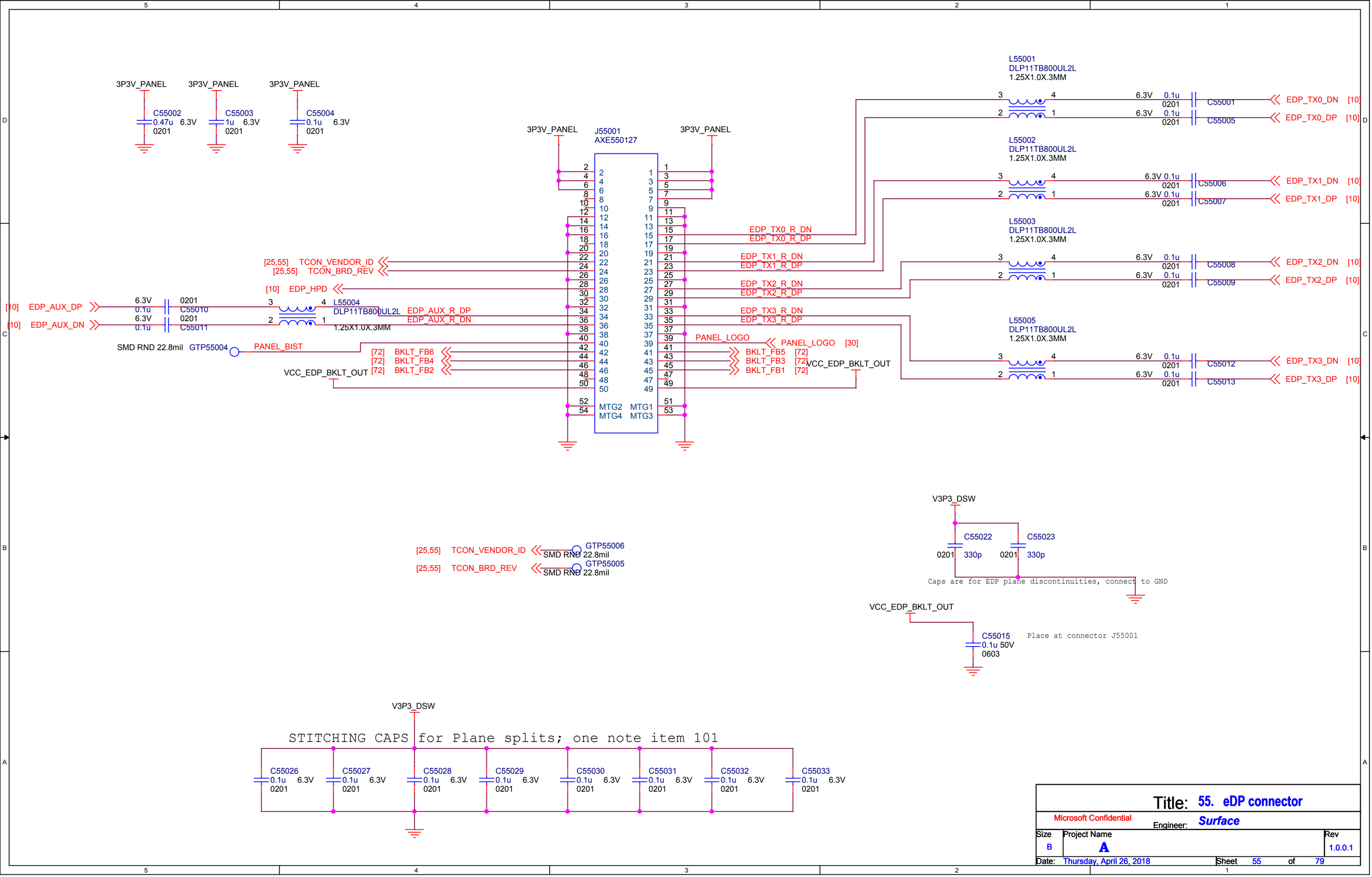
Layout Note: J54001 Pin 1 and Odd Pins along North Edge

Pullups for I2C are on the Camera Flex.

Check with Camera/RF/Power team for regulation, filtering, and component info
Power regulation, Privacy LED and sensors moved locally on sensor board. IRLED Buck regulation local to mb
Odd side of the J54001 connector faces the North edge of the PCB

ALS 7-bit I2C Address = 0x44
RGB Cam 7-bit I2C Address = 0x36
RGB EEPROM 7-bit I2C Address = TBD
IR Cam 7-bit I2C Address = 0x60

Title:	54. Camera/Sensor Conn		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 54 of 79		



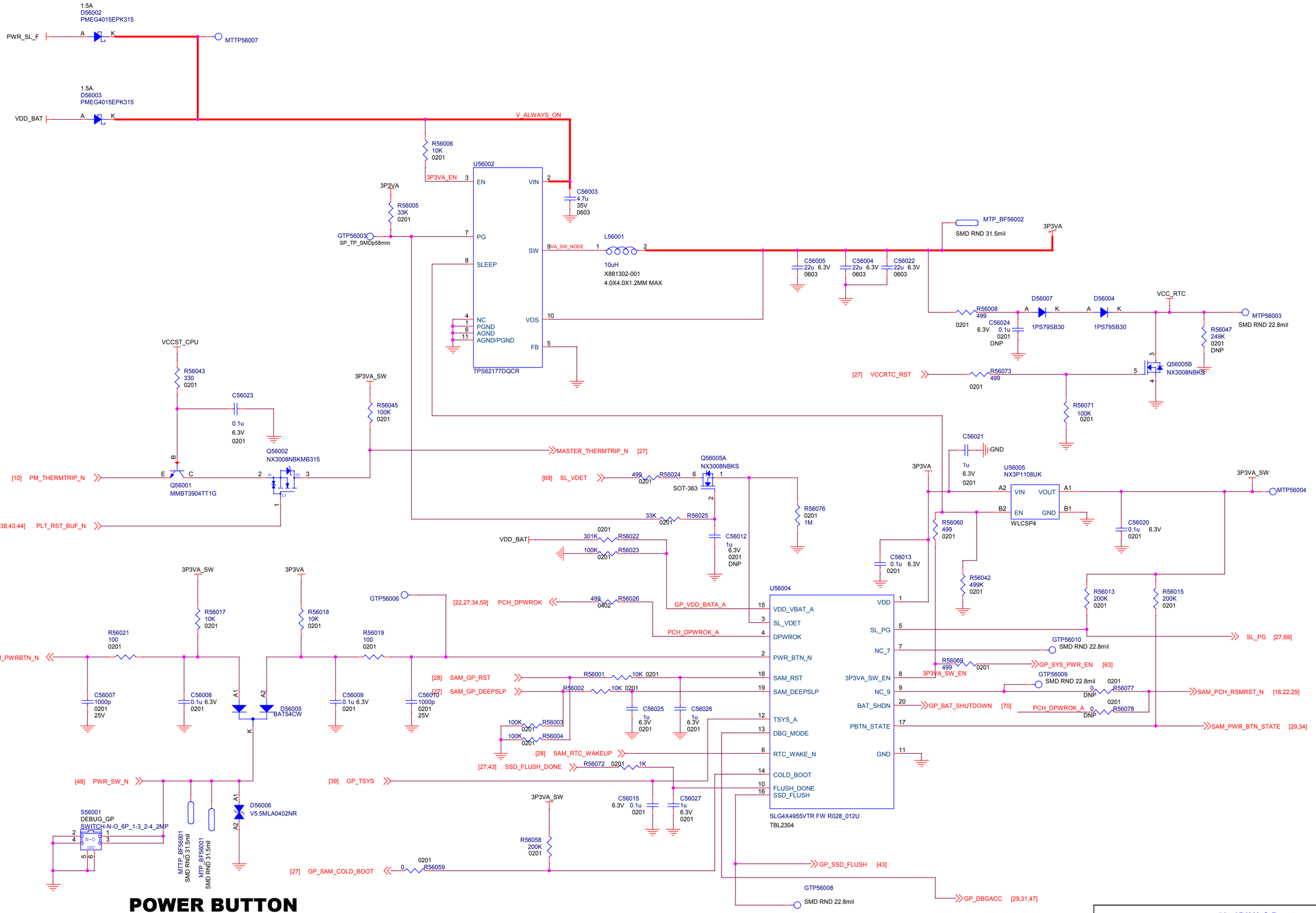
Title: 55. eDP connector

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 55 of 79



POWER BUTTON

Vinafix.com

Title:	56. 3P3VA & Reset	
Microsoft Confidential	Engineer: Surface	
Size: C	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 56 of 79	

U SPECIFIC

Title: 57. VCCEDRAM & VCCEOPIO

Microsoft Confidential

Engineer: *Surface*

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 57 of 79

U58001A

VSYS
C58006 10u 16V 0805
C58005 0.01u 25V 0201
REG5
C58002 1u 6.3V 0402
L2 PVCC4
VCCIO
Q58001 CSD87333Q3D
HG4 J1 HG4
L58002 0.47uH 4.6A 3.2x2.5x1.2mm
R58062 100K 0201
C58012 22u 6.3V 0603
C58016 22u 6.3V 0603
C58013 22u 6.3V 0603
C58017 22u 6.3V 0603
C58018 22u 6.3V 0603
IND-PWR,SM,0.47 uH,4.6 A,.025 OHM,20%,3.2X2.5X1.2MM,HEI322512A-R47M-Q8
C58007 0.1u 16V 10% 0402
R58005 0 0201
K1 SW4
BOOT4 K2 BOOT4
LG4 L1 LG4
C58164 1u 6.3V 0201
R58015 10 0201
[12] VCCIO_SENSE
M1 M2 PGND4_1 PGND4_2
VOUT4 L3 VOUT4
[12] VSSIO_SENSE
K3 SGND4

VSYS
C58026 10u 16V 0805
C58025 0.01u 25V 0201
MTP58005
V5A
Q58002 CSD87333Q3D
HG5 A8 HG5
L58004 WPN4020HR47MTJ02 4X4X2MM
0402 R58067 150
150 R58068 0402
C58032 22u 6.3V 0603
C58033 22u 6.3V 0603
C58034 22u 6.3V 0603
C58035 22u 6.3V 0603
C58036 22u 6.3V 0603
C58162 22u 6.3V 0603
C58163 22u 6.3V 0603
C58064 22u 6.3V 0603
C58065 22u 6.3V 0603
C58027 0.1u 16V 0402
R58020 10 0201
SW5 A7 SW5
BOOT5 A9 BOOT5
LG5 A6 LG5
B6 PGND5
3P3VA
Q58008B NX3008NBKS
R58069 200K 0201
Q58008A NX3008NBKS
1u 6.3V 0201 C58166
DNP
[70] V5A_VR_FB_R
R58030 0201 0
B9 VOUT5
R58073 499 0201
SKL_SLP_SUS_N [22,27,34,58,59]

VSYS
C58046 10u 16V 0805
C58045 0.01u 25V 0201
Q58006 CSD87333Q3D
HG6 J14 HG6
V3P3_VCCDSW
L58007 WPN4020HR47MTJ02 4X4X2MM
C58055 22u 6.3V 0603
C58056 22u 6.3V 0603
C58058 22u 6.3V 0603
C58060 22u 6.3V 0603
C58061 22u 6.3V 0603
C58047 0.1u 16V 0402
R58035 10 0201
SW6 K14 SW6
BOOT6 J13 BOOT6
LG6 L14 LG6
C58168 1u 0201 6.3V DNP
R58045 0 0201
[58] V3P3_DSW_VR_FB_R
M13 M14 PGND6_1 PGND6_2
VOUT6 K13 VOUT6
R58077 150 0603
3P3VA
Q58010B NX3008NBKS
R58078 200K 0201
Q58010A NX3008NBKS
R58079 499 0201
PMIC_EN [29,58,59]
R58081 0.005 0603
U58002 PI3PD22920GBEX
VIN1 VIN2 VIN3 VOUT1 VOUT2 VOUT3 ON GND
V3P3_DSW
C58059 22u 6.3V 0603
C58057 22u 6.3V 0603
R58075 10K 0201 DNP
R58076 0 0201 DNP
[22,27,34,58,59] SKL_SLP_SUS_N
R58070 150 0603 DNP
Q58009B NX3008NBKS
BD99992GW-E2
3P3VA
R58071 200K 0201
Q58009A NX3008NBKS
DNP
R58072 499 0201 DNP
SKL_SLP_SUS_N [22,27,34,58,59]
R58080 499 0201 DNP
PMIC_EN [29,58,59]
V3P3_VCCDSW
R58074 0 0201
V3P3_DSW_VR_FB_R [58]

PVCC7 F13
C58001 1u 6.3V 0402
REG5
VSYS
MTP58004
V3P3A_PCH
VIN7_1 E13
VIN7_2 E14
R58006 10 0201
C58015 0.1u 16V 0402
BOOT7 F14 BOOT7
SW7_1 D13 SW7
SW7_2 D14
L58001 1.0uH 3.6A 2.5X2.0X1.2mm
C58003 10u 25V 0603
C58004 0.01u 25V 0201
C58008 22u 6.3V 0603
C58011 22u 6.3V 0603
C58009 22u 6.3V 0603
C58010 22u 6.3V 0603
C58165 1u 6.3V 0201
DNP
R58063 200K 0201
R58010 0 0201
PGND7_1 C13
PGND7_2 C14
IND-PWR,SM,1.0 uH,3.6 A,.042 OHM,20%,2.5X2.0X1.2MM,HEI252012A-1R0M-Q8
VOUT7 F12
VOUT7
[65] 3P3V_WWAN_IN_VR_FB_R

VIN8_1 A5
VIN8_2 B5
VSYS
MTP58008
V1P8A
R58013 10 0201
C58019 0.1u 16V 0402
BOOT8 C5 BOOT8
SW8_1 A4 SW8
SW8_2 B4
L58005 1.5uH 2.7A 2.5X2.0X1.2mm
C58020 10u 25V 0603
C58021 0.01u 25V 0201
C58022 22u 6.3V 0603
C58023 22u 6.3V 0603
C58024 22u 6.3V 0603
R58064 100K 0201
PGND8_1 A3
PGND8_2 B3
IND-PWR,SM,1.5 uH,2.7 A,.065 OHM,20%,2.5X2.0X1.2MM,HEI252012A-1R5M-Q8
C58167 1u 6.3V 0201
DNP
VOUT8 C6 VOUT8
R58018 0 0201
[62] V1P8A_VR_FB_R
PVCC9 C12
REG5
C58028 1u 6.3V 0402

VIN9_1 A10
VIN9_2 B10
VSYS
MTP58010
V1P8U_2P5U
BOOT9 C11 BOOT9
R58025 10 0201
C58029 0.1u 16V 0402
SW9_1 A11 SW9
SW9_2 B11
L58003 2.2uH 2.5A 2.5X2.0X1.2mm
C58030 10u 25V 0603
C58031 0.01u 25V 0201
C58037 22u 6.3V 0603
C58038 22u 6.3V 0603
C58039 22u 6.3V 0603
C58169 1u 6.3V 0201
R58065 100K 0201
PGND9_1 A12
PGND9_2 B12
IND-PWR,SM,2.2 uH,2.5 A,.083 OHM,20%,2.5X2.0X1.2MM,HEI252012A-2R2M-Q8
VPPID D12
VOUT9 C10 VOUT9
R58029 10 0201
[16] 1P8V_DUAL_VR_FB_R

PVCC10 G2
REG5
C58041 1u 6.3V 0402
C58043 10u 0805 16V
C58044 0.01u 0201 25V
VSYS
Q58007 CSD87333Q3D
V1P2U
HG10 F1 HG10
SW10 G1 SW10
R58033 10 0201
C58042 0.1u 16V 0402
L58006 WPN4020HR47MTJ02 4X4X2MM
BOOT10 F2 BOOT10
C58048 22u 6.3V 0603
C58049 22u 6.3V 0603
C58050 22u 6.3V 0603
C58051 22u 6.3V 0603
C58052 22u 6.3V 0603
C58053 22u 6.3V 0603
C58054 22u 6.3V 0603
LG10 H1 LG10
C58170 1u 6.3V 0201
PGND10 H2
DDRID G8
VOUT10 H3 VOUT10
R58044 10 0201
[16] V1P2U_VR_FB_R
R58066 100K 0201

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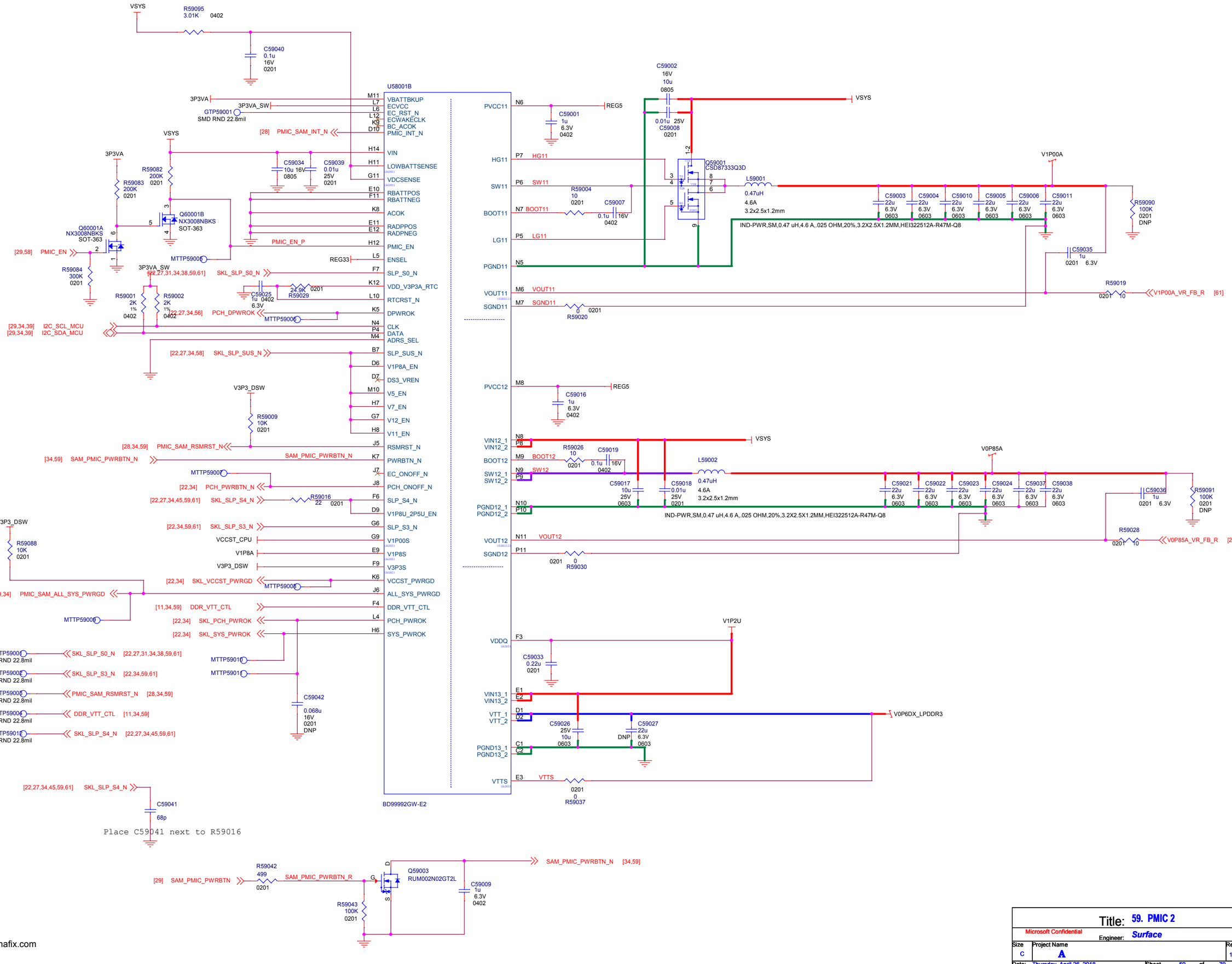
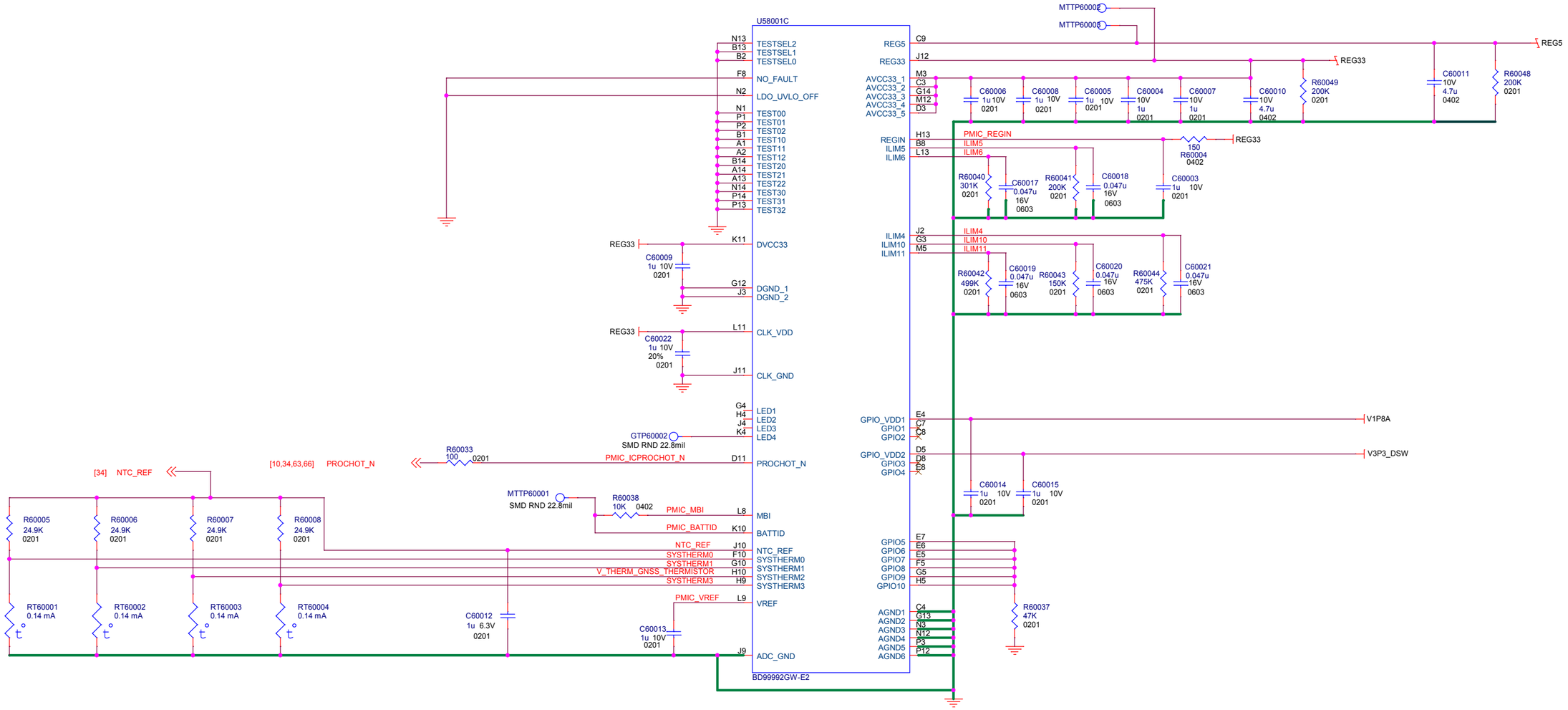
Title: 58. PMIC 1

Engineer: Surface

Size	Project Name	Rev
C	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 58 of 79


U58001B
BD99992GW-E2
VSYS
3P3VA
3P3VA_SW
V3P3_DSW
R59095 3.01K 0402
C59040 0.1u 16V 0201
GTP59001 SMD RND 22.8mil
[28] PMIC_SAM_INT_N
R59082 200K 0201
R59083 200K 0201
C59034 10u 16V 0805
C59039 0.01u 25V 0201
Q60001B NX3008NBKS SOT-363
Q60001A NX3008NBKS SOT-363
[29,58] PMIC_EN
PMIC_EN_P
MTTP59006
R59084 300K 0201
R59001 2K 1% 0402
R59002 2K 1% 0402
[22,27,34,56] PCH_DPWROK
MTTP59005
[29,34,39] I2C_SCL_MCU
[29,34,39] I2C_SDA_MCU
[22,27,31,34,38,59,61] SKL_SLP_S0_N
C59025 1u 0402 6.3V
R59029 24.9K 0201
[22,27,34,58] SKL_SLP_SUS_N
R59009 10K 0201
[28,34,59] PMIC_SAM_RSMRST_N
[34,59] SAM_PMIC_PWRBTN_N
MTTP59007
[22,34] PCH_PWRBTN_N
[22,27,34,45,59,61] SKL_SLP_S4_N
R59016 22 0201
C59041 68p
Place C59041 next to R59016
V3P3_DSW
R59088 10K 0201
[22,34,59,61] SKL_SLP_S3_N
VCCST_CPU
V1P8A
V3P3_DSW
[22,34] SKL_VCCST_PWRGD
MTTP59008
[22,29,34] PMIC_SAM_ALL_SYS_PWRGD
MTTP59009
[11,34,59] DDR_VTT_CTL
[22,34] SKL_PCH_PWROK
[22,34] SKL_SYS_PWROK
MTTP59001 SMD RND 22.8mil
MTTP59002 SMD RND 22.8mil
MTTP59003 SMD RND 22.8mil
MTTP59004 SMD RND 22.8mil
MTTP59010
MTTP59011
C59042 0.068u 16V 0201 DNP
M11 VBATTBKUP
L7 ECVCC
L6 EC_RST_N
L12 ECWAKECLK
K9 BC_ACOK
D10 PMIC_INT_N
H14 VIN
H11 LOWBATTSENSE
G11 VDCSENSE
E10 RBATTPOS
F11 RBATTNEG
K8 ACOK
E11 RADPPOS
E12 RADPNEG
H12 PMIC_EN
L5 ENSEL
F7 SLP_S0_N
K12 VDD_V3P3A_RTC
L10 RTCRST_N
K5 DPWROK
N4 CLK
P4 DATA
M4 ADRS_SEL
B7 SLP_SUS_N
D6 V1P8A_EN
D7 DS3_VREN
M10 V5_EN
H7 V7_EN
G7 V12_EN
H8 V11_EN
J5 RSMRST_N
K7 PWRBTN_N
J7 EC_ONOFF_N
J8 PCH_ONOFF_N
F6 SLP_S4_N
D9 V1P8U_2P5U_EN
G6 SLP_S3_N
G9 V1P00S
E9 V1P8S
F9 V3P3S
K6 VCCST_PWRGD
J6 ALL_SYS_PWRGD
F4 DDR_VTT_CTL
L4 PCH_PWROK
H6 SYS_PWROK
REG33
PVCC11
HG11
SW11
BOOT11
LG11
PGND11
VOUT11
SGND11
N6 REG5
C59001 1u 6.3V 0402
C59002 16V 10u 0805
0.01u 25V C59008 0201
P7 HG11
P6 SW11
N7 BOOT11
P5 LG11
N5
R59004 10 0201
C59007 0.1u 16V 0402
Q59001 CSD87333Q3D
L59001 0.47uH 4.6A 3.2x2.5x1.2mm
IND-PWR,SM,0.47 uH,4.6 A,.025 OHM,20%,3.2X2.5X1.2MM,HEI322512A-R47M-Q8
V1P00A
C59003 22u 6.3V 0603
C59004 22u 6.3V 0603
C59010 22u 6.3V 0603
C59005 22u 6.3V 0603
C59006 22u 6.3V 0603
C59011 22u 6.3V 0603
R59090 100K 0201 DNP
C59035 1u 0201 6.3V
R59019 0201 10
[61] V1P00A_VR_FB_R
M6 VOUT11
M7 SGND11
R59020 0 0201
PVCC12
VIN12_1
VIN12_2
BOOT12
SW12_1
SW12_2
PGND12_1
PGND12_2
VOUT12
SGND12
M8 REG5
C59016 1u 6.3V 0402
N8
P8
M9 BOOT12
N9 SW12
P9
N10
P10
N11 VOUT12
P11
R59026 10 0201
C59019 0.1u 16V 0402
L59002 0.47uH 4.6A 3.2x2.5x1.2mm
IND-PWR,SM,0.47 uH,4.6 A,.025 OHM,20%,3.2X2.5X1.2MM,HEI322512A-R47M-Q8
C59017 10u 25V 0603
C59018 0.01u 25V 0201
C59021 22u 6.3V 0603
C59022 22u 6.3V 0603
C59023 22u 6.3V 0603
C59024 22u 6.3V 0603
C59037 22u 6.3V 0603
C59038 22u 6.3V 0603
V0P85A
C59036 1u 0201 6.3V
R59091 100K 0201 DNP
R59028 0201 10
[26] V0P85A_VR_FB_R
R59030 0 0201
VDDQ
VIN13_1
VIN13_2
VTT_1
VTT_2
PGND13_1
PGND13_2
VTTS
F3
E1
E2
D1
D2
C1
C2
E3 VTTS
V1P2U
C59033 0.22u 0201
C59026 25V 10u 0603
C59027 DNP 22u 6.3V 0603
V0P6DX_LPDDR3
R59037 0 0201
R59042 499 0201
[29] SAM_PMIC_PWRBTN
SAM_PMIC_PWRBTN_R
Q59003 RUM002N02GT2L
R59043 100K 0201
C59009 1u 6.3V 0402
SAM_PMIC_PWRBTN_N [34,59]
Vinafix.com
Title: 59. PMIC 2
Microsoft Confidential
Engineer: Surface
Size C
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 59 of 79



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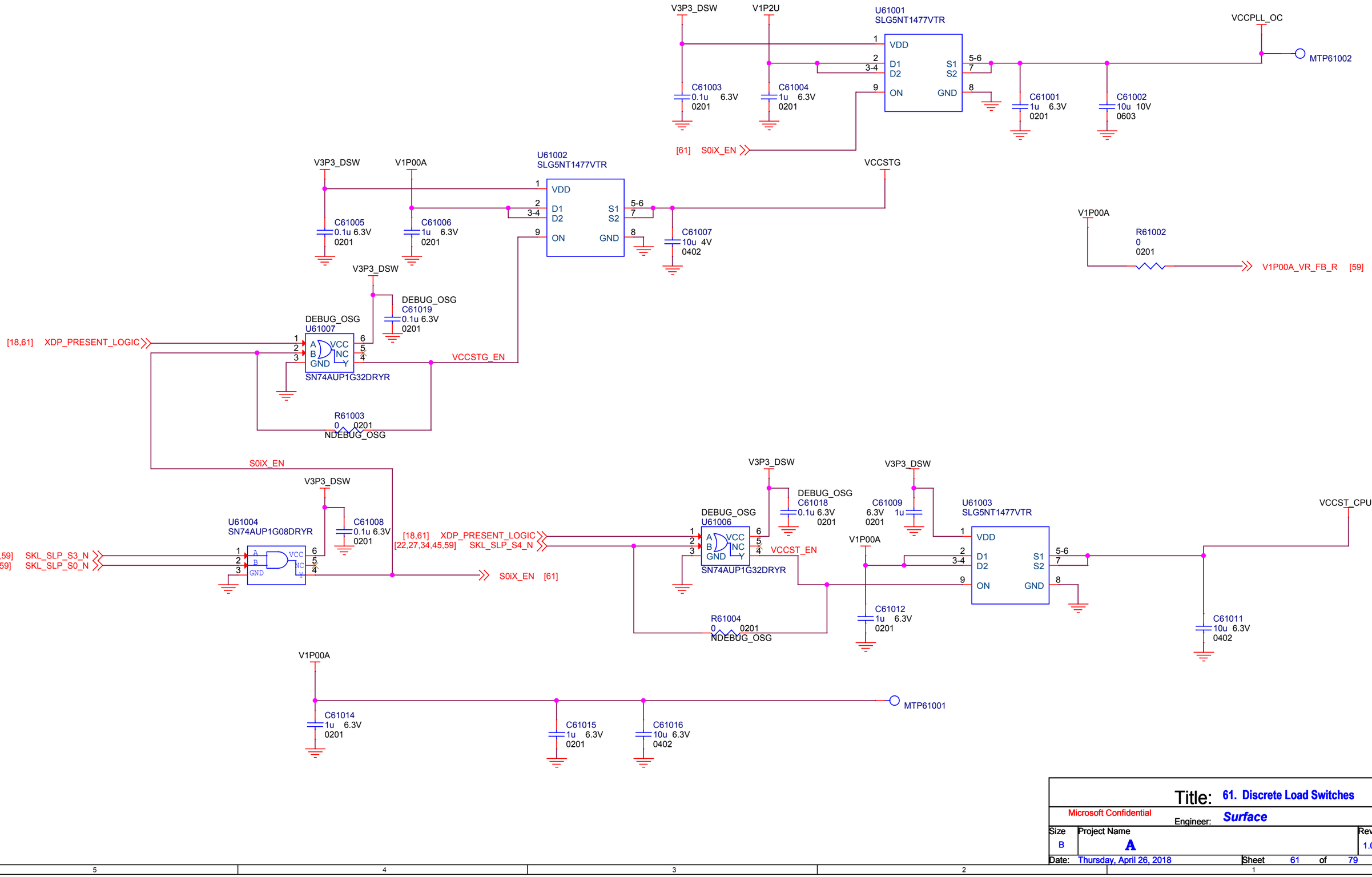
Title: 60. PMIC 3		
Microsoft Confidential	Engineer: Surface	
Size: C	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 60 of 79	



Title: 61. Discrete Load Switches

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

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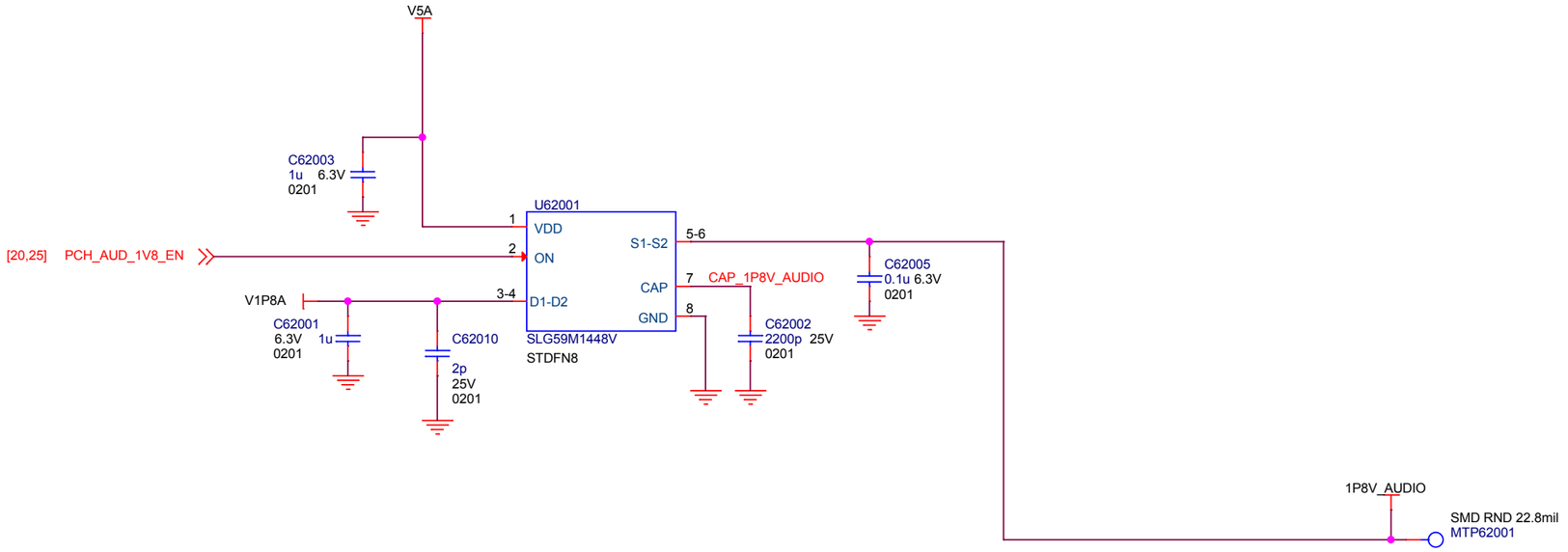
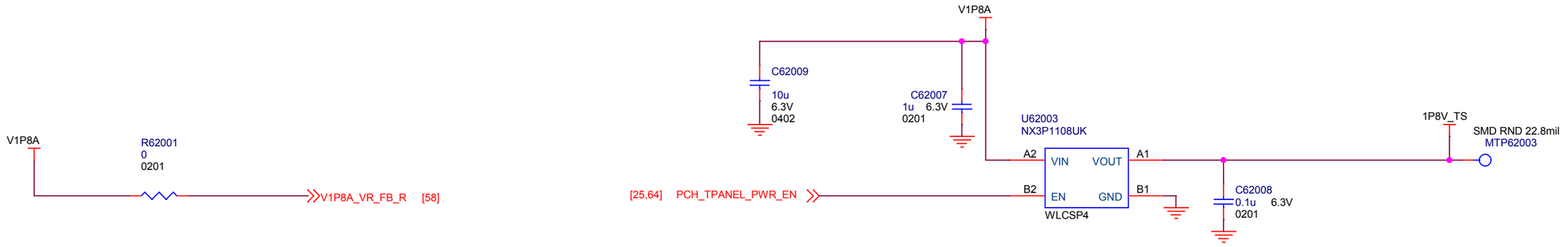


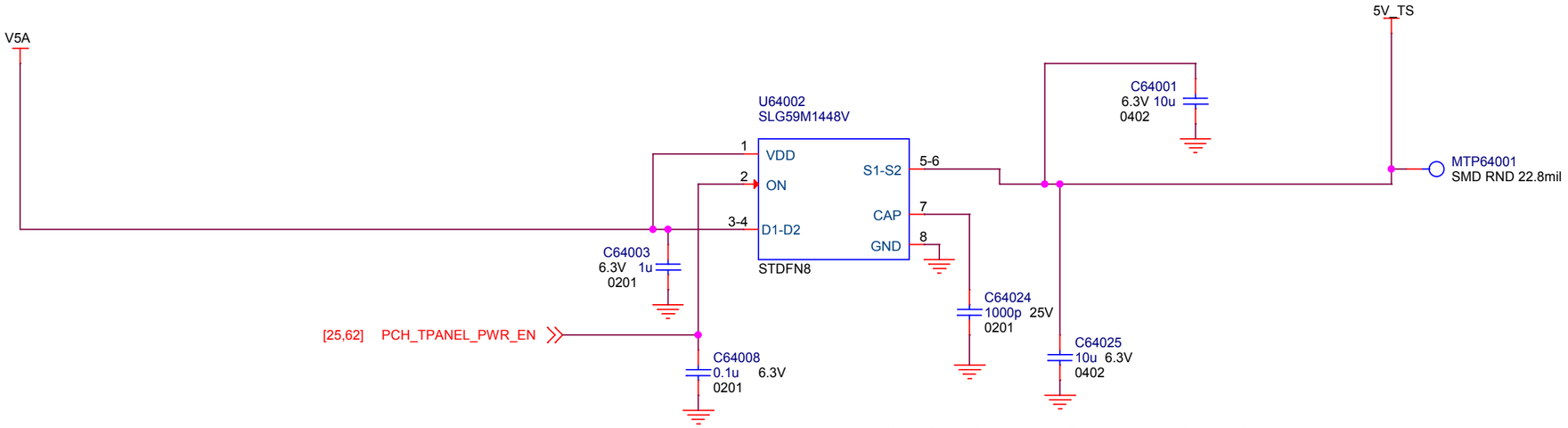


Title:	62. +1.8VSB & Load SW		
Microsoft Confidential	Engineer:	Surface	
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 62 of 79		

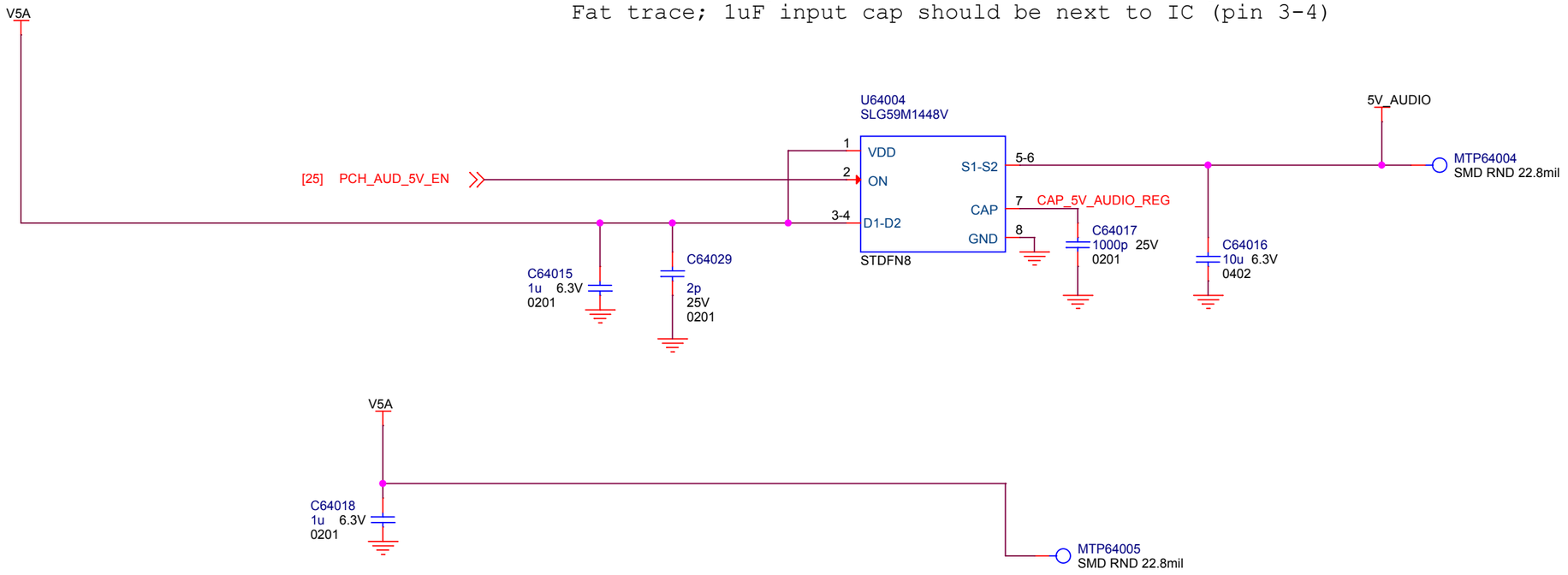
STITCHING CAPS for Plane splits
One-note item 102

PCHGR_IN
C63064 0.1u 25V 0201
C63065 0.1u 25V 0201
V3P3_DSW
VSYS
C63060 16V 0.1u 0201
C63061 16V 0.1u 0201
C63062 0.1u 25V 0201
C63063 0.1u 25V 0201
PWR_SL_F
3P3VA
R63059 100K 0201
Q63005A NX3008NBKS
[29,34] SAM_CHGR_PSU_ON
R63014 301K 0201
AON7405 Q63008
AON7405 Q63009
R63034 150K 0201
Q63005B NX3008NBKS SOT-363
D63001 BAT54CW 200mA
R63049 0603
R63022 14.7K 0201
C63019 0.1u 6.3V 0201
R63033 0 0201
R63055 0 0201
ACP
ACN
PTP63005
PTP63006
R63001 0.02 0612
R63002 1 0201
R63003 1 0201
C63001 1u 6.3V 0201
C63034 0.047u 25V 0402 DNP
C63035 0.047u 25V 0402 DNP
C63032 10u 0603
C63013 10u 0603
C63004 10u 0603
C63005 10u 0603
C63026 10u 0603
CHGR_VIN
C63003 1000p 25V 0201
C63026 0.01u 25V 0201
C63024 0.01u 25V 0201
C63025 1000p 25V 0201
C63027 10u 25V 0603
C63028 10u 25V 0603
C63009 10u 25V 0603
C63010 10u 25V 0603
C63011 10u 25V 0603
C63012 10u 25V 0603
VSYS
MTP63001
1u 25V C63033 0402
U63001
DCIN
ACIN
ADP
ASGATE
CSIP
CSIN
VDD
4.7u 6.3V C63018 0402
R63012 4.7 0402
4.7u 6.3V C63023 0402
VDDP
[10,34,60,66] PROCHOT_N
R63005 0201 100
CHG_PROCHOT_N_R
PROCHOT
3P3VA_SW
R63015 0 0201
R63031 200K 0201
[28] SAM_CHG_IMON
R63032 0201 0
VAMON = 18x(VCSIP-VCSIN); VBMON = 18x(VCSON-VCSOP)
AMON_BMON
[29] SAM_CHG_ACOK
CHG_ACOK
ACOK
[27,31,70] I2C_ROP_SCL
[27,31,70] I2C_ROP_SDA
R63017 49.9 0201
R63016 49.9 0201
CHG_SCL
CHG_SDA
SCL
SDA
[27,70] BATGONE
R63029 100K 0201 DNP
R63050 499
GP_BATGONE_R
BATGONE
133K 0201 R63020
CHG_ILIM_A
PROG
ILIM = 0.475A
0.047u 0402 C63020 25V
R63021 1K 0201
C63027 100p 25V 0201 DNP
COMP
OTG_EN_CMP_IN
OTGPG_CMP_OUT
R63056 499 0201
[27,69] SAM_SL_5V_EN
3P3VA_SW
R63060 200K 0201
R63061 499 0201
[27] SAM_SL_5V_PG
ISL9237HRZ
7-bit I2C Address = 0x12 ??
BOOT1
UGATE1
PHASE1
LGATE1
BOOT2
PHASE2
LGATE2
UGATE2
VSYS
CSOP
CSON
BGATE
VBAT
PSYS
GND_PAD
C63015 0.22u 25V 0603
R63031 0 0402
C63016 0.22u 25V 0603
R63030 0 0402
CHG_HIDRV1_D
CHG_SW1
CHG_LODRV1_D
CHG_SW2
CHG_LODRV2_D
CHG_HIDRV2_D
R63051 0 0402
CHG_SRP_A
CHG_SRN_A
CHG_BATDRV_N
R63058 0.1 0402
CHG_PMON
R63006 0 0603
R63008 7.87K 0201
PMON [66]
C63056 0.22u 0603 25V DNP
change to 7.87K based on Pyxis, and this charger is 1.44uA/W, TI charge is 1uA/W.
and MPS voltage limit is 0.8V
Q63001 CSD87334Q3D
Q63002 CSD87334Q3D
L63001 1.2uH ind_13p7x12p8x2mm
L63002 1.2uH IND_13X13X2
R63048 150 0603
R63052 150 0603
3P3VA
Q63006B NX3008NBKS
R63046 200K 0201
Q63006A NX3008NBKS
R63044 499 0201
GP_SYS_PWR_EN [56,63]
C63070 47uF 16V 1210
C63071 47uF 16V 1210
PTP63003
PTP63004
DNP 0.047u 25V C63022 0402
DNP 0.047u 25V C63021 0402
C63017 1u 6.3V 0201
R63007 1 0201
R63010 1 0201
R63009 0.01 0612
C63031 4700p 10V 0201
SON-8 CSD25402Q3A Q63003
C63029 10u 25V
C63030 10u 25V
VBAT_CHGR
R63053 100 0201
C63057 0.047u 0201 16V
Q63004 CSD25402Q3A SON-8
VBAT_CHGR [28]
VDD_BAT
R63019 100K 0201
Q63007B NX3008NBKS
Q63007A NX3008NBKS
[56,63] GP_SYS_PWR_EN
R63013 499 0201
R63028 200K 0201
R63057 5.11K 0201

Title: 63. CHARGER
Microsoft Confidential
Engineer: Surface
Size: Custom | Project Name: A | Rev: 1.0.0.1
Date: Thursday, April 26, 2018 | Sheet 63 of 79

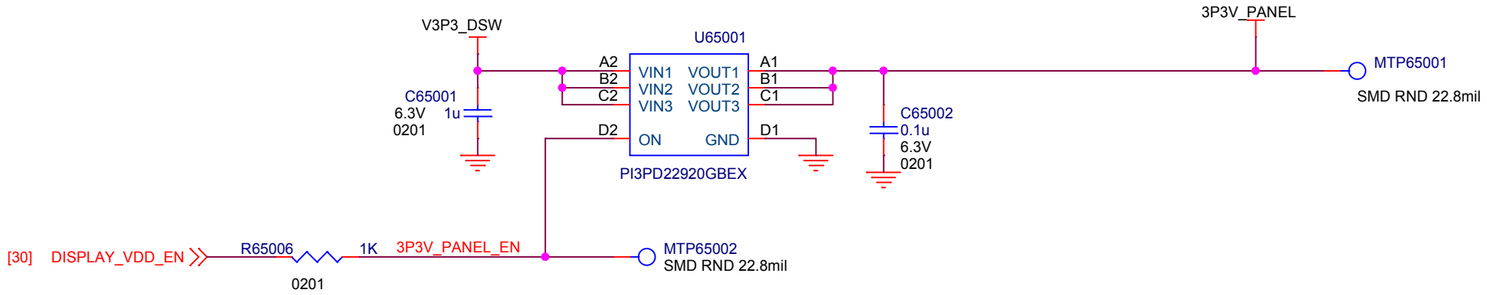


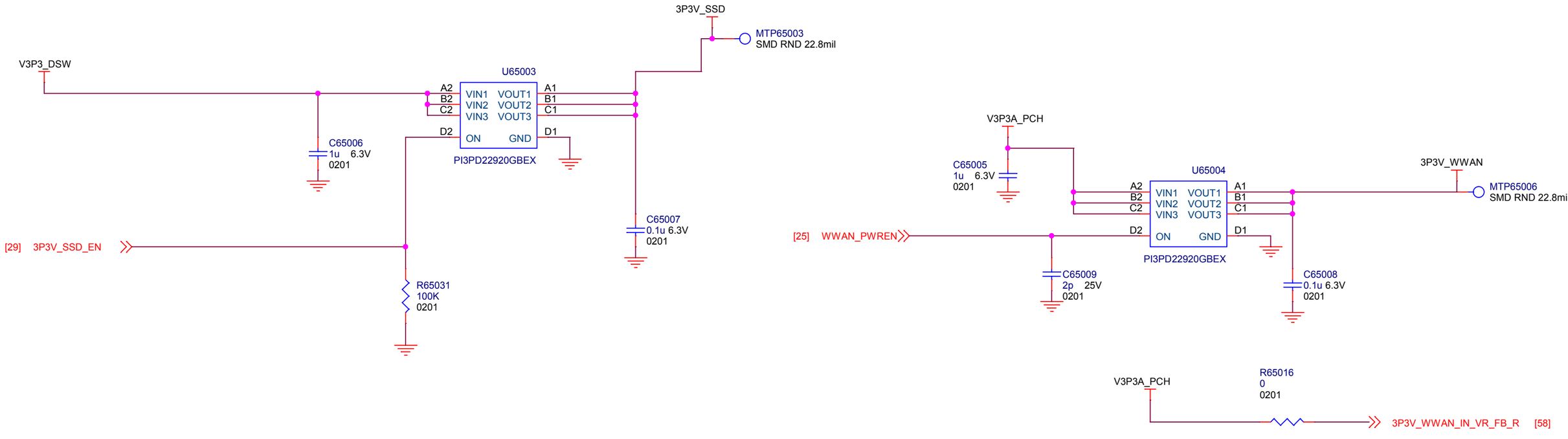
Note: connect pins 1, 3, 4 together at the chip
Fat trace; 1uF input cap should be next to IC (pin 3-4)



U SPECIFIC

Title: 64. +5V Load SW			
Microsoft Confidential	Engineer: Surface		
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 64 of 79		





Title: 65. +3P3V Load SW		
Microsoft Confidential	Engineer: Surface	
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 65 of 79	

Scale to 0.80V for Psys Max.

Check Psys Settings

Should these be pull up to 3V3? VCCST?

EV2.5 18 Oct 2016

IMVP8 PROG

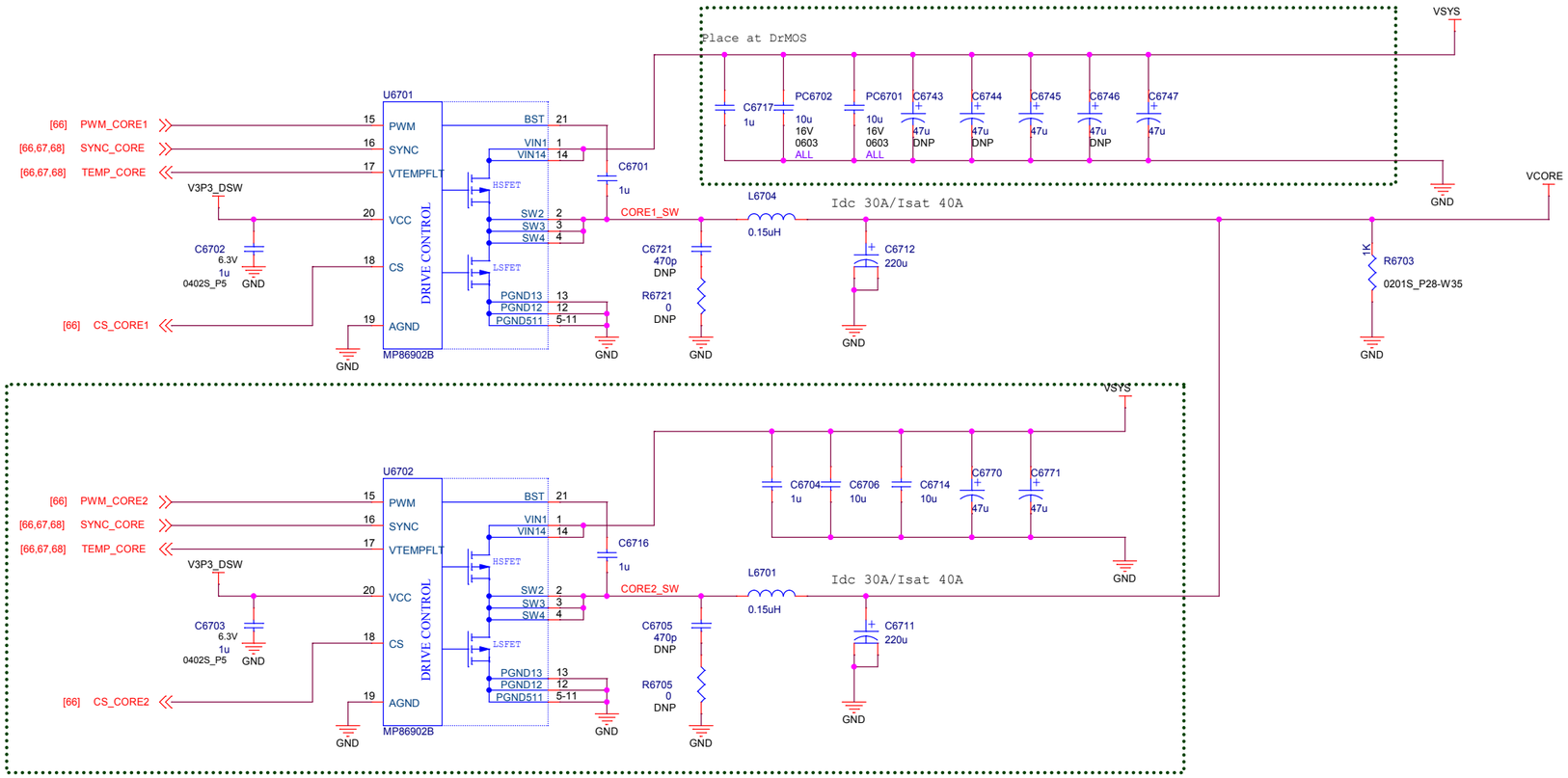
U6601 MP2949A-003F-C555

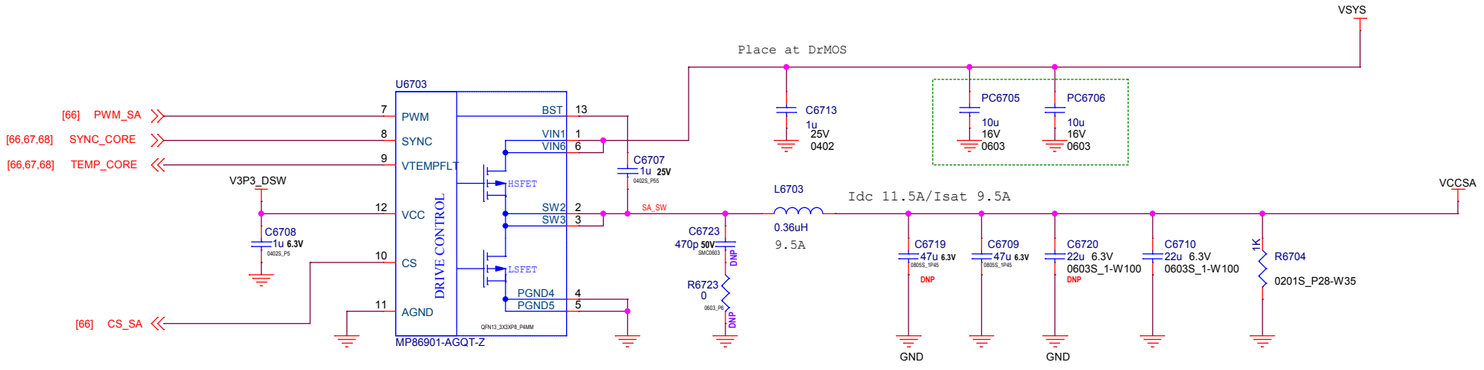
U SPECIFIC

Vinafix.com

Title:	66. VCPU Controller
Microsoft Confidential	Engineer: Surface
Size: C	Project Name: A
Rev:	1.0.0.1
Date:	Tuesday, May 01, 2018
Sheet	66 of 79

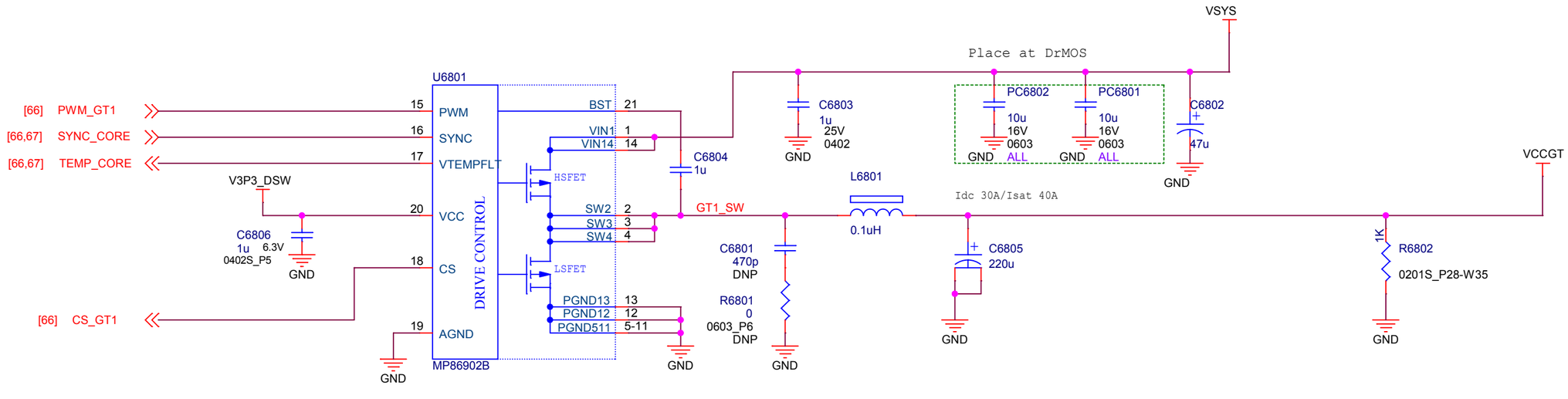
9V to 12V





Vinafix.com

Title: 67. VCORE VCCSA		
Microsoft Confidential	Engineer: Surface	
Size: C	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 67 of 79	



U SPECIFIC

Microsoft Confidential

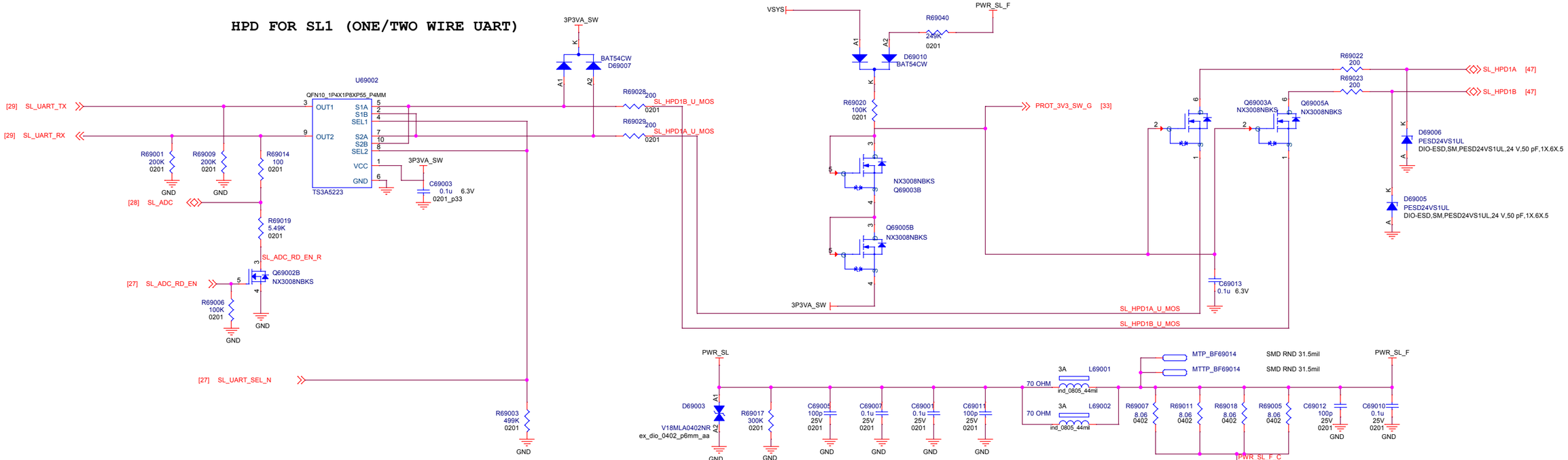
Title: 68. VCCGT

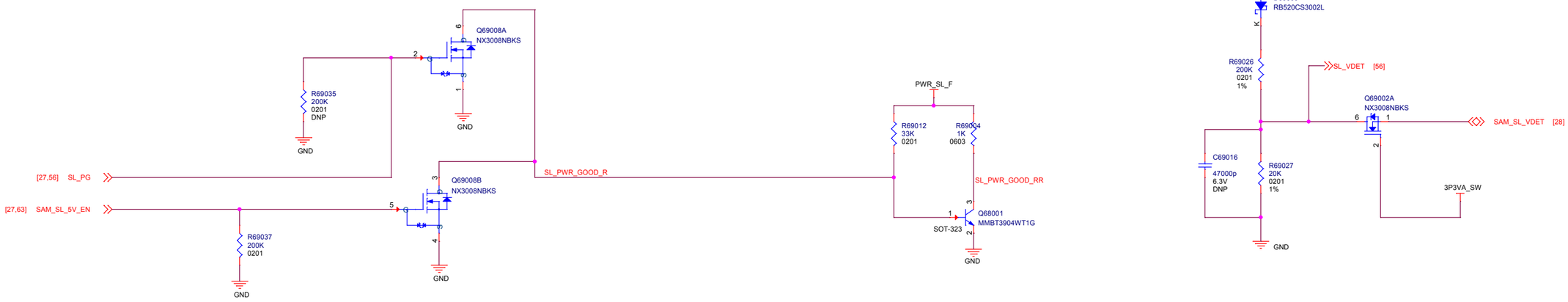
Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 68 of 79

HPD FOR SL1 (ONE/TWO WIRE UART)





SL1 port discharger
limit PSU anti-arc pulse voltage

Title: 69. SF1 POWER			
Microsoft Confidential	Engineer: Surface		
Size: A2	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 69 of 79		

Battery Connector

MTTP_BF70015 SMD RND 31.5mil
MTP_BF70015 SMD RND 31.5mil

V5A
R70040 0 0201
V5A_VR_FB_R [58]

VDD_BAT

R70042 100K 0201

J70003 2287111-2
J70001 X950860-001
J70002 2287111-2

BAT_SHUTDOWN_N
[70] BATT_I2C_DATA
[70] BATT_I2C_CLK

[56] GP_BAT_SHUTDOWN
R70043 100 0201
R70041 100K 0201
Q70007 RUM002N02GT2L
3P3VA_SW
R70070 200K 0201
MTP70008 SMD RND 22.8mil
[27,63] BATGONE
MTP70007 SMD RND 22.8mil
MTP70005 SMD RND 22.8mil
MTP70006 SMD RND 22.8mil
TP70005 SMD SQ 29.5mil ***WHEN SHORTED BATTERY TURNS OFF***

Place TP's 0.2 inch apart,
Place on component side, near battery.
Must be accessible when battery is installed

J70003 to be place North of J70001
North of Board Edge

Board Edge

NOTE: 1.7A/pin

C70015 0.1u 10V 0201

MTP_BF70001 SMD RND 31.5mil
MTP_BF70002 SMD RND 31.5mil
MTP_BF70003 SMD RND 31.5mil
MTP_BF70004 SMD RND 31.5mil
MTP_BF70005 SMD RND 31.5mil
MTP_BF70006 SMD RND 31.5mil
MTP_BF70007 SMD RND 31.5mil
MTP_BF70008 SMD RND 31.5mil
MTP_BF70009 SMD RND 31.5mil
MTP_BF70010 SMD RND 31.5mil
MTP_BF70011 SMD RND 31.5mil
MTP_BF70012 SMD RND 31.5mil

[27,31,63] I2C_ROP_SCL
[27,31,63] I2C_ROP_SDA

L70001 0 0402
DNP C70016 100p 16V 0201
BATT_I2C_CLK [70]
MTP70003 SMD RND 22.8mil

L70002 0 0402
DNP C70017 100p 16V 0201
BATT_I2C_DATA [70]
MTP70004 SMD RND 22.8mil

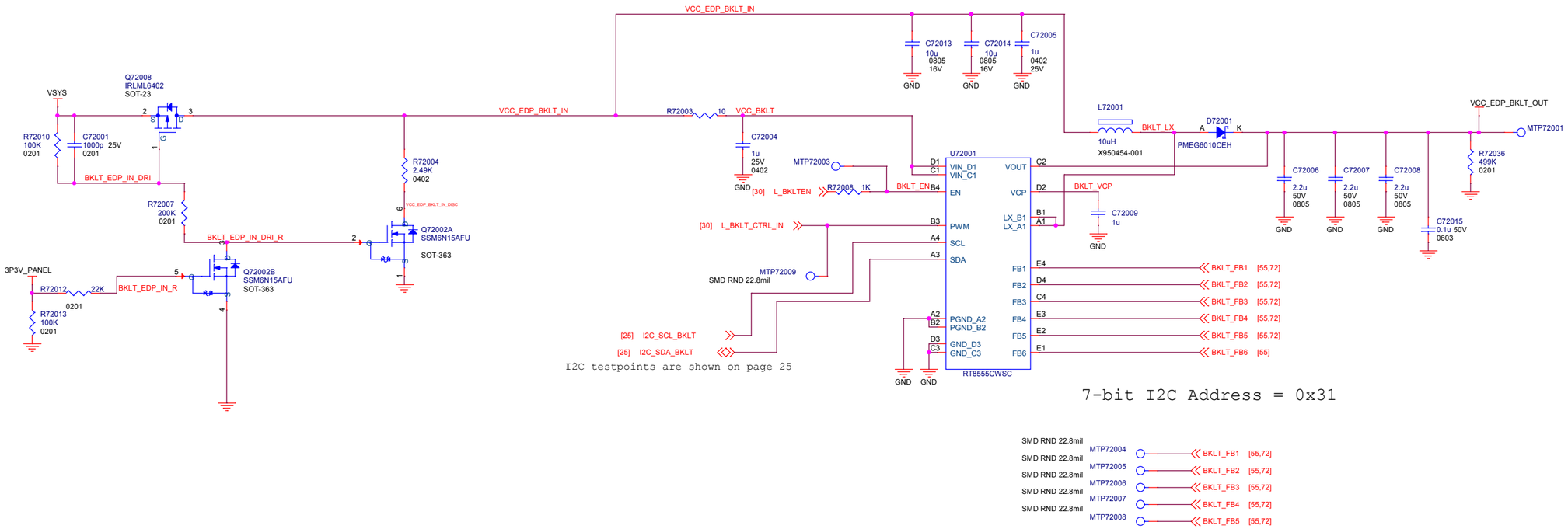
Microsoft Confidential

Title: 70. BATT CONN, power input
Engineer: Surface

Size	Project Name	Rev
A2	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 70 of 79

Title:	71. Empty				
Microsoft Confidential	Engineer:	Surface			
Size	Project Name				Rev
B	A				1.0.0.1
Date:	Thursday, April 26, 2018		Sheet	71 of	79



I2C testpoints are shown on page 25

7-bit I2C Address = 0x31

SMD RND 22.8mil
MTP72004 BKLT_FB1 [55,72]
SMD RND 22.8mil
MTP72005 BKLT_FB2 [55,72]
SMD RND 22.8mil
MTP72006 BKLT_FB3 [55,72]
SMD RND 22.8mil
MTP72007 BKLT_FB4 [55,72]
SMD RND 22.8mil
MTP72008 BKLT_FB5 [55,72]

isolated ground on layer 2 to tie Cin GND, Cout GND, and controller PGND together. Then tie this isolated ground plane to main GND under the exposed pads.

Title:	72. Backlight Controller		
Microsoft Confidential	Engineer:	Surface	
Size: A2	Project Name: A		Rev: 1.0.0.1
Date: Tuesday, May 01, 2018	Sheet 72 of 79		

5	4	3	2	1

D

C

B

A

Title: 73. Empty

Microsoft Confidential

Engineer:

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 73 of XX

5 4 3 2 1

Title: 74. Empty

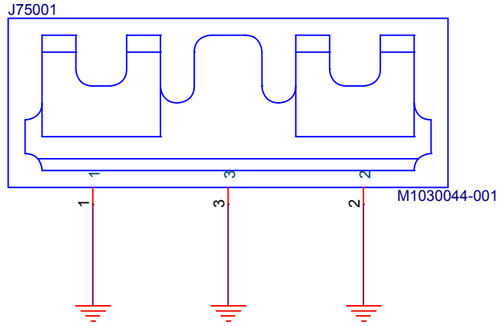
Microsoft Confidential

Engineer:

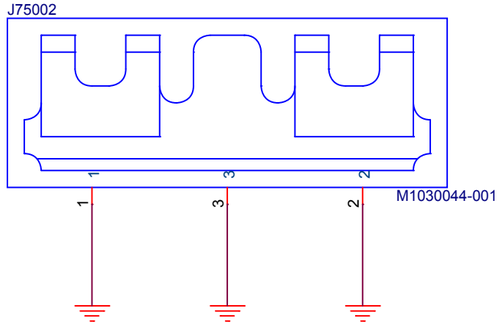
Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 74 of XX

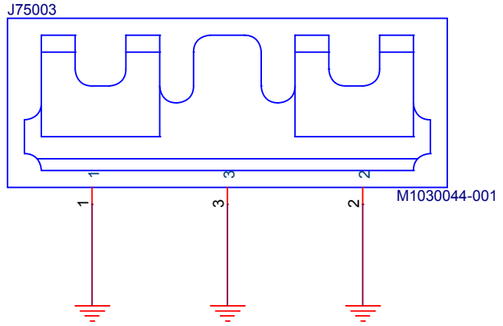
J75001



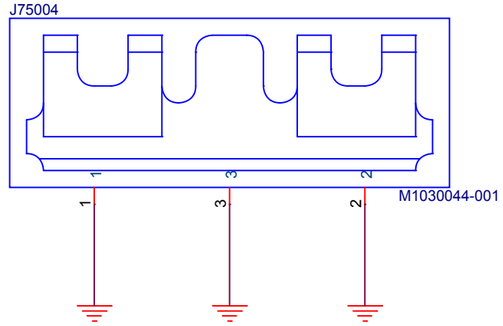
J75002



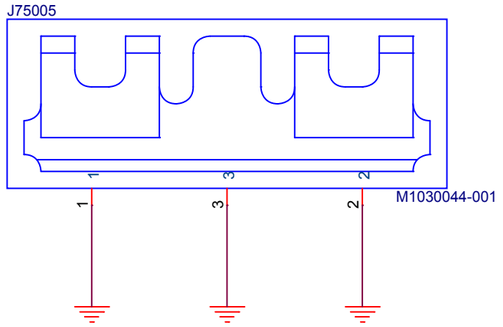
J75003



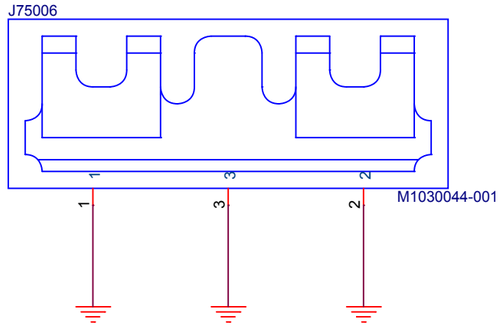
J75004



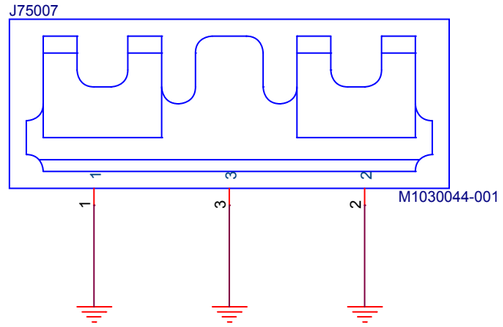
J75005



J75006



J75007



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Microsoft Confidential

Title: 75. Clips		
Engineer: *Surface*		
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 75 of 79	

BOTTOM SIDE spacers

MP76021 M1009352-002
MP76023 M1009352-002
MP76027 M1009352-002
MP76029 M1009352-002
MP76031 M1009352-002
MP76035 M1009352-002
MP76024 M1009352-002
MP76025 M1009352-002
MP76026 M1009352-002
MP76028 M1009352-002
MP76030 M1009352-002
MP76036 M1009352-002
MP76034 M1009352-002

VCCGT

TOP SIDE spacers

MP76033 M1012486-001
MP76032 M1012486-001
MP76037 M1012486-001
MP76038 M1012486-001

TOP SIDE spacers

MP76040 M1012486-001
MP76041 M1012486-001

MTP_BF76004 SMD RND 31.5mil
MTP_BF76005 SMD RND 31.5mil
MTP_BF76006 SMD RND 31.5mil
MTTP_BF76004 SMD RND 31.5mil
MTTP_BF76005 SMD RND 31.5mil
MTTP_BF76006 SMD RND 31.5mil

V0P85A — MTP76001 SMD RND 22.8mil
VCCGT — MTP76003 SMD RND 22.8mil
VCCSA — MTP76004 SMD RND 22.8mil
VCCIO — MTP76005 SMD RND 22.8mil
VCCST_CPU — MTP76006 SMD RND 22.8mil
VCCSTG — MTP76007 SMD RND 22.8mil

H76002 NO-MSPN-157
H76001 NO-MSPN-157

V1P2U — MTP76010 SMD RND 22.8mil
V0P6DX_LPDDR3 — MTP76011 SMD RND 22.8mil
VCORE — MTP76012 SMD RND 22.8mil

COAX Clips

MP76013 FCAU137A02C5PC X943446-001
MP76014 FCAU137A02C5PC X943446-001
MP76015 FCAU137A02C5PC X943446-001
MP76016 FCAU137A02C5PC X943446-001
MP76017 FCAU137A02C5PC X943446-001

PEMNUT for SoCs

MP76002 M1019199-001
MP76003 M1019199-001
MP76004 M1019199-001
MP76005 M1019199-001

PEMNUT for XDP

MP76042 M1019383-001

Shield Fences

SOC/SSD

SHT76001 M1016647-001 ZID = 00 ZOD = 00
SHT76002 X949514-001 ZID = 00 ZOD = 00 — PMIC
SHT76003 X949515-001 ZID = 00 ZOD = 00 — Charger
SHT76004 M1016649-001 ZID = 00 ZOD = 00 — Audio
SHT76005 X949517-001 ZID = 00 ZOD = 00 — Backlight/USB
SHT76006 M1016651-001 ZID = 00 ZOD = 00 — G5/Touch
SHT76007 M1016652-001 ZID = 00 ZOD = 00 — Display/Camera
SHT76008 X949521-001 ZID = 00 ZOD = 00 — Wi-Fi
SHT76009 M1013613-001 ZID = 00 ZOD = 00 — Trackpad
SHT76010 X949524-001 ZID = 00 ZOD = 00 — Surflink
SHB76003 M1016654-001 ZID = 00 ZOD = 00 — Touch

2.3mm NPTH

H76022 NO-MSPN-00212

2.5mm NPTH

H76010 H76011 H76012 H76013 H76014 NO-MSPN-159
H76016 H76017 H76018 H76019 H76020 NO-MSPN-159

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Title:	76. TP's and Mech		
Microsoft Confidential	Engineer:	Surface	
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 76 of 79		