INTEL SYSTEM DIAGRAM

01

+3V/+5V S5 PG.39
+1.05V/+1.5V PG.40/45
CPU Core PG.42~43
DDR4 PG.41
Charge PG.38
VGA POWER PG.46~47
VCCGT/VCCSA PG.44

SODIMM1 Max. 16GB STD PG.17 — 2400MT/s DDR4 L Channel A
SODIMM2 Max. 16GB STD PG.18 — 2400MT/s DDR4 L Channel B

INTEL SkyLake-H
Processor : Daul / Quad Core
Power : 45 (Watt)
Package : BGA1400
Size : 42 x 28 (mm)
PG.2~8

PEG → GPU N16P-GT P19~P23 — X'TAL 27MHz
GPU → VRAM DDR3 P24~P27

eDP (5.4Gb/s) → eDP Conn. P29
DDI2 → ITE6515 P28 → VGA Conn. P29
DDI1 → PS8407 P30 → HDMI Conn. P30

DMI

HDD PG.33 — SATA2 6GB/s

INTEL PCH
Lynx Point
Power : Watt
Package : FCBGA837
Size : 23 x 23 (mm)
PG.9~15

PCI-E x 1
Port4 — LAN RTL8111GSH 10/100/1000 PG.31
Port3 — WLAN BT COMBO PG.34 — USB 2.0 PORT7

PCI-E x 4
NGFF SSD PG.34 — SATA0~1 6GB/s

USB3-1 & USB3-2
USB 3.0 PORT1,2 — USB3.0 Ports X2 PG.36
USB 2.0 PORT1,2 — Webcam PG.29 PORT9
USB 2.0 PORT10 — Card Reader PG.36
USB 2.0 PORT5 — DB IO Port PG.36
USB 2.0 PORT8 — Touch Screen PG.29

KBC ITE IT8987E/BX PG.37 — LPC
LPC Interface
TPM NPCT650 PAGE 33
KB PG.35
TP PG.35
ROM PG.12
FAN PG.35

SLG3NB3454 GreenCLK PAGE 33 — 25MHz

G- Sensor P35

AUDIO CODEC ALC255 PG.32 — Azalia
Universal HP P32
Speaker PAGE 32
Dual Digital MIC PAGE 32

PROJECT :ZRY
Quanta Computer Inc.

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SKYLAKE Processor (CLK,MISC,JTAC)

02

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

HPECI Ra,Ca need placement close to EC.

PROCHOT# (50ohm)
Trace Length <11 inches

Cb need placment near VR

Change net name_20141203

PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches

CPU RESET#

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches

Rb need placment near PCH

New CN to PCH pin Y44_20141203

R14 need change to 20ohm

Processor pull-up (CPU)

B2A
S0->S5 & S0->S3
Power of sequence 1us
SUSB# -> VCCST_PWRGD

CPU XDP

CPU CORE SVID

Layout note: need routing together and ALERT need between CLK and DATA.

CLOSE TO CPU
PLACE THE PU RESISTORS

SVID ALERT

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS

SVID DATA

HWPD VCCST PWRGD CRB is via +1.05V PG

Shortpad change
to 60.4 ohm. 11/6

CPU thermal trip

CPU VDDQ
Del R2574_20141217

Placement close to CPU.

Note: please keep plane is enough for VDDQ 2.8A

PROJECT :ZRY Quanta Computer Inc.			
Size Custom	Document Number 02 -- SKYPAKE 1/20(eDP/DDI)		Rev 1A
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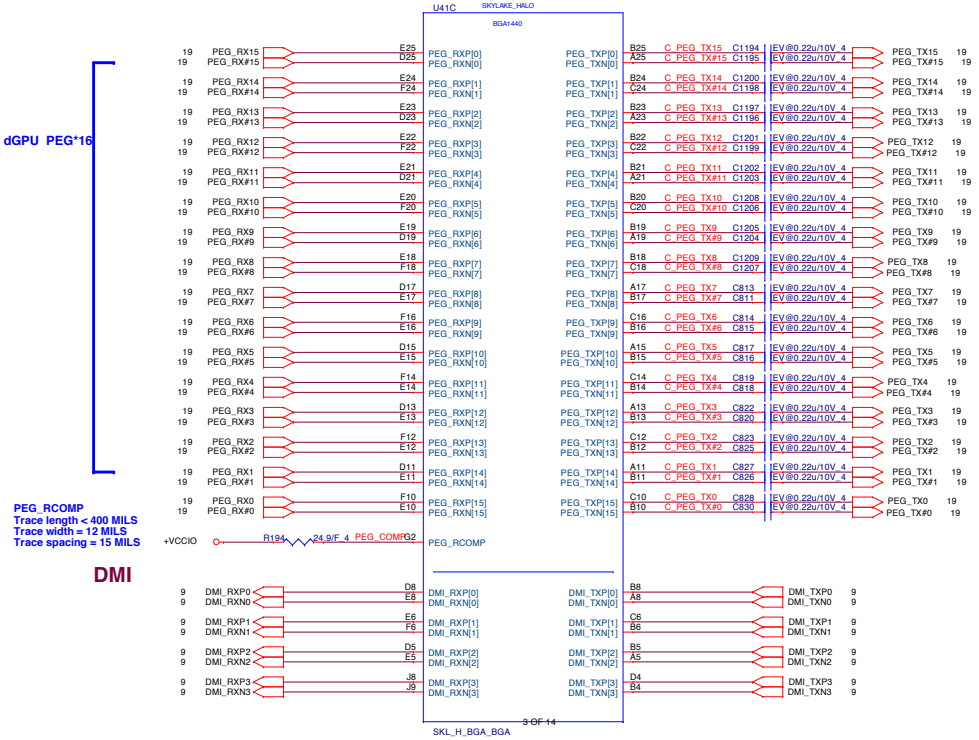
SKYLAKE Processor (DMI,PEG,FDI)

Lane Reversed

dGPU PEG*16



Lane Reversed

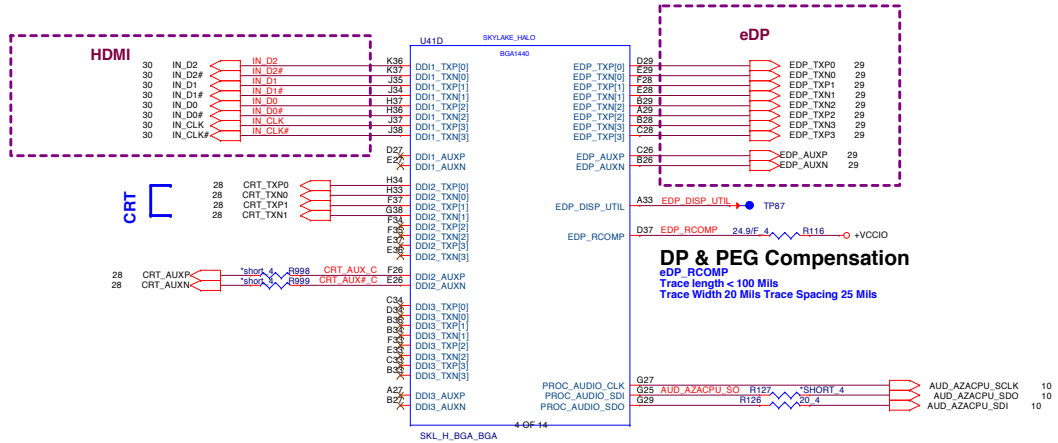
PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

DMI

HDMI

CRT

eDP



DP & PEG Compensation

eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

+VCCIO 6,16,38,40,42,45

+1.0V 2,5,6,10,16,40,45

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Custom	SNB 1/5 (PCIE&DMI&FDI)	1A
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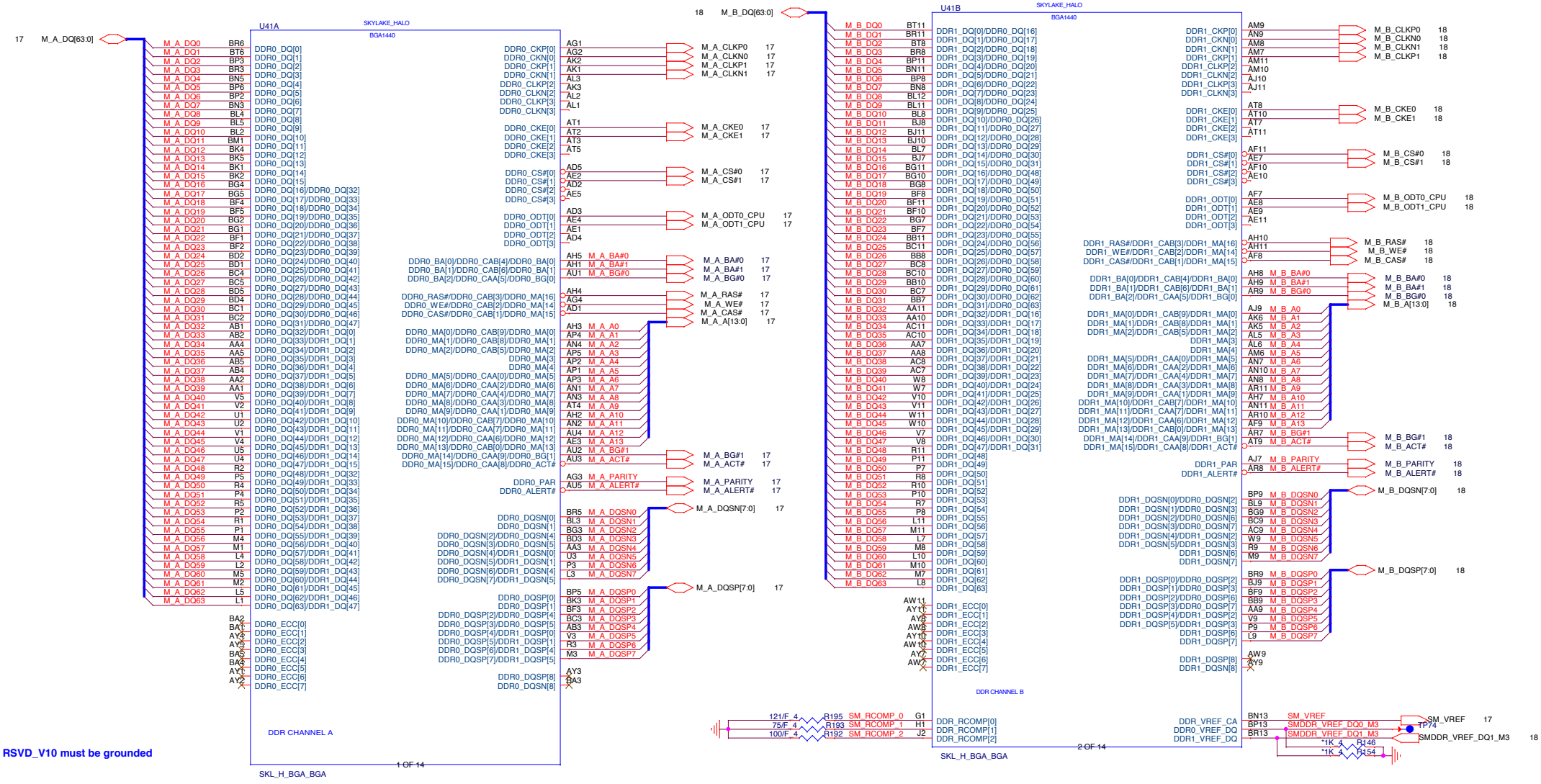
SKYLAKE Processor (DDR3)



RSVD_V10 must be grounded

PROJECT :ZRY Quanta Computer Inc.		
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SKYLAKE Processor (POWER)

05

+1.5V 14,30,32,34,45

+1.2VSUS 2,6,10,17,18,41

Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)

Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

Follow SKL H DG page 574 to place Cap 22uF x 14, 10uF x 35, 1uF x 68

7,42,44 +VCCGT

U41N SKYLAKE_HALO BGA1440

SKL_H_BGA_BGA

14 OF 14

4+4e, Support eDRAM Only, GTX 12A

Need caps...

IO Thrm Protect

+3VPCU

R215 *16.5K/F_4 THRM_MOINTOR

C453 *0.1U/16V_4

R231 *3.3K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 37

R241 *100K_4 NTC

C468 *0.1U/16V_4

+VCCGT

R550 *100/F_4

R549 *100/F_4

TP86 TP85

VCCGT_SENSE 42

VCCGTSS_SENSE 42

VCCGT_SENSE VSSGTX_SENSE VSSGT_SENSE VCCGTX_SENSE

VCC Output Decoupling Recommendations

Local CPU Thermal Sensor

U40 *TMP431ADGKR

10,16,17,18,35 SMB_RUN_CLK

10,16,17,18,35 SMB_RUN_DAT

CPU_THRMTRIP#

R555 10K/F_4 +3V

C806 0.01U/50V_4 +3V

CPU_THERMDA

C809 2200P/50V_4

CPU_THERMDC

Q39 *METR3904-G

CPU Thermal Sensor

AL000431014 TMP431ADGKR(98h)

+1.0V *4.7K_4 R562

Q38 *METR3904-G

2,11,17,18 PM_THRMTRIP#

CPU_THRMTRIP#

PROJECT :ZRY

Quanta Computer Inc.

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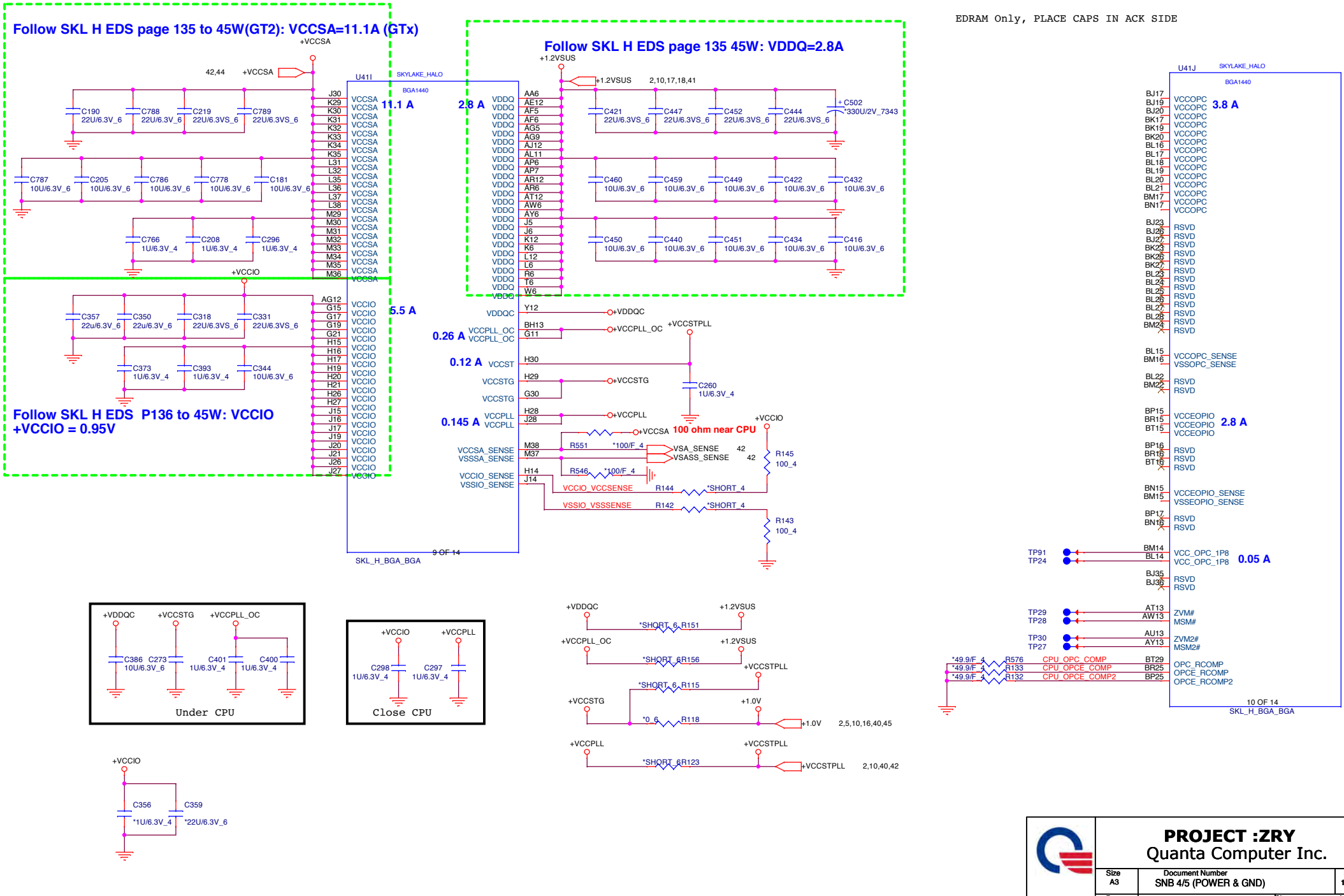
06

EDRAM Only, PLACE CAPS IN ACK SIDE

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A (GTx)

Follow SKL H EDS page 135 45W: VDDQ=2.8A

Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V



Size	A3
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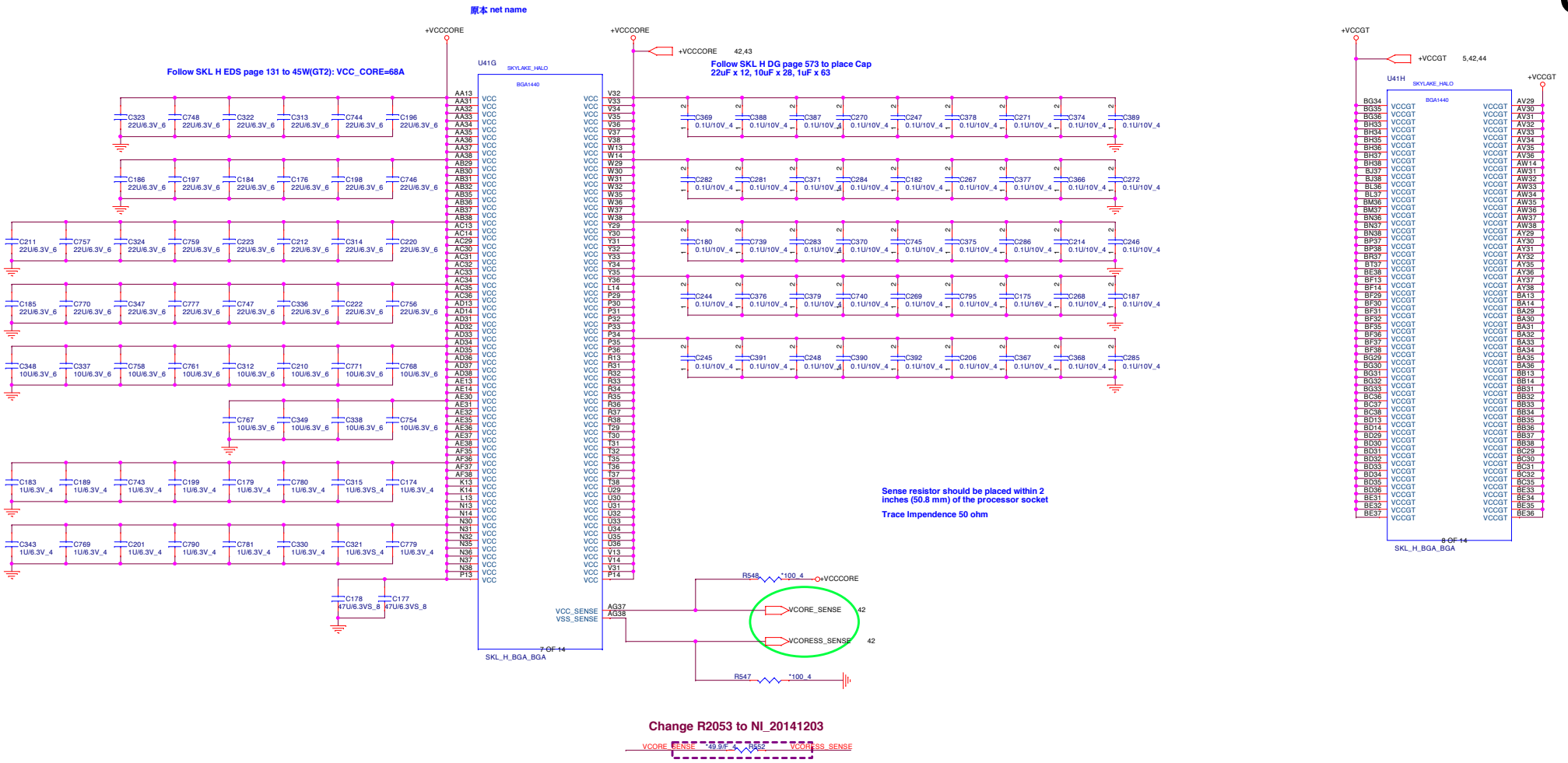
PROJECT :ZRY
Quanta Computer Inc.



PROJECT :ZRY Quanta Computer Inc.		
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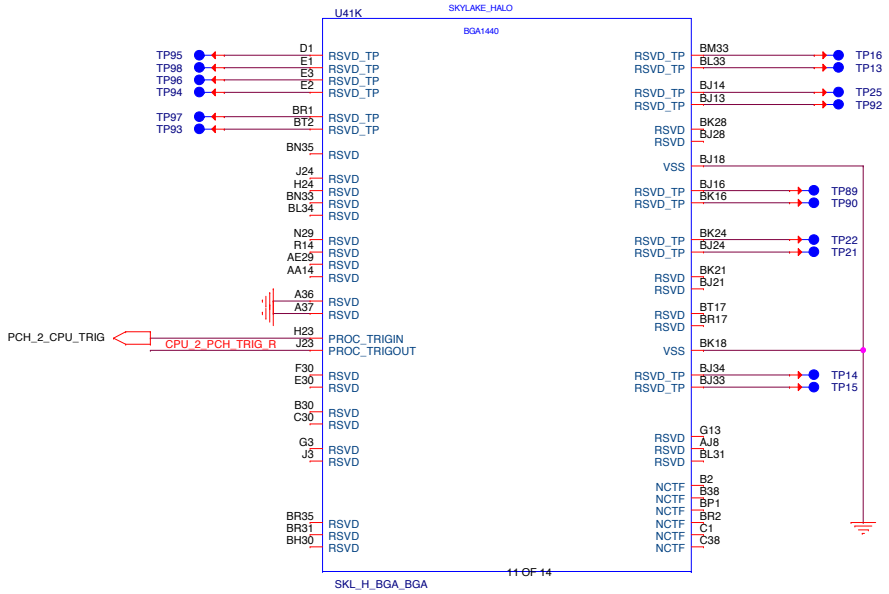
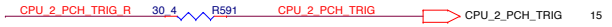
Haswell Processor (GND)

Haswell Processor (RESERVED, CFG)





Processor Strapping

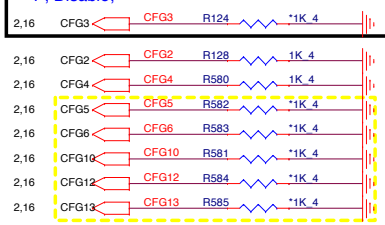
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT :ZRY
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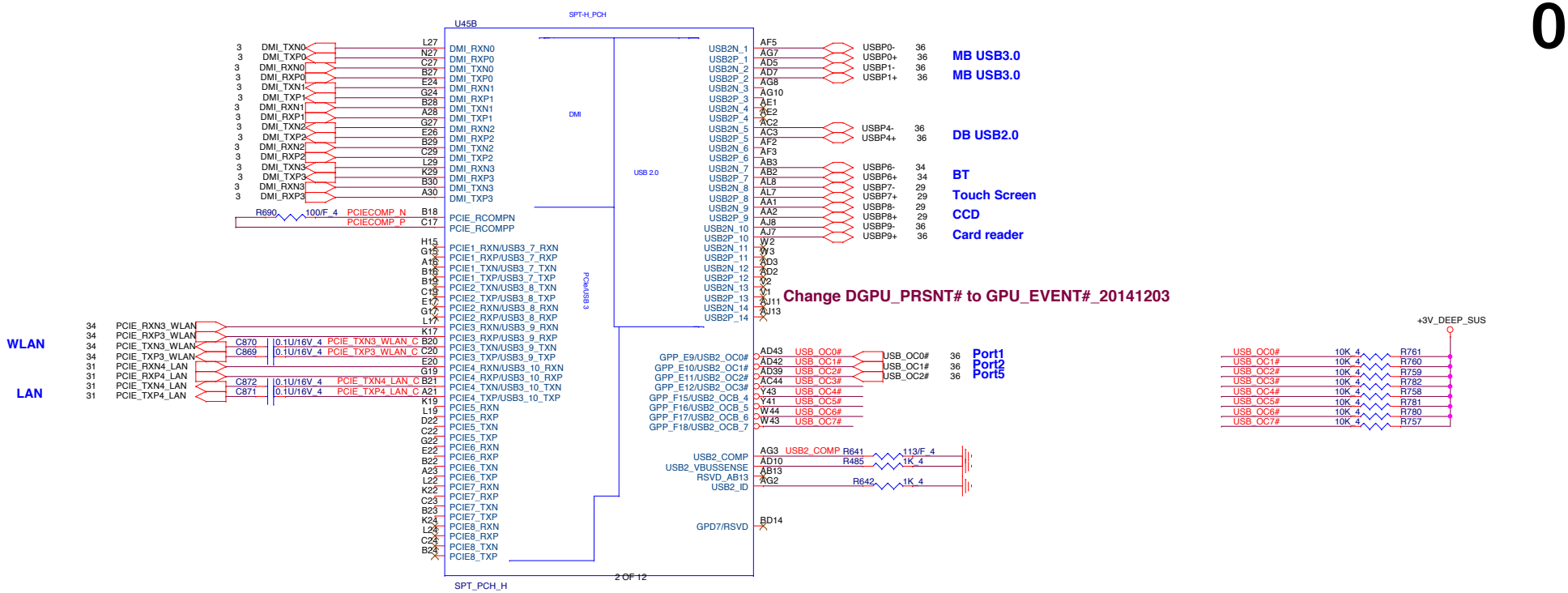

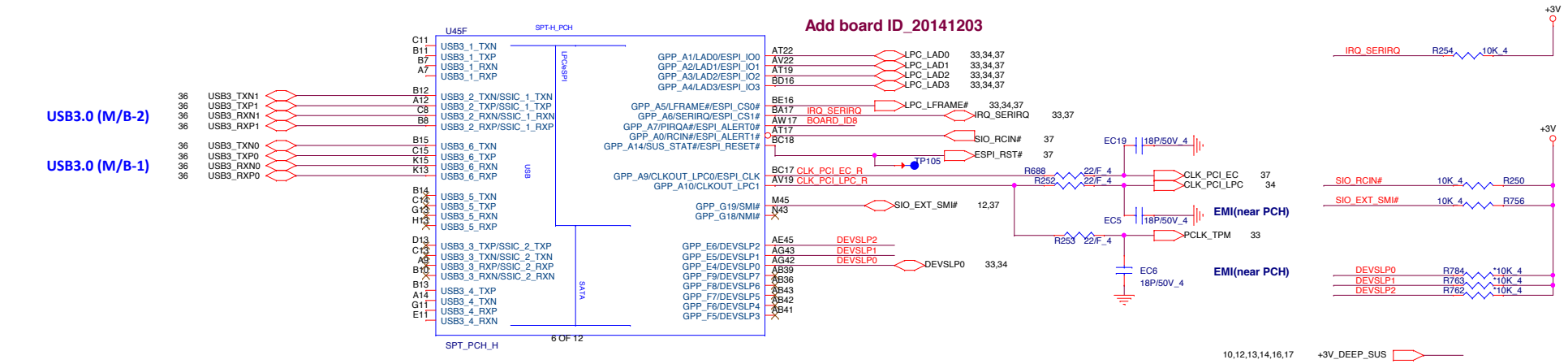

PROJECT :ZRY Quanta Computer Inc.			
Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)		Rev 1A
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HDA Bus(CLG)

0 = *Enable security in the Flash Description (iPD 20K)
1 = Disable Flash Descriptor Security (Override)

Add PU _20141212

Add SSD _20141210

DRAMRST

VGA
EC

Touch Pad
XDP
DDR3-L
CPU heat pipe local thermal sensor
DDR thermal sensor

System PWR_OK(CLG)

SYSPWOK

Non Deep Sx

For DS3 Sequence

For HWPG Sequence

For HWPG Sequence

RTC Circuitry (RTC)

On SKL voltage at VCCRTC does not exceed 3.2V

+3V_RTC
Trace width = 30 mils

+3V_RTC_[0:2]
Trace width = 20 mils

20MIL

REV:E tPLT15(max 200us) ->SLP_S4# assertion to VDDQ(+1.35VSUS) ramp down start(SUSON)

REV:E tPLT17(max 200us) ->SLP_S3# assertion to tMVP VR_ON(VRON) deassertion

REV:E tPLT18(max 200 us) ->SLP_S3# assertion to VCCIO VR(MAINP) for +1V_S5 to +VCCIO) disabled

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Quanta Computer Inc.	
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M.2.SSD

HDD (SATA0 6Gb/s)

24M X'tral--->R2602 (Ra) Un-Install
Green CLK--->R2602 (Ra) Install

+1.0V_DEEP_SUS change to +1V_S5

Add XCLK_RNIAS# port_20141205

VGA

WLAN

LAN

NGFF SSD

RTC Clock 32.768KHz

Change from I to NI(For SCH List) _20141212

PROJECT :ZRY
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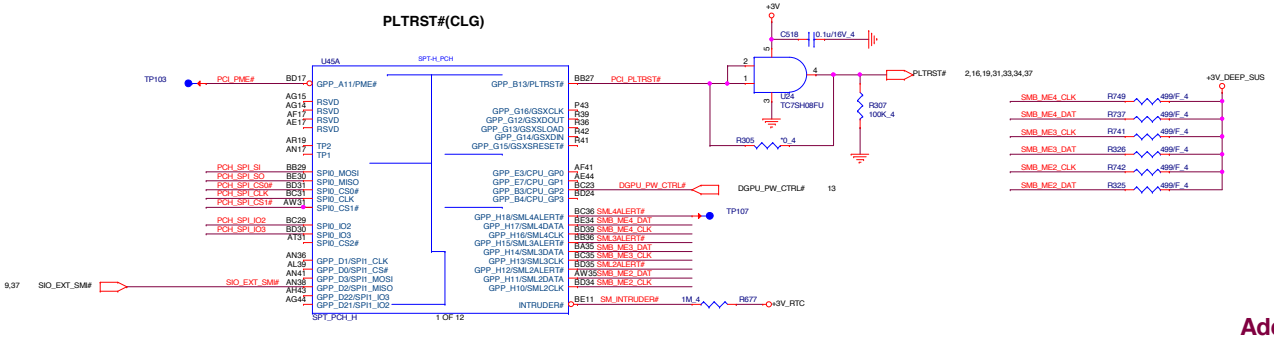
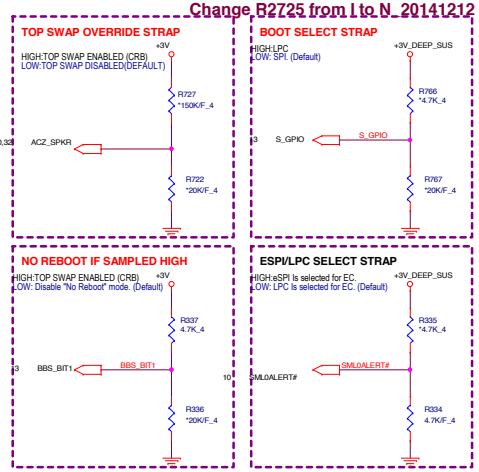
PLTRST# Buffer

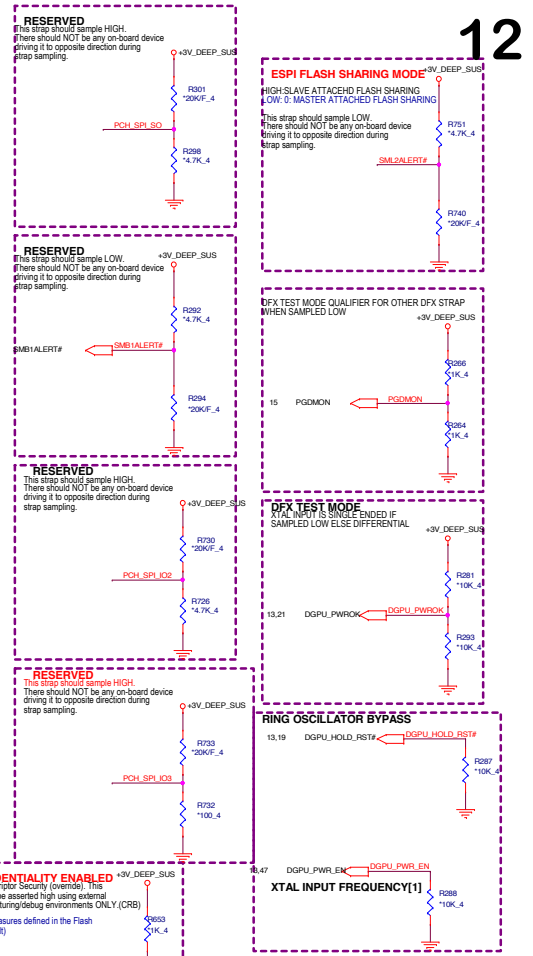
PLTRST#(CLG)



Add PCH Strap Pin_20141203

Change B2725 from L to N_20141212





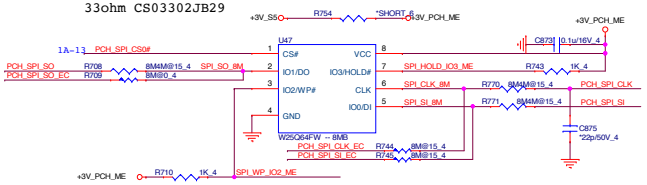
SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
	EON	8M	AKE3EZN0Q01	EN25QH64-104HIP
Skylake 3.3V	WND	16M	AKE3DZN0N01	W25Q128FVSIQ

PCH SPI ROM(8M+4M)

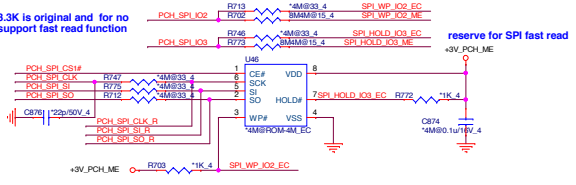
15ohm CS01502JB12

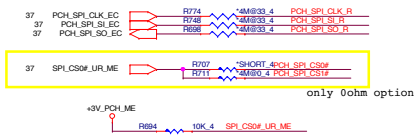
33ohm CS03302JB29



3.3K is original and for no support fast read function

reserve for SPI fast read





1A~3 2013/10/16 Add U34 flash 4M ROM reserve for ZQ0D.

TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)

LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

+3V_DEEP_SUS
R333
4.7K_4
10
SMBALERT#
SMBALERT#
R332
*20K/F_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R729
*20K/F_4
PCH_SPI_SI
R728
*4.7K_4

TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)

LOW: security measures defined in the Flash Descriptor. (Default)

+3V_DEEP_SUS
R653
1K_4
10,37
ME_WR#
ME_WR#
R640
1K_4

PROJECT :ZRY
Quanta Computer Inc.

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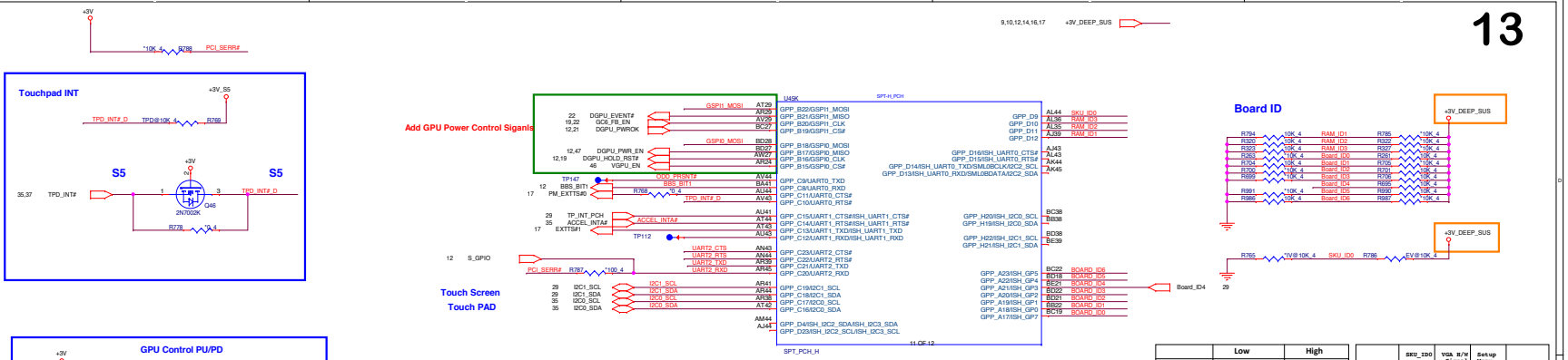

	Low	High
BOARD_ID0	VRAM 2GB	VRAM 4GB
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	No G-sensor	G-sensor
BOARD_ID3	TPM	No TPM
BOARD_ID4	No touch panel	touch panel

	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	UMA	Hidden	UMA boot
dGPU Only	1	GPU	Hidden	GPU boot

	Low	High
BOARD_ID5	Reserved (Before C1)	Reserved (After C2)
BOARD_ID6	Reserved (Default)	Reserve

Skylake-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R725 *1K_4 GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) 1 = Enable Intel ME Cryp to TLS	
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R717 *1K_4 GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

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Custom	PCH 4/6 (GPIO/MISC)	1A
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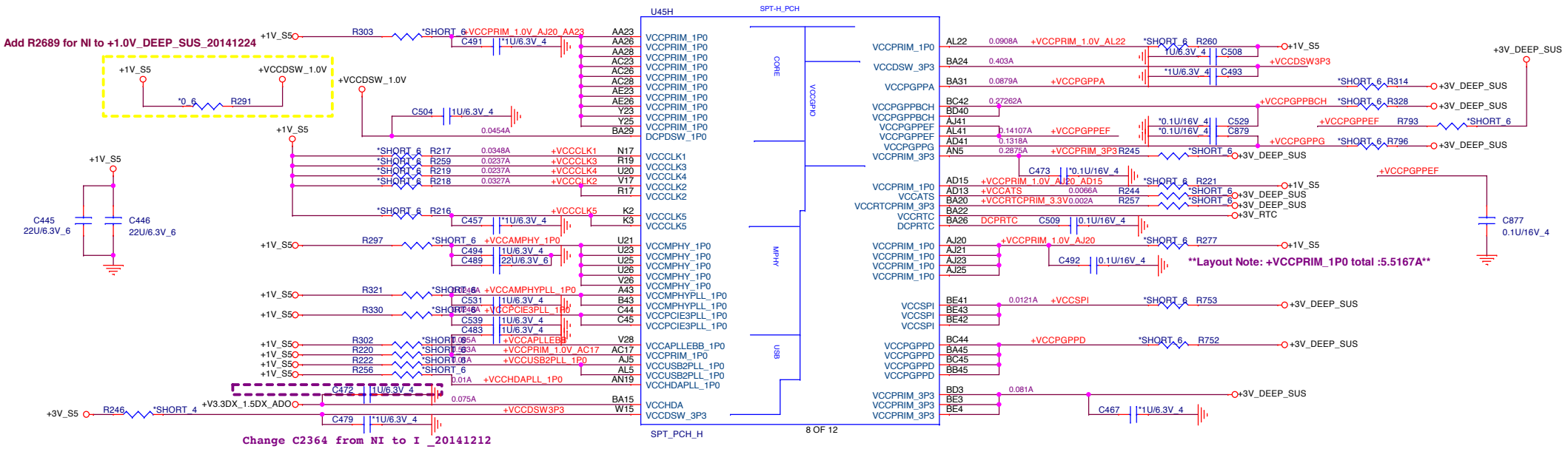
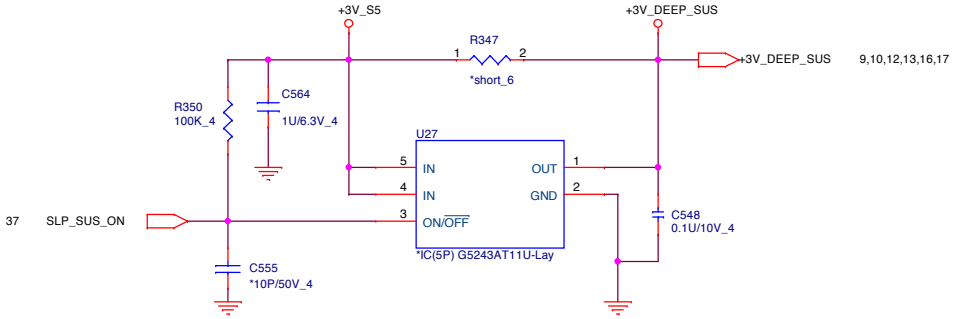


for DS3



PROJECT :ZRY Quanta Computer Inc.		
Size A3	Document Number PCH 5/6 (POWER)	Rev 1A
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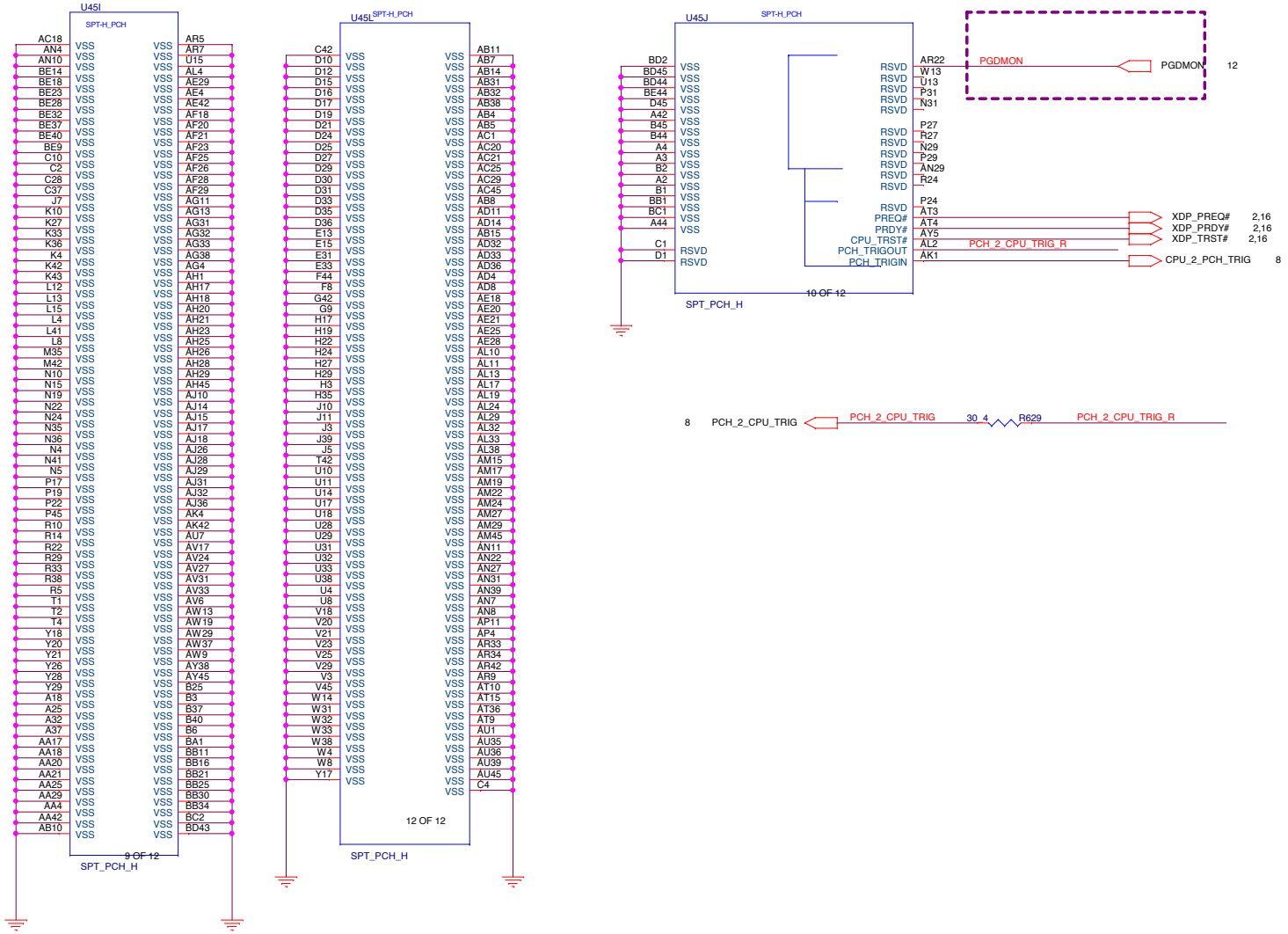

5,10,29,31,32,34,35,37,38,39,46,47 +3VPCU

PROJECT :ZRY Quanta Computer Inc.		
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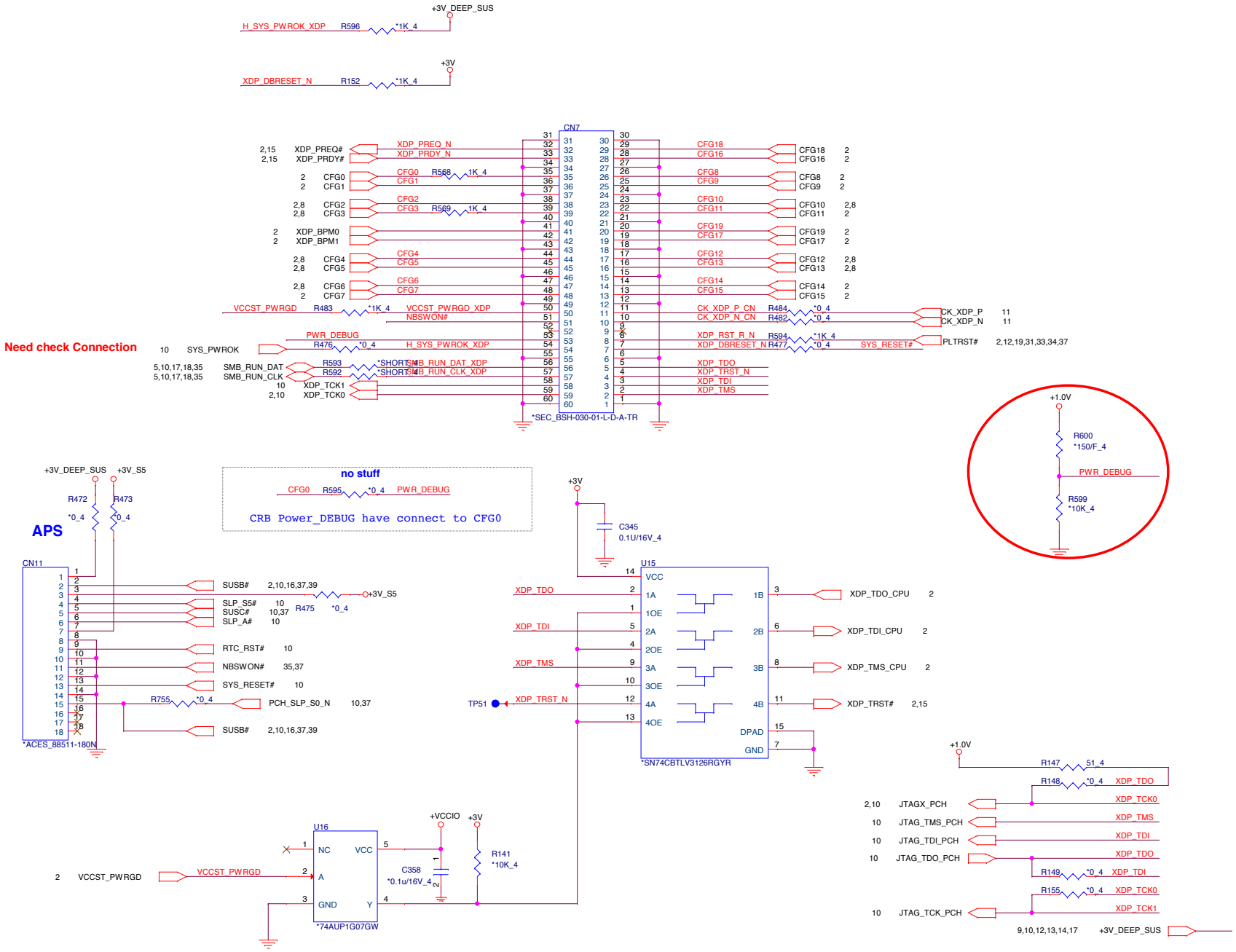

PROJECT :ZRY Quanta Computer Inc.		
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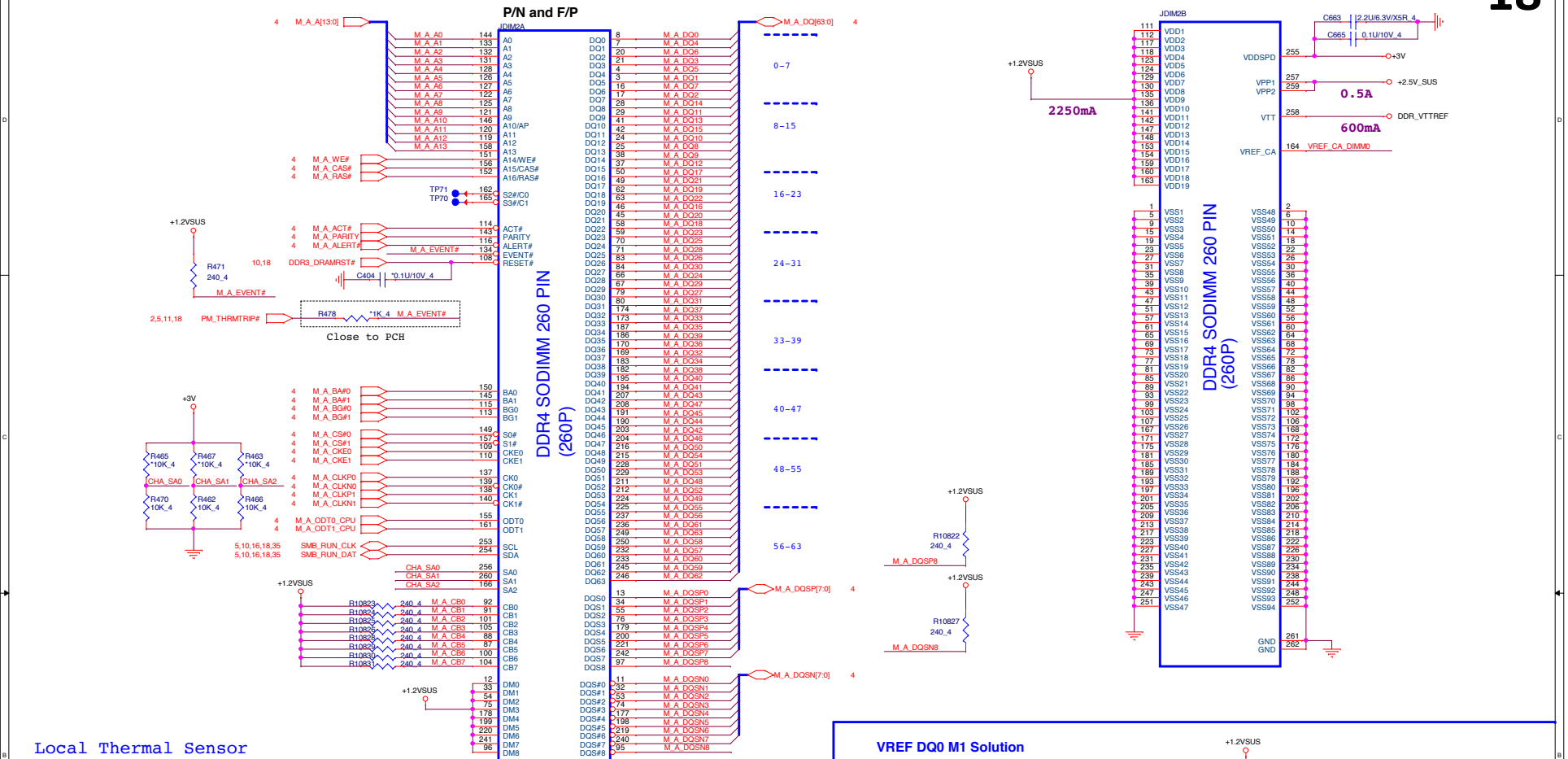
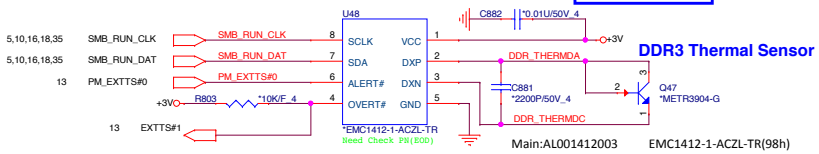


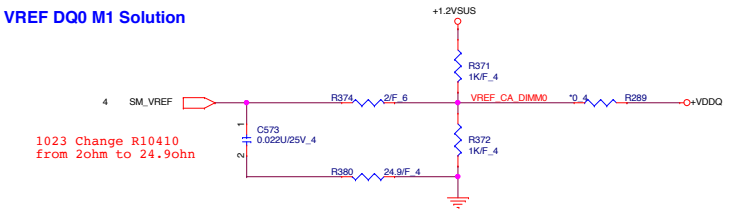
Local Thermal Sensor



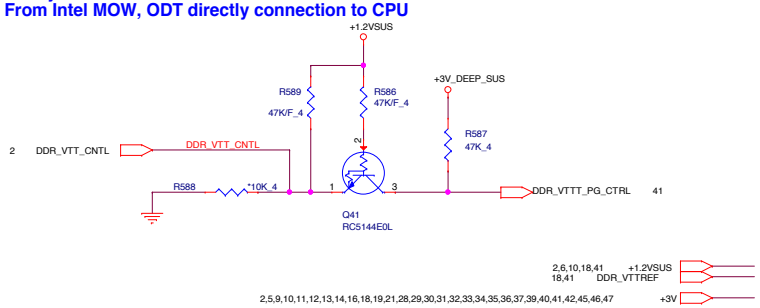
Main:AL001412003 EMC1412-1-ACZL-TR(98h)

2nd:AL000431014 TMP431ADGKR(98h)

VREF DQ0 M1 Solution

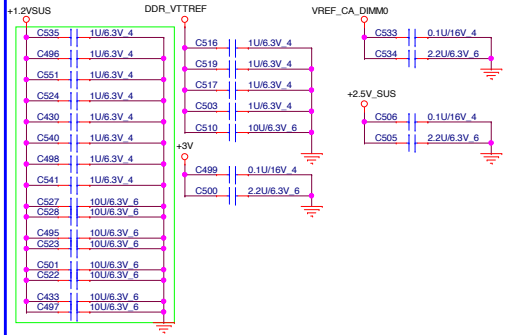


Co-lay for ODT
From Intel MOW, ODT directly connection to CPU



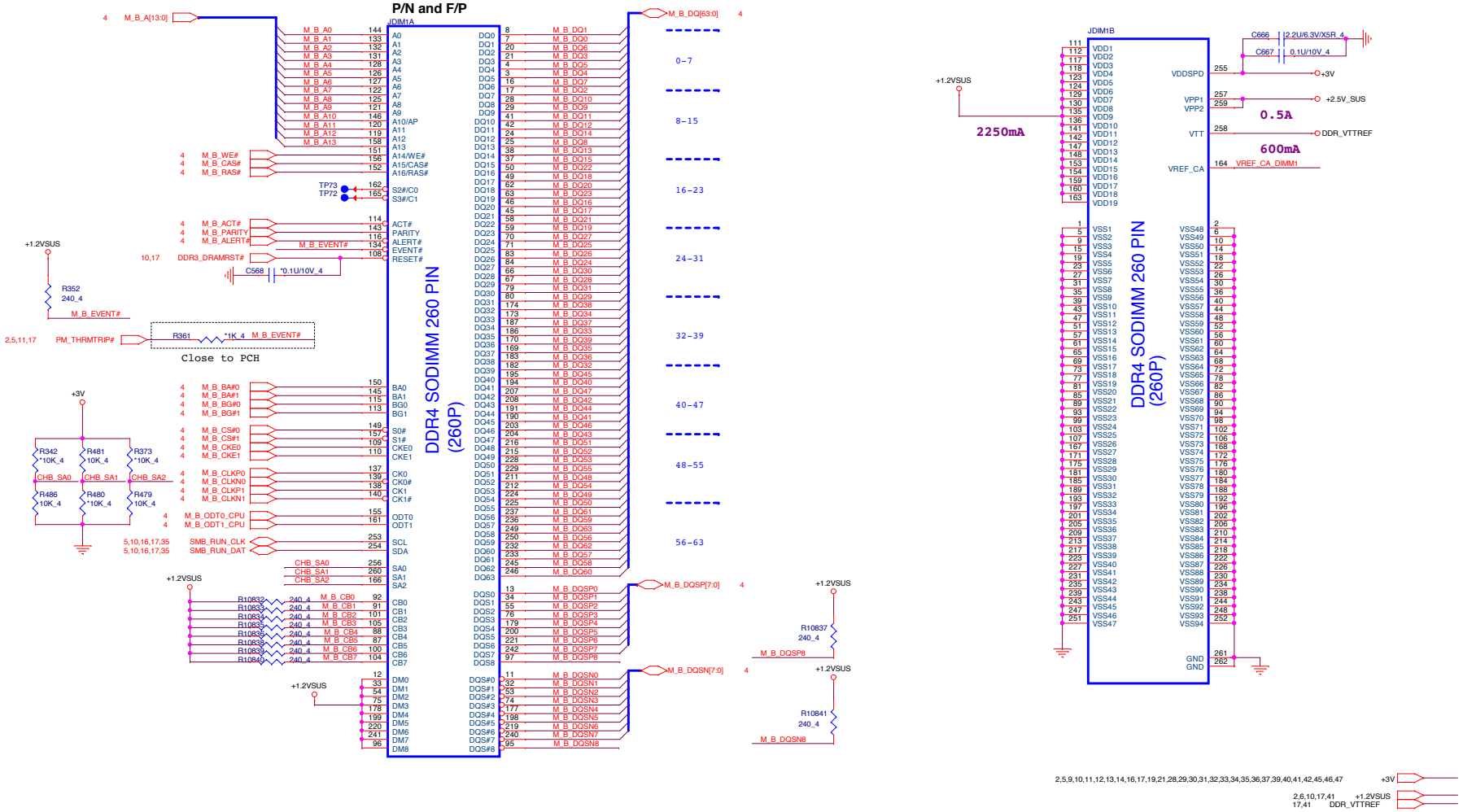
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



PROJECT :ZRY Quanta Computer Inc.			
Size Custom	Document Number 18 -- DDR3 DIMM1-RVS(8.0H)		Rev 1A
Date: Tuesday, August 25, 2015		Sheet 17	of 49

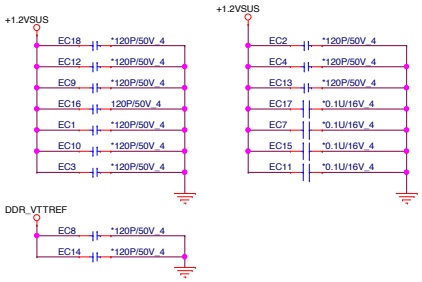
P/N and F/P



2,5,9,10,11,12,13,14,16,17,19,21,28,29,30,31,32,33,34,35,36,37,39,40,41,42,45,46,47 +3V

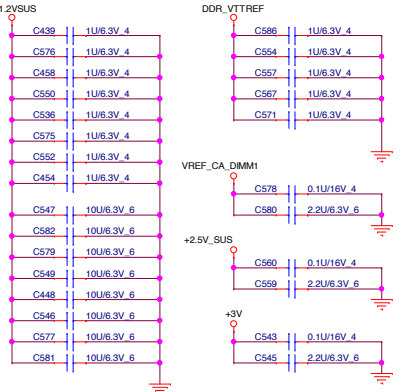
2,6,10,17,41 +1.2VSUS
17,41 DDR_VTTREF

For EMI RESERVE

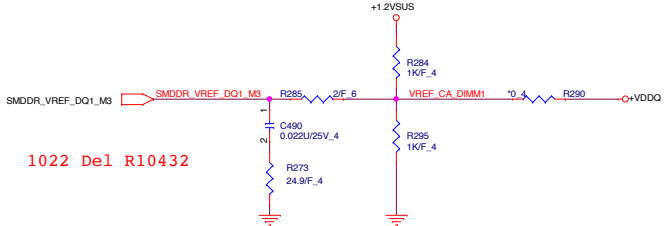


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

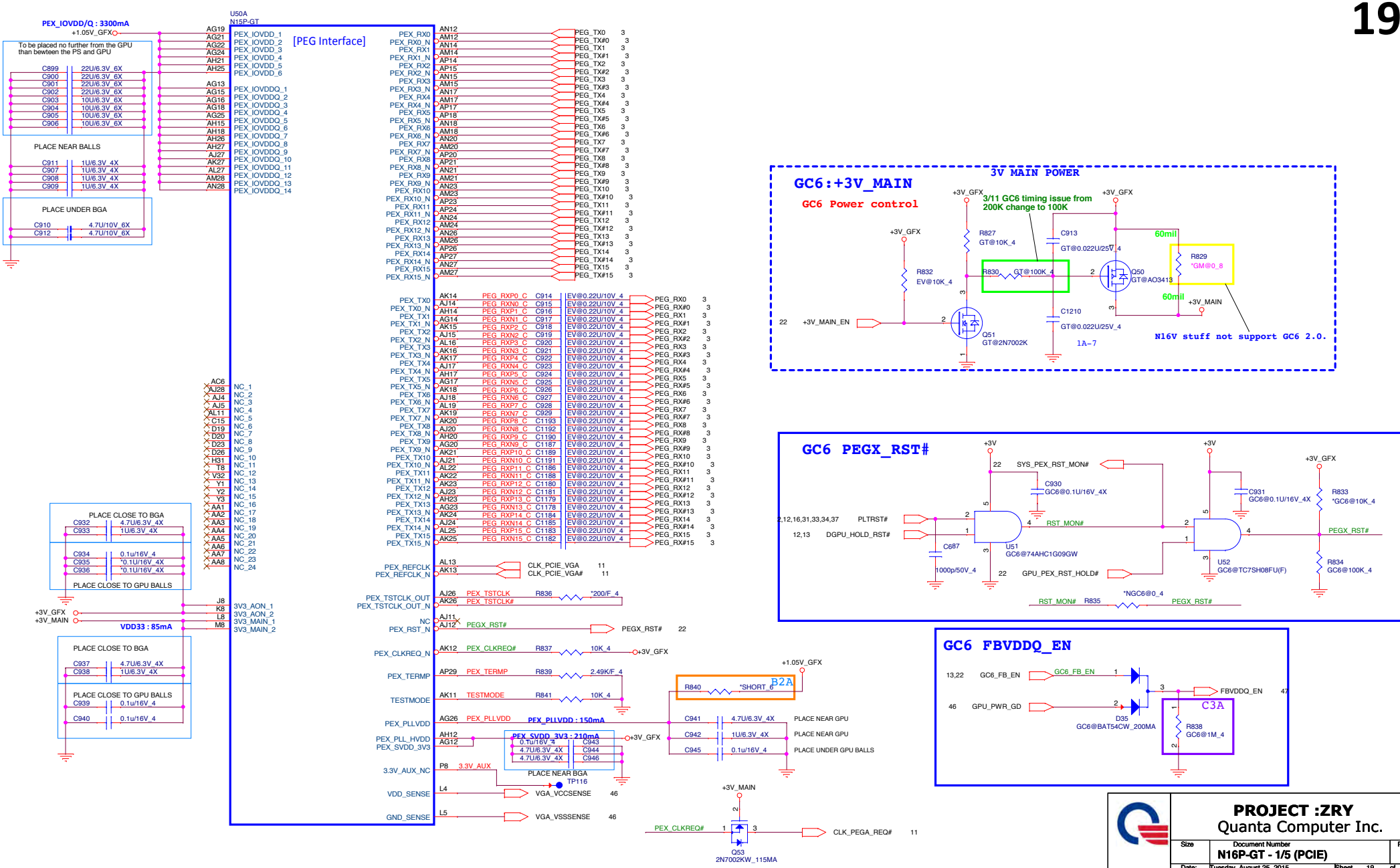


VREF DQ1 M1 Solution

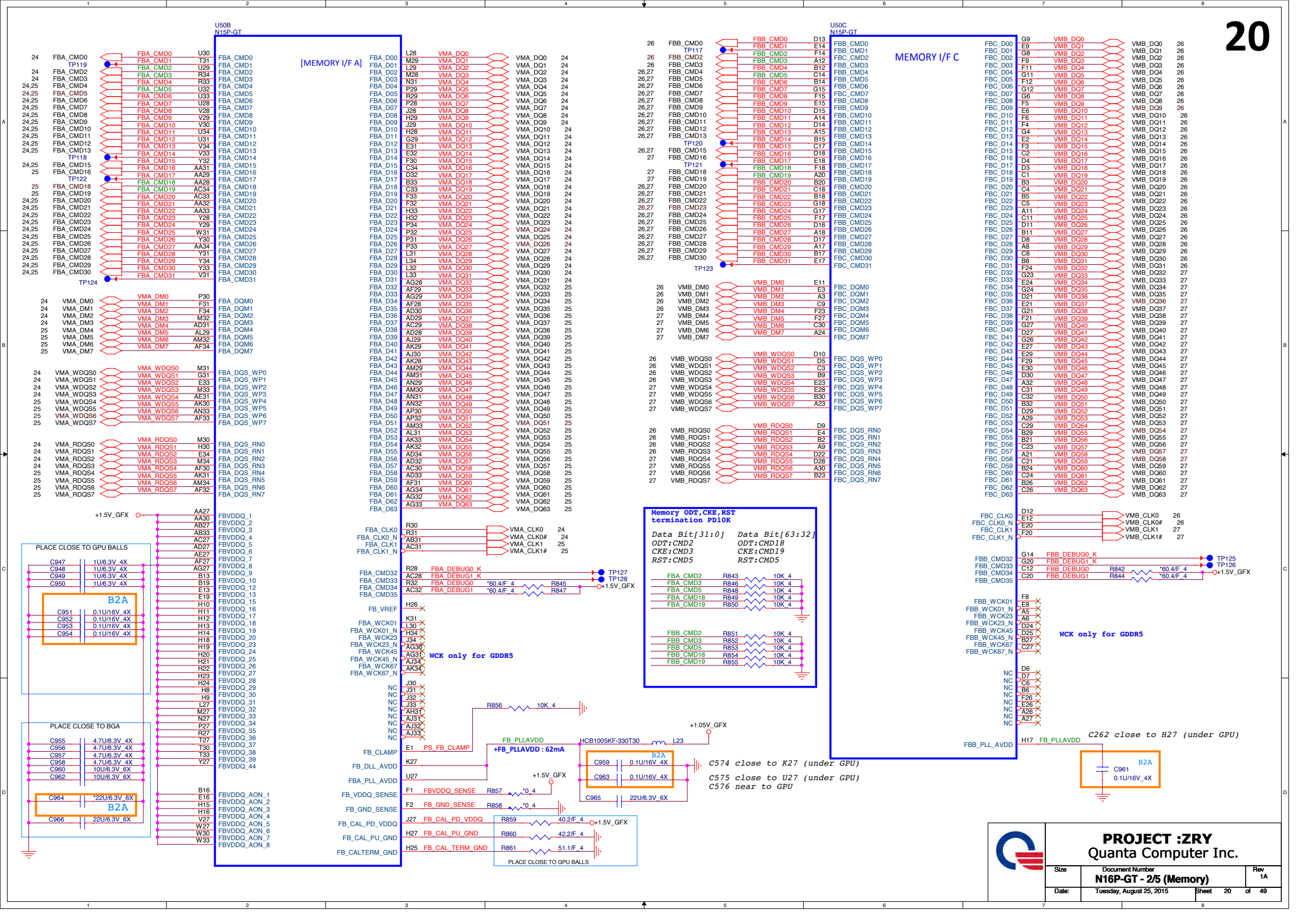


1022 Del R10432

PROJECT :ZRY Quanta Computer Inc.		
Size: Custom	Document Number: 17 – DDR3 DIMM0-STD(4.0H)	Rev: 1A
Date: Tuesday, August 25, 2015	Sheet 18 of 49	



PROJECT :ZRY		
Quanta Computer Inc.		
Size	Document Number: N16P-GT - 1/5 (PCIE)	Rev: 1A
Date: Tuesday, August 25, 2015	Sheet 19 of 49	



PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
	N16P-GT - 2/5 (Memory)	1A
Date: Tuesday, August 25, 2015	Sheet 20 of 49	

U50D
N15P-GT

[IFPA/B_LVDS]
AH8 IFPAB_PLLVDD
AG8 IFPA_IOVDD
AG9 IFPB_IOVDD
AJ8 IFPAB_RSET
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
AF7 IFPC_PLLVDD
AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
AG6 IFPD_IOVDD
AF8 IFPC_RSET
AN2 NC
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

[IFPE/F_DP]
AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
AC8 IFPF_IOVDD
AD6 IFPEF_RSET
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

[DACA/B_CRT]
AG10 DACA_VDD
AP9 DACA_VREF
AP8 DACA_RSET
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL
I2CA_SDA

[XTAL IN]
AD8 PLLVDD
AE8 SP_PLLVDD
AD7 VID_PLLVDD
XTAL_IN H3
XTAL_OUT H2
XTAL_OUTBUFF J4
XTAL_SSIN H1

3V_MAIN_PWGD

+3V_MAIN R104 EV@4.7K_4 C967 *1000p/50V_4
Q8 EV@MMBT3904-7-F
+3V R81 EV@4.7K_4 C147 EV@1000p/50V_4
+3V_GFX R862 EV@1.5K/F_4
Q6 EV@DTC144EU
3V_MAIN_PWGD R863 *100K/F_4
3V_MAIN_PWGD 46,47

+1.05V_GFX and GPU core power EN

DGPU_PWROK

DGPU_PGOK-1
47 HWPG_1.5VGFX R867 EV@4.7K_4 C969 *1000P/50V_4
DGPU_POK2
Q55 EV@METR3904-G
+3V R865 EV@4.7K_4 C968 EV@1000P/50V_4
+3V_GFX R864 EV@4.7K_4
Q54 EV@DTC144EUA
R866 EV@100K/F_4
DGPU_PWROK 12,13

R4 I2CA_SCL 1.8K/F_4 R868
R5 I2CA_SDA 1.8K/F_4 R869

Reserve
+3V_GFX
XTAL_OUTBUFF R870 *10K_4

XTAL27_IN
XTAL27_OUT
Y5 27MHZ_10
C972 10P/50V_4C
C973 10P/50V_4C
B2A

PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS
PLLVDD : 200mA
+1.05V_GFX L24 HCB1005KF-330T30
C970 22U/6.3V_6X
NV_PLLVDD
B2A
C971 0.1U/16V_4X
PLLVDD
C5092 Close to AE8
C5090 Close to AD7
+1.05V_GFX L25 BLM15PX181SN1D_1.5A
C974 22U/6.3V_6X
C975 4.7U/6.3V_4X
B2A
C976 0.1U/16V_4X
C977 0.1U/16V_4X

H3 XTAL27_IN
H2 XTAL27_OUT
J4 XTAL_OUTBUFF R871 10K_4
H1 XTAL_SSIN R872 10K_4

PROJECT :ZRY
Quanta Computer Inc.

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	N16P-GT - 3/5 (Display)	1A
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Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18 GM
49.9K ---> CS34992FB10 GT

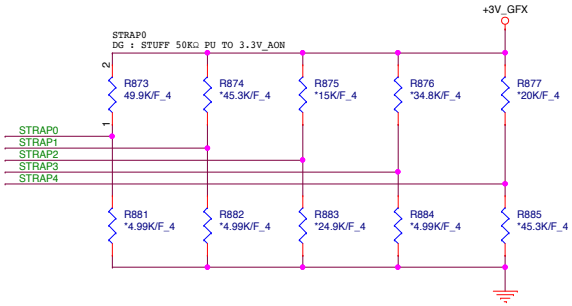
U50E
N15P-GT

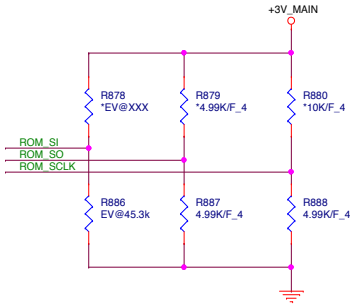
[MIOA]

[MIOB]

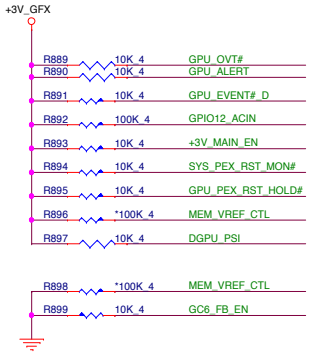
[MISC_GPIO/I2C/JTAG/THER]

[MISC2_ROM]

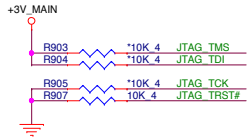


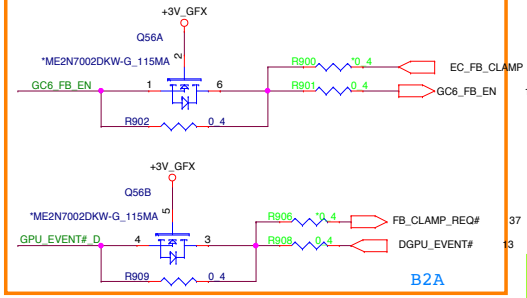


	Package	DevID
N16P-GT-A2	GB4b-128	0x139A
N16V-GM-B1	GB2-64	0x1299
N16S-GM-S-A2	GB2b-64	0x1346



Reserve PU/PD for Debug





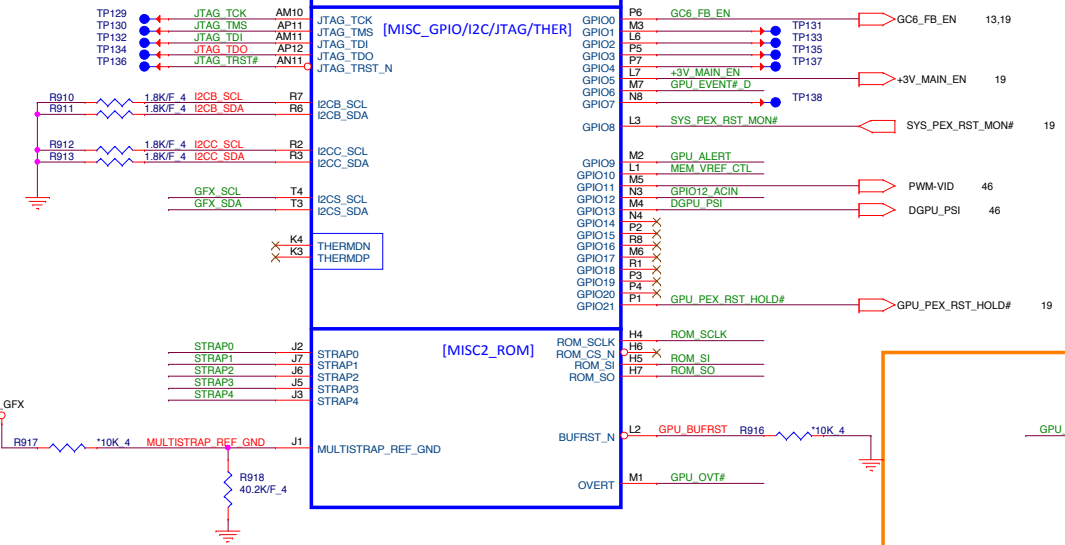
	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Mutil-level mode strapping:
For N16P-GT-A2 :
R886=40.2k PD
1.ROM_SCLK =4.99K PD
2.ROM_SO = 4.99K PD
3.ROM_SI= Memory strap setting
4.STRAP0 = 49.9k PU
5.Strap4~1 = Reserve Pull up and Pull down

N16P-GT-A2 VRAM Configuration Table:

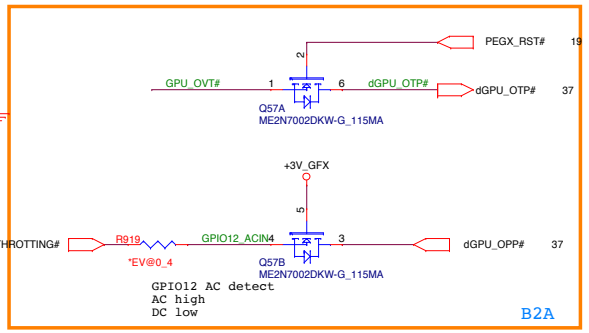
	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	ROM_SI
2Gb	0110 (0x6) 0111 (0x7) 1000 (0x8)	DDR3 128MBx16,1000MHz DDR3 128MBx16,1000MHz DDR3 128MBx16,1000MHz	HYNIX MICRON SAMSUNG	H5TC2G63FFR-11C MT41J128M16JT-093G:K K4W2G1646Q-BC1A		34.8K Pull down 45.3K Pull down 4.99K Pull UP
4Gb	0101 (0x5) 0001 (0x1) 0010 (0x2)	DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz	HYNIX MICRON SAMSUNG	H5TC4G63CFR-11C MT41J256M16HA-093G:E K4W4G1646D-BC1A		30.1K Pull down 10K Pull down 15K Pull down

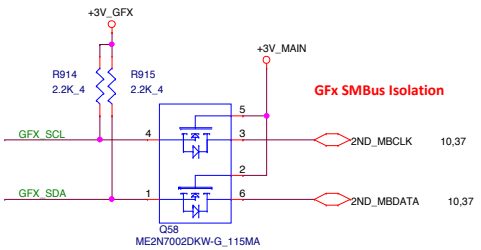
B2B



N16P-GT-A2 (GB4b-128)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0001
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0001
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND [Stuff 49.9K PU]				0001
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND [Do Not Stuff				
STRAP2					
STRAP3					
STRAP4					





PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
	N16P-GT - 4/5 (MISC)	1A
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VDD/XVDD : 43A

+VGPU_CORE

U50F
N15P-GT

[GPU VDD]

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_026	Y4
M23	VDD_024	XVDD_027	Y5
N13	VDD_025	XVDD_028	Y6
N15	VDD_026	XVDD_029	Y7
N17	VDD_027	XVDD_030	Y8
N18	VDD_028		
N20	VDD_029		
N22	VDD_030		
P12	VDD_031		
P14	VDD_032		
P16	VDD_033		
P19	VDD_034		
P21	VDD_035		
P23	VDD_036		
R13	VDD_037		
R15	VDD_038		
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

+VGPU_CORE

U50G
N15P-GT

[GPU GND]

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	R21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN28	GND_79	GND_179	U21
AN30	GND_80	GND_180	U23
AN34	GND_81	GND_181	V12
AN4	GND_82	GND_182	V14
AN7	GND_83	GND_183	V16
AP2	GND_84	GND_184	V19
AP33	GND_85	GND_185	V21
B1	GND_86	GND_186	V23
B10	GND_87	GND_187	W13
B22	GND_88	GND_188	W15
B25	GND_89	GND_189	W17
B28	GND_90	GND_190	W18
B31	GND_91	GND_191	W20
B34	GND_92	GND_192	W22
B4	GND_93	GND_193	W28
B7	GND_94	GND_194	Y12
C10	GND_95	GND_195	Y14
C13	GND_96	GND_196	Y16
C19	GND_97	GND_197	Y19
C22	GND_98	GND_198	Y21
C25	GND_99	GND_199	Y23
C28	GND_100	GND_200	AH11
C7		GND_OPT_1	C16
		GND_OPT_2	W32

+VGPU_CORE

PLACE UNDER GPU

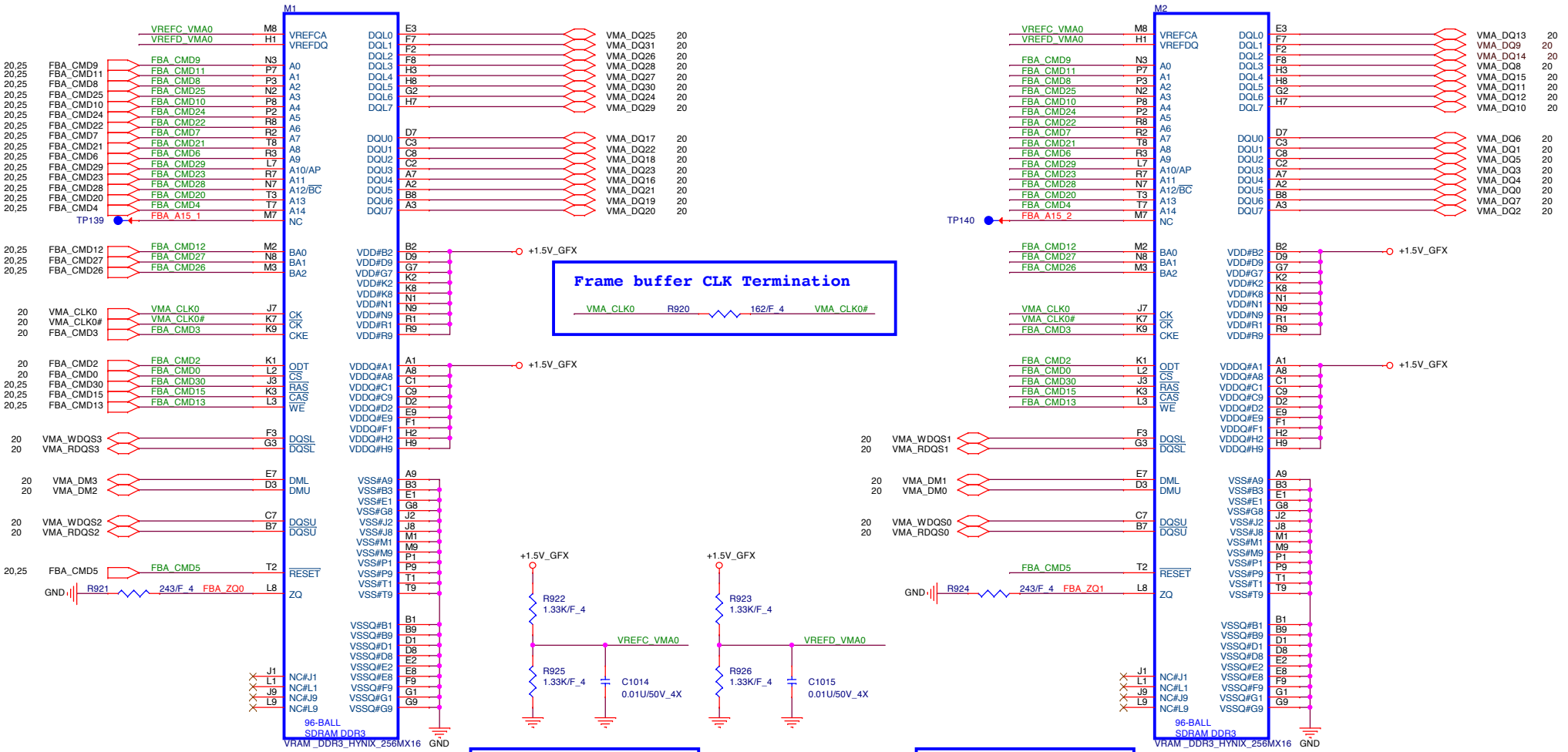
C978	1U/6.3V_4X	
C979	1U/6.3V_4X	
C980	1U/6.3V_4X	
C981	1U/6.3V_4X	
C982	1U/6.3V_4X	
C983	1U/6.3V_4X	
C984	1U/6.3V_4X	
C985	1U/6.3V_4X	
C986	4.7U/10V_6X	
C987	4.7U/10V_6X	
C988	4.7U/10V_6X	
C989	4.7U/10V_6X	
C990	4.7U/10V_6X	
C991	*4.7U/10V_6X	B2A
C992	4.7U/10V_6X	
C993	4.7U/10V_6X	
C994	4.7U/10V_6X	
C995	*4.7U/10V_6X	B2A
C996	4.7U/10V_6X	
C997	*4.7U/10V_6X	B2A
C998	*4.7U/10V_6X	
C999	4.7U/10V_6X	
C1000	4.7U/10V_6X	

PLACE NEAR GPU

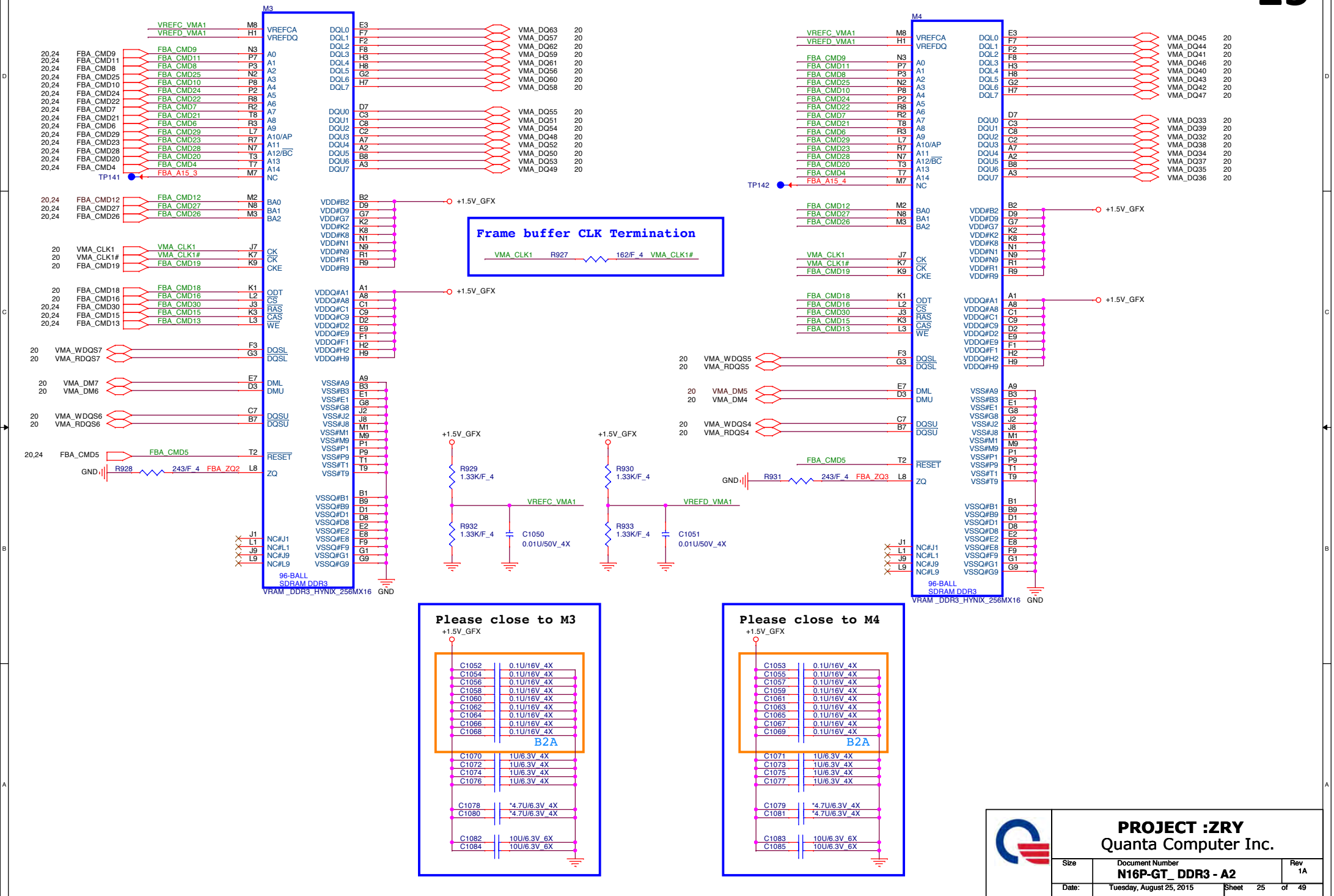
C1001	1 22U/6.3V_6X	B2A
C1002	1 22U/6.3V_6X	
C1003	1 22U/6.3V_6X	
C1004	1 22U/6.3V_6X	
C1005	1 22U/6.3V_6X	
C1006	1 22U/6.3V_6X	
C1007	1 22U/6.3V_6X	
C1008	4.7U/10V_6X	
C1009	4.7U/10V_6X	
C1010	*4.7U/10V_6X	B2A
C1011	4.7U/10V_6X	
C1012	4.7U/10V_6X	
C1013	1 + 2 EV@330u_2.5V_3528	

PROJECT :ZRY
Quanta Computer Inc.
ZRY

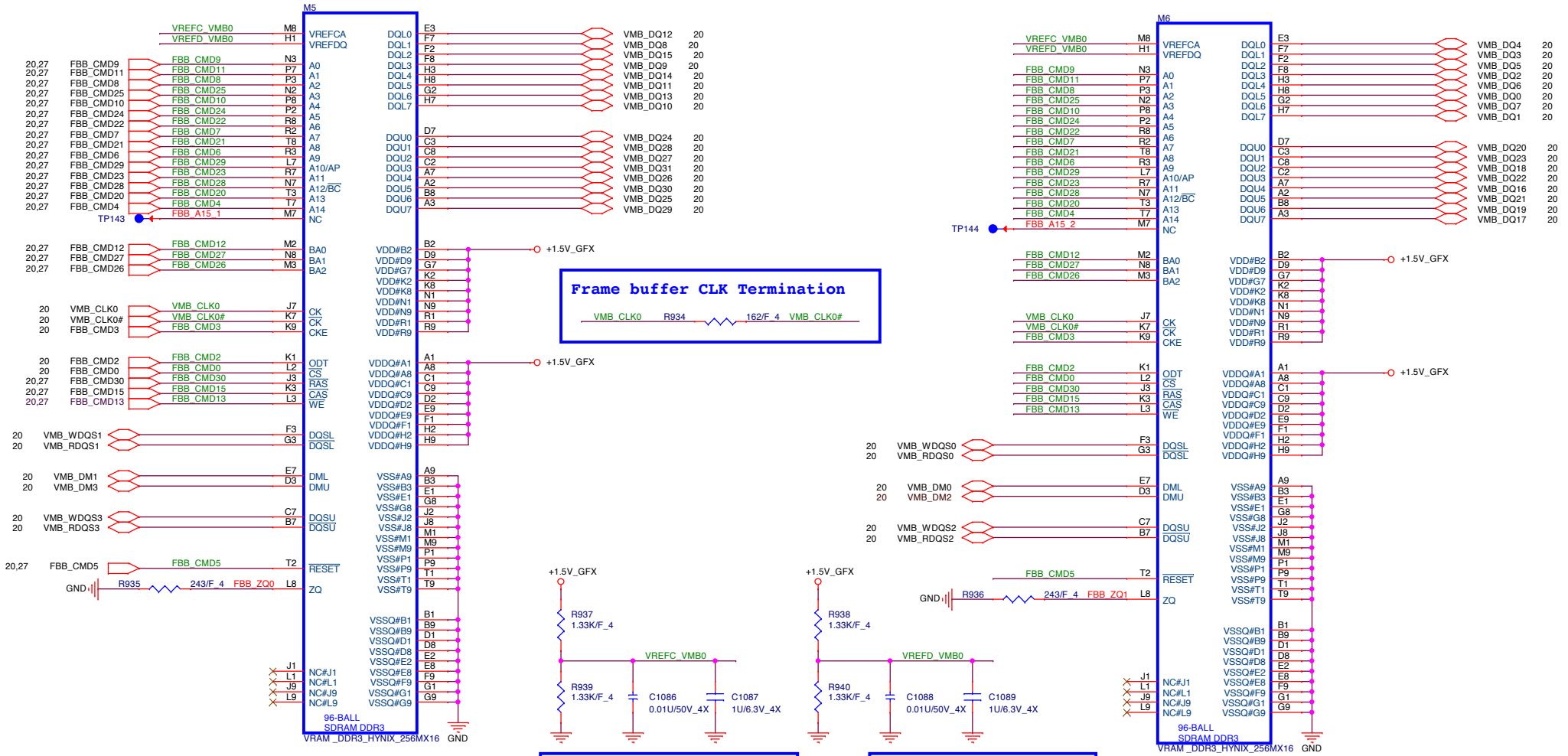
Size	Document Number	Rev
	N16P-GT - 5/5 (Power)	1A
Date:	Tuesday, August 25, 2015	Sheet 23 of 49



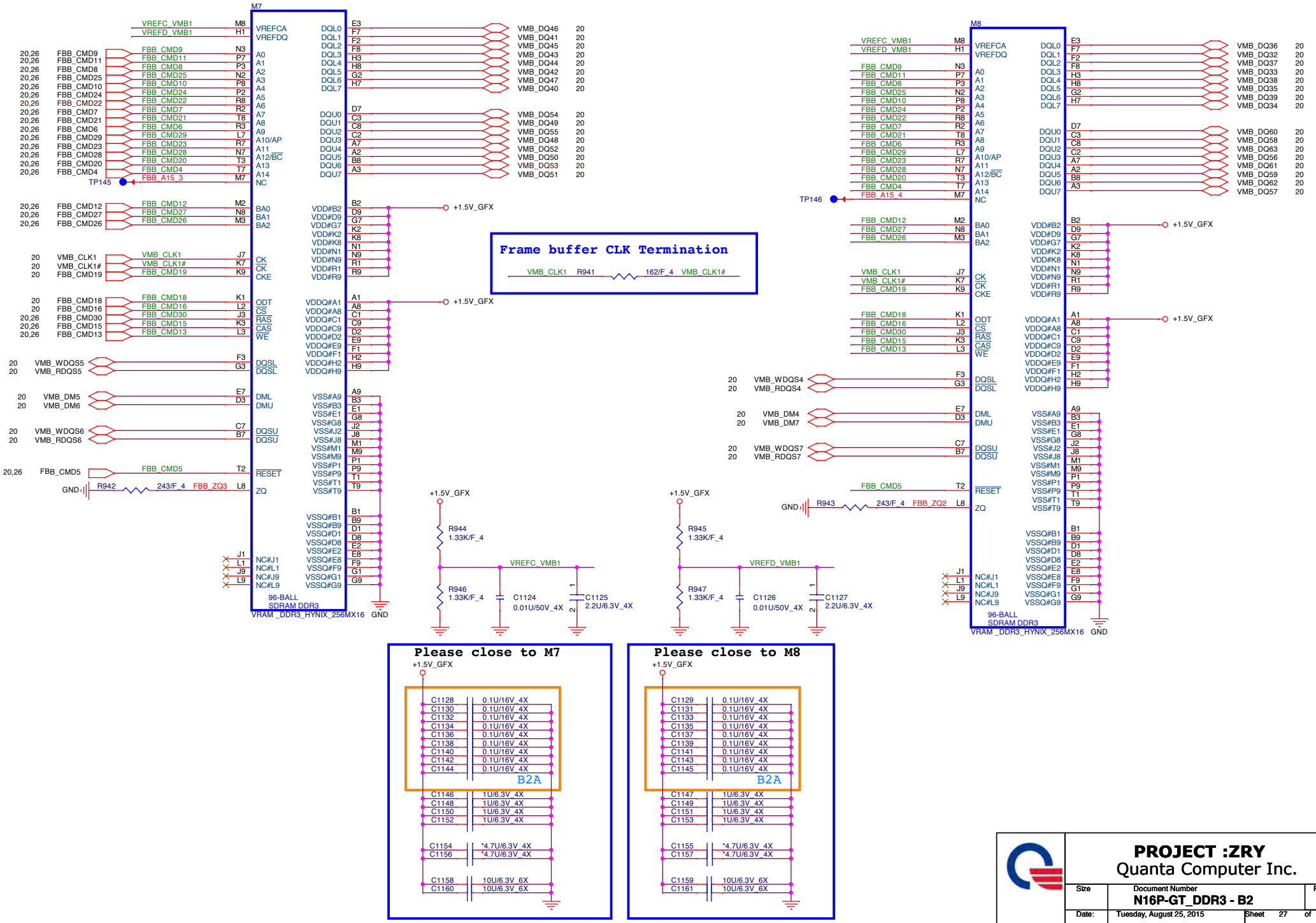
PROJECT :ZRY			
Quanta Computer Inc.			
Size	Document Number		Rev
	N16P-GT_DDR3 - A1		1A
Date:	Tuesday, August 25, 2015	Sheet 24 of 49	



PROJECT :ZRY		
Quanta Computer Inc.		
Size	Document Number: N16P-GT_ DDR3 - A2	Rev: 1A
Date: Tuesday, August 25, 2015	Sheet 25 of 49	



PROJECT :ZRY Quanta Computer Inc.			
Size	Document Number N16P-GT_DDR3 - B1		Rev 1A
Date:	Tuesday, August 25, 2015	Sheet 26 of 49	



PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
	N16P-GT_DDR3 - B2	1A
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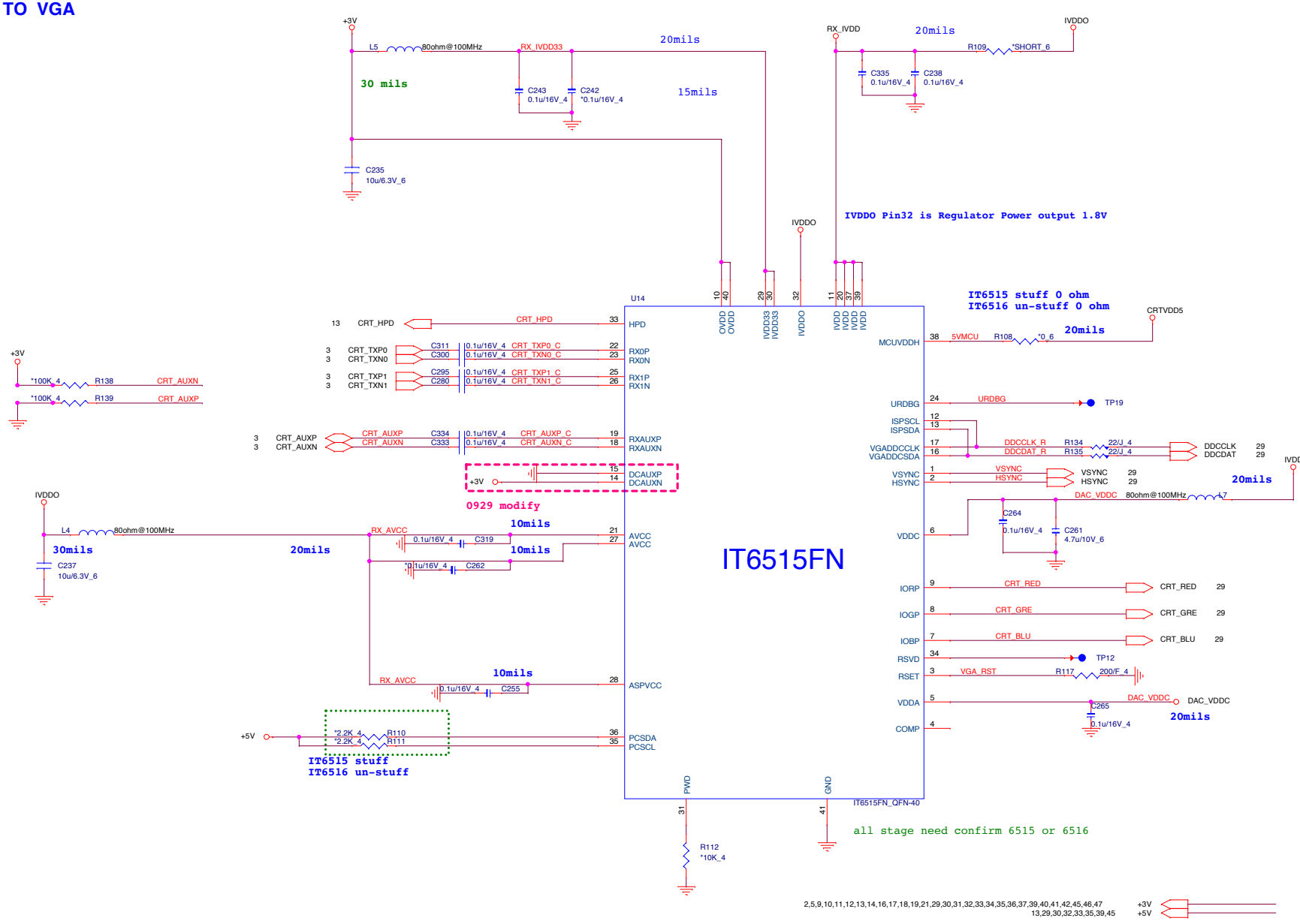
DP TO VGA



PROJECT :ZRY Quanta Computer Inc.		
Size	Document Number DP to VGA iT6165	Rev 1A
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CRT

1C-1 2014/01/10 Remove U29 and add U40 and U41.

U11 M74VHC1GT125DF2G — HSYNC → CRTHSYNC
U9 M74VHC1GT125DF2G — VSYNC → CRTVSYNC

Q40 AP2331SA-7 — +5V → CRTVDD5

CRT_RED, CRT_GRE, CRT_BLU → BLM18BB470_6 → CRT_R1, CRT_G1, CRT_B1 → CN5 CRT CONN

CRT_11 → TP20
DDCDAT → DDCDAT 28
DDCCLK → DDCCLK 28

U12 *RClamp0524P — CRTHSYNC, CRTVDD5, CRTVSYNC, DDCCLK
U13 *RClamp0524P — CRT_R1, CRT_G1, DDCDAT, CRT_B1

DDCDAT 2.2K_4 R561 CRTVDD5
DDCCLK 2.2K_4 R554

C808 *0.22u/6.3V_4
C801 *220p/50V_4
C799 0.1u/16V_4 CRTVDD5
C232 10p/50V_4 CRTVSYNC
C240 10p/50V_4 CRTHSYNC
C800 *10p/50V_4 DDCCLK
C804 *10p/50V_4 DDCDAT

2,5,9,10,11,12,13,14,16,17,18,19,21,28,30,31,32,33,34,35,36,37,39,40,41,42,45,46,47

Power trace tracking

13,28,30,32,33,35,39,45 +3V
5,10,31,32,34,35,37,38,39,46,47 +5V
38,39,40,41,42,43,44,45,46,47 +3VPCU
VIN

LCD CONNECTOR

VIN: C9 4.7u/25V_8, C6 1000p/50V_4
TP_PWR: C688 0.1u/16V_4, C686 1000p/50V_4
CCD_PWR: C7 0.1u/10V_4_X7R, C8 1000p/50V_4

1A-5

R468 *100K_4 EDP_AUX_C, R464 *100K_4 EDP_AUX#_C, R21 *100K_4, R19 *100K_4, TP_RST# R12 *TSI@10K_4

2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage

EDP_HPD — C1 180P/50V_4 — Prevent ESD/EOS Layout near device

eDP FHD

Add 10 ohm Prevent CPU damage

PCH_BRIGHT → R13 *SHORT_4 → BRIGHT
EDP_HPD → R11 33_4 → EDP_HPD_R

EDP_AUXP/N C29/C21 .1U/16V_4 → EDP_AUX_C / EDP_AUX#_C
EDP_TXP1/N C682/C680 → EDP_TXP1_C / EDP_TXN1_C
EDP_TXP0/N C684/C683 → EDP_TXP0_C / EDP_TXN0_C

Touch Panel-I2C: I2C1_SCL_C, I2C1_SDA_C → R18, R15 *0_4

Touch Panel-USB: USBP7+/- → R460, R457 *0_4

CCD-USB: USBP8+/- → R456, R453 *SHORT_4 → USBP8+_R, USBP8-_R

eDP 4k*2k: EDP_TXP2/N C662/C661, EDP_TXP3/N C671/C664 → EDP_TXP2_C, EDP_TXN2_C, EDP_TXP3_C, EDP_TXN3_C

TS_EN → R8 *SHORT_4 → TS_EN_CR

Board_ID4 → R454 33_4 → BOARD_ID4_TOUCH_S

S5

C660 180P/50V_4 — Prevent ESD/EOS Layout near device

TP_INT

CN2 50398-04071-001

MAX 1.5A

R16 *SHORT_8, R17 *SHORT_8 → V_BLIGHT

LCDVCC: C691 *1u/6.3V_4, C692 *10/6.3V_4, R25 *SHORT_8, R14 *SHORT_6 → LCDVCC_R → CCD_PWR

R474 *SHORT_6, R469 0_4 → TP_PWR, TP_RST#

BL_ON

TS_EN R5 *0_4 TP_INT

1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.

Touch Panel interrupt

+3V → R1 10K_4 → TP_INT_PCH → Q2 2N7002K → TP_INT

S5 — S0

LCD Power

+3V → C45 1u/6.3V_4 → U1 G5243AT11U (IN, IN, ON/OFF, OUT, GND, GND) → LCDVCC

C38 *0.1u/16V_4, C33 *2.2u/10V_8, C40 0.1u/16V_4, C39 0.01u/50V_4, C34 22u/6.3V_8

EDP_VDD_EN → R48 *short_4 → EDP_VDD_EN_R → R37 100K_4

Touch screen level shift I2C(reserve)

+3V → R35 *TSI@0_4 → Q4 *TSI@2N7002DW → R22 *TSI@0_4

R27 *TSI@10K_4, R26 *TSI@10K_4

I2C1_SDA, I2C1_SCL → I2C1_SDA_C, I2C1_SCL_C

S5

S0

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10-100u =2.4-0.4k.
100Khz 10-100u=9k-1k.

+3VPCU → R10 *100K_4 → LID# → LID# 37
LID591#,EC intrnal PU

+3V → R7 10K_4, R9 10K_4 → D1 1N4148WS → BL_ON

PCH_BLON → R4 *short_4 → PCH_BLON_R
PCH_BLON_EC → R3 *short_4
R2 100K_4

Q1 2N7002DW — BL# — Q3 DTC144EUA → EC_FPBACK# 37

1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

Hall Sensor (HSR)

+3VPCU → R449 *100K_4 → R445 *SHORT_6 → MR1 AH9249NTR-G1 → LID#

D22 *VPORT_6
C658 4.7U/10V_6
D23 *VPORT_6

1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

PROJECT :ZRY
Quanta Computer Inc.

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	CRT/LVDS/CAMERA/LID	1A
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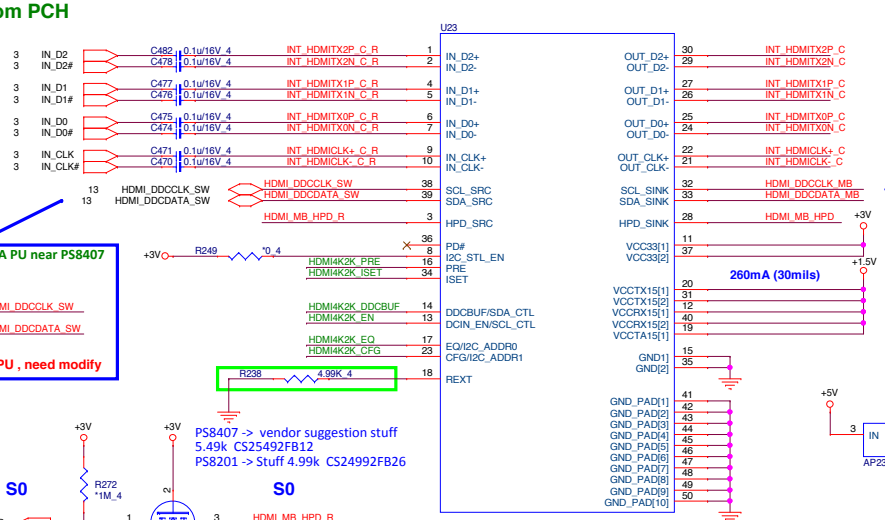
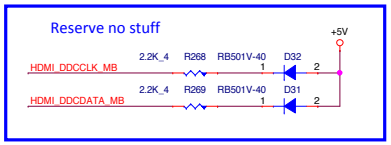
From PCH



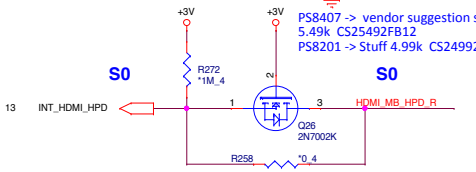
Reserve no stuff



DDCCLK & DDCDATA PU near PS8407

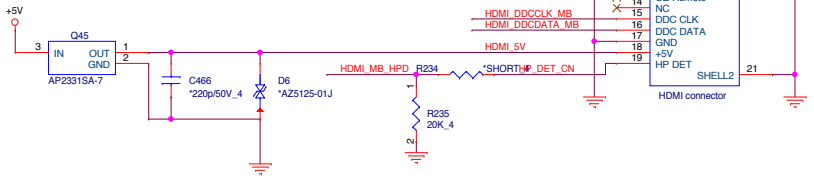
PS8407 internal have PU , need modify

HDMI-detect

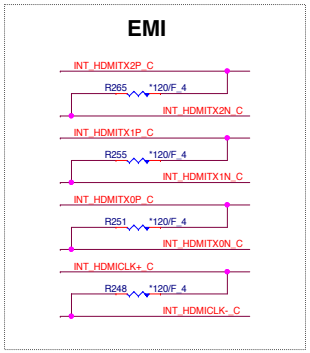


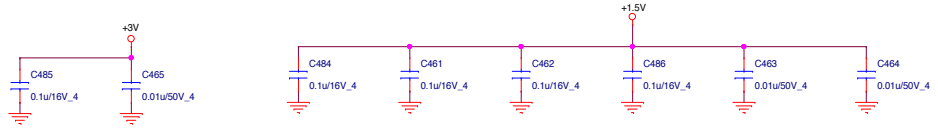
PS8407 -> vendor suggestion stuff
5.49k CS25492FB12
PS8201 -> Stuff 4.99k CS24992FB26

HDMI connector

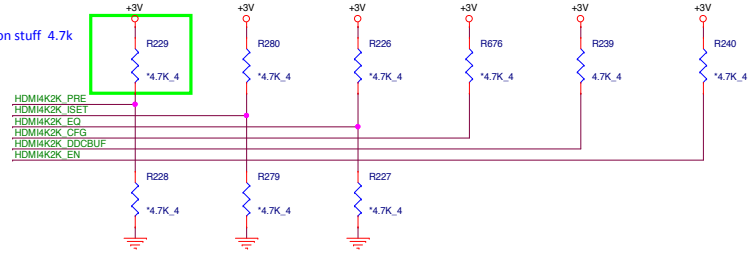


EMI





PS8407 ->vendor suggestion stuff 4.7k
CS24702JB38
PS8201 -> No stuff

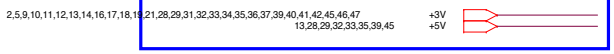


	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

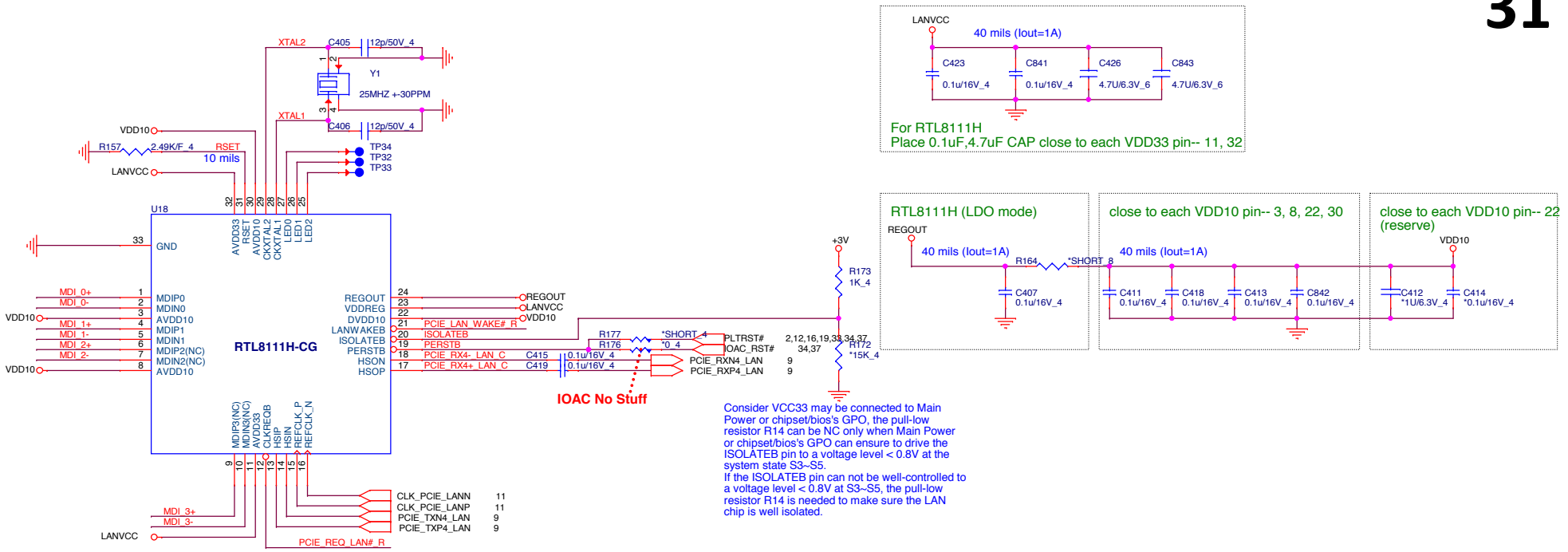
Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

Power trace tracking



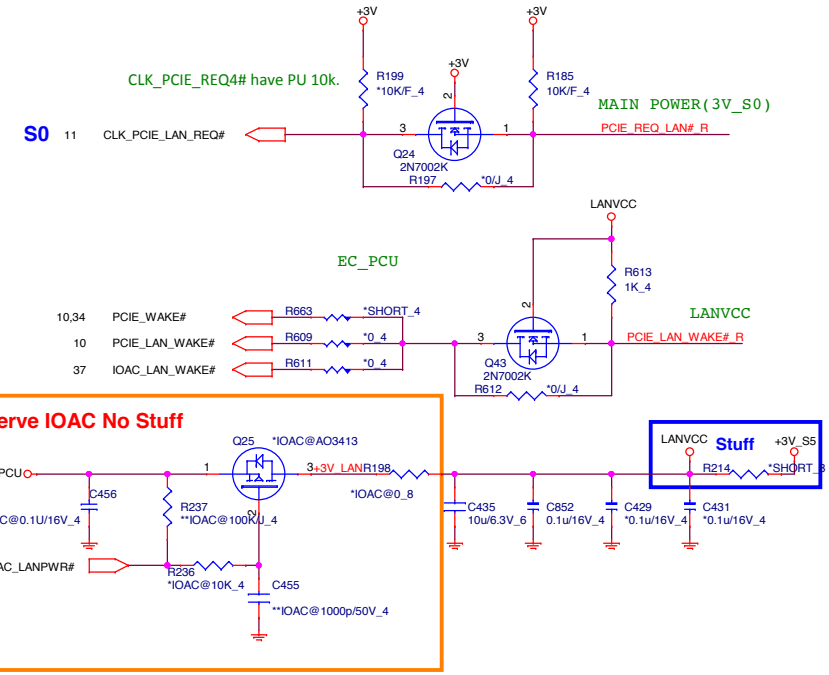
Giga LAN (LAN)



Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S3~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

For RTL8111H
Place 0.1uF,4.7uF CAP close to each VDD33 pin-- 11, 32

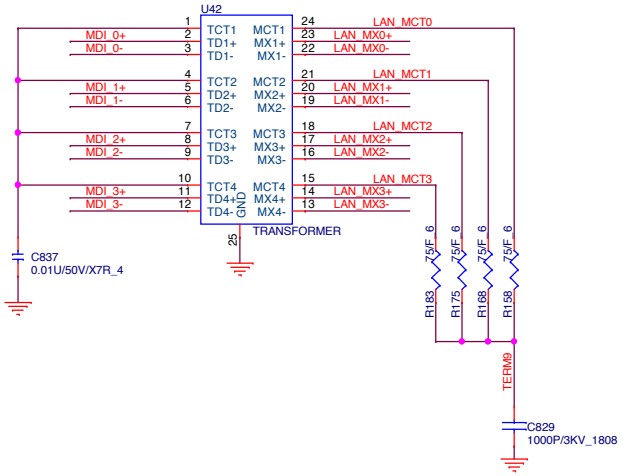
Leakage circuit (MPC)



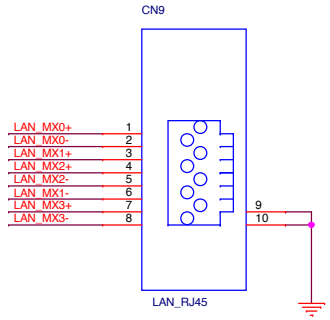
Reserve IOAC No Stuff

Tramsformer

Layout:All termination signal should have 30 mil trace



RJ45 Connector



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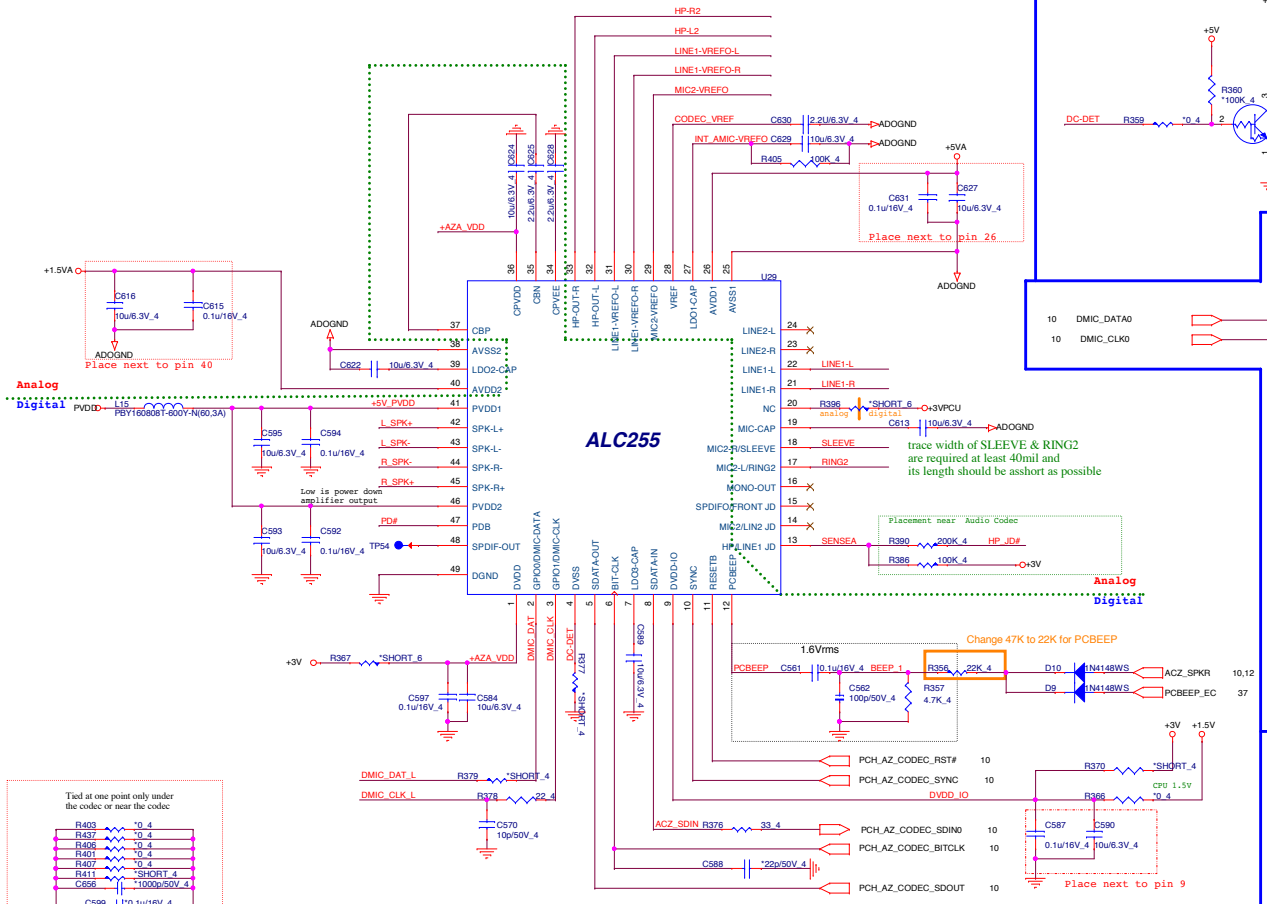
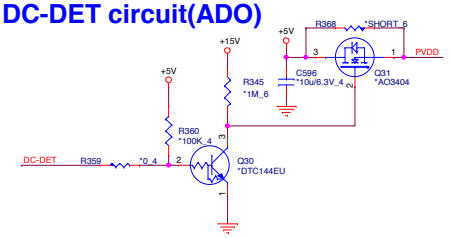
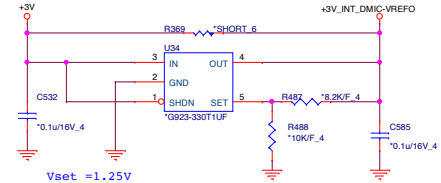
Codec(ADO)



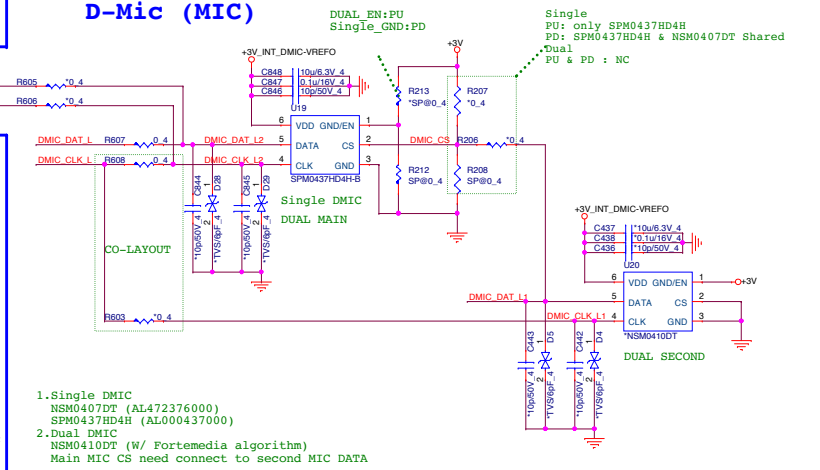
DC-DET circuit(ADO)



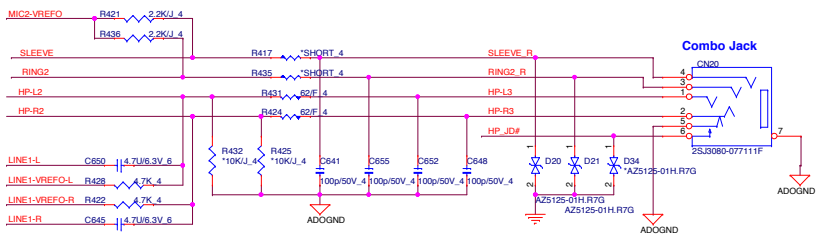
Power (ADO)



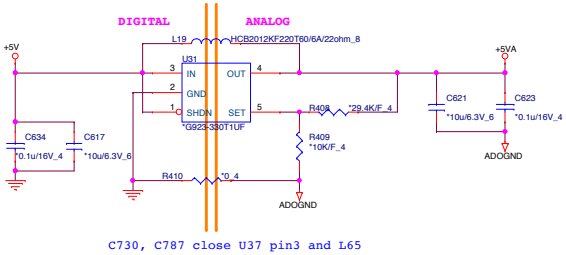
D-Mic (MIC)



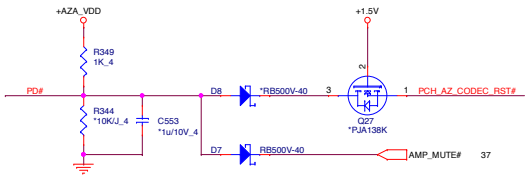
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



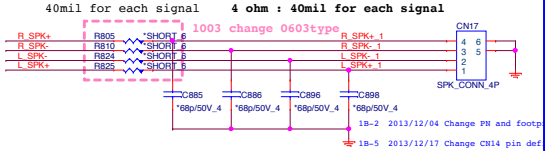
Codec PWR 5V(ADO)



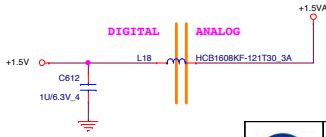
Mute(ADO)



Internal Speaker



Codec PWR 1.5V(ADO)



PROJECT :ZRY		
Quanta Computer Inc.		
Size	Document Number: ALC255/HP/SPK	Rev: 1A
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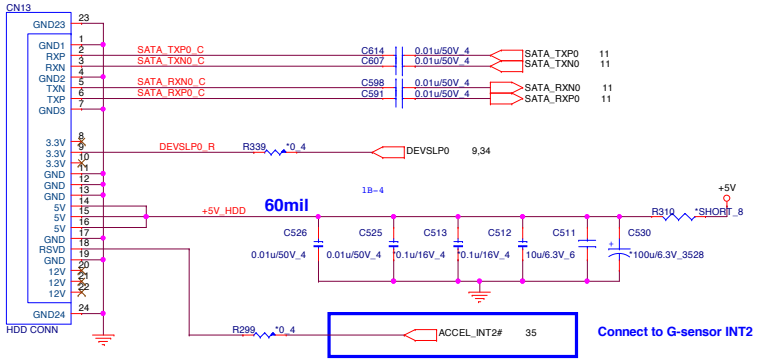
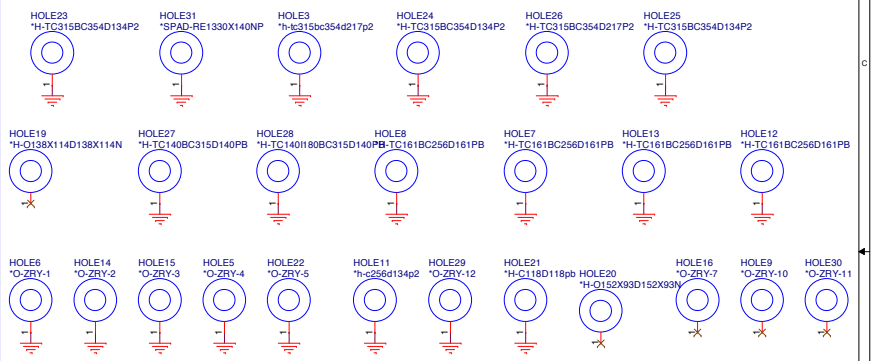
2.5" SATA HDD (HDD)



SATA ODD Connector(Remove)

33

ODD Power (SATA)(Remove)

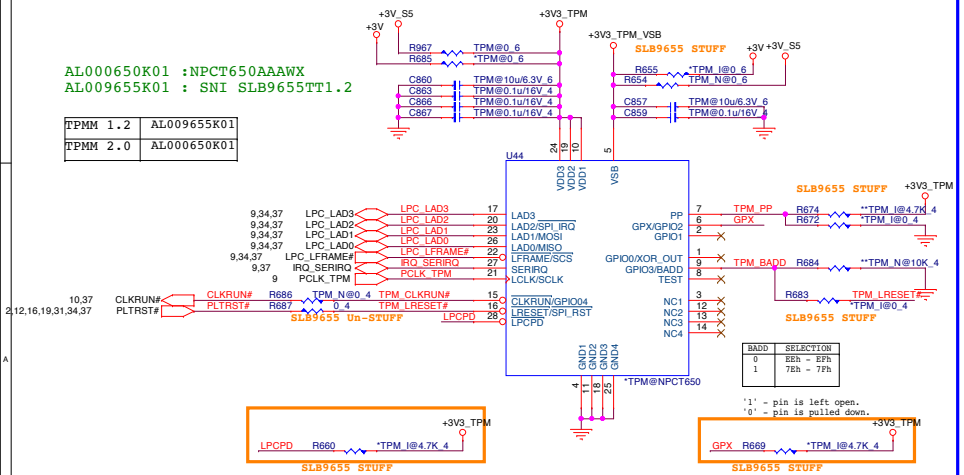


TPM NPCT650 (TPM)

SP@ BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAWX)

AL000650K01 :NPCT650AAAWX
AL009655K01 : SNI SLB9655TT1.2

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01



Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	1A
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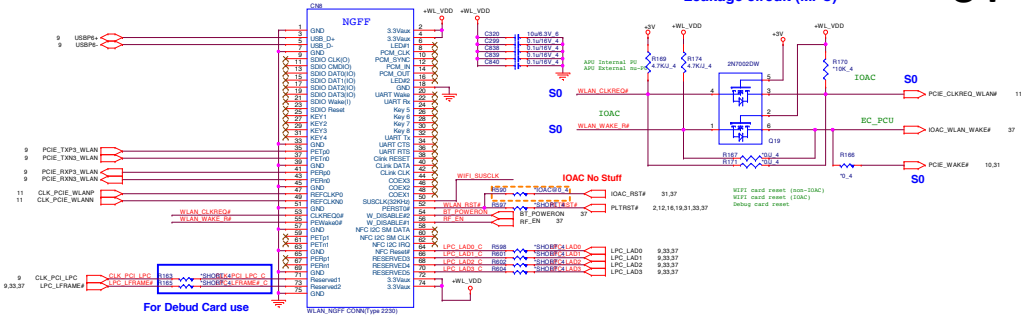
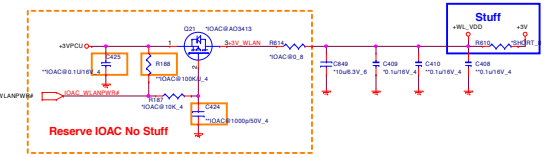
PROJECT :ZRY
Quanta Computer Inc.

NGFF_M.2 WiFi & BT (NGF)

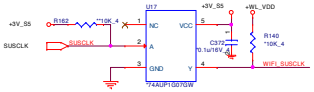
Leakage circuit (MPC)

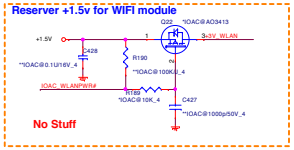


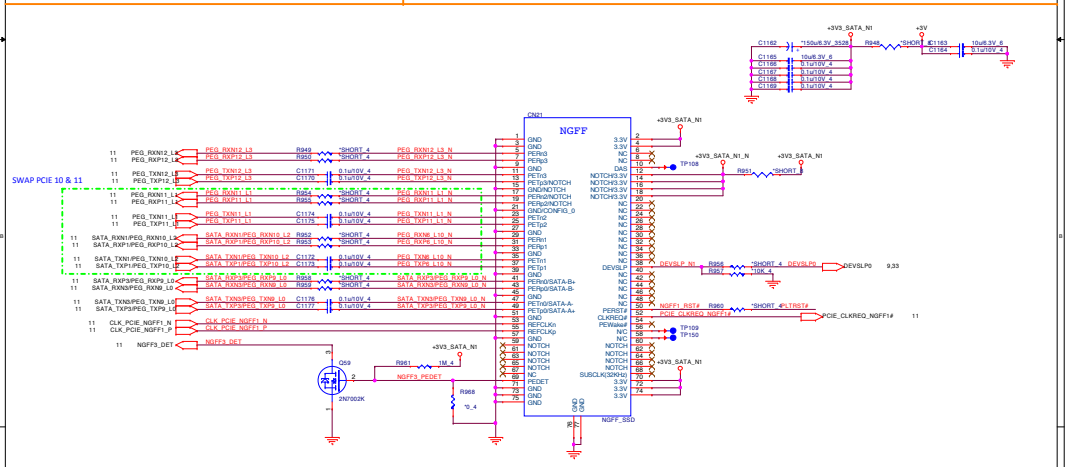
Low	Mini card +3V power enable
High	Mini card +3V power disable



Reserve only for Intel module no need to stuff by default 11/24

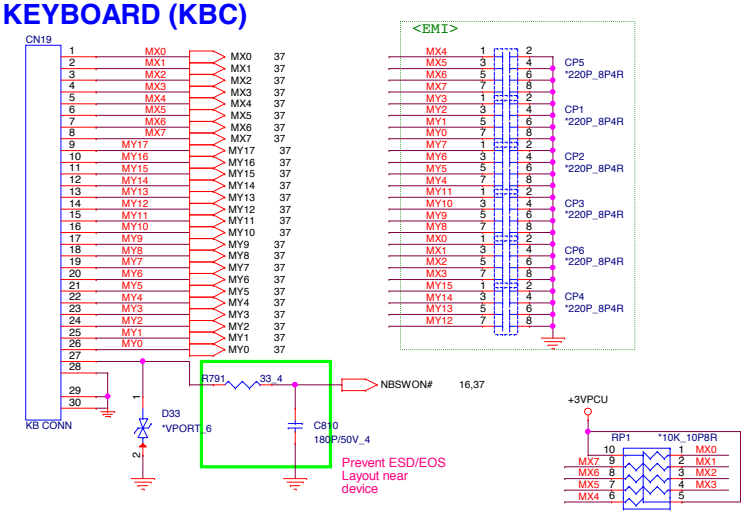




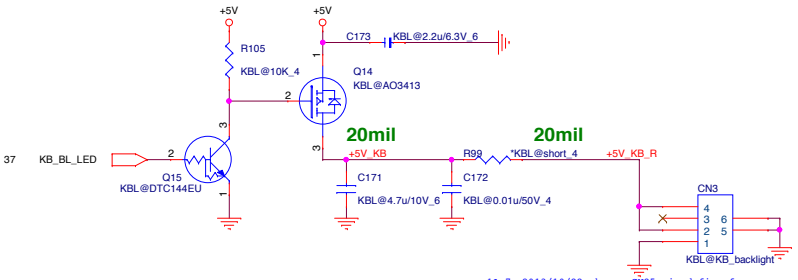


PROJECT :	ZRY
Quanta Computer Inc.	
Size	Document Number: Mini-Card/WL/3G/SIM — Rev: 1A
Date: Monday, September 07, 2015	Sheet 34 of 49

KEYBOARD (KBC)



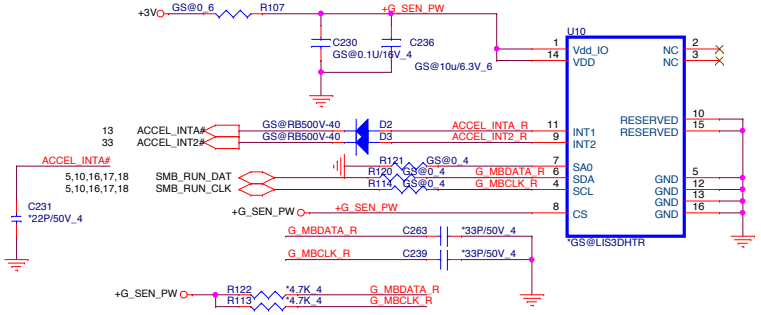
KB_BL LED (KBC)



1A-7 2013/10/22 change CN25 pin define for spec.

1A-8 2013/10/23 change CN25 footprint.

G-sensor(ACS)



TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

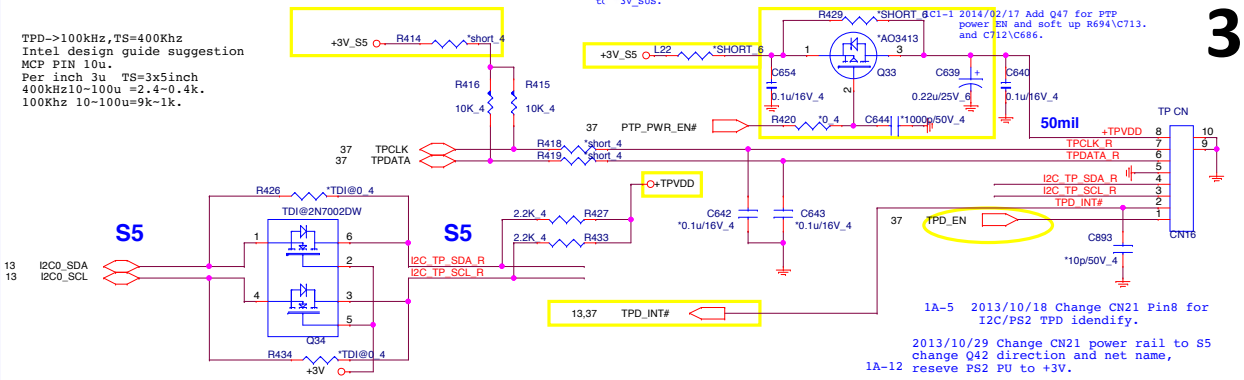
1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.

1C-4 2014/01/15 reserve TP power rail +3V_S5.

1C-1 2014/02/17 Add Q47 for PTP power EN and soft up R694\C713. and C712\C686.

35

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.

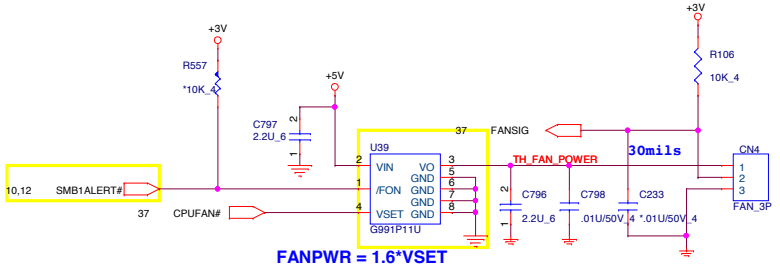


1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.

2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,

1A-12 reseve PS2 PU to +3V.

CPU FAN (THM)



FANPWR = 1.6*VSET

1A-1 2013/10/15 change pin define and add pwm IC U17.

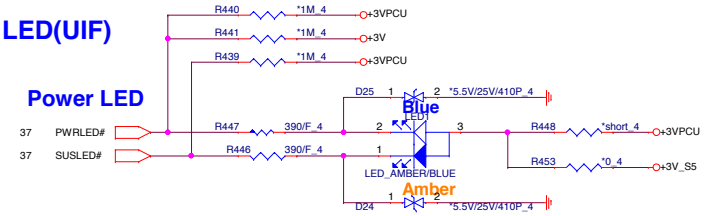
1A-4 2013/10/17 Change U17 to G991P11U and PU U17 pin1.

1A-9 2013/10/24 Add alert on U17.1 for CPU themal tempture.

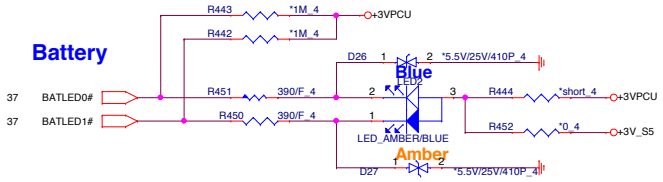
1A-13 2013/10/31CN15 Pin2/3 swap.

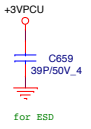
POWER LED(UIF)

Power LED



Battery





PROJECT :ZRY		
Quanta Computer Inc.		
Size	Document Number: KB/TP/FAN	Rev: 1A
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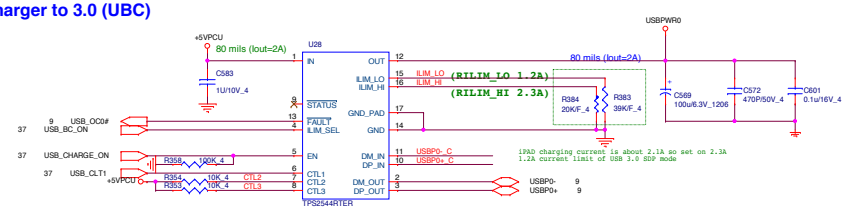
USB Charger to 3.0 (UBC)



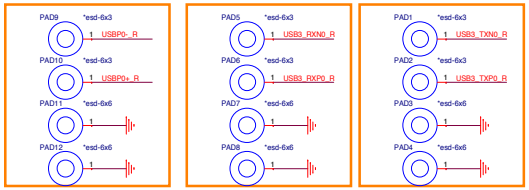
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

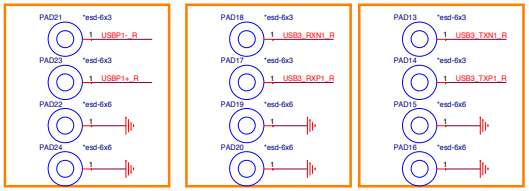
$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

GMT:AL003703000(G3703)
TI:AL002544001(TPS2544)
Silergy:

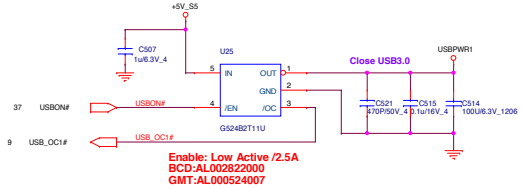
USB 3.0 Connector (UB3)

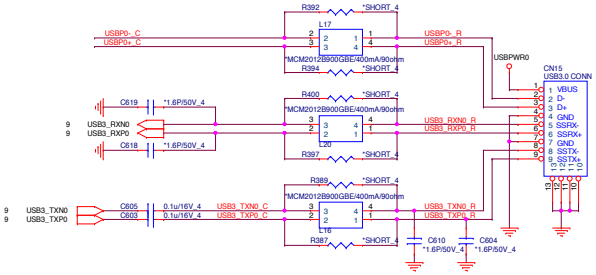


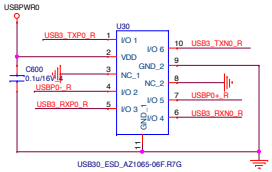
0722 Added PAD1-4
as ESD protection



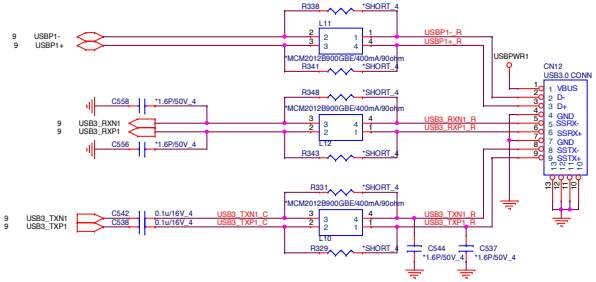
0722 Added PAD1-4
as ESD protection

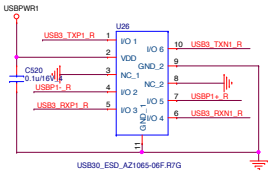






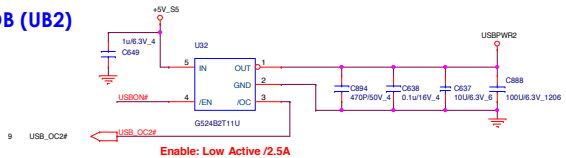
USB protection diodes for ESD.
as close as possible to USB connector pins.

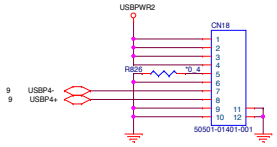




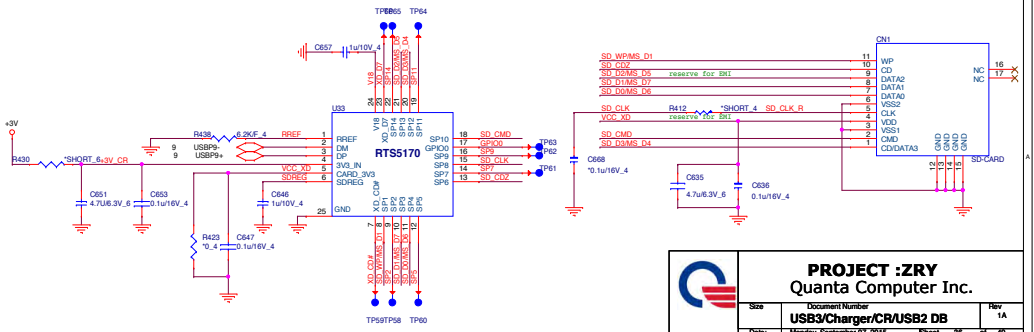
USB protection diodes for ESD.
as close as possible to USB connector pins.

USB2.0 DB (UB2)

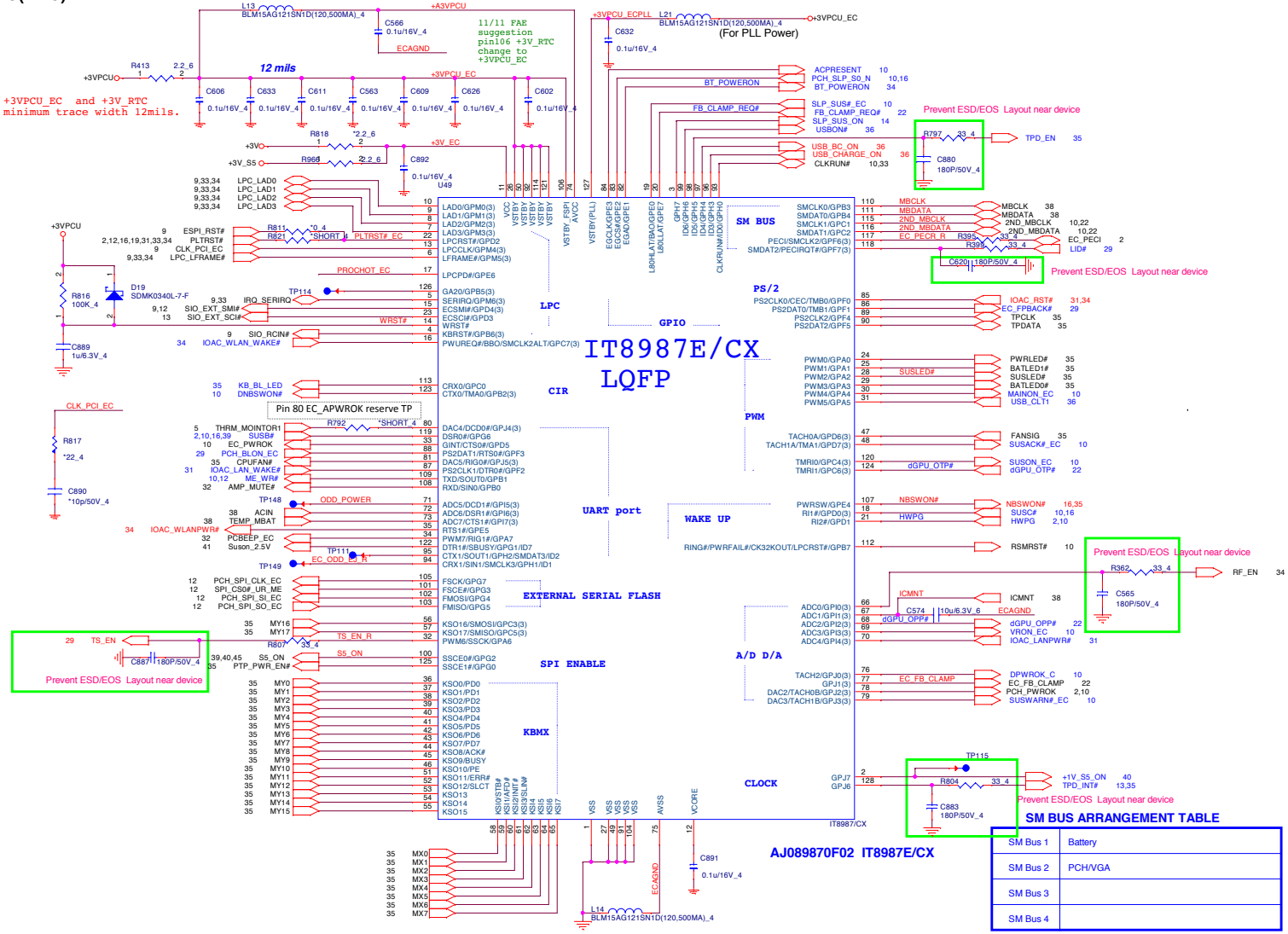




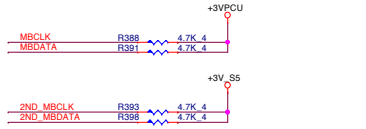
Card Reader (CRD)

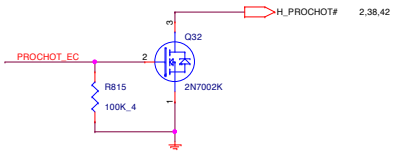


EC(KBC)



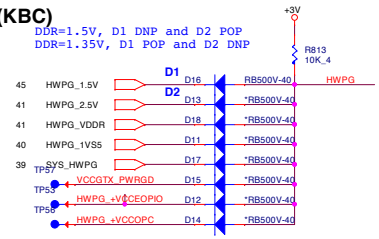
SM BUS PU(KBC)





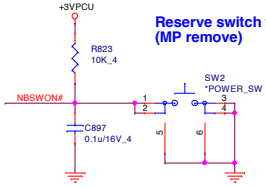
HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP

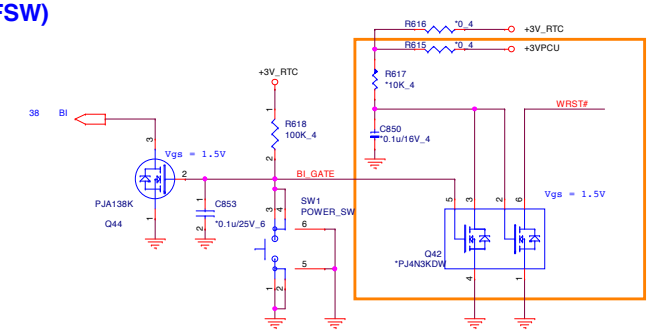


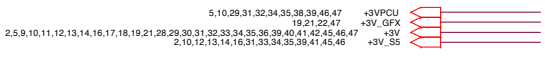
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	



Reset SW (FSW)





PROJECT :ZRY Quanta Computer Inc.			
Size	Document Number KBC IT8587		Rev 1A
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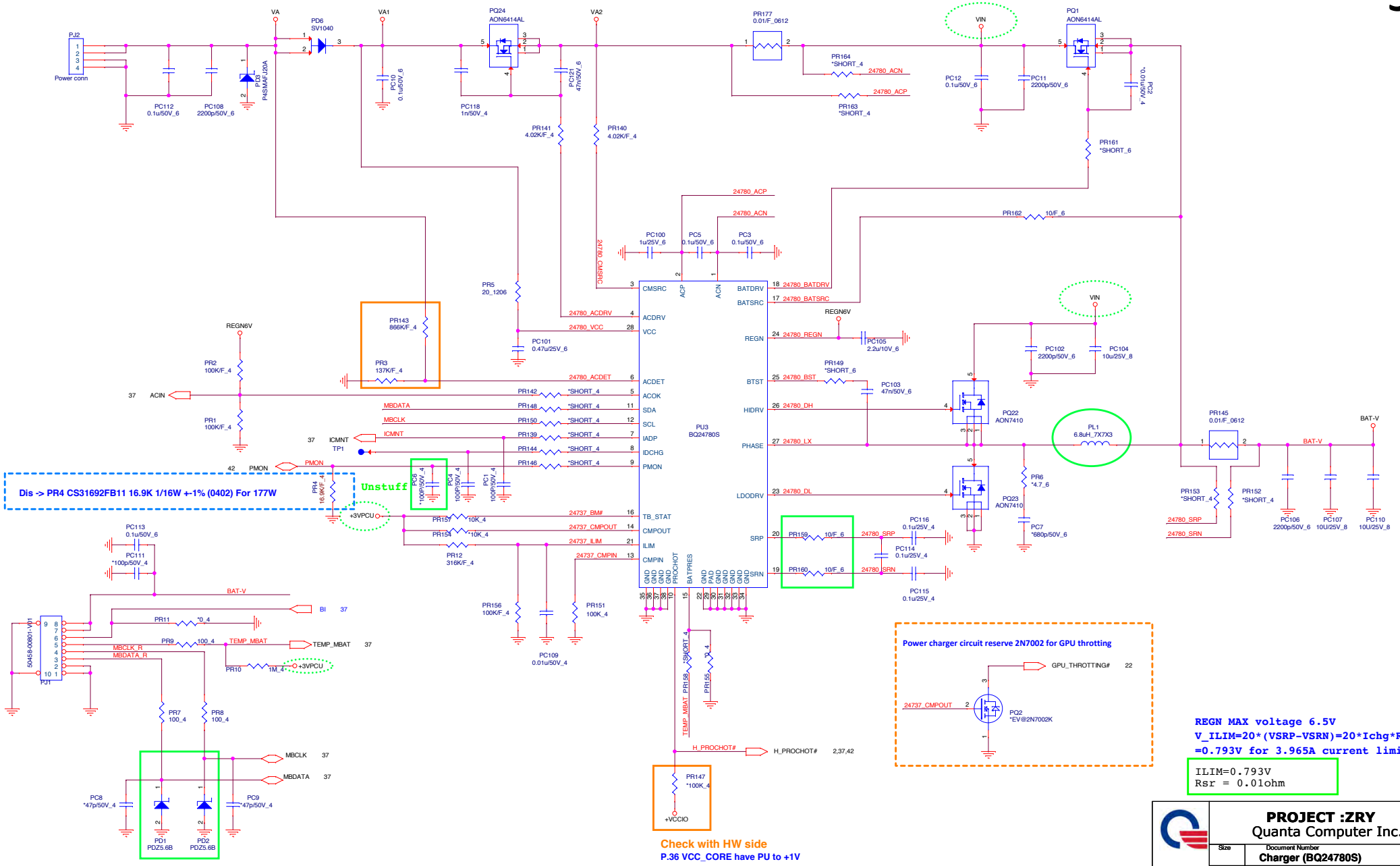
Dis -> PR4 CS31692FB11 16.9K 1/16W +-1% (0402) For 177W
Unstuff
Power charger circuit reserve 2N7002 for GPU throtting
Check with HW side
P.36 VCC_CORE have PU to +1V
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
PROJECT :ZRY
Quanta Computer Inc.
Charger (BQ24780S)
Monday, September 07, 2015
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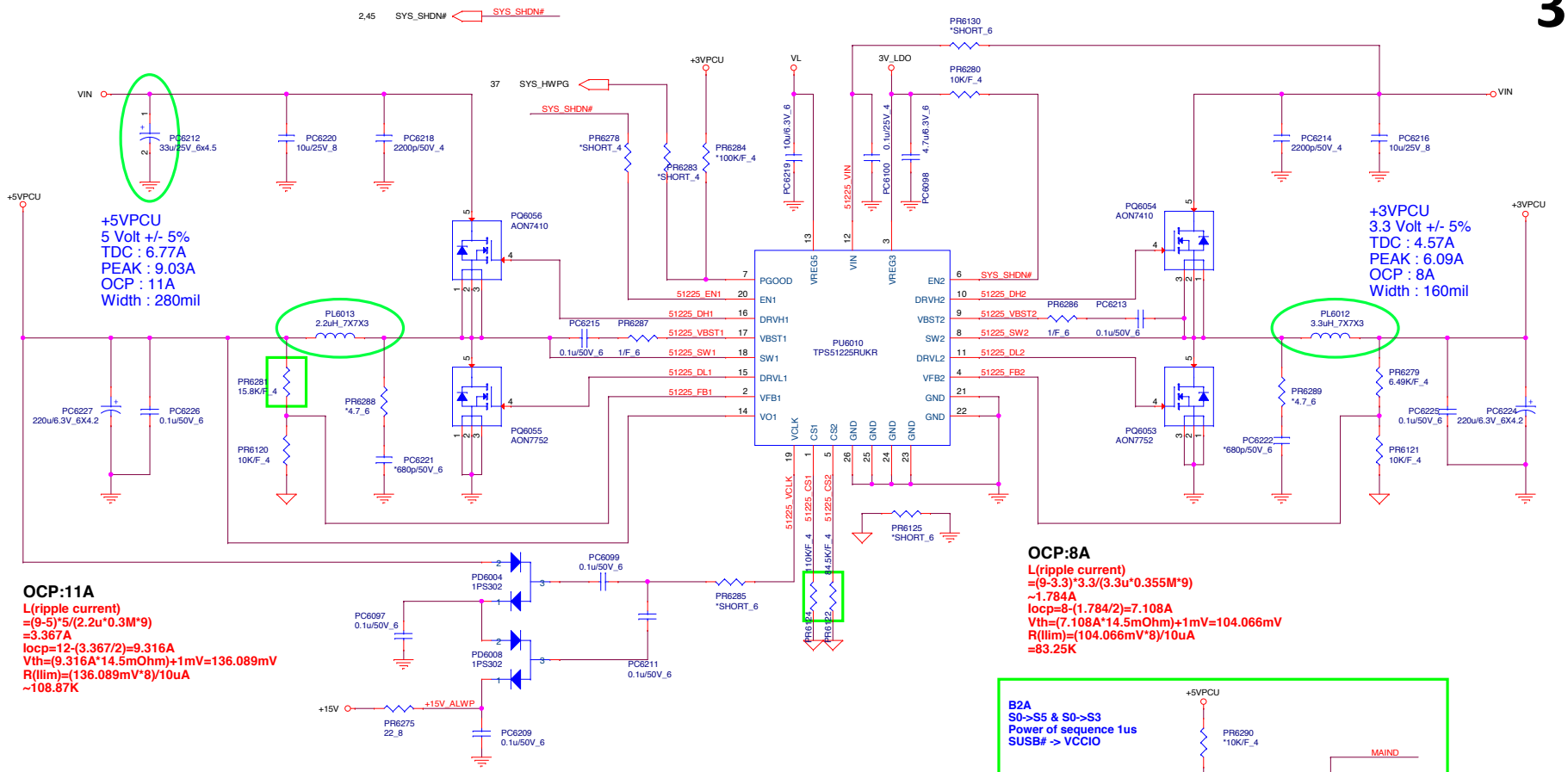

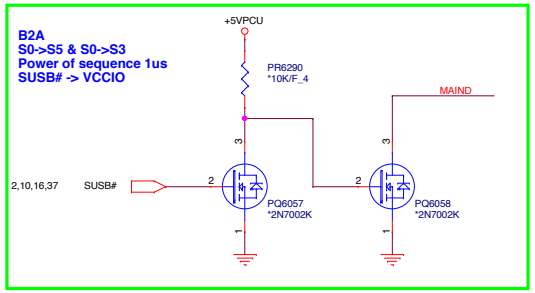

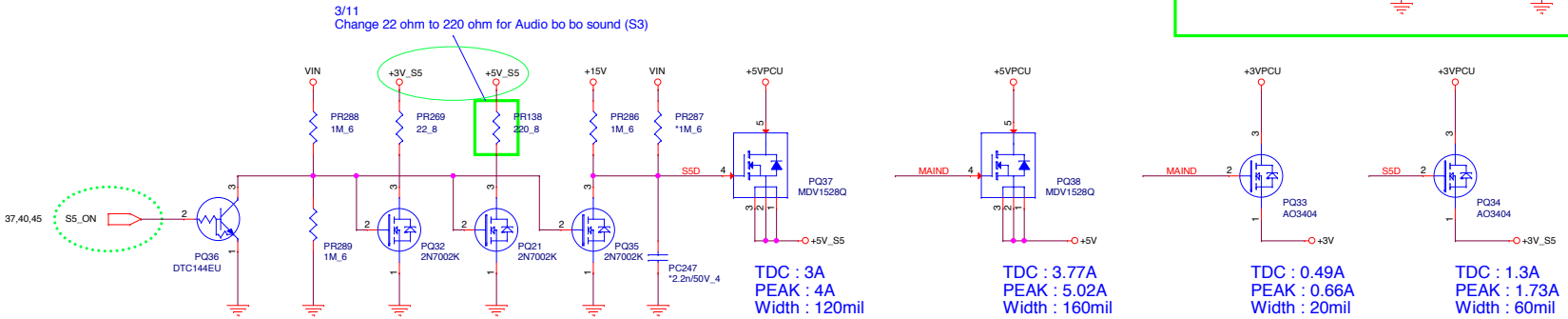

PROJECT :ZRY Quanta Computer Inc.			
Size	Document Number: SYSTEM 5V/3V (TPS51225)		Rev: 1A
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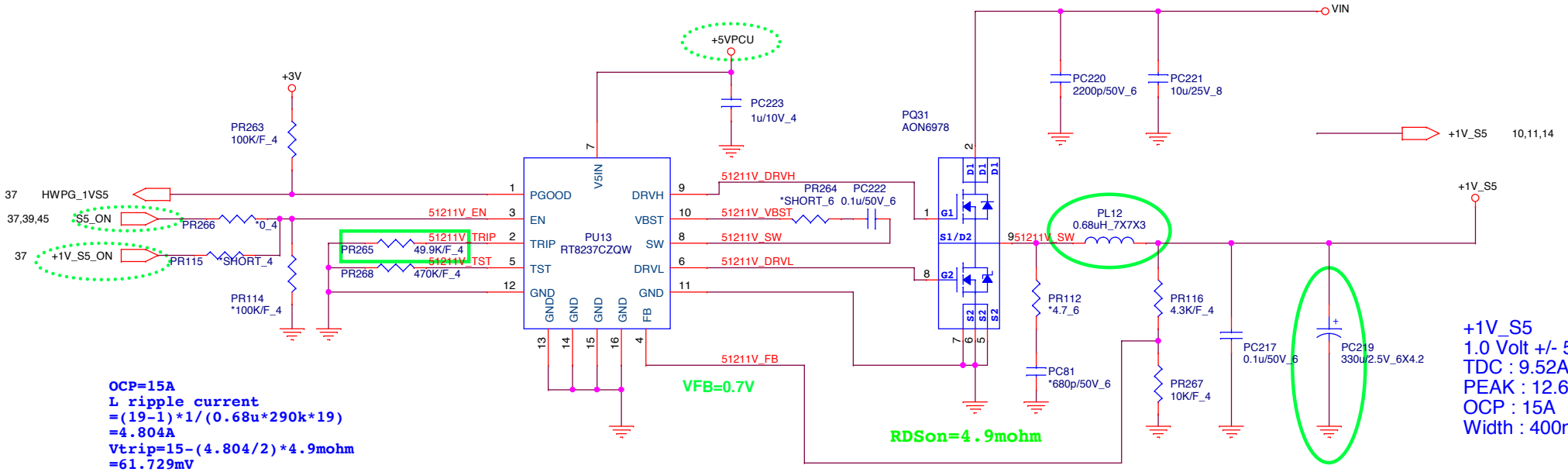
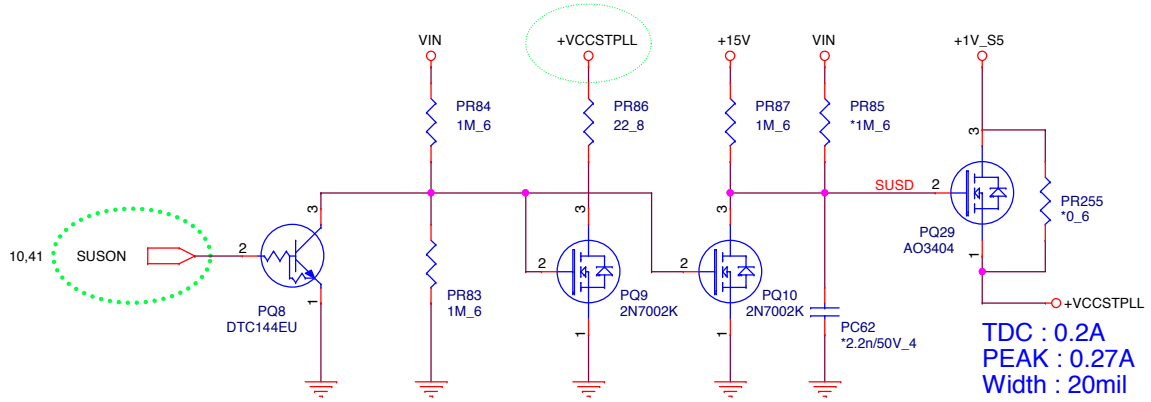
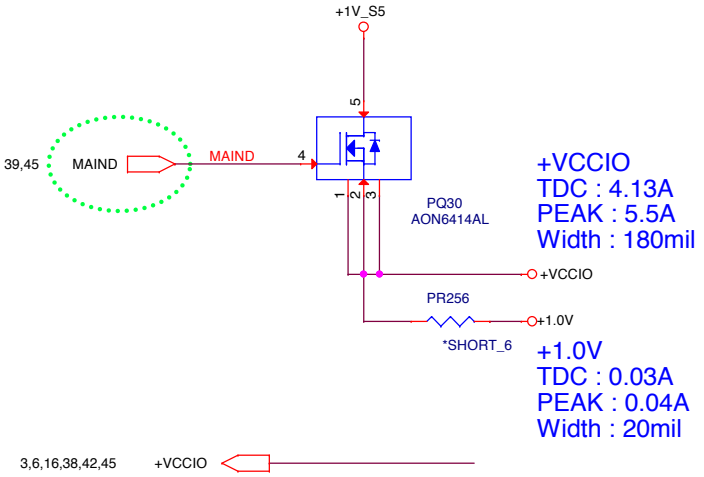


OCP=15A
L ripple current
=(19-1)*1/(0.68u*290k*19)
=4.804A
Vtrip=15-(4.804/2)*4.9mohm
=61.729mV
Rlimit=61.729mV/10uA*8=49.383Kohm

+1V_S5
1.0 Volt +/- 5%
TDC : 9.52A
PEAK : 12.69A
OCP : 15A
Width : 400mil



TDC : 0.2A
PEAK : 0.27A
Width : 20mil



+VCCIO
TDC : 4.13A
PEAK : 5.5A
Width : 180mil

+1.0V
TDC : 0.03A
PEAK : 0.04A
Width : 20mil

PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
	+1V_S5 (RT8237CZQW)	1A
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TDC : 0.45A
PEAK : 0.6A
Width : 40mil

DDR_VTTREF

4/16 Chaneg +VDDQ_VTT to DDR_VTTREF

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+VDDQ

PC258 10u/6.3V_6
PC257 10u/6.3V_6
PC263 0.22u/10V_4

Close to IC

Greater than or equal 40mil

+5VPCU

PC252 10u/6.3V_6
PC259 1u/10V_4

+3V

PR295 100K/F_4

PU17
G5316RZ1D

PAD PAD VTTREF VTTGND VTTSNS VTT VLDOIN

PGOOD S3 S5 MODE TRIP PAD

REF REFIN VDDQSNS PAD PAD PAD GND

VSIN DRVH VBST SW DRVL PGND

37 HWPG_VDDR
10,45 MAINON
10,40 SUSON

PR292 *SHORT_4 51216_S3
PR291 *SHORT_4 51216_S5
PR294 200K/F_4 51216_MODE
PR293 110K/F_4 51216_TRIP

51216_DRVH 51216_VBST 51216_SW 51216_DRVL

PR297 2/F_6
PC256 0.1u/50V_6

PQ39 AON7410
PQ40 AON7752

VIN

PC254 2200p/50V_4
PC253 10u/25V_8

PL16 1uH_7X7X3

51216_SW

+1.2VSUS
1.2 Volt +/- 5%
TDC : 6.6A
PEAK : 8.8A
OCP : 11A
Width : 280mil

+1.2VSUS
+1.2VSUS 2,6,10,17,18

PC260 0.1u/50V_6
PC255 330u/2.5V_6X4.2

RDSon=14.5mohm

Close to output cap

VREF=1.8V

51216_REF
PC262 0.1u/16V_4
PR299 10K/F_4
51216_REFIN

51216_S3 PR296 *0_4 51216_S5

PR300 20K/F_4
PC261 0.01u/50V_4

17 DDR_VTTT_PG_CTRL
PR290 *0_4 51216_S3

PR298 *SHORT_6

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

OCP=11A
L ripple current
=(19-1.2)*1.2/(1u*400k*19)
=2.81A
Vtrip=11-(2.81/2)*14.5mohm
=139.123mV
Rlimit=139.123mV/10uA*8=111.29Kohm

DDR4=1.2V
PR299=10K/F_4
PR300=20K/F_4

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

4/16 Chaneg DDR3L to DDR4
Adding +2.5V Power Rail

+2.5V_SUS 17,18

+3V_S5
PR285 *SHORT_6
PC243 4.7U/6.3V_6

+2.5V_SUS
2.5Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

PU15
APW8824

PG VIN LX EN GND FB

37 HWPG_2.5V
PR301 *SHORT_4

SUSON
PR304 *0_4
PR271 10K_4

37 Suson_2.5V
PR303 *SHORT_4

PC234 0.47uF/4V_4

8824LY-2.5V
PL15 2.2uH/1.85A_2.5X2X1.2

PR275 *SHORT_4
PC228 10U/6.3V_6
PC231 *10U/6.3V_6
PC232 0.1U/16V_4

R1
PR278 47.5K/F_4
R2
PR302 15K/F_4

Vo=(0.6(R1+R2)/R2)

PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
	DDR4 1.2V (G5316RZ1D)	1A
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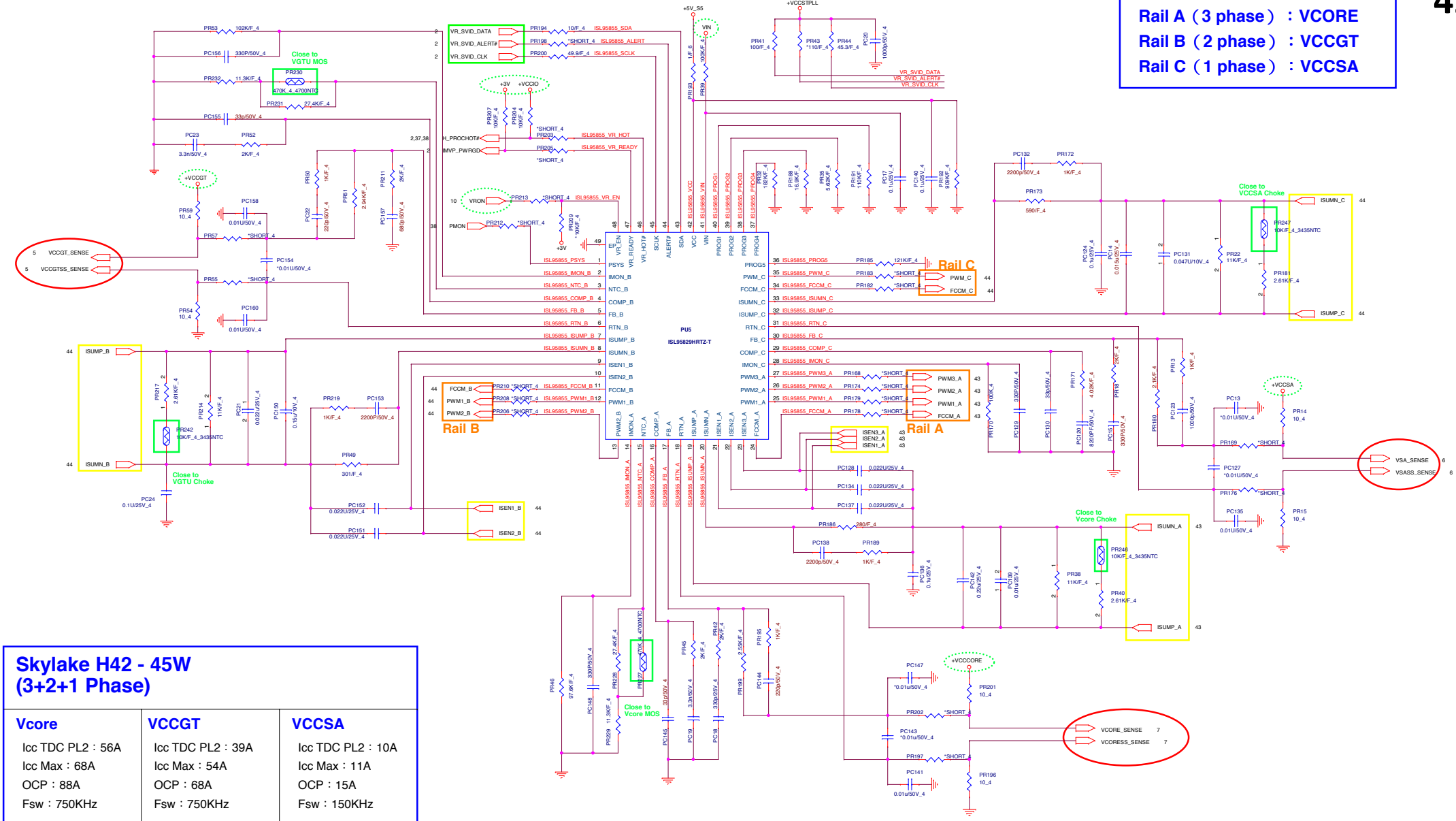
Rail A（3 phase）：VCORE
Rail B（2 phase）：VCCGT
Rail C（1 phase）：VCCSA



Skylake H42 - 45W (3+2+1 Phase)

Vcore	VCCGT	VCCSA
Icc TDC PL2：56A	Icc TDC PL2：39A	Icc TDC PL2：10A
Icc Max：68A	Icc Max：54A	Icc Max：11A
OCP：88A	OCP：68A	OCP：15A
Fsw：750KHz	Fsw：750KHz	Fsw：150KHz
VCORE L/L：	**VCORE L/L：**	**VCORE L/L：**
R_DC_LL：1.8mV/A	R_DC_LL：2.65mV/A	R_DC_LL：9.1mV/A
R_AC_LL：1.8mV/A	R_AC_LL：2.65mV/A	R_AC_LL：9.1mV/A

PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE (ISL95855HRTZ-T)	1A
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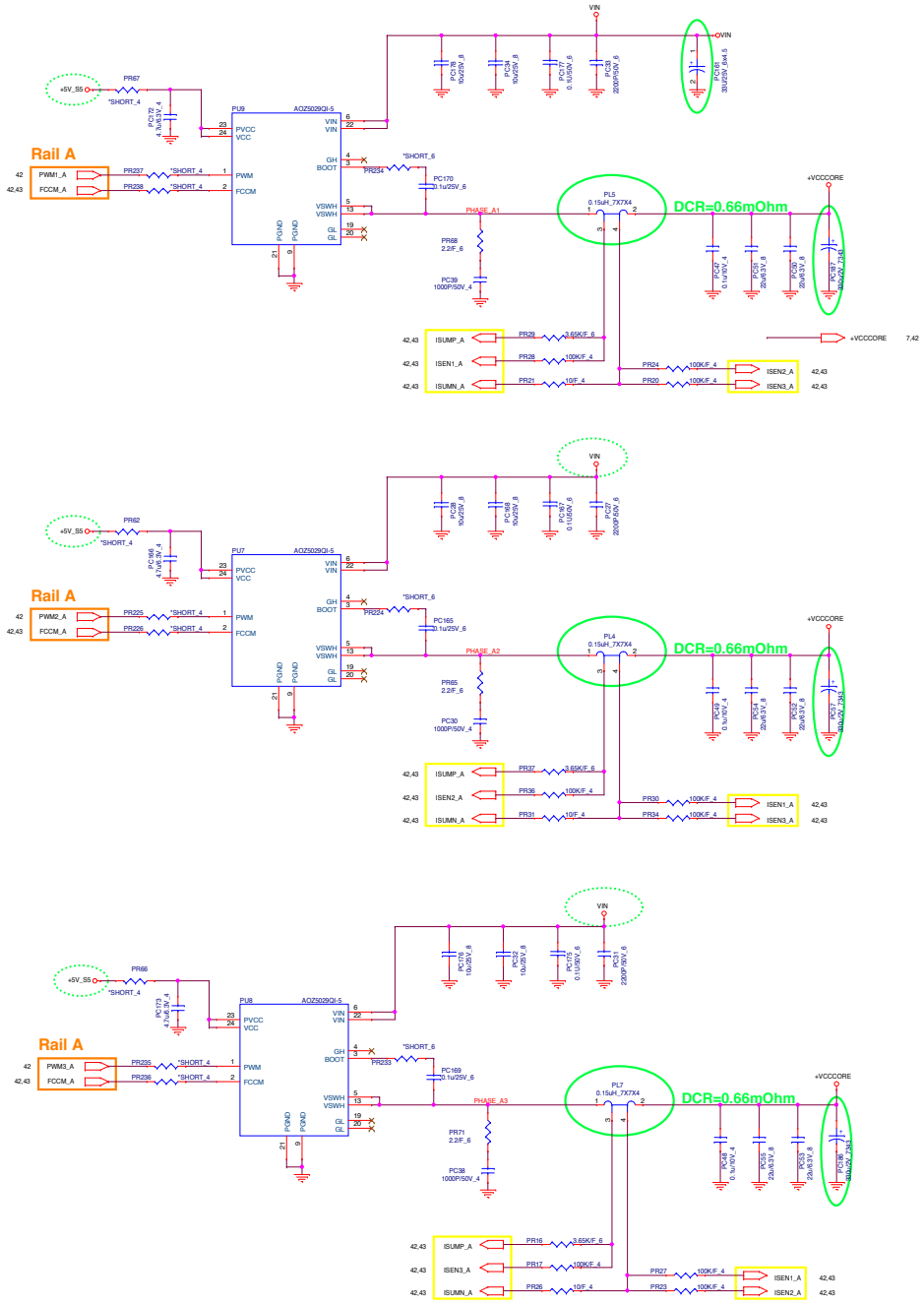
VCORE-3 phase



Vcore

Icc TDC PL2：56A

Icc Max：68A

OCP：A

Fsw：MHz

VCORE L/L :

R_DC_LL：1.8mV/A

R_AC_LL：1.8mV/A

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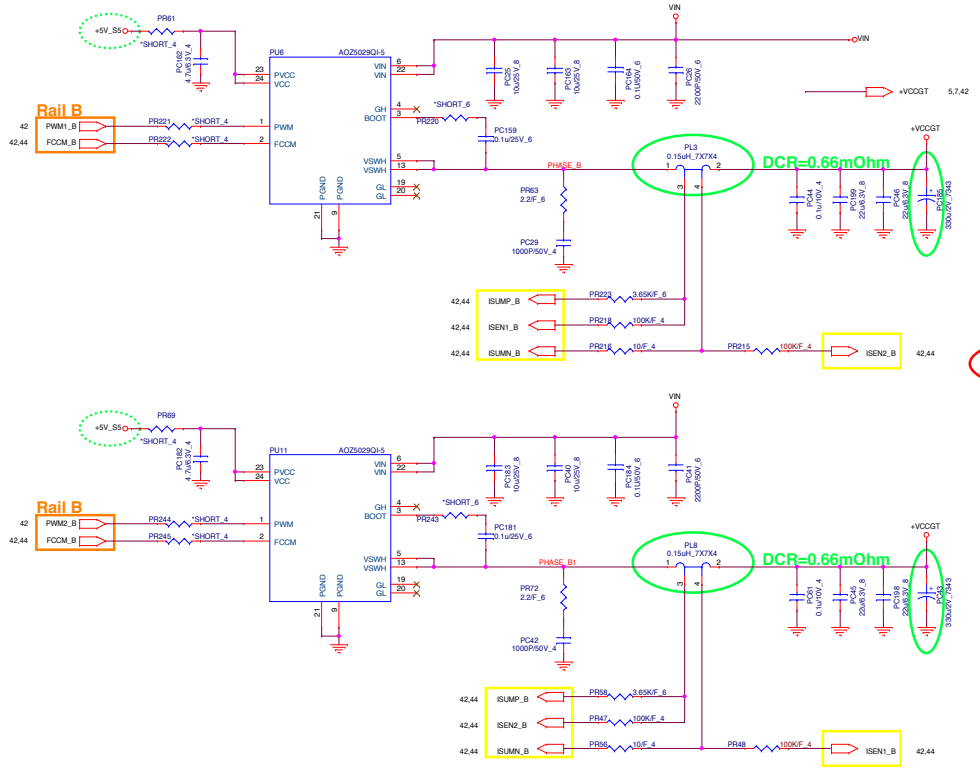
VCCGT-2 phase



VCCGT

Icc TDC PL2：39A

Icc Max：54A

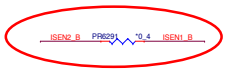
OCP：A

Fsw：MHz

VCORE L/L：

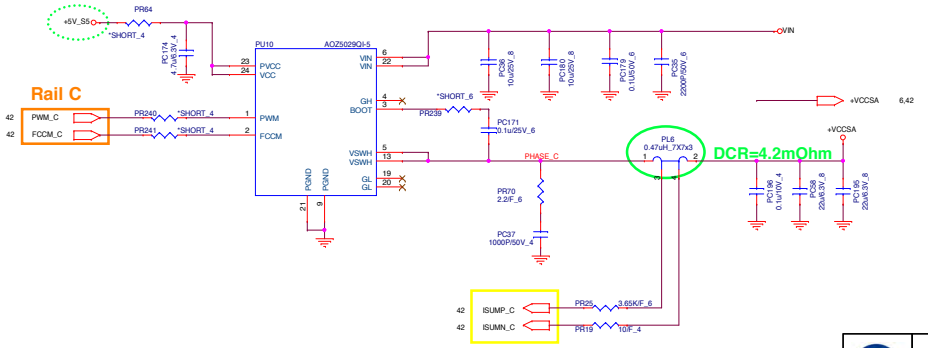
R_DC_LL：2.65mV/A

R_AC_LL：2.65mV/A



8/24 reserve the GT short-circuit

VCCSA-1 phase



VCCSA

Icc TDC PL2：10A

Icc Max：11A

OCP：A

Fsw：MHz

VCORE L/L：

R_DC_LL：9.1mV/A

R_AC_LL：9.1mV/A

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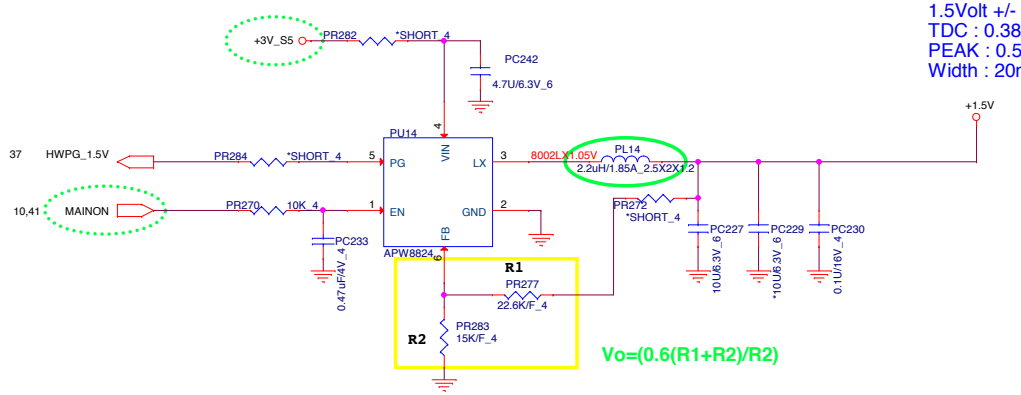
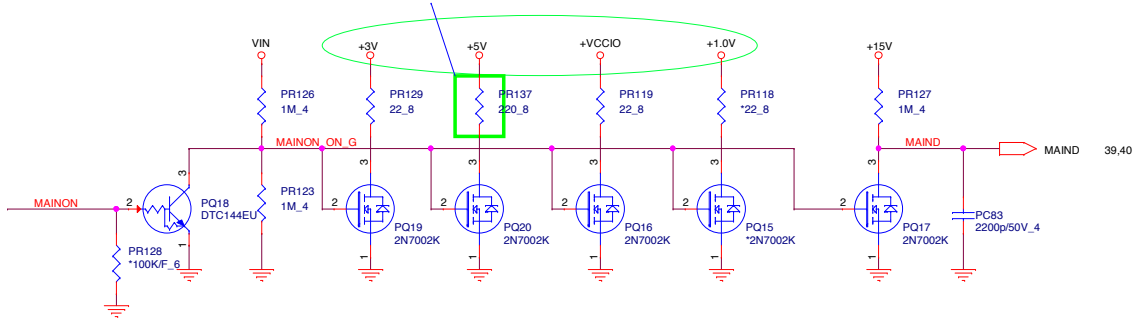
Remove 1.8V

+1.5V 14,30,32,34

+1.5V
1.5Volt +/- 5%
TDC : 0.38A
PEAK : 0.51A
Width : 20mil



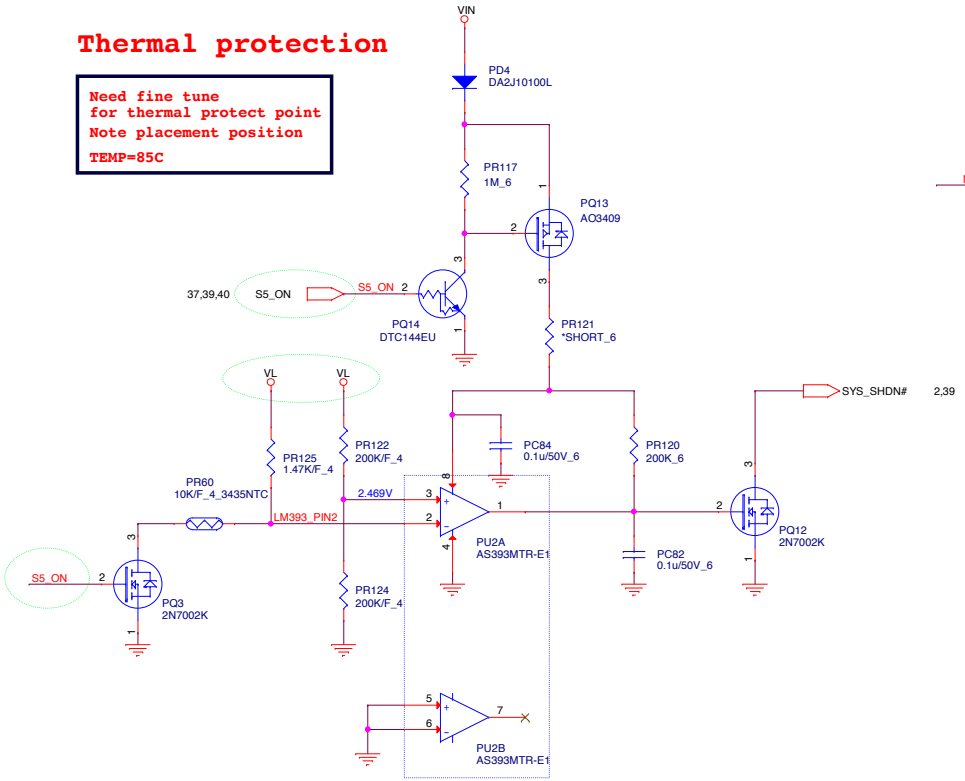
3/11
Change 22 ohm to 220 ohm for Audio bo bo sound (S3)



Thermal protection

Need fine tune
for thermal protect point
Note placement position

TEMP=85C



For EC control thermal protection (output 3.3V)

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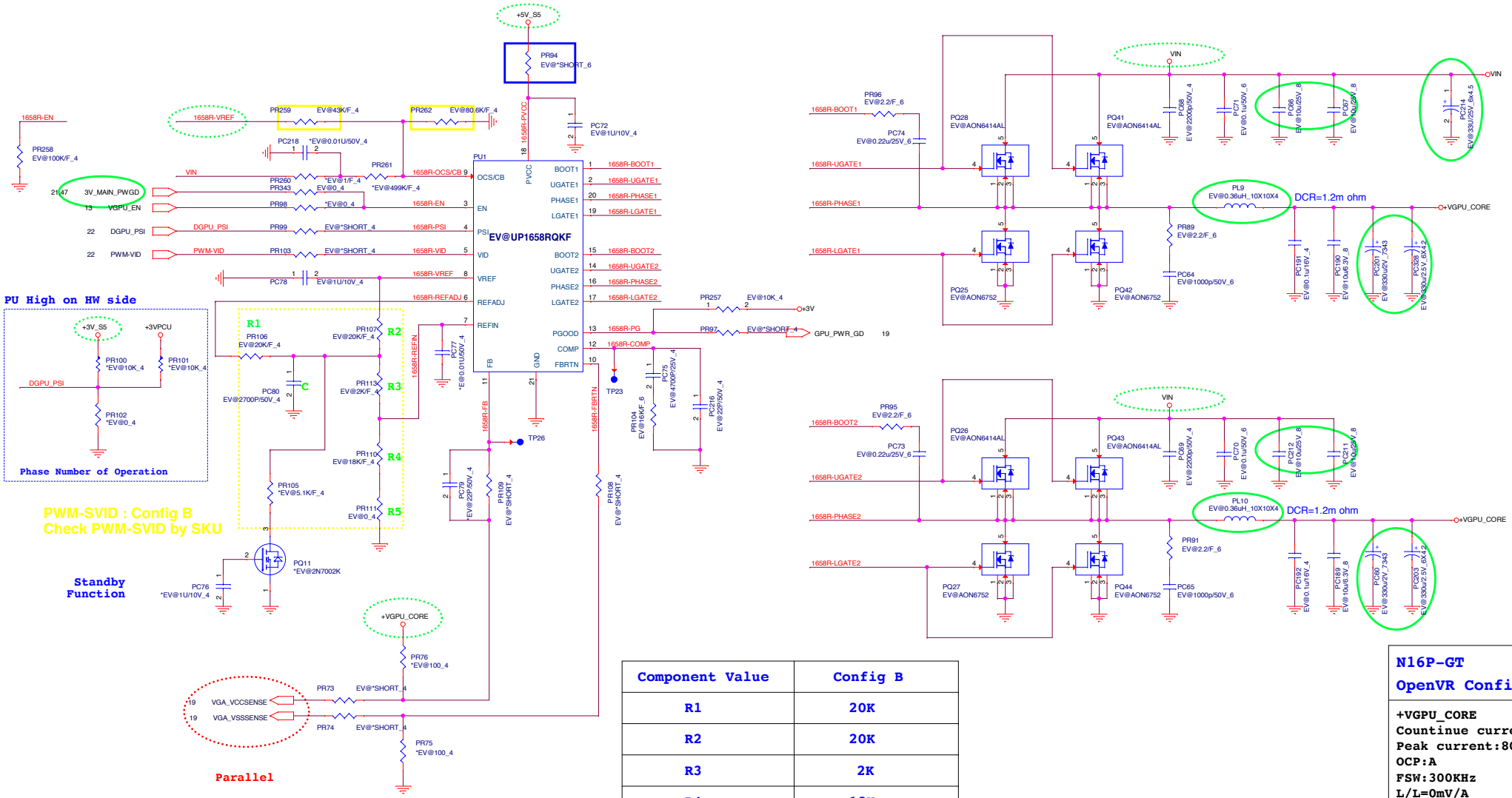

Component Value	Config B
R1	20K
R2	20K
R3	2K
R4	18K
R5	0-ohm
C	2.7nF

N16P-GT

OpenVR Config:B

+VGPU_CORE
Countinue current:42.2A
Peak current:80A
OCP:A
FSW:300KHz
L/L=0mV/A

PROJECT :ZRY
Quanta Computer Inc.

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	+VGPU_CORE (UP1658)	1A
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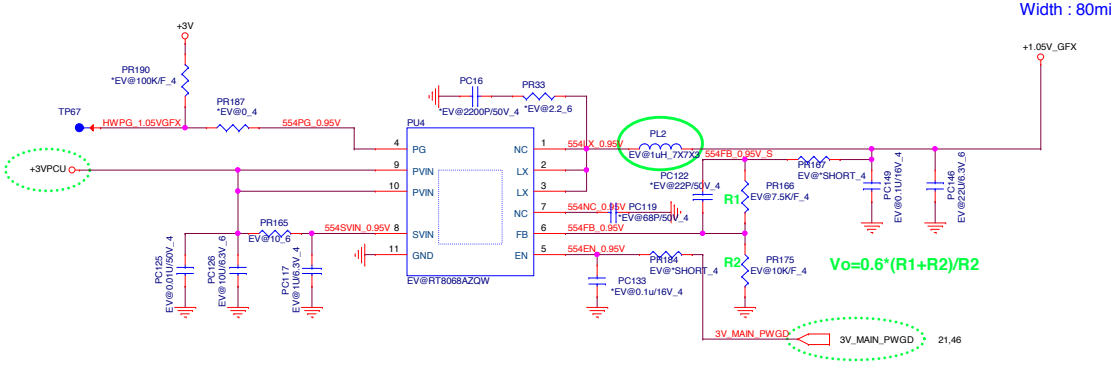
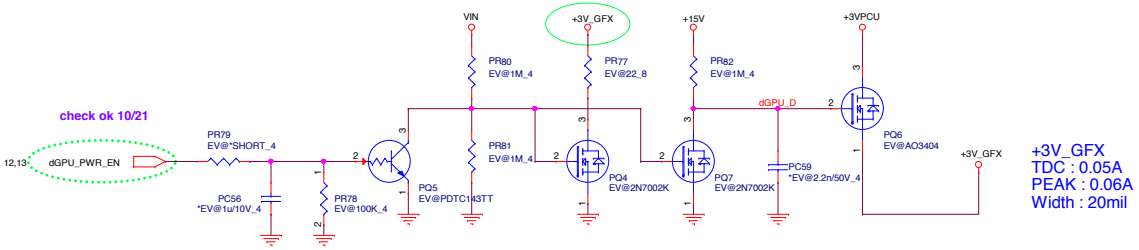
19,20,21 +1.05V_GFX
19,21,22,37 +3V_GFX

+1.05V_GFX
TDC : 1.57A
PEAK : 2.09A
Width : 80mil



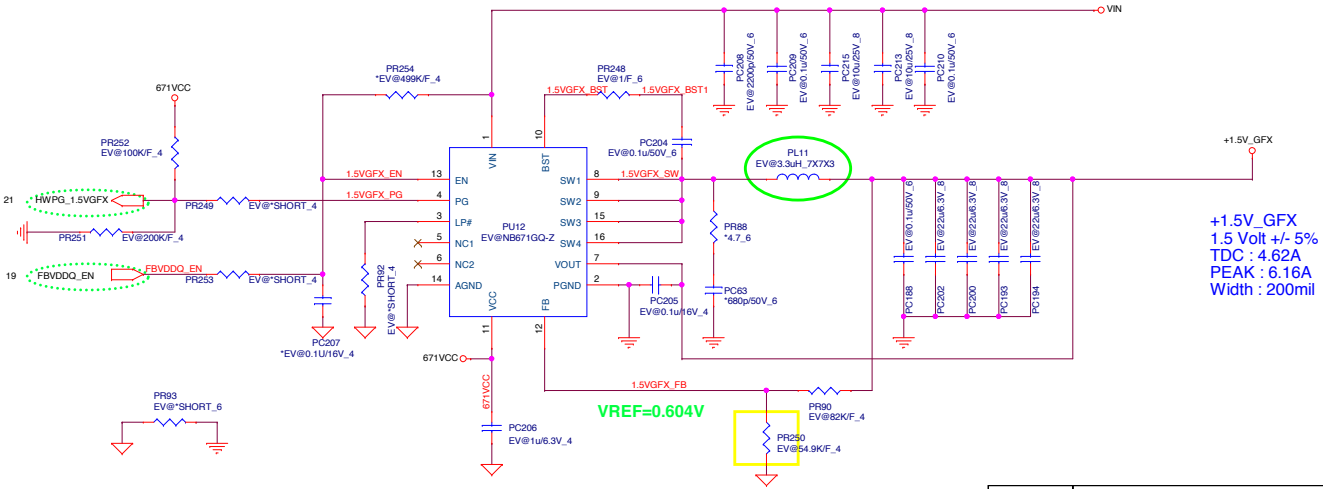
Vo=0.6*(R1+R2)/R2

check ok 10/21



check ok 10/21

+3V_GFX
TDC : 0.05A
PEAK : 0.06A
Width : 20mil



+1.5V_GFX
1.5 Volt +/- 5%
TDC : 4.62A
PEAK : 6.16A
Width : 200mil

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Size	Document Number +1.5V_GFX/+1.05V_GFX/+3V_GFX	Rev 1A
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Model	Date	CHANGE LIST
	A	1. FIRST RELEASED
	B	1. L23,L24 change to correct footprint 0402. 2. Correct CN14 UART from 3V to 5V. (Page13) 3. Nostuff R270,R271,and stuff R268,R2699,D31,D32 for DDC HDMI 7-13 issue. (Page30) 4. Nostuff U22,C441,R200,and stuff R182. (Page2) 5. Chagne HDA power to +3V R296,unstuff R247. (Page14) 6. Chagne Code DVDD-IO to +3V R370 ,unstuff R366. (Page32) 7. Add R204 and unstuff R178 for VCCST_PWRGD. (Page02) 8. Change R424,R431 to 62ohm for Audio EA. (Page32) 9. Unstuff R207 and stuff R208 for DMIC. (Page32) 10. Stuff 50ohm for CATERR#. (Page2) 11. Unstuff R132,R133,R576 for CPU_OPC_COMP. (Page6) 12. Reserve U54,U55,U56 and add R970,R971,R972. (Page10) 13. Add U53,C812 for VCCST PWRGD timing issue. (Page2)
	C	14. Change Jdim1,Jdim2 footprint to fix SMT issue. (Page17,18) 15. Change U14 to version 6516 =>AL006516001 , so unstuff R108, unstuff R110,R111. (Page28) 16. Change U23 to version 8201 =>AL008201003 , so R238 change to 4.99K, unstuff R229. (Page30) 17. SWAP NGFF PCIE10&11, stuff R952/R953 , R949/R950 , C1170/C1171 ,C1172/C1173. (Page34) 18. Add C687 for Pltrst#. (Page19) 19. Reserve C85 for VID . (Page02) 20. Unstuff R732 for PCH_SPI_IO3, it is ES sample only. (Page12) 21. Shortpad 0402 for R316,R301,R661,R656,R3,R4,R48,R99,R448,R444,R414,R418,R419,R182,R540,R543,R556,R998,R999 Shortpad 0603 for R347 22. Del R720,R319 ,Unstuff R719 ,stuff R718,R278,R723,R317 (Page11) 23. Shortpad 0402 for PR139,PR142,PR144,PR146,PR148,PR150,PR152,PR153,PR158,PR163,PR164 Shortpad 0603 for PR149,PR161. (Page38) 24. Shortpad 0402 for PR6278,PR6283 Shortpad 0603 for PR6125,PR6130,PR6285. Shortpad 0603 for PR6125,PR6130,PR6285. Remove JP6018,JP6021,JP6017,JP6019. (Page39) 25. Shortpad 0402 for PR115. Shortpad 0603 for PR164,PR256. Remove JP9,JP10. (Page40) 26. Shortpad 0402 for PR291,PR292,PR301,PR303,PR273 Shortpad 0603 for PR285,PR298. Remove JP13,JP16,JP17 (Page41) 27. Shortpad 0402 for PR57,PR55,PR203,PR205,PR213,PR212,PR198,PR210,PR208,PR206, PR182,PR183,PR168,PR174,PR179,PR178,PR202,PR197,PR169,PR176 (Page42) 28. Shortpad 0402 for PR67,PR237,PR238,PR62,PR225,PR226,PR66,PR235,PR236 Shortpad 0603 for PR234,PR224,PR233 Remove JP4 (Page43) 29. Shortpad 0402 for PR61,PR221,PR222,PR69,PR244,PR245,PR64,PR240,PR241 Shortpad 0603 for PR220,PR243,PR239 Remove JP3,JP5 (Page44) 30. Shortpad 0402 for PR282,PR284,PR272 Shortpad 0603 for PR121 Remove JP12 (Page45.) 31. Shortpad 0402 for PR98,PR99,PR103,PR73,PR74,PR109,PR108,PR97 Shortpad 0603 for PR94 Remove JP7 (Page46.) 32. Shortpad 0402 for PR184,PR167,PR79,PR249,PR253,PR92 Shortpad 0603 for PR93 Remove JP1,JP2,JP6,JP8 (Page47.) 33. C861,C864 change from 10P to 18P for CRB time issue. (Page11) 34. Change PR125 from 1.47k to 1.2K(CS21202FB13). (Page45) 35. Change U1 PN from 5243 to 5245, due to EOL. (Page29) 36. Add R369 and reserve U34 LDO circuit. (Page32)

PROJECT :ZRY Quanta Computer Inc. Size: Document Number: Change list; Rev: 1A Date: Tuesday, August 25, 2015 Sheet 48 of 49	DOC NO.	PROJECT MODEL :	ZRY	APPROVED BY:	DATE:
		PART NUMBER:		DRAWING BY:	REVISON:

Model	Date	CHANGE LIST
	C2	37. PR56 and PR216 change from 1ohm to 10ohm , it is fix black screen issue. 38. Shortpad 0402: R202, R553, R127, R142, R144, R151, R156, R123, R243, R233, R631, R691, R223, R635, R658, R628, R458, R324, R276, R724, R246, R296, R592, R593, R455, R456, R13, R234, R435, R417, R377, R370, R952, R953, R163, R165, R958, R959, R598, R601, R602, R604, R949, R950, R960, R954, R955, R956, R792, R821 39. Shortpad 0603: R754, R244, R245, R216, R256, R796, R219, R321, R218, R260, R314, R793, R277, R222, R217, R303, R302, R257, R220, R753, R328, R330, R259, R221, R297, R752, R109, R474, R14, R445, R810, R805, R824, R825, R396, R367, R368, L22, R429, R430 40. Shortpad 0805: R25, R16, R17, R164, R214, R310, R951, R610, R948 41. Reserve PR6291 for ISEN2_B and ISEN1B the GT short circuit. (page44) 42. Change USB3 Tx and Rx signal from port1 to port6, it is fix crystal issue. (page9) 43. Follow the change list 42, R991 change to NC and R990 connect to +3V_DEEP_SUS. (page13) 44. PR229 and PR232 change from 10kohm to 11.3kohm for VR thermal alert follow ZRW setting 110 degree. 45. PR125 change from 1.2kohm to 1.47kohm for h/w shut down sensor setting 85 degree. 46. PR56 and PR216 change from 10ohm to 1ohm. Its short turn solution no run to next C2 stage (page44)
	MV	1. Shortpad 0402: R565 , R115 , R340 , R619 , R351 , R623 , R707 , R8 , R663 , R177 , R379 , R392 , R397 , R331 , R329 , R348 , R400 , R389 , R343 , R341 , R412 , R394 , R338 , R387 2. Shortpad 0603: R369 3. Remove R460 , R457 for touch panel (page29) 4. Unstuff SW2 for cost down (page37) 5. Reserve TPM U44 (page33) and G sensor U10 (page35) 6. PR19 , PR21, PR31 , PR26 , PR216 , PR56 change from 1ohm to 10ohm for balck screen issue (pag43-44) 7. R769 change from 100K to 10K follow TP issue 8. U41.A36 and U41.A37 connect with GND, The reason to GND these pins is to minimize risk from ESD/EMI