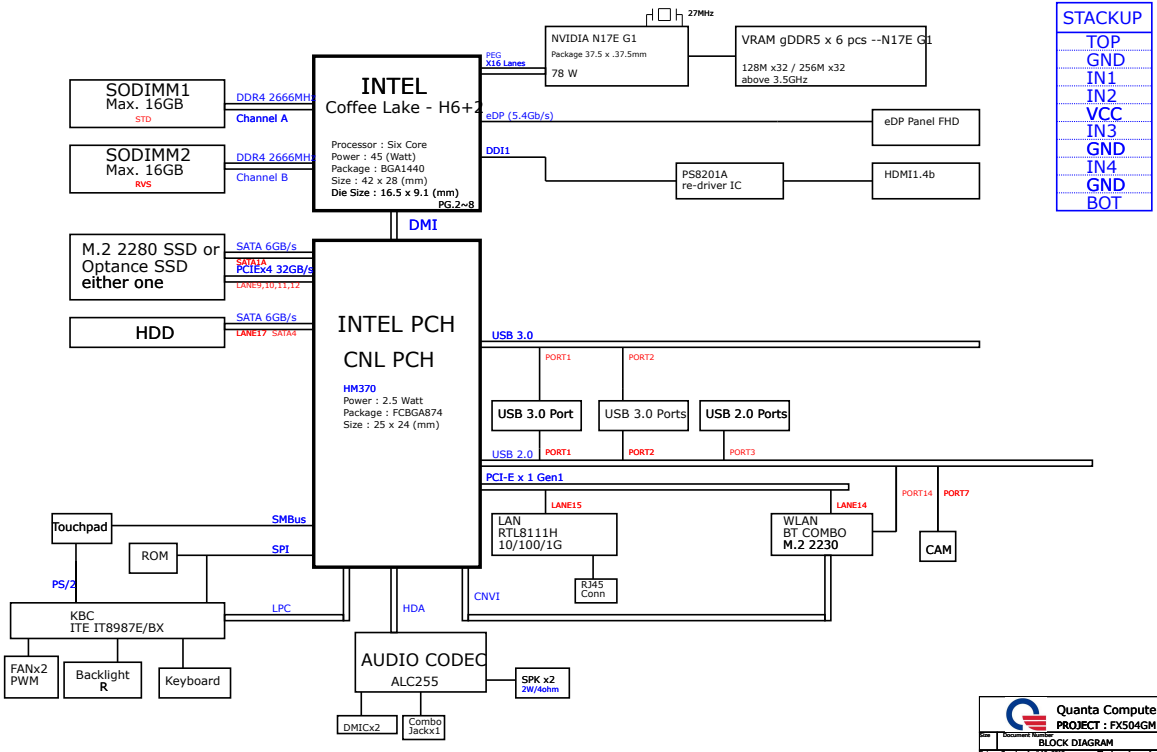
Asus 15" FX504 GM Block Diagram

01

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
IN4
GND
BOT



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BLOCK DIAGRAM
Rev 1A
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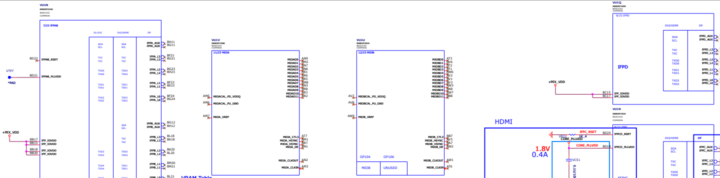
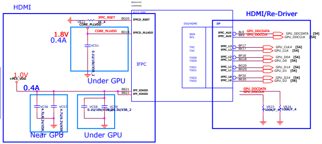
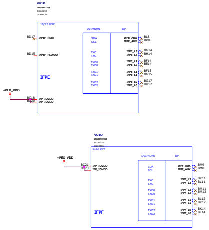






VRAM Table

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	QB P/N	
0x0	GDDR5 256Mx32 8 GHz	Samsung B die	K4G80325FB-HC25	AKG58WWT510	VR31,VR32,VR33 NC ,VR46,VR47,VR48 mount
0x1	GDDR5 256Mx32 8 GHz	Micron A die	MT51J256M32HF-80:A	AKG5QGUTL16	VR46,VR32,VR33 NC ,VR31,VR47,VR48 mount
0x7	GDDR5 128Mx32 4 GHz	Samsung E die	K4G41325FE-HC25	AKG5PGRT502	VR31,VR32,VR33 mount ,VR46,VR47,VR48 NC
	GDDR5 128Mx32 4 GHz	Hynix A die	H5GQ4H24AJR-R4C 0x6	AKG5PGUTW02	VR46,VR32,VR33 mount ,VR31,VR47,VR48 NC

	Vender	Size	P/N
N17E-G2	WINBOND	4Mb	AKE57F00N01
N17E-G1	Macronix	4Mb	AKE5QFP0Z00

Table 5.3 RAMCFG

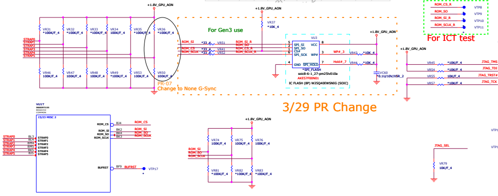
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

	Strap3/4/5 setting	
G-Sync panel	101 Default	VR34,VR53,VR36 mount , VR49,VR35,VR50 no munt
Non G-Sync	100	VR34,VR53,VR50 mount , VR49,VR35,VR36 no munt

Table 2. N17E-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production ready
		1.35V and 1.5V	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production ready
		1.35V and 1.55V	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production ready
4 Gb	128Mx32	1.35V and 1.55V	Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	Full	Post production ready
		1.35V and 1.55V	Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	Full	Post production ready

For N17E-G2/G1
Need to check the Page 54
VRAM power for 1.5V/1.55V
Samsun:1.55V ; Micron:1.5V



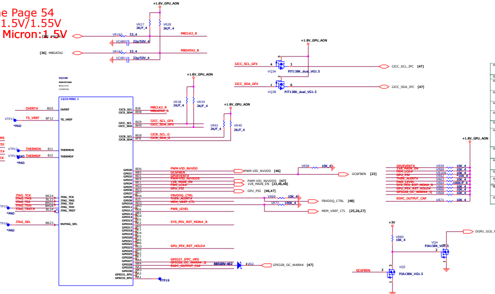
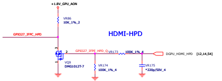
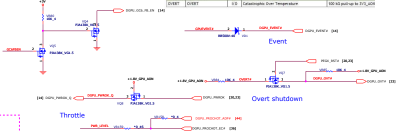


Table 14.3 GPIO Descriptions for GB4-256 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable Control signal to turn on a logo LED	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Turn on heat sink logo LED when present Panel Power enable	10K pull-up to a gated 3V3 100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight EnableFan Tachometer; see Section 14.3.9.	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	PWM output used to control Fan Speed see Section 14.3.9 for definitionSystem side PCIe reset monitor	10K pull-up to a gated 3V3 10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision/STEREO	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	NVVDDS_PSI GC5_MODE			
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI SWAP READY OUT	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset controlInput when master GPU or Output when Slave GPU (SLI with more than 2 boards only)	Open Drain 10 kΩ pull-up to a gated 3V3100K pull-down
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10 kΩ pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	UNUSED	I/O		

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON





Remove TU1 Alert to EC

Nvidia : suggest to connect this pin to EC only
GPIO12 AC detect
AC high
DC low

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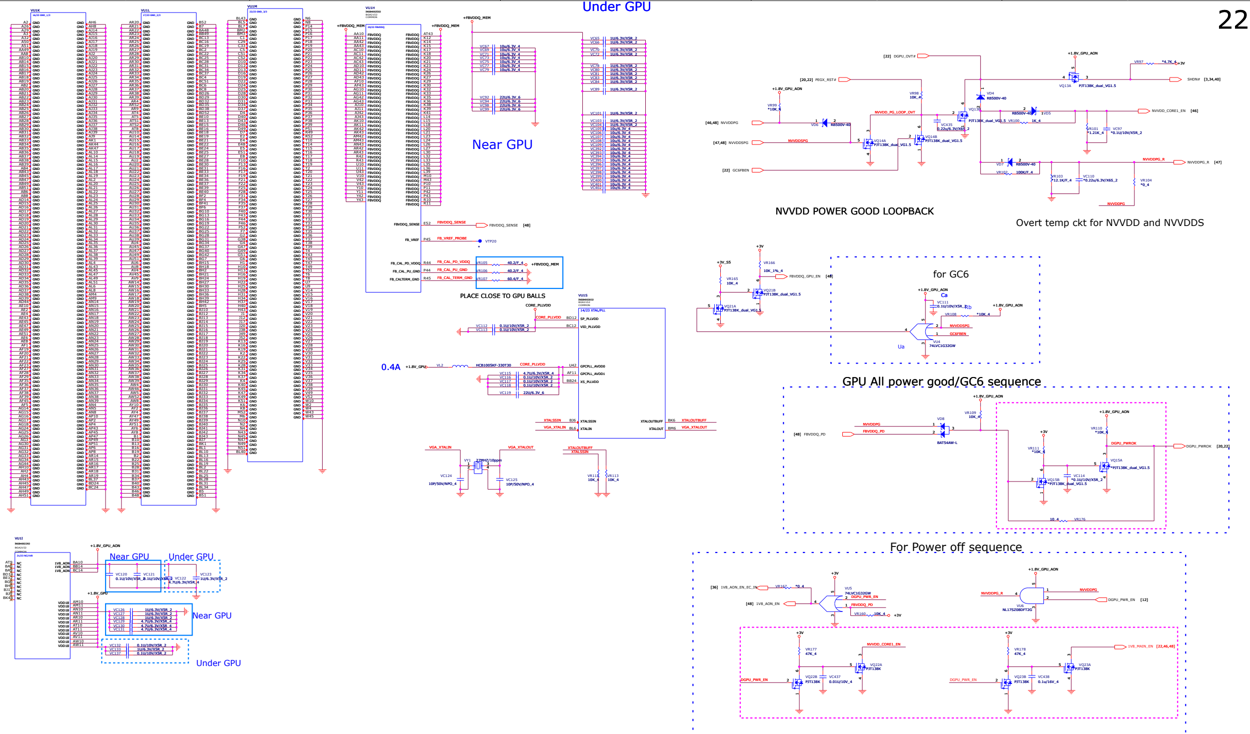

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	N17E-G1 -4/8 (MISC)	1A

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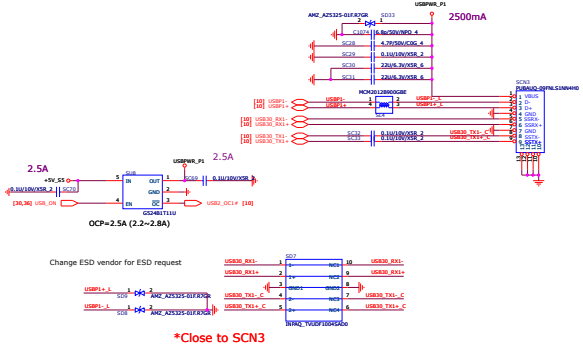
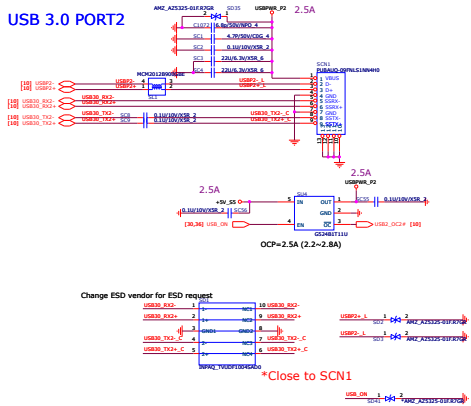
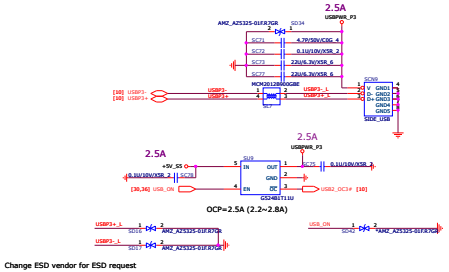
USB 3.0 PORT1



USB 3.0 PORT2



USB 2.0 PORT3



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	USB3.0/USB2.0		1A
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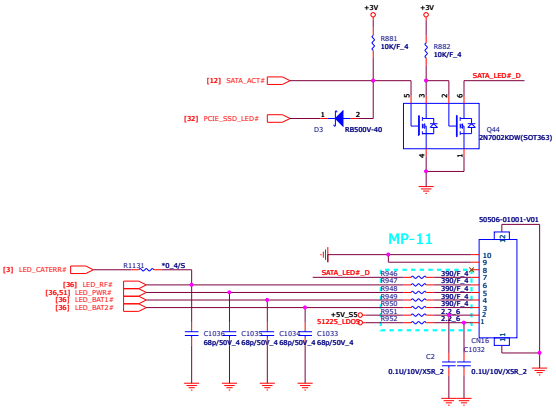
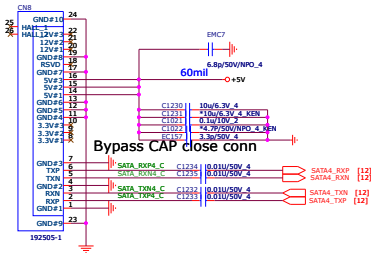
LED



SATA HDD Connector



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	HDD/LED	1A
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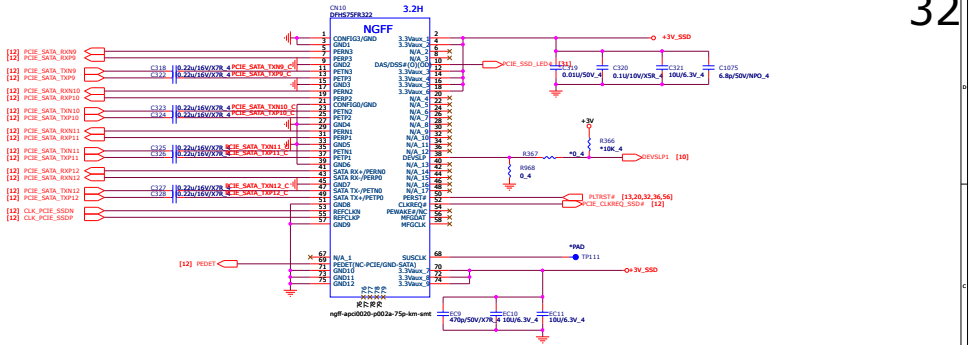
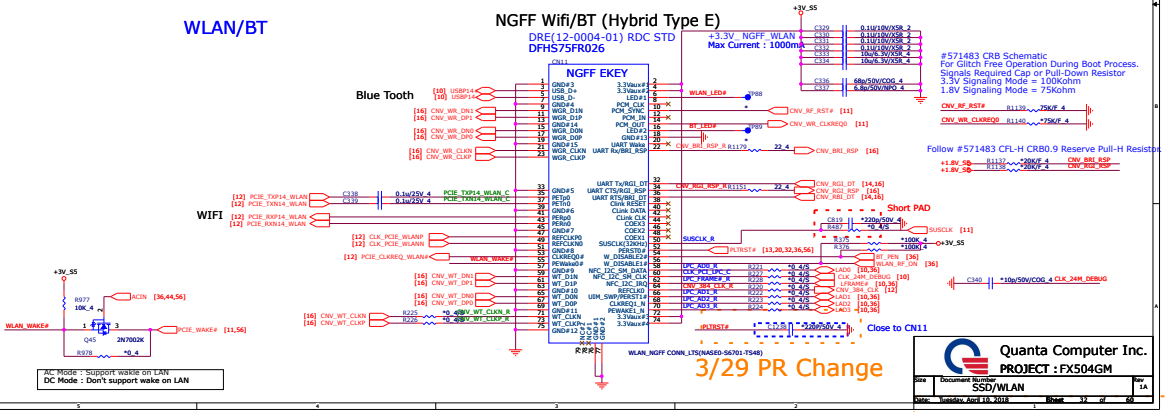
SSD



WLAN/BT



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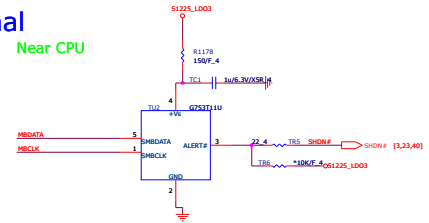
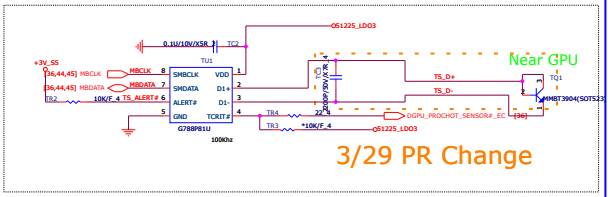
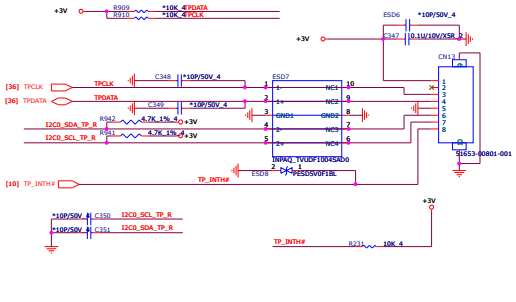
Thermal

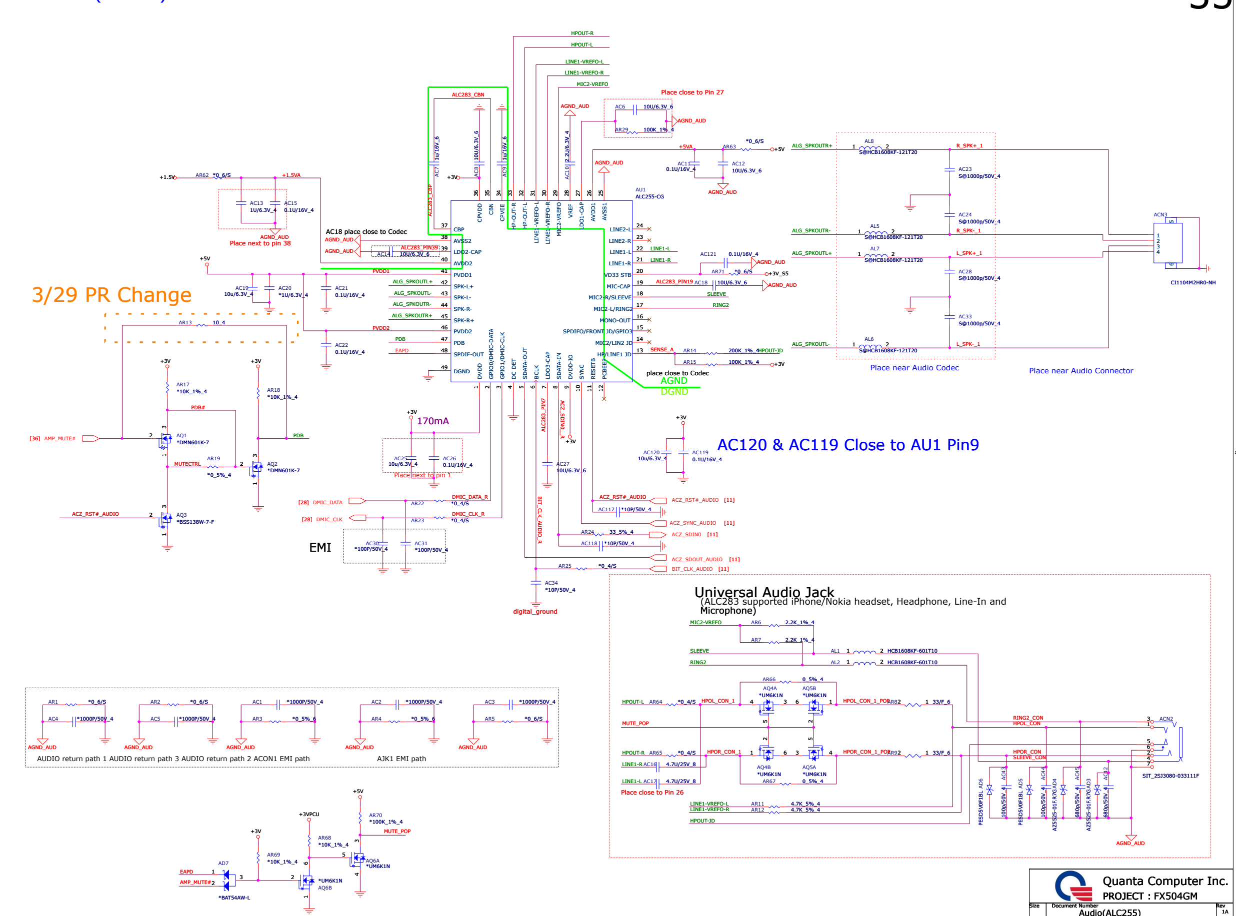
Near CPU





Touch Pad Connector AA type




AU1
ALC255-CG
HPOUT-R
HPOUT-L
LINE1-VREFO-L
LINE1-VREFO-R
MIC2-VREFO
ALC283_CBN
Place close to Pin 27
AC18 place close to Codec
Place next to pin 38
3/29 PR Change
AMP_MUTE#
ACZ_RST#_AUDIO
PDB#
PDB
MUTECTRL
170mA
Place next to pin 1
DMIC_DATA
DMIC_CLK
EMI
ACZ_SYNC_AUDIO
ACZ_SDINO
ACZ_SDOUT_AUDIO
BIT_CLK_AUDIO
digital_ground
AC120 & AC119 Close to AU1 Pin9
place close to Codec
AGND
DGND
ALG_SPKOUTR+
ALG_SPKOUTR-
ALG_SPKOUTL+
ALG_SPKOUTL-
Place near Audio Codec
Place near Audio Connector
CI1104M2HR0-NH
Universal Audio Jack
(ALC283 supported iPhone/Nokia headset, Headphone, Line-In and Microphone)
Place close to Pin 26
SIT_2SJ3080-033111F
AUDIO return path 1 AUDIO return path 3 AUDIO return path 2 ACON1 EMI path
AJK1 EMI path
EAPD
AMP_MUTE#
MUTE_POP
*BAT54AW-L

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3/29 PR Change

Close to KU1

KR6 ,KC9 Close to KU1

3/31 Change KR72 from 200K to 100K for ER stage

3/29 PR Change

KC13 Close to KU1

Reserved only

1.8V level

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

ESD23 CLOSE TO KU1

For Audio Speaker ID

3/29 PR Change

	SPK_ID0	SPK_ID1	
GL503:15	0	0	4013 15" TI Smart Amp/S@
GL703:17	0	1	4013 17" TI Smart Amp/S@
FX504 :15	1	0	18phi 15" RTK CODEC internal Amp/A@
NA	1	1	22phi 17" RTK CODEC internal Amp/A@

Coffee Lake Processor (CLK,MISC,JTAG)

03

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

Close to CPU

For DCI debug

Please remove to CPU side

PROCHOT# (50ohm)
Trace Length <11 inches

Cb need placment near VR

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;

Mark eDP mode Enabled

Mark PCIE port reserved
N17P used port 8~15

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS CLOSE TO VR
PULL UP IS IN THE VR MODULE

Close to CPU

SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS

Close to CPU

SVID ALERT

CLOSE TO CPU
PLACE THE PU RESISTORS

Close to CPU

SVID DATA

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Configuration Signals:

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]	Stall reset sequence after PCU	Pitote that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OEM board.
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-assesed x0 = PEG wait for BIOS fro training

CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

ESD18/ESD19 Close to CPU

Under CPU

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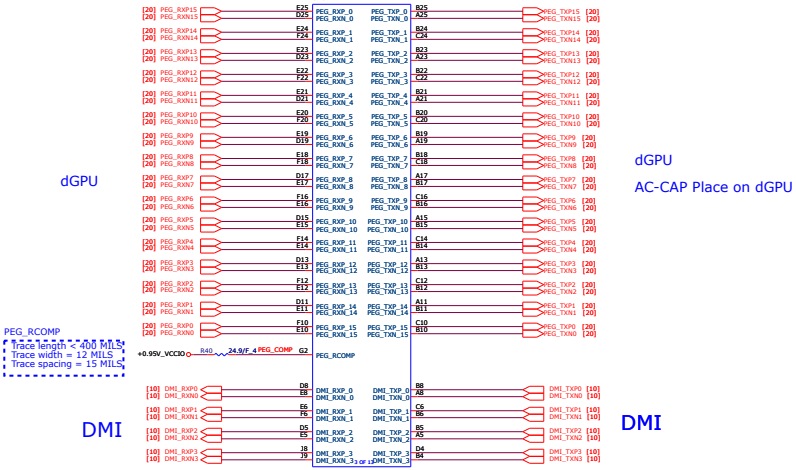
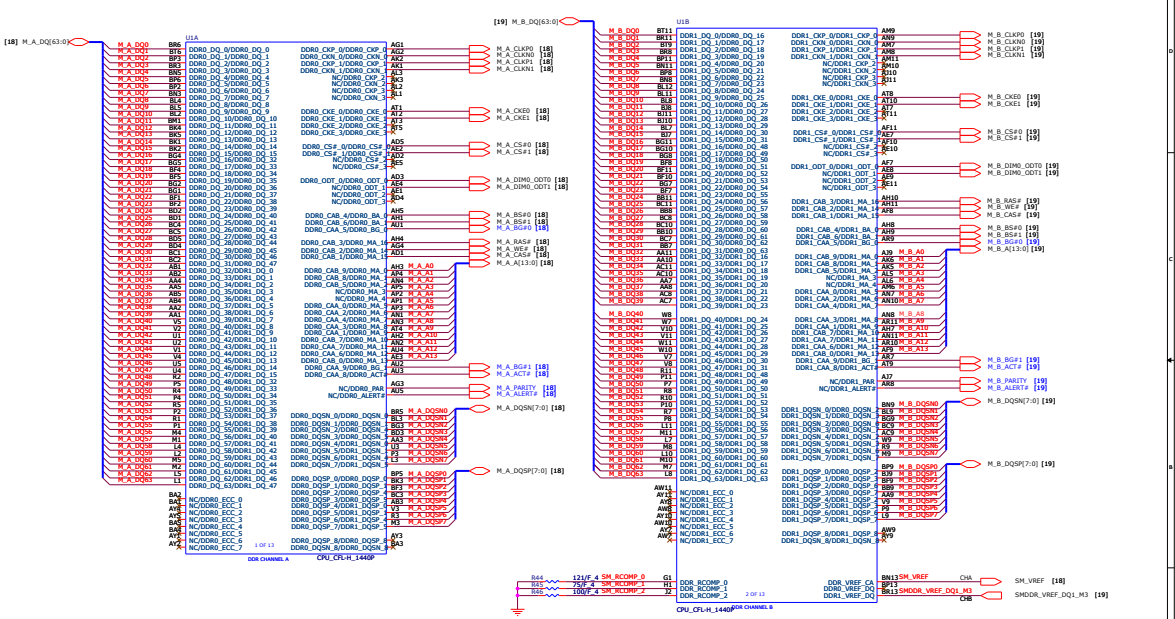

U1C
dGPU
dGPU
AC-CAP Place on dGPU
PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS
DMI
DMI
CPU_CFL-H_1440P
U1D
eDP
DP & PEG Compensation
eDP_RCOMP
Trace length < 100 Mils
Trace Width 5 Mils Trace Spacing 25 Mils
CPU_CFL-H_1440P

Coffee Lake Processor (DDR4)



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CFL 3/7 (DDR4 I/F)
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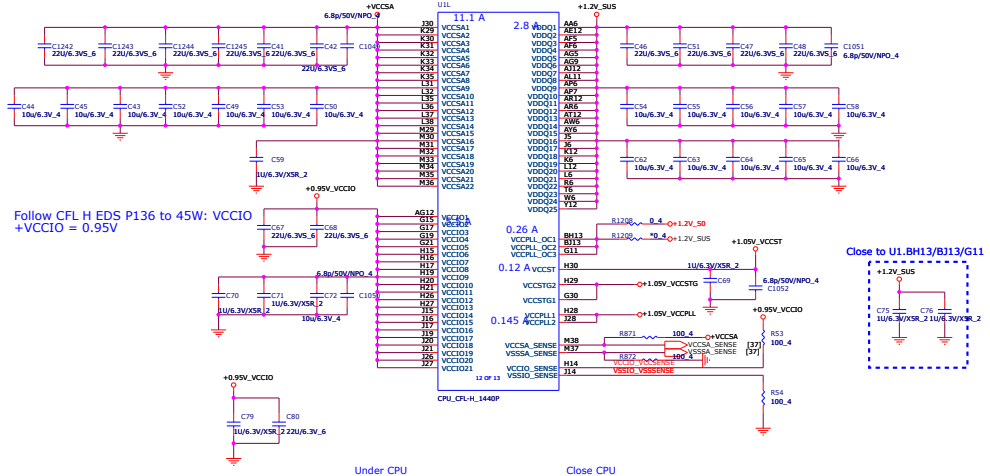
CFL Processor (POWER)

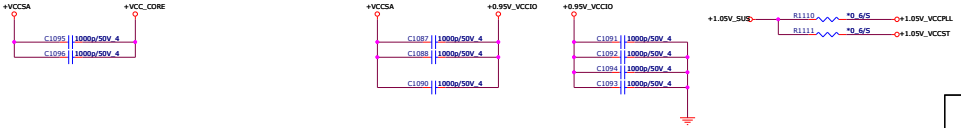
Follow CFL H page 126 to 45W(GT2): +VCCGT=34A

Follow CFL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow CFL H EDS page 135 45W: VDDQ=2.8A

Follow CFL H EDS P136 to 45W: VCCIO +VCCIO = 0.95V





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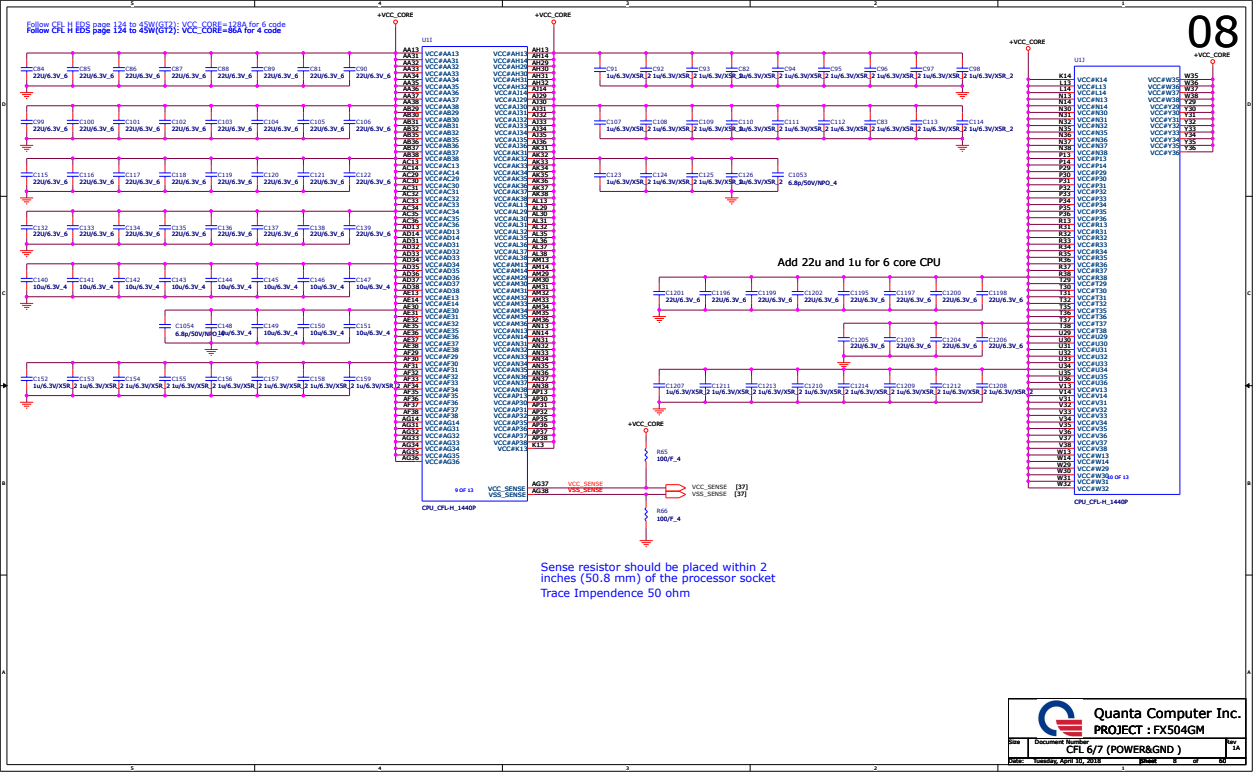
Follow CFL H EDS page 124 to 45W(GT2): VCC_CORE=128A for 6 core
Follow CFL H EDS page 124 to 45W(GT2): VCC_CORE=86A for 4 core
08
+VCC_CORE
U11
CPU_CFL-H_1440P
9 OF 13
Add 22u and 1u for 6 core CPU
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impendence 50 ohm
VCC_SENSE [37]
VSS_SENSE [37]
R65 100/F_4
R66 100/F_4
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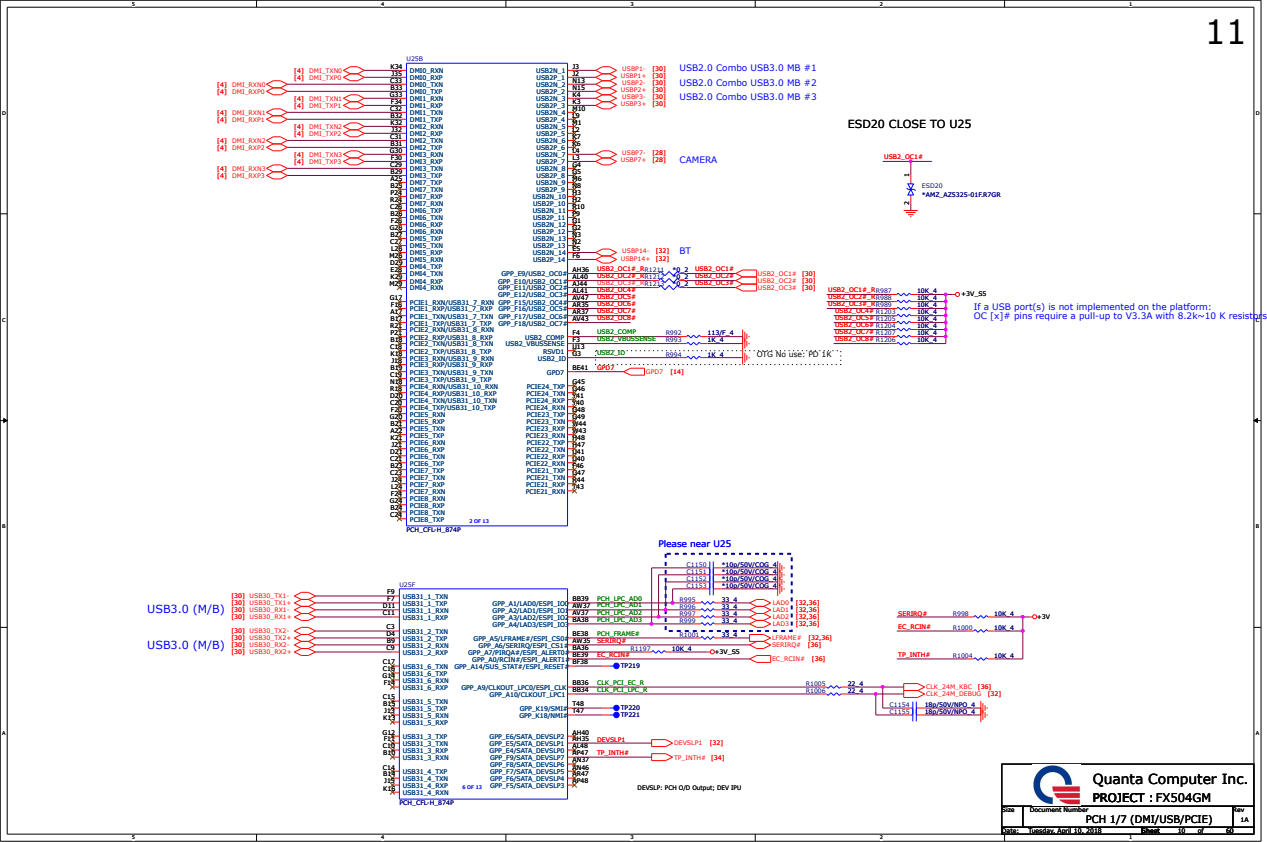
U25B
PCH_CFG_H_8740P
2 OF 13
USB2.0 Combo USB3.0 MB #1
USB2.0 Combo USB3.0 MB #2
USB2.0 Combo USB3.0 MB #3
CAMERA
BT
ESD20 CLOSE TO U25
ESD20
*AMZ_AZS325-01F.R7GR
If a USB port(s) is not implemented on the platform:
OC [x]# pins require a pull-up to V3.3A with 8.2k~10 K resistors
OTG No use: PD 1K
Please near U25
U25F
USB3.0 (M/B)
USB3.0 (M/B)
6 OF 13
PCH_CFG_H_8740P
DEVSLP: PCH O/D Output; DEV IPU
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PCH 1/7 (DMI/USB/PCIE)
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Please near U25

Please near U25

EC Drive High for OVERRIDE

DDR4 SPD

RTC Circuitry(RTC)

RTC Power trace width 20mils.

30mils

Close to PCH

For DCI debug

RTC Detect for EC Check

AHL03003058

S0281-002D1-00R

PCH_CFL-H_874P

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	PCH 2/7 (HDA/SMBUS)		1A
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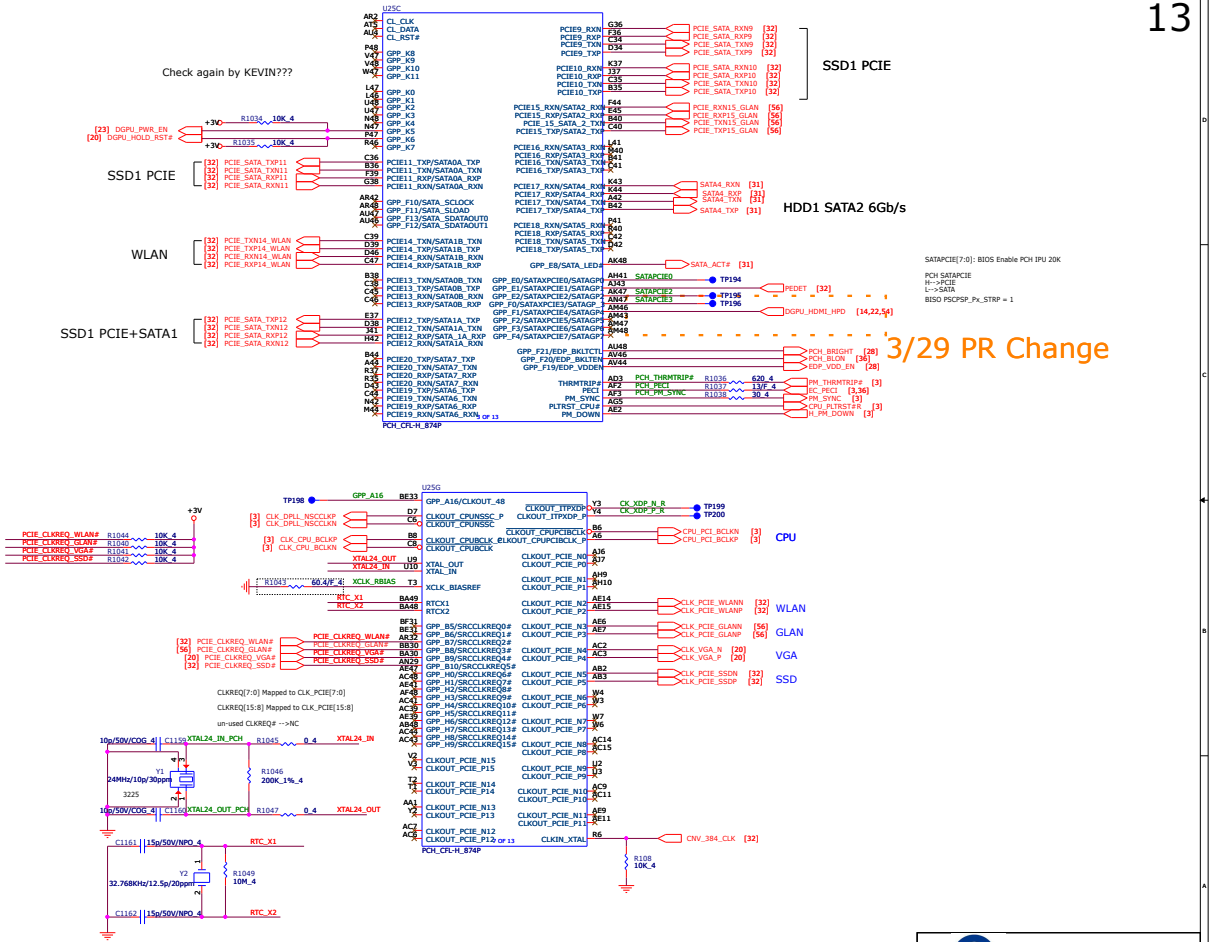
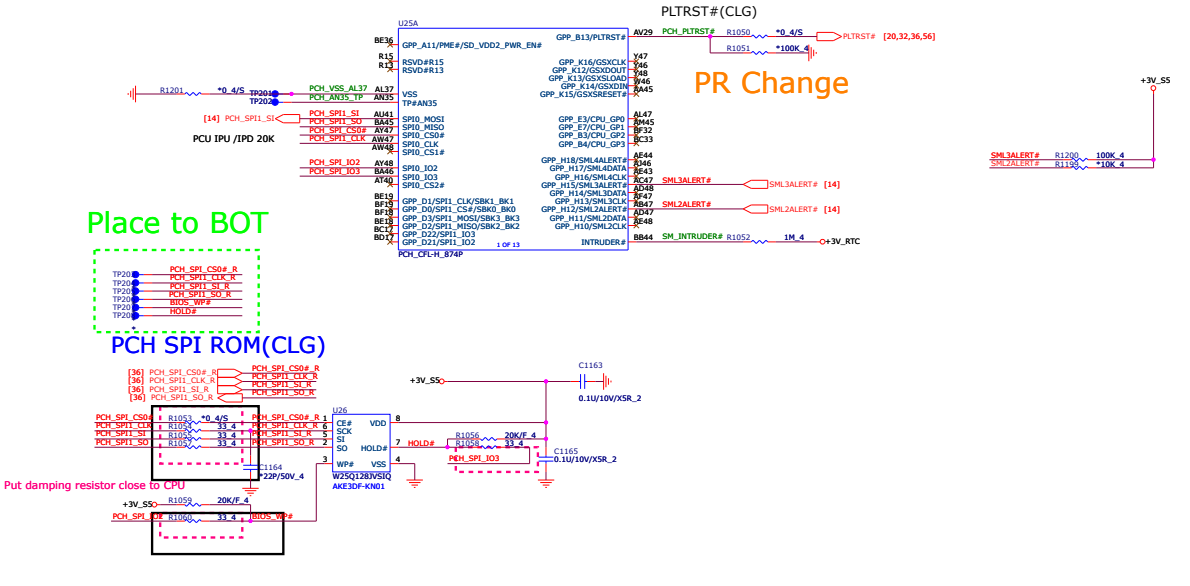

U25C
Check again by KEVIN???
SSD1 PCIE
WLAN
SSD1 PCIE+SATA1
HDD1 SATA2 6Gb/s
SSD1 PCIE
3/29 PR Change
U25G
CPU
WLAN
GLAN
VGA
SSD
CLKREQ[7:0] Mapped to CLK_PCIE[7:0]
CLKREQ[15:8] Mapped to CLK_PCIE[15:8]
un-used CLKREQ# -->NC
PCH_CFL-H_874P



Quanta Computer Inc.		
PROJECT : FX504GM		
Size	Document Number	Rev
	PCH 4/7 (GPIO/MISC)	1A
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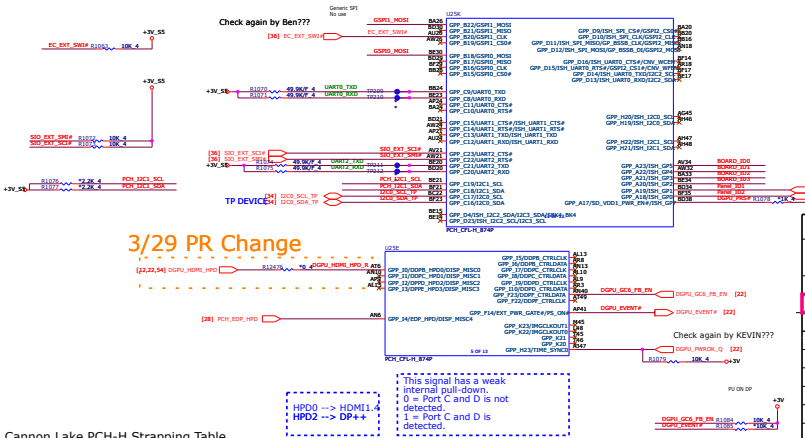


GPIO Pull-up/Pull-down(CLG)

R need place to BOT

R need place to BOT

	Panel ID1	Panel ID2
FHD	1	1
4K2K	1	0
HD	0	1

BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
0	0	0	0
0	0	0	1
0	0	**0**	1
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1

Cannon Lake PCH-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	**PCH_PWROK**	**0 = *Disable Top Swap (iPD 20K) Default** 1 = Enable Top Swap Mode	+3V_S5 R1082 *1K_4 ACZ_SPKR [11]
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) Default **1 = Enable No Reboot Mode**	+3V_S5 R1087 *1K_4 GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	**0 = *Disable Intel ME Cryp to TLS(iPD 20K) Default** **1 = Enable Intel ME Cryp to TLS PU to support AMT TLS**	+3V_S5 R1088 *1K_4 SMBALERT# [11]
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	**0 = *SPI (iPD 20K) Default** **1 = LPC**	+3V_S5 R1089 *1K_4 GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	**0 = *LPC is selected for EC (iPD 20K) Default** **1 = eSPI selected for EC**	TP213 SML0ALERT# [11]
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	+3V_S5 R1220 100K_2 PCH_SPI1_SI [13]
GPP_H15 (SML3ALERT#)	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP214 SML3ALERT# [13]
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP215 SML1ALERT# [11]
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device **driving it to opposite direction during strap sampling.**	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO (I2S0_TXD)	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	**0 = *Enable security in the Flash Description (iPD 20K) Default** **1 = Disable Flash Descriptor Security (Override)**	EC Drive High for OVERRIDE
GPP_H12 (SML2ALERT#)	eSPI Flash Sharing Mode	RSMRST#	**0 = *Master Attached Flash Sharing (MAFS) enabled (iPD 20K)Default** **1 = Slave Attached Flash Sharing (SAFS) enabled.**	TP216 SML2ALERT# [13]
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	**0 = *Port B is not detected (iPD 20K) (Default)** **1 =Port B is detected**	
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	**0 = *Port C is not detected (iPD 20K) (Default)** **1 =Port C is detected**	
GPP_I10 (DDPD_CTRLDATA)	Display Port D Detected	**PCH_PWROK**	**0 = *Port D is not detected (iPD 20K) (Default)** **1 =Port D is detected**	
GPP_F23	**Display Port F Detected**	**PCH_PWROK**	0 = *Port F is not detected (iPD 20K) (Default) **1 =Port F is detected**	CFL - H CPU Not Support DDI Port F
GPP_J4 CNV_BRI_DT/ UART0_RTS#	XTAL Frequency Select	**RSMRST#**	**An external pull-up is required on this strap since 38.4MHz XTAL is not supported on the PCH.** **0 = *38.4MHz XTAL frequency selected. (iPD 20K) (Default)** **1 = 24MHz XTAL frequency selected.**	+1.8V_S5 R1141 *5.7K_5% CNV_RBI_DT [16,32] R1142 *20K/F CNV_RGI_DT [16,32]
GPP_J6 CNV_RGI_DT/ UART0_TXD	M.2 CNV Mode Select	**RSMRST#**	**An external pull-up or pull-down is required.** **0 = Integrated CNVi enable. (Default)** **1 = Integrated CNVi disable.**	+1.8V_S5 R1143 20K/F R1144 *20K/F
GPP_J9	1.8V VCCPSPI	RSMRST#	**0 = *VCCSPI is connected to 3.3V rail. (iPD 20K) (Default)** **1 = VCCSPI is connected to 1.8V rail**	R1145 *10K GPP_J9 [16]
GPD7	Reserved	**DSW_PWROK**	This strap should sample HIGH. There should NOT be any on-board device **driving it to opposite direction during strap sampling.**	**External pull-up is required. Recommend 100K.** +3V_S5 R1095 100K_5% GPD7 [10] R1145 *10K

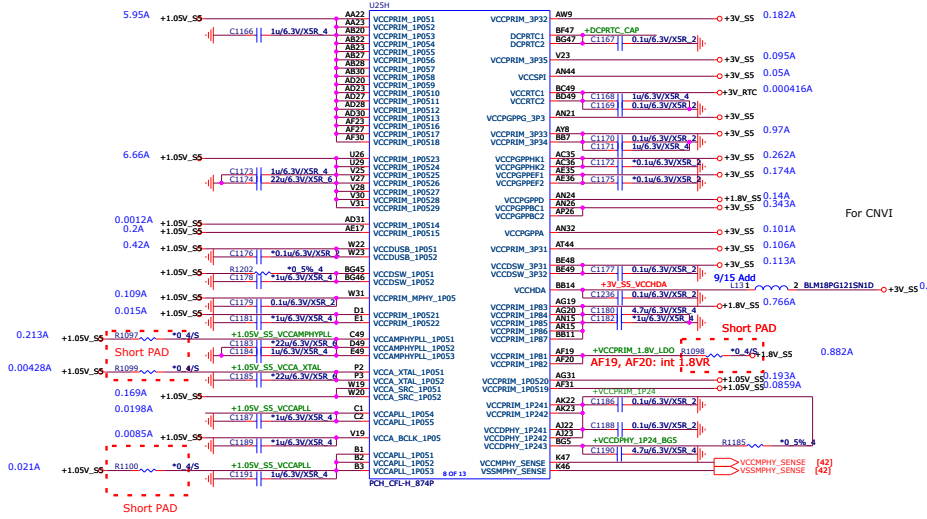
PCH Strap: GPP_J4 = XTAL SELECT.1
HIGH -> 24 MHZ / LOW -> 38.4 MHZ

PCH Strap: GPP_J6 = M.2 CNVI STRAP
HIGH -> DISABLE / LOW -> ENABLE

Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1'
for the proper functionality of the SPI (Flash) I/Os

Warning: This strap must be configured to '0' (SAFS is disabled)
if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

need to add +1.05V power rail



ESD22 CLOSE TO U25

ESD21 CLOSE TO U25.B2

1.24V for CNVi logic = VCCDPHY_1P24 & +VCCPRIM_1P24
This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC.
Refer to the Platform Design Guide for implementation details.

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U25L
U25I
U25J
U25M
For C10
Close to U25
CPU_VCCIO_PWR_GATE#
CNV_BRI_RSP : Model Internal Pull-UP 20k.
CNV_RGI_RSP : Model Internal Pull-UP 20k.
PCH_CFL-H_874P
Quanta Computer Inc.
PROJECT : FX504GM
PCH 7/7 (GND/CNV)
Tuesday, April 10, 2018

1207 Change

H31 *hole
H12
H110 *hole
H13
H40 *hole
EMR9 *0.6
EMR10 *0.6
AGND_AUD
H22 *HOLE
H23 *HOLE
H20 *HOLE
H21 *HOLE
H19 *HOLE
H18 *HOLE
H14 *hole H14_GND
H25 *HOLE
H15 *hole
H16 *hole H16_GND
H39 *HOLE
H115 *HOLE
H100 *HOLE
H114 *HOLE
H36 *HOLE
EMI2 *HOLE
EMI3 *HOLE
EMI4 *HOLE
EMI5 *HOLE
H111 *HOLE
H112 *HOLE
H113 *HOLE

placement on TOP SIDE VIN Plane

VIN
EMC3 6.8p/50V/NPO_4
C1077 0.1u/25V_4
C1078 0.1u/25V_4
C1079 0.1u/25V_4
C1080 0.1u/25V_4
C1081 0.1u/25V_4
C1082 0.1u/25V_4
C1085 0.1u/25V_4
C1086 0.1u/25V_4

placement on TOP SIDE VA+ Plane

VA+
C1083 0.1U/50V/XSR_4
C1084 0.1U/50V/XSR_4
EMC4 6.8p/50V/NPO_4

VA
EMC8 *6.8p/50V/NPO_4
EMC9 *6.8p/50V/NPO_4
EMC10 *6.8p/50V/NPO_4
EMC11 *6.8p/50V/NPO_4

PR Change

+1.2V_SUS
C1273 0.1U/50V/XSR_4
C1274 0.1U/50V/XSR_4
C1276 0.1U/50V/XSR_4
C1275 0.1U/50V/XSR_4

+5V_SS
C1277 0.1U/50V/XSR_4

For EMC

EMC2 6.8p/50V/NPO_4
EMC1 6.8p/50V/NPO_4
+VCC_GFX

For Over place use

+3V_SS
C1108 1000p/50V_4
C1107 1000p/50V_4
C1110 1000p/50V_4
C1109 1000p/50V_4

+3V_SS
+5V
C1103 1000p/50V_4
C1104 1000p/50V_4
C1106 1000p/50V_4
C1105 1000p/50V_4

+5V
+5V_SS
C1112 1000p/50V_4
C1111 1000p/50V_4
C1114 1000p/50V_4
C1113 1000p/50V_4
C1146 1000p/50V_4

+3V_SS
C1133 1000p/50V_4
C1131 1000p/50V_4
C1134 1000p/50V_4
C1132 1000p/50V_4
C1147 10u/6.3V_4

+3V_SS
+5V
C1127 1000p/50V_4
C1130 1000p/50V_4
C1129 1000p/50V_4
C1145 1000p/50V_4

+5V
+5V_SS
C1123 1000p/50V_4
C1126 1000p/50V_4
C1125 1000p/50V_4

+5V_SS
C1135 1000p/50V_4
C1136 1000p/50V_4
C1138 1000p/50V_4
C1137 1000p/50V_4

+5V_SS
C1119 1000p/50V_4
C1120 1000p/50V_4
C1122 1000p/50V_4
C1121 1000p/50V_4

For ESD request

Close to H14 Close to H16

PR Change

H14_GND
EMCIG12
EMCIG2
EMCIG21 *1u/25V_6
EMR13 *0_6
EMR12 *0_6
EMCIG11
EMR11 *0_6
*SHORT_PAD9212
*SHORT_PAD9212
*SHORT_PAD9212

H16_GND
EMR5 *0_6
EMR6 *0_6
EMR7 *0_6
EMR8 *0_6

+3V_SS
C1248 1000p/50V_4
C1250 1000p/50V_4
C1246 1000p/50V_4

+1.05V_SS
+3V_SS
C1253 1000p/50V_4
C1252 1000p/50V_4
C1255 1000p/50V_4
C1254 1000p/50V_4
C1251 1000p/50V_4

+5V_SS
+3V_SS
C1267 1000p/50V_4
C1268 1000p/50V_4
C1270 1000p/50V_4
C1269 1000p/50V_4
C1266 1000p/50V_4

+5V_SS
+1.05V_SS
C1258 1000p/50V_4
C1257 1000p/50V_4
C1260 1000p/50V_4
C1259 1000p/50V_4
C1256 1000p/50V_4

+5V_SS
+1.05V_SS
C1263 1000p/50V_4
C1262 1000p/50V_4
C1265 1000p/50V_4
C1264 1000p/50V_4
C1261 1000p/50V_4

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Size:	Document Number: DDR4 DIMM0-RVS(4.0H)-CHA
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Size:	Document Number: DDR4 DIMM1-STD(5.2H)-CHB
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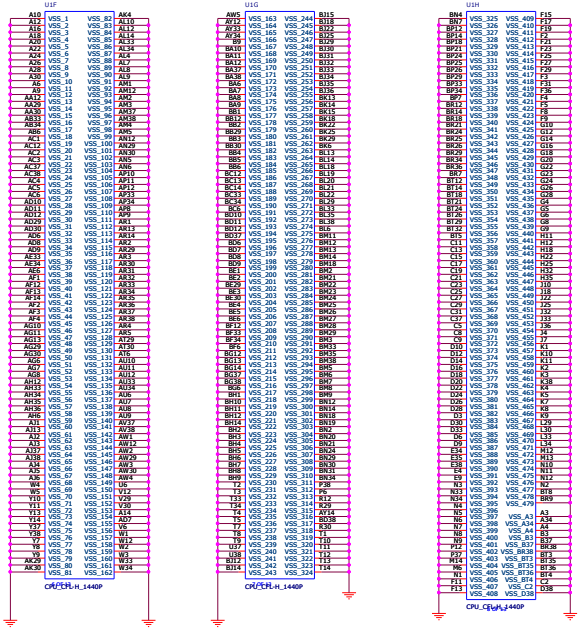
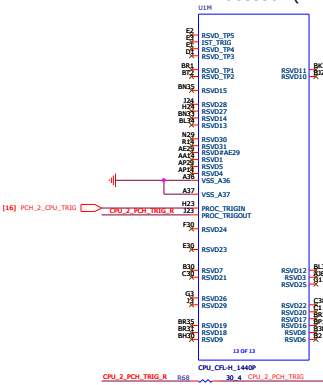
CFL-H Processor (GND)



KBL-H Processor (RESERVED, CFG)



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	CFL 7/7 (GND)		1A
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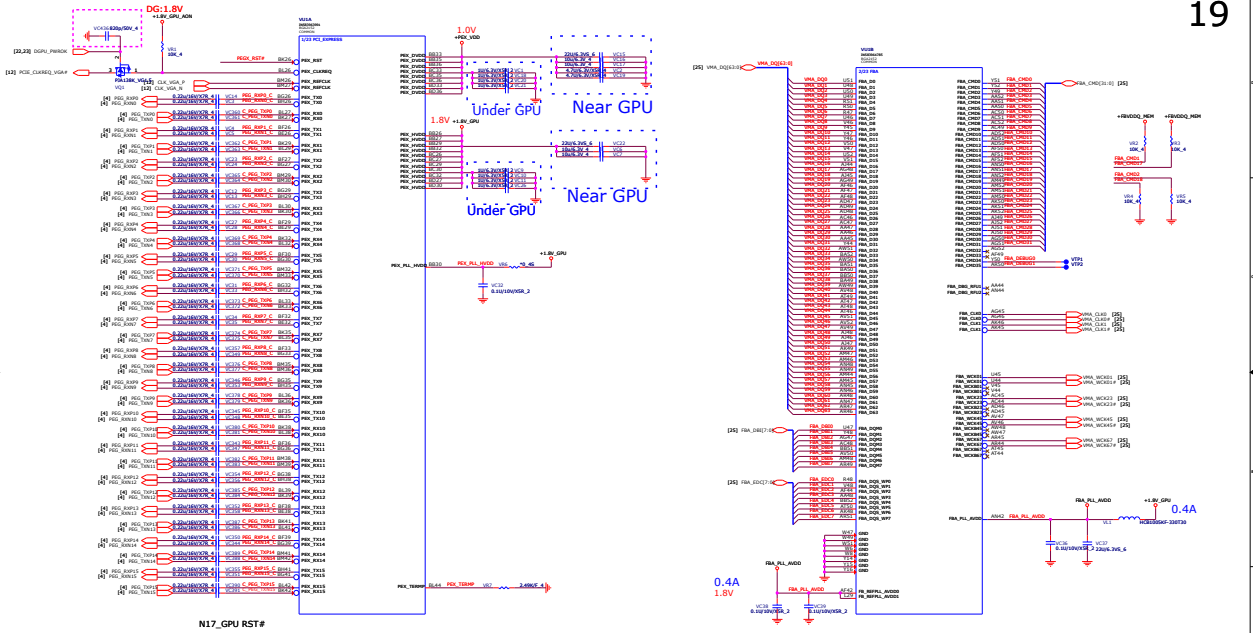
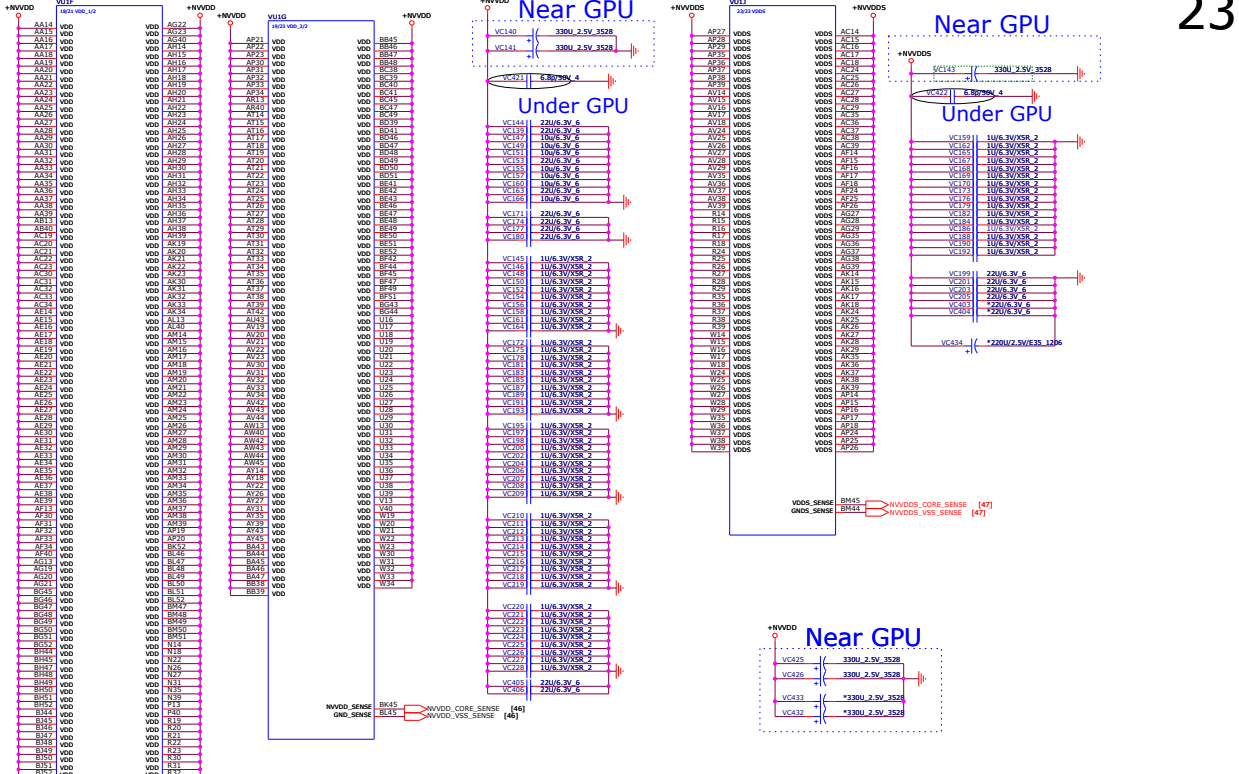

DG:1.8V
+1.8V_GPU_AON
Under GPU
Near GPU
1.0V
+PEX_VDD
1.8V
+1.8V_GPU
Under GPU
Near GPU
+1.8V_GPU
N17_GPU RST#
+1.8V_GPU_AON
Cb
Rg
Ub
RF
+PEX_VDD
+1.8V_GPU
+FBVDDQ_HDH
+FBVDDQ_HDH
FBA_PLL_AVDD
+1.8V_GPU
0.4A
1.8V
FBA_PLL_AVDD
0.4A


Near GPU
Under GPU
Near GPU
Under GPU
Near GPU
+NVVDD
+NVVDDS
VU1F
VU1G
VU1J
VC140 330U_2.5V_3528
VC141 330U_2.5V_3528
VC421 6.8U/20V_4
VC422 6.8U/20V_4
VC425 330U_2.5V_3528
VC426 330U_2.5V_3528
VC433 *330U_2.5V_3528
VC432 *330U_2.5V_3528
VDDS_SENSE BM45 NVVDDS_CORE_SENSE [47]
GNDS_SENSE BM44 NVVDDS_VSS_SENSE [47]
NVDD_SENSE BK45 NVVDD_CORE_SENSE [46]
GND_SENSE BL45 NVVDD_VSS_SENSE [46]
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Size
Document Number
N17E-G1-5/8 (Power)
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1A
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CHANNEL A: 2G/4G GDDR5

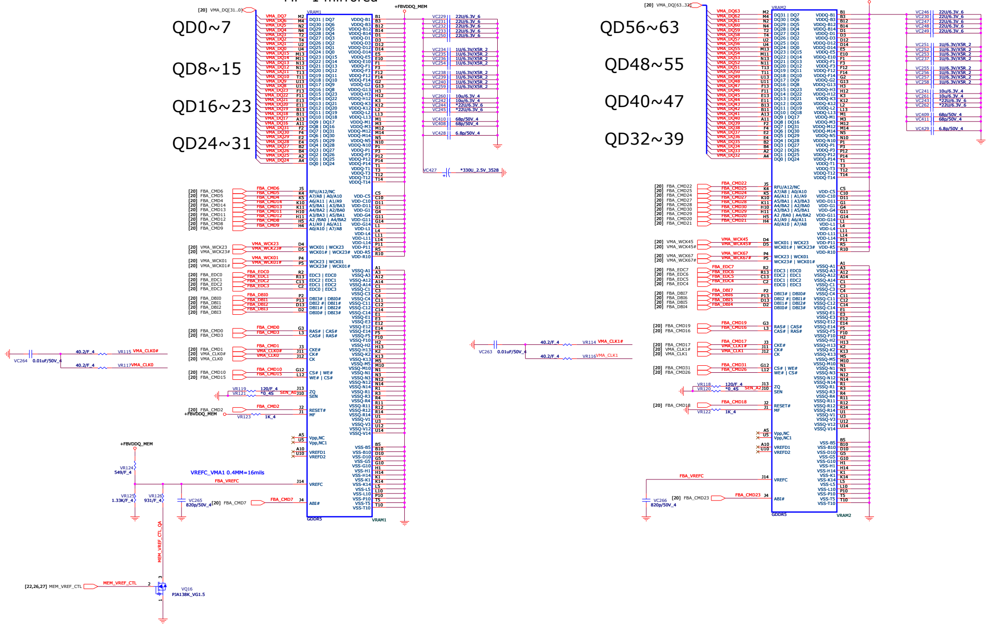


Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	**Channel 0 & 1**		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

CHANNEL B: 2G/4G GDDR5

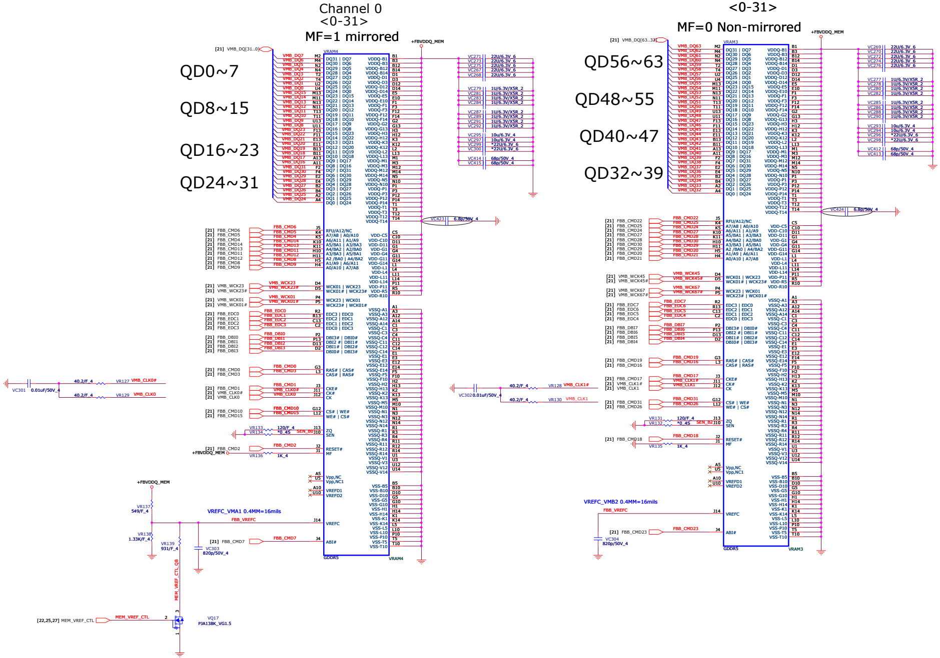
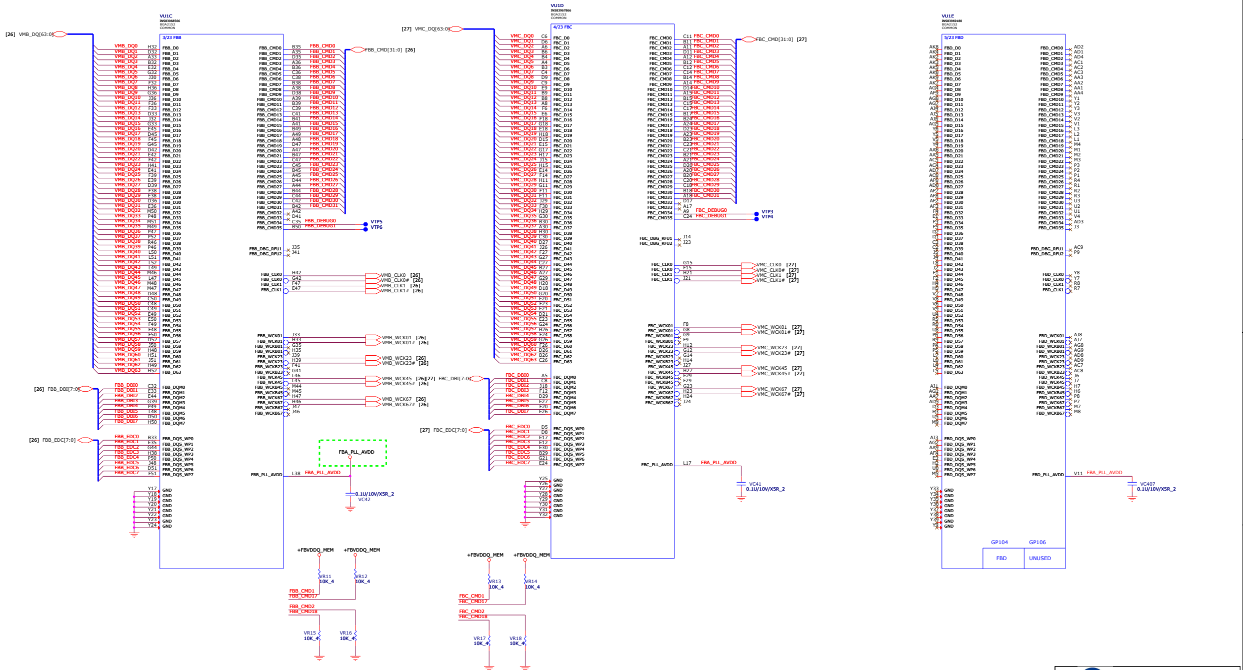


Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	**Channel 0 & 1**		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.


VU1C
3/23 FBB
VU1D
4/23 FBC
VU1E
5/23 FBD
[26] VMB_DQ[63:0]
[26] FBB_DBI[7:0]
[26] FBB_EDC[7:0]
FBB_CMD[31:0] [26]
[27] VMC_DQ[63:0]
[27] FBC_DBI[7:0]
[27] FBC_EDC[7:0]
FBC_CMD[31:0] [27]
VTP5
VTP6
VTP3
VTP4
VMB_CLK0 [26]
VMB_CLK0# [26]
VMB_CLK1 [26]
VMB_CLK1# [26]
VMB_WCK01 [26]
VMB_WCK01# [26]
VMB_WCK23 [26]
VMB_WCK23# [26]
VMB_WCK45 [26]
VMB_WCK45# [26]
VMB_WCK67 [26]
VMB_WCK67# [26]
VMC_CLK0 [27]
VMC_CLK0# [27]
VMC_CLK1 [27]
VMC_CLK1# [27]
VMC_WCK01 [27]
VMC_WCK01# [27]
VMC_WCK23 [27]
VMC_WCK23# [27]
VMC_WCK45 [27]
VMC_WCK45# [27]
VMC_WCK67 [27]
VMC_WCK67# [27]
FBA_PLL_AVDD
0.1U/10V/X5R_2
VC42
VC41
VC407
+FBVDDQ_MEM
VR11 10K_4
VR12 10K_4
VR13 10K_4
VR14 10K_4
VR15 10K_4
VR16 10K_4
VR17 10K_4
VR18 10K_4
FBB_CMD1
FBB_CMD17
FBB_CMD2
FBB_CMD18
FBC_CMD1
FBC_CMD17
FBC_CMD2
FBC_CMD18
GP104
GP106
FBD
UNUSED

Quanta Computer Inc.

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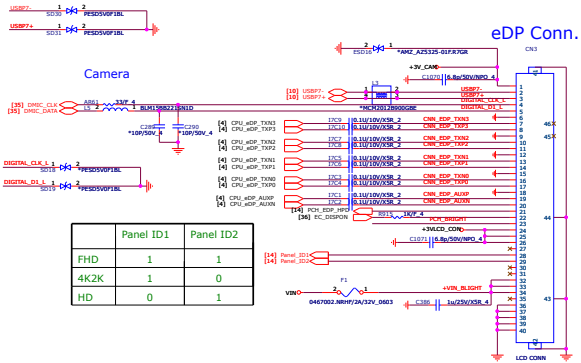
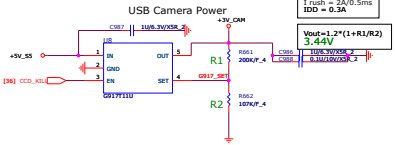
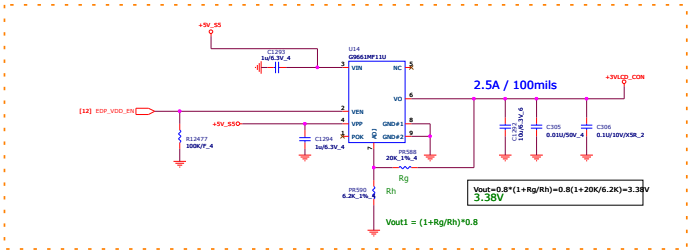


	Panel ID1	Panel ID2
FHD	1	1
4K2K	1	0
HD	0	1





4/3 PR Change

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Size: Document Number: eDP CONN/CAM/D-MIC Rev: 1A
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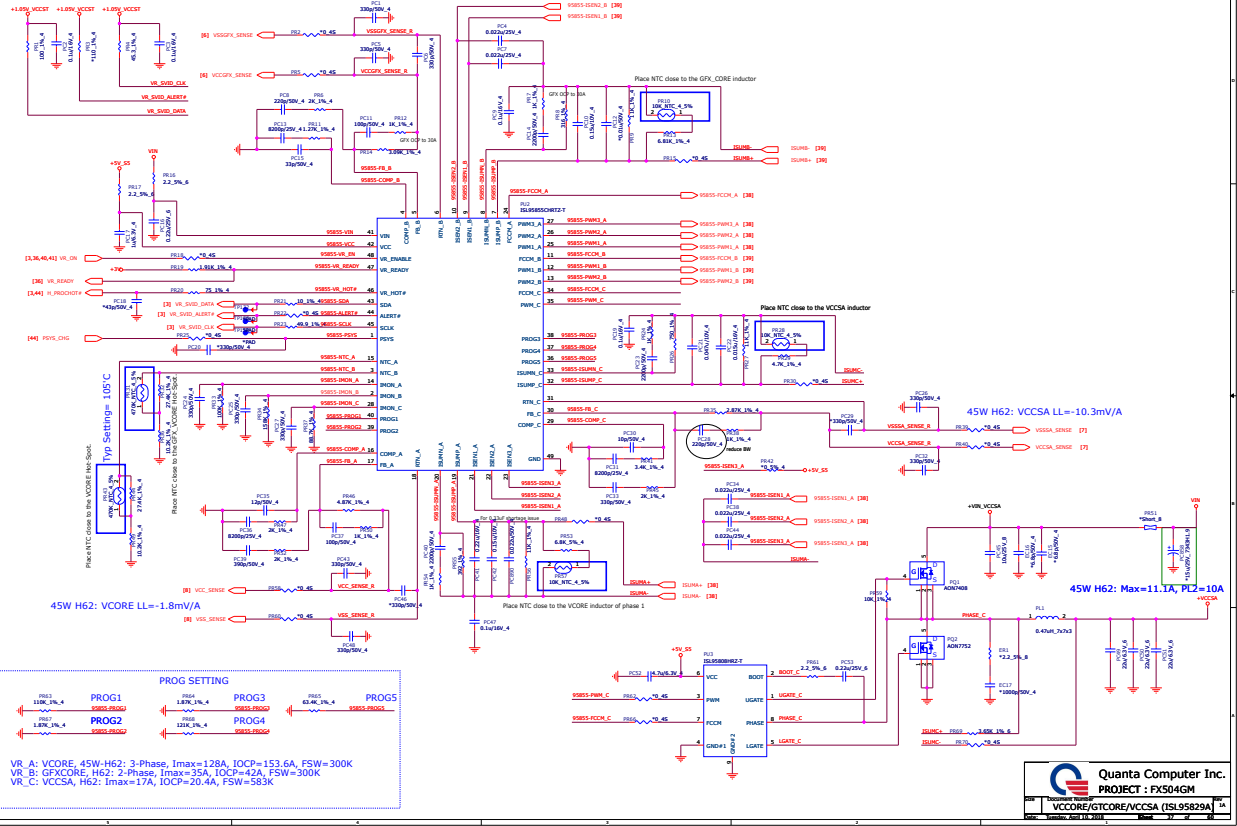
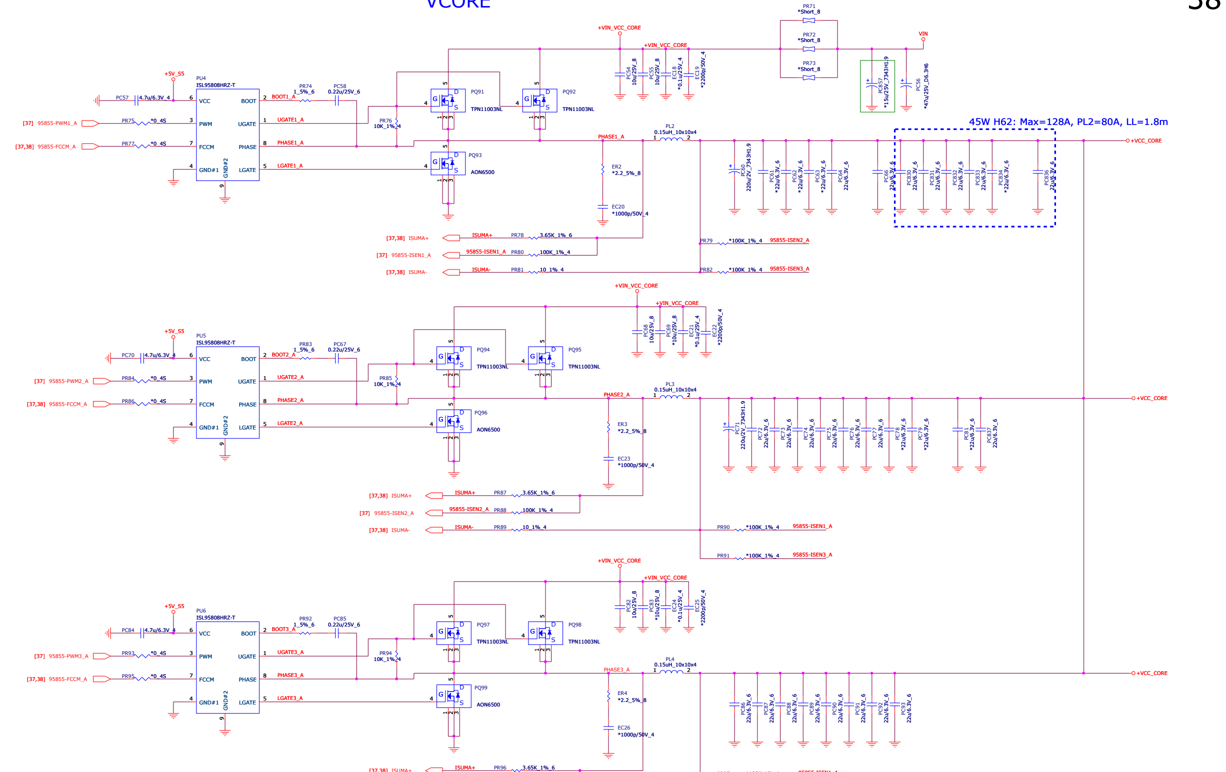

45W H62: GFX_CORE LL=-2.7mV/A
45W H62: VCORE LL=-1.8mV/A
45W H62: VCCSA LL=-10.3mV/A
45W H62: Max=11.1A, PL2=10A
Place NTC close to the GFX_CORE inductor
Place NTC close to the VCCSA inductor
Place NTC close to the VCORE inductor of phase 1
Place NTC close to the VCORE Hot Spot.
Place NTC close to the GFX_VCORE Hot Spot
Typ Setting= 105°C
PROG SETTING
PROG1
PROG2
PROG3
PROG4
PROG5
VR_A: VCORE, 45W-H62: 3-Phase, Imax=128A, IOCP=153.6A, FSW=300K
VR_B: GFXCORE, H62: 2-Phase, Imax=35A, IOCP=42A, FSW=300K
VR_C: VCCSA, H62: Imax=17A, IOCP=20.4A, FSW=583K
Quanta Computer Inc.
PROJECT : FX504GM
VCCORE/GTCORE/VCCSA (ISL95829A)
Tuesday, April 16, 2019

VCORE



Quanta Computer Inc.

PROJECT : FX504GM

Size	Document Number	Rev
	VCORE/GTCORE/VCCSA (ISL95829A)	1A

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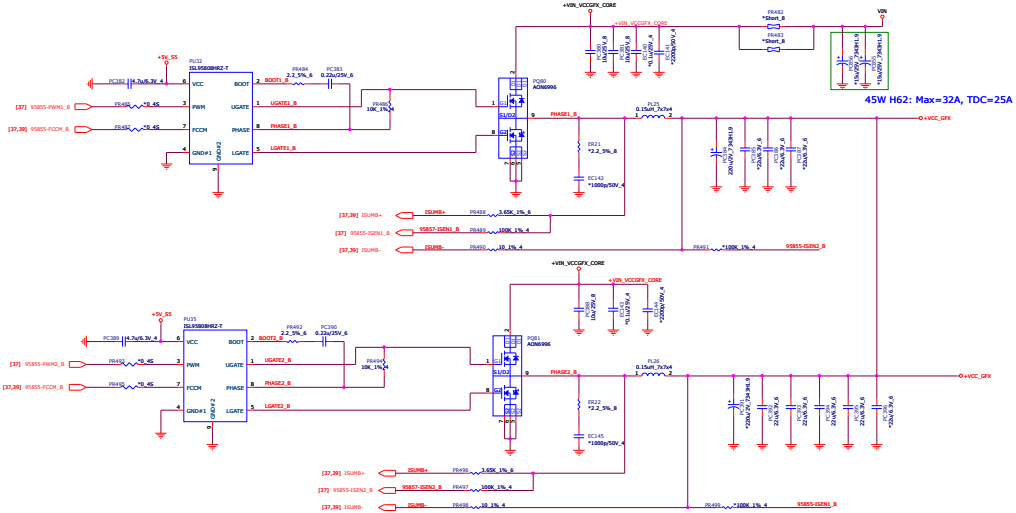
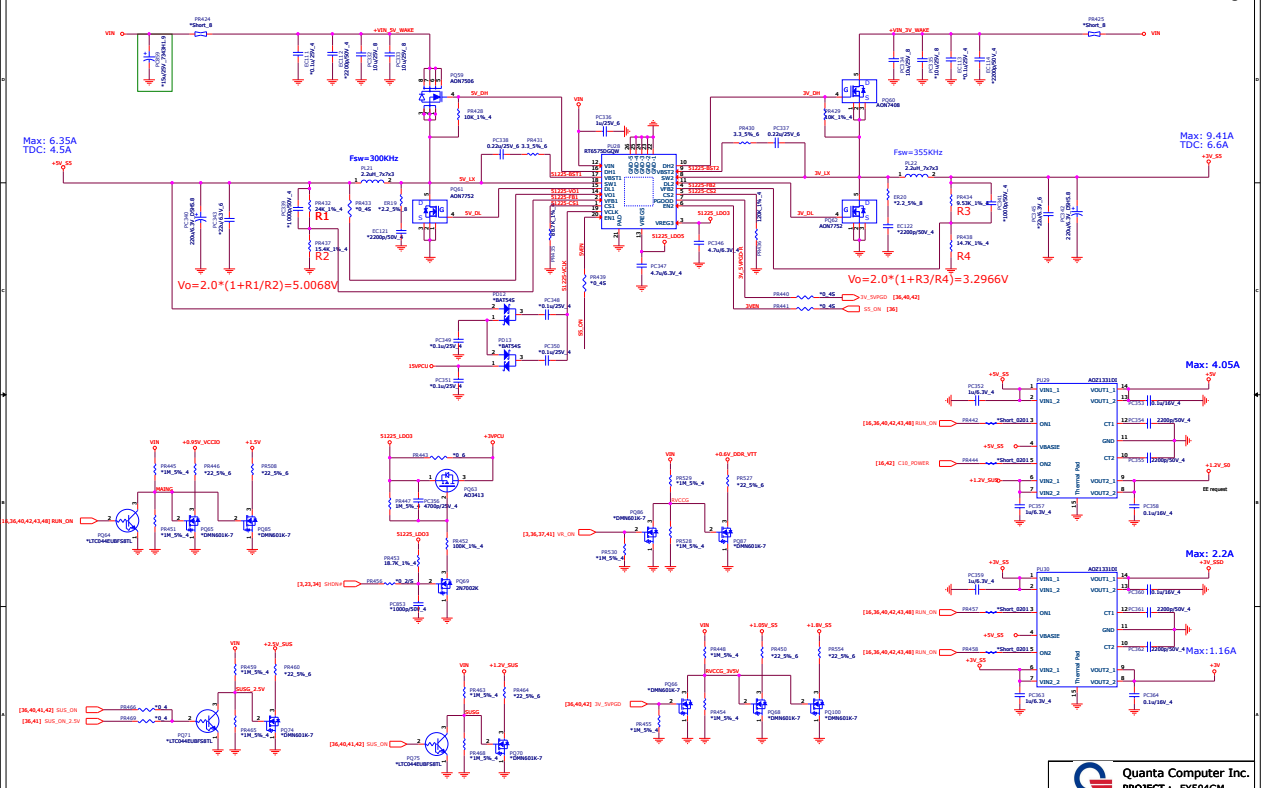
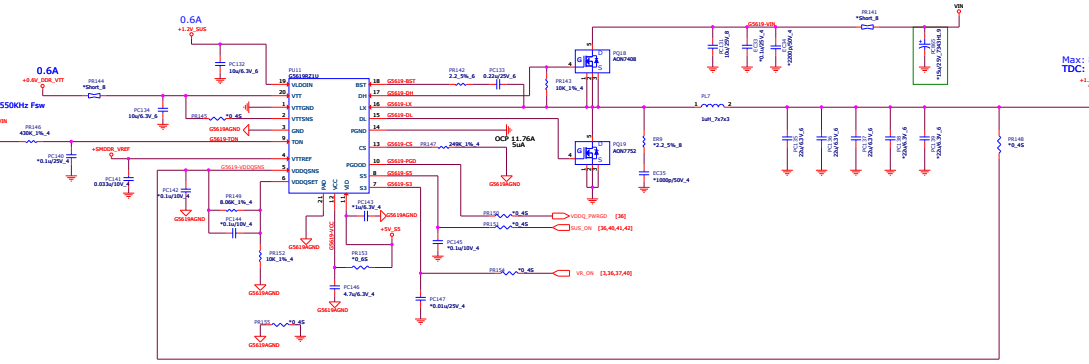
GFX_CORE



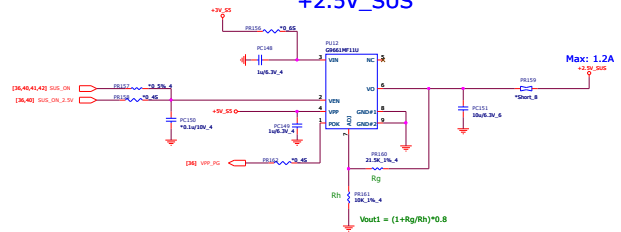
Quanta Computer Inc.		
PROJECT : FX504GM		
Size	Document Number	Rev
	GTCORE (ISL95829A)	1A
Date: Tuesday, April 16, 2019	Sheet 39 of 60	


Max: 6.35A
TDC: 4.5A
Fsw=300KHz
R1
R2
Vo=2.0*(1+R1/R2)=5.0068V
Max: 9.41A
TDC: 6.6A
Fsw=355KHz
R3
R4
Vo=2.0*(1+R3/R4)=3.2966V
Max: 4.05A
Max: 2.2A
Max:1.16A
Quanta Computer Inc.
PROJECT : FX504GM
1.2VSUS/VTT_MEM
Tuesday, April 10, 2018

1.2VSUS & VTT_MEM



+2.5V_SUS



Quanta Computer Inc.			
PROJECT : FX504GM			
Size	Document Number		Rev
	1.2VSUS/VTT_MEM		1A
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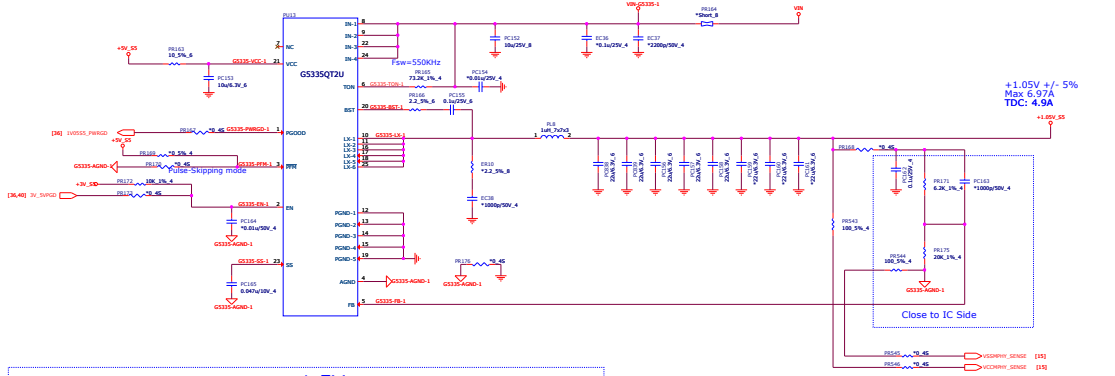
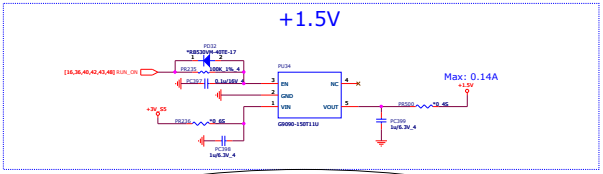
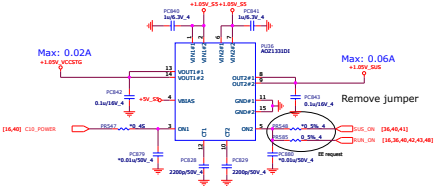
+1.05V_S5



+1.5V



1.8V_S5 circuit delete



Quanta Computer Inc.
PROJECT : FX504GM

Size	Document Number	Rev
	+1.0V_S5 / +1.5V	1A
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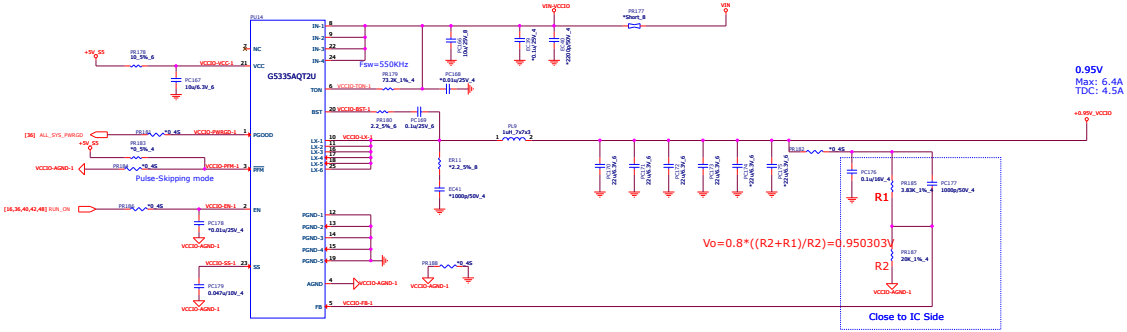
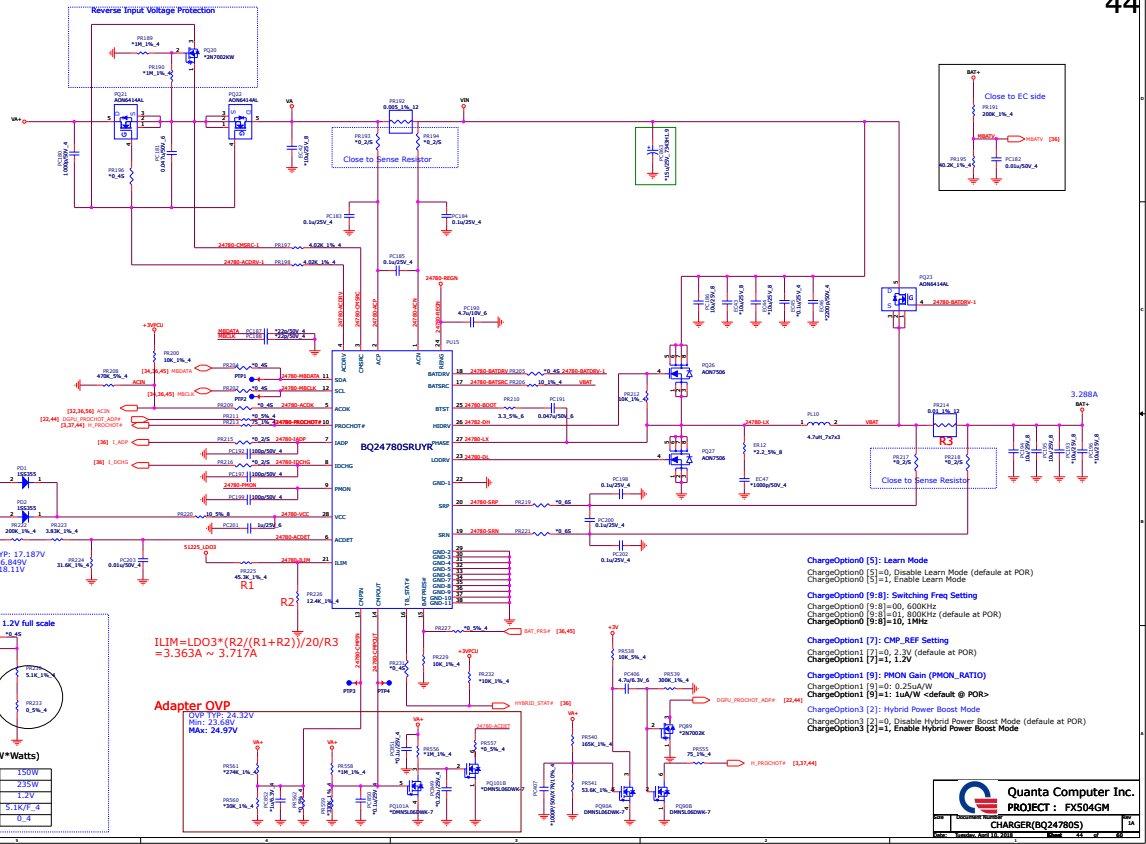
+VCCIO (Fix VCCIO=0.95V)





	ADP	150W
Full Scale	Psys	235W
	PSYS_CHG	1.2V
Location	PR230	5.1K/F_4
	PR233	0_4

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PROJECT : FX504GM
CHARGER(BQ24780S)
Size: A3 | Document Number: | Rev: 1A
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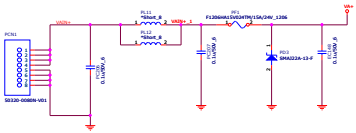
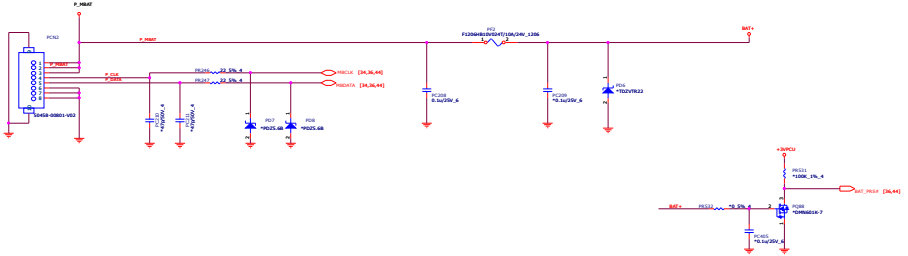
AC IN

AC ADAPTOR IN CONN



BAT IN



Quanta Computer Inc.		
PROJECT : FX504GM		
Size	Document Number	Rev
	ADP IN / BAT IN / Thermal Protection	1A
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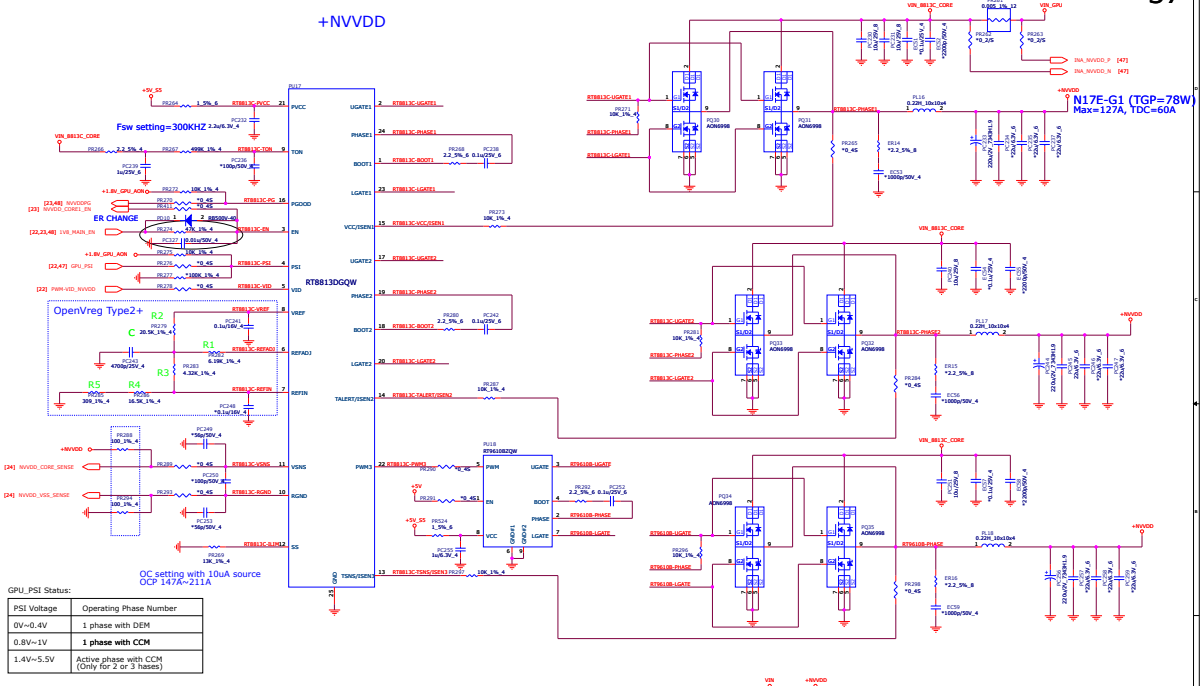
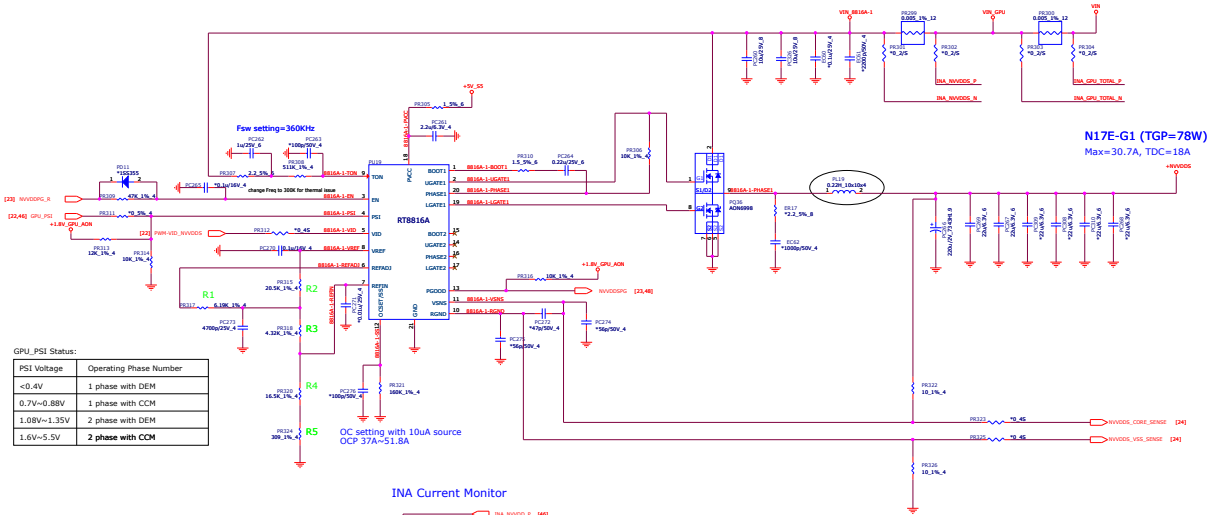

+NVVDD
Fsw setting=300KHZ
ER CHANGE
OpenVreg Type2+
OC setting with 10uA source
OCP 147A~211A
RT8813DGQW
RT8610BZQW
N17E-G1 (TGP=78W)
Max=127A, TDC=60A
GPU_PSI Status:
PSI Voltage | Operating Phase Number
0V~0.4V | 1 phase with DEM
0.8V~1V | 1 phase with CCM
1.4V~5.5V | Active phase with CCM (Only for 2 or 3 hases)
Quanta Computer Inc.
PROJECT : FX504GM
dGPU CORE (RT8813D)

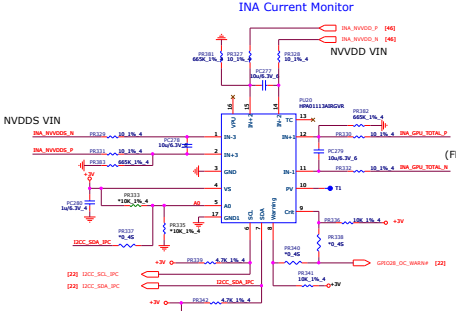
+NVVDDS



GPU_PSI Status:

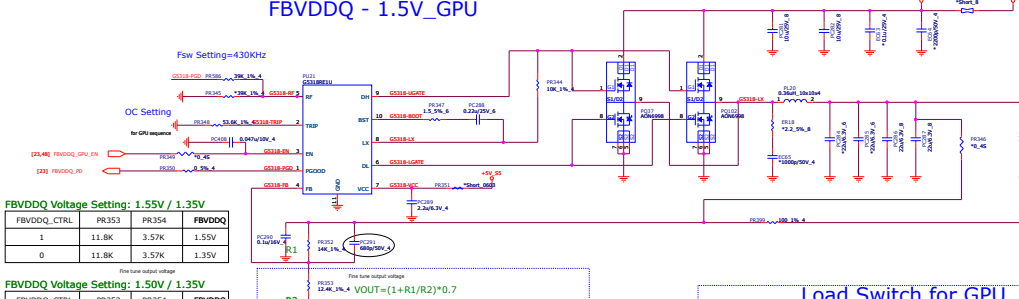
PSI Voltage	Operating Phase Number
<0.4V	1 phase with DEM
0.7V~0.88V	1 phase with CCM
1.08V~1.35V	2 phase with DEM
1.6V~5.5V	**2 phase with CCM**

INA Current Monitor

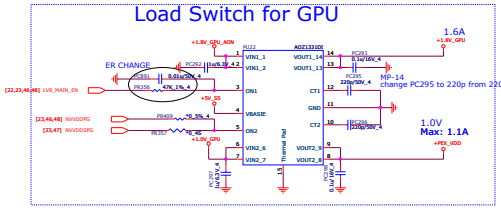


Address	HPA01113AIRGVR Pin5
0X80	10K to GND
0X84	**pin5 connect to pin7**

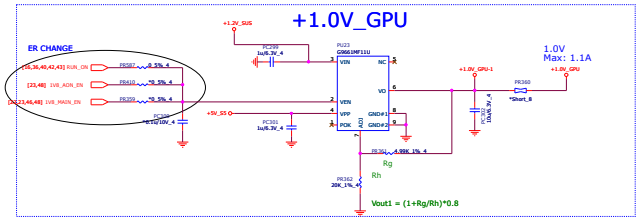
FBVDDQ - 1.5V_GPU



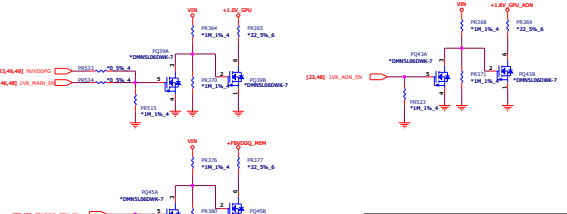
Load Switch for GPU



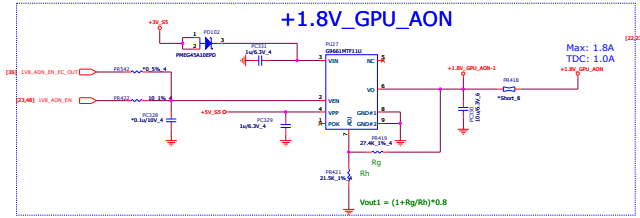
+1.0V_GPU



Discharge



+1.8V_GPU_AON



Quanta Computer Inc.			
PROJECT : FX504GM			
Size	Document Number		Rev
	+FBVDDQ (G5318)		1A
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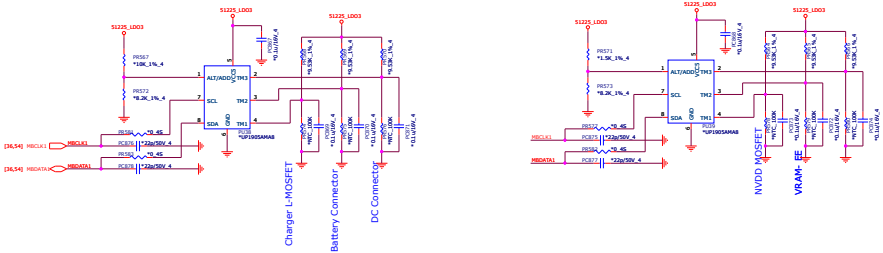

Quanta Computer Inc.			
PROJECT : FX504GM			
Size	Document Number		Rev
	POWER thermal protection		1A
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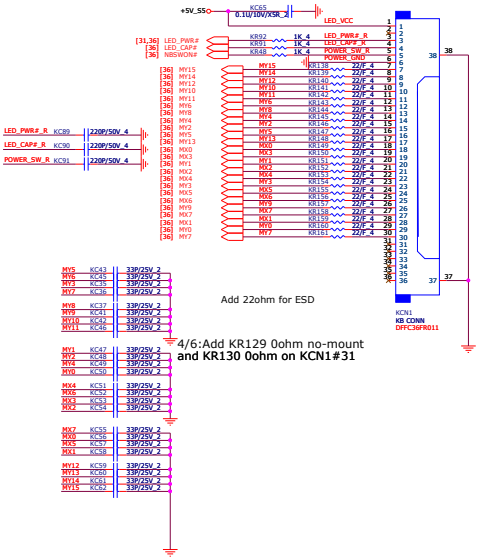
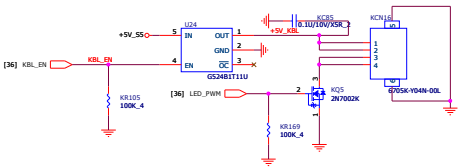
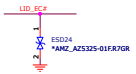
KEYBOARD Con.

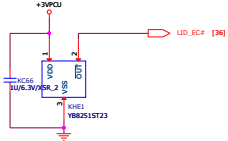


KEYBOARD BACKLIGHT Con.



ESD23 CLOSE TO KHE1





Quanta Computer Inc.
PROJECT : FX504GM

Size	Document Number	Rev
	DB/KB/LID	1A
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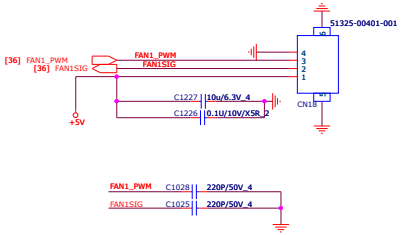
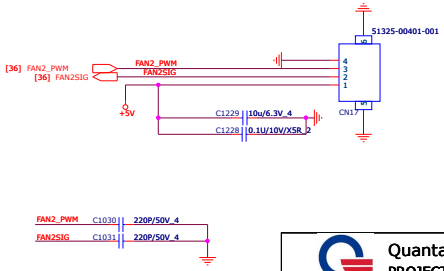
FAN1 for GPU



FAN2 for CPU



Quanta Computer Inc.
PROJECT : FX504GM

Size	Document Number	Rev
	FAN	1A
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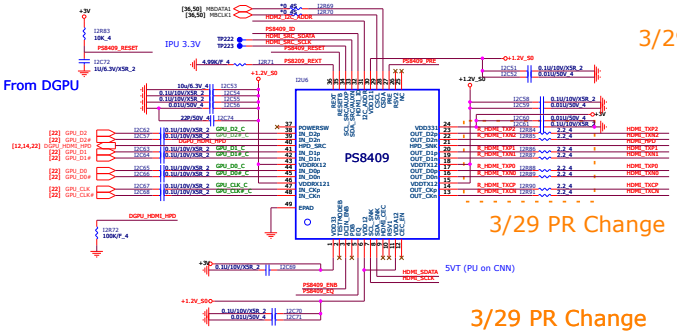
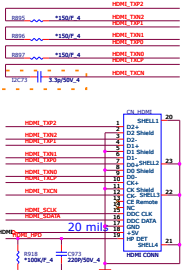
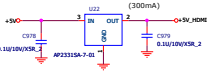
HDMI 2.0 Re-Drive



EMI Solution



4/5:Change I2R61 from 3.9K to 4.99K for EA



Quanta Computer Inc.	
PROJECT : FX504GM	
Size	Document Number: HDMI 1.4b Redriver
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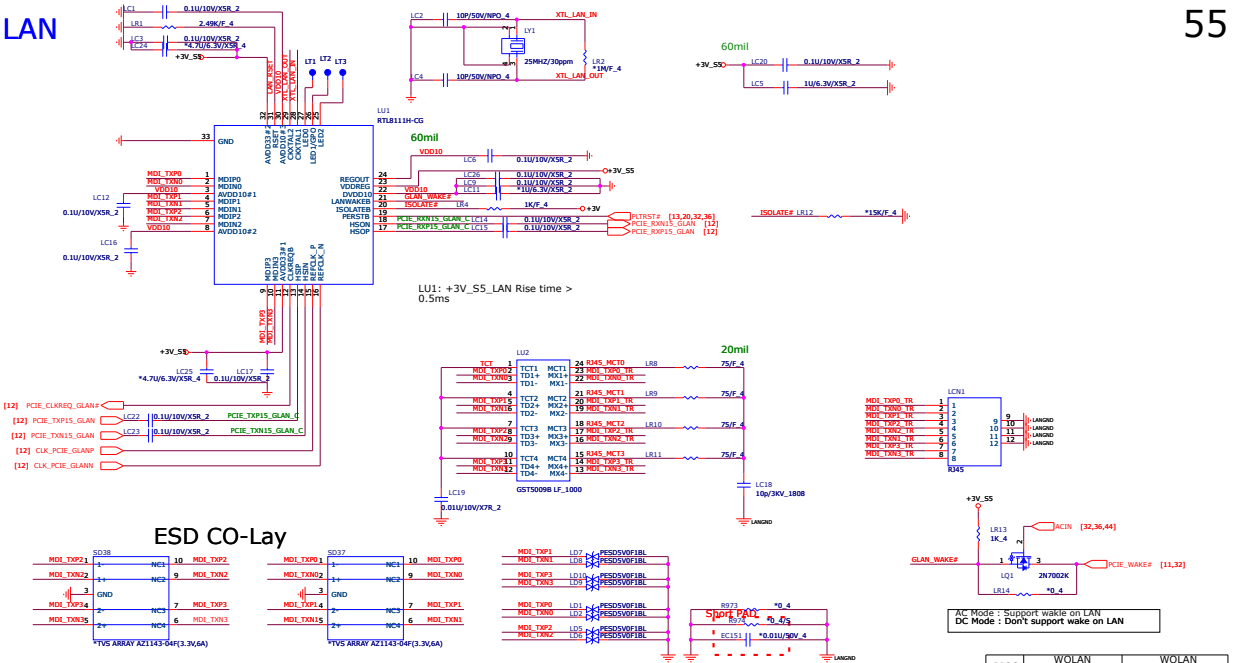
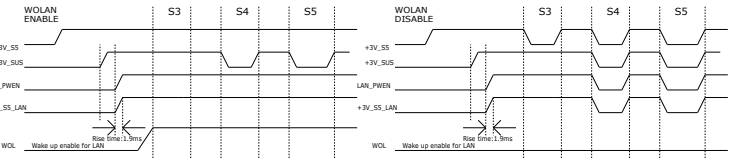
LAN



BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H



Quanta Computer Inc.
PROJECT : FX504GM

Size	Document Number	Rev
	LAN RTL8111H	1A
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Channel 0
<0~31>
MF=0 Non-mirrored

QD0~7
QD8~15
QD16~23
QD24~31

Channel 1
<0~31>
MF=0 Non-mirrored

QD56~63
QD48~55
QD40~47
QD32~39

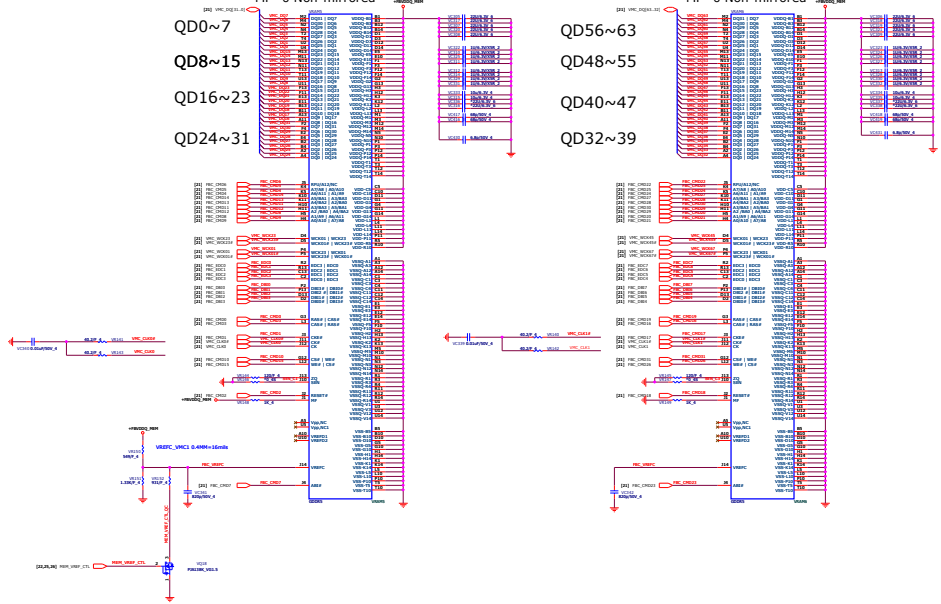
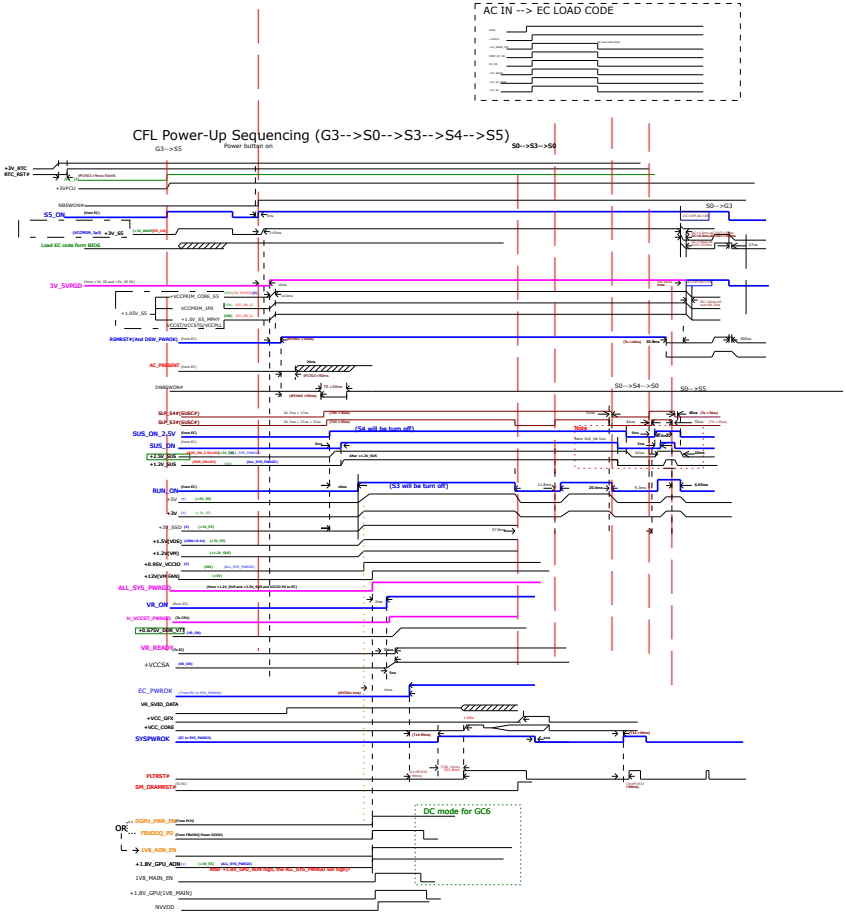
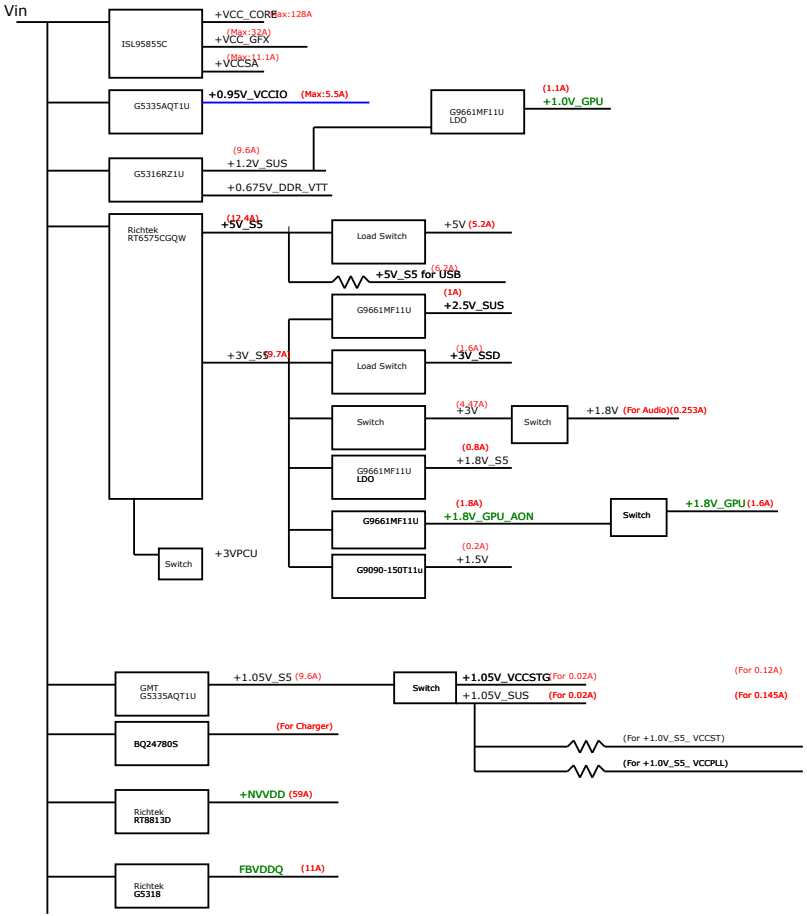


Table 7-5, GDDR5 Mode F Mapping

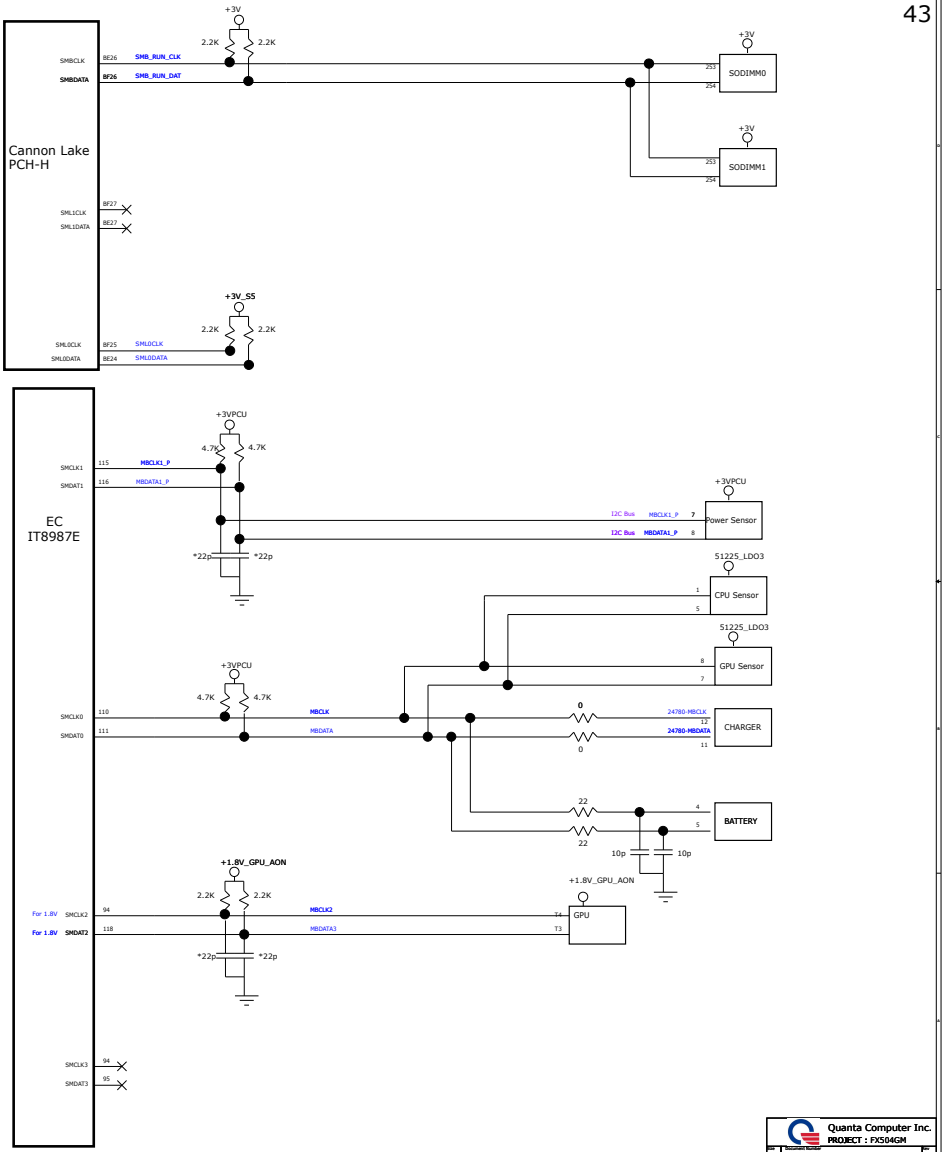
GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	BA5*	CMD19	BA5*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG2		
CMD35	DEBUG1		

Notes:
1. GPU default pull not connected to DRAM. See section 7.1.13.


AC IN --> EC LOAD CODE
CFL Power-Up Sequencing (G3-->S0-->S3-->S4-->S5)
G3-->S5
Power button on
S0-->S3-->S0
S0-->G3
S0-->S4-->S0
S0-->S5
+3V_RTC
RTC_RST#
+3VPCU
NRSWON#
SS_ON
(from EC)
+3V_SS
Load EC code form BIOS
3V_SVPGD
VCCPKIN_CORE_SS
VCCPKIN_UN
+1.05V_SS_MPHY
+1.05V_SS
RSMRST#(And DSW_PWROK)
(from EC)
AC_PRESENT
DNBSWON#
SLP_S4#(SUSC#)
SLP_S3#(SUSC#)
SUS_ON_2_5V
SUS_ON
+2.5V_SUS
+1.2V_SUS
(S4 will be turn off)
RUN_ON
+5V
+3V
+3V_SSD
+1.5V(VDD1)
+1.2V(VR)
+0.95V_VCCIO
+12V(VM/GNN)
ALL_SYS_PWRGD
VR_ON
H_VCCST_PWRGD
+0.675V_DDR_VTT
VR_READY
+VCCSA
(S3 will be turn off)
EC_PWROK
VR_SVID_DATA
+VCC_GFX
+VCC_CORE
SYSPWROK
PLTRST#
SM_DRAMRST#
DC mode for GC6
OR...
DGPU_PWR_EN
FBVDDQ_PD
1V8_AON_EN
+1.8V_GPU_AON
1V8_MAIN_EN
+1.8V_GPU(1V8_MAIN)
NVVDD



Quanta Computer Inc.
PROJECT : FX504GM
Size | Document Number: Power Diagram | Rev: 1A
Date: Tuesday, April 10, 2018 | Sheet 30 of 50



Quanta Computer Inc.
PROJECT : PX504GM
SMBUS

OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	S3		S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "x")	S5 (Fast Startup "x")	
RUN_ON	H	L		L	L	L	L	
+3V	H	L		L	L	L	L	
+5V	H	L		L	L	L	L	
+0.675V_DDR_VTT	H	L		L	L	L	L	
+12V	H	L		L	L	L	L	
+3V_SSD/+3V_PCH_CARD/+1.5V	H	L		L	L	L	L	
+1.05V_VCCSTG	H	L		L	L	L	L	
+VCCSA	H	L		L	L	L	L	
+VCC_GFX	H	L		L	L	L	L	
+VCC_CORE	H	L		L	L	L	L	
+0.95V_VCCIO	H	L		L	L	L	L	
SUS_ON	H	H		L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H		L	L	L	L	
+1.05V_SUS	H	H		L	L	L	L	
+1.2V_SUS	H	H		L	L	L	L	
SUS_ON_2.5V	H	H		L	L	L	L	
+2.5V_SUS	H	H		L	L	L	L	
S5_ON	H	H		H	L	L	L	
+1.8V_S5	H	H		H	L	L	L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	

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PR	1124 Change Page 12 & 14 HDMI HPD change to PCH GPP_F1 for BIOS request Page 22 Del VR37/VR41/VR43/VR44/VR51/VR52/VC60/VU3 for MS-Hybrid Design Page 32 Del C1238 for No Need Page 34 ADD TC3/TQ1 for Thermal Request Page 35 Modify AR13 to 10 Ohm from 0 Ohm for internal tracking Page 36 Del C1237 for No Need Page 36 Add KR72 to 200K for EC Stage ID Page 54 Modify I2R73/I2R75 to 10K Ohm from 2.2K Ohm for HDMI Detect Issue Page 54 DEL I2R79 for HDMI Detect Issue Page 54 Add I2R80 to 4.7K for HDMI Detect Issue Page 54 Add I2C73 to 3.3pF for HDMI2.0 SI Page 54 Modify I2R84/I2R85/I2R86/I2R87/I2R88/I2R89/I2R90/I2R91 to 2.2 Ohm from 0 Ohm for HDMI SI **0403 Change** Page 28 Modify LCD VCC Power Solution for Innolux TN120 Panel Issue
MP	

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