MS-7636 Ver: 1.0

uATX(244mm X 240mm)

CPU:

INTEL - Lynnfield/ Clarkdale LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH (H - 55)

OnBoard Chipset:

Clock Gen:ICS 4105B

HD Audio Codec:ALC889

LAN:RTL8111D 10/100/1000

SIO:F71889

Flash ROM: 64 Mb SPI (CHIP)

IDE X1 JMB-368

Main Memory:

DDRIII (800/1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot *1

PWM:

Controller: uP6206
(3-Phase use STD MOS -- 95W)

OV by uP6264 or SIO
uP6103 (CPU_VTT)
Linear (PCH)
uP6103(DDR)
GPU Power -ISL6314

ACPI:

uPI+SIO

Other:

SATA(SATA2-300MB/s) *6
USB2.0 *10 (Rear*4 / Front*6)
PRINT Header *1
COM pin header *2
TPM Header *1
on BOARD BUZZER
D-SUB *1
DVI PORT*1
HDMI PORT*1

BOM SKUs

H55:chiset
S:solid cap
EL:EL cap
G:giga lan 8111DL
M:Miga lan 8103EL
6: 6 ports
DVI: DVI Stuff

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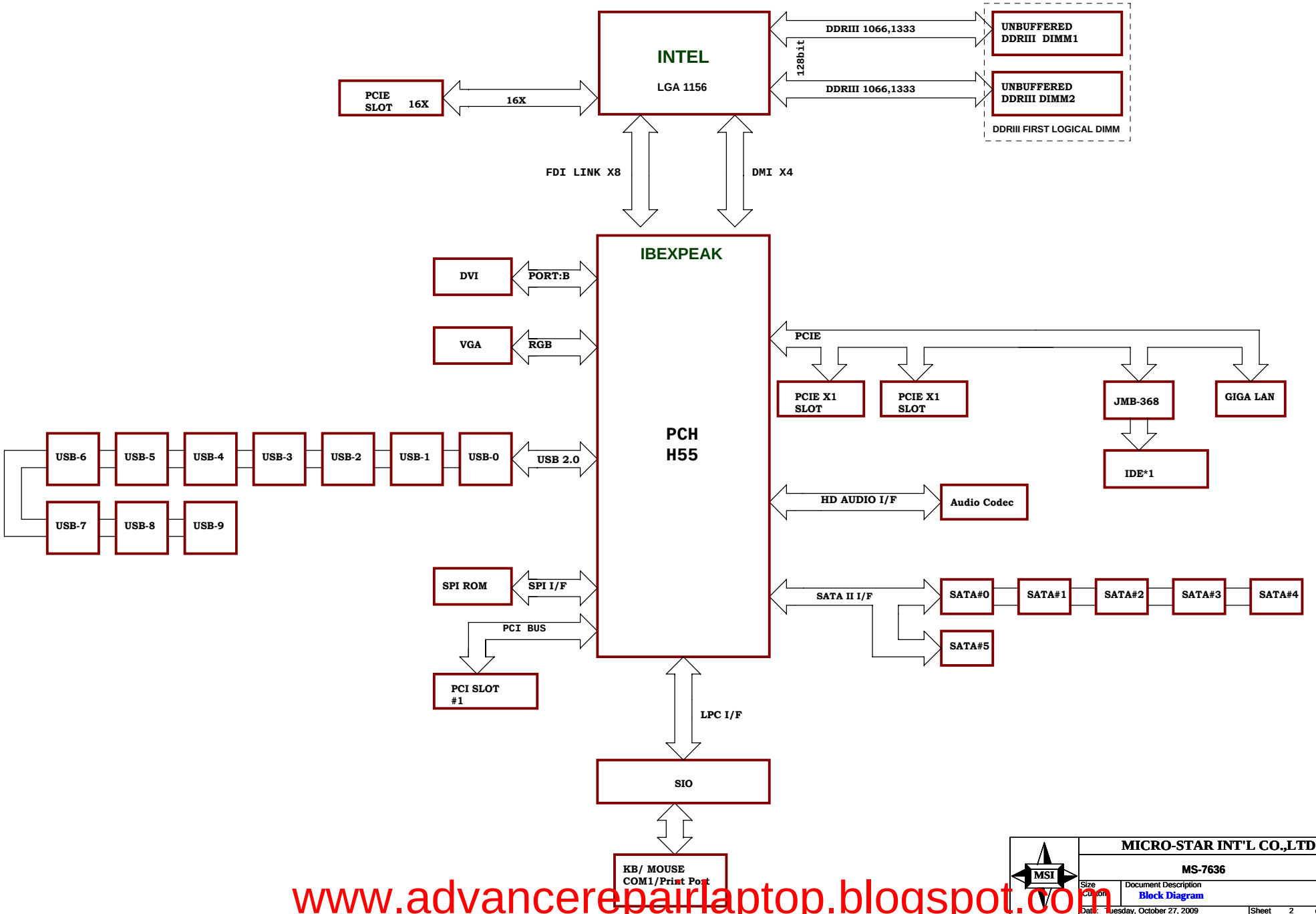
MS-7636

Size: Custom | Document Description: Cover Sheet | Rev: 1.0

Date: Wednesday, October 28, 2009 | Sheet 1 of 38



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Size: Custom | Document Description: Block Diagram | Rev: 1.0

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DDR DIMM config.

Device	Address	Clock	
CHA DIMM1	10100001B	MEM_MA_CLK_H0/L0	H1/L1
CHB DIMM2	10100000B	MEM_MB_CLK_H0/L0	H1/L1

PCI Config

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#A PCI_INT#B PCI_INT#C PCI_INT#D	PCI_REQ0# PCI_GNT0#	AD16	PCH CLKOUT_PCI<0>
TPM				PCH CLKOUT_PCI<3>
SIO				PCH CLKOUT_PCI<2>

TABLE 9
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #x	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#_PCH	PCISLOT1
PLTRST_BU1#	JMB368 IDE
PLTRST_BU2#	PCIE*16 / *1
PLTRST_BU3#	LAN&TPM
PLTRST#	SIO

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Size: Custom | Document Description: Device Map | Rev: 1.0

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History

1.2009-10-13 Change VCC_SENSE to CPU_VCC_SENSE
2.2009-10-13 Add HDMI circuit,change USB circuit,JSP1 circuit update
3.2009-10-13 update NCT3016 circuit ,add VTIN3 circuit for VRM MOS
4.2009-10-18 Add C589 C590
5.2009-10-18 Add R561 R562 For HDMI HPDET
6.2009-10-20 Add R602,Swap HDMI wire for layout
7.2009-10-21 NCT3016 circuit update:add R637 Q65 R592,Change U27 pin16 tp NCT_GPIO16,delete C121
8.2009-10-21A   NCT3016 citcui update:add Q85,chang SATA1&SATA2 to SATA1_2
9.2009-10-23   change JUSB2 & JUSB1 for layout
10.2009-10-23A   NCT3016 circuit update:add R850
11.2009-10-24   delete VCCGATE and DUALGATE circuit
12.2009-10-26   delete C534
13.2009-10-26   Swap RN40

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C	History	1.0

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AA8/Y8 ,these signals for 120 MHz from the Intel?5 Series Chipset CLKOUT_DP_P /CLKOUT_BCLK1_P and CLKOUT_DP_N / CLKOUT_BCLK1_N. Leave as NC on the PCH and connect directly to GND at the processor. 120MHz clock is used for embedded DisplayPort which is no supported on Desktop designs.

CPU1E

BACK SIDE

For DP port

MISC

5 OF 12

N12-160A010-F02

demo board no connect

if not use XDP,add Test point

CFG 0~5 HAVE INTERNAL PULL-UPS

demo board empty
check list not empty

CPU1C

PEG

DMI

3 OF 12

CPU1D

VDDIO

DISPLAY LINK

4 OF 12

Break-out:10mil width, 6 mil space
Other Area:10mil width, 15 mil space

CPU reset

reserve

PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

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Size: Custom | Document Description: CPU-CNTL/CLK/MISC | Rev: 1.0

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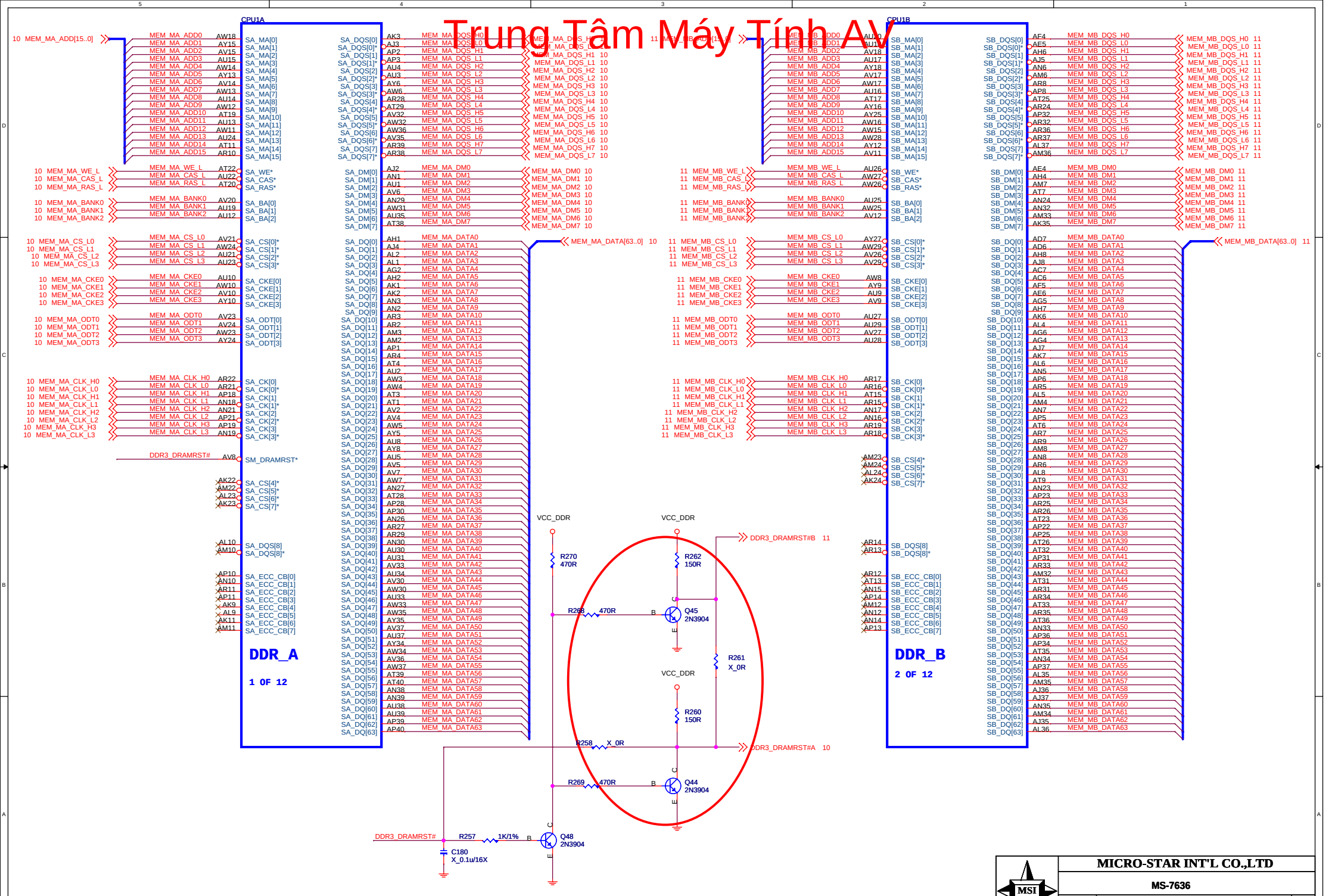

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MS-7636		
Size: Custom	Document Description: CPU-Memory	Rev: 1.0
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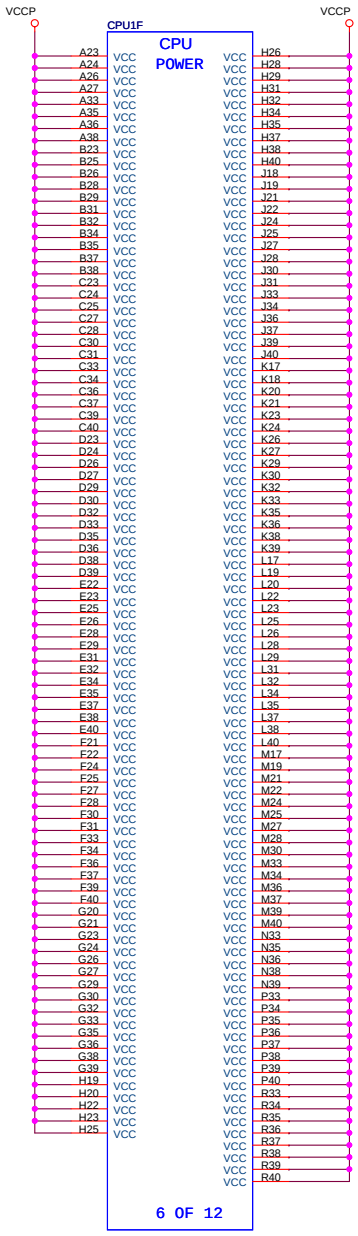
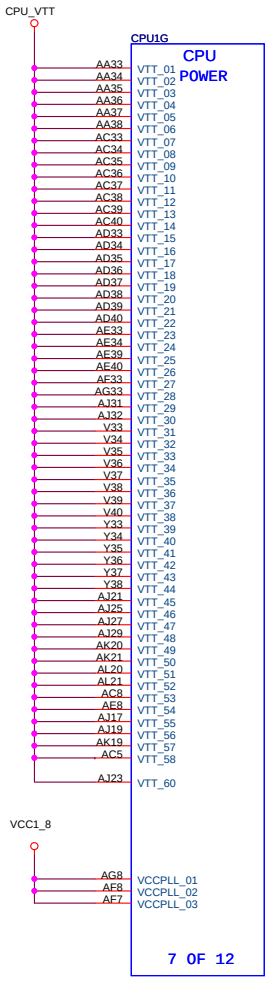
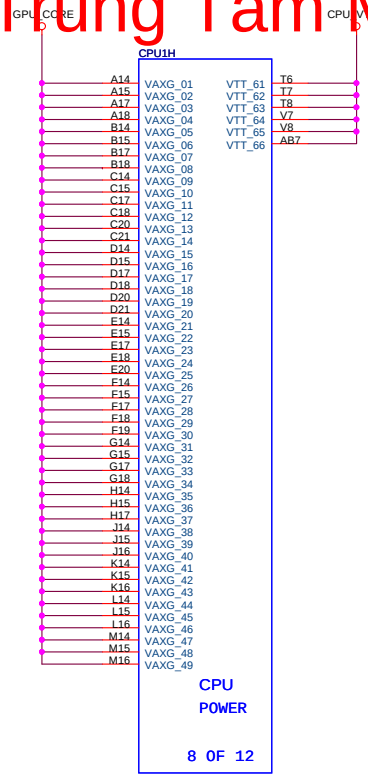
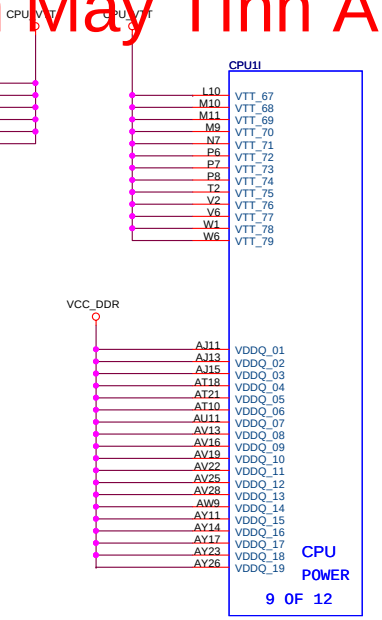
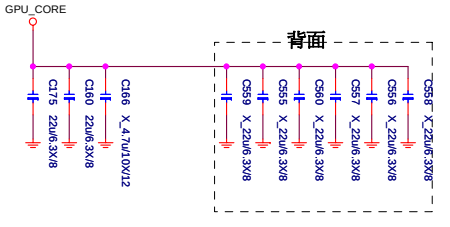






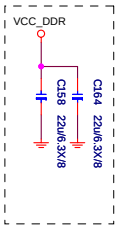


GPU_CORE Decoupling



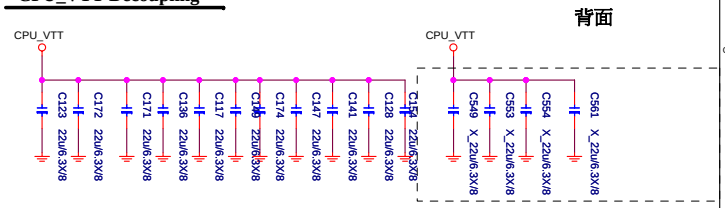
CPU SOCKET CAVITY CAPS

VCC_DDR-Decoupling



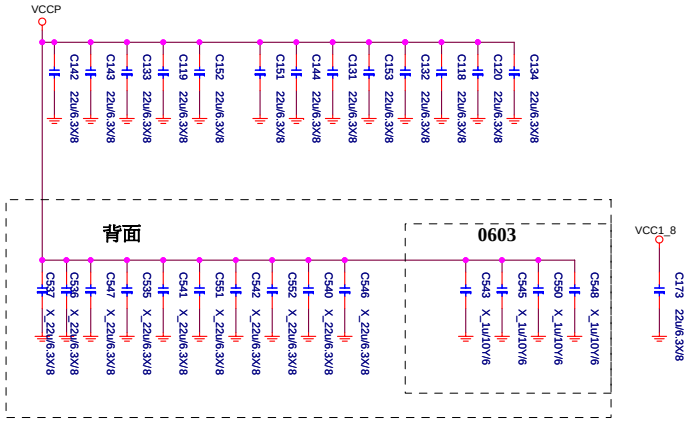
CPU SOCKET CAVITY CAPS

CPU_VTT Decoupling



CPU SOCKET CAVITY CAPS

CPU_VCCP-Decoupling



CPU SOCKET CAVITY CAPS

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7636	
Size: Custom	Document Description: CPU-Power	Rev: 1.0
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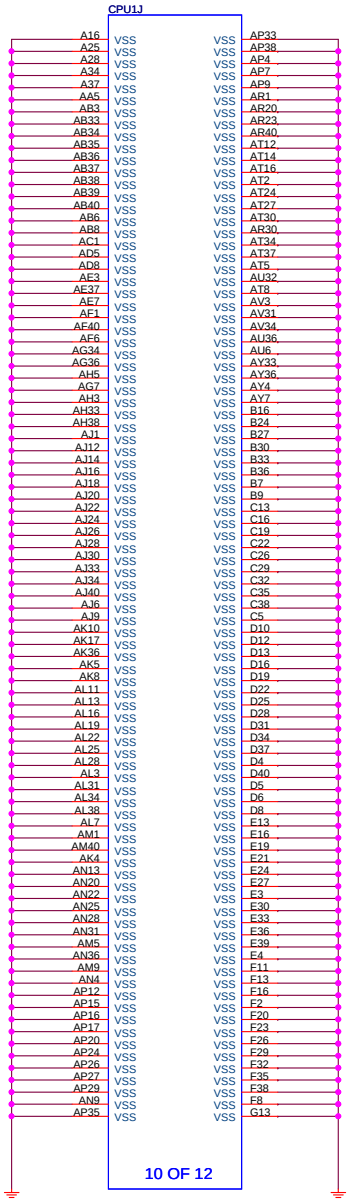
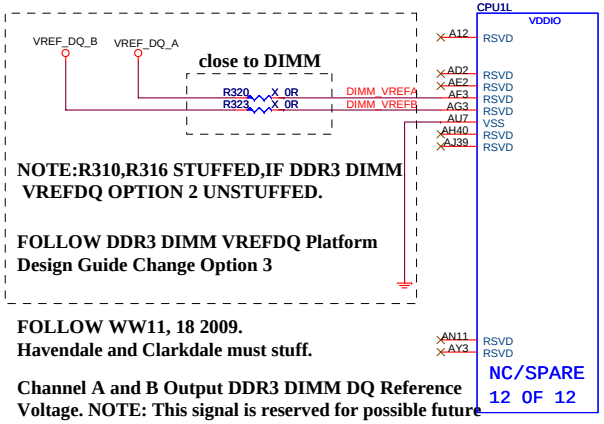
stuff or unstuff ?????





NOTE:R310,R316 STUFFED,IF DDR3 DIMM VREFDQ OPTION 2 UNSTUFFED.

FOLLOW DDR3 DIMM VREFDQ Platform Design Guide Change Option 3

FOLLOW WW11, 18 2009.
Havendale and Clarkdale must stuff.

Channel A and B Output DDR3 DIMM DQ Reference Voltage. NOTE: This signal is reserved for possible future use, and may not be driven on initial steppings. Refer to the Platform Design Guide for DIMM DQ VREF implementation details.

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Size: Custom	Document Description: CPU-GND	Rev: 0A
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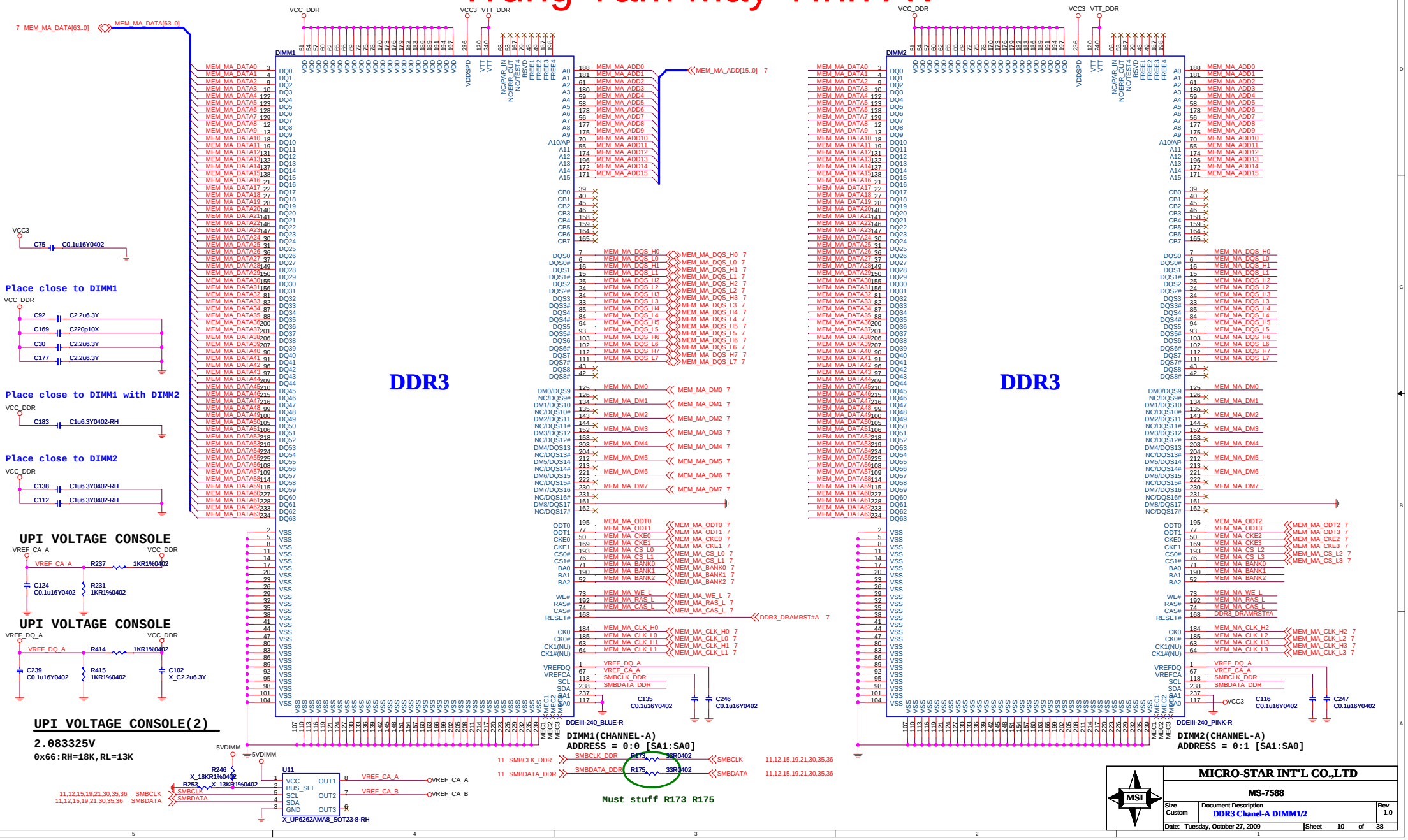
DDRIII DIMM_A1

DDRIII DIMM_A2



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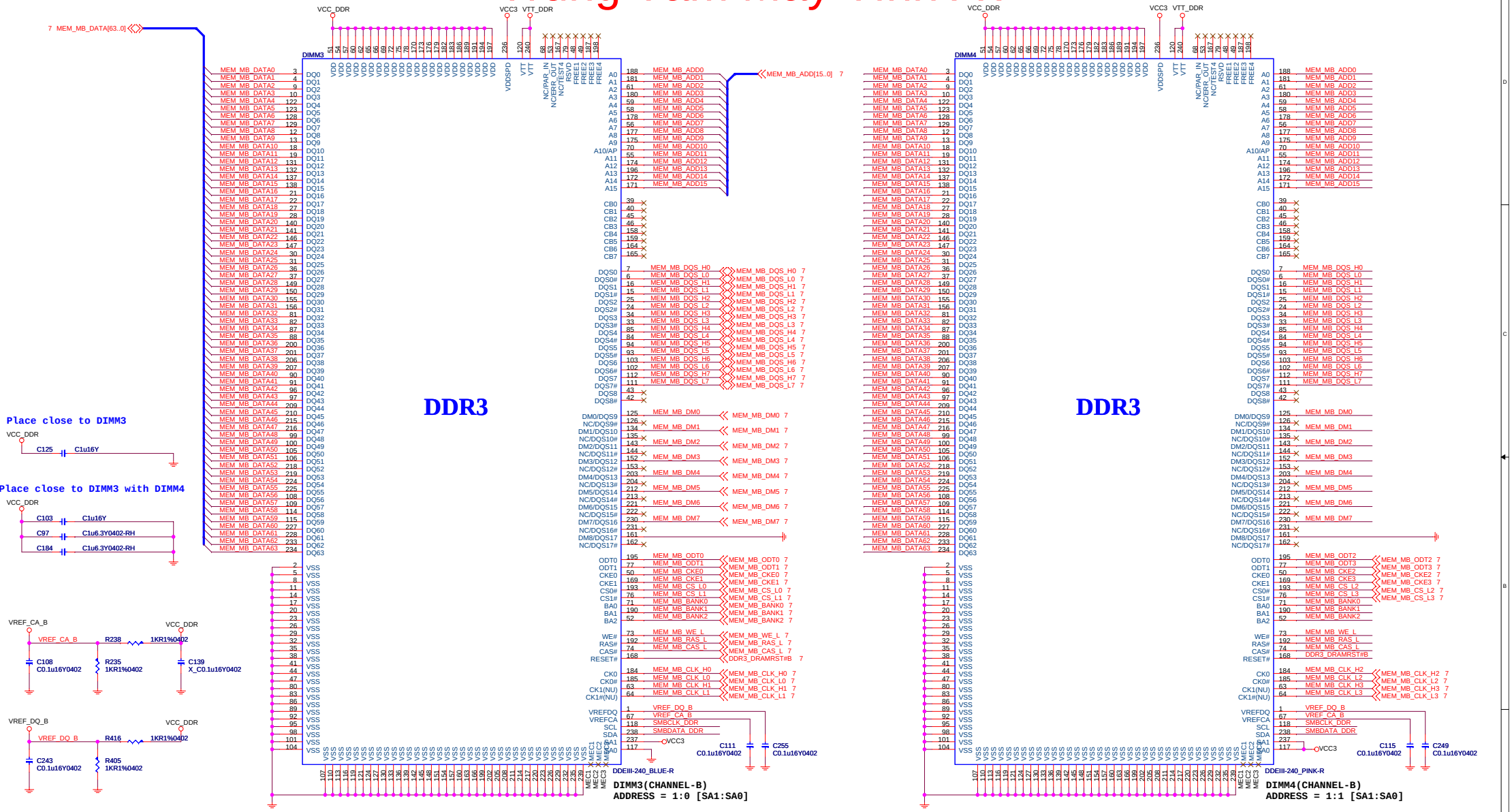
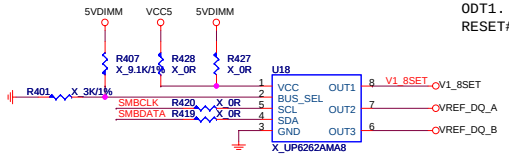
MS-7588	
Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
Rev: 1.0	
Date: Tuesday, October 27, 2009	Sheet 10 of 38

DDRIII DIMM_B1

DDRIII DIMM_B2



UPI VOLTAGE CONSOLE(3) 0x68:RH=9.1K,RL=3K



Vref-DQ : Reference voltage for DQ0 DQ63, CB0 CB7 and PAR_IN. When in single ended mode used for DQS0 DQS7.

Vref-CA : Reference voltage for A0-A15, BA0 BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

MICRO-STAR INT'L CO.,LTD	
MS-7588	
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4
Rev: 1.0	
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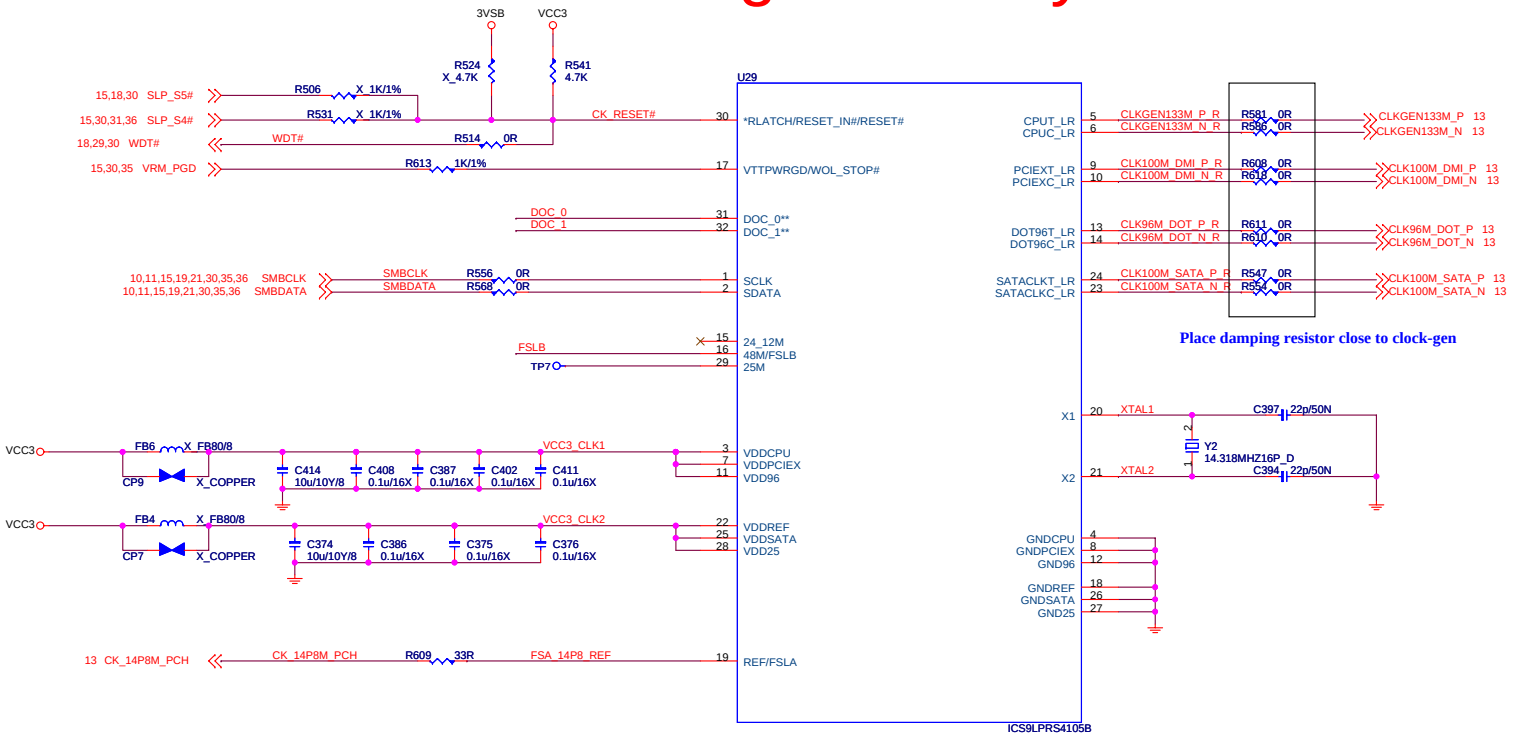
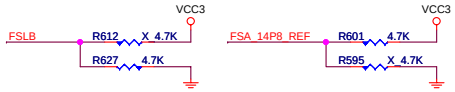


CLOCK GEN STRAPING

FS4 B0b4	FS3 B0b3	FS2 B0b2	FSB B0b1	FSA B0b0	CPU Mhz	Spread %
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5



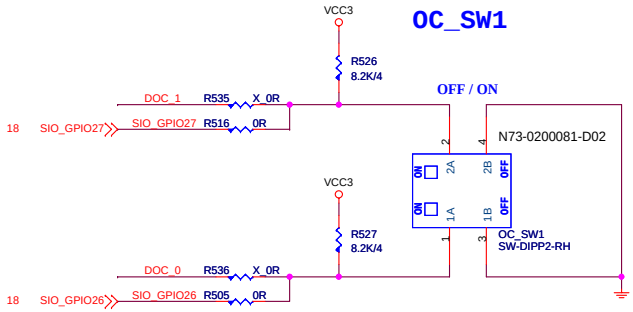
Pin16: 48MHz clock output. / 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values.

Pin19: 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.

OC

DOC_0**:Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2C.

OC_SW1

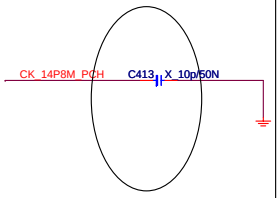


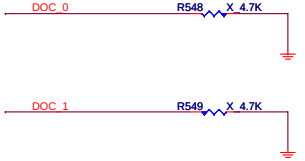
OFF=1 ; ON=0

DOC		TABLE
1	0	CPU FREQUENCY
1	1	133 MHz (default)
1	0	142 MHz
0	1	150 MHz
0	0	166 MHz

(Default) OFF / OFF
OFF / ON
ON / OFF
ON / ON

EMI





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Size	Document Description	Rev
Custom	CLK ICS9LRS4105B	1.0

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PCI Express port 7 and 8 are not available for the H55,

USB port 6 and 7 are not available for the H55,

PCH1A

IBEXPEAK_A

PCI-E

USB

DMI

1 OF 9

Programmable output clock to 48MHZ

unuse

Place near SB

PCH1C

IBEXPEAK_A

CLOCK

CLOCK_IN

3 OF 9

IBEX_0

PCH1B

IBEXPEAK_A

PCI

2 OF 9

For EMI

PCICLK LOOPBACK

DCI:Must stuff 25M crystal when use vga

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

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Size: Custom | Document Description: IBEXPEAK-PCIE/DMI/USB/CLK | Rev: 1.0

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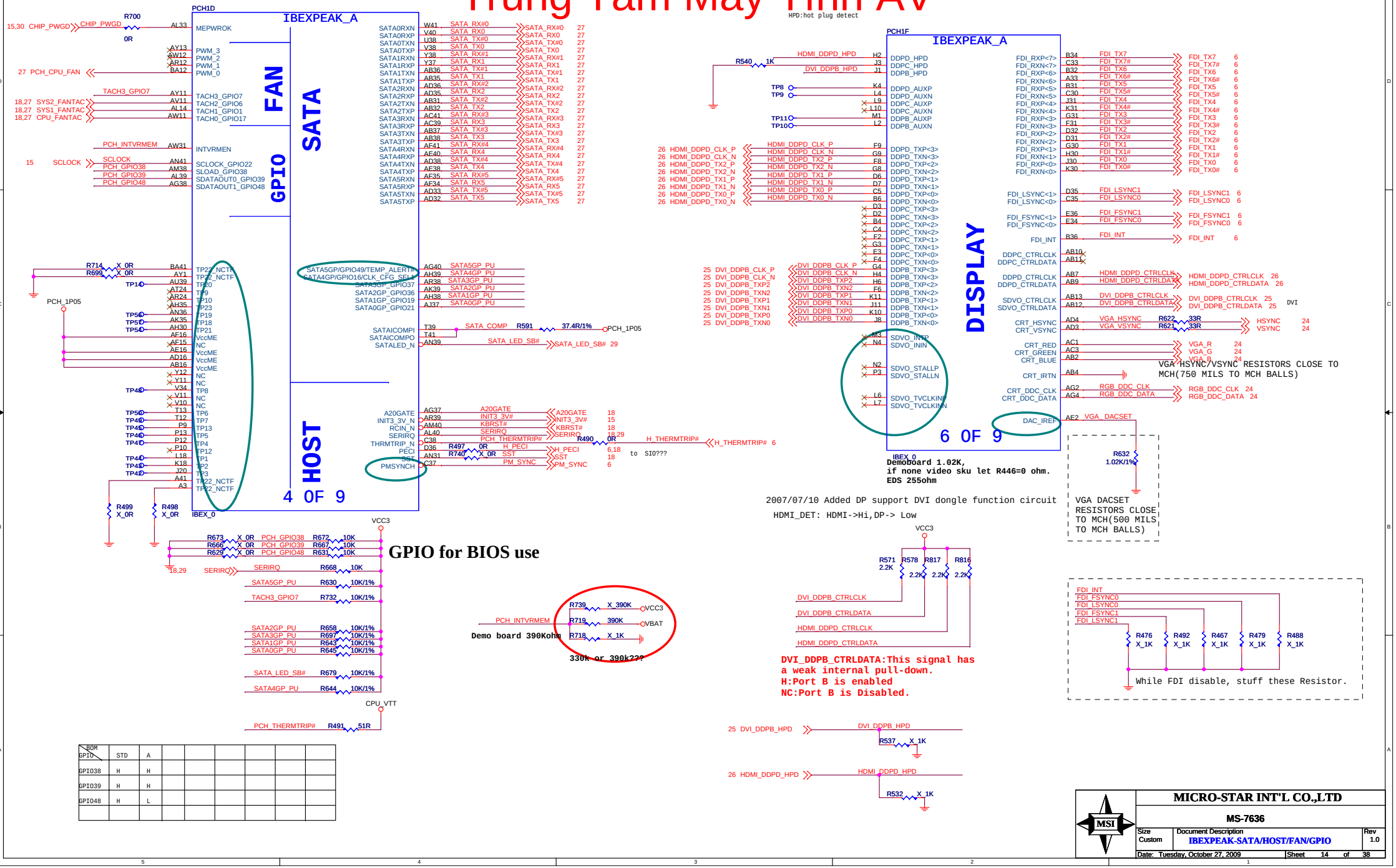
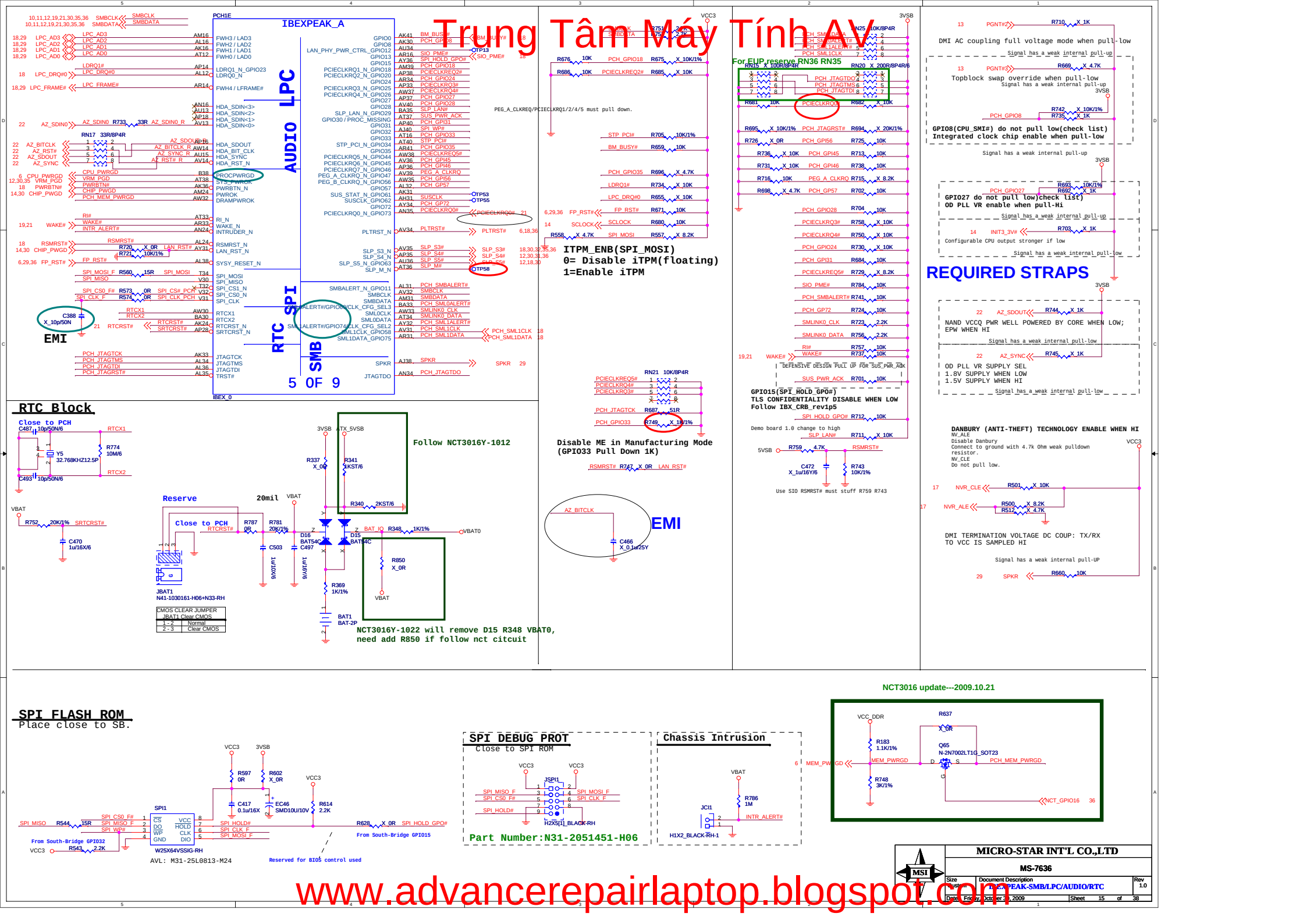


BOM GPIO	STD	A
GPIO38	H	H
GPIO39	H	H
GPIO48	H	L



Change CP13, CP14 to 10uH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

POWER

IBEXPEAK_A

7 OF 9

IBEX_0

Demo board 1.1 change

C599 place bottom as short as possible
C602 place TOP as short as possible

one cap place bottom as short as possible
another place TOP as short as possible

DMI PLL FILTER

SATA PLL FILTER

PCH decoupling cap

EMI

5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore,they can satisfy the requirement.

Near ball AF1

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7636
Size	Custom
Document Description	IBEXPEAK-POWER
Rev	1.0
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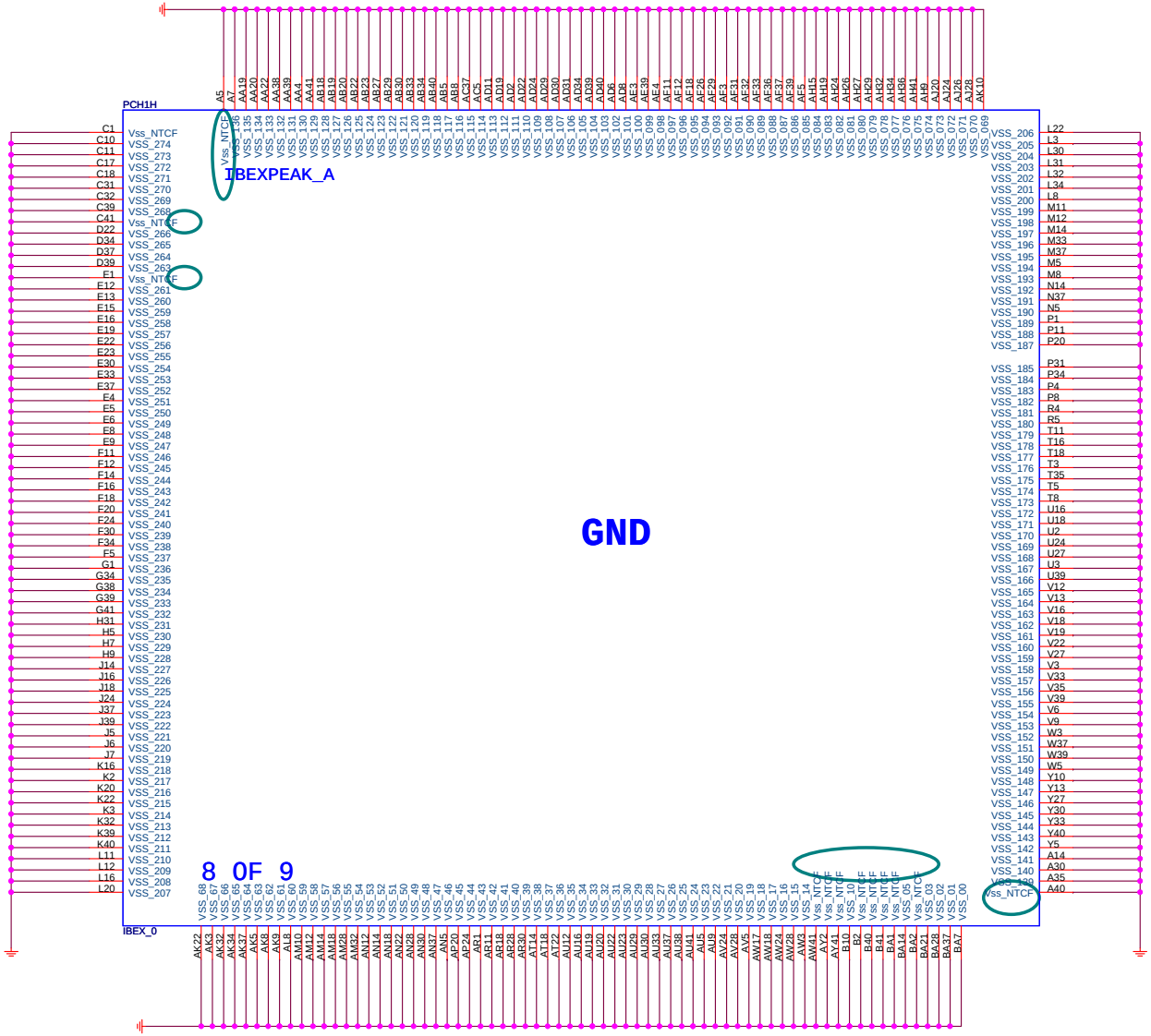

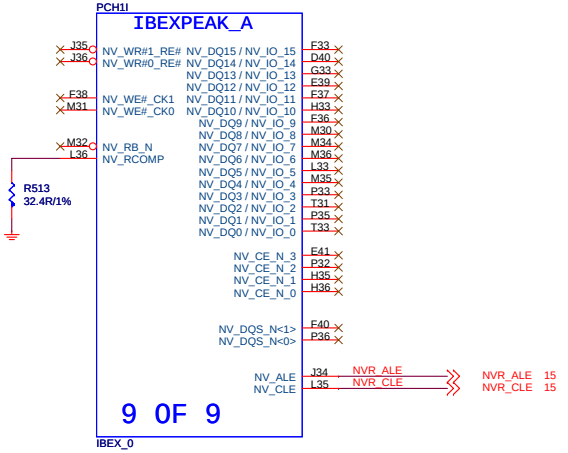

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MS-7636	
Size: Custom	Document Description: IBEXPEAK-GND/NVRAM
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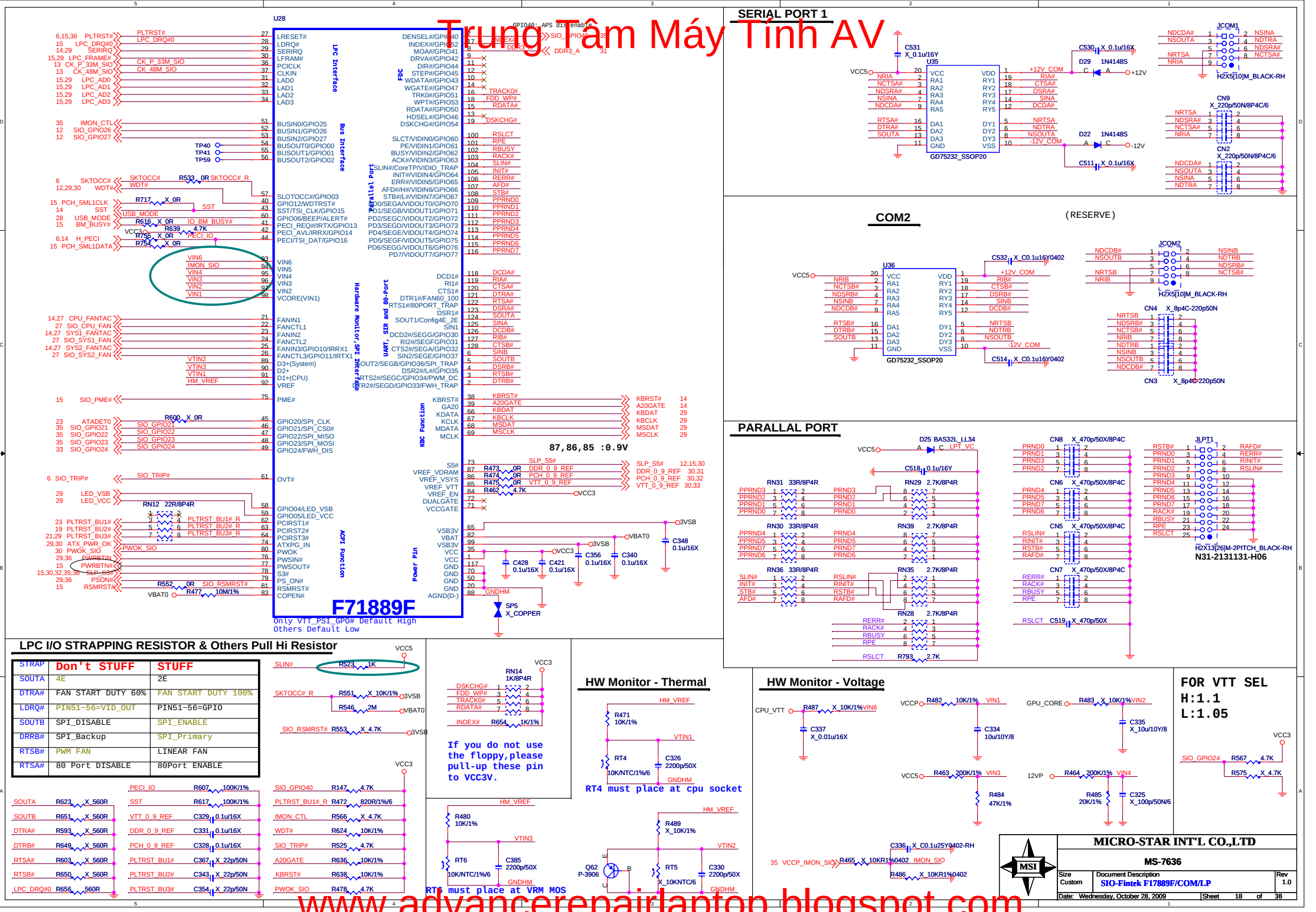
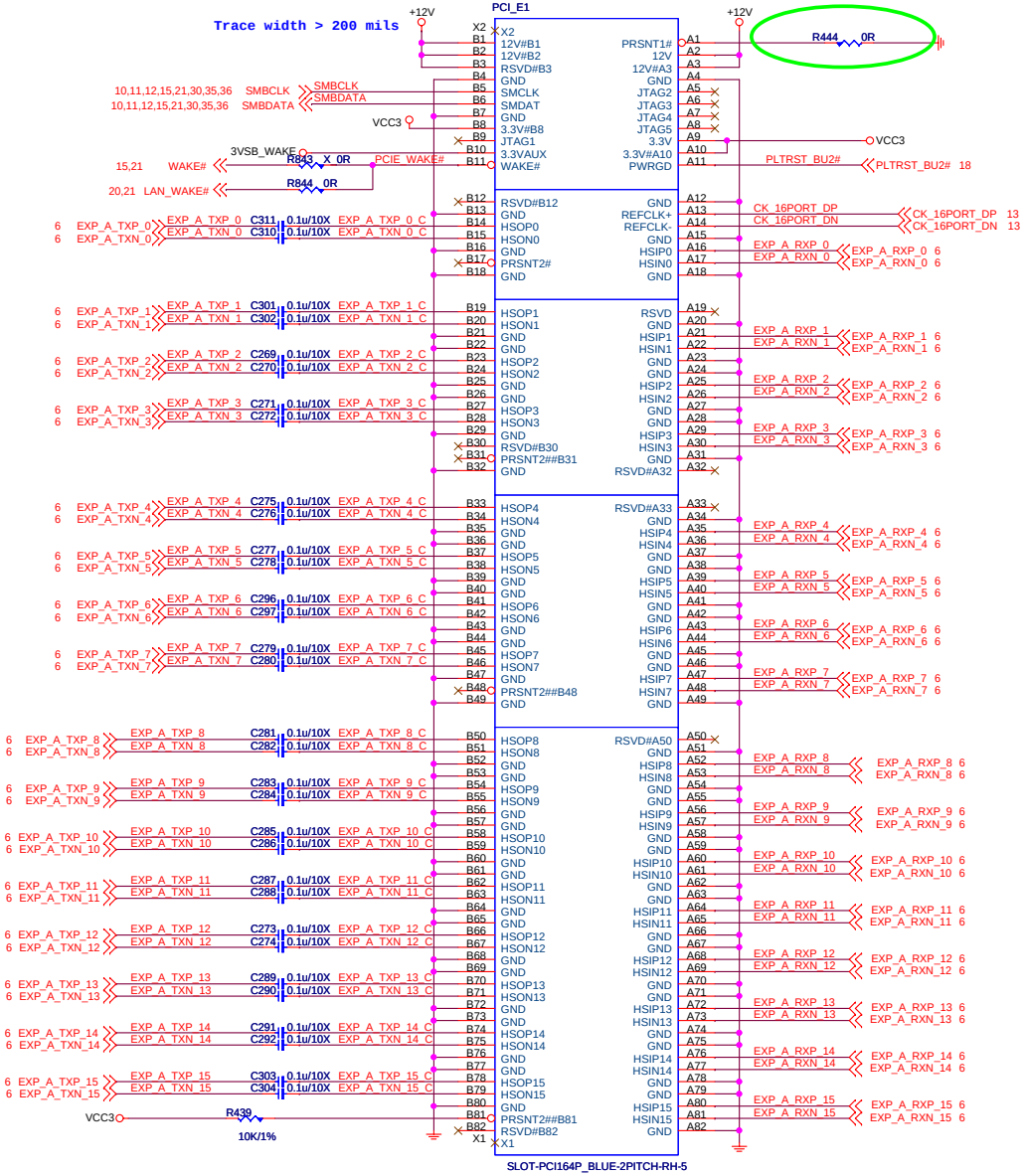
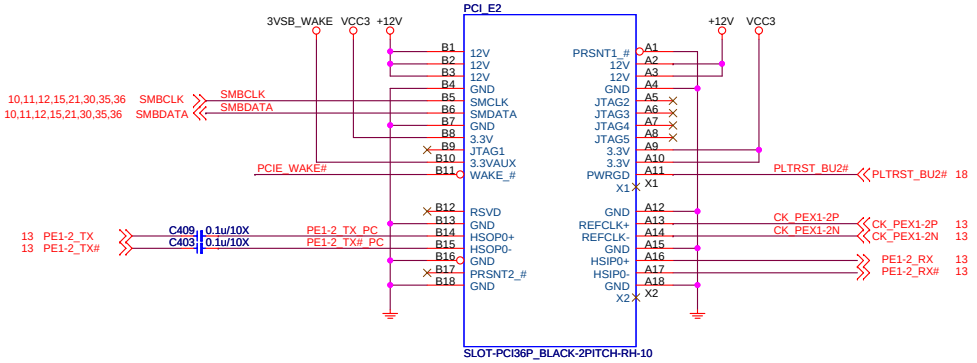


STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LDRQ#	PIN51~56=VID_OUT	PIN51~56=GPIO
SOUTB	SPI_DISABLE	SPI_ENABLE
DRRB#	SPI_Backup	SPI_Primary
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80 Port DISABLE	80Port ENABLE

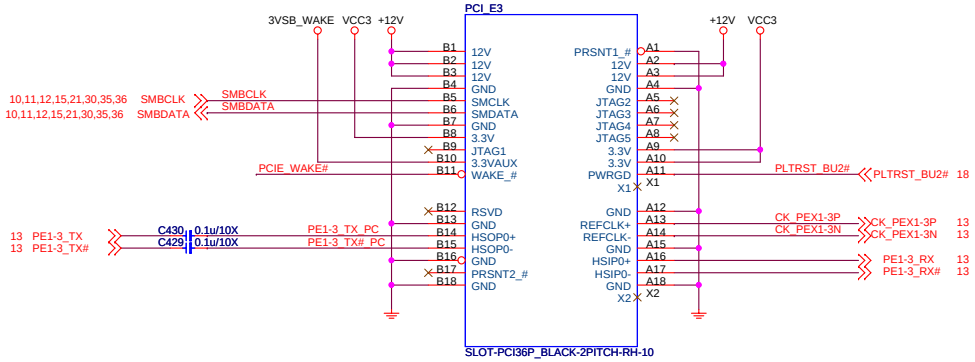
PCI_Express X16 Slot

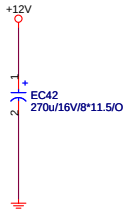


PCI EXPRESS x1-PORT2



PCI EXPRESS x1-PORT3





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MS-7636		
Size: Custom	Document Description: PCIE x16 / x1 / x1 Slots	Rev: 1.0
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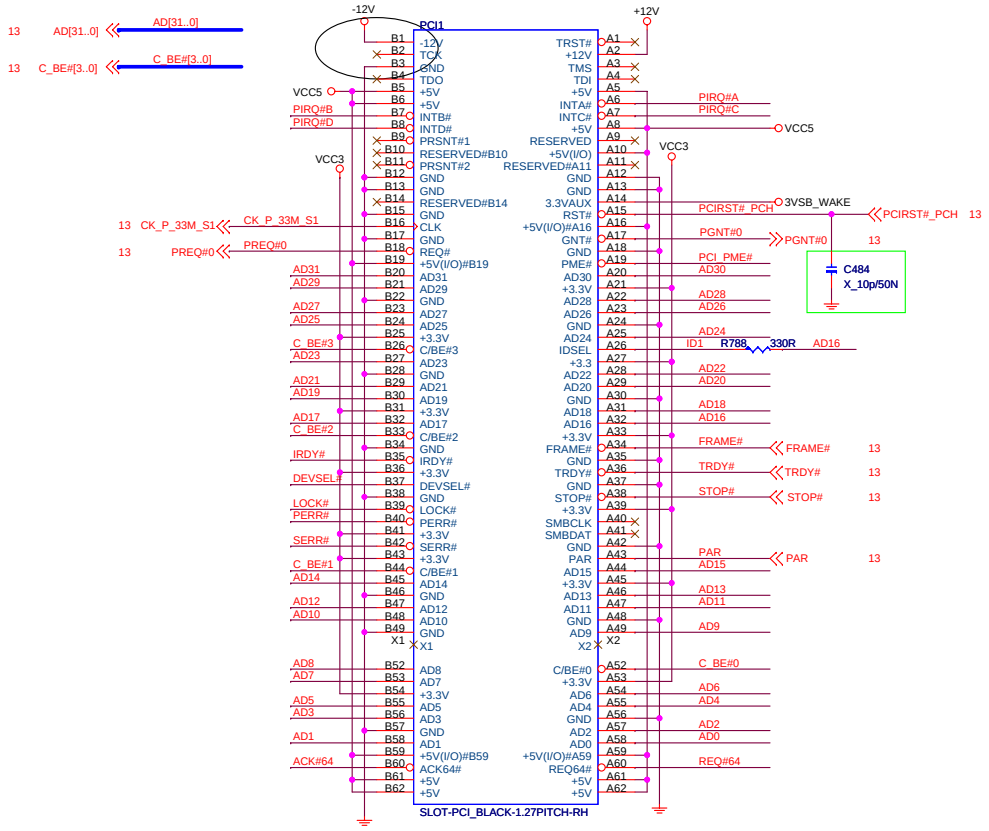
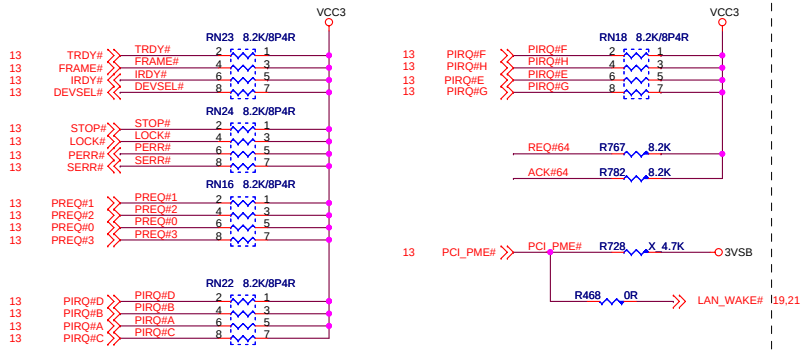
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

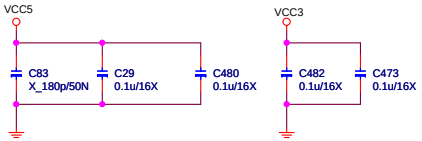


IDSEL = AD16
MASTER = PREQ#0
~~PIRQ#A~~

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR INT'L CO.,LTD	
MS-7636	
Size: Custom	Document Description: PCI Slot
Rev: 1.0	
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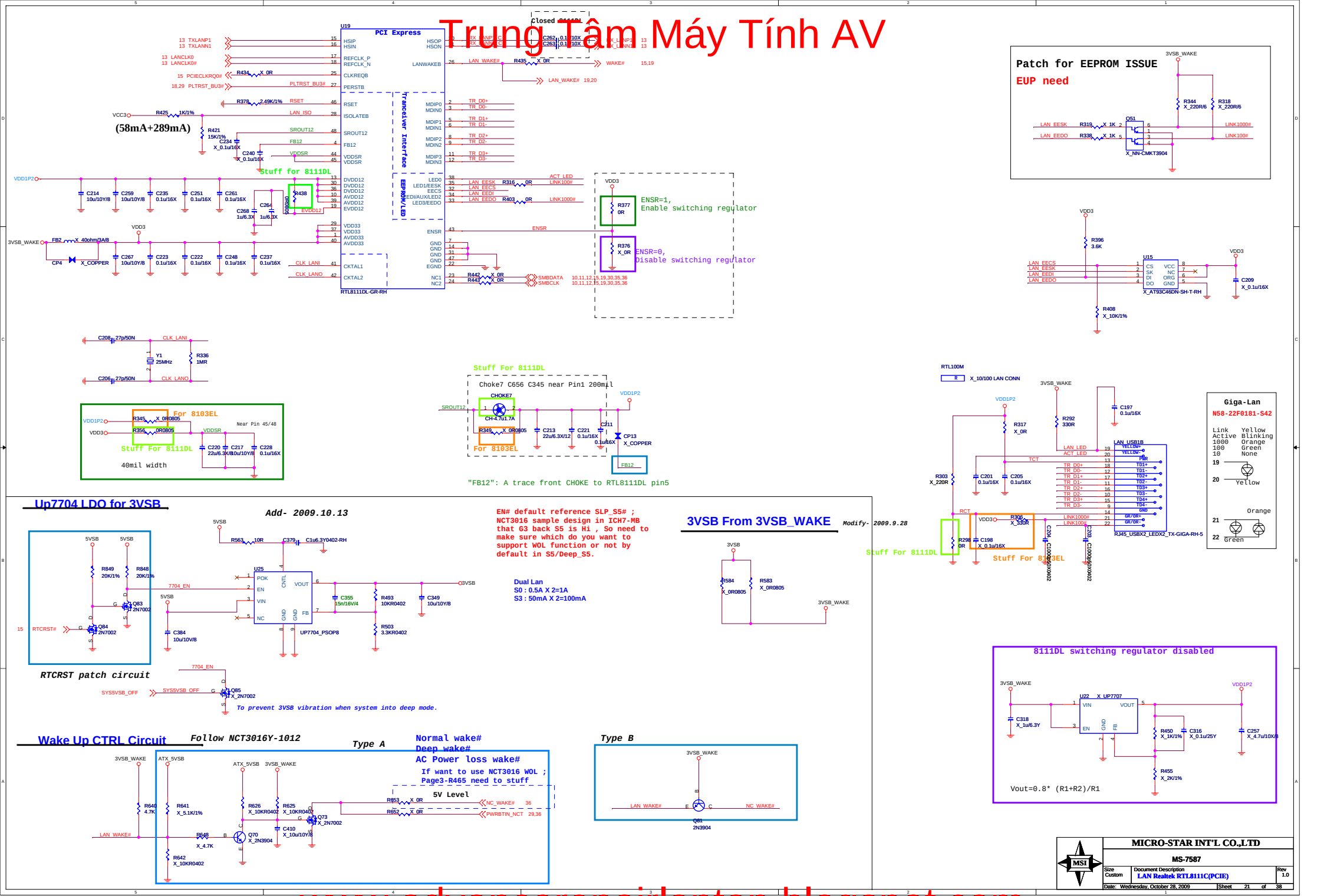

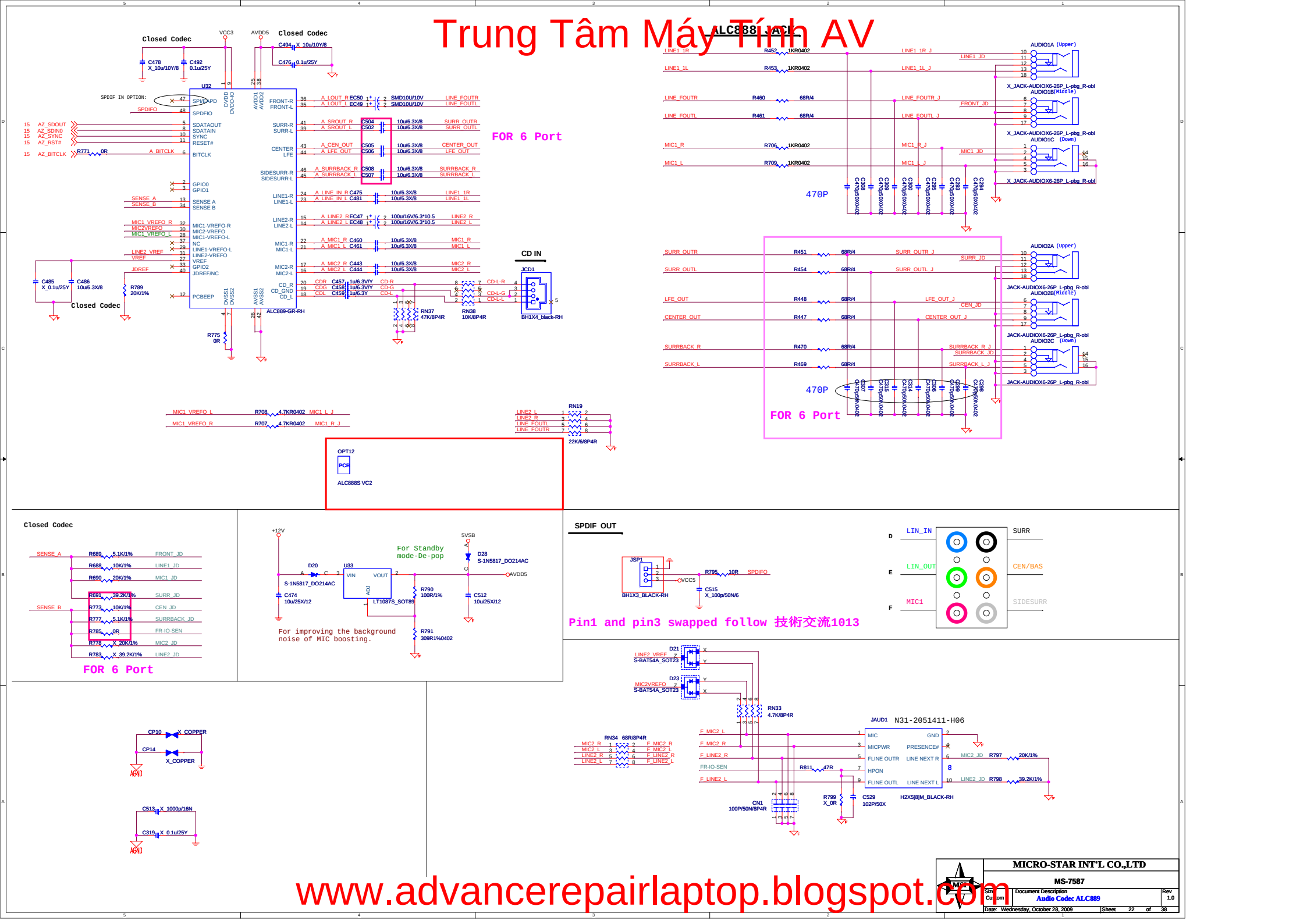

MICRO-STAR INT'L CO.,LTD
MS-7587
Document Description: Audio Codec ALC889
Rev 1.0
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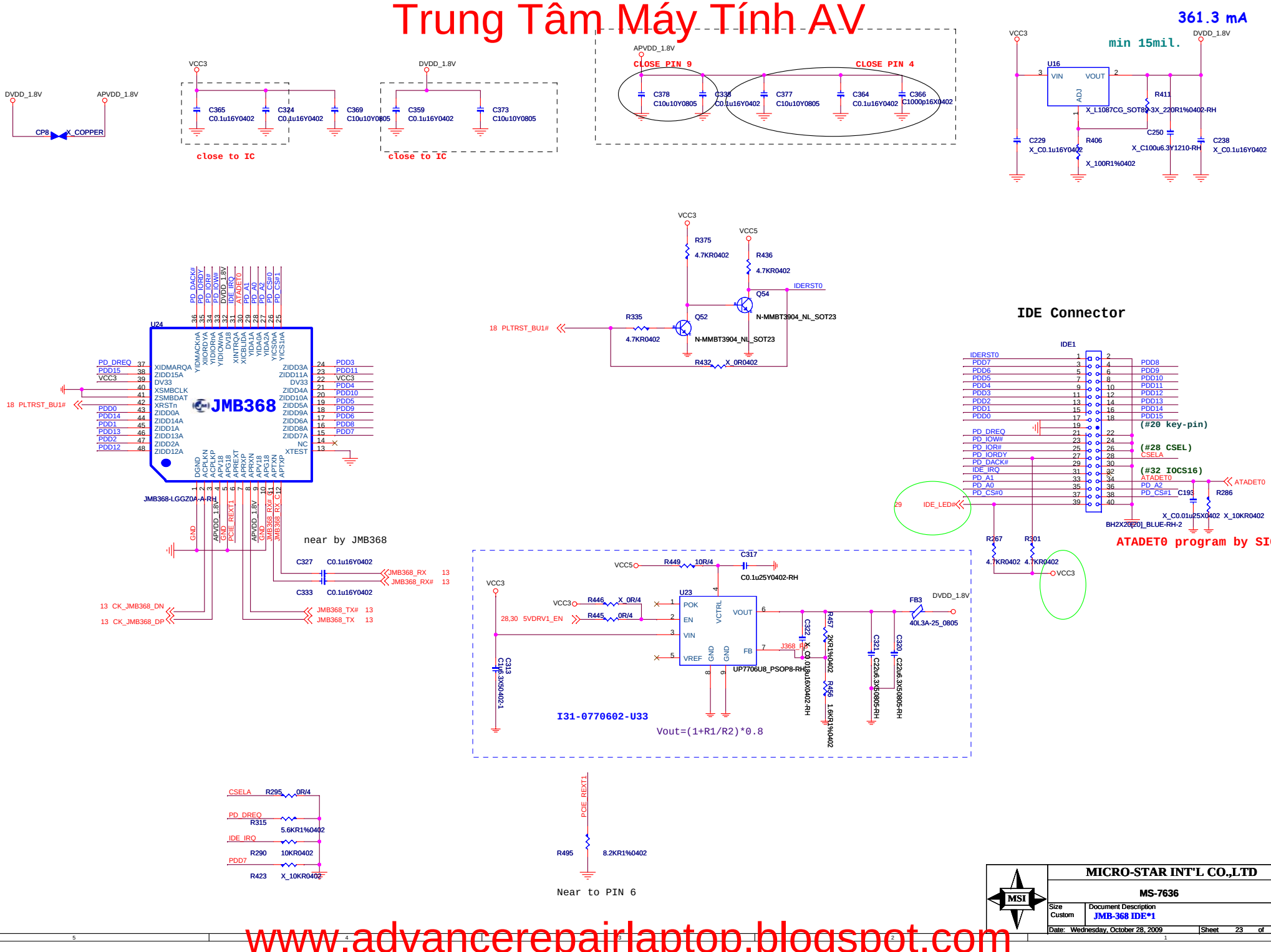

MICRO-STAR INT'L CO.,LTD	
MS-7636	
Size: Custom	Document Description: JMB-368 IDE*1
Rev: 1.0	
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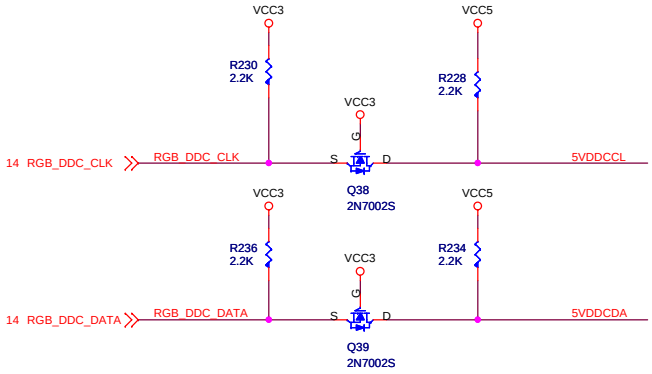
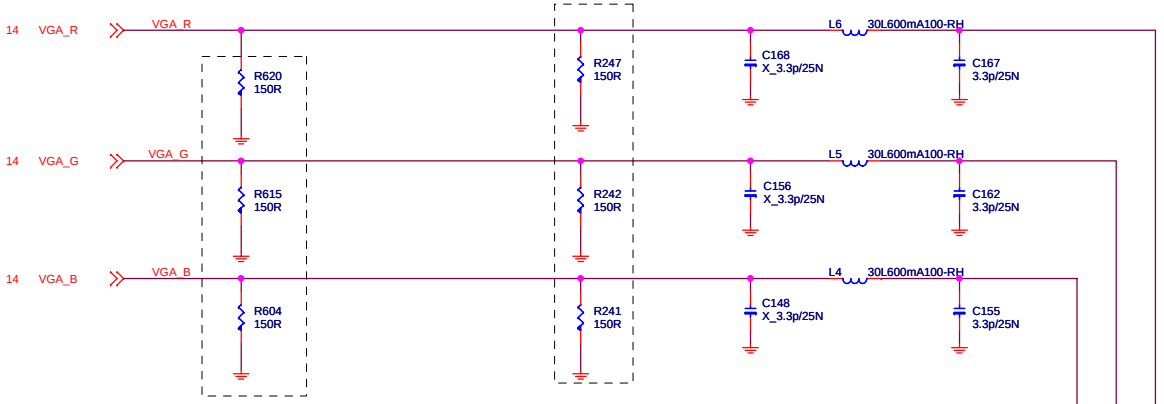
D-Sub

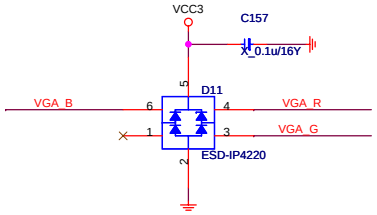
Level shift

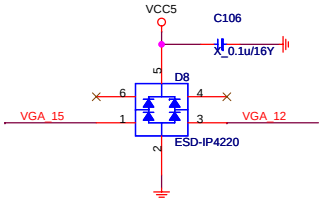


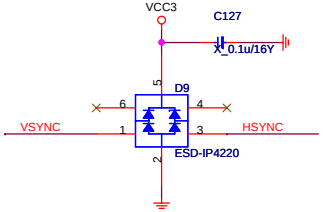
PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



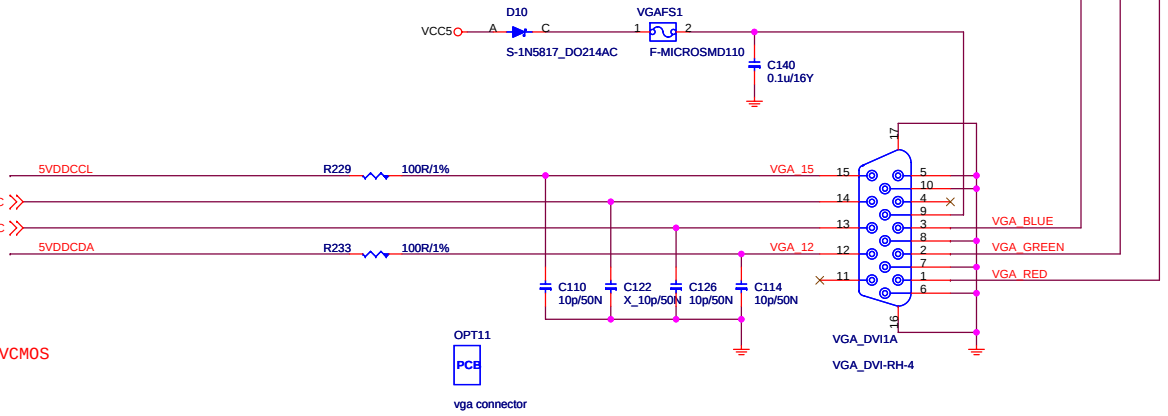
Close to PCH within 250 mils.







VSYNC/HSYNC:HVCMOS
CRB pull VCC3



MICRO-STAR INT'L CO.,LTD		
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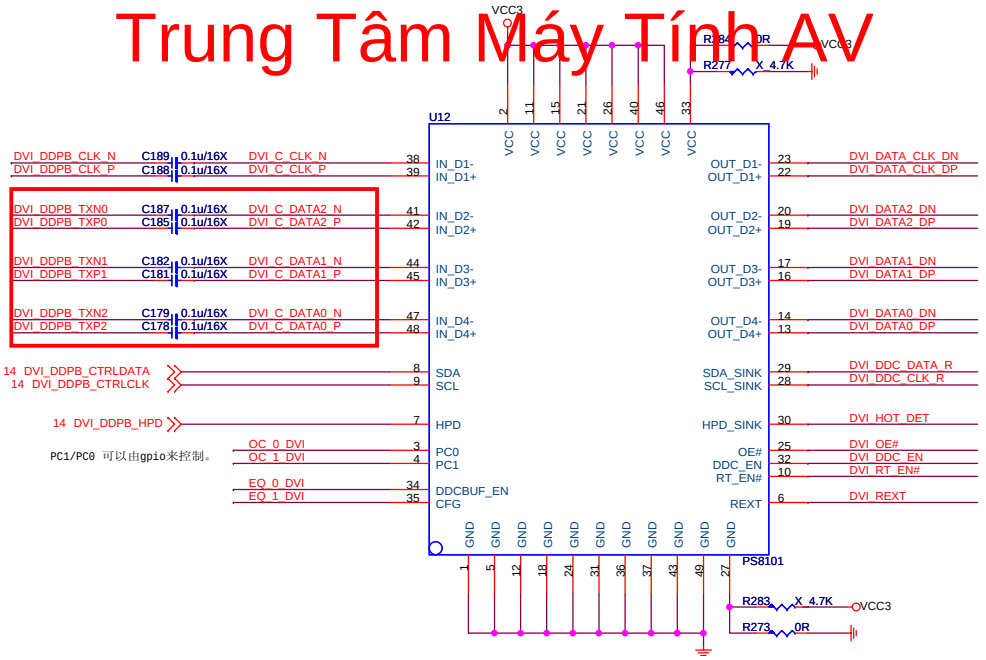
DVI level shifter

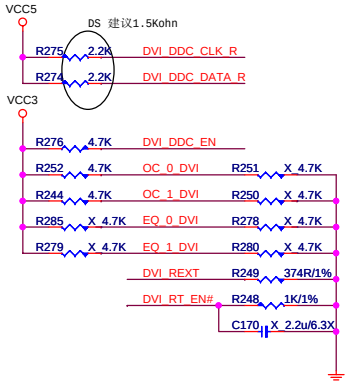
14 DVI_DDPB_TXP0
14 DVI_DDPB_TXN0
14 DVI_DDPB_TXP1
14 DVI_DDPB_TXN1
14 DVI_DDPB_TXP2
14 DVI_DDPB_TXN2
14 DVI_DDPB_CLK_P
14 DVI_DDPB_CLK_N

PCH signal Mappings
DG P156

差分阻抗为100ohm



PARADE 腹:B0B-081010C-P97.

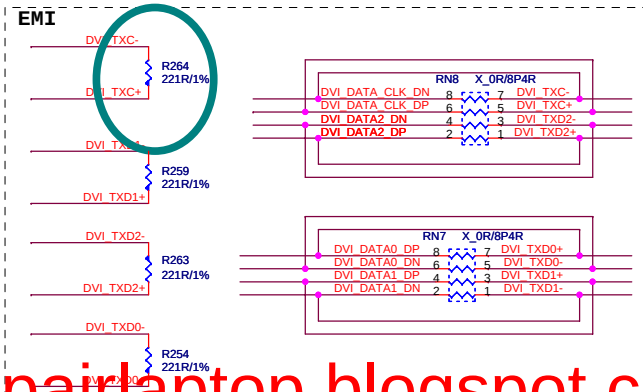


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

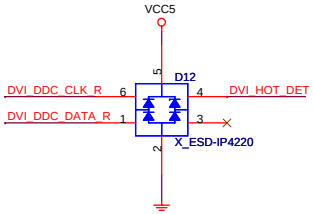
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

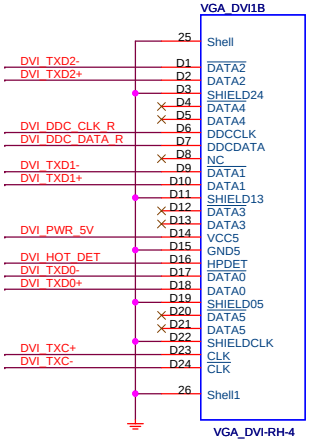
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	The 4-dB equalization setting is recommended for PC motherboard level shifting to compensate PCB trace losses.
10	12 dB	
11	0 dB	

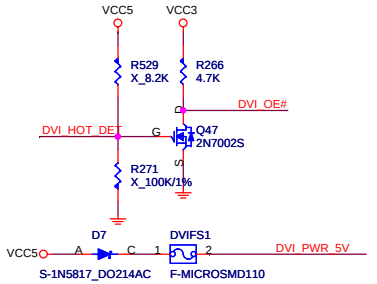
EMI

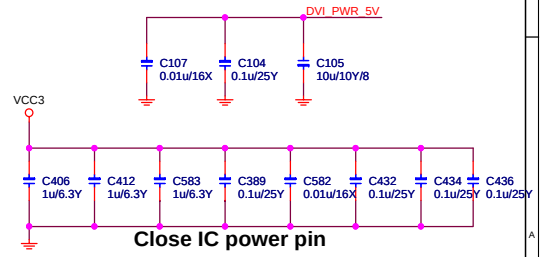


reserve









MICRO-STAR INT'L CO.,LTD

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Custom	DVI transfer	1.0

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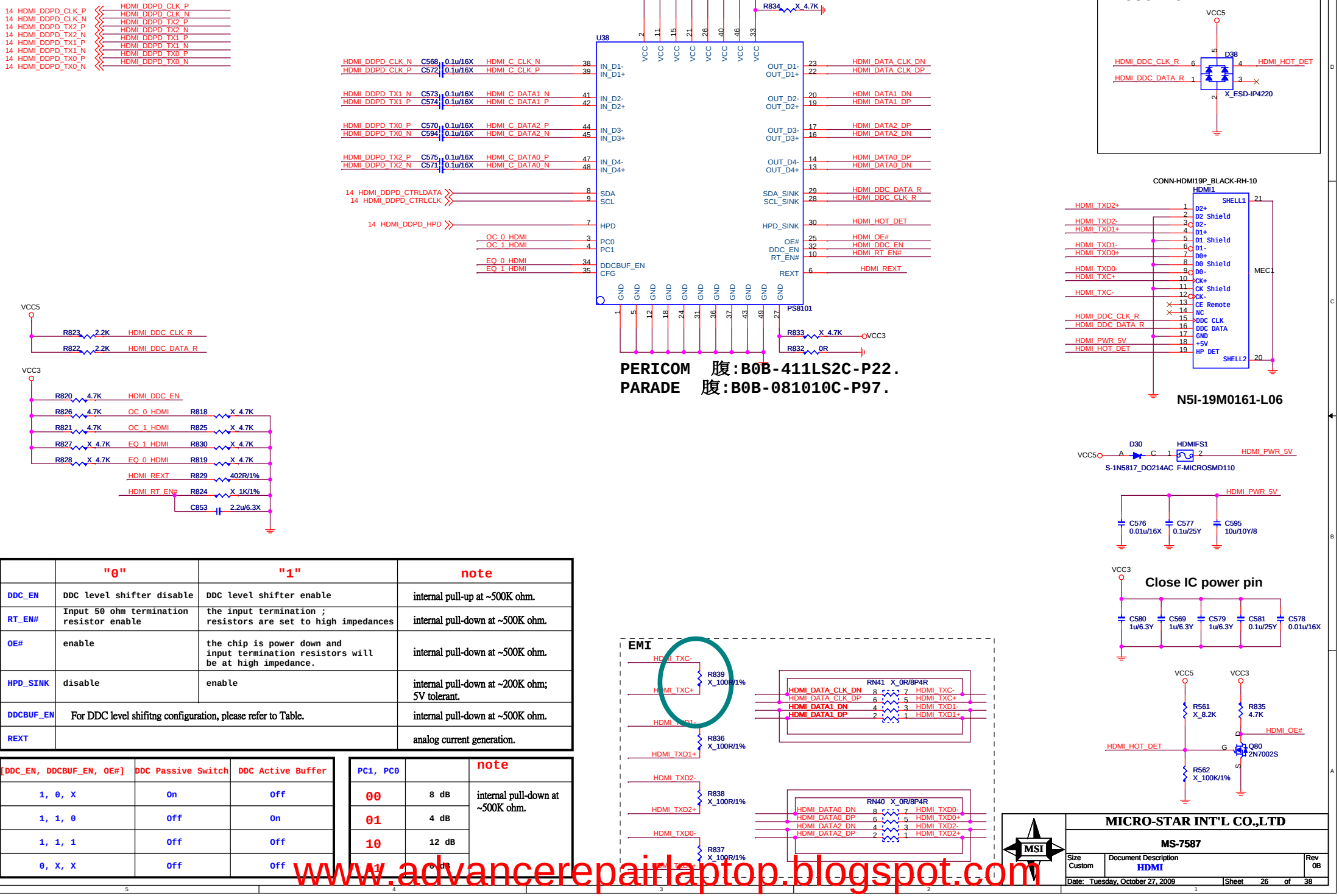
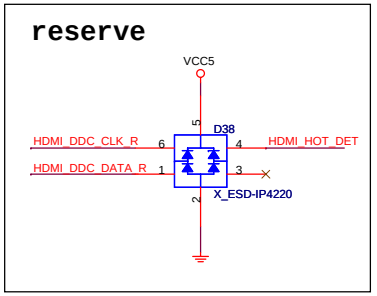
HDMI level shifter



PERICOM 腹:B0B-411LS2C-P22.
PARADE 腹:B0B-081010C-P97.



N5I-19M0161-L06

	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

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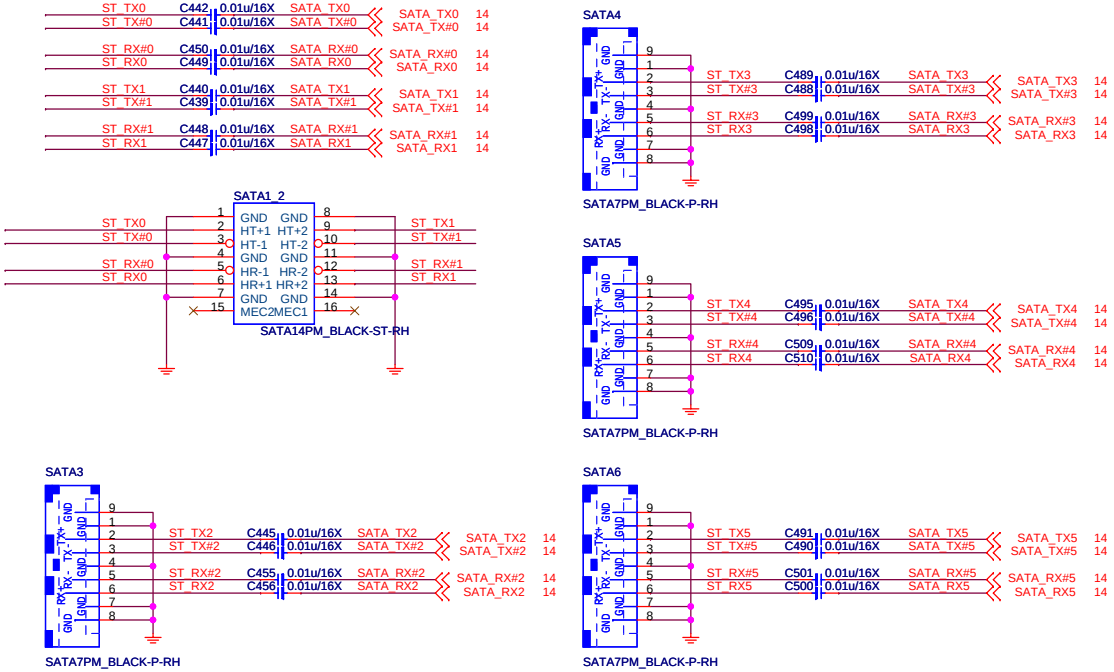
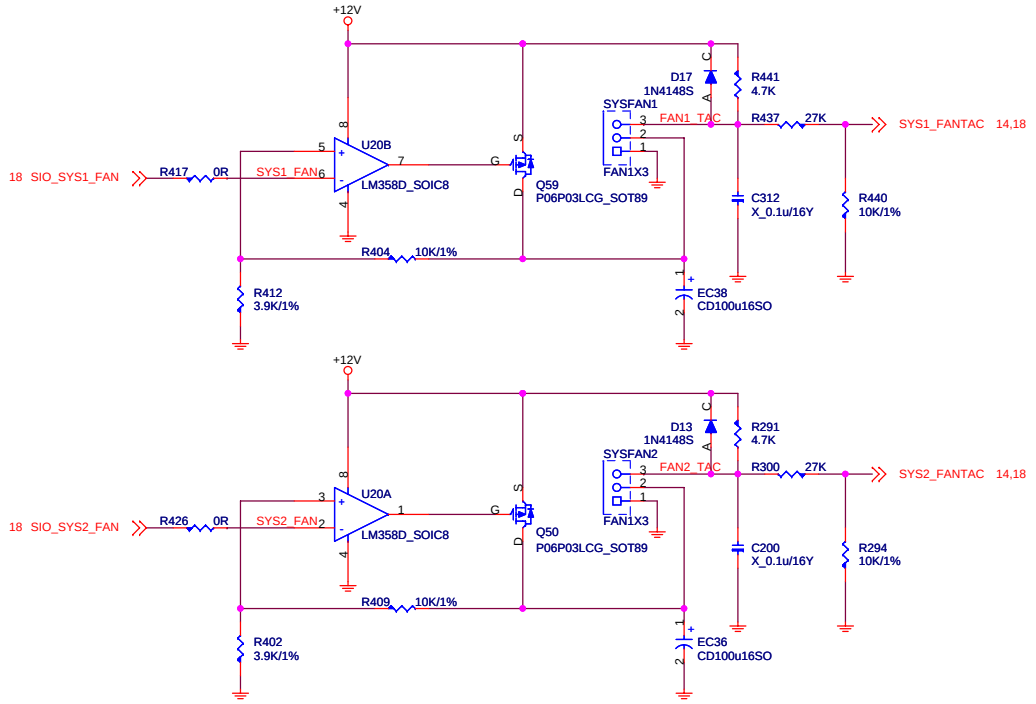
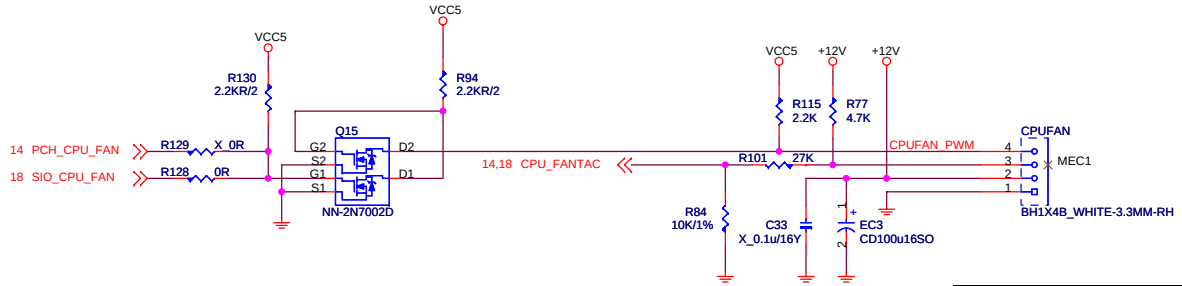
SATA connector (color:Black)



FAN CONTROL CIRCUIT





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Size: Custom	Document Description: SATA & e-SATA Ports and Fan Control
Rev: 1.0	
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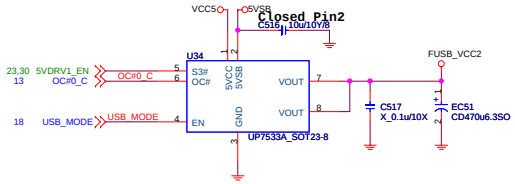
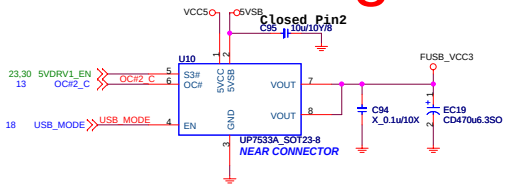
Rear USB Connector

USB POWER FOR PORT 0,1

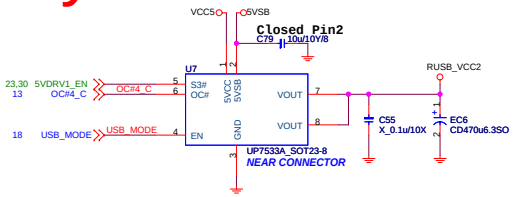


USB POWER FOR PORT 4,5

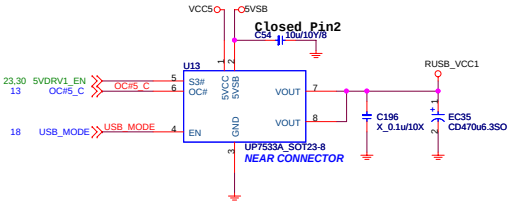


Front USB Connector

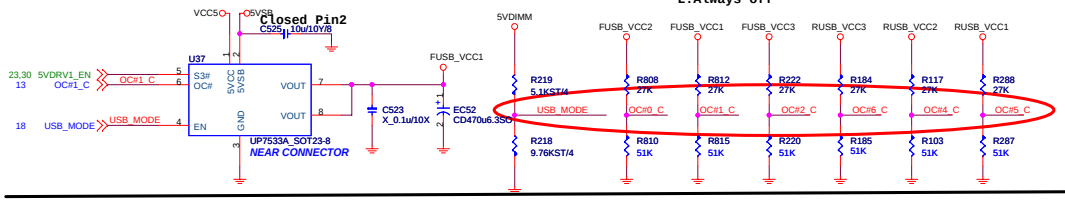
USB POWER FOR PORT 6,7



USB POWER FOR PORT 8,9

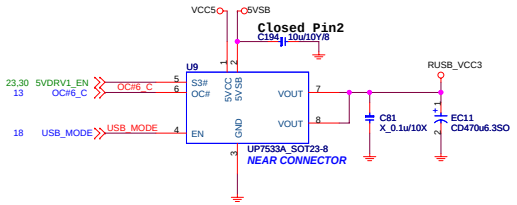


USB POWER REAL PORT 2,3

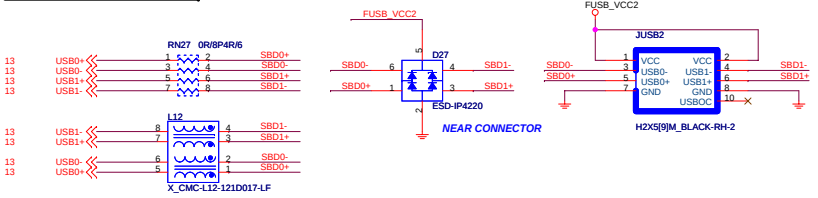


USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

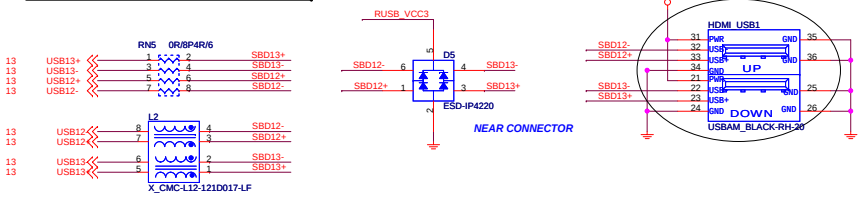
USB POWER FOR PORT 10,11



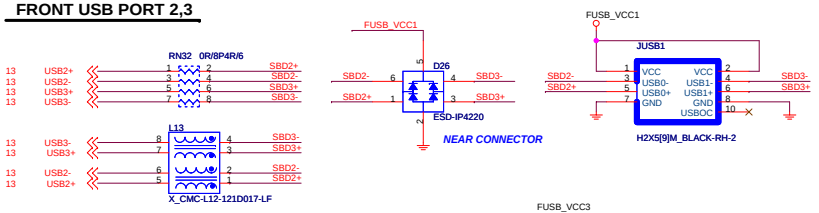
FRONT USB PORT 0,1



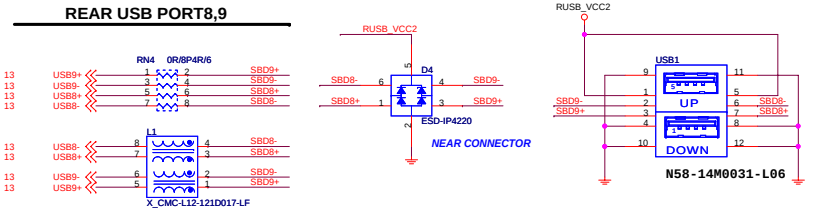
REAR USB PORT 12,13



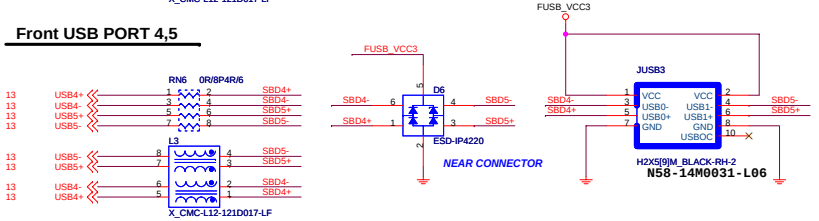
FRONT USB PORT 2,3



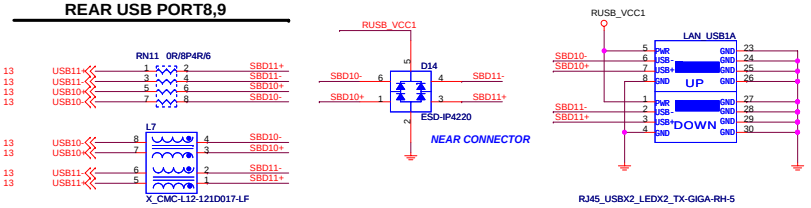
REAR USB PORT8,9



Front USB PORT 4,5



REAR USB PORT8,9



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7636	
Size: Custom	Document Description: USB Connectors-10 ports	Rev: 1.0
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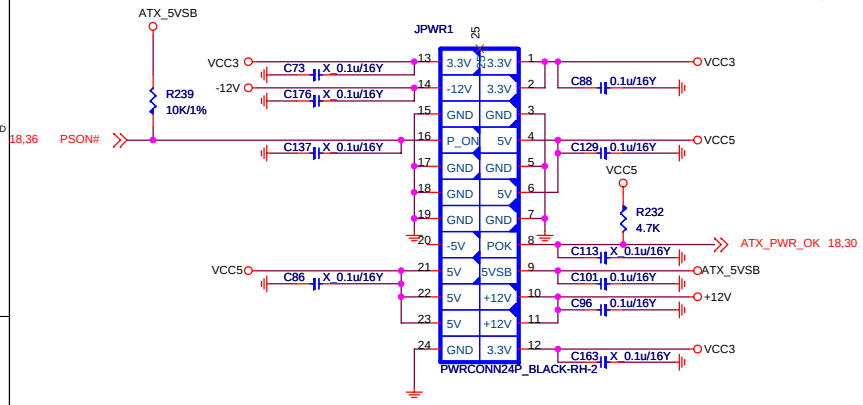
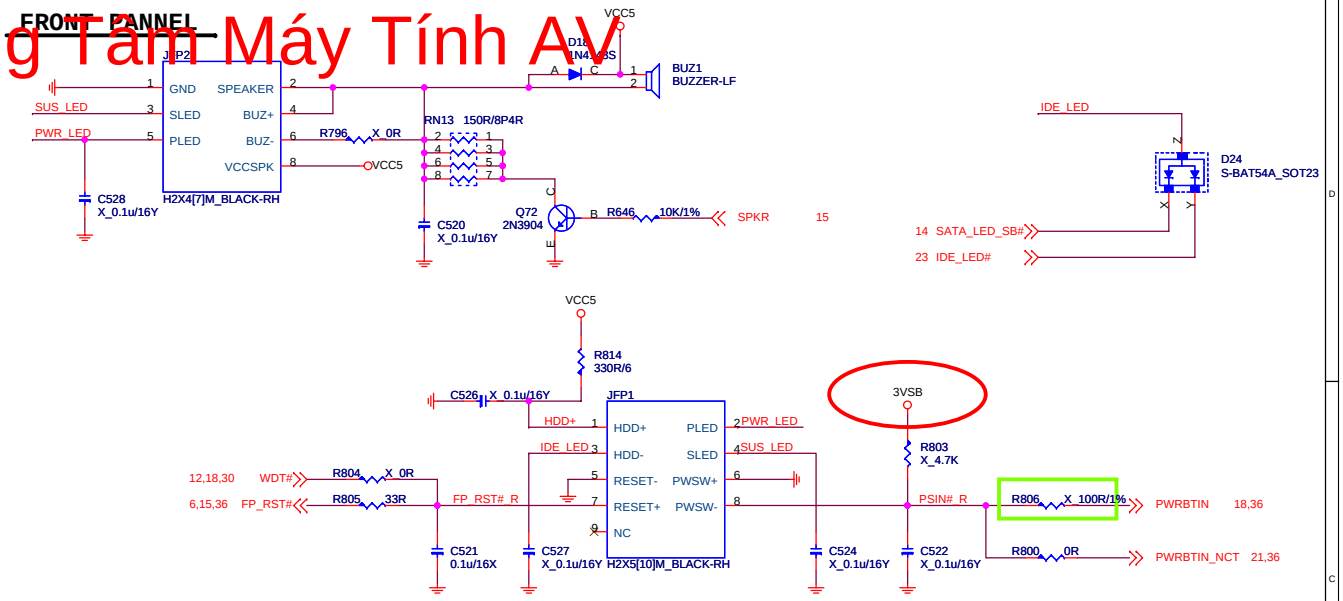
ATX POWER CONNECTOR



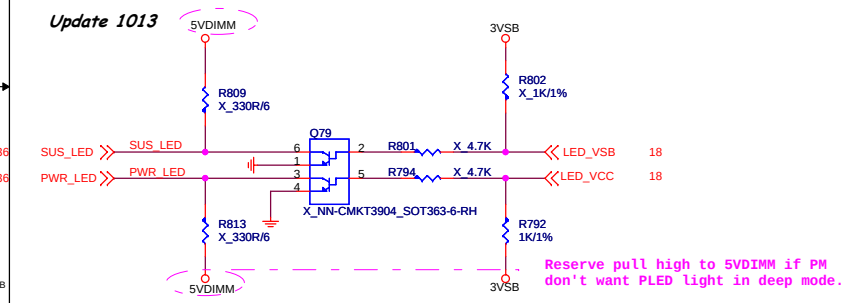
FRONT PANNEL



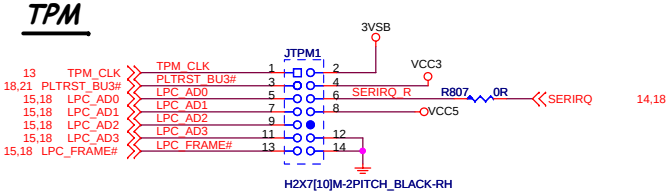
LED (for Fintek 71889)

If use N3016Y LED Ctrl,
SIO LED_VCC / LED_VSB can not to use.

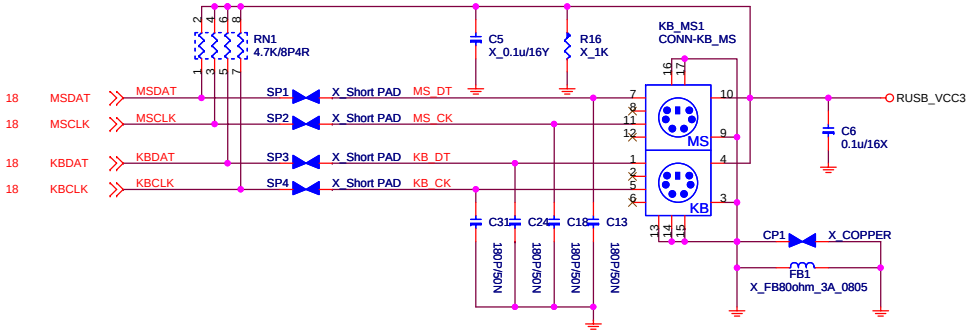
Update 1013



TPM



PS2 KEYBOARD & MOUSE CONNECTOR



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Size: Custom	Document Description: ATX PWR-Connector & Front Panel & EMI	Rev: 1.0
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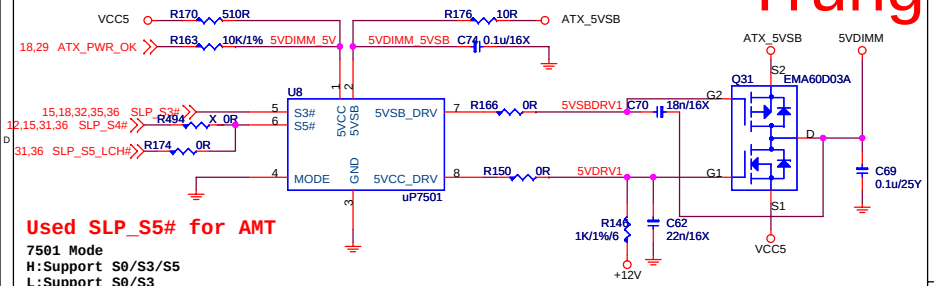
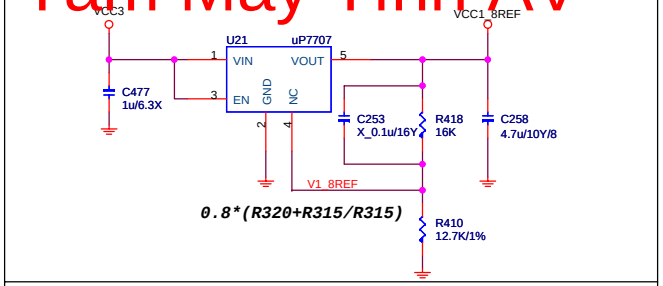
5VDIMM FOR DDR



Used SLP_S5# for AMT

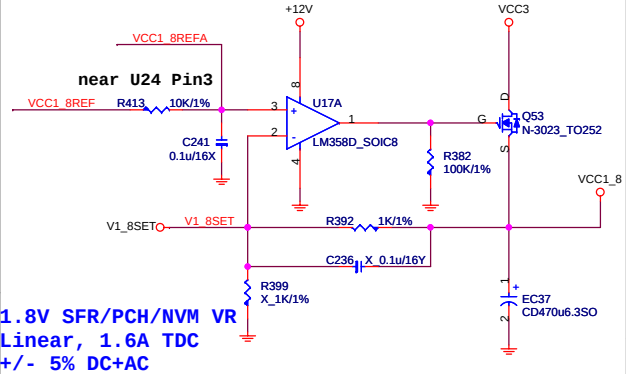
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

VCC1_8REF



0.8*(R320+R315/R315)

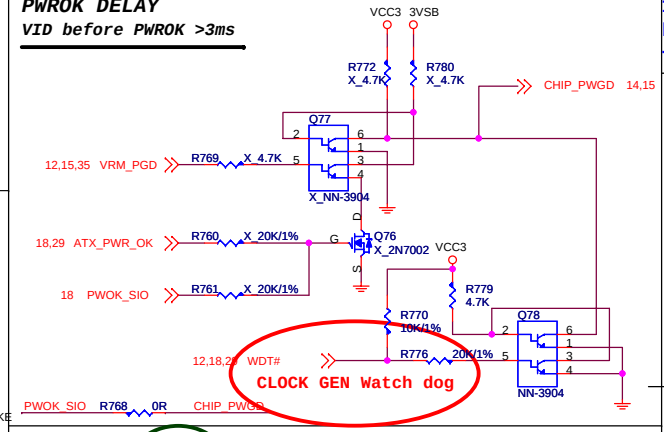
VCC1_8



1.8V SFR/PCH/NVM VR
Linear, 1.6A TDC
+/- 5% DC+AC

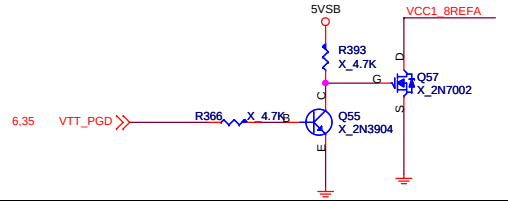
PWROK DELAY

VID before PWROK >3ms

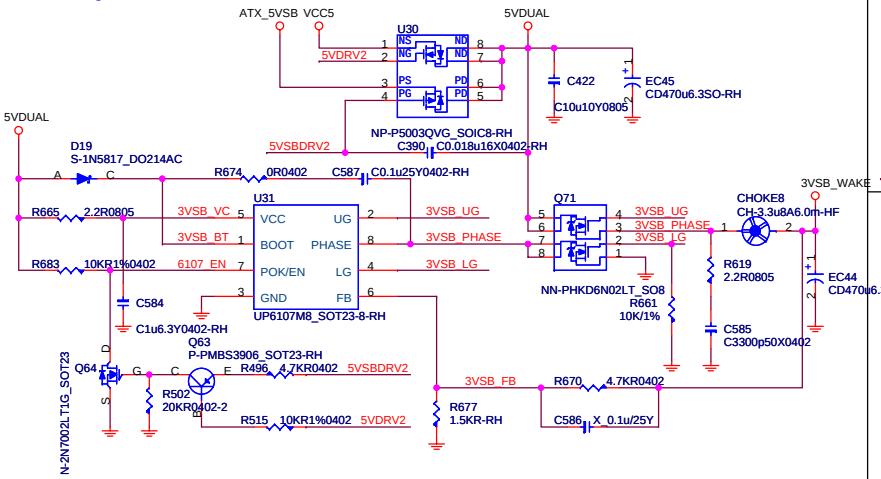


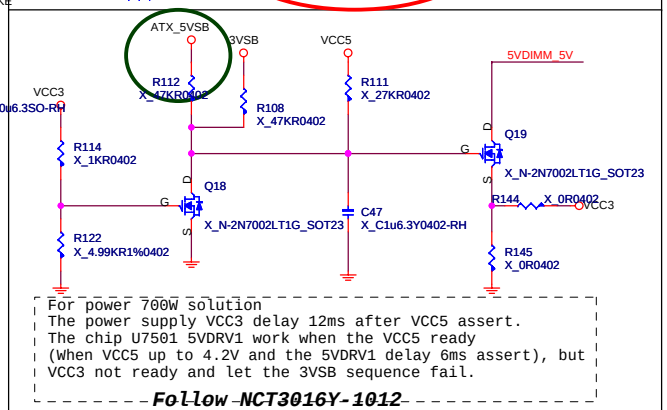
CLOCK GEN Watch dog

cpuvtt & pch vore wait 1.8v



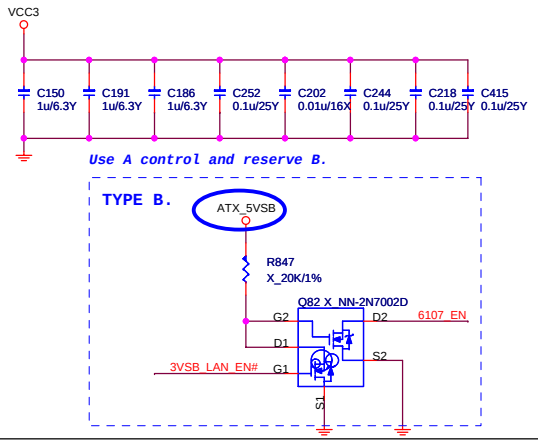
Deep Mode WOL LAN Power CTRL Circuit



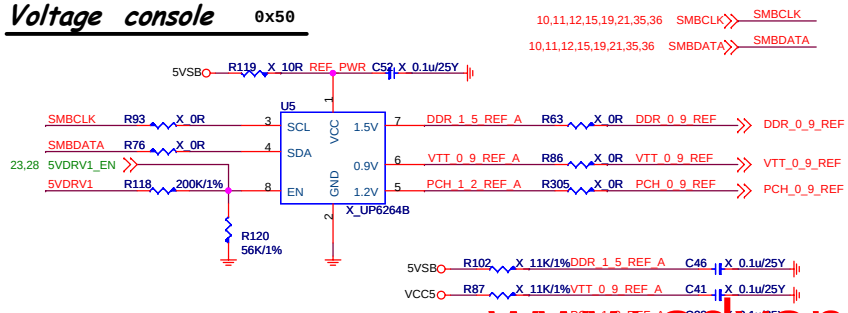


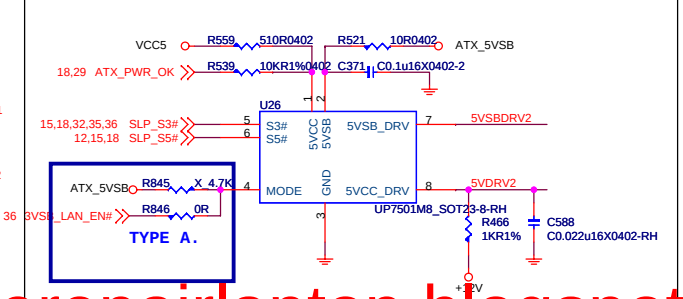
For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

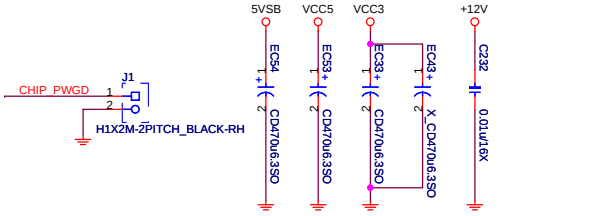
Follow NCT3016Y-1012



Voltage console 0x50







MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ACPI controller UPI	1.0

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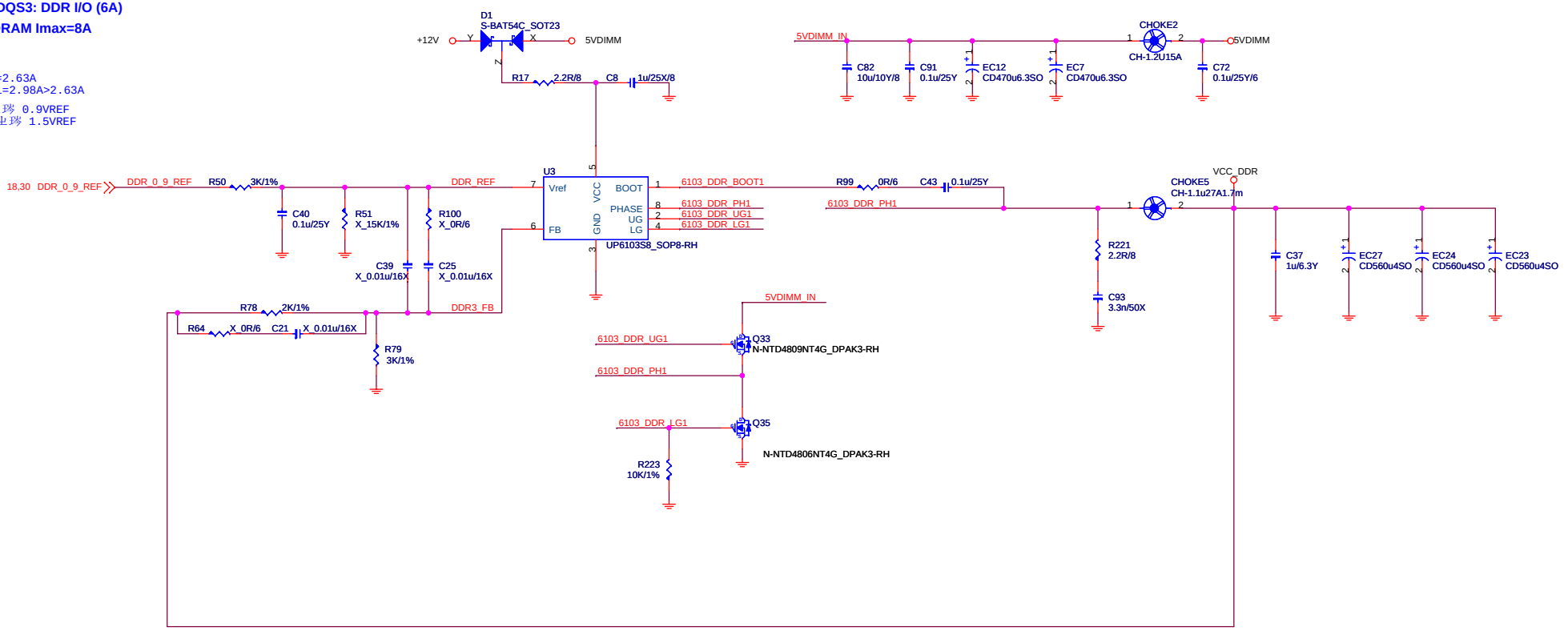
DDR3_1.5V

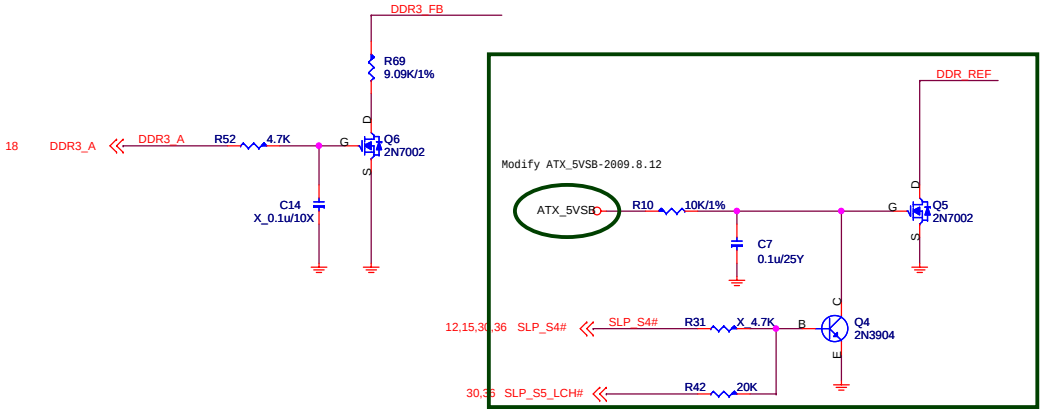
21.25A=6A+8A+0.75A+6.5A

V1.5DDQS3: DDR I/O (6A)
DDR DRAM Imax=8A

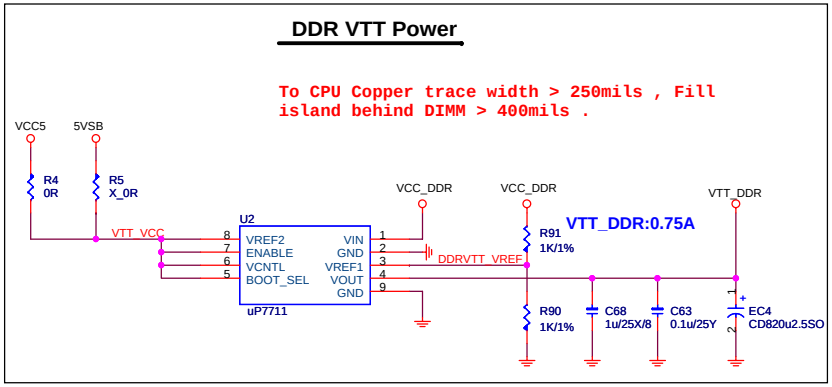
Iripple=2.63A
1.49*2*1=2.98A>2.63A

SIO 业珍 0.9VREF
6264 业珍 1.5VREF





Only for meet Intel power down sequence.



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Size	Document Description	Rev
Custom	DDR POWER - UPI6103_1-Phase	1.0

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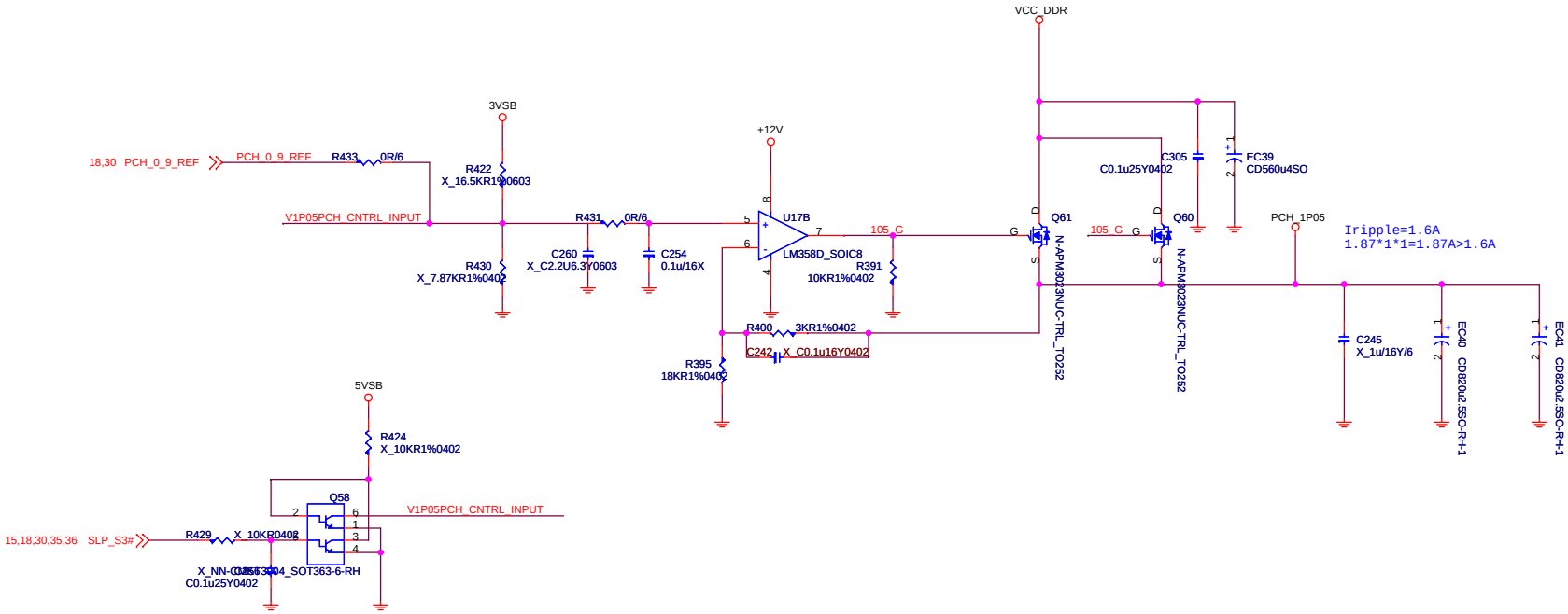
PCH Core 6.8A

V1.05PCHS0: Vcc, VccExp, VccDMI, VccSATA, VccSATAPLL, VccAUPLL, VccSSC, VccDIFFCLK, VccDIFFCLKN, VccUSBCORE, VccDPLL, VccDPLL_EXP,VccDPLL_FDI (4.5A)
V1.05MEM: VccMEW, VccAUX, VccME (2.3A)



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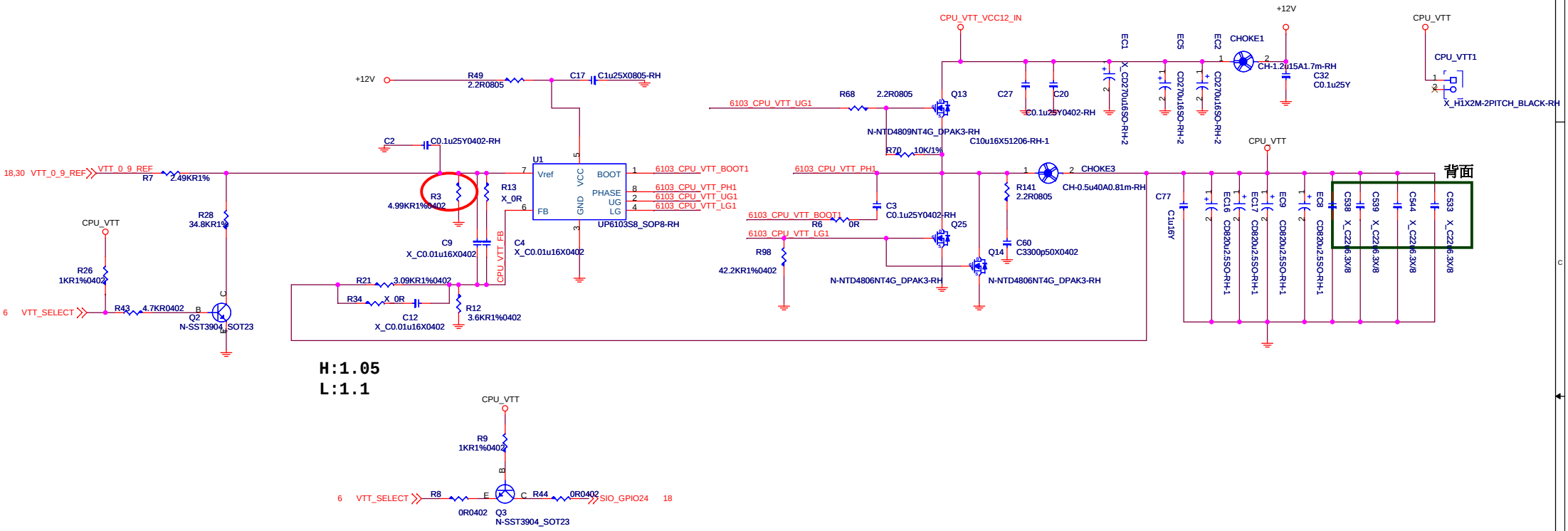
MS-7636		
Size: Custom	Document Description: PCH POWER - UPI6103_1-Phase	Rev: 1.0
Date: Tuesday, October 27, 2009	Sheet 32 of 38	

VTTPWRGD LEVEL SHIFT

CPU_VTT

VTTS0: 1.1V/1.05V CPU Uncore, MCP I/O (30A)

Iripple=8.28A
6.1*2*1=12.2A>8.28A



H:1.05
L:1.1

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MS-7636		
Size: Custom	Document Description: CPU_VTT - UPI6103_1-Phase	Rev: 1.0
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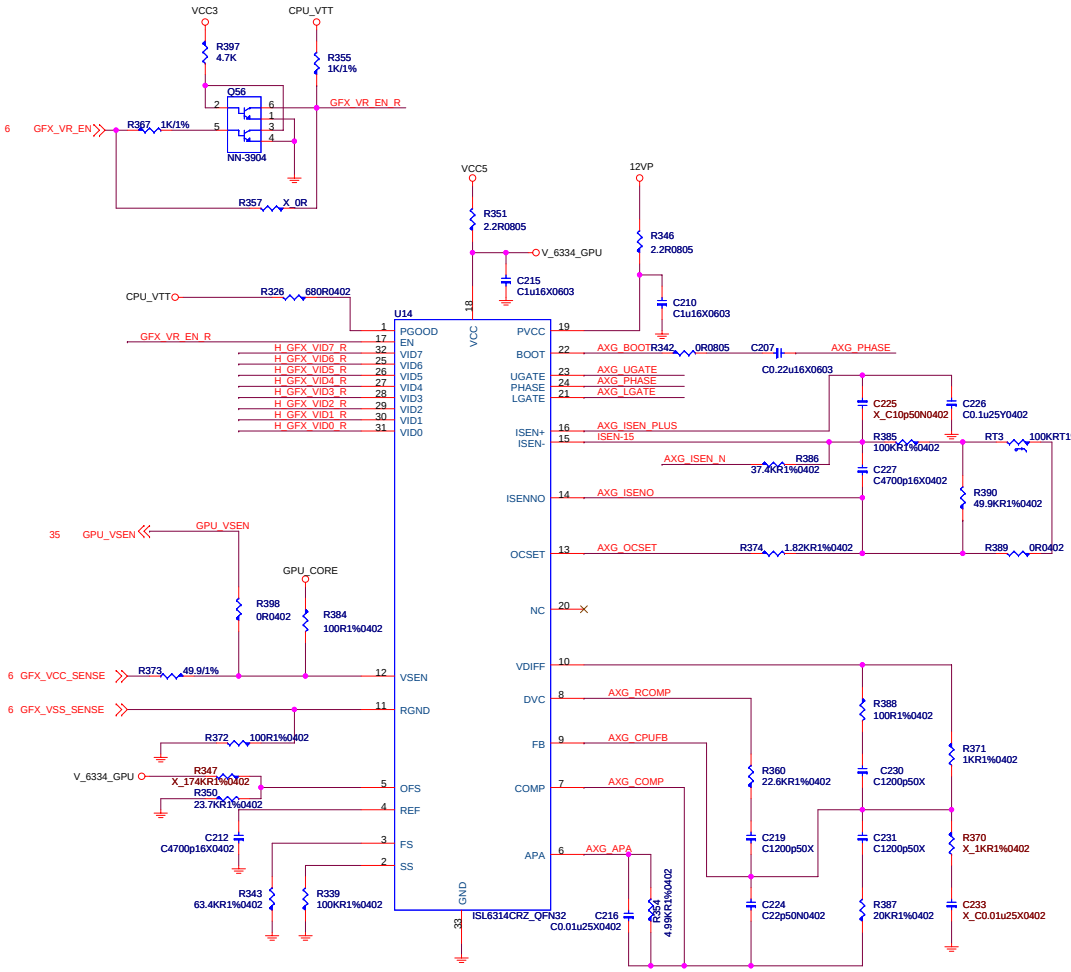
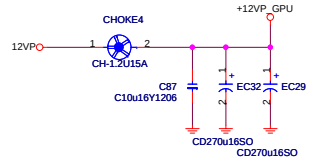
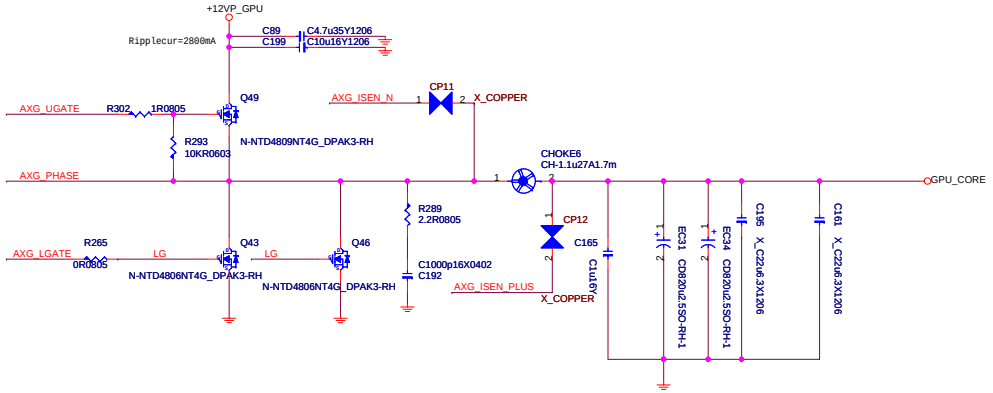


GFX 12V VIN



GFX 1PHASE OUTPUT



GFX VR (Clarkdale Only)
Switcher (7 VID), 16A TDC, 25A Imax

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Size: Custom	Document Description: GPU PowerISL6117_1-Phase	Rev: 1.0
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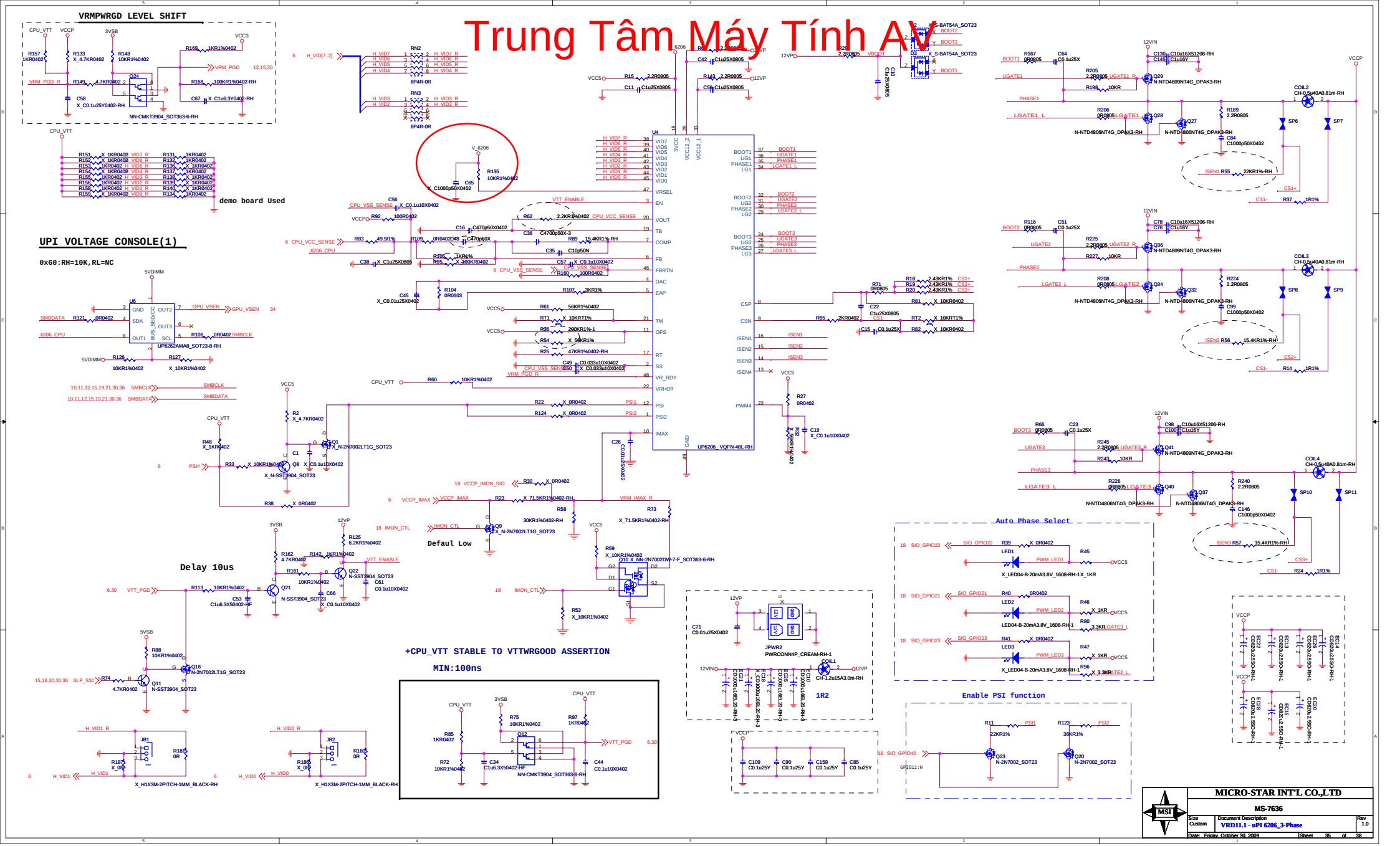

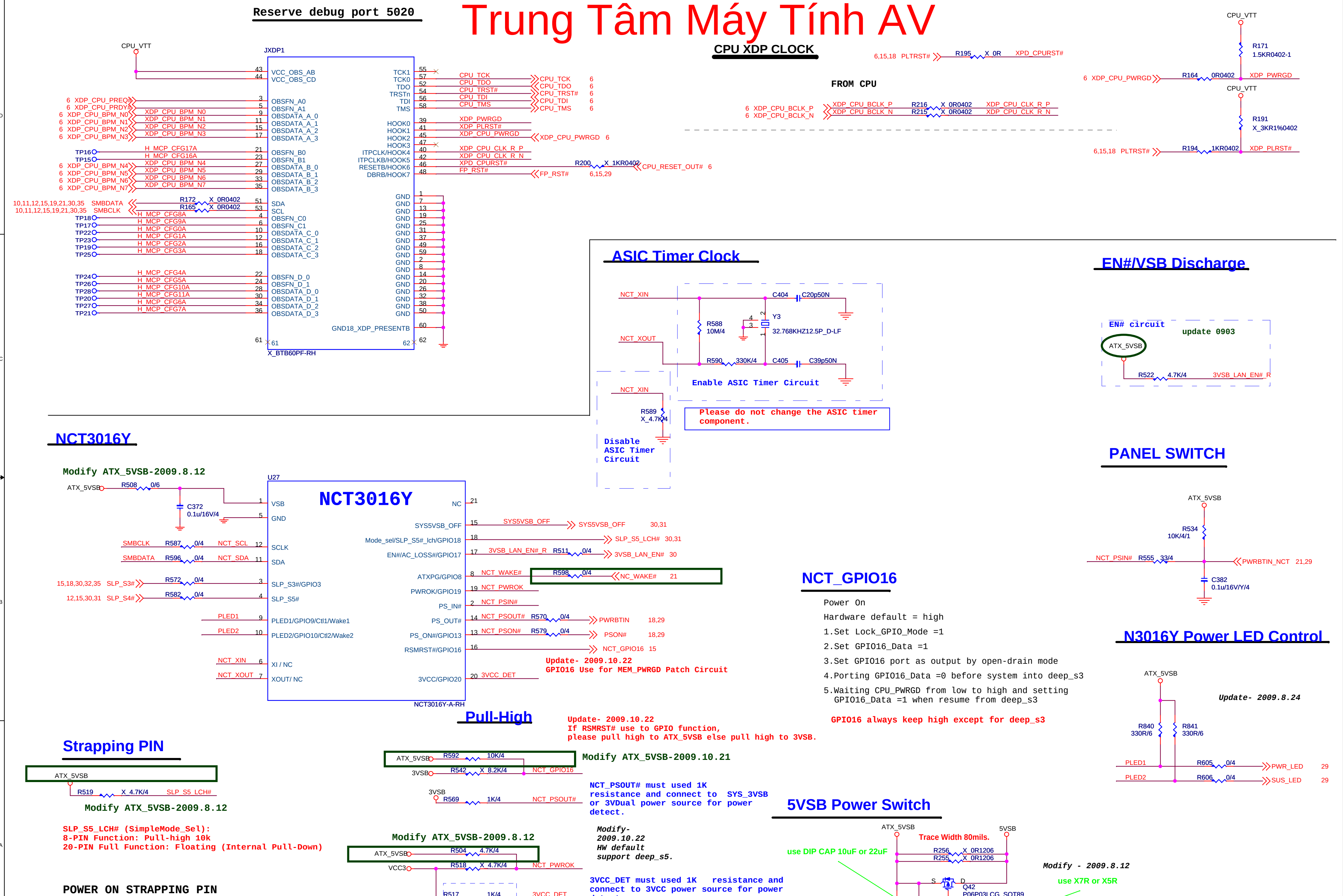

Reserve debug port 5020
CPU XDP CLOCK
JXDP1
X_BTB60PF-RH
FROM CPU
ASIC Timer Clock
Enable ASIC Timer Circuit
Please do not change the ASIC timer component.
Disable ASIC Timer Circuit
32.768KHZ12.5P_D-LF
EN#/VSB Discharge
EN# circuit
update 0903
NCT3016Y
Modify ATX_5VSB-2009.8.12
U27
NCT3016Y-A-RH
PANEL SWITCH
NCT_GPIO16
Power On
Hardware default = high
1.Set Lock_GPIO_Mode =1
2.Set GPIO16_Data =1
3.Set GPIO16 port as output by open-drain mode
4.Porting GPIO16_Data =0 before system into deep_s3
5.Waiting CPU_PWRGD from low to high and setting GPIO16_Data =1 when resume from deep_s3
GPIO16 always keep high except for deep_s3
Update- 2009.10.22
GPIO16 Use for MEM_PWRGD Patch Circuit
N3016Y Power LED Control
Update- 2009.8.24
Pull-High
Update- 2009.10.22
If RSMRST# use to GPIO function, please pull high to ATX_5VSB else pull high to 3VSB.
Modify ATX_5VSB-2009.10.21
NCT_PSOUT# must used 1K resistance and connect to SYS_3VSB or 3VDual power source for power detect.
Modify- 2009.10.22 HW default support deep_s5.
3VCC_DET must used 1K resistance and connect to 3VCC power source for power detect.
Modify ATX_5VSB-2009.8.12
Strapping PIN
Modify ATX_5VSB-2009.8.12
SLP_S5_LCH# (SimpleMode_Sel):
8-PIN Function: Pull-high 10k
20-PIN Full Function: Floating (Internal Pull-Down)
5VSB Power Switch
Trace Width 80mils.
use DIP CAP 10uF or 22uF
Modify - 2009.8.12
use X7R or X5R
New future for WAKE 0 support

POWER ON STRAPPING PIN

PIN	Name	0	1
18	SimpleMode_Sel	Full function	Simple Mode

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3VSB and 3VSB_WAKE POWER MAP

Add- 2009.9.28

+12VIN → Up6213 → VCCP 95W(TDP) → Intel 1156 CPU (85A)

+12V → UP6103 → CPU_VTTD 30A → Intel 1156 CPU (30A)

PE Slot x16 (5.5A)
PEX1 Slot x3(1.5A)
PCI Slot x3 (1.5A)
1394 Connect x2 (3A)
FAN x3 (0.6A)

+12V → LT1087S → AVDD5 0.2A → ALC888S-VC2 (200mA)

ATX_5VSB → uP6107 or uP7706 → 3VSB_WAKE → PCI-E LAN / PCI-E SLOT / PCI SLOT

5VSB → uP7704 → 3VSB → SB / OTHER

Power Delivery

PCI Slot x3
(10A) ~ 玥(2Ax3=6A)

VCC5
5VSB → uP7501 → 5VDIMM 3.8A → UP6103 → VCC_DDR 21.25A

- LDO → PCH 1P05V → PCH (6.5A)
- DDRIII x2(3.6A) Intel 1156 CPU (2.8A)
- W83310DS → VTT_DDR → DDRIII x4(0.75A)

up7706&Linear → 3VSB 4.081A → PCH (1A) PE Slot(0.375mA X5) PCI Slot (0.375mA X2)
RTL8111DL LAN (58mA+289mA)

uP7533 x5 → FUSB_VCC / RUSB_VCC 5.5A → Fron USB x4 (2A) / REAL USB x6 (3A) PS2 KB/MS(500mA)

(18.6A)
VCC3 → OP+MOS → PCH1_8V 1.6A → PCH 1.8V/CPU1.8V (1.6A)

PE Slot x16 (3.0A)
PEX1 Slot x2(2.0X3A=6)
PCI Slot x1 (7.6AX1=7.6)
~ 玥(2Ax3=6A)

uP7706 → JMB368_1.8V 361.3mA → JMB363 (361.3mA)

3.3V 58mA+289mA → RTL8111DL LAN (58mA+289mA)

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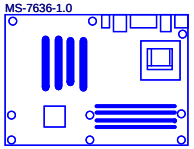
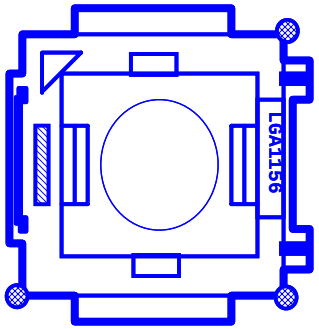
PCB

PCB1
<HP-BOM>
MS-7636-1.0



CPU SOCKET

XU1_X1
<HP-BOM>
CPU SOCKET



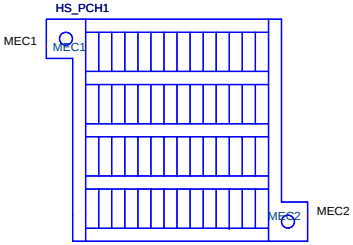
HEATPIPE

BATTERY

BAT1_X1

BAT-BCR2032P-RH

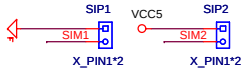
HS_PCH1



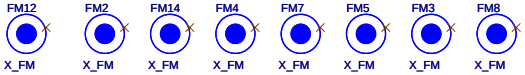
HS-0404591-RH

EL CAP

Simulation

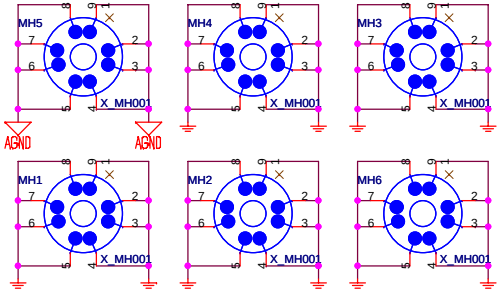


Optical Fiducial Marks-120



Optical Fiducial Marks-100

Mounting Holes



H55EB3:3孔audio（888S VC2）,GB LAN, OC-switch 不上, DVI,HDMI 不上,
JMB368 不上(IDE 也不上), APS LED 不上（SW APS） 半固.
H55SG6DVI:Full spec

MSI	MICRO-STAR INT'L CO.,LTD	
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