# Raichu_GL Schematics

## Gemini Lake





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緯創資通 Wistron Corporation
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|---|---|---|
| Title: Cover Page | | |
| Size: A3 | Document Number: Raichu_GL | Rev: -1M |
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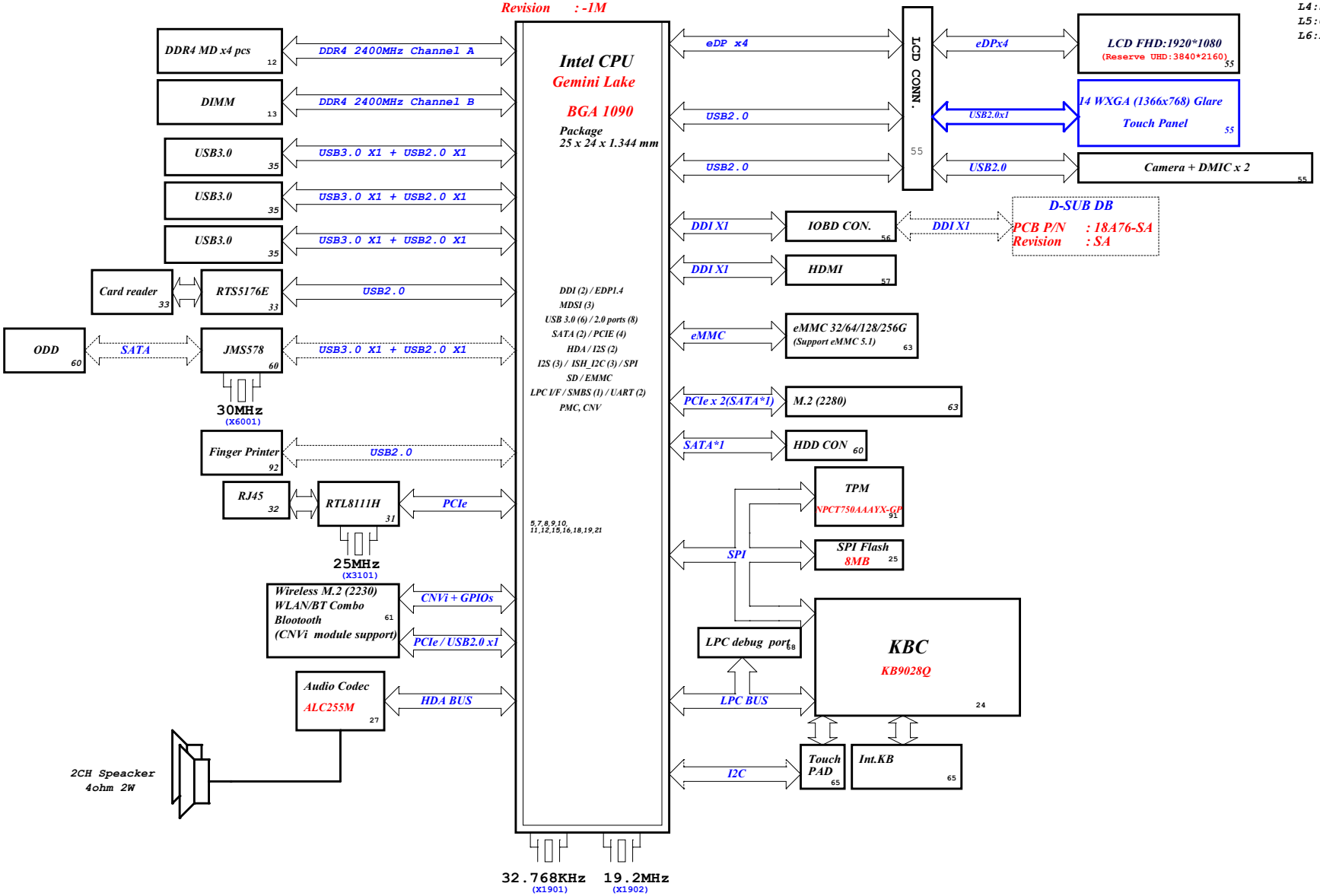
# Gemini Lake Board Block Diagram

Project code : 4PD0FT010001
PCB P/N : 18754
Revision : -1M

PCB Layer
L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND
L6:Bottom




| CHARGER BQ24780S 44 | |
|---|---|
| INPUTS | OUTPUTS |
| 19V_DCBATOUT | BT+ |

| SYSTEM DC/DC SY8288CRAC-GP 45 | |
|---|---|
| INPUTS | OUTPUTS |
| 19V_DCBATOUT | 5V_S5 |

| SYSTEM DC/DC SY8286BRAC-GP 45 | |
|---|---|
| INPUTS | OUTPUTS |
| 19V_DCBATOUT | 3D3V_S5 |

| CPU PMIC BD2671MWV-E2-GP 46 | |
|---|---|
| INPUTS | OUTPUTS |
| 19V_DCBATOUT | 1D8V_S5 |

| CPU PMIC BD9515NUXE2-GP-U 47 | |
|---|---|
| INPUTS | OUTPUTS |
| 5V_S5 | 1V_CPU_VCGI |

| CPU PMIC BD2671MWV-E2-GP 50 | |
|---|---|
| INPUTS | OUTPUTS |
| 5V_S5 | 1V_CPU_VNN<br>1D05V_S0 |

| CPU PMIC BD2671MWV-E2-GP 51 | |
|---|---|
| INPUTS | OUTPUTS |
| 19V_DCBATOUT | 1D2V_CPU_VDDQ_S3 |
| 5V_S5 | 1D2V_S5<br>2D5V_S3 |

| SYSTEM Load switch G2898KD1U 40 | |
|---|---|
| INPUTS | OUTPUTS |
| 5V_S5 | 5V_S0 |
| 3D3V_S5 | 3D3V_S0 |
| 1D8V_S5 | 1D8V_S0 |

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Title: Block Diagram
Size: A2
Document Number: Raichu_GL
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SSID = CPU

# Blanking



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Title: CPU (Reserved)

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SSID = CPU

# Blanking



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Title: CPU (Reserved)

| Size | Document Number | Rev |
|---|---|---|
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**SSID = CPU**

CPU1A — 1 OF 13 — DDR4_LP3_LP4 — DDR0

| | | | | | |
|---|---|---|---|---|---|
| M_A_DQ40 | BJ36 | MEM_CH0_DQ40 | MEM_CH0_DQS0_P | AT53 | M_A_DQS_DP0 |
| M_A_DQ41 | BK37 | MEM_CH0_DQ41 | MEM_CH0_DQS0# | AT55 | M_A_DQS_DN0 |
| M_A_DQ42 | BJ35 | MEM_CH0_DQ42 | MEM_CH0_DQS1_P | AW49 | M_A_DQS_DP1 |
| M_A_DQ43 | BL36 | MEM_CH0_DQ43 | MEM_CH0_DQS1# | AW48 | M_A_DQS_DN1 |
| M_A_DQ44 | BJ39 | MEM_CH0_DQ44 | MEM_CH0_DQS2_P | BC54 | M_A_DQS_DP2 |
| M_A_DQ45 | BL40 | MEM_CH0_DQ45 | MEM_CH0_DQS2# | BB53 | M_A_DQS_DN2 |
| M_A_DQ46 | BJ40 | MEM_CH0_DQ46 | MEM_CH0_DQS3_P | AR41 | M_A_DQS_DP3 |
| M_A_DQ47 | BK41 | MEM_CH0_DQ47 | MEM_CH0_DQS3# | AR43 | M_A_DQS_DN3 |
| M_A_DQ32 | BA35 | MEM_CH0_DQ32 | MEM_CH0_DQS4_P | AV37 | M_A_DQS_DP4 |
| M_A_DQ33 | AY33 | MEM_CH0_DQ33 | MEM_CH0_DQS4# | AV35 | M_A_DQS_DN4 |
| M_A_DQ34 | BA33 | MEM_CH0_DQ34 | MEM_CH0_DQS5_P | BL38 | M_A_DQS_DP5 |
| M_A_DQ35 | AY35 | MEM_CH0_DQ35 | MEM_CH0_DQS5# | BJ38 | M_A_DQS_DN5 |
| M_A_DQ36 | BA37 | MEM_CH0_DQ36 | MEM_CH0_DQS6_P | BF31 | M_A_DQS_DP6 |
| M_A_DQ37 | AY37 | MEM_CH0_DQ37 | MEM_CH0_DQS6# | BD31 | M_A_DQS_DN6 |
| M_A_DQ38 | AY39 | MEM_CH0_DQ38 | MEM_CH0_DQS7_P | BJ32 | M_A_DQS_DP7 |
| M_A_DQ39 | BA39 | MEM_CH0_DQ39 | MEM_CH0_DQS7# | BK31 | M_A_DQS_DN7 |
| M_A_DQ56 | BL34 | MEM_CH0_DQ56 | | | |
| M_A_DQ57 | BL30 | MEM_CH0_DQ57 | NCTF1#BG54 | BG54 | |
| M_A_DQ58 | BJ29 | MEM_CH0_DQ58 | NCTF2#BH54 | BH54 | |
| M_A_DQ59 | BK29 | MEM_CH0_DQ59 | NCTF3#BJ42 | BJ42 | |
| M_A_DQ60 | BJ33 | MEM_CH0_DQ60 | | BF39 | |
| M_A_DQ61 | BK33 | MEM_CH0_DQ61 | MEM_CH0_ODT1 | BK43 | M_A_CS#1 |
| M_A_DQ62 | BJ34 | MEM_CH0_DQ62 | MEM_CH0_CS1# | | |
| M_A_DQ63 | BJ30 | MEM_CH0_DQ63 | NCTF4#BL44 | BL44 | |
| M_A_DQ48 | BD29 | MEM_CH0_DQ48 | MEM_CH0_ODT0 | BD39 | |
| M_A_DQ49 | BF29 | MEM_CH0_DQ49 | MEM_CH0_CS0# | BJ43 | M_A_CS#0 |
| M_A_DQ50 | BH29 | MEM_CH0_DQ50 | MEM_CH0_CKE1 | BF54 | |
| M_A_DQ51 | BF33 | MEM_CH0_DQ51 | MEM_CH0_CKE0 | BF38 | M_A_CKE0 |
| M_A_DQ52 | BC29 | MEM_CH0_DQ52 | | | |
| M_A_DQ53 | BD33 | MEM_CH0_DQ53 | MEM_CH0_CLK0_P | BE49 | M_A_CLK0 |
| M_A_DQ54 | BF35 | MEM_CH0_DQ54 | MEM_CH0_CLK0# | BE51 | M_A_CLK#0 |
| M_A_DQ55 | BH35 | MEM_CH0_DQ55 | | | |
| | | | MEM_CH0_CLK1_P | BC49 | M_A_CLK1 |
| M_A_DQ0 | AR53 | MEM_CH0_DQ0 | MEM_CH0_CLK1# | BC48 | M_A_CLK#1 |
| M_A_DQ1 | AP55 | MEM_CH0_DQ1 | | | |
| M_A_DQ2 | AP53 | MEM_CH0_DQ2 | MEM_CH0_MA0 | BD45 | M_A_A0 |
| M_A_DQ3 | AN54 | MEM_CH0_DQ3 | MEM_CH0_MA1 | BH50 | M_A_A1 |
| M_A_DQ4 | AU54 | MEM_CH0_DQ4 | MEM_CH0_MA2 | BH47 | M_A_A2 |
| M_A_DQ5 | AV53 | MEM_CH0_DQ5 | MEM_CH0_MA10 | BF45 | M_A_A10 |
| M_A_DQ6 | AV55 | MEM_CH0_DQ6 | MEM_CH0_MA13 | BH43 | M_A_A13 |
| M_A_DQ7 | AW53 | MEM_CH0_DQ7 | MEM_CH0_MA16 | BD41 | M_A_A16 |
| M_A_DQ8 | AU51 | MEM_CH0_DQ8 | MEM_CH0_BA1 | BH51 | M_A_BA1 |
| M_A_DQ9 | AU48 | MEM_CH0_DQ9 | MEM_CH0_BA0 | BD43 | M_A_BA0 |
| M_A_DQ10 | AU49 | MEM_CH0_DQ10 | MEM_CH0_BG1 | BF43 | M_A_BG1 |
| M_A_DQ11 | BA46 | MEM_CH0_DQ11 | MEM_CH0_ACT# | BF41 | M_A_ACT_N |
| M_A_DQ12 | BA48 | MEM_CH0_DQ12 | MEM_CH0_MA3 | BG52 | M_A_A3 |
| M_A_DQ13 | BA49 | MEM_CH0_DQ13 | | | |
| M_A_DQ14 | BA51 | MEM_CH0_DQ14 | MEM_CH0_MA4 | BK45 | M_A_A4 |
| M_A_DQ15 | AR51 | MEM_CH0_DQ15 | MEM_CH0_MA5 | BJ46 | M_A_A5 |
| M_A_DQ16 | AY55 | MEM_CH0_DQ16 | MEM_CH0_MA6 | BJ44 | M_A_A6 |
| M_A_DQ17 | BA54 | MEM_CH0_DQ17 | MEM_CH0_MA7 | BJ47 | M_A_A7 |
| M_A_DQ18 | BA53 | MEM_CH0_DQ18 | MEM_CH0_MA8 | BJ45 | M_A_A8 |
| M_A_DQ19 | AY53 | MEM_CH0_DQ19 | MEM_CH0_MA9 | BK47 | M_A_A9 |
| M_A_DQ20 | BC53 | MEM_CH0_DQ20 | MEM_CH0_MA11 | BJ51 | M_A_A11 |
| M_A_DQ21 | BD55 | MEM_CH0_DQ21 | MEM_CH0_MA12 | BJ52 | M_A_A12 |
| M_A_DQ22 | BE54 | MEM_CH0_DQ22 | MEM_CH0_MA14 | BJ48 | M_A_A14 |
| M_A_DQ23 | BD53 | MEM_CH0_DQ23 | MEM_CH0_MA15 | BJ50 | M_A_A15 |
| M_A_DQ24 | AN43 | MEM_CH0_DQ24 | MEM_CH0_BG0 | BL50 | M_A_BG0 |
| M_A_DQ25 | AN44 | MEM_CH0_DQ25 | | | |
| M_A_DQ26 | AR48 | MEM_CH0_DQ26 | MEM_CH0_VREFDQ | AY31 | |
| M_A_DQ27 | AU41 | MEM_CH0_DQ27 | MEM_CH0_VREFCA | AV29 | M_A_VREFCA_CPU |
| M_A_DQ28 | AU43 | MEM_CH0_DQ28 | | | |
| M_A_DQ29 | AN41 | MEM_CH0_DQ29 | | | |
| M_A_DQ30 | AN39 | MEM_CH0_DQ30 | | | |
| M_A_DQ31 | AN44 | MEM_CH0_DQ31 | | | |

GEMINI-LAKE-2-GP

CPU1B — 2 OF 13 — DDR4_LP3_LP4 — DDR1

| | | | | | |
|---|---|---|---|---|---|
| M_B_DQ40 | AY3 | MEM_CH1_DQ40 | MEM_CH1_DQS0_P | BJ24 | M_B_DQS_DP0 |
| M_B_DQ41 | BD3 | MEM_CH1_DQ41 | MEM_CH1_DQS0# | BK25 | M_B_DQS_DN0 |
| M_B_DQ42 | BD1 | MEM_CH1_DQ42 | MEM_CH1_DQS1_P | BD25 | M_B_DQS_DP1 |
| M_B_DQ43 | BC3 | MEM_CH1_DQ43 | MEM_CH1_DQS1# | BF25 | M_B_DQS_DN1 |
| M_B_DQ44 | AY1 | MEM_CH1_DQ44 | MEM_CH1_DQS2_P | BL18 | M_B_DQS_DP2 |
| M_B_DQ45 | BA3 | MEM_CH1_DQ45 | MEM_CH1_DQS2# | BJ18 | M_B_DQS_DN2 |
| M_B_DQ46 | BA2 | MEM_CH1_DQ46 | MEM_CH1_DQS3_P | AV19 | M_B_DQS_DP3 |
| M_B_DQ47 | BE2 | MEM_CH1_DQ47 | MEM_CH1_DQS3# | AV21 | M_B_DQS_DN3 |
| M_B_DQ32 | AR8 | MEM_CH1_DQ32 | MEM_CH1_DQS4_P | AR13 | M_B_DQS_DP4 |
| M_B_DQ33 | AN15 | MEM_CH1_DQ33 | MEM_CH1_DQS4# | AR15 | M_B_DQS_DN4 |
| M_B_DQ34 | AN17 | MEM_CH1_DQ34 | MEM_CH1_DQS5_P | BB3 | M_B_DQS_DP5 |
| M_B_DQ35 | AU12 | MEM_CH1_DQ35 | MEM_CH1_DQS5# | BC2 | M_B_DQS_DN5 |
| M_B_DQ36 | AN12 | MEM_CH1_DQ36 | MEM_CH1_DQS6_P | AW7 | M_B_DQS_DP6 |
| M_B_DQ37 | AN13 | MEM_CH1_DQ37 | MEM_CH1_DQS6# | AW8 | M_B_DQS_DN6 |
| M_B_DQ38 | AU13 | MEM_CH1_DQ38 | MEM_CH1_DQS7_P | AT1 | M_B_DQS_DP7 |
| M_B_DQ39 | AU15 | MEM_CH1_DQ39 | MEM_CH1_DQS7# | AT3 | M_B_DQS_DN7 |
| M_B_DQ56 | AP3 | MEM_CH1_DQ56 | | | |
| M_B_DQ57 | AU2 | MEM_CH1_DQ57 | MEM_CH1_MA0 | BH9 | M_B_A0 |
| M_B_DQ58 | AV3 | MEM_CH1_DQ58 | MEM_CH1_MA1 | BC13 | M_B_A1 |
| M_B_DQ59 | AW3 | MEM_CH1_DQ59 | MEM_CH1_MA2 | BD11 | M_B_A2 |
| M_B_DQ60 | AN2 | MEM_CH1_DQ60 | MEM_CH1_MA3 | BD13 | M_B_A3 |
| M_B_DQ61 | AP1 | MEM_CH1_DQ61 | MEM_CH1_MA10 | BF11 | M_B_A10 |
| M_B_DQ62 | AR3 | MEM_CH1_DQ62 | MEM_CH1_MA13 | BE5 | M_B_A13 |
| M_B_DQ63 | AV1 | MEM_CH1_DQ63 | MEM_CH1_MA16 | BH5 | M_B_A16 |
| M_B_DQ48 | AR5 | MEM_CH1_DQ48 | MEM_CH1_BA0 | BH6 | M_B_BA0 |
| M_B_DQ49 | BA8 | MEM_CH1_DQ49 | MEM_CH1_BA1 | BF13 | M_B_BA1 |
| M_B_DQ50 | AU7 | MEM_CH1_DQ50 | MEM_CH1_BG1 | BG4 | M_B_BG1 |
| M_B_DQ51 | AU5 | MEM_CH1_DQ51 | MEM_CH1_ACT# | BE7 | M_B_ACT_N |
| M_B_DQ52 | BA5 | MEM_CH1_DQ52 | | | |
| M_B_DQ53 | BA7 | MEM_CH1_DQ53 | MEM_CH1_MA11 | BK11 | M_B_A11 |
| M_B_DQ54 | AU8 | MEM_CH1_DQ54 | MEM_CH1_MA12 | BJ12 | M_B_A12 |
| M_B_DQ55 | BA10 | MEM_CH1_DQ55 | MEM_CH1_MA14 | BK9 | M_B_A14 |
| | | | MEM_CH1_MA15 | BJ11 | M_B_A15 |
| M_B_DQ0 | BJ26 | MEM_CH1_DQ0 | MEM_CH1_BG0 | BJ10 | M_B_BG0 |
| M_B_DQ1 | BL26 | MEM_CH1_DQ1 | MEM_CH1_MA4 | BJ4 | M_B_A4 |
| M_B_DQ2 | BJ27 | MEM_CH1_DQ2 | MEM_CH1_MA5 | BL6 | M_B_A5 |
| M_B_DQ3 | BK27 | MEM_CH1_DQ3 | MEM_CH1_MA6 | BJ5 | M_B_A6 |
| M_B_DQ4 | BJ23 | MEM_CH1_DQ4 | MEM_CH1_MA7 | BJ9 | M_B_A7 |
| M_B_DQ5 | BK23 | MEM_CH1_DQ5 | MEM_CH1_MA8 | BJ6 | M_B_A8 |
| M_B_DQ6 | BJ22 | MEM_CH1_DQ6 | MEM_CH1_MA9 | BJ8 | M_B_A9 |
| M_B_DQ7 | BL22 | MEM_CH1_DQ7 | | | |
| M_B_DQ8 | BD27 | MEM_CH1_DQ8 | MEM_CH1_CLK0_P | BF17 | M_B_CLK0 |
| M_B_DQ9 | BF27 | MEM_CH1_DQ9 | MEM_CH1_CLK0# | BD17 | M_B_CLK#0 |
| M_B_DQ10 | BH27 | MEM_CH1_DQ10 | | | |
| M_B_DQ11 | BC27 | MEM_CH1_DQ11 | MEM_CH1_CLK1_P | BF15 | M_B_CLK1 |
| M_B_DQ12 | BH21 | MEM_CH1_DQ12 | MEM_CH1_CLK1# | BH15 | M_B_CLK#1 |
| M_B_DQ13 | BF23 | MEM_CH1_DQ13 | | | |
| M_B_DQ14 | BD23 | MEM_CH1_DQ14 | NCTF3#BJ13 | BJ13 | |
| M_B_DQ15 | BF21 | MEM_CH1_DQ15 | NCTF4#BL12 | BL12 | |
| M_B_DQ16 | BK19 | MEM_CH1_DQ16 | NCTF1#BF1 | BF1 | |
| M_B_DQ17 | BJ20 | MEM_CH1_DQ17 | MEM_CH1_CS1# | BF2 | M_B_CS#1 |
| M_B_DQ18 | BL20 | MEM_CH1_DQ18 | MEM_CH1_ODT1 | BC7 | M_B_ODT1 |
| M_B_DQ19 | BJ21 | MEM_CH1_DQ19 | | | |
| M_B_DQ20 | BJ17 | MEM_CH1_DQ20 | MEM_CH1_CS0# | BH2 | M_B_CS#0 |
| M_B_DQ21 | BJ16 | MEM_CH1_DQ21 | MEM_CH1_ODT0 | BC8 | M_B_ODT0 |
| M_B_DQ22 | BK15 | MEM_CH1_DQ22 | NCTF2#BG2 | BG2 | |
| M_B_DQ23 | BL16 | MEM_CH1_DQ23 | MEM_CH1_CKE0 | BK13 | M_B_CKE0 |
| M_B_DQ24 | BA21 | MEM_CH1_DQ24 | MEM_CH1_CKE1 | BJ14 | M_B_CKE1 |
| M_B_DQ25 | AY23 | MEM_CH1_DQ25 | | | |
| M_B_DQ26 | BA23 | MEM_CH1_DQ26 | MEM_CH0_RCOMP | AY29 | SM_RCOMP_0 |
| M_B_DQ27 | BA17 | MEM_CH1_DQ27 | MEM_CH1_RESET# | BC15 | SM_DRAMRST#_B |
| M_B_DQ28 | AY21 | MEM_CH1_DQ28 | MEM_CH1_RCOMP | AY27 | SM_RCOMP_1 |
| M_B_DQ29 | AY17 | MEM_CH1_DQ29 | | | |
| M_B_DQ30 | AY19 | MEM_CH1_DQ30 | MEM_CH1_VREFCA | AV25 | M_B_VREFCA_CPU |
| M_B_DQ31 | BA19 | MEM_CH1_DQ31 | MEM_CH1_VREFDQ | | |
| | | | MEM_CH0_RESET# | BC43 | SM_DRAMRST#_A |

GEMINI-LAKE-2-GP

12 M_A_DQ[63:0]
12 M_A_A[16:0]
12 M_A_DQS_DN[7:0]
12 M_A_DQS_DP[7:0]
12 M_A_CS#0
12 M_A_CLK0
12 M_A_CLK#0
12 M_A_CKE0
12 M_A_BA1
12 M_A_BA0
12 M_A_BG0
12 M_A_ACT_N
12 V_SM_VREF_CNTA
12 SM_DRAMRST#_A
13 SM_DRAMRST#_B
13 V_SM_VREF_CNTB
13 M_B_DQ[63:0]
13 M_B_A[16:0]
13 M_B_DQS_DN[7:0]
13 M_B_DQS_DP[7:0]
13 M_B_CLK0
13 M_B_CLK#0
13 M_B_CLK1
13 M_B_CLK#1
13 M_B_ODT0
13 M_B_ODT1
13 M_B_ACT_N
13 M_B_CKE0
13 M_B_CKE1
13 M_B_CS#0
13 M_B_CS#1
13 M_B_BG0
13 M_B_BG1
13 M_B_BA0
13 M_B_BA1

TP505 Do Not Stuff
TP501 Do Not Stuff
TP502 Do Not Stuff
TP503 Do Not Stuff

**WE# /A14**
**CAS#/A15**
**RAS#/A16**

R502 1 — Do Not Stuff — DY — 2 V_SM_VREF_CNTA

**WE# /A14**
**CAS#/A15**
**RAS#/A16**

R501 1 — Do Not Stuff — DY — 2 V_SM_VREF_CNTB

SM_DRAMRST#_A — ED502 — AZ5125-02S-R7G-GP
SM_DRAMRST#_B — ED501 — AZ5125-02S-R7G-GP

**75.05125.07D**
**2nd = 075.00353.0A7D**

C501 SM_DRAMRST#_A — SM_DRAMRST#_A_C — DY Do Not Stuff — R505 DY Do Not Stuff
C502 SM_DRAMRST#_B — SM_DRAMRST#_B_C — DY Do Not Stuff — R506 DY Do Not Stuff
Sensitive trace RC filter

SM_RCOMP_1 — R503 110R2F-GP
SM_RCOMP_0 — R504 110R2F-GP
#567247 #82 Figure 5-1 system memory resistive compensation

**Layout Notes:**
**DDR RCOMP trace W/S=15/15mil, and length <500mil**



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Title: **CPU (DDR)**
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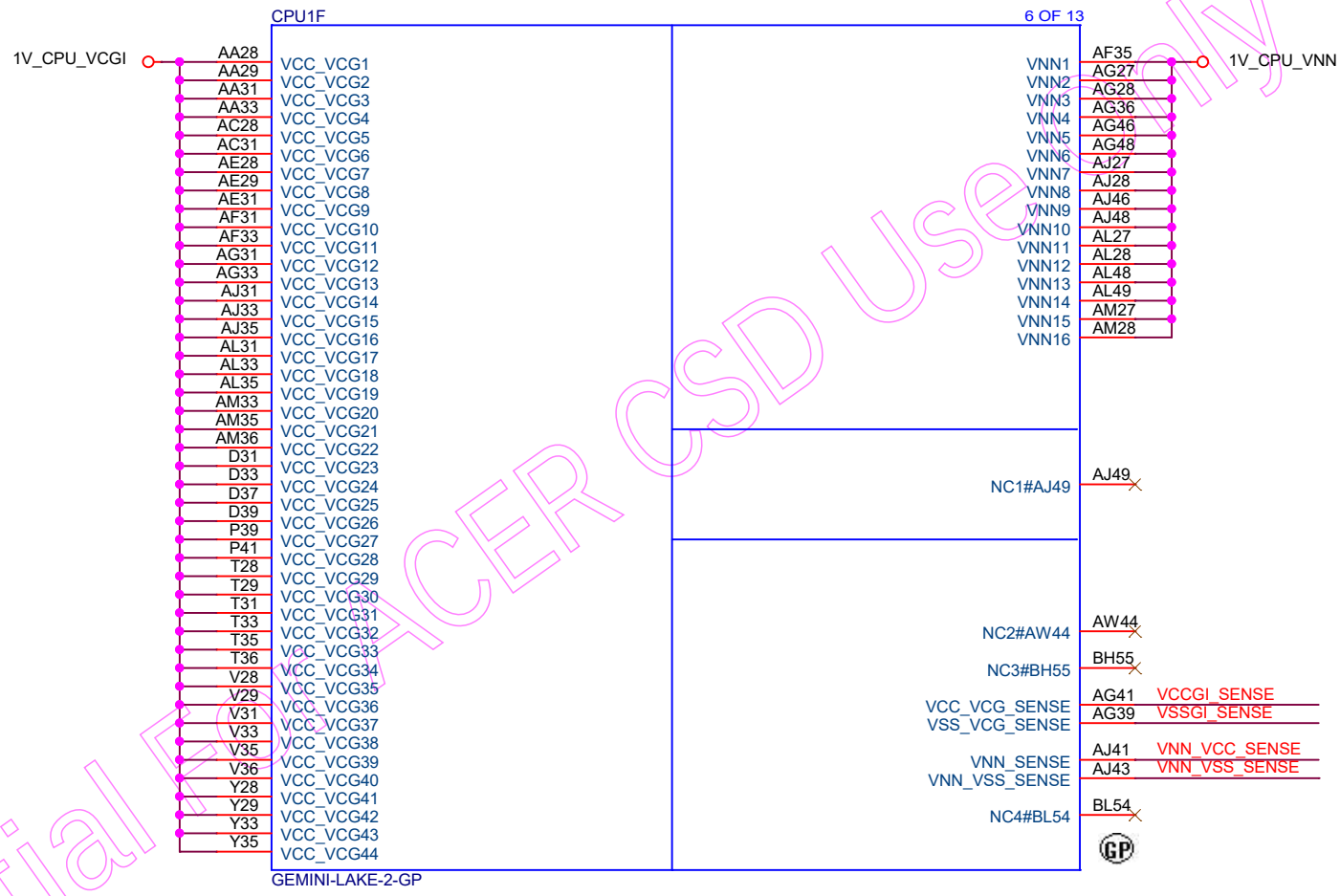
**SSID = CPU** PDG P54

47 VSSGI_SENSE
47 VCCGI_SENSE
50 VNN_VCC_SENSE
50 VNN_VSS_SENSE



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Title: **CPU (VCCGI/VNN/Others)**

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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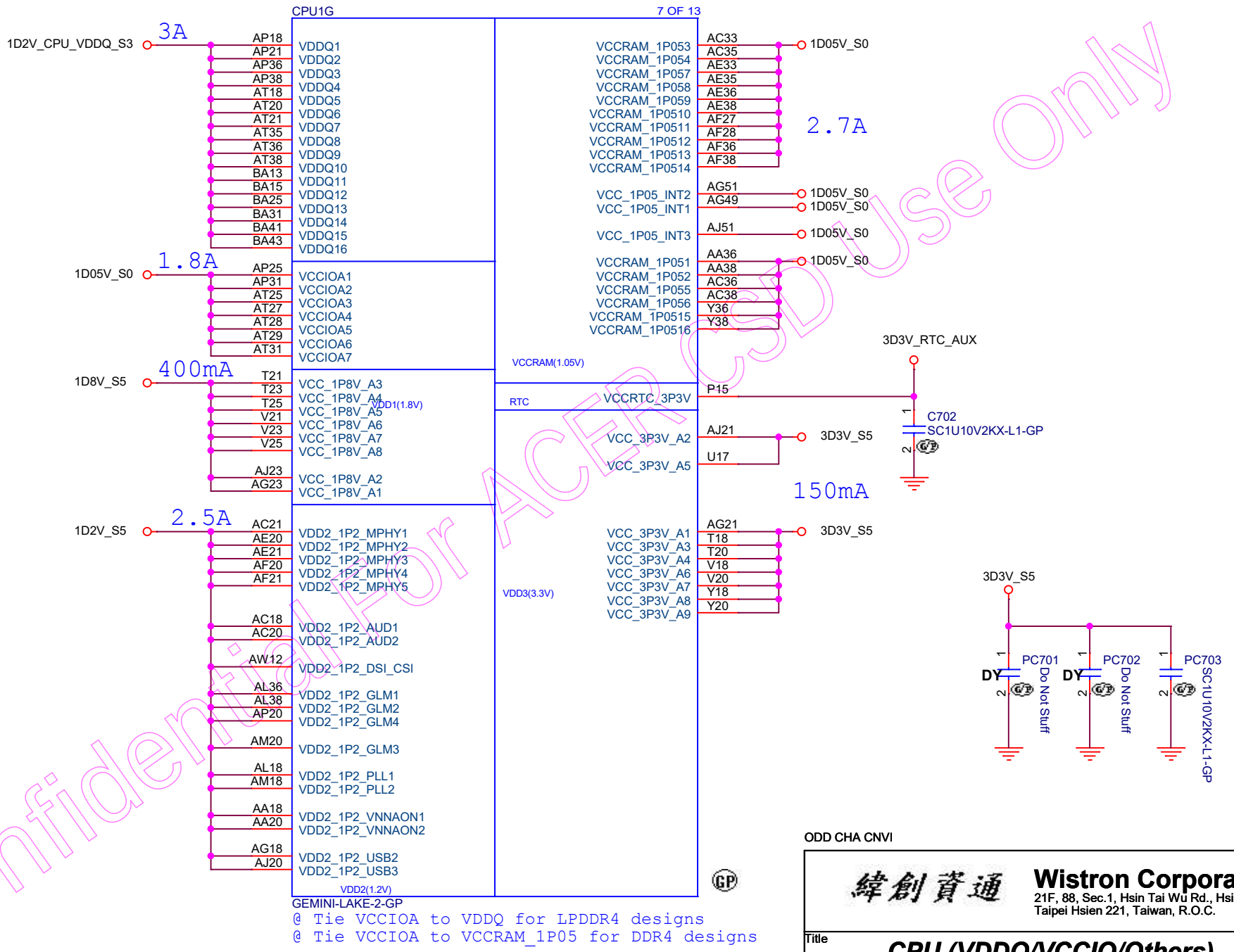
**SSID = CPU**



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VDDQ/VCCIO/Others)**

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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SSID = CPU

## CRT

56 CRT_DDI_TX_P0
56 CRT_DDI_TX_N0
56 CRT_DDI_TX_P1
56 CRT_DDI_TX_N1
56 CRT_AUX_CPU_P
56 CRT_AUX_CPU_N
56 CRT_HPD_CON

## HDMI

57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_HPD_CON

## EDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
24 eDP_BLEN_CPU
55 eDP_VDDEN_CPU
55 eDP_HPD_CPU
55 eDP_BLCTRL_CPU

15 GPIO42_FLASH_OVR
24 ME_UNLOCK

CRT_HPD_CON → Q806 (CRT) → CRT_HPD_CPU
R802 Do Not Stuff (CRT)
Do Not Stuff
2ND = 084.27002.0N31
3rd = 084.27002.0L31

SB-20180629
3D3V_S5 → R808 Do Not Stuff (CRT)

HDMI_HPD_CON → Q805 → HDMI_DET_CPU
R820 100KR2J-4-GP
PJA138KA-GP
084.00138.0A31
-1M:20181001

SB-20180629
3D3V_S5 → R809 10KR2J-L-GP
3D3V_S5 → RN802 Do Not Stuff (DY) (HDMI)

1D8V_S0 → R807 100KR2J-4-GP
eDP_HPD_CPU → Q802 → eDP_HPD_CPU_D
PJA138KA-GP
084.00138.0A31

HV_DDIX_HPD
It is required to enable internal 20k pull up resistor on the HV_DDI2_HPD signals by BIOS.

| Offset from 0x48 | Bits | Default Value | Description | Usage | FIT Visible |
|---|---|---|---|---|---|
| 0x048h (Cont'd) | 36 | 1'h0 | GPIO_134 (vccio_pad_gpio_134): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V | | Yes |
| | 35 | 1'h1 | HV_EDP_HPD (vccio_pad_hv_edp_hpd): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default) | | Yes |
| | 34 | 1'h0 | HV_DDI1_HPD (vccio_pad_hv_ddi1_hpd): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V | | Yes |
| | 33 | 1'h0 | HV_DDI0_HPD (vccio_pad_hv_ddi0_hpd): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V | | Yes |
| | 32 | 1'h1 | PANEL0_BKLTCTL (vccio_pad_panel0_bkltctl): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default) | | Yes |
| | 31 | 1'h1 | PANEL0_BKLTEN (vccio_pad_panel0_bklten): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default) | | Yes |
| | 30 | 1'h1 | PANEL0_VDDEN (vccio_pad_panel0_vdden): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default) | | Yes |
| | 29 | 1'h0 | HV_DDI1_DDC_SCL (vccio_pad_hv_ddi1_ddc_scl): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V | | Yes |
| | 28 | 1'h0 | HV_DDI1_DDC_SDA (vccio_pad_hv_ddi1_ddc_sda): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V | | Yes |
| | 27 | 1'h0 | HV_DDI0_DDC_SCL (vccio_pad_hv_ddi0_ddc_scl): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V | | Yes |
| | 26 | 1'h0 | HV_DDI0_DDC_SDA (vccio_pad_hv_ddi0_ddc_sda): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V | | Yes |

## CRT

CPU1C — 3 OF 13

CRT_DDI_TX_P0 AH1 → DDI0_TXP_0
CRT_DDI_TX_N0 AH3 → DDI0_TXN_0
CRT_DDI_TX_P1 AE2 → DDI0_TXP_1
CRT_DDI_TX_N1 AE3 → DDI0_TXN_1
AJ2 → DDI0_TXP_2
AJ3 → DDI0_TXN_2
AG2 → DDI0_TXP_3
AG3 → DDI0_TXN_3
CRT_AUX_CPU_P AC12 → DDI0_AUXP
CRT_AUX_CPU_N AC10 → DDI0_AUXN
CRT_HPD_CPU C39 → DDI0_HPD
B43 → DDI0_DDC_SCL
C43 → DDI0_DDC_SDA
DDI0/DDI_B

3.3V (default)

## HDMI

HDMI_DDI_TX_P2 AA2 → DDI1_TXP_0
HDMI_DDI_TX_N2 AA3 → DDI1_TXN_0
HDMI_DDI_TX_P1 Y3 → DDI1_TXP_1
HDMI_DDI_TX_N1 Y1 → DDI1_TXN_1
HDMI_DDI_TX_P0 AD1 → DDI1_TXP_2
HDMI_DDI_TX_N0 AD3 → DDI1_TXN_2
HDMI_DDI_TX_P3 AC2 → DDI1_TXP_3
HDMI_DDI_TX_N3 AC3 → DDI1_TXN_3
AC7 → DDI1_AUXP
AC5 → DDI1_AUXN
HDMI_SCL_CPU C42 → DDI1_DDC_SCL
HDMI_SDA_CPU A42 → DDI1_DDC_SDA
HDMI_DET_CPU C38 → DDI1_HPD
DDI1/DDI_C

1.8V level
3.3V (default)

## EDP

eDP_TX_CPU_P0 AE12 → EDP_TXP_0
eDP_TX_CPU_N0 AE13 → EDP_TXN_0
eDP_TX_CPU_P1 AC15 → EDP_TXP_1
eDP_TX_CPU_N1 AC17 → EDP_TXN_1
eDP_TX_CPU_P2 AE10 → EDP_TXP_2
eDP_TX_CPU_N2 AE8 → EDP_TXN_2
eDP_TX_CPU_P3 AE5 → EDP_TXP_3
eDP_TX_CPU_N3 AE7 → EDP_TXN_3
eDP_AUX_CPU_P W17 → EDP_AUXP
eDP_AUX_CPU_N W15 → EDP_AUXN
eDP_HPD_CPU_D B39 → EDP_HPD
eDP_BLCTRL_CPU_E B41 → PNL0_BKLCTL
eDP_BLEN_CPU C40 → PNL0_BKLTEN
eDP_VDDEN_CPU_E C41 → PNL0_VDDEN
EDP_RCOMP_P AA5 → EDP_RCOMP_P
EDP_RCOMP_N AA7 → EDP_RCOMP#
GEMINI-LAKE-2-GP
eDP/DDI_A

1.8V (default)

R801 100R2F-L-GP-U
#567247 #253 Table15-6
eDP signals disable guideline

Layout Notes:
Impedance 85 Ohm and space 20mil, length <400mil.

3D3V_S0 → RN801 Do Not Stuff (DY)
SB-20180629
-1M:20180903
eDP_BLCTRL_CPU → R812 → eDP_BLCTRL_CPU_E
eDP_VDDEN_CPU → R813 → eDP_VDDEN_CPU_E
Do Not Stuff

MDSI_A_CLKP AL2
MDSI_A_CLKN AM3
MDSI_C_CLKP AG13
MDSI_C_CLKN AG12
MDSI_A_DP_0 AN5
MDSI_A_DN_0 AN7
MDSI_A_DP_1 AJ15
MDSI_A_DN_1 AJ17
MDSI_A_DP_2 AJ7
MDSI_A_DN_2 AJ5
MDSI_A_DP_3 AJ10
MDSI_A_DN_3 AJ12
MDSI_C_DP_0 AG15
MDSI_C_DN_0 AG17
MDSI_C_DP_1 AG8
MDSI_C_DN_1 AG10
MDSI_C_DP_2 AG7
MDSI_C_DN_2 AG5
MDSI_C_DP_3 AE15
MDSI_C_DN_3 AE17
MDSI

MIPI_I2C_SCL → R53
MIPI_I2C_SDA → R54

GPIO_43 MDSI_C_TE → T53 GPIO43_DSI_TE2 → TP801
GPIO_42 MDSI_A_TE → T55 GPIO42_FLASH_OVR
R811 ME_UNLOCK
Do Not Stuff

MDSI_RCOMP AL5 → MDSI_RCOMP
R810 150R2F-4-L-GP

Layout Notes:
layout W/S=10/15mil, length <1000mil.

15.1.2.5HPD Implementation
The hot-plug detect output from eDP* sink device is a 3.3V active high signal. Since the input on the processor is a 3.3V active low signal, a logic inversion circuit is required on the motherboard. Fi gure 15-7 shows an example of this implementation.



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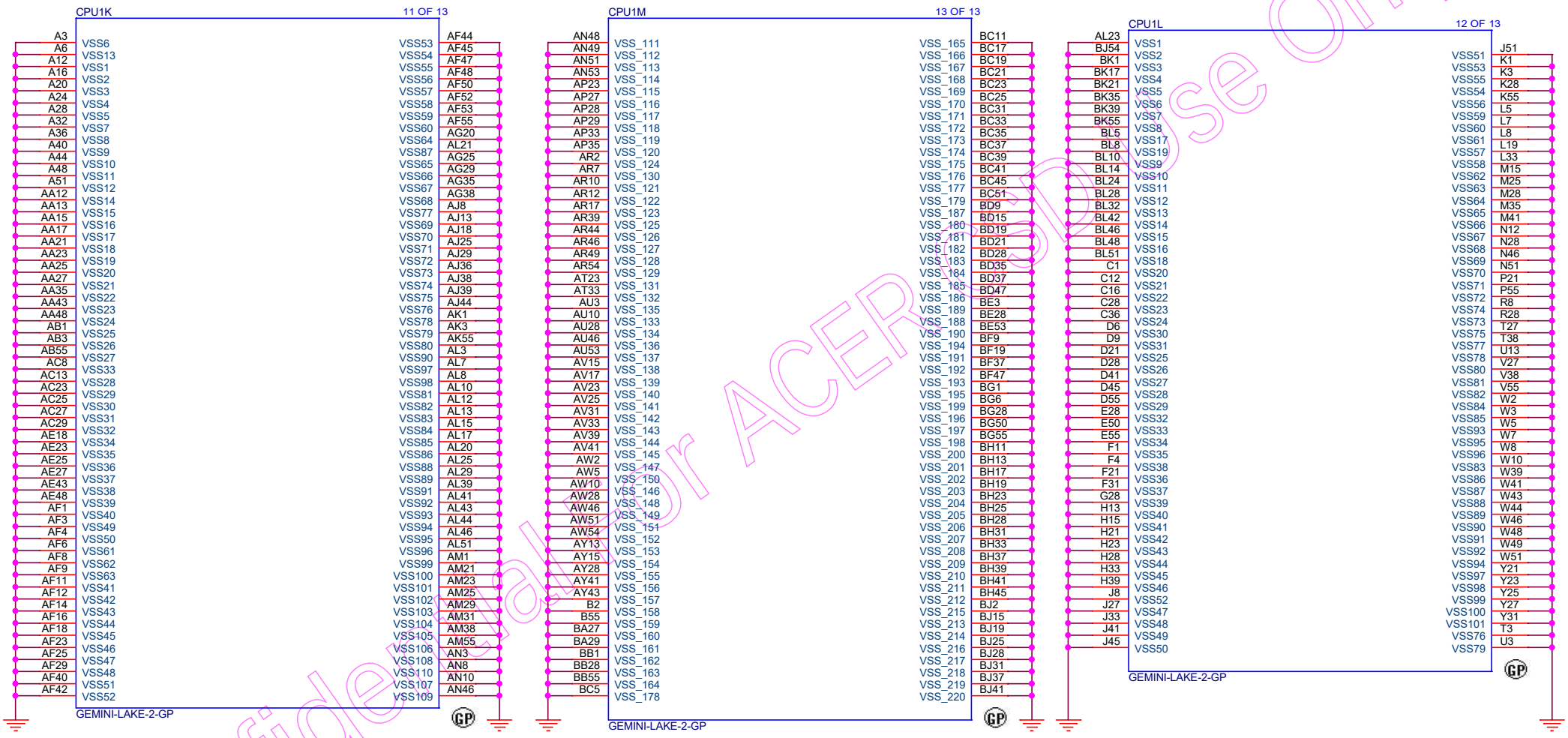
Title: CPU (DDI/EDP/MDSI)
Size: Custom | Document Number: Raichu_GL | Rev: -1M
Date: Monday, October 01, 2018 | Sheet 8 of 106

SSID = CPU



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Title: CPU (VSS)

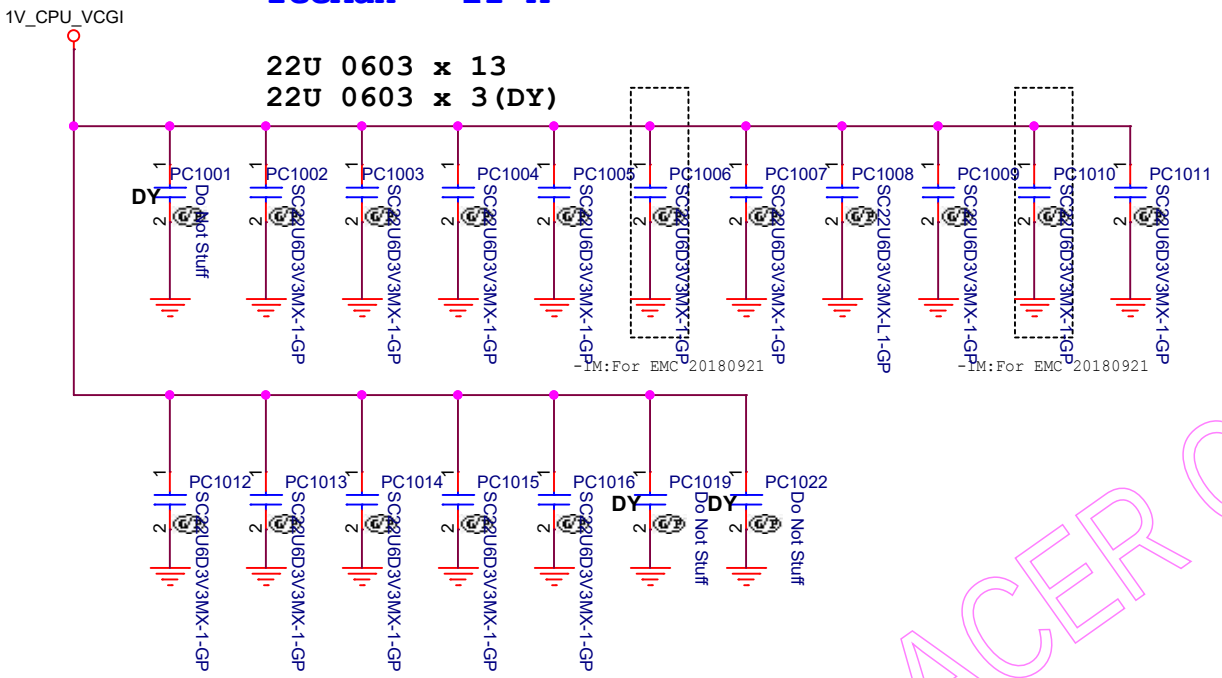
| Size | Document Number | Rev |
|---|---|---|
| Custom | Raichu_GL | -1M |

Date: Monday, October 01, 2018 Sheet 9 of 106

**SSID = CPU**

# VCCGI

**IccMax = 21 A**




# VNN

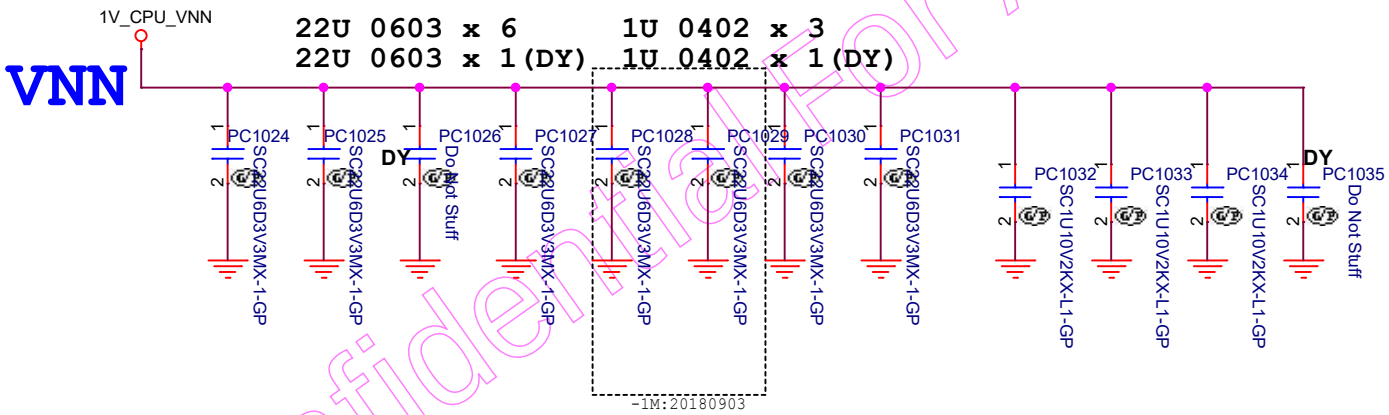



Table 4-3. Decoupling Requirements of BSC, ESC, MLCC, Bulk Cap and SoC Ball Groups (Sheet 1 of 2)

| System Rail Name | Power Balls [GND] | Max L from Ball to nearest BSC [0402-1uF] | | | Max L from Ball to nearest ESC [0402 - 1uF] | | | Max L from Ball to nearest MLCC [0603 - 22uF *0805 - 22uF #0805 - 47uF] | | | Max L / R from Ball to VR Bulk [330uF_9mOhm] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Back Side Cap | BSC (nH) | Total (nH) | Top Side Edge Cap | ESC (nH) | Total (nH) | Top Side MLCC | MLCC (nH) | Total (nH) | Top Side Bulk | Bulk (nH) | (mΩ) |
| VCC_VCGI | T28,T29,T31,T33,T35,T36, V28,V29,V31,V33,V35,V36, Y28,Y29,Y33,Y35,AA28,AA29,A A31,AA33,C28,AC31,AE28,E29, AE31,F31,AF33,AG31,AG33,AJ 31,AJ33,AJ35,AL31,AL33,AL35, AM33,AM35,AM36,D33,D39,D3 1,P41,P39,D37 [AM38,AG38,Y27,AA27,AC27,A F29,AG29,AJ29,AL29,AM29,AM 31,AP29,V27,T27,R28,Y31,AG3 5,AJ36,AA35,AC29,V38,T38,C3 6,E28,F31,H39,E27,AP33,AP35 ,M41, AL39,N28,D41] | C414 C410 C422 C440 C420 C411 C407 C425 C441 C416 C426 C421 | 1.3 0.875 1.1 0.654 0.496 0.452 0.602 0.688 0.405 0.387 0.417 0.386 | 0.103 | | | | C612 C613 C614 C615 C616 C617 C618 | 0.424 0.418 0.425 0.409 0.406 0.437 0.420 | 0.226 | C702 C703 | 0.410 0.415 | 1.41 1.41 |
| VNN-SVID | AF35,G36,G27,AG28,AJ27,AJ2 8,AL27,AL28,AJ48,AL48,AL49,A J46,AG46,AG48,AM28,AM27 [AF29,AG29,AJ29,AL29,AM29,A P27,AP28,AP29,AF25,AG25,AJ2 5,AL25,AM25,AG35,AJ36,AG38 ,AL46,AN48,AN49,AJ44,AF45,A F47,AF48,AL51] | C431 C401 C419 C430 | 0.565 0.652 0.435 0.434 | 0.332 | | | | C605 C606 C604 | 1.68 1.78 1.75 | 1.519 | | | |



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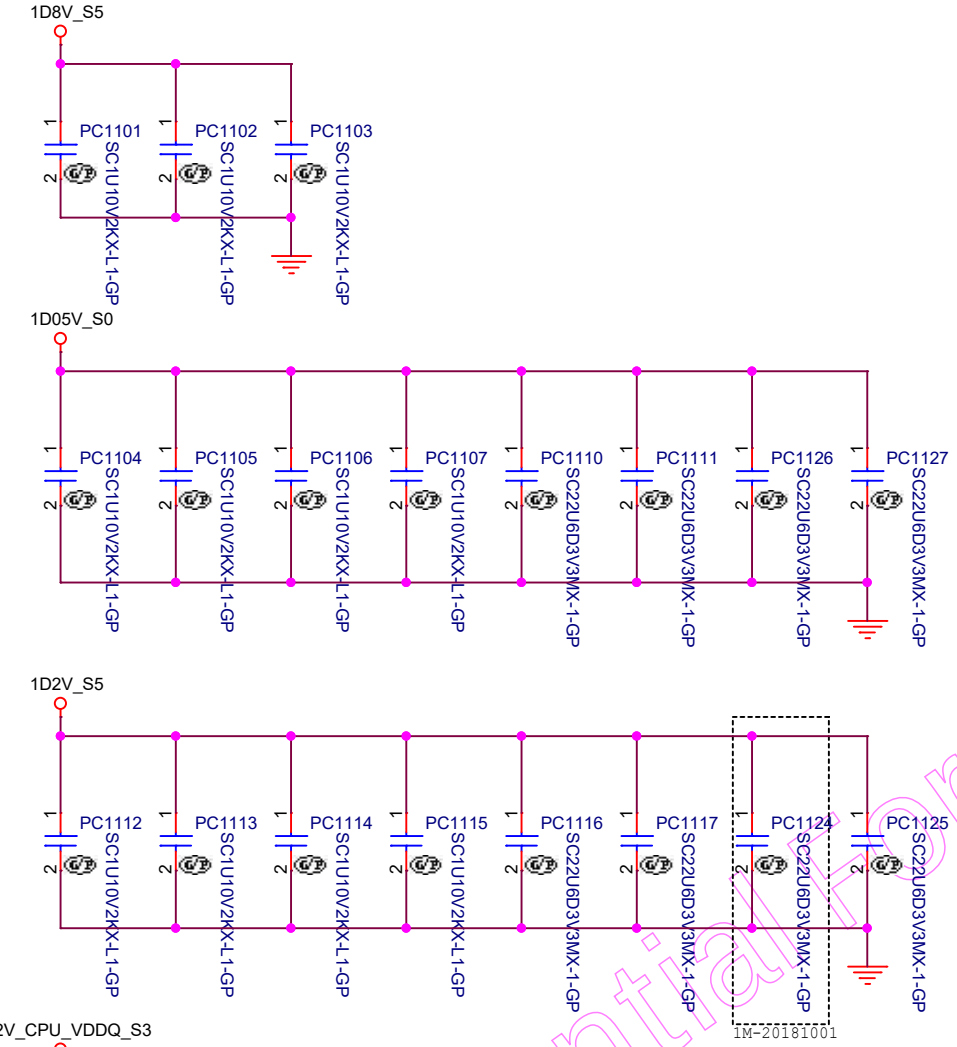
Title: **CPU (Power CAP1)**

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |
| Date: Monday, October 01, 2018 | Sheet 10 of 106 | |

# SSID = CPU




| System Rail Name | Power Balls [GND] | Max L from Ball to nearest BSC [0402-1uF] | | | Max L from Ball to nearest ESC [0402 - 1uF] | | | Max L from Ball to nearest MLCC [0603 - 22uF *0805 - 22uF #0805 - 47uF] | | | Max L / R from Ball to VR Bulk [330uF_9mOhm] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Back Side Cap | BSC (nH) | Total (nH) | Top Side Edge Cap | ESC (nH) | Total (nH) | Top Side MLCC | MLCC (nH) | Total (nH) | Top Side Bulk | Bulk (nH) | (mΩ) |
| VCC_1P8V_A | V21,T25,V25,T23,V23,T21 [Y27,Y25,Y23,Y21,T27,V27,P21 ] AJ23,AG23[AJ25, AG25] | C417 C438 BSC_USB | 1.36 0.714 1.29 | 0.673 | | | | | | | | | |
| VCCIOA | AT27,AT28,AT29,AT25,AP31,AT31,AP25 [AM29,AP27,AP28,AP28,AP33,AT33,AP23,AT23,AU28,AM31] | C429 C418 | 0.475 0.475 | 0.426 | C202 C203 | 3.72 4.10 | 3.6 | C601 C602 | 5.12 4.78 | 4.537 | | | |
| VDDQ | AP36,AT36,AP38,AT38,AT35,AT18,AP18,AP21,AT20,AT21,BA43,BA41,BA31,BA13,BA15,BA25 [AV39,AR39,AP35,AM38,AT33,AP33,AT23,AR17,AP23,AM23,AM21,AY43,AV33,BC31,AV23,AV17,AV41,AY41,BC25,AY13,AY15 ] | C412 C428 | 0.475 0.523 | 0.223 | | | | *C816 *C817 *C820 *C821 | 2.06 4.10 1.62 3.30 | 0.496 | | | |
| VCCRAM_1P05 | AC35,AE35,AE38,AE36,AF28,AF27,AF38,AF36,AC33,AE33 [AE27,AF29,AF40,AG38,AJ38,AC29,AA35,AG35,AJ36,AF25] | C424 | 0.712 | | | | | C608 | 2.89 | | | | |
| VCCRAM_1P05_IO | AA36,AA38,Y36,Y38,AC38,AC36 [V38,W39,AF40,W41,T38,AA35 ] | C405 | 0.989 | | | | | C609 | 3.62 | | | | |
| VDD2_1P24_GLM | AP20,AL38,AL36 [AM21,AR17,AJ38, AJ36] | C415 | 0.619 | | C219 | 1.78 | | C610 C611 | 2.10 2.09 | 1.978 | | | |
| VDD2_1P24_AUD_ISH_PLL | AM18,AL18 [AJ18, AL17] | C435 | 0.791 | | | | | #C823 #C824 | 1.88 1.88 | 1.75 | | | |
| VDD2_1P24_USB2 | AJ20,AG18 [AG20, AJ18] | C433 | 0.747 | | C217 | 1.723 | | C623 | 2.13 | | | | |
| VDD2_1P24_MPHY | AC21,AE20,AE21,AF20,AF21 [AG20,AF18,AE18,AA23,AC23,AE23,AF23,AA21] | C442 | 0.667 | | C218 | 1.6 | | C624 | 2.08 | | | | |
| VDD2_1P24_DSI_CSI | AW12[AW10] | | | | | | | C625 | 2.22 | | | | |



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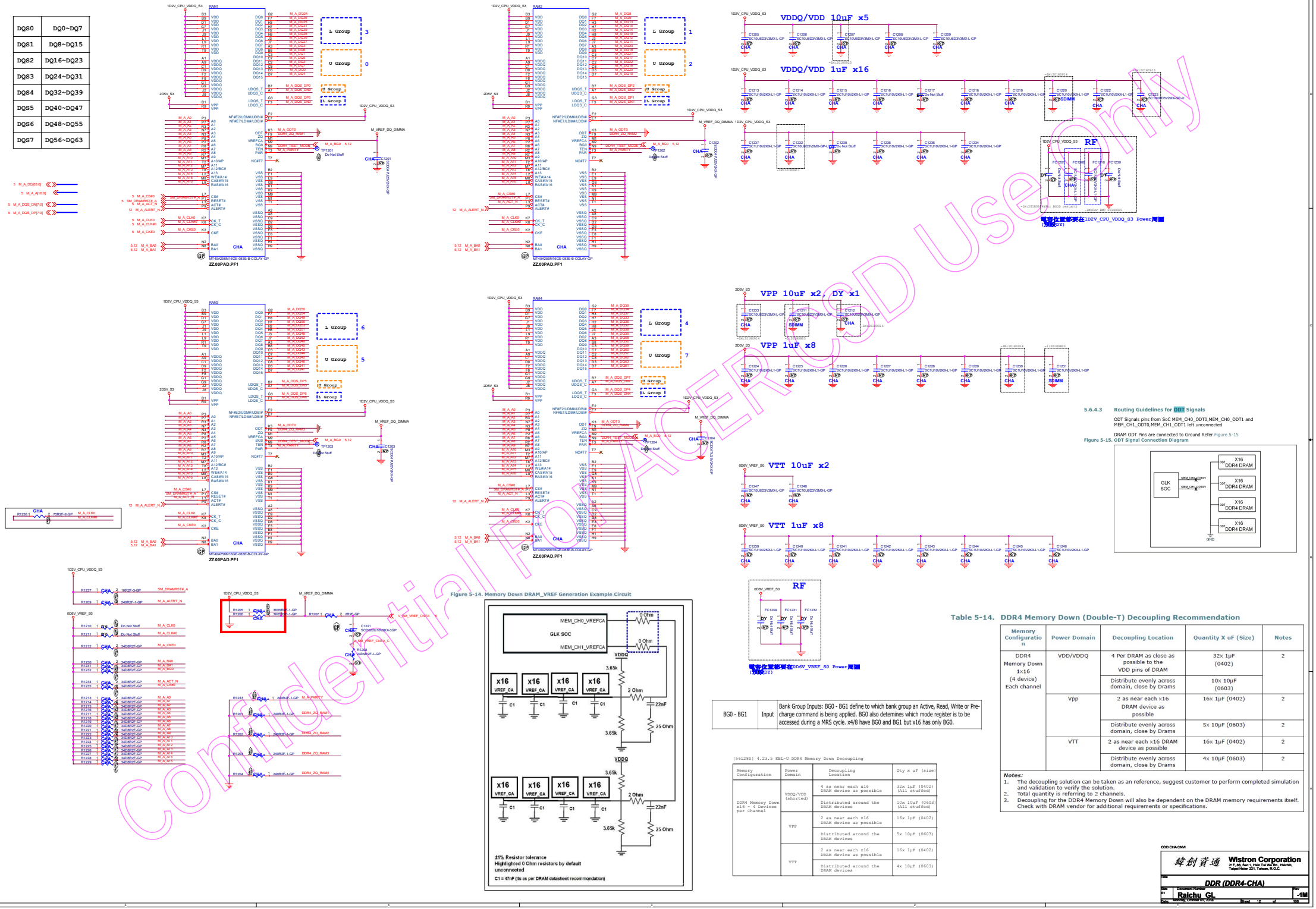
Title: CPU (Power CAP2)

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

Date: Monday, October 01, 2018 Sheet 11 of 106

# Main Func = DDR4 On Board with Single Rank

| | |
|---|---|
| DQS0 | DQ0~DQ7 |
| DQS1 | DQ8~DQ15 |
| DQS2 | DQ16~DQ23 |
| DQS3 | DQ24~DQ31 |
| DQS4 | DQ32~DQ39 |
| DQS5 | DQ40~DQ47 |
| DQS6 | DQ48~DQ55 |
| DQS7 | DQ56~DQ63 |




| | | |
|---|---|---|
| BG0 - BG1 | Input | Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Pre-charge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0. |

[561280] 4.23.5 KBL-U DDR4 Memory Down Decoupling

| Memory Configuration | Power Domain | Decoupling Location | Qty x µF (size) |
|---|---|---|---|
| DDR4 Memory Down x16 - 4 Devices per Channel | VDDQ/VDD (shorted) | 4 as near each x16 DRAM device as possible | 32x 1µF (0402) (All stuffed) |
| | | Distributed around the DRAM devices | 10x 10µF (0603) (All stuffed) |
| | VPP | 2 as near each x16 DRAM device as possible | 16x 1µF (0402) |
| | | Distributed around the DRAM devices | 5x 10µF (0603) |
| | VTT | 2 as near each x16 DRAM device as possible | 16x 1µF (0402) |
| | | Distributed around the DRAM devices | 4x 10µF (0603) |

Table 5-14. DDR4 Memory Down (Double-T) Decoupling Recommendation

| Memory Configuration | Power Domain | Decoupling Location | Quantity X uF (Size) | Notes |
|---|---|---|---|---|
| DDR4 Memory Down 1x16 (4 device) Each channel | VDD/VDDQ | 4 Per DRAM as close as possible to the VDD pins of DRAM | 32x 1µF (0402) | 2 |
| | | Distribute evenly across domain, close by Drams | 10x 10µF (0603) | |
| | Vpp | 2 as near each x16 DRAM device as possible | 16x 1µF (0402) | 2 |
| | | Distribute evenly across domain, close by Drams | 5x 10µF (0603) | 2 |
| | VTT | 2 as near each x16 DRAM device as possible | 16x 1µF (0402) | 2 |
| | | Distribute evenly across domain, close by Drams | 4x 10µF (0603) | 2 |

*Notes:*
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 Memory Down will also be dependent on the DRAM memory requirements itself. Check with DRAM vendor for additional requirements or specifications.



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Title: DDR (DDR4-CHA)

Size: A3 | Document Number: Raichu_GL | Rev: -1M

Date: Monday, October 01, 2018 | Sheet 12 of 86

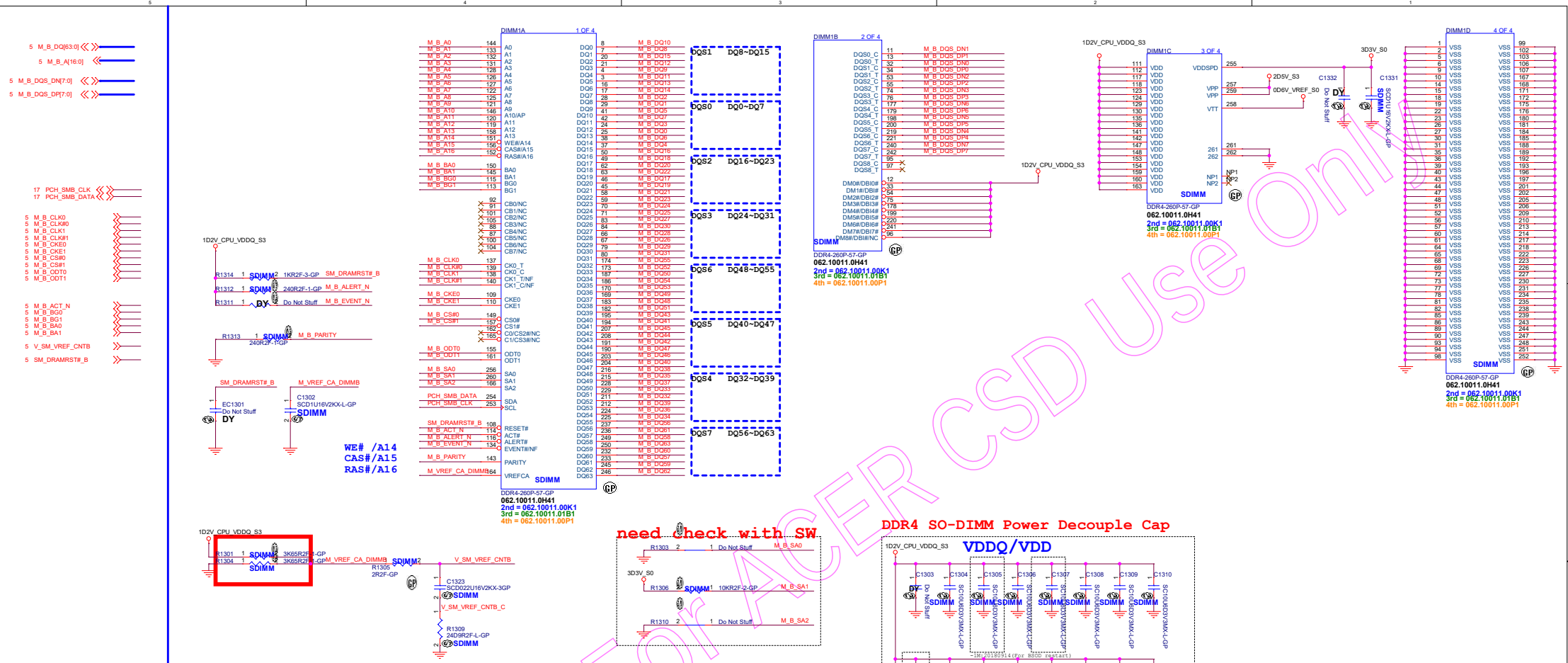




Table 5-9. SODIMM DDR4 VREF Layout Requirements

| Parameter | Guidelines |
|---|---|
| VREF Width | 15 mils / 0.381 mm in the main route |
| VREF Spacing | 15 mils / 0.381 mm in the main route |
| MEM_CH0/1_VREFCA | Left unconnected, Provide "0" Ohm series Resistor with "No Stuff" |
| SODIMM ECC bit signals Pins and DM8 Pin | Should be pulled to VDDQ |
| VREFDQ | Left unconnected |
| SODIMM "ALERT" and "EVENT" Pins | Should be pulled to VDDQ WITH 240 Ohm Resistor |
| SODIMM "Parity" pin | Should be pulled down to GND WITH 240 Ohm Resistor |

Figure 5-8. SODIMM DRAM_VREF Generation Example Circuit

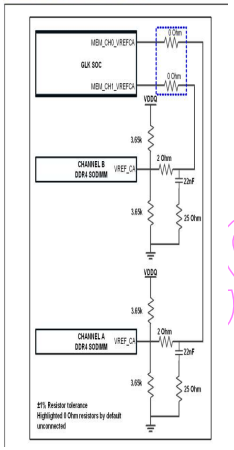


Table 5-10. DDR4 Decoupling Recommendation for SODIMM

| Memory Configuration | Power Domain | Decoupling Location | Quantity X uF (Size) | Notes |
|---|---|---|---|---|
| DDR4 SODIMM 1DPC | VDDQ | 4 near each side of the DIMM connector close to VDD pins | 16x 1μF (0402) | |
| | | | 16x 10μF (0603) | |
| | | 4 near each side of the DIMM connector close to VDD pins | 2x - 4x 0.1μF (0402) | |
| | VTT | On the Vtt island | 1x 22μF (0603) or 2x 10μF (0603) | 3<br>3 |

*Notes:*
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 SODIMM will also be dependent on the SODIMM requirements itself. Check with your SODIMM vendor for additional requirements or specifications.

[561280] 4.23.6 KBL-U DDR4 SODIMM Decoupling

| Memory Configuration | Power Domain | Decoupling Location | Qty x μF (size) |
|---|---|---|---|
| DDR4 SODIMM 1DPC | VDDQ | 4 near each side of the DIMM connector close to VDD pins | 16x 10μF (0603) |
| | | 4 near each side of the DIMM connector close to VDD pins | 16x 1μF (0402) |
| | | 1 placeholder | 1x 330μF (7343) |
| | VTT | Place these caps on the VTT plane close to SODIMM | 1x 10μF (0805) |
| | | Placeholder<br>Place these caps on the VTT plane close to SODIMM | 1x 10μF (0805) |
| | | Place these caps on the VTT plane close to SODIMM | 4x 1μF (0402) |
| | VPP | DRAM Side | 2x 10μF (0603) |
| | | DRAM Side | 2x 1μF (0402) |
| | VDDSPD | Place close to DIMM | 1x 0.1μF (0402) |
| | | Place close to DIMM | 1x 2.2μF (0402) |

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Title: DDR4_SODIMM
Size: A2 | Document Number: Raichu_GL | Rev: -1M
Date: Monday, October 01, 2018 | Sheet 13 of 106

SSID = DDR

# Blanking





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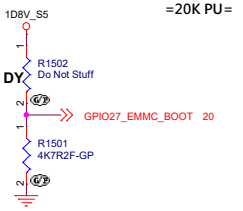
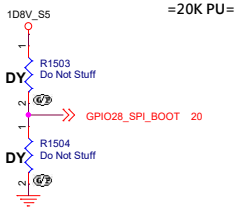
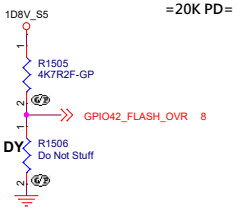
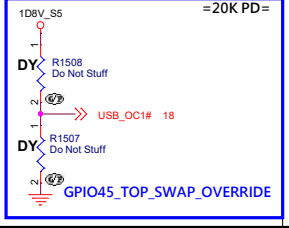
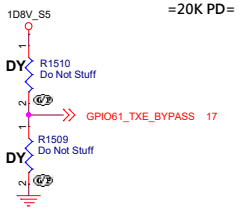
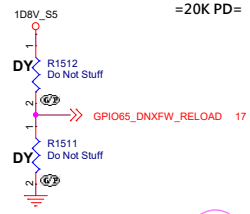
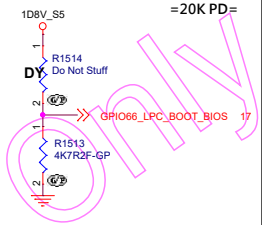
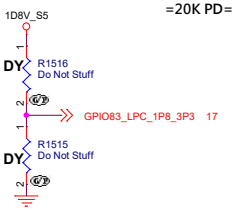
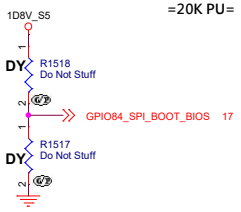
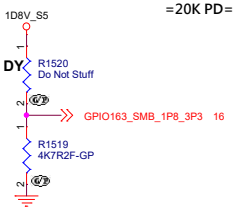
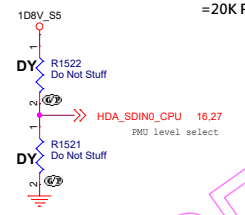
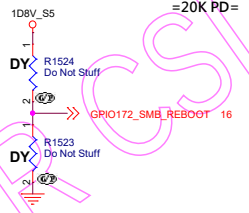
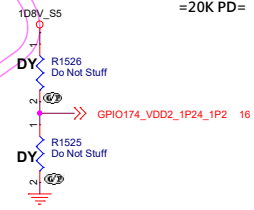
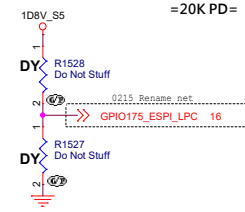
Title: *DDR (Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

Date: Monday, October 01, 2018 Sheet 14 of 106

# SSID = STRAP

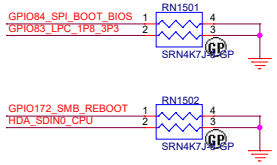
| GPIO | GPIO_27 | GPIO_28 | GPIO_42 | GPIO_45 | GPIO_61 | GPIO_65 | GPIO_66 |
|---|---|---|---|---|---|---|---|
| Schematic |  |  |  |  |  |  |  |
| High | Enable =default= | Enable =default= | Override Normal | Enable =debug= | Enable | Force | Boot form LPC |
| Low | Disable | Disable | No Override | Disable =default= | Disable =default= | Not Force =default= | Not form LPC =default= |

| GPIO | GPIO_83 | GPIO_84 | GPIO_163 | GPIO_168 | GPIO_172 | GPIO_174 | GPIO_175 |
|---|---|---|---|---|---|---|---|
| Schematic |  |  |  |  |  |  |  |
| High | Buffer set 1.8v | Disable boot from SPI | 1.8v | 1.8v | Enable | 1.24v | eSPI mode |
| Low | Buffer set 3.3v =default= | Enable boot from SPI =default= | 3.3v =default= | 3.3v =default= | Disable =default= | 1.20v =default= | LPC mode =default= |

| GPIO # | Pin Name | Purpose | Internal Termination | Pin Strap Usage/Description/Polarity |
|---|---|---|---|---|
| GPIO_27 | GPIO_27 | Allow eMMC as a boot source | 20K PU | 1=enable (default);<br>0=disable;<br>If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC |
| GPIO_28 | GPIO_28 | Allow SPI as a boot source | 20K PU | 1=enable (default)<br>0=disable<br>***Note:*** If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI. |
| GPIO_42 | MDSI_A_TE | Flash Descriptor Override | 20K PD | 0 = No Override (Normal Operation)<br>1 = Override<br>***Note:*** This strap enables the platform to override security features in the SPI. |
| GPIO_45 | USB2_OC1_N | Top swap override | 20K PD | 1 = Enable<br>0 = Disable (default)<br>***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only. |
| GPIO_61 | SIO_UART0_TXD | Enable TXE ROM Bypass | 20K PD | 1 = enable bypass<br>0 = disable bypass (default)<br>***Note:*** This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead. |

| GPIO # | Pin Name | Purpose | Internal Termination | Pin Strap Usage/Description/Polarity |
|---|---|---|---|---|
| GPIO_174 | AVS_M_CLK_AB2 | VDD2 1.24V vs. 1.20V select | 20K PD | 1=VDD2 is 1.24V;<br>0=VDD2 is 1.20V (default) |
| GPIO_175 | AVS_M_DATA_2 | eSPI vs. LPC | 20K PD | 1=eSPI mode;<br>0=LPC mode (default)<br>Note: The default for A0 will be eSPI due to a bug on LPC. |

| GPIO # | Pin Name | Purpose | Internal Termination | Pin Strap Usage/Description/Polarity |
|---|---|---|---|---|
| GPIO_65 | SIO_UART2_TXD | Force DNX FW Load | 20K PD | 1 = Force<br>0 = Do not force (default)<br>***Notes:***<br>1. DnX: Download and Execute<br>2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap. |
| GPIO_66 | SIO_UART2_RTS_N | LPC boot BIOS strap | 20K PD | 1=boot from LPC;<br>0=do not boot from LPC (default)<br>***Note:*** The board should strap this low and do not use otherwise |
| GPIO_83 | SIO_SPI_0_TXD | LPC 1.8V/3.3V mode select | 20K PD | 1=buffers set to 1.8V mode<br>0=buffers set to 3.3V mode (default) |
| GPIO_84 | SIO_SPI_2_CLK | Allow SPI as a boot source | 20K PU | 1=disable<br>0=enable (default) |
| GPIO_163 | AVS_I2S1_WS_SYNC | SMBus 1.8V/3.3V mode select | 20K PD | 1=buffers set to 1.8V mode<br>0=buffers set to 3.3V mode (default) |
| GPIO_164 | AVS_I2S1_SDI | RSVD | 20K PD | Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation. |
| GPIO_168 | AVS_HDA_SDI | PMU (Power Management Unit) 1.8V/3.3V mode select | 20K PD | 1=buffers set to 1.8V mode<br>0=buffers set to 3.3V mode (default) |
| GPIO_172 | AVS_M_CLK_B1 | SMBus No Re-Boot | 20K PD | 1 = Enable<br>0 = Disable (default)<br>***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC. |






ODD CHA CNVI

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Title: CPU(STRAP)

Size: Custom | Document Number: Raichu_GL | Rev: -1M

Date: Monday, October 01, 2018 | Sheet 15 of 106

**SSID = PCH**

## SPI ROM

24,25,91 SPI_MISO_ROM
24,25,91 SPI_MOSI_ROM
25 SPI_WP_ROM
25 SPI_HOLD_ROM
24,25 SPI_CS_CPU_N0
24,25,91 SPI_CLK_ROM

## EMMC

63 EMMC_RCLK
63 EMMC_CLK
63 EMMC_D0
63 EMMC_D1
63 EMMC_D2
63 EMMC_D3
63 EMMC_D4
63 EMMC_D5
63 EMMC_D6
63 EMMC_D7
63 EMMC_CMD
63 EMMC_RST#

## STRAP

15 GPIO163_SMB_1P8_3P3
15 GPIO172_SMB_REBOOT
15 GPIO174_VDD2_1P24_1P2
15 GPIO175_ESPI_LPC

24 LPC_CLK_KBC
68 LPC_CLK_DBG

24,68 INT_SERIRQ
24 LPC_CLKRUN#_CPU
24,68 LPC_FRAME#_CPU
24,68 LPC_AD_CPU_P0
24,68 LPC_AD_CPU_P1
24,68 LPC_AD_CPU_P2
24,68 LPC_AD_CPU_P3
27 HDA_BITCLK_CODEC
27 HDA_SYNC_CODEC
27 HDA_SDOUT_CODEC
27 HDA_RST#_CODEC
15,27 HDA_SDIN0_CPU

CPU1J — 10 OF 13 — GEMINI-LAKE-2-GP

AUDIO-AVS: AVS_I2S0_MCLK C26, AVS_I2S0_BCLK B25, AVS_I2S0_WS_SYNC C25, AVS_I2S0_SDI C24 GPIO_159 / Delay Vref switch, AVS_I2S0_SDO B23; AVS_I2S1_MCLK M23, AVS_I2S1_BCLK L21, AVS_I2S1_WS_SYNC J21 GPIO_163 / SMBus 1.8v / 3,3v mode, AVS_I2S1_SDI M21 GPIO_164 / Stall boot FSM for debug, AVS_I2S1_SDO P23; AVS_HDA_BCLK A22, AVS_HDA_WS_SYNC C23, AVS_HDA_SDI B21 GPIO_168 / PMU 1.8v 3.3v mode, AVS_HDA_SDO C22, AVS_HDA_RST# C21; AVS_DMIC_CLK_A1 B19, AVS_DMIC_CLK_B1 C20 GPIO_172 / SMbus no reboot, AVS_DMIC_DATA_1 C19, AVS_DMIC_CLK_AB2 C18 GPIO_174 / VDD2 1.24v, 1.2v mode, AVS_DMIC_DATA_2 A18 GPIO_175 / eSPI, LPC mode

eMMC: EMMC_CLK J13, EMMC_RCLK L15; EMMC_D0 M19, EMMC_D1 H19, EMMC_D2 J19, EMMC_D3 P17, EMMC_D4 P19, EMMC_D5 J15, EMMC_D6 L17, EMMC_D7 M17, EMMC_CMD M13; EMMC_RST# U44, EMMC_PWR_EN# G51, EMMC_RCOMP L13

SDCARD: SDCARD_CLK L29, SDCARD_D0 M29, SDCARD_D1 P29, SDCARD_D2 M27, SDCARD_D3 P27, SDCARD_CMD L27, SDCARD_CD# L25, SDCARD_LVL_WP P25, SDCARD_PWR_DWN# L23, SDCARD_RCOMP J25

LPC/eSPI: LPC_CLKOUT0 C37, LPC_CLKOUT1 A38, LPC_AD0 A34, LPC_AD1 C34, LPC_AD2 B35, LPC_AD3 C35, LPC_CLKRUN# C33, LPC_FRAME# B33, LPC_SERIRQ B37

FAST_SPI: FST_SPI_CLK B29, FST_SPI_MOSI_IO0 B31, FST_SPI_MISO_IO1 C30, FST_SPI_IO2 A30, FST_SPI_IO3 C29, FST_SPI_CS0# C31, FST_SPI_CS1# C32

1.8V / 3.3V
1.8V
1.8V / 3.3V
1.8V

GPIO163_SMB_1P8_3P3
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDIN0_CPU
HDA_SDOUT_CPU
HDA_RST_N_CPU
GPIO172_SMB_REBOOT
GPIO174_VDD2_1P24_1P2
GPIO175_ESPI_LPC
EMMC_CLK
EMMC_RCLK
EMMC_D0
EMMC_D1
EMMC_D2
EMMC_D3
EMMC_D4
EMMC_D5
EMMC_D6
EMMC_D7
EMMC_CMD

TP1601 Do Not Stuff
EC_EMMC_RST#
EMMC_PWR_EN#
EMMC_RCOMP

Layout Note: W/S=10/8, length <500 mil
R1605 200R2F-L-GP

LPC_CLK_KBC_R R1603 33R2J-2-GP LPC_CLK_KBC
LPC_CLK_DBG_R R1602 Do Not Stuff LPC_CLK_DBG
LAB

SPI_CLK_CPU R1604 Do Not Stuff SPI_CLK_ROM
SPI_SI_CPU R1611 Do Not Stuff SPI_MOSI_ROM
SPI_SO_CPU R1612 Do Not Stuff SPI_MISO_ROM
SPI_WP_CPU R1613 Do Not Stuff SPI_WP_ROM
SPI_HOLD_CPU R1614 Do Not Stuff SPI_HOLD_ROM
SPI_CS_CPU_N0

RN1601 SRN33J-7-GP-U
HDA_SYNC_CODEC — HDA_SYNC_CPU
HDA_SDOUT_CODEC — HDA_SDOUT_CPU
HDA_BITCLK_CODEC — HDA_BITCLK_CPU
HDA_RST#_CODEC — HDA_RST_N_CPU

3D3V_S0
R1625 10KR2J-L-GP
LPC_CLKRUN#_CPU

1D8V_S0 1D8V_S5
R1627 Do Not Stuff
R1628 Do Not Stuff
EMMC_RST#
R1629 DY Do Not Stuff
EC_EMMC_RST#

LPC_CLK_KBC
C1601 DY Do Not Stuff

3D3V_S0
R1630 Do Not Stuff DY
EMMC_PWR_EN#

ODD CHA CNVI



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Title: CPU (AVS/EMMC/SD/LPC/ESPI)
Size: A3 | Document Number: Raichu_GL | Rev: -1M
Date: Monday, October 01, 2018 | Sheet 16 of 106

SSID = PCH

15 GPIO83_LPC_1P8_3P3
15 GPIO84_SPI_BOOT_BIOS
15 GPIO061_TXE_BYPASS
15 GPIO65_DNXFW_RELOAD
15 GPIO66_LPC_BOOT_BIOS

65 CPU_I2C_SCL_P4
65 CPU_I2C_SDA_P4
91 SIO_SPI_0_FS1

68 LPSS_UART0_TXD
68 LPSS_UART0_RXD

61 CNV_WR_CLKP
61 CNV_WR_CLKN
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1
61 CNV_WT_CLKP
61 CNV_WT_CLKN
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1
61 CLKIN_XTAL_LCP
61,89 XTAL_CLKREQ
61 CNV_BRI_RSP
61 CNV_RGI_RSP
61 CNV_BRI_DT_R
61 CNV_RGI_DT_R
61 CNV_RF_RESET#

13 PCH_SMB_DATA
13 PCH_SMB_CLK

CPU1I — 9 OF 13

Touch Pad
CPU_I2C_SCL_P4 R49
CPU_I2C_SDA_P4 R51
SIO_I2C0_SCL U49 / U51
SIO_I2C0_SDA
SIO_I2C1_SCL U46 / U48
SIO_I2C1_SDA
SIO_I2C2_SCL AA39 / AA41 — 1.8V
SIO_I2C2_SDA
SIO_I2C3_SCL R44 / R43
SIO_I2C3_SDA
SIO_I2C4_SCL
SIO_I2C4_SDA
SIO_I2C5_SCL C50 / A50
SIO_I2C5_SDA
SIO_I2C6_SCL C48 / C47 — 3.3V
SIO_I2C6_SDA
SIO_I2C7_SCL B47 / C46
SIO_I2C7_SDA
SMB_ALERT#_CPU A26
CPU_SMB_SCL B27
CPU_SMB_SDA C27
SMB_ALERT#
SMB_CLK
SMB_DATA — 3.3V / 1.8V
GPIO_177 / WC_PRESENT
LPSS SMBus
3D3V_S5 — R1701 1KR2J-1-GP

CNVi RX for wifi
CNV_WR_CLKP H29 / CNV_WR_CLKN H31 — CNV_WGR_CLK_P / CNV_WGR_CLK#
CNV_WR_DP0 M31 / CNV_WR_DN0 P31 — CNV_WGR_D0_P / CNV_WGR_D0#
CNV_WR_DP1 D29 / CNV_WR_DN1 F29 — CNV_WGR_D1_P / CNV_WGR_D1#

CNVi TX for wifi
CNV_WT_CLKP F35 / CNV_WT_CLKN D35 — CNV_WT_CLK_P / CNV_WT_CLK#
CNV_WT_DP0 J35 / CNV_WT_DN0 H35 — CNV_WT_D0_P / CNV_WT_D0#
CNV_WT_DP1 L31 / CNV_WT_DN1 J31 — CNV_WT_D1_P / CNV_WT_D1#

CNVi Companion RF M.2 module

CLKIN_XTAL_LCP_R J29 / XTAL_CLKREQ F19 — CLKIN_XTAL_LCP / XTAL_CLKREQ
GPIO_196 / Spare 9
GPIO_191 / eSPI Flash Sharing Mode
CNV_BRI_DT H17 / CNV_BRI_RSP J17 — CNV_BRI_DT / CNV_BRI_RSP
GPIO_192 / Spare 5
GPIO_193 / XTAL startup
CNV_RGI_DT D19 / CNV_RGI_RSP D17 — CNV_RGI_DT / CNV_RGI_RSP
GPIO_194 / Spare 7
GPIO_195 / Spare 8
CNV_RF_RESET# F17 — CNV_RF_RESET#
CNV_WT_RCOMP F33 — CNV_WT_RCOMP

PCM bus from module
CNV_BRI_DT_R — R1710 — Do Not Stuff
CNV_RGI_DT_R — R1708 — Do Not Stuff
CNVi R17041 150R2F-1-GP 2 CNV_WT_RCOMP

GEMINI-LAKE-2-GP

LPSS_SPI
GPIO_79 / spare 6
GPIO_83 / LPC 1.8v 3.3v mode
GPIO_80 / EXI Boot
GPIO_81 / Halts early boot for debug
GPIO_84 / SPI boot BIOS
GPIO_89 / Stall boot FSM for debug
GPIO_85 / Enable metal password
GPIO_86 / SVID Enable
GPIO_87 / XTAL
SIO_SPI_0_CLK M39
SIO_SPI_0_TXD J37 — GPIO83_LPC_1P8_3P3
SIO_SPI_0_RXD L39
SIO_SPI_0_FS0 L37
SIO_SPI_0_FS1 J39 — SIO_SPI_0_FS1
SIO_SPI_2_CLK M37 — GPIO84_SPI_BOOT_BIOS
SIO_SPI_2_TXD M33
SIO_SPI_2_RXD P35
SIO_SPI_2_FS0 P33
SIO_SPI_2_FS1 P37
SIO_SPI_2_FS2 L35

LPSS_UART
GPIO_61 / CSE ROM
GPIO_62 / RTC clock time bypass
GPIO_65 / DNX FW
GPIO_66 / LPC boot BIOS
SIO_UART0_TXD N54 — GPIO61_TXE_BYPASS — R1702 1 LAB 2 Do Not Stuff
SIO_UART0_RXD P53 — LPSS_UART0_RXD_R — R1703 1 LAB 2 Do Not Stuff
SIO_UART0_RTS# N53
SIO_UART0_CTS# M55
SIO_UART2_TXD L54 — GPIO65_DNXFW_RELOAD
SIO_UART2_RXD M53 — GPIO66_LPC_BOOT_BIOS
SIO_UART2_RTS# K53
SIO_UART2_CTS# L53
LPSS_UART0_RXD
LPSS_UART0_TXD

Close to J29
CLKIN_XTAL_LCP_R — EL1701 HCB1005KF-121T20-GP — CLKIN_XTAL_LCP
68.00358.031
2nd = 068.00006.0041
C1701 SC4D7P8V2BN-GP
R1705 10KR2J-L-GP
-1: For ESD(20180810)

CNV_RF_RESET# — R1706 75KR2F-GP — R1707 Do Not Stuff — CNV_BRI_RSP
1D8V_S5 — R1709 Do Not Stuff — CNV_RGI_RSP

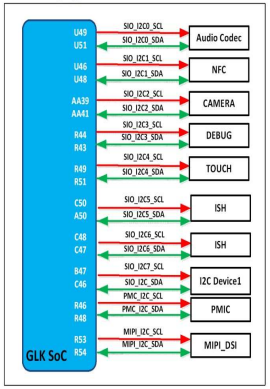
3D3V_S5 — RN1701 SRN1KJ-7-GP
3D3V_S0 — RN1709 SRN10KJ-5-GP
Q1701 SSM6N7002KFU-GP
CPU_SMB_SDA — PCH_SMB_DATA
CPU_SMB_SCL — PCH_SMB_CLK
075.67002.007C
2ND = 075.27002.0E7C
3rd = 75.27002.F7C

Table 23-1. I²C Signal Interface Description

| Signal Name | Direction | Maximum Frequency/ Data Rate | Description |
|---|---|---|---|
| SIO_I2C0_SDA SIO_I2C0_SCL | Input/Output Output | 3.14MHz | I²C clock and data for Audio Codec |
| SIO_I2C1_SDA SIO_I2C1_SCL | Input/Output Output | 3.14MHz | I²C clock and data for NFC or any other I²C interfaces |
| SIO_I2C2_SDA SIO_I2C2_SCL | Input/Output Output | 3.14MHz | I²C clock and data for CAMERA or any other I²C interfaces |
| SIO_I2C3_SDA SIO_I2C3_SCL | Input/Output Output | 3.14MHz | I²C clock and data for DEBUG or any other I²C interfaces |
| SIO_I2C4_SDA SIO_I2C4_SCL | Input/Output Output | 3.14MHz | I²C clock and data for Touch panel or any other I²C interfaces |
| SIO_I2C5_SDA SIO_I2C5_SCL | Input/Output Output | 3.14MHz (Note 3) | I²C clock and data for ISH or any other I²C interfaces |
| SIO_I2C6_SDA SIO_I2C6_SCL | Input/Output Output | 3.14MHz (Note 3) | I²C clock and data for ISH or any other I²C interfaces |
| SIO_I2C7_SDA SIO_I2C7_SCL | Input/Output Output | 3.14MHz (Note 3) | I²C clock and data for any other I²C interfaces |
| PMC_I2C_SDA PMC_I2C_SCL | Input/Output Output | 3.14MHz | I²C clock and data for PMIC or any other I²C interfaces |
| MIPI_I2C_SDA MIPI_I2C_SCL | Input/Output Output | 3.14MHz | I²C clock and data for DSI or any other I²C interfaces |

**Notes:**
1. The I²C port assignment refers to the CRB implementation. It is an example of how the I²C ports can be configured.
2. For LPSS I²C ports muxed with ISH I²C ports, refer Gemini Lake SoC – External Design Specification (EDS) and choose the appropriate port function.
3. At 3.3V Mode Port 5,6 and 7 support up to 1MHz Data rate only. Data rate 1.7MHz and 3.14MHz not supported at 3.3V Mode.

Figure 23-1. I²C Interface Topology




To configure the I²C ports, follow the pin muxing options listed out in the Gemini Lake SoC – External Design Specification (EDS).

ODD CHA CNVI



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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (I2C/SMB/SPI/UART/CNVI)
Size: Custom | Document Number: Raichu_GL | Rev: -1M
Date: Monday, October 01, 2018 | Sheet 17 of 106

SSID = CPU

**USB3.0 Type A**

35 USB1_USB30_TX_P
35 USB1_USB30_TX_N
35 USB1_USB30_RX_P
35 USB1_USB30_RX_N

35 USB2_USB30_TX_P
35 USB2_USB30_TX_N
35 USB2_USB30_RX_P
35 USB2_USB30_RX_N

35 USB3_USB30_TX_P
35 USB3_USB30_TX_N
35 USB3_USB30_RX_P
35 USB3_USB30_RX_N

**USB3.0 to SATA ODD**

60 ODD_USB30_TX_P
60 ODD_USB30_TX_N
60 ODD_USB30_RX_P
60 ODD_USB30_RX_N

**WLAN**

61 WLAN_PCIE_TX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_RX_N
61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N
61,89 PCIE_WAKE#_CPU

**M.2 PCIe SSD**

63,89 SSD_CLK_CPU_P
63,89 SSD_CLK_CPU_N
63 SSD_CLKREQ_CPU_N
63 SSD_PCIE_TX_P0
63 SSD_PCIE_TX_N0
63 SSD_PCIE_RX_P0
63 SSD_PCIE_RX_N0
63 SSD_PCIE_TX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_RX_N1

**LAN**

31 LAN_PCIE_TX_P
31 LAN_PCIE_TX_N
31 LAN_PCIE_RX_P
31 LAN_PCIE_RX_N
31 LAN_CLK_CPU_P
31 LAN_CLK_CPU_N
31 LAN_CLKREQ_CPU_N
31 PCIE_WAKE2_CPU

**M.2 SATA SSD**

63 SSD_SATA_TX_P
63 SSD_SATA_TX_N
63 SSD_SATA_RX_P
63 SSD_SATA_RX_N

**SATA HDD**

60 HDD_SATA_TX_P
60 HDD_SATA_TX_N
60 HDD_SATA_RX_P
60 HDD_SATA_RX_N

**ODD**

60 ODD_USB20_P
60 ODD_USB20_N

**FP**

92 FP_USB20_P
92 FP_USB20_N

**USB3.0 Port1**

35 USB1_USB20_P
35 USB1_USB20_N

**USB3.0 Port2**

35 USB2_USB20_P
35 USB2_USB20_N

**USB3.0 Port3**

35 USB3_USB20_P
35 USB3_USB20_N

**CCD**

55 CCD_USB20_P
55 CCD_USB20_N

**CARD READER**

33 CR_USB20_P
33 CR_USB20_N

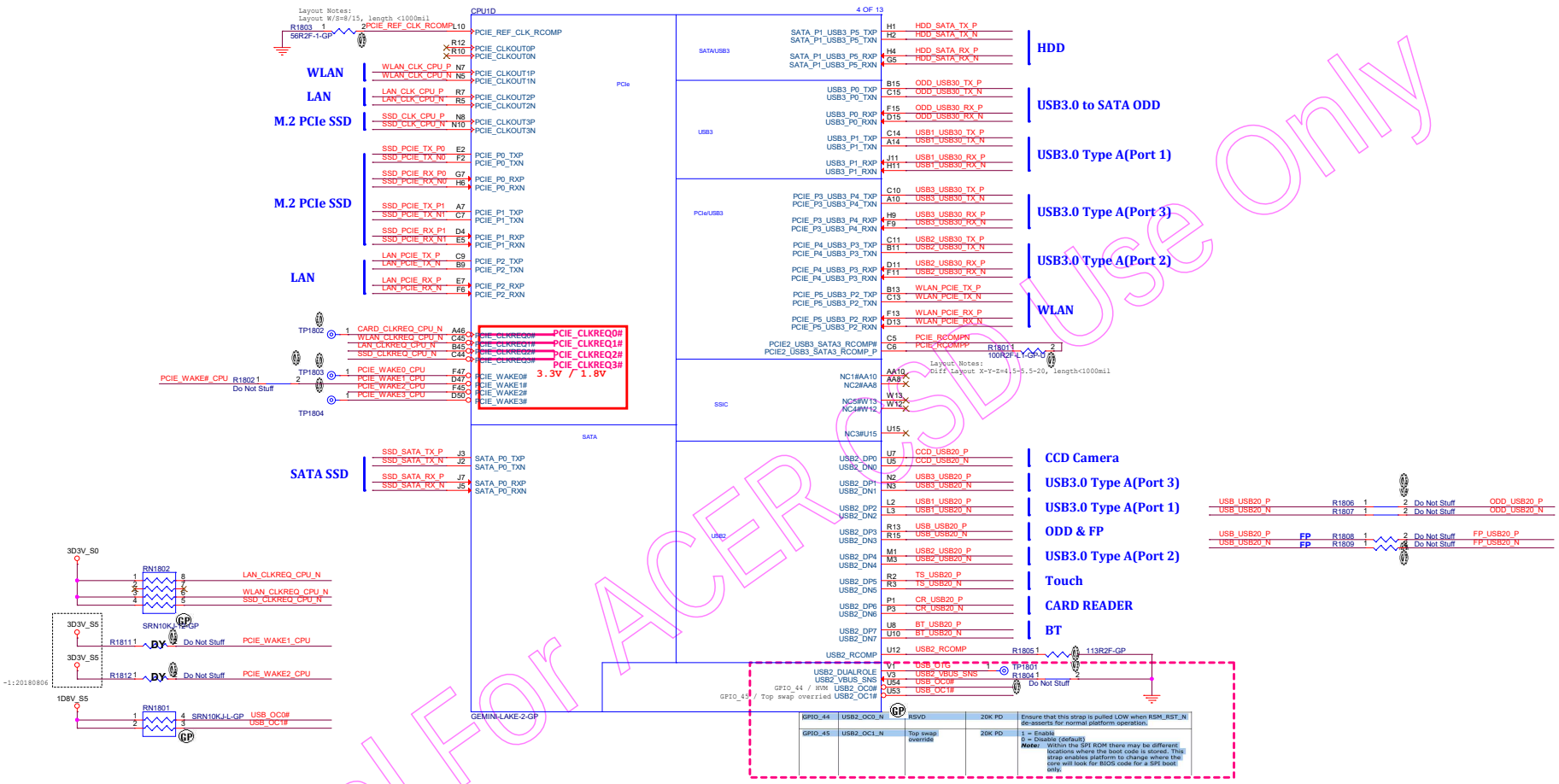
**TS**

55 TS_USB20_P
55 TS_USB20_N

**BT**

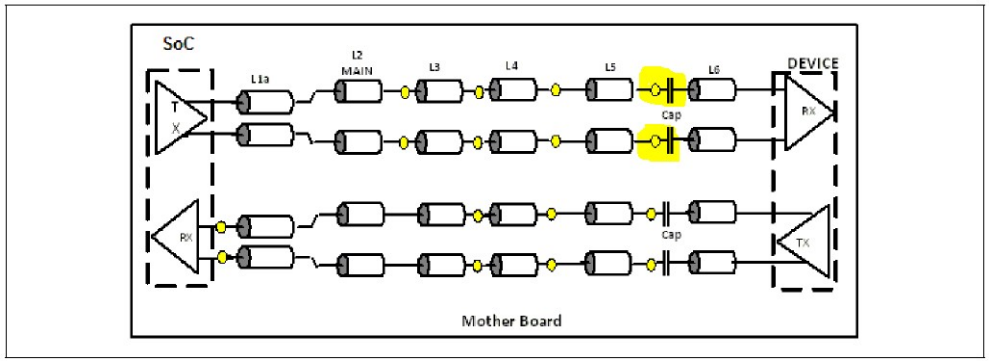
61 BT_USB20_P
61 BT_USB20_N

15 USB_OC1#




| | | | |
|---|---|---|---|
| PCIE_WAKE[3:0]_N | I | V1P8/V3P3 | PCIe* Wake Signals |
| PCIE_CLKREQ[3:0]_N | I/O | V1P8/V3P3 | **PCIE Clock Request**: Used for devices that need to request one of the four output clocks. Each clock request maps to the matching clock output (for example, PCI_CLKREQ[0] maps to PCIE_CLKP/N[0]). These signals are multiplexed and may be used by other functions. |

Figure 9-8. PCI Express* Device Down Topology





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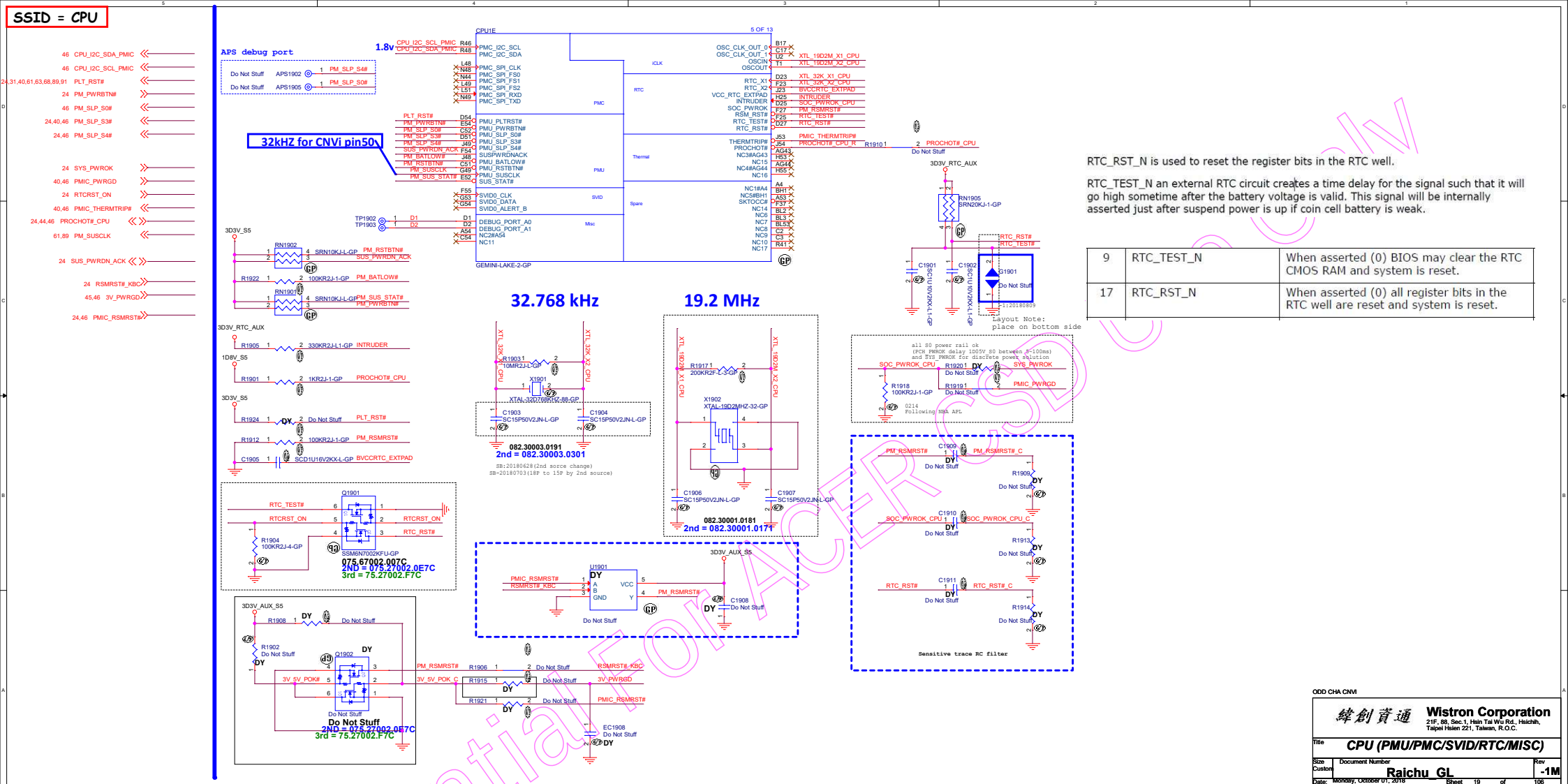
Title: CPU (PCIE/SATA/USB3/USB2)

Size: A2 | Document Number: Raichu_GL | Rev: -1M

Date: Monday, October 01, 2018 | Sheet 18 of 106

**SSID = CPU**




RTC_RST_N is used to reset the register bits in the RTC well.

RTC_TEST_N an external RTC circuit creates a time delay for the signal such that it will go high sometime after the battery voltage is valid. This signal will be internally asserted just after suspend power is up if coin cell battery is weak.

| | | |
|---|---|---|
| 9 | RTC_TEST_N | When asserted (0) BIOS may clear the RTC CMOS RAM and system is reset. |
| 17 | RTC_RST_N | When asserted (0) all register bits in the RTC well are reset and system is reset. |



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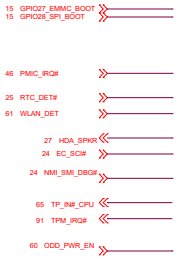
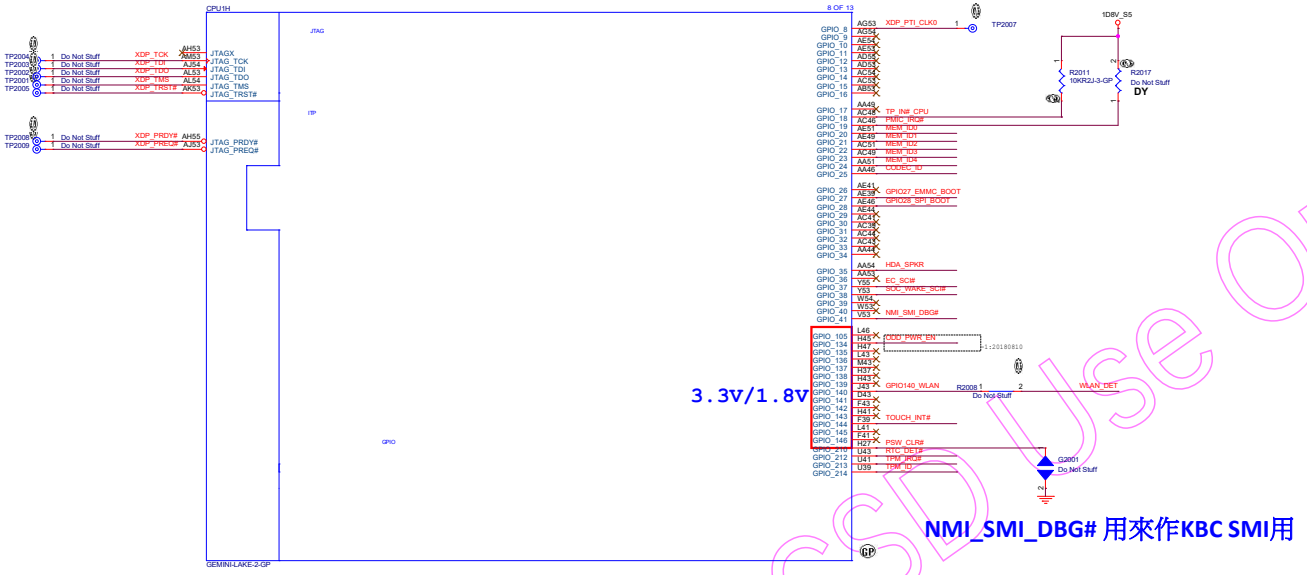
Title: CPU (PMU/PMC/SVID/RTC/MISC)

Size: Custom | Document Number: Raichu_GL | Rev: -1M

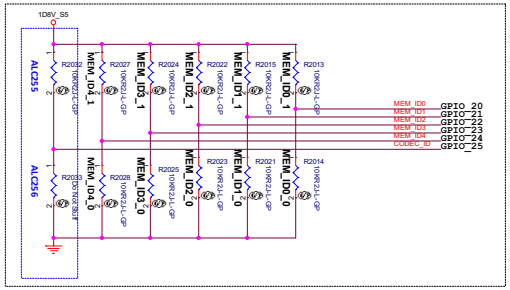
Date: Monday, October 01, 2018 | Sheet 19 of 106

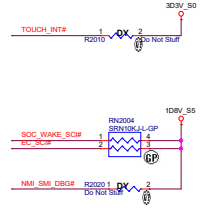
SSID = PCH



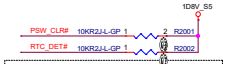



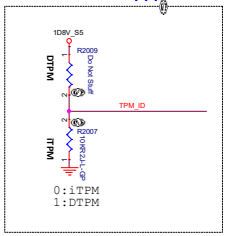

NMI_SMI_DBG# 用來作KBC SMI用








0=L,1=H

| | | Truth Table | | | | CHA | | | |
|---|---|---|---|---|---|---|---|---|---|
| RAMID | MD_ID4 | MD_ID3 | MD_ID2 | MD_ID1 | MD_ID0 | WISTRON PN | Vendor PN | Vendor | Density |
| 0 | 0 | 0 | 0 | 0 | 0 | KN.00404.010 | MT40A256M16GE-083E:B | MICRON | 2GB |
| 1 | 0 | 0 | 0 | 0 | 1 | KN.0040G.026 | H5AN4G6NBJR-UHC | HYNIX | 2GB |
| 2 | 0 | 0 | 0 | 1 | 0 | KN.8GB04.027 | MT40A512M16LY-075:E LF+HF | MICROM | 4GB |
| 3 | 0 | 0 | 0 | 1 | 1 | KN.8GB0G.049 | H5AN8G6NAFR-UHC | HYNIX | 4GB |
| 4 | 0 | 0 | 1 | 0 | 0 | KN.8GB0G.061 | H5AN8G6NCJR-VKC | HYNIX | 4GB |
| 5 | 0 | 0 | 1 | 0 | 1 | NA | DUMMY | NA | NA |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

## 13.2 SATA Signal Description

### 13.2.1 SATA Signal Groups

Table 13-3. SATA Signal Groups

| Group | Signal Name | Direction/ Reference | Description |
|---|---|---|---|
| GPIO | **SATA_GP0** (GPIO_138) | I/O V1P8A | Serial ATA Port [0] General Purpose. |
| | **SATA_GP1** (GPIO_139) | I/O V1P8A | Serial ATA Port [1] General Purpose. |
| | **SATA_DEVSLP0** (GPIO_140) | O V1P8A | Serial ATA Port [0] Device Sleep. |
| | **SATA_DEVSLP1** (GPIO_141) | O V1P8A | Serial ATA Port [1] Device Sleep. |
| | **SATA_LED_NSATA_LED_N** (GPIO_142) | O V1P8A | LED |
| SATA Transmit | **SATA_P0_TXN**<br>**SATA_P0_TXP**<br>**SATA_P1_USB3_P5_TXN**<br>**SATA_P1_USB3_P5_TXP** | O V1P24A | Differential Transmit Pair. |
| SATA Receive | **SATA_P0_RXN**<br>**SATA_P0_RXP**<br>**SATA_P1_USB3_P5_RXN**<br>**SATA_P1_USB3_P5_RXP** | I V1P24A | Differential Receive Pair. |

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| | | |
|---|---|---|
| Title | CPU (GPIO/JTAG/ITP) | |
| Size: Custom | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 20 of 106 | |

SSID = CPU

# Blanking



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| | | |
|---|---|---|
| Title | CPU (Reserved) | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 21 of 106 | |

SSID = CPU

# Blanking





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Title: CPU (Reserved)

Size: A4 | Document Number: Raichu_GL | Rev: -1M

Date: Monday, October 01, 2018 | Sheet 22 of 106

SSID = CPU

# Blanking





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| | | |
|---|---|---|
| Title | (RESERVED) | |
| Size A4 | Document Number Raichu_GL | Rev -1M |
| Date: Monday, October 01, 2018 | Sheet 23 of 106 | |

**SSID = KBC**

**Power**

- +3D3V_AUX_S5
- +3D3V_S0
- +3D3V_RTC_AUX

**Signal**

- INT_SERIRQ 16,68
- TP_FUN_OFF# 65,89
- LPC_FRAME#_CPU 16,68
- LPC_AD_CPU_P3 16,68
- LPC_AD_CPU_P2 16,68
- LPC_AD_CPU_P1 16,68
- LPC_AD_CPU_P0 16,68
- LPC_CLK_KBC 16
- PLT_RST# 19,31,40,61,63,68,89,91
- TOUCH_EN 24,55,89
- LID_CLOSE# 67,89
- PTP_PWR_EN 65
- PURE_HW_SHUTDOWN# 26,40
- LPC_CLKRUN#_CPU 16
- ES1_TXD 61,68
- EC_TP_IN# 24,65
- KBC_BEEP 27
- KSI0 65,89
- KSI1 65,89
- KSI2 65,89
- KSI3 65,89
- KSI4 65,89
- KSI5 65,89
- KSI6 65,89
- KSI7 65,89
- KSO0 65,89
- KSO1 65,89
- KSO2 65,89
- KSO3 65,89
- KSO4 65,89
- KSO5 65,89
- KSO6 65,89
- KSO7 65,89
- KSO8 65,89
- KSO9 65,89
- KSO10 65,89
- KSO11 65,89
- KSO12 65,89
- KSO13 65,89
- KSO14 65,89
- KSO15 65,89
- KSO16 65,89
- KSO17 65,89
- AC_IN# 44
- KBC_PWRBTN# 65,89
- BAT_IN# 43,44
- AD_IA 44
- BT_IA 44
- ALL_SYS_PWRGD 40
- STDBY_LED 64,89
- DC_Protect_EC 44
- 5V_EN 45
- PMIC_RSMRST# 19,46
- BAT_SCL 43,44
- BAT_SDA 43,44
- SPI_WP_ROM 16,25
- TOUCH_EN 24,55,89
- EC_TP_CLK 65
- EC_TP_DATA 65
- ME_UNLOCK 8
- EC_TP_IN# 24,65
- PCRST_ON 19
- BLON_OUT 55
- VD_IN1 26
- VD_OUT1 26
- PROCHOT#_CPU 19,44,46
- CHARGE_LED 64,89
- DC_BATFULL 64,89
- RSMRST#_KBC 19
- AMP_MUTE# 27
- SS_ENABLE 40
- SYS_PWROK 19
- POWER_LED 64,89
- SPI_MISO_ROM 16,25,91
- SPI_MOSI_ROM 16,25,91
- SPI_CLK_ROM 16,25,91
- SPI_CS_CPU_N0 16,25
- WIFI_RF_EN 61,89
- BLUETOOTH_EN 61,89
- USB_PWR_EN 35
- CHG_ON# 44
- MM_SMI_DBG# 20
- WLAN_PERST# 61
- SUS_PWRDN_ACK 19,24
- Jmicron_RST# 60

**SOC need 1.8V**

- eDP_BLEN_CPU 8
- PM_PWRBTN# 19

**SOC need level shift**

- EC_SCI# 20

**3.3V**

- PM_SLP_S3# 19,40,46
- PM_SLP_S4# 19,46

- SUS_PWRDN_ACK 19,24

Close to the EC Intel suggest 100K PD

PLT_RST# — R2460 47KR2J-L2-GP

For EC power consumption reserver

3D3V_AUX_KBC — R2406 — 3D3V_AUX_S5 (Do Not Stuff)

VCC_LPC(Pin9)

3D3V_AUX_KBC — R2435 Do Not Stuff — VCC_LPC

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

U2401 KB9028Q-C-GP

BATTER /CHARGER --->

Touch Pad

SYS_PWROK(SO_PWR_GOOD) ==DELAY 99ms

GPIO0 High Active

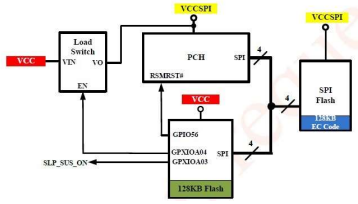
Do Not Stuff
2nd = 83.R2003.A8M

84.T3906.I11
2nd = 84.T3906.E11
3rd = 84.03906.R11

071.09028.000G

### 3.3 Power-up Scenarios and Timing Sequence

1. For the first time KB9028C boots up when its embedded flash is empty, it will automatically drive ***GPXIOA04*** and ***GPXIOA03*** to "High" and ***GPIO56*** to "Low" within 30ms after the ***ECRST#*** is de-asserted. This behavior is particularly designed to switch on certam power wells (including the **VCC_SPI** which located in the deep sleep power well and the suspend power well) and to drive the ***RSMRST#*** to low. The PCH's SPI interface will only be tri-stated when these conditions are established.
2. The **VCC_SPI** voltage must be valid within <30ms when it is being switched on by the ***GPXIOA04*** signal. This timing requirement is crucial because the KB9028C will start to fetch code from the external SPI flash device after 30ms (min).
3. Once the code-moving from the external SPI flash to the KB9028C's embedded flash is accomplished, the KB9028C will conduct self-reset of the 8051 and thus it starts booting from the embedded flash ever since. There will be no more SPI Flash Load-Code Scenario happen ever again. Refer to the Embedded Flash Boot Scenario depicted in the following diagram




| PCB_VER_AD | Pull-Low Register | Pull-High Register | Typical Voltage | Max Voltage | KBC Firmware Setting | |
|---|---|---|---|---|---|---|
| SA | 100.0 K | 10.0 K | 3.000 V | 3.005 V | >= 2.875 V | |
| SB | 100.0 K | 20.0 K | 2.750 V | 2.759 V | >= 2.616 V | < 2.875 V |
| SC | 100.0 K | 33.0 K | 2.481 V | 2.493 V | >= 2.363 V | < 2.616 V |
| -1 | 100.0 K | 47.0 K | 2.245 V | 2.259 V | >= 2.123 V | < 2.363 V |
| -1M | 100.0 K | 64.9 K | 2.001 V | 2.017 V | >= 1.934 V | < 2.123 V |
| -2 | 100.0 K | 76.8 K | 1.867 V | 1.883 V | >= 1.758 V | < 1.934 V |
| Reserved for project use | 100.0 K | 100.0 K | 1.650 V | 1.667 V | >= 1.504 V | < 1.758 V |
| Reserved for project use | 100.0 K | 143.0 K | 1.358 V | 1.374 V | >= 1.281 V | < 1.504 V |
| Reserved for project use | 100.0 K | 174.0 K | 1.204 V | 1.220 V | >= 1.126 V | < 1.281 V |
| Reserved for project use | 100.0 K | 215.0 K | 1.048 V | 1.062 V | >= 0.524 V | < 1.126 V |

| Model_ID | Pull-Low Register | Pull-High Register | Typical Voltage | Max Voltage | KBC Firmware Setting | |
|---|---|---|---|---|---|---|
| 45W | N/A | 100.0 K | 3.300 V | | >= 3.200 V | |
| 90W | 100.0 K | N/A | 0.000 V | | | < 3.193 V |
| 33W | 19.6 K | 100.0 K | 0.382 V | >= 0.150 V | < 0.425 V | |
| 45W | 28.0 K | 100.0 K | 0.550 V | >= 0.425 V | < 0.664 V | |
| 120W | 33.0 K | 100.0 K | 0.619 V | >= 0.564 V | < 0.837 V | |
| 135W | 47.0 K | 100.0 K | 1.065 V | 1.070 V | >= 0.837 V | < 1.077 V |
| 150W | 64.9 K | 100.0 K | 1.298 V | 1.310 V | >= 1.077 V | < 1.388 V |
| Reserved | 76.8 K | 100.0 K | 1.433 V | 1.450 V | >= 1.388 V | < 1.542 V |
| Reserved | 100.0 K | 100.0 K | 1.650 V | 1.667 V | >= 1.542 V | < 1.742 V |



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Title: ECIO(KBC KB9028)

Size: Document Number: Rev: -1M

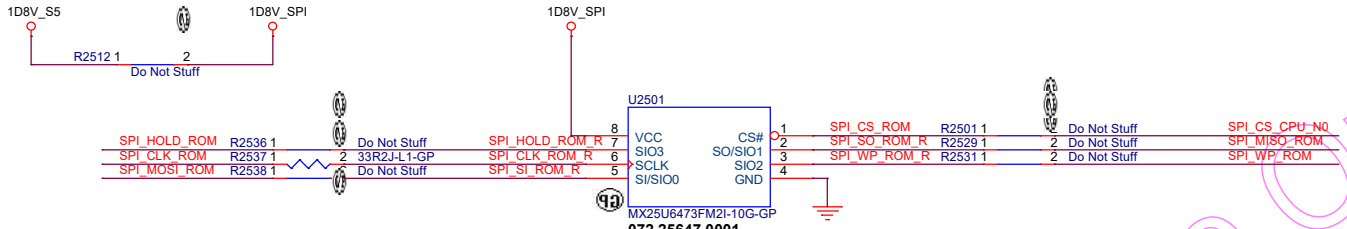
Custom: Raichu_GL

Date: Monday, October 01, 2018 Sheet 24 of 100

SSID = Flash.ROM

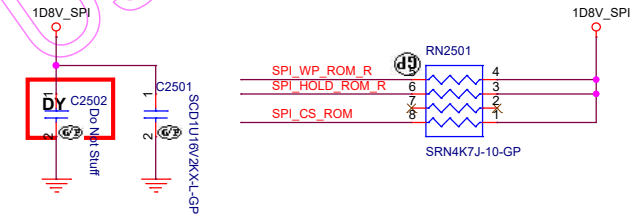
# SPI FLASH ROM (8M byte) for PCH

16 SPI_HOLD_ROM
16,24,91 SPI_CLK_ROM
16,24,91 SPI_MOSI_ROM
16,24 SPI_CS_CPU_N0
16,24,91 SPI_MISO_ROM
16 SPI_WP_ROM



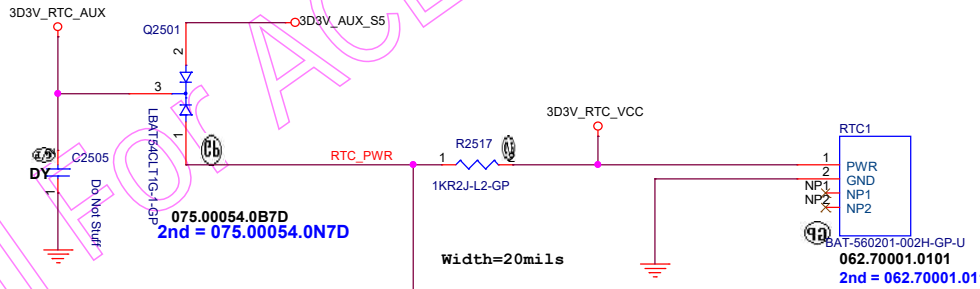

072.25647.0001
2nd = 072.02564.0A01

072.25647.0001_MX25U6473FM2I-10G-GP
072.02564.0A01_GD25LB64CSIGR

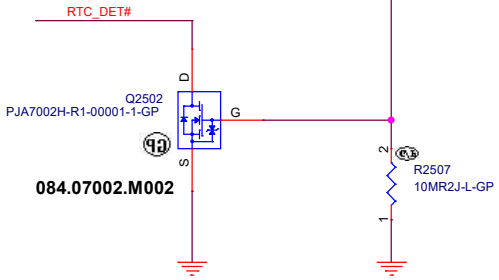



Vinafix

SSID = RBAT




20 RTC_DET#




RTC Battery:
Main:23.20068.001
2nd:023.20004.0011

ODD CHA CNVI

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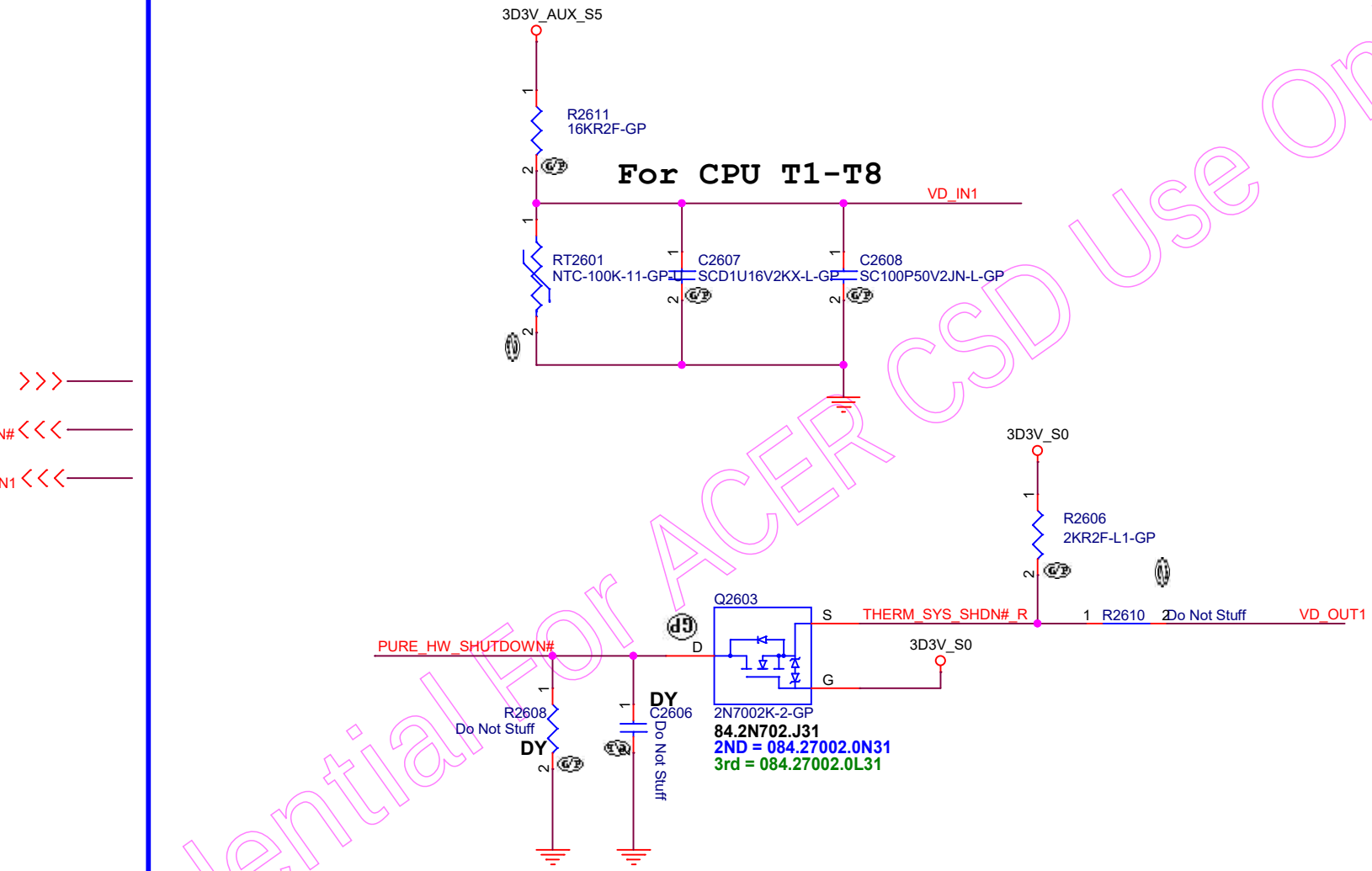
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | Flash/RTC | |
| Size: Custom | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 25 of 106 | |

# Main Func = Thermal Sensor




24 VD_OUT1

24,40 PURE_HW_SHUTDOWN#

24 VD_IN1



ODD CHA CNVI

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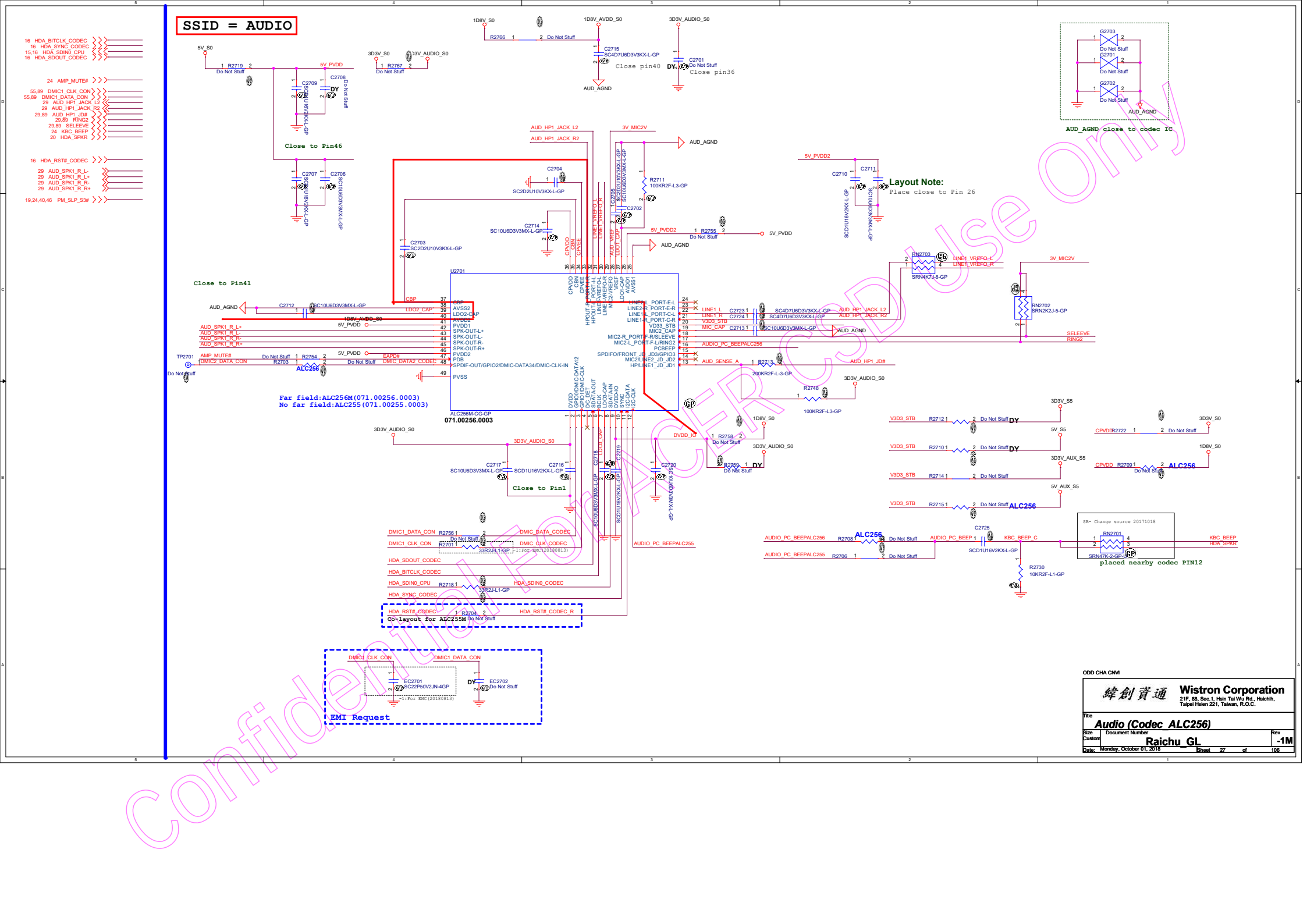
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | INT IO(THERMAL) | |
| Size A4 | Document Number Raichu_GL | Rev -1M |
| Date: Monday, October 01, 2018 | Sheet 26 of 106 | |

# SSID = AUDIO



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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (Codec ALC256)

Size: Custom | Document Number: Raichu_GL | Rev: -1M

Date: Monday, October 01, 2018 | Sheet 27 of 106

# Blanking



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緯創資通 Wistron Corporation
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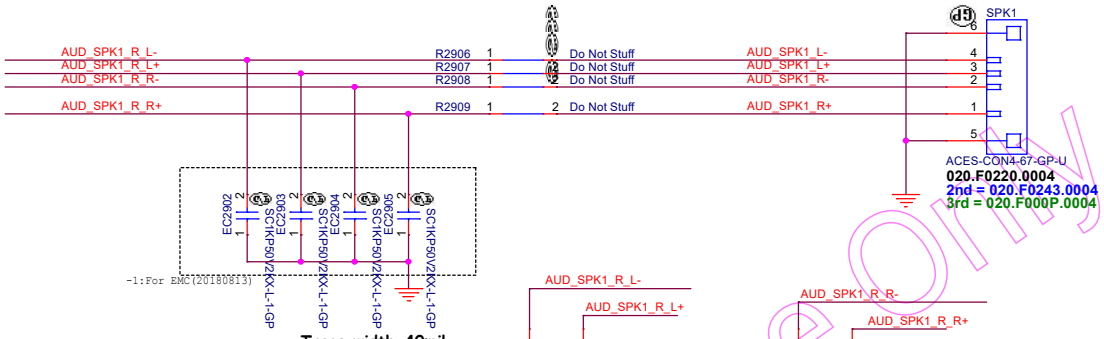
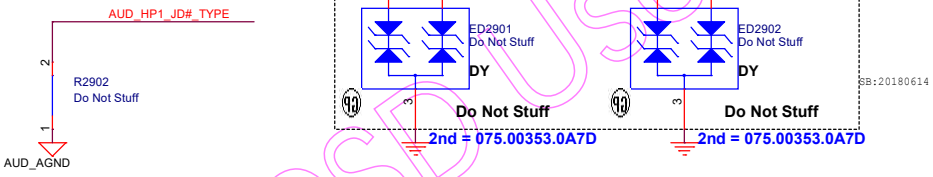
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *(Reserved) Audio AMP* | |
| Size: A4 | Document Number: *Raichu_GL* | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 28 of 106 | |

**SSID = AUDIO** *Speaker*



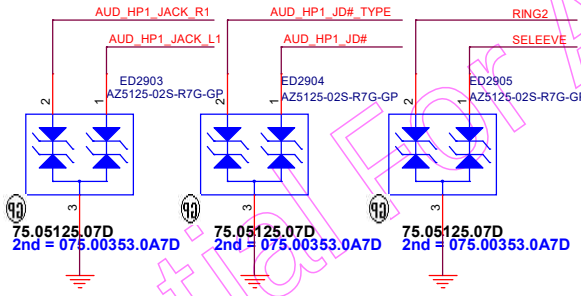

27 AUD_SPK1_R_L-
27 AUD_SPK1_R_L+
27 AUD_SPK1_R_R-
27 AUD_SPK1_R_R+

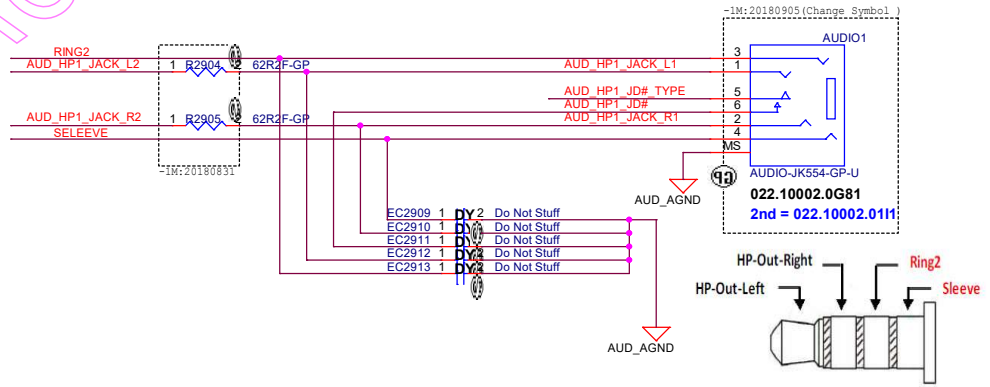
27 AUD_HP1_JACK_L2
27 AUD_HP1_JACK_R2
27,89 AUD_HP1_JD#
27,29,89 RING2
27,29,89 SELEEVE

29,89 AUD_HP1_JACK_L1
27,29,89 RING2
27,29,89 SELEEVE

89 AUD_SPK1_L-
89 AUD_SPK1_L+
89 AUD_SPK1_R-
89 AUD_SPK1_R+

29,89 AUD_HP1_JACK_L1
89 AUD_HP1_JACK_R1
89 AUD_HP1_JD#_TYPE



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| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***Audio (HP/SPK/MIC Jack)*** | |
| Size A3 | Document Number **Raichu_GL** | Rev **-1M** |
| Date: Monday, October 01, 2018 | Sheet 29 of 106 | |

SSID = LOM

# Blanking



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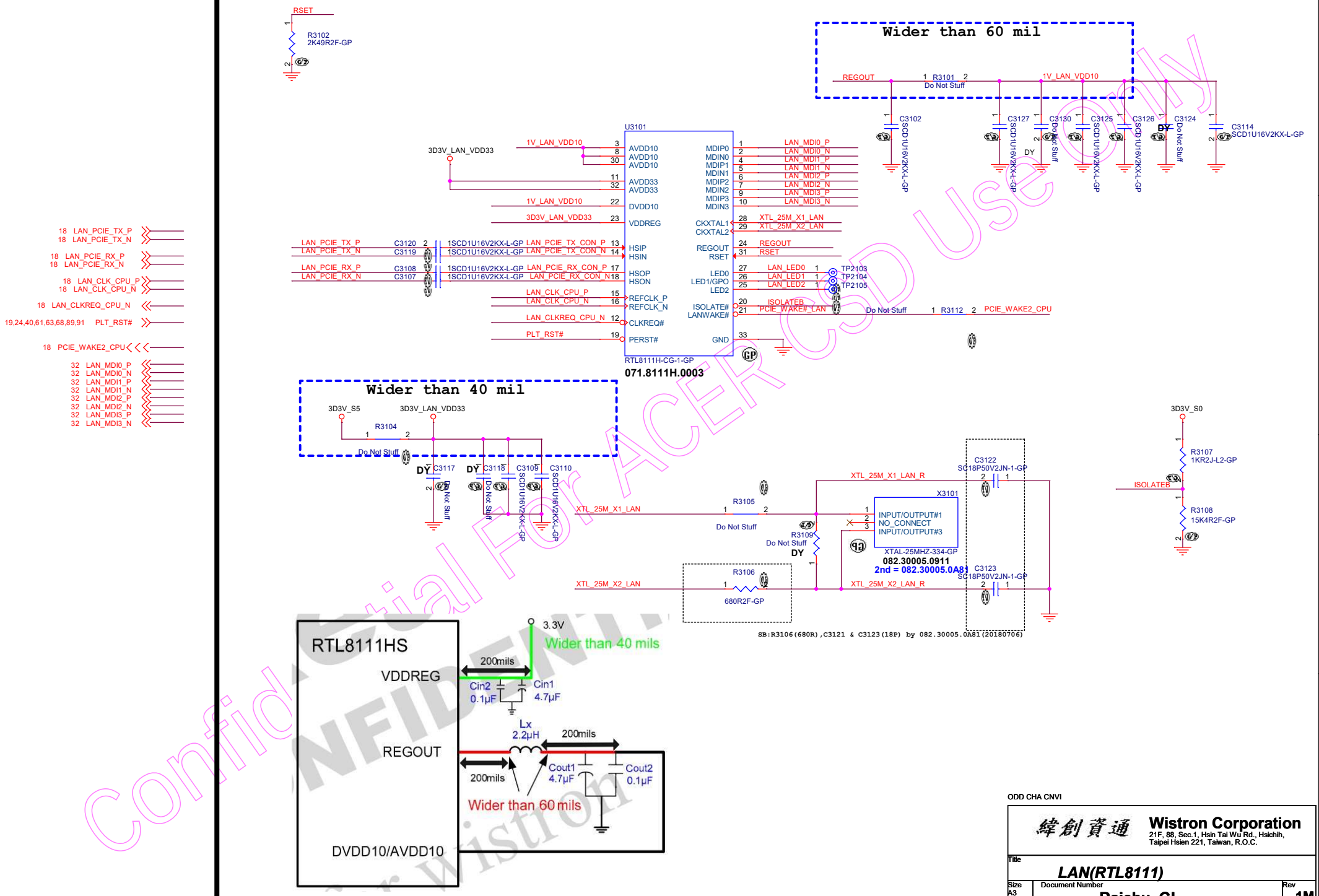
| | | |
|---|---|---|
| Title | (Reserved) | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 30 of 106 | |



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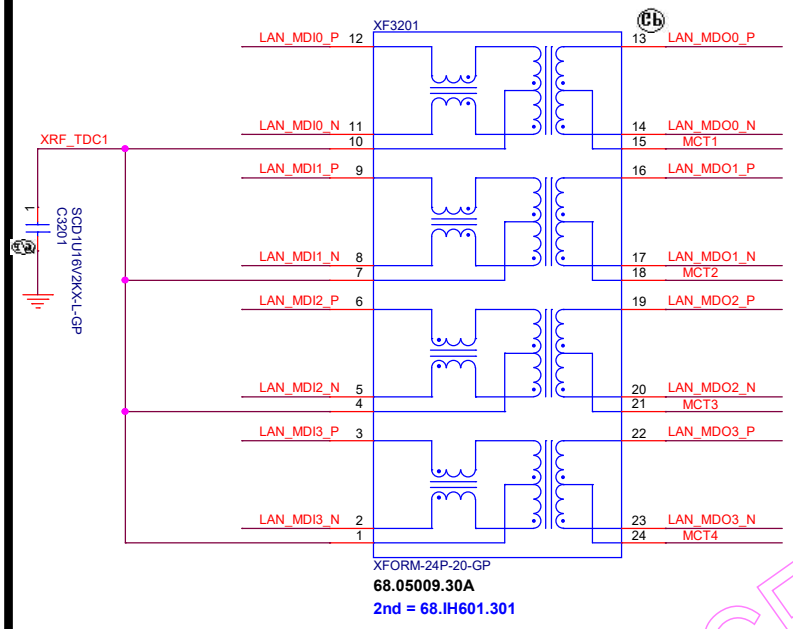
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN(RTL8111)***

| Size | Document Number | Rev |
|---|---|---|
| A3 | Raichu_GL | -1M |

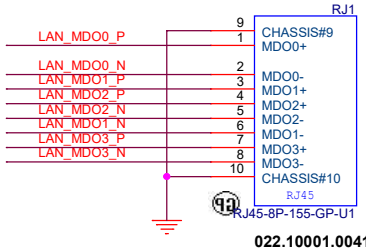
Date: Monday, October 01, 2018 Sheet 31 of 106

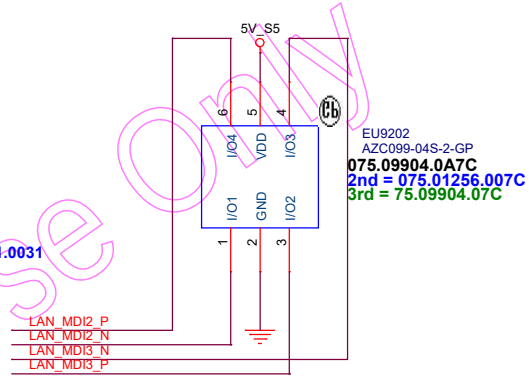
**SSID = LAN**

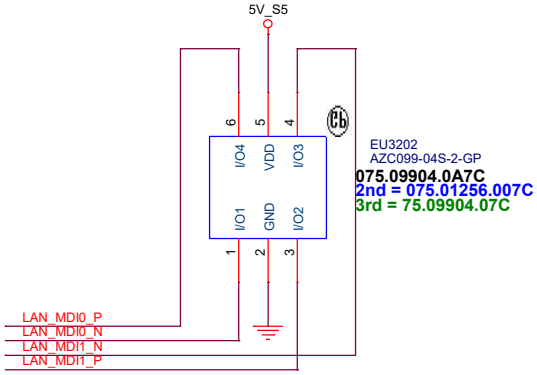


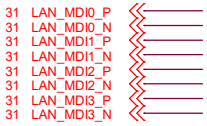




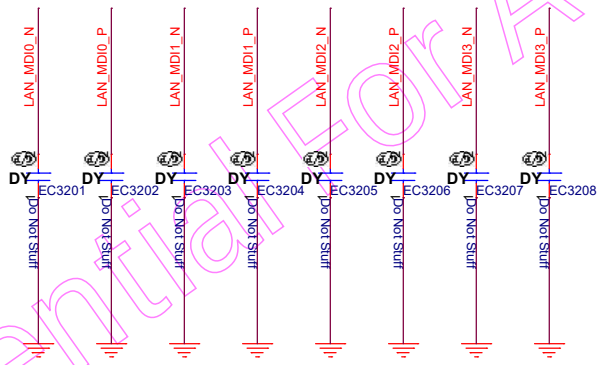


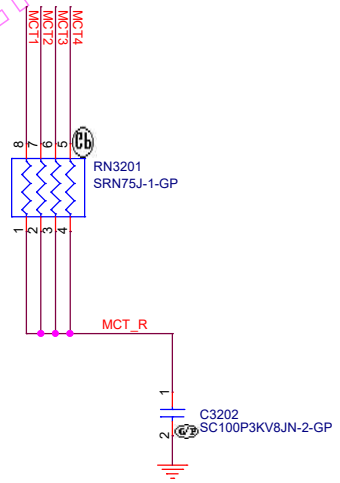







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Title: ***RJ45+Transformer***

| Size | Document Number | Rev |
|---|---|---|
| B | Raichu_GL | -1M |

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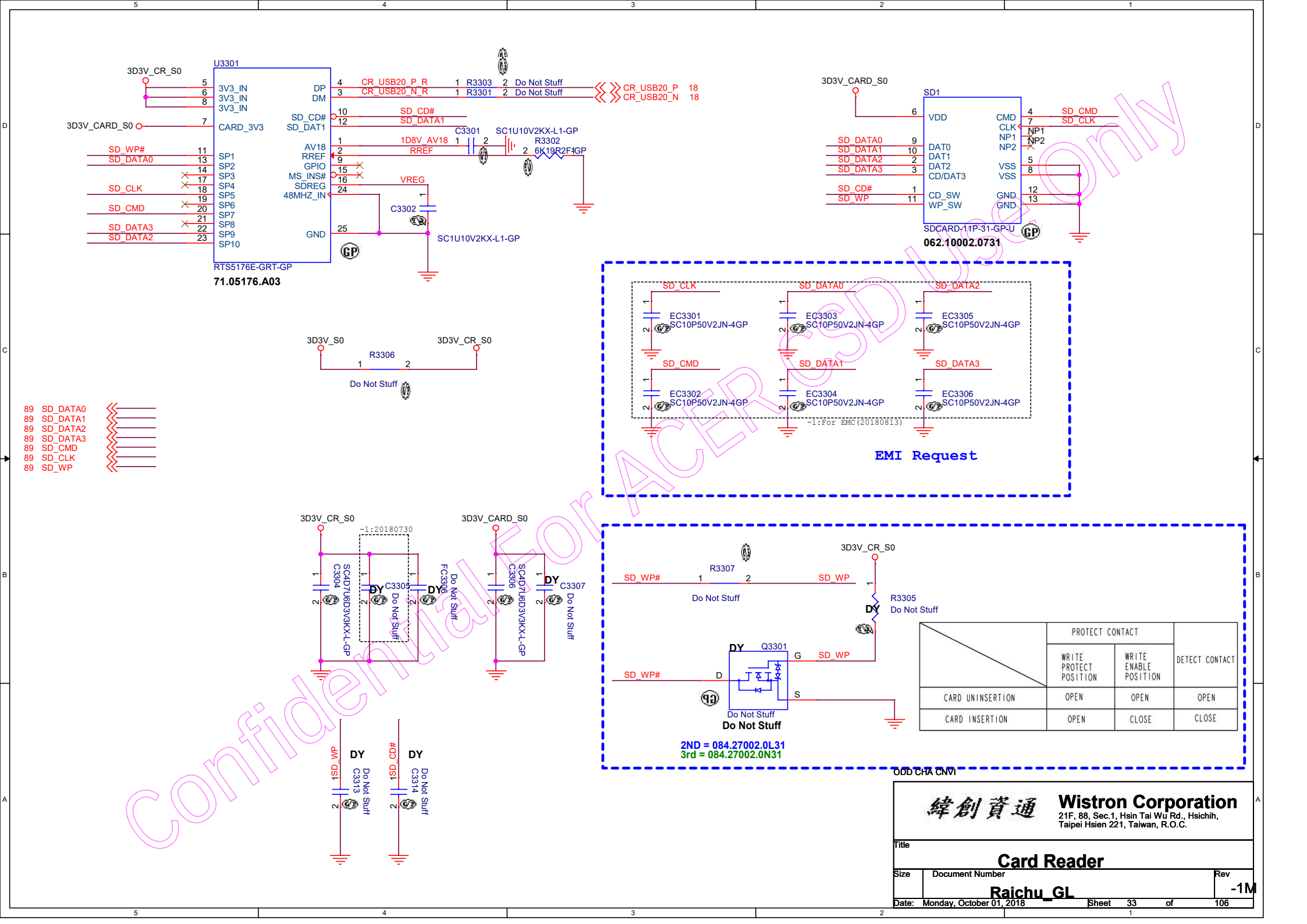




| | | |
|---|---|---|
| Wistron Corporation | Title: Card Reader | |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | Size: | Document Number: Raichu_GL |
| | Rev: -1M | |
| | Date: Monday, October 01, 2018 | Sheet 33 of 106 |

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Title: *Reserved (USB2.0 CONN)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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## USB1

18 USB1_USB20_N
18 USB1_USB20_P
18 USB1_USB30_RX_N
18 USB1_USB30_RX_P
18 USB1_USB30_TX_N
18 USB1_USB30_TX_P

## USB2

18 USB2_USB20_N
18 USB2_USB20_P
18 USB2_USB30_RX_N
18 USB2_USB30_RX_P
18 USB2_USB30_TX_N
18 USB2_USB30_TX_P

## USB3

18 USB3_USB20_N
18 USB3_USB20_P
18 USB3_USB30_RX_N
18 USB3_USB30_RX_P
18 USB3_USB30_TX_N
18 USB3_USB30_TX_P

## USB Power enable

24 USB_PWR_EN

89 USB1_CON_USB20_N
89 USB1_CON_USB20_P
89 USB2_CON_USB20_N
89 USB2_CON_USB20_P
89 USB3_CON_USB20_N
89 USB3_CON_USB20_P

High Active 3A

5V_S5 — U3501 SY6288E1AAC-GP — 5V_USB30
USB_PWR_EN
C3501 SC1U10V2KX-L1-GP
C3502 Do Not Stuff
074.06288.0B9B
2nd = 074.51711.009F

5V_USB30 — C3512 C3513 C3514 C3515 C3516 DY
5V_USB30 — C3517 C3518 C3519 C3520 C3521 DY
5V_USB30 — C3522 C3523 C3524 C3525 C3526 DY
SCD1U16V3MX-L-GP
1M-20181001

USB1_USB30_RX_N — R3501 Do Not Stuff — USB1_USB30_RX_CON_N
USB1_USB30_RX_P — R3502 Do Not Stuff — USB1_USB30_RX_CON_P
EU3501 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
USB1_USB30_TX_N — SCD1U16V2KX-L-GP — C3508
USB1_USB30_TX_P — SCD1U16V2KX-L-GP — C3509

USB1_USB20_P / USB1_USB20_N — EL3502 DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001

USB2_USB30_RX_N — R3503 Do Not Stuff — USB2_USB30_RX_CON_N
USB2_USB30_RX_P — R3504 Do Not Stuff — USB2_USB30_RX_CON_P
EU3502 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
USB2_USB30_TX_N — SCD1U16V2KX-L-GP — C3510
USB2_USB30_TX_P — SCD1U16V2KX-L-GP — C3511

USB2_USB20_P / USB2_USB20_N — EL3501 DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001

USB3_USB30_RX_N — R3505 Do Not Stuff — USB3_USB30_RX_CON_N
USB3_USB30_RX_P — R3506 Do Not Stuff — USB3_USB30_RX_CON_P
EU3504 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
USB3_USB30_TX_N — SCD1U16V2KX-L-GP — C3503
USB3_USB30_TX_P — SCD1U16V2KX-L-GP — C3504

USB3_USB20_P / USB3_USB20_N — EL3503 DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001

5V_USB30 — USB1 SKT-USB13-440-GP
022.10005.0GF1
USB1_CON_USB20_N / USB1_CON_USB20_P
USB1_USB30_RX_CON_N / USB1_USB30_RX_CON_P
USB1_USB30_TX_CON_N / USB1_USB30_TX_CON_P

EU3503 AZC099-04S-2-GP — 5V_S5
USB1_CON_USB20_N / USB1_CON_USB20_P
USB2_CON_USB20_N / USB2_CON_USB20_P
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

5V_USB30 — USB2 SKT-USB13-440-GP
022.10005.0GF1
USB2_CON_USB20_N
USB2_USB30_RX_CON_N / USB2_USB30_RX_CON_P
USB2_USB30_TX_CON_N / USB2_USB30_TX_CON_P

EU3505 AZC099-04S-2-GP — 5V_S5
USB3_CON_USB20_N / USB3_CON_USB20_P
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

5V_USB30 — USB3 SKT-USB13-440-GP
022.10005.0GF1
USB3_CON_USB20_N
USB3_USB30_RX_CON_N / USB3_USB30_RX_CON_P
USB3_USB30_TX_CON_N / USB3_USB30_TX_CON_P

### 5.PIN DEFINE TABLE:

| PIN NO. | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| SIGNAL NAME | VBUS | D- | D+ | GND |

| PIN NO. | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|
| SIGNAL NAME | StdA_SSRX- | StdA_SSRX+ | GND_DRAIN | StdA_SSTX- | StdA_SSTX+ |



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Title: USB (USB3.0 Conn)
Size: A2 | Document Number: Raichu_GL | Rev: -1M
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Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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| | | |
|---|---|---|
| Title: USB (RSVD) | | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 38 of 106 | |

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| | | |
|---|---|---|
| Title | (Reserved) | |
| Size A4 | Document Number Raichu_GL | Rev -1M |
| Date: Monday, October 01, 2018 | Sheet 39 of 106 | |

SSID = Reset.Suspend

# Power Sequence

## ALL_SYS_PWRGD

PMIC_PWRGD — R4006 1 — 2 — ALL_SYS_PWRGD (Do Not Stuff)

To EC

19,46 PMIC_PWRGD
24 ALL_SYS_PWRGD
45 3V_S5_EN
24 S5_ENABLE
24,26 PURE_HW_SHUTDOWN#
19,46 PMIC_THERMTRIP#
19,24,31,61,63,68,89,91 PLT_RST#
19,24,46 PM_SLP_S3#

# To 3V/ 5V Power IC S5 ENABLE

PMIC_THERMTRIP#_R — R4005 1 — 2 — PMIC_THERMTRIP# (Do Not Stuff)

PLT_RST# — R4001 (DY, Do Not Stuff) — H_PWRGD_R — Q4002 (Do Not Stuff, DY)

R4002 (DY, Do Not Stuff)

PLACE CLOSE TO PCH1

D4001 RB551V30-GP

3V_S5_EN — PURE_HW_SHUTDOWN#

Do Not Stuff
2nd = 84.T3904.H11

83.R5003.H8H
2ND = 83.R5003.T8F

R4004 1 — 2KR2F-L1-GP — S5_ENABLE

# RUN Power

## 5V_S0/3D3V_S0

5V_S5 — C4007 (DY, Do Not Stuff) — C4006 SC1U10V2KX-L1-GP

3D3V_S5 — C4008 (DY, Do Not Stuff) — C4009 SC1U10V2KX-L1-GP

U4001 G2898KD1U-GP

VBIAS, IN1#1, IN1#2, IN2#6, IN2#7, EN1, EN2, CT1, CT2, OUT1#13, OUT1#14, OUT2#8, OUT2#9, GND, THERMAL_PAD

SW_5V_S0_CT — C4004 (DY, Do Not Stuff)
SW_3D3V_S0_CT — C4001 (DY, Do Not Stuff)

5V_S0 — 3.5A — C4011 SCD1U16V2KX-L-GP

3D3V_S0 — 3A — C4010 SCD1U16V2KX-L-GP

PM_SLP_S3# — R4003 — 3V_5V_S0_EN — C4051 (DY, Do Not Stuff)

074.02898.0093
2nd = 074.22976.0091

## 1D8V_S0

1D8V_S5 — C4015 SC1U10V2KX-L1-GP

U4002 APE8939GN3-GP

VIN, VBIAS, EN, VOUT#8, VOUT#7, VOUT#6, GND, VIN

3D3V_S0 — R4059 — 1D8V_S0_EN — R4060 PM_SLP_S3# (DY, Do Not Stuff)

C4017 (DY, Do Not Stuff)

1D8V_S0 — 0.5A — C4016 SCD1U16V2KX-L-GP

074.08939.0093
2nd = 074.05027.0093

# Discharge circuit

3D3V_AUX_S5 — R4056 (DY, Do Not Stuff) — 3D3V_S5_EN_DCG

Q4001 (DY, Do Not Stuff)

0221 Rename Net — 3V_S5_EN

3D3V_S5_DISCHG — R4048 (DY, Do Not Stuff) — 3D3V_S5

Do Not Stuff
2ND = 075.27002.0E7C
3rd = 75.27002.F7C



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Title: Sequence (Power Plane EN)

Size: A3 | Document Number: Raichu_GL | Rev: -1M

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| | | |
|---|---|---|
| Title | (Reserved)DS3 | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 41 of 106 | |

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Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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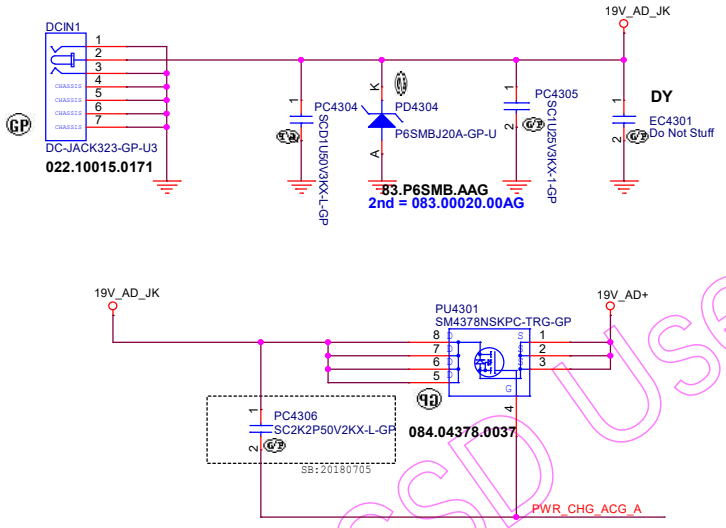
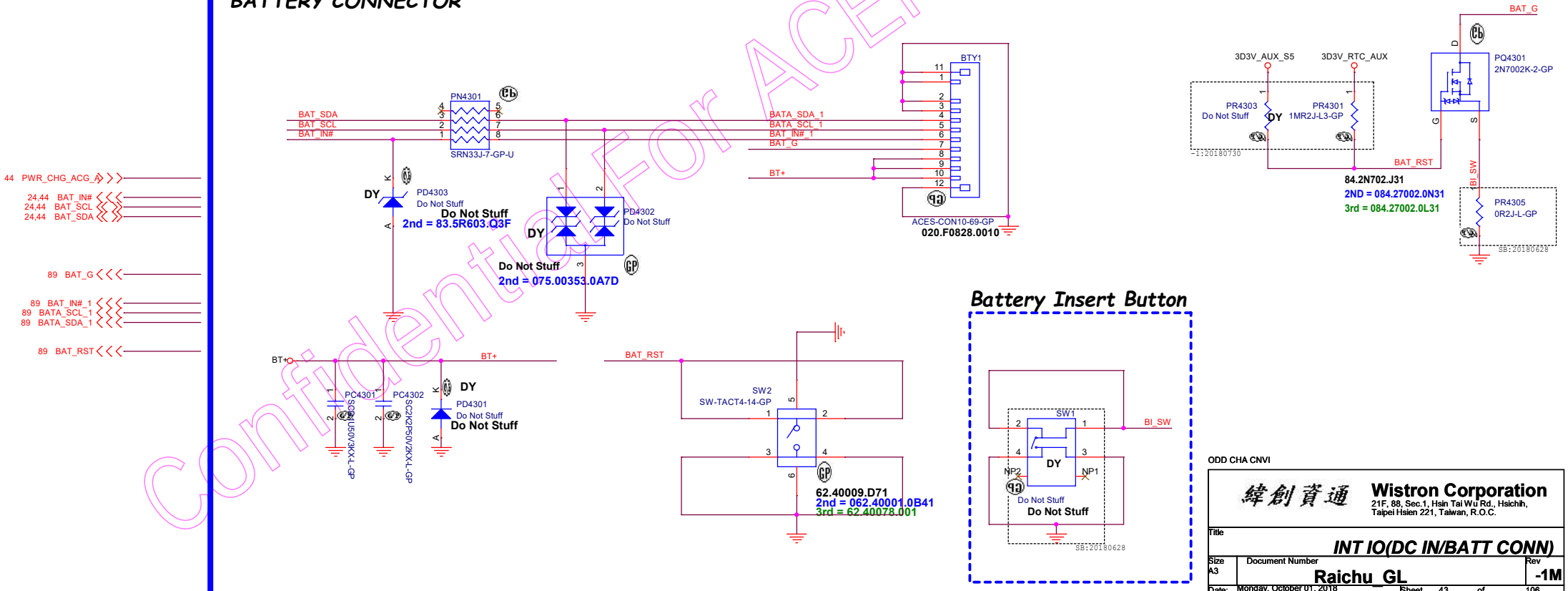
## ANNIE solution

### Adaptor in to generate DCBATOUT




## BATTERY CONNECTOR



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Title: INT IO(DC IN/BATT CONN)

| Size | Document Number | Rev |
|---|---|---|
| A3 | Raichu_GL | -1M |
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## OFFPAGE

24,43 BAT_SCL — PG4408 Do Not Stuff — PWR_CHG_CLK
24,43 BAT_SDA — PG4410 Do Not Stuff — PWR_CHG_DATA
24 BT_IA — PG4418 Do Not Stuff — PWR_CHG_IDCHG
24 AD_IA — PR4413 Do Not Stuff — PWR_CHG_IADP
43 PWR_CHG_ACG_A — PWR_CHG_ACG_A
19,24,44,46 PROCHOT#_CPU — PR4444 Do Not Stuff — PWR_CHG_PROCHOT#
19,24,44,46 PROCHOT#_CPU — PR4445 Do Not Stuff — PROCHOT#_BAT
24 DC_Protect_EC — PR4440 DY Do Not Stuff
24,43 BAT_IN# — PR4420 Do Not Stuff — PWR_CHG_BATPRES#
24 AC_IN# — PR4448 Do Not Stuff — PWR_AC_IN#
24 CHG_ON# — PR4449 Do Not Stuff — PWR_CHG_ON#

PMON : Total system power

TP4401 — PWR_CHG_PMON_TP — PG4412 Do Not Stuff — PWR_CHG_PMON

AC_IN — PG4414 Do Not Stuff — PWR_CHG_ACOK

## SSID = Charger

19V_AD+ — PU4401 SM3317NSQAC-TRG-GP — 084.03317.0A37
SB:Change to 0.1uF(20180706) — PC4407 SCD1U25V2KX-L-GP
PWR_CHG_ACG — PR4421 4K02R2F-GP — PWR_CHG_ACG_A

AD+_TO_SYS — PR4404 D02R3721F-GP-U — 19V_DCBATOUT
PG4401 Do Not Stuff — PG4402 Do Not Stuff
DY PR4409 Do Not Stuff — PC4403 SCD1U25V2KX-L-GP
PWR_CHG_ACP — PC4402 SCD1U25V2KX-L-GP — CHG_AGND
PWR_CHG_ACN — PC4404 SCD1U25V2KX-L-GP — CHG_AGND

BT+_R — PU4402 SM3317NSQAC-TRG-GP — 084.03317.0A37
PWR_CHG_BTG_A — PR4411 4K02R2F-GP — PWR_CHG_BTG

3D3V_AUX_S5 — PR4427 100KR2F-L3-GP — PWR_CHG_ILIM
PR4430 100KR2F-L3-GP — PWR_AC_IN#
PG4406 — SSM6N7002KFU-GP — PWR_CHG_ON#
075.67002.007C
2ND = 075.27002.0E7C
3rd = 75.27002.F7C

19V_AD_JK — PD4404 RB520S30-GP — PWR_CHG_VCC_R — PR4415 20R5J-GP — PWR_CHG_VCC
BT+ — PD4405 RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
PC4401 SC1U25V3KX-1-GP — CHG_AGND

3D3V_AUX_KBC
DY PR4434 Do Not Stuff — DY PR4416 Do Not Stuff
PWR_CHG_DATA
PWR_CHG_CLK

19V_AD_JK — PD4406 RB520S30-GP — PWR_CHG_ACDET_A
3D3V_S5 — PD4407 RB520S30-GP — PWR_CHG_ACDET_B — PR4450 100KR2F-L3-GP
83.R2003.A8M
2nd = 083.52030.008F
PR4406 316KR2F-GP

19V_AD+ — PR4403 4K02R2F-GP — PWR_CHG_CMSRC
PR4410 52K3R2F-L-GP — PC4410 SCD1U25V2KX-L-GP — CHG_AGND
PR4429 100KR2J-4-GP — PWR_CHG_REGN
PR4433 120KR2J-L-GP — PWR_CHG_ACOK

PU4403 BQ24781RUYR-GP
ACN, ACP, CMSRC, ACDRV, ACDET, SDA, SCL, ACOK, IADP, IDCHG, PMON, PROCHOT#, NC#13, NC#14, ILIM
REGN, BATDRV, BATSRC, BTST, HIDRV, PHASE, LODRV, GND, SRP, SRN, TB_STAT#, BATPRES#, THERMAL_PAD
VCC
074.24781.0073
SB:Change to BQ24781(20180621)

PWR_CHG_BOOT_A — PR4414 10R2F-L-GP — PC4417 SCD047U25V2KX-GP
PR4408 Do Not Stuff
PWR_CHG_BTST
PWR_CHG_BOOT
PWR_CHG_HG
PWR_CHG_PH
PWR_CHG_LG
PG4413 Do Not Stuff — PR4425 10R2F-L1-GP — PR4424 10R2F-L1-GP
PWR_CHG_SRP
PWR_CHG_SRN
PR4405 10KR2F-L1-GP — 3D3V_AUX_S5
PWR_CHG_BM#
PWR_CHG_BATPRES#

PWR_CHG_REGN — PC4409 SC2D2U10V3KX-L-GP
PQ4403 AON7408-GP — 084.07408.0037 — 2nd = 084.03319.0033
PQ4404 AON7408-GP — 084.07408.0037 — 2nd = 084.03319.0033
PC4419 SCD1U25V2KX-L-GP — CHG_AGND
PC4416 SCD1U25V2KX-L-GP
PC4412 SCD1U25V2KX-L-GP — CHG_AGND
PWR_CHG_SRP_A
PWR_CHG_SRN_A

19V_DCBATOUT — PC4405 SCD47U25V3KX-L-GP — PC4425 SCD47U25V3KX-L-GP — PC4406 SCD1U25V2KX-L-GP

PL4401 DCIL4D1JH-33-GP — 68.4R71A.20H — 2nd = 068.4R710.1301
Cyntec, 6.8mm x 7.3mm x 3.0mm
DCR: 28.0m~33.0mOhm
Idc : 5.5 A , Isat : 6.5A

BT+_R — PR4417 D01R3721F-GP-U — BT+_R
BT+
PG4403 Do Not Stuff — PG4404 Do Not Stuff
PC4420 SCD1U25V2KX-L-GP — PC4421 SCD1U25V2KX-L-GP — PC4422 SCD1U25V2KX-L-GP — PC4423 SCD1U25V2KX-L-GP

PC4411 SC100P50V2JN-L-GP — DY PR4428 Do Not Stuff — CHG_AGND
PC4408 SC100P50V2JN-L-GP — PR4447 30K5R2F-GP — CHG_AGND
DY PR4432 Do Not Stuff

IADP : AC adapter detect current :
IADP : 20 or 40 x ( Vacp - Vacn ) / 10mohm
IDCHG : Dischange detect current :
= 8 or 16 x ( Vsrn - Vsrp )

**Total Power Setting**

PR4407 45W 73.2K ADT PROTECT 110%
PR4407 45W 105K ADT PROTECT 130%
PR4407 65W 150K ADT PROTECT 110%
PR4407 65W 196K ADT PROTECT 130%

PWR_CHG_REGN — PR4431 Do Not Stuff DY — PWR_CHG_CMPOUT
PR4402 Do Not Stuff DY — PWR_CHG_CMPIN
PWR_CHG_IADP — R1 PR4407 Do Not Stuff DY
R2 PR4401 Do Not Stuff — CHG_AGND
PR4401 100K for BQ24780S
PR4401 0 ohm for BQ24781

PQ4408 上件 for BQ24780S
PQ4408 DY for BQ24781
PWR_CHG_PROCHOT# — PQ4408 — PWR_CHG_CMPOUT
Do Not Stuff
2ND = 084.27002.0N31
3rd = 084.27002.0L31
DY PC4426 Do Not Stuff

| | Stat | PM_SLP_A# | Adaptor Current | AC_Protect protect | AC_Protect Current | PR4408 Sense resistor | 0x12H_Bit4 IADP GAIN | 0x3BH_Bit7 CM_VREF | Current to Voltage | R1 PR4407 | R2 PR4401 | CAL Vcomp | Vsense | R1 | R2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 40W | AC + Battery | High | 2.1 | 102% | 2.142 | 20 | 40 | 1.2 V | 1.7136 | 41.2 | 100 | 1.213598 | 1.7136 | 41.2 | 100 |
| 45W | AC + Battery | High | 2.37 | 102% | 2.4174 | 20 | 40 | 1.2 V | 1.93392 | 60.4 | 100 | 1.205686 | 1.93392 | 60.4 | 100 |
| 65W | AC + Battery | High | 3.42 | 102% | 3.4884 | 10 | 40 | 1.2 V | 1.39536 | 16.2 | 100 | 1.200826 | 1.39536 | 16.2 | 100 |
| 90W | AC + Battery | High | 4.74 | 102% | 4.8348 | 10 | 40 | 1.2 V | 1.93392 | 60.4 | 100 | 1.205686 | 1.93392 | 60.4 | 100 |
| 120W | AC + Battery | High | 6.31 | 102% | 6.4362 | 10 | 40 | 1.2 V | 2.57448 | 113 | 100 | 1.208676 | 2.57448 | 113 | 100 |
| 135W | AC + Battery | High | 7.1 | 102% | 7.242 | 10 | 40 | 1.2 V | 2.8968 | 180 | 100 | 1.207 | 2.8968 | 140 | 100 |

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Title: 044_Power (Charger_BQ24780S)
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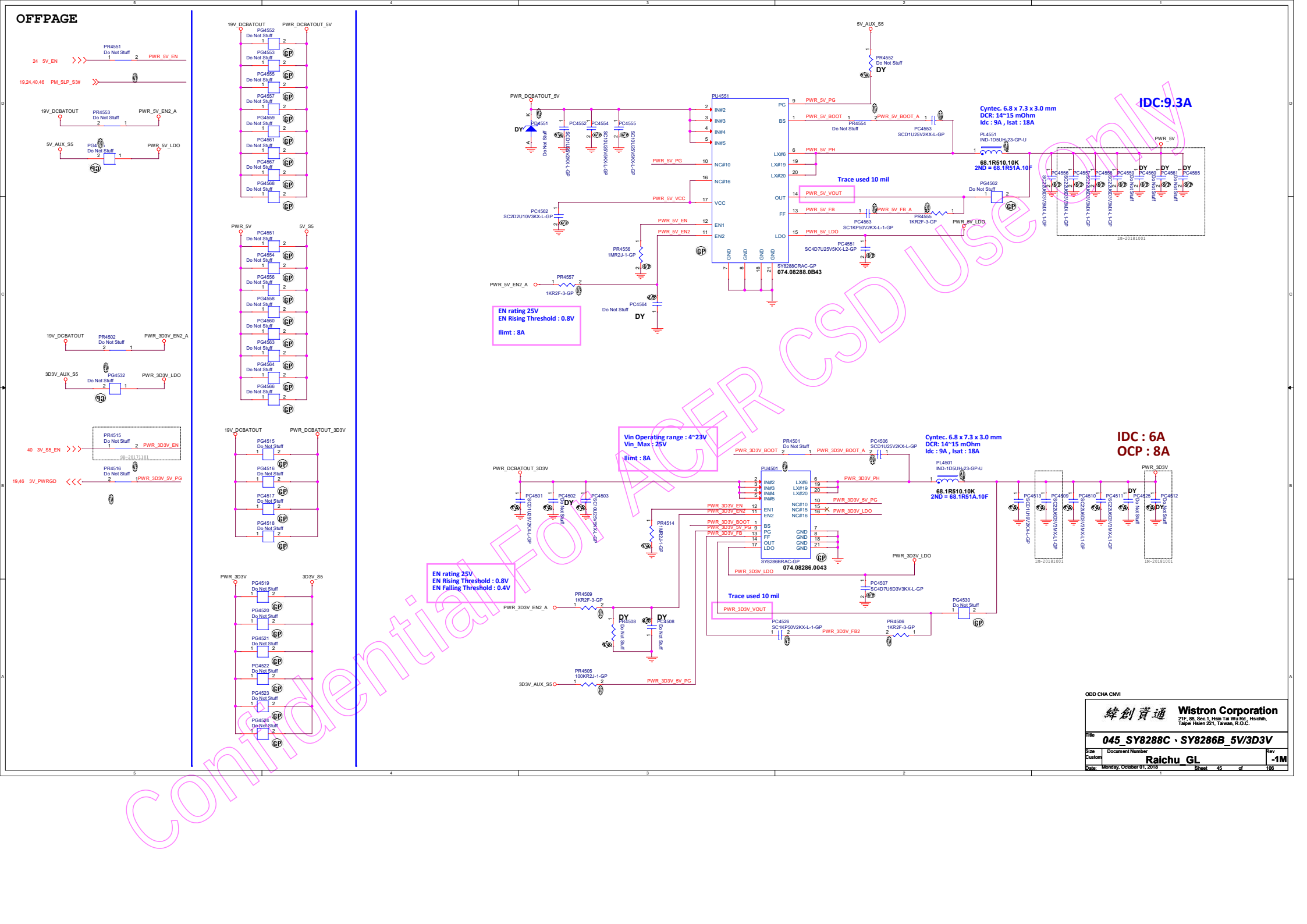
OFFPAGE
24 5V_EN
PR4551 Do Not Stuff PWR_5V_EN
19,24,40,46 PM_SLP_S3#
19V_DCBATOUT PR4553 Do Not Stuff PWR_5V_EN2_A
5V_AUX_S5 PG4 Do Not Stuff PWR_5V_LDO
19V_DCBATOUT PR4502 Do Not Stuff PWR_3D3V_EN2_A
3D3V_AUX_S5 PG4532 Do Not Stuff PWR_3D3V_LDO
40 3V_S5_EN
PR4515 Do Not Stuff PWR_3D3V_EN
SB-20171101
19,46 3V_PWRGD
PR4516 Do Not Stuff PWR_3D3V_5V_PG
19V_DCBATOUT PWR_DCBATOUT_5V
PG4552 PG4553 PG4555 PG4557 PG4559 PG4561 PG4567 PG4568 Do Not Stuff
PWR_5V 5V_S5
PG4551 PG4554 PG4556 PG4558 PG4560 PG4563 PG4564 PG4566 Do Not Stuff
19V_DCBATOUT PWR_DCBATOUT_3D3V
PG4515 PG4516 PG4517 PG4518 Do Not Stuff
PWR_3D3V 3D3V_S5
PG4519 PG4520 PG4521 PG4522 PG4523 PG4524 Do Not Stuff
5V_AUX_S5
PR4552 Do Not Stuff DY
PWR_DCBATOUT_5V
PD4551 Do Not Stuff
PC4551 PC4552 PC4554 PC4555
PU4551
IN#2 IN#3 IN#4 IN#5
PWR_5V_PG NC#10 NC#16 PWR_5V_VCC VCC
PWR_5V_EN PWR_5V_EN2 EN1 EN2
PG BS LX#6 LX#19 LX#20 OUT FF LDO
GND GND GND GND
SY8288CRAC-GP
074.08288.0B43
PC4562 SC2D2U10V3KX-L-GP
PR4556 1MR2J-1-GP
PR4557 1KR2F-3-GP PWR_5V_EN2_A
PC4564 Do Not Stuff DY
EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A
PWR_5V_PG PWR_5V_BOOT PWR_5V_PH PWR_5V_VOUT PWR_5V_FB PWR_5V_LDO
PR4554 Do Not Stuff
PC4553 SCD1U25V2KX-L-GP
PWR_5V_BOOT_A
Trace used 10 mil
PL4551 IND-1D5UH-23-GP-U
Cyntec. 6.8 x 7.3 x 3.0 mm
DCR: 14~15 mOhm
Idc : 9A , Isat : 18A
IDC:9.3A
68.1R510.10K
2ND = 68.1R51A.10F
PG4582 Do Not Stuff
PWR_5V_FB_A
PC4563 SC1KP50V2KX-L-1-GP
PR4555 1KR2F-3-GP
PWR_5V_LDO
PC4551 SC4D7U25V5KX-L2-GP
PWR_5V
PC4556 PC4557 PC4558 PC4559 PC4560 PC4561 PC4565 DY Do Not Stuff
1M-20181001
Vin Operating range : 4~23V
Vin_Max : 25V
Ilimt : 8A
PWR_3D3V_BOOT PWR_3D3V_PH PWR_3D3V_5V_PG PWR_3D3V_LDO PWR_3D3V_EN PWR_3D3V_EN2 PWR_3D3V_FB PWR_3D3V_VOUT PWR_3D3V_FB2
PR4501 Do Not Stuff
PC4506 SCD1U25V2KX-L-GP
PWR_3D3V_BOOT_A
PU4501
IN#2 IN#3 IN#4 IN#5
EN1 EN2
BS PG FF OUT LDO
LX#6 LX#19 LX#20
NC#10 NC#15 NC#16
GND GND GND GND
SY8286BRAC-GP
074.08286.0043
PL4501 IND-1D5UH-23-GP-U
Cyntec. 6.8 x 7.3 x 3.0 mm
DCR: 14~15 mOhm
Idc : 9A , Isat : 18A
IDC : 6A
OCP : 8A
68.1R510.10K
2ND = 68.1R51A.10F
PWR_3D3V
PC4513 PC4509 PC4510 PC4511 PC4525 PC4512 DY Do Not Stuff
1M-20181001
PC4501 PC4502 PC4503 DY Do Not Stuff
PR4514 1MR2J-1-GP
EN rating 25V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
PR4509 1KR2F-3-GP PWR_3D3V_EN2_A
PR4508 PC4508 DY Do Not Stuff
PR4505 100KR2J-1-GP 3D3V_AUX_S5
PC4507 SC4D7U6D3V3KX-L-GP
PG4530 Do Not Stuff
PC4526 SC1KP50V2KX-L-1-GP
PR4506 1KR2F-3-GP
Trace used 10 mil
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19 CPU_I2C_SCL_PMIC — PR4609 Do Not Stuff — PWR_CLK
19 CPU_I2C_SDA_PMIC — PR4615 Do Not Stuff — PWR_DATA
19,45 3V_PWRGD — PR4616 Do Not Stuff — PWR_PMIC_EN
19 PM_SLP_S0# — PR4617 Do Not Stuff — PWR_SLP_S0_B
19,24,40 PM_SLP_S3# — PR4618 Do Not Stuff — PWR_SLP_S3_B
19,24 PM_SLP_S4# — PR4619 Do Not Stuff — PWR_SLP_S4_B
19,24 PMIC_RSMRST# — PR4620 Do Not Stuff — PWR_RSMEST_B
19,40 PMIC_PWRGD — PR4621 Do Not Stuff — PWR_PCH_PWROK
19,40 PMIC_THERMTRIP# — PR4622 Do Not Stuff — PWR_THERMTRIP_B
19,24,44 PROCHOT#_CPU — PR4623 Do Not Stuff — PWR_PROCHOT_B
20 PMIC_IRQ# — PR4624 Do Not Stuff — PWR_IRQ_B

19V_DCBATOUT — PG4613 Do Not Stuff — PWR_VSYS
1D8V_S5 — PG4601 Do Not Stuff — PWR_VDD_1VP8A
5V_S5 — PG4614 Do Not Stuff — PWR_VSYS_V5A_0A
5V_S5 — PG4616 Do Not Stuff — PWR_VSYS_V5A_1
5V_S5 — PG4615 Do Not Stuff — PWR_VSYS_V5A_2

# Main Func = CPU_CORE

## I2C, Other signals

PWR_VSYS — PC4602 SC1U25V3KX-1-GP
PWR_VDD_1VP8A — PC4601 SC1U10V2KX-L1-GP

Table 4-2. Gemini Lake PMIC and SoC Signal Connections

| Gemini Lake PMIC Pin | Gemini Lake SoC Pin Name | SoC Pin | SoC Pin Type | Voltage Rail |
|---|---|---|---|---|
| IRQ# | TBD | TBD | Input | 1.8V (SoC internal) |
| THERMTRIP# | THERMTRIP_N | J53 | Output | 1.8V (SoC internal) |
| PROCHOT# | PROCHOT_N | J54 | Input | 1.8V (SoC internal) |
| SLP_S4# | PMU_SLP_S4_N | J49 | Output | 1.8V (SoC internal) |
| SLP_S3# | PMU_SLP_S3_N | D51 | Output | 1.8V (SoC internal) |
| SLP_S0# | PMU_SLP_S0_N | C52 | Output | 1.8V (SoC internal) |
| PCH_PWROK | SoC_PWROK | D35 | Input | External PU 20K to V3P3A and PD 100K to GND |
| RSMRST# | RSM_RST_N | F27 | Input | External PU 20K to V3P3A and PD 100K to GND |
| DATA | PMIC_I2C_SDA | TBD | Input/ Output | 1.8V (SoC internal) |
| CLK | PMIC_I2C_SCL | TBD | Output | 1.8V (SoC internal) |

3D3V_S5 — RN4601 SRN10KJ-L-GP
DY — PR4628 Do Not Stuff
DY — PR4627 Do Not Stuff

PU4601E (5 OF 5) BD2671MWV-E2-GP 074.02671.0073

| | | | | | |
|---|---|---|---|---|---|
| PWR_VSYS | 57 | VSYS | VSYS_V5A_0 | 31 | PWR_VSYS_V5A_0 |
| PWR_VDD_1VP8A | 29 | VDD_V1P8A | VSYS_V5A_1 | 4 | PWR_VSYS_V5A_1 |
| PWR_CLK | 37 | CLK | VSYS_V5A_2 | 50 | PWR_VSYS_V5A_2 |
| PWR_DATA | 36 | DATA | LDO15 | 30 | PWR_PMIC_LDO1D5V |
| PWR_PMIC_EN | 33 | PMIC_EN | EXTMODE | 32 | PWR_EXTMODE |
| PWR_SLP_S0_B | 20 | SLP_S0_B | TEST0 | 39 | PWR_TEST0 |
| PWR_SLP_S3_B | 21 | SLP_S3_B | DDR_SEL0 | 2 | PWR_EXTMODE0 |
| PWR_SLP_S4_B | 22 | SLP_S4_B | DDR_SEL1 | 12 | PWR_EXTMODE1 |
| PWR_RSMEST_B | 19 | RSMRST_B | DDR_SEL2 | 17 | PWR_EXTMODE2 |
| PWR_PCH_PWROK | 18 | PCH_PWROK | GND0 | 28 | |
| PWR_THERMTRIP_B | 34 | THERMTRIP_B | GND1 | 46 | |
| PWR_PROCHOT_B | 35 | PROCHOT_B | GND2 | 64 | |
| PWR_IRQ_B | 38 | IRQ# | PGND | 69 | |

PWR_VSYS_V5A_0A — PR4603 20R2J-3-GP — PC4603 SC4D7U6D3V3KX-L-GP
PWR_VSYS_V5A_1 — PC4604 SC4D7U6D3V3KX-L-GP
PWR_VSYS_V5A_2 — PC4615 SC4D7U6D3V3KX-L-GP
PC4605 SC4D7U6D3V3KX-L-GP
PR4608 100KR2F-L3-GP

5V_S5 —
PR4631 Do Not Stuff DY
PR4604 Do Not Stuff
PR4605 Do Not Stuff
PR4632 Do Not Stuff DY
PR4630 Do Not Stuff
PR4606 Do Not Stuff DY
PR4607 Do Not Stuff DY
PR4633 Do Not Stuff

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

| DDR_SEL2,1,0 | DDR selection | VDDQ voltage | LDO_VPP voltage | V1P2A Voltage | VTT Voltage | Description |
|---|---|---|---|---|---|---|
| (L,L,L) | LPDDR3 | 1.200V | 1.800V | 1.200V | 0.600V | - |
| (L,L,H) | DDR3L | 1.350V | OFF | 1.200V | 0.675V | LDO_VPP unused |
| (L,H,L) | LPDDR4 | 1.100V | 1.800V | 1.200V | 0.550V | - |
| (L,H,H) | DDR4 | 1.200V | 2.500V | 1.200V | 0.600V | - |
| (H,L,L) | LPDDR3 | 1.200V (V1P2A boot timing) | 1.800V | OFF | 0.600V | V1P2A merged to VDDQ |
| (H,L,H) | DDR3L | 1.350V | 1.800V (SLP_S3_B control) | 1.200V | 0.675V | LDO_VPP can be used as optional LDO |
| (H,H,L) | LPDDR4 | 1.100V | 1.800V | 1.200V | OFF | VTT unused |
| (H,H,H) | DDR4 | 1.200V (V1P2A boot timing) | 2.500V | OFF | 0.600V | V1P2A merged to VDDQ |



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Main Func = CPU_CORE

# BUCK2 [VCCGI] : 1.0V_21A

## OFFPAGE

6 VCCGI_SENSE — PR4723 Do Not Stuff — PWR_VCCGI_FBPC

6 VSSGI_SENSE — PR4724 Do Not Stuff — PWR_VCCGI_FBNB

19V_DCBATOUT — PWR_DCBATOUT_VCORE

PG4701 Do Not Stuff
PG4702 Do Not Stuff
PG4703 Do Not Stuff
PG4704 Do Not Stuff
PG4705 Do Not Stuff
PG4706 Do Not Stuff
DY PT4702 Do Not Stuff

5V_S5 — PR4701 Do Not Stuff — PWR_VCCGI_PVCC

PC4705 SC4D7U6D3V3KX-L-GP

## MOSFET GATE Driver

PWR_VCCGI_PVCC — PC4716 SC1U10V2KX-L1-GP

PU4701 BD9515NUXE2-GP-U 74.09515.043
PVCC, BOOT, PWM, HG, EN, SW, PAD/PGND, LG
PWR_VCCGI_PWM_A
PWR_VCCGI_BOOT — PR4720 Do Not Stuff — PC4711 SCD47U25V3KX-1GP
PWR_VCCGI_HG
PWR_VCCGI_PH
PWR_VCCGI_LG
DY PR4721 Do Not Stuff — PWR_VCCGI_HG_A

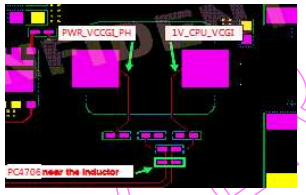
PU4702 FDMS3600-02-RJK0215-COLAY-GP
075.00046.0073
2nd = 075.07321.0073

PWR_DCBATOUT_VCORE
PC4702 PC4703 PC4701 PC4704 SC10U25V6KX-L-GP

PR4702 Do Not Stuff

PU4601A 1 OF 5
VCCGI_PWM 49 PWR_VCCGI_PWM
VCCGI_DRVEN 48 PWR_VCCGI_DRVEN
VCCGI_CSP 51 PWR_VCCGI_CSP
VCCGI_CSN 52 PWR_VCCGI_CSN
VCCGI_VOS 53 PWR_VCCGI_VOS
VCCGI_FBP 54 PWR_VCCGI_FBP
VCCGI_FBN 55 PWR_VCCGI_FBN
BD2671MWV-E2-GP 074.02671.0073

PC4717 SC68P50V2JN-1GP
PR4710 Do Not Stuff
PR4711 390R2F-2GP




PL4701 COIL-D15UH-8-GP 068.R1510.2091
CYNTEC 6.8 X 7.6 X 2.4 mm
DCR: 0.92 +-7% m ohm
Idc :32A , Isat : 41A

PG4710 Do Not Stuff — PG4711 Do Not Stuff
PWR_VCCGI_CSPB
PR4707 1K8R2F-GP
PR4708 2K7R2F-GP
PWR_VCCGI_PHA
PR4719 NTC-10K-27-GP-U 69.60013.131 2nd = 69.60011.201
PR4709 3K3R2F-2-GP
SB-20171116
close choke

close PMIC
PC4714 SCD047U25V2KX-GP
close choke
PC4706 SCD22U25V3KX-GP
PWR_VCCGI_CSPA
PWR_VCCGI_CSNA

close PMIC
PC4710 SCD047U25V2KX-GP
PR4716 Do Not Stuff
PR4712 4K3R3F-GP
PR4715 Do Not Stuff
PWR_VCCGI_FBPA
PWR_VCCGI_FBPB
DY PC4712 Do Not Stuff
PC4713 SC1U10V2KX-L1-GP
PR4713 Do Not Stuff
PWR_VCCGI_FBNA
DY PC4736 Do Not Stuff

PG4707 Do Not Stuff — PWR_VCCGI_FBPC — PR4717 100R2F-L1-GP-U — 1V_CPU_VCGI
PG4708 Do Not Stuff — PWR_VCCGI_FBNB — PR4733 100R2F-L1-GP-U

PC4707 Do Not Stuff DY

close choke
VCCGI :1D0V_25A
1V_CPU_VCGI
PC4718 SC22U6D3V3MX-L1-GP
PT4701 SE330U2VDM-4-GP 79.33719.20C 2nd = 077.53371.0081
Panasonic 7.3 * 4.3 * 1.9 mm
ESR: 9 m ohm

ICCMAX=25A
TDC=17.5A

PWR_VCCGI_PH
22uF_6.3V_0603 *13pcs
DY*3pcs
DY PR4722 Do Not Stuff
PWR_VCCGI_SNUB
DY PC4715 Do Not Stuff



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| | |
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Taipei Hsien 221, Taiwan, R.O.C.

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| Date: Monday, October 01, 2018 | Sheet 48 of 106 | |

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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|---|---|---|
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5V_S5 — PG5001 Do Not Stuff — PWR_VNN_VIN

1V_CPU_VNN — PG5002 Do Not Stuff — PWR_1V_VNN

PG5003 Do Not Stuff

PG5005 Do Not Stuff

PG5006 Do Not Stuff

PG5011 Do Not Stuff

PR5011 Do Not Stuff

6 VNN_VCC_SENSE — PWR_VNN_FBP

PR5012 Do Not Stuff

6 VNN_VSS_SENSE — PWR_VNN_FBA

5V_S5 — PG5007 Do Not Stuff — PWR_VCCRAM_VIN

-1M:20180828

# VNN[BUCK1], VCCRAM[BUCK3]

PU4601C 3 OF 5

VNN_VIN0 / VNN_VIN1 — PWR_VNN_VIN

PC5001 SC10U6D3V3MX-L-GP

VNN_LX00 / VNN_LX01 — PWR_VNN_PHA — PL5001 IND-D47UH-92-GP 068.R4710.1101 2nd = 68.R4750.10F

VNN_LX10 / VNN_LX11 — PWR_VNN_PHB — PL5002 IND-D47UH-92-GP 068.R4710.1101 2nd = 68.R4750.10F

PWR_1V_VNN

Back1 [VNN] :1.05V_4A

PC5009 SC1U10V2KX-L1-GP

22uF_6.3V_0603 *6pcs
Dummy 2pcs

VNN_FBP — PWR_VNN_FBP

PR5001 100R2F-L1-GP-U

PC5013 DY Do Not Stuff

PC5015 Do Not Stuff

PR5018 100R2F-L1-GP-U

PWR_VNN_FBA

PC5014 DY Do Not Stuff

PWR_VCCRAM_VIN

VCCRAM_VIN0 / VCCRAM_VIN1 — PWR_VCCRAM_VIN

PC5002 SC10U6D3V3MX-L-GP

Back3 [VCCRAM] :1.05V_4.5A

1D05V_S0

VCCRAM_LX00 / VCCRAM_LX01 — PWR_VCCRAM_PHA — PL5003 IND-D47UH-92-GP 068.R4710.1101 2nd = 68.R4750.10F

VCCRAM_LX10 / VCCRAM_LX11 — PWR_VCCRAM_PHB — PL5004 IND-D47UH-92-GP 068.R4710.1101 2nd = 68.R4750.10F

1M:20181001

PC5012 SC1U10V2KX-L1-GP

PC5011 PC5010 PC5003 PC5004 PC5005 PC5006 SC22U6D3V3MX-L1-GP

PC5007 DY Do Not Stuff

PC5008 DY Do Not Stuff

PG5004 Do Not Stuff

VCCRAM_FBP — PWR_VCCRAM_FBP

BD2671MWV-E2-GP
074.02671.0073

5-5 G3 to S5/S4 & S5/S4 to S0 Power Sequence (DDR_SEL2,1,0="000""010""011")

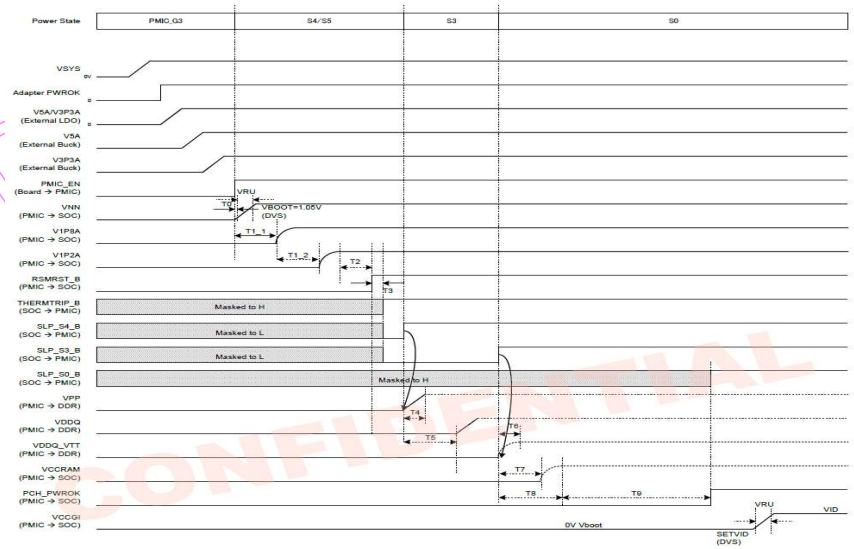


Figure 5-2 G3 to S5/S4 & S5/S4 to S0 Power Sequence



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## OFFPAGE

19V_DCBATOUT
PWR_DCBATOUT_VDDQ
1D2V_CPU_VDDQ_S3
PWR_VDDQ
5V_S5
PWR_VDDQ_PVCC
5V_S5
PWR_1D2V_VIN
1D2V_S5
PWR_1D2V
5V_S5
PWR_1D8V_VIN
1D8V_S5
PWR_1D8V
0D6V_VREF_S0
PWR_VTT
3D3V_S5
PWR_VPP_VIN
2D5V_S3
PWR_VPP

# VDDQ[BUCK6], V1P2A[BUCK5]

## MOSFET GATE Driver

PWR_DCBATOUT_VDDQ
PU5102 AON7408-GP
084.07408.0037
2nd = 084.03319.0033
PU5103 AON7506-GP
84.07506.037
2nd = 084.03317.0A37
PWR_VDDQ_PVCC
PU5101 BD9515NUXE2-GP-U
74.09515.043
PWR_VDDQ_BOOT
PWR_VDDQ_HG
PWR_VDDQ_PH
PWR_VDDQ_LG
PWR_VDDQ_HG_A
PWR_VDDQ_PWM_A
PU4601B BD2671MWV-E2-GP
074.02671.0073
VDDQ_PWM
VDDQ_DRVEN
PWR_VDDQ_PWM
PWR_VDDQ_DRVEN
68.R4710.10M
2nd = 068.R4710.1461
PL5101 IND-D47UH-22-GP-U
Cyntec 6.8mm × 7.3mm × 3.0mm
DCR: 4.0~4.2 m ohm
Idc :17.5A , Isat : 26A
Near the inductor
VDDQ :1.11V / 1.12V 8.2A
close PMIC
close choke
VDDQ_CSP
VDDQ_CSN
VDDQ_FBP
PWR_VDDQ_CSP
PWR_VDDQ_CSN
PWR_VDDQ_FBP
PWR_VDDQ_CSPA
PWR_VDDQ_CSNA
PWR_VDDQ_CSPB
PWR_VDDQ_PHA
PWR_VDDQ_PH
PWR_VDDQ_SNUB
NTC-10K-27-GP-U
59.60013.131
2nd = 59.60011.201
Do Not Stuff
2nd = 077.53371.0081

# V1P2A[BUCK5] : 1.2V, 2.5A

V1P2A_VIN0
V1P2A_VIN1
V1P2A_LX0
V1P2A_LX1
V1P2A_FBP
PWR_1D2V_VIN
PWR_1D2V_PH
PWR_1D2V_FBP
PWR_1D2V
PL5102 IND-D47UH-92-GP
068.R4710.1101
2nd = 68.R4750.10F

# V1P8A[BUCK6] : 1.8V, 1.4A

PU4601D BD2671MWV-E2-GP
074.02671.0073
V1P8A_VIN0
V1P8A_VIN1
V1P8A_LX0
V1P8A_LX1
V1P8A_FBP
PWR_1D8V_VIN
PWR_1D8V_PH
PWR_1D8V_FBP
PWR_1D8V
PL5103 IND-D47UH-92-GP
068.R4710.1101
2nd = 68.R4750.10F
1.8V_1.4A

# VTT: VDDQ/2 1.2A

VTT_VIN
VTT0
VTT1
VTT_FBP
PWR_VTT_VIN
PWR_VTT_FB
PWR_VTT
PWR_VDDQ

# 2.5V_1A

LDO_VPP_VIN
LDO_VPP
LDO_VPP_FBP
PWR_VPP_VIN
PWR_VPP_FB
PWR_VPP

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

| DDR_SEL2,1,0 | DDR selection | VDDQ voltage | LDO_VPP voltage | V1P2A Voltage | VTT Voltage | Description |
|---|---|---|---|---|---|---|
| (L,L,L) | LPDDR3 | 1.200V | 1.800V | 1.200V | 0.600V | - |
| (L,L,H) | DDR3L | 1.350V | OFF | 1.200V | 0.675V | LDO_VPP unused |
| (L,H,L) | LPDDR4 | 1.100V | 1.800V | 1.200V | 0.550V | - |
| (L,H,H) | DDR4 | 1.200V | 2.500V | 1.200V | 0.600V | - |
| (H,L,L) | LPDDR3 | 1.200V (V1P2A boot timing) | 1.800V | OFF | 0.600V | V1P2A merged to VDDQ |
| (H,L,H) | DDR3L | 1.350V | 1.800V (SLP_S3_B control) | 1.200V | 0.675V | LDO_VPP can be used as optional LDO |
| (H,H,L) | LPDDR4 | 1.100V | 1.800V | 1.200V | OFF | VTT unused |
| (H,H,H) | DDR4 | 1.200V (V1P2A boot timing) | 2.500V | OFF | 0.600V | V1P2A merged to VDDQ |

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|---|---|---|
| A4 | Raichu_GL | -1M |

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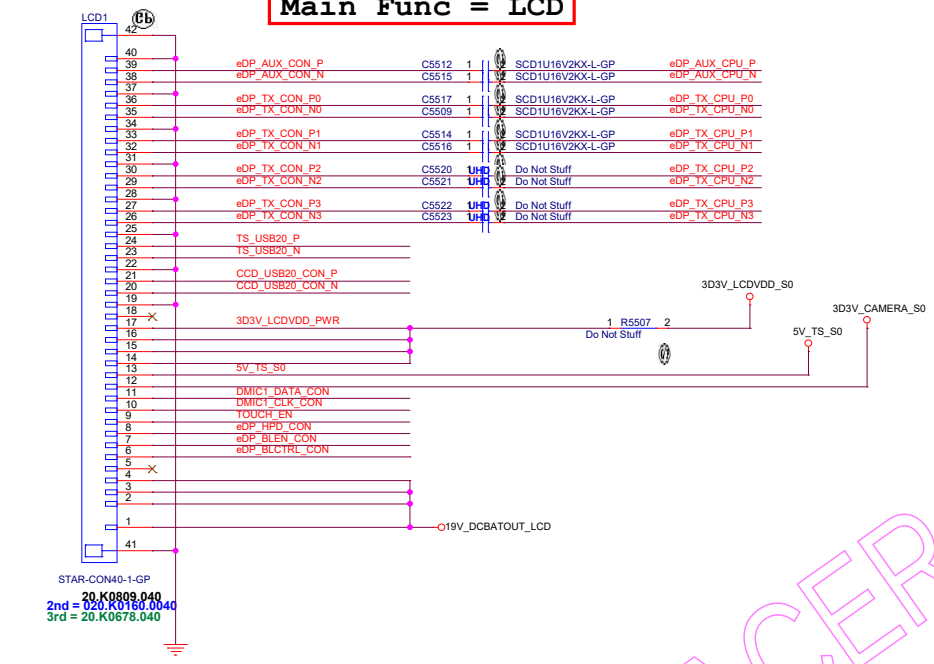
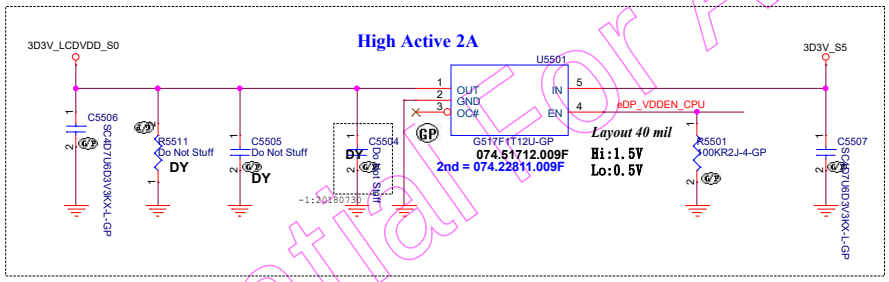
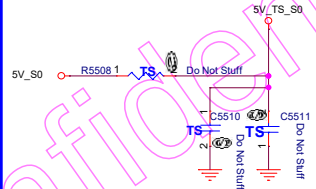
SSID = VIDEO

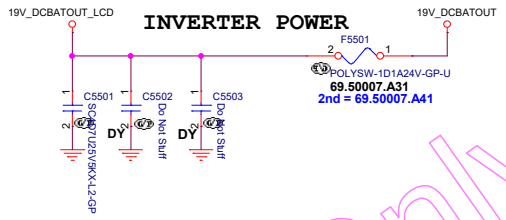
Panel Conn.

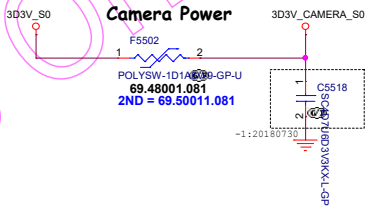
Main Func = LCD

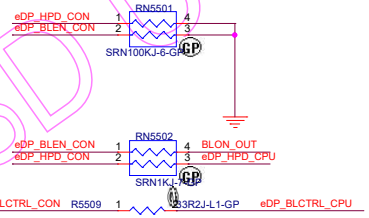


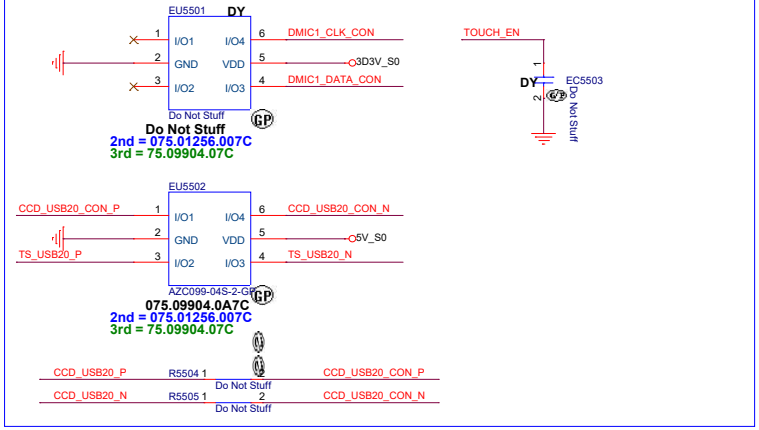




EMI Request:

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8 CRT_DDI_TX_N0
8 CRT_DDI_TX_P0
8 CRT_DDI_TX_N1
8 CRT_DDI_TX_P1

8 CRT_AUX_CPU_N
8 CRT_AUX_CPU_P

8 CRT_HPD_CON

Colay

R5601 1 CRT 2 Do Not Stuff

EL5601

CRT_DDI_TX_P0 4 3 CRT_DDI_TX_CON_P0

CRT_DDI_TX_N0 1 2 CRT_DDI_TX_CON_N0

DY

Do Not Stuff

Do Not Stuff

R5602 1 CRT 2 Do Not Stuff

Colay

R5603 1 CRT 2 Do Not Stuff

EL5602

CRT_DDI_TX_P1 4 3 CRT_DDI_TX_CON_P1

CRT_DDI_TX_N1 1 2 CRT_DDI_TX_CON_N1

DY

Do Not Stuff

Do Not Stuff

R5604 1 CRT 2 Do Not Stuff

Colay

R5605 1 CRT 2 Do Not Stuff

EL5603

CRT_AUX_CPU_P 4 3 CRT_AUX_CPU_CON_P

CRT_AUX_CPU_N 1 2 CRT_AUX_CPU_CON_N

DY

Do Not Stuff

Do Not Stuff

R5606 1 CRT 2 Do Not Stuff

IOBD1

17
1
CRT_DDI_TX_CON_P0 2
CRT_DDI_TX_CON_N0 3
4
CRT_DDI_TX_CON_P1 5
CRT_DDI_TX_CON_N1 6
7
CRT_AUX_CPU_CON_P 8
CRT_AUX_CPU_CON_N 9
10
CRT_HPD_CON 11
12
13
14
15
16
18

CRT

3D3V_S0
5V_S0

Do Not Stuff

Do Not Stuff

2nd = 20.K0460.016



ODD CHA CNVI

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Title: Display (CRT)

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|---|---|---|
| A4 | Raichu_GL | -1M |

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SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

## HDMI CONN

8 HDMI_DDI_TX_P0
8 HDMI_DDI_TX_N0
8 HDMI_DDI_TX_P1
8 HDMI_DDI_TX_N1
8 HDMI_DDI_TX_P2
8 HDMI_DDI_TX_N2
8 HDMI_DDI_TX_P3
8 HDMI_DDI_TX_N3
8 HDMI_SCL_CPU
8 HDMI_SDA_CPU

89 HDMI_DDI_TX_CON_N3
89 HDMI_DDI_TX_CON_P3
89 HDMI_DDI_TX_CON_P0
89 HDMI_DDI_TX_CON_N0
89 HDMI_DDI_TX_CON_P1
89 HDMI_DDI_TX_CON_N1
89 HDMI_DDI_TX_CON_P2
89 HDMI_DDI_TX_CON_N2
89 HDMI_SCL_CON
89 HDMI_SDA_CON
89 HDMI_HPD_CON

8 HDMI_HPD_CON

HDMI1
5V_HDMI_S0 18 +5V_POWER
HDMI_DDI_TX_CON_P0 7 TMDS_DATA0+
HDMI_DDI_TX_CON_N0 9 TMDS_DATA0-
HDMI_DDI_TX_CON_P1 4 TMDS_DATA1+
HDMI_DDI_TX_CON_N1 6 TMDS_DATA1-
HDMI_DDI_TX_CON_P2 1 TMDS_DATA2+
HDMI_DDI_TX_CON_N2 3 TMDS_DATA2-
8 TMDS_DATA0_SHIELD
5 TMDS_DATA1_SHIELD
2 TMDS_DATA2_SHIELD
HDMI_DDI_TX_CON_P3 11 TMDS_CLOCK_SHIELD
HDMI_DDI_TX_CON_N3 10 TMDS_CLOCK+
12 TMDS_CLOCK-
15 SCL
16 SDA
13 CEC
17 DDC/CEC_GROUNG
19 HOT_PLUG_DETECT
14 RESERVED#14
20 GND
21 GND
22 GND
23 GND
HDMI (A_Type)
HDMI_SCL_CON
HDMI_SDA_CON
HDMI_HPD_CON
SKT-HDMI23-124-GP-U
022.10025.0041

5V_HDMI_S0 — F5701 — 5V_S0
POLYSW-1D1A6V-9-GP-U
69.48001.081
2ND = 69.50011.081

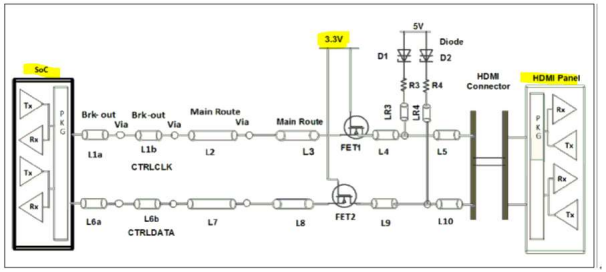
5V_HDMI_S0
D5701
BAW56-9-GP-U
75.00056.07D
2nd = 83.00056.Y11
5V_DDC_HDMI1
5V_DDC_HDMI2
RN5701
SRN2K2J-5-GP
HDMI_SCL_CON
HDMI_SDA_CON

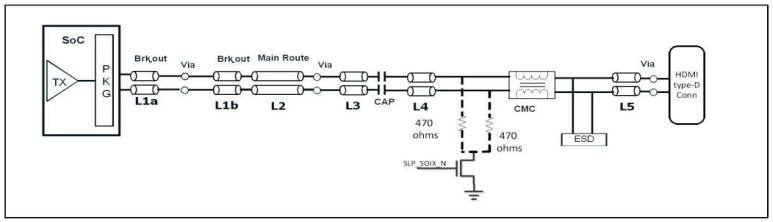
HDMI_DDI_TX_P0 C5709 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_N0 C5711 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_P1 C5710 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_N1 C5712 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_P2 C5714 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_N2 C5713 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_P3 C5716 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_N3 C5715 SCD1U16V2KX-L-GP HDMI_DDI_TX_CON_N3

1R5701 1R5702 1R5703 1R5704 1R5705 1R5706 1R5707 1R5708
470R2F-GP

3D3V_S0
Q5702
HDMI_SDA_CPU
HDMI_SDA_CON
HDMI_SCL_CPU
HDMI_SCL_CON
SSM6N7002KFU-GP
075.67002.007C
2ND = 075.27002.0E7C
3rd = 75.27002.F7C

3D3V_S0
Q5701
G
D
S
HDMI_PLL_GND
2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0N31
3rd = 084.27002.0L31




EMI Request:

ED5701
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

ED5702
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

ED5703
HDMI_SCL_CON
HDMI_SDA_CON
HDMI_HPD_CON
5V_HDMI_S0
AZC199-04S-R7G
075.00199.07C
2nd = 075.08105.007C

HDMI_DDI_TX_CON_N3 ER5701 Do Not Stuff HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N0 ER5702 Do Not Stuff HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1 ER5703 Do Not Stuff HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2 ER5704 Do Not Stuff HDMI_DDI_TX_CON_P2

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Title: HDMI Level Shifter/Connector
Size: Custom
Document Number: Raichu_GL
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| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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|---|---|---|
| A4 | Raichu_GL | -1M |

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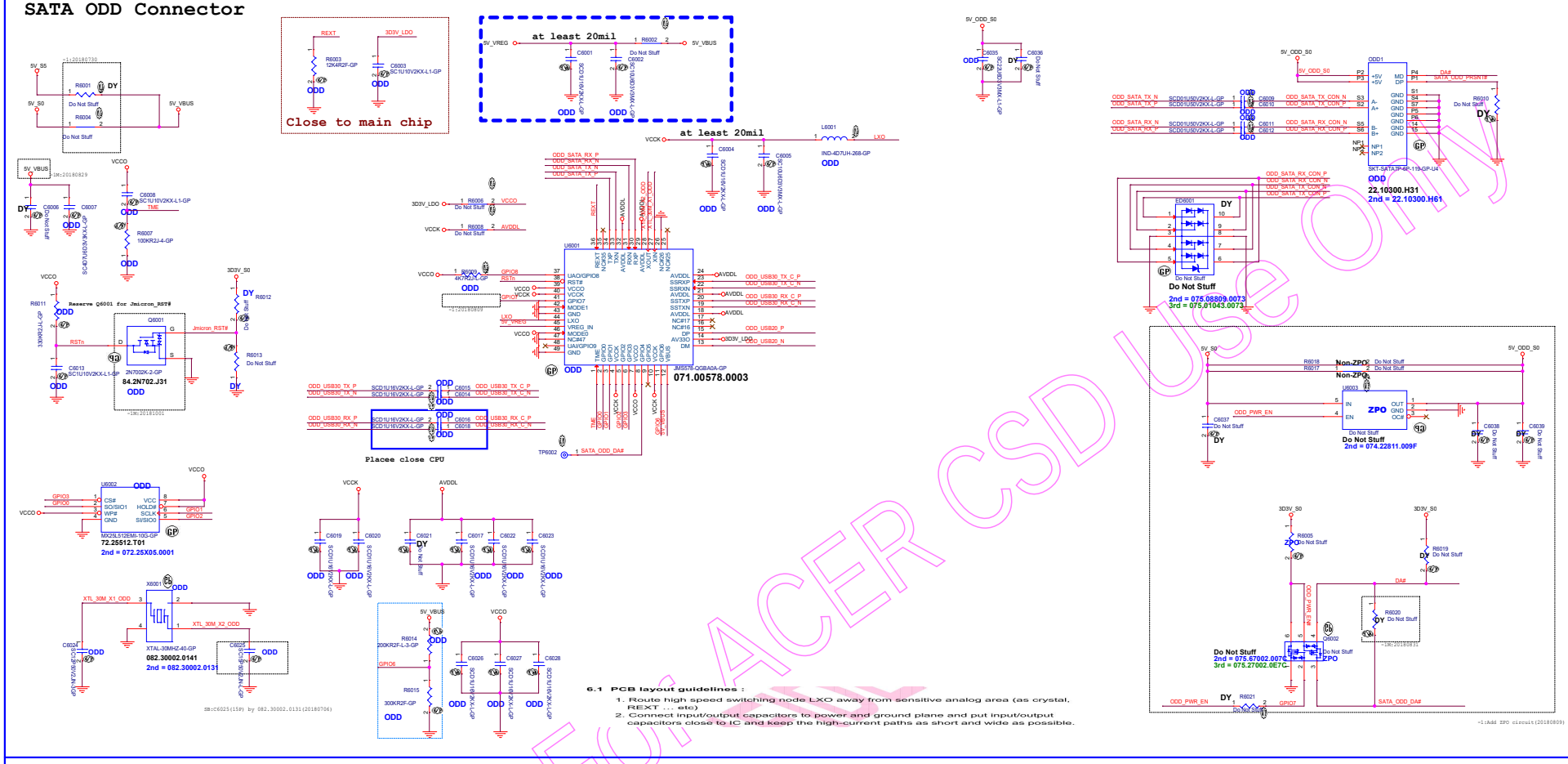
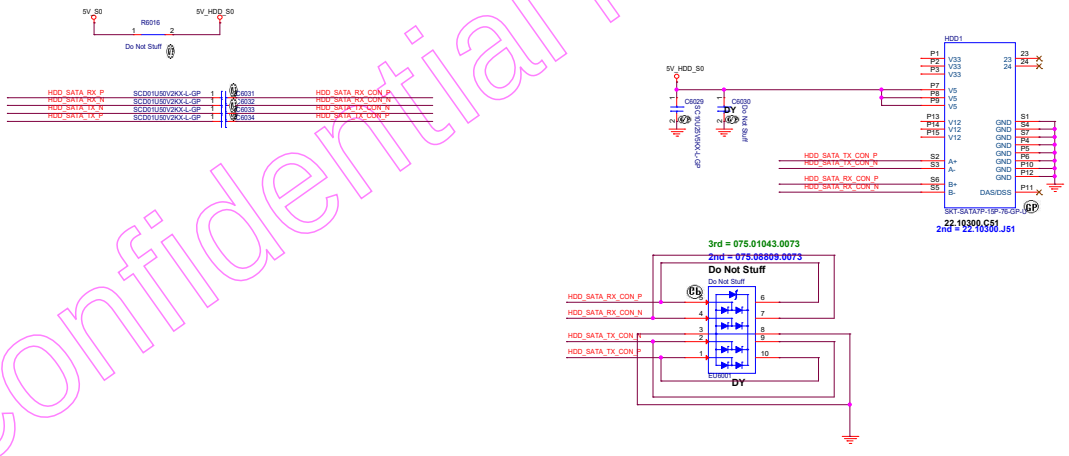
SSID = SATA

# SATA ODD Connector




# SATA HDD Connector






ODD CHA CNVI

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Title: OOD

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**SSID = WLAN**

**CNVI**

17 CNV_RF_RESET#
17 CNV_WR_DN1
17 CNV_WR_DP1
17 CNV_WR_DN0
17 CNV_WR_DP0
17 CNV_WR_CLKP
17 CNV_WR_CLKN
17 CNV_WT_DN1
17 CNV_WT_DP1
17 CNV_WT_DN0
17 CNV_WT_DP0
17 CNV_WT_CLKN
17 CNV_WT_CLKP
17,89 XTAL_CLKREQ
17 CNV_BRI_RSP
17 CNV_RGI_DT_R
17 CNV_RGI_RSP
17 CNV_BRI_DT_R

**BT**

18 BT_USB20_P
18 BT_USB20_N

**WLAN**

18 WLAN_PCIE_TX_P
18 WLAN_PCIE_TX_N
18 WLAN_PCIE_RX_P
18 WLAN_PCIE_RX_N
18 WLAN_CLK_CPU_P
18 WLAN_CLK_CPU_N
18,89 PCIE_WAKE#_CPU
20 WLAN_DET
18 WLAN_CLKREQ_CPU_N

**Other**

24,89 WIFI_RF_EN
24,89 BLUETOOTH_EN
24,68 E51_TXD
19,89 PM_SUSCLK
9,24,31,40,63,68,89,91 PLT_RST#
17 CLKIN_XTAL_LCP
24 WLAN_PERST#
89 WLAN_RST
89 CNV_RF_RESET#_R
89 WLAN_DET_R
89 WLAN_PCIE_TX_P4
89 WLAN_E51_TXD
89 PEG_CLKREQ5_WLAN#

3D3V_S0 — R6103 Non CNVI 0R5J-5-GP — 3D3V_WLAN
R6105 Non CNVI 0R5J-5-GP
3D3V_S5 — R6104 CNVI 0R5J-5-GP
R6106 CNVI 0R5J-5-GP

3D3V_WLAN — C6102 SCD1U16V2KX-L-GP; C6103 SCD1U50V2KX-L-GP; C6104 DY Do Not Stuff; C6105 SC10U6D3V3MX-GP; C6106 DY Do Not Stuff

3D3V_WLAN — RN6102 DY — BLUETOOTH_EN, WIFI_RF_EN — Do Not Stuff

1D8V_S5 — CNV_BRI_DT_R R6102 DY Do Not Stuff
CNV_RGI_DT_R R6127 CNVI 20KR2J-L2-GP

WLAN1 — NP1 / NP2 — SKT-NGFF75P-164-GP

BT
BT_USB20_P
BT_USB20_N

CNVI RX for wifi
CNV_WR_DN1
CNV_WR_DP1
CNV_WR_DN0
CNV_WR_DP0
CNV_WR_CLKN
CNV_WR_CLKP

Decap close to device
Non CNVI
SCD1U16V2KX-L-GP C6111 WLAN_PCIE_TX_P4
SCD1U16V2KX-L-GP C6110 WLAN_PCIE_TX_N4
Non CNVI
WLAN_PCIE_TX_P
WLAN_PCIE_TX_N
WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
PEG_CLKREQ5_WLAN#
PCIE_WAKE#_CPU

CNVI TX for wifi
CNV_WT_DN1
CNV_WT_DP1
CNV_WT_DN0
CNV_WT_DP0
CNV_WT_CLKN
CNV_WT_CLKP

CNVi Companion RF M.2 module

3D3V_WLAN — WLAN_LED#1 — TP6101
CNV_RF_RESET#_R — R6120 Do Not Stuff — CNV_RF_RESET#
XTAL_CLKREQ
WLAN_DET_R — R6134 Do Not Stuff — WLAN_DET
CNV_BRI_RSP_R — R6101 Do Not Stuff — CNV_BRI_RSP
CNV_RGI_DT_R
CNV_RGI_RSP_R — R6107 Do Not Stuff — CNV_RGI_RSP
CNV_BRI_DT_R
WLAN_E51_TXD — G6101 Do Not Stuff — E51_TXD
PM_SUSCLK
WLAN_RST
BLUETOOTH_EN
WIFI_RF_EN
CLKIN_XTAL_LCP

3D3V_WLAN — SB-RF request.(20180704) Closed to pin 72 & 74
C6107 DY; C6108 DY; C6109 DY — Do Not Stuff

062.10003.0B11
Only for PCIE:062.10007.0251
SB-20180725
3rd = 62.10043.I91

PLT_RST# — R6133 Do Not Stuff — WLAN_RST
WLAN_PERST# — R6132 DY Do Not Stuff

3D3V_WLAN — R6110 100KR2J-4-GP — PCIE_WAKE#_CPU
PEG_CLKREQ5_WLAN# — R6109 Do Not Stuff — WLAN_CLKREQ_CPU_N

XTAL_CLKREQ — Intel suggestion — R6126 Do Not Stuff DY

WIFI_RF_EN — EMI Request
WLAN_RST
ED6101 Do Not Stuff DY
Do Not Stuff
2nd = 075.00353.0A7D

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Title: INT IO (WLAN M.2)
Size: Custom | Document Number: Raichu_GL | Rev: -1M
Date: Monday, October 01, 2018 | Sheet 61 of 106

# Blanking



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Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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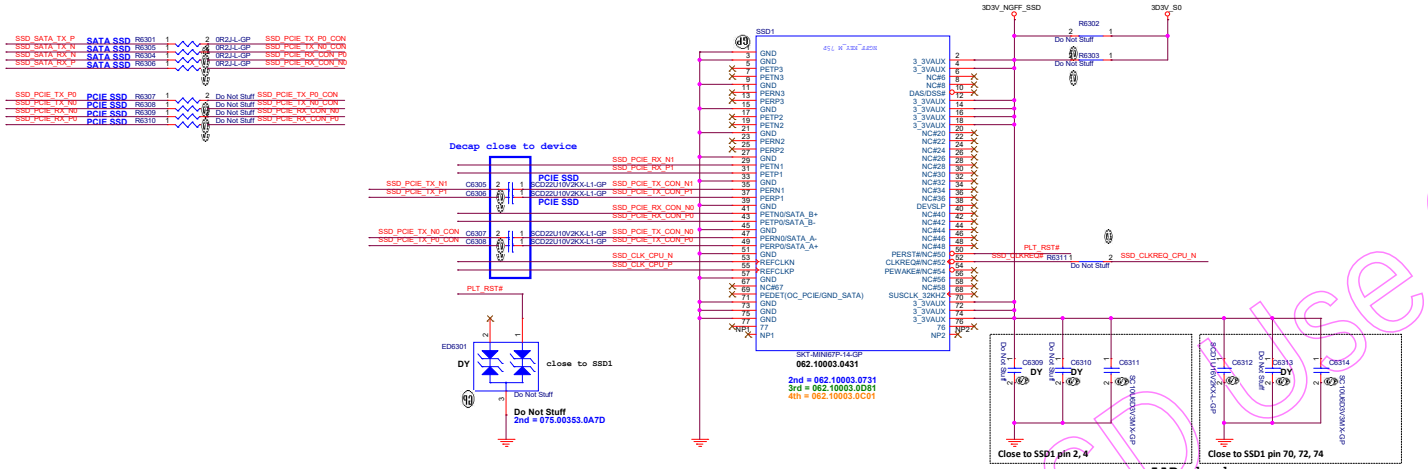
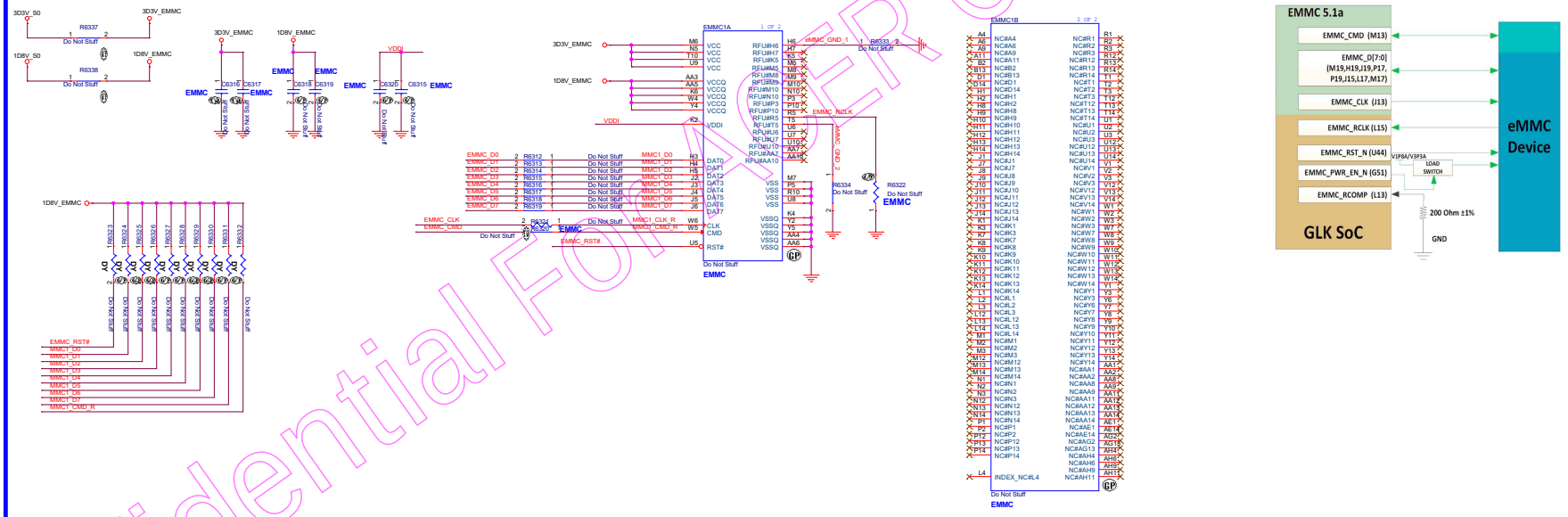
**Main Func = SSD**

# TYPE-M NGFF CARD FOR PCIE/SATA SSD




**SSID = eMMC**



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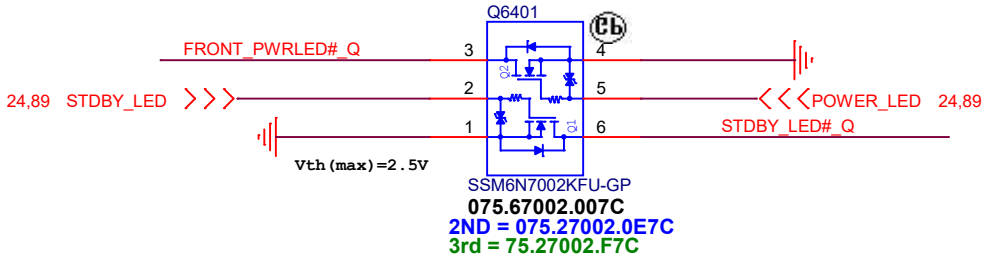
Title: INT IO (SSD M.2/ eMMC)

| Size | Document Number | Rev |
|---|---|---|
| Custom | Raichu_GL | -1M |

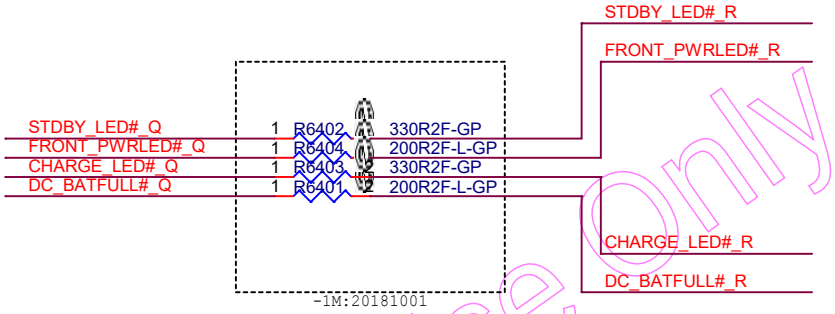
Date: Monday, October 01, 2018 Sheet 83 of 106

# Power button LED

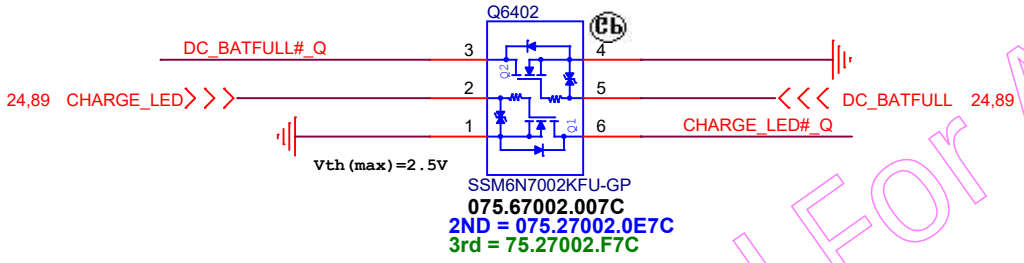



075.67002.007C
2ND = 075.27002.0E7C
3rd = 75.27002.F7C

# Power STDBY_LED

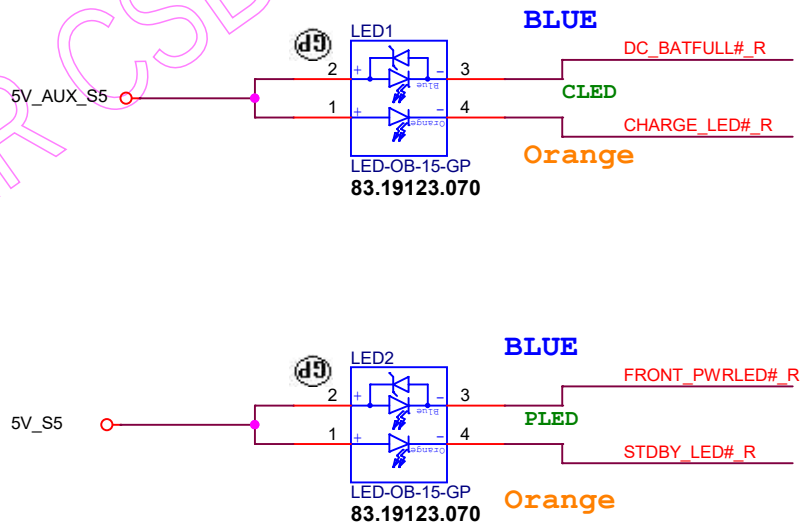



# Battery LED2(DC_BATFULL)




075.67002.007C
2ND = 075.27002.0E7C
3rd = 75.27002.F7C

# Battery LED1(CHARGE)



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Title: ***LED / Button / Power Button***

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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**SSID = KBC**

## *Internal KeyBoard Connector*

24,89 KBC_PWRBTN#
24,89 KSI[0..7]
24,89 KSO[0..17]

17 CPU_I2C_SCL_P4
17 CPU_I2C_SDA_P4

24 EC_TP_CLK
24 EC_TP_DATA
89 CPU_I2C_SDA_TP
89 CPU_I2C_SCL_TP

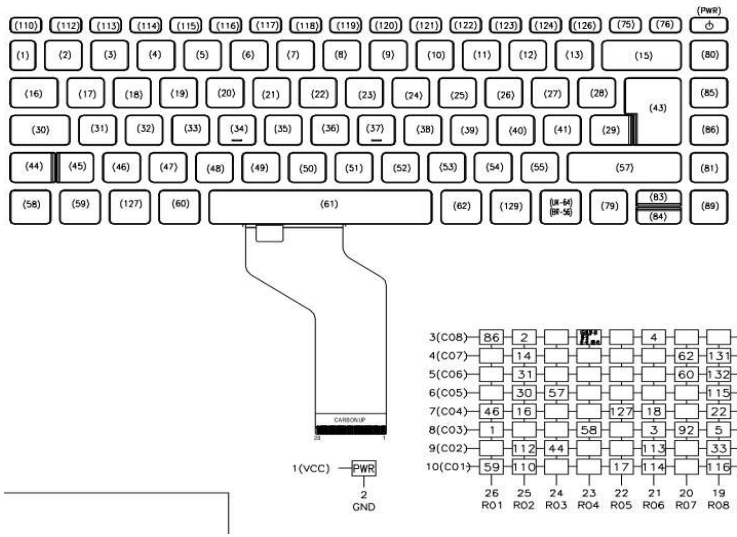
89 EC_TP_CLK_C
89 EC_TP_DATA_C

89 TP_IN#_R
24,89 TP_FUN_OFF#

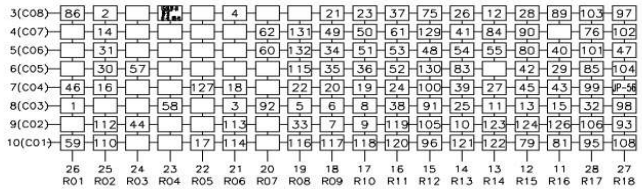
20 TP_IN#_CPU

24 EC_TP_IN#

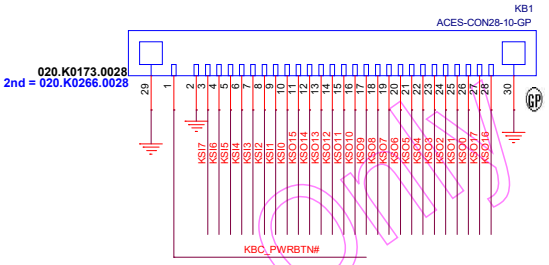
24 PTP_PWR_EN

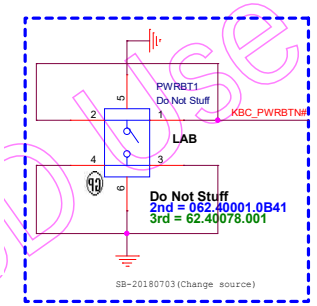


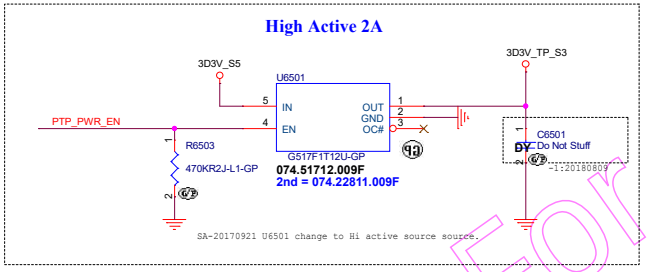

| | 14" |
|---|---|
| 1 | POWER(VCC) |
| 2 | POWER(GND) |
| 3 | CO8 |
| 4 | CO7 |
| 5 | CO6 |
| 6 | CO5 |
| 7 | CO4 |
| 8 | CO3 |
| 9 | CO2 |
| 10 | CO1 |
| 11 | RI6 |
| 12 | RI5 |
| 13 | RI4 |
| 14 | RI3 |
| 15 | RI2 |
| 16 | RI1 |
| 17 | RI0 |
| 18 | RO9 |
| 19 | RO8 |
| 20 | RO7 |
| 21 | RO6 |
| 22 | RO5 |
| 23 | RO4 |
| 24 | RO3 |
| 25 | RO2 |
| 26 | RO1 |
| 27 | RI8 |
| 28 | RI7 |

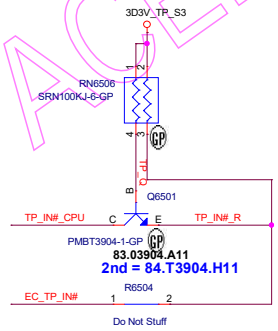


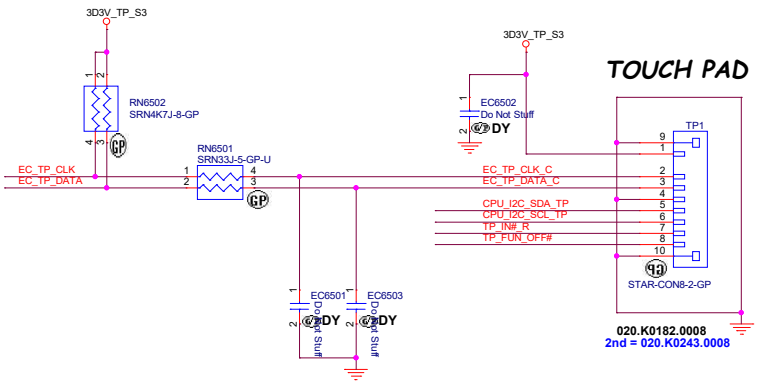

KB1 source
配合Keyboard(CARBON UP)改為抽屜式connector(金手指上接觸)



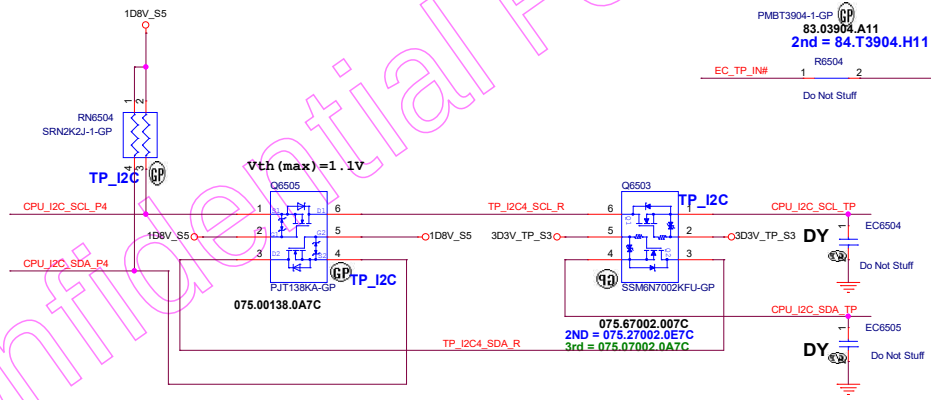



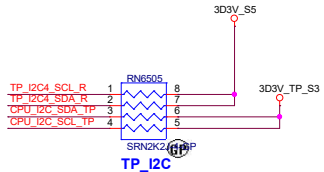




## TOUCH PAD

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| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | **Key Board/Touch Pad** | |
| Size: Custom | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 65 of 106 | |

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|---|---|---|
| Title | ***Reserved*** | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
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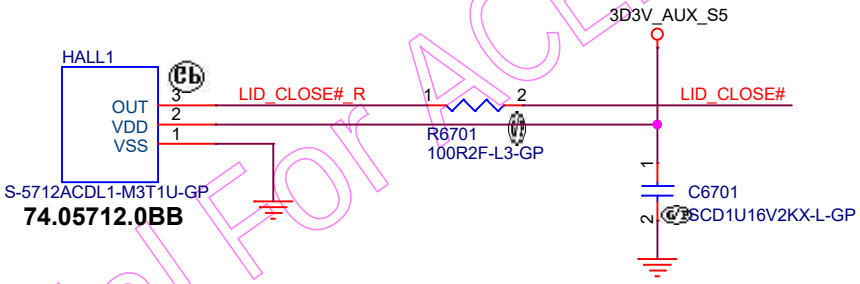
24,89 LID_CLOSE#





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Title: ***Sensor (Hall-Sensor)***

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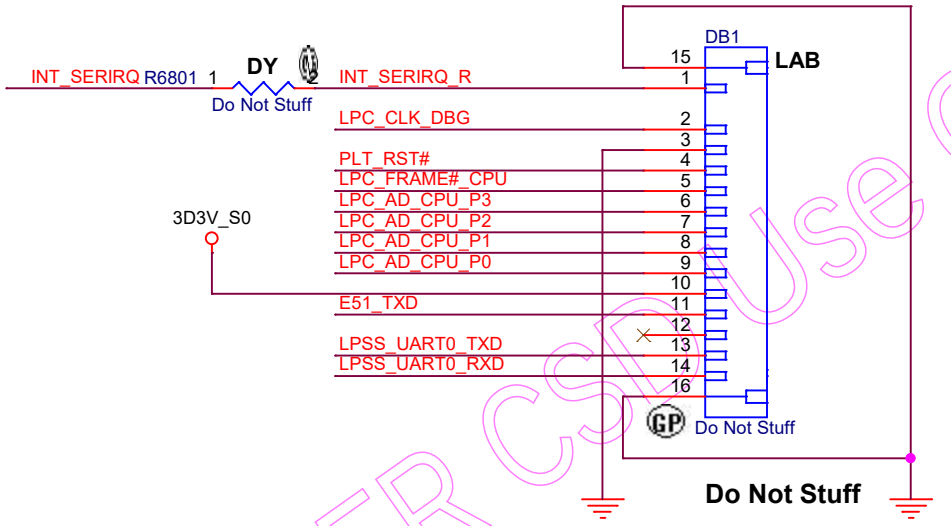
16,24 INT_SERIRQ
16 LPC_CLK_DBG
9,24,31,40,61,63,89,91 PLT_RST#
16,24 LPC_FRAME#_CPU
16,24 LPC_AD_CPU_P3
16,24 LPC_AD_CPU_P2
16,24 LPC_AD_CPU_P1
16,24 LPC_AD_CPU_P0
24,61 E51_TXD
17 LPSS_UART0_TXD
17 LPSS_UART0_RXD



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Title: ***Debug(LPC connector)***

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Title: *G Sensor (Reserved)*

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Title: *(Reserved)*

| Size | Document Number | Rev |
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|---|---|---|
| Title | ***Reserved*** | |
| Size A4 | Document Number **Raichu_GL** | Rev **-1M** |
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Title: ***Reserved***

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Title: *Reserved*

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Title: *(Reserved)*

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Title

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| | | |
|---|---|---|
| Title | GPU (1/5) PEG | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
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| | | |
|---|---|---|
| Title | GPU (2/5) DIGITAL | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
| Date: Monday, October 01, 2018 | Sheet 77 of 106 | |

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| | | |
|---|---|---|
| Title | GPU (3/5) VRAM | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
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Title: GPU (4/5) GPIO

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Title: GPU (5/5) PWR/GND

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Title: *VRAM1,2 (1/4)*

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| | | |
|---|---|---|
| Title | *VRAM3,4 (2/4)* | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
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| | | |
|---|---|---|
| Title | *VRAM5,6 (3/4)* | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
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| | | |
|---|---|---|
| Title | *VRAM7,8 (4/4)* | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
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| | | |
|---|---|---|
| Title | VGA_CORE | |
| Size: A4 | Document Number: Raichu_GL | Rev: -1M |
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Title: DISCRETE VGAPOWER

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|---|---|---|
| A4 | Raichu_GL | -1M |

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Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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Title: *(Reserved)*

| Size | Document Number | Rev |
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| A4 | Raichu_GL | -1M |

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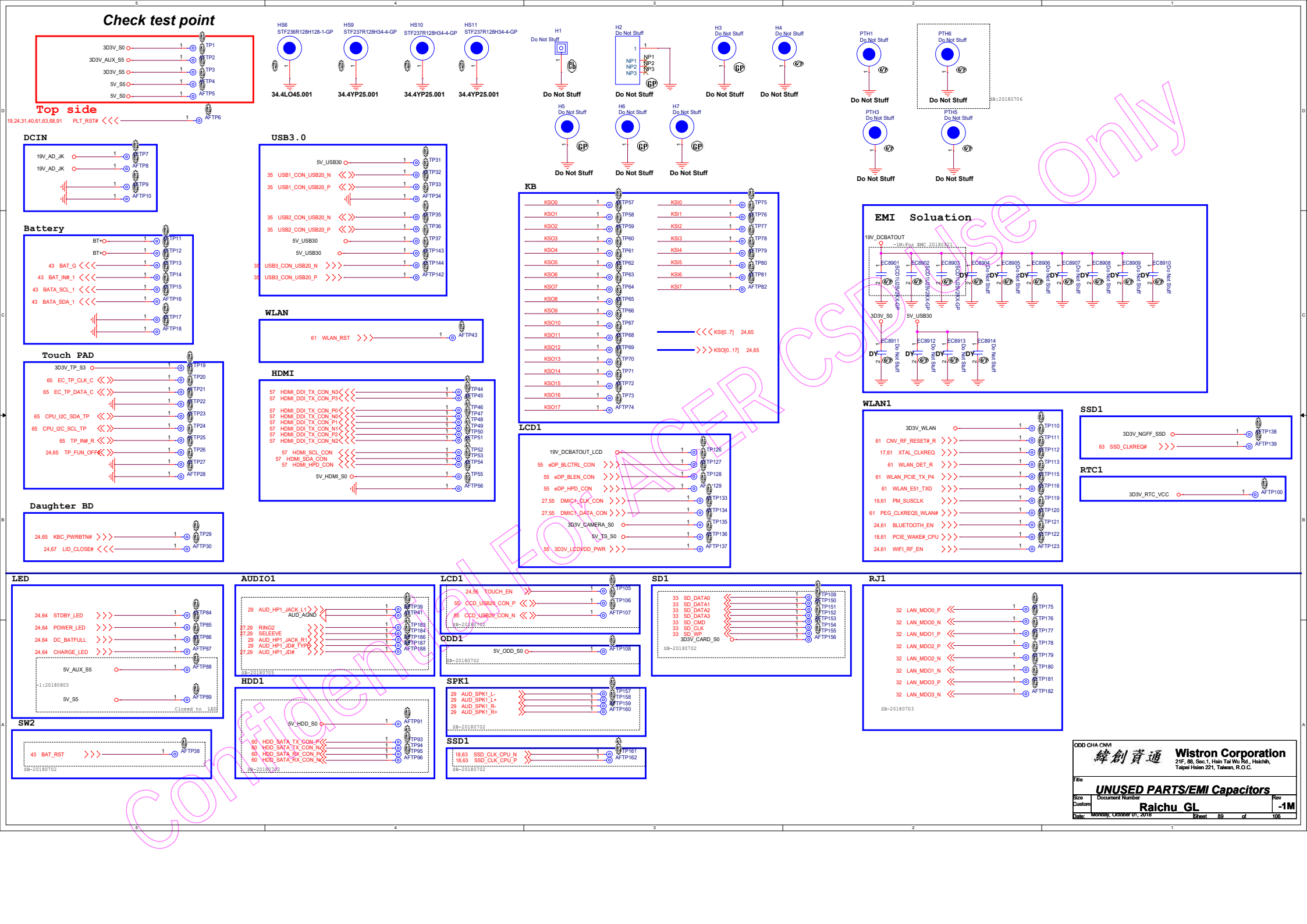
Check test point
Top side
3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
5V_S0
PLT_RST#
DCIN
Battery
Touch PAD
Daughter BD
USB3.0
WLAN
HDMI
KB
LCD1
EMI Soluation
WLAN1
SSD1
RTC1
LED
SW2
AUDIO1
HDD1
ODD1
SPK1
SD1
RJ1
Do Not Stuff
Confidential LOACER Use Only
Wistron Corporation
Raichu_GL
UNUSED PARTS/EMI Capacitors
-1M

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Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | Raichu_GL | -1M |

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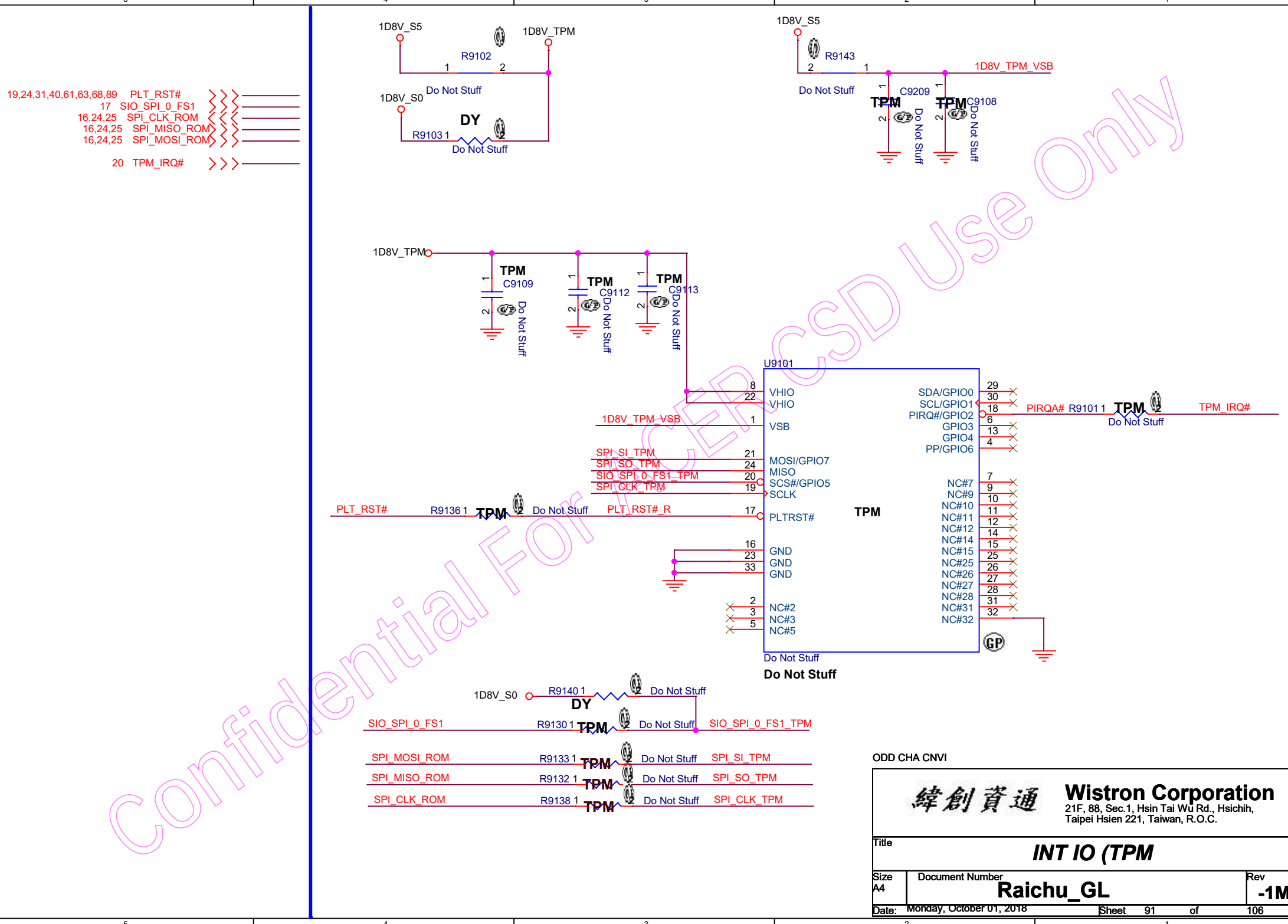




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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: INT IO (TPM

| Size | Document Number | Rev |
|---|---|---|
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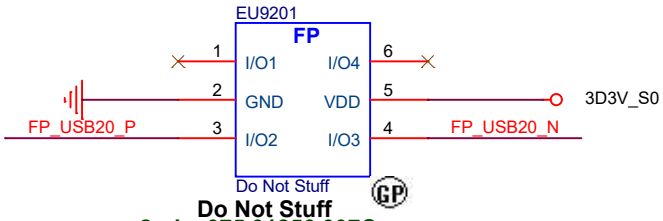
18 FP_USB20_P
18 FP_USB20_N

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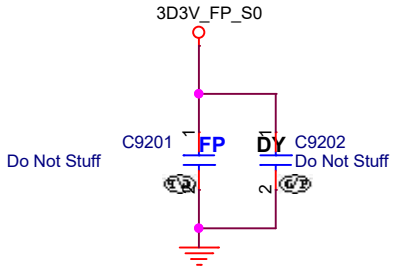


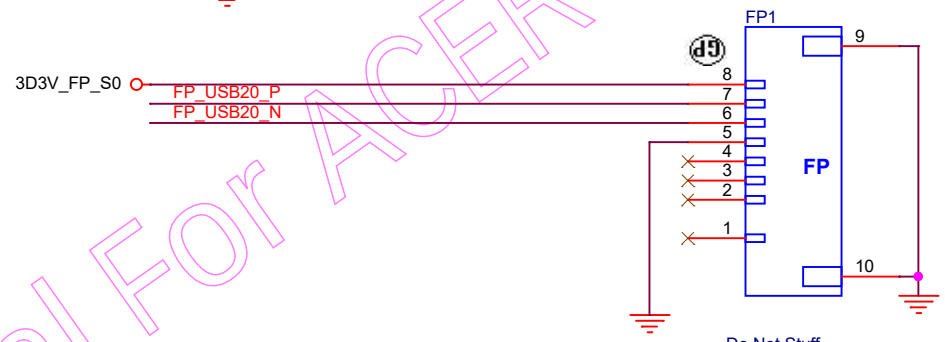


Do Not Stuff
Do Not Stuff
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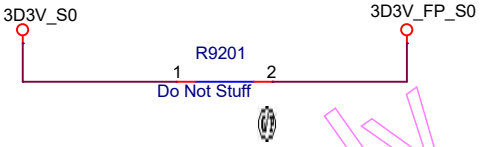






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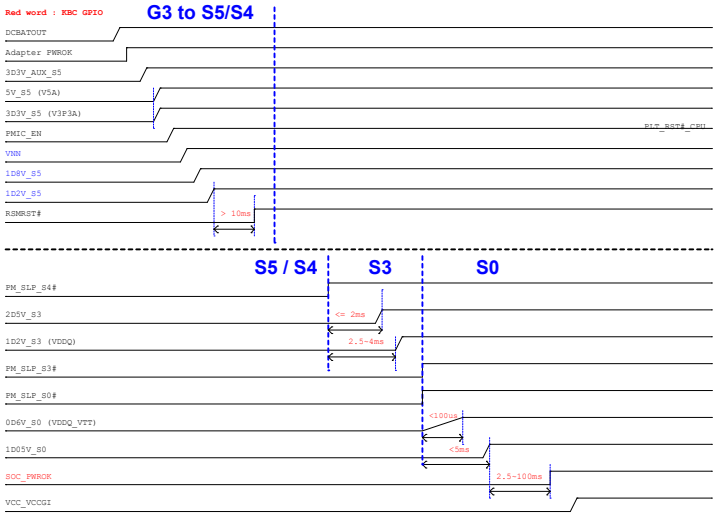
# Intel-Power Up Sequence

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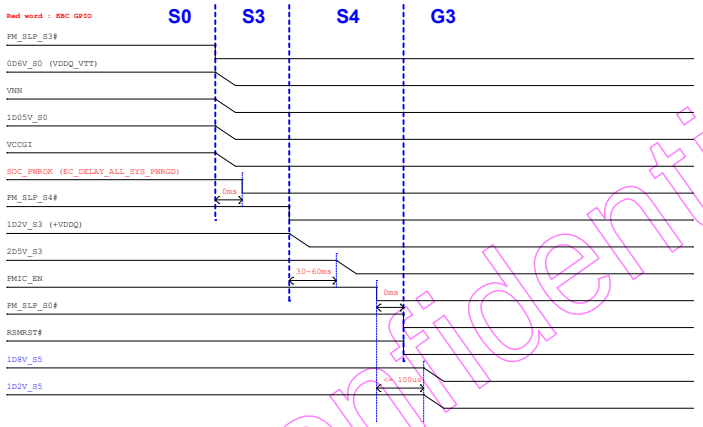
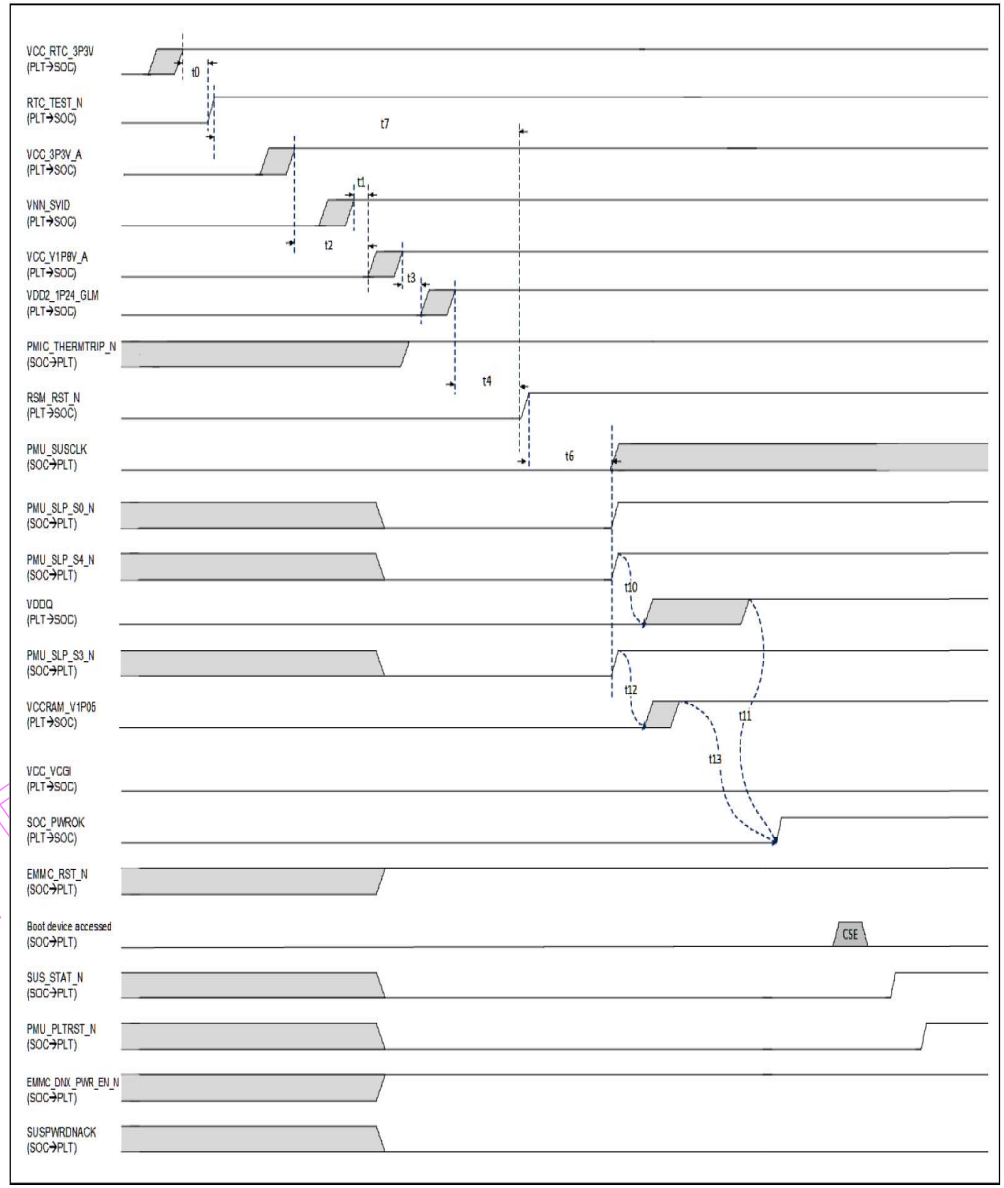



# Gemini Lake Sequence

## Gemini Lake G3 Cold Boot Power-Up








ODD CHA CAN4

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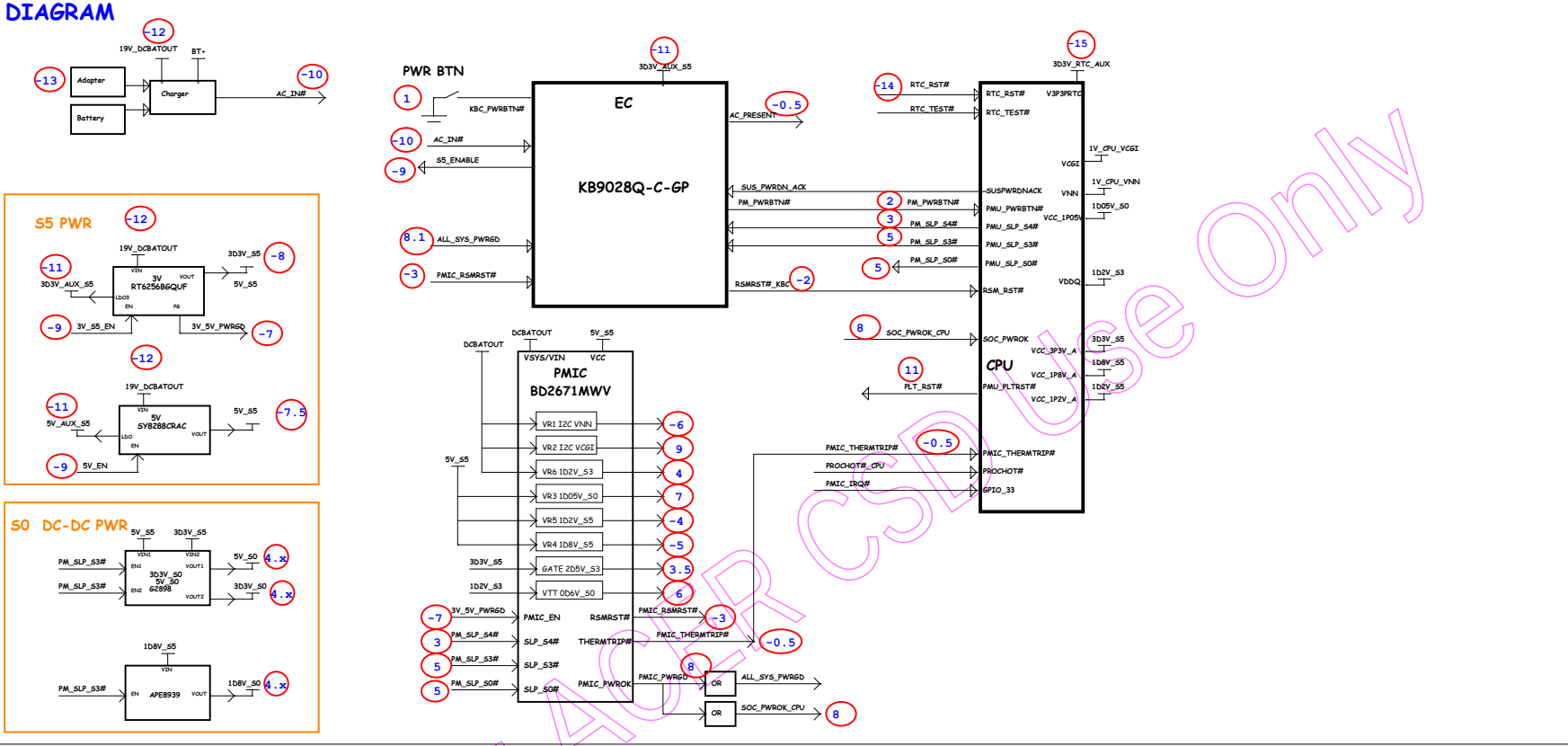
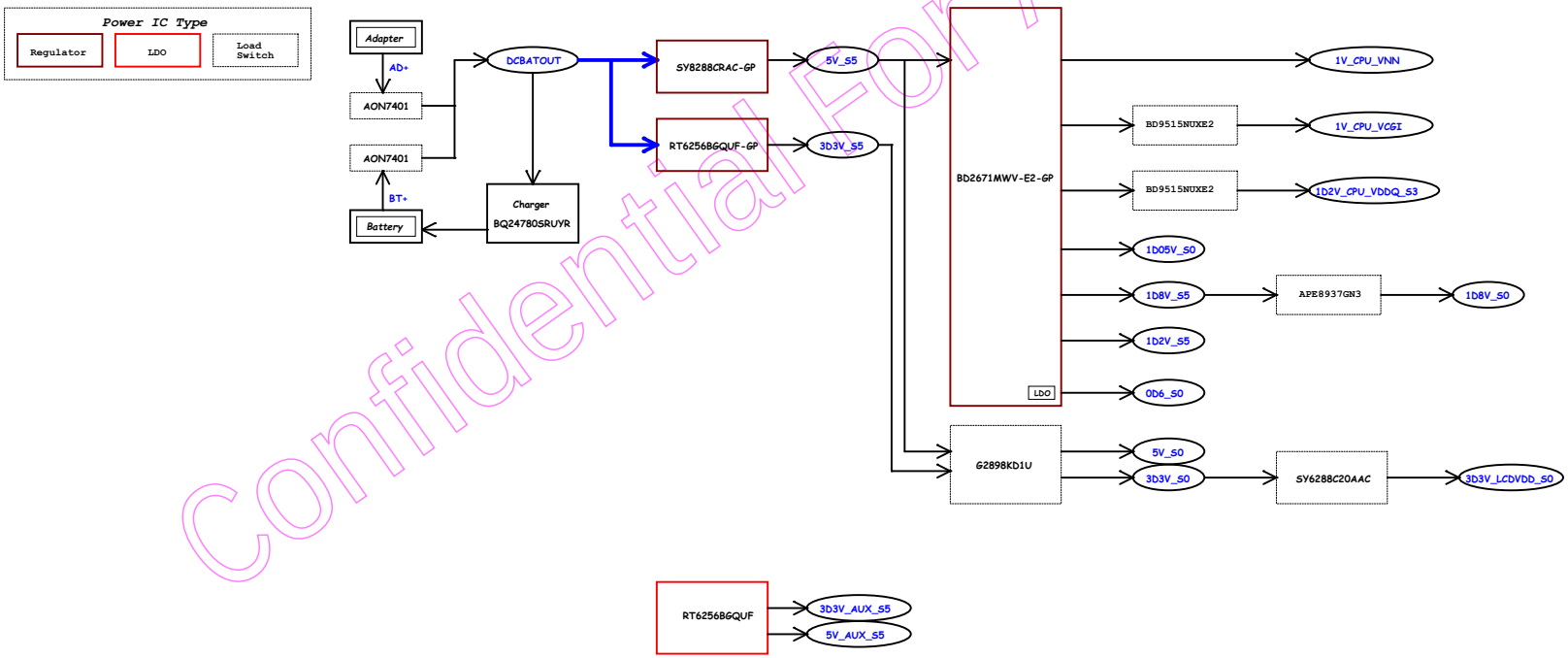
# Gemini LAKE SEQUENCE & BLOCK DIAGRAM



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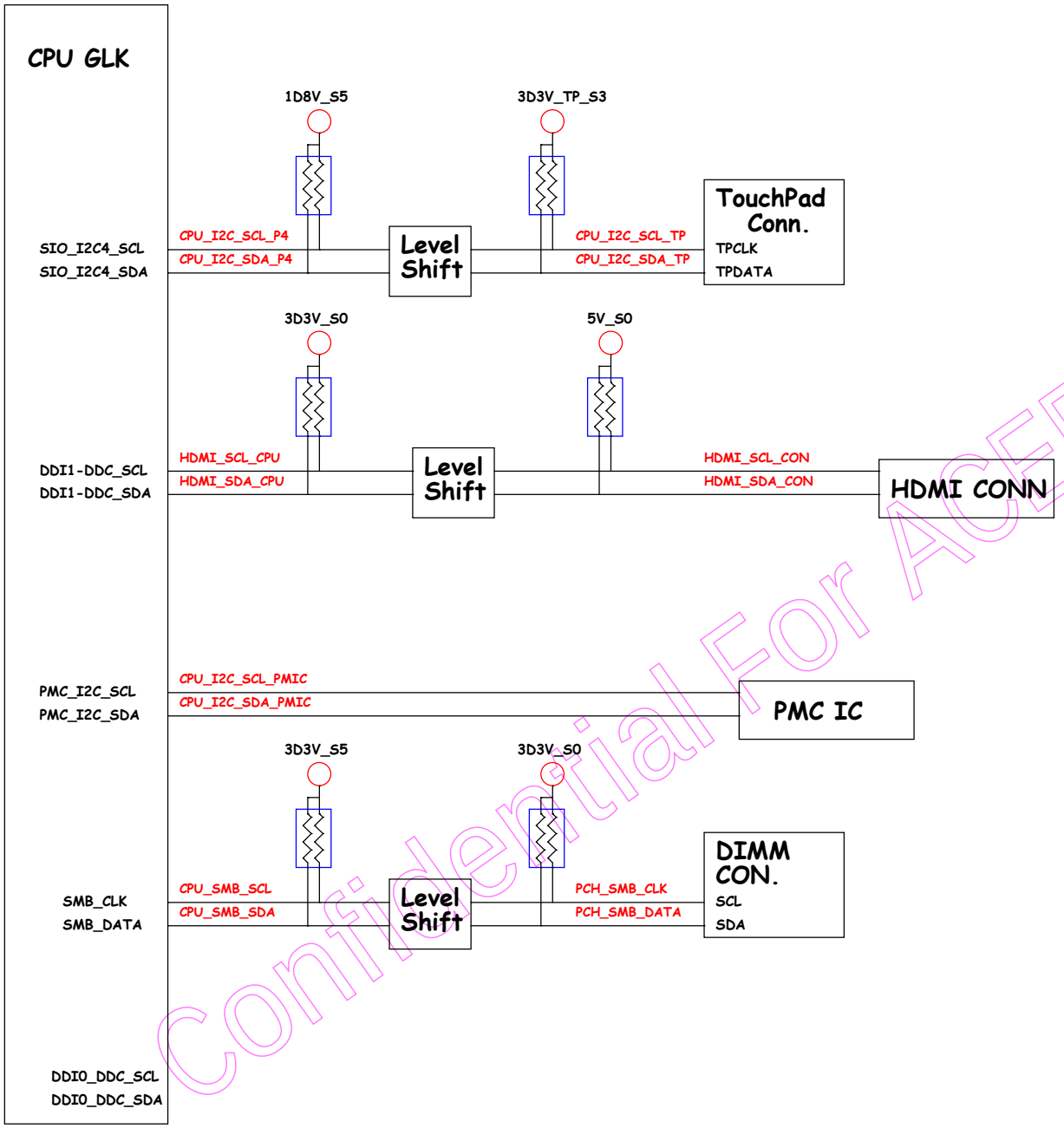
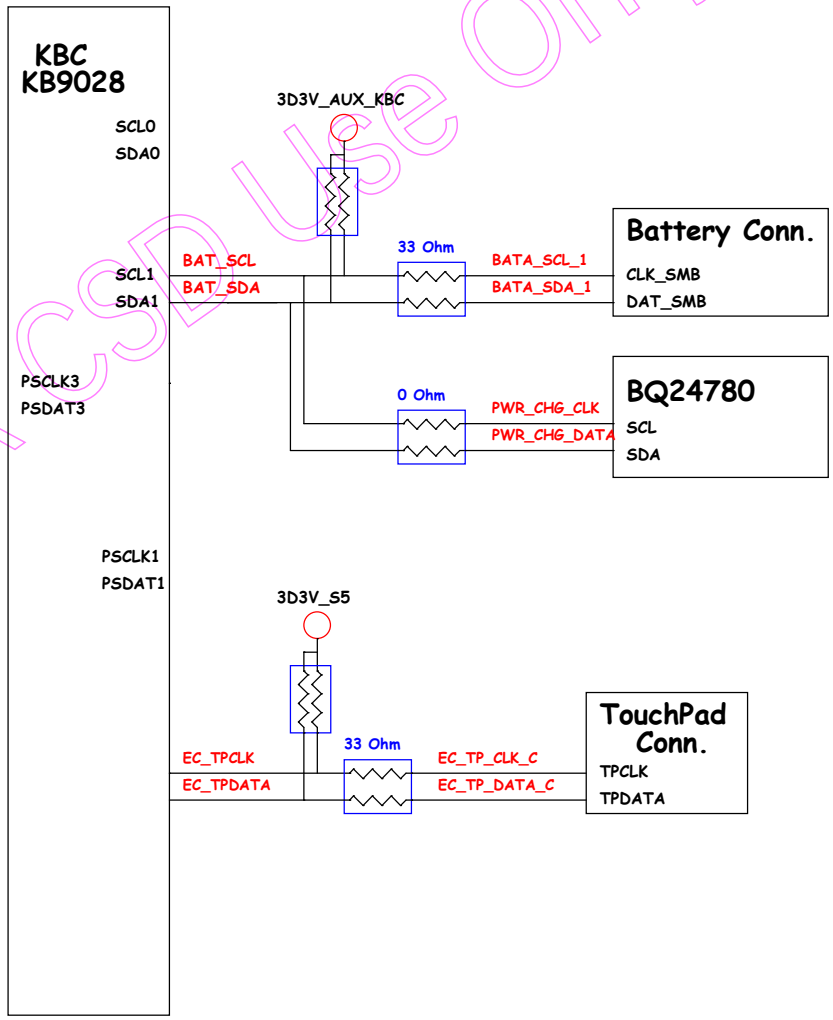
# PCH SMBus Block Diagram




# KBC SMBus Block Diagram



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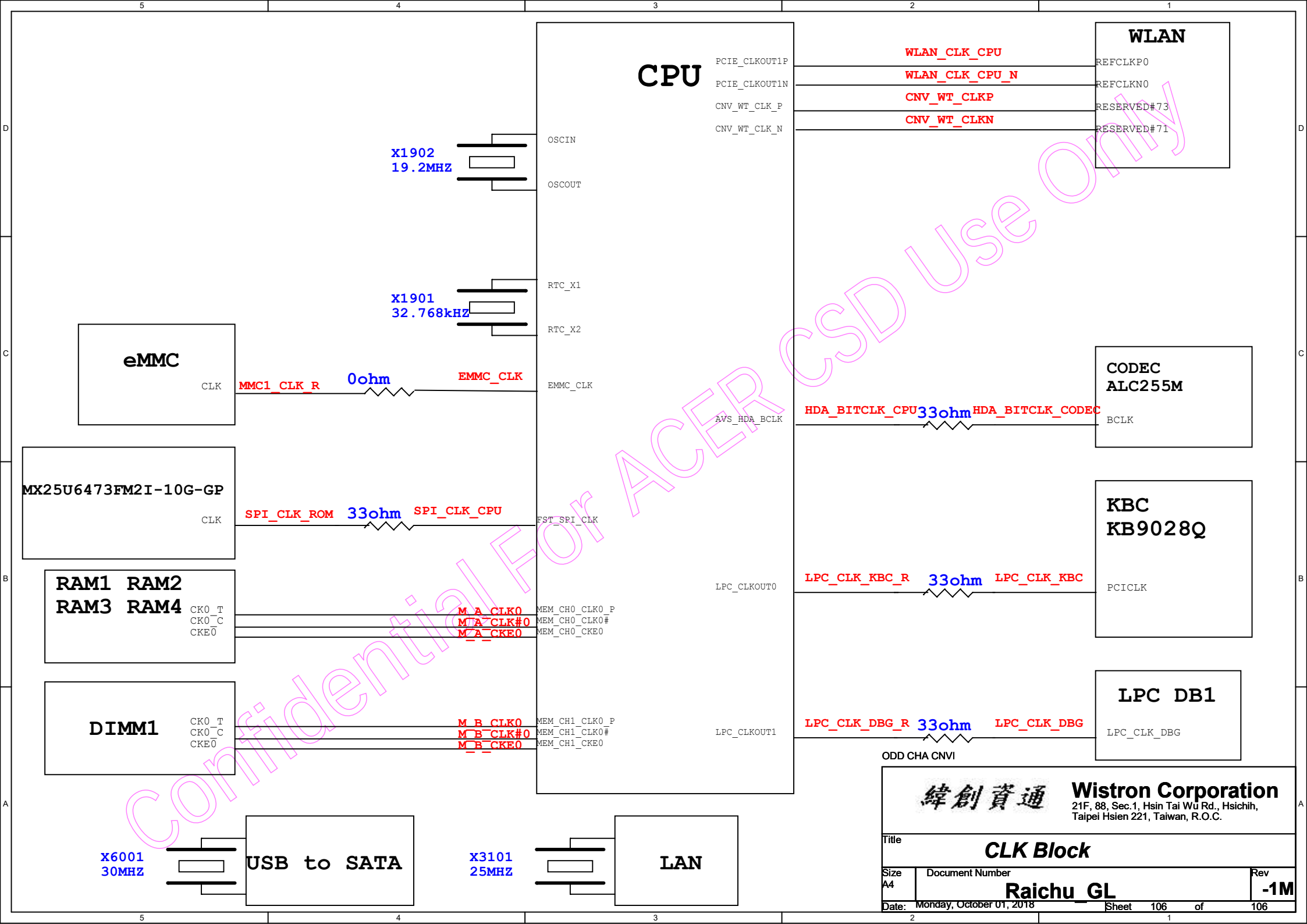




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