1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-10-12

SCHEM,FLYING_DUTCHMAN,MLB,K91F

REV B RELEASE, 01/31/11

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8620	1	SCHEM,MLB,K91	SCH	CRITICAL	
820-2915	1	PCBF,MLB,K91	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Jan 31 12:49:37 2011

DRAWING TITLE: SCHEM,MLB,K91

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

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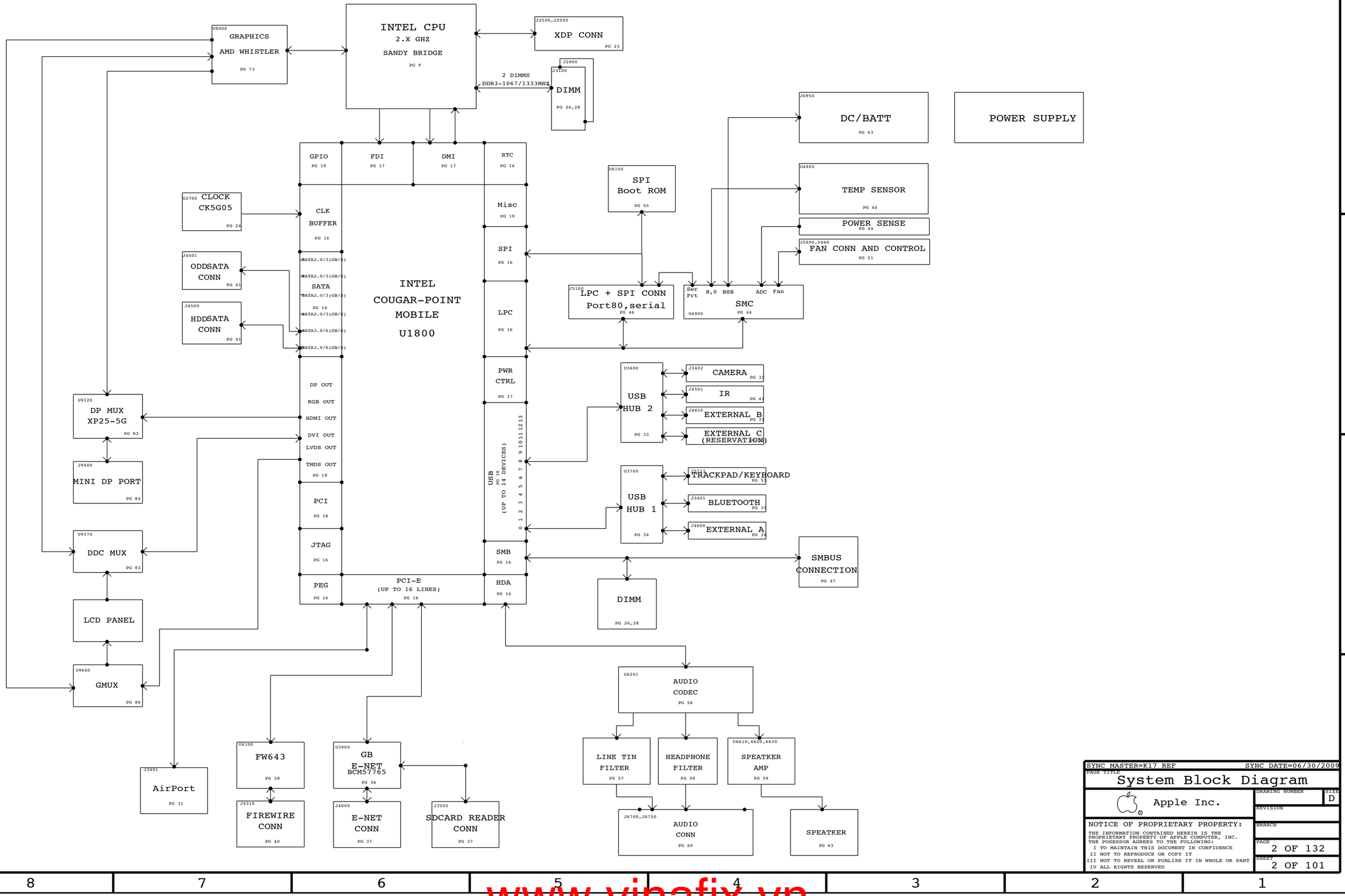

SYNC MASTER=K17 REF SYNC DATE=06/30/2009

PAGE TITLE

System Block Diagram

Apple Inc.

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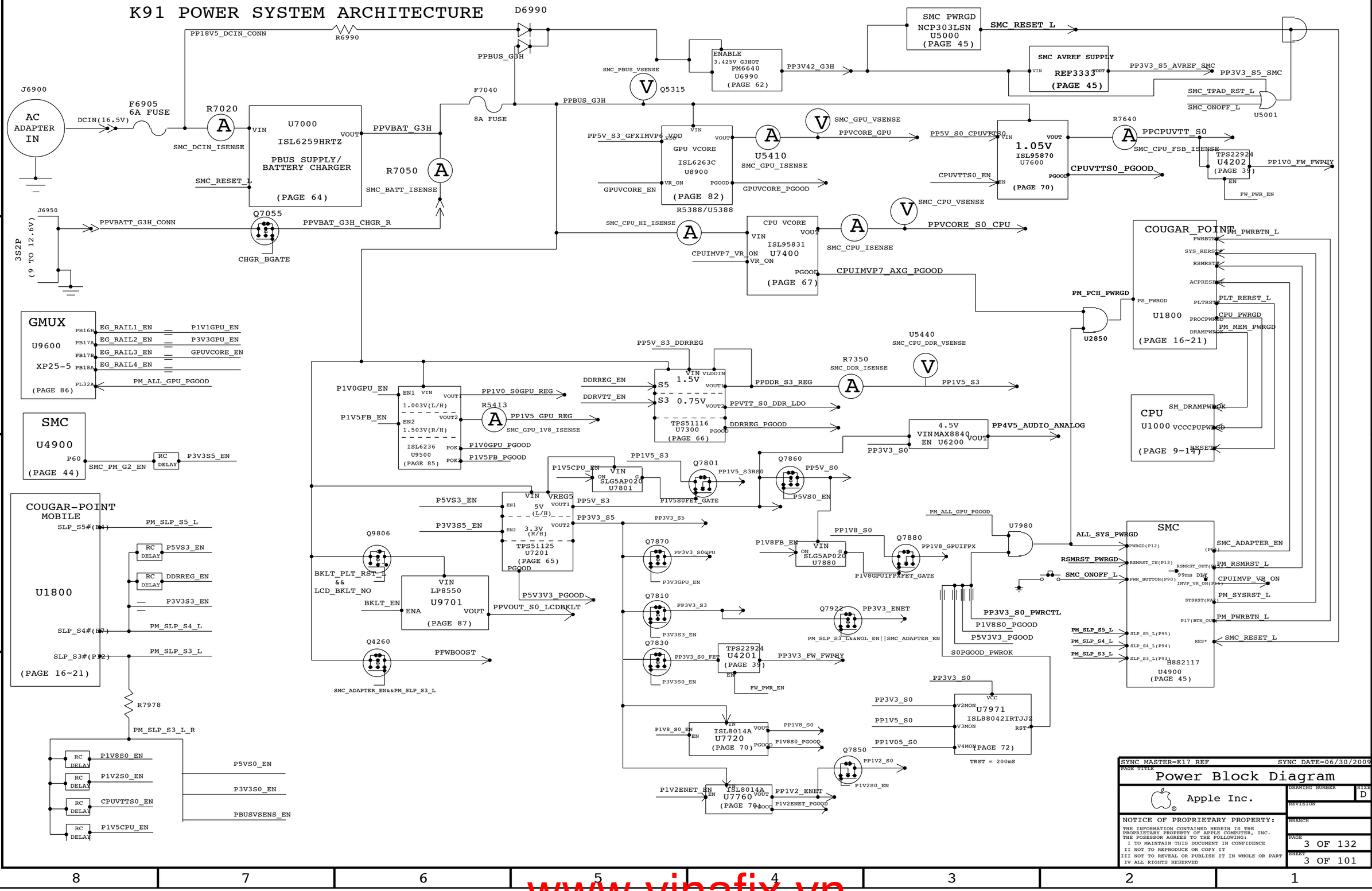
K91 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE: Power Block Diagram

Apple Inc.

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Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1468	PCBA,MLB,K91F,DG64	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG64
639-1972	PCBA,MLB,K91F,DL83	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL83
639-1971	PCBA,MLB,K91F,DL82	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL82
639-1469	PCBA,MLB,K91F,DG65	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG65
639-1970	PCBA,MLB,K91F,DL86	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL86
639-1956	PCBA,MLB,K91F,DL7W	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7W
639-1470	PCBA,MLB,K91F,DG66	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG66
639-1974	PCBA,MLB,K91F,DL87	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL87
639-1976	PCBA,MLB,K91F,DL88	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL88
639-1471	PCBA,MLB,K91F,DG67	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG67
639-1973	PCBA,MLB,K91F,DL81	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL81
639-1954	PCBA,MLB,K91F,DL7T	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7T
639-1573	PCBA,MLB,K91,DHMV	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DHMV
639-1945	PCBA,MLB,K91,DL7Q	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7Q
639-1953	PCBA,MLB,K91,DL7R	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7R
639-1574	PCBA,MLB,K91,DHMW	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DHMW
639-1959	PCBA,MLB,K91,DL80	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL80
639-1960	PCBA,MLB,K91,DL7Y	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL7Y
085-1901	K91/K91F DEVELOPMENT BOM	K91_DEVEL:ENG

K91 BOM GROUPS

BOM GROUP	BOM OPTIONS
K91_COMMON	ALTERNATE,COMMON,K91_COMMON1,K91_COMMON2,K91_PROGPARTS,K91_PROGPARTS1,UVGLUE_K91_K91F,K91_PVT
K91_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_2NONREM,USBHUB_2513B
K91_COMMON2	GPUVID_1P11V,KB_BL,T29:YES,ENET_SD:B0,T29BST:Y,SDRV_PD,SDRVI2C:MCU,T29_DP_HPD:ALL_OR
K91_PVT	BMON:PROD,VREFMRGN_NOT,XDP,XDP_CPU_BPM,BKLT:PROD,ISNS_ON:NO,LPCPLUS_R:YES
K91_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:PVT,ENETROM_PROG:PVT,T29ROM:PROG,T29MCU:PROG
K91_PROGPARTS1	SMC_PROG:PVT,BOOTROM_PROG:PVT
K91_DEVEL:ENG	SNB_CPT_XDP,BMON:ENG,GMUX_JTAG_CONN,VREFMRGN,LPCPLUS_CONN:YES,LPCPLUS_R:YES,BKLT:ENG,80PGOOD_ISL,CPURIPPLE_ENG,IMVPISNS_ENG,ISNS_ON:YES,DEBUG_ADC,DIGI_MIC
K91_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS_CONN:YES,LPCPLUS_R:YES
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4031	1	IC,CPU,SNB,SR030,PRQ,D2,2.0,45W,4+2,1.20,6M,BGA	U1000	CRITICAL	CPU:2_0GHZ
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ,D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	GPU:WHISTLER
337S3979	1	IC,GPU,AMD,SEYMOUR,M2 LP,ES1,962BGA	U8000	CRITICAL	GPU:SEYMOUR
338S0945	1	IC,ASSP,LIGHTRIDGE,S LHAJ,PRQ,FCBGA,15X15MM	U3600	CRITICAL	T29:YES
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,B0	U3900	CRITICAL	ENET_SD:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,A0	U3900	CRITICAL	ENET_SD:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32:1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
333S0543	2	IC,SGRAM,GDDR5,32MX32:1.25GHz,E-DIE,HF	U8500,U8550	CRITICAL	FB_256_SAMSUNG
333S0564	2	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8500,U8550	CRITICAL	FB_256_HYNIX
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
725-1479	1	MLB LOCTITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_K91_K91F	CRITICAL	UVGLUE_K91_K91F
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET,1MBITFLASH,C1V REV01,K74/K75,K40	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S2973	1	IC,ENET,1MBITFLASH,C1V REV01,K60/K62	U3990	CRITICAL	ENETROM_PROG:B0_SD
341S3026	1	IC,ENET,1MBITFLASH,C1V REV01,K90i/K91/K92	U3990	CRITICAL	ENETROM_PROG:EVT
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K90i/K91x	U3990	CRITICAL	ENETROM_PROG:PVT

Alternate Parts

(Alternate) (Primary)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	ROHM alt to Toshiba N-FET
376S0855	376S0613		ALL	Diodes alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt for Samsung
152S0685	152S0796		ALL	Vishay/TSM alt for Cystec
376S0977	376S0859		ALL	Diodes alt for Rohm
353S2592	353S3199		ALL	Unity source needs via GND in schematic for EMI EMC
335S0550	335S0777		ALL	add 4K byte as alternative to 2K
371S0679	371S0652		ALL	EXP alternate for pin diodes
138S0671	138S0673		ALL	Taiyo Yuden alt for Murata 10 uF caps

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO0, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO2, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

PSOC

341S2902	1	IC,TP PSOC,K9x,PROTO0	U5701	CRITICAL	TPAD_PROG:PROTO0
341S2940	1	IC,TP PSOC,K9x,PROTO1	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3001	1	IC,TP PSOC,K9x,PROTO2	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,K9x,EVT	U5701	CRITICAL	TPAD_PROG:EVT
341S3099	1	IC,TP PSOC,K9x,DVT,PVT	U5701	CRITICAL	TPAD_PROG:PVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DDKG]	CRITICAL	EEEE:DDKG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG63]	CRITICAL	EEEE:DG63
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG64]	CRITICAL	EEEE:DG64
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG65]	CRITICAL	EEEE:DG65
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG66]	CRITICAL	EEEE:DG66
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG67]	CRITICAL	EEEE:DG67
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMV]	CRITICAL	EEEE:DHMV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMW]	CRITICAL	EEEE:DHMW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL81]	CRITICAL	EEEE:DL81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL82]	CRITICAL	EEEE:DL82
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL83]	CRITICAL	EEEE:DL83
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL84]	CRITICAL	EEEE:DL84
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL85]	CRITICAL	EEEE:DL85
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL86]	CRITICAL	EEEE:DL86
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL87]	CRITICAL	EEEE:DL87
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL88]	CRITICAL	EEEE:DL88
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL89]	CRITICAL	EEEE:DL89
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Q]	CRITICAL	EEEE:DL7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7R]	CRITICAL	EEEE:DL7R
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7T]	CRITICAL	EEEE:DL7T
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7V]	CRITICAL	EEEE:DL7V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7W]	CRITICAL	EEEE:DL7W
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Y]	CRITICAL	EEEE:DL7Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL80]	CRITICAL	EEEE:DL80

Programmables - All Builds

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,CY7C63833-LFXC	U4800	CRITICAL	IR_PROG
341S3129	1	IC,T29 EEPROM,PVT,K9x	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3128	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,PVT,HVQFN25	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92,PROG	U8701	CRITICAL	GPUROM:PROG
335S0724	1	IC,GPU ROM,K91/F,K92,BLANK	U8701	CRITICAL	GPUROM:BLANK

SMC

338S0895	1	IC,SMC,HSB/2117,90MX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2854	1	IC,SMC,DEVELOPMENT-PROTO0,K91	U4900	CRITICAL	SMC_PROG:PROTO0
341S2935	1	IC,SMC,DEVELOPMENT-PROTO1,K91	U4900	CRITICAL	SMC_PROG:PROTO1
341S2994	1	IC,SMC,DEVELOPMENT-PROTO2,K91	U4900	CRITICAL	SMC_PROG:PROTO2
341S2861	1	IC,SMC,DEVELOPMENT-EVT,K91	U4900	CRITICAL	SMC_PROG:EVT
341S2864	1	IC,SMC,DEVELOPMENT-DVT,K91	U4900	CRITICAL	SMC_PROG:DVT
341S2867	1	IC,SMC,DEVELOPMENT-PVT,K91	U4900	CRITICAL	SMC_PROG:PVT

SYNC MASTER=K17 REF SYNC DATE=05/28/2009

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BOM Configuration

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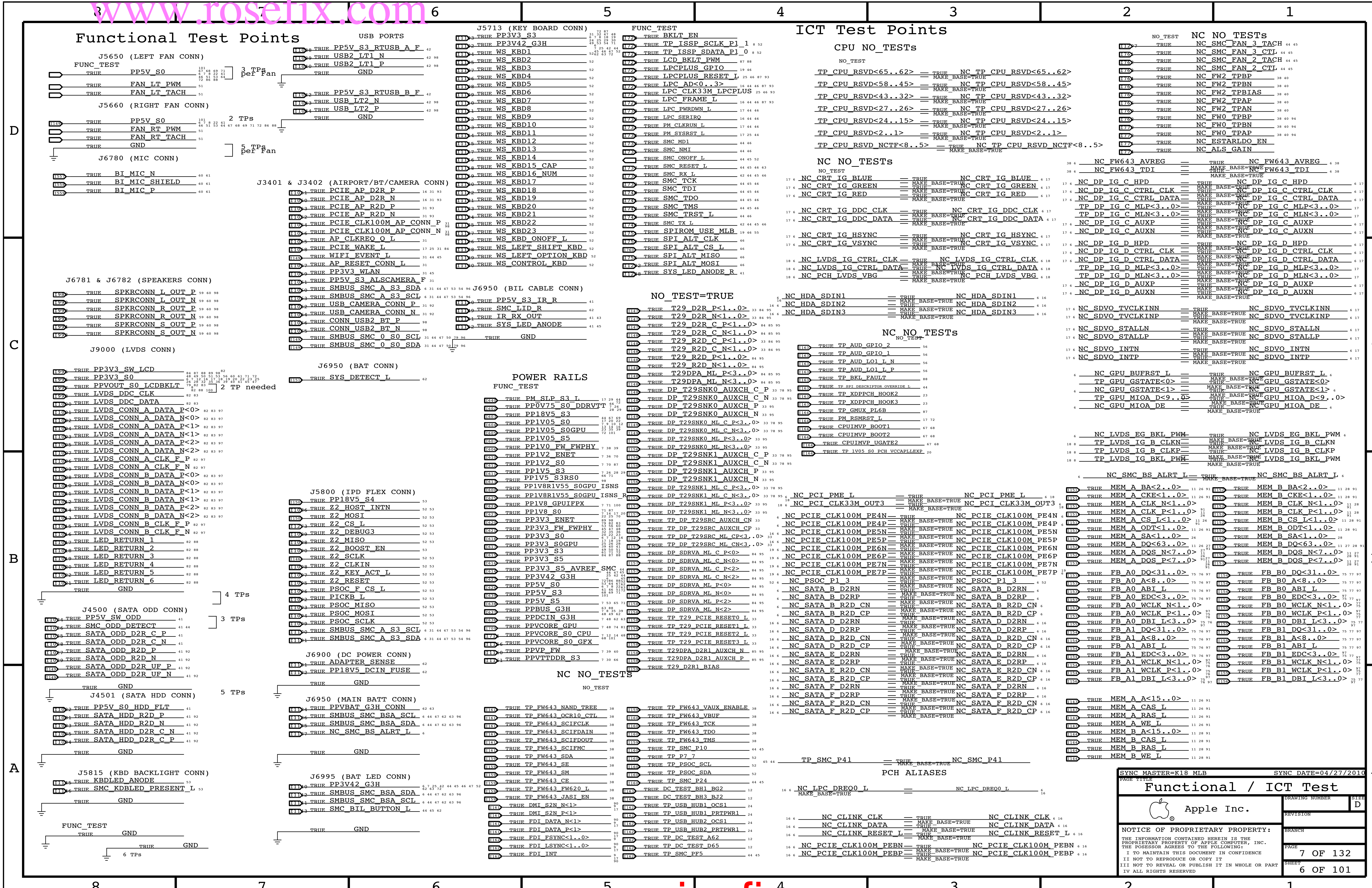

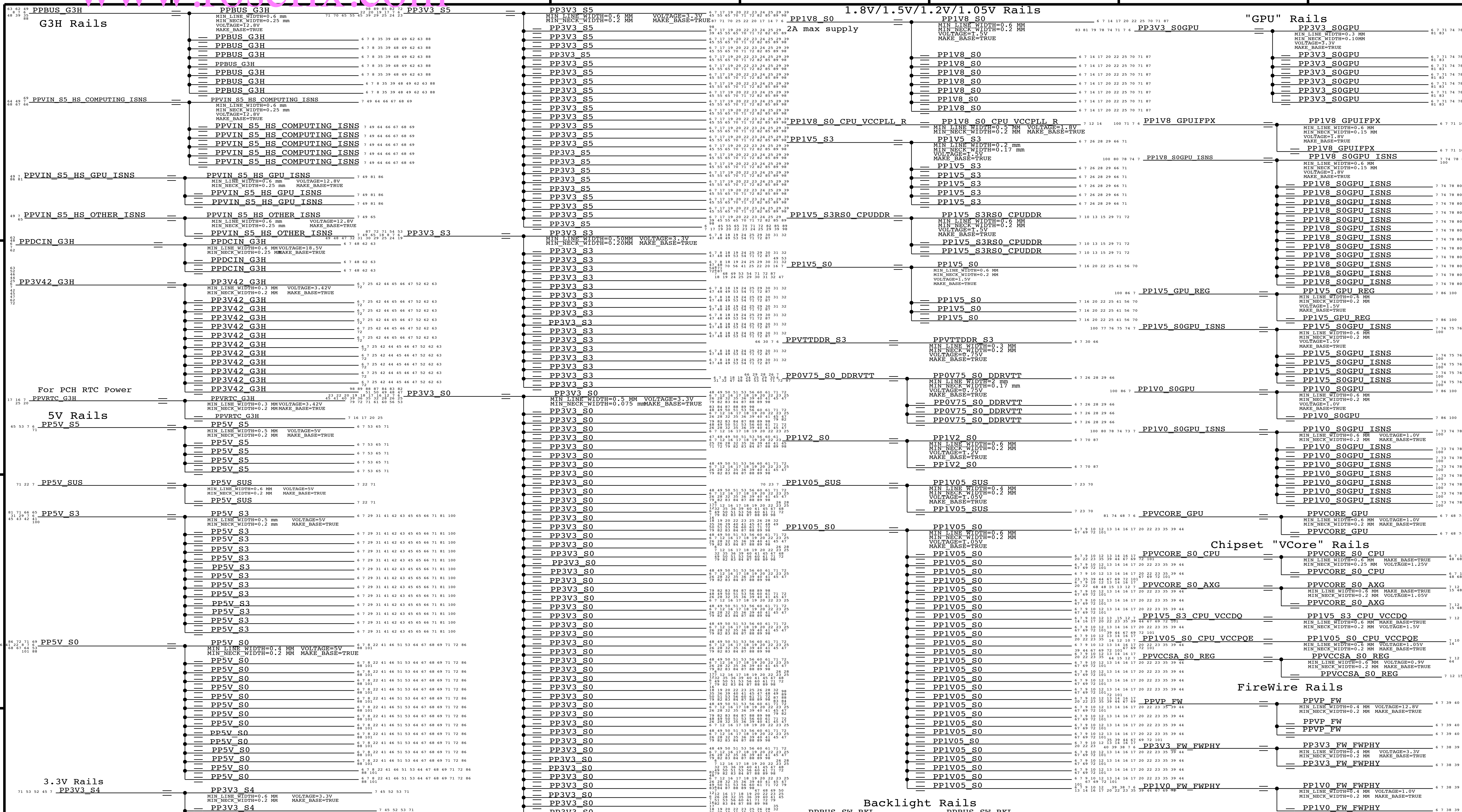

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

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Power Aliases

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Thermal Module Holes

ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 GND
ZT0940 3R2P5 GND
ZT0950 TH GND SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 GND
ZT0990 3R2P5 GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 POGO-2.0OD-3.5H-K86-K87
SH0900 POGO-2.0OD-3.5H-K86-K87
SH0903 POGO-2.0OD-3.5H-K86-K87
SH0916 POGO-2.0OD-3.5H-K86-K87
SH0904 POGO-2.0OD-3.5H-K86-K87

Short (IO Row) EMI pogo pins

SH0911 1.4DIA-SHORT-SILVER-K99
SH0910 1.4DIA-SHORT-SILVER-K99
SH0913 1.4DIA-SHORT-SILVER-K99
SH0912 1.4DIA-SHORT-SILVER-K99
SH0917 1.4DIA-SHORT-SILVER-K99
SH0901 1.4DIA-SHORT-SILVER-K99
SH0914 1.4DIA-SHORT-SILVER-K99
SH GND_CHASSIS_AUDIO_JACK

Heat spreader mounting boss for T29 router

SH0920 STDOFF-4.0OD1.85H-SM
SH0923 STDOFF-4.0OD1.85H-SM

Heat spreader mounting boss for PCH

SH0921 STDOFF-4.0OD2.23H-SM
SH0922 STDOFF-4.0OD2.23H-SM

R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_P0 — C0901 0.01UF 10% 10V X5R 201
R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_N0 — C0902 0.01UF 10% 10V X5R 201
R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_P1 — C0903 0.01UF 10% 10V X5R 201
R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_N1 — C0904 0.01UF 10% 10V X5R 201

T29 / GMUX JTAG Signals

JTAG_ISP_TCK — JTAG_ISP_TCK
JTAG_ISP_TDI — JTAG_ISP_TDI
JTAG_ISP_TDO — JTAG_ISP_TDO
T29_LSEO_LSOE3 — T29_LSEO_LSOE3 — T29_LSEO_LSOE3
T29_LSEO_LSOE2 — T29_LSEO_LSOE2 — T29_LSEO_LSOE2

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
PPVOUT_S0_LCDBKLT — PPVOUT_S0_LCDBKLT
GMUX_VSYNC — GMUX_VSYNC
PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L
PM_ENET_EN — PM_ENET_EN

FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L
TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
NC_PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N
NC_PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P
NC_PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N
NC_PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P
NC_PEG_B_CLKRQ_L_GPIO56 — NC_PEG_B_CLKRQ_L_GPIO56
NC_PCIECLKRQ4_L_GPIO26 — NC_PCIECLKRQ4_L_GPIO26
TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0
GND
NC_PCH_CLKOUT_DPN — NC_PCH_CLKOUT_DPN
NC_PCH_CLKOUT_DPP — NC_PCH_CLKOUT_DPP
NC_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3
NC_FSB_CLK133M_PCHP — NC_FSB_CLK133M_PCHP
NC_FSB_CLK133M_PCHN — NC_FSB_CLK133M_PCHN
NC_LT_GAIN_TP — NC_LT_GAIN_TP
NC_RT_GAIN_TP — NC_RT_GAIN_TP
NC_SW_GAIN_TP — NC_SW_GAIN_TP

PP5V_S0 — XW0901 SM — PP5V_S0_AUDIO — PP5V_S0_AUDIO
XW0902 SM — PP5V_S0_AUDIO_AMP_L
XW0903 SM — PP5V_S0_AUDIO_AMP_R

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN

Unused PEG signals

NC_PEG_D2R_P<15..12> — =PEG_D2R_P<15..12>
NC_PEG_D2R_N<15..12> — =PEG_D2R_N<15..12>
NC_PEG_R2D_C_P<15..12> — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_C_N<15..12> — =PEG_R2D_C_N<15..12>

T29 Signals Through PEG

PCIE_T29_D2R_P<3..0> — =PEG_D2R_P<11..8>
PCIE_T29_D2R_N<3..0> — =PEG_D2R_N<11..8>
PCIE_T29_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8>
PCIE_T29_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8>

GPU signals

PEG_D2R_P<7..0> — =PEG_D2R_P<7..0>
PEG_D2R_N<7..0> — =PEG_D2R_N<7..0>
PEG_R2D_C_P<7..0> — =PEG_R2D_C_P<7..0>
PEG_R2D_C_N<7..0> — =PEG_R2D_C_N<7..0>

Unused T29 Ports

T29_D2R_P<3..2> — NC_T29_D2RP<3..2>
T29_D2R_N<3..2> — NC_T29_D2RN<3..2>
T29_R2D_C_P<3..2> — NC_T29_R2D_CP<3..2>
T29_R2D_C_N<3..2> — NC_T29_R2D_CN<3..2>

DP_EG_AUXCH_N — DP_EG_AUXCH_N
DP_EG_AUXCH_P — DP_EG_AUXCH_P
NC_DPB_EG_AUX_CHN — NC_DPB_EG_AUX_CHN
NC_DPB_EG_AUX_CHP — NC_DPB_EG_AUX_CHP
NC_DPB_EG_DDC_CLK — NC_DPB_EG_DDC_CLK
NC_DPB_EG_DDC_DATA — NC_DPB_EG_DDC_DATA
NC_DPB_EG_MLN<3..0> — DPB_EG_ML_N<3..0>
NC_DPB_EG_MLP<3..0> — DPB_EG_ML_P<3..0>

R0901 4.7K 5% 1/16W MF-LF 402 — LCD_BKLT_EN

T29BST:N — R0950 0 5% 1/8W MF-LF 805 — PPBUS_G3H — PP15V_T29

TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM
NC_GPU_XTALOUT — NC_GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3>

NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS4 — NC_USB_HUB2_OCS4

PP3V3_S3
NOSTUFF R0903 10K 5% 1/16W MF-LF 402 — NOSTUFF R0904 10K 5% 1/16W MF-LF 402
USB_EXTC_N
USB_EXTC_P

PP3V3_S3
NOSTUFF R0913 10K 5% 1/16W MF-LF 402 — NOSTUFF R0914 10K 5% 1/16W MF-LF 402
USB_SDCARD_P — USB_SDCARD_P
USB_SDCARD_N — USB_SDCARD_N

PP3V3_S3
R0915 10K 5% 1/16W MF-LF 402 — R0916 10K 5% 1/16W MF-LF 402
USB_T29A_N
USB_T29A_P

R0926 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_D2R_P1 — C0906 0.01UF 10% 10V X5R 201
R0927 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_D2R_N1 — C0907 0.01UF 10% 10V X5R 201

DP_A_BIAS2
DP_A_BIAS0
C0905 0.01UF 10% 10V X5R 201
C0908 0.01UF 10% 10V X5R 201

NC_DP_IG_MLP<3..0> — TP_DP_IG_B_MLP<3..0>
NC_DP_IG_MLN<3..0> — TP_DP_IG_B_MLN<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD

GND MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.095 mm VOLTAGE=0V

Digital Ground

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Signal Aliases

Apple Inc.

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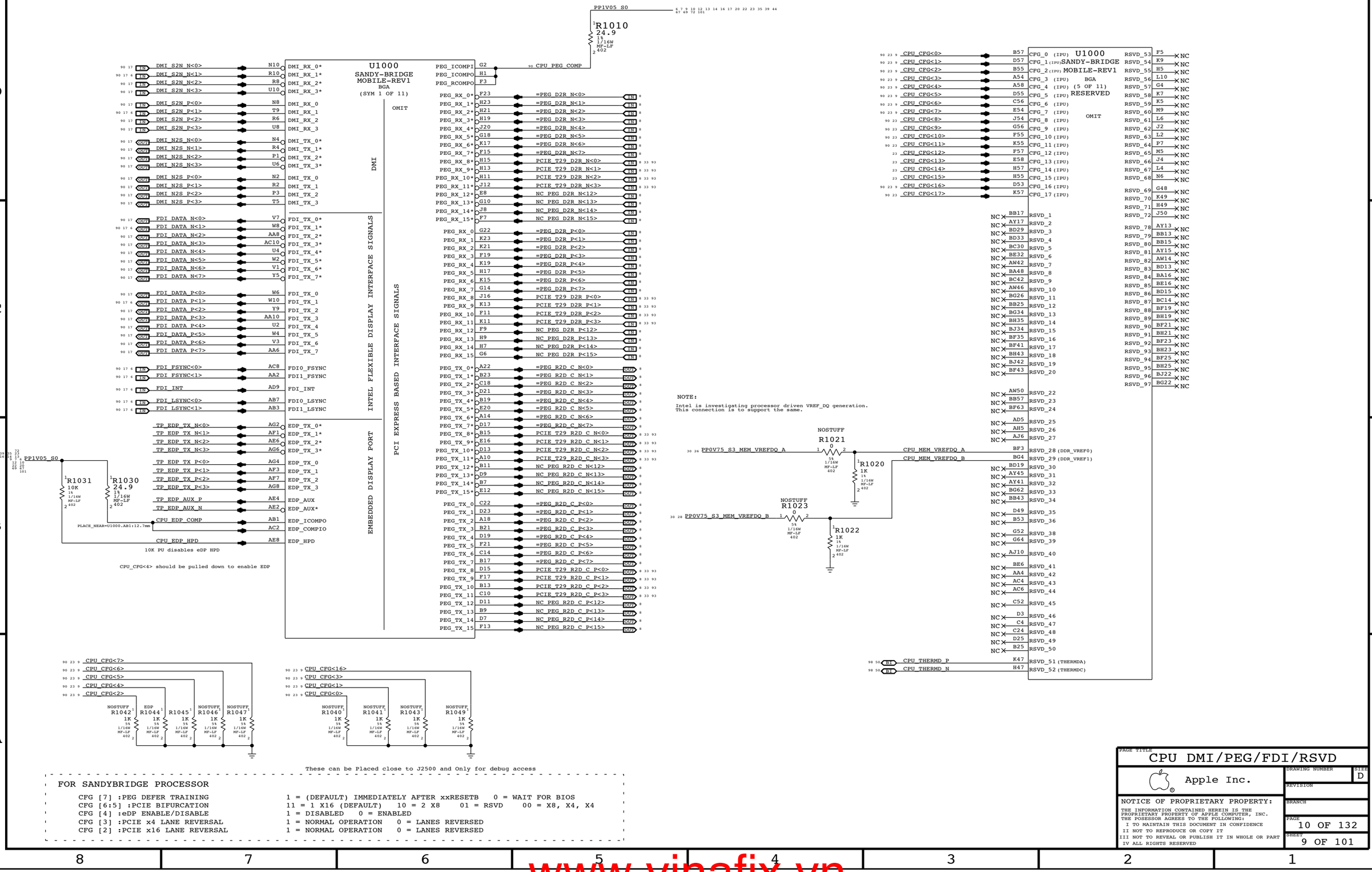

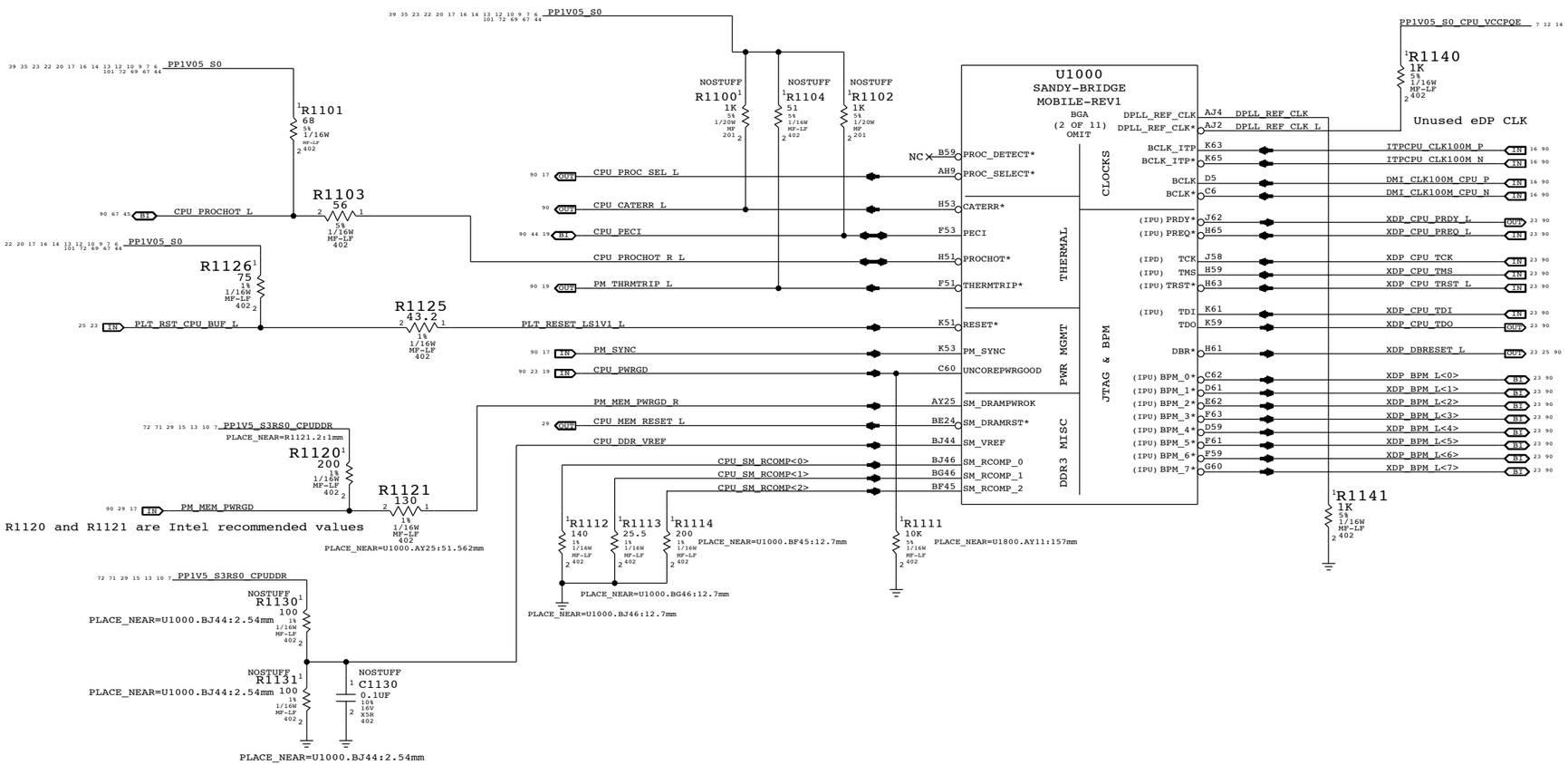

PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

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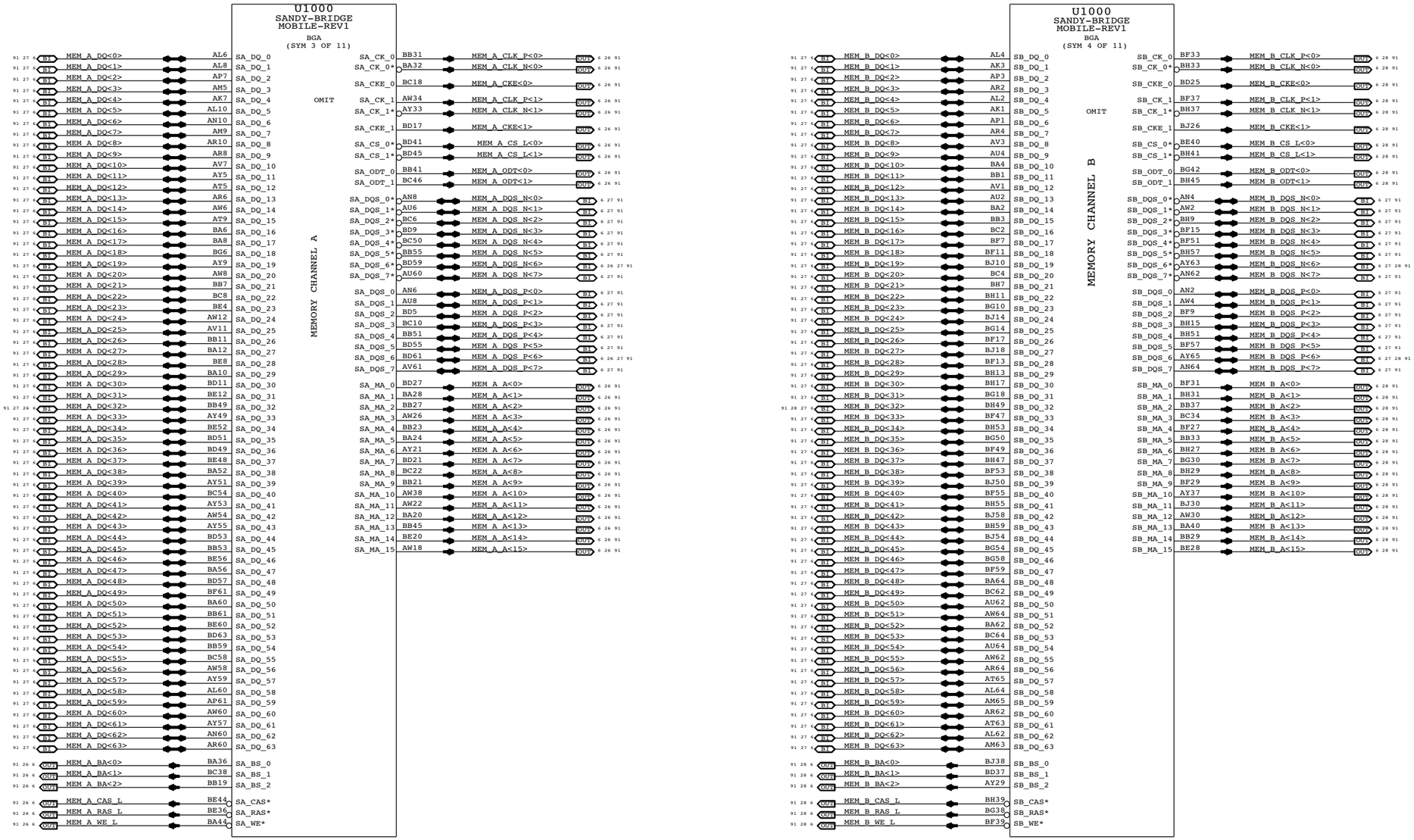

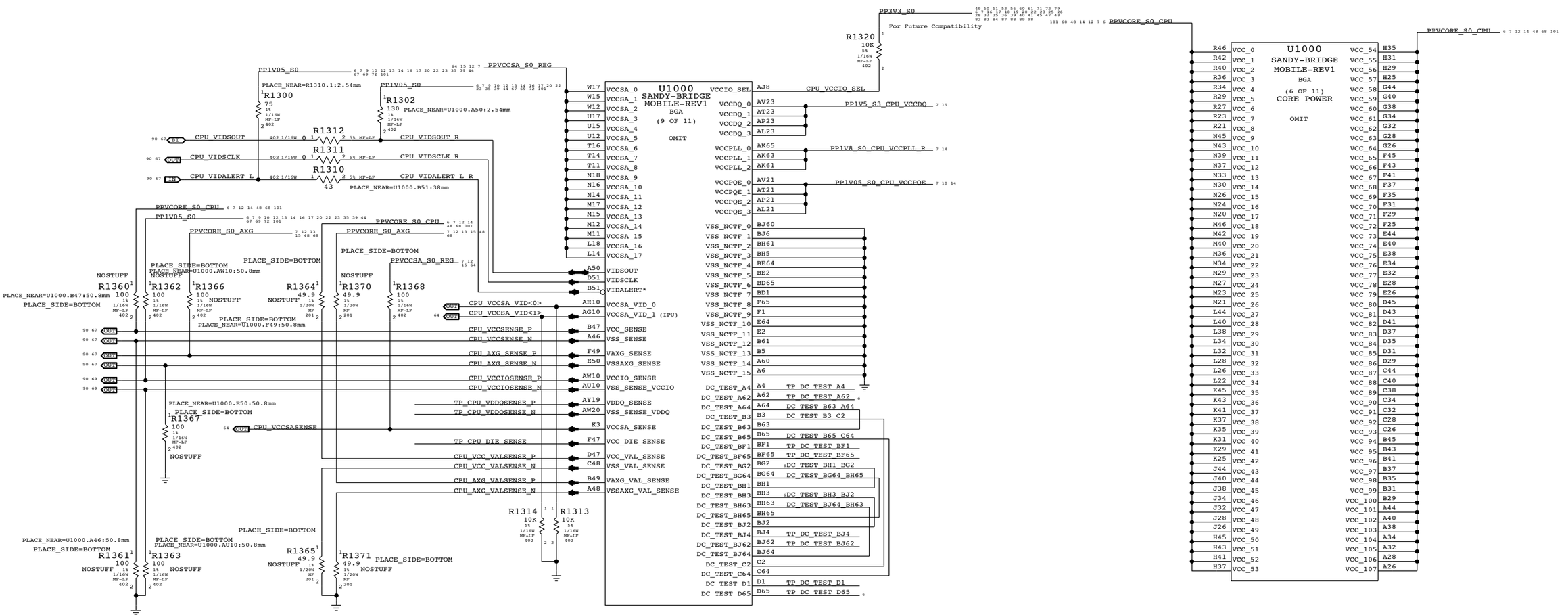

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K92_MLB SYNC_DATE=08/03/2010

PAGE TITLE: CPU POWER

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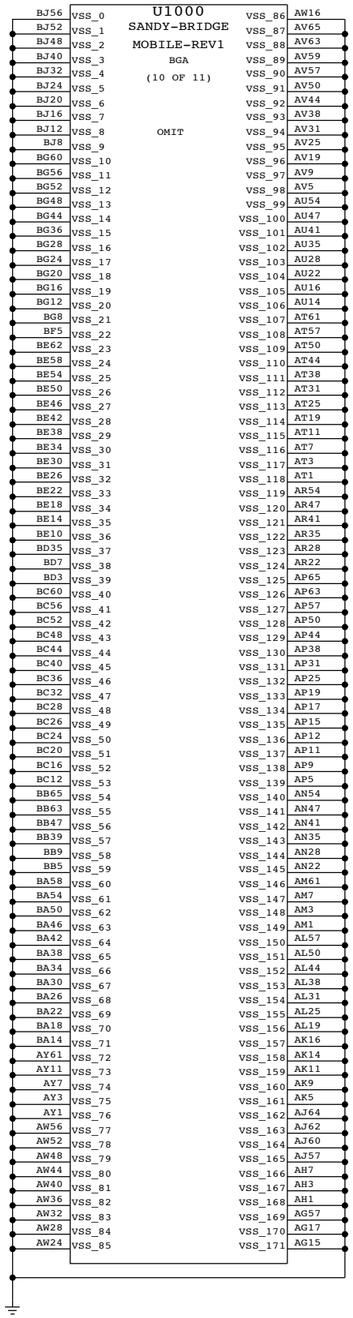
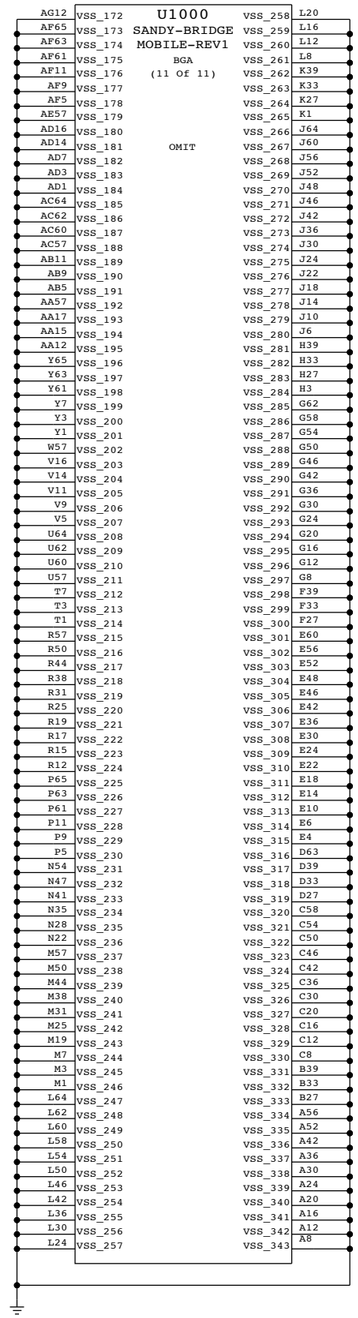
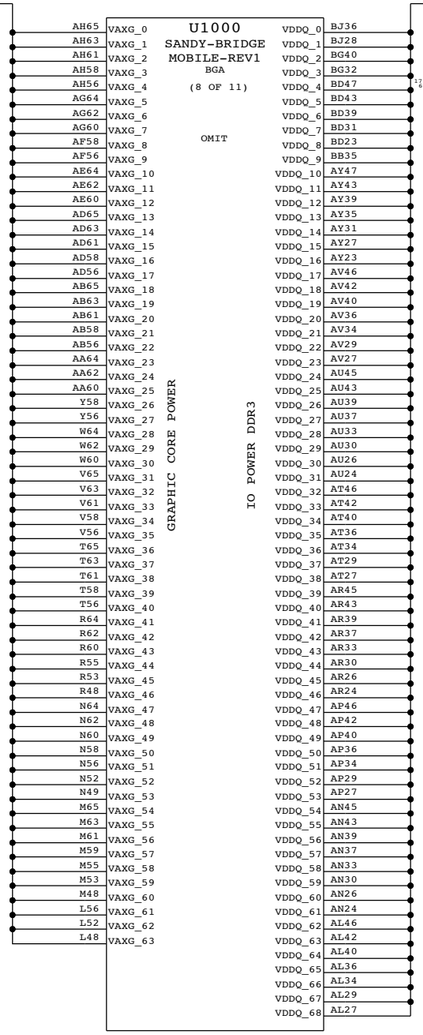


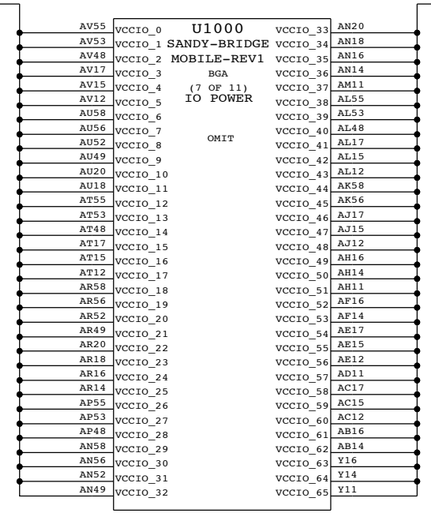


PPVCORE_S0_AXG



PP1V5_S3RS0_CPUDDR

PP1V05_S0



PP1V05_S0

PP1V05_S0

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 20% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

CRITICAL C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5R-CERM1 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CRITICAL C1640 C1641 C1642 C1643
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NOSTUFF C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

PP1V05_S0

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X5R 402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

CRITICAL C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL C1682
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL C1683
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W MF 0603

PP1V05_S0_CPU_VCCPQE

C1684
1UF 10% 10V X5R 402

CPU VCCPLL DECOUPLING

PP1V8_S0

R1600
0
5% 1/16W MF-LF 402

PP1V8_S0_CPU_VCCPLL_R

C1685
1UF 10% 10V X5R 402

C1686
1UF 10% 10V X5R 402

CRITICAL C1687
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

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CPU DECOUPLING-I

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VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

68 48 13 12 7 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
NOSTUFF C1712 1UF 10% 10V X5R 402
NOSTUFF C1713 1UF 10% 10V X5R 402
NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.

C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
NOSTUFF C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

PLACEMENT_NOTE (C1738-C1747):

72 71 29 13 10 7 PP1V5_S3RS0_CPUDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

PLACEMENT_NOTE (C1758-C1762):

64 12 7 PPVCCSA_S0_REG

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

C1768 270UF 20% 2V TANT CASE-B4-SM

SYNC MASTER=K92_MLB SYNC DATE=08/19/2010

PAGE TITLE: CPU DECOUPLING-II

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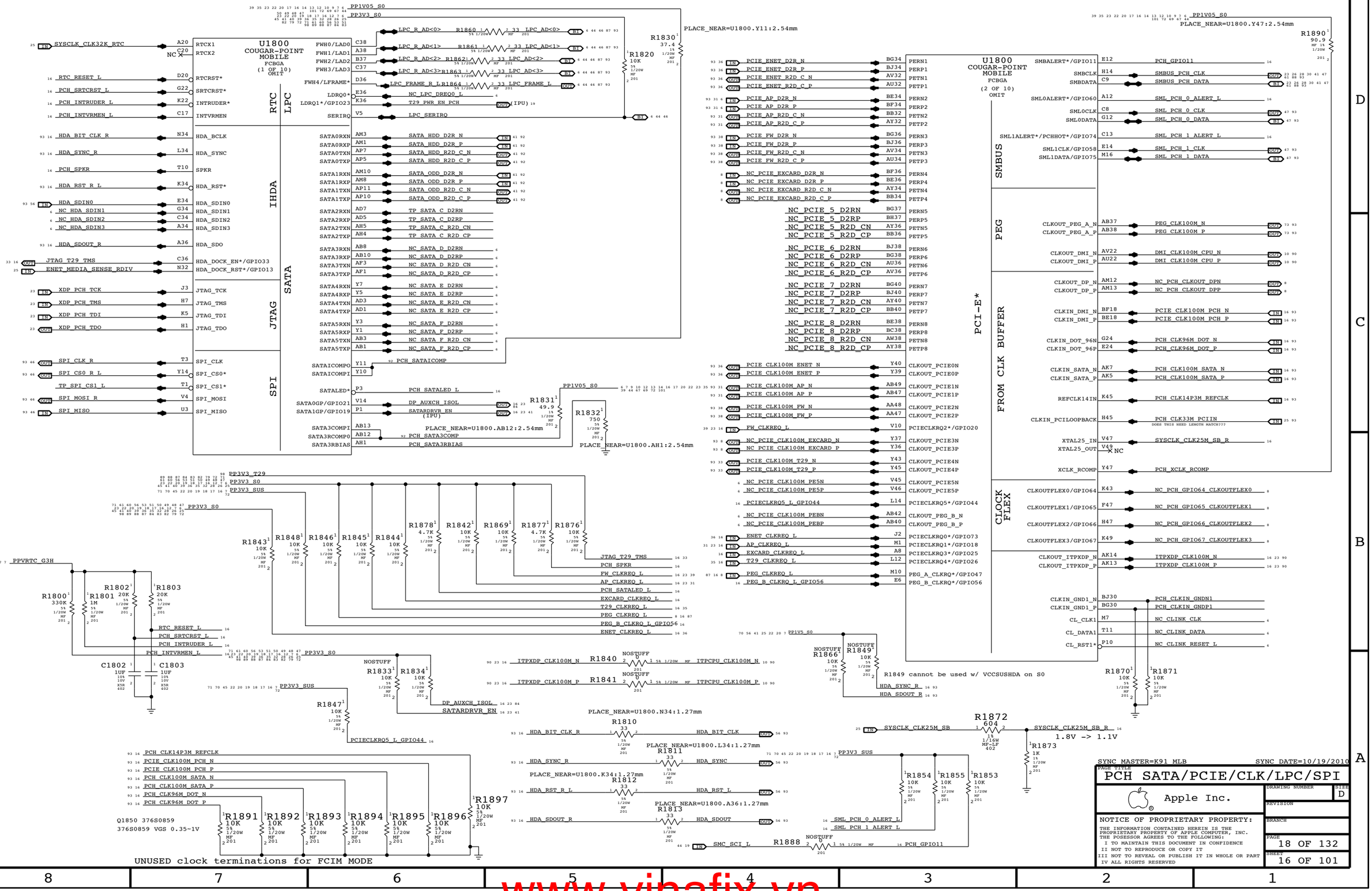

PP3V3_SUS
PP1V05_S0
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201 PLACE_NEAR=U1800.BJ24:12.7mm

U1800 COUGAR-POINT MOBILE FCBGA (3 OF 10) OMIT

DMI_N2S_N<0> BC24 DMI0RXN
DMI_N2S_N<1> BE20 DMI1RXN
DMI_N2S_N<2> BG18 DMI2RXN
DMI_N2S_N<3> BG20 DMI3RXN
DMI_N2S_P<0> BE24 DMI0RXP
DMI_N2S_P<1> BC20 DMI1RXP
DMI_N2S_P<2> BJ18 DMI2RXP
DMI_N2S_P<3> BJ20 DMI3RXP
DMI_S2N_N<0> AW24 DMI0TXN
DMI_S2N_N<1> AW20 DMI1TXN
DMI_S2N_N<2> BB18 DMI2TXN
DMI_S2N_N<3> AV18 DMI3TXN
DMI_S2N_P<0> AY24 DMI0TXP
DMI_S2N_P<1> AY20 DMI1TXP
DMI_S2N_P<2> AY18 DMI2TXP
DMI_S2N_P<3> AU18 DMI3TXP
PCH_DMI2RBIAS BH21 DMI2RBIAS
PLACE_NEAR=U1800.BH21:2.54mm
PCH_DMI_COMP BJ24 DMI_ZCOMP
BG25 DMI_IRCOMP

DMI

FDI_DATA_N<0> BJ14 FDI_RXN0
FDI_DATA_N<1> AY14 FDI_RXN1
FDI_DATA_N<2> BE14 FDI_RXN2
FDI_DATA_N<3> BH13 FDI_RXN3
FDI_DATA_N<4> BC12 FDI_RXN4
FDI_DATA_N<5> BJ12 FDI_RXN5
FDI_DATA_N<6> BG10 FDI_RXN6
FDI_DATA_N<7> BG9 FDI_RXN7
FDI_DATA_P<0> BG14 FDI_RXP0
FDI_DATA_P<1> BB14 FDI_RXP1
FDI_DATA_P<2> BF14 FDI_RXP2
FDI_DATA_P<3> BG13 FDI_RXP3
FDI_DATA_P<4> BE12 FDI_RXP4
FDI_DATA_P<5> BG12 FDI_RXP5
FDI_DATA_P<6> BJ10 FDI_RXP6
FDI_DATA_P<7> BH9 FDI_RXP7
FDI_INT AW16 FDI_INT
FDI_FSYNC<0> AV12 FDI_FSYNC0
FDI_FSYNC<1> BC10 FDI_FSYNC1
FDI_LSYNC<0> AV14 FDI_LSYNC0
FDI_LSYNC<1> BB10 FDI_LSYNC1

FDI

SYSTEM POWER MANAGEMENT

PM_SYSRST_L K3 SYS_RESET*
PM_PCH_SYS_PWROK P12 SYS_PWROK
PM_PCH_PWROK L22 PWROK
PM_MEM_PWRGD B13 DRAMPWROK
PM_DSW_PWRGD E22 DPWROK
PM_PCH_PWROK L10 APWROK
PM_RSMRST_L C21 RSMRST*
SUSWARN_L K16 SUSWARN*/SUSPWRDNACK/GPIO30
PM_PWRBTN_L E20 PWRBTN*
PD on SMC page SMC_ADAPTER_EN H20 ACPRESENT/GPIO31
PM_BATLOW_L E10 BATLOW*/GPIO72
PCH_RI_L A10 RI*

WAKE* B9 PCIE_WAKE_L
CLKRUN*/GPIO32 N3 PM_CLKRUN_L
SUS_STAT*/GPIO61 G8 LPC_PWRDWN_L
SUSCLK/GPIO62 N14 PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63 D10 PM_SLP_S5_L
SLP_S4* H4 PM_SLP_S4_L
SLP_S3* F4 PM_SLP_S3_L
SLP_A* G10 TP_PM_SLP_A_L
TP23 AY16 TP_PCH_TP23
PMSYNCH AP14 PM_SYNC
SLP_LAN*/GPIO29 K14 GPIO29_SLP_LAN_L

PPVRTC_G3H
PP1V8_S0
R1981 2.2K 5% 1/20W MF 201
R1915 390K 5% 1/20W MF 201
R1980 1K 5% 1/20W MF 201
CPU_PROC_SEL_L

DF_TVS AY1 PCH_DF_TVS
DSWVRMEN A18 PCH_DSWVRMEN
SLP_SUS* G16 PM_SLP_SUS_L
SUSACK* C12 PCH_SUSACK_L

R1909 100K 5% 1/20W MF 201

DF_TVS:DMI & FDI Term Voltage
Set to Vss when Low
Set to Vcc when High

PLACE_NEAR=U1800.T43:2.54mm

U1800 COUGAR-POINT MOBILE FCBGA (4 OF 10) OMIT

DIGITAL DISPLAY INTERFACE

NC_CRT_IG_BLUE N48 CRT_BLUE
NC_CRT_IG_GREEN P49 CRT_GREEN
NC_CRT_IG_RED T49 CRT_RED
NC_CRT_IG_DDC_CLK T39 CRT_DDC_CLK
NC_CRT_IG_DDC_DATA M40 CRT_DDC_DATA
NC_CRT_IG_HSYNC M47 CRT_HSYNC
NC_CRT_IG_VSYNC M49 CRT_VSYNC
PCH_DAC_IREF T43 DAC_IREF
T42 CRT_IRTN

CRT

R1951 1K 5% 1/20W MF 201

SDVO_TVCLKINN AP43 NC_SDVO_TVCLKINN
SDVO_TVCLKINP AP45 NC_SDVO_TVCLKINP
SDVO_STALLN AM42 NC_SDVO_STALLN
SDVO_STALLP AM40 NC_SDVO_STALLP
SDVO_INTN AP39 NC_SDVO_INTN
SDVO_INTP AP40 NC_SDVO_INTP
SDVO_CTRLCLK P38 DP_IG_DDC_CLK
SDVO_CTRLDATA M39 DP_IG_DDC_DATA
DDPB_AUXN AT49 DP_IG_AUX_CH_N
DDPB_AUXP AT47 DP_IG_AUX_CH_P
DDPB_HPD AT40 DP_IG_HPD
DDPB_0N AV42 NC_DP_IG_MLN<0>
DDPB_0P AV40 NC_DP_IG_MLP<0>
DDPB_1N AV45 NC_DP_IG_MLN<1>
DDPB_1P AV46 NC_DP_IG_MLP<1>
DDPB_2N AU48 NC_DP_IG_MLN<2>
DDPB_2P AU47 NC_DP_IG_MLP<2>
DDPB_3N AV47 NC_DP_IG_MLN<3>
DDPB_3P AV49 NC_DP_IG_MLP<3>
DDPC_CTRLCLK P46 NC_DP_IG_C_CTRL_CLK
DDPC_CTRLDATA P42 NC_DP_IG_C_CTRL_DATA
DDPC_AUXN AP47 NC_DP_IG_C_AUXN
DDPC_AUXP AP49 NC_DP_IG_C_AUXP
DDPC_HPD AT38 NC_DP_IG_C_HPD
DDPC_0N AY47 NC_DP_IG_C_MLN<0>
DDPC_0P AY49 NC_DP_IG_C_MLP<0>
DDPC_1N AY43 NC_DP_IG_C_MLN<1>
DDPC_1P AY45 NC_DP_IG_C_MLP<1>
DDPC_2N BA47 NC_DP_IG_C_MLN<2>
DDPC_2P BA48 NC_DP_IG_C_MLP<2>
DDPC_3N BB47 NC_DP_IG_C_MLN<3>
DDPC_3P BB49 NC_DP_IG_C_MLP<3>
DDPD_CTRLCLK M43 NC_DP_IG_D_CTRL_CLK
DDPD_CTRLDATA M36 NC_DP_IG_D_CTRL_DATA
DDPD_AUXN AT45 NC_DP_IG_D_AUXN
DDPD_AUXP AT43 NC_DP_IG_D_AUXP
DDPD_HPD BH41 NC_DP_IG_D_HPD
DDPD_0N BB43 NC_DP_IG_D_MLN<0>
DDPD_0P BB45 NC_DP_IG_D_MLP<0>
DDPD_1N BF44 NC_DP_IG_D_MLN<1>
DDPD_1P BE44 NC_DP_IG_D_MLP<1>
DDPD_2N BF42 NC_DP_IG_D_MLN<2>
DDPD_2P BE42 NC_DP_IG_D_MLP<2>
DDPD_3N BJ42 NC_DP_IG_D_MLN<3>
DDPD_3P BG42 NC_DP_IG_D_MLP<3>

PCIE_WAKE_L — PCIE_WAKE_L (MAKE_BASE=TRUE) — IN
SUSWARN_L — R1986 0 5% 1/20W MF 201 — PCH_SUSACK_L

PP3V3_S0
R1991 8.2K 5% 1/20W MF 201
PM_CLKRUN_L

PP3V3_SUS
PP3V3_S5
PP3V3_SUS
R1925 1K 1% 1/20W MF 201
R1985 1K 1% 1/20W MF 201
R1982 10K 5% 1/20W MF 201
R1983 10K 5% 1/20W MF 201
SUSWARN_L
GPIO29_SLP_LAN_L
PM_PWRBTN_L
PCIE_WAKE_L

PM_SLP_S3_L
PM_SLP_SUS_L
PM_SLP_S5_L
PM_SLP_S4_L
R1921 100K 5% 1/20W MF 201
R1922 100K 5% 1/20W MF 201
R1923 100K 5% 1/20W MF 201
R1924 100K 5% 1/20W MF 201

PAGE TITLE: PCH DMI/FDI/GRAPHICS

Apple Inc.

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SIZE: D
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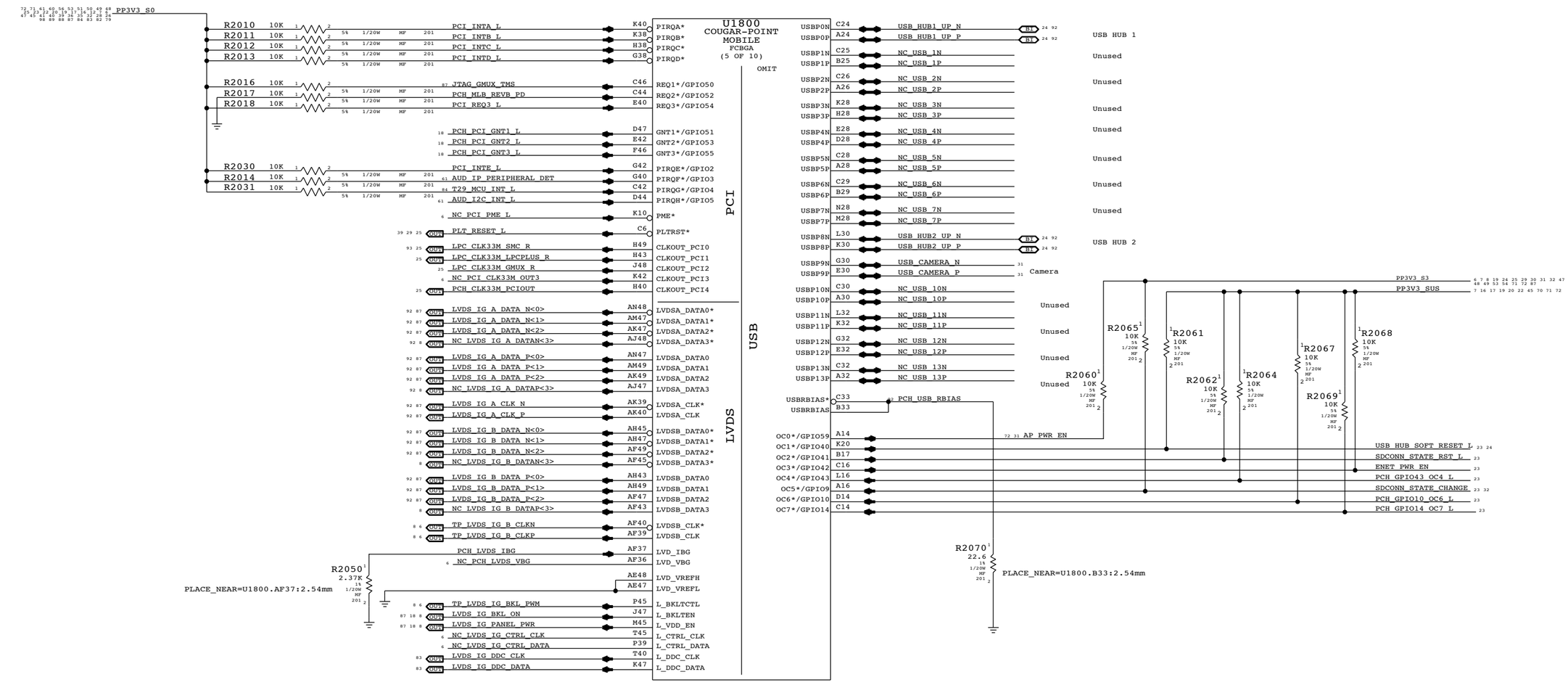

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE
PCH PCI/FLASHCACHE/USB

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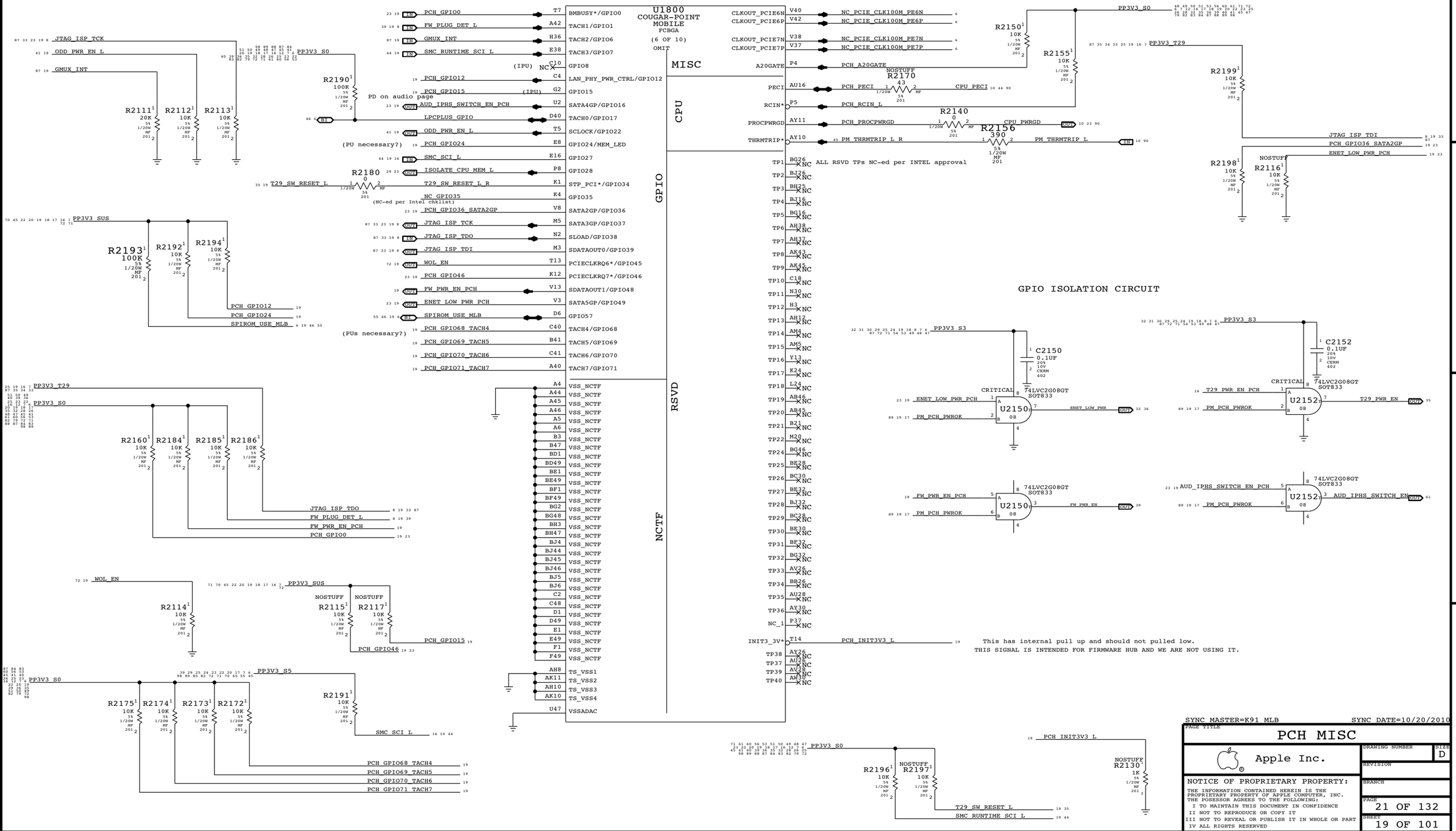

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PAGE TITLE: PCH MISC

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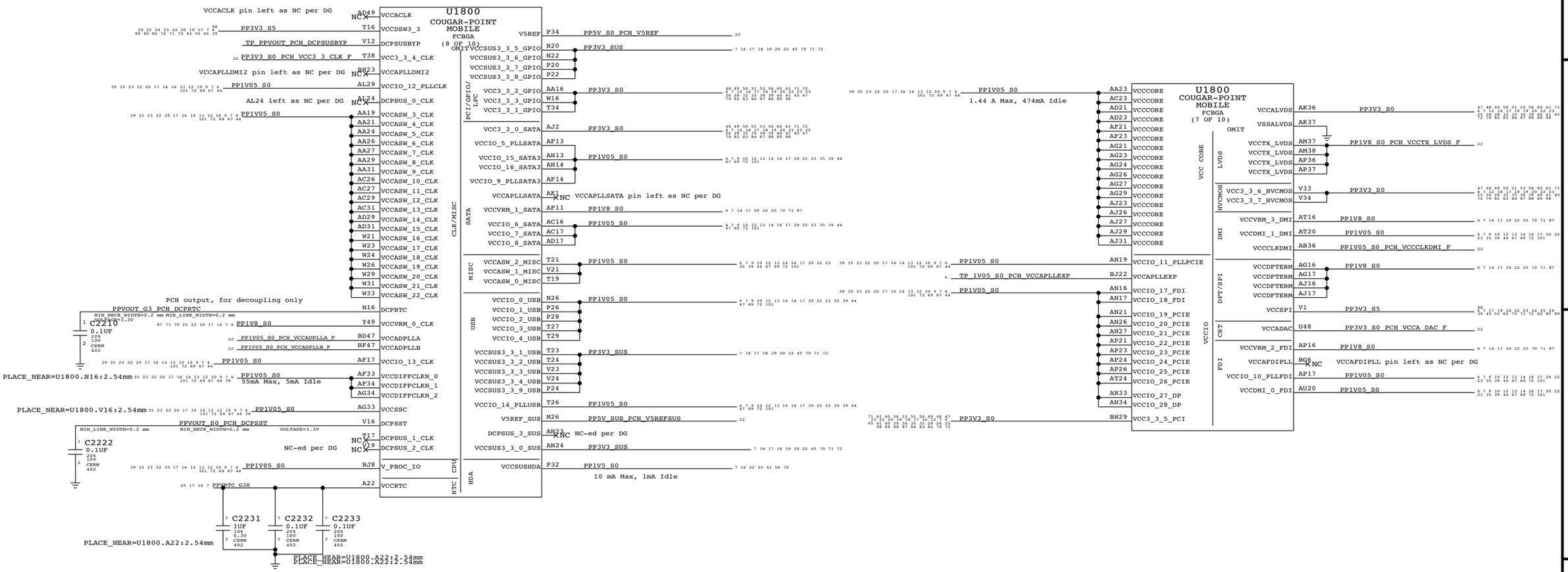

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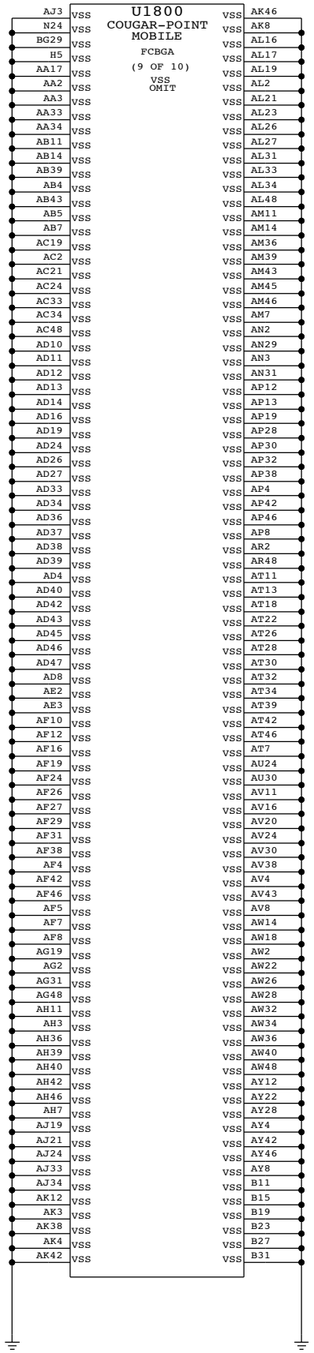

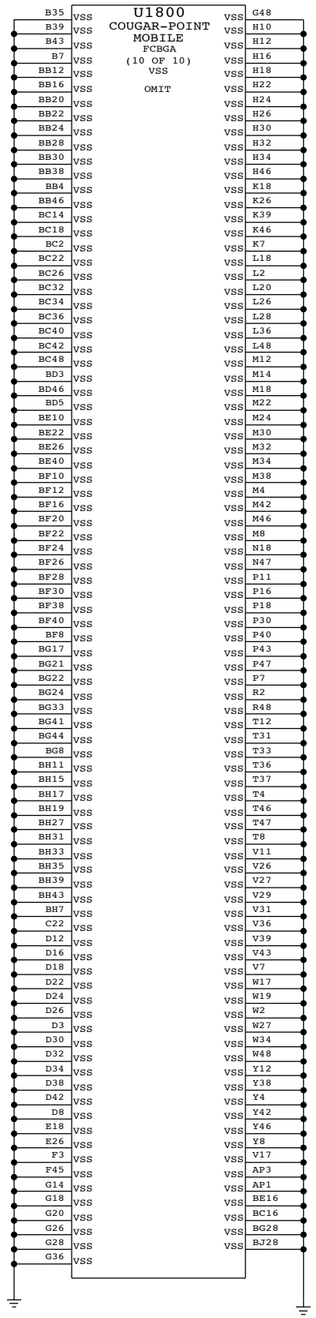

SYNC MASTER=K92 MLB SYNC DATE=04/30/2010

PAGE TITLE

PCH GROUNDS

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8 7 6 5 4 3 2 1

CRITICAL
L2406
10UH-0.45A
1210-HF
PP1V05_S0
PP1V05_S0_PCH_VCCCLKDMI_R
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
R2415
5%
1/16W
MF-LF
402
PP1V05_S0_PCH_VCCCLKDMI_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
C2411
1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.AB36:2.54mm

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_SUS
C2484
0.1UF
10%
16V
X5R
402
C2413
0.1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.P24:2.54mm
PLACE_NEAR=U1800.V24:2.54mm

PP1V8_S0
PLACE_NEAR=U1800.AJ16:2.54mm
C2440
0.1UF
20%
10V
CERM
402

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
PP1V05_S0
C2444
1UF
10%
6.3V
CERM
402
C2452
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.AH13:2.54mm
PLACE_NEAR=U1800.AC17:2.54mm
C2446
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.P28:2.54mm

CRITICAL
L2407
0.1UH
0805
PP1V8_S0
PP1V8_S0_PCH_VCCTX_LVDS_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.8V
CRITICAL
C2400
22UF
20%
6.3V
CERM
805
C2406
0.01UF
10%
16V
CERM
402
C2408
0.01UF
10%
16V
CERM
402
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm

PCH VCCSUSHDA BYPASS
PP1V5_S0
C2441
0.1UF
20%
10V
CERM
402
PLACE_NEAR=U1800.P32:2.54mm

PP1V05_S0
C2416
4.7UF
20%
6.3V
X5R
402
C2417
0.1UF
10%
16V
X5R
402
C2430
0.1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm

PP1V05_S0
C2475
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.AG33:2.54mm
PP3V3_SUS
C2476
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.P22:2.54mm

PP3V3_S0
R2450
0
5%
1/20W
MF
201
PP3V3_S0_PCH_VCCA_DAC_F
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
CRITICAL
C2450
10UF
20%
6.3V
CERM
805
C2451
0.1UF
10%
16V
X5R
402
C2455
0.01UF
10%
16V
CERM
402
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm

PP3V3_S5
PLACE_NEAR=U1800.V1:2.54mm
C2442
1UF
10%
6.3V
CERM
402

PCH VCCIO BYPASS
PP1V05_S0
C2419
1UF
10%
6.3V
CERM
402
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PLACE_NEAR=U1800.AT20:2.54mm

PP3V3_S5
PLACE_NEAR=U1800.T16:2.54mm
C2499
0.1UF
20%
10V
CERM
402

PP1V05_S0
PLACE_NEAR=U1800.AF34:2.54mm
C2434
1UF
10%
6.3V
CERM
402
PP1V05_S0
C2469
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.AF17:2.54mm

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C2481
1UF
10%
6.3V
CERM
402
C2482
1UF
10%
6.3V
CERM
402
C2483
1UF
10%
6.3V
CERM
402
C2460
10UF
20%
6.3V
CERM
805
PLACE_NEAR=U1800.AD21:2.54mm
PLACE_NEAR=U1800.AG24:2.54mm
PLACE_NEAR=U1800.AJ21:2.54mm
PLACE_NEAR=U1800.AJ26:2.54mm

PP3V3_S0
PP5V_S0
1 mA
R2405
100
5%
1/16W
MF-LF
402
NCX
D2400
BAT54DW-X-G
SOT-363
NEED PWR CONSTRAINT
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA
PP5V_S0_PCH_V5REF
C2439
1UF
10%
10V
X5R
402
PLACE_NEAR=U1800.P34:2.54mm
PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)

PP3V3_S0
R2451
5%
1/16W
MF-LF
402
PP3V3_S0_PCH_VCC3_3_CLK_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
CRITICAL
L2451
10UH-0.12A-0.36OHM
0603
PP3V3_S0_PCH_VCC3_3_CLK_F
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
CRITICAL
C2453
10UF
20%
6.3V
X5R
603
C2454
1UF
10%
10V
X5R
402
PLACE_NEAR=U1800.T38:2.54mm
PLACE_NEAR=U1800.T38:2.54mm

PP1V05_S0
C2426
1UF
10%
6.3V
CERM
402
C2456
1UF
10%
6.3V
CERM
402
C2496
1UF
10%
6.3V
CERM
402
C2428
22UF
20%
6.3V
CERM
805
C2420
22UF
20%
6.3V
CERM
805
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm

PP3V3_SUS
PP5V_SUS
1 mA S0-S5
R2404
10
5%
1/16W
MF-LF
402
NCX
D2400
BAT54DW-X-G
SOT-363
NEED PWR CONSTRAINT
PP5V_SUS_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA S0-S5
PP5V_SUS_PCH_V5REFSUS
C2438
0.1UF
20%
10V
CERM
402
PLACE_NEAR=U1800.M26:2.54mm
PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)

PP1V05_S0
R2490
0
5%
1/16W
MF-LF
402
PP1V05_S0_PCH_VCCADPLLA_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
CRITICAL
L2490
10UH-0.12A-0.36OHM
0603
PP1V05_S0_PCH_VCCADPLLA_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
NO STUFF
68 mA
CRITICAL
C2491
220UF
20%
2.5V
POLY-TANT
CASE-B2-SM1
C2492
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.BD47:2.54MM
PLACE_NEAR=U1800.BD47:2.54MM
PCH VCCADPLLA Filter
(PCH DPLLA PWR)

R2491
0
5%
1/16W
MF-LF
402
PP1V05_S0_PCH_VCCADPLLB_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
CRITICAL
L2491
10UH-0.12A-0.36OHM
0603
PP1V05_S0_PCH_VCCADPLLB_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
NO STUFF
69 mA
CRITICAL
C2493
220UF
20%
2.5V
POLY-TANT
CASE-B2-SM1
C2494
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.BF47:2.54MM
PLACE_NEAR=U1800.BF47:2.54MM
PCH VCCADPLLB Filter
(PCH DPLLB PWR)

PP1V05_S0
C2429
1UF
10%
6.3V
CERM
402
C2414
1UF
10%
6.3V
CERM
402
C2407
1UF
10%
6.3V
CERM
402
C2463
1UF
10%
6.3V
CERM
402
C2401
10UF
20%
16V
X5R-CERM
0805
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm

PP3V3_S0
C2421
0.1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.BH29:2.54mm

PP3V3_S0
C2423
0.1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.AJ2:2.54mm

PP3V3_S0
C2424
0.1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.V33:2.54mm

PP3V3_S0
C2486
0.1UF
10%
25V
X5R
402
C2485
0.1UF
10%
25V
X5R
402
PLACE_NEAR=U1800.T34:2.54mm
PLACE_NEAR=U1800.AA16:2.54mm

SYNC MASTER=K92_MLB SYNC DATE=07/06/2010

PAGE TITLE
PCH DECOUPLING

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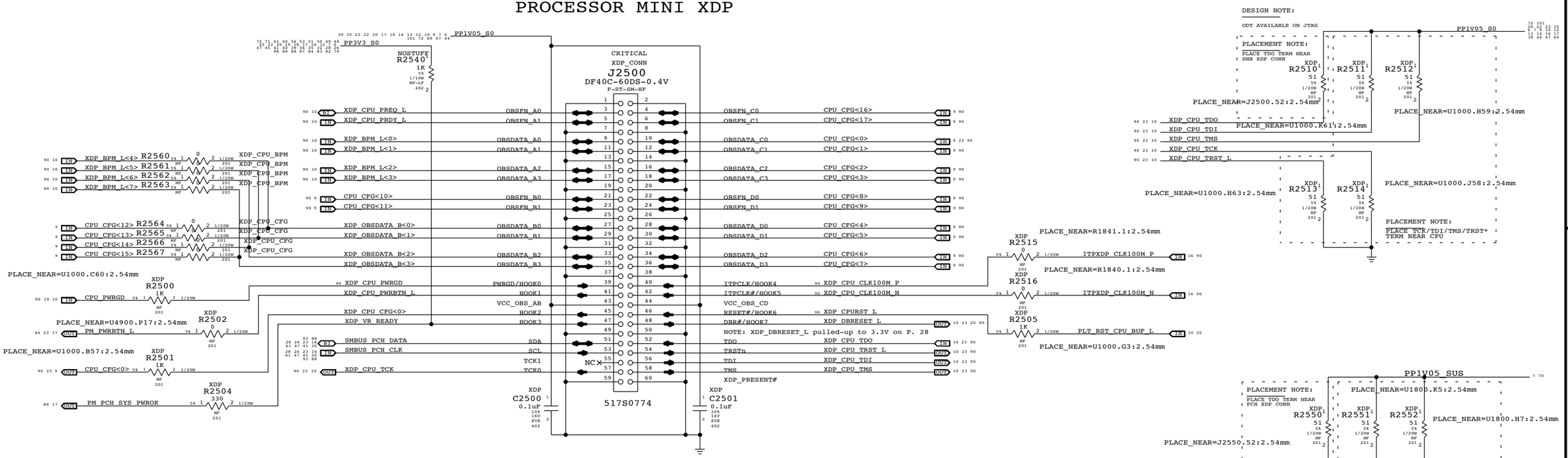
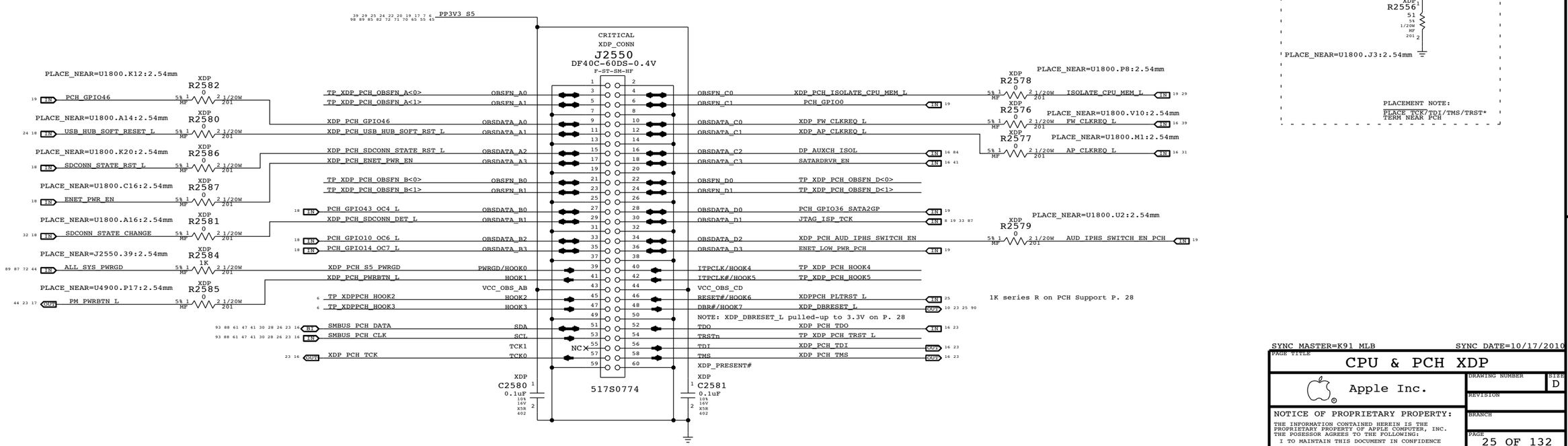
PROCESSOR MINI XDP



PCH MINI XDP



SYNC_MASTER=K91_MLB SYNC_DATE=10/17/2010

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: SIZE D

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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

T29 - no longer used, pulled up to 3V3 S0

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

External A

SD Card/Express Card

SYNC MASTER=K91 ERIC SYNC DATE=10/08/2010

PAGE TITLE: USB HUBS

Apple Inc.

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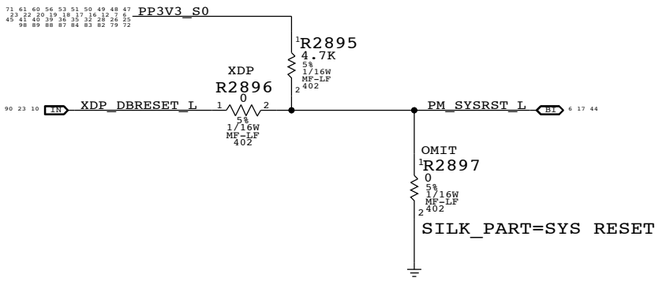
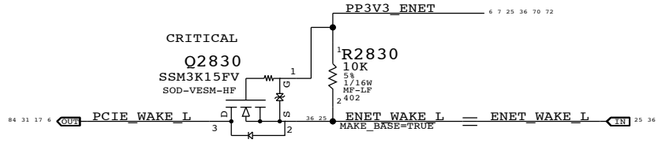
PCH Reset Button

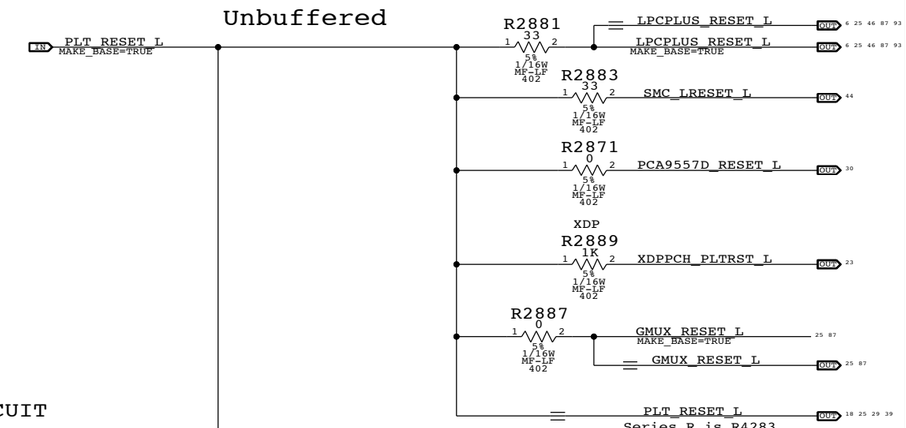


Ethernet WAKE# Isolation

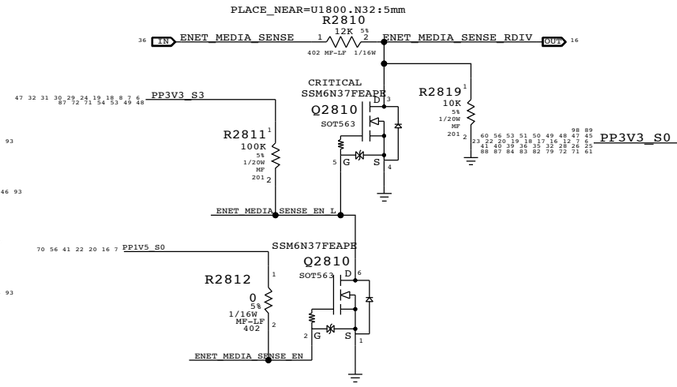


Platform Reset Connections

Unbuffered

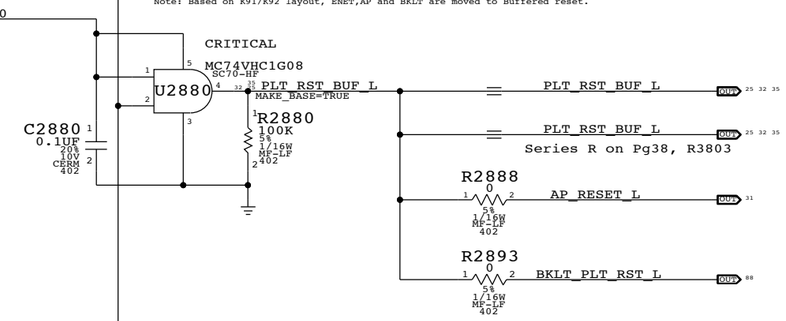


ENET_MEDIA_SENSE ISOLATION CIRCUIT

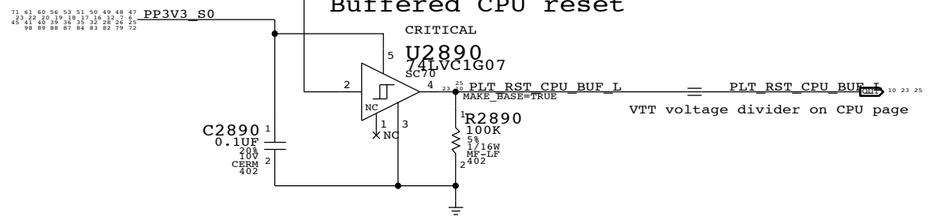


Buffered

Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.



Buffered CPU reset

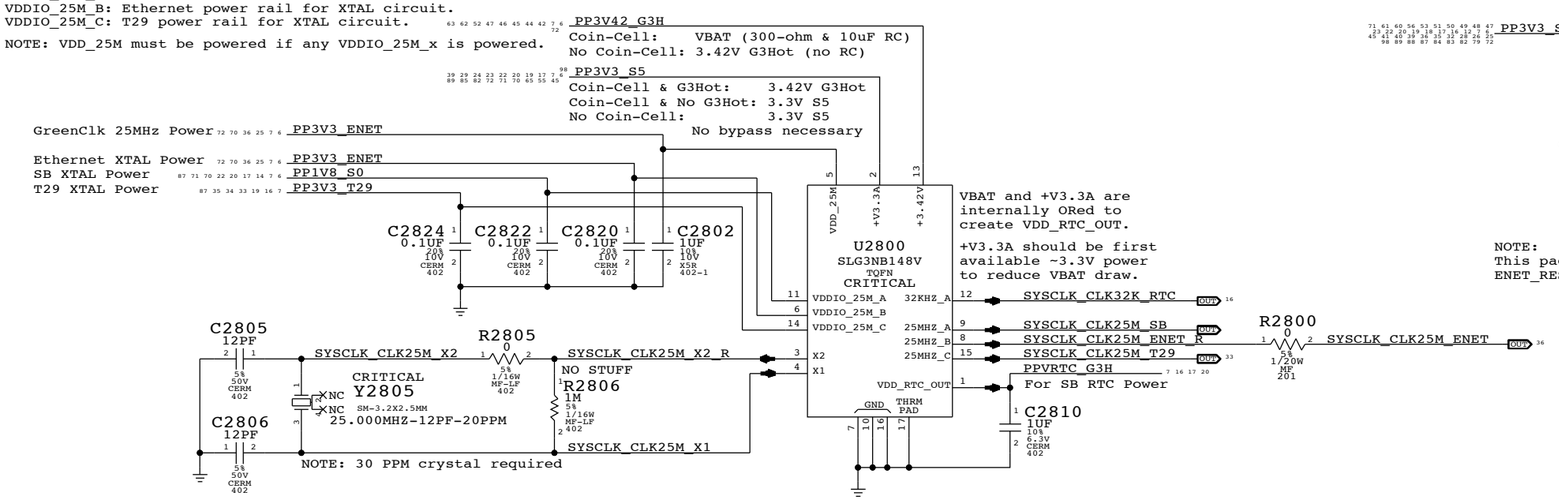


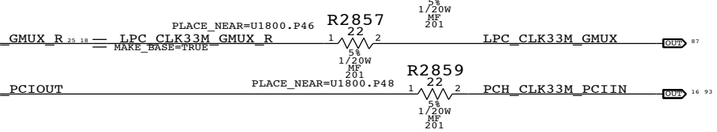
NOTE:
This page is different for K92.
ENET_RESET_L hooked up differently on both the projects.

System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.





SYNC_MASTER=K92_MLB	SYNC_DATE=07/06/2010
PAGE TITLE: Chipset Support	
Apple Inc.	DRAWING NUMBER: SIZE D
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	BRANCH:
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S3_MEM_VTT_A
- =PP5PD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

PLACE_NEAR=J2900.75:2.54mm

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603

PLACE_NEAR=J2900.75:2.54mm

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

OMIT_TABLE

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2)

MEM_A_CKE<0>	73 CKE0	CKE1 74	MEM_A_CKE<1>
NC	75 VDD	VDD 76	
MEM_A_BA<2>	77 NC	A15 78	MEM_A_A<15>
	79 BA2	A14 80	MEM_A_A<14>
MEM_A_A<12>	81 VDD	VDD 82	
MEM_A_A<9>	83 A12/BC*	A11 84	MEM_A_A<11>
	85 A9	A7 86	MEM_A_A<7>
MEM_A_A<8>	87 VDD	VDD 88	
MEM_A_A<5>	89 A8	A6 90	MEM_A_A<6>
	91 A5	A4 92	MEM_A_A<4>
MEM_A_A<3>	93 VDD	VDD 94	
MEM_A_A<1>	95 A3	A2 96	MEM_A_A<2>
	97 A1	A0 98	MEM_A_A<0>
MEM_A_CLK_P<0>	99 VDD	VDD 100	
MEM_A_CLK_N<0>	101 CK0	CK1 102	MEM_A_CLK_P<1>
	103 CK0*	CK1* 104	MEM_A_CLK_N<1>
MEM_A_A<10>	105 VDD	VDD 106	
MEM_A_BA<0>	107 A10/AP	BA1 108	MEM_A_BA<1>
	109 BA0	RAS* 110	MEM_A_RAS_L
MEM_A_WE_L	111 VDD	VDD 112	
MEM_A_CAS_L	113 WE*	S0* 114	MEM_A_CS_L<0>
	115 CAS*	ODT0 116	MEM_A_ODT<0>
MEM_A_A<13>	117 VDD	VDD 118	
MEM_A_CS_L<1>	119 A13	ODT1 120	MEM_A_ODT<1>
NC	121 S1*	NC 122	NC
	123 VDD	VDD 124	
NC	125 TEST	VREFCA 126	
	127 VSS	VSS 128	
=MEM_A_DQ<32>	129 DQ32	DQ36 130	MEM_A_DQ<32>
=MEM_A_DQ<33>	131 DQ33	DQ37 132	=MEM_A_DQ<37>
	133 VSS	VSS 134	
=MEM_A_DQS_N<4>	135 DQS4*	DM4 136	
=MEM_A_DQS_P<4>	137 DQS4	VSS 138	
	139 VSS	DQ38 140	=MEM_A_DQ<38>
=MEM_A_DQ<34>	141 DQ34	DQ39 142	=MEM_A_DQ<39>
=MEM_A_DQ<35>	143 DQ35	VSS 144	
	145 VSS	DQ44 146	=MEM_A_DQ<44>
=MEM_A_DQ<40>	147 DQ40	DQ45 148	=MEM_A_DQ<45>
=MEM_A_DQ<41>	149 DQ41	VSS 150	
	151 VSS	DQS5* 152	=MEM_A_DQS_N<5>
	153 DM5	DQS5 154	=MEM_A_DQS_P<5>
	155 VSS	VSS 156	
=MEM_A_DQ<42>	157 DQ42	DQ46 158	=MEM_A_DQ<46>
=MEM_A_DQ<43>	159 DQ43	DQ47 160	=MEM_A_DQ<47>
	161 VSS	VSS 162	
=MEM_A_DQ<48>	163 DQ48	DQ52 164	=MEM_A_DQ<52>
=MEM_A_DQ<49>	165 DQ49	DQ53 166	=MEM_A_DQ<53>
	167 VSS	VSS 168	
MEM_A_DQS_N<6>	169 DQS6*	DM6 170	
MEM_A_DQS_P<6>	171 DQS6	VSS 172	
	173 VSS	DQ54 174	=MEM_A_DQ<54>
=MEM_A_DQ<50>	175 DQ50	DQ55 176	=MEM_A_DQ<55>
=MEM_A_DQ<51>	177 DQ51	VSS 178	
	179 VSS	DQ60 180	=MEM_A_DQ<60>
=MEM_A_DQ<56>	181 DQ56	DQ61 182	=MEM_A_DQ<61>
=MEM_A_DQ<57>	183 DQ57	VSS 184	
	185 VSS	DQS7* 186	=MEM_A_DQS_N<7>
	187 DM7	DQS7 188	=MEM_A_DQS_P<7>
	189 VSS	VSS 190	
=MEM_A_DQ<58>	191 DQ58	DQ62 192	=MEM_A_DQ<62>
=MEM_A_DQ<59>	193 DQ59	DQ63 194	=MEM_A_DQ<63>
	195 VSS	VSS 196	
MEM_A_SA<0>	197 SA0	EVENT* 198	MEM_EVENT_L
	199 VDDSPD	SDA 200	SMBUS_PCH_DATA
MEM_A_SA<1>	201 SA1	SCL 202	SMBUS_PCH_CLK
	203 VTT	VTT 204	

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

OMIT_TABLE

J2900 CRITICAL F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2)

	1 VREFDQ	VSS 2	
=MEM_A_DQ<0>	3 VSS	DQ4 4	=MEM_A_DQ<4>
=MEM_A_DQ<1>	5 DQ0	DQ5 6	=MEM_A_DQ<5>
	7 DQ1	VSS 8	
	9 VSS	DQS0* 10	=MEM_A_DQS_N<0>
	11 DM0	DQS0 12	=MEM_A_DQS_P<0>
=MEM_A_DQ<2>	13 VSS	VSS 14	
=MEM_A_DQ<3>	15 DQ2	DQ6 16	=MEM_A_DQ<6>
	17 DQ3	DQ7 18	=MEM_A_DQ<7>
=MEM_A_DQ<8>	19 VSS	VSS 20	
=MEM_A_DQ<9>	21 DQ8	DQ12 22	=MEM_A_DQ<12>
	23 DQ9	DQ13 24	=MEM_A_DQ<13>
=MEM_A_DQS_N<1>	25 VSS	VSS 26	
=MEM_A_DQS_P<1>	27 DQS1*	DM1 28	
	29 DQS1	RESET* 30	MEM_RESET_L
=MEM_A_DQ<10>	31 VSS	VSS 32	
=MEM_A_DQ<11>	33 DQ10	DQ14 34	=MEM_A_DQ<14>
	35 DQ11	DQ15 36	=MEM_A_DQ<15>
=MEM_A_DQ<16>	37 VSS	VSS 38	
=MEM_A_DQ<17>	39 DQ16	DQ20 40	=MEM_A_DQ<20>
	41 DQ17	DQ21 42	=MEM_A_DQ<21>
=MEM_A_DQS_N<2>	43 VSS	VSS 44	
=MEM_A_DQS_P<2>	45 DQS2*	DM2 46	
	47 DQS2	VSS 48	
=MEM_A_DQ<18>	49 VSS	DQ22 50	=MEM_A_DQ<22>
=MEM_A_DQ<19>	51 DQ18	DQ23 52	=MEM_A_DQ<23>
	53 DQ19	VSS 54	
=MEM_A_DQ<24>	55 VSS	DQ28 56	=MEM_A_DQ<28>
=MEM_A_DQ<25>	57 DQ24	DQ29 58	=MEM_A_DQ<29>
	59 DQ25	VSS 60	
	61 VSS	DQS3* 62	=MEM_A_DQS_N<3>
	63 DM3	DQS3 64	=MEM_A_DQS_P<3>
=MEM_A_DQ<26>	65 VSS	VSS 66	
=MEM_A_DQ<27>	67 DQ26	DQ30 68	=MEM_A_DQ<30>
	69 DQ27	DQ31 70	=MEM_A_DQ<31>
	71 VSS	VSS 72	

See CSA05 BOM table

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

PP0V75_S0_DDRVTT

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

"Factory" (top) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

91 11 6	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	26
91 11 6	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	26
91 11 6	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	26
91 11 6	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	26
91 11 6	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	26
91 11 6	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	26
91 11 6	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	26
91 11 6	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	26
91 11 6	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	26
91 11 6	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	26

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

91 11 6	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	26
91 11 6	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	26
91 11 6	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	26
91 11 6	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	26
91 11 6	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	26
91 11 6	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	26
91 11 6	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	26
91 11 6	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	26
91 11 6	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	26
91 11 6	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	26

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

91 11 6	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	26
91 11 6	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	26
91 11 6	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	26
91 11 6	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	26
91 11 6	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	26
91 11 6	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	26
91 11 6	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	26
91 11 6	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	26
91 11 6	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	26
91 11 6	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	26

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

91 11 6	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	26
91 11 6	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	26
91 11 6	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	26
91 11 6	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	26
91 11 6	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	26
91 11 6	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	26
91 11 6	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	26
91 11 6	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	26
91 11 6	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	26
91 11 6	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	26

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

91 11 6	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	26
91 11 6	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	26
91 11 6	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	26
91 11 6	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	26
91 11 6	MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	26
91 11 6	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	26
91 11 6	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	26
91 11 6	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	26
91 11 6	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	26
91 27 26 11 6	MEM_A_DQ<32>	MAKE_BASE=TRUE	MEM_A_DQ<32>	6 11 26 27 91

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

91 11 6	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	26
91 11 6	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	26
91 11 6	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	26
91 11 6	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	26
91 11 6	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	26
91 11 6	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	26
91 11 6	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	26
91 11 6	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	26
91 11 6	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	26
91 11 6	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	26

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

91 27 26 11 6	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	MEM_A_DQS_N<6>	6 11 26 27 91
91 27 26 11 6	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	MEM_A_DQS_P<6>	6 11 26 27 91
91 11 6	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	26
91 11 6	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	26
91 11 6	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	26
91 11 6	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	26
91 11 6	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	26
91 11 6	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	26
91 11 6	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	26
91 11 6	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	26

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

91 11 6	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	26
91 11 6	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	26
91 11 6	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	26
91 11 6	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	26
91 11 6	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	26
91 11 6	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	26
91 11 6	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	26
91 11 6	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	26
91 11 6	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	26
91 11 6	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	26

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

91 11 6	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	28
91 11 6	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	28
91 11 6	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	28
91 11 6	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	28
91 11 6	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	28
91 11 6	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	28
91 11 6	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	28
91 11 6	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	28
91 11 6	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	28
91 11 6	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	28

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

91 11 6	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	28
91 11 6	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	28
91 11 6	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	28
91 11 6	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	28
91 11 6	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	28
91 11 6	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	28
91 11 6	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	28
91 11 6	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	28
91 11 6	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	28
91 11 6	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	28

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

91 11 6	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	28
91 11 6	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	28
91 11 6	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	28
91 11 6	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	28
91 11 6	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	28
91 11 6	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	28
91 11 6	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	28
91 11 6	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	28
91 11 6	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	28
91 11 6	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	28

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

91 11 6	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	28
91 11 6	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	28
91 11 6	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	28
91 11 6	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	28
91 11 6	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	28
91 11 6	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	28
91 11 6	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	28
91 11 6	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	28
91 11 6	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	28
91 11 6	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	28

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

91 11 6	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	28
91 11 6	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	28
91 11 6	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	28
91 11 6	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	28
91 11 6	MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	28
91 11 6	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	28
91 11 6	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	28
91 11 6	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	28
91 11 6	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	28
27 11 6 91 28	MEM_B_DQ<32>	MAKE_BASE=TRUE	MEM_B_DQ<32>	6 11 27 28 91

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

91 11 6	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	28
91 11 6	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	28
91 11 6	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	28
91 11 6	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	28
91 11 6	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	28
91 11 6	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	28
91 11 6	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	28
91 11 6	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	28
91 11 6	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	28
91 11 6	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	28

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

27 11 6 91 28	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	MEM_B_DQS_N<6>	6 11 27 28 91
27 11 6 91 28	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	MEM_B_DQS_P<6>	6 11 27 28 91
91 11 6	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	28
91 11 6	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	28
91 11 6	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	28
91 11 6	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	28
91 11 6	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	28
91 11 6	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	28
91 11 6	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	28
91 11 6	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	28

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

91 11 6	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	28
91 11 6	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	28
91 11 6	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	28
91 11 6	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	28
91 11 6	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	28
91 11 6	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	28
91 11 6	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	28
91 11 6	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	28
91 11 6	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	28
91 11 6	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	28

SYNC MASTER=K92 SUMA SYNC DATE=05/10/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

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REVISION:

BRANCH:

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

PLACE_NEAR=J3100.75:2.54mm

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603

PLACE_NEAR=J3100.75:2.54mm

PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (2 OF 2)

MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>
	75	VDD	VDD	76	
NC	77	NC	A15	78	MEM_B_A<15>
MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>
	81	VDD	VDD	82	
MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>
MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>
	87	VDD	VDD	88	
MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>
MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>
	93	VDD	VDD	94	
MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>
MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>
	99	VDD	VDD	100	
MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>
MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>
	105	VDD	VDD	106	
MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>
MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L
	111	VDD	VDD	112	
MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>
MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>
	117	VDD	VDD	118	
MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>
MEM_B_CS_L<1>	121	S1*	NC	122	NC
	123	VDD	VDD	124	
NC	125	TEST	VREFCA	126	
	127	VSS	VSS	128	
MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>
=MEM_B_DQ<33>	131	DQ33	DQ37	132	=MEM_B_DQ<37>
	133	VSS	VSS	134	
=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	
=MEM_B_DQS_P<4>	137	DQS4	VSS	138	
	139	VSS	DQ38	140	=MEM_B_DQ<38>
=MEM_B_DQ<34>	141	DQ34	DQ39	142	=MEM_B_DQ<39>
=MEM_B_DQ<35>	143	DQ35	VSS	144	
	145	VSS	DQ44	146	=MEM_B_DQ<44>
=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>
=MEM_B_DQ<41>	149	DQ41	VSS	150	
	151	VSS	DQS5*	152	=MEM_B_DQS_N<5>
	153	DM5	DQS5	154	=MEM_B_DQS_P<5>
	155	VSS	VSS	156	
=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>
=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>
	161	VSS	VSS	162	
=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>
=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>
	167	VSS	VSS	168	
MEM_B_DQS_N<6>	169	DQS6*	DM6	170	
MEM_B_DQS_P<6>	171	DQS6	VSS	172	
	173	VSS	DQ54	174	=MEM_B_DQ<54>
=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>
=MEM_B_DQ<51>	177	DQ51	VSS	178	
	179	VSS	DQ60	180	=MEM_B_DQ<60>
=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>
=MEM_B_DQ<57>	183	DQ57	VSS	184	
	185	VSS	DQS7*	186	=MEM_B_DQS_N<7>
	187	DM7	DQS7	188	=MEM_B_DQS_P<7>
	189	VSS	VSS	190	
=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>
=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>
	195	VSS	VSS	196	
MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L
PP3V3_S0	199	VDDSPD	SDA	200	SMBUS_PCH_DATA
MEM_B_SA<1>	201	SA1	SCL	202	SMBUS_PCH_CLK
	203	VTT	VTT	204	PP0V75_S0_DDRVTT
	205	MTG PIN	MTG PIN	206	
	207	MTG PIN	MTG PIN	208	
	209	MTG PIN	MTG PIN	210	
	211	MTG PIN	MTG PIN	212	

516S0806

SPD ADDR=0xA4(WR)/0xA5(RD)

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (1 OF 2) CRITICAL

	1	VREFDQ	VSS	2	
=MEM_B_DQ<0>	3	VSS	DQ4	4	=MEM_B_DQ<4>
=MEM_B_DQ<1>	5	DQ0	DQ5	6	=MEM_B_DQ<5>
	7	DQ1	VSS	8	
	9	VSS	DQS0*	10	=MEM_B_DQS_N<0>
	11	DM0	DQS0	12	=MEM_B_DQS_P<0>
	13	VSS	VSS	14	
=MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6>
=MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7>
	19	VSS	VSS	20	
=MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12>
=MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13>
	25	VSS	VSS	26	
=MEM_B_DQS_N<1>	27	DQS1*	DM1	28	
=MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L
	31	VSS	VSS	32	
=MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14>
=MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15>
	37	VSS	VSS	38	
=MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20>
=MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21>
	43	VSS	VSS	44	
=MEM_B_DQS_N<2>	45	DQS2*	DM2	46	
=MEM_B_DQS_P<2>	47	DQS2	VSS	48	
	49	VSS	DQ22	50	=MEM_B_DQ<22>
=MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23>
=MEM_B_DQ<19>	53	DQ19	VSS	54	
	55	VSS	DQ28	56	=MEM_B_DQ<28>
=MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29>
=MEM_B_DQ<25>	59	DQ25	VSS	60	
	61	VSS	DQS3*	62	=MEM_B_DQS_N<3>
	63	DM3	DQS3	64	=MEM_B_DQS_P<3>
	65	VSS	VSS	66	
=MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30>
=MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31>
	71	VSS	VSS	72	

516S0806

PP0V75_S3_MEM_VREFCA_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

"Expansion" (bottom) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE
DDR3 SO-DIMM Connector B

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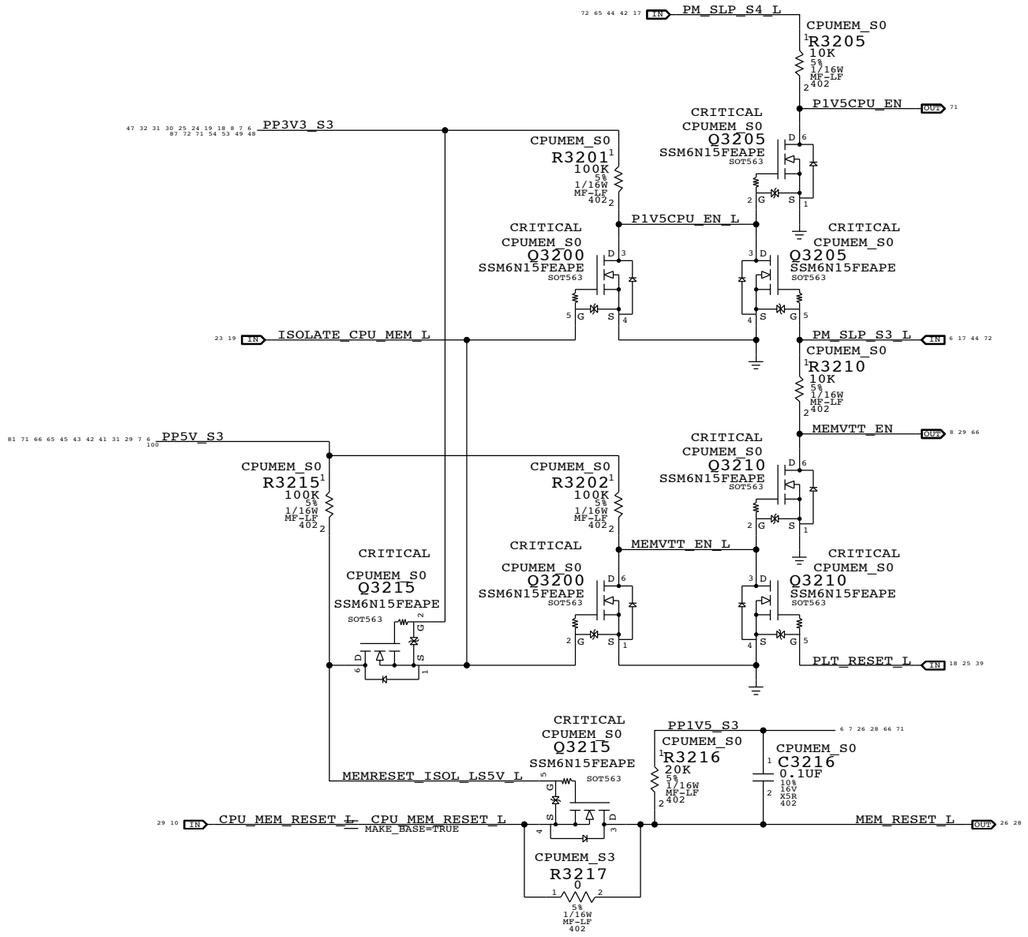
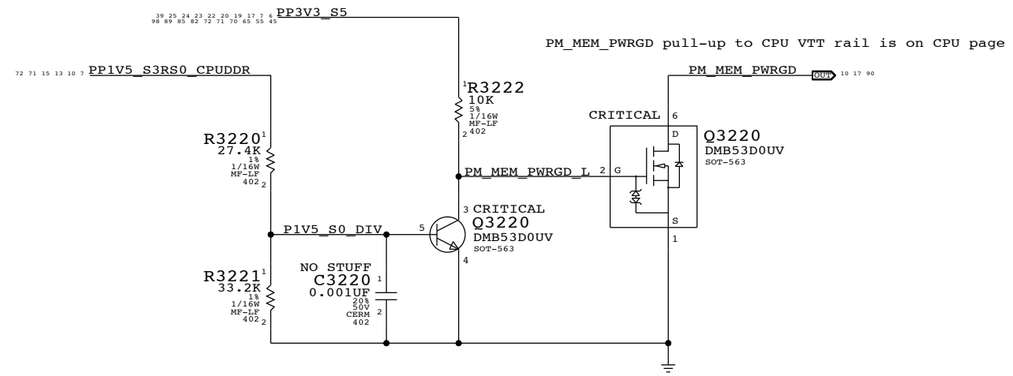
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

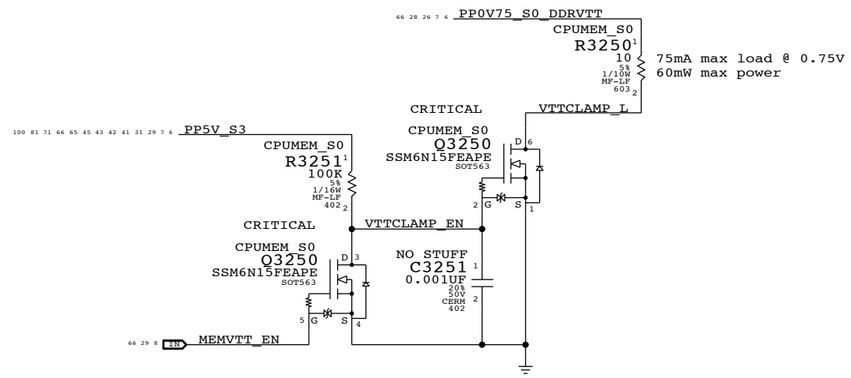


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: CPU Memory S3 Support

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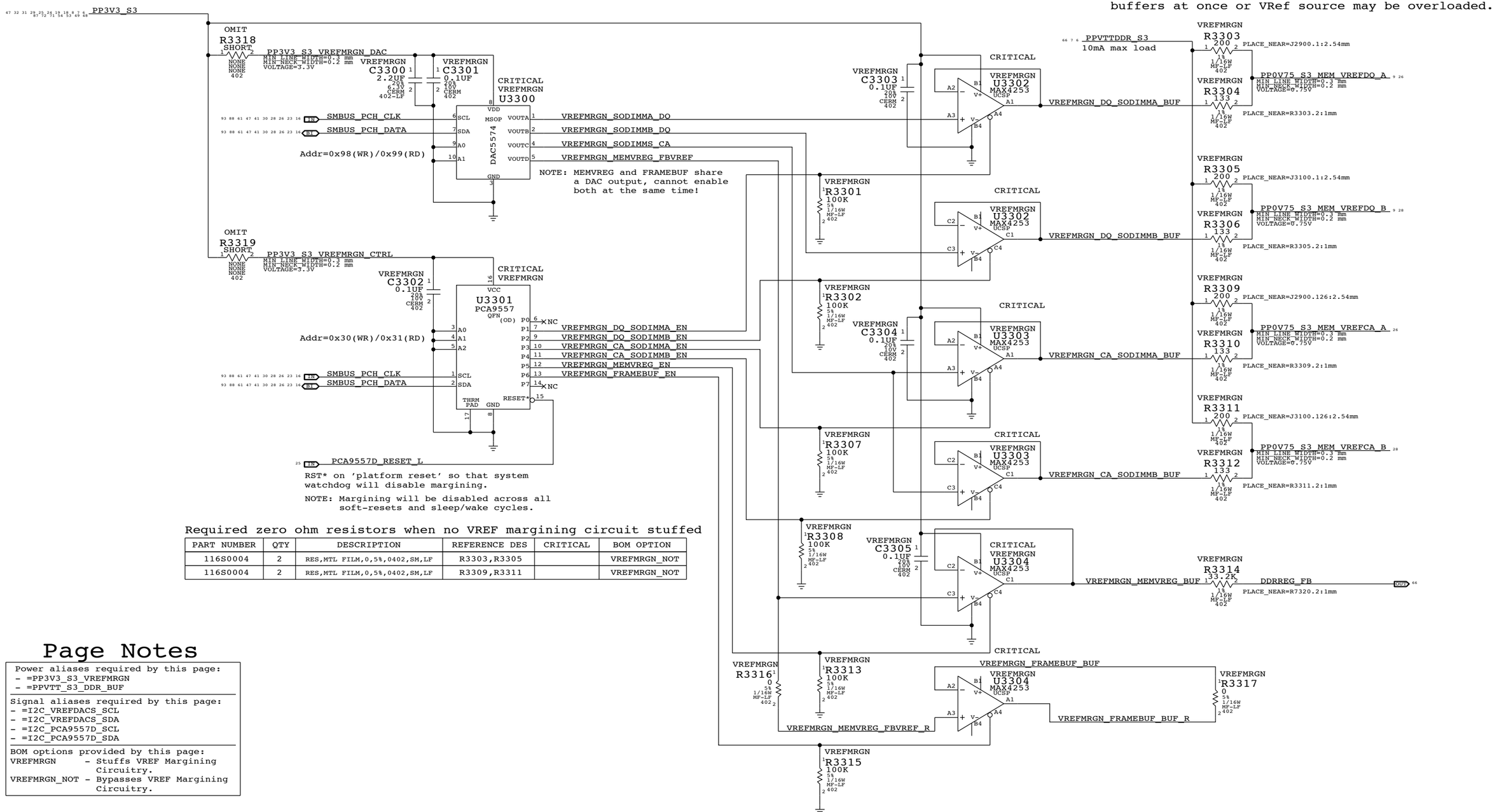

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

AIRPORT

BLUETOOTH

ALS CAMERA

Supervisor & CLKFREG # Isolation

Delay = 60 ms +/- 20%

275 mA peak
206 mA nominal max

SYNC MASTER=K91 MARY SYNC DATE=10/08/2010

PAGE TITLE: X19/ALS/CAMERA CONNECTOR

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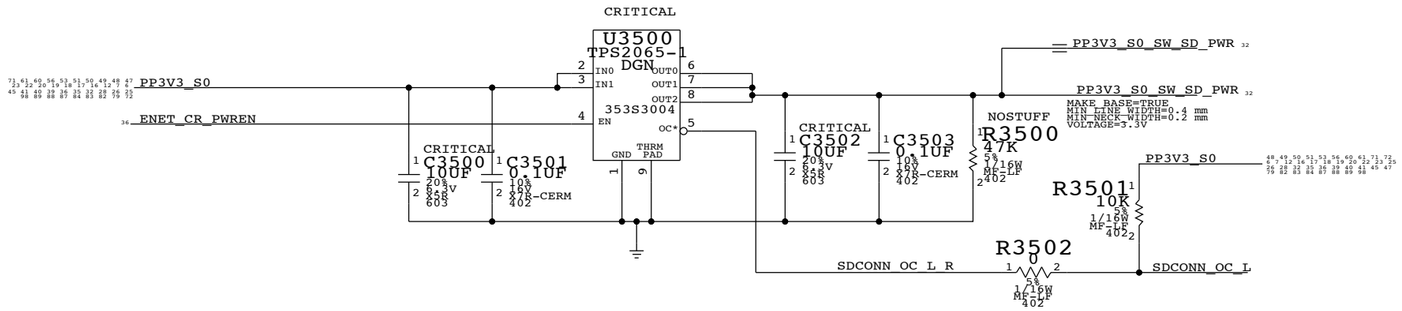
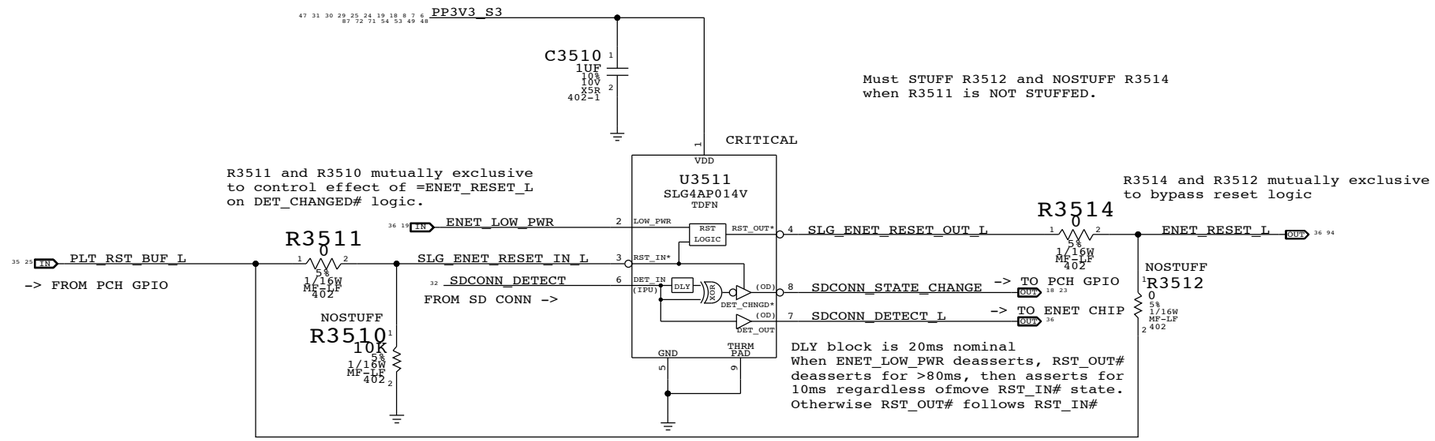
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

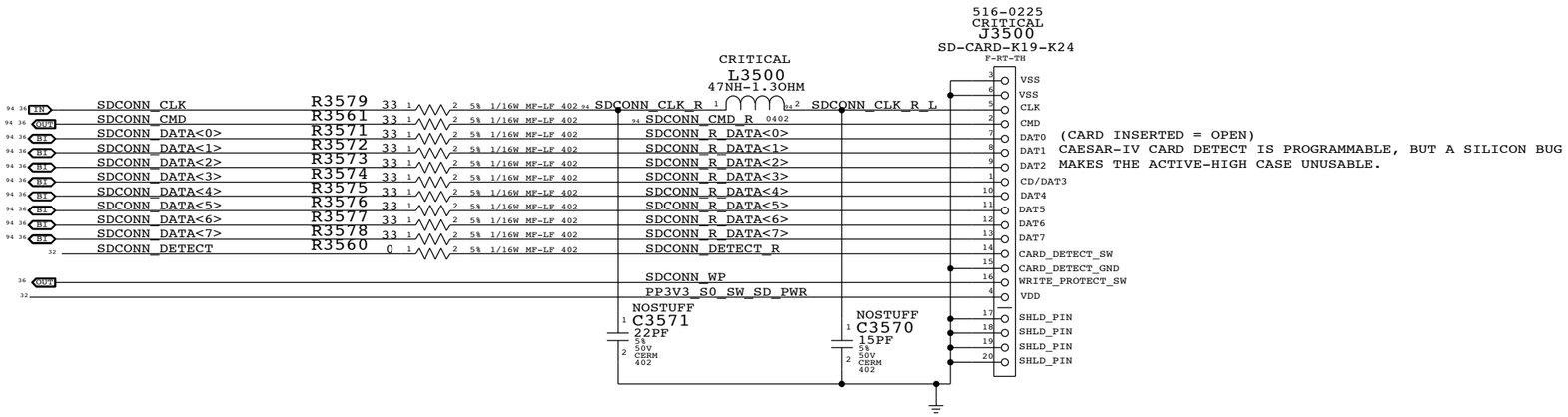
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT



SD CARD CONNECTOR



SYNC MASTER=K91 ERIC SYNC DATE=10/08/2010

PAGE TITLE

SD READER CONNECTOR

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CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_T29_R2D_C_P<0>	C3600 0.1uF	PCIE_T29_R2D_P<0>	V19 PER_0_P
PCIE_T29_R2D_C_N<0>	C3601 0.1uF	PCIE_T29_R2D_N<0>	T19 PER_0_N
PCIE_T29_R2D_C_P<1>	C3602 0.1uF	PCIE_T29_R2D_P<1>	P19 PER_1_P
PCIE_T29_R2D_C_N<1>	C3603 0.1uF	PCIE_T29_R2D_N<1>	M19 PER_1_N
PCIE_T29_R2D_C_P<2>	C3604 0.1uF	PCIE_T29_R2D_P<2>	K19 PER_2_P
PCIE_T29_R2D_C_N<2>	C3605 0.1uF	PCIE_T29_R2D_N<2>	H19 PER_2_N
PCIE_T29_R2D_C_P<3>	C3606 0.1uF	PCIE_T29_R2D_P<3>	F19 PER_3_P
PCIE_T29_R2D_C_N<3>	C3607 0.1uF	PCIE_T29_R2D_N<3>	D19 PER_3_N

TRANSMIT

PCIE_T29_D2R_C_P<0>	C3640 0.1uF	PCIE_T29_D2R_P<0>	V21 PET_0_P
PCIE_T29_D2R_C_N<0>	C3641 0.1uF	PCIE_T29_D2R_N<0>	T21 PET_0_N
PCIE_T29_D2R_C_P<1>	C3642 0.1uF	PCIE_T29_D2R_P<1>	P21 PET_1_P
PCIE_T29_D2R_C_N<1>	C3643 0.1uF	PCIE_T29_D2R_N<1>	M21 PET_1_N
PCIE_T29_D2R_C_P<2>	C3644 0.1uF	PCIE_T29_D2R_P<2>	K21 PET_2_P
PCIE_T29_D2R_C_N<2>	C3645 0.1uF	PCIE_T29_D2R_N<2>	H21 PET_2_N
PCIE_T29_D2R_C_P<3>	C3646 0.1uF	PCIE_T29_D2R_P<3>	F21 PET_3_P
PCIE_T29_D2R_C_N<3>	C3647 0.1uF	PCIE_T29_D2R_N<3>	D21 PET_3_N

NO STUFF
TP_T29_MONDC0 — R3610 0 — T29_MONDC0 — B21 MONDC0
DEBUG: For monitoring current/voltage
TP_T29_MONDC1 — R3611 0 — T29_MONDC1 — A20 MONDC1
NO STUFF
TP_T29_MONOBSP — C3615 0.1uF — T29_MONOBSP — K17 MONOBSP
DEBUG: For monitoring clock
TP_T29_MONOBSN — C3616 0.1uF — T29_MONOBSN — M17 MONOBSN

WAKE* F1 T29_PCIE_WAKE_L — R3651 10K — PP3V3_T29
PERST* E6 T29_RESET_L
RSENSE E14 T29_RSENSE — R3655 1.0K 0.5% 1/16W MF-LF 603
RBIAS E16 T29_RBIAS

PP3V3_T29 — R3690 3.3K, R3691 3.3K, C3690 1UF 10% 6.3V CERM 402, R3692 3.3K, R3623 10K, R3622 10K, R3621 10K

CRITICAL
OMIT_TABLE
U3690
M95160
2KX8-1.8V
MLP

(T29_SPI_MOSI) D
(T29_SPI_CLK) C
(T29_SPI_CS_L) S_L
T29ROM_WP_L W_L
T29ROM_HOLD_L HOLD_L
(T29_SPI_MISO) Q
VCC, VSS, THM PAD

R3693 3.3K

T29_CLKREQ_ISOL_L — P3 PCIE_CLKREQ_0*
T29_GPIO<1> — N4 PCIE_CLKREQ_1*
T29_GPIO<2> — M3 PCIE_CLKREQ_2*
T29_RSVD — L4 PCIE_CLKREQ_3*

CLK REQUEST

T29_SPI_MOSI — P1 EE_DI
T29_SPI_MISO — M1 EE_DO
T29_SPI_CS_L — N2 EE_CS*
T29_SPI_CLK — L2 EE_CLK

EEPROM

T29_THERMD_P — A2 THERM_DP
Use B1 GND ball for THERM_DN
T29_TEST_EN — E4 TEST_EN
TP_T29_TEST_POINT_0 — P5 TEST_POINT_0
TP_T29_TEST_POINT_1 — N6 TEST_POINT_1
TP_T29_TEST_POINT_2 — M5 TEST_POINT_2
T29_TEST_POINT_3 — L6 TEST_POINT_3

TEST PORT

R3625 0
R3629 0

DP_T29SNK0_ML_P<3> — AA4 DPSNK0_ML_LANE_3P
DP_T29SNK0_ML_N<3> — Y3 DPSNK0_ML_LANE_3N
DP_T29SNK0_ML_P<2> — AA6 DPSNK0_ML_LANE_2P
DP_T29SNK0_ML_N<2> — Y5 DPSNK0_ML_LANE_2N
DP_T29SNK0_ML_P<1> — AA8 DPSNK0_ML_LANE_1P
DP_T29SNK0_ML_N<1> — Y7 DPSNK0_ML_LANE_1N
DP_T29SNK0_ML_P<0> — AA10 DPSNK0_ML_LANE_0P
DP_T29SNK0_ML_N<0> — Y9 DPSNK0_ML_LANE_0N
DP_T29SNK0_AUXCH_P — V1 DPSNK0_AUX_CHP
DP_T29SNK0_AUXCH_N — W2 DPSNK0_AUX_CHN
DP_T29SNK0_HPD — V5 DPSNK0_HOT_PLUG_DET

SINK PORT 0

R3630 100K

DP_T29SNK1_ML_P<3> — V9 DPSNK1_ML_LANE_3P
DP_T29SNK1_ML_N<3> — U8 DPSNK1_ML_LANE_3N
DP_T29SNK1_ML_P<2> — V11 DPSNK1_ML_LANE_2P
DP_T29SNK1_ML_N<2> — U10 DPSNK1_ML_LANE_2N
DP_T29SNK1_ML_P<1> — V13 DPSNK1_ML_LANE_1P
DP_T29SNK1_ML_N<1> — U12 DPSNK1_ML_LANE_1N
DP_T29SNK1_ML_P<0> — V15 DPSNK1_ML_LANE_0P
DP_T29SNK1_ML_N<0> — U14 DPSNK1_ML_LANE_0N
DP_T29SNK1_AUXCH_P — V7 DPSNK1_AUX_CHP
DP_T29SNK1_AUXCH_N — U6 DPSNK1_AUX_CHN
DP_T29SNK1_HPD — U4 DPSNK1_HOT_PLUG_DET

SINK PORT 1

R3631 100K

DISPLAY

SOURCE PORT 0

DPSRC0_ML_LANE_3P — AA18 TP_DP_T29SRC_ML_CP<3>
DPSRC0_ML_LANE_3N — Y17 TP_DP_T29SRC_ML_CN<3>
DPSRC0_ML_LANE_2P — AA16 TP_DP_T29SRC_ML_CP<2>
DPSRC0_ML_LANE_2N — Y15 TP_DP_T29SRC_ML_CN<2>
DPSRC0_ML_LANE_1P — AA14 TP_DP_T29SRC_ML_CP<1>
DPSRC0_ML_LANE_1N — Y13 TP_DP_T29SRC_ML_CN<1>
DPSRC0_ML_LANE_0P — AA12 TP_DP_T29SRC_ML_CP<0>
DPSRC0_ML_LANE_0N — Y11 TP_DP_T29SRC_ML_CN<0>
DPSRC0_AUX_CHP — W16 TP_DP_T29SRC_AUXCH_CP
DPSRC0_AUX_CHN — U16 TP_DP_T29SRC_AUXCH_CN
DPSRC0_HOT_PLUG_DET — V3 DP_T29SRC_HPD

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm

DP_ATEST — Y19 T29_DP_ATEST
DP_RES_0 — Y21
DP_RES_1 — AA20 T29_DP_RES

R3685 14.0K 1% 1/16W MF-LF 402
R3632 100K 5% 1/16W MF-LF 402
C3685 100PF 5% 50V CERM 402
C3686 0.01UF 10% 16V CERM 402

MISC

POWER ON RESET

PCIE_RST_0* — K1 TP_T29_PCIE_RESET0_L
PCIE_RST_1* — J2 TP_T29_PCIE_RESET1_L
PCIE_RST_2* — K3 TP_T29_PCIE_RESET2_L
PCIE_RST_3* — J4 TP_T29_PCIE_RESET3_L

Not used in host mode.

JTAG

TDI — T3 JTAG_ISP_TDI
TMS — R4 JTAG_T29_TMS
TCK — R2 JTAG_ISP_TCK
TDO — T1 JTAG_ISP_TDO

CLOCKS

REFCLK_100_IN_P — H17 PCIE_CLK100M_T29_P
REFCLK_100_IN_N — G16 PCIE_CLK100M_T29_N
XTAL_25_IN — P17 SYSCLK_CLK25M_T29_R
XTAL_25_OUT — R16 TP_T29_XTAL25OUT
TMU_CLK_OUT — U2 T29_TMU_CLK_OUT
TMU_CLK_IN — E2 T29_TMU_CLK_IN

PP3V3_T29 — R3698 10K — R3696 1K — R3695 806 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_T29
NO STUFF
R3699 10K

PORTS

PORT2

PRT2_T29T_P — A14 NC_T29_R2D_CP<2>
PRT2_T29T_N — A12 NC_T29_R2D_CN<2>
PRT2_T29R_P — C12 NC_T29_D2RP<2>
PRT2_T29R_N — C10 NC_T29_D2RN<2>
T29_2_LSEO — G4 T29_LSEO_LSOE2
T29_2_LSOE — H3 T29_LSEO_LSOE2

PORT3

PRT3_T29T_P — A18 NC_T29_R2D_CP<3>
PRT3_T29T_N — A16 NC_T29_R2D_CN<3>
PRT3_T29R_P — C16 NC_T29_D2RP<3>
PRT3_T29R_N — C14 NC_T29_D2RN<3>
T29_3_LSEO — G2 T29_LSEO_LSOE3
T29_3_LSOE — H1 T29_LSEO_LSOE3

PORT0

T29_R2D_C_P<0> — A6
T29_R2D_C_N<0> — A4
T29_D2R_P<0> — C4
T29_D2R_N<0> — C2
T29_LSEO<0> — J6
T29_LSOE<0> — K5

PORT1

T29_R2D_C_P<1> — A10
T29_R2D_C_N<1> — A8
T29_D2R_P<1> — C8
T29_D2R_N<1> — C6
T29_LSEO<1> — G6
T29_LSOE<1> — H5

I2C_T29_SDA — F3 T29_SDA
I2C_T29_SCL — F5 T29_SCL

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SNK0 AC Coupling

DP_T29SNK0_ML_C_P<0>	C3620 0.1uF	DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_C_N<0>	C3621 0.1uF	DP_T29SNK0_ML_N<0>
DP_T29SNK0_ML_C_P<1>	C3622 0.1uF	DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_C_N<1>	C3623 0.1uF	DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_C_P<2>	C3624 0.1uF	DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_C_N<2>	C3625 0.1uF	DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_C_P<3>	C3626 0.1uF	DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_C_N<3>	C3627 0.1uF	DP_T29SNK0_ML_N<3>
DP_T29SNK0_AUXCH_C_P	C3628 0.1uF	DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_C_N	C3629 0.1uF	DP_T29SNK0_AUXCH_N

SNK1 AC Coupling

DP_T29SNK1_ML_C_P<0>	C3630 0.1uF	DP_T29SNK1_ML_P<0>
DP_T29SNK1_ML_C_N<0>	C3631 0.1uF	DP_T29SNK1_ML_N<0>
DP_T29SNK1_ML_C_P<1>	C3632 0.1uF	DP_T29SNK1_ML_P<1>
DP_T29SNK1_ML_C_N<1>	C3633 0.1uF	DP_T29SNK1_ML_N<1>
DP_T29SNK1_ML_C_P<2>	C3634 0.1uF	DP_T29SNK1_ML_P<2>
DP_T29SNK1_ML_C_N<2>	C3635 0.1uF	DP_T29SNK1_ML_N<2>
DP_T29SNK1_ML_C_P<3>	C3636 0.1uF	DP_T29SNK1_ML_P<3>
DP_T29SNK1_ML_C_N<3>	C3637 0.1uF	DP_T29SNK1_ML_N<3>
DP_T29SNK1_AUXCH_C_P	C3638 0.1uF	DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_C_N	C3639 0.1uF	DP_T29SNK1_AUXCH_N

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (1 of 2)

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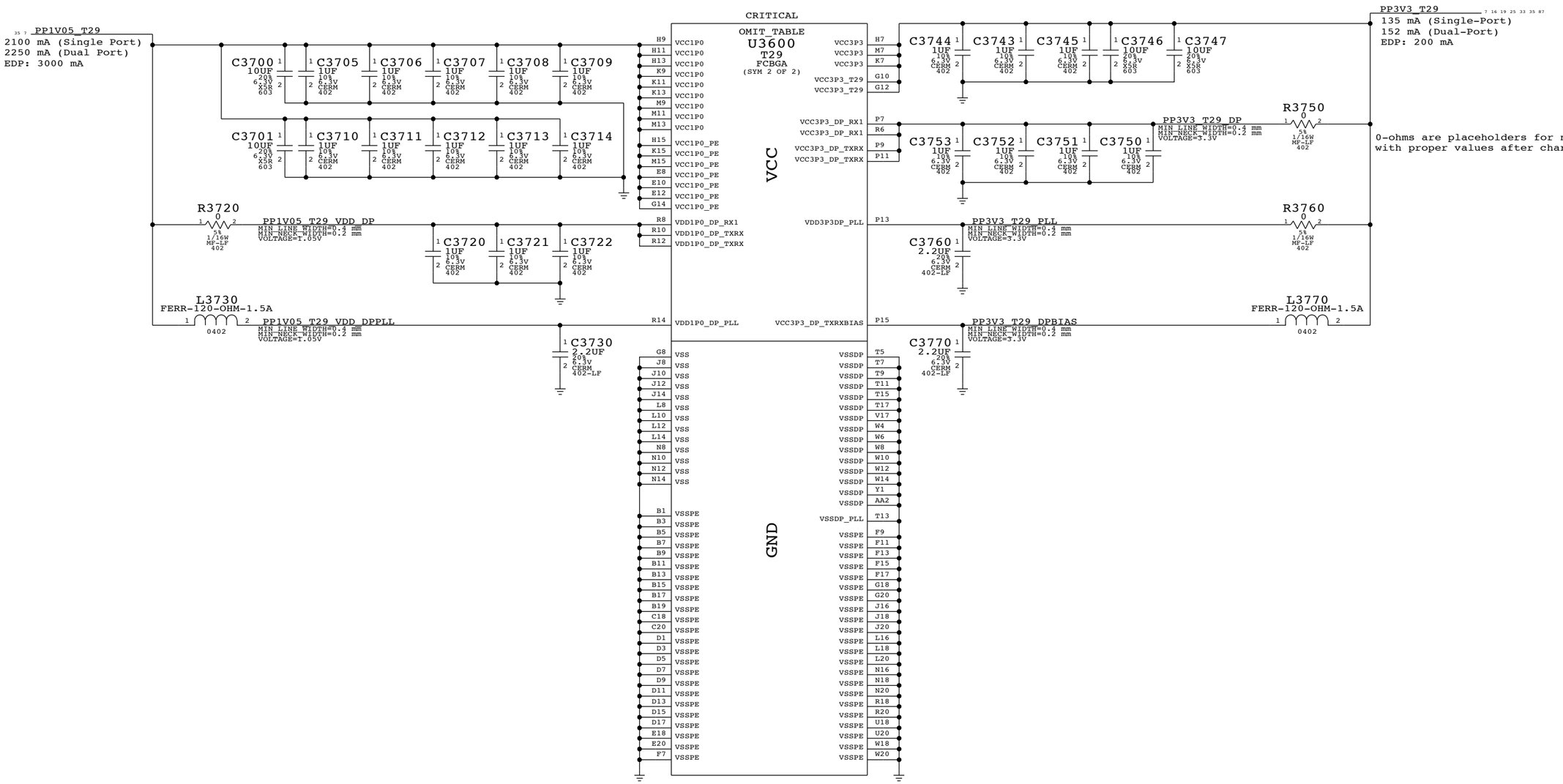

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (2 of 2)

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPBUS_G3H
8-13V Input
Changes required for 2S.

Q3880 SI8409DB BGA
R3880 470K 5% 1/16W MF-LF 402
C3880 0.1UF 10% 25V X5R 402
R3881 330K 5% 1/16W MF-LF 402
Q3805 SSM3K15FV SOD-VESM-HF
T29_A_HV_EN

PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

C3890 10UF 10% 25V X5R 805
C3891 10UF 10% 25V X5R 805
R3891 200K 1% 1/16W MF-LF 402 <R1>
R3892 73.2K 1% 1/16W MF-LF 402 <R2>

L3895 10UH-4A-68-MOHM PCMB063T-100MS
T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

D3895 POWERDI-123 DFLS230L

U3890 LT3957 QFN
VIN, SW, SNS1, SNS2, EN/UVLO, INTVCC, VC, RT, SS, SYNC, FBX, NC, SGND, GND

T29BST_EN_UVLO
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
T29BST_SNS1
T29BST_SNS2
T29BST_FBX

C3892 4.7UF 10% 10V X5R 805
C3887 47PF 5% 50V CERM 402
R3893 10K 1% 1/16W MF-LF 402
T29BST_VC_RC
C3893 3300PF 10% 50V X7R-CERM 0402
R3894 41.2K 1% 1/16W MF-LF 402
C3894 0.33UF 10% 6.3V CERM-X5R 402

GND_T29BST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

R3889 0 5% 1/16W MF-LF 402
XW3895 SM
PLACE_NEAR=C3895.1:2 mm
C3888 10PF 5% 50V CERM 402
R3895 137K 1% 1/16W MF-LF 402 <Ra>
C3889 100PF 5% 50V CERM 402 NO STUFF
R3896 15.8K 1% 1/16W MF-LF 402 <Rb>

C3895 4.7UF 10% 10V X7R-CERM 1206
C3896 4.7UF 10% 50V X7R-CERM 1206
C3897 4.7UF 10% 50V X7R-CERM 1206
C3898 4.7UF 10% 50V X7R-CERM 1206
C3899 0.001UF 10% 50V X7R 402

PP15V_T29
Vout = 15V
Max Current = 0.8A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

Supervisor & CLKREQ# Isolation

PP3V3_S0
C3800 0.1UF 10% 25V X5R 402
Platform (PCIe) Reset
PLT_RST_BUF_L
R3803 10K 5% 1/16W MF-LF 402
Open-Drain GPIO
T29_SW_RESET_L
T29_CLKREQ_L
Pull-up provided by SB page.

U3800 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD

PP3V3_T29
R3807 100K 5% 1/16W MF-LF 402
PP1V05_T29
T29_RESET_L
DLY = 60 ms +/- 20%
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
R3888 330K 5% 1/16W MF-LF 402
T29BST_SHDN_DIV
R3887 330K 5% 1/16W MF-LF 402
SMC_DELAYED_PWRGD

3.3V T29 Switch

PP3V3_S0
U3810 TPS22924 CSP
VIN, VOUT, ON, GND
C3810 1UF 10% 6.3V CERM 402
PP3V3_T29
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

PP1V05_S0
U3815 TPS22924 CSP
C3815 1UF 10% 6.3V CERM 402
PP1V05_T29
Max Current = 3.4A (85C)

U3816 TPS22924 CSP
T29_PWR_EN
Pull-up provided by SB page.
U3816.A2: PLACE_NEAR=U3815.B2:3 mm

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE: T29 Power Support

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH — C3900 0.1UF 10% 16V X7R-CERM 402
CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH — C3905 0.1UF 10% 16V X7R-CERM 402
CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH — R3910 4.7K 5% 1/16W MF-LF 402; C3910 0.1UF; C3911 0.1UF
(MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

ENET_SR_LX
PP1V2_ENET
Internal 1.2V Switching Regulator pins.

PP1V2_ENET
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL — C3921 0.1UF; C3920 4.7UF 10% 6.3V X5R-CERM 603
CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL — C3926 0.1UF; C3925 4.7UF
CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL — C3931 0.1UF; C3930 4.7UF
(MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

CRITICAL C3935 10UF 10% 6.3V X5R 805
C3936 0.1UF 10% 16V X7R-CERM 402

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402

PP3V3_S0
R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF — PCIE_ENET_D2R_N
C3951 0.1uF — PCIE_ENET_D2R_P
C3955 0.1uF — PCIE_ENET_R2D_C_P
C3956 0.1uF — PCIE_ENET_R2D_C_N
R3943 0 5% 1/16W MF-LF 402 — ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT
U3900
BCM57765B0
QFN-8X8

ENET_VMAIN_PRSNT	58	VMAIN_PRSNT (IPD)
PCIE_ENET_D2R_C_N	27	PCIE_TXD_N
PCIE_ENET_D2R_C_P	28	PCIE_TXD_P
PCIE_ENET_R2D_P	33	PCIE_RXD_P
PCIE_ENET_R2D_N	34	PCIE_RXD_N
PCIE_CLK100M_ENET_P	31	PCIE_REFCLK_P
PCIE_CLK100M_ENET_N	30	PCIE_REFCLK_N
ENET_RESET_L	11	PERST* (IPD)
ENET_CLKREQ_L	12	CLKREQ* (OD)
ENET_WAKE_R_L	3	WAKE* (OD)
ENET_LOW_PWR	4	LOW_PWR (IPD)
BCM57765_SMB_CLK	6	SMB_CLK
BCM57765_SMB_DATA	10	SMD_DATA (IPD)
BCM57765_SCLK	66	SCLK
BCM57765_MISO	64	SI/LINKLED*
BCM57765_MOSI	65	SO
BCM57765_CS_L	63	CS*
TP_BCM57765_SPD100LED_L	2	SPD100LED*/SERIAL_DO (OD)
TP_BCM57765_TRAFFICLED_L	67	TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET	18	XTALI
NC	19	XTALO
BCM57765_RDAC	38	RDAC
	69	THRM_PAD

ENET_MDI_P<0>	40	TRD0_P
ENET_MDI_N<0>	41	TRD0_N
ENET_MDI_P<1>	44	TRD1_P
ENET_MDI_N<1>	43	TRD1_N
ENET_MDI_P<2>	46	TRD2_P
ENET_MDI_N<2>	47	TRD2_N
ENET_MDI_P<3>	50	TRD3_P
ENET_MDI_N<3>	49	TRD3_N
NC	5	GPIO_0
GPIO_1/CR_BUS_PWR	8	
RE*/GPIO_2	9	
(IPD) SD_DETECT/WE*	24	
(IPU) CR_CMD/CLE	26	
CR_CLK/RY_BY*	21	
CR_DATA0	25	
CR_DATA1	24	
CR_DATA2	23	
CR_DATA3	22	
CR_DATA4	52	
CR_DATA5	53	
CR_DATA6	54	
CR_DATA7	55	
CE*/MS_INS*	59	
CR_LED/ALE	60	
CR_WP*/XD_WP*	57	
XD_DETECT	68	

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

ENET_MEDIA_SENSE
SDCONN_DETECT_L
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
TP_CE_L_MS_INS_L
ENET_CR_PWREN
BDM57765_SR_DISABLE — R3980 1K 5% 1/16W MF-LF 402
SDCONN_WP

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

PP3V3_ENET
U3990 AT45DB011D SOIC-8S1 OMIT
C3990 0.1UF
R3990 4.7K — NOSTUFF
R3997 4.7K
BCM57765_SCLK, BCM57765_CS_L, BCM57765_MOSI, BCM57765_MISO

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010
PAGE TITLE: ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER — SIZE D
REVISION
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Place one of 0.1uf cap close to each centertap pin of transformer

ENETCONN_CTAP

C4000 C4002 C4004 C4006
0.1UF 10% 16V X5R 402-1

CRITICAL
T4000
SM
TX
TLA-6T213HF
RX

CRITICAL
T4001
SM
TX
TLA-6T213HF
RX

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_N<1>
ENET_MDI_P<1>
ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_N<3>
ENET_MDI_P<3>

ENETCONN_P<0>
ENETCONN_N<0>
ENET_CTAP0
ENET_CTAP1
ENETCONN_N<1>
ENETCONN_P<1>
ENETCONN_N<2>
ENETCONN_P<2>
ENET_CTAP2
ENET_CTAP3
ENETCONN_N<3>
ENETCONN_P<3>

Transformers should be mirrored on opposite sides of the board

R4000 R4001 R4002 R4003
75 5% 1/16W MF-LF 402

CRITICAL
J4000
RJ45-M97-3
F-RT-TH
514-0636

CRITICAL
C4008
1000PF
10% 2KV CERAM 1206

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25 mm

PLACE_NEAR=T4001.1:5mm
PLACE_NEAR=T4000.5:5mm

D4001
RCLAMP0524P
SLP2510P8
CRITICAL
NOSTUFF

D4000
RCLAMP0524P
SLP2510P8
CRITICAL
NOSTUFF

SYNC_MASTER=K91 TRINHNI SYNC_DATE=05/26/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

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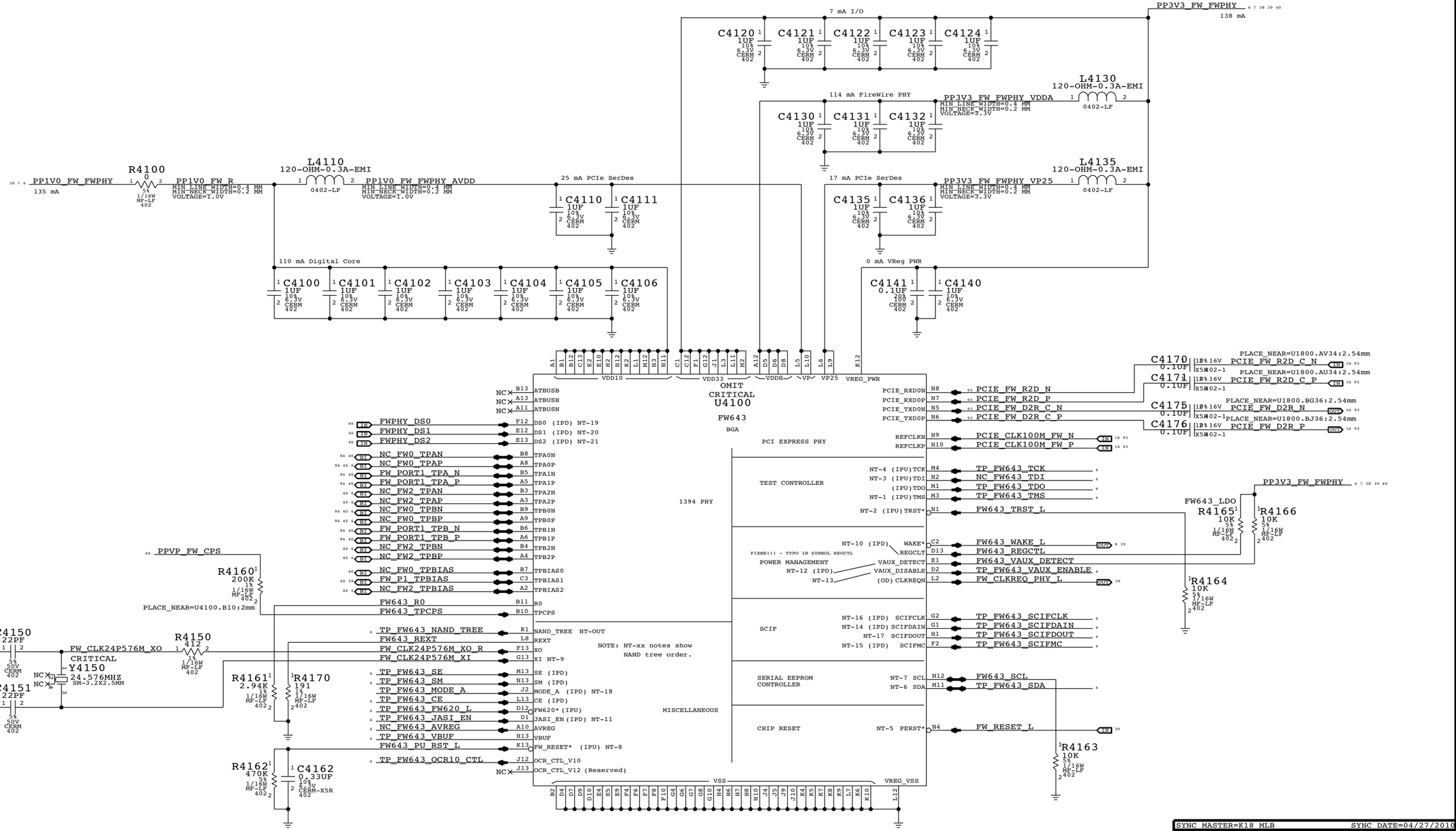

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER — SIZE D

REVISION

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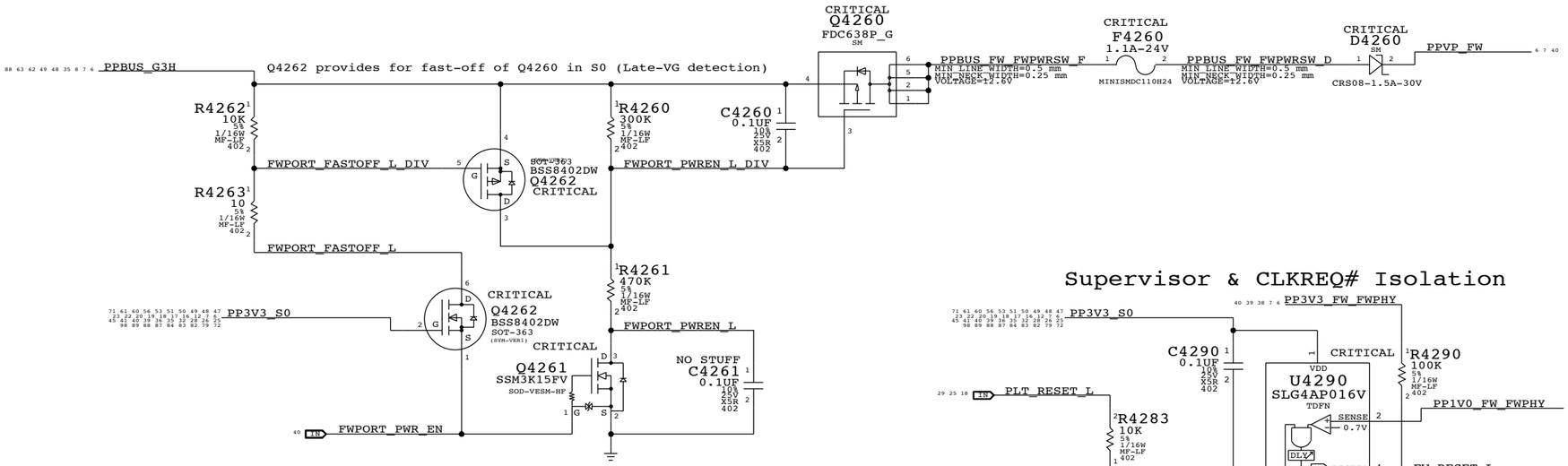
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_SO_FWLATEVG
- =PP3V3_SO_FWPWRCTL
- =PP1V05_SO_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

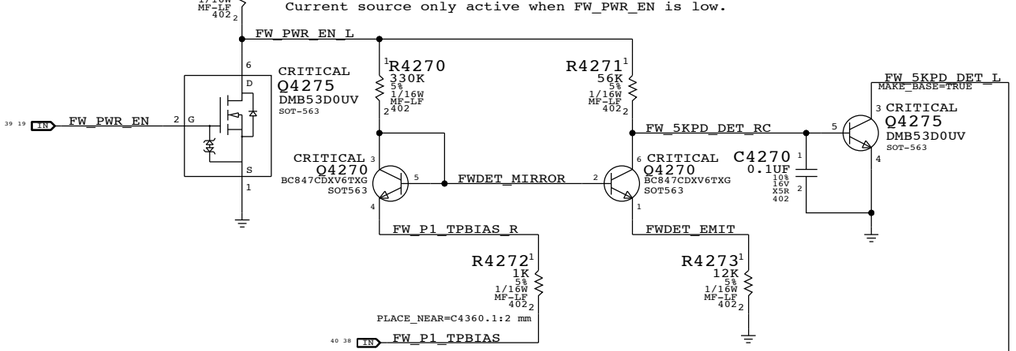
FireWire Port Power Switch



Supervisor & CLKREQ# Isolation

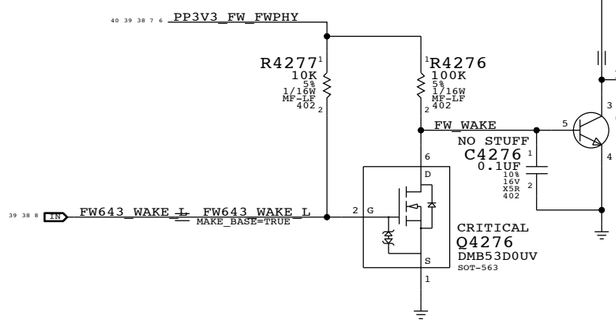
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

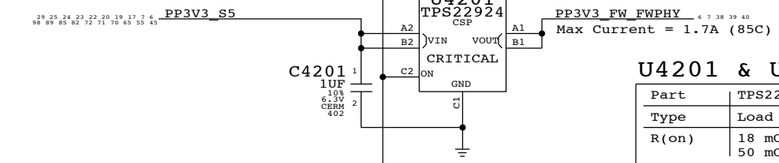


Dual-purpose output:

1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

FW_PLUG_DET_L
Pull-up provided on another page.

3.3V FW Switch

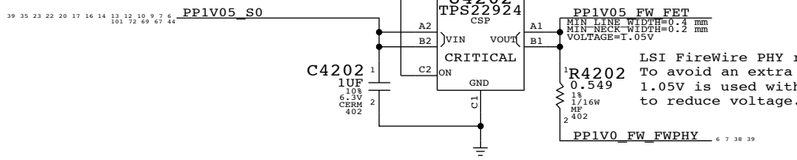


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER | SIZE: D
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BRANCH
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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

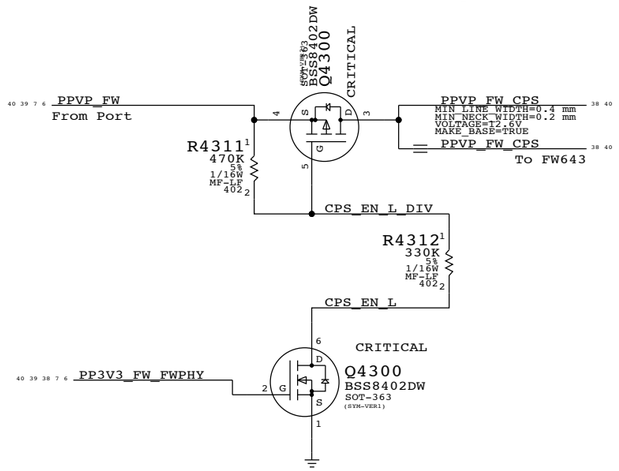
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

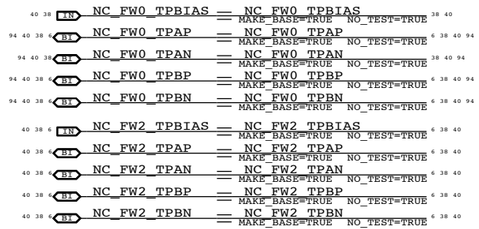
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



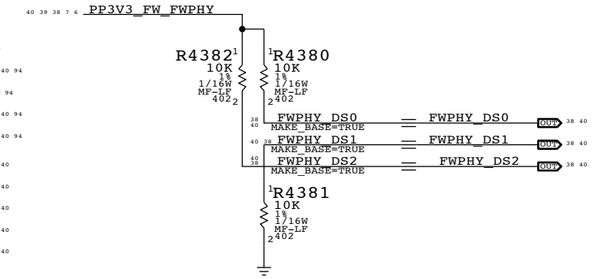
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



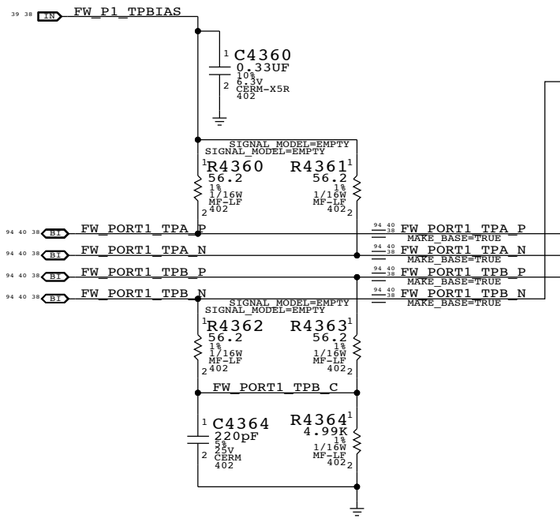
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

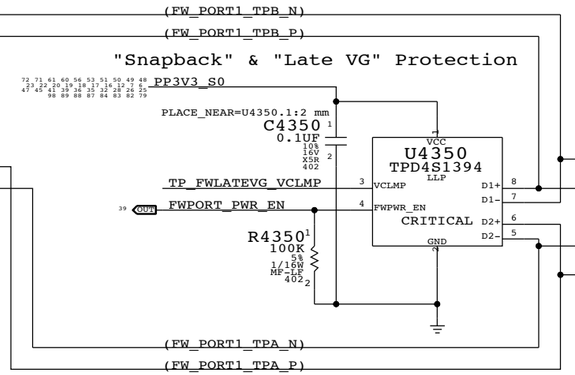


Termination

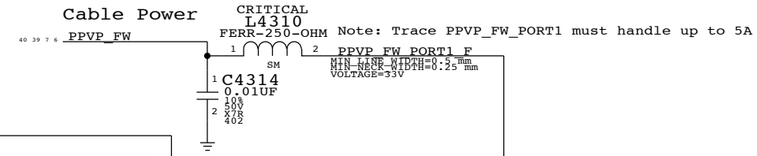
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



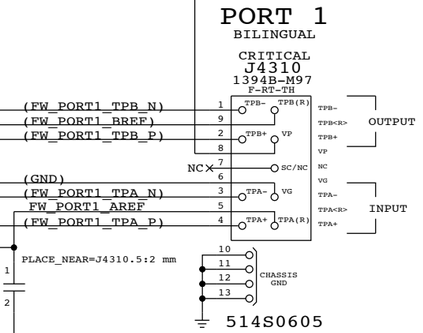
Cable Power



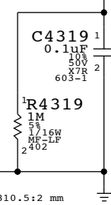
Note: Trace PPVP_FW_PORT1 must handle up to 5A

PORT 1

BILINGUAL



514S0605



AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE: FireWire Connector

Apple Inc.

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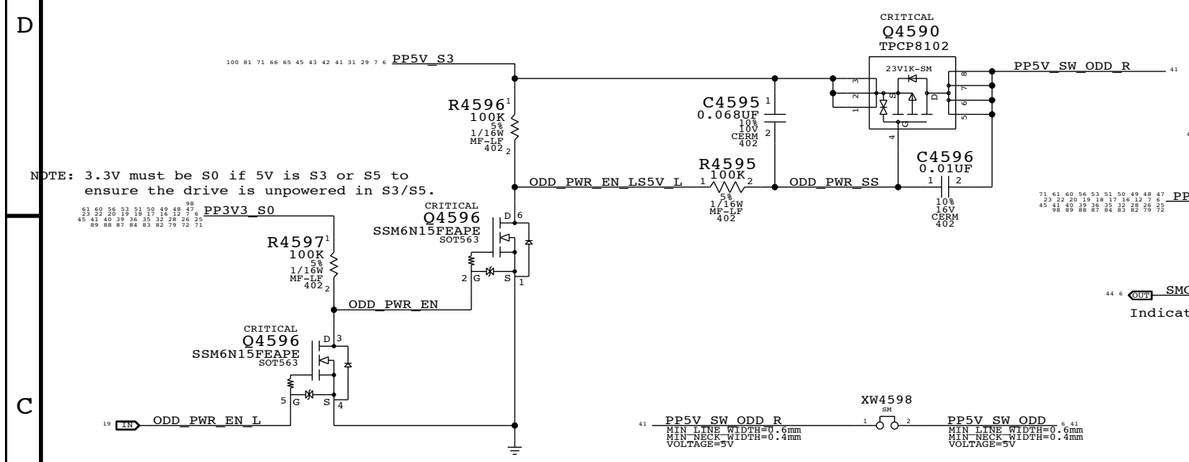
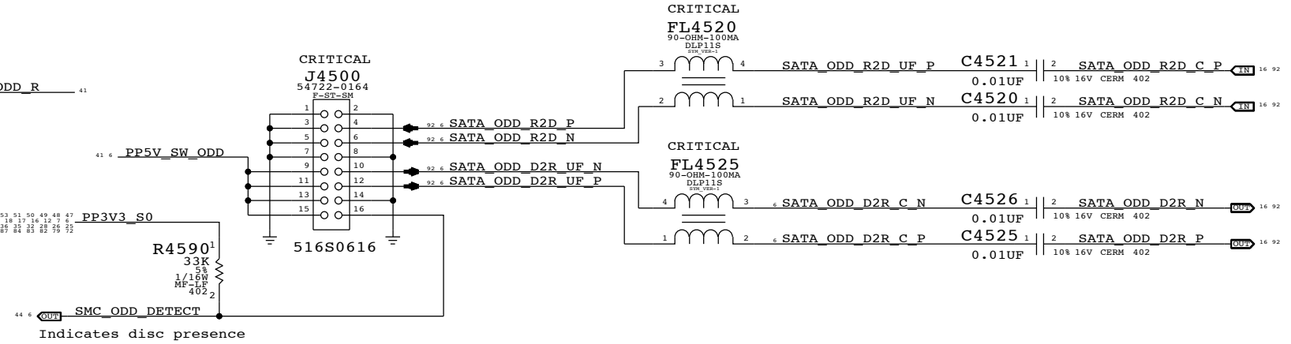
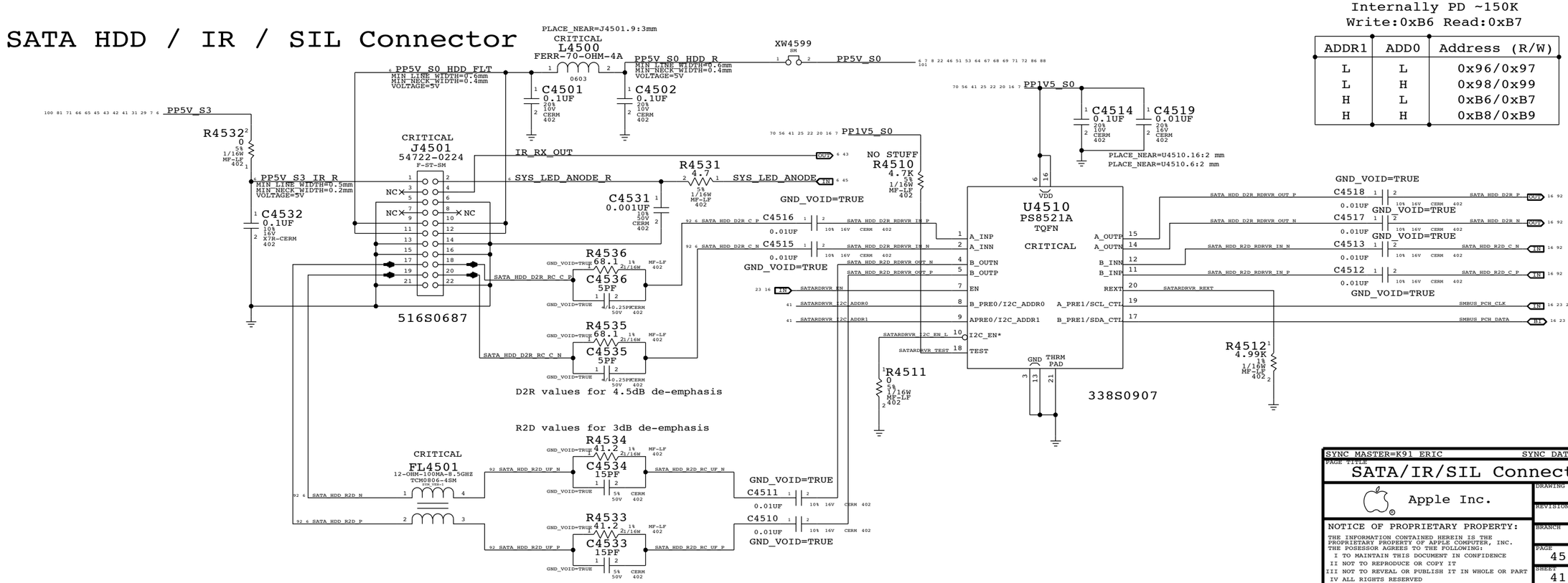
ODD Power Control



SATA ODD Connector



SATA HDD / IR / SIL Connector



PP1V5_S0

NO STUFF R4513 4.7K 5% 1/16W MF-LF 402

R4515 4.7K 5% 1/16W MF-LF 402

SATARDRVR_I2C_ADDR0

SATARDRVR_I2C_ADDR1

Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SYNC_MASTER=K91_ERIC SYNC_DATE=11/08/2010

PAGE TITLE

SATA/IR/SIL Connectors

Apple Inc.

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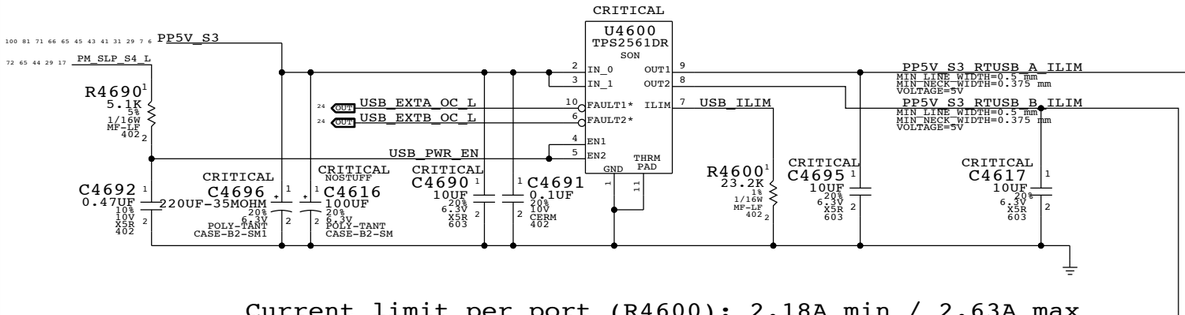
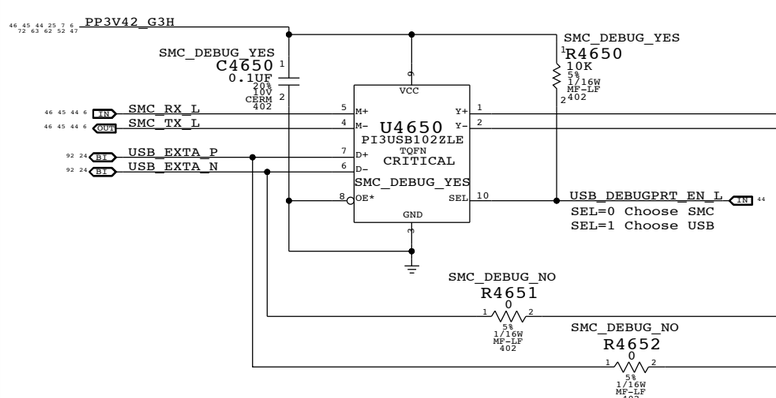
USB Port Power Switch

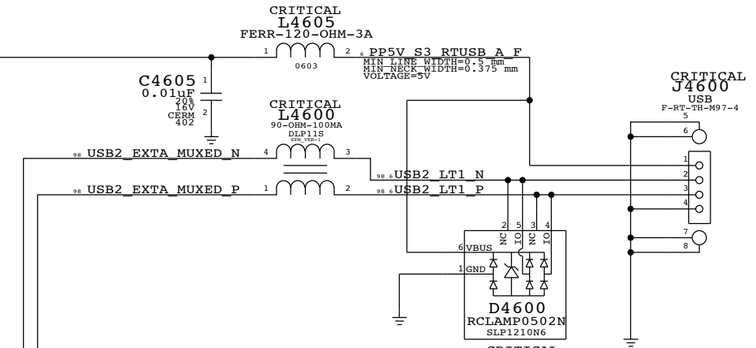


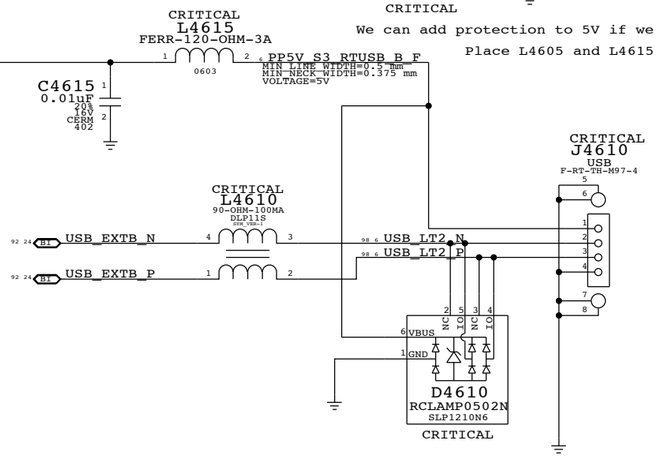
Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux



Left USB Port A





We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin

Left USB Port B

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: External USB Connectors

Apple Inc.

DRAWING NUMBER | SIZE: D

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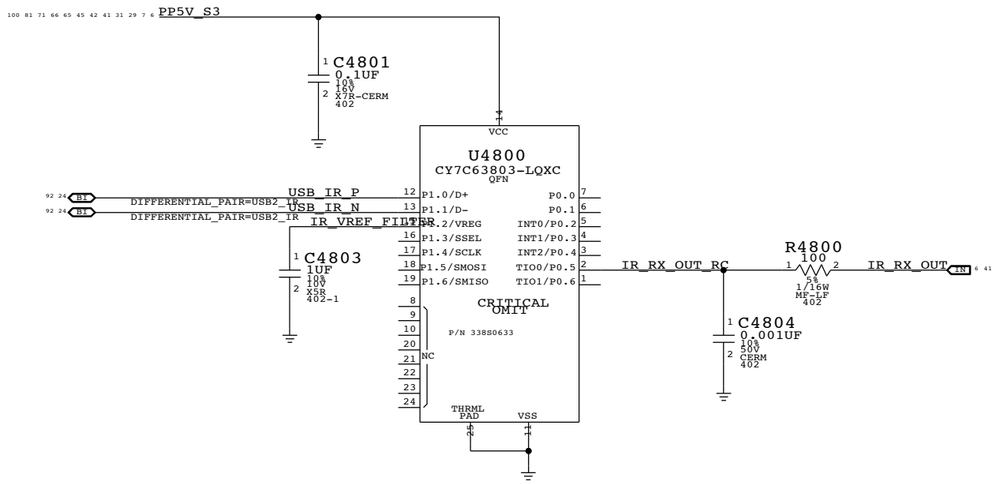
IR SUPPORT



SYNC MASTER=K18 MLB SYNC DATE=04/27/2010

PAGE TITLE

Front Flex Support

Apple Inc.

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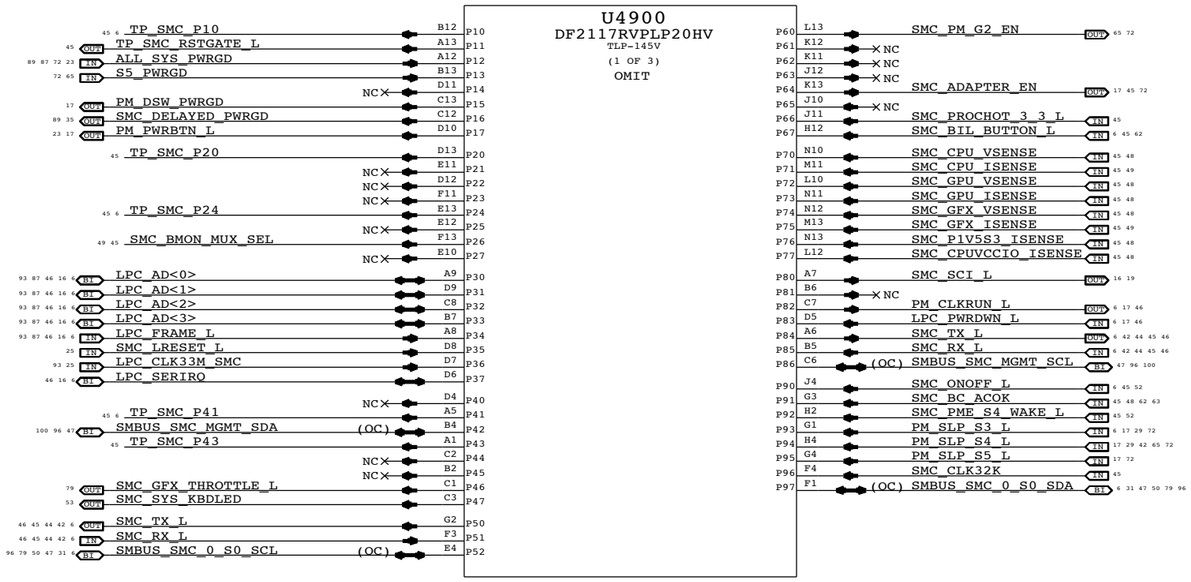
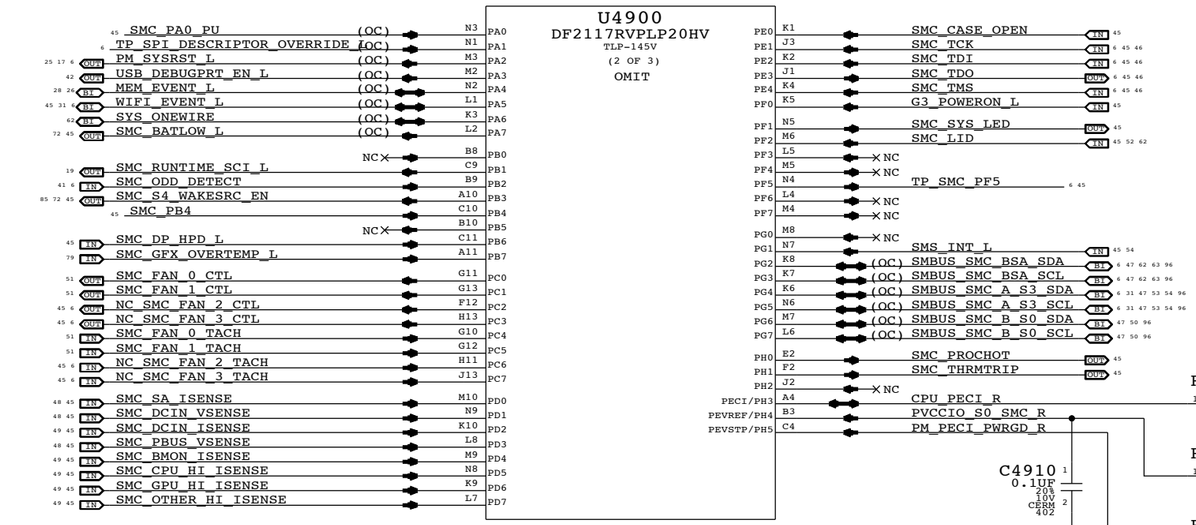
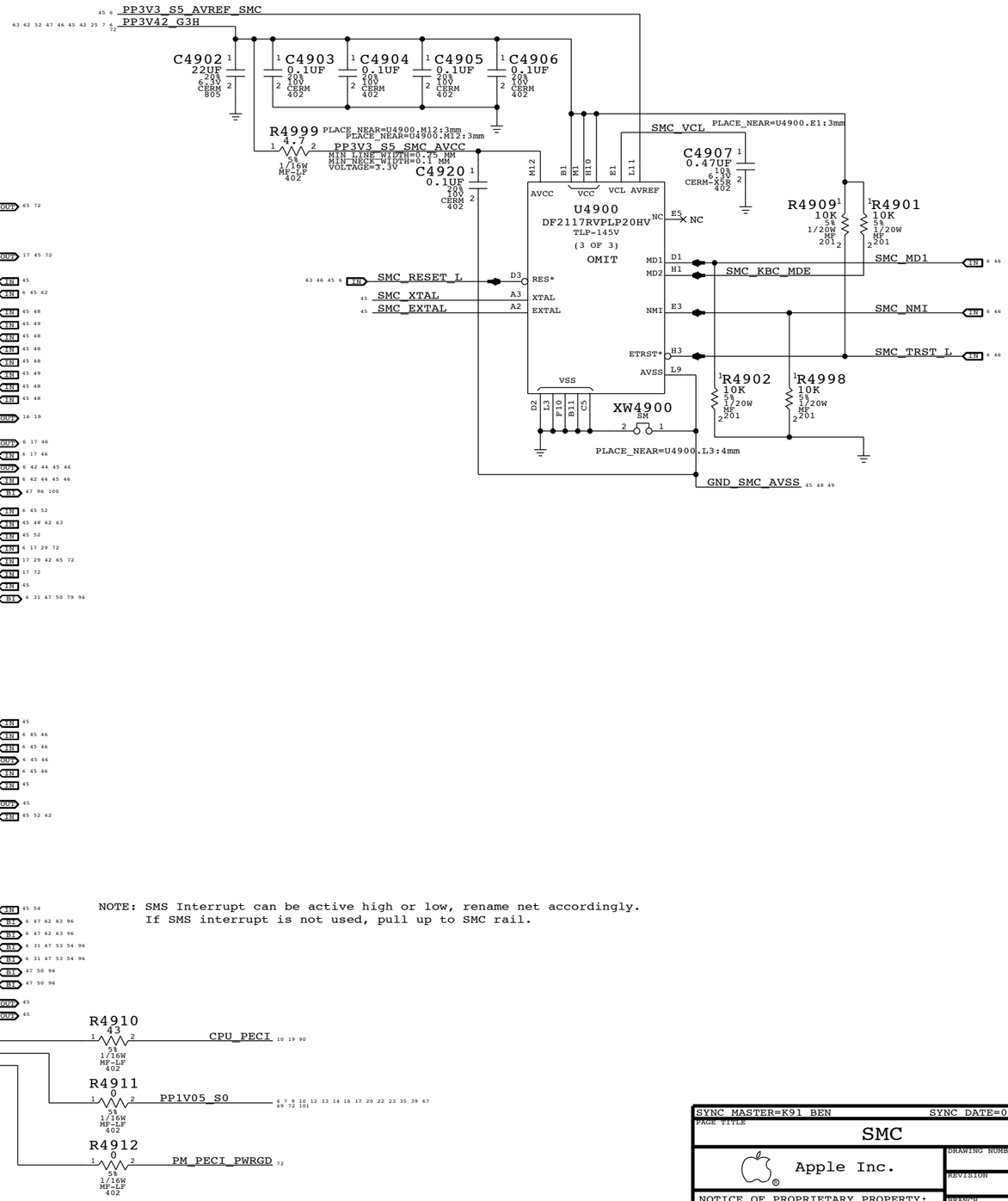
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=K91_BEN	SYNC_DATE=07/12/2010
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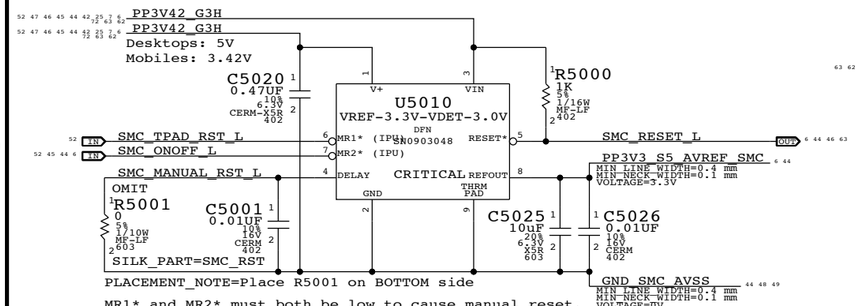
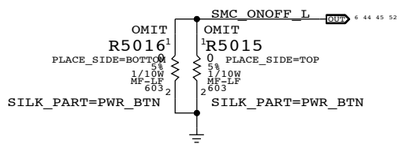
SMC Reset "Button", Supervisor & AVREF Supply



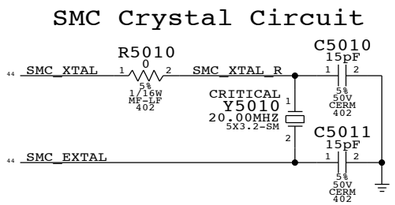
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

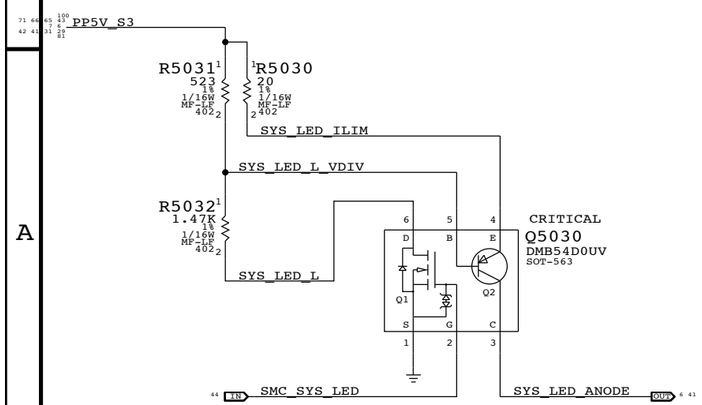
Debug Power "Buttons"



SMC Crystal Circuit

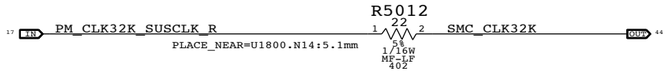


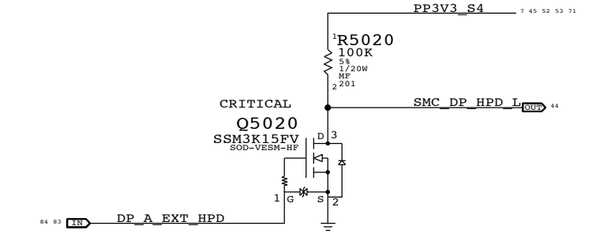
System (Sleep) LED Circuit

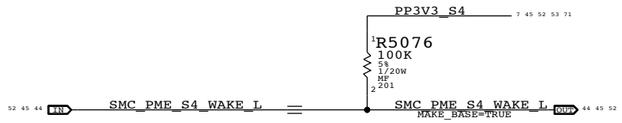


SMC_*_L Pull-ups

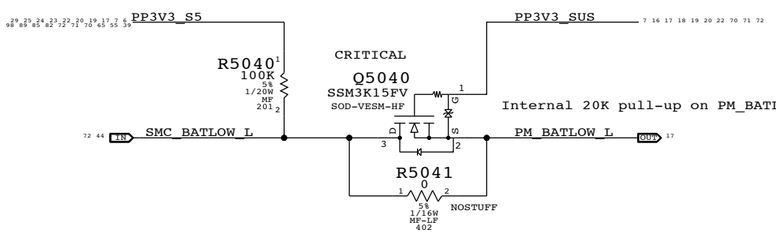
NC_SMC_FAN_2_CTL	= NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_2_TACH	= NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE	
NC_SMC_FAN_3_CTL	= NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_3_TACH	= NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE	
SMC_BC_ACOK	= SMC_BC_ACOK	MAKE_BASE=TRUE	
SMS_INT_L	= SMS_INT_L	MAKE_BASE=TRUE	
SMC_CPU_VSENSE	= SMC_CPU_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_ISENSE	= SMC_CPU_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_VSENSE	= SMC_GPU_VSENSE	MAKE_BASE=TRUE	
SMC_GPU_ISENSE	= SMC_GPU_ISENSE	MAKE_BASE=TRUE	
SMC_GFX_VSENSE	= SMC_GFX_VSENSE	MAKE_BASE=TRUE	
SMC_GFX_ISENSE	= SMC_GFX_ISENSE	MAKE_BASE=TRUE	
SMC_P1V5S3_ISENSE	= SMC_P1V5S3_ISENSE	MAKE_BASE=TRUE	
SMC_CPUVCCIO_ISENSE	= SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE	
SMC_SA_ISENSE	= SMC_SA_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_VSENSE	= SMC_DCIN_VSENSE	MAKE_BASE=TRUE	
SMC_DCIN_ISENSE	= SMC_DCIN_ISENSE	MAKE_BASE=TRUE	
SMC_PBUS_VSENSE	= SMC_PBUS_VSENSE	MAKE_BASE=TRUE	
SMC_BMON_ISENSE	= SMC_BMON_ISENSE	MAKE_BASE=TRUE	
SMC_CPU_HI_ISENSE	= SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_HI_ISENSE	= SMC_GPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_OTHER_HI_ISENSE	= SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE	
TP_SMC_P10	= TP_SMC_P10	MAKE_BASE=TRUE	
TP_SMC_P20	= TP_SMC_P20	MAKE_BASE=TRUE	
TP_SMC_P24	= TP_SMC_P24	MAKE_BASE=TRUE	
SMC_BMON_MUX_SEL	= SMC_BMON_MUX_SEL	MAKE_BASE=TRUE	
TP_SMC_P41	= TP_SMC_P41	MAKE_BASE=TRUE	
TP_SMC_P43	= TP_SMC_P43	MAKE_BASE=TRUE	
TP_SMC_PF5	= TP_SMC_PF5	MAKE_BASE=TRUE	
TP_SMC_RSTGATE_L	= TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	





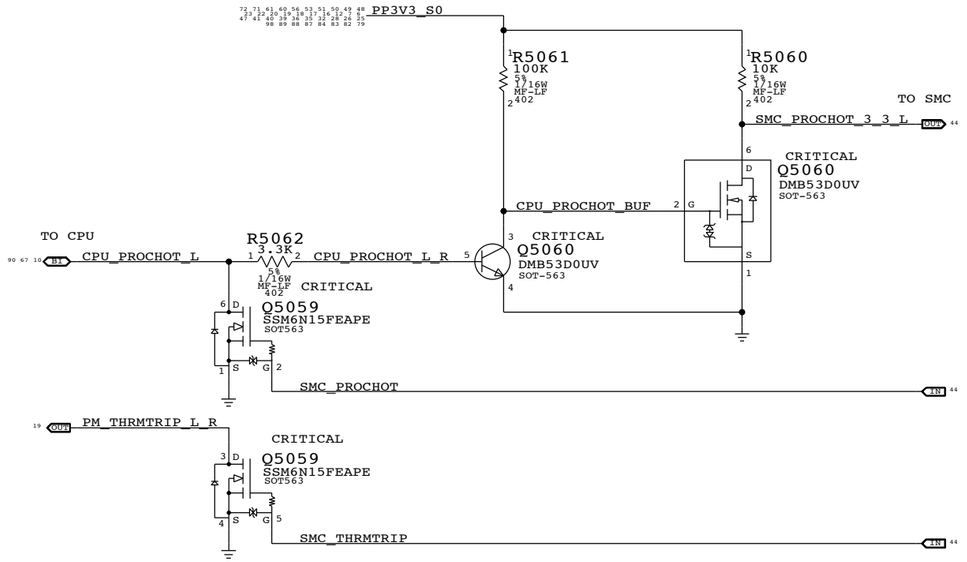


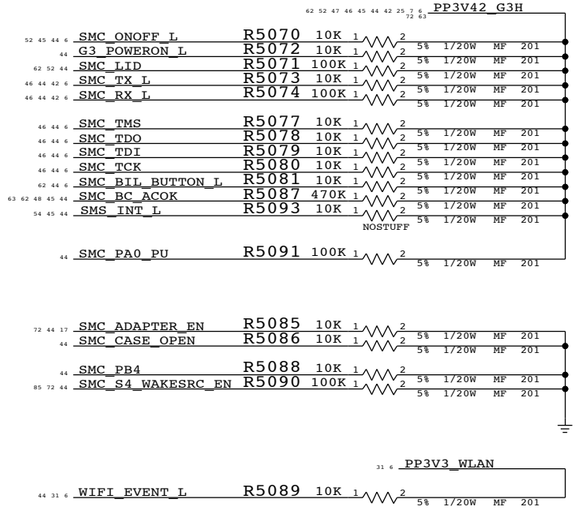
BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

SMC FSB to 3.3V Level Shifting





SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

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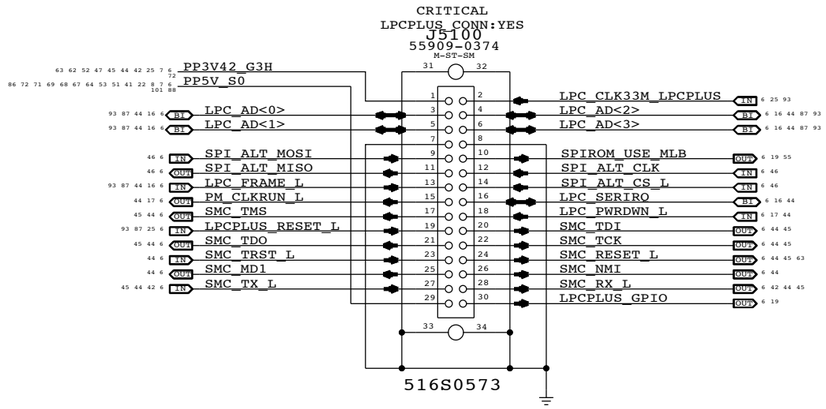
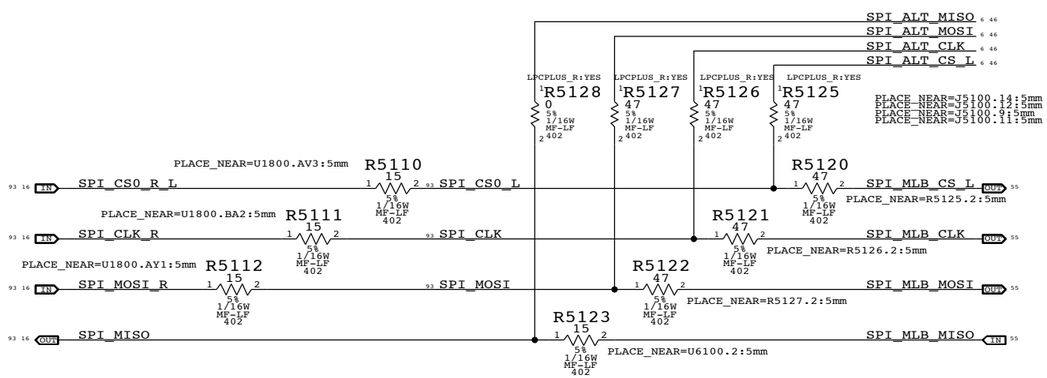
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

LPC+SPI Debug Connector

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 5% 1/16W MF-LF 402

R5201 1K 5% 1/16W MF-LF 402

Cougar Point
U1800
(MASTER)
- SMBUS_PCH_CLK — MAKE_BASE=TRUE
- SMBUS_PCH_DATA — MAKE_BASE=TRUE

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U3301
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SATA Redriver
U4510
(Write: 0xB6 Read: 0xB7)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2500 & J2550
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6880
(Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SDRVI2C:SB
R5237 0 5% 1/16W MF-LF 402

SDRVI2C:SB
R5236 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL — MAKE_BASE=TRUE
- I2C_DPSDRVA_SDA — MAKE_BASE=TRUE

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402

R5211 8.2K 5% 1/16W MF-LF 402

Cougar Point
U1800
(MASTER)
- SML_PCH_0_CLK — MAKE_BASE=TRUE
- SML_PCH_0_DATA — MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402

NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402

R5222 0 5% 1/16W MF-LF 402

Cougar Point
U1800
(Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK — MAKE_BASE=TRUE
- SML_PCH_1_DATA — MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402

R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_0_S0_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_0_S0_SDA — MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
Whistler: U8000
(Write: 0x82 Read: 0x83)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

X19
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 5% 1/16W MF-LF 402

R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_A_S3_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_A_S3_SDA — MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

J3401
ALS
(Write: 0x72 Read: 0x73)
Lid Angle Detect
(Write: 0x32 Read: 0x33)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

Digital SMS
LIS331DLH: U5920
(Write: 0x30 Read: 0x31)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402

R5261 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_B_S0_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_B_S0_SDA — MAKE_BASE=TRUE

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

T29 Temp
EMC1412-A: U5520
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 2.0K 5% 1/16W MF-LF 402

R5281 2.0K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_BSA_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_BSA_SDA — MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

R5290 4.7K 5% 1/16W MF-LF 402

R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_MGMT_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_MGMT_SDA — MAKE_BASE=TRUE

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

T29 SMBus Connections

PP3V3_S0

R5230 4.7K 5% 1/16W MF-LF 402

R5231 4.7K 5% 1/16W MF-LF 402

T29 IC
U3600
(MASTER)
- I2C_T29_SCL — MAKE_BASE=TRUE
- I2C_T29_SDA — MAKE_BASE=TRUE

T29 Port A MCU
J9330
(Write: 0x26 Read: 0x27)
- I2C_T29_SCL
- I2C_T29_SDA

SDRVI2C:MCU
R5234 0 5% 1/16W MF-LF 402

SDRVI2C:MCU
R5235 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL — MAKE_BASE=TRUE
- I2C_DPSDRVA_SDA — MAKE_BASE=TRUE

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: SMBus Connections

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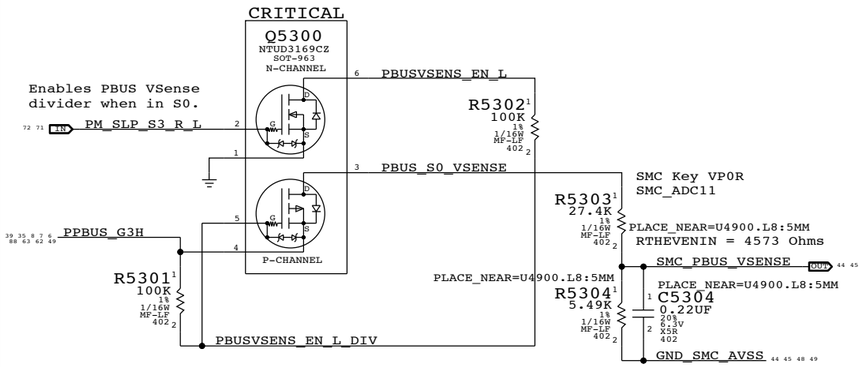
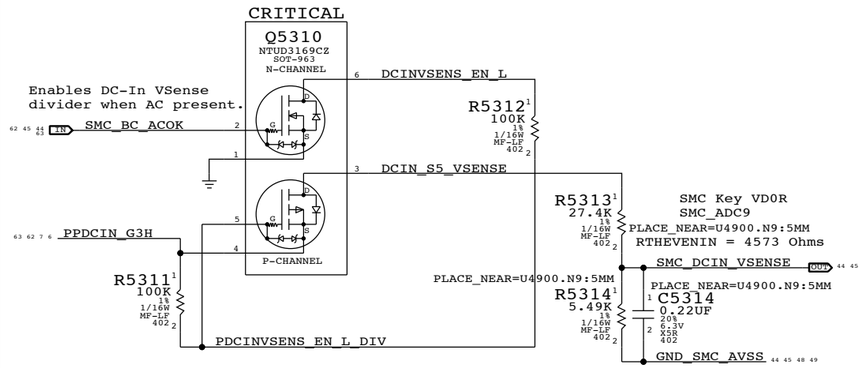
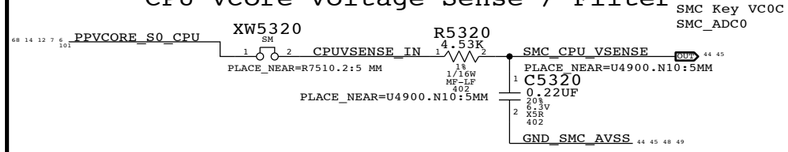
PBUS Voltage Sense Enable & Filter



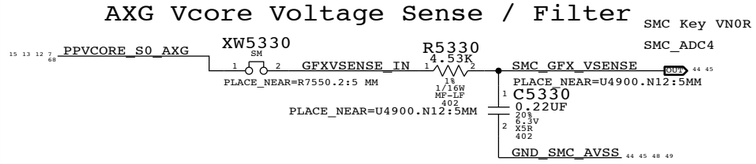
DC-In Voltage Sense Enable & Filter



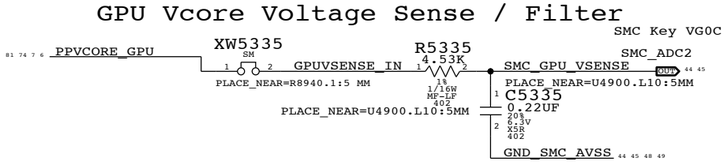
CPU Vcore Voltage Sense / Filter



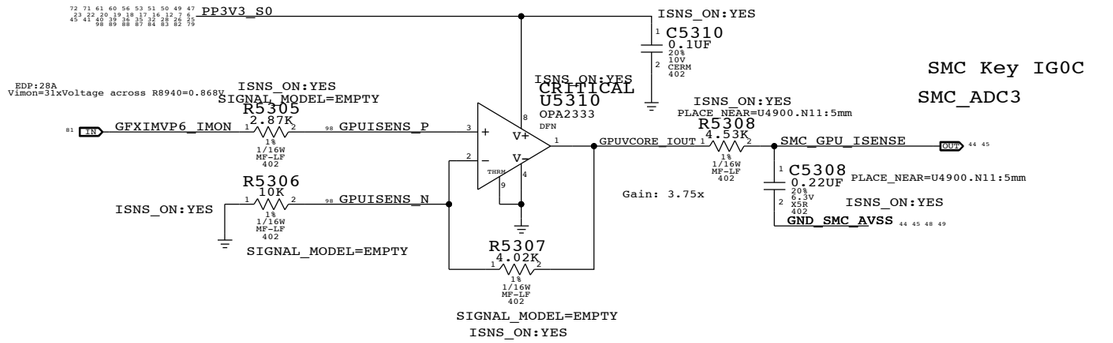
AXG Vcore Voltage Sense / Filter



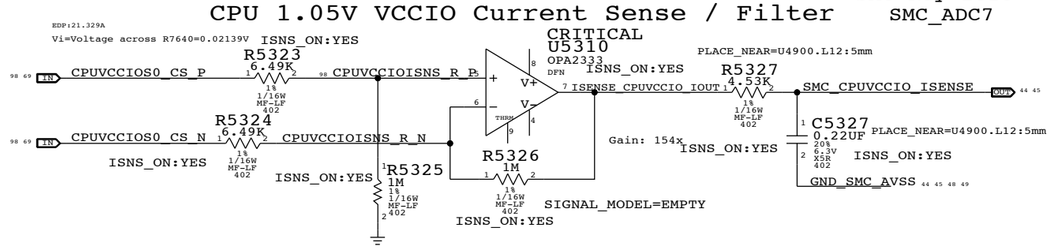
GPU Vcore Voltage Sense / Filter



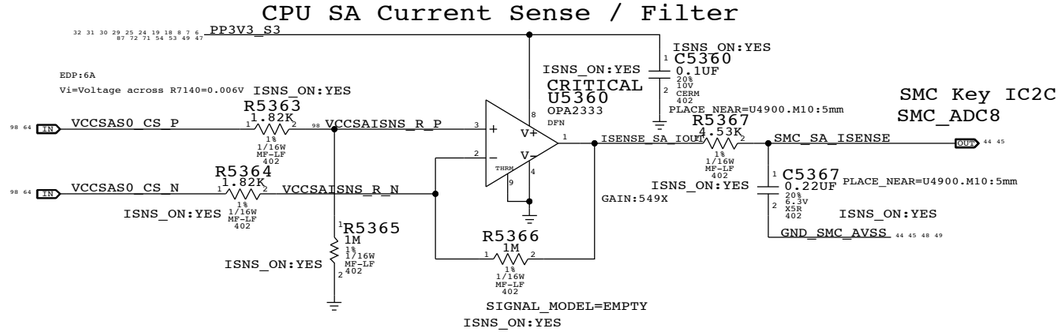
GPU VCore Load Side Current Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter

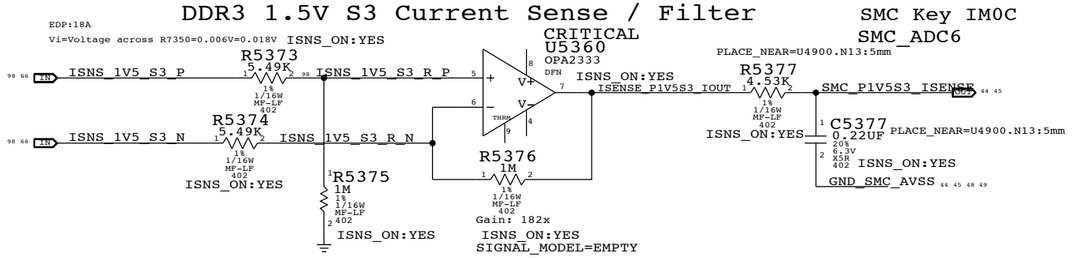


CPU SA Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	4	RES, 0OHM, 0402	C5308,C5327,C5367,C5377		ISNS_ON:NO

DDR3 1.5V S3 Current Sense / Filter



SYNC_MASTER=K91_DINESH SYNC_DATE=08/16/2010

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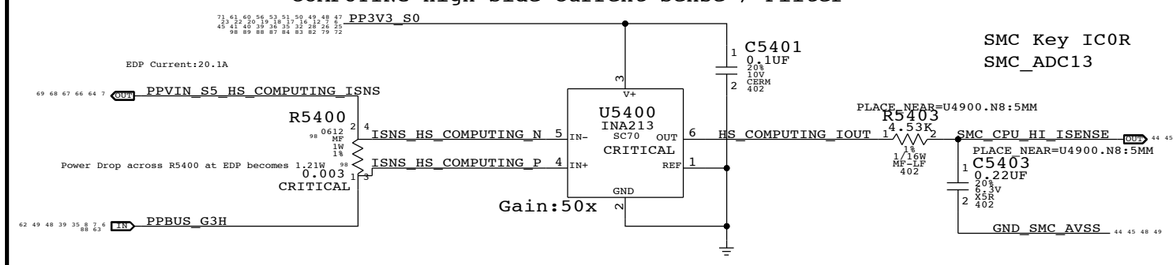
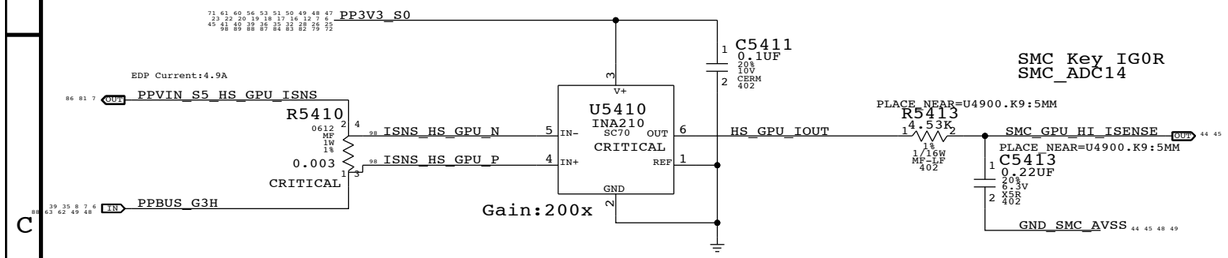
COMPUTING High Side Current Sense / Filter



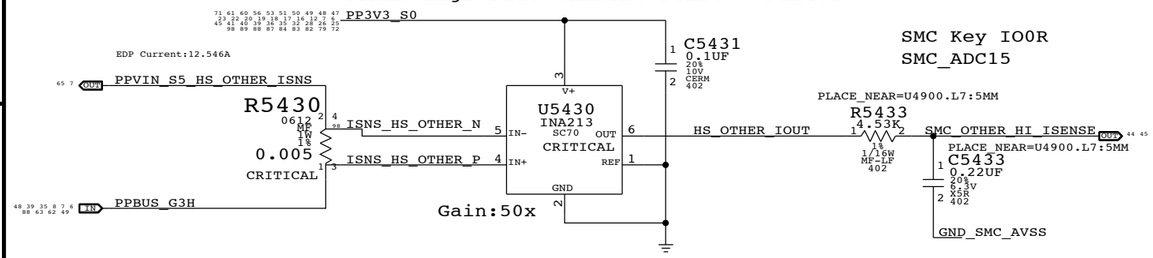
SMC Key IC0R
SMC_ADC13

GRAPHICS High Side Current Sense / Filter



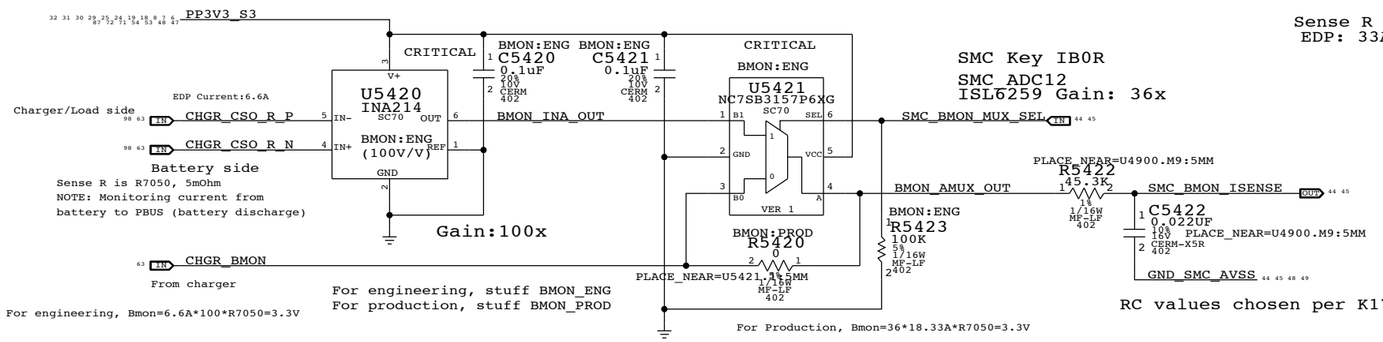
SMC Key IG0R
SMC_ADC14

OTHER High Side Current Sense / Filter



SMC Key IO0R
SMC_ADC15

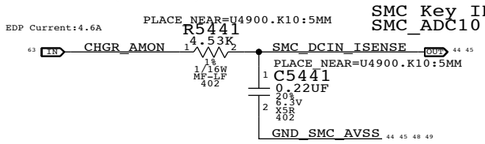
CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter



SMC Key IB0R
SMC_ADC12
ISL6259 Gain: 36x

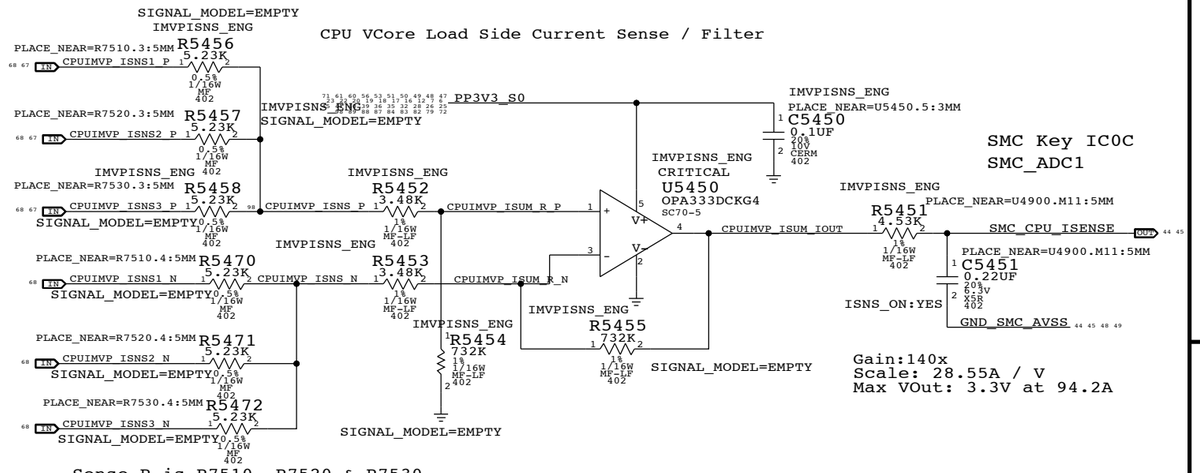
RC values chosen per K17 Radar 7337775

DC-IN (AMON) Current Sense Filter



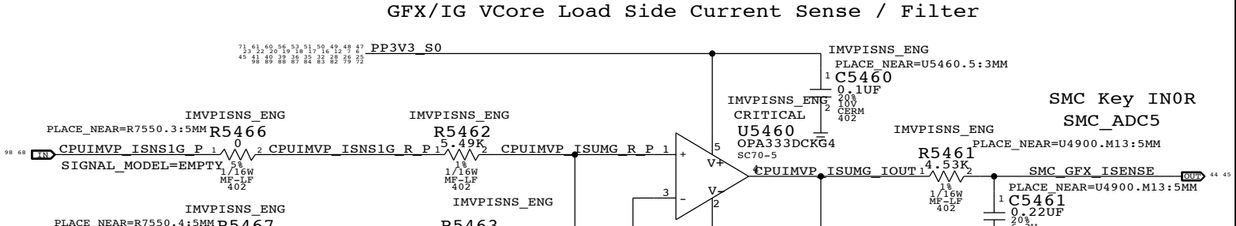
SMC Key ID0R
SMC_ADC10

CPU VCore Load Side Current Sense / Filter



SMC Key IC0C
SMC_ADC1

GFX/IG VCore Load Side Current Sense / Filter



SMC Key IN0R
SMC_ADC5

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	2	RES, 0OHM, 0402	C5451,C5461		ISNS_ON:NO

SYNC_MASTER=K91_DINESH SYNC_DATE=10/29/2010

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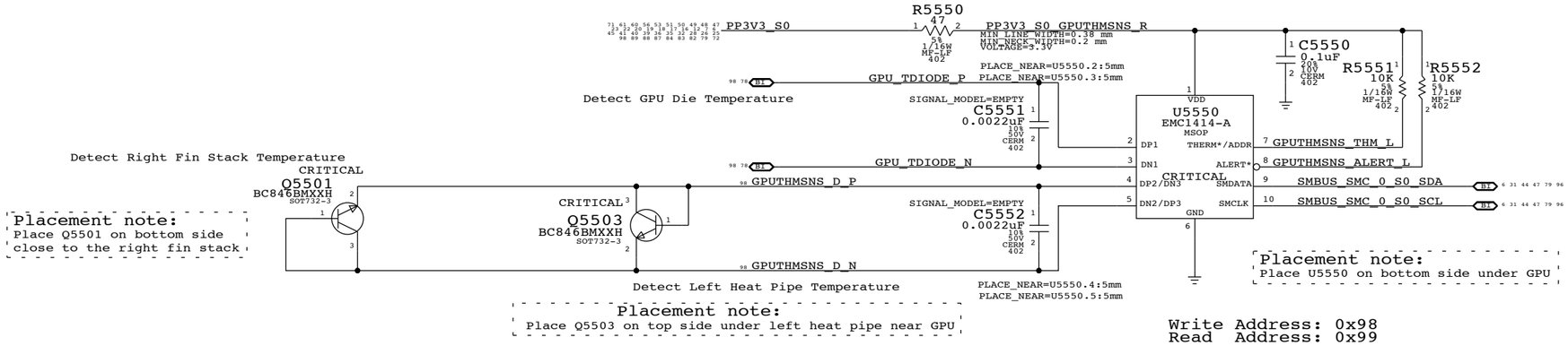
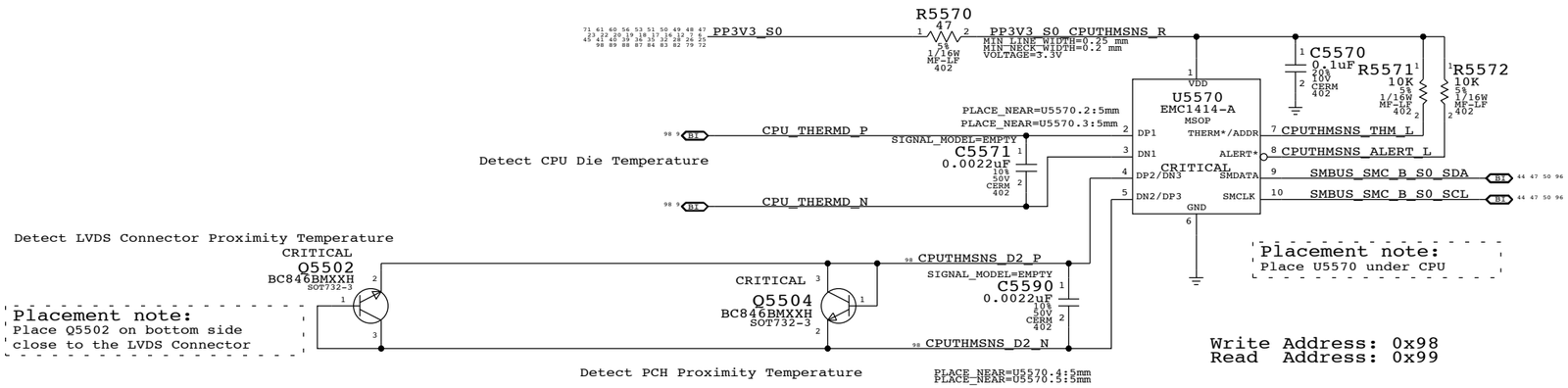
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



Write Address: 0x98
Read Address: 0x99

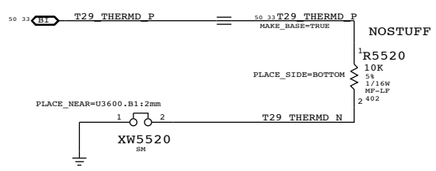
CPU Proximity/CPU Die/PCH Proximity/LVDS Connector Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

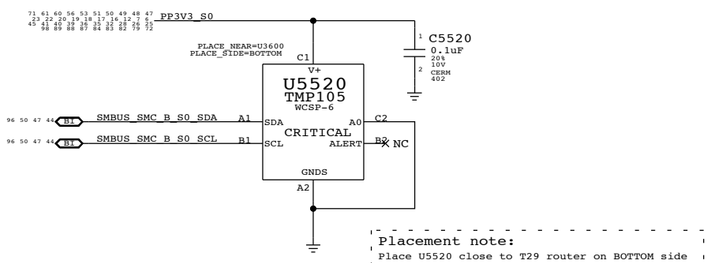
Write Address: 0x98
Read Address: 0x99

T29 Die



Use GND pin B1 on U3600 for N leg

T29 Proximity



Write Address: 0x90
Read Address: 0x91

SYNC_MASTER=K91_DINESH SYNC_DATE=09/22/2010

PAGE TITLE
Thermal Sensors

Apple Inc.

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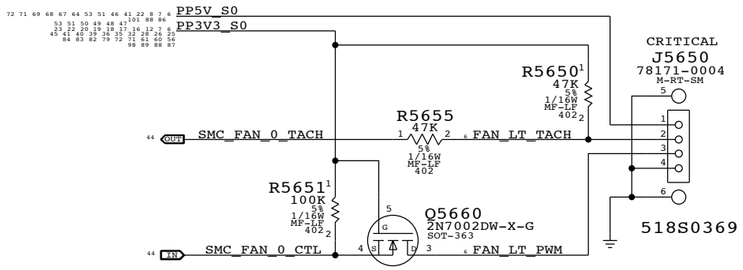
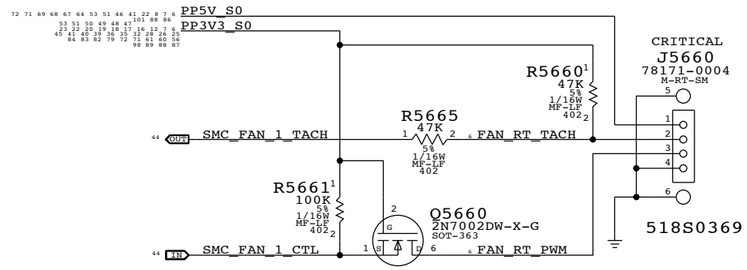
Left Fan



Right Fan



SYNC MASTER=K18 MLB SYNC DATE=04/27/2010

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER

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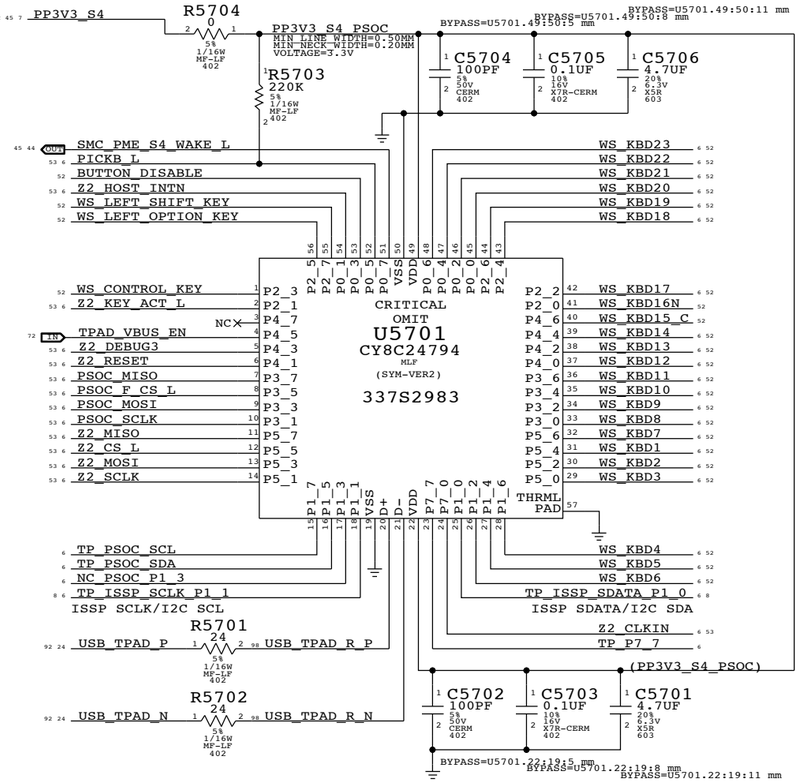
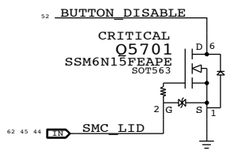
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

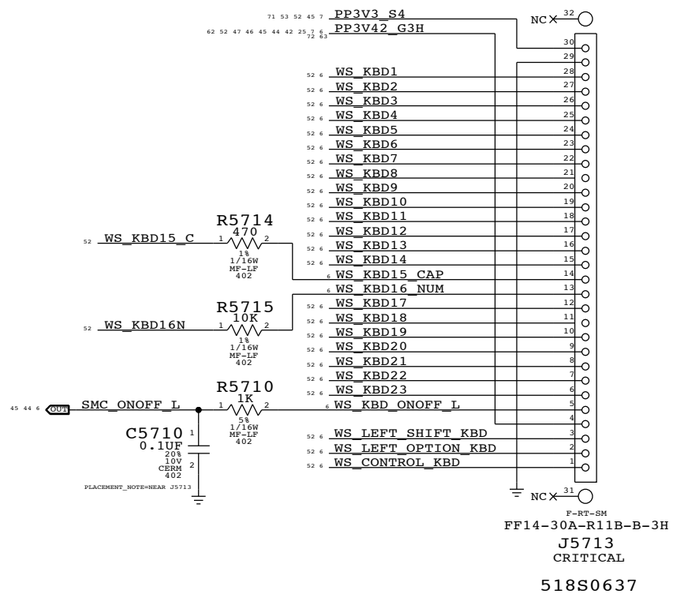


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

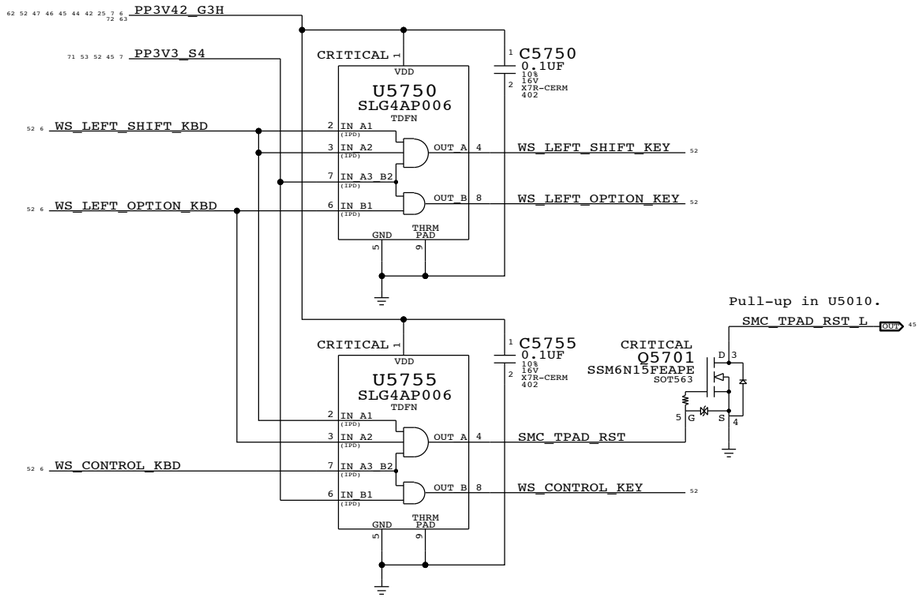
Keyboard Connector



518S0637

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC MASTER=K91 ERIC	SYNC DATE=10/08/2010
PAGE TITLE	WELLSPRING 1
Apple Inc.	DRAWING NUMBER — SIZE D
	REVISION
	BRANCH
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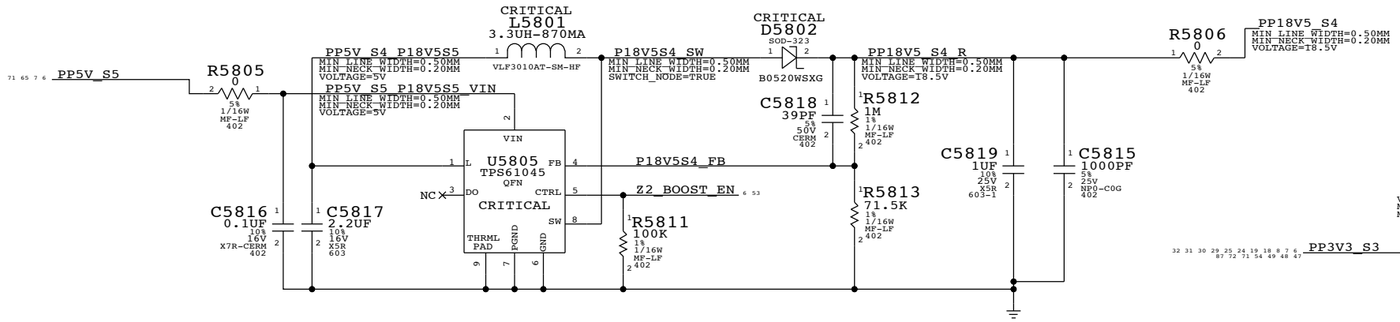
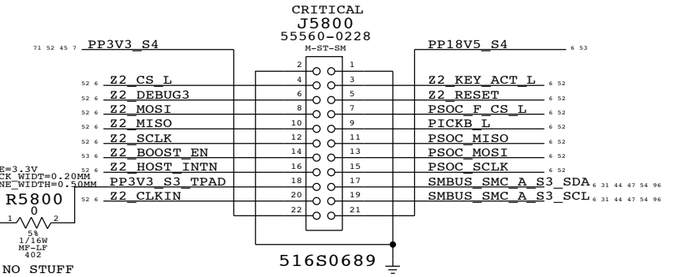
BOOSTER +18.5VDC FOR SENSORS

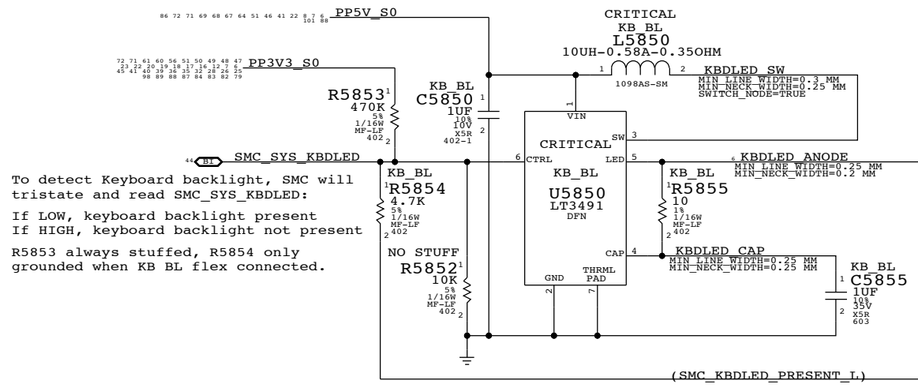
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

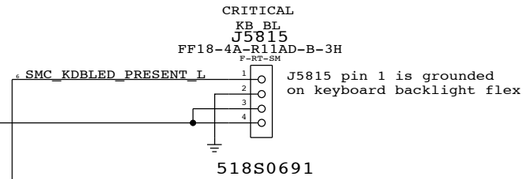


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



SYNC_MASTER=K91_ERIC SYNC_DATE=07/14/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER | SIZE: D

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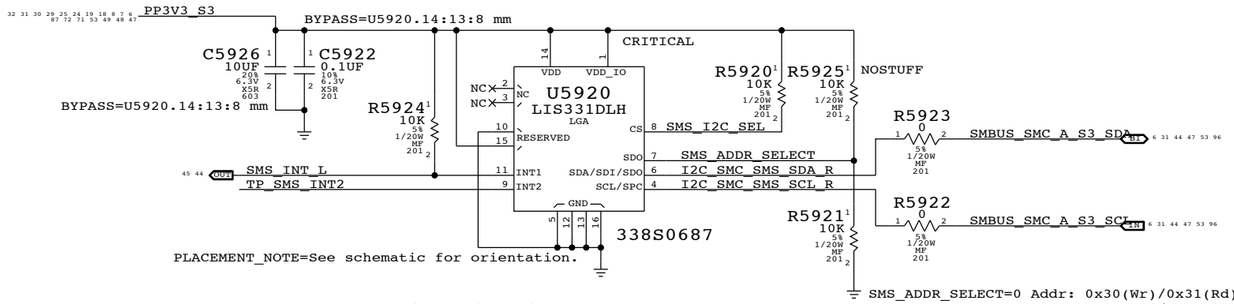
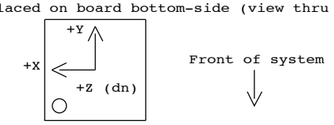


SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when
placed on board bottom-side (view thru top):



Front of system

Circle indicates pin 1 location when placed
in correct orientation

SYNC MASTER=K91 DINESH SYNC DATE=08/06/2010

PAGE TITLE
Digital Accelerometer

Apple Inc.

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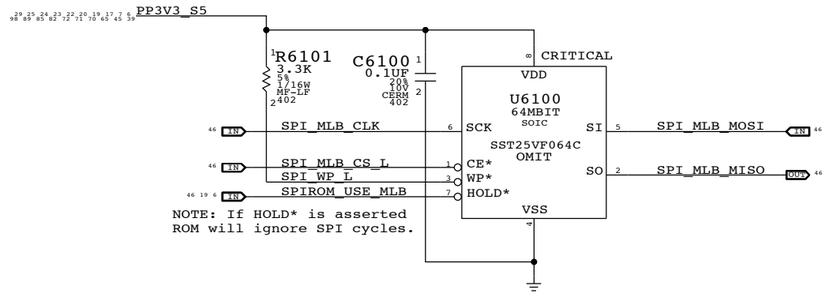

SYNC MASTER=K91 BEN SYNC DATE=06/08/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER — SIZE D

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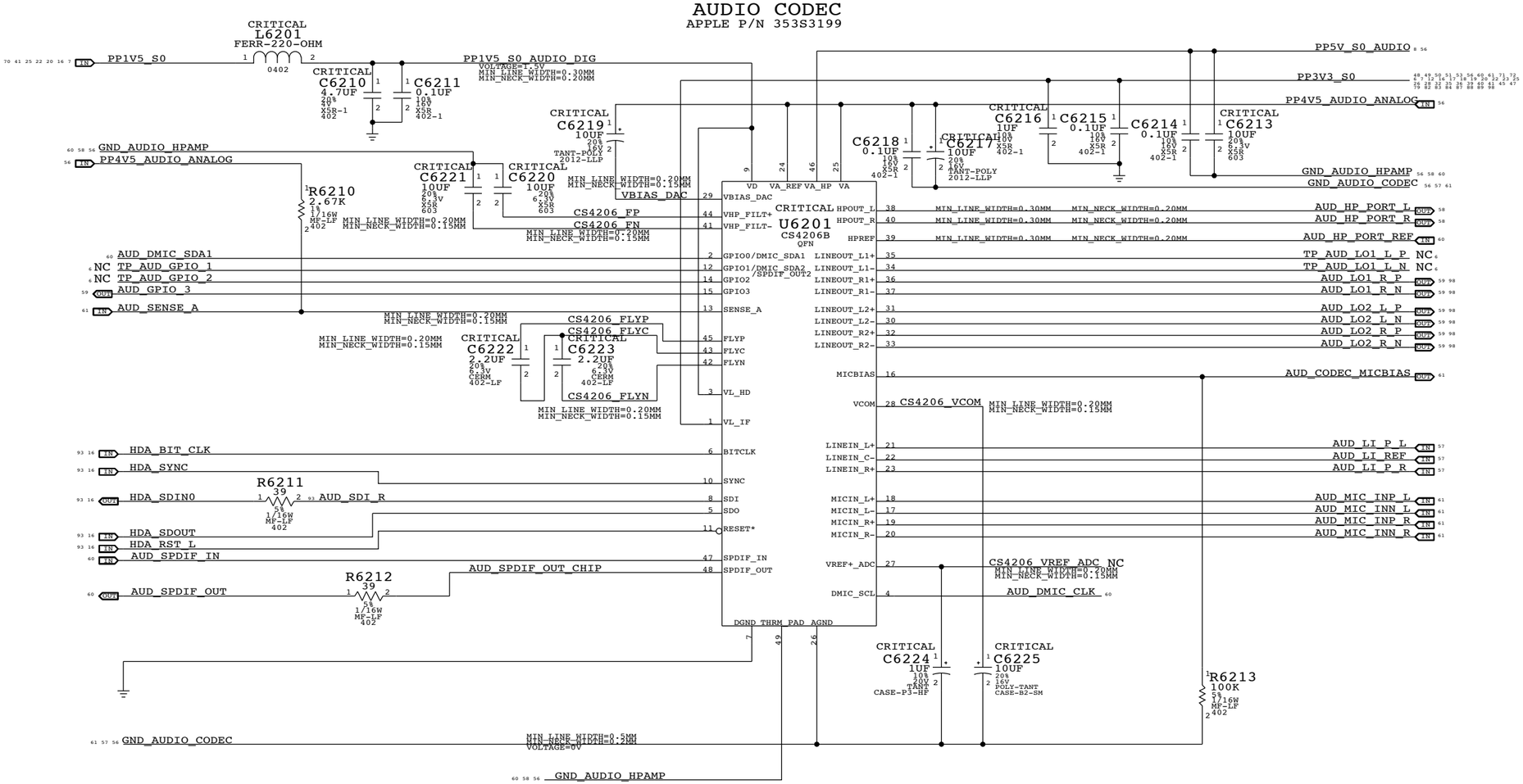
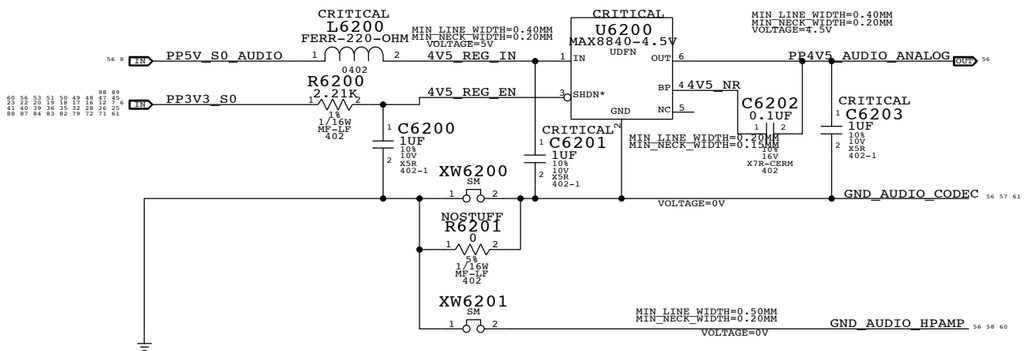
AUDIO CODEC
APPLE P/N 353S3199



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K91 AUDIO
SYNC_DATE=09/30/2010

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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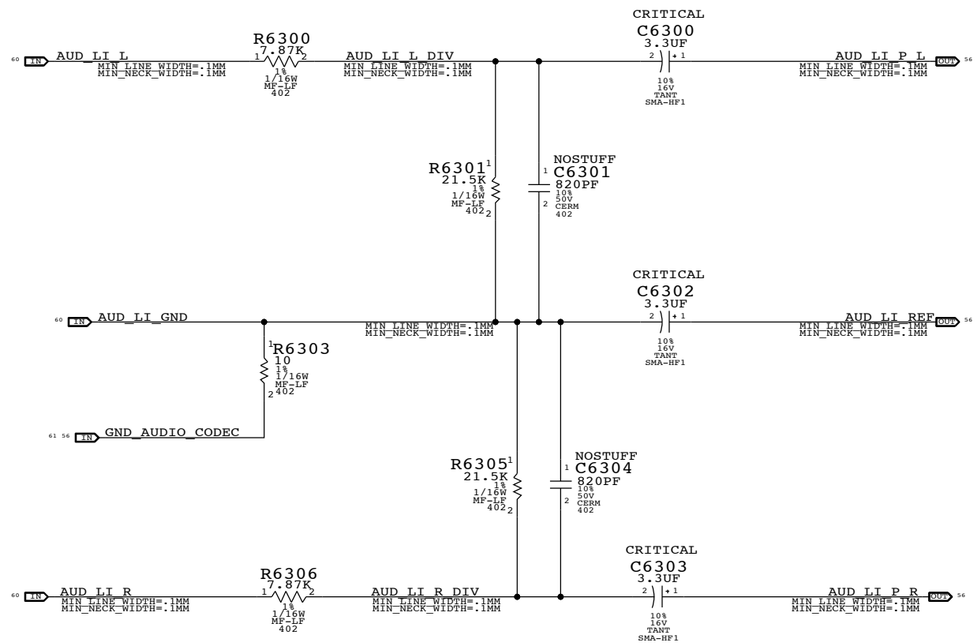
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC MASTER=K91 AUDIO SYNC DATE=07/12/2010

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

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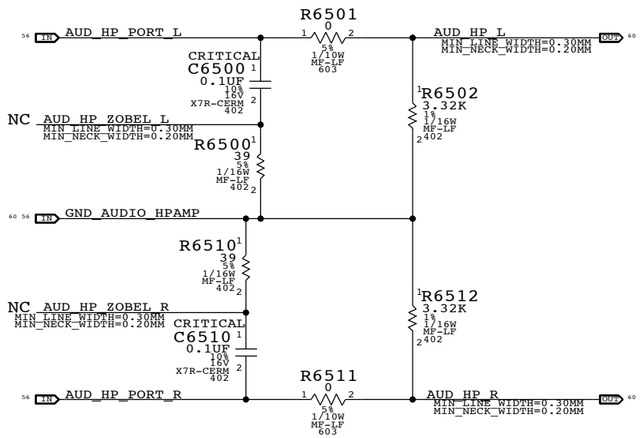
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC MASTER=K91 AUDIO SYNC DATE=07/12/2010

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

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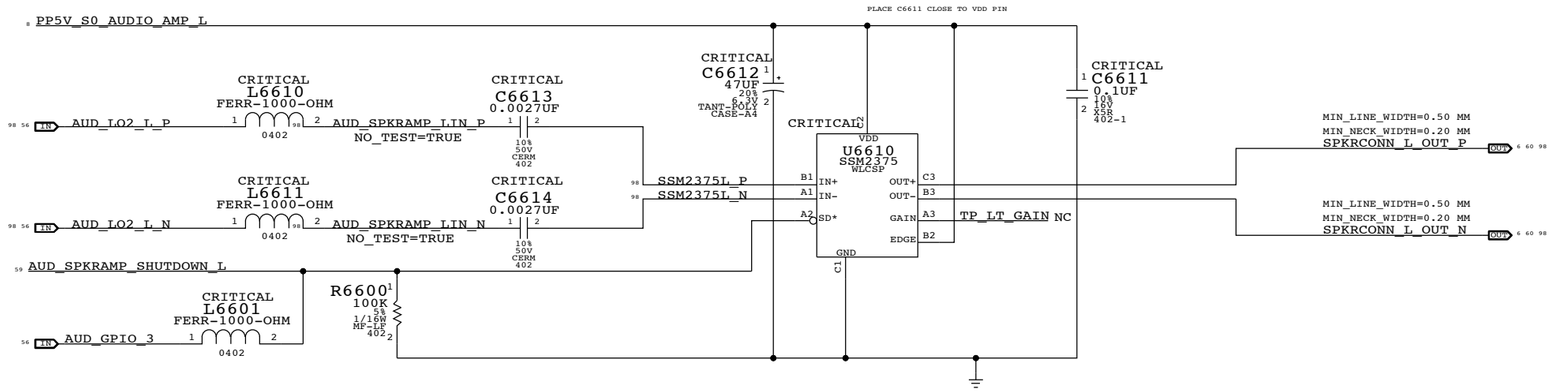
3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958

GAIN = +3 DB
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ



SYNC MASTER=K91 AUDIO | SYNC DATE=07/12/2010

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

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AUDIO JACK 1 LO/HP JACK, SPDIF TX

APN: 514-0671

CRITICAL J6700 SPDIF-TXRX-K24 F-RT-TH

MIC, DETECT, SWITCH, LEFT, RIGHT, GND

AUDIO

A - VIN, B - VCC, C - GND

OPERATING VOLTAGE 3.3

POF

SHELL, SHIELD PINS

PP3V3_S0

C6700 0.1UF 10% 16V X5R 402-1

C6701 2.2UF 20% 6.3V CERM 402-LF

AUD_CONNJ1_SLEEVE2

AUD_CONNJ1_SLEEVEDET

AUD_CONNJ1_TIPDET

AUD_CONNJ1_TIP

AUD_CONNJ1_RING

AUD_CONNJ1_SLEEVE

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.20MM

AUD_SPDIF_OUT

L6703 FERR-1000-OHM CRITICAL 0402

L6702 FERR-1000-OHM CRITICAL 0402

L6707 CRITICAL FERR-220-OHM 0402

L6701 CRITICAL FERR-220-OHM-2.5A 0603

L6704 CRITICAL FERR-220-OHM 0402

L6706 CRITICAL FERR-220-OHM 0402

L6705 FERR-1000-OHM CRITICAL 0402

HS_MIC_P

HS_MIC_N

AUD_HP_PORT_REF

GND_AUDIO_HPAMP

AUD_HP_R

AUD_HP_L

AUD_J1_SLEEVEDET_R

AUD_J1_TIPDET_R

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM

MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

R6700 10K 5% 1/16W MF-LF 402

CRITICAL DZ6703 6.8V-100PF 402

CRITICAL DZ6704 6.8V-100PF 402

CRITICAL DZ6706 6.8V-100PF 402

CRITICAL DZ6700 6.8V-100PF 402

CRITICAL DZ6701 6.8V-100PF 402

C6705 100PF 5% 50V CERM 402

GND_CHASSIS_AUDIO_JACK

XW6701 SM

XW6702 SM

R6701 0 5% 1/16W MF-LF 402

GND PATCH

GND_CHASSIS_AUDIO_JACK

AUDIO JACK 2 LINE IN JACK, SPDIF RX

APN: 514-0635

CRITICAL J6750 AUDIO-RCVR-M97 F-RT-TH5

DETECT_FOR_PLUG_TYPE, SWITCH, LEFT, RIGHT, GROUND

AUDIO

A - VDD, B - GND, C - VOUT

OPERATING VOLTAGE 3.3

POF

SHELL, SHIELD PINS

PP3V3_S0

C6750 1UF 10% 10V X5R 402-1

AUD_J2_OPT_OUT

R6749 4.7 5% 1/16W MF-LF 402

AUD_SPDIF_IN

AUD_CONNJ2_TIPDET

AUD_CONNJ2_RING

AUD_CONNJ2_TIP

AUD_CONNJ2_SLEEVE

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM

CRITICAL L6754 FERR-1000-OHM 0402

CRITICAL L6756 FERR-1000-OHM 0402

CRITICAL L6758 600-OHM-300MA 0402

CRITICAL L6752 FERR-1000-OHM 0402

AUD_LI_R

AUD_LI_L

AUD_LI_GND

AUD_J2_TIPDET_R

CRITICAL DZ6758 ESDALC5-1BM2 SOD882

CRITICAL DZ6757 ESDALC5-1BM2 SOD882

CRITICAL DZ6754 6.8V-100PF 402

CRITICAL DZ6756 6.8V-100PF 402

C6756 100PF 5% 50V CERM 402

GND_CHASSIS_AUDIO_JACK

MIC CONNECTOR

Dual DMIC removed.Added single analog mic like K18.

Sept 21st 2010

Place this in place of DMIC connector J6780

CRITICAL J6780 78171-0003 M-RT-SM

BI_MIC_N

BI_MIC_SHIELD

BI_MIC_P

DIGI_MIC CRITICAL J6783 78171-0004 M-RT-SM

DIGI_MIC CRITICAL L6783 600-OHM-300MA 0402

AUD_DMIC_CLK1 — CON_DMIC_CLK

DIGI_MIC CRITICAL L6784 600-OHM-300MA 0402

AUD_DMIC_SDA1 — CON_DMIC_SDA

DIGI_MIC CRITICAL L6785 600-OHM-300MA 0402

PP3V3_S0 — CON_DMIC_PWR

SPEAKER CONNECTOR

APN: 518S0519

CRITICAL J6781 78171-0002 M-RT-SM

SPKRCONN_L_OUT_P

SPKRCONN_L_OUT_N

CRITICAL J6782 78171-0004 M-RT-SM

APN: 518S0521

SPKRCONN_S_OUT_P

SPKRCONN_S_OUT_N

SPKRCONN_R_OUT_P

SPKRCONN_R_OUT_N

NOSTUFF CRITICAL C6781 33PF 5% 50V CERM 402

NOSTUFF CRITICAL C6782 33PF 5% 50V CERM 402

NOSTUFF CRITICAL C6783 33PF 5% 50V CERM 402

NOSTUFF CRITICAL C6784 33PF 5% 50V CERM 402

SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE: AUDIO: JACKS

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

PULLUPS ON MCP PAGE

SMBUS_PCH_CLK, SMBUS_PCH_DATA, AUD_I2C_INT_L, AUD_IPHS_SWITCH_EN

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

PP3V3_S0, R6886 10K, L6880 FERR-1000-OHM 0402, PP3V3_S0_HS_RX
MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=3.3V
C6880 10UF, C6887 0.1UF, R6882 0, R6883 0, R6884 0, R6885 0, R6887 100K
CSP MIKEY
APN:353S2640
U6880 CD3282A1 WCSP
HS_SCL, HS_SDA, HS_INT_L, HS_ENABLE, TIPDET_UNFILT
HS_MIC_BIAS, HS_SW_DET, HS_RX_BP
C6882 2.2UF, C6881 0.01UF, R6880 1K, R6881 2.2K
GND_AUDIO_CODEC

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)

AUD_SENSE_A, PP3V3_S0_AUDIO_F
R6801 220K, R6802 47K, C6801 0.1UF, AUD_J1_TIPDET_R, AUD_J1_DET_RC
APN:376S0613
AUD_OUTJACK_INSERT_L
Q6800 SSM6N15FEAPE SOT563
R6806 39.2K, R6805 20.0K
AUD_PORTA_DET_L NC, AUD_PORTB_DET_L NC
Q6801 SSM6N15FEAPE SOT563
R6803 220K, R6804 220K, C6802 0.01UF
AUD_J1_SLEEVEDET_INV, AUD_J1_SLEEVEDET_R
GND_AUDIO_CODEC

EXTRACTION NOTIFICATION

L6862 FERR-1000-OHM 0402, PP3V3_S0, PP3V3_S0_AUDIO_F
MIN_LINE_WIDTH=0.1MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=3.3V
C6861 0.1UF
R6865 100K, R6867 0, AUD_PERPH_DET_R, AUD_IP_PERIPHERAL_DET
R6864 220K, AUD_J1_TIPDET_INV
R6866 0, TIPDET_UNFILT
R6860 15K, AUD_J1_TIPDET_R, TIPDET_FILT
Q6803 SSM6N15FEAPE SOT563
C6860 0.1UF
GND_AUDIO_CODEC

PORT B RIGHT(BUILT-IN MIC)

AUD_CODEC_MICBIAS, R6850 100, MIC_BIAS_FILT, R6851 2.4K
C6852 2.2UF
GND_AUDIO_CODEC
C6850 0.1UF, AUD_MIC_INP_R, BI_MIC_HI_F, L6850 FERR-1000-OHM, BI_MIC_P
R6852 100K, C6853 0.001UF
C6851 0.1UF, AUD_MIC_INN_R, BI_MIC_LO_F, L6851 FERR-1000-OHM, BI_MIC_N
R6853 2.4K
XW6851 SM, BI_MIC_SHIELD
HP=80HZ
Place this next to the connector

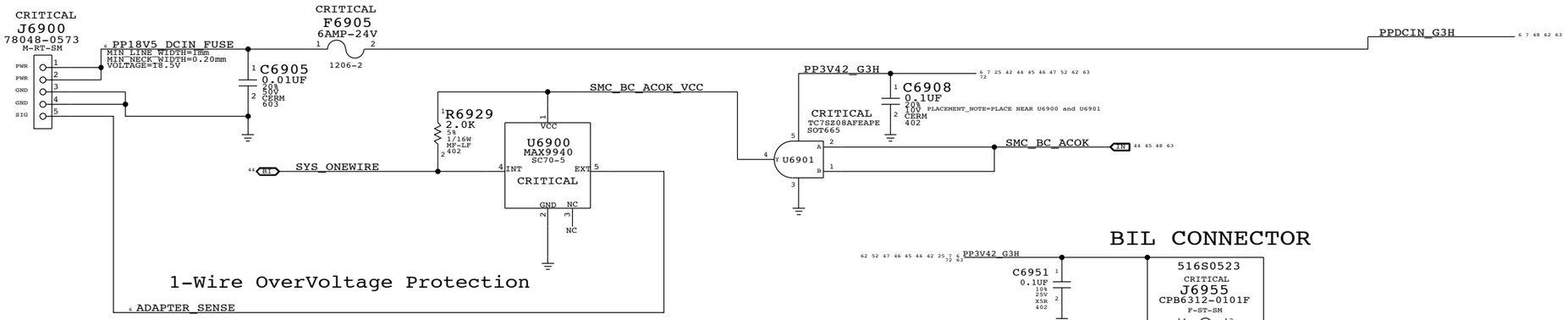
PORT C DETECT (LINE-IN)

AUD_SENSE_A, PP3V3_S0_AUDIO_F
R6813 10K, R6811 270K
AUD_INJACK_INSERT_L NC
Q6802 SSM3K15FV SOD-VESM-HF
APN:376S0612
R6812 47K, AUD_J2_TIPDET_R, AUD_J2_DET_RC
C6811 0.1UF
GND_AUDIO_CODEC

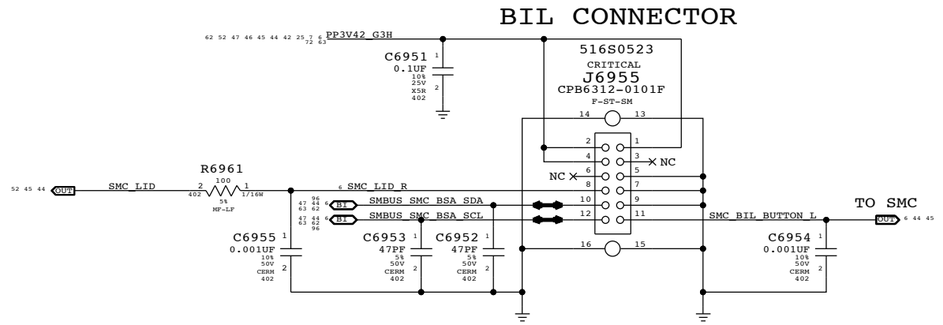
AUD_MIC_INP_L, AUD_MIC_INN_L, C6883 0.1UF, C6886 0.1UF, XW6880 SM
R6890 2.2K, R6888 100K, C6884 0.0082UF, C6885 27PF
HS_MIC_HI_RC, HS_MIC_P, HS_MIC_N
GND_AUDIO_CODEC

SYNC_MASTER=K91_AUDIO	SYNC_DATE=09/21/2010
PAGE TITLE	AUDIO: JACK TRANSLATORS
Apple Inc.	DRAWING NUMBER: D; SIZE: D; REVISION; BRANCH; PAGE: 68 OF 132; SHEET: 61 OF 101

MagSafe DC Power Jack

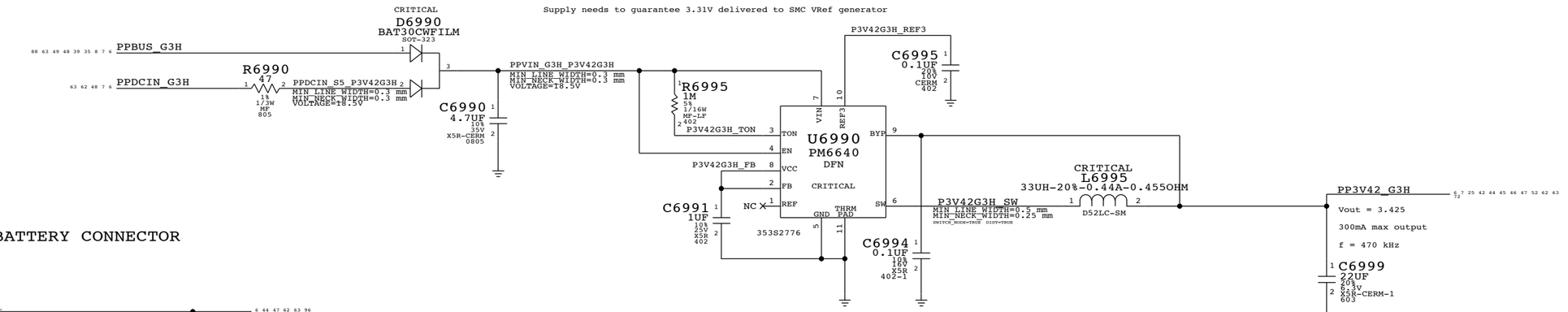


The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

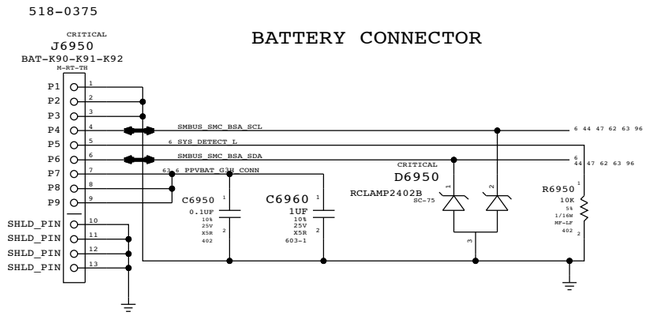


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER — SIZE: D

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BRANCH

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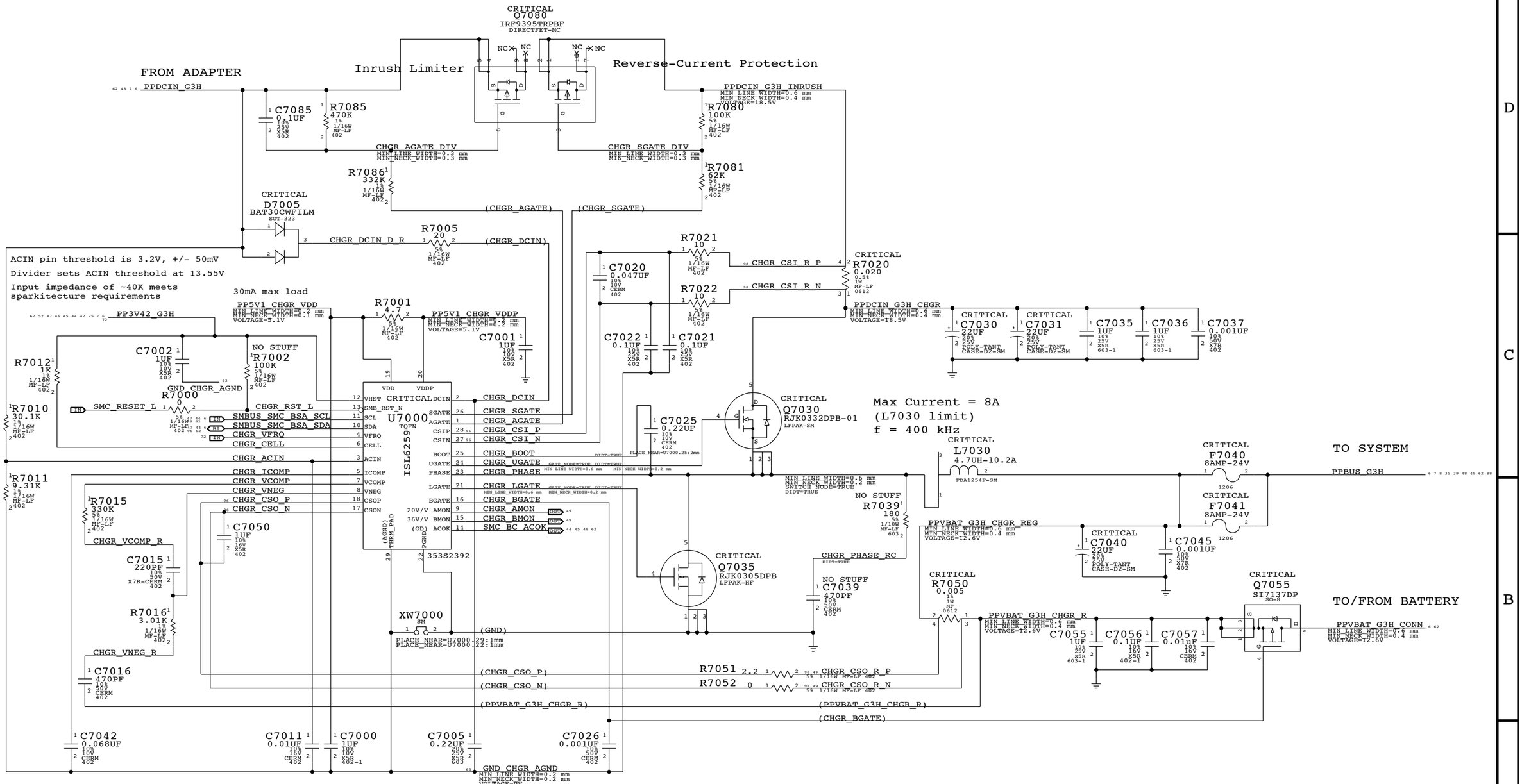

SYNC MASTER=K91 CHANG	SYNC DATE=07/20/2010
PAGE TITLE: PBus Supply & Battery Charger	
Apple Inc.	DRAWING NUMBER: SIZE: D
	REVISION:
	BRANCH:
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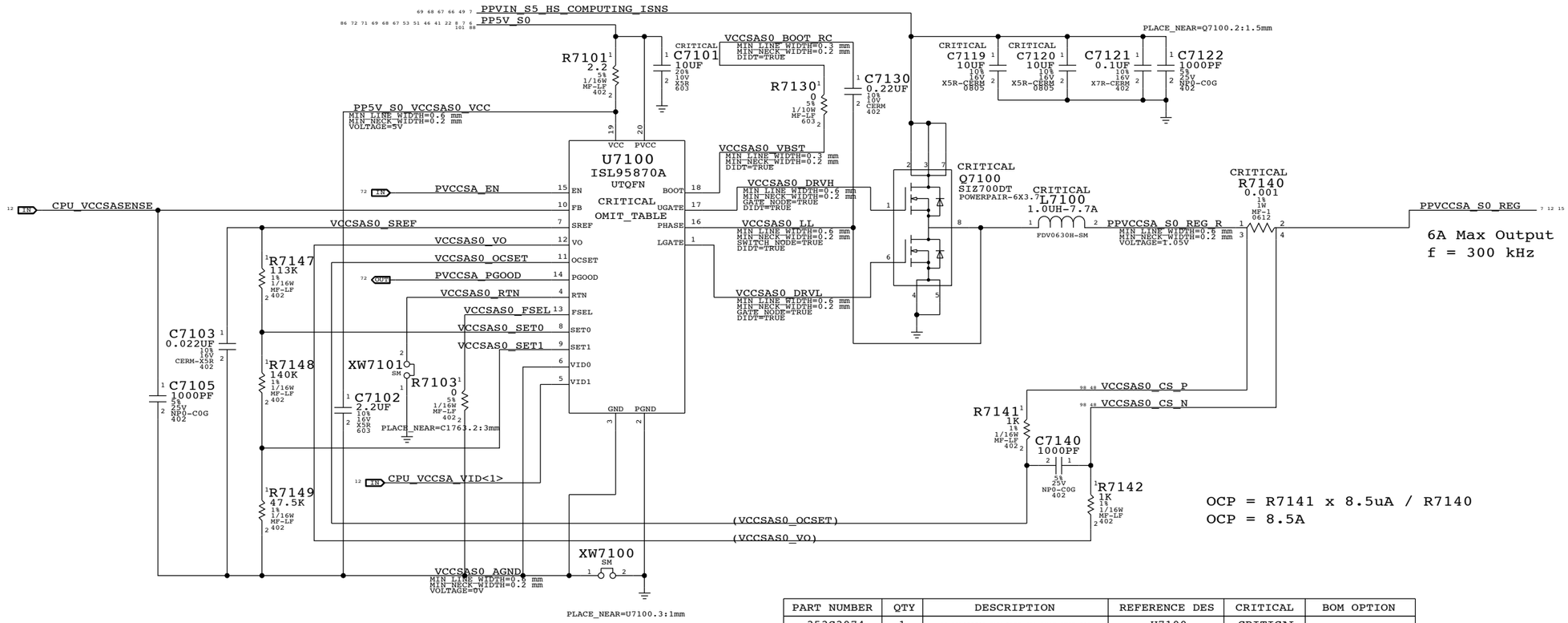

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC MASTER=K91_ERIC SYNC DATE=10/08/2010

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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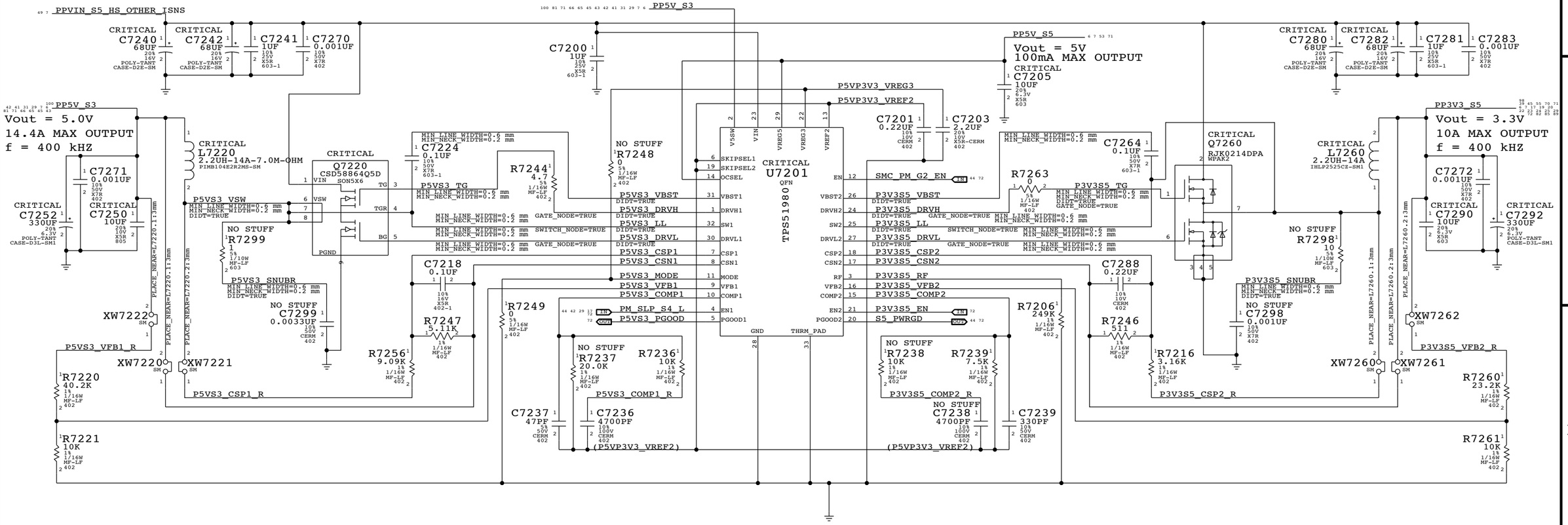

SYNC MASTER=K91 ERIC SYNC DATE=10/08/2010

PAGE TITLE
5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER | SIZE D

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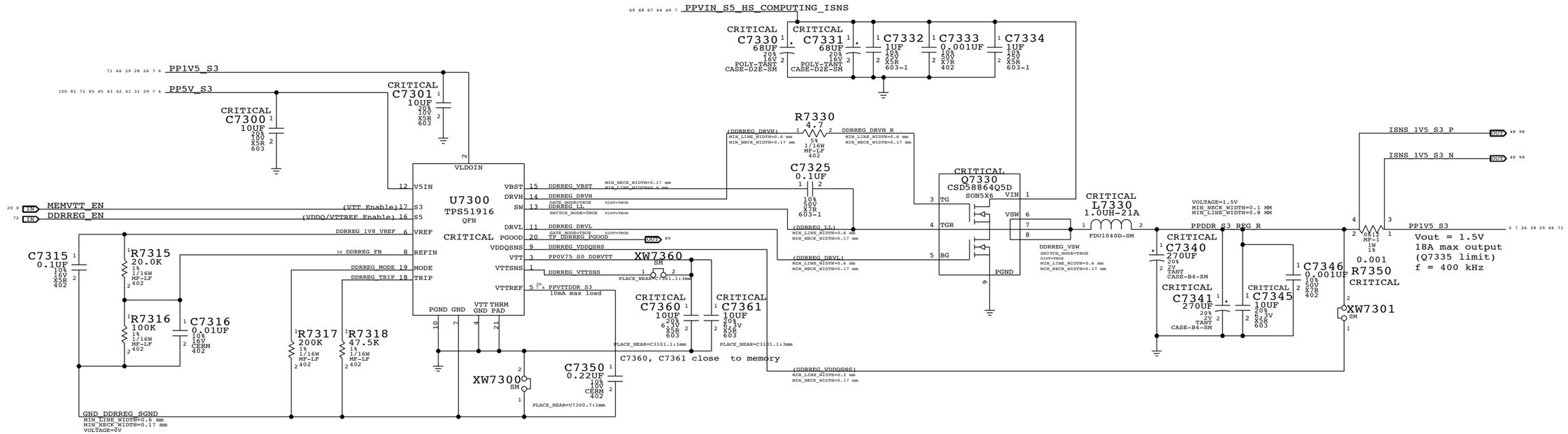

SYNC MASTER=K91 ERIC	SYNC DATE=10/08/2010
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION
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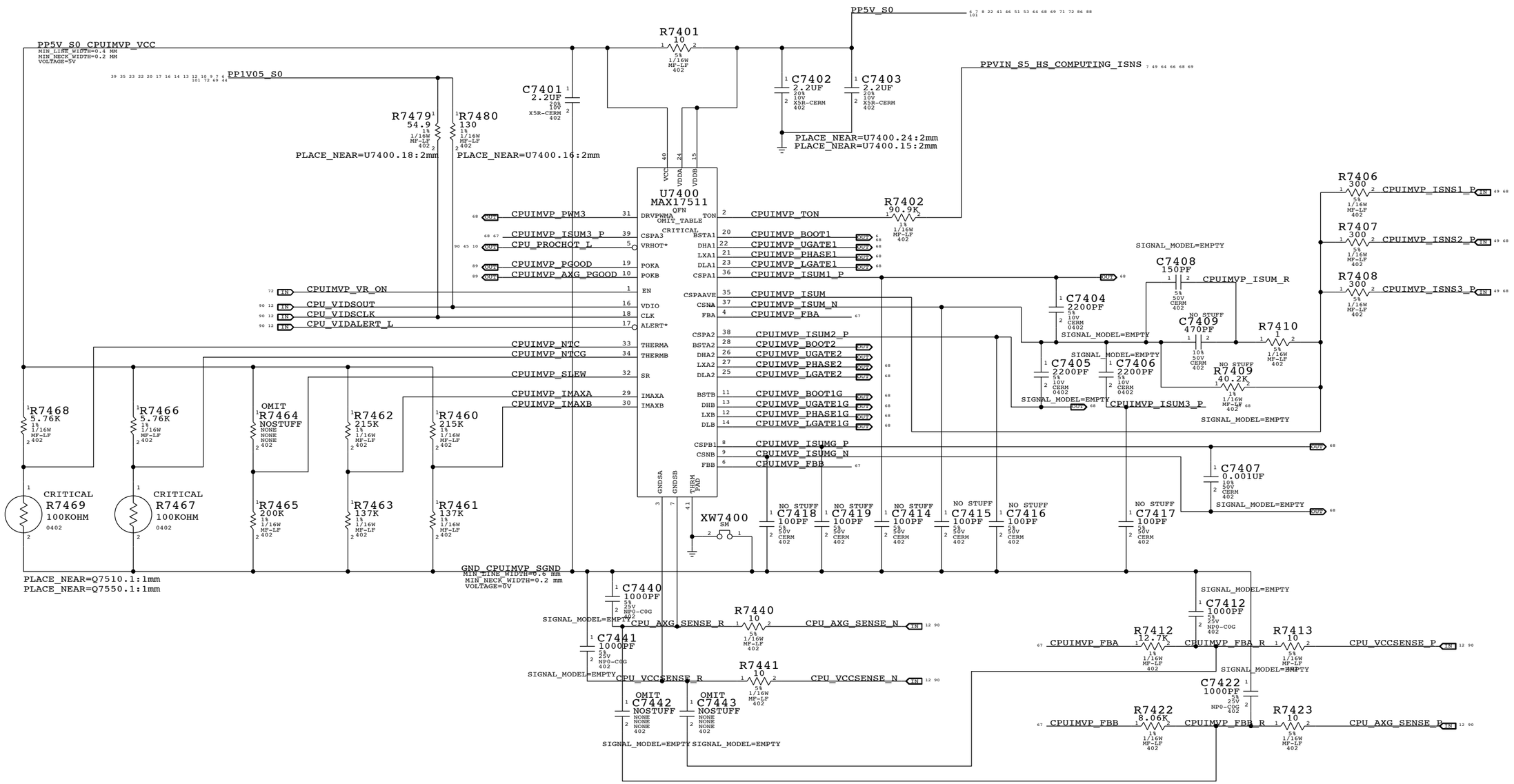
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	



SYNC MASTER=K91_ERIC SYNC DATE=10/08/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

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PHASE 1

PPVIN_S5_HS_COMPUTING_ISNS

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7510 0.36UH-20%-40A-0.00075OHM PIMA104E-SM 152S1019

CRITICAL R7510 0.00075 1% 1W MF 0612

PPVCORE_S0_CPU_PH1_L → PPVCORE_S0_CPU_PH1 → PPVCORE_S0_CPU

CPUIMVP_ISNS1_P / CPUIMVP_ISNS1_N → CPUIMVP_ISUM_N / CPUIMVP_ISUM1_P

CPUIMVP_BOOT1_RC: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

R7511 0 5% 1/16W MF-LF 402; C7511 0.22UF 10% 10V CERM 402

CPUIMVP_BOOT1: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

CPUIMVP_UGATE1: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE1: MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE1: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

376S0930

CRITICAL Q7515 IRF6798MTRPBF DIRECTFET-MX

R7512 2.2 5% 1/10W MF-LF 603; NOSTUFF

CPUIMVP_PH1_SNUB: NOSTUFF C7512 0.001UF 10% 50V CERM 402; DIDT=TRUE

R7513 46.4 1% 1/16W MF-LF 402

R7514 10.2 1% 1/16W MF-LF 402

NOSTUFF C7571 330PF 10% 50V CERM 402

THESE TWO CAPS ARE FOR EMC

CRITICAL C7513 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7514 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7515 10UF 10% 16V X5R-CERM 0805

CRITICAL C7516 10UF 10% 16V X5R-CERM 0805

CRITICAL C7517 1UF 10% 16V X5R 402

CRITICAL C7518 0.001UF 10% 50V X7R 402

CRITICAL C7519 0.001UF 10% 50V X7R 402

PHASE 2

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7520 0.36UH-20%-40A-0.00075OHM PIMA104E-SM 152S1019

CRITICAL R7520 0.00075 1% 1W MF 0612

PPVCORE_S0_CPU_PH2_L → PPVCORE_S0_CPU_PH2 → PPVCORE_S0_CPU

CPUIMVP_ISNS2_P / CPUIMVP_ISNS2_N → CPUIMVP_ISUM_N / CPUIMVP_ISUM2_P

CPUIMVP_BOOT2_RC: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

R7521 0 5% 1/16W MF-LF 402; C7521 0.22UF 10% 10V CERM 402

CPUIMVP_BOOT2: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

CPUIMVP_UGATE2: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE2: MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE2: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

376S0930

CRITICAL Q7525 IRF6798MTRPBF DIRECTFET-MX

R7522 2.2 5% 1/10W MF-LF 603; NOSTUFF

CPUIMVP_PH2_SNUB: NOSTUFF C7522 0.001UF 10% 50V CERM 402; DIDT=TRUE

R7523 46.4 1% 1/16W MF-LF 402

R7524 10.2 1% 1/16W MF-LF 402

NOSTUFF C7572 330PF 10% 50V CERM 402

THESE TWO CAPS ARE FOR EMC

CRITICAL C7523 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7524 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7525 10UF 10% 16V X5R-CERM 0805

CRITICAL C7526 10UF 10% 16V X5R-CERM 0805

CRITICAL C7527 1UF 10% 16V X5R 402

CRITICAL C7528 0.001UF 10% 50V X7R 402

CRITICAL C7529 0.001UF 10% 50V X7R 402

PHASE 3

PP5V_S0

U7541 MAX17491 TQFN CRITICAL

VDD; PWN; BST; DH; LX; DL; SKIP*; GND; THRM PAD

R7547 10K 5% 1/16W MF-LF 402

C7541 1UF 10% 16V X5R 402

CPUIMVP_PWM3 → CPUIMVP_SKIP

CPUIMVP_BOOT3: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.27 MM, DIDT=TRUE

CPUIMVP_UGATE3: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE3: MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE3: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_BOOT3_RC: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

R7531 0 5% 1/16W MF-LF 402; C7531 0.22UF 10% 10V CERM 402

376S0772

CRITICAL Q7530 IRF6710 S1

CRITICAL L7530 0.36UH-20%-40A-0.00075OHM PIMA104E-SM 152S1019

CRITICAL R7530 0.00075 1% 1W MF 0612

SWITCH_NODE=TRUE; PPVCORE_S0_CPU_PH3_L → PPVCORE_S0_CPU_PH3 → PPVCORE_S0_CPU

CPUIMVP_ISNS3_P / CPUIMVP_ISNS3_N → CPUIMVP_ISUM_N / CPUIMVP_ISUM3_P

376S0930

CRITICAL Q7535 IRF6798MTRPBF DIRECTFET-MX

R7532 2.2 5% 1/10W MF-LF 603; NOSTUFF

CPUIMVP_PH3_SNUB: NOSTUFF C7532 0.001UF 10% 50V CERM 402; DIDT=TRUE

R7533 46.4 1% 1/16W MF-LF 402

R7534 10.2 1% 1/16W MF-LF 402

NOSTUFF C7573 330PF 10% 50V CERM 402

THESE TWO CAPS ARE FOR EMC

CRITICAL C7533 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7534 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7535 10UF 10% 16V X5R-CERM 0805

CRITICAL C7536 10UF 10% 16V X5R-CERM 0805

CRITICAL C7537 1UF 10% 16V X5R 402

CRITICAL C7538 0.001UF 10% 50V X7R 402

CRITICAL C7539 0.001UF 10% 50V X7R 402

Additonal Input Bulk Caps

CRITICAL C7561 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7562 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7563 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7564 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7565 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7566 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7567 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7568 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7569 68UF 20% 16V POLY-TANT CASE-D2E-SM

AXG PHASE

PPVIN_S5_HS_COMPUTING_ISNS

CRITICAL Q7550 CSD58864Q5D SON5X6

CRITICAL L7550 0.36UH-20%-40A-0.00075OHM PIMA104E-SM 152S1019

CRITICAL R7550 0.00075 1% 1W MF 0612

CPUIMVP_VSWG; PPVCORE_S0_AXG_L → PPVCORE_S0_AXG

CPUIMVP_ISNS1G_P / CPUIMVP_ISNS1G_N → CPUIMVP_ISUMG_N / CPUIMVP_ISUMG_P

376S0906

CPUIMVP_BOOT1G: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE

R7556 0 5% 1/16W MF-LF 402; CPUIMVP_BOOT1G_R: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE

C7551 0.22UF 10% 10V CERM 402

CPUIMVP_UGATE1G: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

R7555 4.7 5% 1/16W MF-LF 402; CPUIMVP_UGATE1G_R: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE1G: MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE1G: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

R7552 2.2 5% 1/10W MF-LF 603; NOSTUFF

CPUIMVP_AXG_SNUB: NOSTUFF C7552 0.001UF 10% 50V CERM 402; DIDT=TRUE

R7553 46.4 1% 1/16W MF-LF 402

R7554 10.2 1% 1/16W MF-LF 402

NOSTUFF C7574 330PF 10% 50V CERM 402

THESE TWO CAPS ARE FOR EMC

CRITICAL C7553 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7554 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7555 10UF 10% 16V X5R-CERM 0805

CRITICAL C7556 10UF 10% 16V X5R-CERM 0805

CRITICAL C7557 1UF 10% 16V X5R 402

CRITICAL C7558 0.001UF 10% 50V X7R 402

C7559 0.001UF 10% 50V X7R 402

SYNC MASTER=K91_ERIC	SYNC DATE=09/22/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER: — SIZE: D
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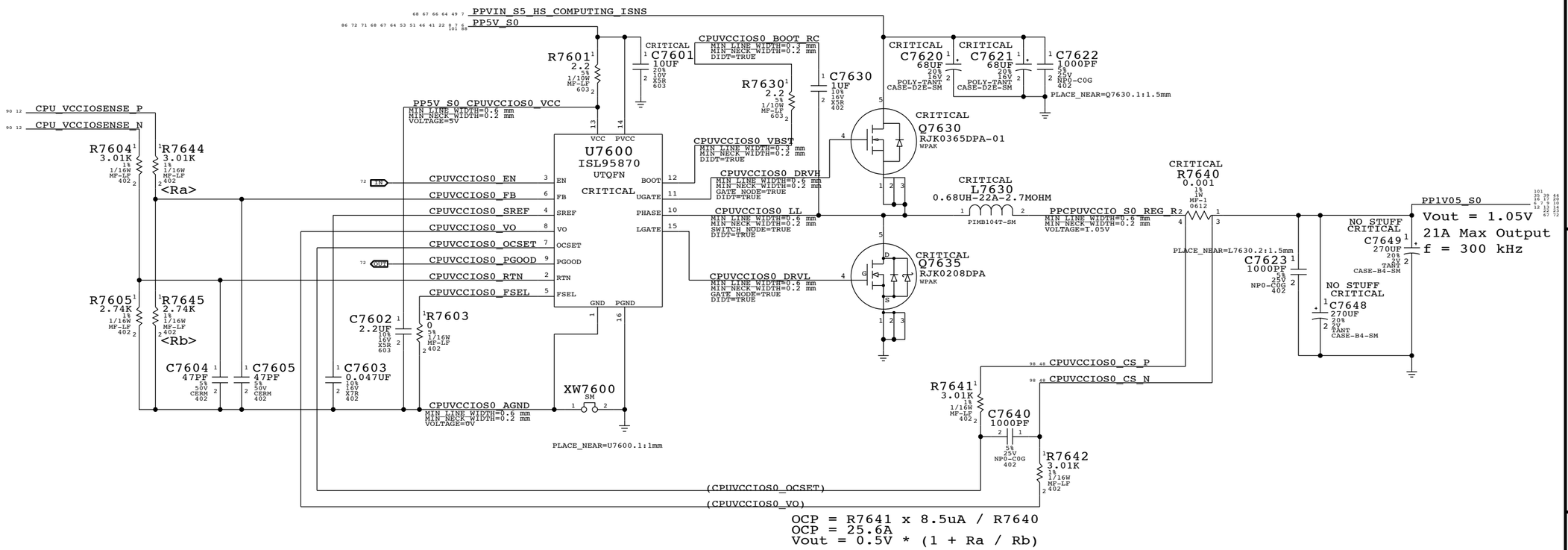
CPU VCCIO (1.05V S0) Regulator



SYNC MASTER=K91 ERIC — SYNC DATE=10/08/2010

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

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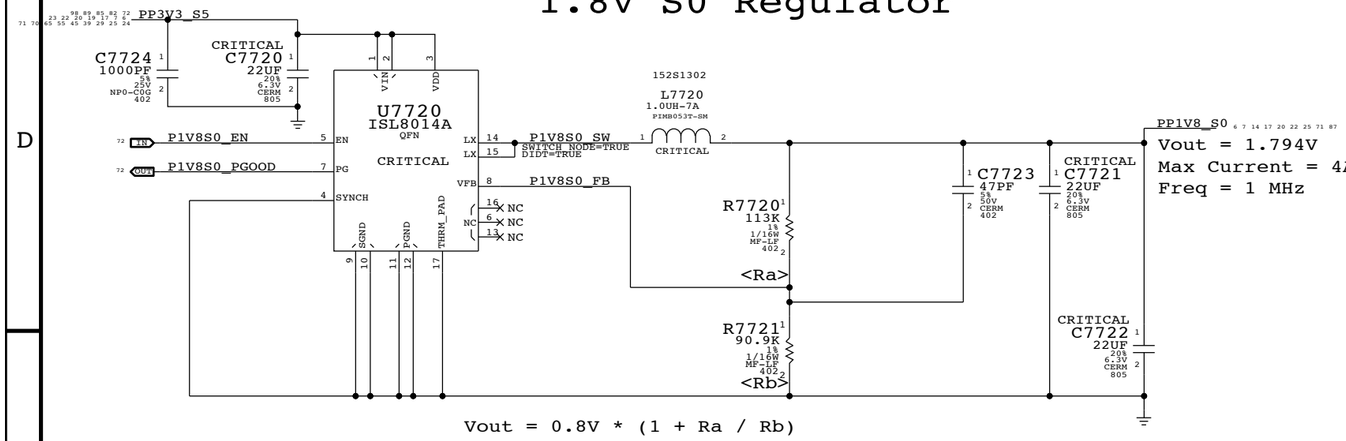
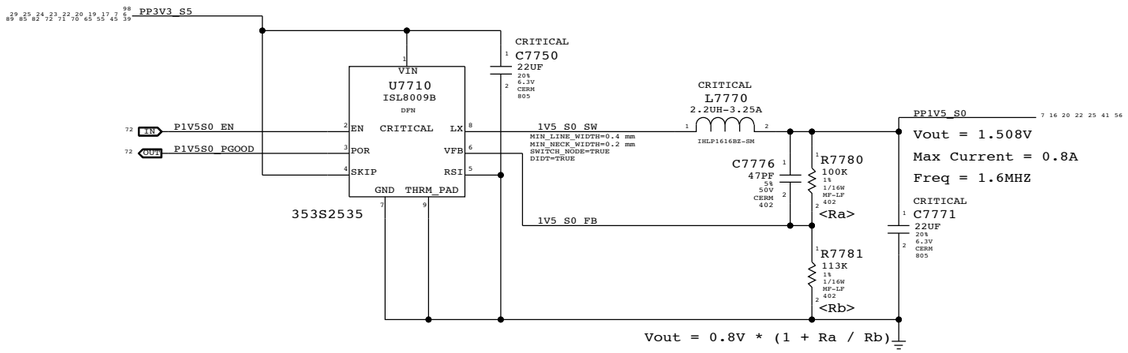
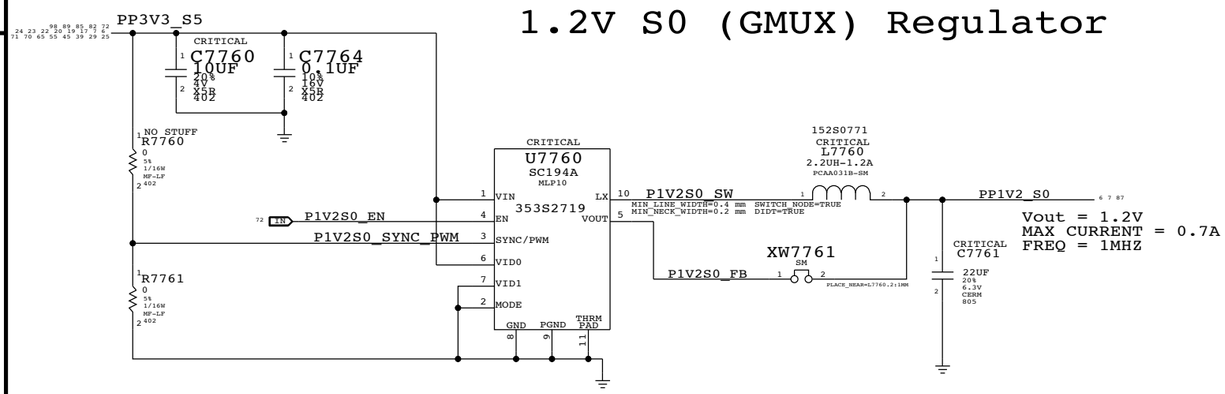
1.8V S0 Regulator



1.5V S0 Regulator

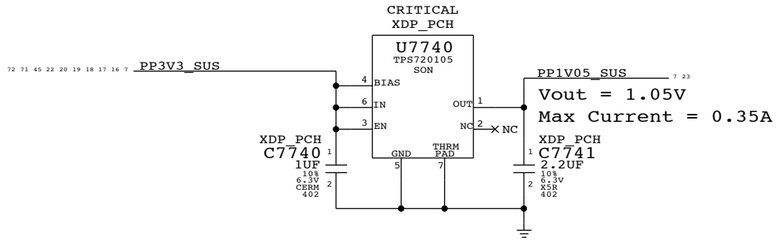


1.2V S0 (GMUX) Regulator

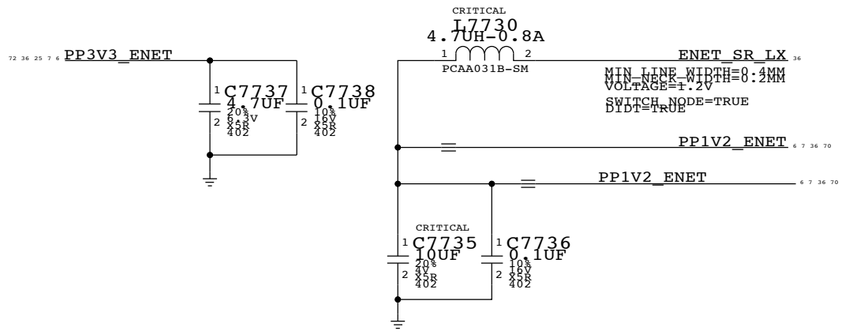


1.05V SUS LDO

Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



CAESAR IV 1.2V INT.VR CMPTS



SYNC_MASTER=K91_ERIC SYNC_DATE=11/01/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER | SIZE: D

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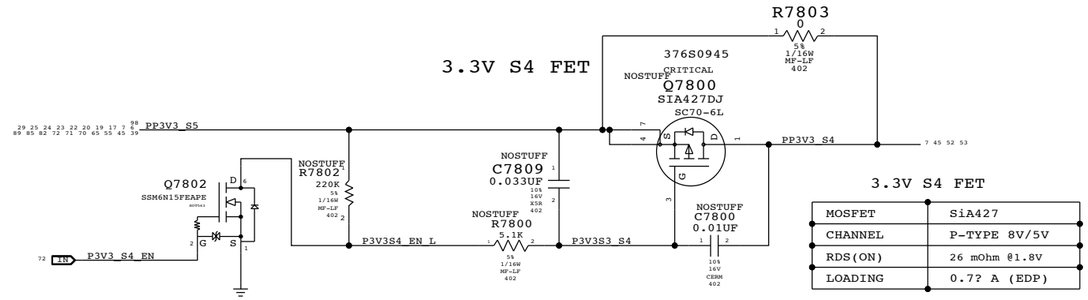
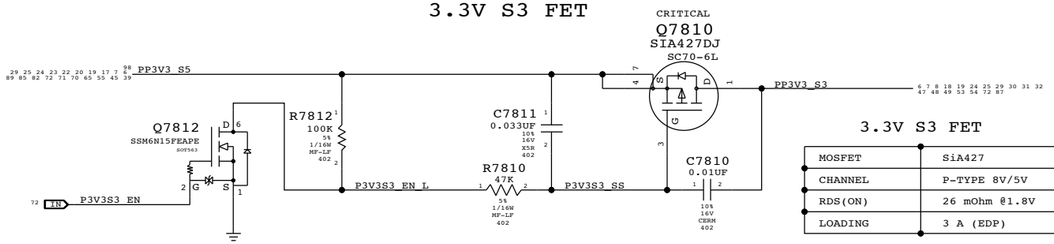
3.3V S4 FET



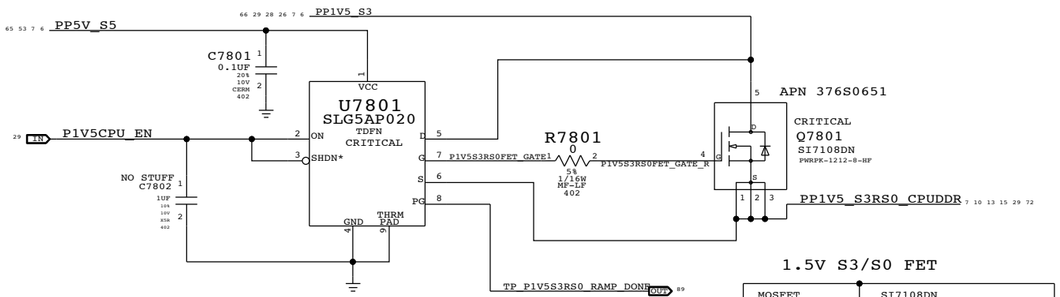
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



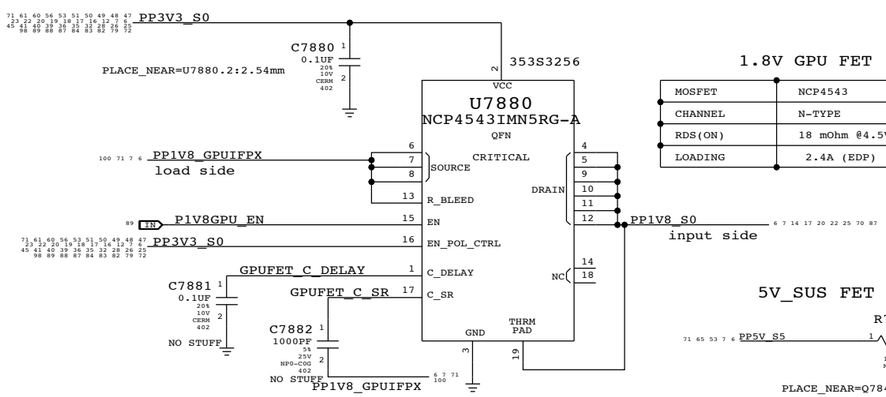
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



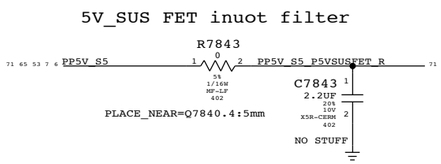
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET



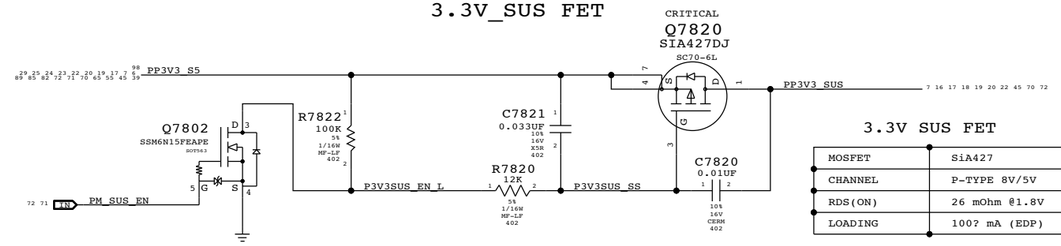
1.8V GPU FET	
MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter



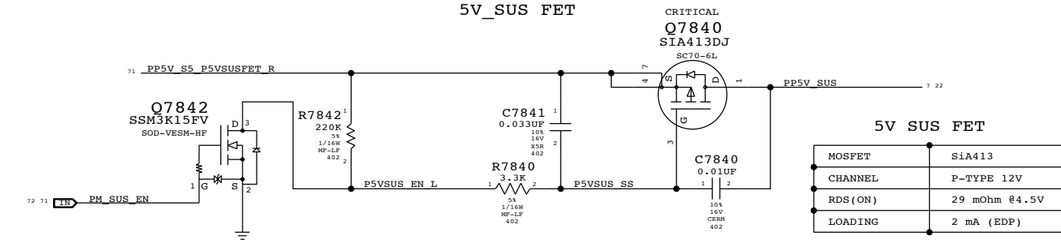
U7880 default Turn on delay EN--> on is 200~650us.

3.3V_SUS FET



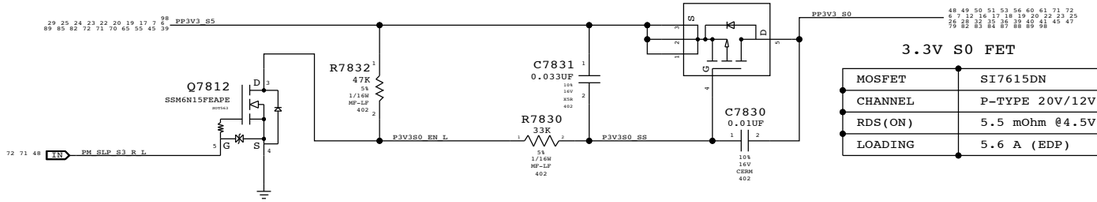
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



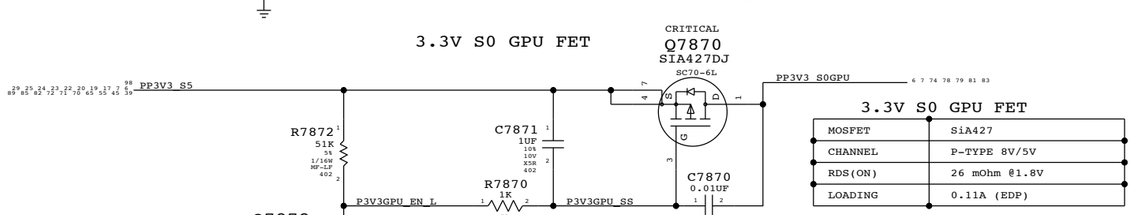
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



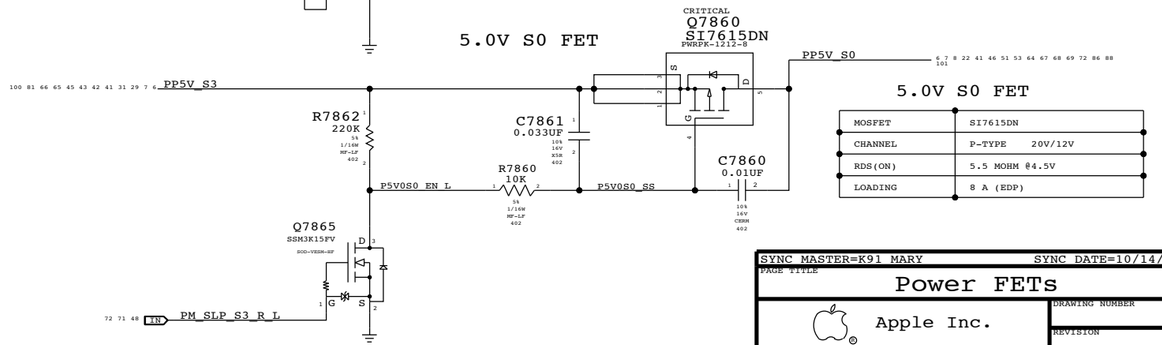
3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC_MASTER=K91_MARY SYNC_DATE=10/14/2010

PAGE TITLE

Power FETs

Apple Inc.

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S5 Rail Enables & PGOOD

SMC_PM_G2_EN (OUT) → SMC_PM_G2_EN (IN), MAKE_BASE=TRUE
R7940 100 5% 1/16W MF-LF 402, PLACE_NEAR=U7201.21:7mm
P3V3S5_EN (OUT) → P3V3S5_EN (IN), MAKE_BASE=TRUE
C7942 0.0033UF 10% 50V CERM 402 NO STUFF

PP3V42_G3H, PLACE_NEAR=U7201.20:7mm
R7941 100K 5% 1/16W MF-LF 402

S5_PWRGD (OUT) → S5_PWRGD (IN), MAKE_BASE=TRUE

S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V/5.0V S4 ENABLE

NOSTUFF
R7916 0 5% 1/16W MF-LF 402, PLACE_NEAR=U1800.G18:5mm
PM_SLP_S5_L (IN) → P3V3_S4_EN (OUT), MAKE_BASE=TRUE
PM_SLP_S5_L:100K pull down on PCH page

3.3V,5V S3 ENABLE

PM_SLP_S4_L (IN), MAKE_BASE=TRUE
PM_SLP_S4_L:100K pull down in PCH page
(PM_SLP_S4_L)
R7911 5.1K 5% 1/16W MF-LF 402, PLACE_NEAR=U7300.16:6mm
R7912 0 5% 1/16W MF-LF 402, PLACE_NEAR=Q7812.2:6mm
R7913 3.3K 5% 1/16W MF-LF 402, PLACE_NEAR=U5701.4:6mm
PM_SLP_S4_L (OUT), TPAD_VBUS_EN (OUT)
P3V3S3_EN (IN) → P3V3S3_EN (OUT), MAKE_BASE=TRUE
DDRREG_EN (IN) → DDRREG_EN (OUT), MAKE_BASE=TRUE
C7910 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C7912 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

ALL_SYS_PWRGD → R7974 0 5% 1/16W MF-LF 402, PLACE_NEAR=U7400.7:5mm → CPUIMVP_VR_ON (OUT)
PLACE_NEAR=U7400.7:5mm
R7976 0 NO STUFF 5% 1/16W MF-LF 402
CPUVCCIOS0_PGOOD → R7975 0 5% 1/16W MF-LF 402, PLACE_NEAR=U7400.7:5mm → PM_PECI_PWRGD (OUT)

3.3V/5.0V Sus ENABLE

PP3V3_S5, PLACE_NEAR=U7940.1:2.3mm
C7940 0.1uF 20% 10V CERM 402
U7940 74AUP1G3208 SOT891 (VCC, A, B, C, Y, GND)
SMC_BATLOW_L:100K pull up on SMC page
SMC_BATLOW_L (IN)
PM_SLP_SUS_L:100K pull down on PCH page
PM_SLP_SUS_L (IN)
PM_SUS_EN (OUT), MAKE_BASE=TRUE
NO STUFF R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

R7978 100 5% 1/16W MF-LF 402
PM_SLP_S3_L (IN)
PM_SLP_S3_L:100K pull down in PCH page
(PM_SLP_S3_R_L)
R7987 33K 5% 1/16W MF-LF 402, PLACE_NEAR=U7100.15:6mm
R7981 20K 5% 1/16W MF-LF 402, PLACE_NEAR=U7600.3:6mm
R7985 20K 5% 1/16W MF-LF 402, PLACE_NEAR=U7760.4:6mm
R7988 10K 5% 1/16W MF-LF 402, PLACE_NEAR=U7710.2:6mm
R7986 5.1K 5% 1/16W MF-LF 402, PLACE_NEAR=U7720.5:6mm
PM_SLP_S3_R_L (OUT), MAKE_BASE=TRUE
P1V8S0_EN (OUT), MAKE_BASE=TRUE
P1V5S0_EN (OUT), MAKE_BASE=TRUE
P1V2S0_EN (OUT), MAKE_BASE=TRUE
CPUVCCIOS0_EN (OUT), MAKE_BASE=TRUE
PVCCSA_EN (OUT), MAKE_BASE=TRUE
C7987 C7981 C7985 1UF C7988 C7986 0.47UF 10% 6.3V CERM-X5R 402

CHGR VFRQ Generation

PP3V42_G3H
R7931 100K 5% 1/16W MF-LF 402
CHGR_VFRQ (OUT)
Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

PP3V3_S5, PP3V3_S0
R7951 15.0K 1% 1/16W MF-LF 402
R7956 150K 1% 1/16W MF-LF 402
S0PGD_C
ALL_SYS_PWRGD
R7953 1K 5% 1/16W MF-LF 402
VMON_3V3_DIV, VMON_Q2_BASE
R7952 7.15K 1% 1/16W MF-LF 402
R7954 1K 5% 1/16W MF-LF 402
PP1V5_S3RS0_CPUDDR, PP1V5_S3RS0, VMON_Q3_BASE
R7955 1K 5% 1/16W MF-LF 402
PP1V05_S0, VMON_Q4_BASE
Q7950 ASMCC0179 DFN2015H4-8 (Q1 Q2 Q3 Q4) CRITICAL
NC NC NC
353S2809 S0PGD_BJT_GND_R
R7957 100 5% 1/16W MF-LF 402

Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

PP3V3_S5, PLACE_NEAR=U7930.6:2.3mm
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
C7930 0.1uF 20% 10V CERM 402
CRITICAL
U7930 TPS3808G33DBVRG4 SOT23-6 (VDD, SENSE, CT, RESET*, MR*, GND)
R7933 100K 5% 1/16W MF-LF 402
PP3V3_SUS
PM_RSMRST_L (OUT)
PM_RSMRST_L goes to U1800.C21
Sus_PGOOD_CT
C7931 0.001UF 20% 50V CERM 402 NO STUFF

ENET Enable Generation

3.3V ENET FET
CRITICAL
Q7922 NTR4101P SOT-23-HF
PP3V3_S3
R7921 10K 5% 1/16W MF-LF 402
R7922 100K 5% 1/16W MF-LF 402
PM_SLP_S3_ENET
P3V3ENET_SS
C7921 0.033UF 10% 16V X5R 402
C7922 0.01UF 10% 16V CERM 402
PP3V3_ENET

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

Q7921 SSM3K15FV SOD-VESM-HF
PM_SLP_S3_L (IN)
Q7925 2N7002DW-X-G SOT-363
WOL_EN (IN)
PM_WLAN_EN_L (OUT)
Q7925 2N7002DW-X-G SOT-363
AP_PWR_EN (IN)
AC_EN_L
(AC_EN_L)
Q7920 2N7002DW-X-G SOT-363
NO STUFF R7929 0 5% 1/16W MF-LF 402
SMC_ADAPTER_EN (IN)
Q7920 2N7002DW-X-G SOT-363
(PM_SLP_S3_L)

S0 Rail PGOOD Circuitry

Thresholds: (ISL Version in development)
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP5V_S0, PP3V3_S0
R7960 6.04K 1% 1/16W MF-LF 402
R7970 10K 1% 1/16W MF-LF 402
R7972 6.04K 1% 1/16W MF-LF 402
R7961 15.0K 1% 1/16W MF-LF 402
R7971 10K 1% 1/16W MF-LF 402
R7973 15.0K 1% 1/16W MF-LF 402
PP5V_DIV_VMON, PP1V05_DIV_VMON, PP1V05_VID_VMON
PP1V05_S3RS0_CPUDDR, PP1V05_S0
C7960 0.1uF 20% 10V CERM 402
S0PGOOD_ISL
U7960 ISL88042IRTEZ TDFN (IPU) CRITICAL (VDD, V2MON, V3MON, V4MON, MR*, RST*, GND, THRM_PAD)
NC
353S2310
S0PGOOD_ISL → R7962 330 5% 1/16W MF-LF 402 → ALL_SYS_PWRGD_R → ALL_SYS_PWRGD (OUT)
R7967 10K 5% 1/16W MF-LF 402 → PP3V3_S0
P1V5S0_PGOOD (IN) → R7968 100 5% 1/16W MF-LF 402
P1V5S0_PGOOD from U7710
P1V8S0_PGOOD (IN) → R7966 100 5% 1/16W MF-LF 402
P5VS3_PGOOD (IN) → R7965 100 5% 1/16W MF-LF 402
CPUVCCIOS0_PGOOD (IN) → R7964 100 5% 1/16W MF-LF 402
PVCCSA_PGOOD (IN) → R7963 100 5% 1/16W MF-LF 402

SMC_S4_WAKESRC_EN → SMC_S4_WAKESRC_EN (OUT), MAKE_BASE=TRUE

SYNC_MASTER=K91_MARY SYNC_DATE=07/22/2010
PAGE TITLE: Power Control 1/ENABLE
Apple Inc.
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BRANCH:
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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEG_R2D_C_P<0>	C8020 0.1UF	PEG_R2D_P<0>	PEG_D2R_C_P<0>	C8055 0.1UF	PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8021 0.1UF	PEG_R2D_N<0>	PEG_D2R_C_N<0>	C8056 0.1UF	PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8022 0.1UF	PEG_R2D_P<1>	PEG_D2R_C_P<1>	C8057 0.1UF	PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8023 0.1UF	PEG_R2D_N<1>	PEG_D2R_C_N<1>	C8058 0.1UF	PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8024 0.1UF	PEG_R2D_P<2>	PEG_D2R_C_P<2>	C8059 0.1UF	PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8025 0.1UF	PEG_R2D_N<2>	PEG_D2R_C_N<2>	C8060 0.1UF	PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8026 0.1UF	PEG_R2D_P<3>	PEG_D2R_C_P<3>	C8061 0.1UF	PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8027 0.1UF	PEG_R2D_N<3>	PEG_D2R_C_N<3>	C8062 0.1UF	PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8028 0.1UF	PEG_R2D_P<4>	PEG_D2R_C_P<4>	C8063 0.1UF	PEG_D2R_P<4>
PEG_R2D_C_N<4>	C8029 0.1UF	PEG_R2D_N<4>	PEG_D2R_C_N<4>	C8064 0.1UF	PEG_D2R_N<4>
PEG_R2D_C_P<5>	C8030 0.1UF	PEG_R2D_P<5>	PEG_D2R_C_P<5>	C8065 0.1UF	PEG_D2R_P<5>
PEG_R2D_C_N<5>	C8031 0.1UF	PEG_R2D_N<5>	PEG_D2R_C_N<5>	C8066 0.1UF	PEG_D2R_N<5>
PEG_R2D_C_P<6>	C8032 0.1UF	PEG_R2D_P<6>	PEG_D2R_C_P<6>	C8067 0.1UF	PEG_D2R_P<6>
PEG_R2D_C_N<6>	C8033 0.1UF	PEG_R2D_N<6>	PEG_D2R_C_N<6>	C8068 0.1UF	PEG_D2R_N<6>
PEG_R2D_C_P<7>	C8034 0.1UF	PEG_R2D_P<7>	PEG_D2R_C_P<7>	C8069 0.1UF	PEG_D2R_P<7>
PEG_R2D_C_N<7>	C8035 0.1UF	PEG_R2D_N<7>	PEG_D2R_C_N<7>	C8070 0.1UF	PEG_D2R_N<7>

All: 1 | 2 | 10%6.3VX5R201

PEG_R2D_P<0>	AA38	PCIE_RX0P	U8000 FCBGA (1 OF 9) PCIE WHISTLER 40NM-ES OMIT	PCIE_TX0P	Y33	PEG_D2R_C_P<0>
PEG_R2D_N<0>	Y37	PCIE_RX0N		PCIE_TX0N	Y32	PEG_D2R_C_N<0>
PEG_R2D_P<1>	Y35	PCIE_RX1P		PCIE_TX1P	W33	PEG_D2R_C_P<1>
PEG_R2D_N<1>	W36	PCIE_RX1N		PCIE_TX1N	W32	PEG_D2R_C_N<1>
PEG_R2D_P<2>	W38	PCIE_RX2P		PCIE_TX2P	U33	PEG_D2R_C_P<2>
PEG_R2D_N<2>	V37	PCIE_RX2N		PCIE_TX2N	U32	PEG_D2R_C_N<2>
PEG_R2D_P<3>	V35	PCIE_RX3P		PCIE_TX3P	U30	PEG_D2R_C_P<3>
PEG_R2D_N<3>	U36	PCIE_RX3N		PCIE_TX3N	U29	PEG_D2R_C_N<3>
PEG_R2D_P<4>	U38	PCIE_RX4P		PCIE_TX4P	T33	PEG_D2R_C_P<4>
PEG_R2D_N<4>	T37	PCIE_RX4N		PCIE_TX4N	T32	PEG_D2R_C_N<4>
PEG_R2D_P<5>	T35	PCIE_RX5P		PCIE_TX5P	T30	PEG_D2R_C_P<5>
PEG_R2D_N<5>	R36	PCIE_RX5N		PCIE_TX5N	T29	PEG_D2R_C_N<5>
PEG_R2D_P<6>	R38	PCIE_RX6P		PCIE_TX6P	P33	PEG_D2R_C_P<6>
PEG_R2D_N<6>	P37	PCIE_RX6N		PCIE_TX6N	P32	PEG_D2R_C_N<6>
PEG_R2D_P<7>	P35	PCIE_RX7P		PCIE_TX7P	P30	PEG_D2R_C_P<7>
PEG_R2D_N<7>	N36	PCIE_RX7N		PCIE_TX7N	P29	PEG_D2R_C_N<7>
NC	N38	PCIE_RX8P		PCIE_TX8P	N33	NC
NC	M37	PCIE_RX8N		PCIE_TX8N	N32	NC
NC	M35	PCIE_RX9P		PCIE_TX9P	N30	NC
NC	L36	PCIE_RX9N		PCIE_TX9N	N29	NC
NC	L38	PCIE_RX10P		PCIE_TX10P	L33	NC
NC	K37	PCIE_RX10N		PCIE_TX10N	L32	NC
NC	K35	PCIE_RX11P		PCIE_TX11P	L30	NC
NC	J36	PCIE_RX11N		PCIE_TX11N	L29	NC
NC	J38	PCIE_RX12P		PCIE_TX12P	K33	NC
NC	H37	PCIE_RX12N		PCIE_TX12N	K32	NC
NC	H35	PCIE_RX13P		PCIE_TX13P	J33	NC
NC	G36	PCIE_RX13N		PCIE_TX13N	J32	NC
NC	G38	PCIE_RX14P		PCIE_TX14P	K30	NC
NC	F37	PCIE_RX14N		PCIE_TX14N	K29	NC
NC	F35	PCIE_RX15P		PCIE_TX15P	H33	NC
NC	E37	PCIE_RX15N		PCIE_TX15N	H32	NC
PEG_CLK100M_P	AB35	PCIE_REFCLKP		PCIE_CALRP	Y30	PEG_CALRP
PEG_CLK100M_N	AA36	PCIE_REFCLKN		PCIE_CALRN	Y29	PEG_CALRN
GPU_PWRGOOD	AH16	PWRGOOD				
GPU_RESET_R_L	AA30	PERST*				

PM_ALL_GPU_PGOOD — R8003 NOSTUFF 0 5% 1/16W MF-LF 402 — R8004 10K 5% 1/16W MF-LF 402

EG_RESET_L — R8000 0 5% 1/16W MF-LF 402 — GPU_RESET_R_L

R8001 2.0K 1% 1/16W MF-LF 402 — PP1V0_S0GPU_ISNS

R8002 1.27K 1% 1/16W MF-LF 402

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE: Whistler PCI-E

Apple Inc.

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Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

U8000
WHISTLER
40NM-ES
FCBGA
(7 OF 9)

MEM I/O
CORE
LEVEL TRNSL
I/O
PLL
VOLT SENSE
PCIE
ISOLATED CORE I/O

PP1V5_S0GPU_ISNS — TBD mA
C8100 C8101 C8102 C8103 C8104 10UF 20% 10V X5R 603
C8105 C8106 C8107 C8108 C8109 C8110 C8111 C8112 C8113 C8114 1UF 10% 25V X5R 402
C8115 C8116 C8117 C8118 C8119 C8120 C8121 C8122 C8123 C8124 0.1UF 10% 6.3V X5R 201

L8120 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU_ISNS — PP1V8_GPU_VDD_CT — 219mA
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8125 10UF 20% 10V X5R 603
C8126 C8127 C8128 1UF 10% 25V X5R 402
C8129 0.1UF 10% 6.3V X5R 201

L8130 470OHM-1A-150MOHM 0603 CRITICAL
PP1V0_S0GPU_ISNS — PP1V0_GPU_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V
C8130 10UF 20% 10V X5R 603
C8131 1UF 10% 25V X5R 402
C8132 0.1UF 10% 6.3V X5R 201
GND_GPU_PLL

PP3V3_S0GPU — 60 mA
C8133 10UF 20% 10V X5R 603
C8134 C8135 1UF 10% 25V X5R 402
C8136 1UF 10% 25V X5R 402

L8131 470OHM-1A-150MOHM 0603 CRITICAL
PP1V8_S0GPU_ISNS — PP1V8_GPU_MEM_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8137 10UF 20% 10V X5R 603
C8138 1UF 10% 25V X5R 402
C8139 C8140 0.1UF 10% 6.3V X5R 201
C8141 0.1UF 10% 6.3V X5R 201

PP1V8_GPU_VDDR4 — TBD mA — 150mA

L8132 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU_ISNS — PP1V8_GPU_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8142 10UF 20% 10V X5R 603
C8143 1UF 10% 25V X5R 402
C8144 0.1UF 10% 6.3V X5R 201
75mA
PP1V0_GPU_PLL — 120mA
GND_GPU_PLL

XW8100 SM
GPU_VDD_SENSE
GPU_GND_SENSE

L8140 FERR-220-OHM-2A 0603 CRITICAL
PP1V8_S0GPU_ISNS — PP1V8_GPU_PCIE_VDDR — 504mA
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8145 10UF 20% 10V X5R 603
C8146 C8147 C8148 1UF 10% 25V X5R 402
C8149 C8150 0.1UF 10% 6.3V X5R 201

L8155 FERR-120-OHM-3A 0603 CRITICAL
PP1V0_S0GPU_ISNS — PP1V0_GPU_PCIE_VDDC — 1920mA
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V
C8151 10UF 20% 10V X5R 603
C8152 C8153 C8154 C8155 C8156 C8157 C8158 1UF 10% 25V X5R 402

L8150 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU_ISNS — PP1V8_GPU_VDDR4
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C81C0 1UF 10% 25V X5R 402
C81C1 0.1UF 10% 6.3V X5R 201

PPVCORE_GPU
C8160 C8161 C8162 C8163 C8164 C8165 C8166 C8167 C8168 C8169 1UF 10% 25V X5R 402
C8170 C8171 C8172 C8173 C8174 C8175 C8176 C8177 C8178 C8179 1UF 10% 25V X5R 402
C8180 C8181 C8182 C8183 C8184 C8185 C8186 C8187 C8188 C8189 1UF 10% 25V X5R 402
C8190 C8191 C8192 C8193 C8194 C8195 C8196 C8197 C8198 C8199 10UF 20% 10V X5R 603

C81A0 C81A1 C81A2 C81A3 C81A4 C81A5 C81A6 C81A7 C81A8 C81A9 1UF 10% 25V X5R 402
C81B0 C81B1 C81B2 10UF 20% 10V X5R 603

VDDR1_AC7	AC7	U8000
VDDR1_AD11	AD11	
VDDR1_AF7	AF7	
VDDR1_AG10	AG10	
VDDR1_AJ7	AJ7	
VDDR1_AK8	AK8	
VDDR1_AL9	AL9	
VDDR1_G11	G11	
VDDR1_G14	G14	
VDDR1_G17	G17	
VDDR1_G20	G20	
VDDR1_G23	G23	
VDDR1_G26	G26	
VDDR1_G29	G29	
VDDR1_H10	H10	
VDDR1_J7	J7	
VDDR1_J9	J9	
VDDR1_K8	K8	
VDDR1_K11	K11	
VDDR1_K13	K13	
VDDR1_L7	L7	
VDDR1_L12	L12	
VDDR1_L16	L16	
VDDR1_L21	L21	
VDDR1_L23	L23	
VDDR1_L26	L26	
VDDR1_M11	M11	
VDDR1_N11	N11	
VDDR1_P7	P7	
VDDR1_R11	R11	
VDDR1_U7	U7	
VDDR1_U11	U11	
VDDR1_Y7	Y7	
VDDR1_Y11	Y11	
VDD_CT_AF26	AF26	
VDD_CT_AF27	AF27	
VDD_CT_AG26	AG26	
VDD_CT_AG27	AG27	
VDDR3_AF23	AF23	
VDDR3_AF24	AF24	
VDDR3_AG23	AG23	
VDDR3_AG24	AG24	
VDDR4_AF13	AF13	
VDDR4_AF15	AF15	
VDDR4_AG13	AG13	
VDDR4_AG15	AG15	
VDDR4_AD12	AD12	
VDDR4_AF11	AF11	
VDDR4_AF12	AF12	
VDDR4_AG11	AG11	
NC/VDDRHA	M20	
NC/VSSRHA	M21	
NC/VSSRHB	U12	
NC/VDDRHB	V12	
MPV18_H7	H7	
MPV18_H8	H8	
SPV18	AM10	
SPV10	AN9	
SPVSS	AN10	
FB_VDDC	AF28	
FB_VDDCI	AG28	
FB_GND	AH29	
PCIE_VDDR_AA31	AA31	
PCIE_VDDR_AA32	AA32	
PCIE_VDDR_AA33	AA33	
PCIE_VDDR_AA34	AA34	
PCIE_VDDR_AB37	AB37	
PCIE_VDDR_V28	V28	
PCIE_VDDR_W29	W29	
PCIE_VDDR_W30	W30	
PCIE_VDDR_Y31	Y31	
PCIE_VDDC_G30	G30	
PCIE_VDDC_G31	G31	
PCIE_VDDC_H29	H29	
PCIE_VDDC_H30	H30	
PCIE_VDDC_J29	J29	
PCIE_VDDC_J30	J30	
PCIE_VDDC_L28	L28	
PCIE_VDDC_M28	M28	
PCIE_VDDC_N28	N28	
PCIE_VDDC_R28	R28	
PCIE_VDDC_T28	T28	
PCIE_VDDC_U28	U28	

VDDC_AA15	AA15
VDDC_AA17	AA17
VDDC_AA20	AA20
VDDC_AA22	AA22
VDDC_AA24	AA24
VDDC_AA27	AA27
VDDC_AB16	AB16
VDDC_AB18	AB18
VDDC_AB21	AB21
VDDC_AB23	AB23
VDDC_AB26	AB26
VDDC_AB28	AB28
VDDC_AC17	AC17
VDDC_AC20	AC20
VDDC_AC22	AC22
VDDC_AC24	AC24
VDDC_AC27	AC27
VDDC_AD18	AD18
VDDC_AD21	AD21
VDDC_AD23	AD23
VDDC_AD26	AD26
VDDC_AF17	AF17
VDDC_AF20	AF20
VDDC_AF22	AF22
VDDC_AG16	AG16
VDDC_AG18	AG18
VDDC_AG21	AG21
VDDC_AH22	AH22
VDDC_AH27	AH27
VDDC_AH28	AH28
VDDC_M26	M26
VDDC_N24	N24
BIF_VDDC_N27	N27
VDDC_R18	R18
VDDC_R21	R21
VDDC_R23	R23
VDDC_R26	R26
VDDC_T17	T17
VDDC_T20	T20
VDDC_T22	T22
VDDC_T24	T24
BIF_VDDC_T27	T27
VDDC_U16	U16
VDDC_U18	U18
VDDC_U21	U21
VDDC_U23	U23
VDDC_U26	U26
VDDC_V17	V17
VDDC_V20	V20
VDDC_V22	V22
VDDC_V24	V24
VDDC_V27	V27
VDDC_Y16	Y16
VDDC_Y18	Y18
VDDC_Y21	Y21
VDDC_Y23	Y23
VDDC_Y26	Y26
VDDC_Y28	Y28
VDDCI_AA13	AA13
VDDCI_AB13	AB13
VDDCI_AC12	AC12
VDDCI_AC15	AC15
VDDCI_AD13	AD13
VDDCI_AD16	AD16
VDDCI_M15	M15
VDDCI_M16	M16
VDDCI_M18	M18
VDDCI_M23	M23
VDDCI_N13	N13
VDDCI_N15	N15
VDDCI_N17	N17
VDDCI_N20	N20
VDDCI_N22	N22
VDDCI_R12	R12
VDDCI_R13	R13
VDDCI_R16	R16
VDDCI_T12	T12
VDDCI_T15	T15
VDDCI_V15	V15
VDDCI_Y13	Y13

SYNC_MASTER=K92_SUMA — SYNC_DATE=06/15/2010

PAGE TITLE: Whistler CORE/FB POWER

Apple Inc.

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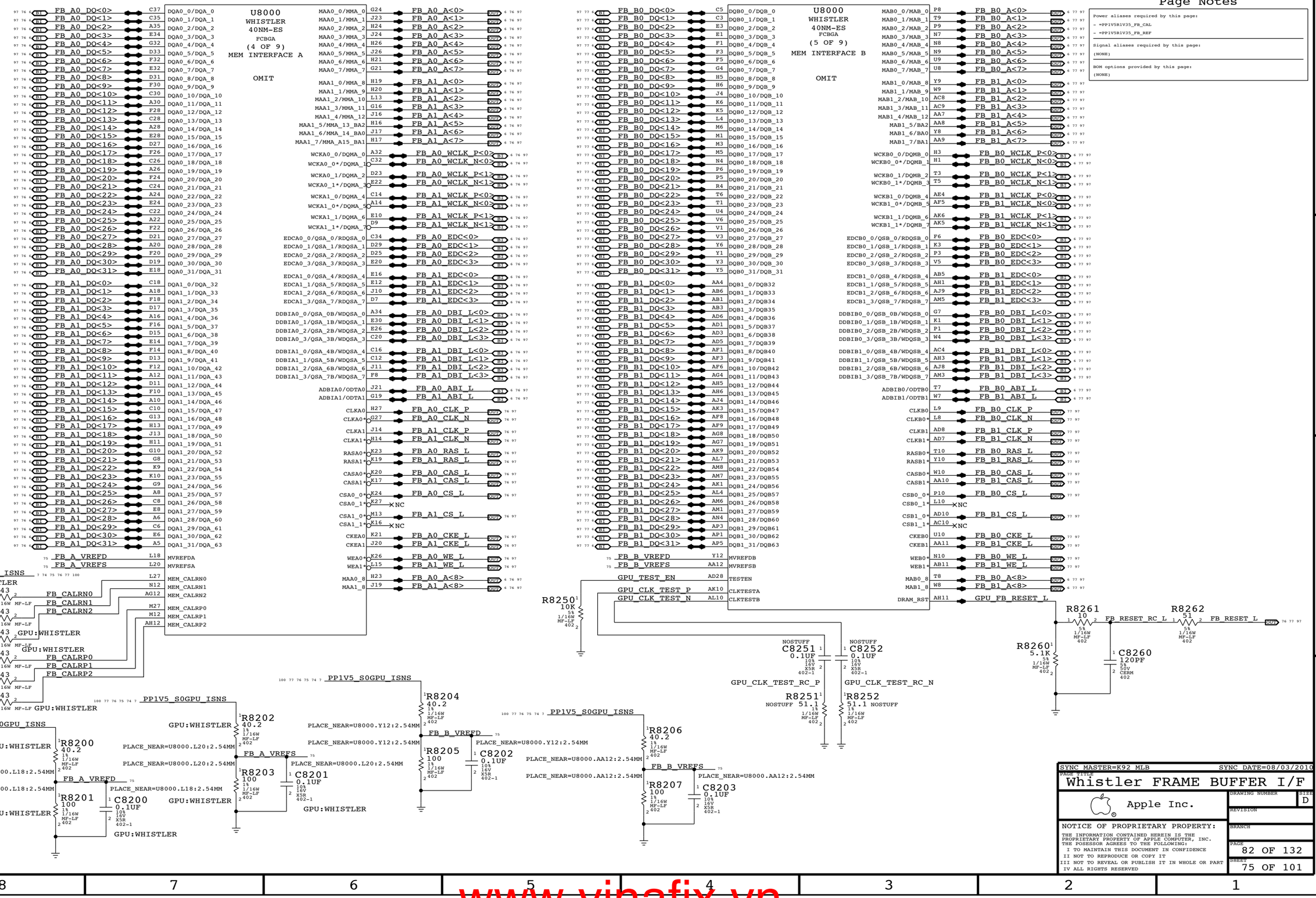

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
GPU:WHISTLER is the BOM option called out on all Rs and Cs on this page

GPU:WHISTLER is the BOM option called out on ALL Rs and Cs on this page!

U8400 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (1 OF 2) OMIT

U8450 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (1 OF 2) OMIT

U8400 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (2 OF 2) OMIT

U8450 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (2 OF 2) OMIT

SYNC MASTER=K92_MLB	SYNC DATE=08/19/2010
PAGE TITLE: GDDR5 Frame Buffer A	
Apple Inc.	DRAWING NUMBER / SIZE: D
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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

U8500 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (1 OF 2) OMIT

U8550 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (1 OF 2) OMIT

U8500 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (2 OF 2) OMIT

U8550 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (2 OF 2) OMIT

SYNC MASTER=K92_MLB	SYNC DATE=08/19/2010
PAGE TITLE: GDDR5 Frame Buffer B	
Apple Inc.	DRAWING NUMBER / SIZE: D
	REVISION
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VRAM BOM OPTION TABLE

	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS

PP1V8_S0GPU_ISNS

R8610 10K 5% 1/16W MF-LF 402 — NOSTUFF
R8611 10K 5% 1/16W MF-LF 402 — VRAM_DVP2
R8612 10K 5% 1/16W MF-LF 402 — VRAM_DVP1
R8613 10K 5% 1/16W MF-LF 402 — VRAM_DVP0

U8000 WHISTLER 40NM-ES FCBGA (2 OF 9)

TP_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0	
TP_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1	
TP_DVPCNTL<0>	AP8	DVPCNTL_0	
TP_DVPCNTL<1>	AW8	DVPCNTL_1	
TP_DVPCNTL<2>	AR3	DVPCNTL_2	
TP_DVPCLK	AR1	DVPCLK	
DVPDATA<0>	AU1	DVPDATA_0	
DVPDATA<1>	AU3	DVPDATA_1	OMIT
DVPDATA<2>	AW3	DVPDATA_2	
DVPDATA<3>	AP6	DVPDATA_3	
TP_DVPDATA<4>	AW5	DVPDATA_4	
TP_DVPDATA<5>	AU5	DVPDATA_5	
TP_DVPDATA<6>	AR6	DVPDATA_6	
TP_DVPDATA<7>	AW6	DVPDATA_7	
TP_DVPDATA<8>	AU6	DVPDATA_8	
TP_DVPDATA<9>	AT7	DVPDATA_9	
TP_DVPDATA<10>	AV7	DVPDATA_10	
TP_DVPDATA<11>	AN7	DVPDATA_11	
TP_DVPDATA<12>	AV9	DVPDATA_12	
TP_DVPDATA<13>	AT9	DVPDATA_13	
TP_DVPDATA<14>	AR10	DVPDATA_14	
TP_DVPDATA<15>	AW10	DVPDATA_15	
TP_DVPDATA<16>	AU10	DVPDATA_16	
TP_DVPDATA<17>	AP10	DVPDATA_17	
TP_DVPDATA<18>	AV11	DVPDATA_18	
TP_DVPDATA<19>	AT11	DVPDATA_19	
TP_DVPDATA<20>	AR12	DVPDATA_20	
TP_DVPDATA<21>	AW12	DVPDATA_21	
TP_DVPDATA<22>	AU12	DVPDATA_22	
TP_DVPDATA<23>	AP12	DVPDATA_23	
NC	AJ21	SWAPLOCKA	
NC	AK21	SWAPLOCKB	
GPU_I2C_SCL	AK26	SCL	
GPU_I2C_SDA	AJ26	SDA	
GPU_PCIE_TX_PWR	AH20	GPIO_0	
GPU_GPIO_TX_DEEMP	AH18	GPIO_1	
GPU_PCIE_GEN2	AN16	GPIO_2	
GPU_SMB_DAT	AH23	GPIO_3_SMBDATA	
GPU_SMB_CLK	AJ23	GPIO_4_SMBCLK	
GPU_AC_BATT	AH17	GPIO_5_AC_BATT	
GPU_VCORE_VID0	AJ17	GPIO_6	
EG_BKLT_EN	AK17	GPIO_7_BLON	
GPU_ROM_SO	AJ13	GPIO_8_ROMSO	
GPU_ROM_SI	AH15	GPIO_9_ROMSI	
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK	
GPU_CONFIG_0	AK16	GPIO_11	
GPU_CONFIG_1	AL16	GPIO_12	
GPU_CONFIG_2	AM16	GPIO_13	
DP_T29SNK0_HPD_GPU	AM14	GPIO_14_HPD2	
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0	
GPU_VCORE_VID2	AK14	GPIO_16	
SMC_GFX_THROTTLE_R_L	AG30	GPIO_17_THERMAL_INT	
DP_T29SNK1_HPD_GPU	AN14	GPIO_18_HPD3	
SMC_GFX_OVERTEMP_R_L	AM17	GPIO_19_CTF	
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1	
FBVDD_ALTVO	AJ14	GPIO_21_BB_EN	
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*	
PEX_CLKREQ_L_R	AN13	GPIO_23_CLKREQ*	
TP_GPU_JTAG_TRST_L	AM23	JTAG_TRST*	
TP_GPU_JTAG_TDI	AN23	JTAG_TDI	
TP_GPU_JTAG_TCK	AK23	JTAG_TCK	
TP_GPU_JTAG_TMS	AL24	JTAG_TMS	
TP_GPU_JTAG_TDO	AM24	JTAG_TDO	
NC_GPU_GENERICA	AJ19	GENERICA	
NC_GPU_GENERICB	AK19	GENERICB	
NC_GPU_GENERICC	AJ20	GENERICC	
DP_CA_DET_EG_R	AK20	GENERICD	
NC_GPU_GENERICE	AJ24	GENERICE_HPD4	
NC_GPU_GENERICF	AH26	GENERICF_HPD5	
NC_GPU_GENERICG	AH24	GENERICG_HPD6	
DP_EG_HPD	AK24	HPD1	
GPU_VREFG	AH13	VREFG	
PP1V8_GPU_DPLL 75mA (GND_GPU_DPLL)	AM32 / AN32	DPLL_PVDD / DPLL_PVSS	
PP1V0_GPU_DPLL 125mA	AN31	DPLL_VDDC	
NC	AV33	XTALIN	
NC	AU34	XTALOUT	
GPU_CLK27M	AW34	XO_IN	
GPU_CLK100M	AW35	XO_IN2	
GPU_TDIODE_P	AF29	DPLUS	
GPU_TDIODE_N	AG29	DMINUS	
NC	AK32	TS_FDO	
NC	AL31	TSA/NC	
PP1V8_GPU_TSVDD 20mA (GND_GPU_TSVSS)	AJ32 / AJ33	TSVDD / TSVSS	

PP3V3_S0GPU

R8600 4.7K 5% 1/16W MF-LF 402
R8601 4.7K 5% 1/16W MF-LF 402

PP1V8_S0GPU_ISNS

R8602 499 1% 1/16W MF-LF 402
C8600 0.1UF 10% 16V X5R 402-1
R8603 249 1% 1/16W MF-LF 402

CRITICAL L8600 470OHM-1A-150MOHM 0603 — PP1V8_S0GPU_ISNS, VOLTAGE=1.8V
C8601 10UF 20% 10V X5R 603
C8602 1UF 10% 25V X5R 402
C8603 0.1UF 10% 16V X5R 402-1
MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V

CRITICAL L8601 470OHM-1A-150MOHM 0603 — PP1V0_S0GPU_ISNS, VOLTAGE=1V
C8604 10UF 20% 10V X5R 603
C8605 1UF 10% 25V X5R 402
C8606 0.1UF 10% 16V X5R 402-1
MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

XW8600 SM — GND_GPU_DPLL

CRITICAL L8602 120OHM-0.3A 0402 — PP1V8_S0GPU_ISNS, VOLTAGE=1.8V
C8607 10UF 20% 10V X5R 603
C8608 1UF 10% 25V X5R 402
C8609 0.1UF 10% 16V X5R 402-1
MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

XW8601 SM — GND_GPU_TSVSS

TXCAP_DPA3P	AU24	DP_EXTA_ML_C_P<3>	OUT
TXCAM_DPA3N	AV23	DP_EXTA_ML_C_N<3>	OUT
TX0P_DPA2P	AT25	DP_EXTA_ML_C_P<2>	OUT
TX0M_DPA2N	AR24	DP_EXTA_ML_C_N<2>	OUT
TX1P_DPA1P	AU26	DP_EXTA_ML_C_P<1>	OUT
TX1M_DPA1N	AV25	DP_EXTA_ML_C_N<1>	OUT
TX2P_DPA0P	AT27	DP_EXTA_ML_C_P<0>	OUT
TX2M_DPA0N	AR26	DP_EXTA_ML_C_N<0>	OUT
TXCBP_DPB3P	AR30	DP_T29SNK0_ML_C_P<3>	OUT
TXCBM_DPB3N	AT29	DP_T29SNK0_ML_C_N<3>	OUT
TX3P_DPB2P	AV31	DP_T29SNK0_ML_C_P<2>	OUT
TX3M_DPB2N	AU30	DP_T29SNK0_ML_C_N<2>	OUT
TX4P_DPB1P	AR32	DP_T29SNK0_ML_C_P<1>	OUT
TX4M_DPB1N	AT31	DP_T29SNK0_ML_C_N<1>	OUT
TX5P_DPB0P	AT33	DP_T29SNK0_ML_C_P<0>	OUT
TX5M_DPB0N	AU32	DP_T29SNK0_ML_C_N<0>	OUT
TXCCP_DPC3P	AU14	DP_T29SNK1_ML_C_P<3>	OUT
TXCCM_DPC3N	AV13	DP_T29SNK1_ML_C_N<3>	OUT
TX0P_DPC2P	AT15	DP_T29SNK1_ML_C_P<2>	OUT
TX0M_DPC2N	AR14	DP_T29SNK1_ML_C_N<2>	OUT
TX1P_DPC1P	AU16	DP_T29SNK1_ML_C_P<1>	OUT
TX1M_DPC1N	AV15	DP_T29SNK1_ML_C_N<1>	OUT
TX2P_DPC0P	AT17	DP_T29SNK1_ML_C_P<0>	OUT
TX2M_DPC0N	AR16	DP_T29SNK1_ML_C_N<0>	OUT
TXCDP_DPD3P	AU20	NC	
TXCDM_DPD3N	AT19	NC	
TX3P_DPD2P	AT21	NC	
TX3M_DPD2N	AR20	NC	
TX4P_DPD1P	AU22	NC	
TX4M_DPD1N	AV21	NC	
TX5P_DPD0P	AT23	NC	
TX5M_DPD0N	AR22	NC	
R	AD39	NC	
R*	AD37	NC	
G	AE36	NC	
G*	AD35	NC	
B	AF37	NC	
B*	AE38	NC	
HSYNC	AC36	GPU_AUD_1	
VSYNC	AC38	GPU_AUD_0	
RSET	AB34	NC	
AVDD	AD34	PP1V8_S0GPU_ISNS	
AVSSQ	AE34		
VDD1DI	AC33		
VSS1DI	AC34		
R2/NC	AC30	NC	
R2*/NC	AC31	NC	
G2/NC	AD30	NC	
G2*/NC	AD31	NC	
B2/NC	AF30	NC	
B2*/NC	AF31	NC	
C/NC	AC32	NC	
Y/NC	AD32	NC	
COMP/NC	AF32	NC	
H2SYNC/GENLK_CLK	AD29	NC	
V2SYNC/GENLK_VSYNC	AC29	NC	
VDD2DI/NC	AG31	NC	
VSS2DI/NC	AG32	NC	
A2VDD/NC	AG33	NC	
A2VDDQ/NC	AD33	NC	
A2VSSQ/TSVSSQ	AF33	GND_GPU_TVSSQ	
R2SET/NC	AA29	NC	
DDC1CLK	AM26	DP_EG_DDC_CLK	OUT
DDC1DATA	AN26	DP_EG_DDC_DATA	BI
AUX1P	AM27	DP_EG_AUXCH_P	BI
AUX1N	AL27	DP_EG_AUXCH_N	BI
DDC2CLK	AM19	NC	
DDC2DATA	AL19	NC	
AUX2P	AN20	DP_T29SNK0_AUXCH_C_P	BI
AUX2N	AM20	DP_T29SNK0_AUXCH_C_N	BI
DDCCLK_AUX3P	AL30	DP_T29SNK1_AUXCH_C_P	BI
DDCDATA_AUX3N	AM30	DP_T29SNK1_AUXCH_C_N	BI
DDCCLK_AUX4P	AL29	NC	
DDCDATA_AUX4N	AM29	NC	
DDCCLK_AUX5P	AN21	LVDS_EG_DDC_CLK	OUT
DDCDATA_AUX5N	AM21	LVDS_EG_DDC_DATA	BI
DDC6CLK	AJ30	NC	
DDC6DATA	AJ31	NC	
DDCCLK_AUX7P	AK30	NC	
DDCDATA_AUX7N	AK29	NC	

XW8602 SM — GND_GPU_TVSSQ, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

PP3V3_S0GPU — Straps for audio on DP and HDMI

R8604 10K 5% 1/16W MF-LF 402
R8605 10K 5% 1/16W MF-LF 402

U8000 WHISTLER 40NM-ES FCBGA (3 OF 9) LVTMDP

VARY_BL	AK27	LVDS_EG_BLK_PWM	
DIGON	AJ27	EG_LCD_PWR_EN	OUT
LVDS CNTL			
TXCLK_UP_DPF3P	AK35	NC_LVDS_EG_B_CLK_P	
TXCLK_UN_DPF3N	AL36	NC_LVDS_EG_B_CLK_N	
TXOUT_U0P_DPF2P	AJ38	LVDS_EG_B_DATA_P<0>	OUT
TXOUT_U0N_DPF2N	AK37	LVDS_EG_B_DATA_N<0>	OUT
TXOUT_U1P_DPF1P	AH35	LVDS_EG_B_DATA_P<1>	OUT
TXOUT_U1N_DPF1N	AJ36	LVDS_EG_B_DATA_N<1>	OUT
TXOUT_U2P_DPF0P	AG38	LVDS_EG_B_DATA_P<2>	OUT
TXOUT_U2N_DPF0N	AH37	LVDS_EG_B_DATA_N<2>	OUT
TXOUT_U3P	AF35	NC_LVDS_EG_B_DATA_P<3>	
TXOUT_U3N	AG36	NC_LVDS_EG_B_DATA_N<3>	
TXCLK_LP_DPE3P	AP34	LVDS_EG_A_CLK_P	OUT
TXCLK_LN_DPE3N	AR34	LVDS_EG_A_CLK_N	OUT
TXOUT_L0P_DPE2P	AW37	LVDS_EG_A_DATA_P<0>	OUT
TXOUT_L0N_DPE2N	AU35	LVDS_EG_A_DATA_N<0>	OUT
TXOUT_L1P_DPE1P	AR37	LVDS_EG_A_DATA_P<1>	OUT
TXOUT_L1N_DPE1N	AU39	LVDS_EG_A_DATA_N<1>	OUT
TXOUT_L2P_DPE0P	AP35	LVDS_EG_A_DATA_P<2>	OUT
TXOUT_L2N_DPE0N	AR35	LVDS_EG_A_DATA_N<2>	OUT
TXOUT_L3P	AN36	NC_LVDS_EG_A_DATA_P<3>	
TXOUT_L3N	AP37	NC_LVDS_EG_A_DATA_N<3>	

R8606 10K 5% 1/16W MF-LF 402

OMIT

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_MLB	SYNC_DATE=12/01/2010
PAGE TITLE	Whistler LVDS/DP/GPIO
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GPIOs

GPU_PCIE_TX_PWR	GP	GPU_PCIE_TX_PWR
GPU_GPIO_TX_DEEMP	GP	GPU_GPIO_TX_DEEMP
GPU_PCIE_GEN2	GP	GPU_PCIE_GEN2
GPU_SMB_DAT	GP	GPU_SMB_DAT
GPU_SMB_CLK	GP	GPU_SMB_CLK
GPU_AC_BATT	GP	GPU_AC_BATT
GPU_VCORE_VID0	GP	GPU_VCORE_VID0
EG_BKLT_EN	GP	EG_BKLT_EN
GPU_ROM_SO	GP	GPU_ROM_SO
GPU_ROM_SI	GP	GPU_ROM_SI
GPU_ROM_SCLK	GP	GPU_ROM_SCLK
GPU_CONFIG_0	GP	GPU_CONFIG_0
GPU_CONFIG_1	GP	GPU_CONFIG_1
GPU_CONFIG_2	GP	GPU_CONFIG_2
DP_T29SNK0_HPD_GPU	GP	DP_T29SNK0_HPD_GPU
GPU_VCORE_VID1	GP	GPU_VCORE_VID1

All: MAKE_BASE=TRUE

GPIOs

GPU_VCORE_VID2	GP	GPU_VCORE_VID2
SMC_GFX_THROTTLE_R_L	GP	SMC_GFX_THROTTLE_R_L
DP_T29SNK1_HPD_GPU	GP	DP_T29SNK1_HPD_GPU
SMC_GFX_OVERTEMP_R_L	GP	SMC_GFX_OVERTEMP_R_L
GPU_VCORE_VID3	GP	GPU_VCORE_VID3
FBVDD_ALTVO	GP	FBVDD_ALTVO
GPU_ROM_CS_L	GP	GPU_ROM_CS_L
PEX_CLKREQ_L_R	GP	PEX_CLKREQ_L_R
NC_GPU_GENERICA	GP	NC_GPU_GENERICA
NC_GPU_GENERICB	GP	NC_GPU_GENERICB
NC_GPU_GENERICC	GP	NC_GPU_GENERICC
DP_CA_DET_EG_R	GP	DP_CA_DET_EG_R
NC_GPU_GENERICE	GP	NC_GPU_GENERICE
NC_GPU_GENERICF	GP	NC_GPU_GENERICF
NC_GPU_GENERICG	GP	NC_GPU_GENERICG
DP_EG_HPD	GP	DP_EG_HPD

All: MAKE_BASE=TRUE; NO_TEST=TRUE

T29 HPD GPU isolation

DP_T29SNK0_HPD → U8741 (74LVC2G08GT SOT833, CRITICAL) → DP_T29SNK0_HPD_GPU
PP3V3_S0 → C8741 0.1UF 20% 10V CERM 402 → U8741 pin 8
PP3V3_GPU_VDD33_R → R8741 0 5% 1/16W MF-LF 402 → PP3V3_S0GPU
DP_T29SNK1_HPD → U8741 → DP_T29SNK1_HPD_GPU

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L
NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE; NO_TEST=TRUE	NC_LVDS_EG_B_CLK_P
NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE; NO_TEST=TRUE	NC_LVDS_EG_B_CLK_N
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE; NO_TEST=TRUE	NC_LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE; NO_TEST=TRUE	NC_LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE; NO_TEST=TRUE	NC_LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE; NO_TEST=TRUE	NC_LVDS_EG_B_DATA_N<3>

ISOLATION R's for GPU Int Temp Sense

GPU_SMB_DAT → R8780 (NOSTUFF) 0 5% 1/16W MF-LF 402 → SMBUS_SMC_0_S0_SDA
GPU_SMB_CLK → R8781 (NOSTUFF) 0 5% 1/16W MF-LF 402 → SMBUS_SMC_0_S0_SCL

Config Straps

PP3V3_S0GPU → R8700 10K, R8701 10K, R8702 10K (NOSTUFF) → GPU_PCIE_TX_PWR, GPU_GPIO_TX_DEEMP, GPU_PCIE_GEN2
R8703 10K, R8704 10K, R8705 10K (NOSTUFF) → GPU_SMB_DAT, GPU_SMB_CLK, GPU_AC_BATT
R8706 10K, R8707 10K, R8708 10K (NOSTUFF) → EG_BKLT_EN, GPU_ROM_SO, GPU_ROM_SI
R8709 10K, R8710 10K, R8711 10K (NOSTUFF) → GPU_ROM_SCLK, GPU_CONFIG_0, GPU_CONFIG_1
R8712 10K (GPU_ROM:YES), R8713 10K, R8714 10K (NOSTUFF) → GPU_CONFIG_2, FBVDD_ALTVO, PEX_CLKREQ_L_R

GPU_ROM

PP3V3_S0GPU → C8721 0.1UF 20% 10V CERM 402 (GPU_ROM:YES)
R8723 33 (GPU_ROM:YES) ← GPU_ROM_SI
R8724 33 (GPU_ROM:YES) ← GPU_ROM_SCLK
R8725 33 (GPU_ROM:YES) ← GPU_ROM_CS_L
R8720 10K, R8721 0 (GPU_ROM:YES) → GPU_ROM_SI_R
R8722 (NO STUFF) 0 → GPU_ROM_WP_L
U8701 M25P10A UFDFPN8 CRITICAL OMIT_TABLE
GPU_ROM_SI_R, GPU_ROM_SCLK_R, GPU_ROM_CS_L_R, GPU_ROM_WP_L
U8701 pin 2 → GPU_ROM_SO_R → R8726 33 → GPU_ROM_SO (GPU_ROM:YES)

DP_EG_DDC / DP_IG_DDC

PP3V3_S0 / PP3V3_S0GPU
R8750 (NO STUFF) 2.2K, R8751 2.2K, R8752 4.7K, R8753 4.7K
DP_EG_DDC_CLK (IN), DP_EG_DDC_DATA (BI), DP_IG_DDC_CLK (IN), DP_IG_DDC_DATA (BI)

GPU_OSC

PP3V3_S0GPU → L8703 120OHM-0.3A → PP3V3_GPU_OSC_27M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)
L8702 120OHM-0.3A → PP3V3_GPU_OSC_100M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)
C8702 0.1UF, C8703 0.1UF

GPU Reference Clocks

U8700 SL16010DC TDFN (CRITICAL)
GPU_OSC_27M_XTALIN, GPU_OSC_27M_XTALOUT
Y8700 CRITICAL SM-2.5X2.0MM 27MHZ-15PPM-18PF
C8700 30PF, C8701 30PF
SSELO, SSEL1
SCLK → R8730 0 → GPU_CLK100M_R → GPU_CLK100M (OUT)
REFCLK → R8731 0 → GPU_CLK27M_R → GPU_CLK27M (OUT)

R8796 / R8797 / R8792 / R8793 / R8794

PP3V3_S0GPU → R8796 (NO STUFF) 2.2K, R8797 2.2K
SMC_GFX_OVERTEMP_R_L → R8798 0 → SMC_GFX_OVERTEMP_L (OUT)
SMC_GFX_THROTTLE_R_L → R8799 0 → SMC_GFX_THROTTLE_L (IN)
EG_LCD_PWR_EN (OUT)
EG_BKLT_EN (OUT)
FBVDD_ALTVO (OUT)
R8792 10K, R8793 10K, R8794 10K

R8791 / R8795

DP_CA_DET_EG_R → R8791 0 → DP_CA_DET_EG (IN)
PEX_CLKREQ_L_R → R8795 0 → PEX_CLKREQ_L (OUT)

SYNC_MASTER=K92_MLB SYNC_DATE=11/23/2010

PAGE TITLE: Whistler GPIOs & STRAPs

Apple Inc.

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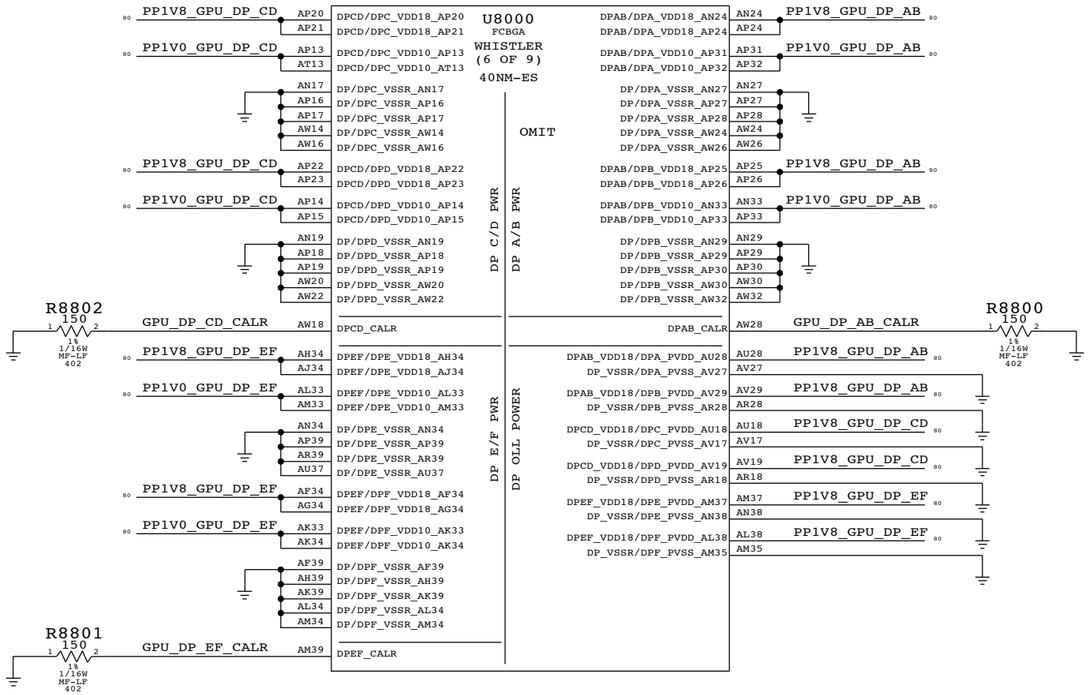

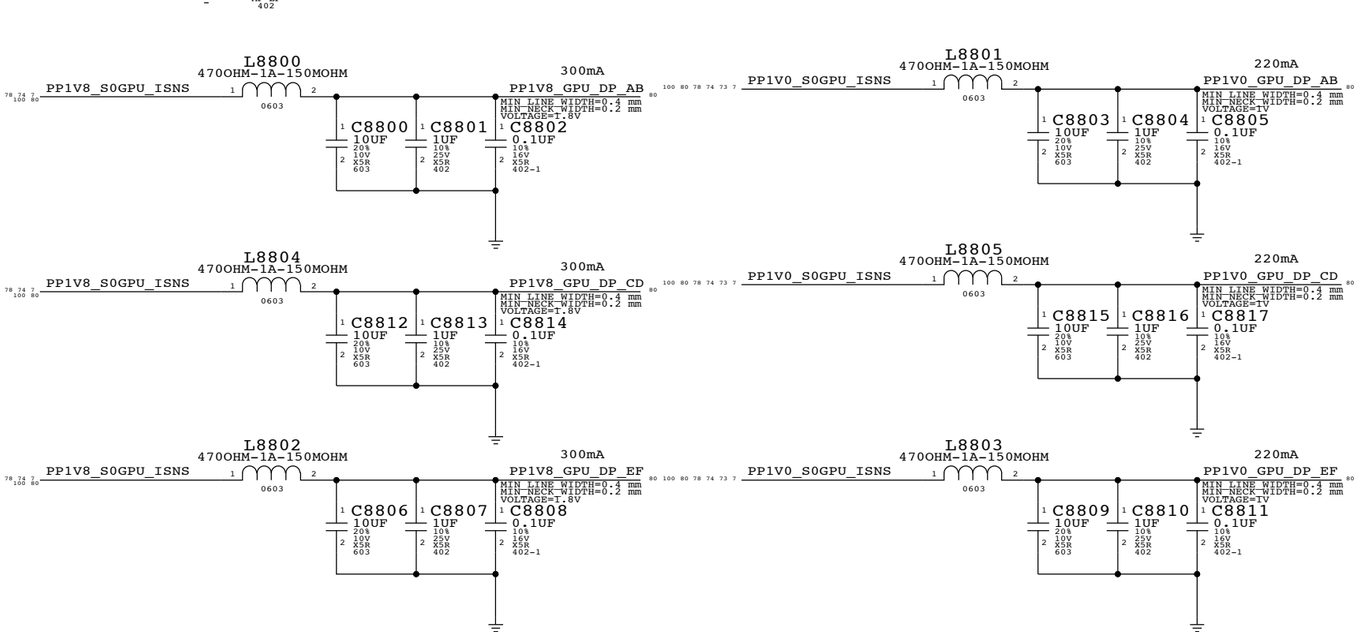

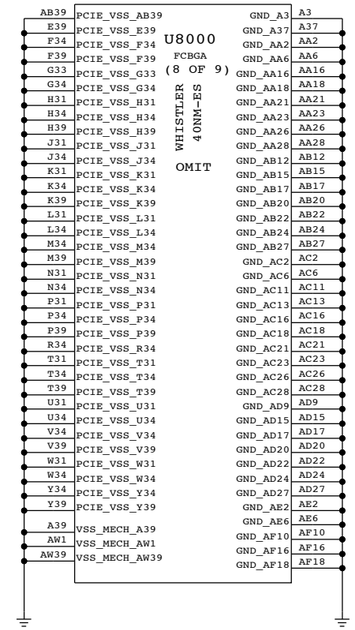

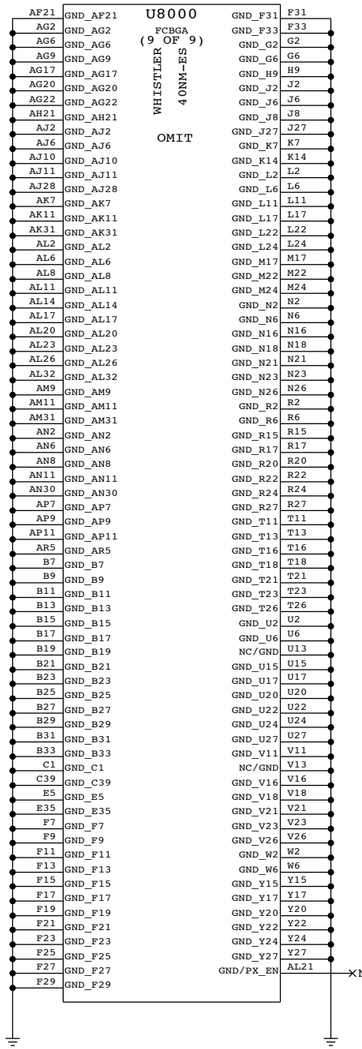

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE
Whistler DP PWR/GNDs

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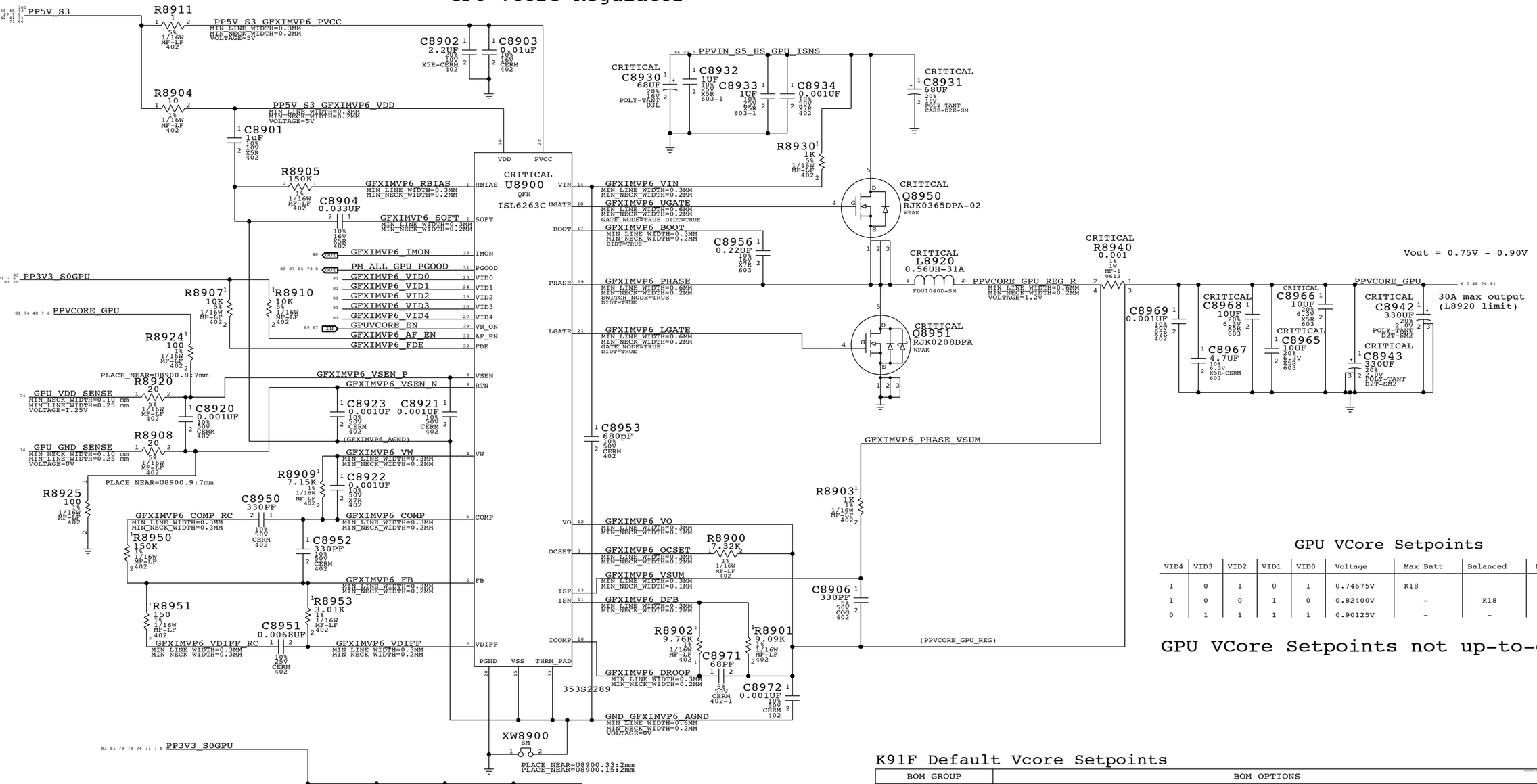
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K91F Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

VIMON = 31 x Io x Rsns x (1 + Ris2/Ris1)
In K9x, the equation will be:
VIMON = 31 x Io x R8940 x (1+ R8902/R8901)
VIMON = 31x Io x 1mOhm x 2.074 = Io x 64.29 mV/A

SYNC_MASTER=K91_ERIC SYNC_DATE=12/21/2010
PAGE TITLE: GPU (Whistler) CORE SUPPLY
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LCD (LVDS) INTERFACE

LCD_PWR_EN

R9094 10K 5% 1/16W MF-LF 402

CRITICAL U9000 FPF1009 MFET-2X2

PP3V3_S5

C9009 0.1UF 10% 16V X5R 402-1

C9011 0.1UF 10% 16V X5R 402-1

C9012 10UF 20% 6.3V X5R 603

CRITICAL L9000 FERR-250-OHM SM

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

C9001 0.1UF 10% 16V X5R 402-1

C9002 0.001UF 10% 50V X7R 402

CRITICAL J9000 20474-040E-11 F-RT-SM

PP3V3_S0

100K pull-ups are for no-panel case (development).
Panel has 2K pull-ups

R9010 100K 5% 1/16W MF-LF 402

R9011 100K 5% 1/16W MF-LF 402

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

LVDS_DDC_CLK
LVDS_DDC_DATA

C9010 0.001UF 10% 50V X7R 402

CRITICAL L9010 90-OHM-100MA DLP11S

LVDS_CONN_A_CLK_N
LVDS_CONN_A_CLK_P

Place close to the connector

CRITICAL L9011 90-OHM-100MA DLP11S

LVDS_CONN_B_CLK_N
LVDS_CONN_B_CLK_P

Place close to the connector

NC

LVDS_CONN_A_DATA_N<0>
LVDS_CONN_A_DATA_P<0>
LVDS_CONN_A_DATA_N<1>
LVDS_CONN_A_DATA_P<1>
LVDS_CONN_A_DATA_N<2>
LVDS_CONN_A_DATA_P<2>
LVDS_CONN_A_CLK_F_N
LVDS_CONN_A_CLK_F_P
LVDS_CONN_B_DATA_N<0>
LVDS_CONN_B_DATA_P<0>
LVDS_CONN_B_DATA_N<1>
LVDS_CONN_B_DATA_P<1>
LVDS_CONN_B_DATA_N<2>
LVDS_CONN_B_DATA_P<2>
LVDS_CONN_B_CLK_F_N
LVDS_CONN_B_CLK_F_P
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1
NC
PPVOUT_S0_LCDBKLT

C9000 0.001UF 10% 50V CERM 402

518S0651

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: LVDS Display Connector

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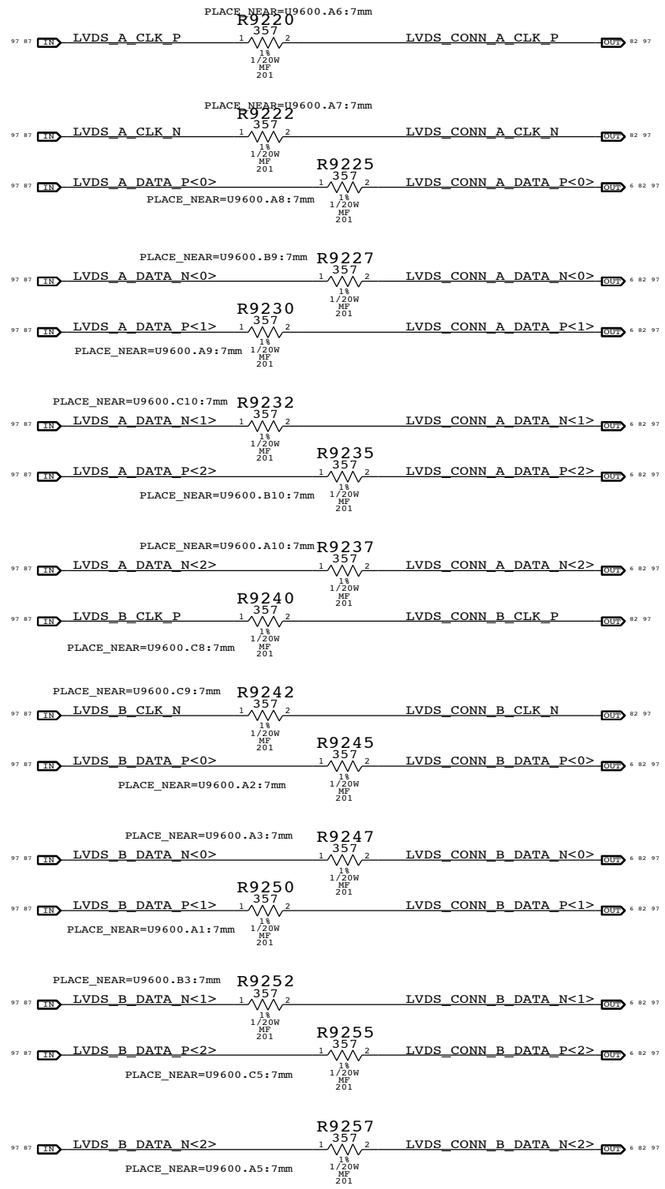
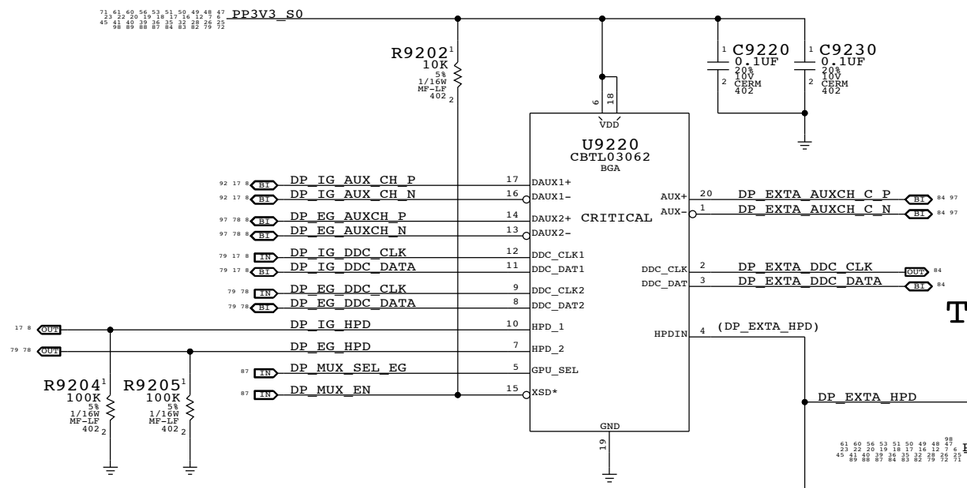
LVDS Transmitter Termination

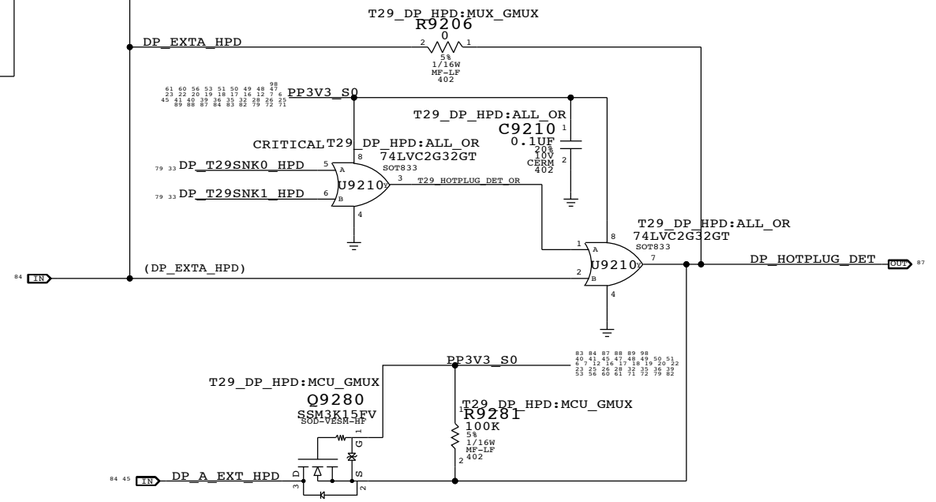
All emulated LVDS outputs require this termination



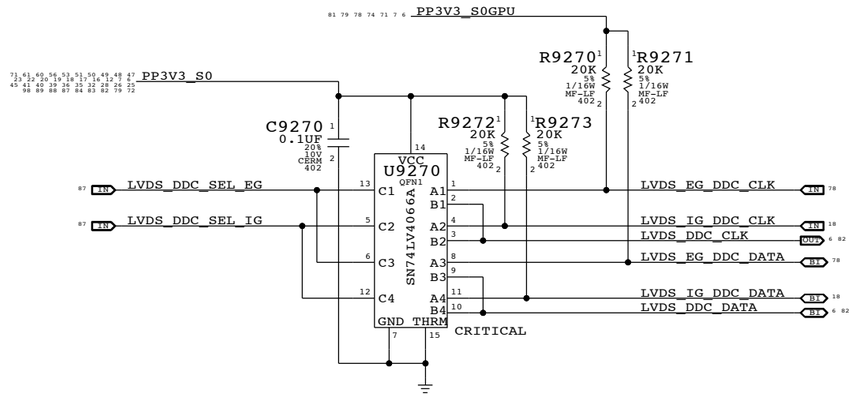
DP AUX, DDC, & HPD muxing to IG/EG



T29/DP HOT PLUG IN



LVDS DDC MUX



SYNC_MASTER=K92_MLB SYNC_DATE=11/21/2010

PAGE TITLE

Muxed Graphics Support

Apple Inc.

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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1uF 10% 16V X5R 402 → DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF → DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF → DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF → DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF → DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF → DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF → DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF → DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF → DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF → DP_EXTA_AUXCH_N

PP3V3_S0 → R9309 1M 5% MF-LF 1/16W 402 → DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_N → R9308 1M 5% MF-LF 1/16W 402 → GND

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29_D2R_N<0> → L9372 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_N<0> → C9372 0.47UF 10% 6.3V CERM-X5R 402 → T29_R2D_C_N<0>
T29_D2R_P<0> → L9373 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_P<0> → C9373 0.47UF → T29_R2D_C_P<0>

OVERSIZE_PAD=0.875 mm^2 (Both L's)
Inductor values TBD

T29 signals are P/N-swapped after AC caps to improve layout.

T29_A_BIAS_R2D_P0 → C9370 0.47UF 20% 4V CERM-X5R-1 201 → GND_VOID=TRUE (C9370/C9371) → C9371 0.47UF → T29_A_BIAS_R2D_N0
T29_A_BIAS_R2D_P1 → C9380 0.47UF → GND_VOID=TRUE (C9380/C9381) → C9381 0.47UF → T29_A_BIAS_R2D_N1

T29 Path Biasing

T29_R2D_P<0> → R9372 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE → T29_D2R_C_P<0>
T29_R2D_N<0> → R9373 1.5K → GND_VOID=TRUE → T29_D2R_C_N<0>
T29_R2D_P<1> → R9382 1.5K → GND_VOID=TRUE → T29_D2R_C_P<1>
T29_R2D_N<1> → R9383 1.5K → GND_VOID=TRUE → T29_D2R_C_N<1>

D9364 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9364.2)
D9372 BAR90-02LRH TSLP-2-7 → T29: TX_0 → T29DPA_ML_C_P<0> / T29DPA_ML_C_N<0>
D9373 BAR90-02LRH TSLP-2-7
D9365 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9372/D9373) → GND_VOID=TRUE (D9365.2)
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
R9374 1.5K → GND_VOID=TRUE
R9375 1.5K → GND_VOID=TRUE

D9360 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9360.2)
D9382 BAR90-02LRH TSLP-2-7 → T29: TX_1 → T29DPA_ML_C_P<2> / T29DPA_ML_C_N<2>
D9383 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9382/D9383)
D9361 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9361.2)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
R9384 1.5K → GND_VOID=TRUE
R9385 1.5K → GND_VOID=TRUE

DP A Super-Driver

PP3V3_S0 → C9310 2.2UF 20% 6.3V CERM 402-LF; C9311 0.1UF 20% 10V CERM 402; C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K; R9310 1K; R9312 1K

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	IN_D0P	OUT_D0P	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	IN_D0N	OUT_D0N	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	IN_D1P	OUT_D1P	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	IN_D1N	OUT_D1N	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	IN_D2P	OUT_D2P	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	IN_D2N	OUT_D2N	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	IN_D3P	OUT_D3P	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	IN_D3N	OUT_D3N	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	IN_SCL	AC_AUXP	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	IN_SDA	AC_AUXN	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	IN_HPD	(IPD) OUT_HPD	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	I2C_CTL_EN (IPU)	CA_DET	DP_A_CA_DET
DPSDRVA_I2C_ADDR0	I2C_ADDR0 (IPD)	CEXT	DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	I2C_ADDR1 (IPD)		
I2C_DPSDRVA_SCL	SCL_CTL		
I2C_DPSDRVA_SDA	SDA_CTL		
DPSDRVA_REXT	REXT		
DP_AUXCH_ISOL	AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	PD (IPD)		

DPSDRVA_CEXT → PLACE_NEAR=U9310.11:2 mm → C9319 2.2UF 20% 6.3V CERM 402-LF

SDRV_PD R9318 0 → R9319 4.99K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9354 30 5% 1/20W MF 201 → DP_SDRVA_ML_R_P<0>
R9353 270 5% 1/20W MF 201 → DP_SDRVA_ML_R_N<0>
R9355 30 → DP_SDRVA_ML_R_P<2>
R9350 30 → DP_SDRVA_ML_R_N<2>
R9351 30
R9352 270

C9364 0.22UF 20% 6.3V X5R 0201 → DP_SDRVA_ML_P<0>
C9365 0.22UF → DP_SDRVA_ML_N<0>
C9360 0.22UF → DP_SDRVA_ML_P<2>
C9361 0.22UF → DP_SDRVA_ML_N<2>

C9363 0.1uF → DP_SDRVA_ML_C_P<1>
C9362 0.1uF → DP_SDRVA_ML_C_N<1>
C9367 0.1uF → DP_SDRVA_ML_C_P<3>
C9366 0.1uF → DP_SDRVA_ML_C_N<3>

AUXCH Snoop Port, used by PS8301 during training.

C9369 0.1uF → DP_SDRVA_AUXCH_C_P
C9368 0.1uF → DP_SDRVA_AUXCH_C_N

DP_SDRVA_ML_N<3> / DP_SDRVA_ML_P<3> / DP_SDRVA_ML_N<1> / DP_SDRVA_ML_P<1> / DP_SDRVA_AUXCH_P / DP_SDRVA_AUXCH_N / DP_SDRVA_HPD → U9390 CBTL04DP081 HVQFN

CKPLUS_WAIVE=NdifPr_badTerm
T29_A_RSVD_N
T29_A_RSVD_P
(T29_A_LSX_P2R)
(T29_A_LSX_R2P)
T29_D2R1_BIASP
T29_D2R1_BIASN

DP Path Biasing

R9361 1.5K → DP_A_BIAS0 VOLTAGE=3.3V
R9360 1.5K
R9365 1.5K → DP_A_BIAS2 VOLTAGE=3.3V
R9364 1.5K
PLACE_NEAR=C9361.1:2mm

PP3V3_S0 → C9359 0.1UF → DP_A_PWRDWN
CRITICAL U9359 74LVC1G04DBCKR SC70 → DP_A_BIAS

IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

C9390 0.1UF; C9391 0.1UF

R9399 100K

DP_SDRVA_ML_N<3>	DIN1_0+	DOUT_0+	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	DIN1_0-	DOUT_0-	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	DIN1_1+		T29: Unused
DP_SDRVA_ML_P<1>	DIN1_1-	DOUT_1+	T29DPA_ML_N<1>
DP_SDRVA_AUXCH_P	AUX1+	DOUT_1-	T29DPA_ML_P<1>
DP_SDRVA_AUXCH_N	AUX1-		T29: LSX_A_R2P/P2R (P/N)
DP_SDRVA_HPD	HPD_1	AUX+	DP_A_EXT_AUXCH_P
		AUX-	DP_A_EXT_AUXCH_N
			T29: RX_1 Bias Sink
		HPD_IN	DP_A_EXT_HPD

CRITICAL

R9392 51 → R9393 51

R9396 1K; R9397 1K

DP_A_PWRDWN → GPU_SEL
T29_A_BIAS → AUX_SEL
NC
LO=Port A
HI=Port B

OMIT_TABLE

R9398 100K

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 11 for HPD.

SIGNAL_MODEL=T29DP_MUX

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

C9330 0.1UF; C9331 0.1UF

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	RESET#/PIO0_0	R/PIO1_0/AD1	T29DPA_CONFIG1_RC
	PIO0_1/CLKOUT	R/PIO1_1/AD2	T29DPA_CONFIG2_RC
T29_LSEO<0>	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3	T29_A_HV_EN_R
I2C_T29_SCL	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4	T29_A_UC_ADDR
I2C_T29_SDA	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP	DP_A_EXT_HPD
T29DPA_HPD	PIO0_6/SCK	PIO1_6/RXD	T29_A_LSX_P2R
T29_A_BIAS	PIO0_7/CTS#	PIO1_7/TXD	T29_A_LSX_R2P
T29_LSOE<0>	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0	T29_LSEO<1>
T29_LSOE<1>	PIO0_9/MOSI/CT16B0_MAT1		
	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
T29_MCU_INT_L	R/PIO0_11/AD0 (OD)	XTALIN	

R9338 10K → R9334 10K → T29_A_HV_EN

P2R = Plug to Receptacle
R2P = Receptacle to Plug

R9339 1M

I2C Addr: 0x26/0x27 (Wr/Rd)

R9335 1K; R9336 10K

=T29_WAKE_L: use PCIe WAKE#

PCIE_WAKE_L → OMIT R9330 0 → SWCLK / SWDIO → T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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3.3V/HV Power MUX

Port A HV Power Switch

PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP15V_T29
20V Max

R9416 470K 1% 1/16W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 SN1010017 QFN
VIN VOUT EN* (IPU-Weak!) FLT* RTRY* ILIM CT IFLT GND THRM PAD

C9411 0.1UF 10% 50V X7R 603-1

PPHV_SW_DPAPWR

D9410 SM STPS2L30AF

TP_DPAPWRSW_FLT_L

DPAPWRSW_HVEN_L_R

DPAPWRSW_ILIM

DPAPWRSW_IFLT

DPAPWRSW_CT

C9412 OMIT_TABLE 0.47UF 10% 16V X5R-CERM 402 <CT>

R9410 100K 1% 1/16W MF-LF 402 <RFLT>

R9411 210K 1% 1/16W MF-LF 402 <RLIM>

(*) U9410 tolerance unknown

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

Bleeder Resistor
2.5V / 249 ohm = 10mA
R9419 249 1% 1/16W MF-LF 402 P = ~27mW
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Q9419 DMB53D0UV SOT-563

DPAPWR_BLDR_B

DPAPWR_BLDR_E

Q9419 DMB53D0UV SOT-563

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

T29_A_HV_EN

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL D9425 POWERDI-123 DFLS1100

CRITICAL Q9425 SI8409DB BGA

3.3V/HV MUXed

3.3V Always

Blocking FET, off when Source >3.4V or HV_EN high.

R9427 100K 1% 1/16W MF-LF 402

R9428 21.5K 1% 1/16W MF-LF 402

R9425 4.7K 5% 1/16W MF-LF 402

R9426 1K 5% 1/16W MF-LF 402

R9430 4.7K 5% 1/16W MF-LF 402

DPAPWRSW_VREF

DPAPWRSW_P3V3_ON_L

DPAPWRSW_HV_DET_R_L

CRITICAL U9426 ZXRE060A SOT353

R9429 4.7K 5% 1/16W MF-LF 402

C9424 0.47UF 10% 16V CERM-X5R 402

DPAPWRSW_ON_L_C

Q9426 MMDT3946XG SOT363

C9426 0.1UF 20% 10V CERM 402

NO STUFF C9429 0.1UF 20% 10V CERM 402

R9424 22 5% 1/16W MF-LF 402

DPAPWRSW_HV_DET_L

DPAPWRSW_NPN_E

R9418 1K 5% 1/16W MF 402

DPAPWRSW_HV_DET

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

Port A 3.3V Power Switch

CRITICAL U9480 TPS2051B SOT23

DP_PWR must be S4 to support wake from T29 devices.

PP3V3_S5

T29_A_HV_EN

SMC_S4_WAKESRC_EN

C9486 10UF 20% 6.3V X5R 603

C9485 0.1UF 20% 10V CERM 402

C9481 0.1UF 20% 10V CERM 402

C9480 22UF 20% 6.3V X5R-CERM-1 603

CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

T29_A_BIAS

CRITICAL U9435 ZXRE060A SOT353

C9435 0.1UF 20% 10V CERM 402

DPAPWRSW_P3V3_ON

C9436 1UF 10% 10V X5R 402

Q9430 SSM6N37FEAPE SOT563

Q9430 SSM6N37FEAPE SOT563

DPAPWRSW_ON_C

T29_A_HV_EN

R9437 82 5% 1/16W MF-LF 402

T29_2V9_ENABLE

R9435 100K 1% 1/16W MF-LF 402

DPAPWR_FB_DIV

R9436 24.9K 1% 1/16W MF-LF 402

R9433 220 5% 1/16W MF-LF 402

R9432 10K 5% 1/16W MF 402

Circuit threshold range: 2.877-2.941V (2.903V nominal)

DisplayPort/T29 A Connector

PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

L9400 FERR-120-OHM-3A 0603

C9400 0.01UF 10% 50V X7R 402

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

T29_A_BIAS

C9490 0.1UF 10% 6.3V X5R 201

PLACE_NEAR=C9490.1:2mm

R9490 51 5% 1/20W MF 201

T29_A_BIAS_R
VOLTAGE=3.3V

T29 Dir DP Dir

T29_D2R_C_P<0>
T29_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

T29_A_BIAS_D2R_P1
T29_A_BIAS_D2R_N1

R9498 2.2K 5% 1/20W MF 201

R9499 2.2K 5% 1/20W MF 201

T29: Unused

T29DPA_ML_P<3>
T29DPA_ML_N<3>

CRITICAL L9498 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY

CRITICAL L9499 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY

D9498 BAR90-02LRH TSLP-2-7

D9499 BAR90-02LRH TSLP-2-7

CRITICAL GND_VOID=TRUE SIGNAL_MODEL=T29PIN (Both L's)

T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N

DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

R9403 12 5% 1/16W MF-LF 402 GND_DPACONN_8

R9404 12 5% 1/16W MF-LF 402 GND_DPACONN_14

R9402 12 5% 1/16W MF-LF 402

T29DPA_HPD_R

R9401 12 5% 1/16W MF-LF 402

DPACONN_20_RC

C9498 30PF 5% 50V CERM 402

C9499 30PF 5% 50V CERM 402

C9402 0.01UF 10% 50V X7R 402

C9401 0.01UF 10% 50V X7R 402

T29DPA_HPD
T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC

R9452 1M 5% 1/16W MF-LF 402

R9451 1M 5% 1/16W MF-LF 402

C9494 330PF 10% 50V CERM 402

C9495 330PF 10% 50V CERM 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/16W MF-LF 402

For J9400 T29 SMT pads (3, 5, 17 & 19):
GND_VOID=TRUE

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	GND 1
4	CONFIG1	ML_LANE0P 3
6	CONFIG2	ML_LANE0N 5
8	GND	GND 7
10	ML_LANE3P	ML_LANE1P 9
12	ML_LANE3N	ML_LANE1N 11
14	GND	GND 13
16	AUX_CHP	ML_LANE2P 15
18	AUX_CHN	ML_LANE2N 17
20	DP_PWR	RETURN 19

SHIELD PINS 22 21

OMIT_TABLE R9405 12 5% 1/20W MF 201 GND_DPACONN_1 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

DP Dir T29 Dir

T29DPA_ML_P<0>
T29DPA_ML_N<0>

T29: TX_0

OMIT_TABLE R9406 12 5% 1/20W MF 201 GND_DPACONN_7 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

T29DPA_ML_P<1>
T29DPA_ML_N<1>

T29: LSX_R2P/P2R (P/N)

R9407 12 5% 1/20W MF 201 GND_DPACONN_13 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

T29DPA_ML_P<2>
T29DPA_ML_N<2>

T29: TX_1

GND_DPACONN_19 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

L9408 FERR-120-OHM-3A 0603

R9408 12 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)

C9470 0.47UF 20% 4V CERM-X5R-1 201

C9471 0.47UF 20% 4V CERM-X5R-1 201

R9470 470K 5% 1/20W MF 201

R9471 470K 5% 1/20W MF 201

C9472 0.47UF 20% 4V CERM-X5R-1 201

C9473 0.47UF 20% 4V CERM-X5R-1 201

R9472 470K 5% 1/20W MF 201

R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0 OHM,5,1/16W,0402,SMD,LF	C9412		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,X5R,0201,SMD	R9405		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,X5R,0201,SMD	R9406		

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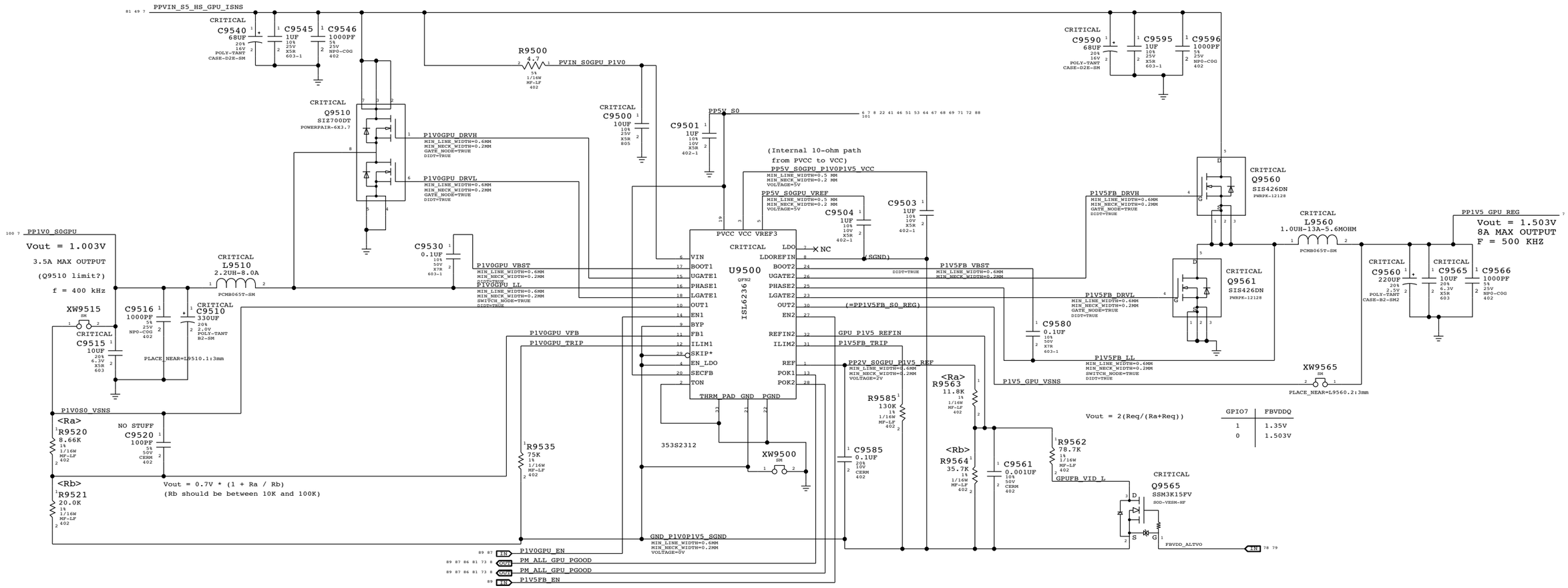

SYNC MASTER=K91 ERIC	SYNC DATE=10/08/2010
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GMUX CPLD

R9600 0 5% 1/16W MF-LF 402 — PP3V3_S0

C9610 0.1UF 20% 10V CERM 402 — PP3V3_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V)

R9610 0 5% 1/16W MF-LF 402 — PP1V8_S0

C9611 0.1UF 20% 10V CERM 402 — PP1V8_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=1.8V)

C9600 4.7UF 20% 4V X5R-1 402 — PP1V2_S0

C9604 0.1UF 20% 10V CERM 402

C9605 0.1UF 20% 10V CERM 402

C9606 0.1UF 20% 10V CERM 402

C9607 0.1UF 20% 10V CERM 402

C9608 0.1UF 20% 10V CERM 402

C9609 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_ULC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V) — L9621 FERR-220-OHM 0402 — C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V) — L9620 FERR-220-OHM 0402 — C9630 0.1UF 20% 10V CERM 402

VCC: C4, J3, J13, N11, P8 — VCCAUX: C11, J2, J14, M8 — VCCIO00: B5 — VCCIO01: B7 — VCCIO02: A12 — VCCIO03: C14 — VCCIO04: F13 — VCCIO05: M12 — VCCIO06: M9 — VCCIO07: M3 — GNDIO00: N5 — GNDIO01: M1 — GNDIO02: C3 — GNDIO03: F2 — VCCJ: K12 — ULC_VCCPLL: A4 — LRC_VCCPLL: P11

OMIT CRITICAL

U9600 XP25-5 CSBGA

JTAG_ISP_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	
JTAG_GMUX_TDO	K13	TDO	
JTAG_GMUX_TMS	L12	TMS	
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB7A	BANK5
LCD_BKLT_PWM	N2	PB7B	BANK5
LVDS_DDC_SEL_EG	P4	PB14A	BANK5
LVDS_DDC_SEL_IG	N4	PB14B	BANK5
DP_MUX_EN	N3	PB15A(OD)	BANK5
DP_MUX_SEL_EG	M4	PB15B	BANK5
EG_RESET_L	P5	PB16A	BANK5
P3V3GPU_EN	M5	PB16B	BANK5
GPUVCORE_EN	P6	PB17A	BANK5
P1V0GPU_EN	M6	PB17B	BANK5
P1V5FB1V8GPU_R_EN	P7	PB18A	BANK5
PEG_CLKREQ_L	M7	PB18B(OD)	BANK5
DP_CA_DET_EG	N7	PB19A	BANK5
LCD_PWR_EN	N8	PB19B	BANK5
LPC_AD<0>	P9	PB20A	BANK4
LPC_AD<1>	N9	PB20B	BANK4
LPC_AD<2>	P10	PB26A	BANK4
LPC_AD<3>	M10	PB26B	BANK4
LPC_FRAME_L	P12	PB27A	BANK4
LPCPLUS_RESET_L	P13	PB27B	BANK4
LPC_CLK33M_GMUX	N12	PB28A	BANK4
GMUX_INT	P14	PB28B	BANK4
LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK7
LVDS_IG_B_DATA_N<2>	B2	PL2B	BANK7
GMUX_PL6A	C2	PL6A	BANK7
TP_GMUX_PL6B	D3	PL6B	BANK7
LVDS_IG_A_DATA_P<0>	D1	PL7A	BANK7
LVDS_IG_A_DATA_N<0>	E1	PL7B	BANK7
LVDS_IG_A_DATA_P<1>	D2	PL8A	BANK7
LVDS_IG_A_DATA_N<1>	E3	PL8B	BANK7
LVDS_IG_A_DATA_P<2>	F1	PL9A	BANK7
LVDS_IG_A_DATA_N<2>	G1	PL9B	BANK7
LVDS_IG_B_DATA_P<0>	F3	PL10A	BANK7
LVDS_IG_B_DATA_N<0>	G2	PL10B	BANK7
LVDS_IG_B_DATA_P<1>	H2	PL11A	BANK7
LVDS_IG_B_DATA_N<1>	G3	PL11B	BANK7
LVDS_IG_A_CLK_P	H1	PL12A	BANK7
LVDS_IG_A_CLK_N	H3	PL12B	BANK7
TP_LVDS_MUX_SEL_EG	L1	PL14A	BANK6
TP_GMUX_PL14B	L3	PL14B	BANK6
GMUX_RESET_L	K3	PL15A	BANK6
GMUX_VSYNC	L2	PL15B	BANK6
PM_ALL_GPU_PGOOD	N1	PL25A	BANK6
PEX_CLKREQ_L	P1	PL25B	BANK6

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

LVDS_B_DATA_P<0>	A2	PT7A	BANK0
LVDS_B_DATA_N<0>	A3	PT7B	BANK0
LVDS_B_DATA_P<1>	A1	PT8A	BANK0
LVDS_B_DATA_N<1>	B3	PT8B	BANK0
LVDS_B_DATA_P<2>	C5	PT9A	BANK0
LVDS_B_DATA_N<2>	A5	PT9B	BANK0
EG_PWRSEQ_EN	B6	PT14A	BANK0
GMUX_DEBUG_RESET_L	C7	PT14B	BANK0
LVDS_A_CLK_P	A6	PT15A	BANK0
LVDS_A_CLK_N	A7	PT15B	BANK0
LVDS_B_CLK_P	C8	PT16A	BANK0
LVDS_B_CLK_N	C9	PT16B	BANK0
LVDS_A_DATA_P<0>	A8	PT17A	BANK0
LVDS_A_DATA_N<0>	B9	PT17B	BANK0
LVDS_A_DATA_P<1>	A9	PT18A	BANK0
LVDS_A_DATA_N<1>	C10	PT18B	BANK0
LVDS_A_DATA_P<2>	B10	PT19A	BANK0
LVDS_A_DATA_N<2>	A10	PT19B	BANK0
GND	A11	PT20A	BANK1
GND	B12	PT20B	BANK1
GND	B13	PT28A	BANK1
GND	A13	PT28B	BANK1
DP_A_CA_DET	A14	PR2A	BANK2
DP_HOTPLUG_DET	B14	PR2B	BANK2
LVDS_EG_A_DATA_P<0>	D12	PR6A	BANK2
LVDS_EG_A_DATA_N<0>	D13	PR6B	BANK2
LVDS_EG_A_DATA_P<1>	D14	PR7A	BANK2
LVDS_EG_A_DATA_N<1>	E14	PR7B	BANK2
LVDS_EG_A_DATA_P<2>	E12	PR8A	BANK2
LVDS_EG_A_DATA_N<2>	F12	PR8B	BANK2
LVDS_EG_B_DATA_P<0>	F14	PR9A	BANK2
LVDS_EG_B_DATA_N<0>	G14	PR9B	BANK2
LVDS_EG_B_DATA_P<1>	G12	PR10A	BANK2
LVDS_EG_B_DATA_N<1>	G13	PR10B	BANK2
LVDS_EG_B_DATA_P<2>	H13	PR11A	BANK2
LVDS_EG_B_DATA_N<2>	H12	PR11B	BANK2
LVDS_EG_A_CLK_P	H14	PR12A	BANK2
LVDS_EG_A_CLK_N	J12	PR12B	BANK2
LVDS_IG_PANEL_PWR	L14	PR14A	BANK3
EG_LCD_PWR_EN	M13	PR14B	BANK3
LVDS_IG_BKL_ON	N14	PR24A	BANK3
EG_BKLT_EN	N13	PR24B	BANK3

R9645 10K 1% 1/20W MF 201 — PP3V3_S0

R9640 10K 1% 1/20W MF 201 — PP3V3_S0

NO STUFF R9646 10K 1% 1/20W MF 201

NO STUFF R9641 10K 1% 1/20W MF 201

CRITICAL J9600 1909782 M-RT-SM — GMUX_JTAG_CONN

1	PP3V3_S0	
2	JTAG_GMUX_TDO	
3	JTAG_GMUX_TDI	
4	JTAG_GMUX_TMS	
5		
6	JTAG_ISP_TCK	
7		
8		

NO STUFF R9647 10K 1% 1/20W MF 201

NO STUFF R9670 10K 1% 1/20W MF 201 — GMUX_VSYNC

R9605 1K 5% 1/20W MF 201 — PP3V3_T29 — T29_JTAG_FET

Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDI — JTAG_ISP_TDI

Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDO — JTAG_ISP_TDO

PP3V3_S3 — R9676 100K 5% 1/20W MF 201 — GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563 — GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563 — ALL_SYS_PWRGD

R9678 4.7K 5% 1/20W MF 201 — P3V3GPU_EN

R9671 4.7K 5% 1/20W MF 201 — P1V0GPU_EN

R9672 4.7K 5% 1/20W MF 201 — GPUVCORE_EN

R9673 4.7K 5% 1/20W MF 201 — P1V5FB1V8GPU_R_EN

R9674 4.7K 5% 1/20W MF 201 — PP3V3_S0

NO STUFF R9675 0 5% 1/16W MF-LF 402 — GMUX_S3_PD_GND

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100 1% 1/20W MF 201	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100 1% 1/20W MF 201	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100 1% 1/20W MF 201	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100 1% 1/20W MF 201	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100 1% 1/20W MF 201	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100 1% 1/20W MF 201	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100 1% 1/20W MF 201	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100 1% 1/20W MF 201	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100 1% 1/20W MF 201	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100 1% 1/20W MF 201	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100 1% 1/20W MF 201	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100 1% 1/20W MF 201	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100 1% 1/20W MF 201	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100 1% 1/20W MF 201	LVDS_EG_B_DATA_N<2>

SIGNAL_MODEL=EMPTY

Required Pullups

PP3V3_S0

EG_PWRSEQ_EN	R9684	1K 5% 1/20W MF 201	
JTAG_GMUX_TDI	R9685	10K 5% 1/20W MF 201	
JTAG_GMUX_TDO	R9686	10K 5% 1/20W MF 201	
GMUX_DEBUG_RESET_L	R9680	1K 5% 1/20W MF 201	

NO STUFF R9679 10K 1% 1/16W MF-LF 402 — SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K 5% 1/20W MF 201	
LVDS_DDC_SEL_IG	R9682	10K 5% 1/20W MF 201	
LVDS_DDC_SEL_EG	R9683	10K 5% 1/20W MF 201	NO STUFF
EG_RESET_L	R9691	100K 5% 1/20W MF 201	
LCD_BKLT_PWM	R9693	100K 5% 1/20W MF 201	

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

CRITICAL
Q9706
FDC638APZ_SBMS001
SSOT6-HF

PPBUS_G3H
F9700
3AMP-32V-467
603-HF
BOTTOM
PPBUS_S0_LCDBKLT_FUSED
PPBUS_SW_LCDBKLT_PWR
THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

R9788 301K 1% 1/16W MF-LF 402
C9782 0.1UF 10% 16V X5R 402
LCDBKLT_EN_DIV
R9789 147K 1% 1/16W MF-LF 402
LCDBKLT_EN_L
Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L

PP5V_S0
PPBUS_SW_BKL
CRITICAL
C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=L9701.1:3mm
CRITICAL
L9701
33UH-1.8A-110MOHM
1217AS-2SM
PPBUS_SW_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=50V
SWITCH_MODE=TRUE
DIDT=TRUE
PLACE_NEAR=L9701.2:3mm
CRITICAL
D9701
SOD-123
RB160M-60G
PLACE_NEAR=U9701.A5:3mm
C9796 220PF 10% 50V X7R-CERM 402
CRITICAL
C9797 10UF 10% 50V X5R 1210-1
CRITICAL
C9799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm
PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V

PLACE_NEAR=U9701.D1:5mm
C9710 1UF 10% 25V X5R 603-1
PLACE_NEAR=U9701.D1:3mm
C9714 0.010UF 10% 25V X7R-CERM 402
XW9720
SM
PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
PLACE_NEAR=C9797.1:5mm

PP3V3_S0
PLACE_NEAR=U9701.C4:4mm
C9711 0.1UF 10% 16V X5R 402

BKL_VSYNC_R
MIN_NECK_WIDTH=0.075 mm
NO STUFF
R9754 0 5% 1/16W MF-LF 402
R9755 10K 5% 1/16W MF-LF 402
NO STUFF
C9741 1UF 10% 6.3V X5R 402
GMUX_VSYNC
NO STUFF
C9740 10UF 20% 6.3V X5R 603
NO STUFF
R9740 47.0K 1% 1/16W MF-LF 402
BKL_FLTR_R
R9741 10K 5% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.075 mm
MIN_NECK_WIDTH=0.075 mm
MIN_NECK_WIDTH=0.075 mm
MIN_NECK_WIDTH=0.075 mm

U9701
25-BUMP-MICRO
LP8550
VDDIO VLDO VIN
VSYNC FILTER ISET FSET SCLK SDA PWM EN FAULT
SW_0 SW_1 FB OUT1 OUT2 OUT3 OUT4 OUT5 OUT6
GND_S GND_L GND_SW GND_SW
CRITICAL

BKL_FLTR
BKL_ISET
BKL_FSET
BKL_SCL
BKL_SDA
BKL_PWM
BKL_EN
TP_BKL_FAULT
PLACE_SIDE=BOTTOM

BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6

R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_CLK
R9757 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA
Addr: 0x58(Wr)/0x59(Rd)
PPBUS_SW_LCDBKLT_PWR
R9731 301K 1% 1/16W MF-LF 402
R9715 100K 1% 1/16W MF-LF 402
R9704 33 5% 1/16W MF-LF 402
LCD_BKLT_PWM
C9704 33PF 5% 50V C0BM 402

R9716 90.9K 1% 1/16W MF-LF 402
Fpwm=9.62kHz
see spec for others
R9714 16.2K 1% 1/16W MF-LF 402
I_LED=22.7mA
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)
XW9710
SM
GND_BKL_SGND
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402
LED_RETURN_1
R9718 0 5% 1/16W MF-LF 402
LED_RETURN_2
R9719 0 5% 1/16W MF-LF 402
LED_RETURN_3
R9720 0 5% 1/16W MF-LF 402
LED_RETURN_4
R9721 0 5% 1/16W MF-LF 402
LED_RETURN_5
R9722 0 5% 1/16W MF-LF 402
LED_RETURN_6
PLACE_NEAR=U9701.E5:10mm
PLACE_NEAR=U9701.D5:10mm
PLACE_NEAR=U9701.C5:10mm
PLACE_NEAR=U9701.E3:10mm
PLACE_NEAR=U9701.E2:10mm
PLACE_NEAR=U9701.E1:10mm
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
BOTTOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMT	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMT	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K901 KIRAN SYNC DATE=06/25/2010

LCD Backlight Driver

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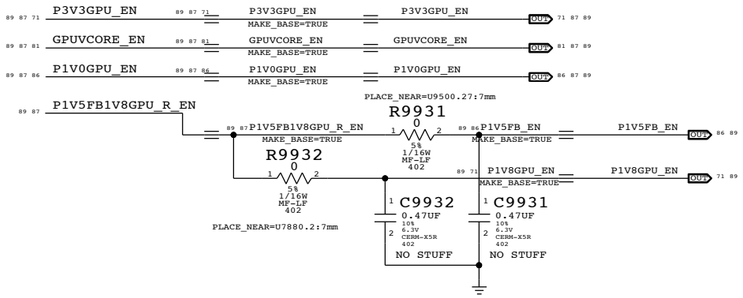
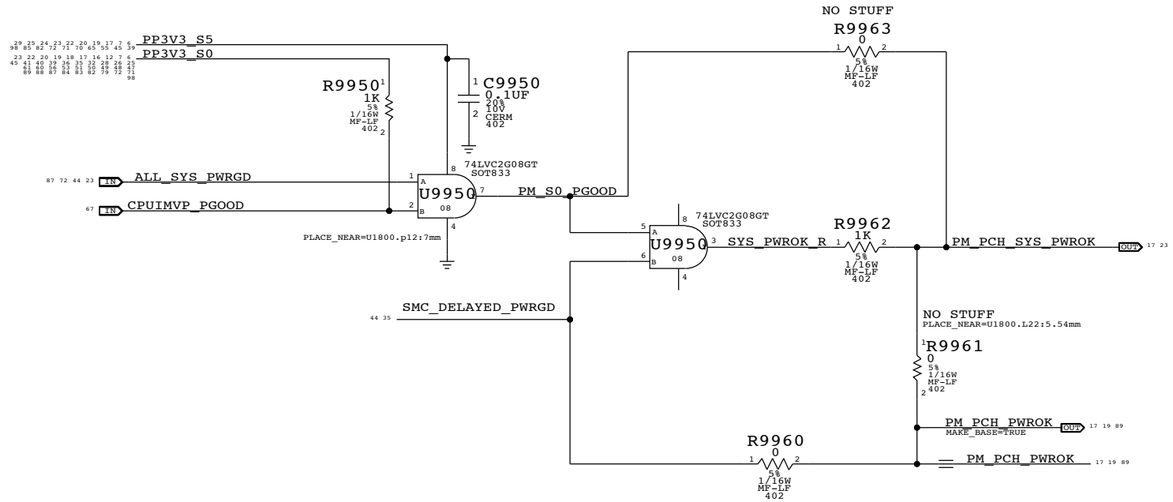
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

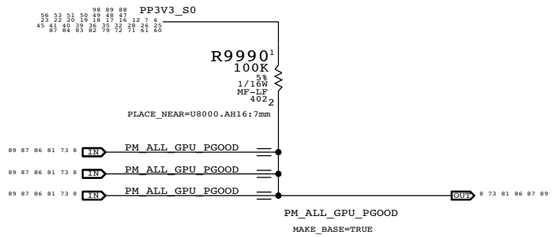
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V;GDDR5 1.5/1.35V



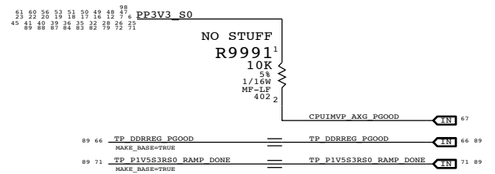
PCH S0 PWRGD



EXT GPU PWRGD Pullup



Unused PGOOD signal



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Power Sequencing EG/PCH S0

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	6 9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	CPU_50S	CPU_AGTL	FDI_INT	6 9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 44
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 67
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 67
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	73
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	73
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 73
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	73
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	73
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 67
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 67
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 67

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PAGE TITLE: CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:

DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 6 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 6 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 6 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 6 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 6 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 6 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 6 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 6 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 6 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 6 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 6 11 26 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 6 11 26 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 6 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 6 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 6 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 6 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 6 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 6 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 6 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 6 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 6 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 6 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 6 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 6 11 27 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 6 11 27 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 6 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 6 11 27

SYNC MASTER=K18 MLB SYNC DATE=04/27/2010

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 17 83
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 17 83
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 87
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N 16 41
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_N 6 41
T21 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P 41
T21	SATA_90D	SATA	SATA_HDD_R2D_UF_N 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 6 41
T21 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 18 24
	USB_85D	USB	USB_HUB1_UP_N 18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 18 24
	USB_85D	USB	USB_HUB2_UP_N 18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P 24 42
	USB_85D	USB	USB_EXTA_N 24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P 24 42
	USB_85D	USB	USB_EXTB_N 24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 24
	USB_85D	USB	USB_EXTC_N 8 24
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 31
	USB_85D	USB	USB_CAMERA_CONN_N 6 31
USB_BT	USB_85D	USB	USB_BT_P 24 31
	USB_85D	USB	USB_BT_N 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P 24 52
	USB_85D	USB	USB_TPAD_N 24 52
USB_IR	USB_85D	USB	USB_IR_P 24 43
	USB_85D	USB	USB_IR_N 24 43
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
T21 USB_T29A	USB_85D	USB	USB_T29A_P 8 24
T21	USB_85D	USB	USB_T29A_N 8 24

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 44 46 87
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 44 46 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 25 46 87
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 44
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 46
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 26 28 30 41 47 61 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 26 28 30 41 47 61 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 47
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 47
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 47
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 47
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 56
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 56
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 56
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 56
	HDA_50S	HDA	AUD_SDI_R	56
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 56
	HDA_50S	HDA	HDA_SDOUT_R	16
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 46
	SPI_55S	SPI	SPI_CLK	46
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 46
	SPI_55S	SPI	SPI_MOSI	46
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 46
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 46
	SPI_55S	SPI	SPI_CS0_L	46
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 73
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 73
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 16
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 9 33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 9 33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 9 33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 9 33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE: PCH Constraints 2

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR	*	=3X_DIELECTRIC	?

SOURCE: Attila Farkas Email - 8/2/10

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA_R<7..0>	
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD_R	32
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R	32
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA<7..0>	32 36
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R_L	32

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 38 40
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	38 40

Port 2 Not Used

SYNC MASTER=K91 ERIC SYNC DATE=08/03/2010

PAGE TITLE: Ethernet/FW Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 84
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 84
	T29DP_80D	T29DP	T29_R2D_C_P_P<1..0>	84
	T29DP_80D	T29DP	T29_R2D_C_P_N<1..0>	84
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 84 85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 84 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	84
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 84 95
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 84 95
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	84
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	84
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	84 85
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	84 85
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_P_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_P_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	95
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	95
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 78
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 78
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 78
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 78
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 47 84
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 47 84
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 84
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 84

Only used on hosts supporting T29 video-in

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 31 44 47 53 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 31 44 47 53 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 44 47 50
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 44 47 50
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 6 31 44 47 50 79
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 6 31 44 47 50 79
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 44 47 62 63
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 44 47 62 63
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 44 47 100
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 44 47 100

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 63
	1TO1_DIFFPAIR		CHGR_CSI_N 63
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 63
	1TO1_DIFFPAIR		CHGR_CSO_N 63

SYNC MASTER=K18 MLB SYNC DATE=04/27/2010

PAGE TITLE: SMC Constraints

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	75 76
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0>	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0>	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L	75 76
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	6 75 76
1297 FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	6 75 76
1298 FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	6 75 76
1299 FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	6 75 76
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	6 75 76
1296 FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	6 75 76
1295 FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	6 75 76
1294 FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	6 75 76
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	6 75 76
1299 FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	6 75 76
1300 FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	6 75 76
1301 FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	6 75 76
1302 FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	6 75 76
1303 FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	6 75 76
1304 FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	6 75 76
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	6 75 76
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	6 75 76
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	6 75 76
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	6 75 76
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	6 75 76
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	6 75 76
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	6 75 76
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	6 75 76
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	6 75 76
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	75 76 77

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	75 77
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	75 77
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 75 77
1305 FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 75 77
1306 FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 75 77
1307 FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 75 77
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 75 77
1308 FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 75 77
1309 FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 75 77
1310 FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 75 77
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 75 77
1311 FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 75 77
1312 FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 75 77
1313 FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 75 77
1314 FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 75 77
1315 FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 75 77
1316 FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 75 77
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 75 77
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	6 75 77
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	6 75 77
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	6 75 77
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	6 75 77
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	6 75 77
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	6 75 77
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	6 75 77
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	6 75 77

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	83 87
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	83 87
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	4 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	4 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	4 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	4 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 82 83

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	78 79
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	78 79
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	78 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	78 87
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	78 79
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	78 79
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	78 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	78 87
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	78 79
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	78 79
DP_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	83 84
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUXCH_P	8 78 83
	DP_85D	DISPLAYPORT	DP_EG_AUXCH_N	8 78 83

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

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GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 mm		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	50 78
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N	50 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	48 64
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	48 64
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	48 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	48 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	48 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	48 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 68
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 68
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 59
	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_N	59

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	63
	1TO1_DIFFPAIR		CHGR_CSI_R_N	63
	1TO1_DIFFPAIR		CHGR_CSO_R_P	49 63
	1TO1_DIFFPAIR		CHGR_CSO_R_N	49 63
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 42
	USB_85D	USB	CONN_USB2_BT_P	6
	USB_85D	USB	CONN_USB2_BT_N	6
	USB_85D	USB	USB_LT2_P	6 42
	USB_85D	USB	USB_LT2_N	6 42
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375L_P	59
	AUDIODIFF	AUDIO	SSM2375L_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375R_P	59
	AUDIODIFF	AUDIO	SSM2375R_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375S_P	59
	AUDIODIFF	AUDIO	SSM2375S_N	59
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 59 60
	USB_85D	USB	USB_TPAD_R_P	52
	USB_85D	USB	USB_TPAD_R_N	52
		SB_POWER	PP3V3_S5	45 55 65 70 71 72 82 85 89 4 7 17 19 20 22 23 24 25 29 39
		SB_POWER	PP3V3_S0	48 49 50 51 53 56 60 61 71 72 4 7 12 16 17 18 19 20 22 23 25 75 82 83 84 87 88 89 41 45 47 8
		SB_POWER	PP1V5_S3RS0	
		GND	GND	

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Project Specific Constraints

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K91 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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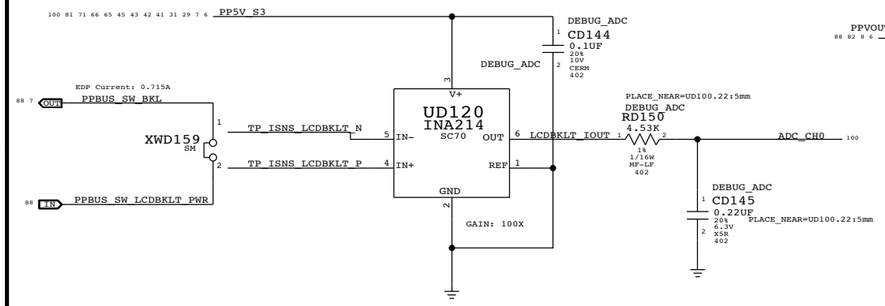
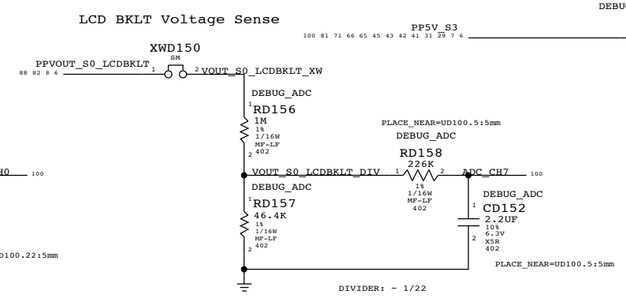
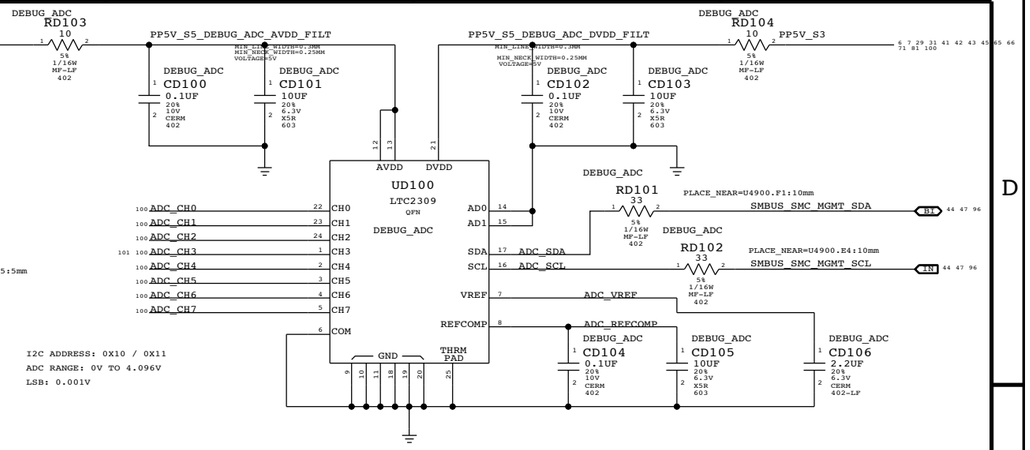
LCD BKLT Current Sense

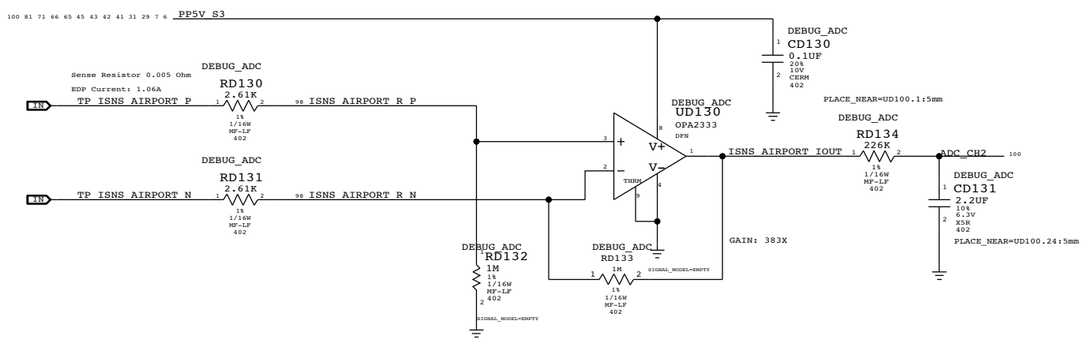


LCD BKLT Voltage Sense

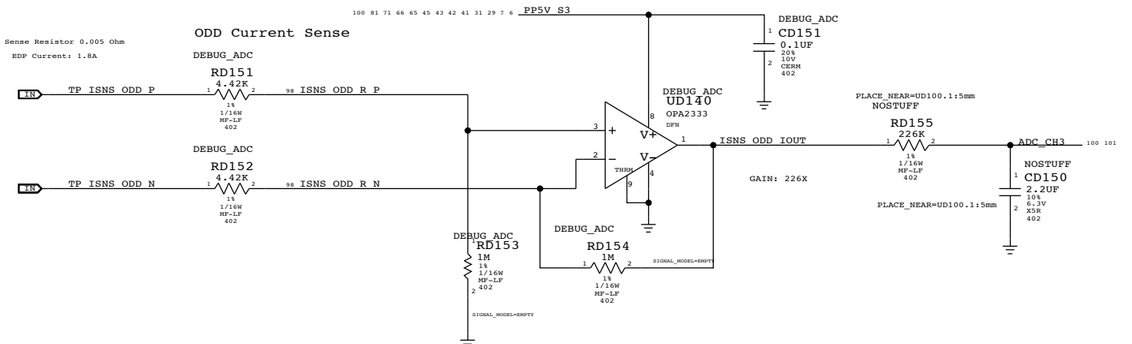




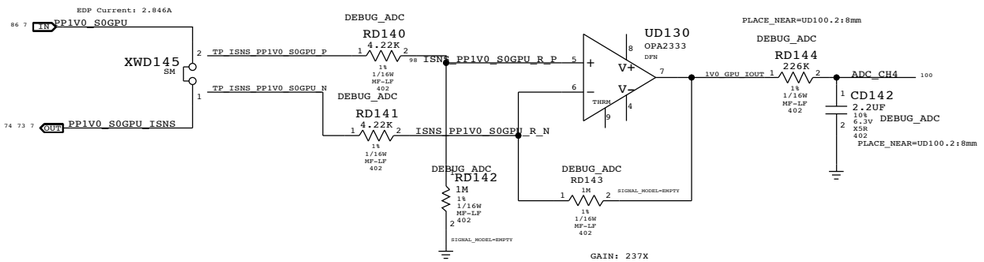
AIRPORT Current Sense



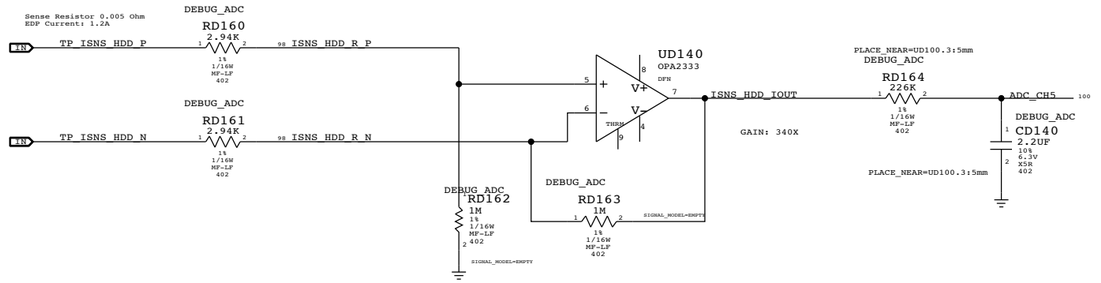
ODD Current Sense



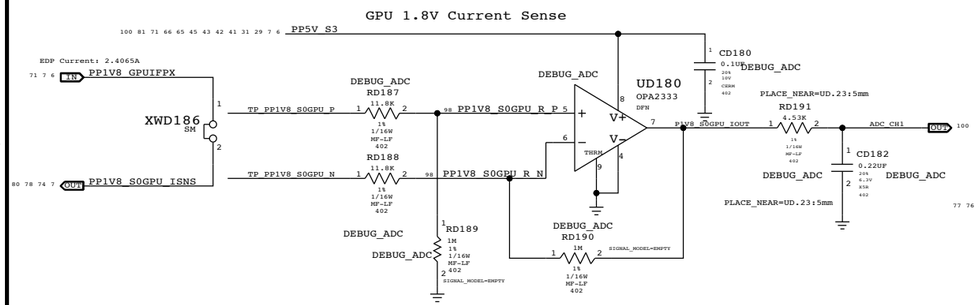
GPU 1.0V Current Sense



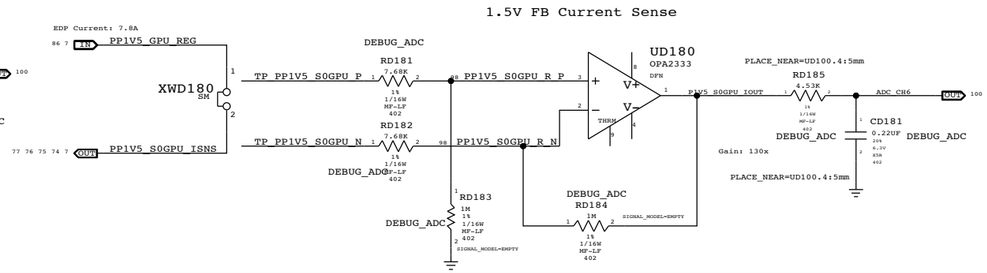
HDD Current Sense



GPU 1.8V Current Sense



1.5V FB Current Sense



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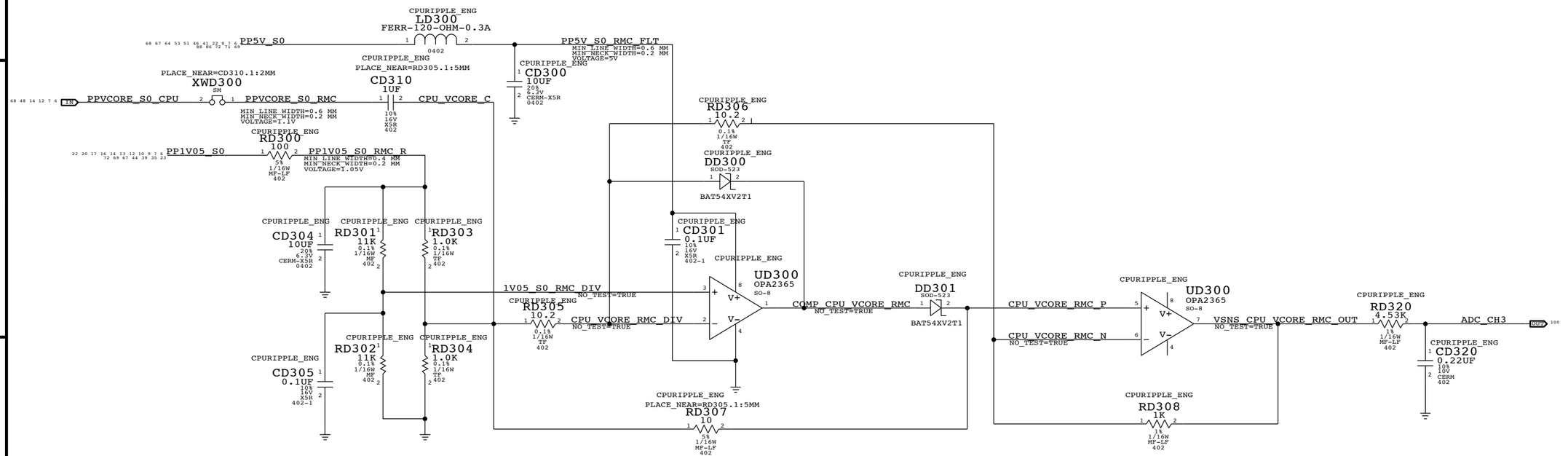

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