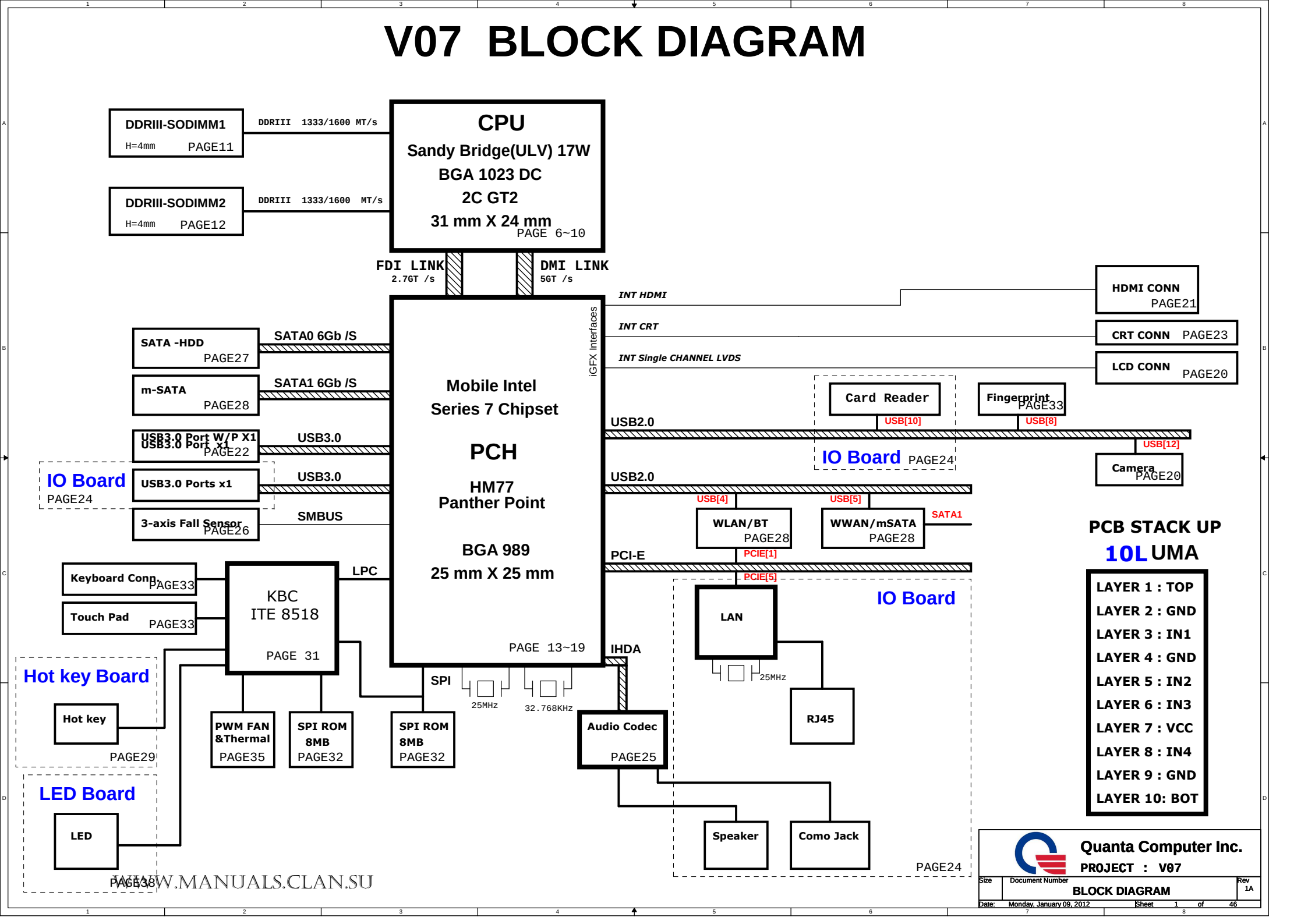
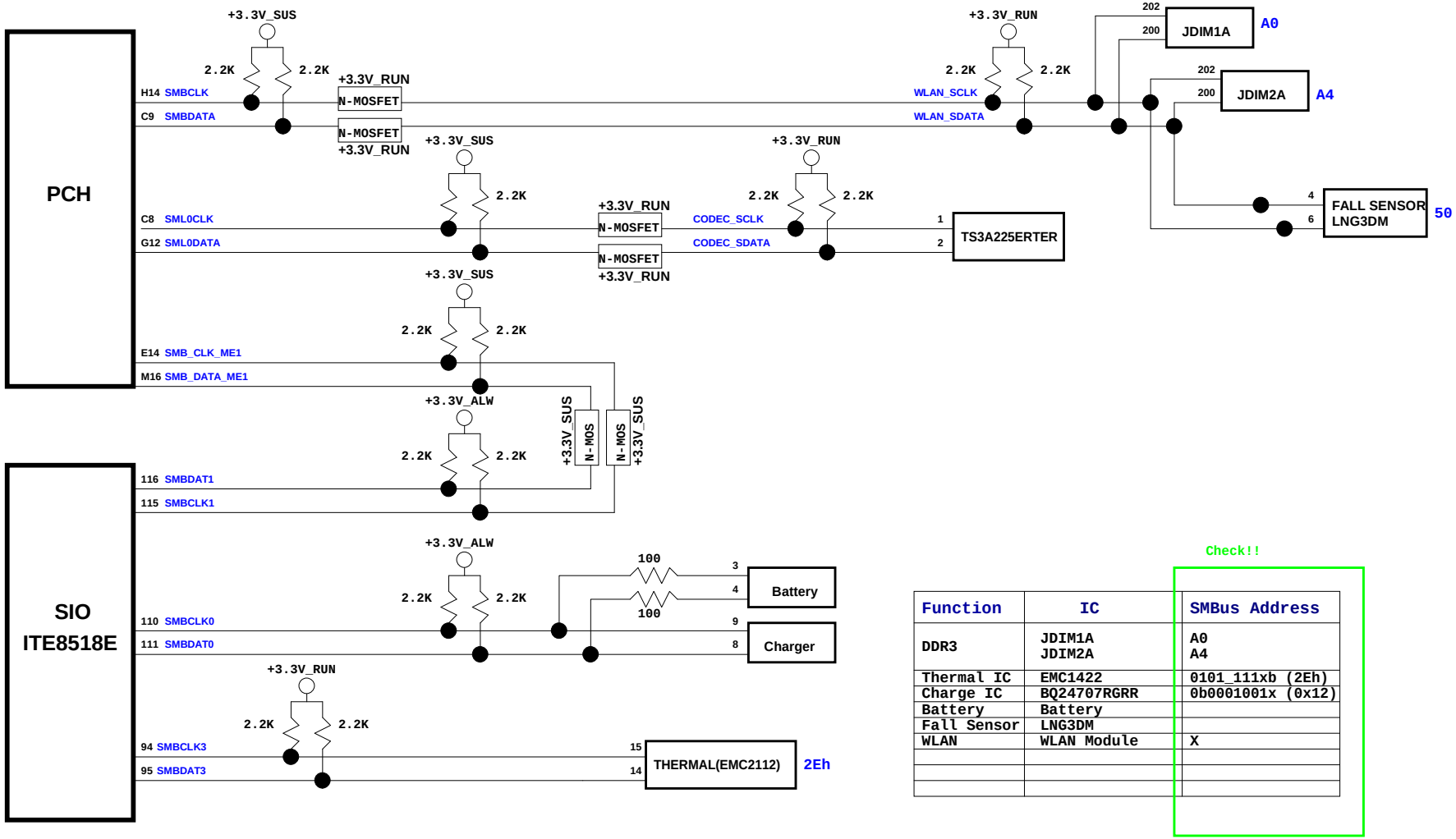
V07 BLOCK DIAGRAM





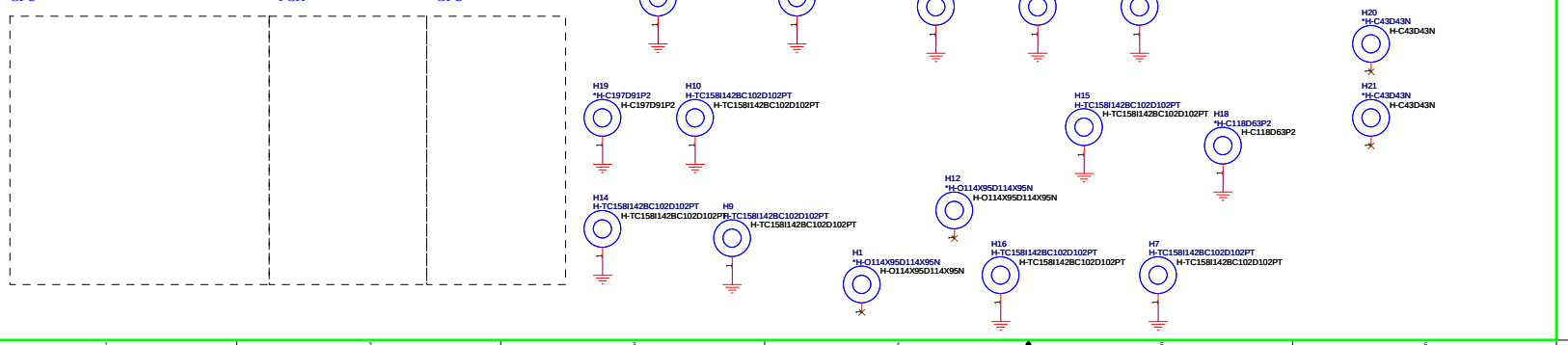
Check!!

Function	IC	SMBus Address
DDR3	JDIM1A JDIM2A	A0 A4
Thermal IC	EMC1422	0101_111xb (2Eh)
Charge IC	BQ24707RGRR	0b0001001x (0x12)
Battery	Battery	
Fall Sensor	LNG3DM	
WLAN	WLAN Module	X

SCREW PAD

0704 Delet H1~H10, H12~H25

MB



For CPU Use

0704 Modify footprint from "INTEL-CPU-BRACKET" to "intel-cpu-bkt2"

Quanta Computer Inc.
PROJECT : V07
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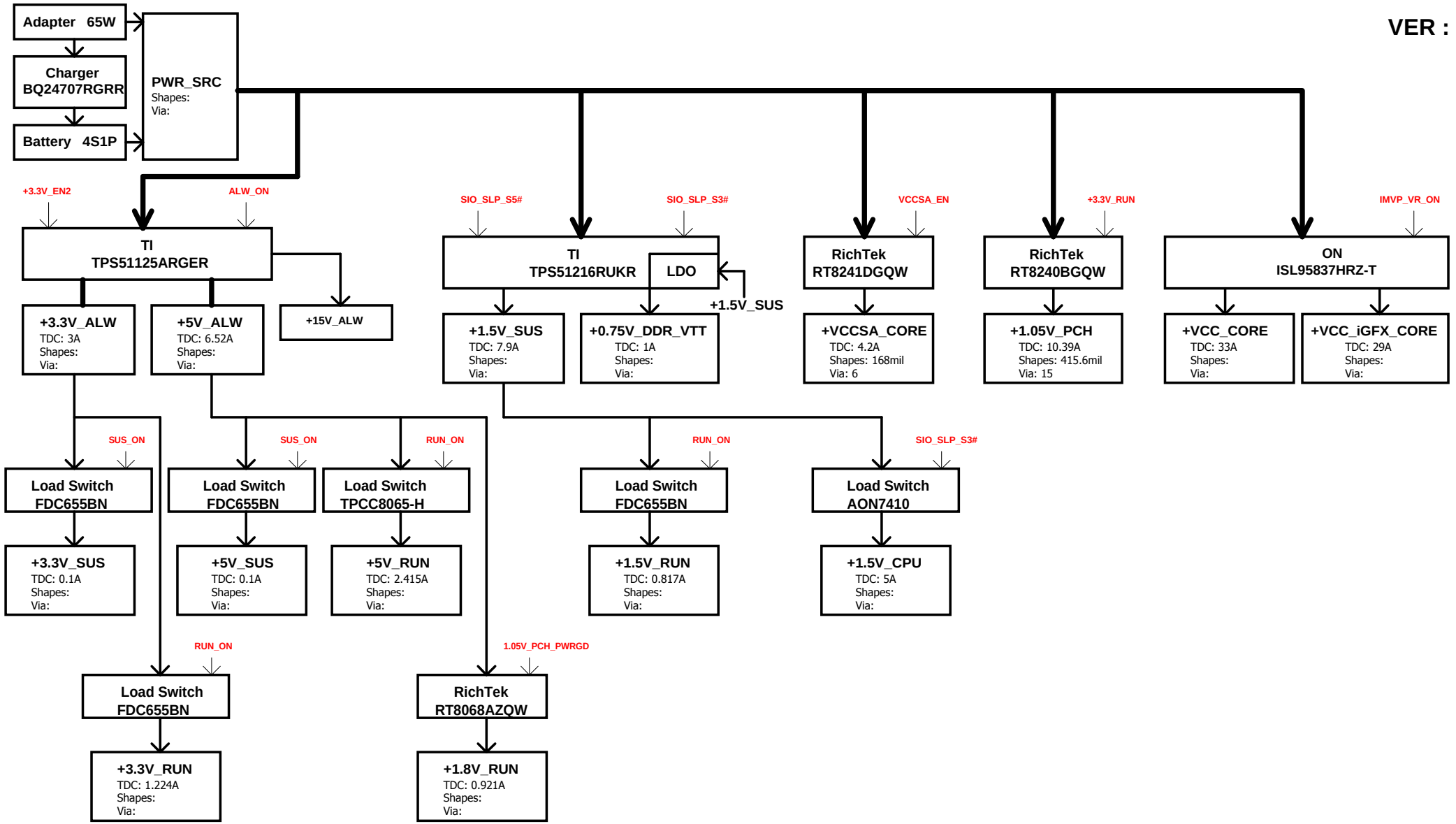
SMB/SCREW PAD
Date: Monday, January 09, 2012 | Sheet 2 of 46

USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0/eSATA/ Power share/ debug port)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0) (NC)
USB4	MiniCard 1 (WLAN/BT/WiMAX)
USB5	MiniCard 2 (WWAN)
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	Touch panel (NC, for debug)
USB10	Card Reader
USB11	Express Card (NC)
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD (NC)
SATA4	eSATA (NC)
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	WWAN (NC)
PCIE 3	Card reader (NC)
PCIE 4	NC
PCIE 5	LAN
PCIE 6	Express card (NC)
PCIE 7	NC
PCIE 8	NC

VER : 1A



Quanta Computer Inc.

PROJECT : V04

Size	Document Number	Rev
	Power Block Diagram	1A

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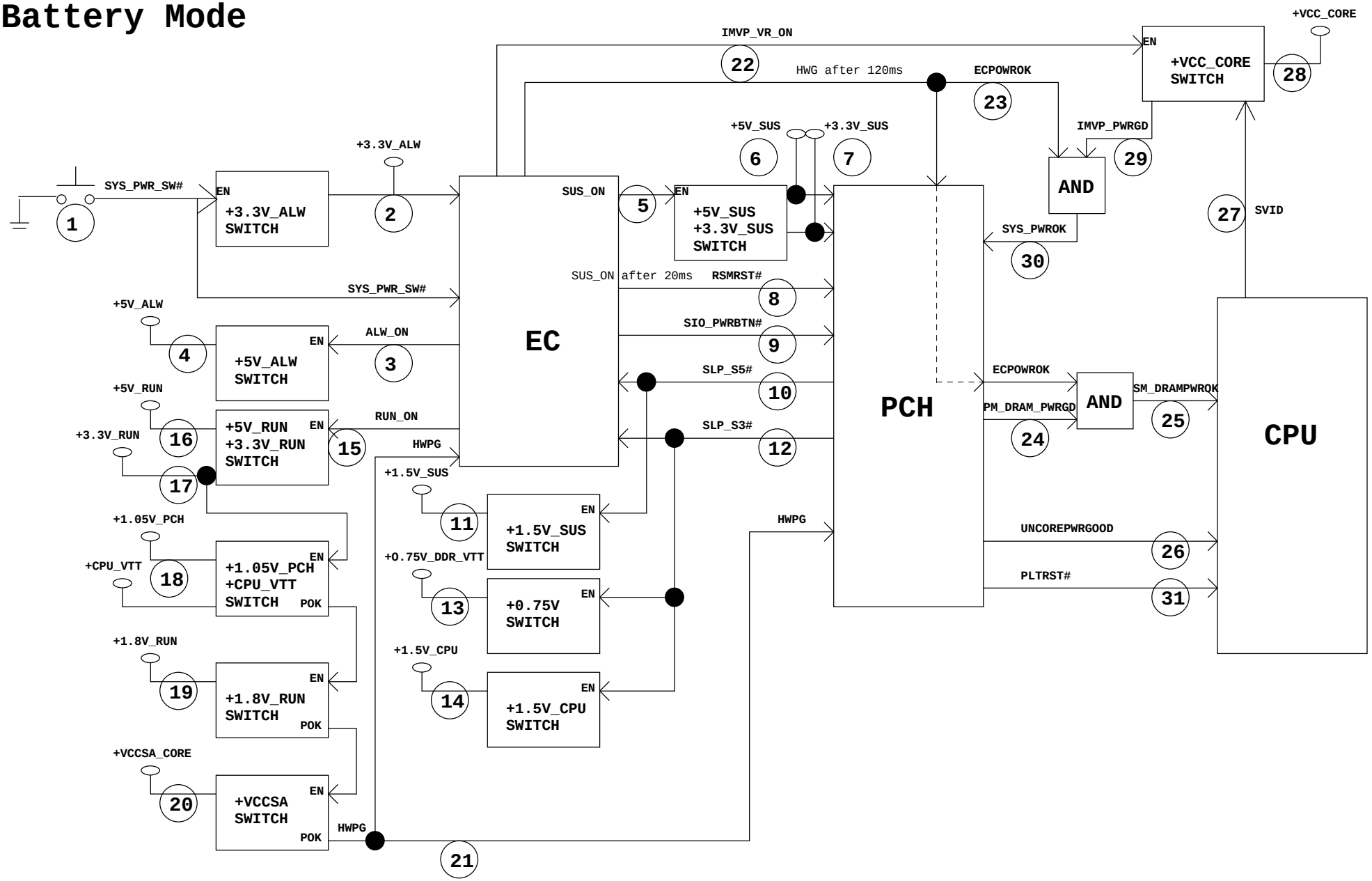
Battery Mode



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	POWER SEQUENCE	1A

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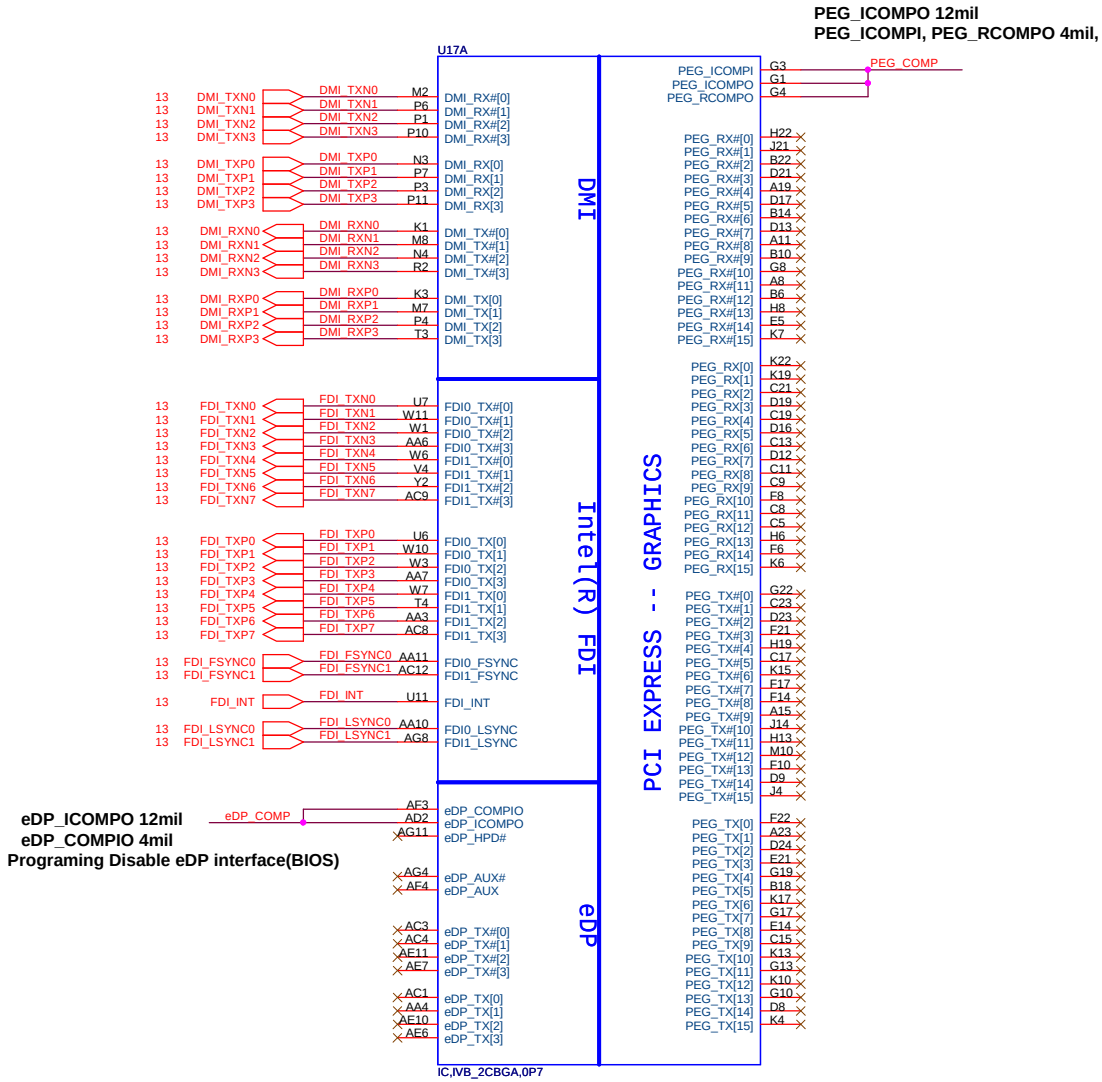
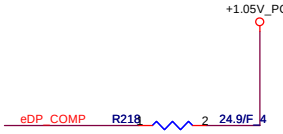
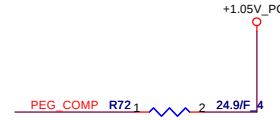
Ivy Bridge Processor (RESERVED, CFG)



DP & PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

Quanta Computer Inc.

PROJECT : V07

Size	Document Number	Rev
	Ivy Bridge 1/5	1A

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Ivy Bridge Processor (CLK,MISC,JTAG)

U17B

MISC | CLOCKS | THERMAL | DDR3 MISC | PWR MANAGEMENT | JTAG & BPM

SNB_IVB# N.A at SNB EDS #27637 0.7v1

16 H_SNB_IVB# — H_SNB_IVB# — F49 PROC_SELECT#
31 H_CPUDET# — H_CPUDET# — C57 PROC_DETECT#

TP2 — CATERR# — C49 CATERR#

31 PECI_EC — PECI_EC — R21 43_4 — PECI_EC_R — A48 PECI

31,45,46 IMVP7_PROCHOT# — IMVP7_PROCHOT# — R255 56_4 — H_PROCHOT# — C45 PROCHOT#

Over 130 degree C will drive low

18 PM_THRMTRIP# — PM_THRMTRIP# — D45 THERMTRIP#

13 H_PM_SYNC — H_PM_SYNC — C48 PM_SYNC

18 H_PWRGOOD — H_PWRGOOD — B46 UNCOREPWRGOOD

10K_4 — R259

SM_DRAMPWROK — BE45 SM_DRAMPWROK

1.1V

16,24,28,31 PLTRST# — PLTRST# — R254 1.5K/F_4 — CPU_PLTRST#_R — D44 RESET#

R251 750/F_4

IC,IVB_2CBGA,0P7

BCLK — J3 CLK_CPU_BCLKP — CLK_CPU_BCLKP 17
BCLK# — H2 CLK_CPU_BCLKN — CLK_CPU_BCLKN 17

DPLL_REF_CLK — AG3 CLK_DP_P_R — R216 1K_4
DPLL_REF_CLK# — AG1 CLK_DP_N_R — R217 1K_4 — +1.05V_PCH

SM_DRAMRST# — AT30 CPU_DRAMRST#

SM_RCOMP[0] — BF44 SM_RCOMP_0 — R110 140/F_4
SM_RCOMP[1] — BF43 SM_RCOMP_1 — R111 25.5/F_4
SM_RCOMP[2] — BG43 SM_RCOMP_2 — R112 200/F_4

SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

PRDY# — N53
PREQ# — N55

TCK — L56 XDP_TCLK
TMS — L55 XDP_TMS
TRST# — J58 XDP_TRST#

TDI — M60 XDP_TDI
TDO — L59 XDP_TDO

DBR# — K58 XDP_DBRST# — R267 1K_4 — +3.3V_RUN

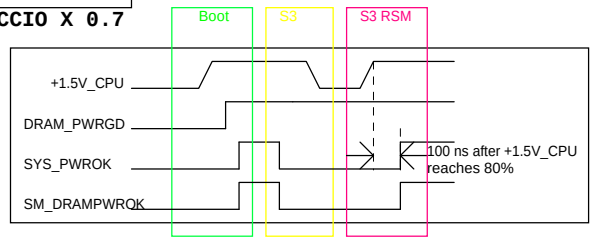
BPM#[0] — G58
BPM#[1] — E55
BPM#[2] — E59
BPM#[3] — G55
BPM#[4] — G59
BPM#[5] — H60
BPM#[6] — J59
BPM#[7] — J61

+1.05V_PCH

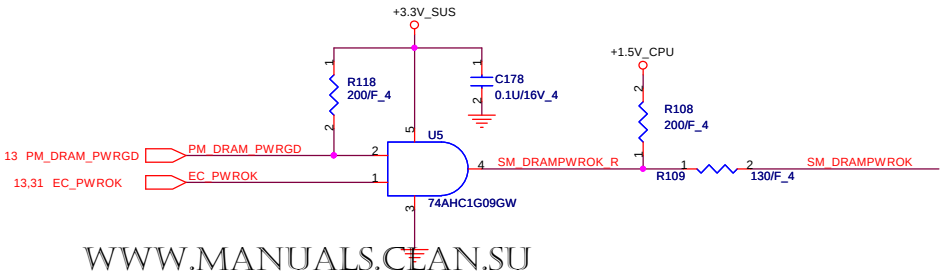
XDP_TMS — R268 *51_4_NC
XDP_TDI — R261 *51_4_NC
XDP_TDO — R262 *51_4_NC
IMVP7_PROCHOT# — R258 62_4

XDP_TCLK — R266 *51_4_NC
XDP_TRST# — R263 *51_4_NC

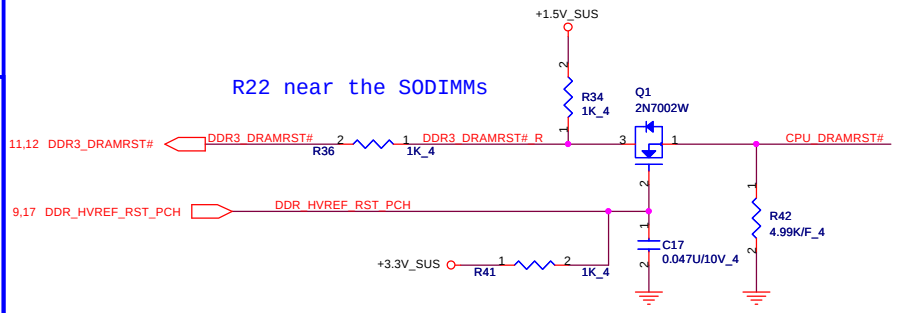
Intel spec VinH min =VCCIO X 0.7



Follow #DG1.0 436735 P105
DDR Power Gating Topology



Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration



Quanta Computer Inc.
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	Ivy Bridge 2/5	1A
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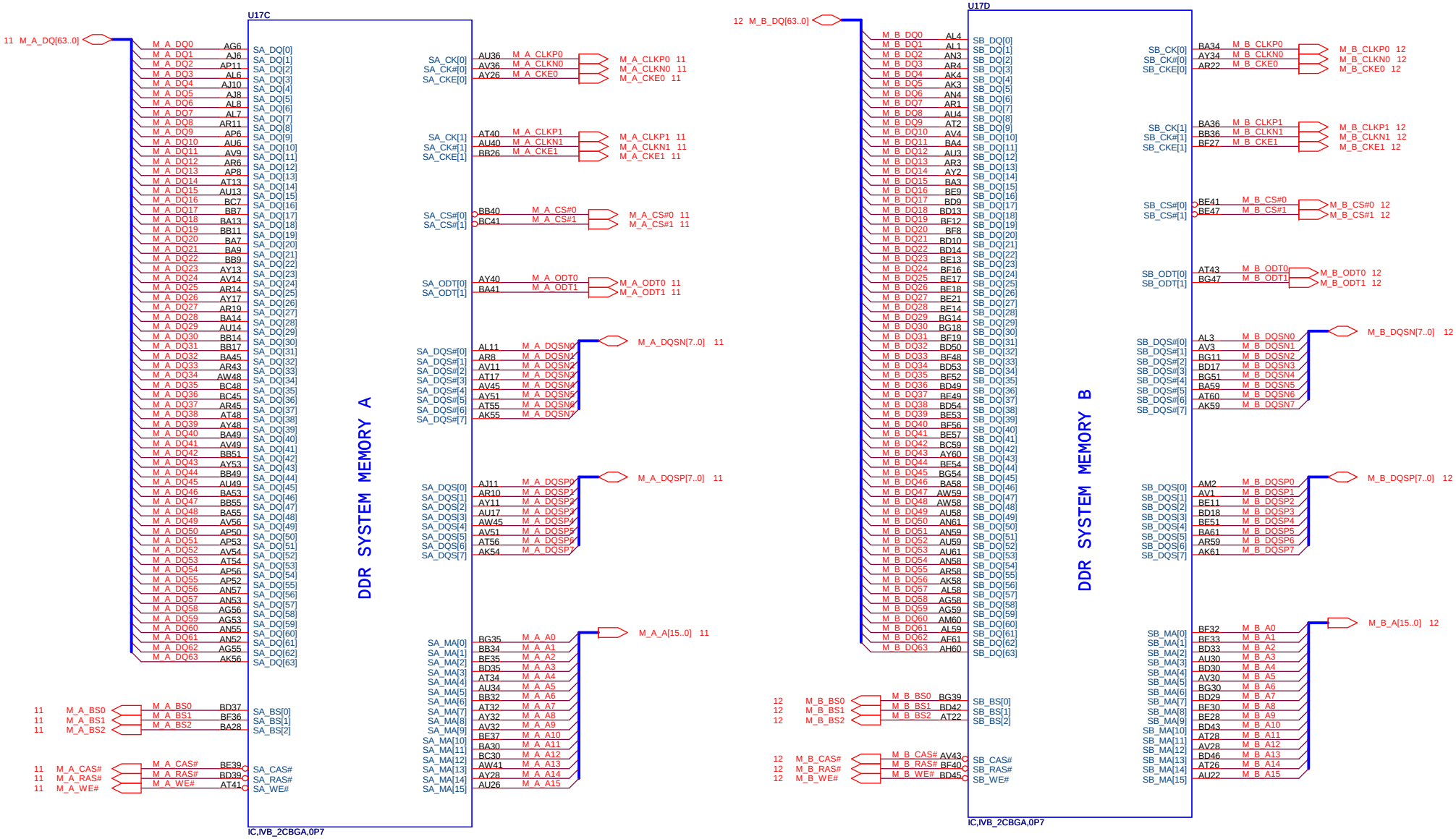
Ivy Bridge Processor (DDR3)



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Size	Document Number	Rev
	Ivy Bridge 3/5	1A

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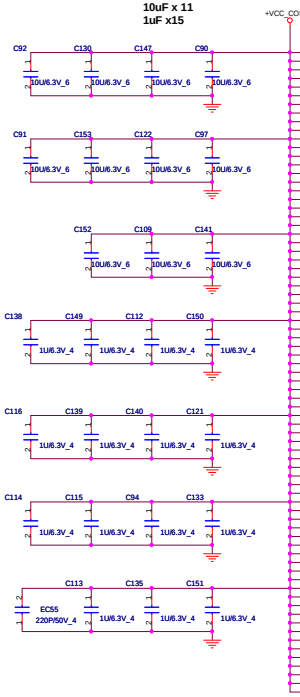
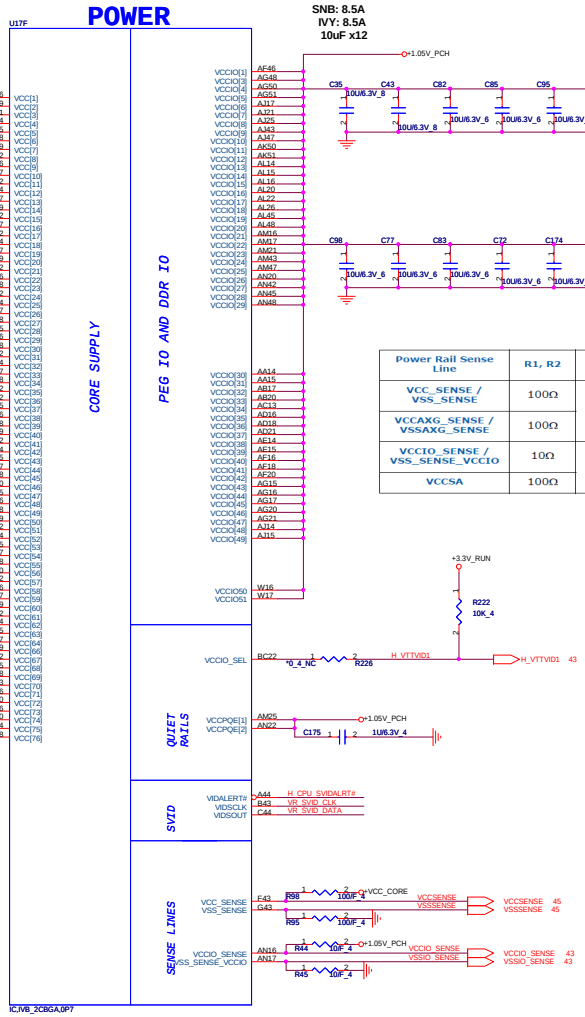
Ivy Bridge Processor

CPU Core Power

SNB: 33A
IVY: 33A
10uF x 11
1uF x15

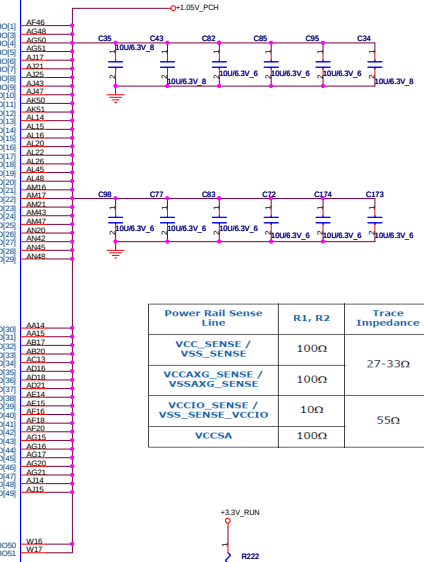


POWER



1.05V_PCH

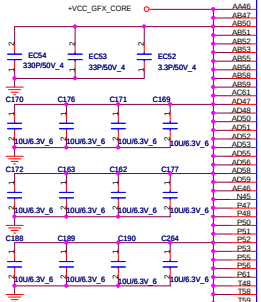
SNB: 8.5A
IVY: 8.5A
10uF x12



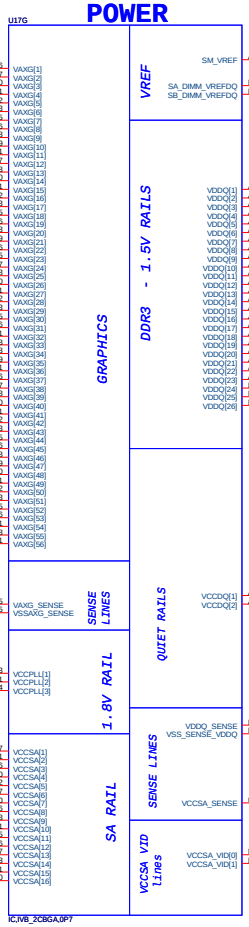
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

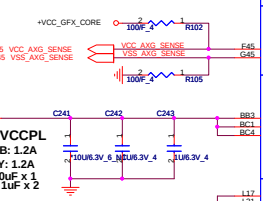
CPU VGT

SNB: 29A
IVY: 29A
10uF x 12



POWER



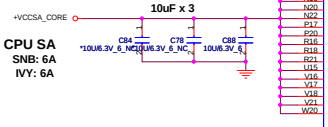


CPU VCCPL

SNB: 1.2A
IVY: 1.2A
10uF x 1
1uF x 2

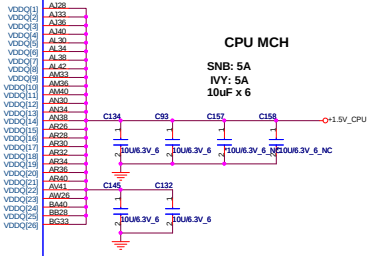
CPU SA

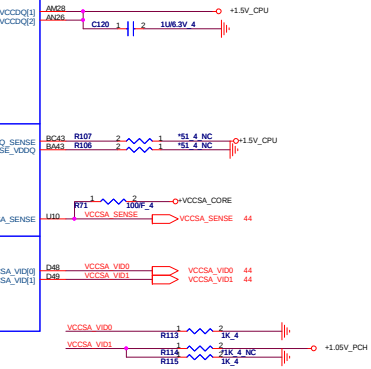
SNB: 6A
IVY: 6A



CPU MCH

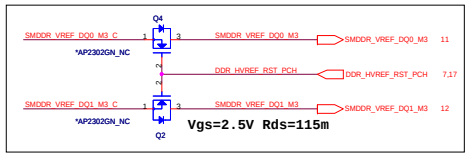
SNB: 5A
IVY: 5A
10uF x 6



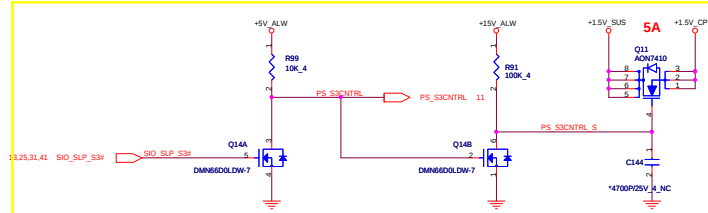


CAD Note: +VDDR_REF_CPU should have 10 mil trace width

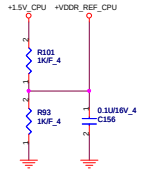
M3 VREF

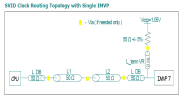


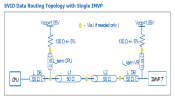
S3 Power reduce

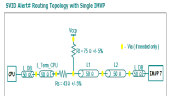


Take care Q3 Vgs(MAX)=2.5





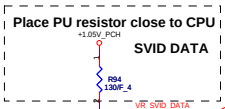




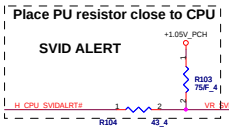
Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Place PU resistor close to CPU



Place PU resistor close to CPU



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Size	Document Number	Rev
	Ivy Bridge 4/5	1A
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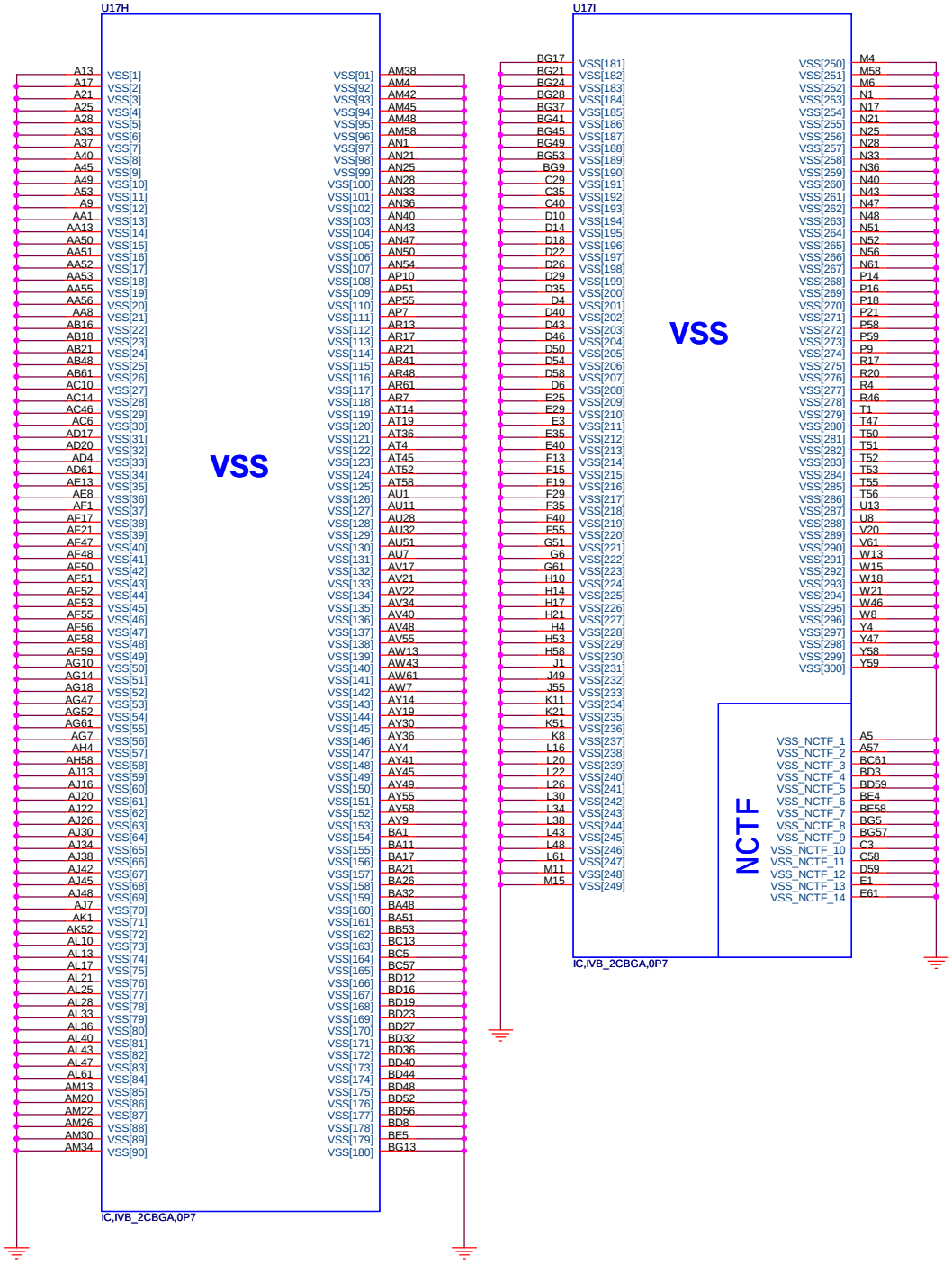
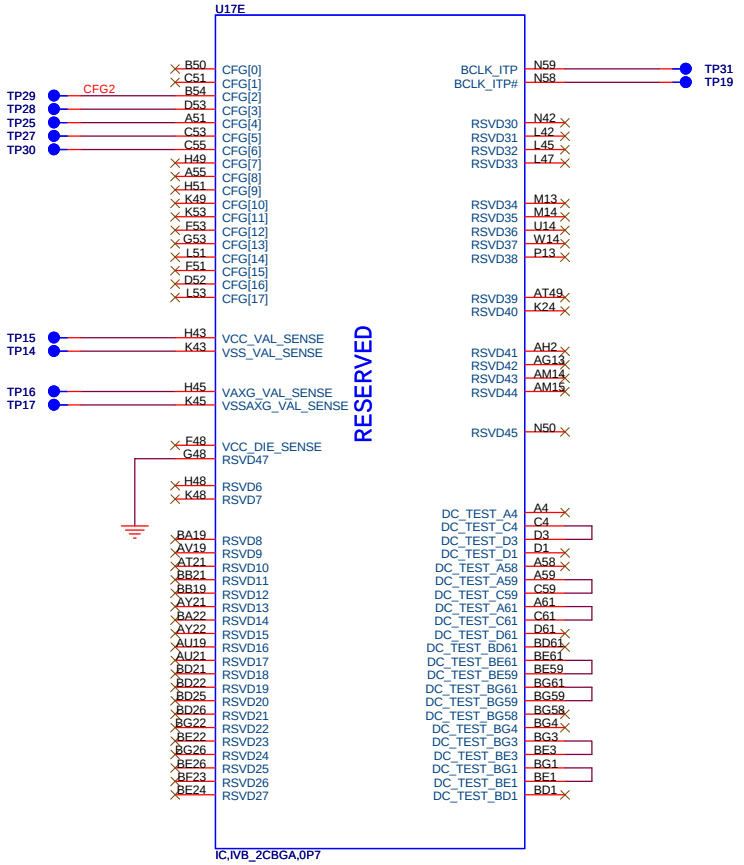
Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)



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	Ivy Bridge 5/5	1A
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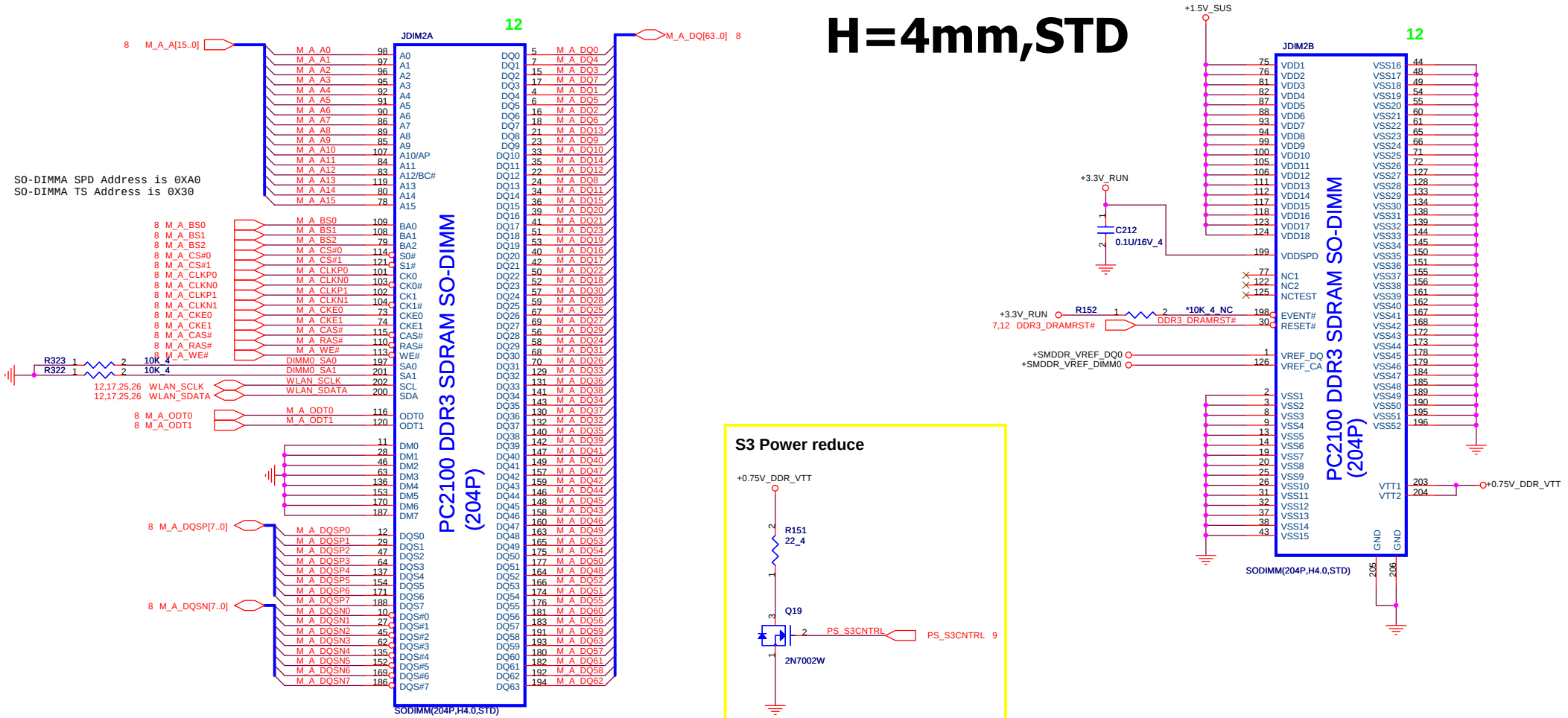
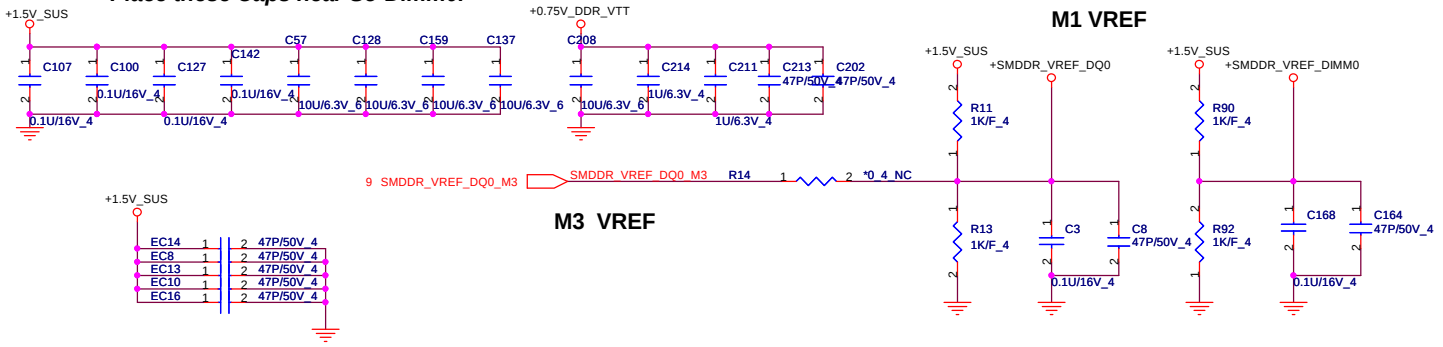
H=4mm,STD



M1 VREF

Place these Caps near So-Dimm0.



M3 VREF

Place these Caps near So-Dimm0.

Quanta Computer Inc.

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Size	Document Number	Rev
	DDR3 DIMM-0	1A

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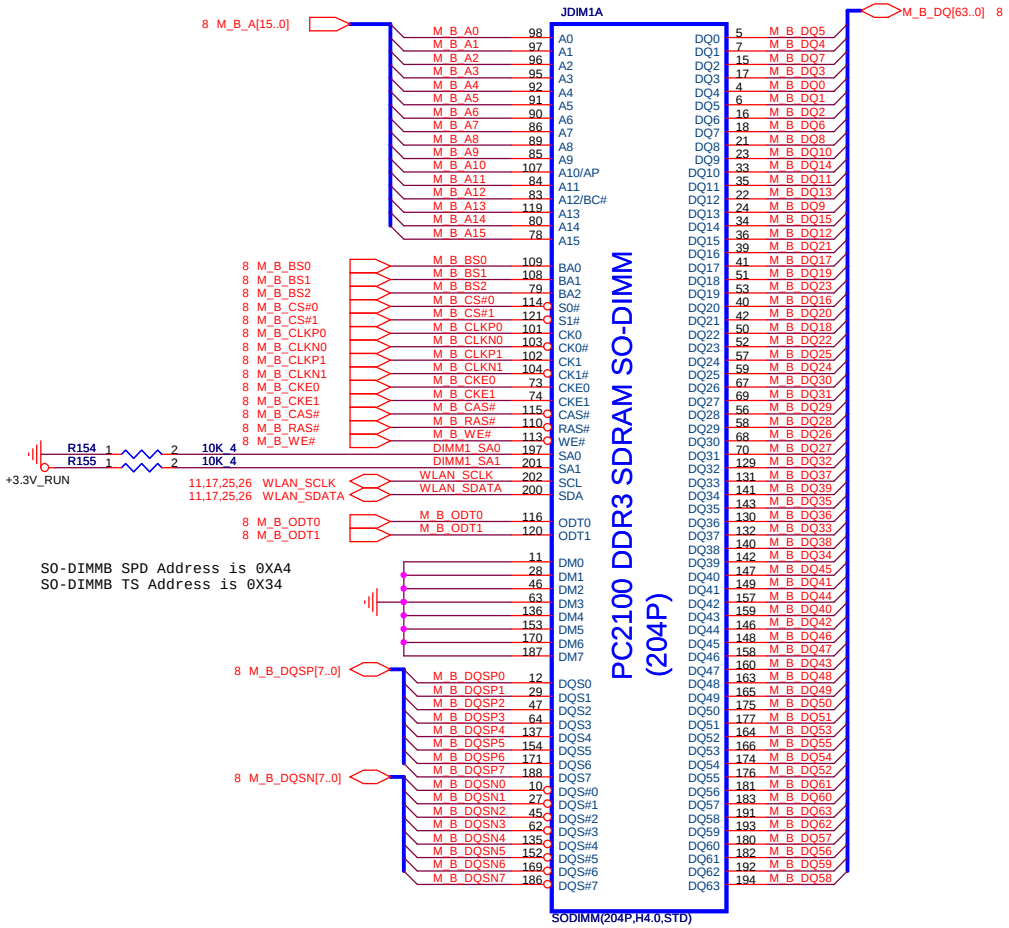
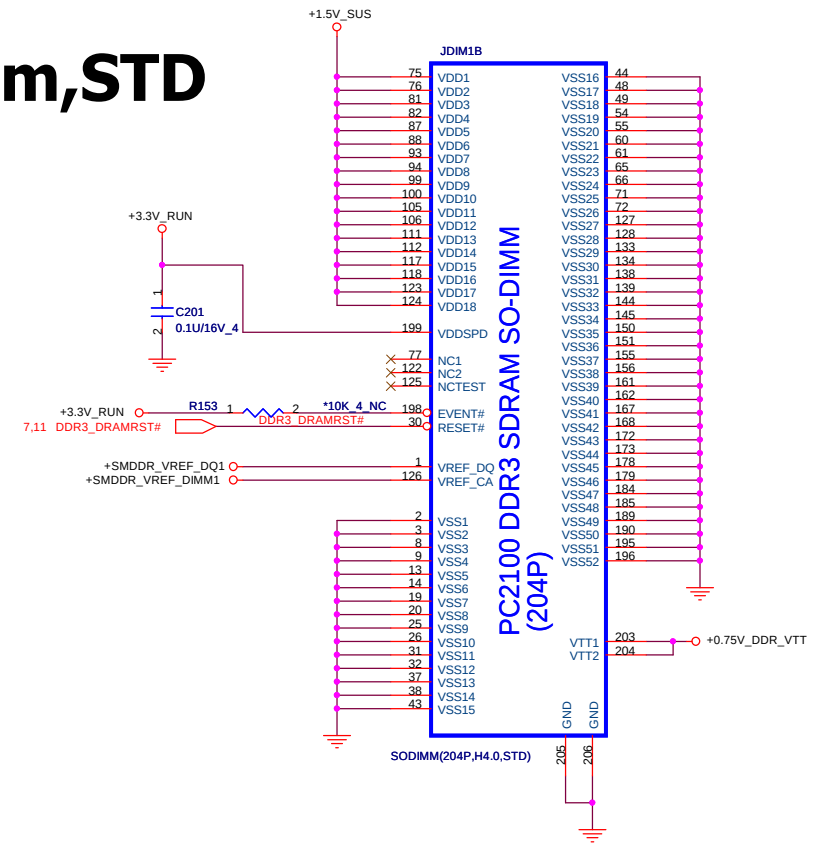
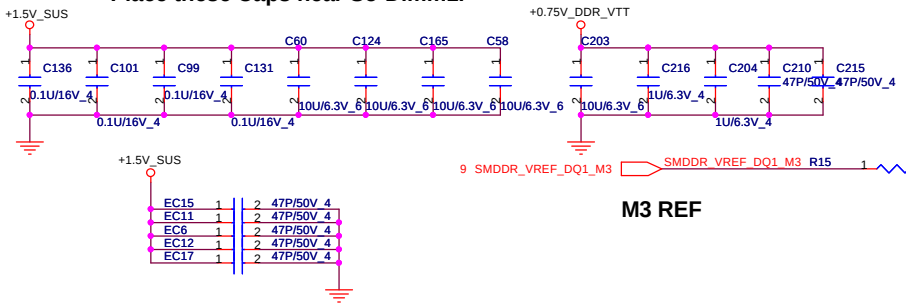
H=4mm,STD



SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34



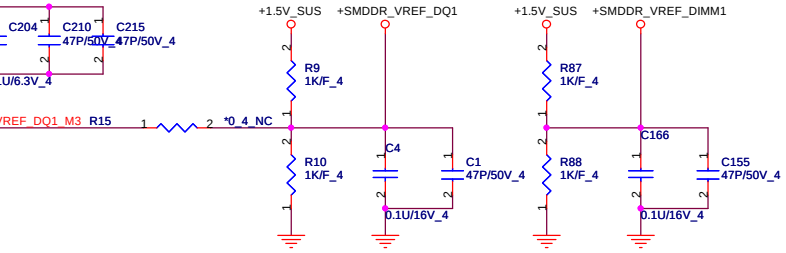
Place these Caps near So-Dimm1.



Place these Caps near So-Dimm0.

M1 VREF

M3 REF



Quanta Computer Inc.
PROJECT : V07

Size	Document Number	Rev
	DDR3 DIMM-1	1A

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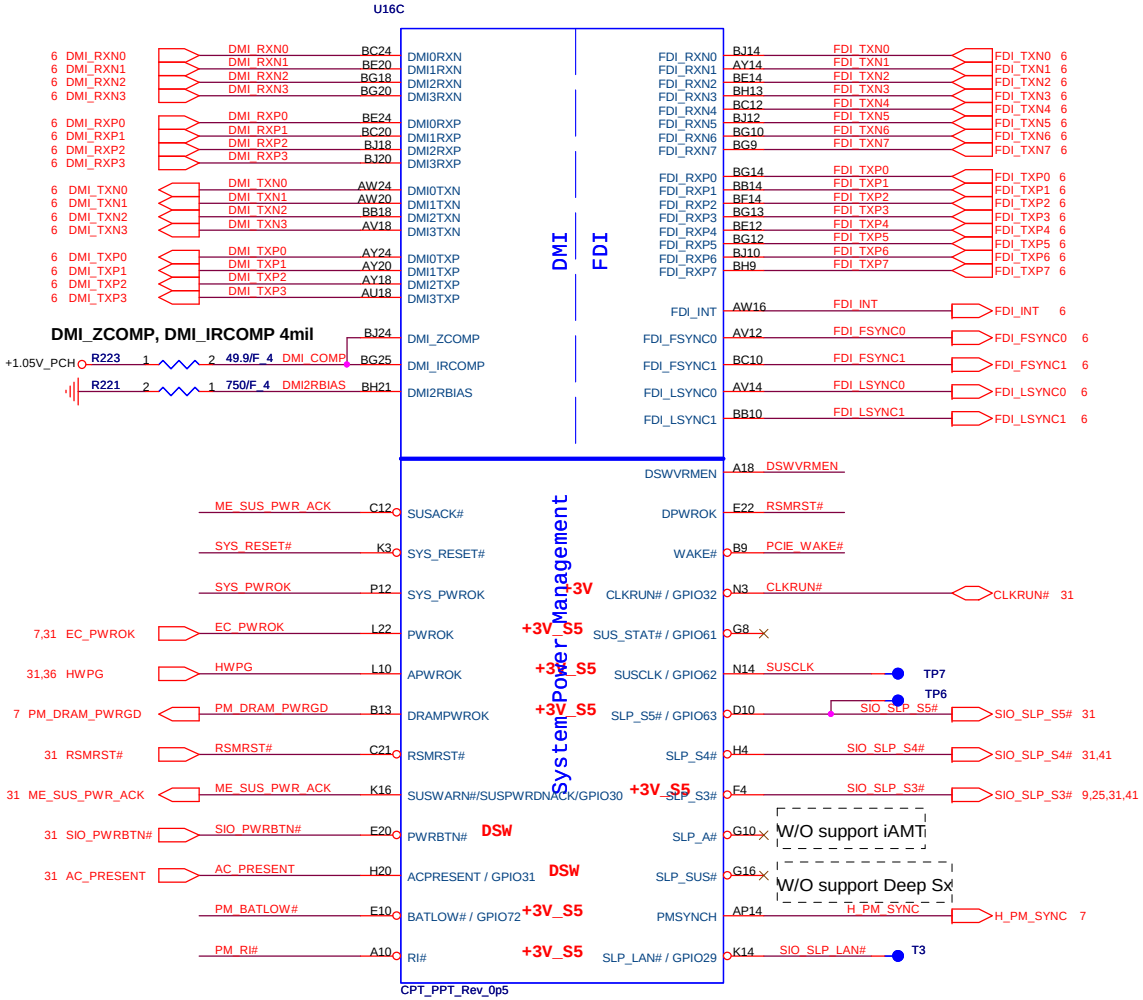
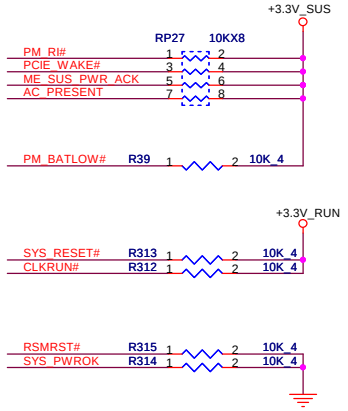
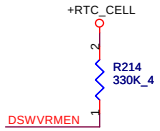
Cougar Point/Panther Point (DMI,FDI,PM)

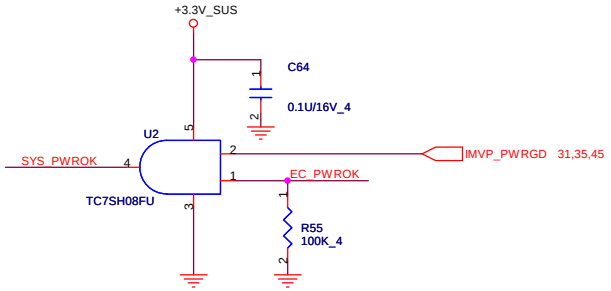


PCH Pull-high/low(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable



Quanta Computer Inc.
PROJECT : V07

Size	Document Number	Rev
	Panther Point 1/7	1A
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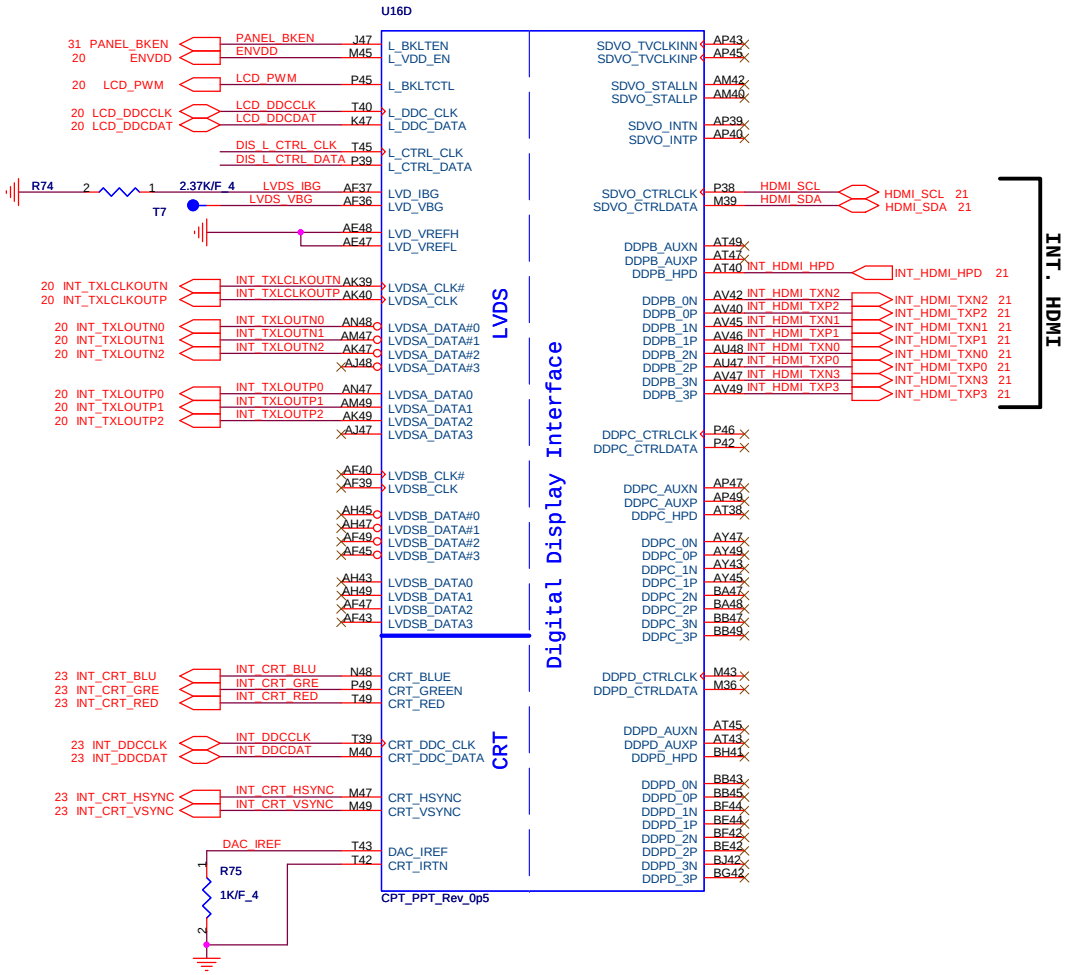
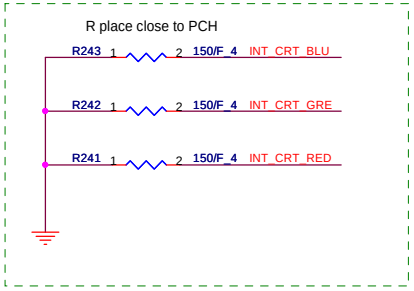
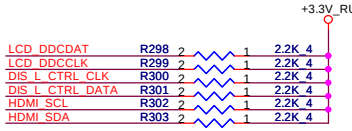
Cougar Point/Panther Point (LVDS,DDI)



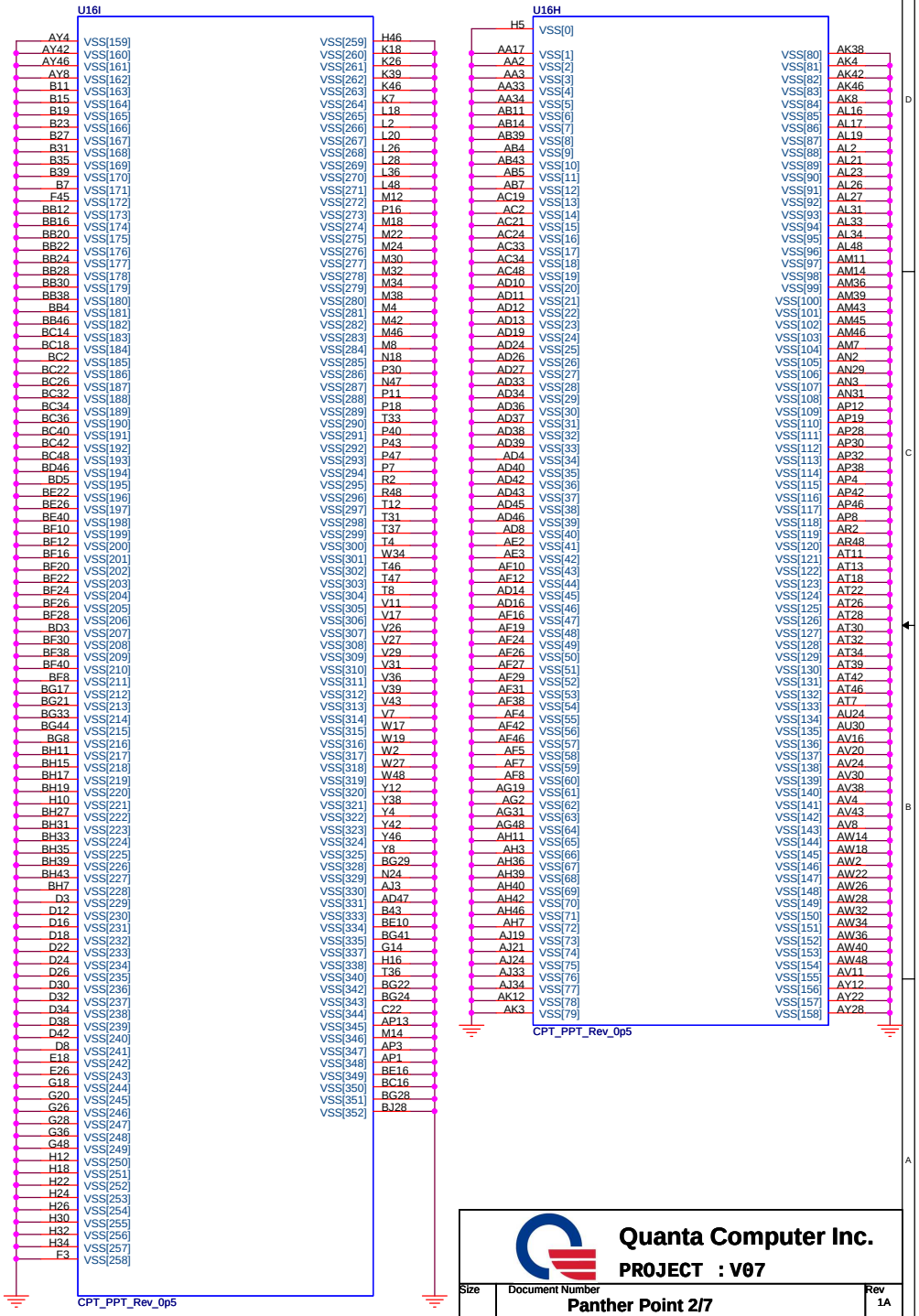
R place close to PCH





BOM setup	Vostro	Inspiron
R241,R242,R243	POP	NC

Cougar Point/Panther Point (GND)



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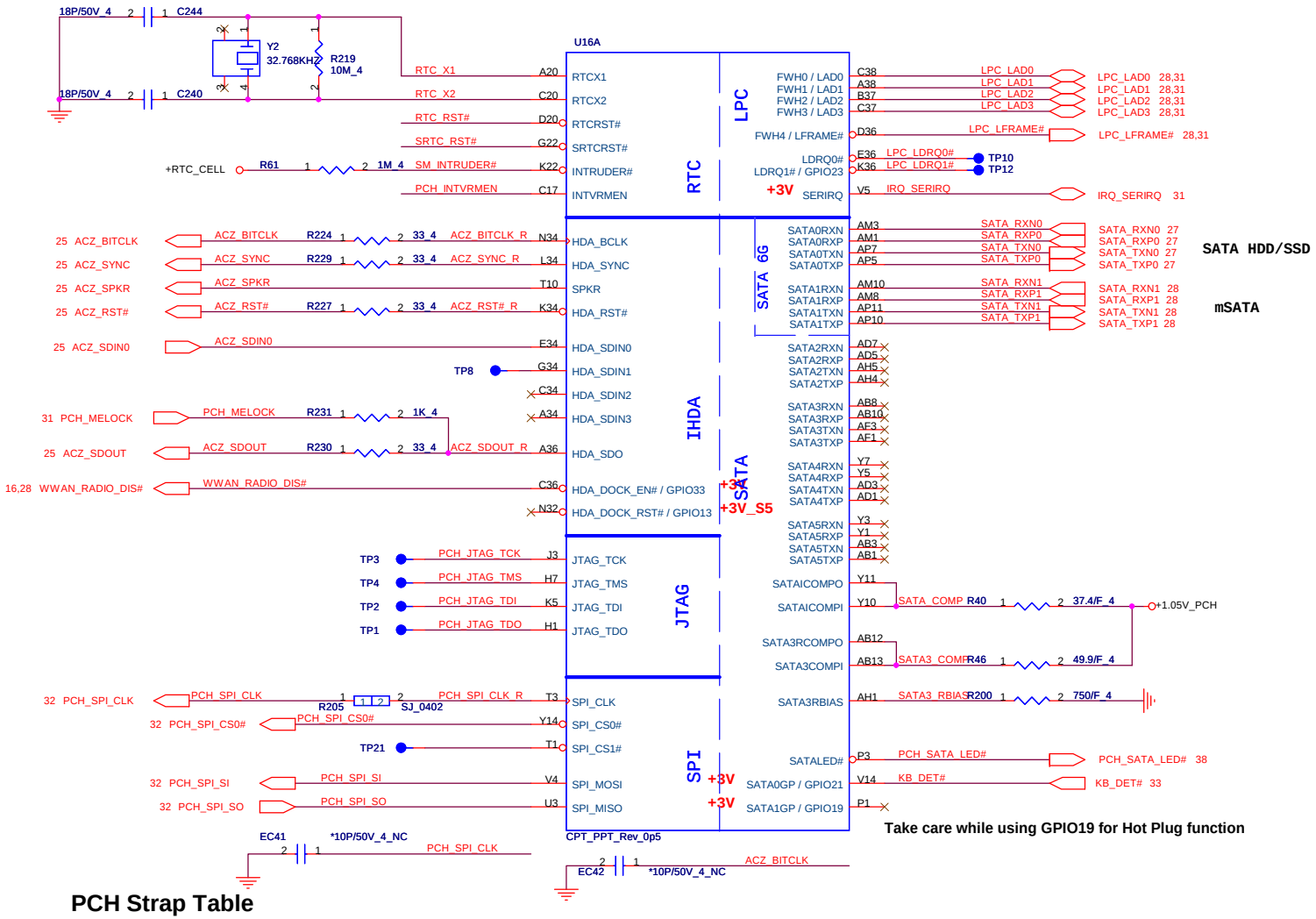
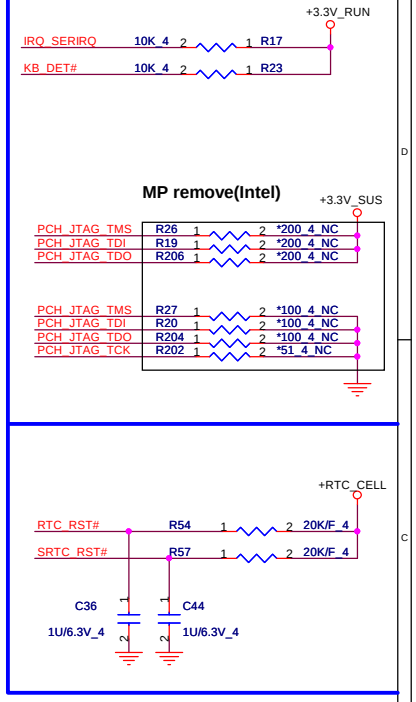
Cougar Point/Panther Point (HDA,JTAG,SATA)





PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R215 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R67 1K_4 ACZ_SYNC_R

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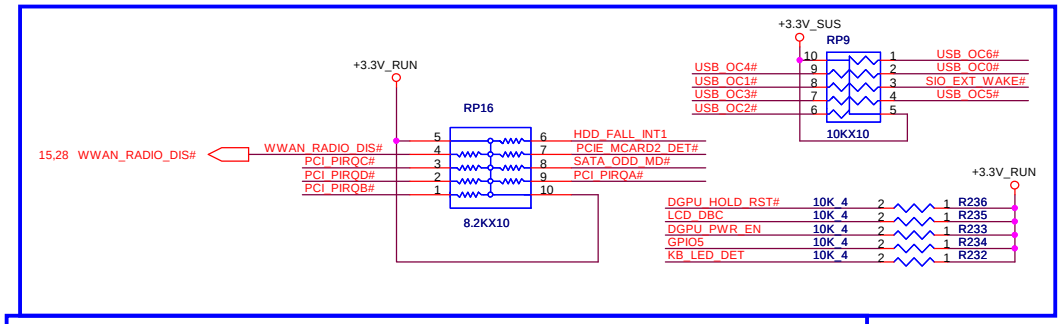
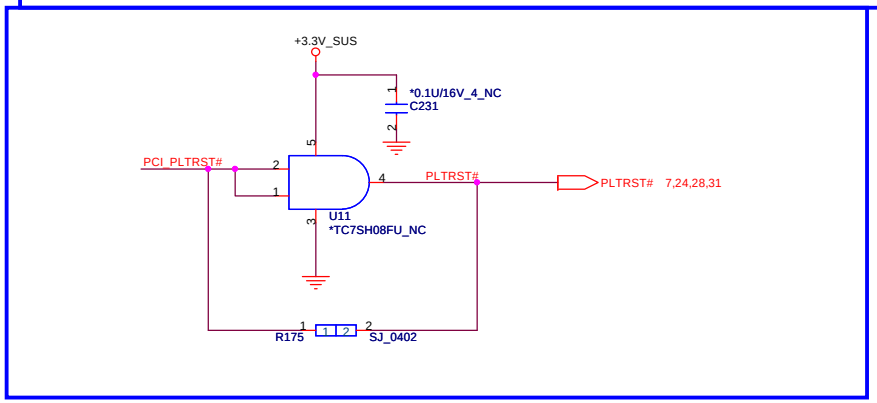
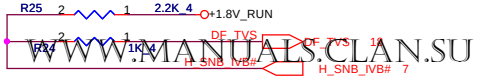
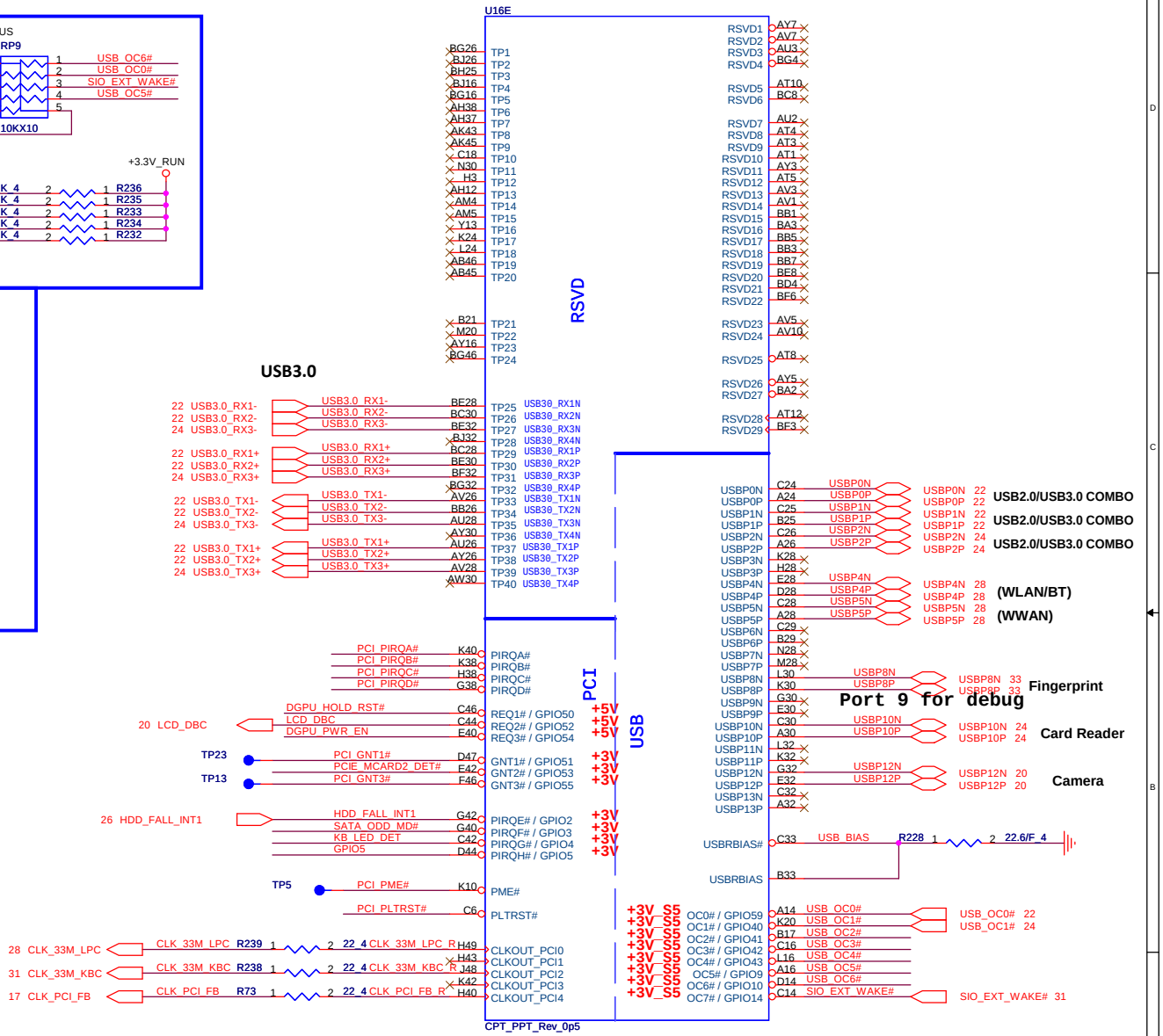
Cougar Point-M/Panther Point (PCI,USB,NVRAM)

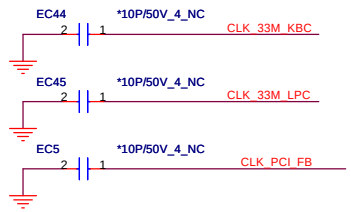


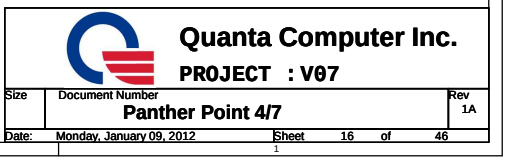


Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
			Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm









U16B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic ‘0’
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic ‘0’
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode

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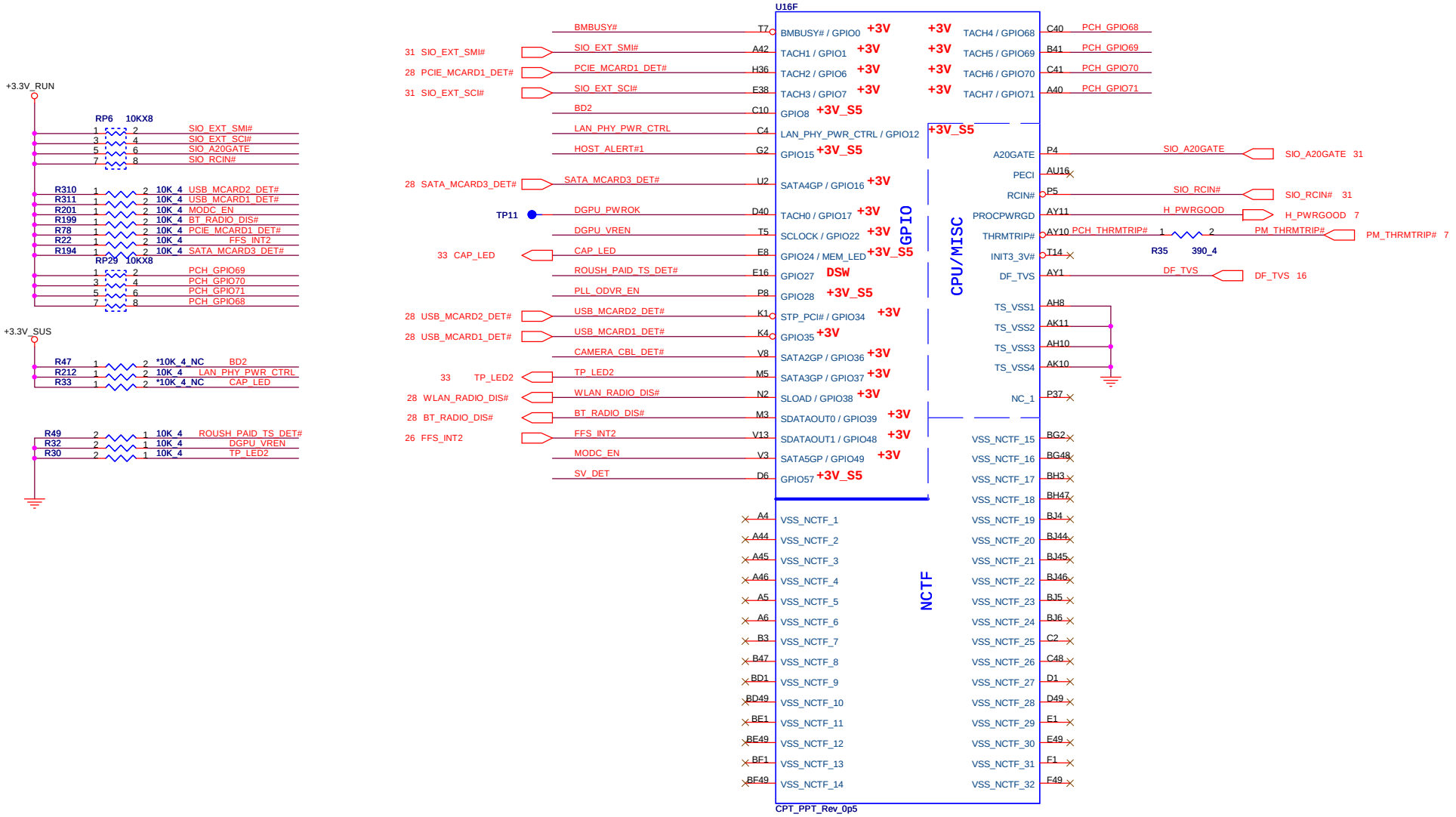
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

R43 1 2 *1K_4_NC PLL_ODVR_EN

CAMERA_CBL_DET# R18 1 2 10K_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO

BMBUSY# R3 1 2 10K_4 +3.3V_RUN

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

HOST_ALERT#1 R195 1 2 1K_4 +3.3V_SUS

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

+3.3V_SUS R28 1 2 10K_4 SV_DET

MFG-TEST

WLAN_RADIO_DIS# R2 1 2 10K_4 +3.3V_RUN

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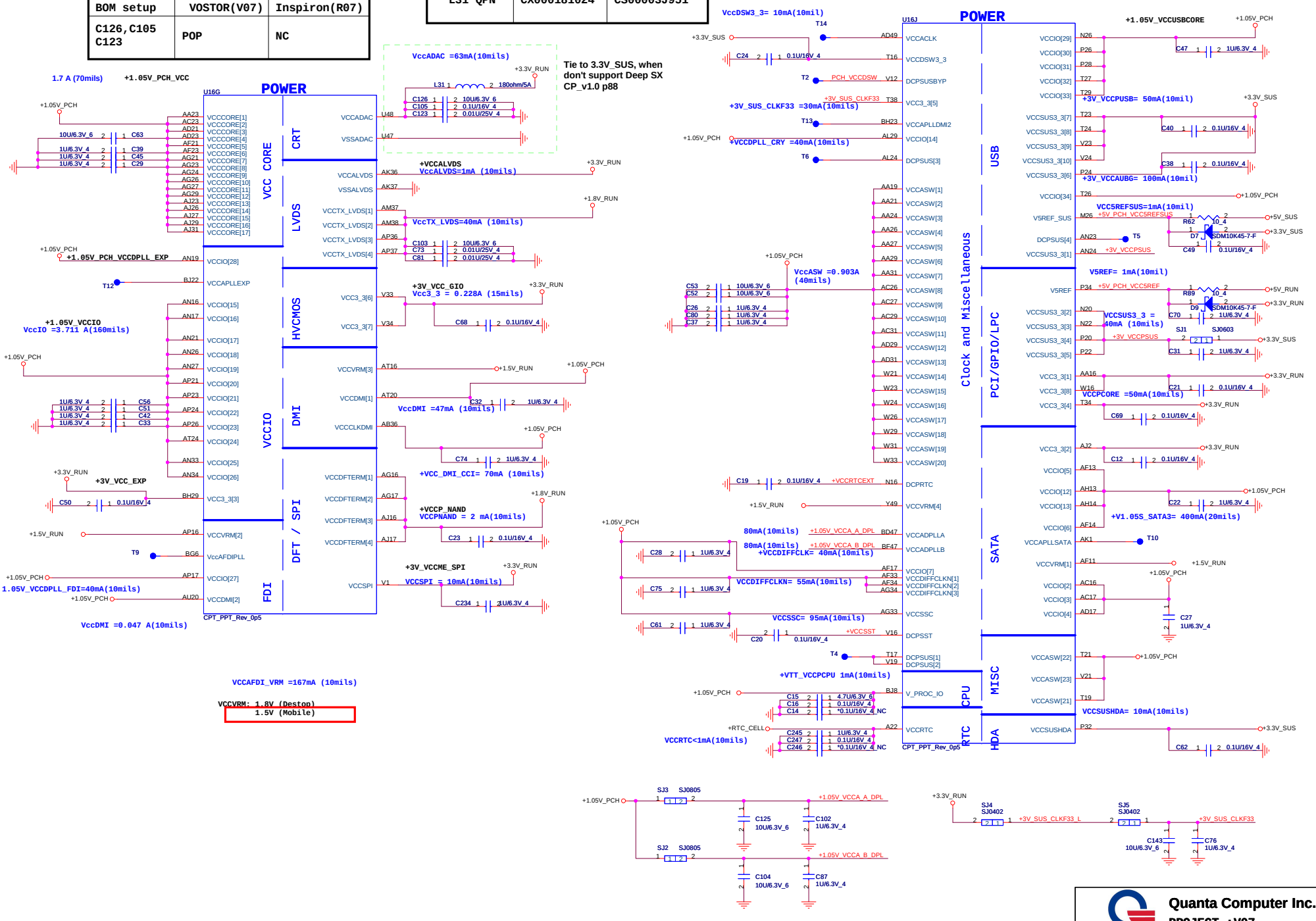
Cougar Point/Panther Point (POWER)

BOM setup	VOSTOR(V07)	Inspiron(R07)
C126,C105 C123	POP	NC

BOM setup	VOSTOR(V07)	Inspiron(R07)
L31 QPN	CX000181024	CS00003J951

Cougar Point/Panther Point (POWER)



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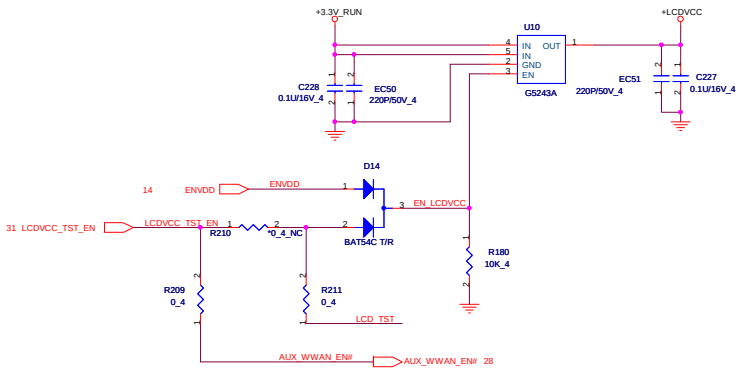
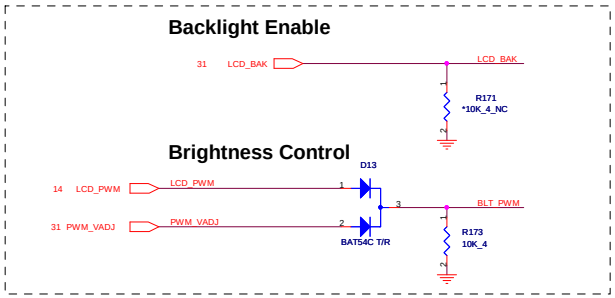
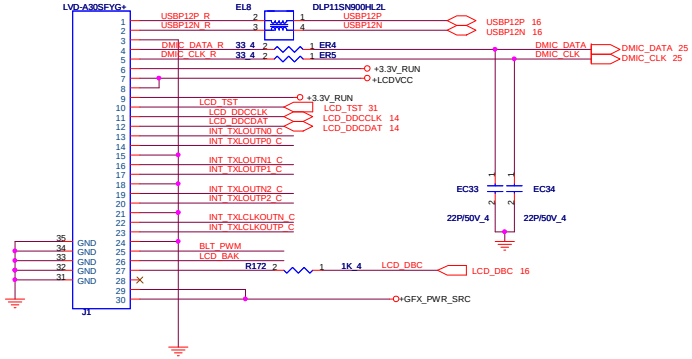
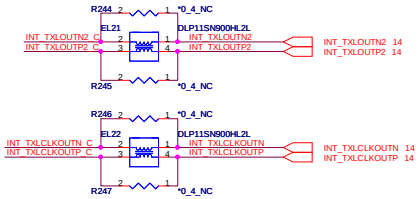
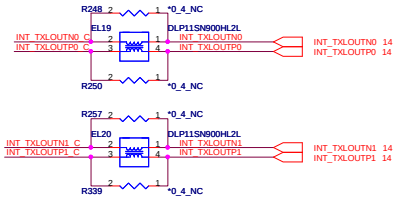
Flow PDC connector PN

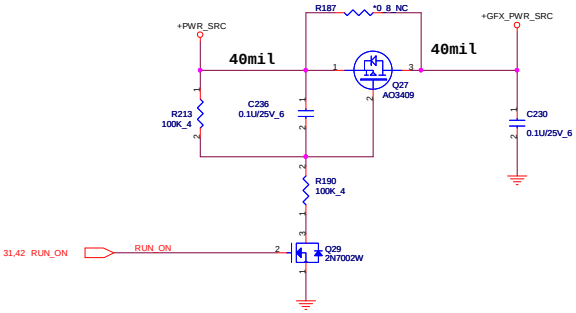












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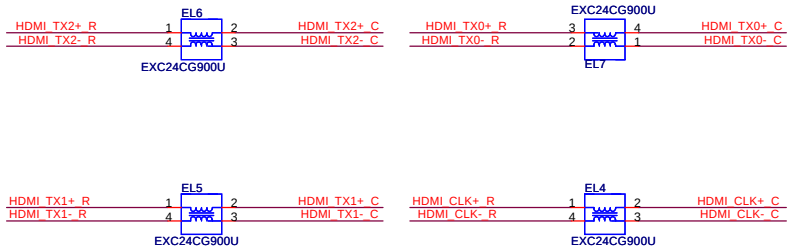
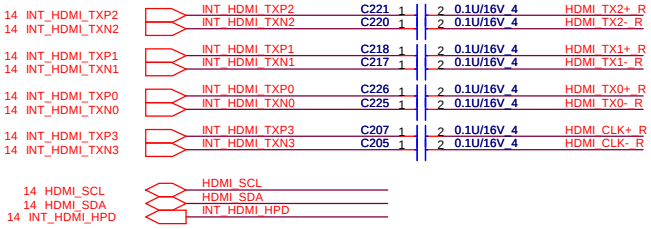
Reserve for EMI and close to HDMI CONN

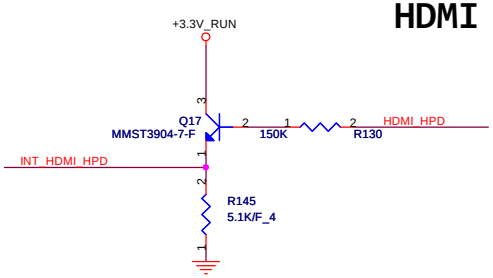


INT HDMI

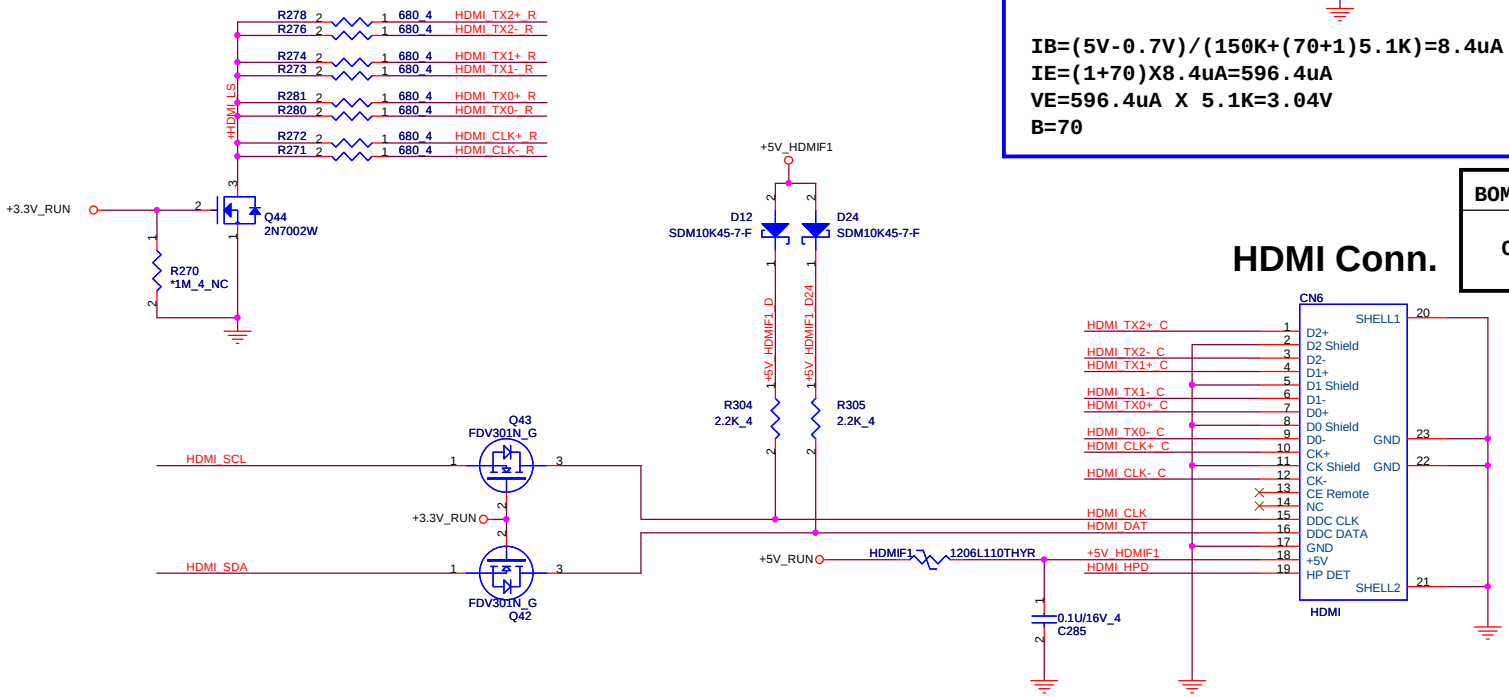


HDMI_HPD spec VinH_min=2.0V

HDMI HPD



IB=(5V-0.7V)/(150K+(70+1)5.1K)=8.4uA
IE=(1+70)X8.4uA=596.4uA
VE=596.4uA X 5.1K=3.04V
B=70



HDMI Conn.

BOM setup	VOSTOR(V07)	Inspiron(R07)
CN6 QPN	DFHS19FR067	DFHS19FR066

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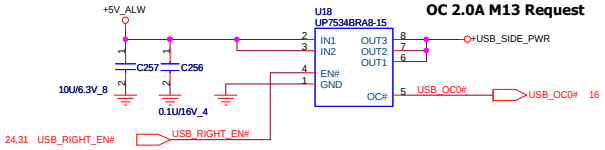
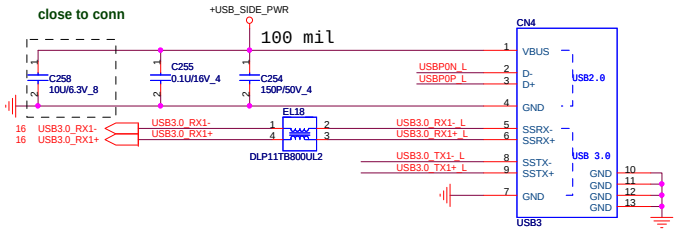
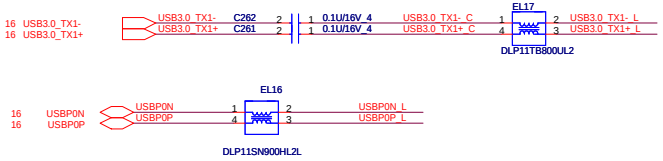
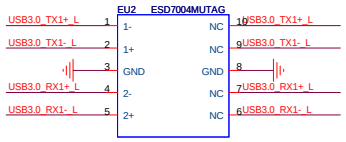
USB3.0 x2 (x1 with powershare)

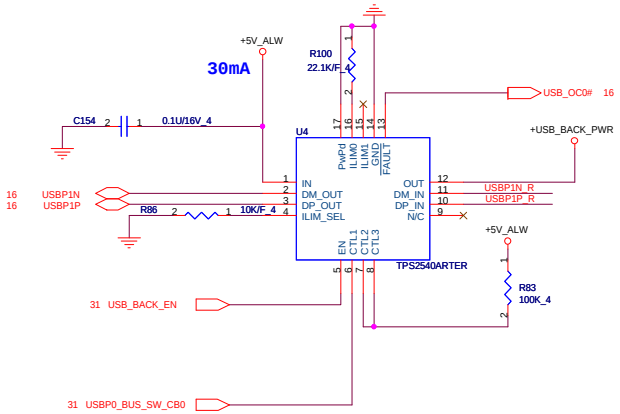


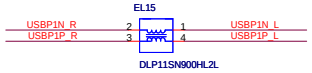






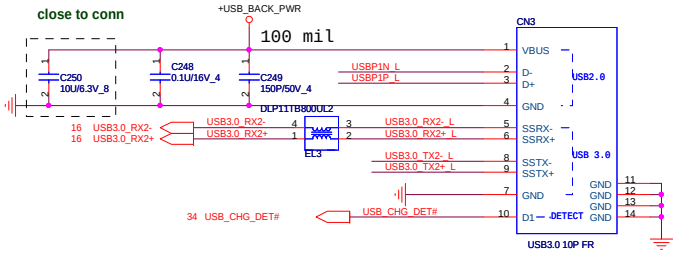
S3/S5 USB charging circuit

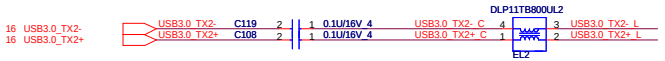




USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

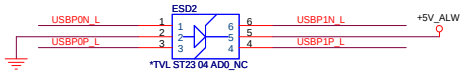
	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

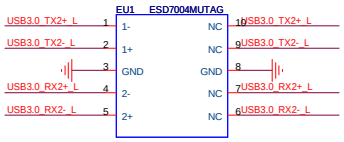




ESD Function

Place ESD diodes as close as USB connector.





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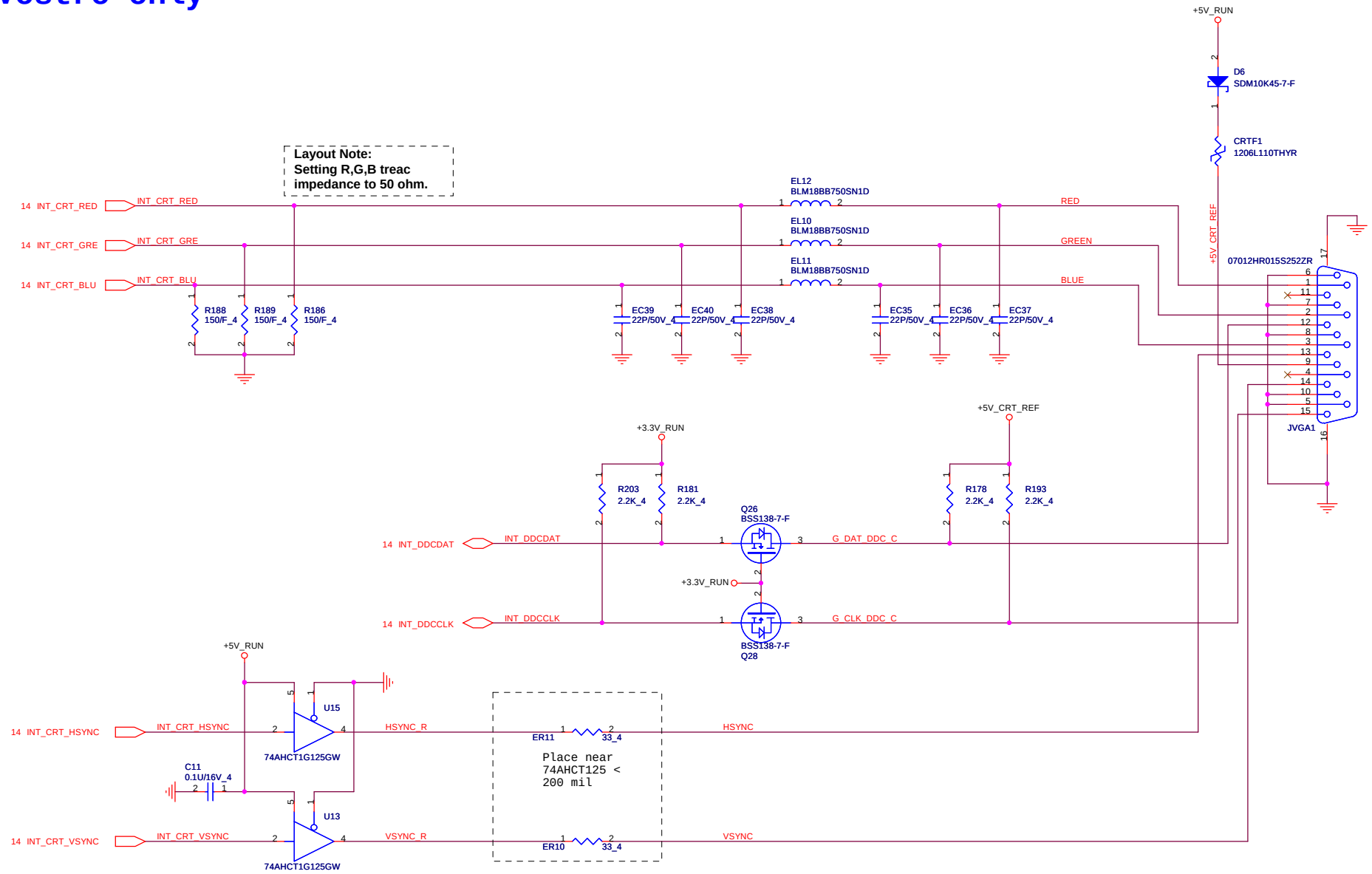
Vostro only



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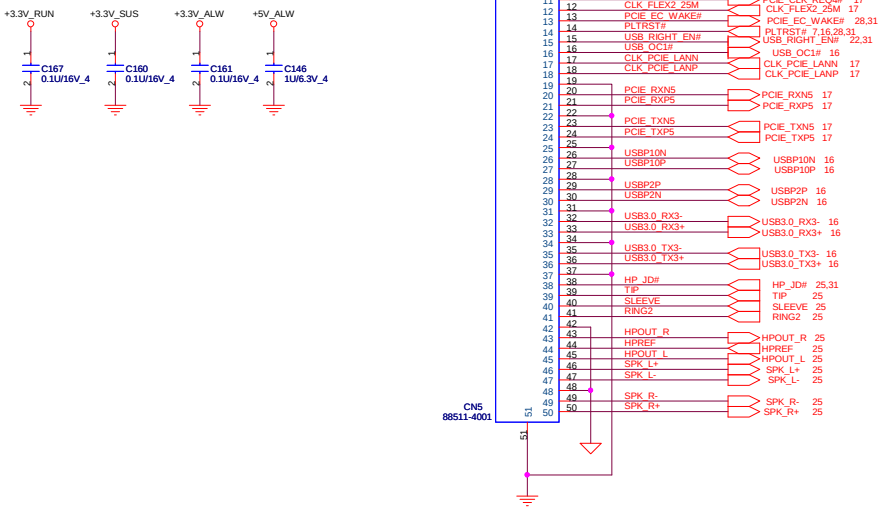

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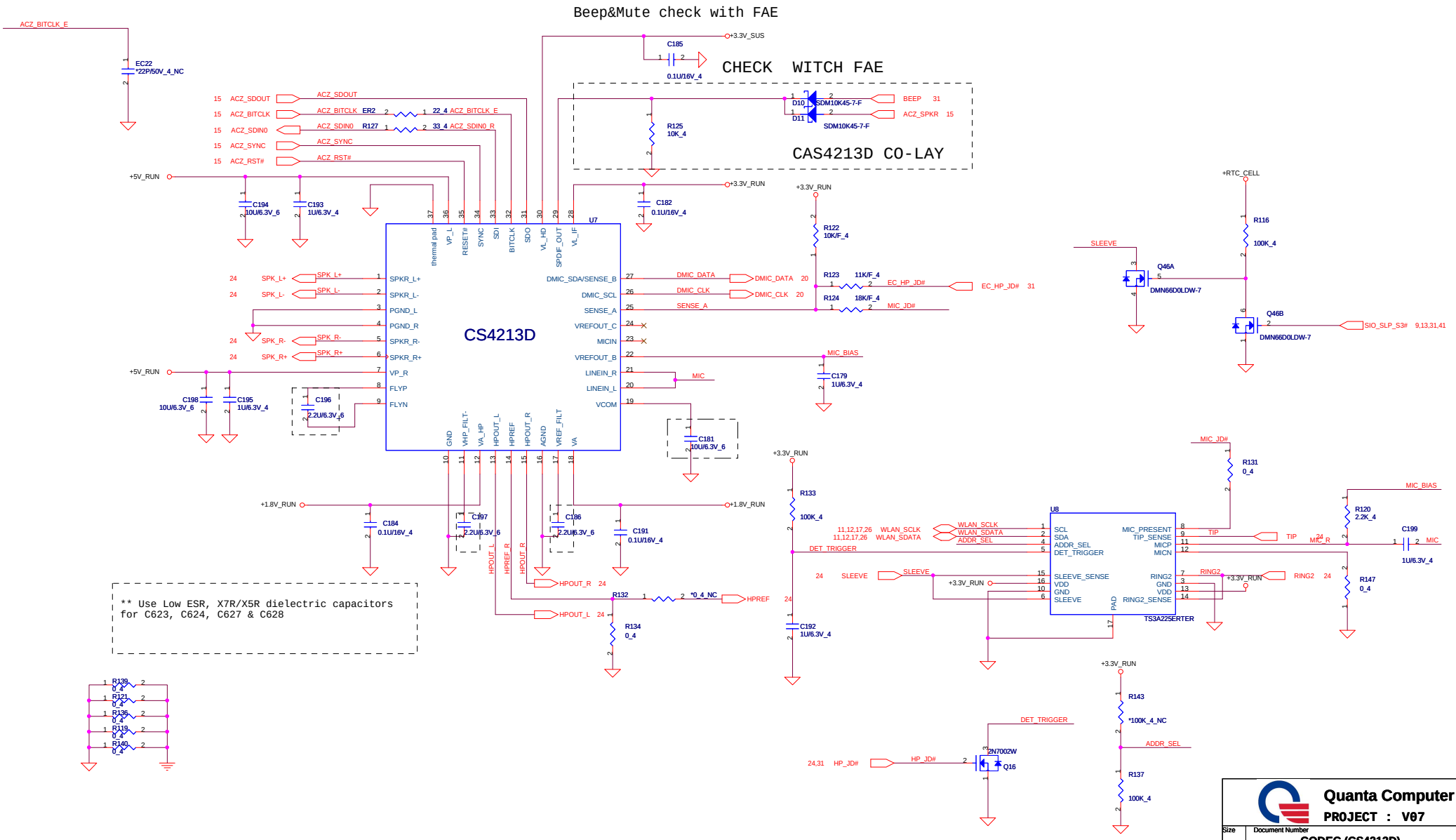
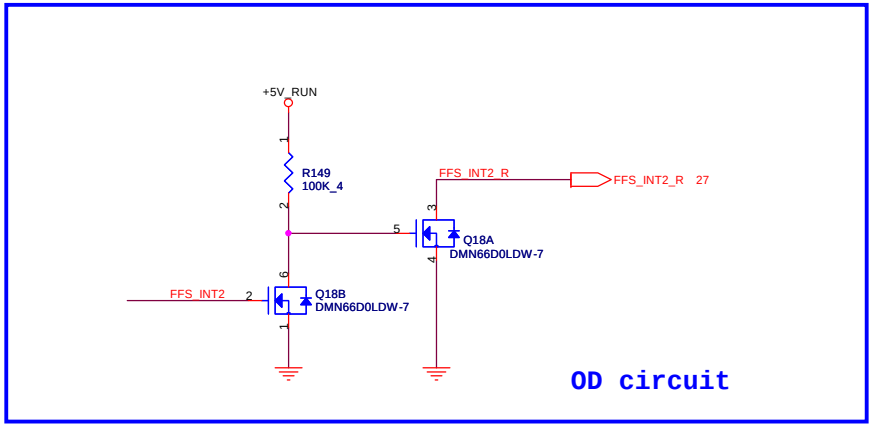
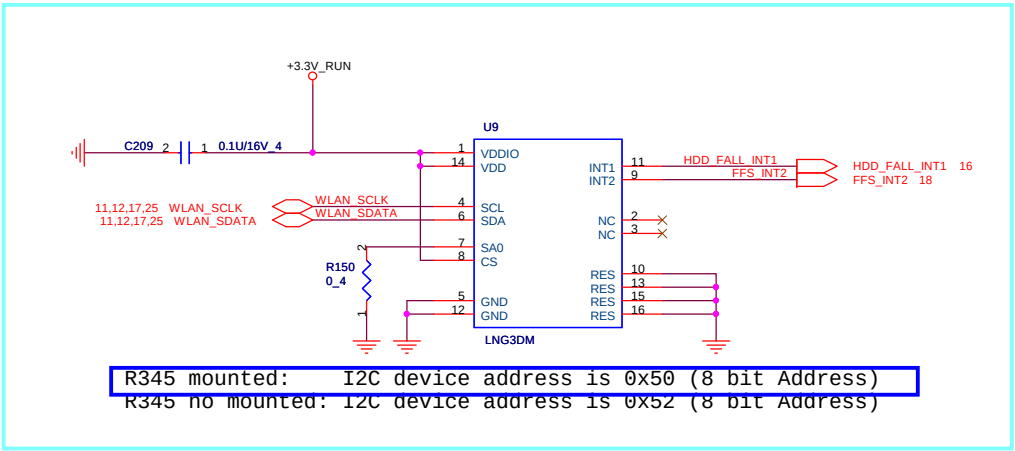


3-axis Fall Sensor

Vostro only

If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit





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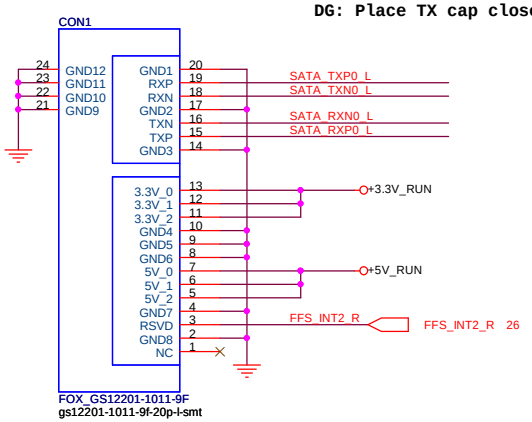
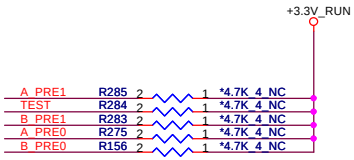
HDD

DG: Place TX cap close to connector

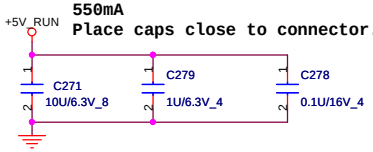


A_PRE0	A_PRE1	SATA TX Emphasis
0	0	0db
0	1	1.5db
1	0	2.5db
1	1	3db

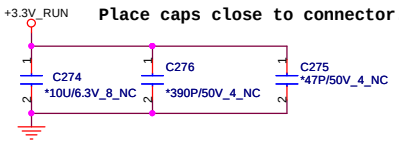
B_PRE0	B_PRE1	SATA RX Emphasis
0	0	0db
0	1	1.5db
1	0	2.5db
1	1	3db

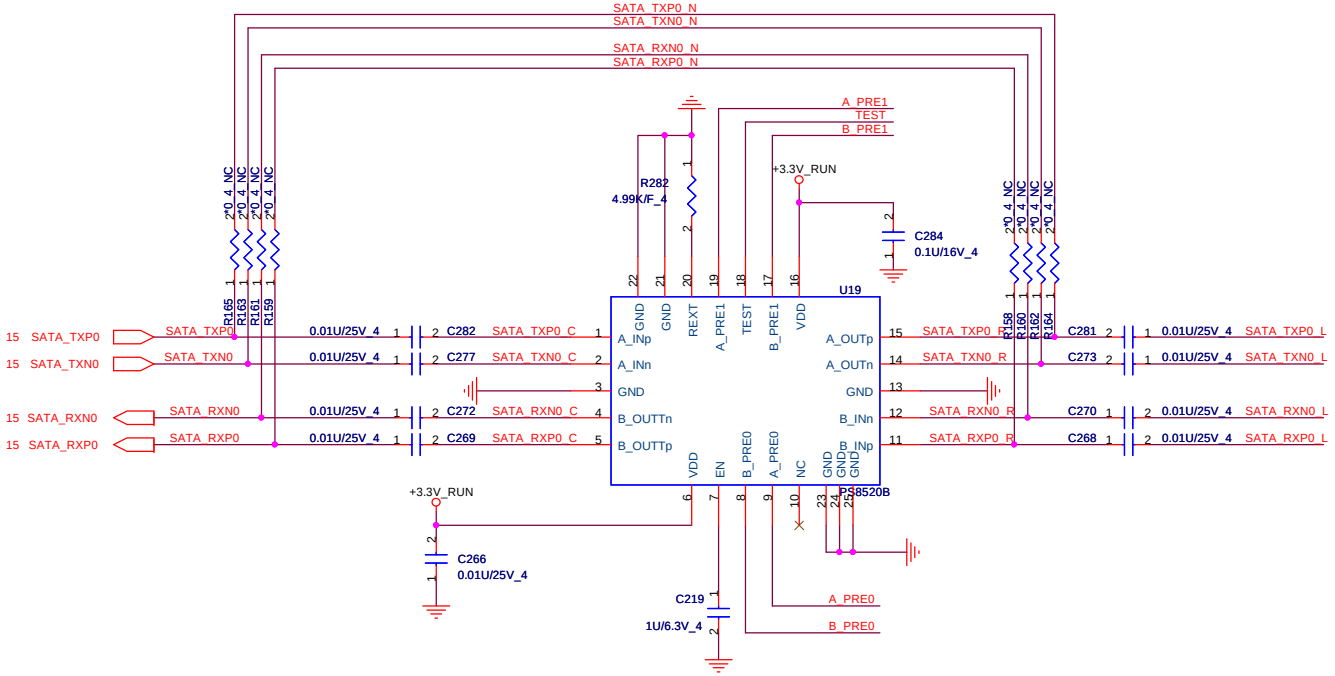


550mA
Place caps close to connector.



Place caps close to connector.





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	SATA HDD/ODD	1A

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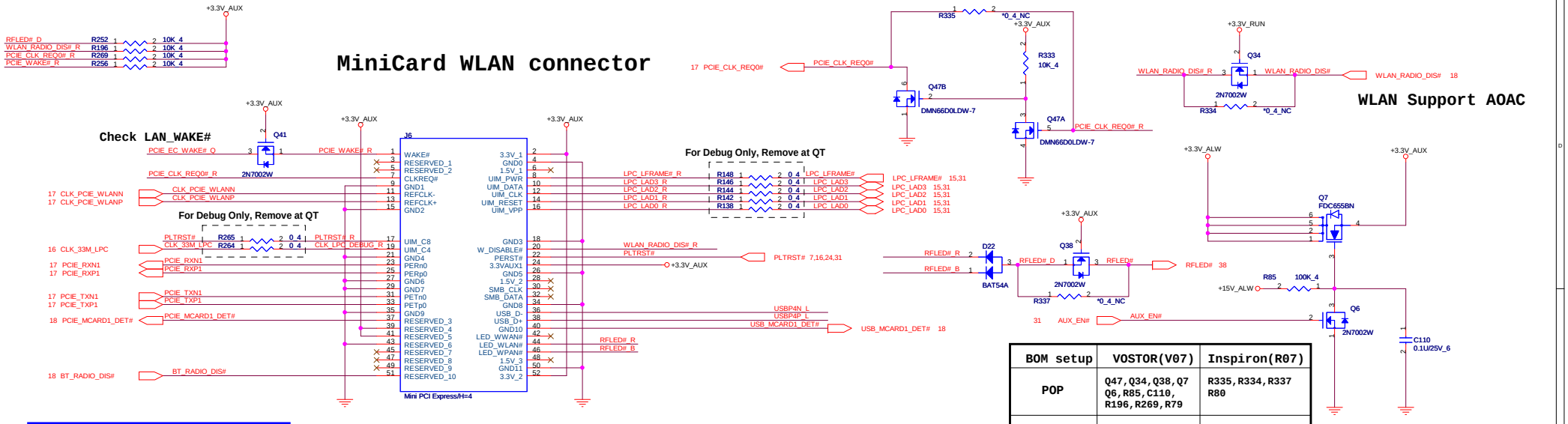
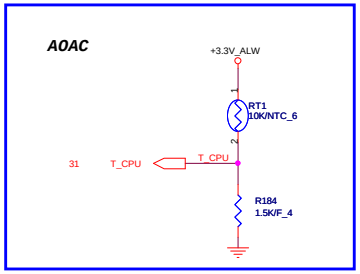
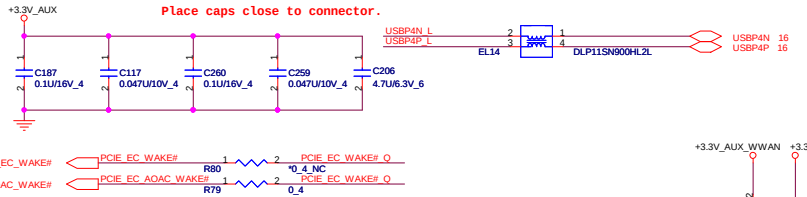
MiniCard WLAN connector

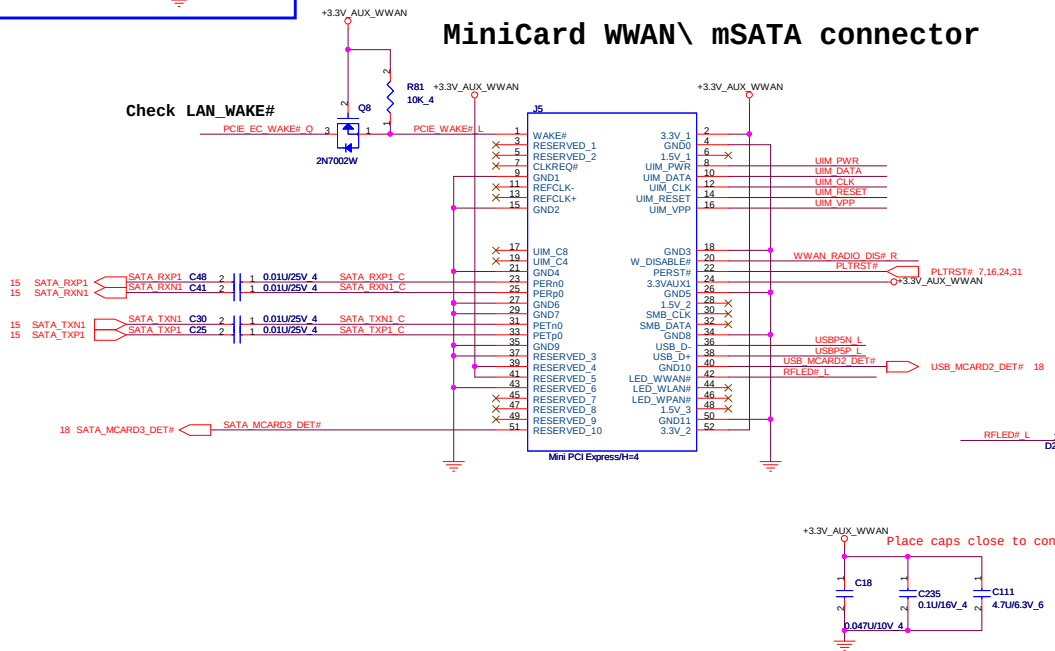


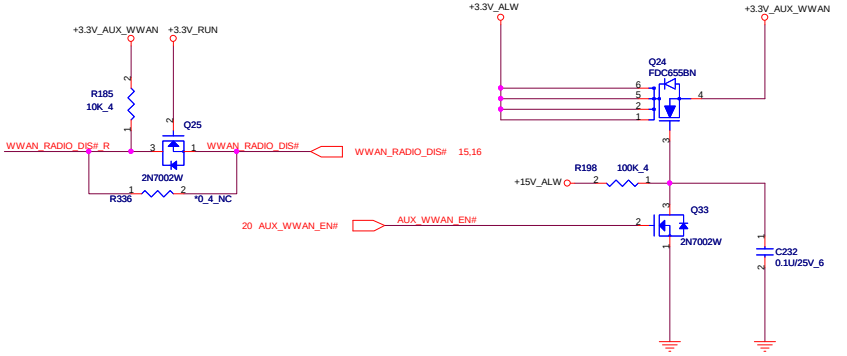
BOM setup	VOSTOR(V07)	Inspiron(R07)
POP	Q47,Q34,Q38,Q7 Q6,R85,C110, R196,R269,R79	R335,R334,R337 R80
NC	R335,R334,R337 R80	Q47,Q34,Q38,Q7 Q6,R85,C110,R196 R269,R79



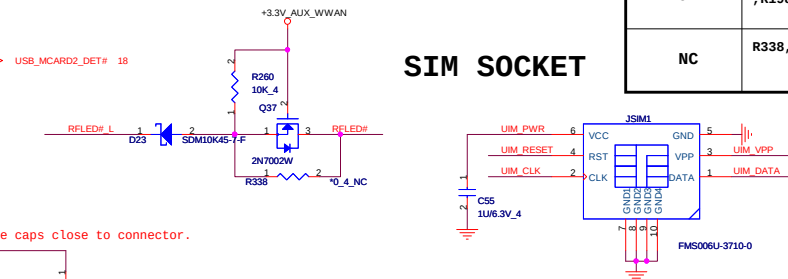


MiniCard WWAN\ mSATA connector

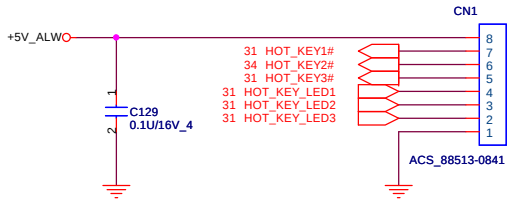




BOM setup	VOSTOR(V07)	Inspiron(R07)
POP	Q37,Q25,Q24,Q33 ,R198,C232,R185	R338,R336
NC	R338,R336	Q37,Q25,Q24,Q33 ,R198,C232,R185



Quanta Computer Inc.
PROJECT : V07
Size | Document Number: WLAN/WWAN | Rev 3A
Date: Monday, January 09, 2012 | Sheet 28 of 46



HOTKEY CON

Quanta Computer Inc.		
PROJECT : V07		
Size	Document Number	Rev 1A
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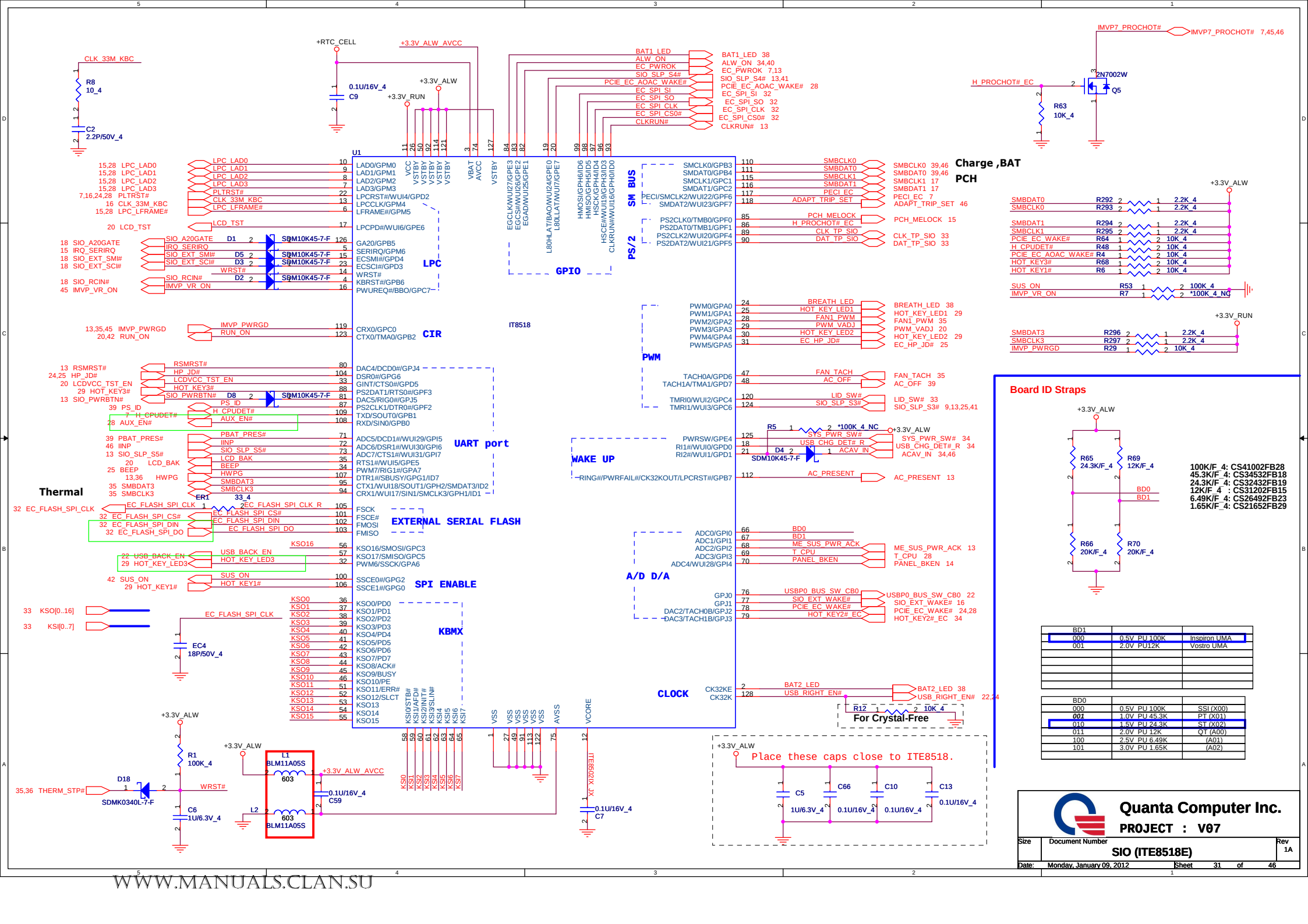
Quanta Computer Inc.

PROJECT : V07

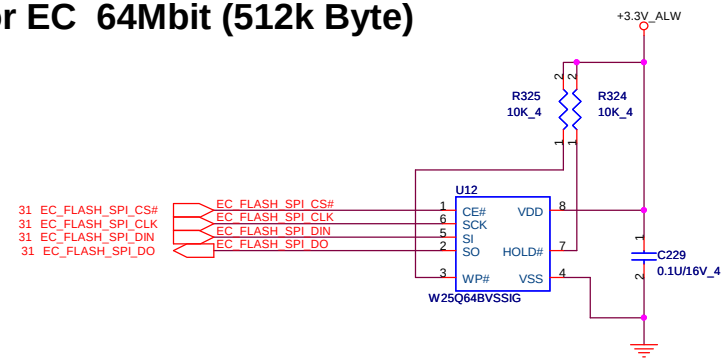
Size	Document Number	Rev
	CODEC	1A

Date: Monday, January 09, 2012 Sheet 30 of 46

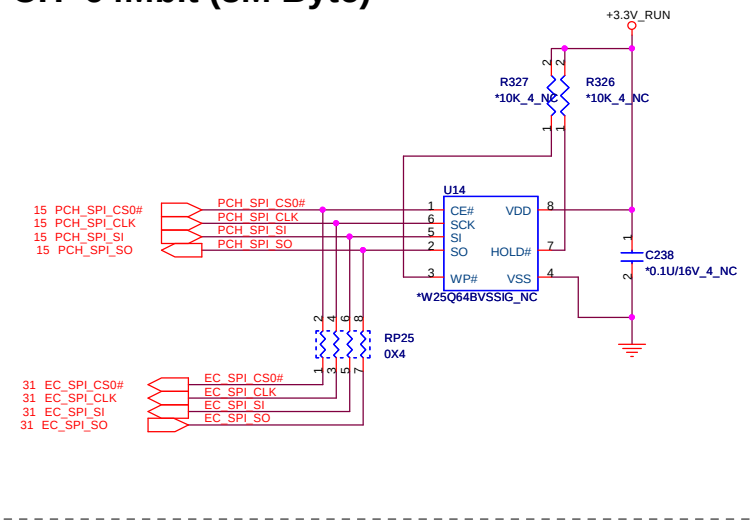

U1
IT8518
LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
Board ID Straps
Thermal
For Crystal-Free
Place these caps close to ITE8518.
Quanta Computer Inc.
PROJECT : V07
SIO (ITE8518E)
Monday, January 09, 2012
WWW.MANUALS.CLAN.SU

FLASH / RTC

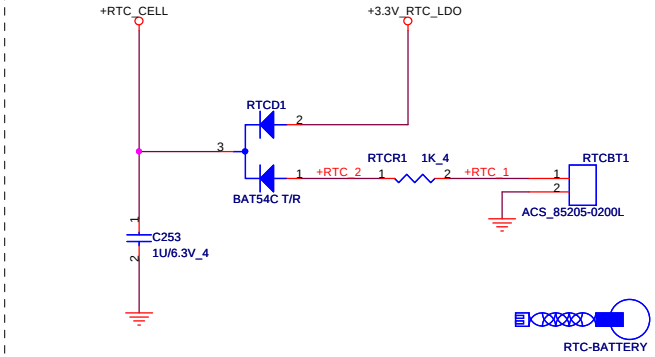
For EC 64Mbit (512k Byte)



For PCH 64Mbit (8M Byte)



RTC



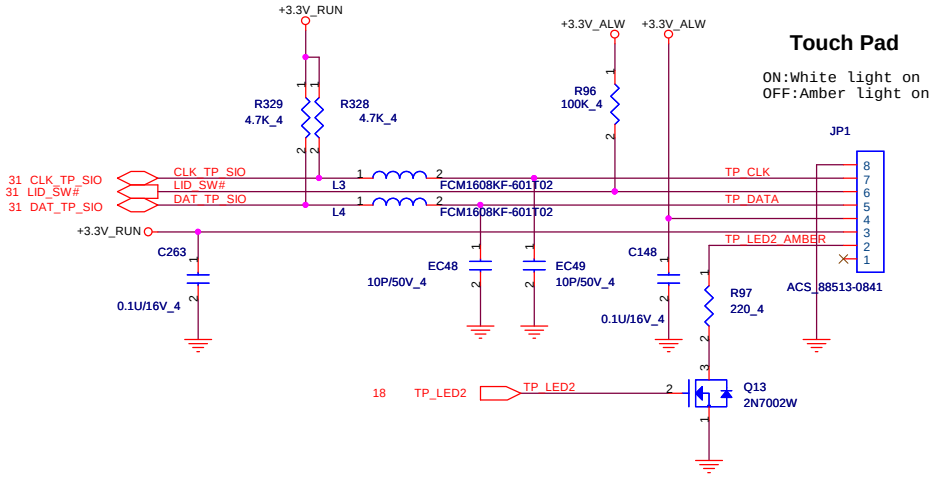
Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

Quanta Computer Inc.		
PROJECT : V07		
Size	Document Number: FLASH / RTC	Rev: 1A
Date: Monday, January 09, 2012	Sheet 32 of 46	

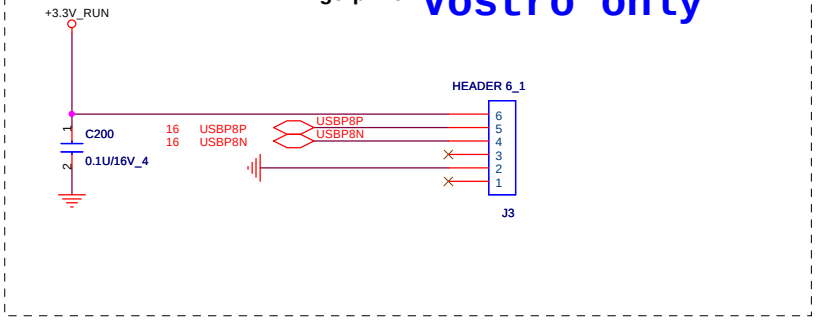
KEYBOARD CONNECTOR

Touch Pad

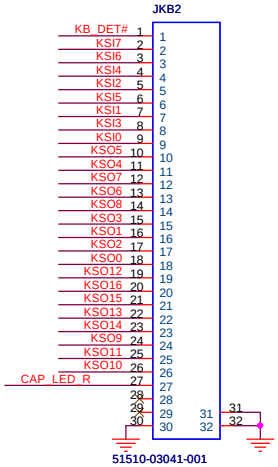
ON:White light on
OFF:Amber light on



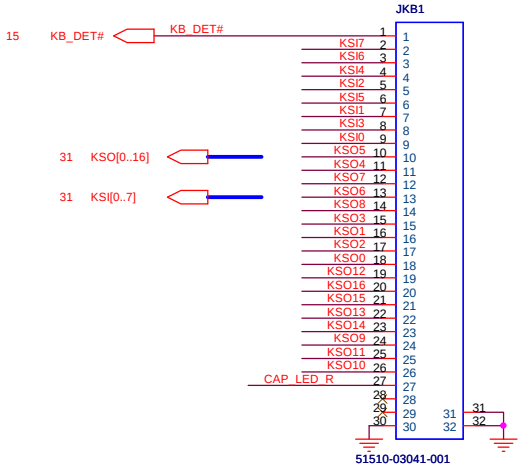
Fingerprint Vostro only

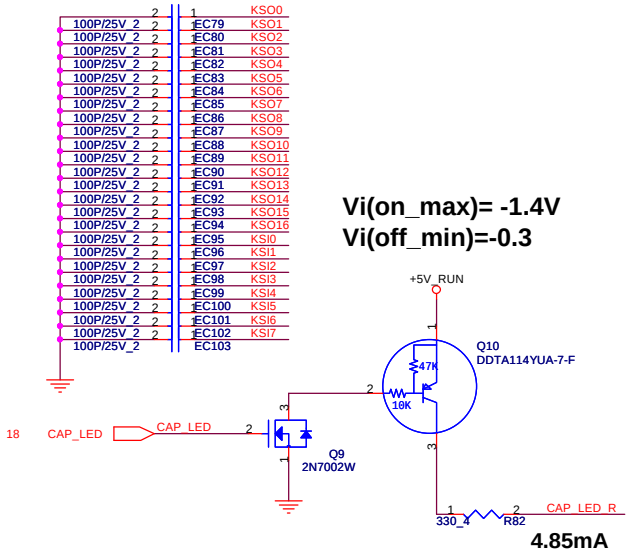


Vostro



Inspiron





Vi(on_max)= -1.4V
Vi(off_min)=-0.3

4.85mA

Quanta Computer Inc.		
PROJECT : V07		
Size	Document Number: TP / KB	Rev: 1A
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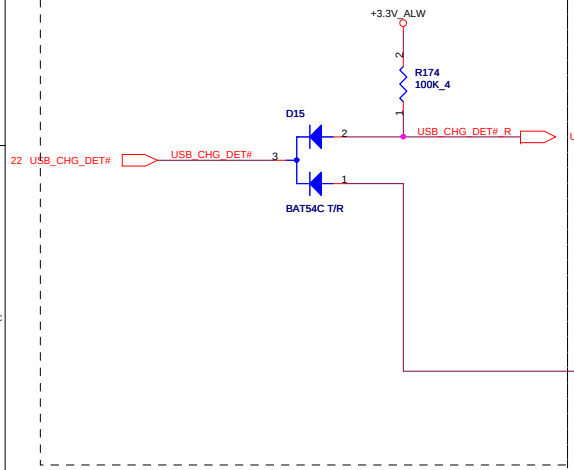
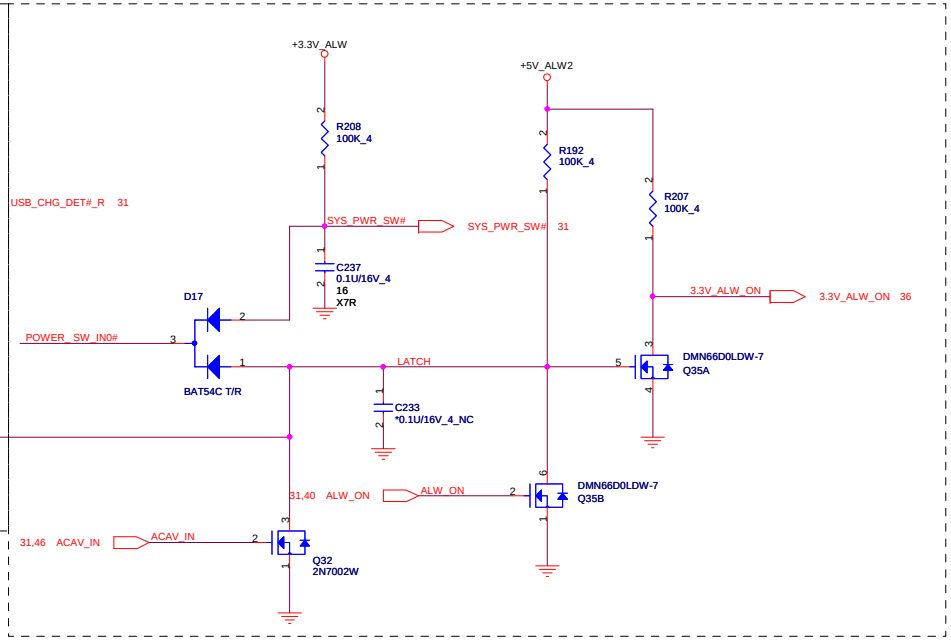
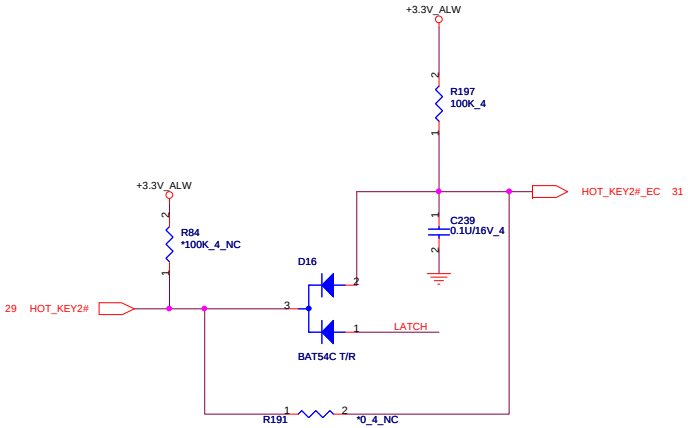
For USB charger usage



3V ALW ON POWER LOGIC

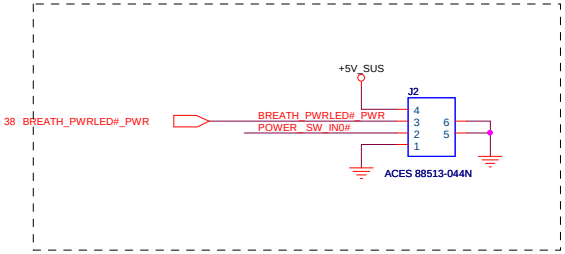


Instant ON function Vostor only



BOM setup	NC	POP
Vostro	R84.R191	D16,C239,R197
Inspiron	D16,C239,R197	R84.R191

TO PWR button board

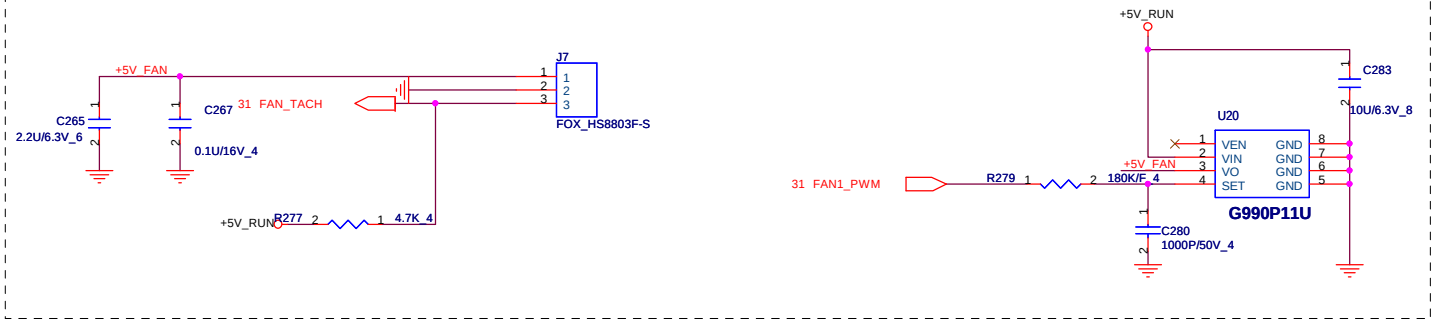


Quanta Computer Inc.

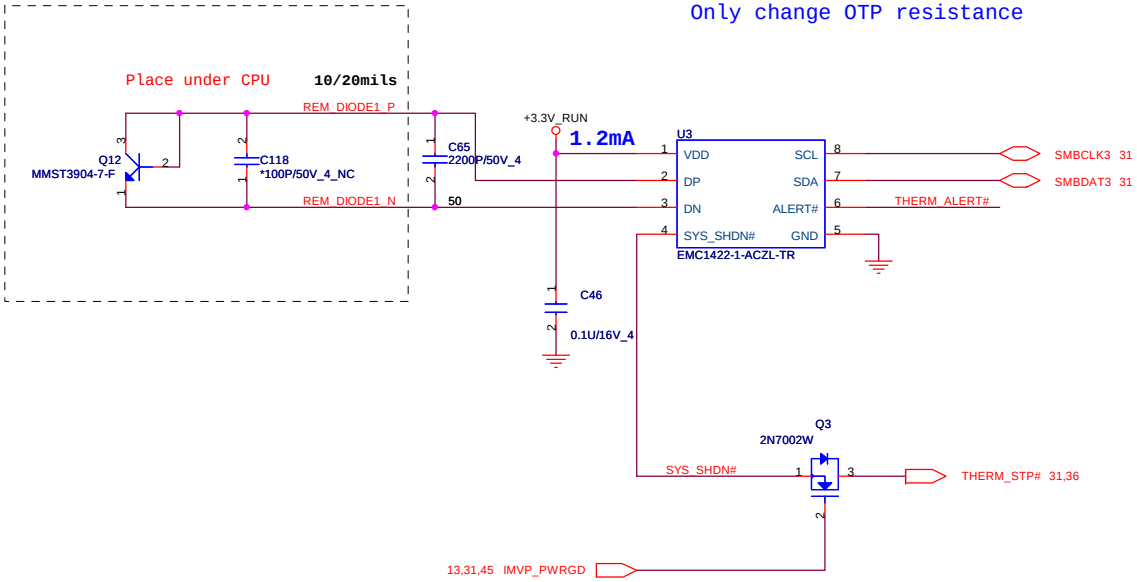
PROJECT : V07

Size	Document Number	Rev
	PWR SW/LED	1A
Date: Monday, January 09, 2012	Sheet 34 of 46	

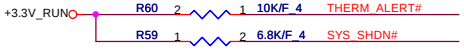
FAN CONTROL



EMC 1422 and NCT7718 PIN TO PIN
Only change OTP resistance



OTP 85 degree C



SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

Quanta Computer Inc.
PROJECT : V07

Size	Document Number	Rev
	FAN & THERMAL	1A

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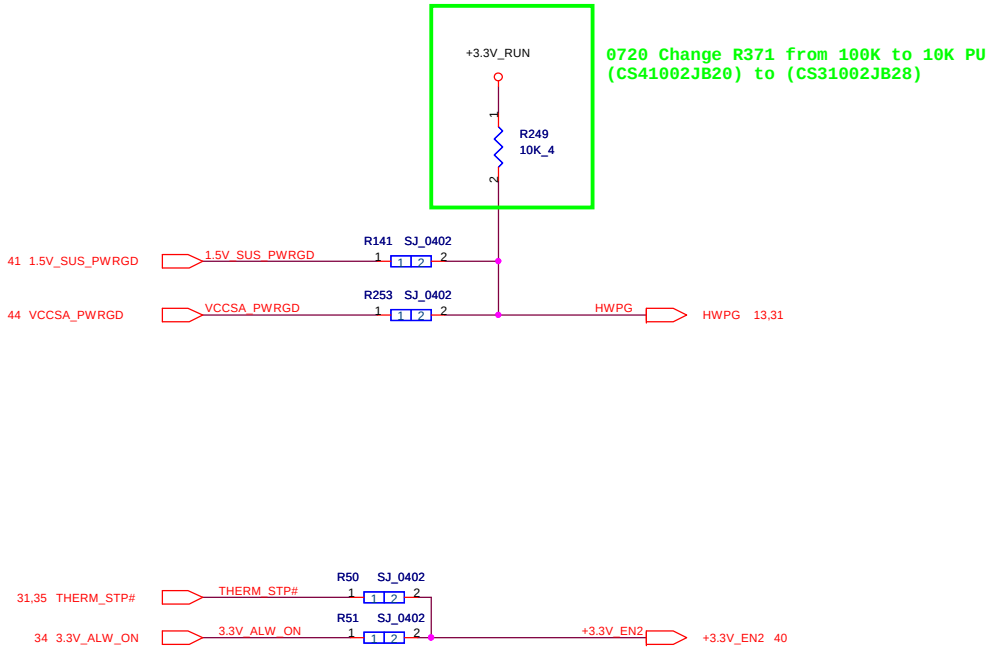

Quanta Computer Inc.

PROJECT : V07

Size	Document Number	Rev
	System Reset Circuit	1A

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Quanta Computer Inc.

PROJECT : V07

Size	Document Number	Rev
	MiniCard / mSATA	1A

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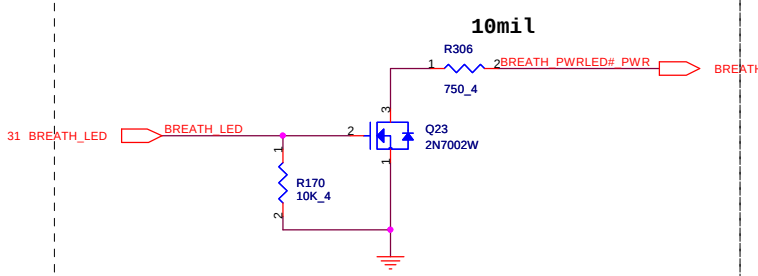
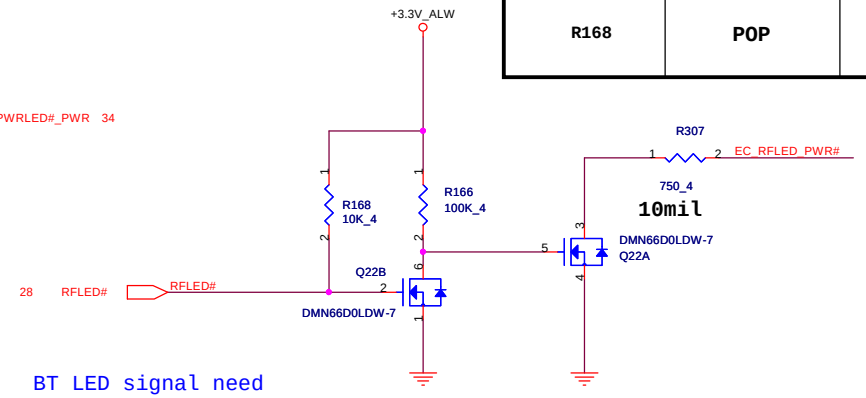
Power



Bluetooth / WLAN on/off LED

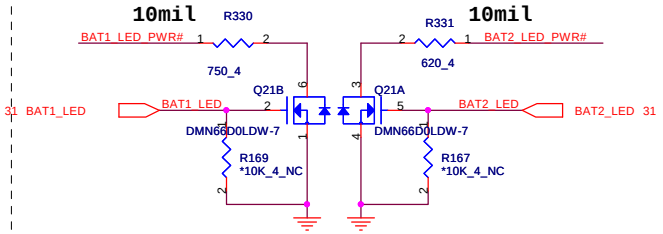
BOM setup	VOSTOR(V07)	Inspiron(R07)
R168	POP	NC



BT LED signal need

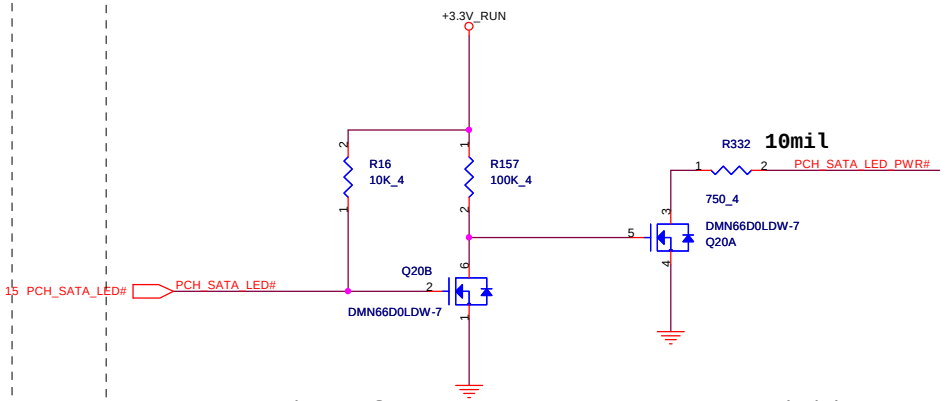
Change from 2N7002W-7-F to DMN66D0LDW-7

Battery

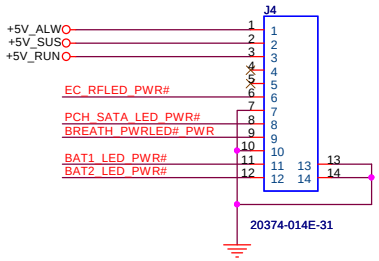


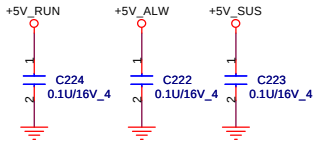
Change from 2N7002W-7-F to DMN66D0LDW-7(9/2)

HDD activity LED.



Change from 2N7002W-7-F to DMN66D0LDW-7(9/2)





Quanta Computer Inc.
PROJECT : V07

Size	Document Number	Rev
	LED board CONN	1A
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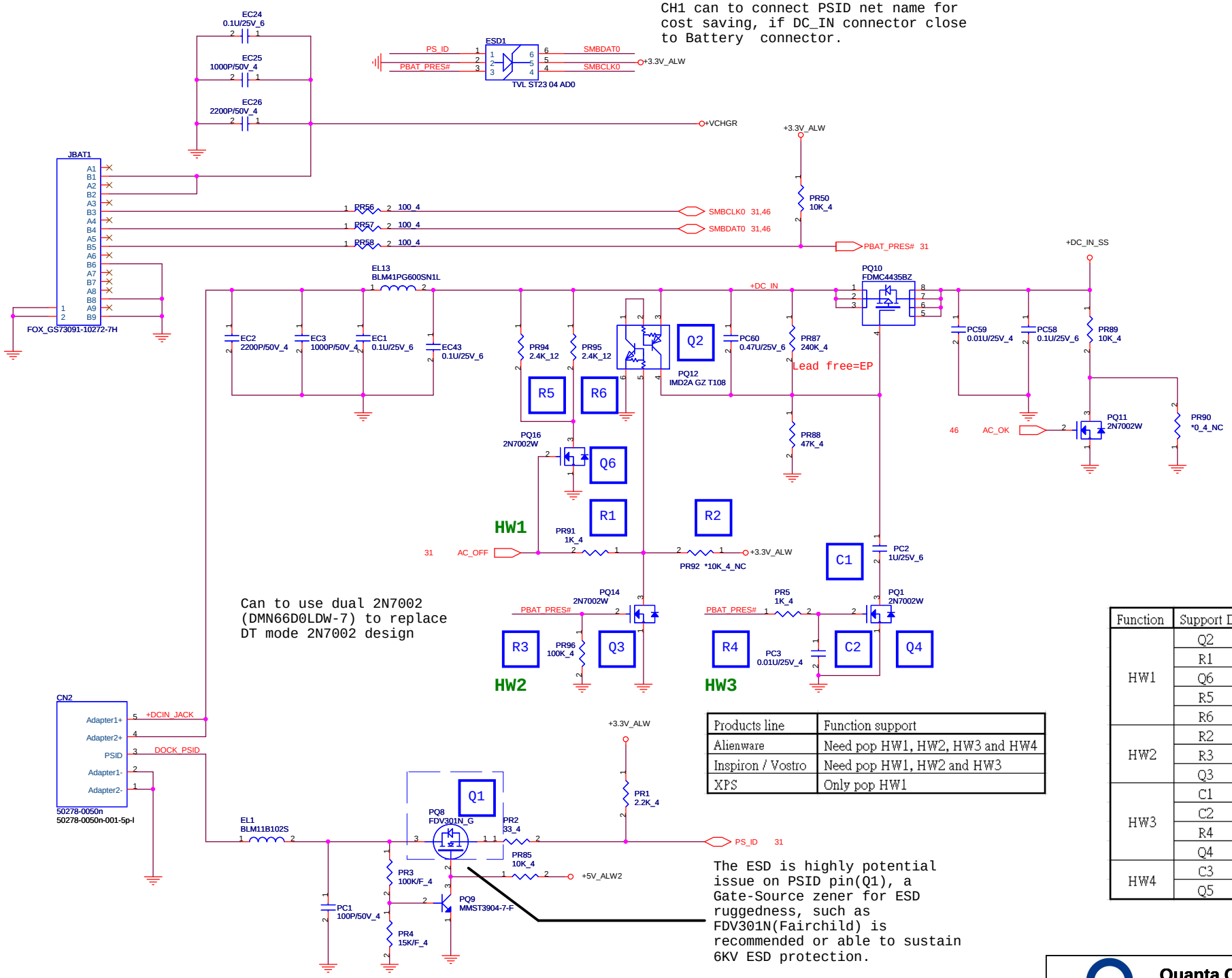
CH1 can to connect PSID net name for cost saving, if DC_IN connector close to Battery connector.



Can to use dual 2N7002 (DMN66D0LDW-7) to replace DT mode 2N7002 design

Products line	Function support
Alienware	Need pop HW1, HW2, HW3 and HW4
Inspiron / Vostro	Need pop HW1, HW2 and HW3
XPS	Only pop HW1

Function	Support DT Mode Components	
HW1	Q2	IMD2AT108
	R1	1K_4
	Q6	2N7002W-7-F
	R5	2.2K_12
	R6	2.2K_12
HW2	R2	10K_4
	R3	100K_4
	Q3	2N7002W-7-F
HW3	C1	1U/6.3V_4
	C2	0.01U/25V_4
	R4	1K_4
	Q4	2N7002W-7-F
HW4	C3	1U/6.3V_4
	Q5	2N7002W-7-F

The ESD is highly potential issue on PSID pin(Q1), a Gate-Source zener for ESD ruggedness, such as FDV301N(Fairchild) is recommended or able to sustain 6KV ESD protection.

Quanta Computer Inc.
PROJECT : R07/V07

Size	Document Number	Rev
	DC IN / BATT	1A
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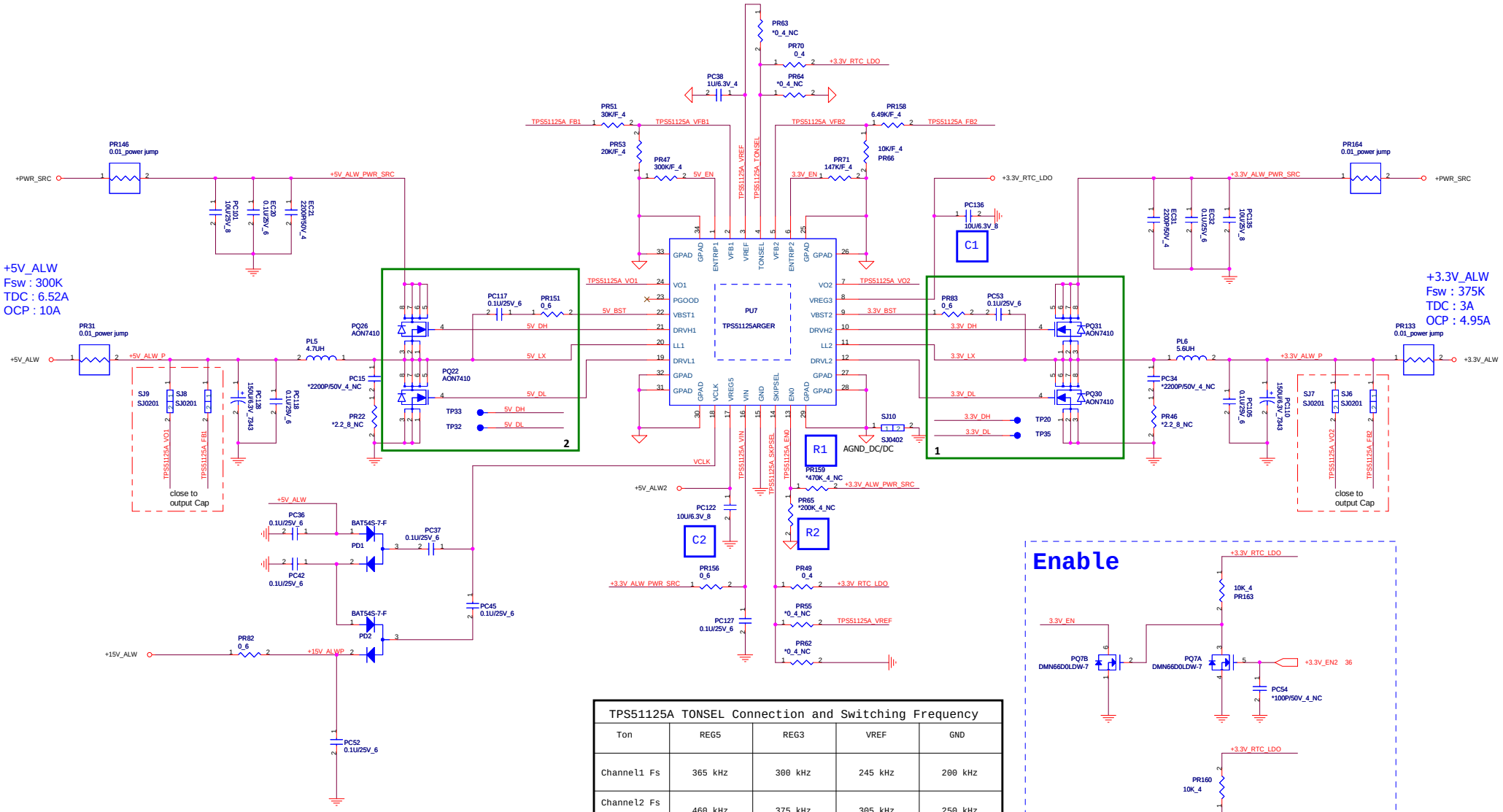

TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz

P_1. Change PQ30 and PQ31 from FDMC8884 to AON7410, change PR83 to 0ohm

P_2. Change PQ22 and PQ26 from FDMC8884 to AON7410, change PR151 to 0ohm

Quanta Computer Inc.
PROJECT : R07/V07

Size	Document Number	Rev
	3.3V_ALW / 5V_ALW (TPS51125ARGER)	1A
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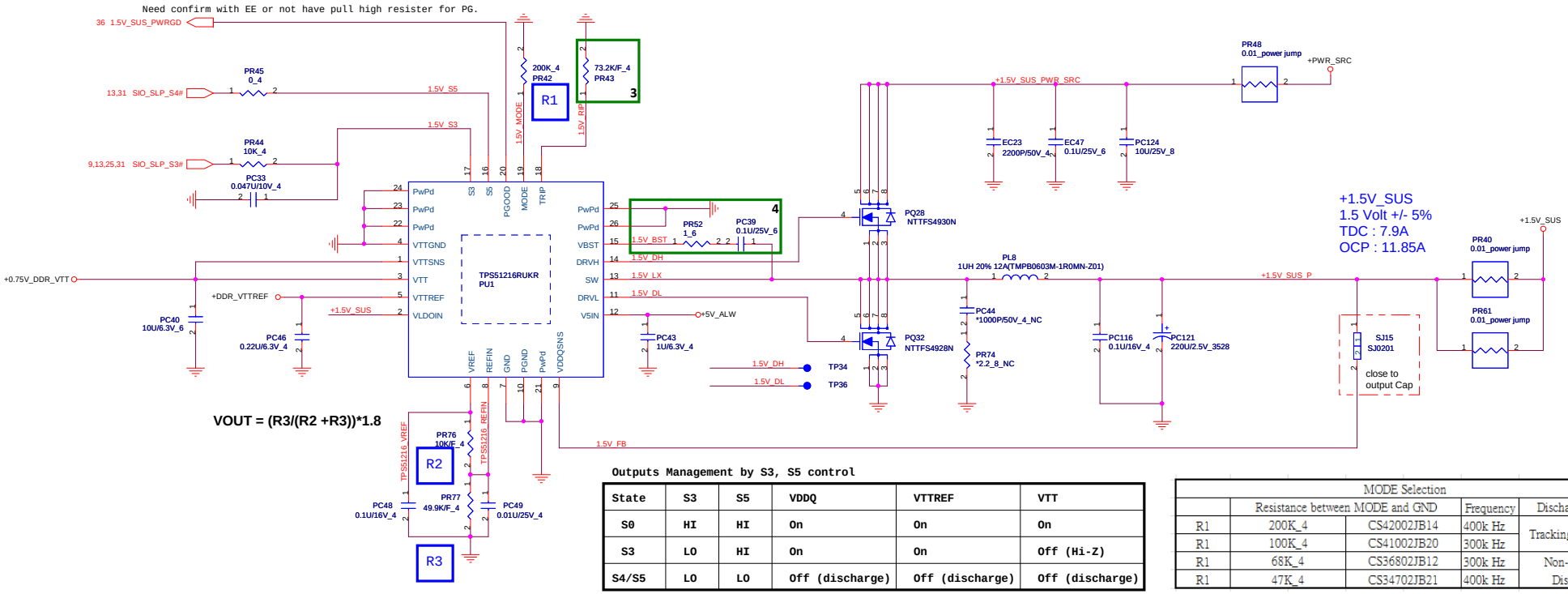

VOUT = (R3/(R2 +R3))*1.8

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

MODE Selection

	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz	Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz	
R1	68K_4	CS36802JB12	300k Hz	Non-tracking
R1	47K_4	CS34702JB21	400k Hz	Discharge

P_3. Change PR43 to 73.2Kohm for OCP fine tune
P_4. Change PR52 from 0ohm to 1ohm

Quanta Computer Inc.
PROJECT : R07/V07

Size	Document Number	Rev
	1.5_SUS/0.75_DDR_VTT (TPS51216RUKR)	1A

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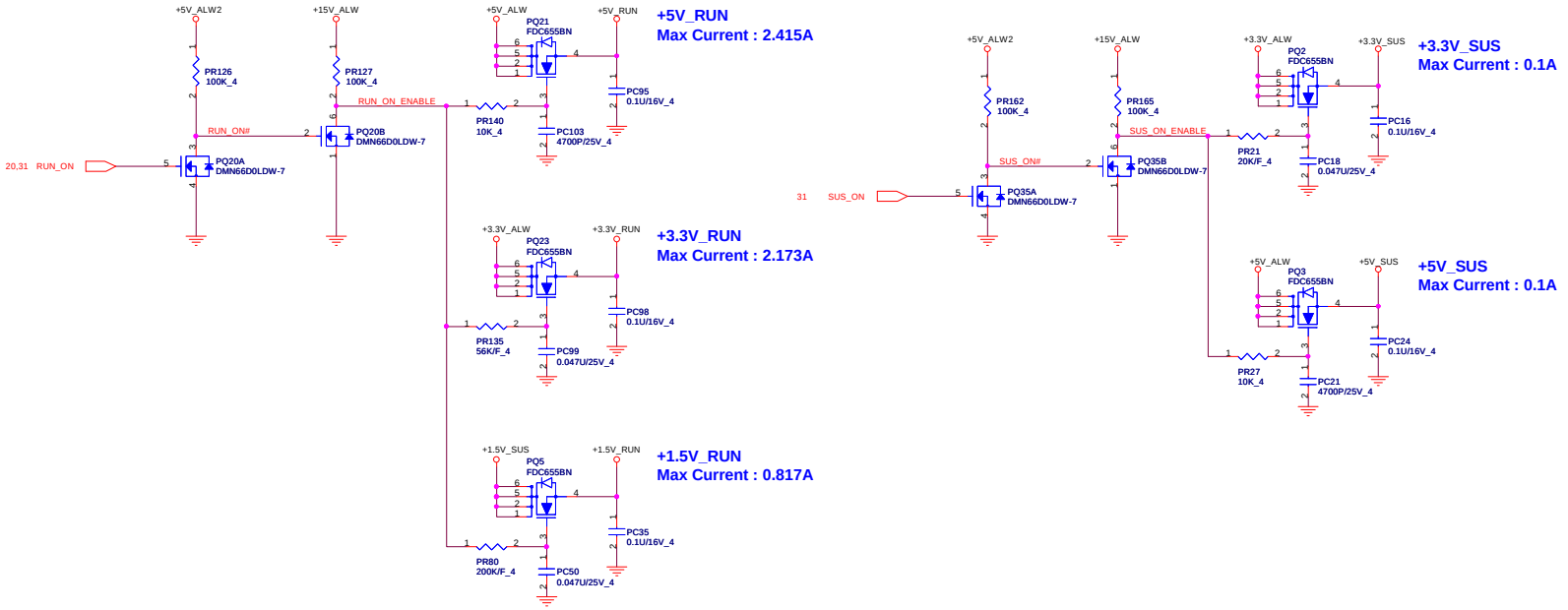

Quanta Computer Inc.

PROJECT : R07/V07

Size	Document Number	Rev
	Load Switch	1A

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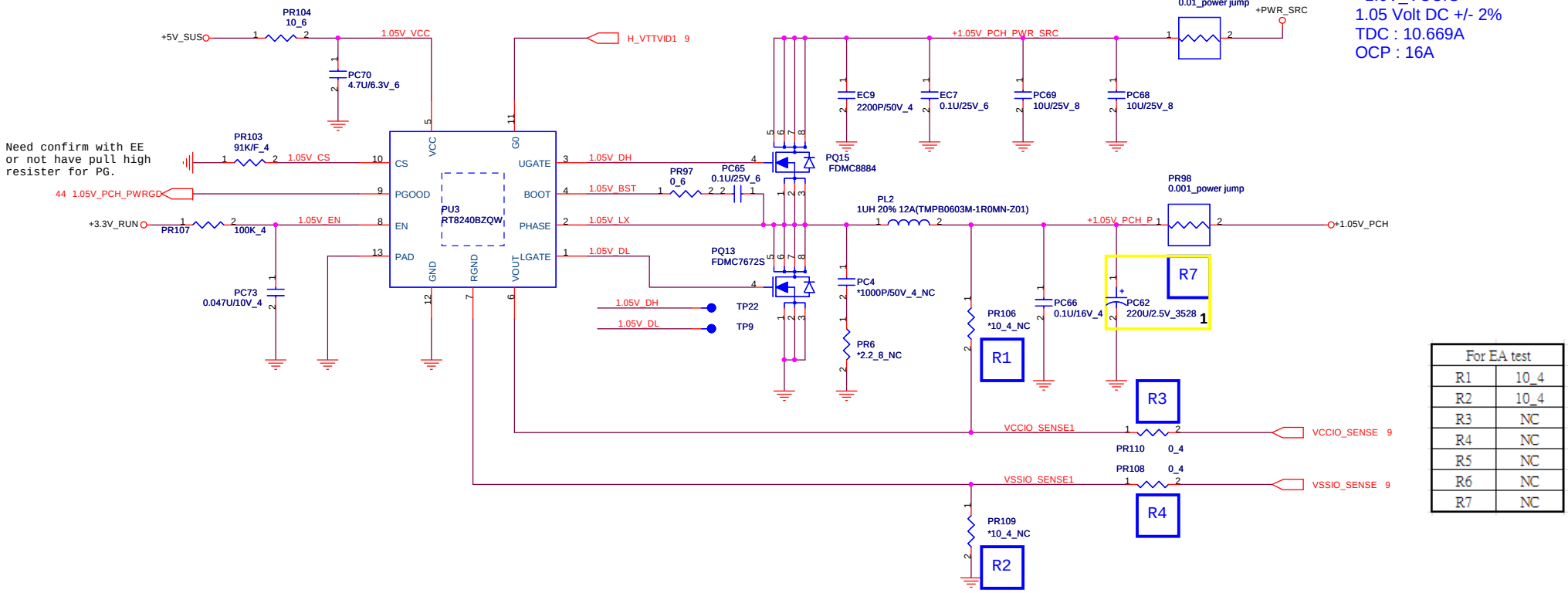

For EA test	
R1	10_4
R2	10_4
R3	NC
R4	NC
R5	NC
R6	NC
R7	NC

S_1. Change PC62 to 220uF/ESR15 for shortage issue

Quanta Computer Inc.
PROJECT : R07/V07

Size	Document Number	Rev
	+1.05V_PCH / VTT (RT8240BGQW)	1A

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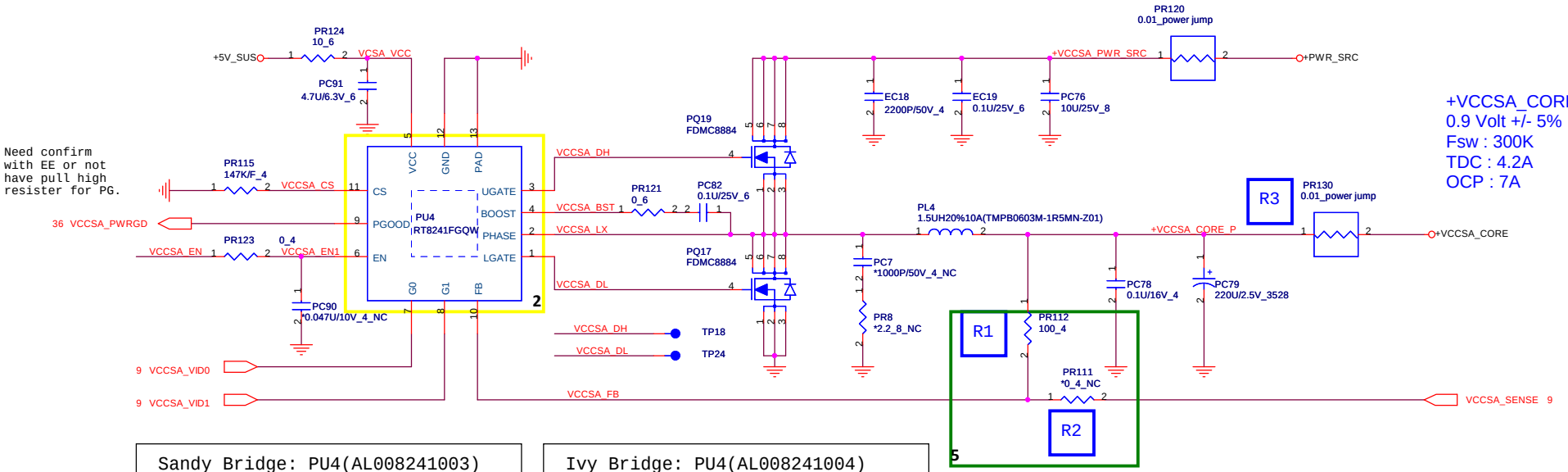


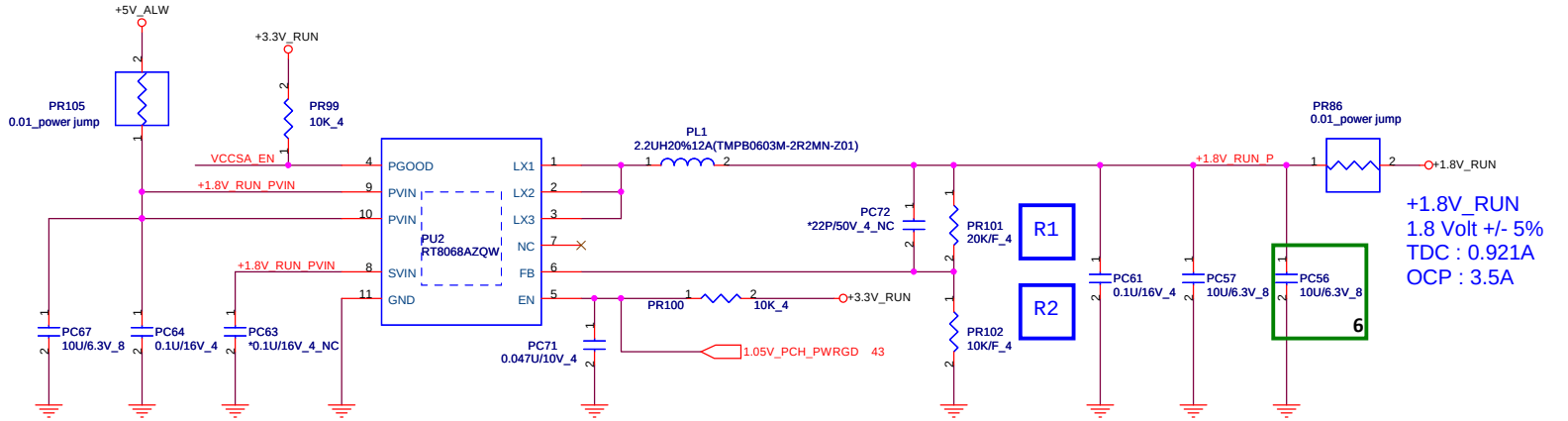
Need confirm with EE or not have pull high resister for PG.

+VCCSA_CORE
0.9 Volt +/- 5%
Fsw : 300K
TDC : 4.2A
OCP : 7A

Sandy Bridge: PU4(AL008241003)		
VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.85V
Low	High	0.725V
High	High	0.675V

Ivy Bridge: PU4(AL008241004)		
VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.85V
Low	High	0.775V
High	High	0.75V

For EA test	
R1	100_4
R2	NC
R3	NC
R4	NC



+1.8V_RUN
1.8 Volt +/- 5%
TDC : 0.921A
OCP : 3.5A

VOUT = 0.6(1+R1/R2)

P_5. Change to local sense
P_6. Pop PC56
S_2. Change PU4 P/N for IVB CPU change

Quanta Computer Inc.
PROJECT : R07/V07

Size	Document Number	Rev
	VCCSA (RT8241DGQW)	1A

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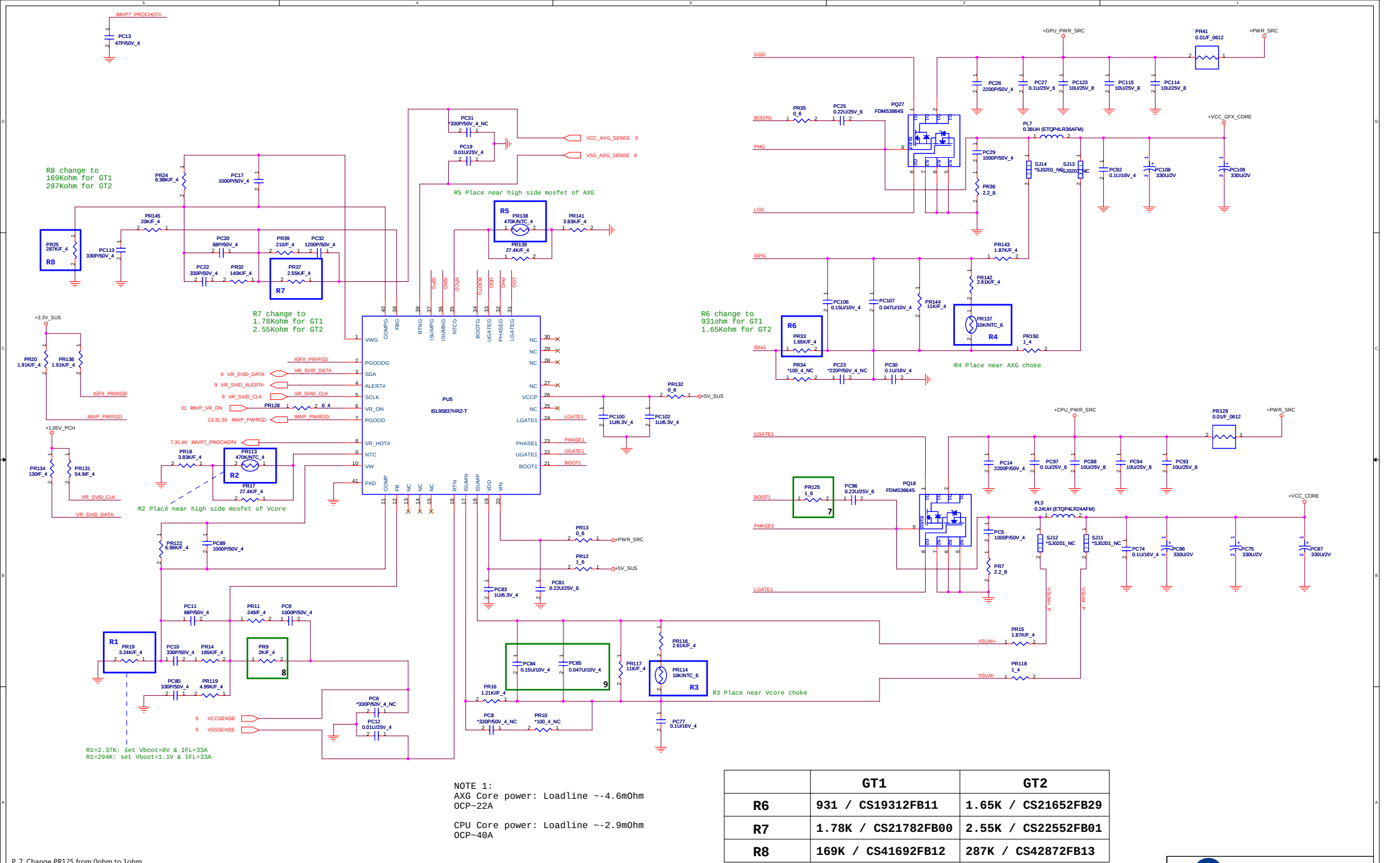


NOTE 1:
AXG Core power: Loadline ~-4.6mOhm
OCP~22A

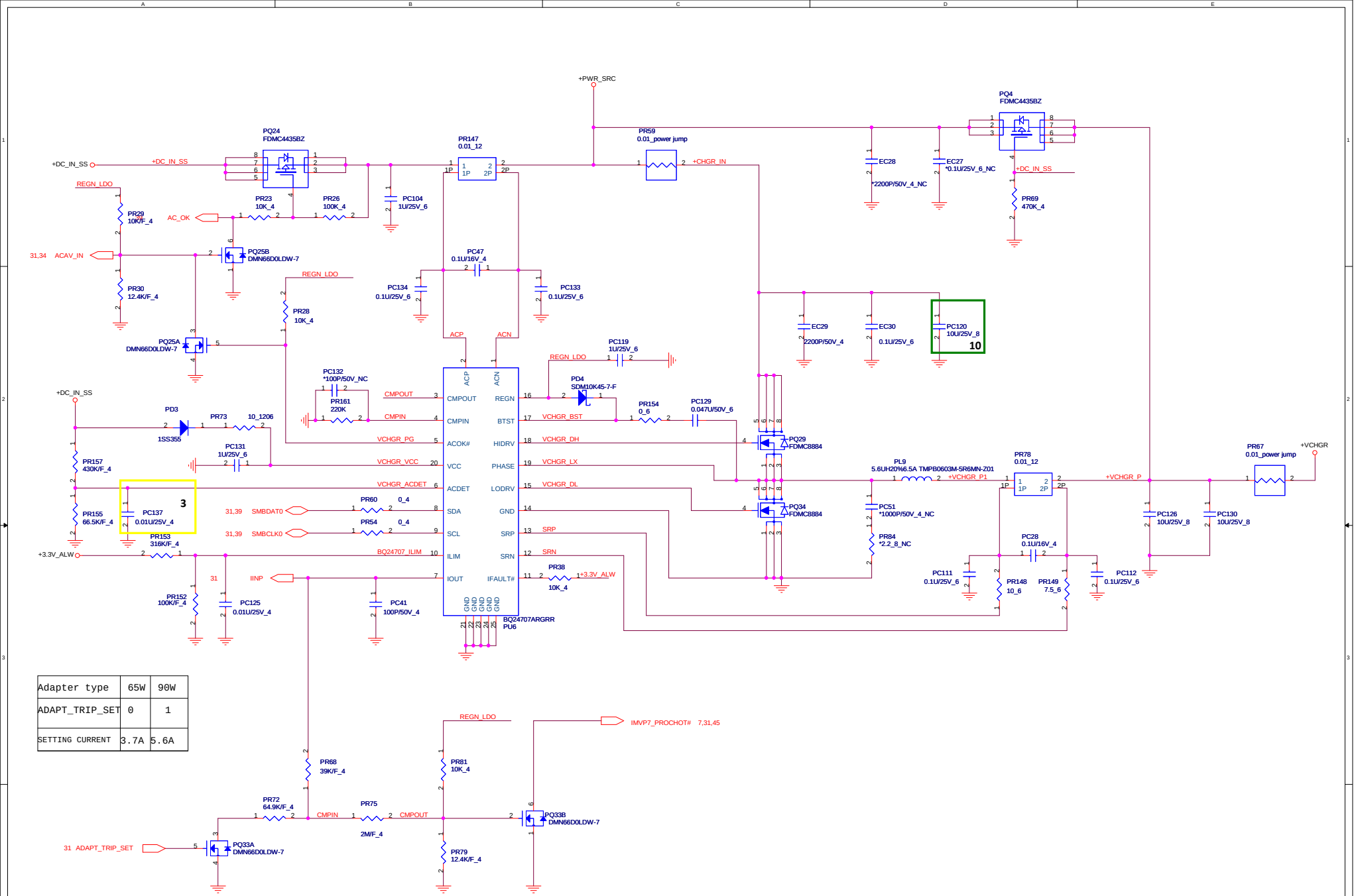
CPU Core power: Loadline ~-2.9mOhm
OCP~40A

	GT1	GT2
R6	931 / CS19312FB11	1.65K / CS21652FB29
R7	1.78K / CS21782FB00	2.55K / CS22552FB01
R8	169K / CS41692FB12	287K / CS42872FB13

P_7. Change PR125 from 0ohm to 1ohm
P_8. Change PR9 from 2.15Kohm to 2Kohm
P_9. Change PC84 to 0.15uF and change PC85 to 0.047uF

Quanta Computer Inc.
PROJECT : R07/V07

Size	Document Number	Rev
	VCC_CORE/IGPU_CORE	1A
Date: Monday, January 09, 2012	Sheet 45 of 46	



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

P_10. Change PC120 to 10uF.
S_1. Add PC137 for input voltage stability.

Quanta Computer Inc.
PROJECT : R07/V07

Size	Document Number	Rev
	Charger (BQ24707ARGRR)	1A
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