Foxconn MCP61M05

Fab :A

nVIDIA MCP61 Chipset for AMD M2 CPU

(3/31/2008)

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Title: Cover		
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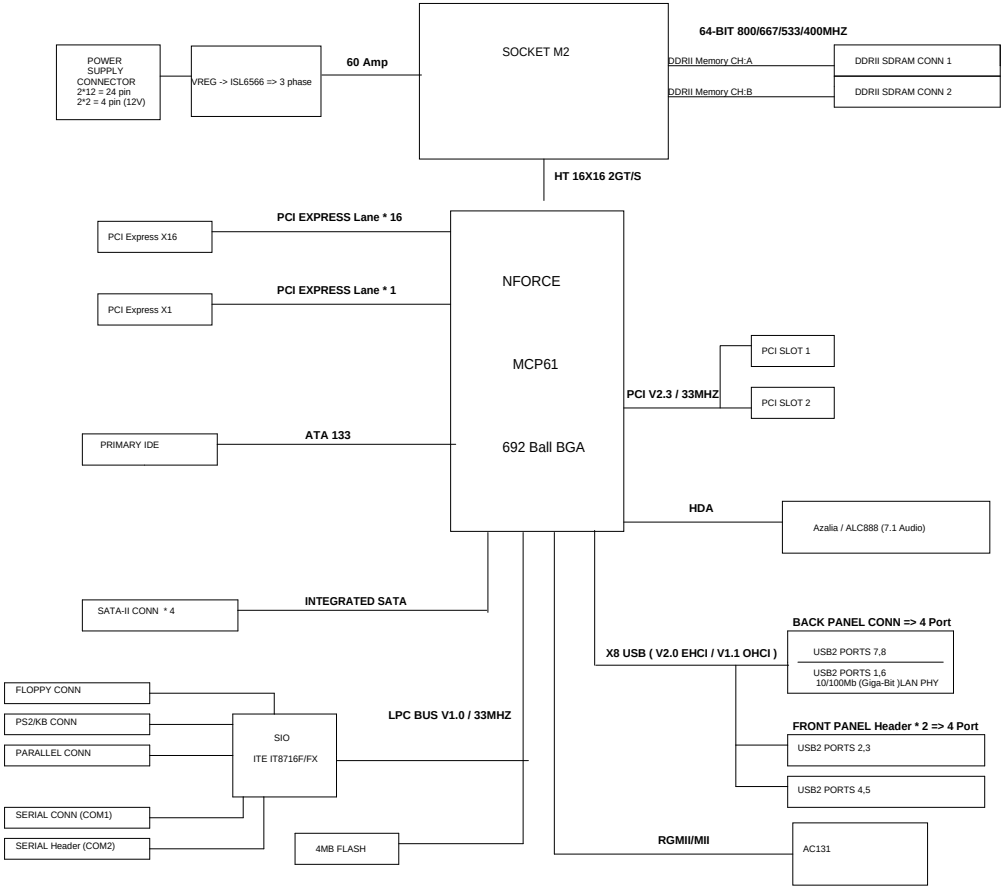
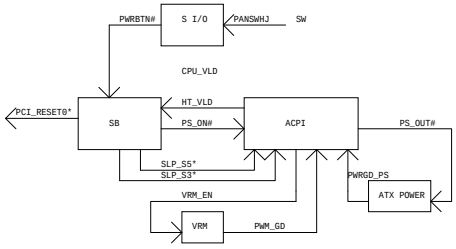
MCP61M05 Block Diagram





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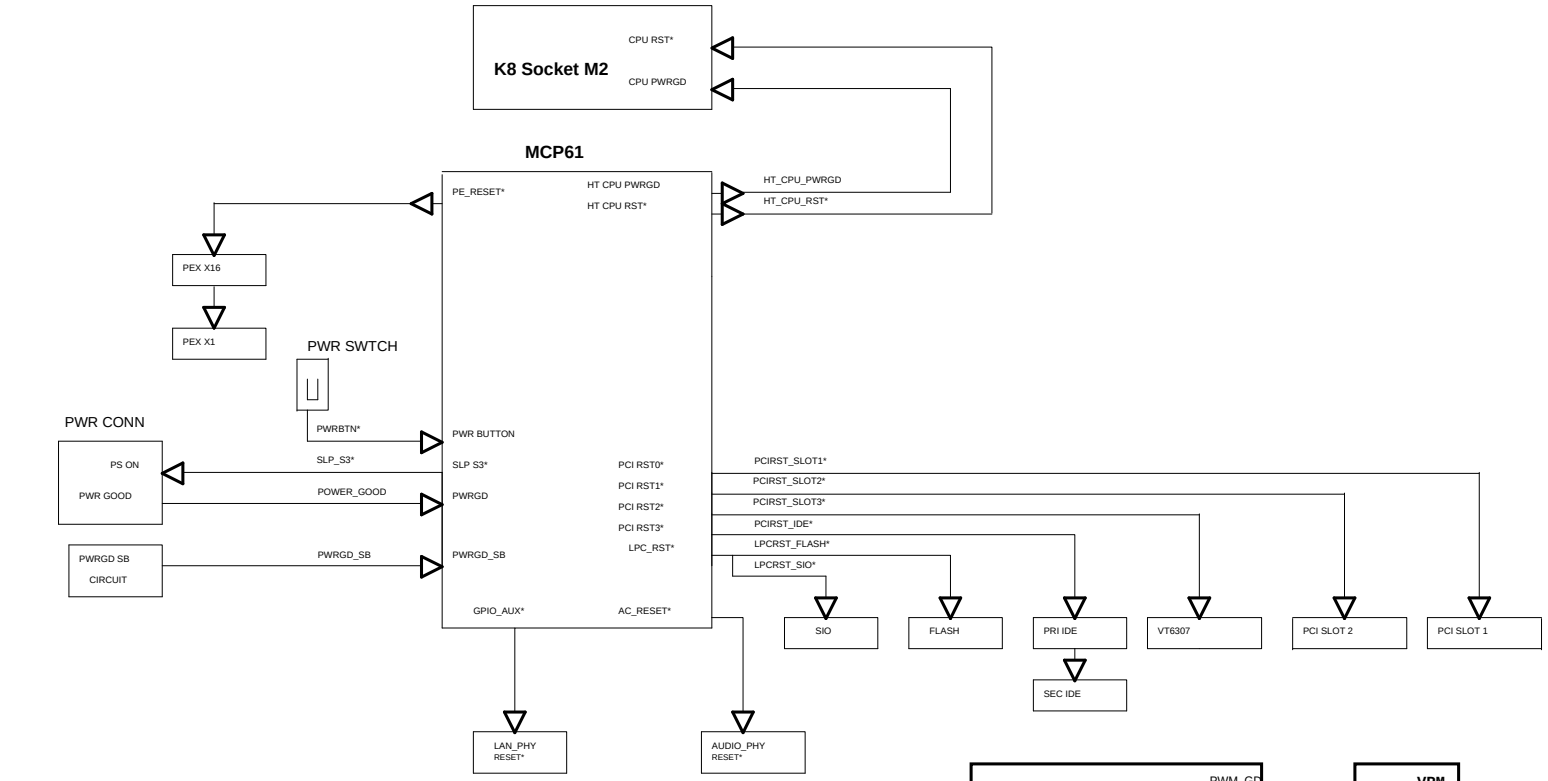
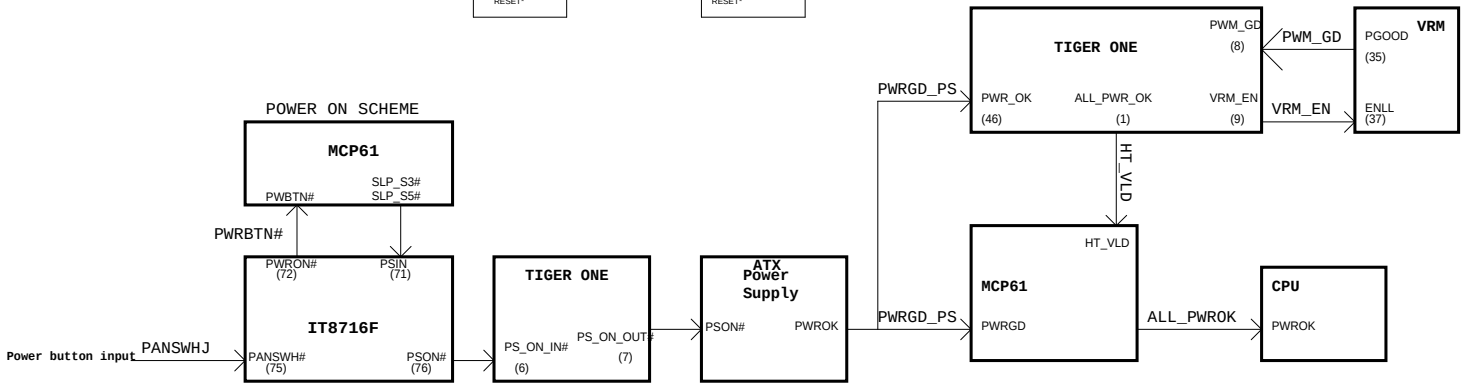
RESET MAP





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Title: Reset Map	MCP61M05	
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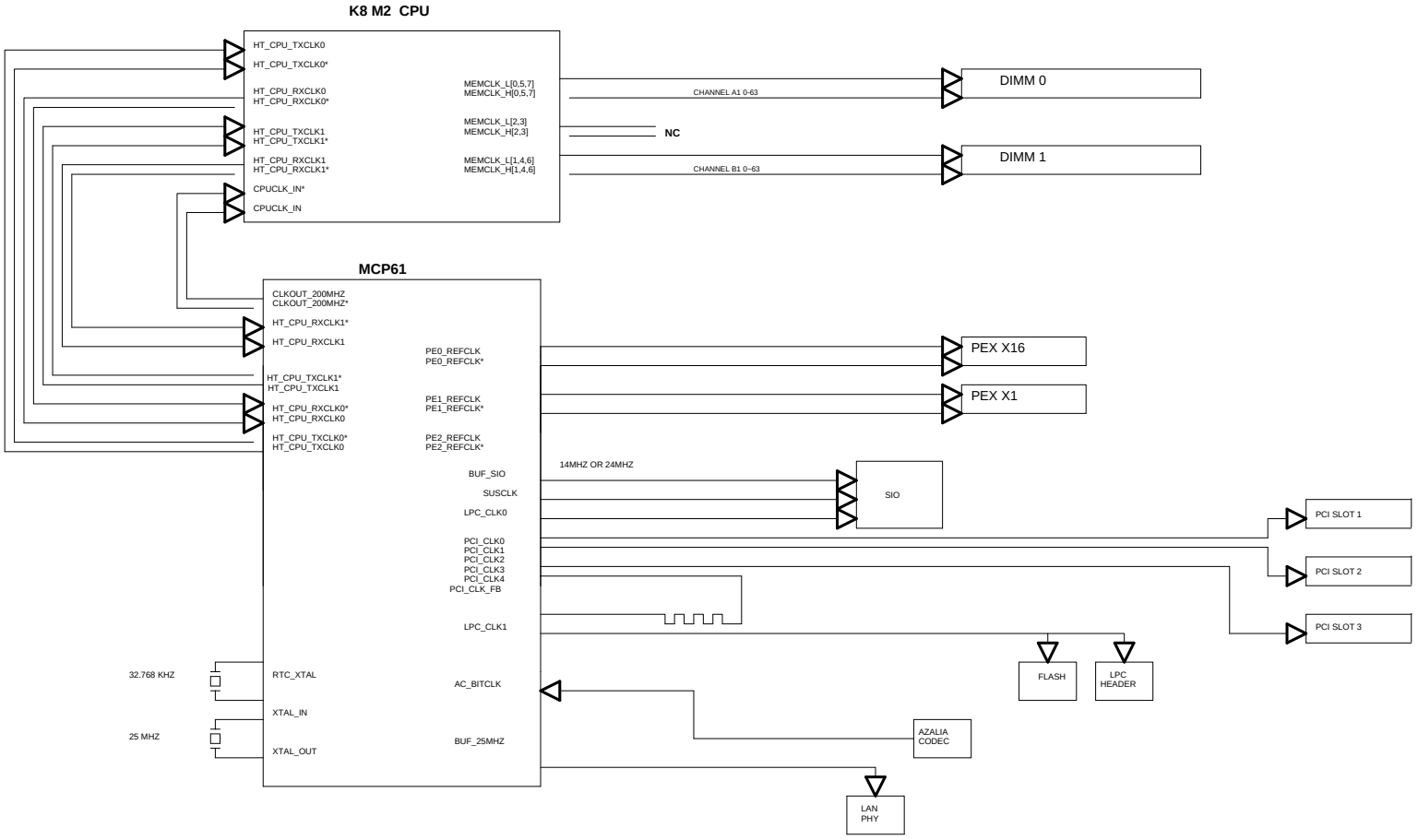

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Title: Clock Distribution

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CPU VID TABLE

VID [4..0]	VDD		VID [4..0]	VDD
0X00000	1.550V		0X10000	1.150V
0X00001	1.525V		0X10001	1.125V
0X00010	1.500V		0X10010	1.100V
0X00011	1.475V		0X10011	1.075V
0X00100	1.450V		0X10100	1.050V
0X00101	1.425V		0X10101	1.025V
0X00110	1.400V		0X10110	1.000V
0X00111	1.375V		0X10111	0.975V
0X01000	1.350V		0X11000	0.950V
0X01001	1.325V		0X11001	0.925V
0X01010	1.300V		0X11010	0.900V
0X01011	1.275V		0X11011	0.875V
0X01100	1.250V		0X11100	0.850V
0X01101	1.225V		0X11101	0.825V
0X01110	1.200V		0X11110	0.800V
0X01111	1.175V		0X11111	OFF

SMBUS ADDRESS MAP

DEVICE	SMBUS #	ADDRESS
DIMM 0	0	1010 000 = 0X50
DIMM 1	0	1010 001 = 0X51
DIMM 2	0	1010 010 = 0X52
DIMM 3	0	1010 011 = 0X53
SIO	1	0101 101 = 0X2D
PCI SLOT 1	1	ARP
PCI SLOT 2	1	ARP
1394	1	ARP
DDC BUS	A	?
DDC BUS	B	?

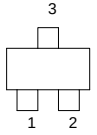
PCI INTERRUPT/IDSEL MAP

BACK PANEL SLOT	PCI BUS#	DEVICE#	IDSEL PIN	PCI SLOT INTA*	PCI SLOT INTB*	PCI SLOT INTC*	PCI SLOT INTD*	REQ/GNT
VT6308	01	0X06	22	P_INTZ*				1/1
PCI 2	01	0X08	23	P_INTW*	P_INTX*	P_INTY*	P_INTZ*	2/2
PCI 1	01	0X09	24	P_INTX*	P_INTY*	P_INTZ*	P_INTW*	3/3

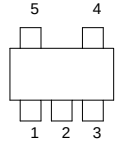
PCI DEVICE MAP

DEVICE	PCI BUS#	DEVICE#	FUNCTION	DEVICE ID
MCP 61	MCP51 LOGICAL PCI BUS 0	0X01-0X0F	--	--
MAC /MAC	0	XA	0	0X56/57
PCI-PCI BRIDGE	0	X9	0	0X005C
SATA1	0	X8	0	0X0055
SATA0	0	X8	0	0X0054
IDE	0	X6	0	0X0053
MODEM CODEC	0	X4	1	0X0058
AUDIO CODEC	0	X4	0	0X0059
USB 2.0	0	X2	1	0X005B
USB 1.1	0	X2	0	0X005A
SHAPE TRIM	0	X1	2	0X005F
LDT	0	X0	0	0X005E
SMBUS2	0	X1	1	0X0052
LEGACY SLAVE	0	?	?	0X00D3
LPC	0	X1	0	0X0050/51
LOGICAL PCI BUS	1	?	?	?
PCI SLOT 1				
PCI SLOT 2				
PCI SLOT 3				
PCI SLOT 4				
PCI SLOT 5				

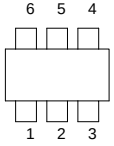
SOT23



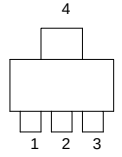
SOT23-5/SC70
SOT89-5



SOT23-6



SOT223



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Title: PCI Device / VID Table

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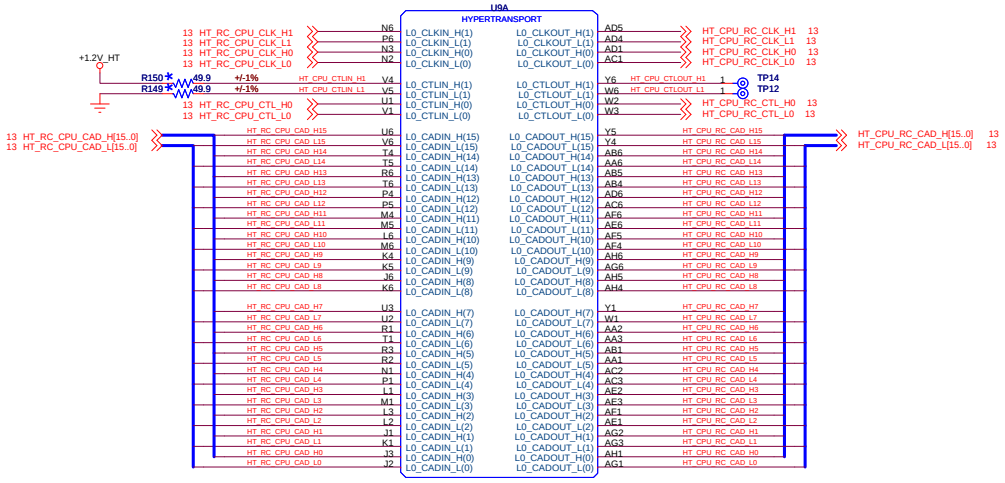

Layout: Add stitching caps if crossing plane split

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Title	M2 HyperTransport		
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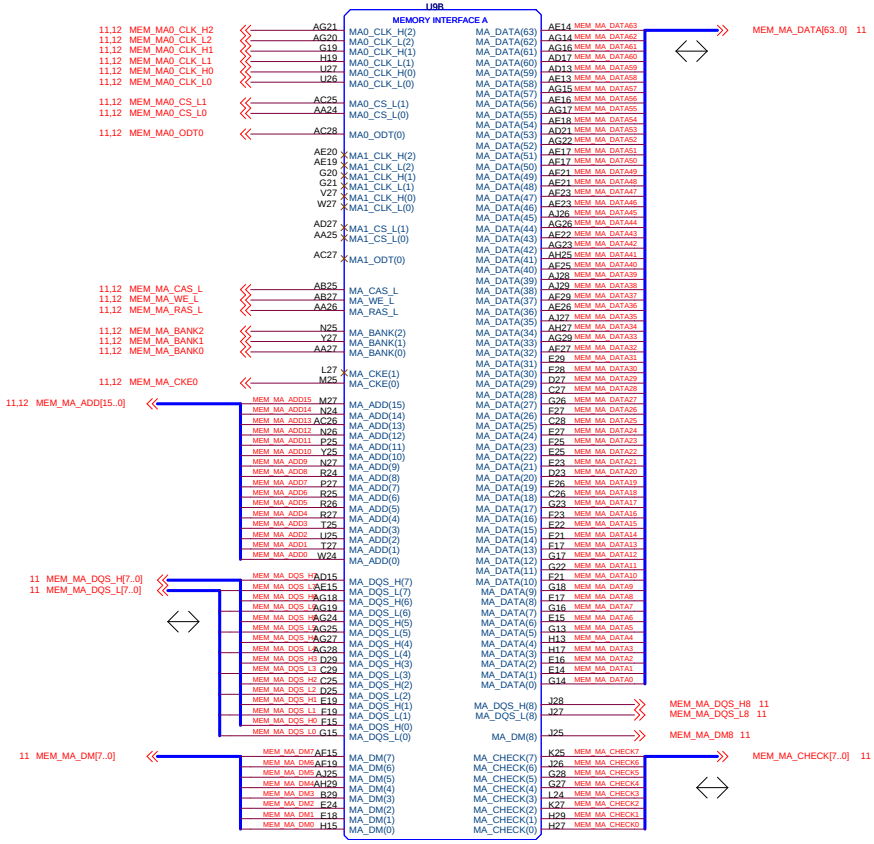
U9B
MEMORY INTERFACE A
11,12 MEM_MA0_CLK_H2
11,12 MEM_MA0_CLK_L2
11,12 MEM_MA0_CLK_H1
11,12 MEM_MA0_CLK_L1
11,12 MEM_MA0_CLK_H0
11,12 MEM_MA0_CLK_L0
11,12 MEM_MA0_CS_L1
11,12 MEM_MA0_CS_L0
11,12 MEM_MA0_ODT0
11,12 MEM_MA_CAS_L
11,12 MEM_MA_WE_L
11,12 MEM_MA_RAS_L
11,12 MEM_MA_BANK2
11,12 MEM_MA_BANK1
11,12 MEM_MA_BANK0
11,12 MEM_MA_CKE0
11,12 MEM_MA_ADD[15..0]
11 MEM_MA_DQS_H[7..0]
11 MEM_MA_DQS_L[7..0]
11 MEM_MA_DM[7..0]
MEM_MA_DATA[63..0] 11
MEM_MA_DQS_H8 11
MEM_MA_DQS_L8 11
MEM_MA_DM8 11
MEM_MA_CHECK[7..0] 11

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M2- 2 DDR -1
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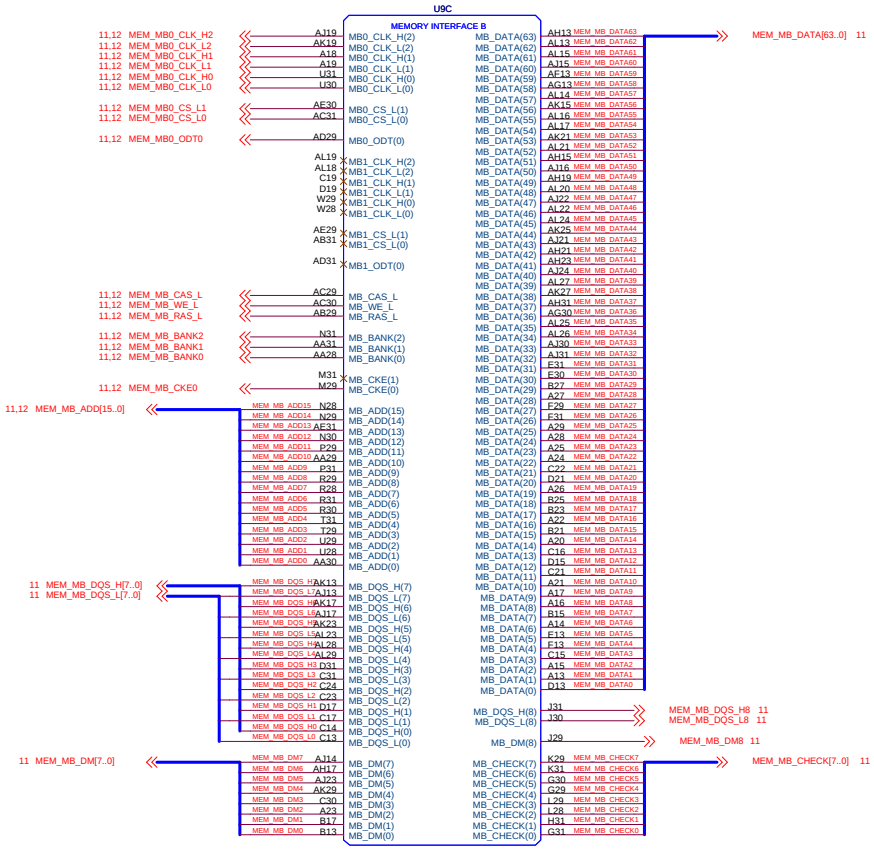

Title	M2- 2 DDR -2
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Level translation buffers
Assuming system devices
Do not provide VDDIO
compatible voltage levels

modify 8/20

Keep trace to resistor
less than 600mils from CPU pin and
trace to AC caps less than 1250mils

Required for compatibility
with future processors

Keep trace to resistors
less than 1.5" from CPU pin

Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin

CPU_M_VREF_SUS

Layout: Place near CPU socket

Erratum 133, Revision Guide for
AMD NPT 0Fh Processors

Erratum 133, Revision Guide for
AMD NPT 0Fh Processors

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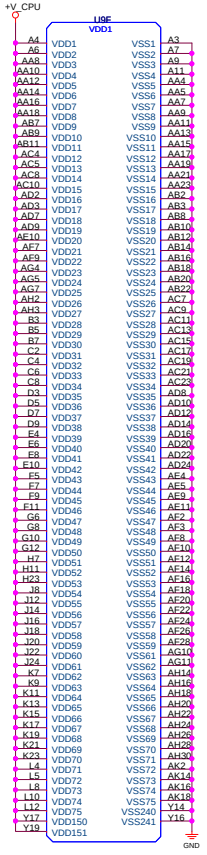
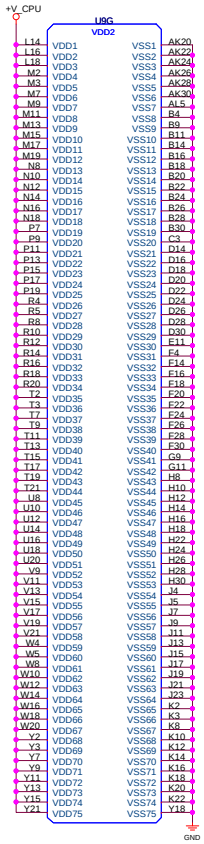
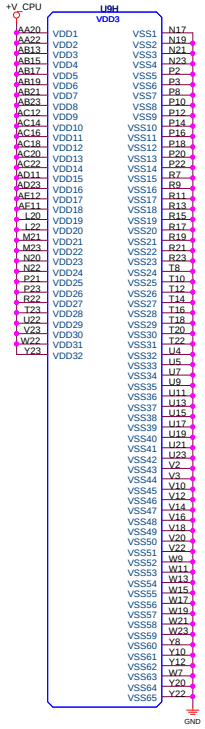
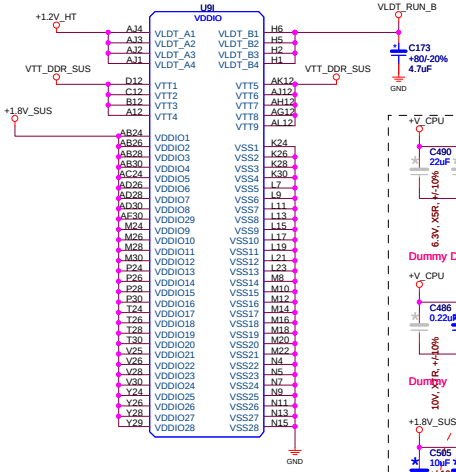
Processor Power & Ground



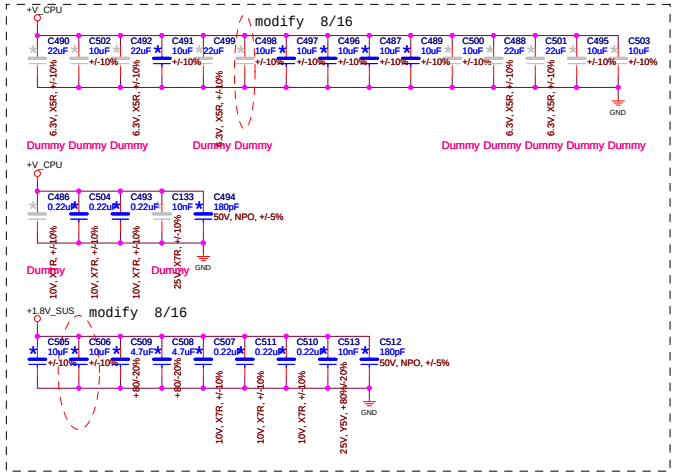




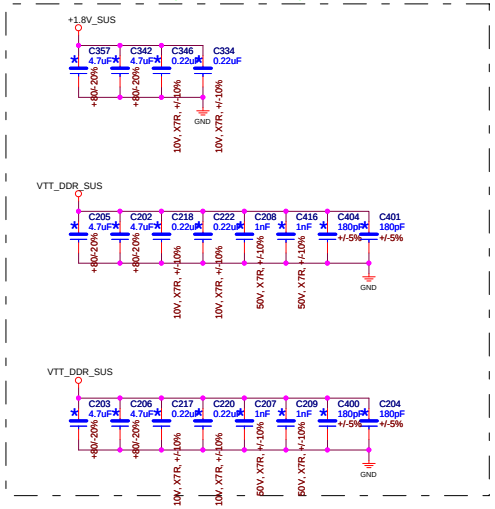
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



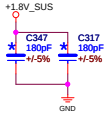
Bottomside Decoupling



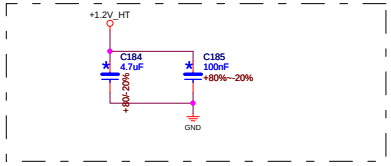
Decoupling Between Processor and DIMMs
Place as close to processor as possible.



Decoupling Between Processor and DIMMs



Place near processor on VLDT pour.



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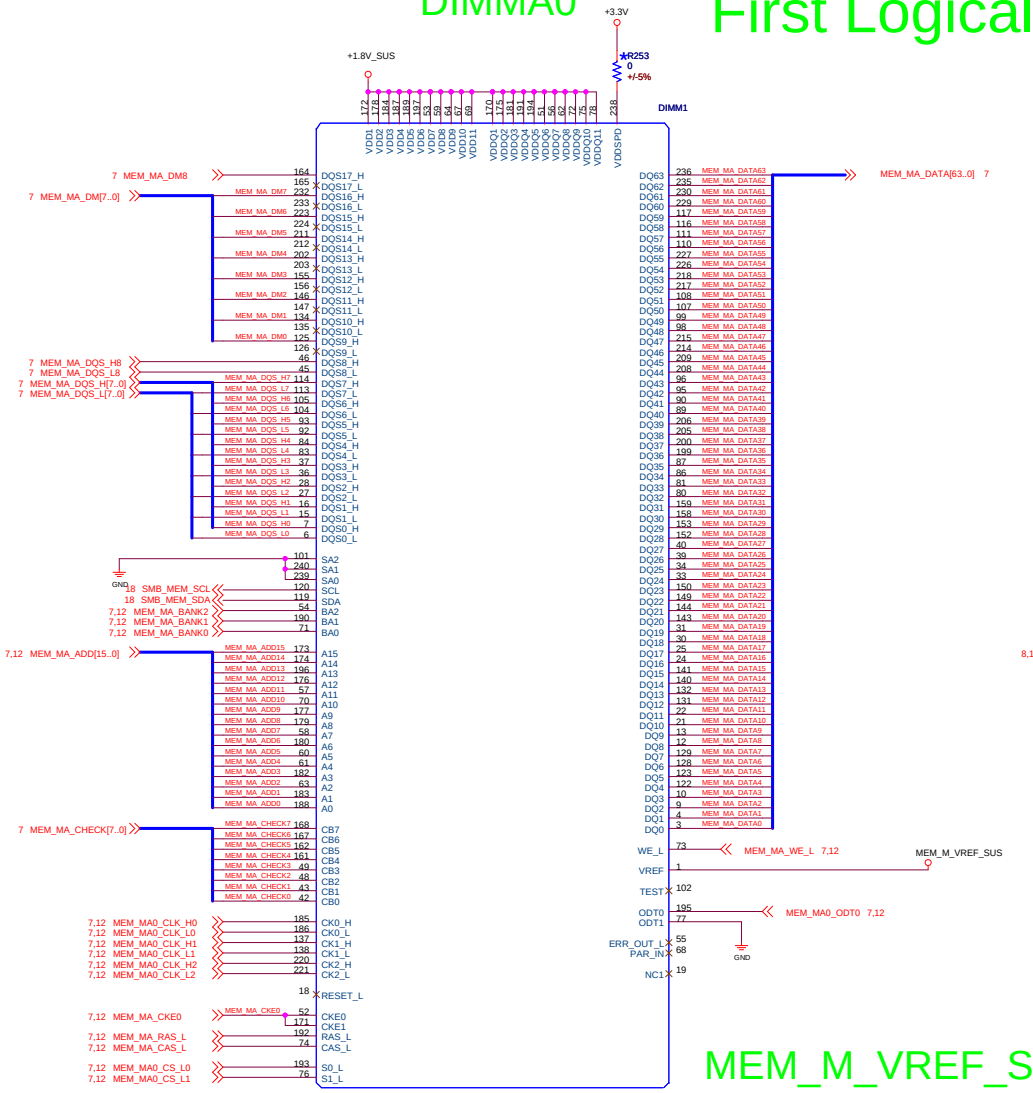
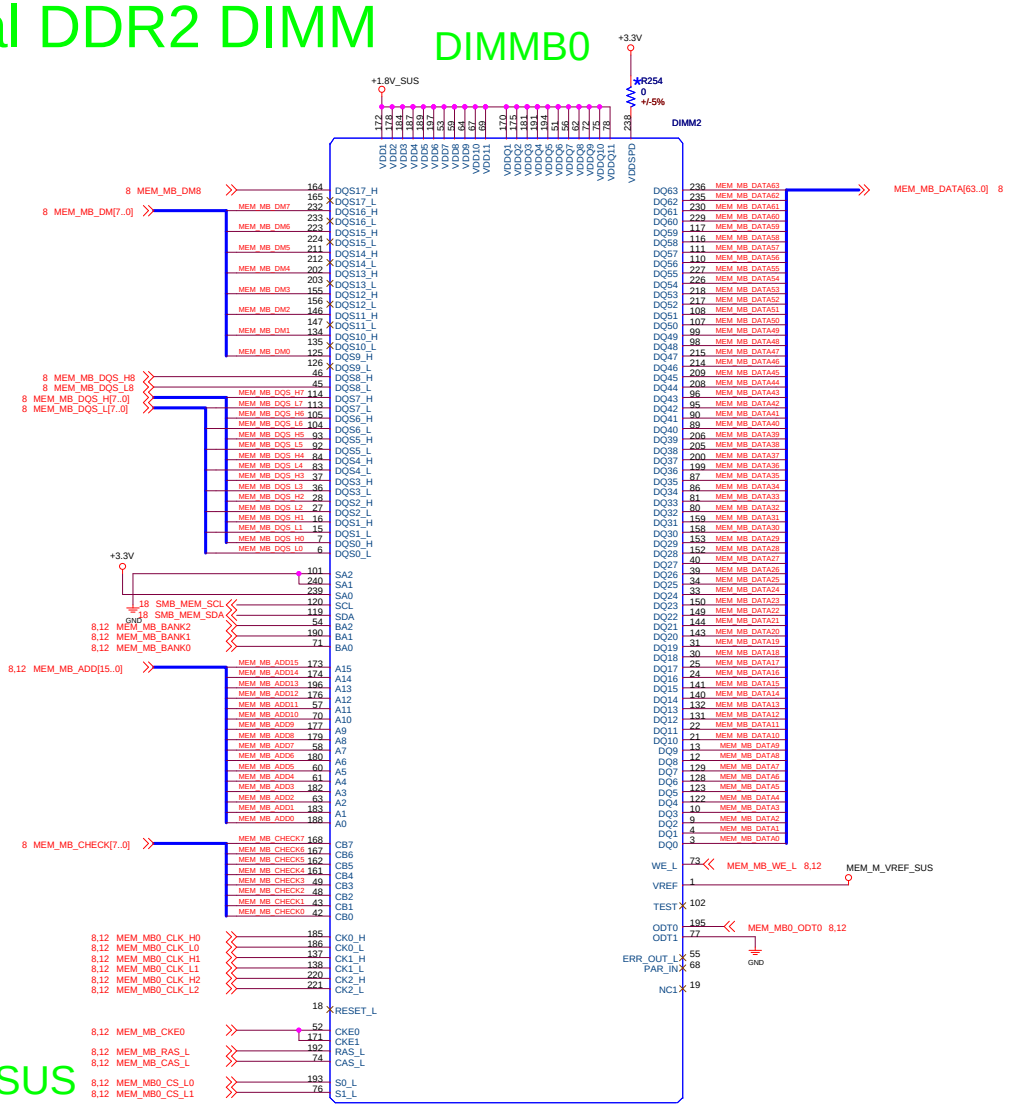
First Logical DDR2 DIMM

SMB_MEM BUS ADDRESS	
DIMM 0	1010 000
DIMM 1	1010 001
DIMM 2	1010 010
DIMM 3	1010 011

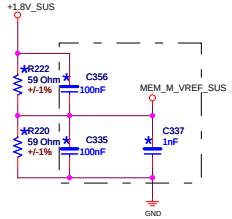
DIMMA0



DIMMB0



MEM_M_VREF_SUS



Layout: Place near DIMM sockets

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Title	DDR SDRAM DIMM 1 - 2	
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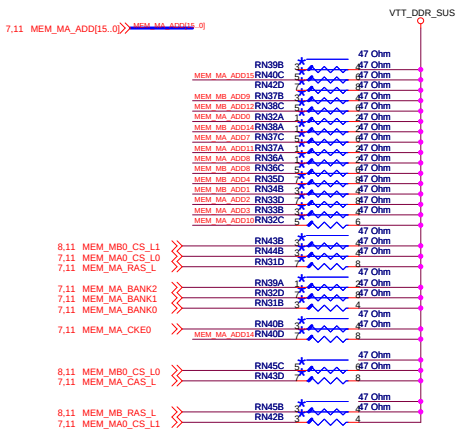
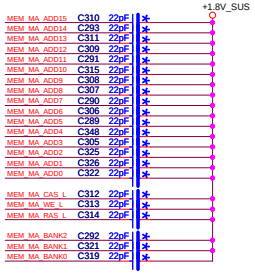
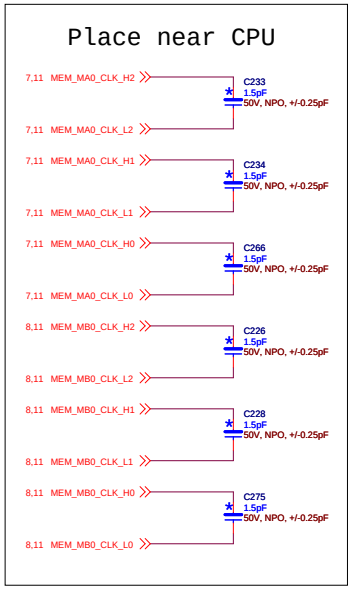
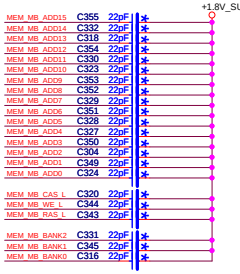
DDR2 Termination

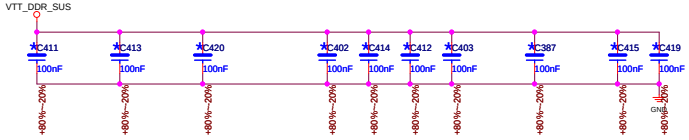


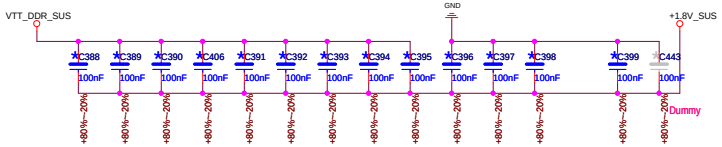






Layout: Spread out on VTT pour





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Title: DDR II terminator		
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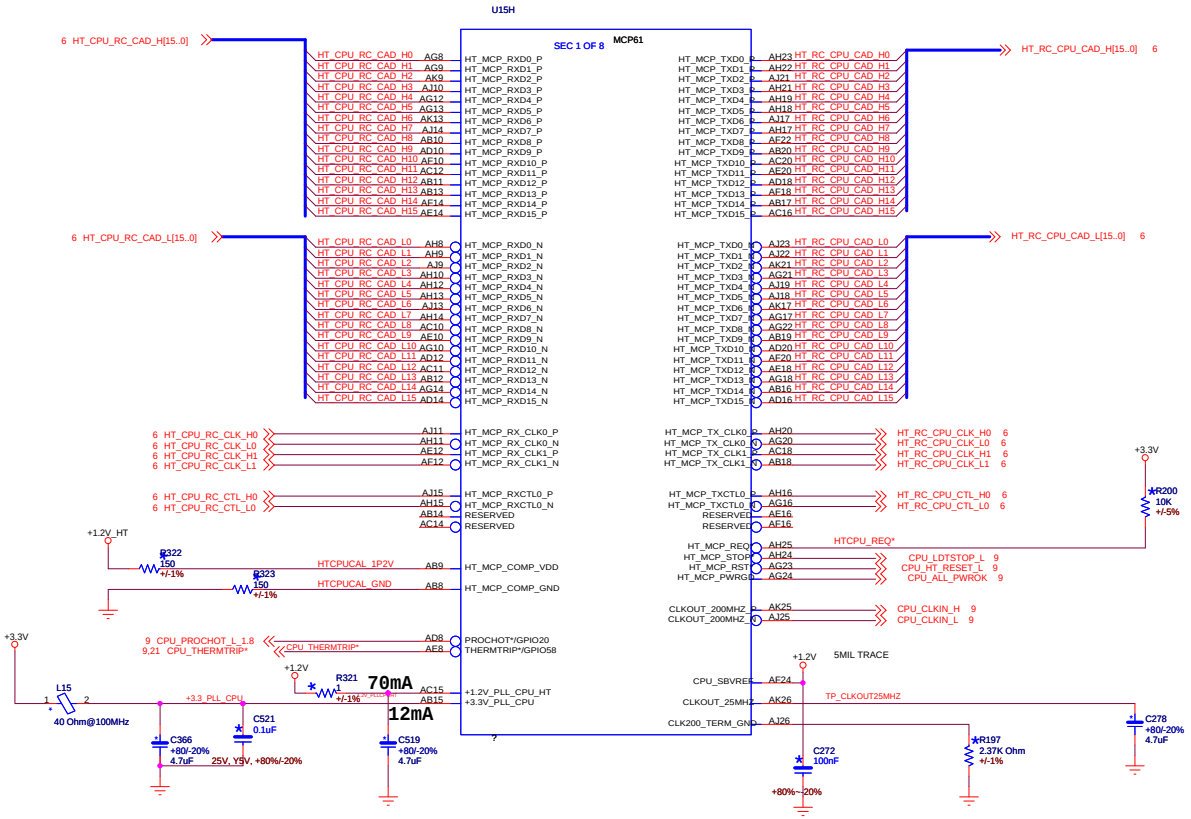

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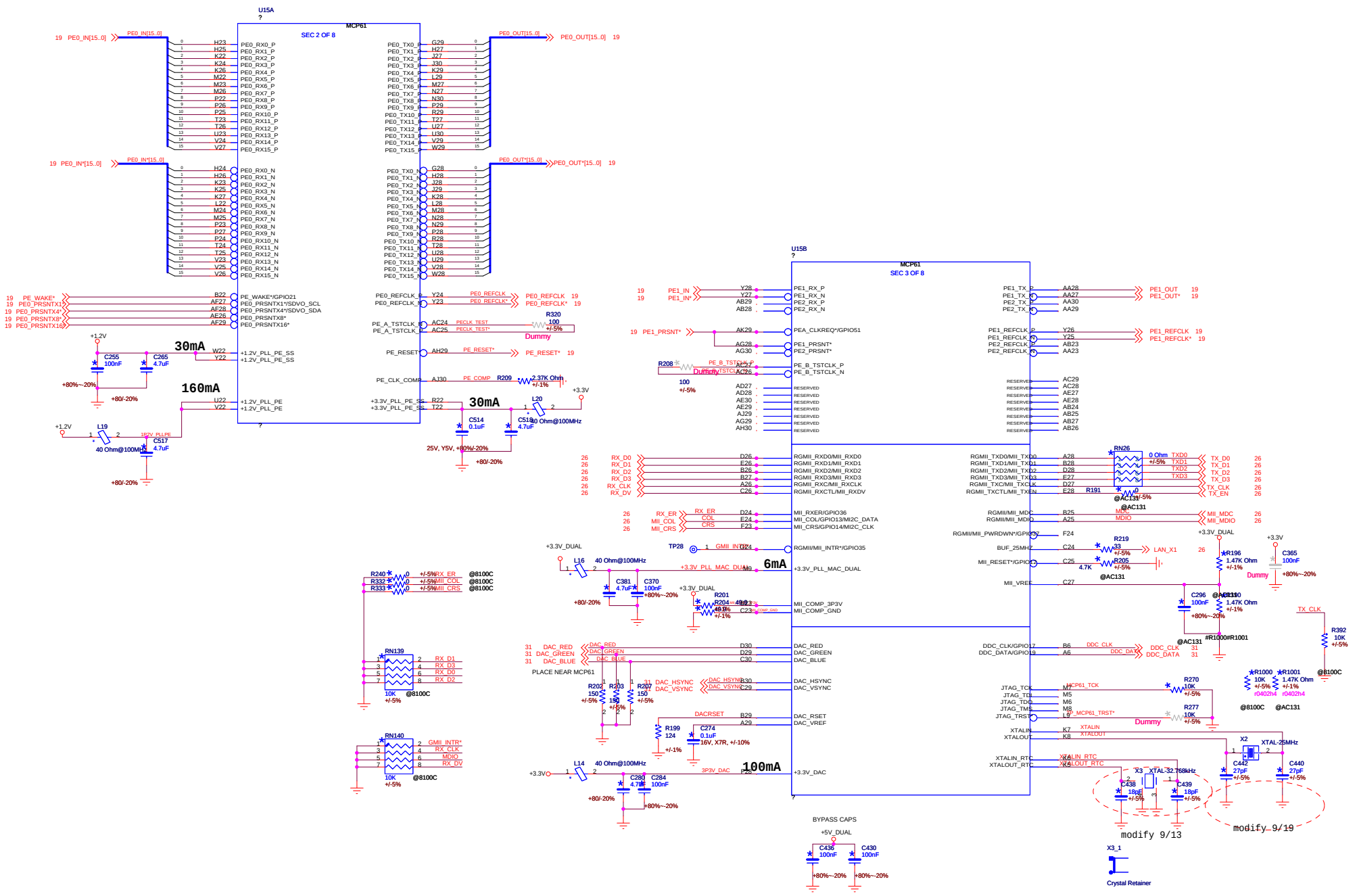

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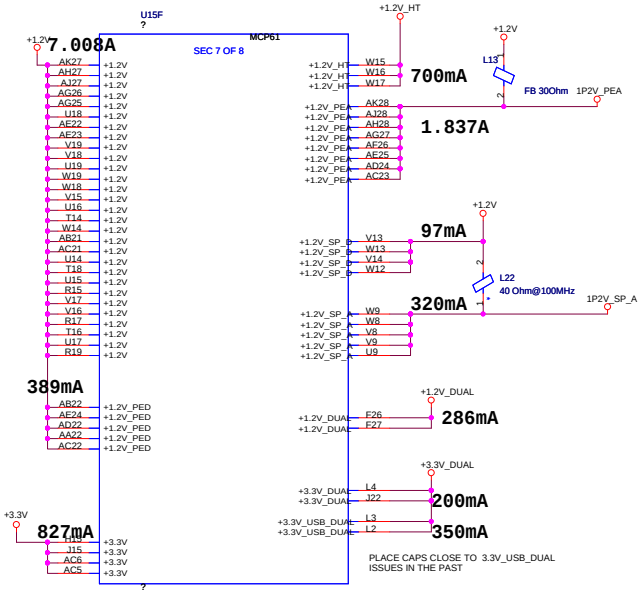
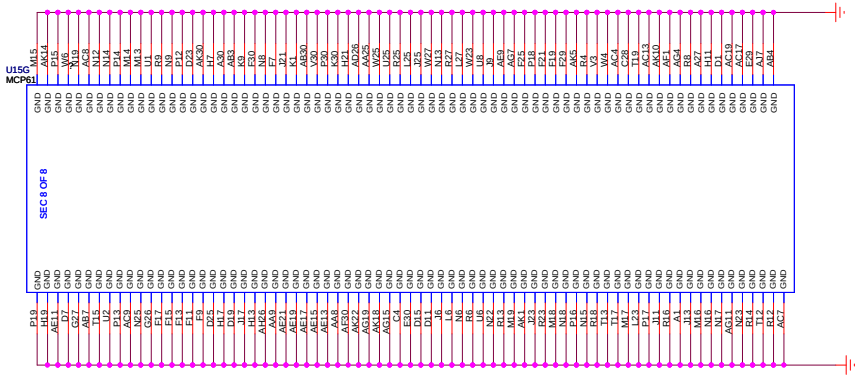
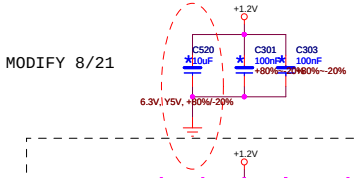
modify 8/20

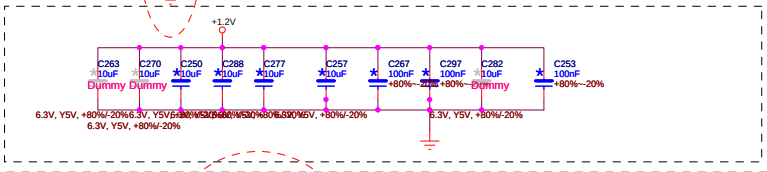


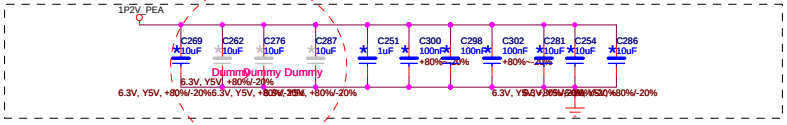


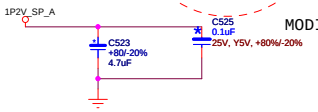
MCP61 DECOUPLING

MODIFY 8/21

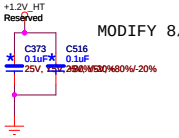




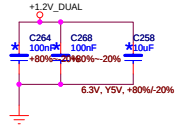


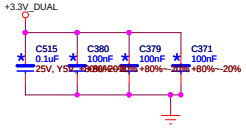


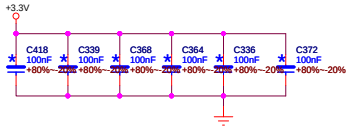
MODIFY 8/21



MODIFY 8/21







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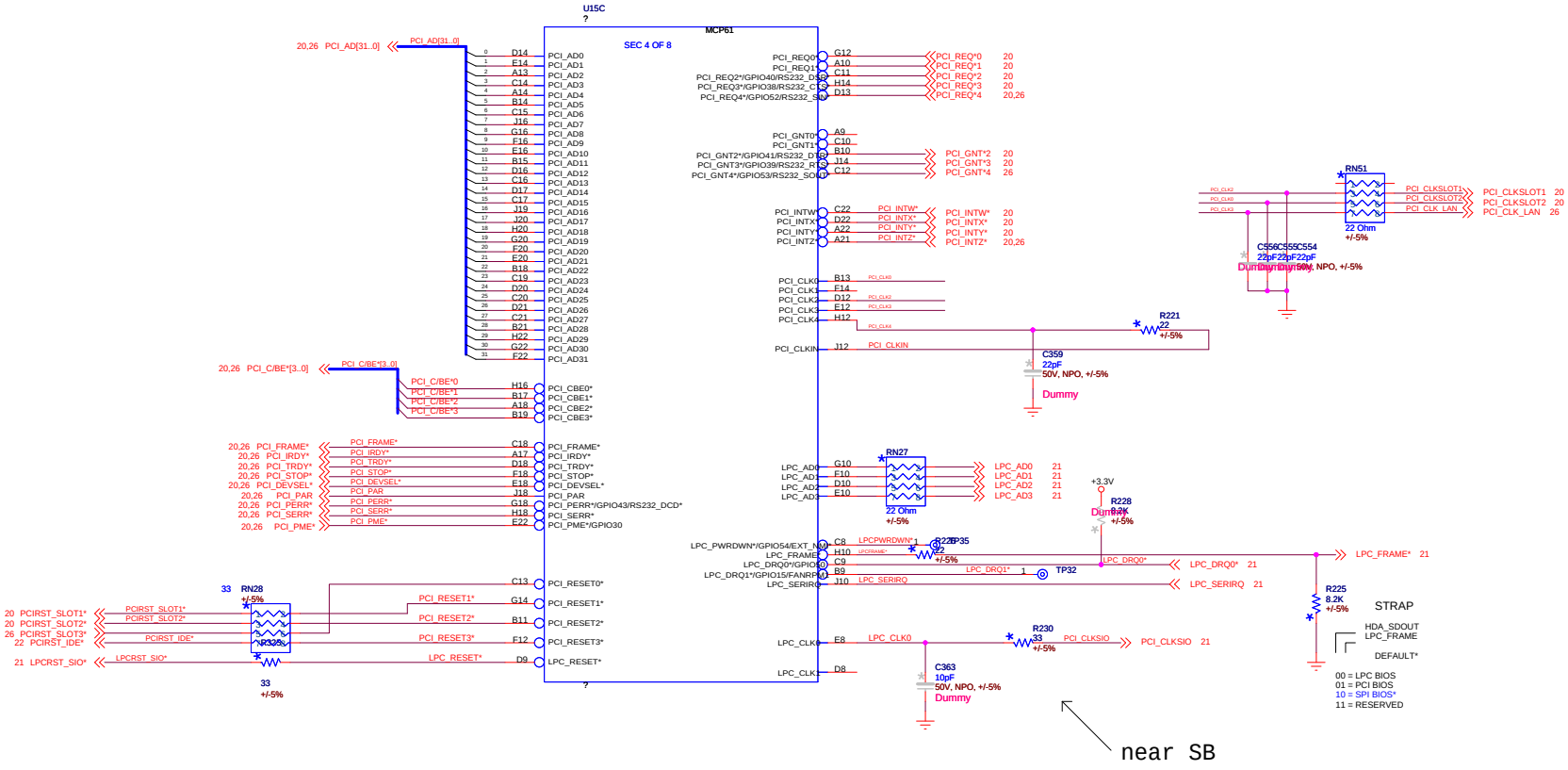

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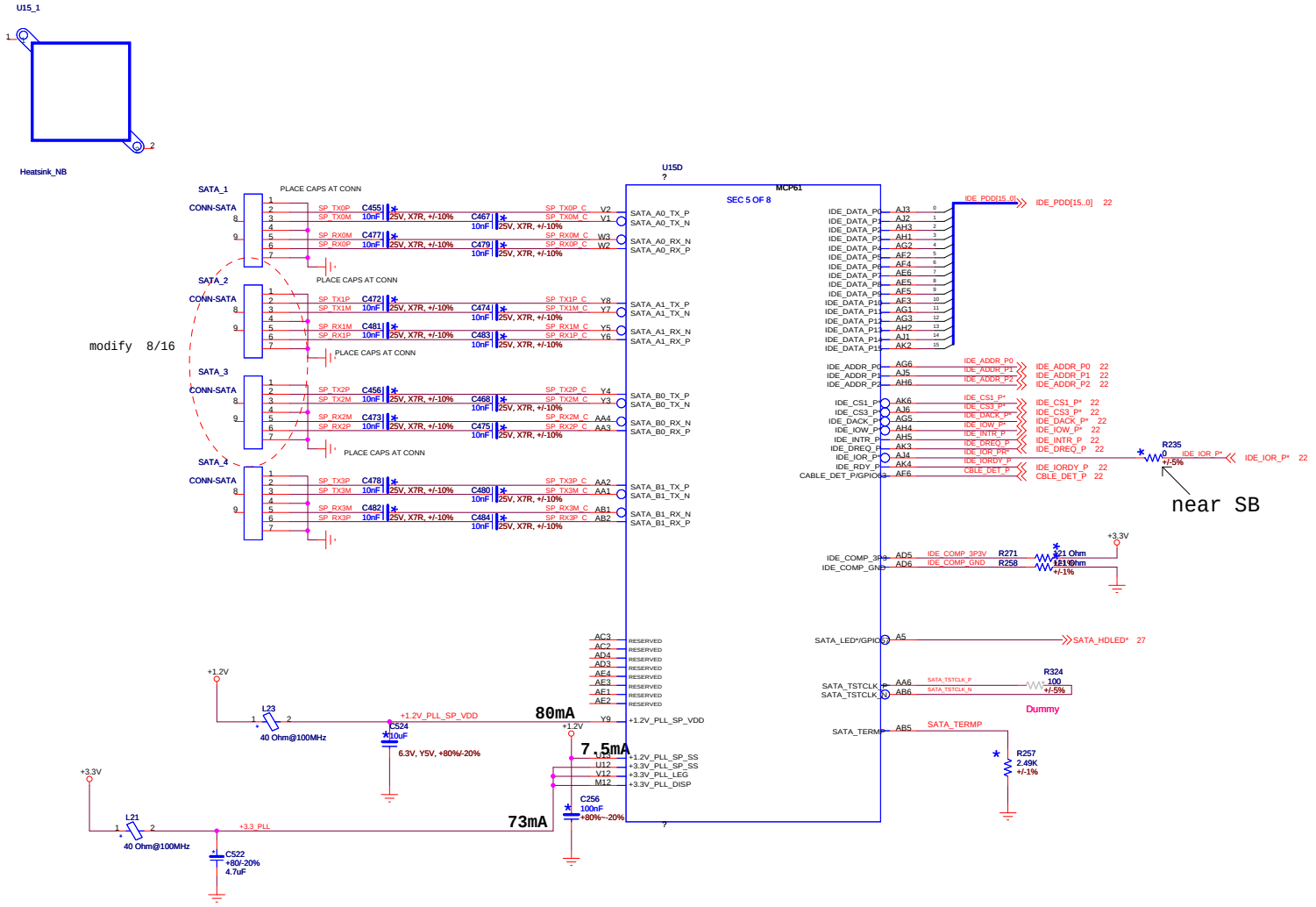
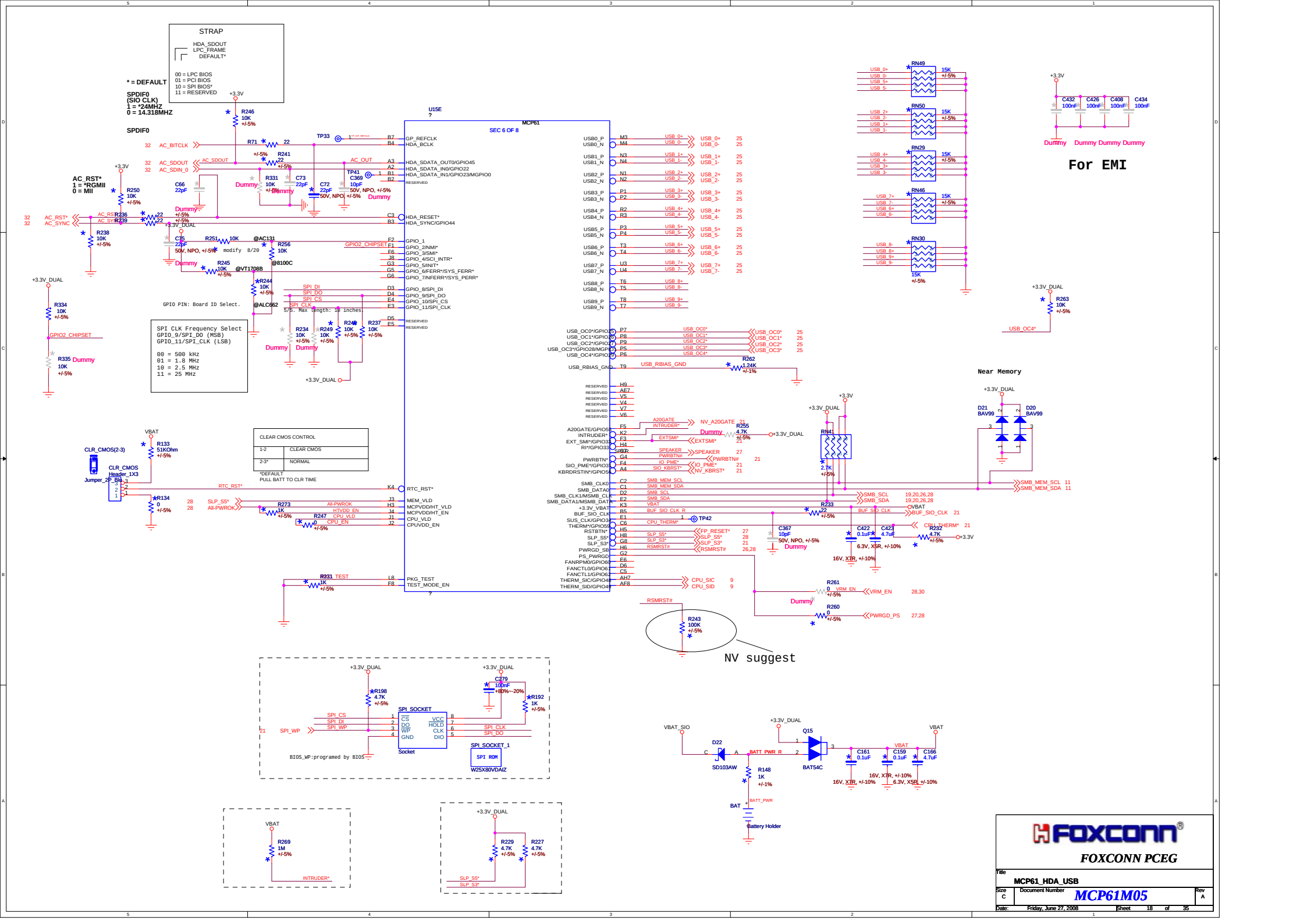


FOXCONN PCEG

Title	MCP61_SATA_IDE	
Size C	Document Number MCP61M05	Rev A
Date: Friday, June 27, 2008	Sheet 17 of 35	


STRAP
HDA_SDOUT
LPC_FRAME
DEFAULT*
00 = LPC BIOS
01 = PCI BIOS
10 = SPI BIOS*
11 = RESERVED
* = DEFAULT
SPDIF0
(SIO CLK)
1 = *24MHZ
0 = 14.318MHZ
SPDIF0
AC_RST*
1 = *RGMII
0 = MII
U15E
MCP61
SEC 6 OF 8
GPIO PIN: Board ID Select.
SPI CLK Frequency Select
GPIO_9/SPI_DO (MSB)
GPIO_11/SPI_CLK (LSB)
00 = 500 kHz
01 = 1.8 MHz
10 = 2.5 MHz
11 = 25 MHz
CLEAR CMOS CONTROL
1-2 CLEAR CMOS
2-3* NORMAL
*DEFAULT
PULL BATT TO CLR TIME
CLR_CMOS(2-3)
CLR_CMOS
Header_1X3
Jumper_2P_BM
SPI_SOCKET
Socket
SPI_SOCKET_1
SPI ROM
W25X80VDAIZ
BIOS_WP:programed by BIOS
SD103AW
BAT54C
Battery Holder
Near Memory
For EMI
NV suggest
FOXCONN PCEG
MCP61_HDA_USB
MCP61M05
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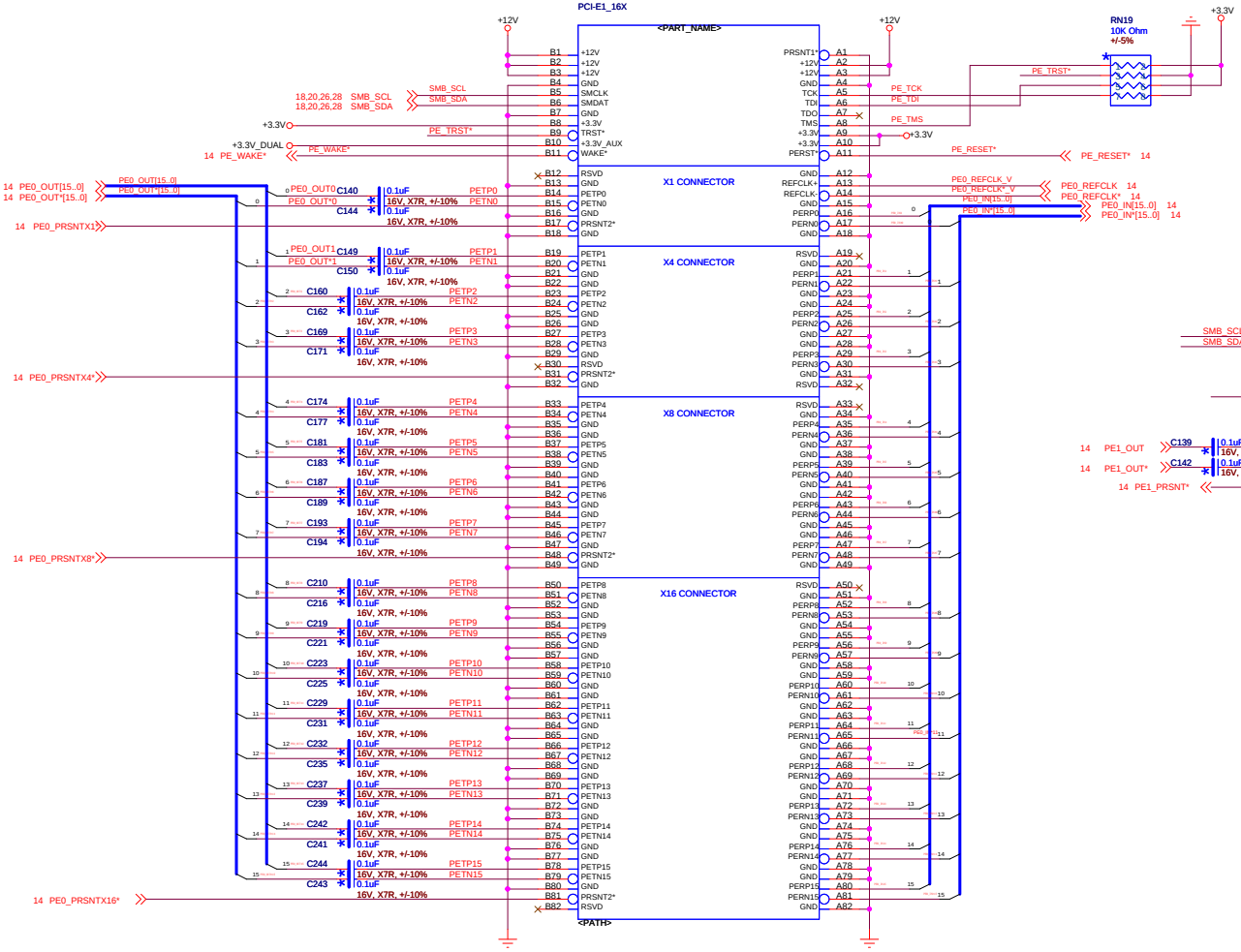
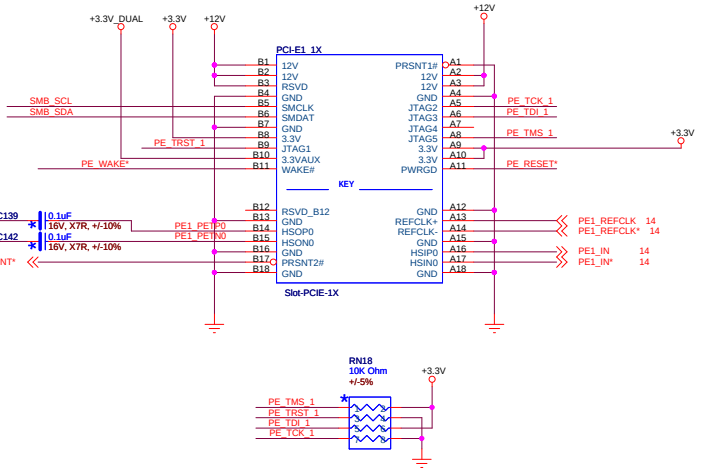
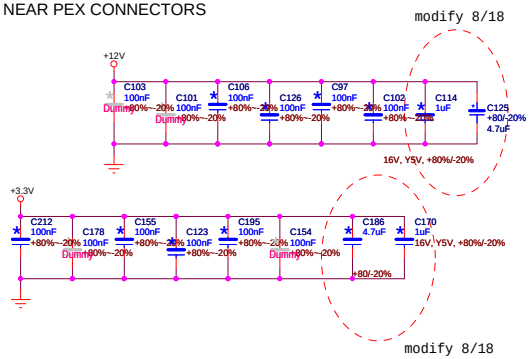
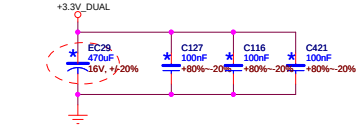




PLACE CAPS NEAR PEX CONNECTORS





FOXCONN PCEG

Title: PCI Express Slot x16 & X1

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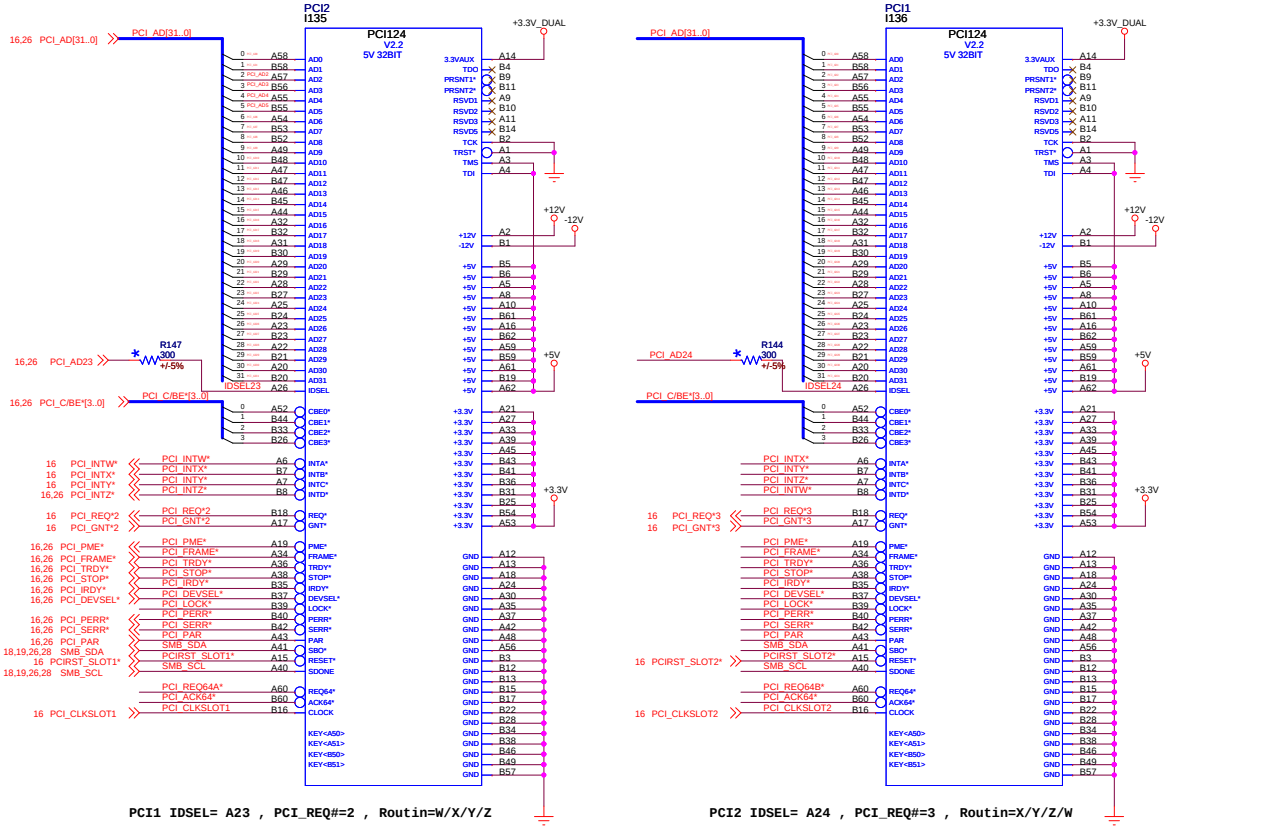
SLOT 2

IDSEL23

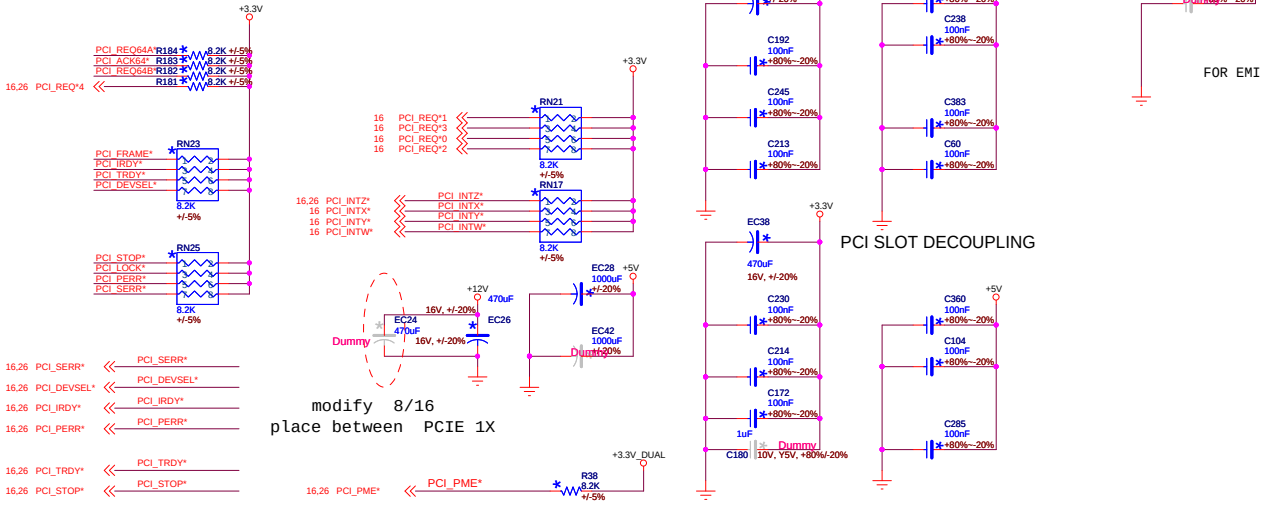
SLOT 1

IDSEL24



PCI1 IDSEL= A23 , PCI_REQ#=2 , Routin=W/X/Y/Z

PCI2 IDSEL= A24 , PCI_REQ#=3 , Routin=X/Y/Z/W



FOXCONN PCEG

Title: PCI Slot 12

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Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFFE_0000h~FFFF_FFFFh, 000F_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO1 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO2 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are open-drain.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

Note:

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

modify 8/16

modify 8/16

IT8716F-S/FX-L

Serial Port 1/2

Parallel Port

Power-on Control

MISC

SPI I/F

Floppy I/F

LPC I/F

Hardware Monitor

KB/MS

24MHz

IR Connector

Near SIO (U22)

Near CPU

Near IO

output to SB

POWER ON SCHEME

MCP61

IT8716F

W83304

ATX Power Supply

Power button input

Dummy

FOXCONN PCEG

SIO IT8716F

MCP61M05

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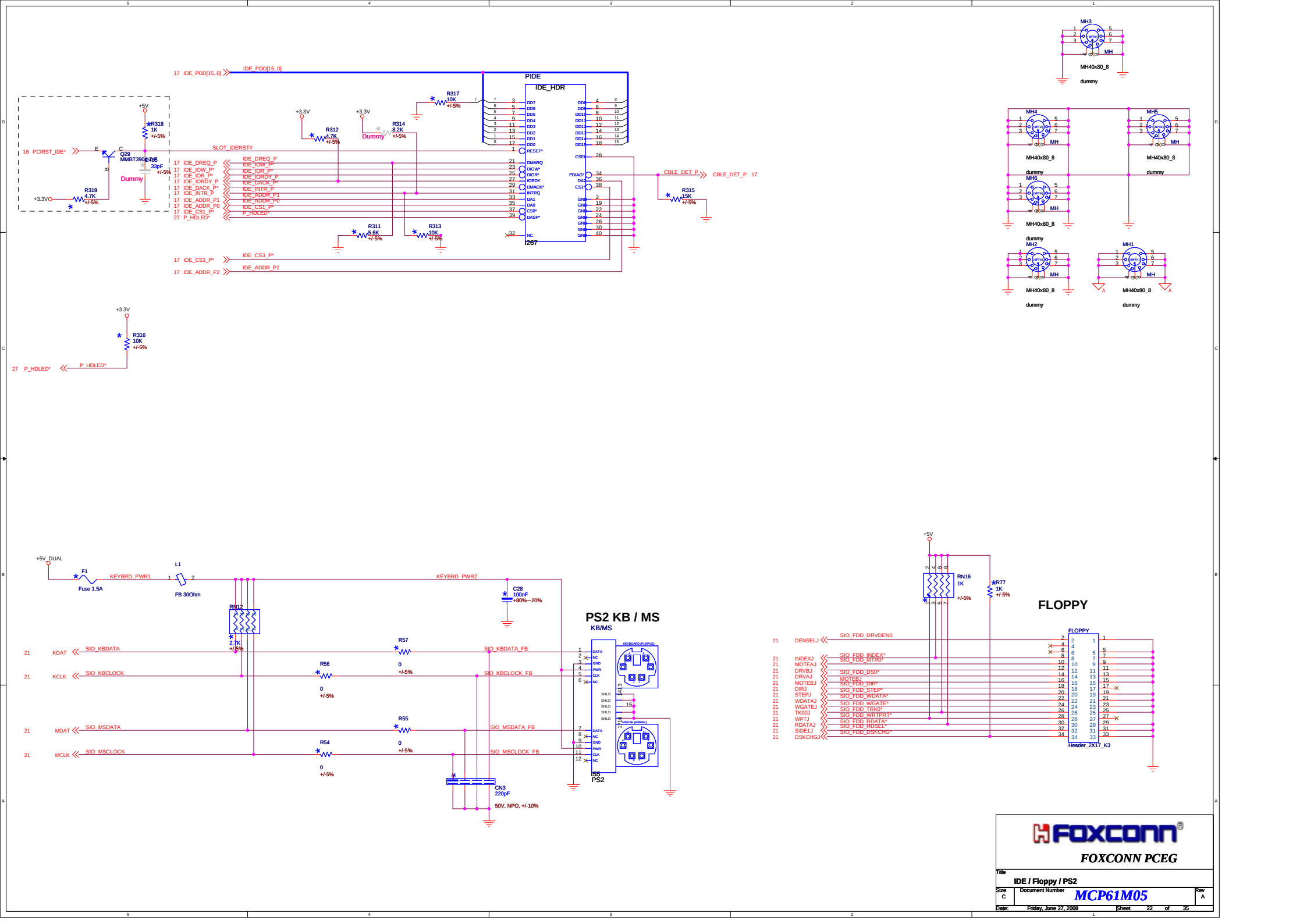

FOXCONN PCEG

Title	IDE / Floppy / PS2	
Size C	Document Number MCP61M05	Rev A
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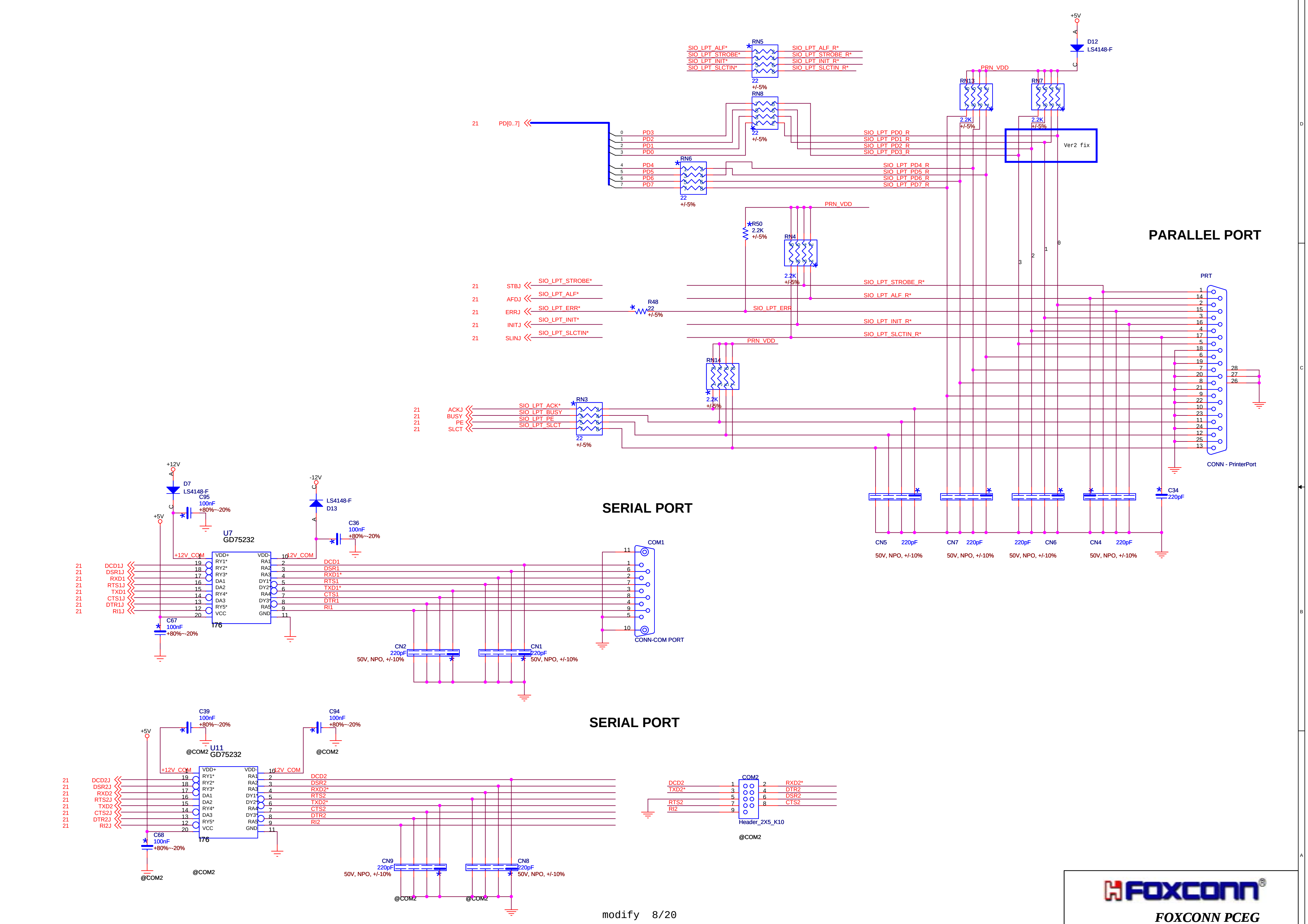
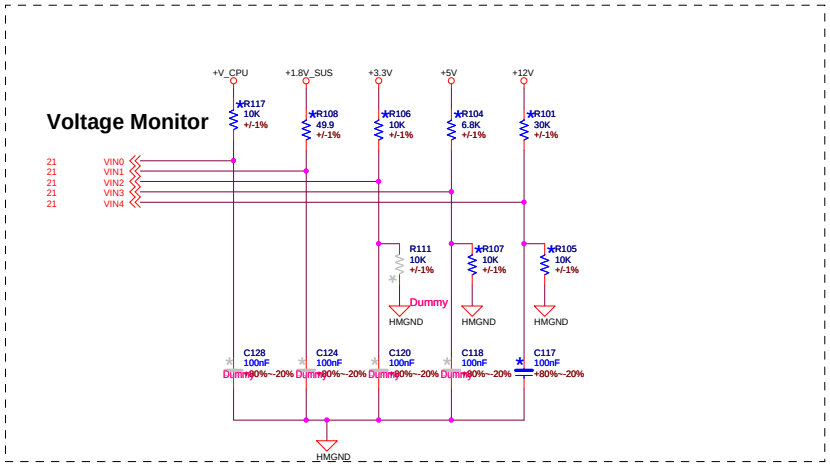
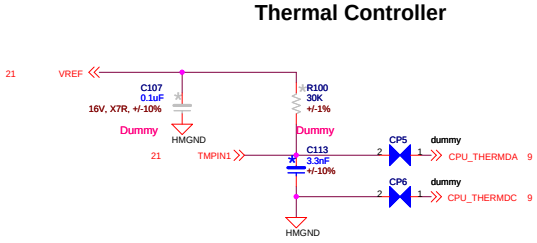
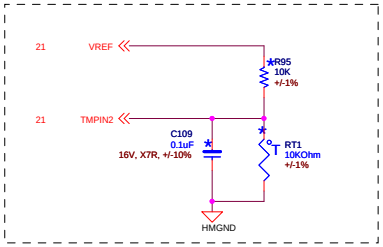
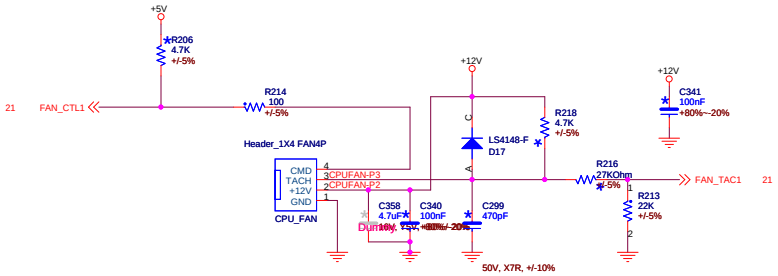


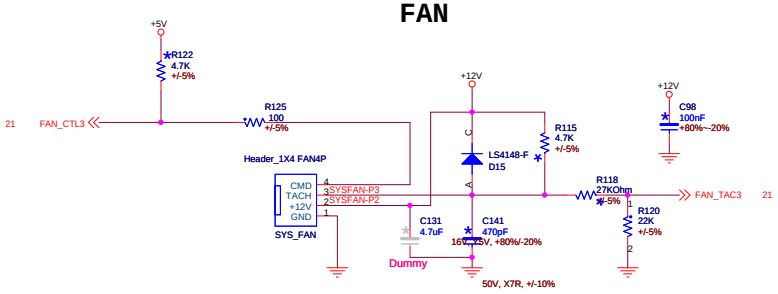
FOXCONN PCEG	
Title	Parallel / Gamr Port
Size C	Document Number MCP61M05	Rev A
Date: Friday, June 27, 2008	Sheet 23 of 35











Need to check GPIO default value at power-on .

FOXCONN PCEG

Title: Hardware Monitor / Over Volt

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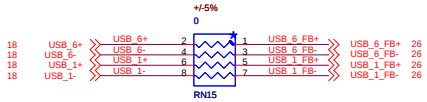
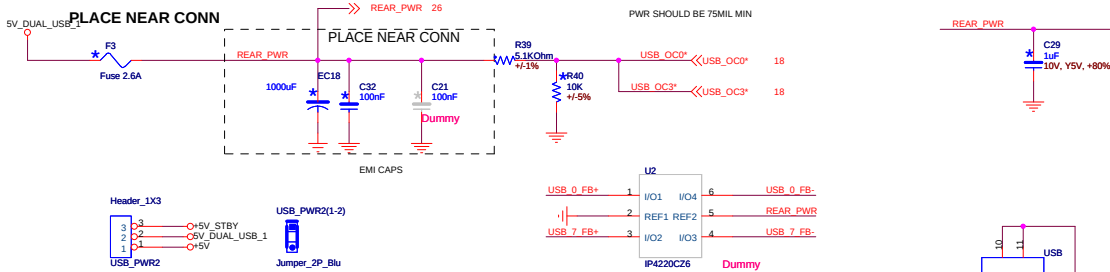
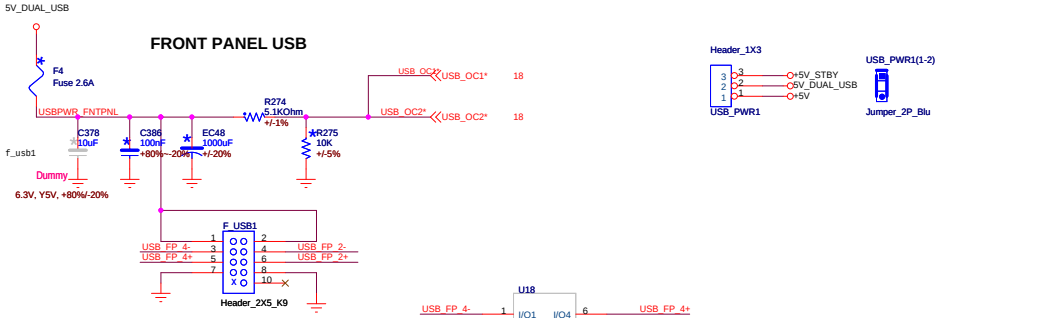
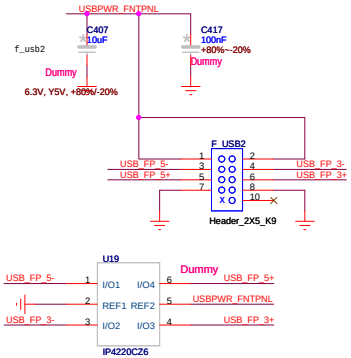
BACK PANEL LAN/USB -> Near Connector

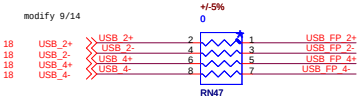
Connect to rear LAN/USB port



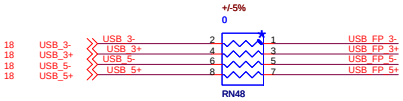








modify 9/13



FOXCONN PCEG

Title: USB Connector

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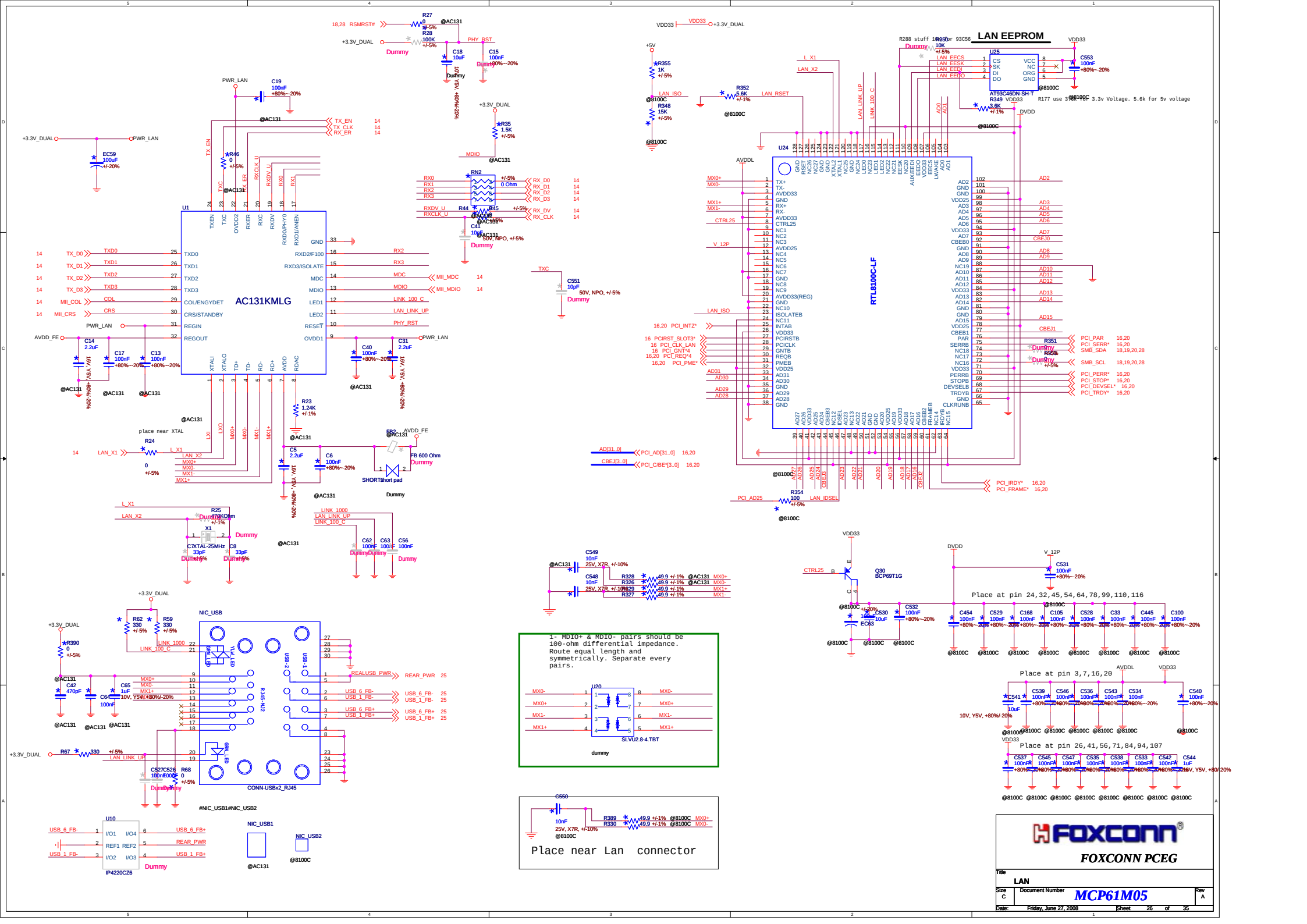
Date: Friday, June 27, 2008 | Sheet 25 of 35


LAN EEPROM
AC131KMLG
RTL8100C-LF
U1
U24
U25
AT93C46DN-SH-T
Place near Lan connector
1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.
SLVU2.8-4.TBT
CONN-USBx2_RJ45
IP4220CZ6
FOXCONN PCEG
LAN
MCP61M05
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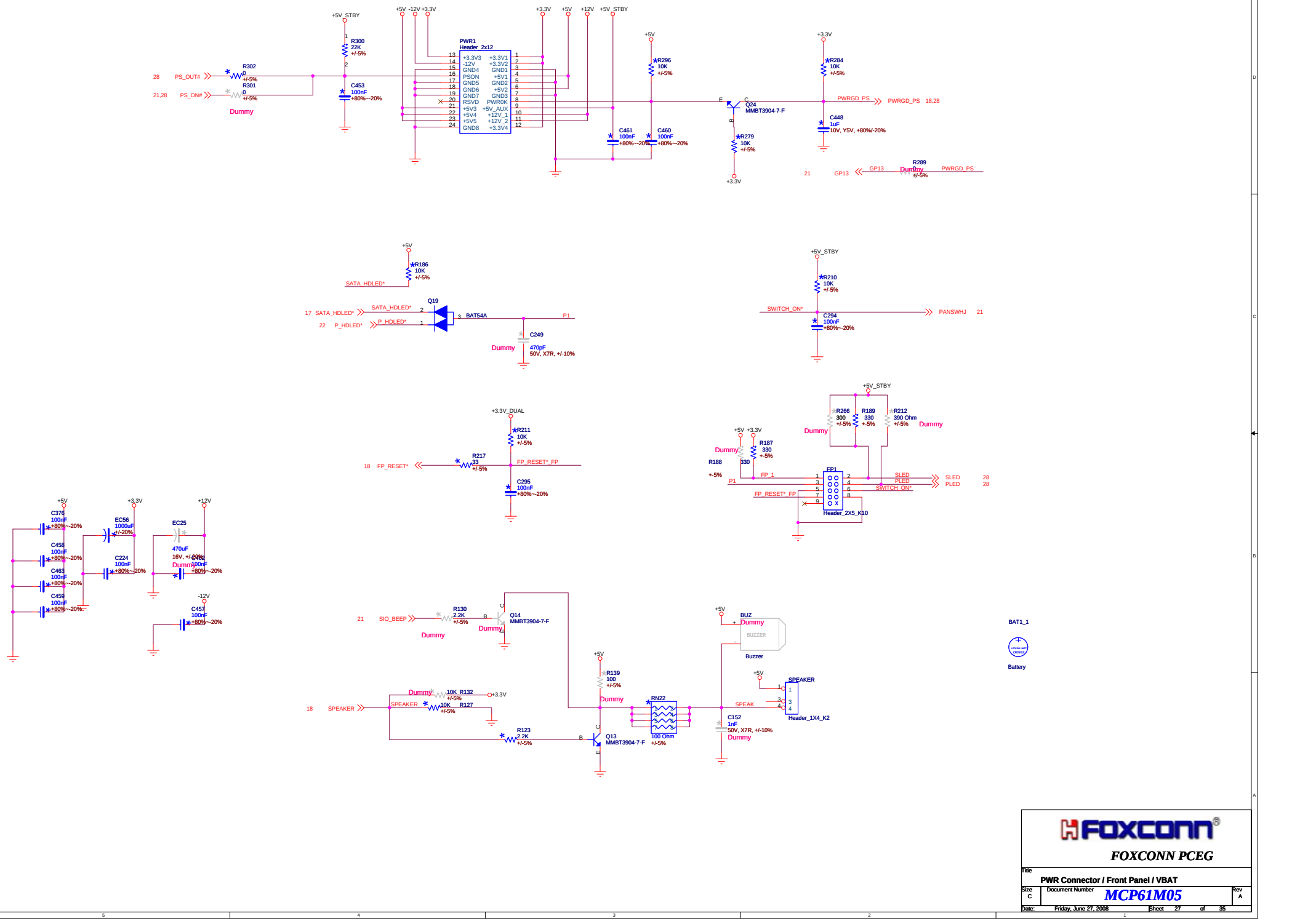

FOXCONN PCEG

Title	PWR Connector / Front Panel / VBAT	
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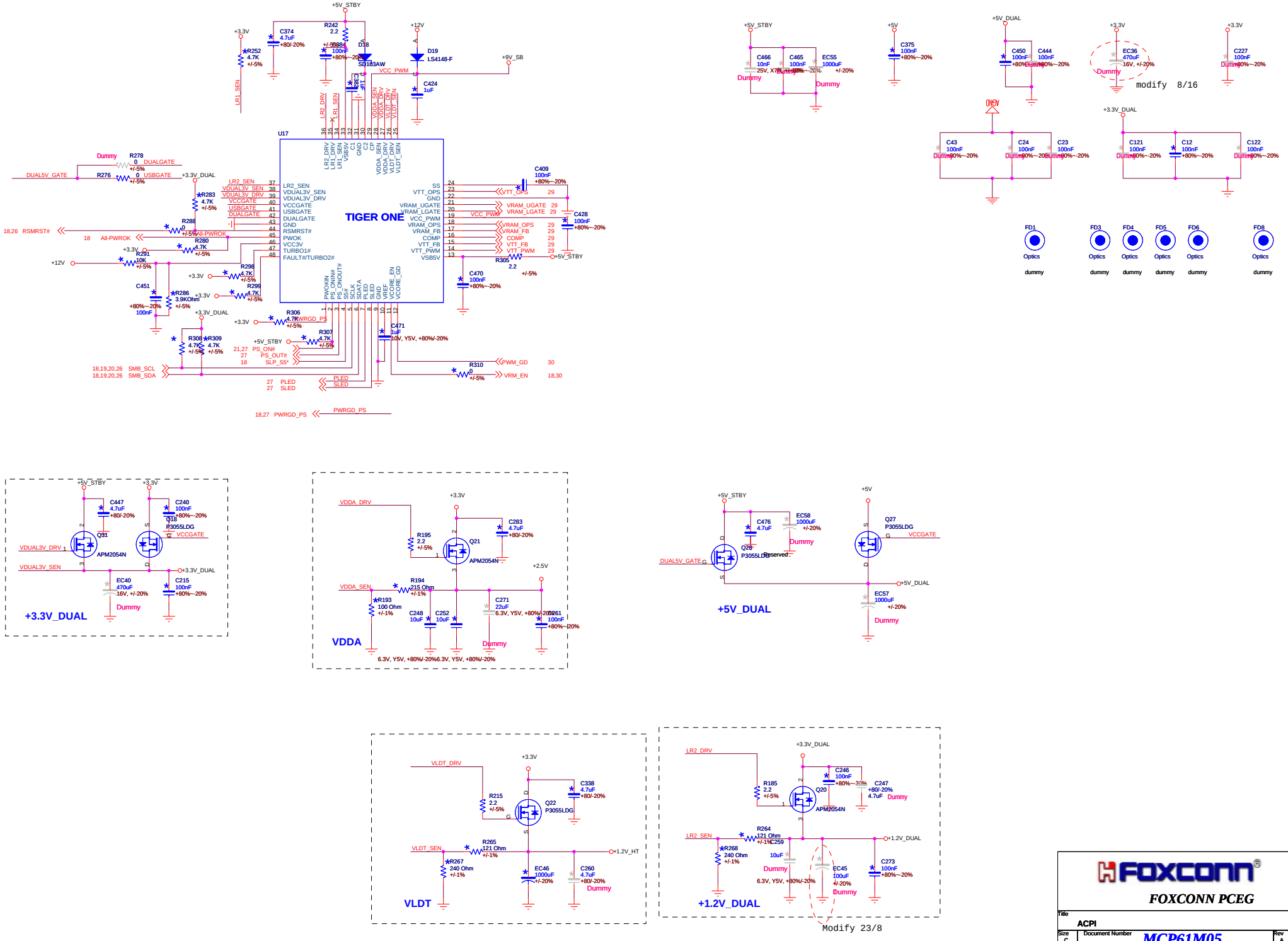

Title	ACPI
Size	C
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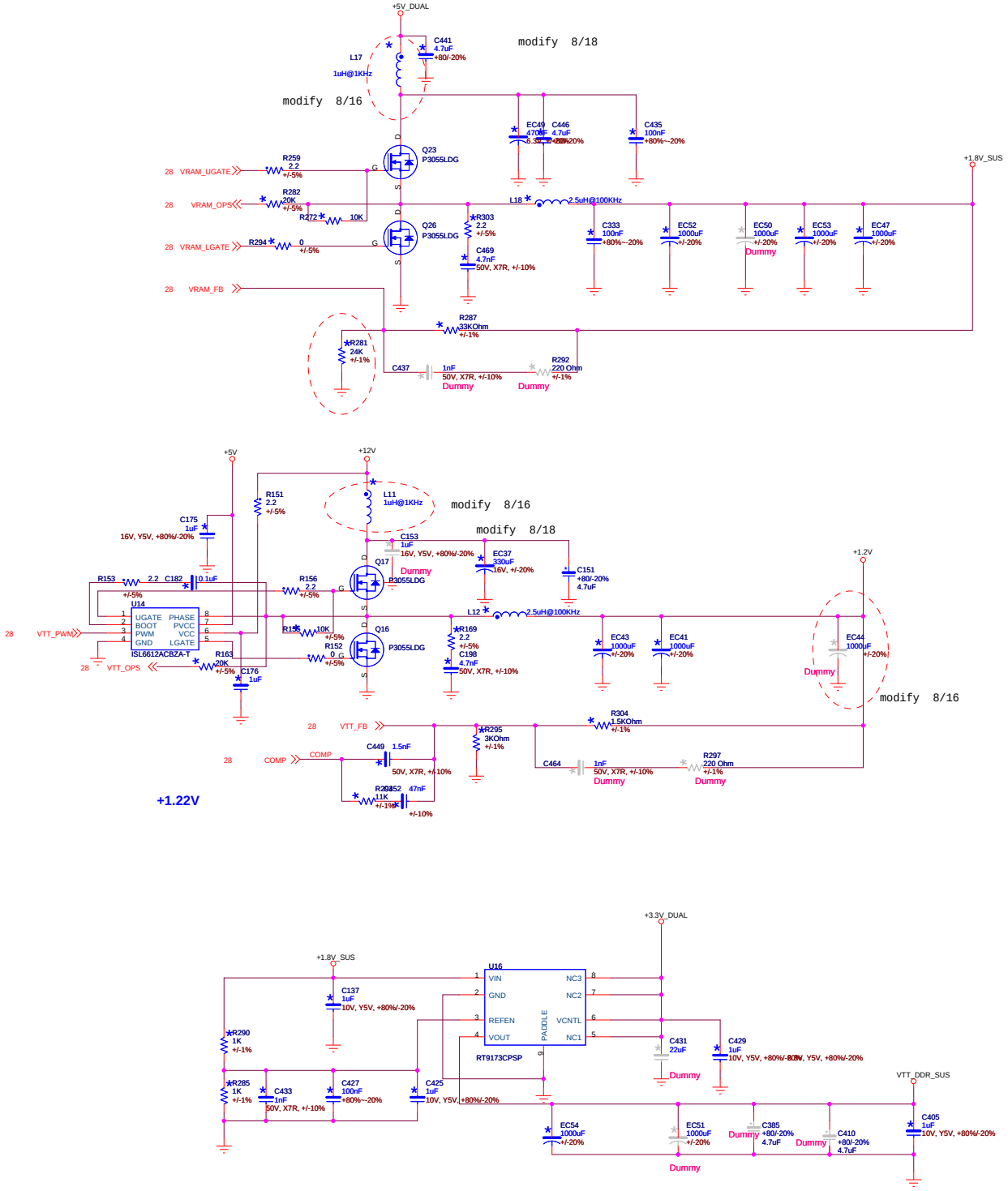
FOXCONN PCEG



FOXCONN PCEG

Title	MCP CORE +1.2V	
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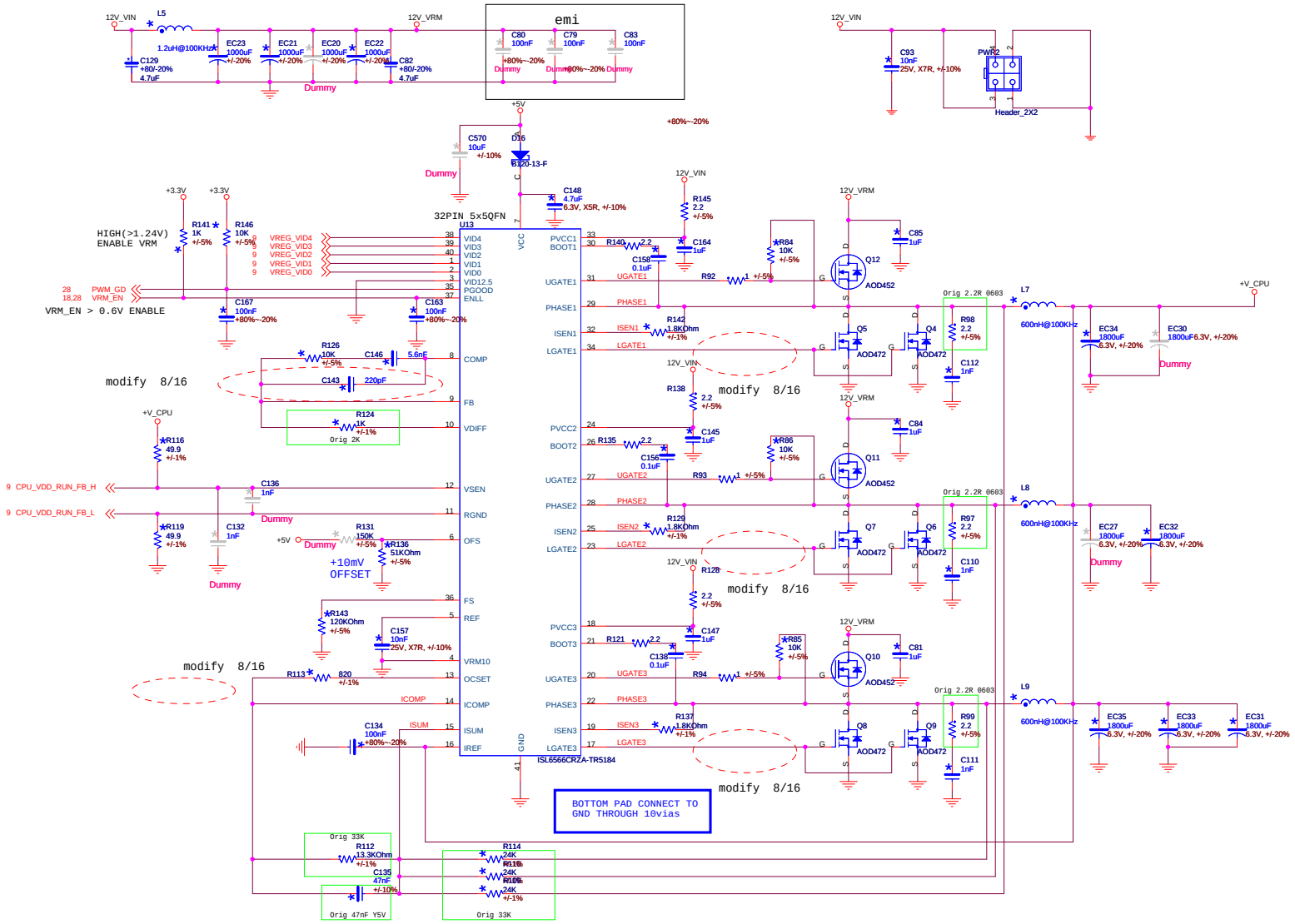

FOXCONN PCEG

Title: VRM			
Size: C	Document Number: MCP61M05		Rev: A
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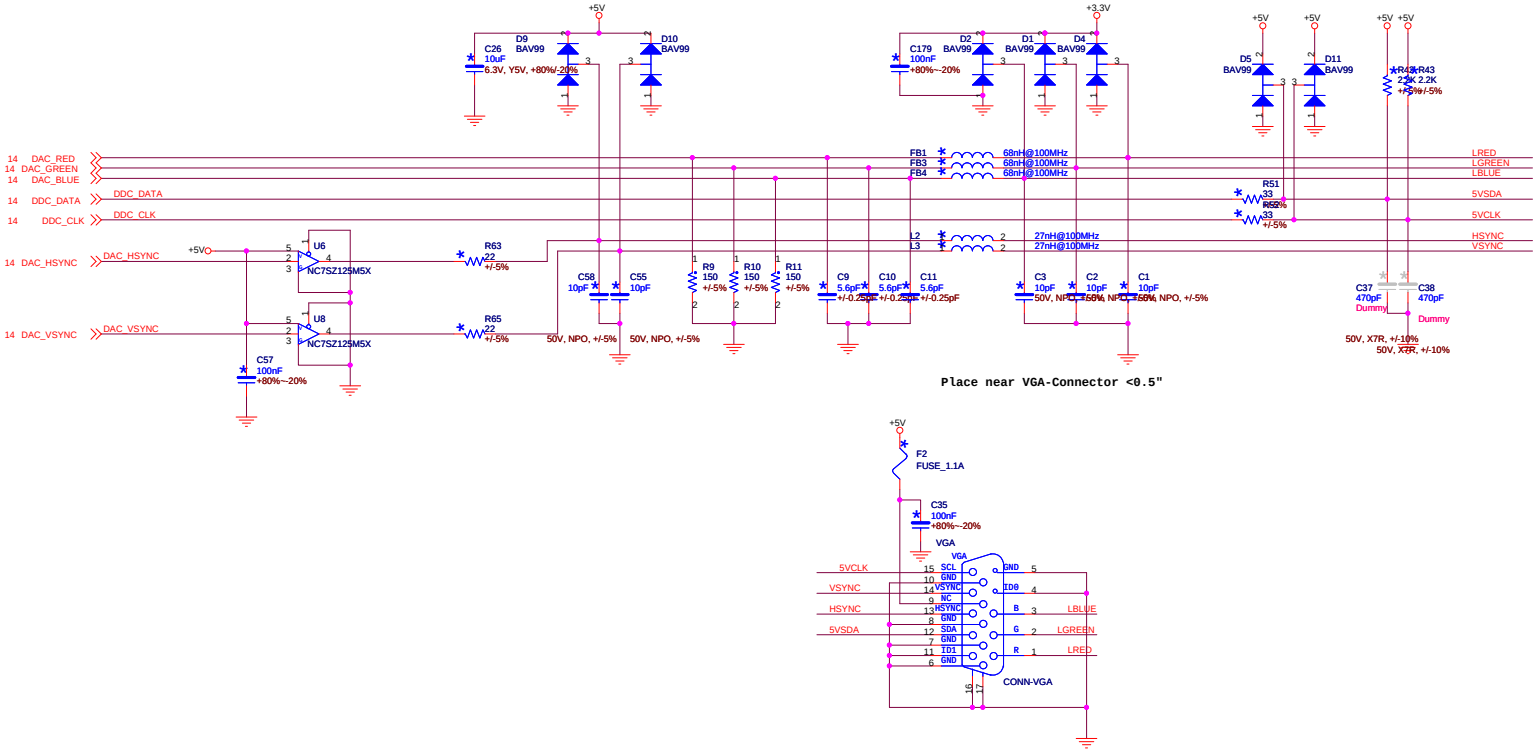

FOXCONN PCEG

Title: VGA		
Size: C	Document Number: MCP61M05	Rev: A
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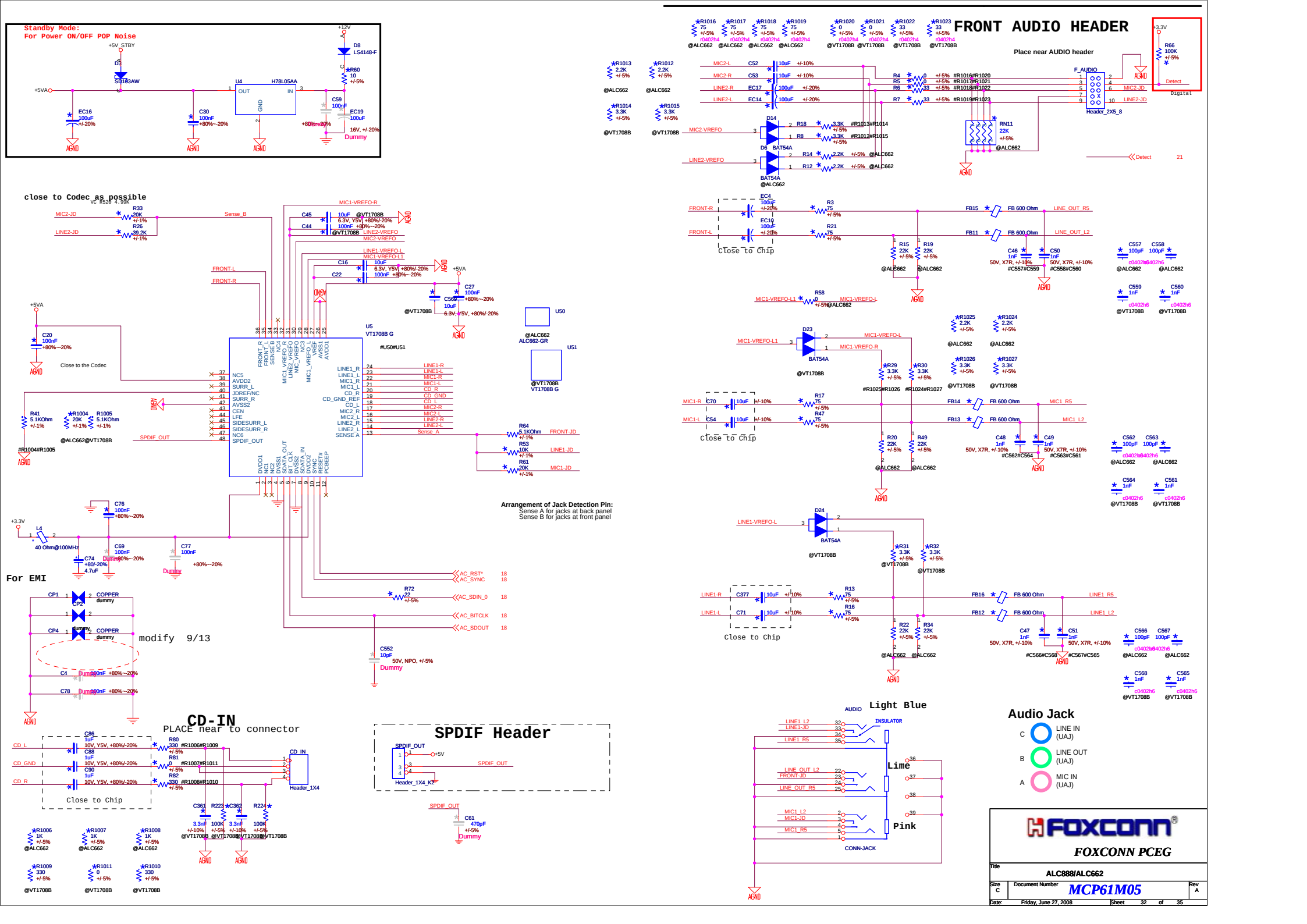
Standby Mode:
For Power ON/OFF POP Noise
+5V_STBY
D5
SD103AW
+5VA
U4
H78L05AA
OUT
IN
GND
EC16
100uF
+/-20%
C30
100nF
+80%~-20%
C59
100nF
EC19
100uF
16V, +/-20%
Dummy
AGND
+12V
D8
LS4148-F
R60
10
+/-5%
close to Codec as possible
MIC2-JD
LINE2-JD
R33
20K
+/-1%
R26
39.2K
+/-1%
Sense_B
MIC1-VREFO-R
C45
10uF
6.3V, Y5V, +80%/-20%
C44
100nF
+80%~-20%
@VT1708B
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO-L
MIC1-VREFO-L1
C16
10uF
C22
100nF
FRONT-L
FRONT-R
DNEN
C27
100nF
C563
10uF
6.3V, Y5V, +80%/-20%
U5
VT1708B G
#U50#U51
U50
@ALC662
ALC662-GR
U51
@VT1708B
VT1708B G
C20
100nF
Close to the Codec
R41
5.1KOhm
R1004
20K
R1005
5.1KOhm
@ALC662@VT1708B
#R1004#R1005
SPDIF_OUT
LINE1_R
LINE1_L
MIC1_R
MIC1_L
CD_R
CD_GND_REF
CD_L
MIC2_R
MIC2_L
LINE2_R
LINE2_L
Sense_A
R64
5.1KOhm
FRONT-JD
R53
10K
LINE1-JD
R61
20K
MIC1-JD
C76
100nF
L4
40 Ohm@100MHz
C74
+80/-20%
4.7uF
C69
100nF
C77
100nF
Dummy
AC_RST*
AC_SYNC
AC_SDIN_0
AC_BITCLK
AC_SDOUT
R72
22
+/-5%
C552
10pF
50V, NPO, +/-5%
Arrangement of Jack Detection Pin:
Sense A for jacks at back panel
Sense B for jacks at front panel
For EMI
CP1
CP2
CP4
COPPER
dummy
modify 9/13
C4
C78
CD-IN
PLACE near to connector
CD_L
CD_GND
CD_R
C86
1uF
C88
C90
10V, Y5V, +80%/-20%
Close to Chip
R80
330
#R1006#R1009
R81
#R1007#R1011
R82
#R1008#R1010
CD_IN
Header_1X4
C361
3.3nF
R223
100K
C362
R224
R1006
1K
R1007
R1008
R1009
R1011
R1010
SPDIF Header
SPDIF_OUT
+5V
Header_1X4_K2
C61
470pF
FRONT AUDIO HEADER
Place near AUDIO header
R1016
R1017
R1018
R1019
R1020
R1021
R1022
R1023
@ALC662
@VT1708B
R1013
R1012
R1014
R1015
MIC2-L
MIC2-R
LINE2-R
LINE2-L
C52
C53
EC17
EC14
10uF
100uF
+/-10%
+/-20%
R4
R5
R6
R7
#R1016#R1020
#R1017#R1021
#R1018#R1022
#R1019#R1023
F_AUDIO
Header_2X5_8
MIC2-JD
LINE2-JD
D14
D6
BAT54A
R18
R8
R14
R12
3.3K
2.2K
#R1013#R1014
#R1012#R1015
RN11
22K
Detect
21
FRONT-R
FRONT-L
EC4
EC10
R3
R21
75
Close to Chip
FB15
FB11
FB 600 Ohm
LINE_OUT_R5
LINE_OUT_L2
R15
R19
C46
1nF
50V, X7R, +/-10%
#C557#C559
C50
#C558#C560
C557
C558
C559
C560
c0402h6
MIC1-VREFO-L1
R58
MIC1-VREFO-L
R1025
R1024
R1026
R1027
D23
R29
R30
#R1025#R1026
#R1024#R1027
MIC1-R
MIC1-L
C70
C54
R17
R47
FB14
FB13
MIC1_R5
MIC1_L2
R20
R49
C48
C49
#C562#C564
#C563#C561
C562
C563
C564
C561
D24
R31
R32
LINE1-R
LINE1-L
C377
C71
R13
R16
FB16
FB12
LINE1_R5
LINE1_L2
R22
R34
C47
C51
#C566#C568
#C567#C565
C566
C567
C568
C565
AUDIO
Light Blue
INSULATOR
Lime
Pink
CONN-JACK
Audio Jack
C
LINE IN
(UAJ)
B
LINE OUT
(UAJ)
A
MIC IN
(UAJ)
FOXCONN
FOXCONN PCEG
Title
ALC888/ALC662
Size
C
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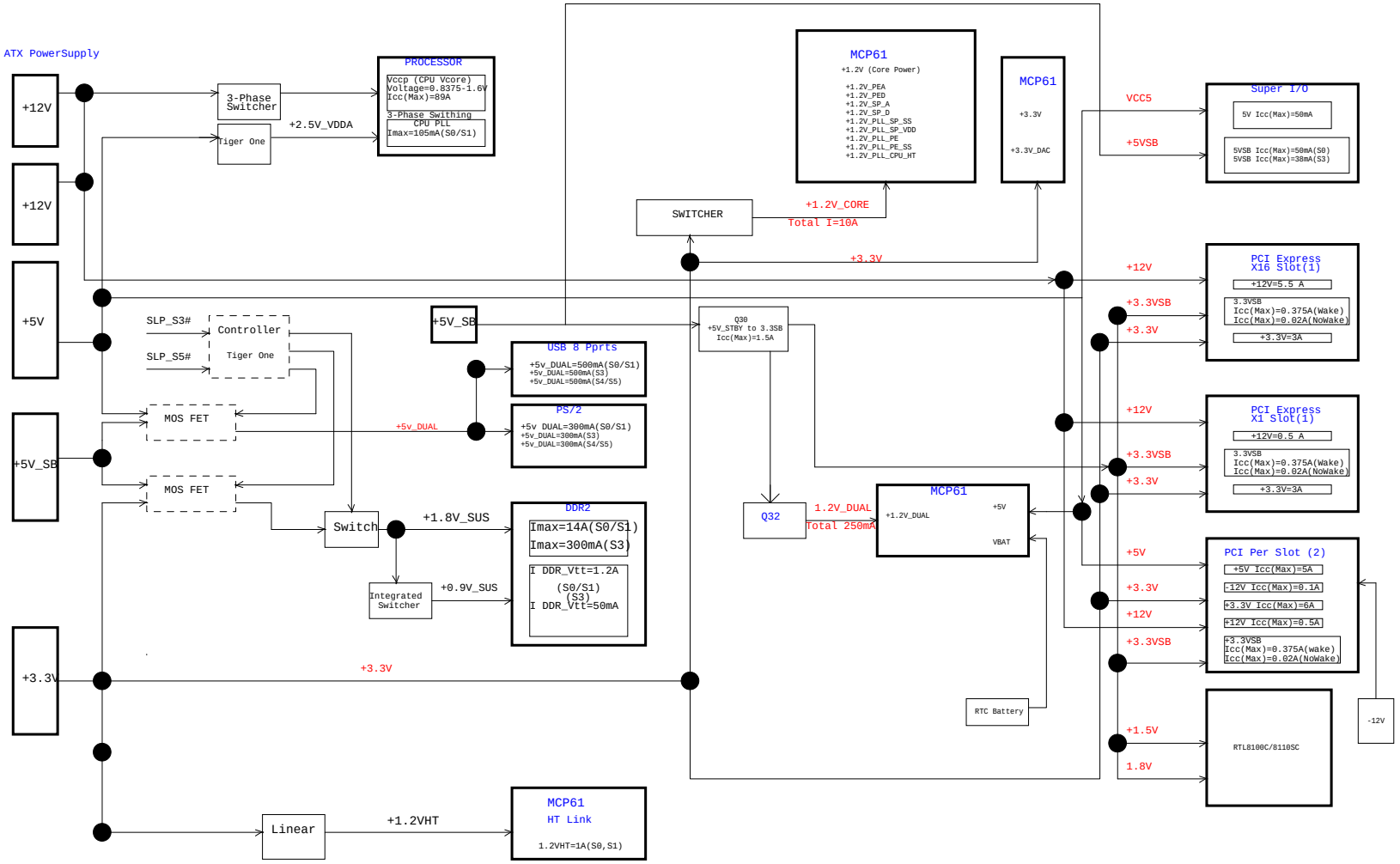

FOXCONN PCEG

Title: Power Map		
Size: C	Document Number: MCP61M05	Rev: A
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6/18 ： 1,USB: 0 ohm R change to 0 ohm RN, 4pin Bead change to 8pin Bead; 2, BIOS,LPC change to SPI . 3, LAN change to AC131 + PCI LAN :RTL8100C/8110SC,

6/20 ： 1,LAN_CLK 走南橋，Dummy 外部晶振，Remove AC131 PHY LAN；2，R623，R624 16.9 ohm 改為15 ohm ； 3，USB Fuse 2.6A 替代2個1.5A ；4，F_Audio 75 ohm /22k ohm 電阻閤並成排阻

6/21 ： 1，LAN 49.9 ohm 電阻閤並成排阻49.9 ohm；
2，R388 去掉，SIO部分有串接10ohm 電阻；
3，Dummy C332,C301,C310,C300,C320,C290,C347.

6/22 ： 1,去掉R355，R829，R830，R832； 2， dummy C572 ；
3， ADD C2136 0.1uF to GMII_RXCLK, R57 change to 330K;

6/29: 1, Add 75 ohm damping resistance for Audio ; 2,F_Audio detect pin connect to sense_B pin of CODEC; 3, ADD prtection Diode to COM port .

7/2 : 1,remove L99,L100,L102; Change heatsink with foxconn log; 2, Remove RN122 .

7/3: 1, ADD C 956(4.7uF/805) to 3.3v_Dual ; 2, dummy EC83 (5V_SB); 3, Remove C412, C352,C354;

7/5: 1, change C374,C378 to 0.1uF/0603; 2, dummy C157,C244,C267,C193,C286,C645,C199,C247,C312,C315,C325,C327,C328; 3, Remove C385,C386,C407,C865,C387,C866;

7/7: 1, Change D6,D7,D8,D17,D20,D23,D47 footprint to so80h16; 2, change RN45,RN46 from 8p4r0603 to 8p4r0402 ; 3, add EC106 100uF to +1.2V_dual, dummy EC105 ; 4, Q129,Q131 change to AP15N03GH;

7/9: 1, GPIO PIN: Board ID Select. add R363,R364,R365; Default add R363; 2, Remove C808,C809,C810,C811,C821,C89,C806,C807,C156,C268,C970, C52,C74,C49,C976,C61,C83,C73,C76,C72,EC66 ; 3, add EC50, dummy EC14;

7/11 : 1, add EC107 to aduio 12 V power, C733 change to 10uF, add L28 to audio power DVDD ; 2, ADD EC60 to 3.3V_DUAL for LAN Power ,default dumy ; 3, add R368, R371 to modify the SPI clock; 4, Remove C7,C8,C11,R517,R530,R536 (Audio).

8/16 : 1 .L12/L20 change to 1uH/1kHz

2 .EC39/38 change to 680uF

3 . add R501/502 for CD-IN

4 .PCI SLOT IDSEL

5 .add EC103 (1.2V OUTPUT)

6 .EC35/37 change to 470uF

7 . add EC104/105

8 .C392/396 change to 22p

9 .Retention Module for CPU change HH P/N

10 .PEA POWER del copper,FB

11 .R83 dummy,and add thermal trip to SIO through level shift

12 .C238 change to 220pF

13 .R163 change to 680R

14 .SATA2,SATA3 change each other

15 .Del R77/72/133

16 .R262 change to 1.1k

17 .C495 change to 10uF and reserved

18 .C496 reserved

9/12 : 1 .USB_OC add R550/R51/R552/R553 for 3.3V

2 .Exchange usb3/4;

2 .change C385/C391/C392/C396 from 0603 to 0402

9/19 : 1 .change c392/c396 22pf to 24pf

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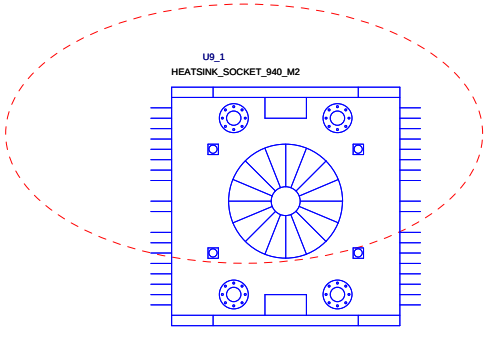

modify 8/16

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