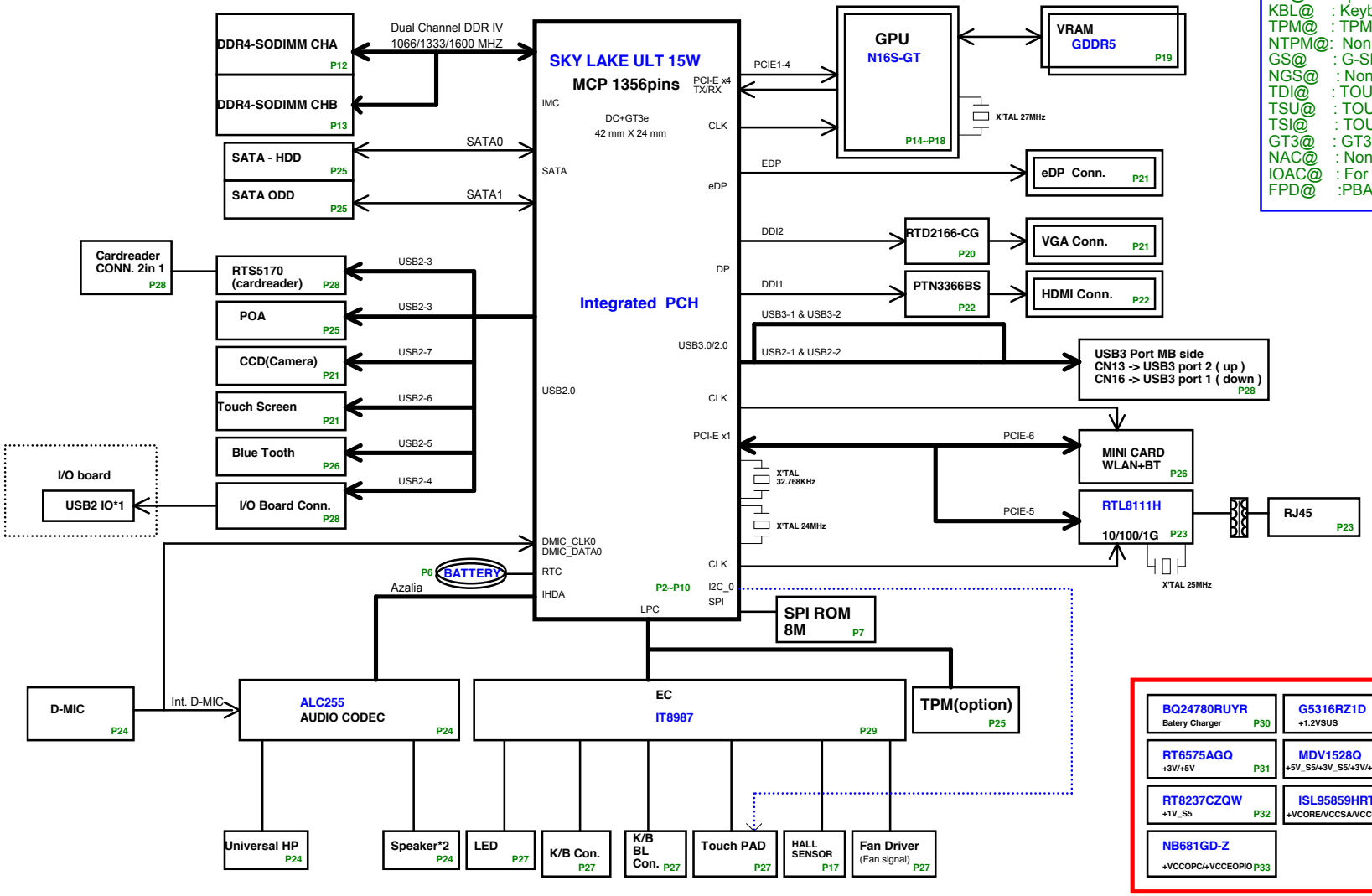
Z8VR Serials SKL ULT SYSTEM BLOCK DIAGRAM



BOM

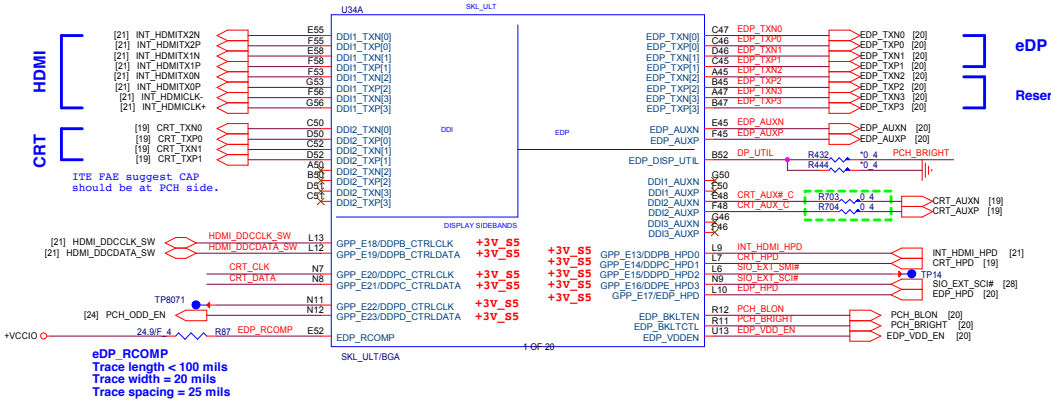
IV@ : iGPU
EV@ : Optimus
KBL@ : Keyboard backlight
TPM@ : TPM
NTPM@: Non TPM
GS@ : G-SENSOR
NGS@ : NonG-SENSOR
TDI@ : TOUCH PAD I2C
TSU@ : TOUCH SCREEN USB
TSI@ : TOUCH SCREEN I2C
GT3@ : GT3 CPU
NAC@ : Non IOAC
IOAC@ : For IOAC
FPD@ :PBA

BQ24780RUYR Batery Charger P30	G5316RZ1D +1.2VSUS P34	Thermal Protection Discharger P38
RT6575AGQ +3V/+5V P31	MDV1528Q +5V_S5/+3V_S5/+3V/+5V P31	UP1658RQKF +VGPU_CORE P39
RT8237CZQW +1V_S5 P32	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P35	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P40
NB681GD-Z +VCCOPC/+VCCEOPIO P33		

Quanta Computer Inc.
PROJECT : Z8VR
Block Diagram
Rev 1A
Date: Thursday, June 22, 2017 Sheet 1 of 46

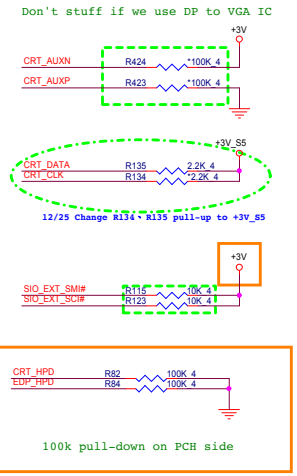
Skylake ULT (DISPLAY,eDP)

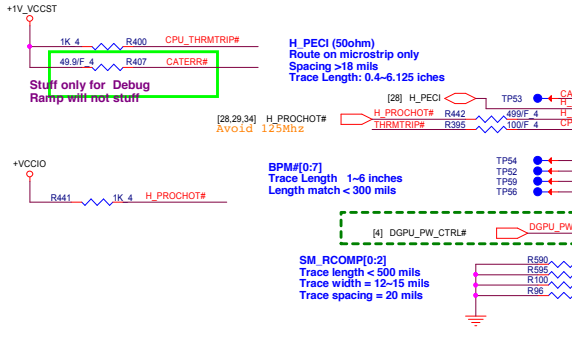
02



eDP Panel

Reserve 2 Lane for 4K x 2K





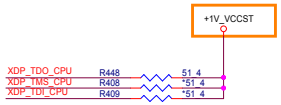
If use Intel DCI USB 3.0 fixture need to short
1. XDP_TDO <--> XDP_TDO_CPU
2. XDP_TDI <--> XDP_TDI_CPU
3. XDP_TMS <--> XDP_TMS_CPU

PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

TCK,TMS
Trace Length < 9000mils

MP remove(Intel)

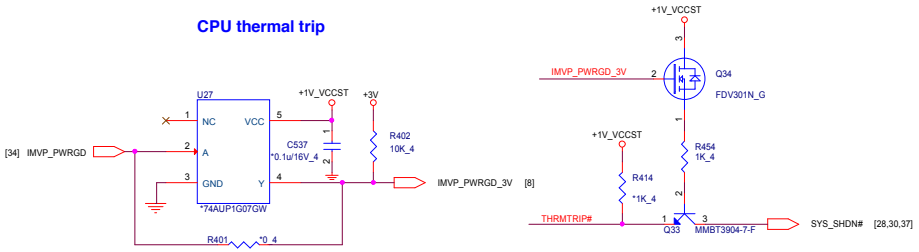


H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

,XDP_TCK1,XDP_TMS
don't need pull up or pull down

XDP_TCK0 R558 Stuff

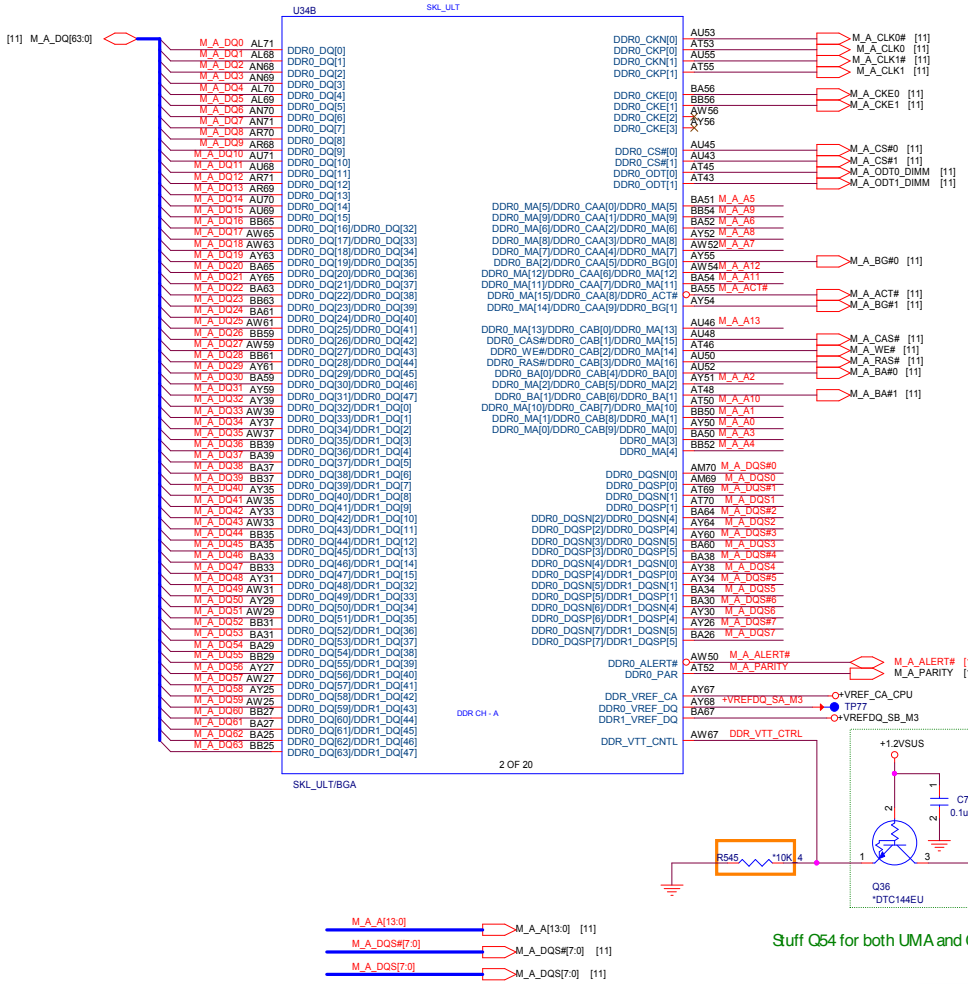
CPU thermal trip



Quanta Computer Inc.			
PROJECT : Z8VR			
Size	Document Number		Rev
	Skylake 1/4 (DDI/eDP)		1A
Date: Thursday, June 22, 2017	Sheet 2	of 46	

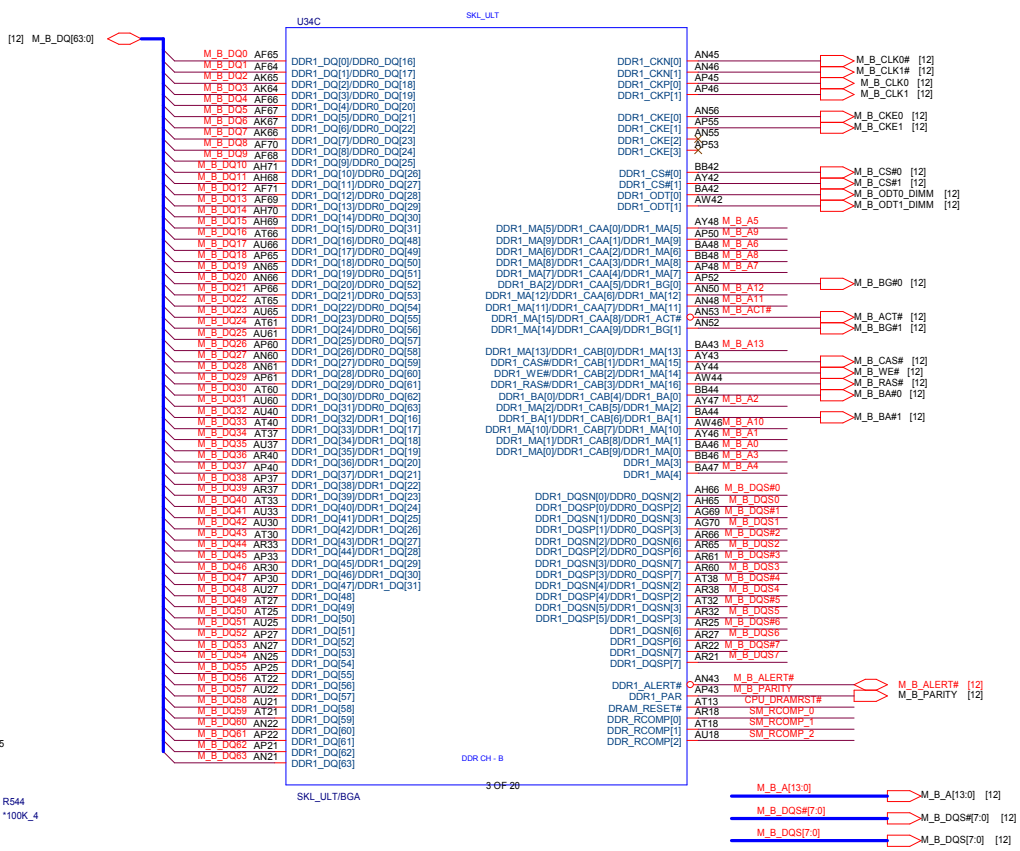
Change Data and DQS to interleave.

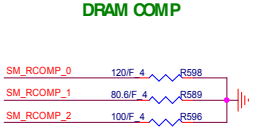
SKL ULT (DDR4)

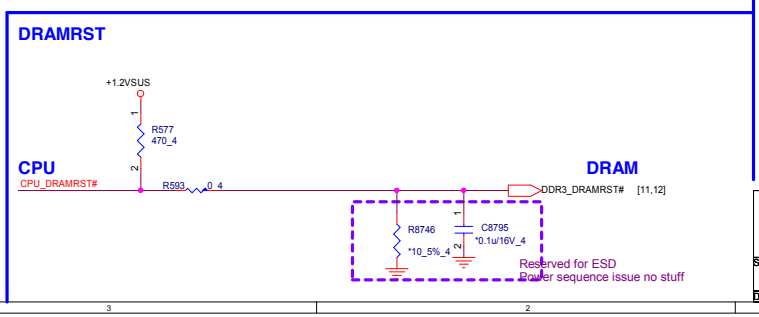


Stuff Q54 for both UMA and GPU in DDR_VTT_CNTL

SKL ULT (DDR4)







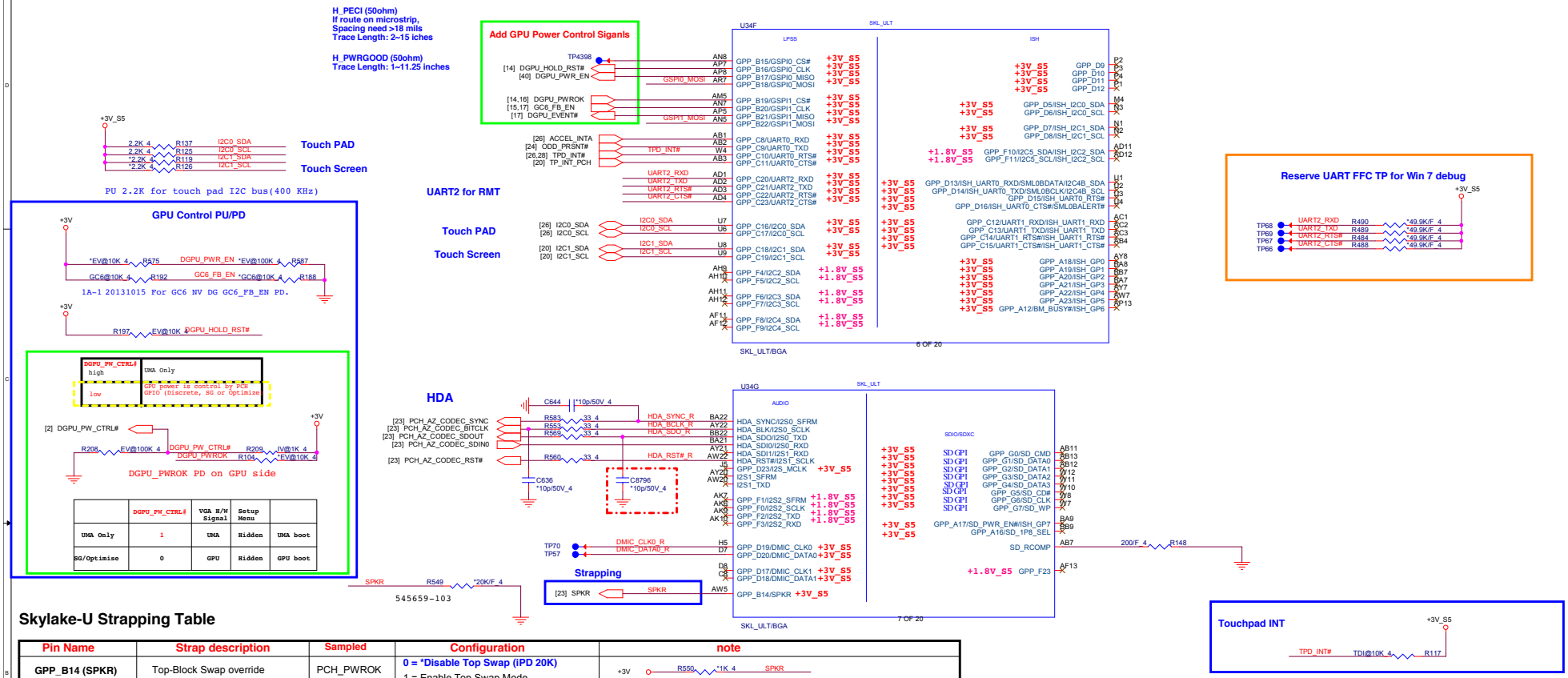
Quanta Computer Inc.

PROJECT : Z8VR

Size	Document Number	Rev
	Skylake 2/3 (DDR3 I/F)	1A
Date: Thursday, June 22, 2017	Sheet 3 of 46	

SKL ULT (SIDEBAND) GPIO

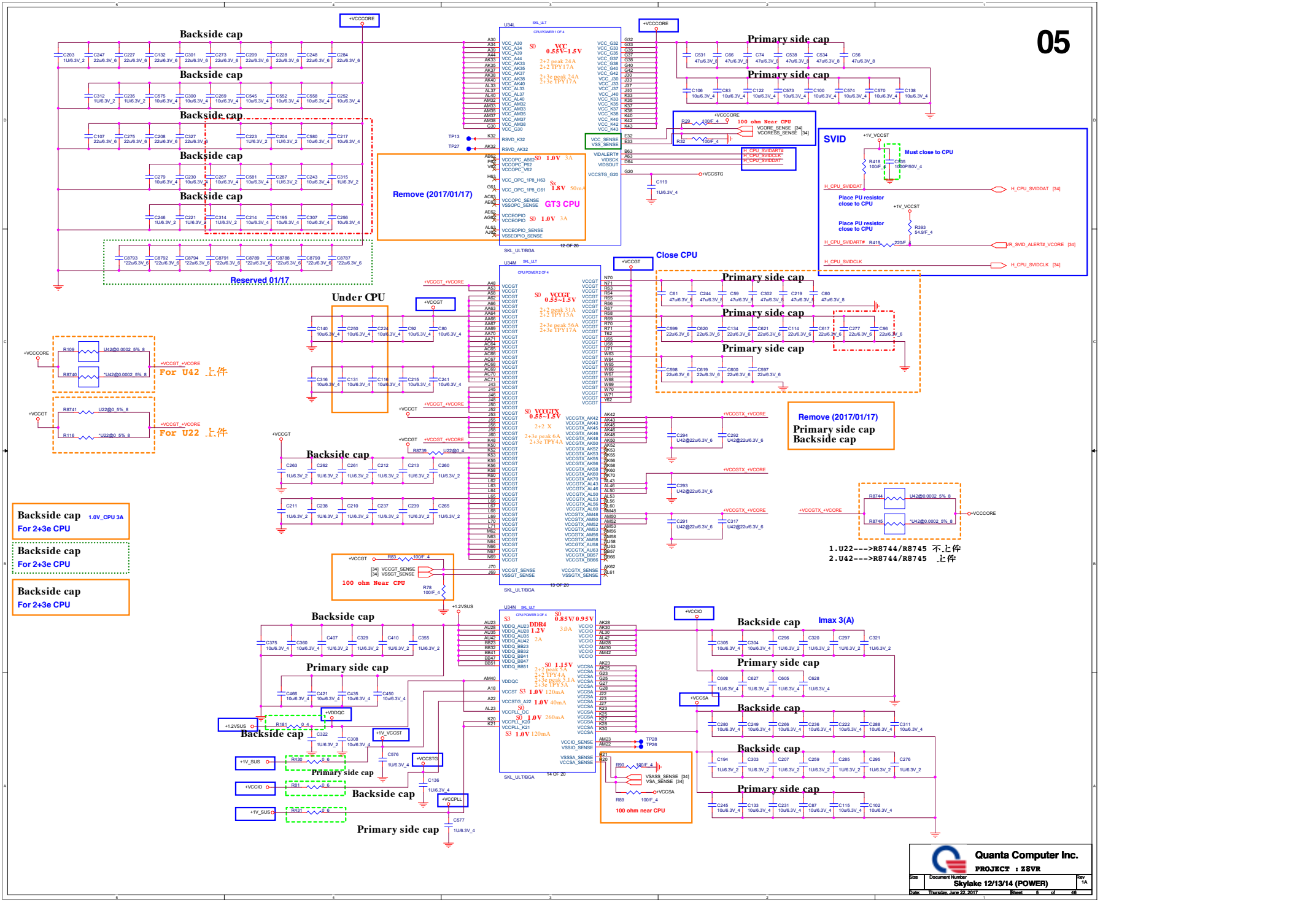
04



Skylake-U Strapping Table

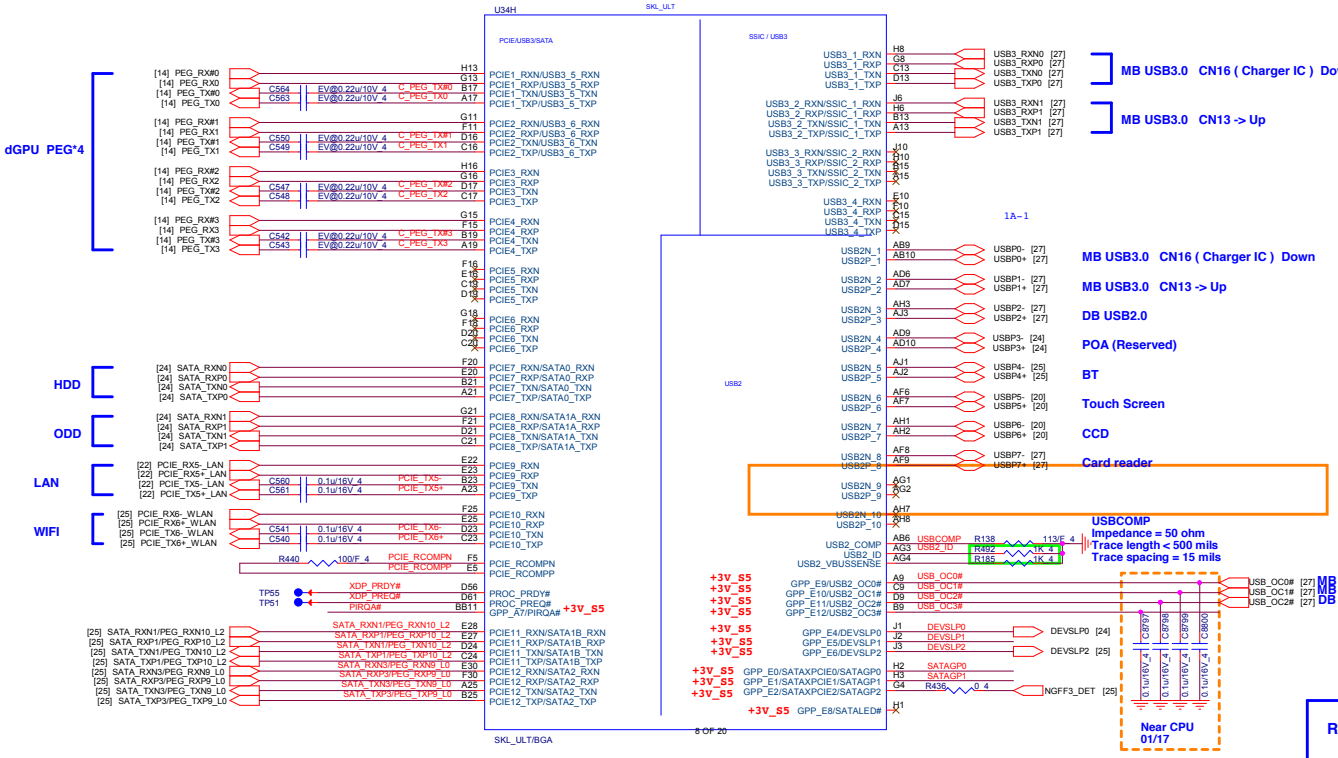
Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V R550 *1K SPKR
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R543 *1K GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) 1 = Enable Intel ME Cryp to TLS	+3V_S5 R144 *10K SMBALERT# [7]
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R191 *1K GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_S5 R481 *1K SML0ALERT# [7]
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal HDA_SDO_R R570 *1K ME_WR# [28]
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

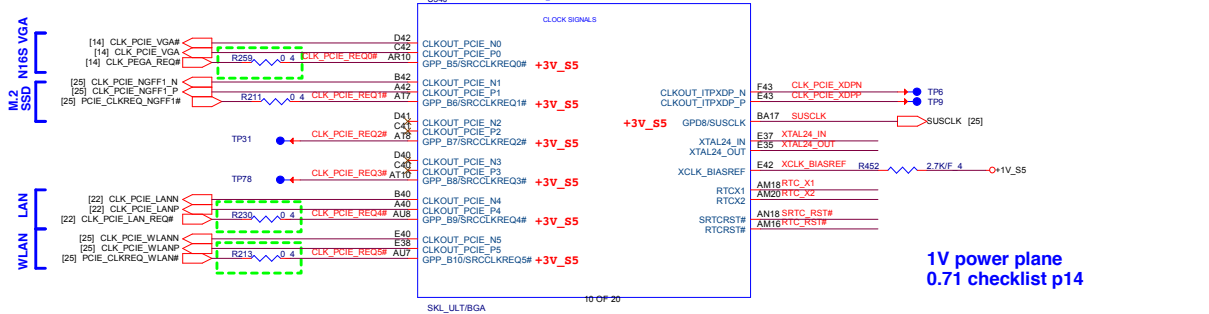
Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number: Skylake 6/7 (PEG/DMI/FDI) | Rev 1A
Date: Thursday, June 22, 2017 | Sheet 4 of 46

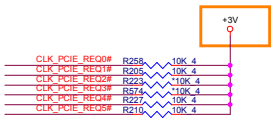

05
Backside cap
Primary side cap
Reserved 01/17
Remove (2017/01/17)
GT3 CPU
Under CPU
Close CPU
SVID
Must close to CPU
Place PU resistor close to CPU
For U42 上件
For U22 上件
Remove (2017/01/17)
Primary side cap
Backside cap
Backside cap 1.0V_CPU 3A
For 2+3e CPU
100 ohm Near CPU
Imax 3(A)
1.U22--->R8744/R8745 不上件
2.U42--->R8744/R8745 上件
Quanta Computer Inc.
PROJECT : Z8VR
Skylake 12/13/14 (POWER)
Thursday, June 22, 2017

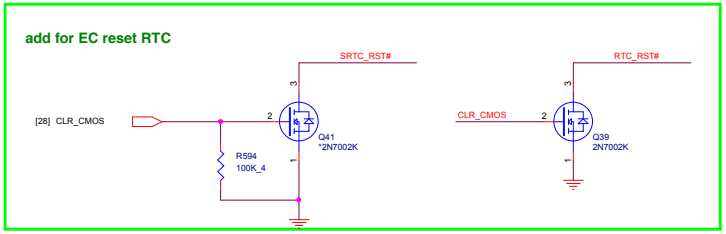
Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

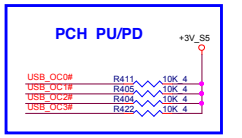
06

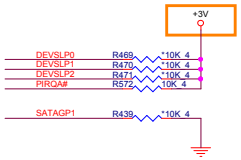


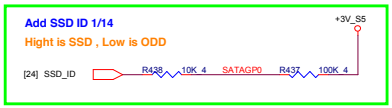


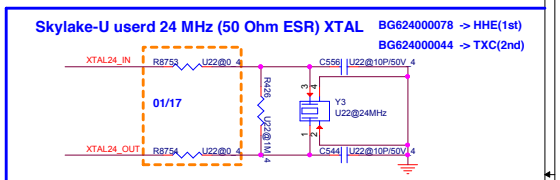


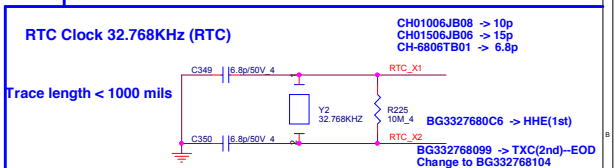


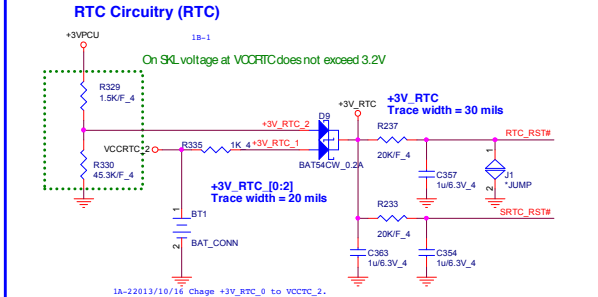












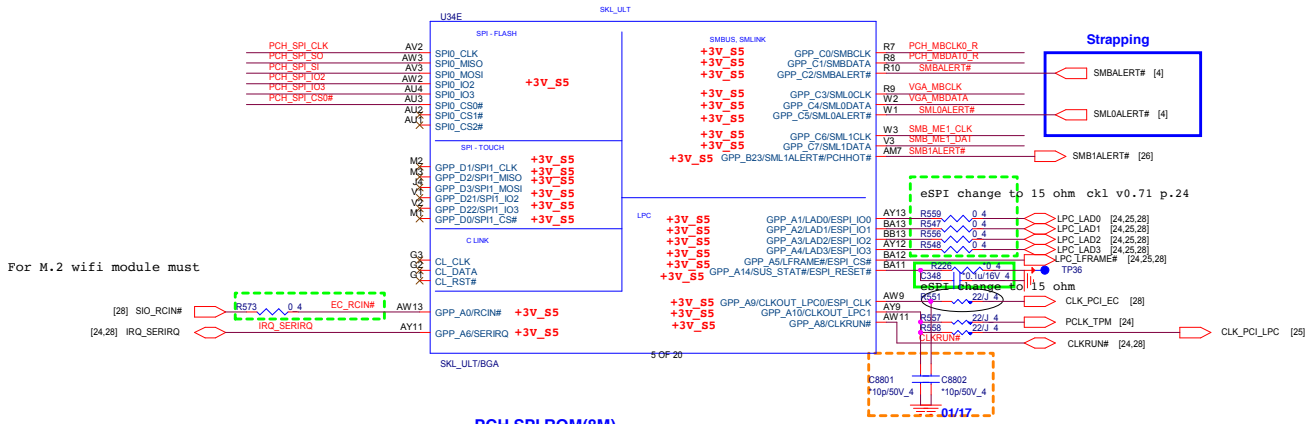
1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032

Quanta Computer Inc.

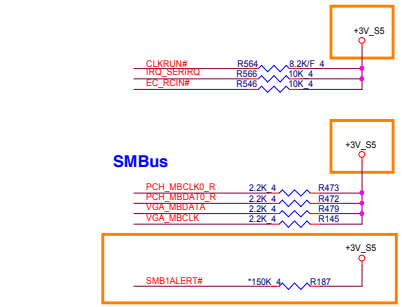
PROJECT : Z8VR

Size	Document Number	Rev
	Skylake 9/10 (PEG/USB/CLK)	1A

Date: Thursday, June 22, 2017 Sheet 6 of 46



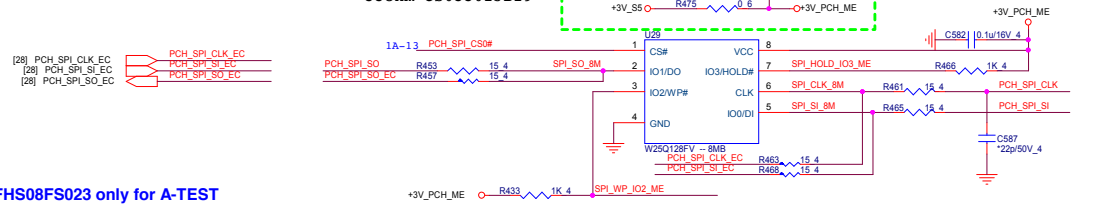
For M.2 wifi module must



Termination Resistor Requirement for PCH PCHHOT# Pin
Reserve PU 150K resistor

PCH SPI ROM(8M)

15ohm CS01502JB12
33ohm CS03302JB29

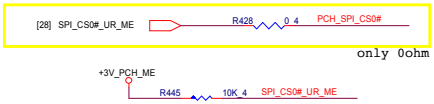


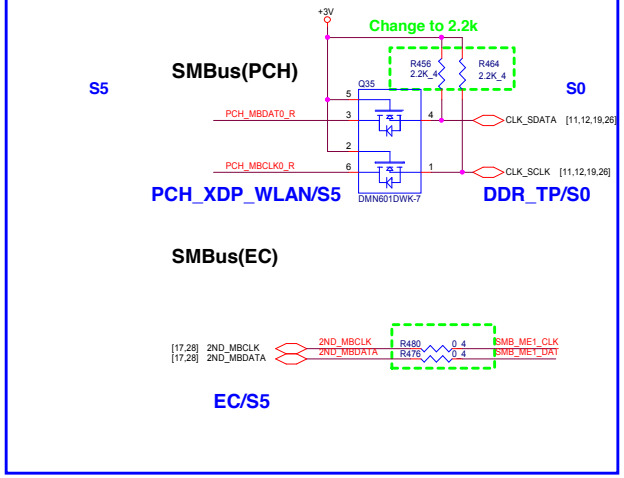
SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
	WND	16M	AKE3DZN0N01	W25Q128FVSIQ
	GGD	16M	AKE3DZN0Q02	GD25B127DSIGR

3.3K is original and for no support fast read function

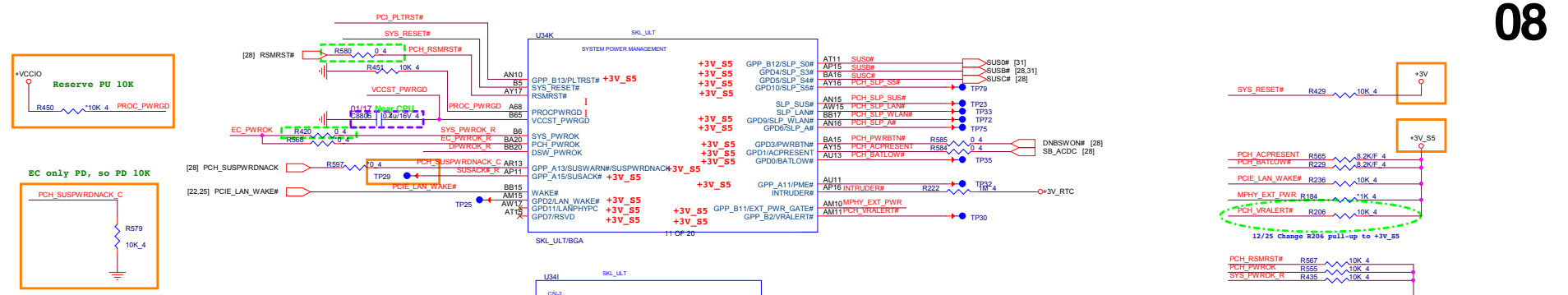
reserve for SPI fast read



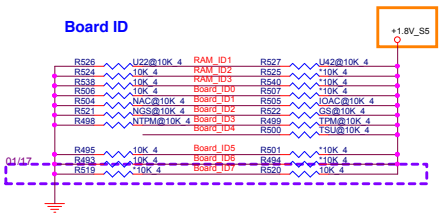


Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number: Skylake 5 (SATA/HDA/SPI) | Rev: 1A
Date: Thursday, June 22, 2017 | Sheet 7 of 46

08



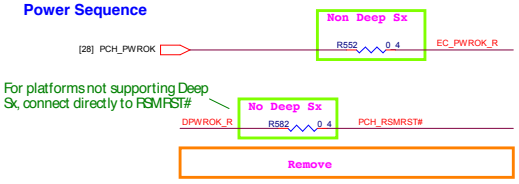
Board ID



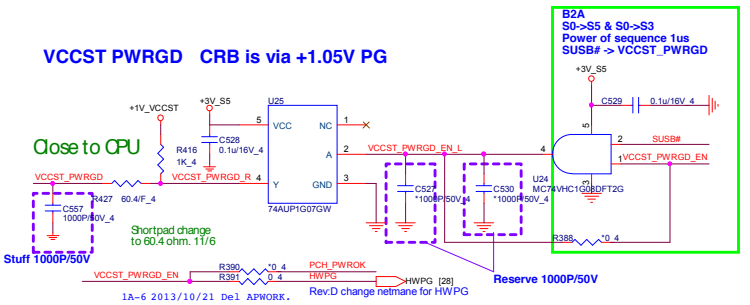
	Low	High
BOARD_ID0	VRAM X32 (R506)	VRAM X16 (R507)
BOARD_ID1	Non IOAC (R504)	IOAC (R505)
BOARD_ID2	Non G-sensor (R521)	G-sensor (R522)
BOARD_ID3	No TPM (R498)	TPM (R499)
BOARD_ID4	No-Touch panel	Touch panel (R500)

	Low	High
BOARD_ID5	For 14" (R495)	For 15" / 17" (R501)
BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID7	Z8V (R519)	Z8VR (R520)

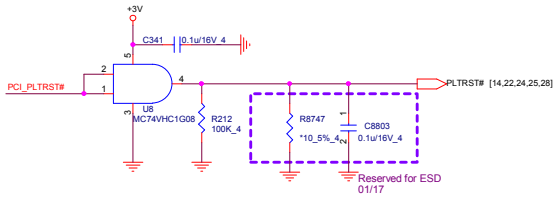
Power Sequence



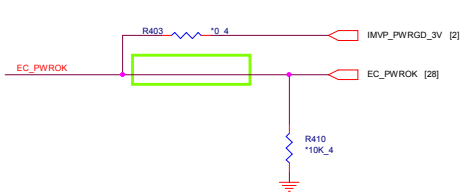
VCCST PWRGD CRB is via +1.05V PG



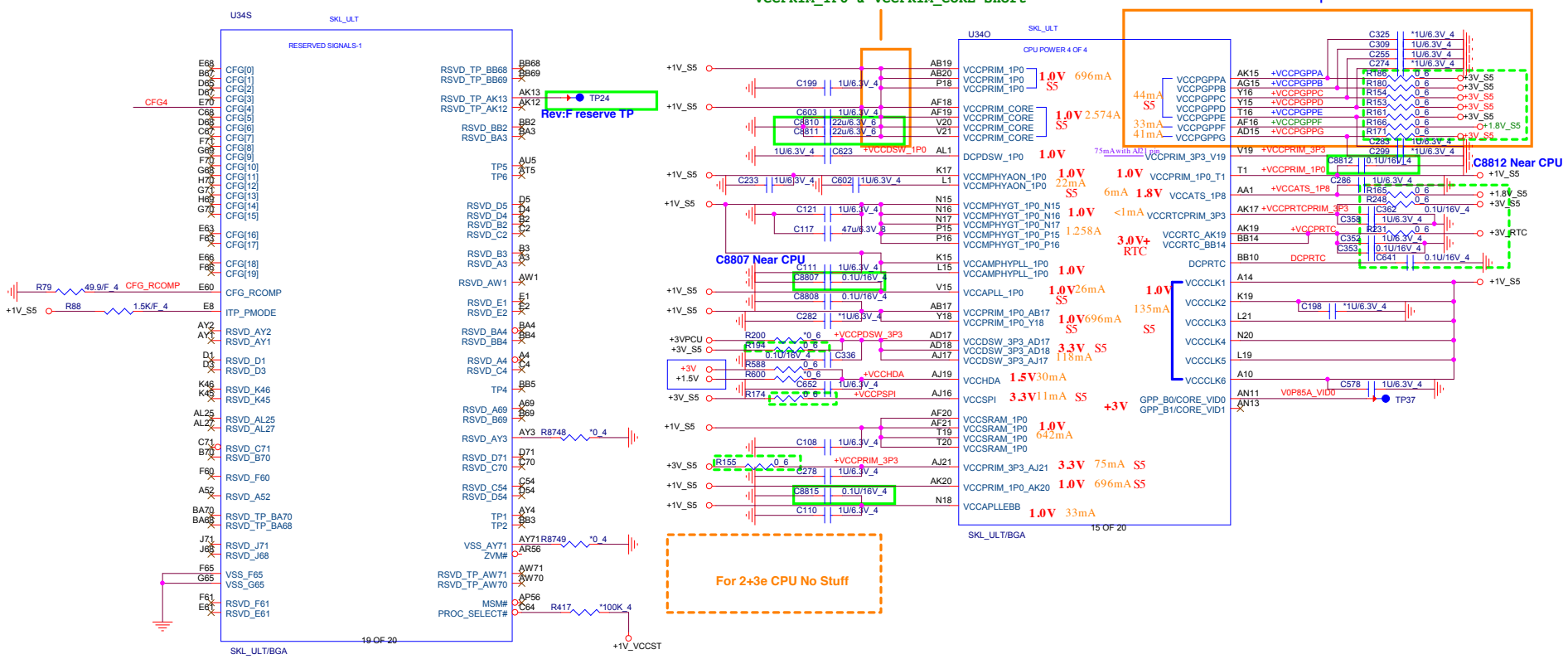
PLTRST# Buffer



SYSPWOK



Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: Skylake 9/11 (PWROK/Board_ID)	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 8 of 46	

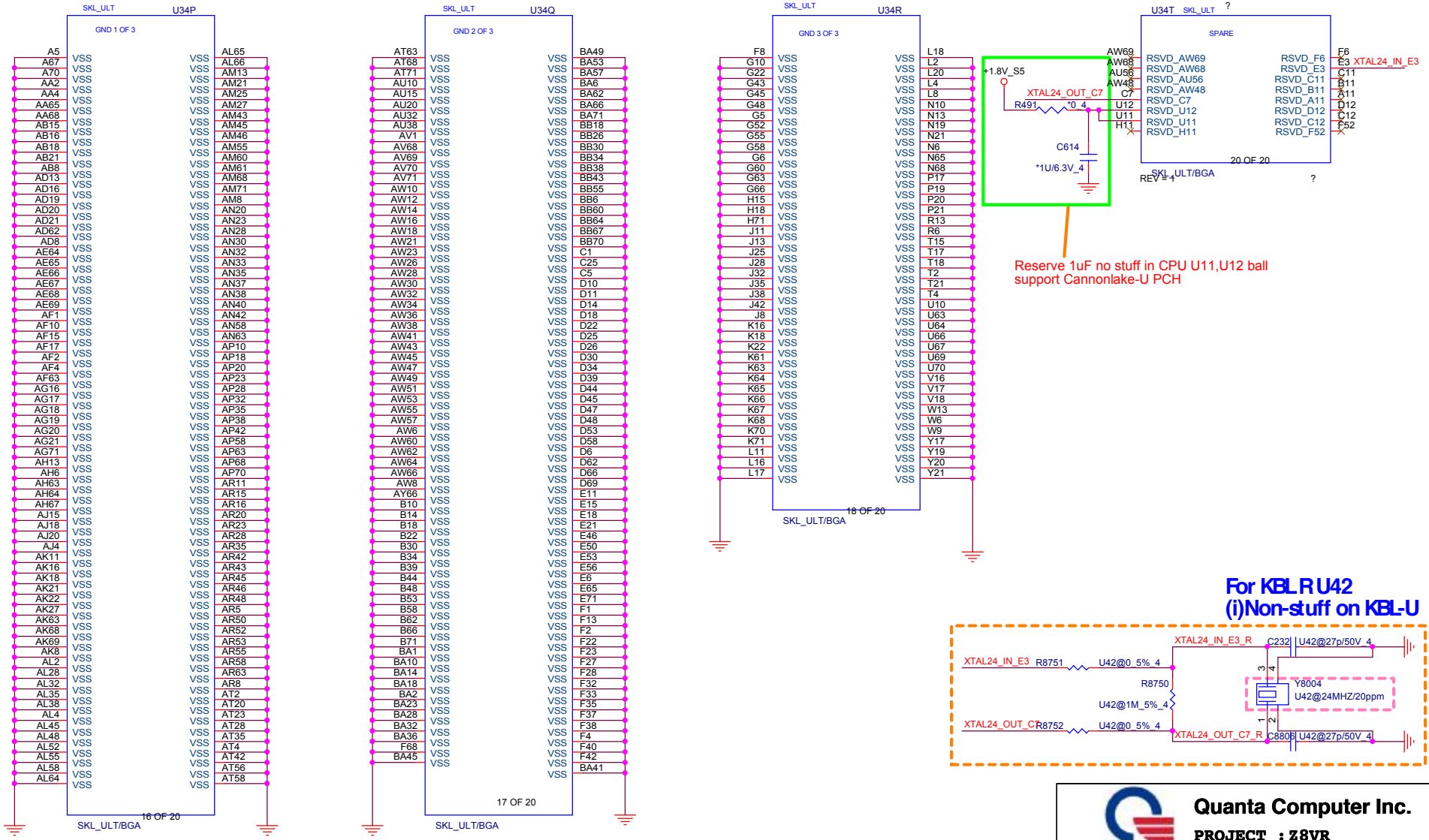


Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	**1 = *Normal Operation; No stall (iPU 3K)** 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	**1 = *Normal Operation(iPU 3K)** 0 = Lan number reversed	**H & S processor used only**
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) **0 = *Enabled**	CFG4 R455 1K_4
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	**H & S processor used only**
CFG[7]	PEG Training	**1 = *PEG Train immediatedly follow RESET# de-assertion (iPU 3K)** 0 = PEG wait for BIOS for training	**H & S processor used only**
CFG[19:8]	Reserved Configuration lane		

Quanta Computer Inc.
PROJECT : Z8VR

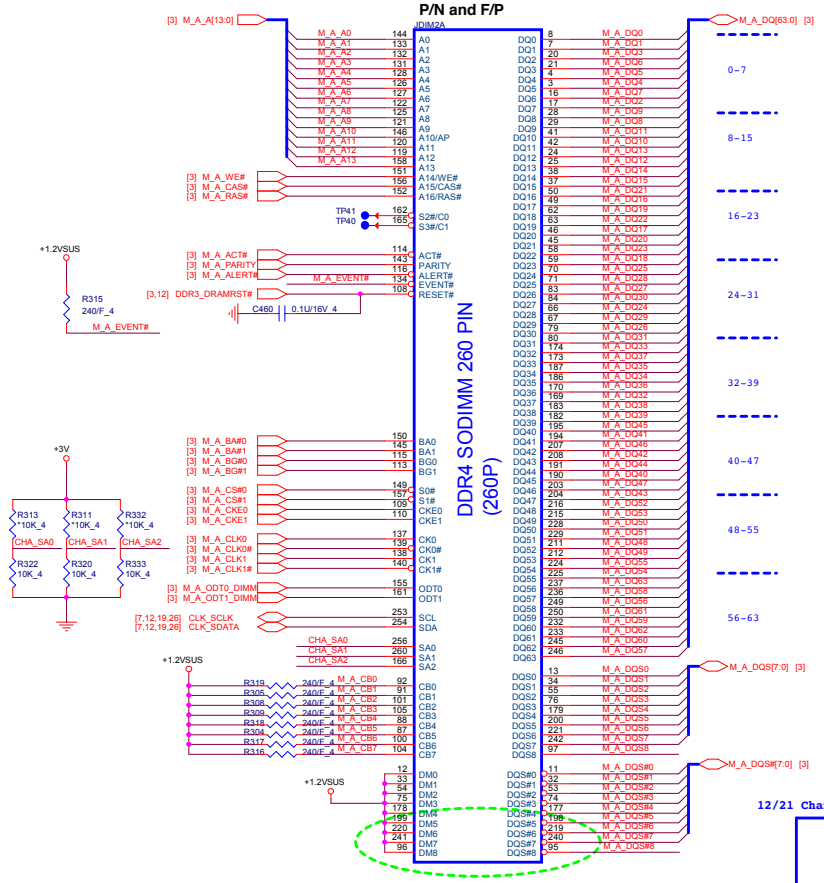
Size	Document Number	Rev
	Skylake PCH-LP 15/19 (POWER)	1A
Date: Thursday, June 22, 2017	Sheet 9 of 46	

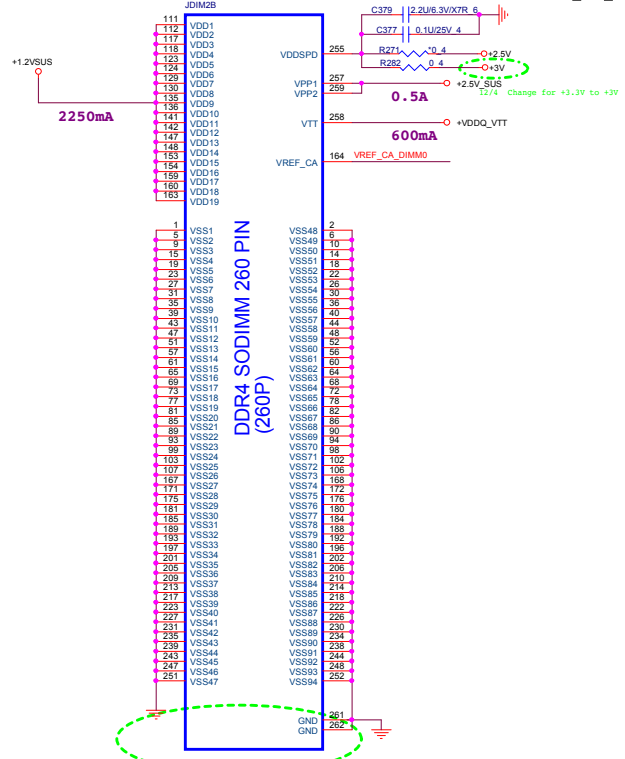
Skylake ULT (GND)



Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: Skylake 10/17/18 (GND)	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 10 of 46	

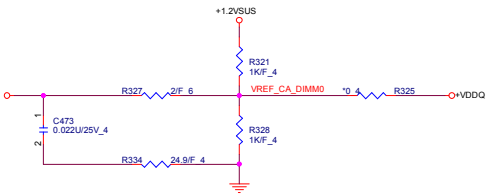
P/N and F/P





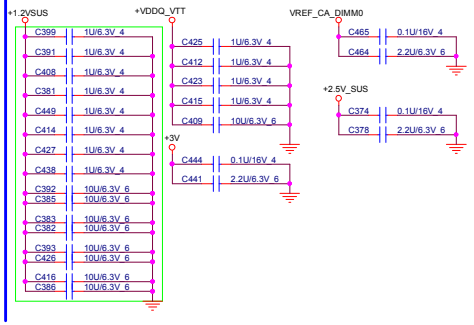
12/21 Change JDIM2 footprint to "ddr4-d4as0-26001-1p52-std-smt " for SMT requset

VREF DQ0 M1 Solution



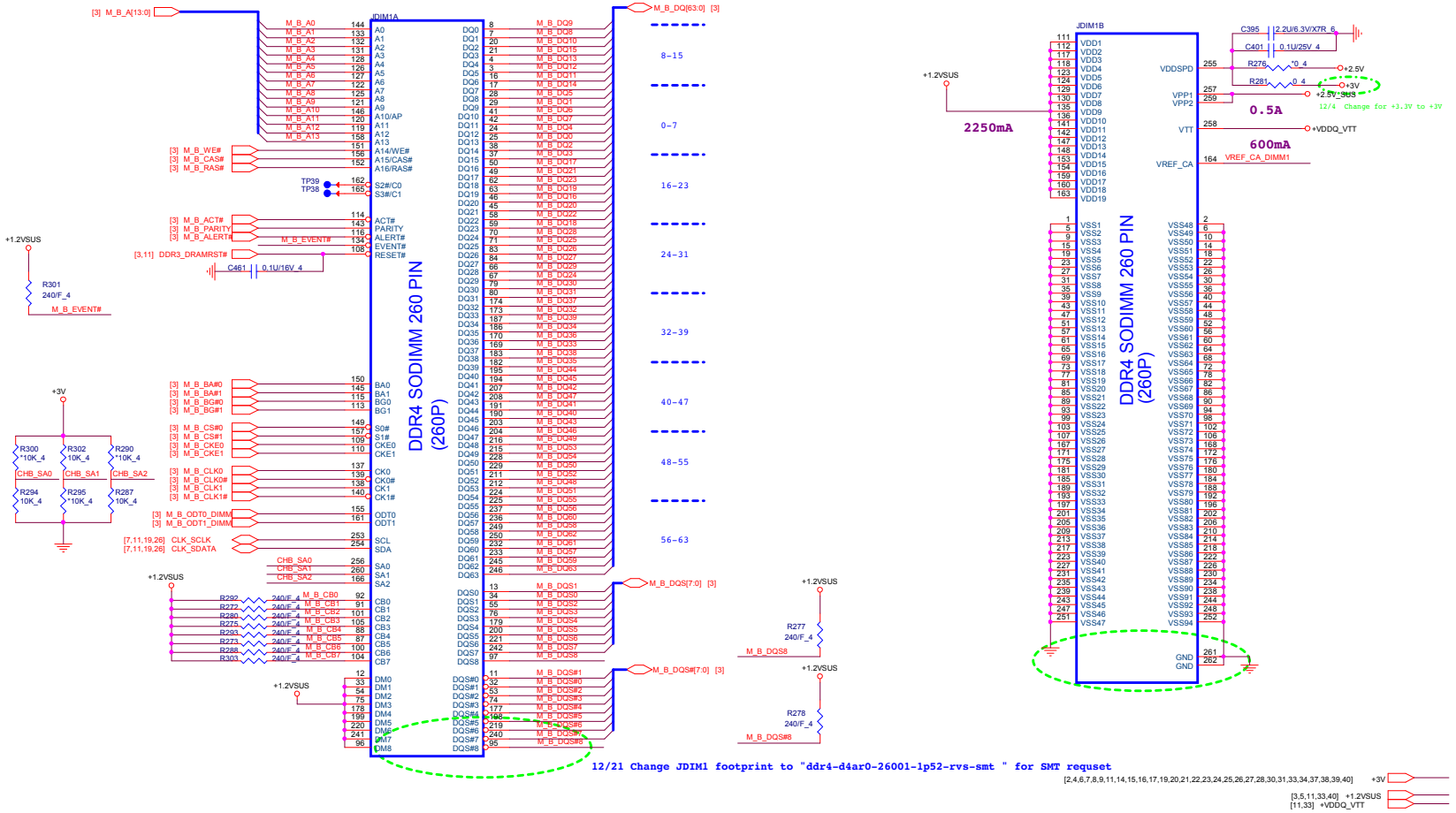
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

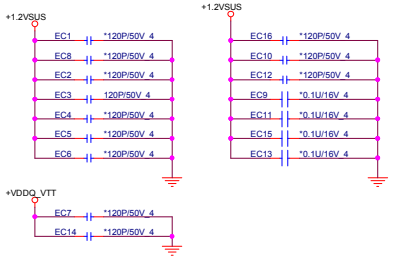


[3,5,12,33,40] +1.2VSUS
[12,33] +VDDQ_VTT
[2,4,6,7,8,9,12,14,15,16,17,19,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40] +3V

Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: DDR4 DIMM-RVS(5.2H) CHA	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 11 of 46	

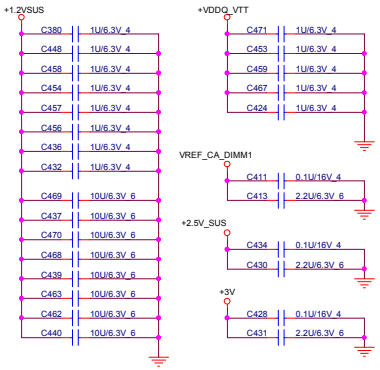


For EMI RESERVE

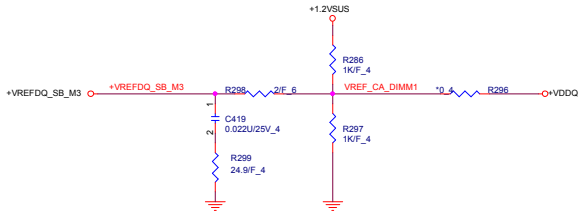


Place these Caps near So-Dimm0.

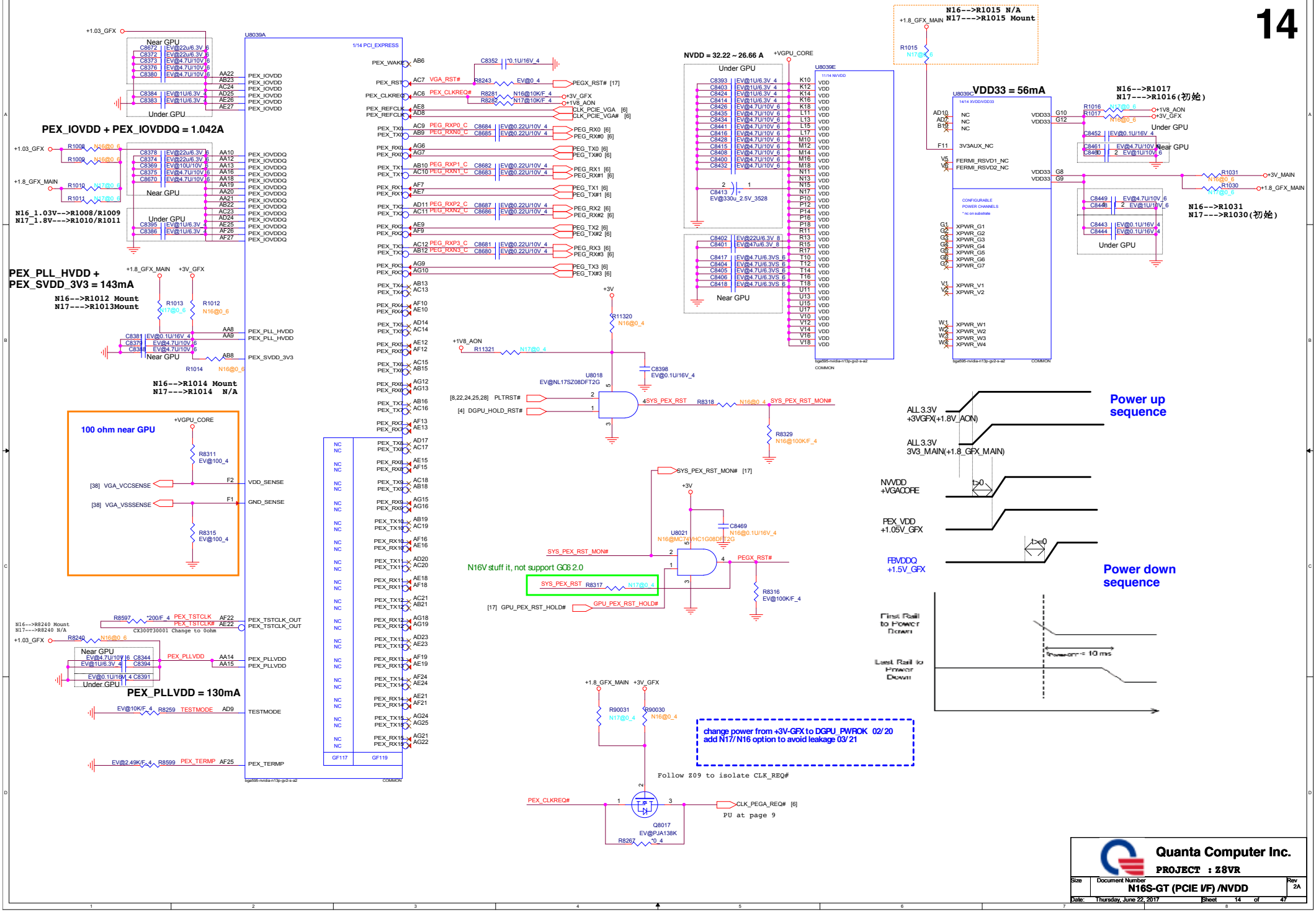
1uF/10uF 4pcs on each side of connector

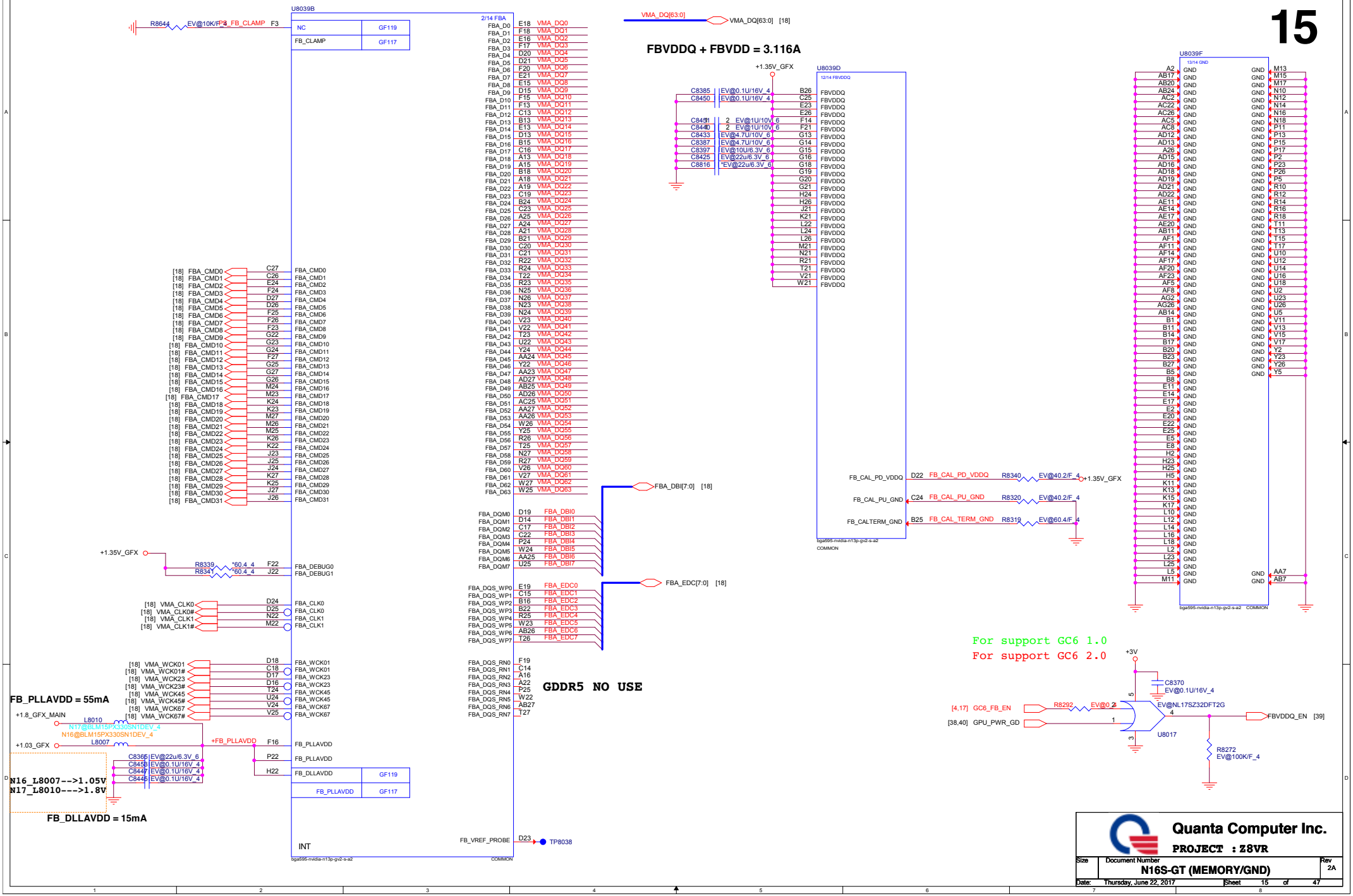


VREF DQ1 M1 Solution



Quanta Computer Inc.			
PROJECT : Z8VR			
Size	Document Number		Rev
	DDR4 DIMM-STD(5.2H) CHB		1A
Date: Thursday, June 22, 2017		Sheet 12 of 46	


PEX_IOVDD + PEX_IOVDDQ = 1.042A
N16_1.03V-->R1008/R1009
N17_1.8V--->R1010/R1011
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
N16-->R1012 Mount
N17--->R1013Mount
N16-->R1014 Mount
N17--->R1014 N/A
100 ohm near GPU
PEX_PLLVDD = 130mA
N16-->R8240 Mount
N17--->R8240 N/A
CX300T30001 Change to 0ohm
N16V stuff it, not support GC6 2.0
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
N16-->R1015 N/A
N17--->R1015 Mount
N16-->R1017
N17--->R1016(初始)
N16-->R1031
N17--->R1030(初始)
change power from +3V-GFX to DGPU_PWROK 02/20
add N17/N16 option to avoid leakage 03/21
Follow Z09 to isolate CLK_REQ#
PU at page 9
Power up sequence
Power down sequence
ALL 3.3V
+3VGFX(+1.8V_AON)
ALL 3.3V
3V3_MAIN(+1.8_GFX_MAIN)
NVVDD
+VGACORE
PEX_VDD
+1.05V_GFX
FBVDDQ
+1.5V_GFX
First Rail to Power Down
Last Rail to Power Down
Tpowerdown <= 10 ms
Near GPU
Under GPU
U8039A
U8039E
U8039C
U8018
U8021
Q8017
Quanta Computer Inc.
PROJECT : Z8VR
N16S-GT (PCIE I/F) /NVDD
Thursday, June 22, 2017

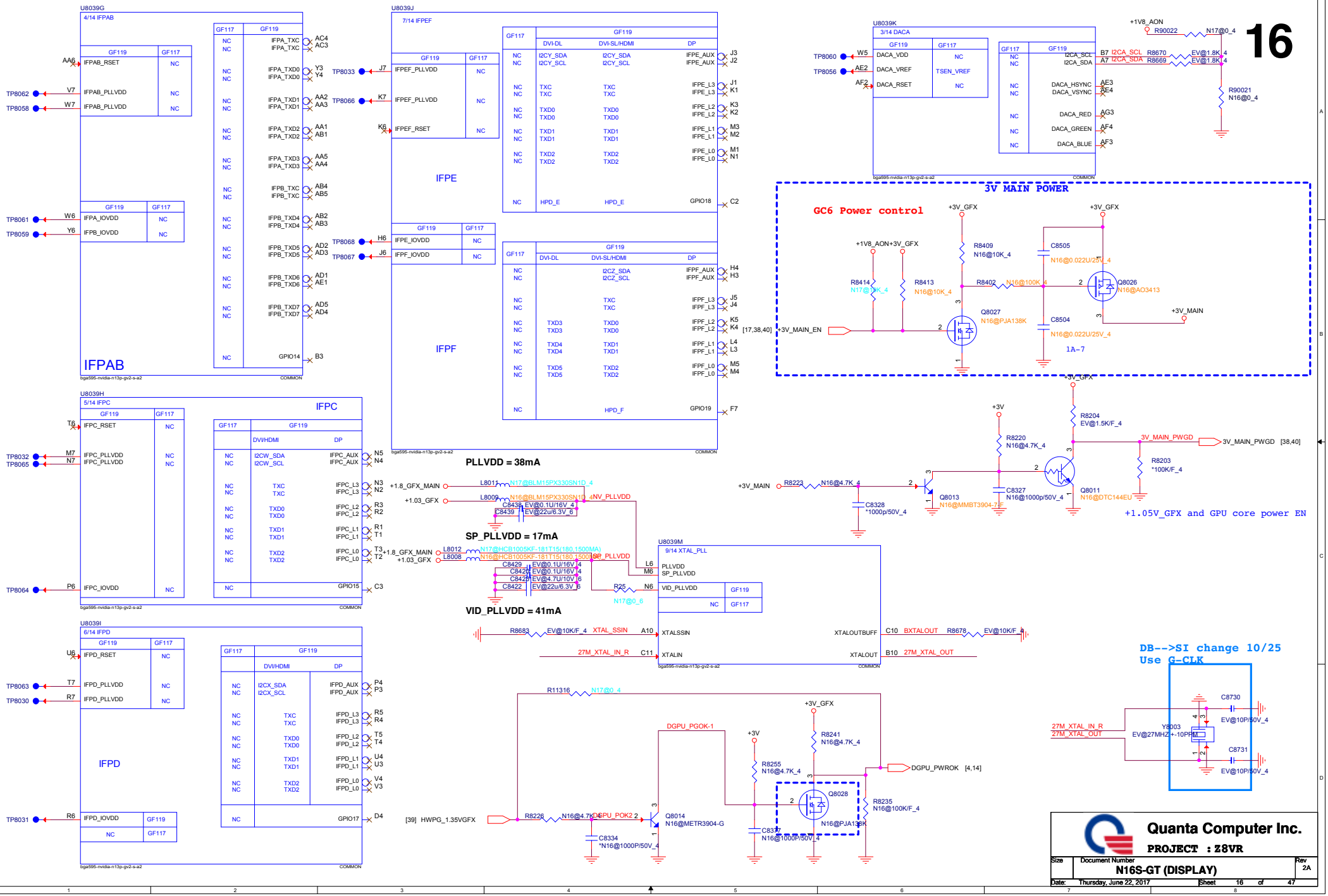


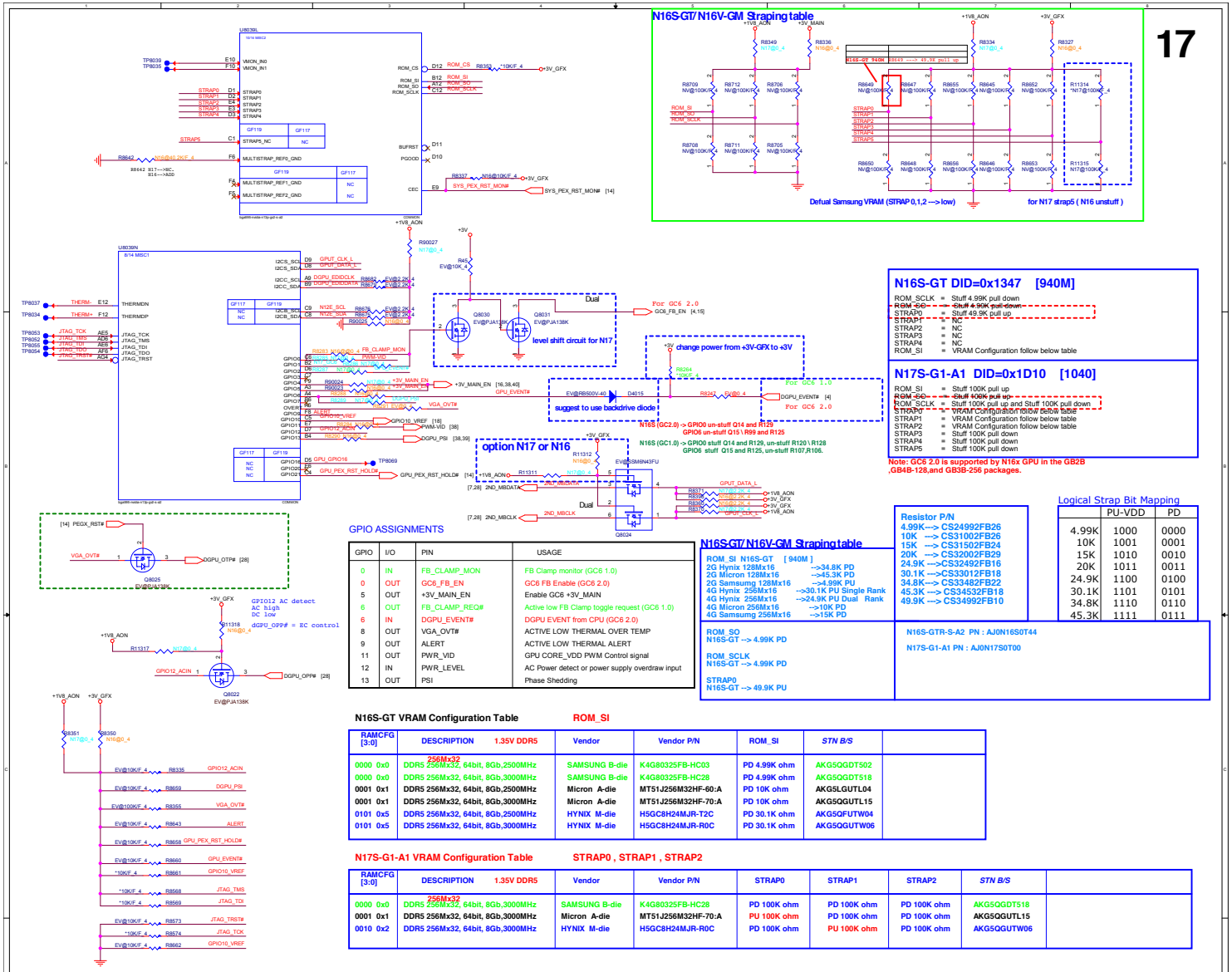
Quanta Computer Inc.

PROJECT : Z8VR

Size	Document Number	Rev
	N16S-GT (MEMORY/GND)	2A

Date: Thursday, June 22, 2017 Sheet 15 of 47


16
U8039G
4/14 IFPAB
IFPAB
U8039J
7/14 IFPEF
IFPE
IFPF
U8039K
3/14 DACA
3V MAIN POWER
GC6 Power control
+3V_MAIN_EN
+3V_MAIN_PWGD [38,40]
+1.05V_GFX and GPU core power EN
U8039H
5/14 IFPC
IFPC
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
U8039M
9/14 XTAL_PLL
U8039I
6/14 IFPD
IFPD
DB-->SI change 10/25
Use G-CLK
Quanta Computer Inc.
PROJECT : Z8VR
Size
Document Number
N16S-GT (DISPLAY)
Rev
2A
Date: Thursday, June 22, 2017
Sheet 16 of 47



N16S-GT/ N16V-GM Straping table

N16S-GT DID=0x1347 [940M]

ROM_SCLK	=	Stuff 4.99K pull down
ROM_CS	=	Stuff 4.99K pull down
STRAP0	=	Stuff 49.9K pull up
STRAP1	=	NC
STRAP2	=	NC
STRAP3	=	NC
STRAP4	=	NC
ROM_SI	=	VRAM Configuration follow below table

N17S-G1-A1 DID=0x1D10 [1040]

ROM_SI	=	Stuff 100K pull up
ROM_CS	=	Stuff 100K pull up
ROM_SCLK	=	Stuff 100K pull up and Stuff 100K pull down
STRAP0	=	VRAM Configuration follow below table
STRAP1	=	VRAM Configuration follow below table
STRAP2	=	VRAM Configuration follow below table
STRAP3	=	Stuff 100K pull down
STRAP4	=	Stuff 100K pull down
STRAP5	=	Stuff 100K pull down

Note: GC6 2.0 is supported by N16x GPU in the GB2B ,GB4B-128,and GB3B-256 packages.

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16S-GT/ N16V-GM Straping table

ROM_SI N16S-GT [940M]
2G Hynix 128Mx16 -->34.8K PD
2G Micron 128Mx16 -->45.3K PD
2G Samsumg 128Mx16 -->4.99K PU
4G Hynix 256Mx16 -->30.1K PU Single Rank
4G Hynix 256Mx16 -->24.9K PU Dual Rank
4G Micron 256Mx16 -->10K PD
4G Samsumg 256Mx16 -->15K PD

ROM_SO
N16S-GT --> 4.99K PD

ROM_SCLK
N16S-GT --> 4.99K PD

STRAP0
N16S-GT --> 49.9K PU

Resistor P/N

4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18
49.3K ---> CS34992FB10

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N16S-GTR-S-A2 PN : AJ0N16S0T44

N17S-G1-A1 PN : AJ0N17S0T00

N16S-GT VRAM Configuration Table ROM_SI

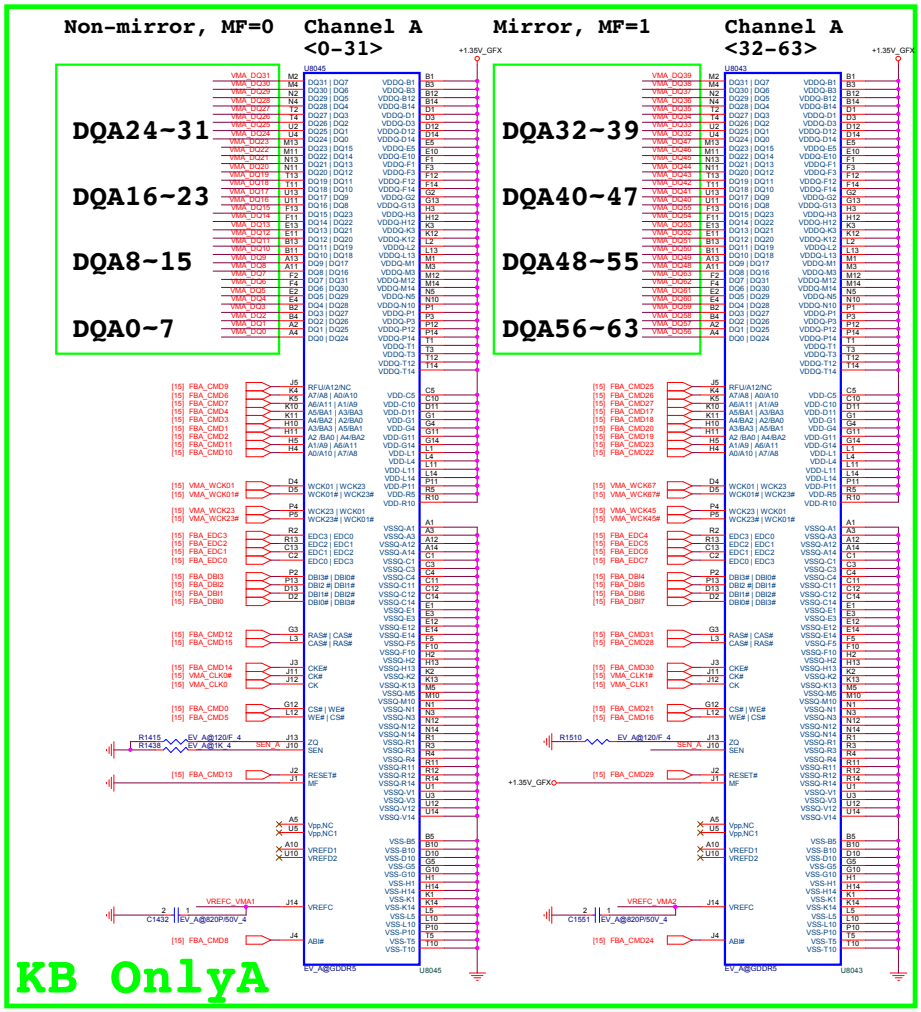
RAMCFG [3:0]	DESCRIPTION 1.35V DDR5	Vendor	Vendor P/N	ROM_SI	STN B/S	
0000 0x0	DDR5 256Mx32, 64bit, 8Gb,2500MHz	SAMSUNG B-die	K4G80325FB-HC03	PD 4.99K ohm	AKG5QGDT502	
0000 0x0	DDR5 256Mx32, 64bit, 8Gb,3000MHz	SAMSUNG B-die	K4G80325FB-HC28	PD 4.99K ohm	AKG5QGDT518	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb,2500MHz	Micron A-die	MT51J256M32HF-60:A	PD 10K ohm	AKG5LGUTL04	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb,3000MHz	Micron A-die	MT51J256M32HF-70:A	PD 10K ohm	AKG5QGUTL15	
0101 0x5	DDR5 256Mx32, 64bit, 8Gb,2500MHz	HYNIX M-die	H5GC8H24MJR-T2C	PD 30.1K ohm	AKG5QFUTW04	
0101 0x5	DDR5 256Mx32, 64bit, 8Gb,3000MHz	HYNIX M-die	H5GC8H24MJR-R0C	PD 30.1K ohm	AKG5QGUTW06	

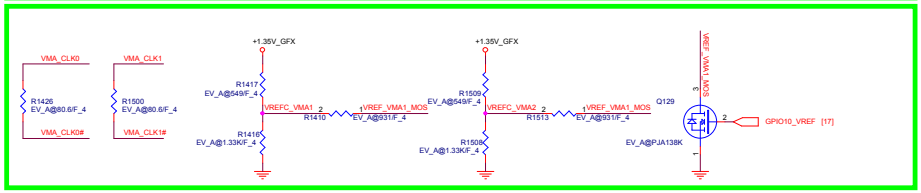
N17S-G1-A1 VRAM Configuration Table STRAP0 , STRAP1 , STRAP2

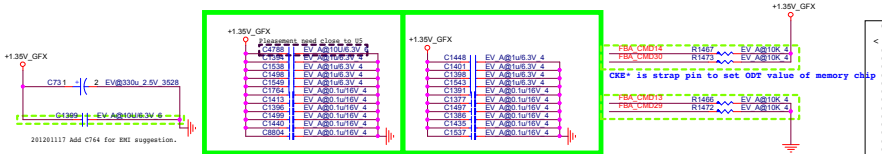
RAMCFG [3:0]	DESCRIPTION 1.35V DDR5	Vendor	Vendor P/N	STRAP0	STRAP1	STRAP2	STN B/S	
0000 0x0	DDR5 256Mx32, 64bit, 8Gb,3000MHz	SAMSUNG B-die	K4G80325FB-HC28	PD 100K ohm	PD 100K ohm	PD 100K ohm	AKG5QGDT518	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb,3000MHz	Micron A-die	MT51J256M32HF-70:A	PU 100K ohm	PD 100K ohm	PD 100K ohm	AKG5QGUTL15	
0010 0x2	DDR5 256Mx32, 64bit, 8Gb,3000MHz	HYNIX M-die	H5GC8H24MJR-R0C	PD 100K ohm	PU 100K ohm	PD 100K ohm	AKG5QGUTW06	

Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number: N16S-GT (GPIO/STRAPS) | Rev: 2A
Date: Thursday, June 22, 2017 | Sheet 17 of 47

CHANNEL A: 1024MB GDDR5x32







RST PD place @ the end of daisy-chain.

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

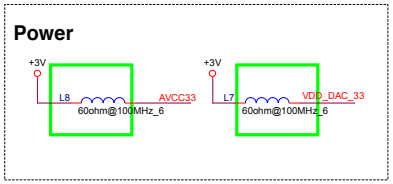
Quanta Computer Inc.

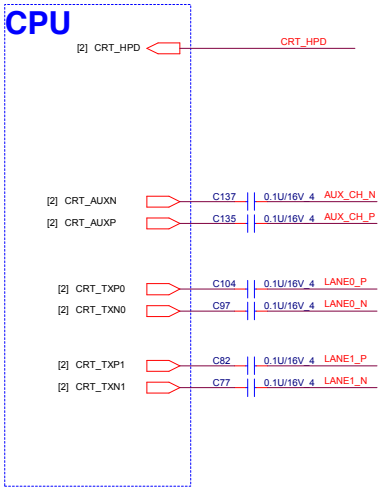
PROJECT : Z8VR

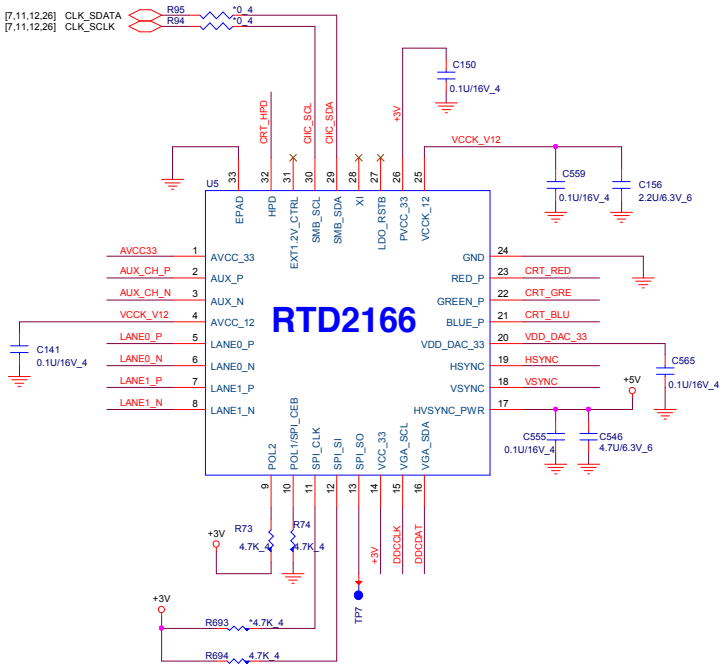
Size	Document Number	Rev
	N16x - 6/6 (GDDR5x32)	3A

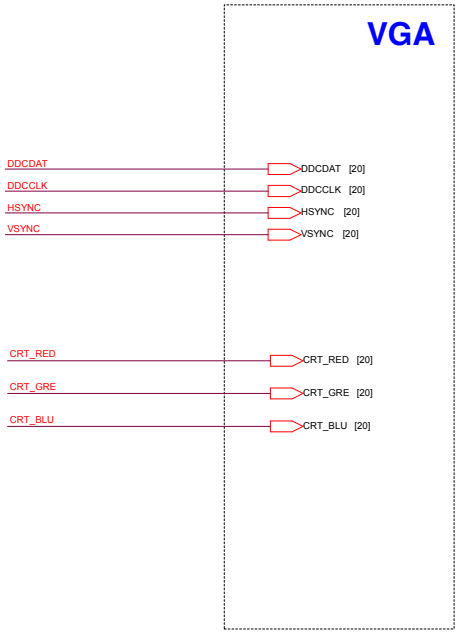
Date: Thursday, June 22, 2017 Sheet 18 of 47

DP TO VGA









Note:

1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
2- C5 shold be X5R material
3- R6, R7, R8 should be 75 ohm with +/-1%
4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
5- This configuration is for internal ROM mode and using embedded LDO mode.

[2,4,6,7,8,9,11,12,14,15,16,17,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40] +3V
[20,21,23,24,26,30,37] +5V

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	DP to VGA IT6165	1A
Date: Thursday, June 22, 2017	Sheet 19 of 46	

CRT

RTD2166 integrate 5V HSYNC/VSYNC buffer inside IC

12/24 Delete R449
12/18 Change R412 to 47ohm for vendor requset
12/24 Delete R396
12/18 Change R399 to 47ohm for vendor requset
Co-Layout
Realtek FAE suggest close to connector
*M74VHC1GT125DF2G

Close to RTD2166 IC
AP2331SA-7
12/18 Change to BLM15BB220SN1D (CZSBB220005) for vendor requset
12/18 Un-Stuff C95/C128/C148 for vendor requset
12/21 Change CN5 footprint to "dsub-95-0005-01-15p" for layout requset
CRT CONN
AZ1045-04F.R7G
Realtek FAE suggest close to connector
12/18 Un-Stuff C539/C551 for vendor requset

Power trace tracking

LCD CONNECTOR

ESD
2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage
MAX 1.5A
eDP FHD
Touch Panel-I2C
Touch Panel-USB
eDP 4k*2k
CCD-USB
Prevent ESD/EOS Layout near device
50398-04071-001

1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.

Touch Panel interrupt

Hall Sensor (HSR)

1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

LCD Power

1st : AL005245000---GMT
2nd : AL007553000---UPI

Touch screen level shift I2C(reserve)

S5
S0
TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.

LID591#,EC intrnal PU

1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

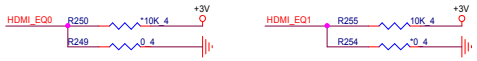
Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number: CRT/LVDS/CAMERA/LID | Rev 1A
Date: Thursday, June 22, 2017 | Sheet 20 of 46

HDMI

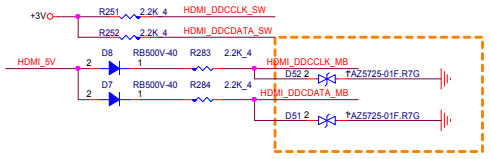
<HDM>

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode: DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

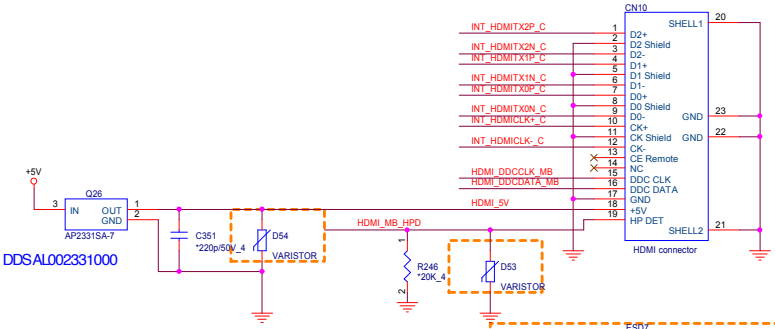
Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB



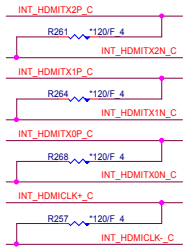
HDMI-detect

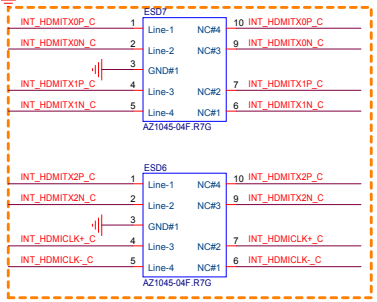


HDMI connector



EMI





Power trace tracking

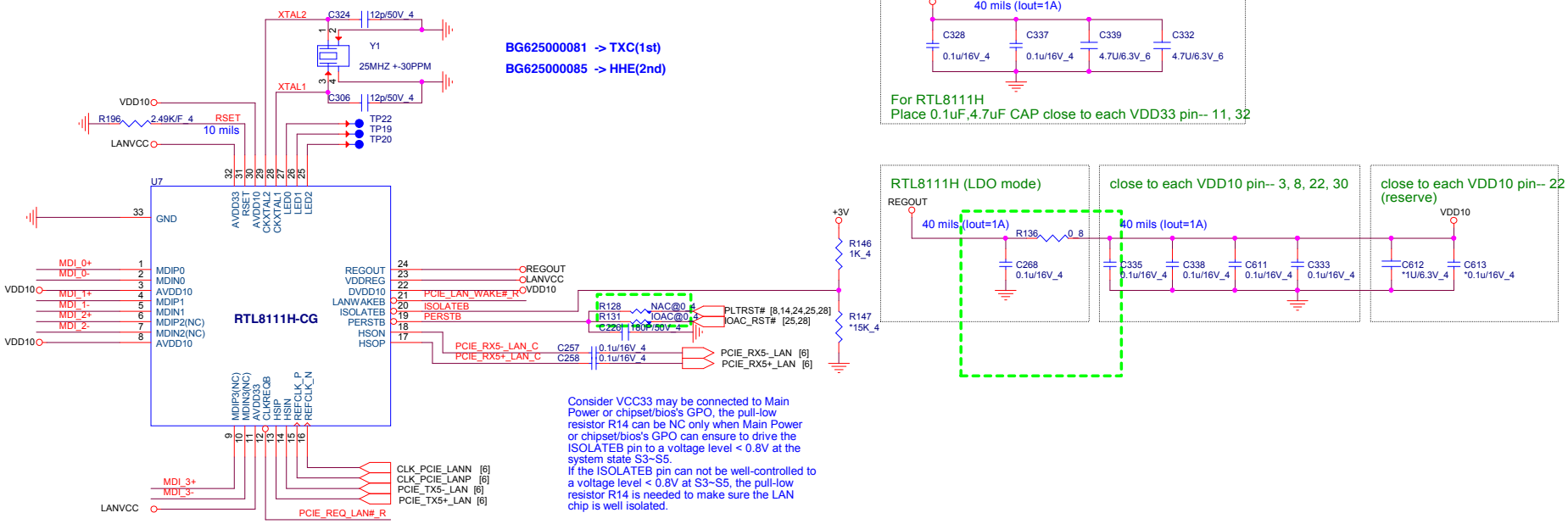
[2,4,6,7,8,9,11,12,14,15,16,17,19,20,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40] +3V
[19,20,23,24,26,30,37] +5V

Quanta Computer Inc.

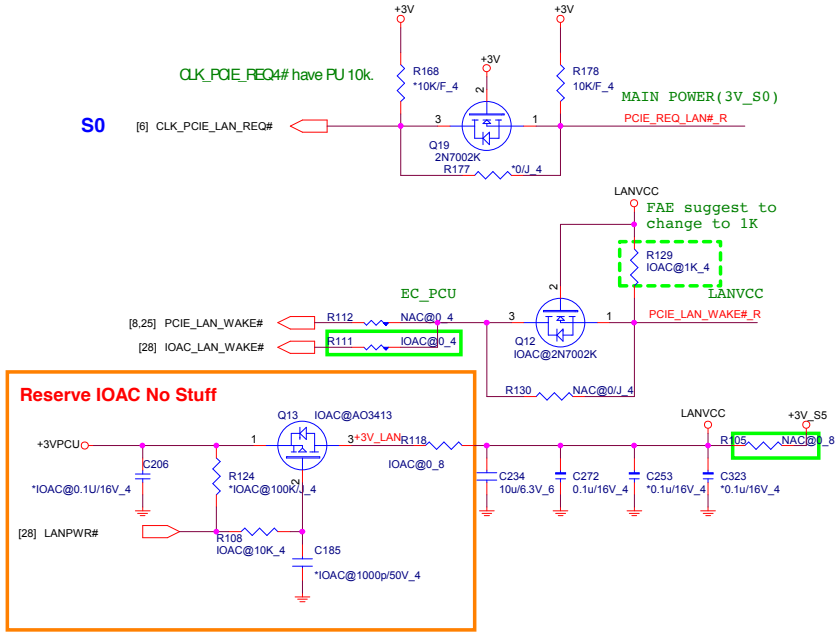
PROJECT : Z8VR

Size	Document Number	Rev
	HDMI (PS8407 4k*2k)	1A
Date: Thursday, June 22, 2017	Sheet 21 of 46	

Giga LAN (LAN)

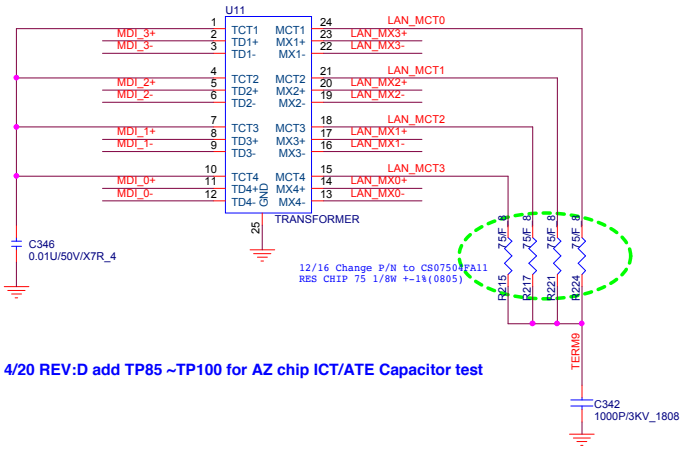


Leakage circuit (MPC)



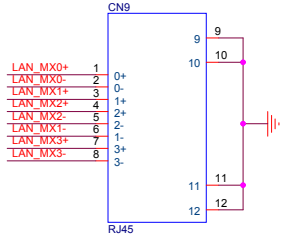
Tramsformer

Layout:All termination signal should have 30 mil trace



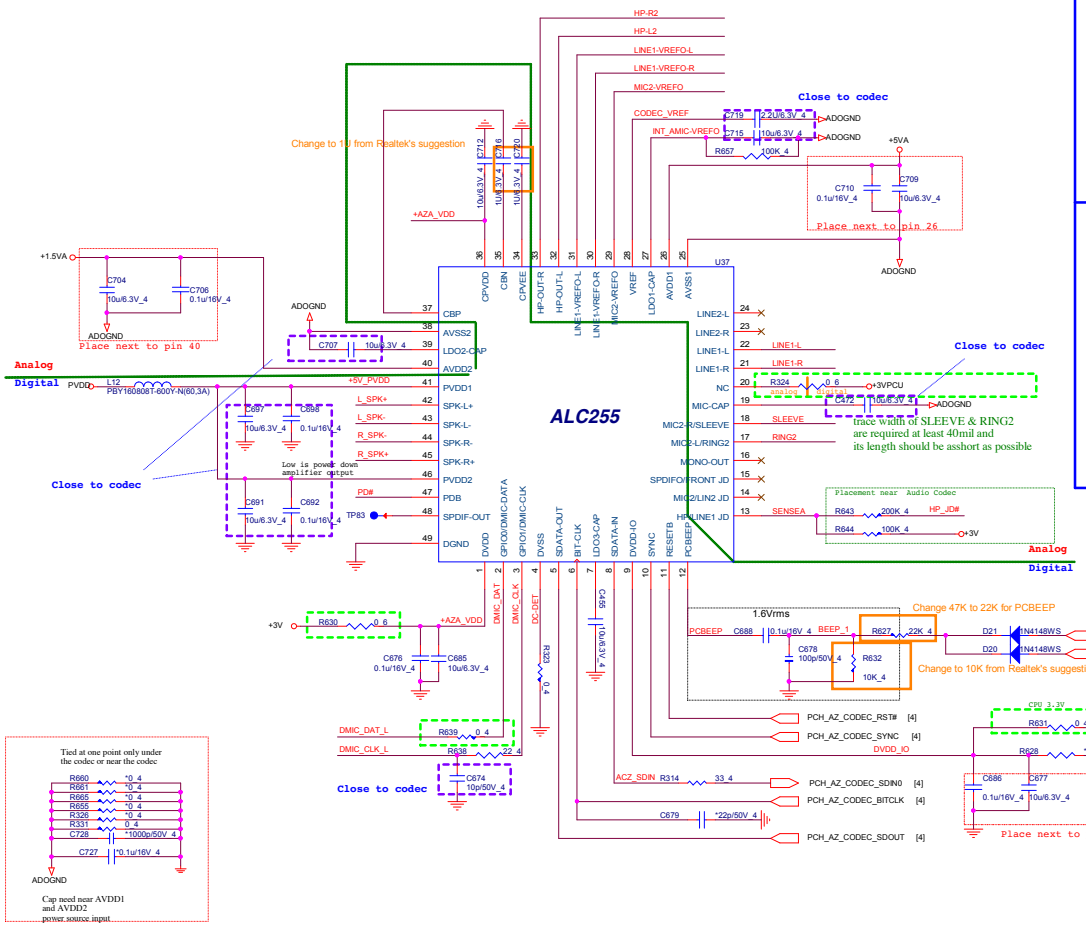
4/20 REV:D add TP85 ~TP100 for AZ chip ICT/ATE Capacitor test

RJ45 Connector

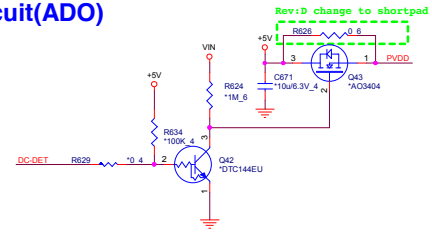


Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: LAN(RTL8111H)	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 22 of 46	

Codec(ADO)

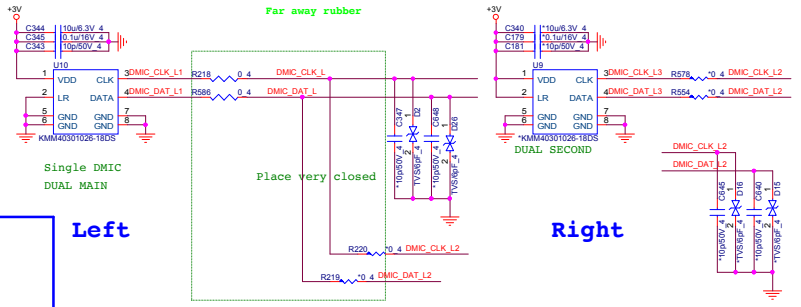


DC-DET circuit(ADO)



D-Mic (MIC)

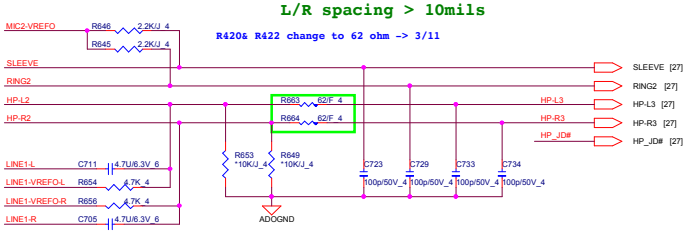
Single DMIC and Dual DIMC same PN: AL403010A00



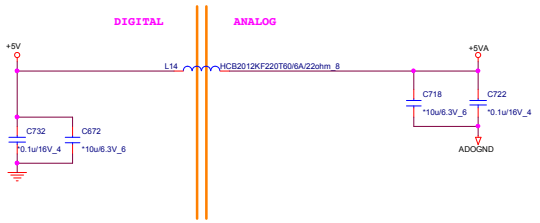
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils

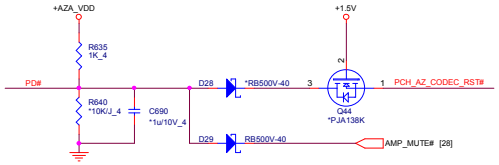
R420& R422 change to 62 ohm -> 3/11



Codec PWR 5V(ADO)

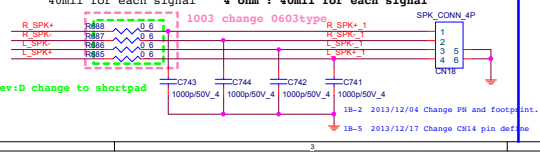


Mute(ADO)

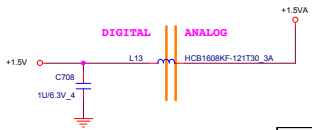


Internal Speaker

40mil for each signal 4 ohm : 40mil for each signal



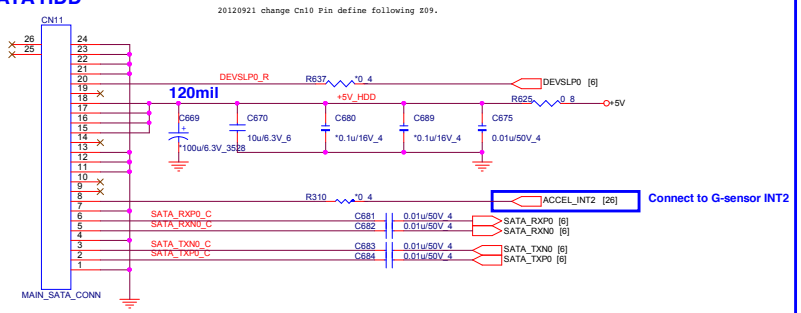
Codec PWR 1.5V(ADO)



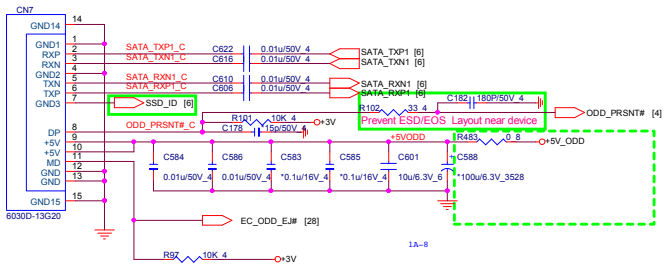
Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	ALC255/HP/SPK	1A
Date: Thursday, June 22, 2017	Sheet 23 of 48	

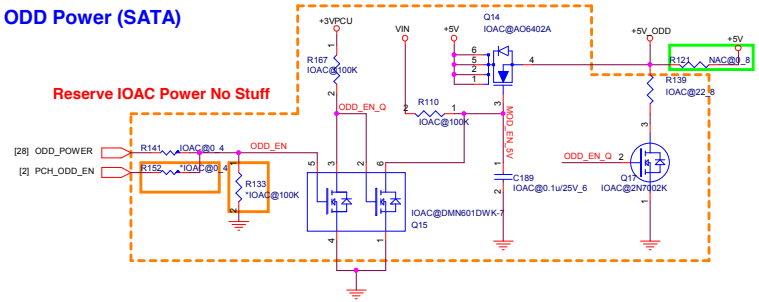
SATA HDD



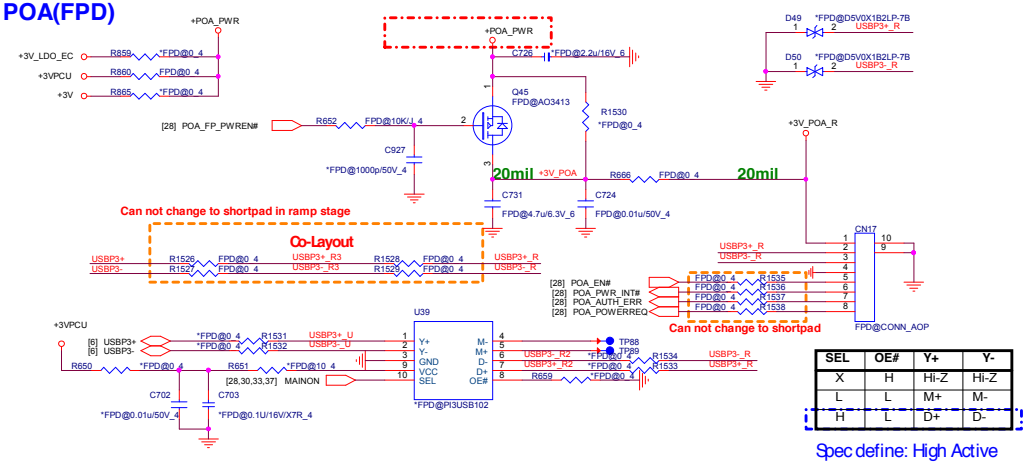
SATA ODD Connector



ODD Power (SATA)



POA(FPD)



SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

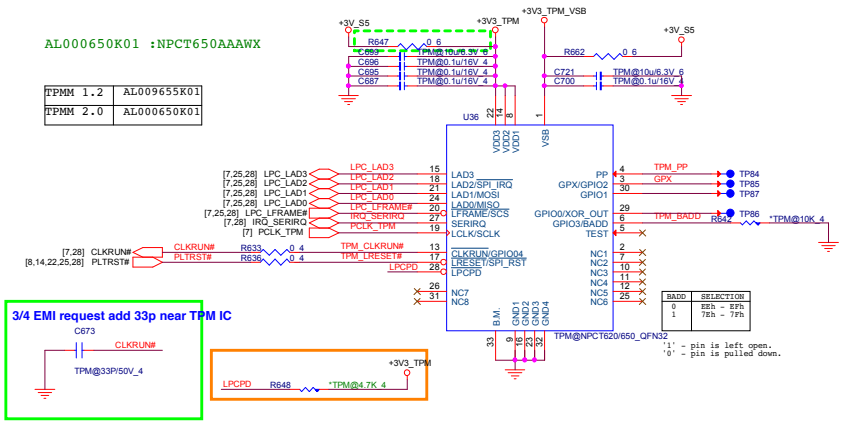
Spec define: High Active

TPM NPCT650 (TPM)

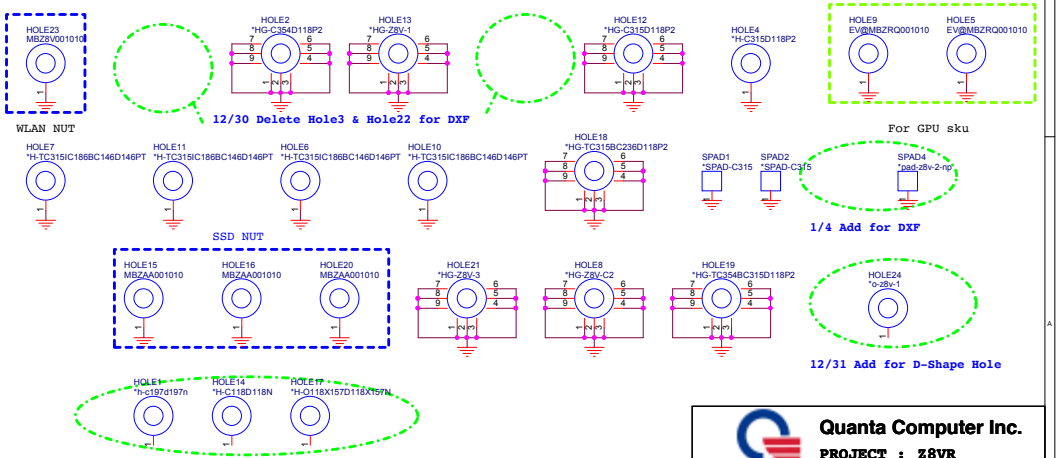
SP@ BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAWX)

AL000650K01 :NPCT650AAAWX

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01



3/4 EMI request add 33p near TPM IC

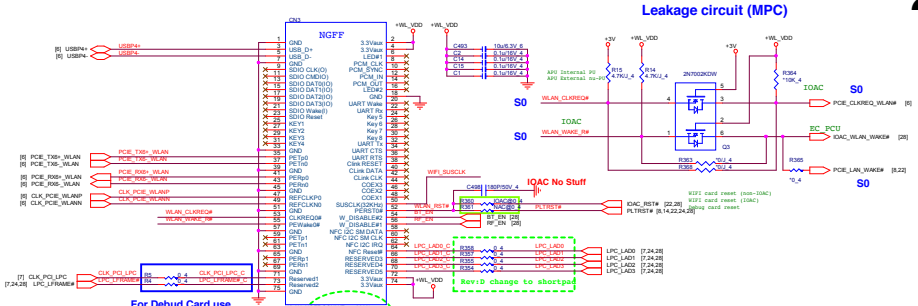


Quanta Computer Inc.	PROJECT : Z8VR	
Size	Document Number: HDD/ODD/TPM NPCT650	Rev 1A
Date: Thursday, June 22, 2017	Sheet 24 of 46	

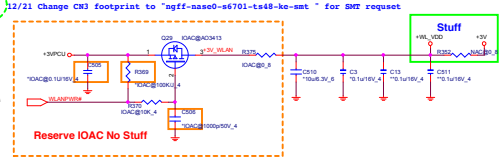
NGFF_M.2 WiFi & BT (NGF)

25

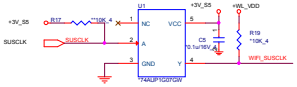
Leakage circuit (MPC)

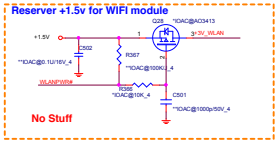


Low	Mini card +3V power enable
High	Mini card +3V power disable

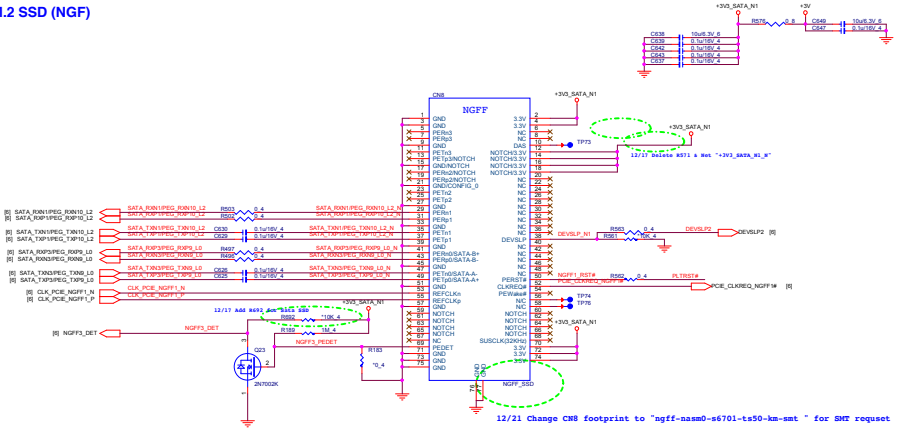


Reserve only for Intel module no need to stuff by default 11/24



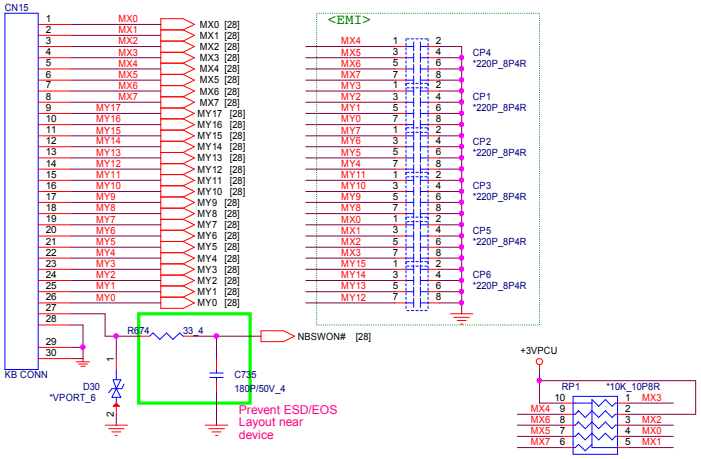


NGFF_M.2 SSD (NGF)

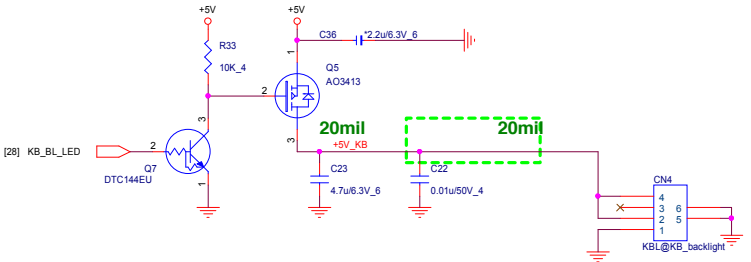


Quanta Computer Inc.			
PROJECT : Z8VR			
Size	Document Number		Rev
	NGFF WiFi & BT & SSD		1A
Date: Thursday, June 22, 2017	Sheet 25 of 46		

KEYBOARD (KBC)



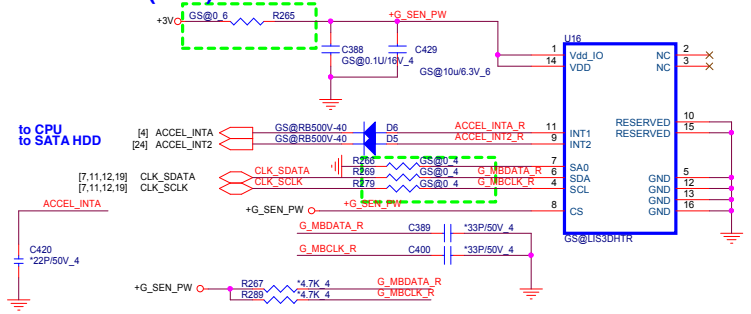
KB_BL LED (KBC)



1A-7 2013/10/22 change CN25 pin define for spec.

1A-8 2013/10/23 change CN25 footprint.

G-sensor(ACS)



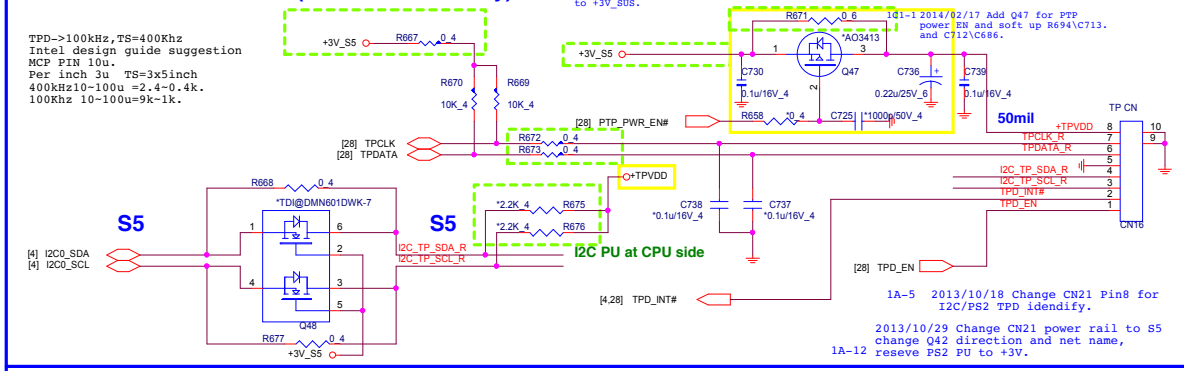
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.

1A-4 2014/01/15 reserve TP power rail +3V_S5.

1A-1 2014/02/17 Add Q47 for PTP power EN and soft up R694\C713. and C712\C686.

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4-0.4k.
100Khz 10~100u=9k~1k.



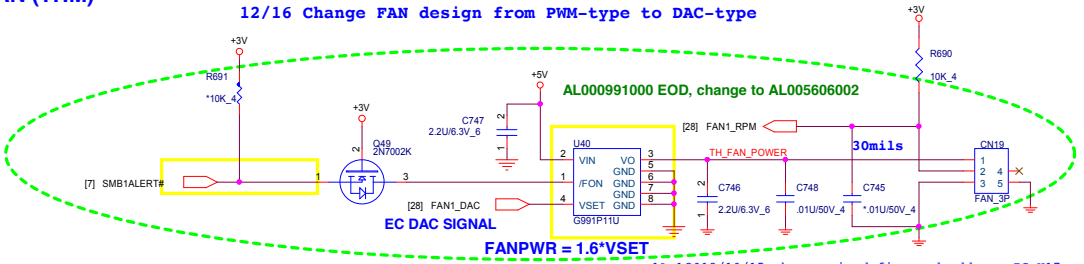
1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.

2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,

1A-12 reseve PS2 PU to +3V.

CPU FAN (THM)

12/16 Change FAN design from PWM-type to DAC-type



1A-12013/10/15 change pin define and add pwm IC U17.

1A-42013/10/17 Change U17 to G991P11U and PU U17 pin1.

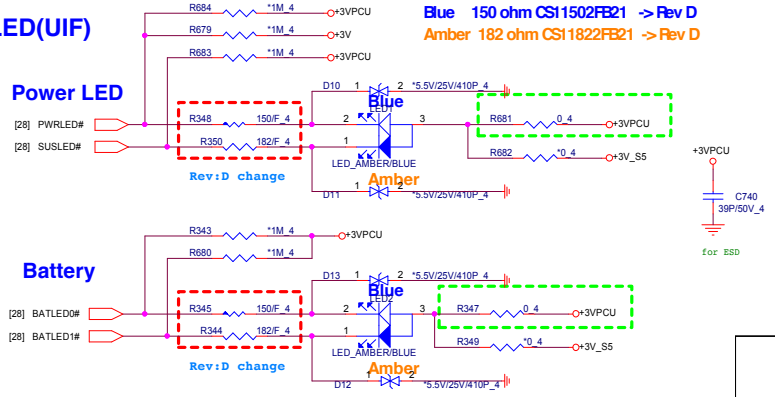
1A-92013/10/24 Add alert on U17.1 for CPU themal tempture.

1A-13 2013/10/31CN15 Pin2/3 swap.

POWER LED(UIF)

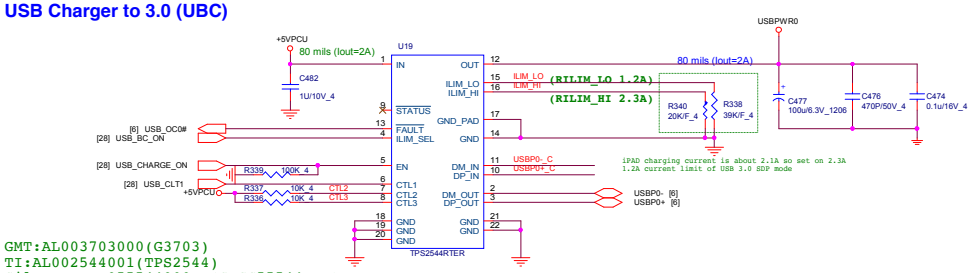
Blue 150 ohm CS11502FB21 -> Rev D

Amber 182 ohm CS11822FB21 -> Rev D



Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: KB/TP/FAN	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 26 of 46	

USB Charger to 3.0 (UBC)



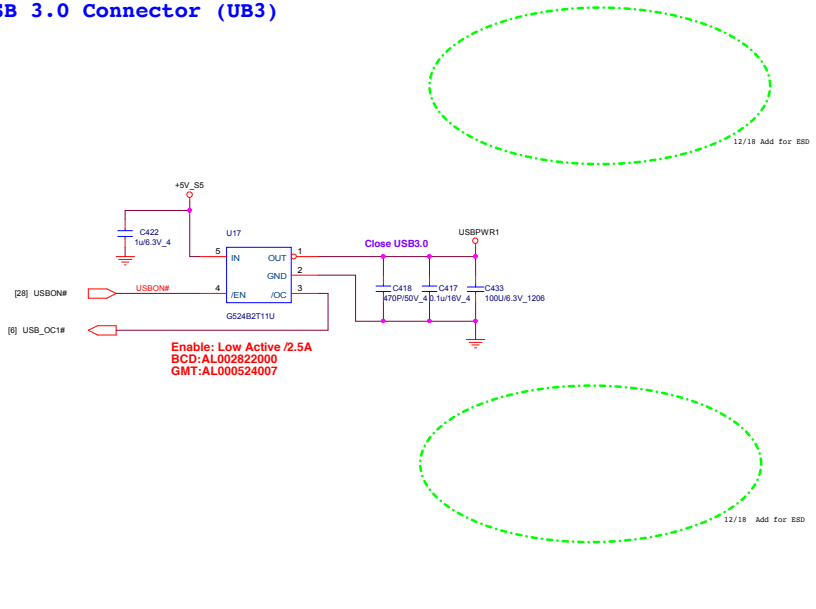
GMT:AL003703000(G3703)
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

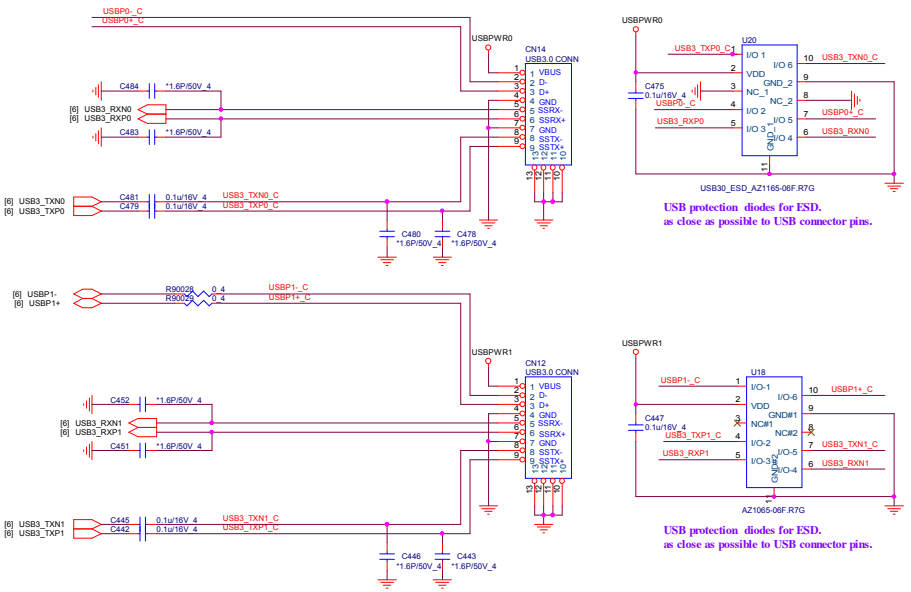
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

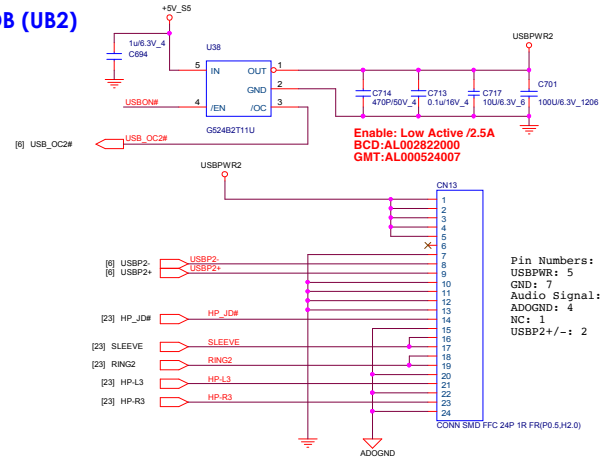
$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

USB 3.0 Connector (UB3)

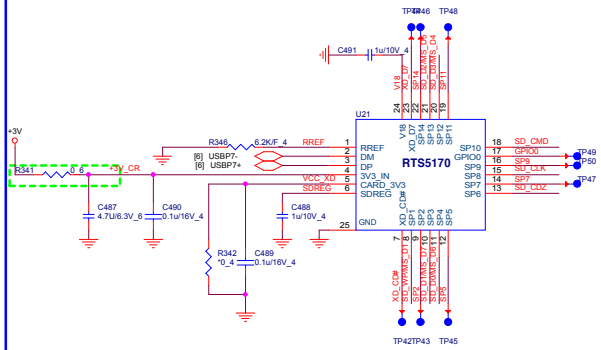


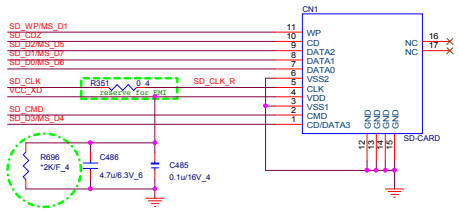


USB2.0 DB (UB2)

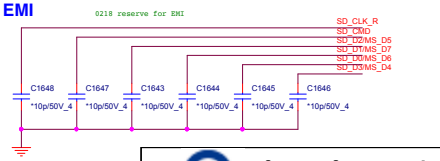


Card Reader (CRD)





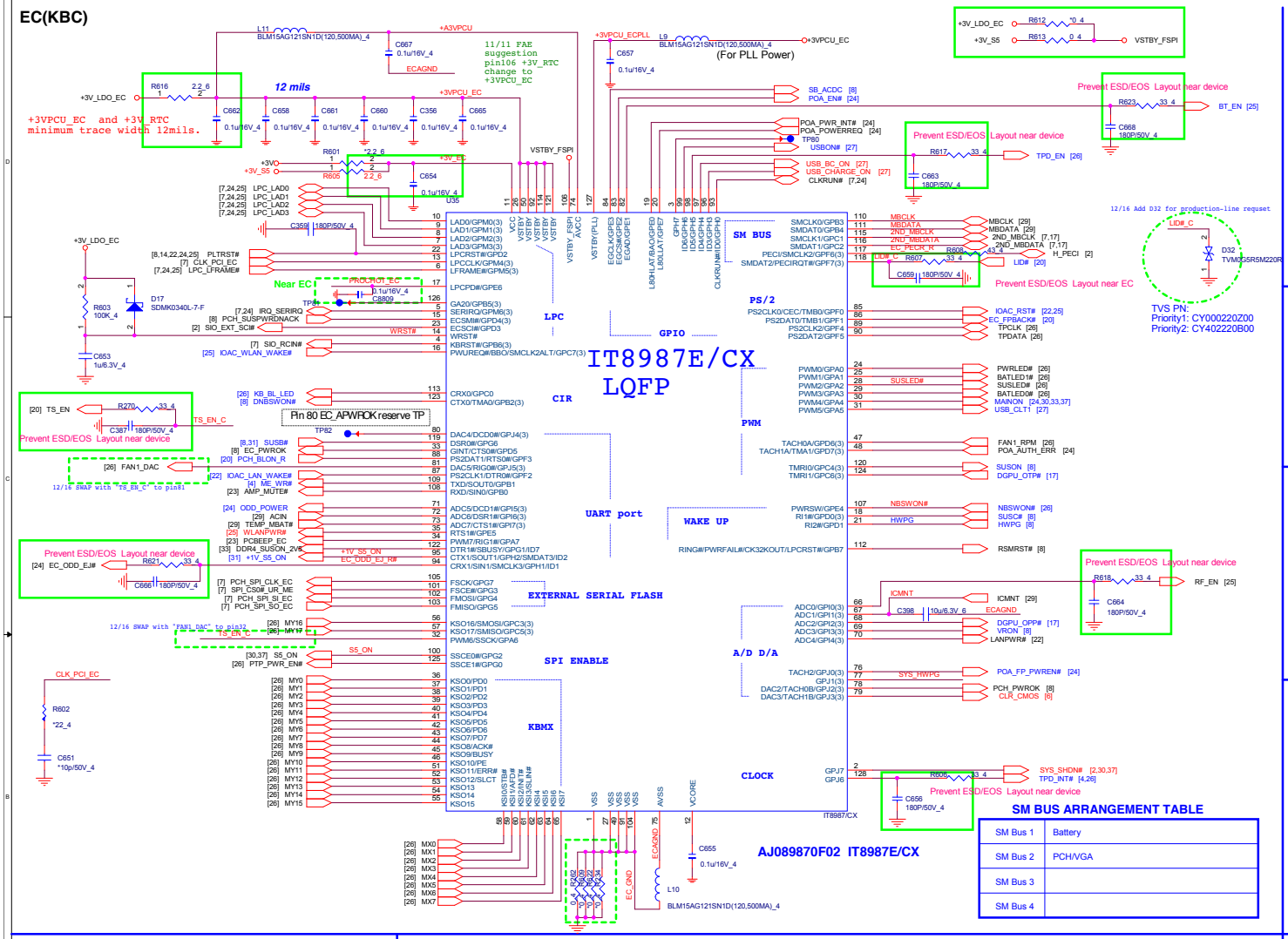
EMI



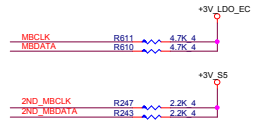
Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	USB3/Charger/CR/USB2 DB	1A
Date: Thursday, June 22, 2017	Sheet 27 of 48	

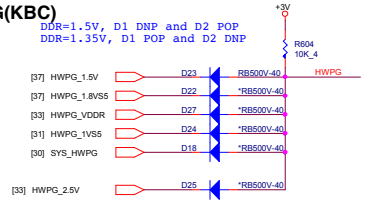
EC(KBC)



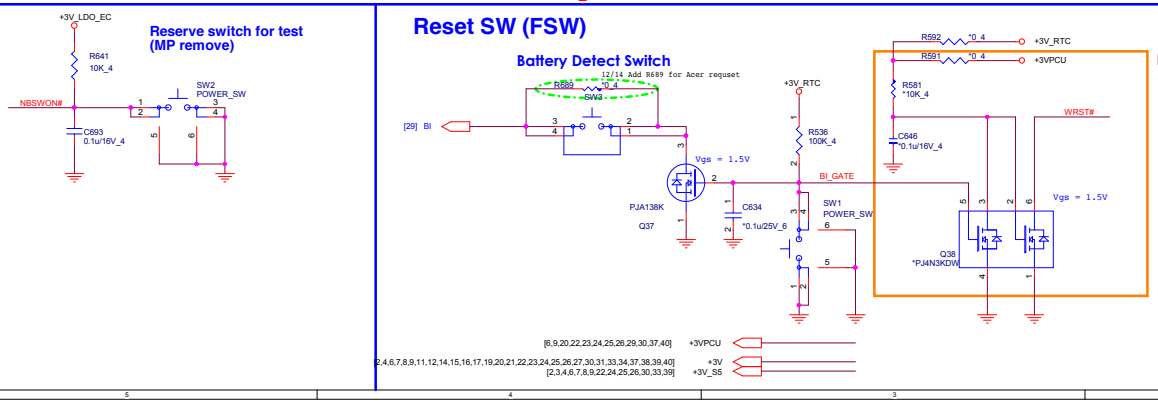
SM BUS PU(KBC)



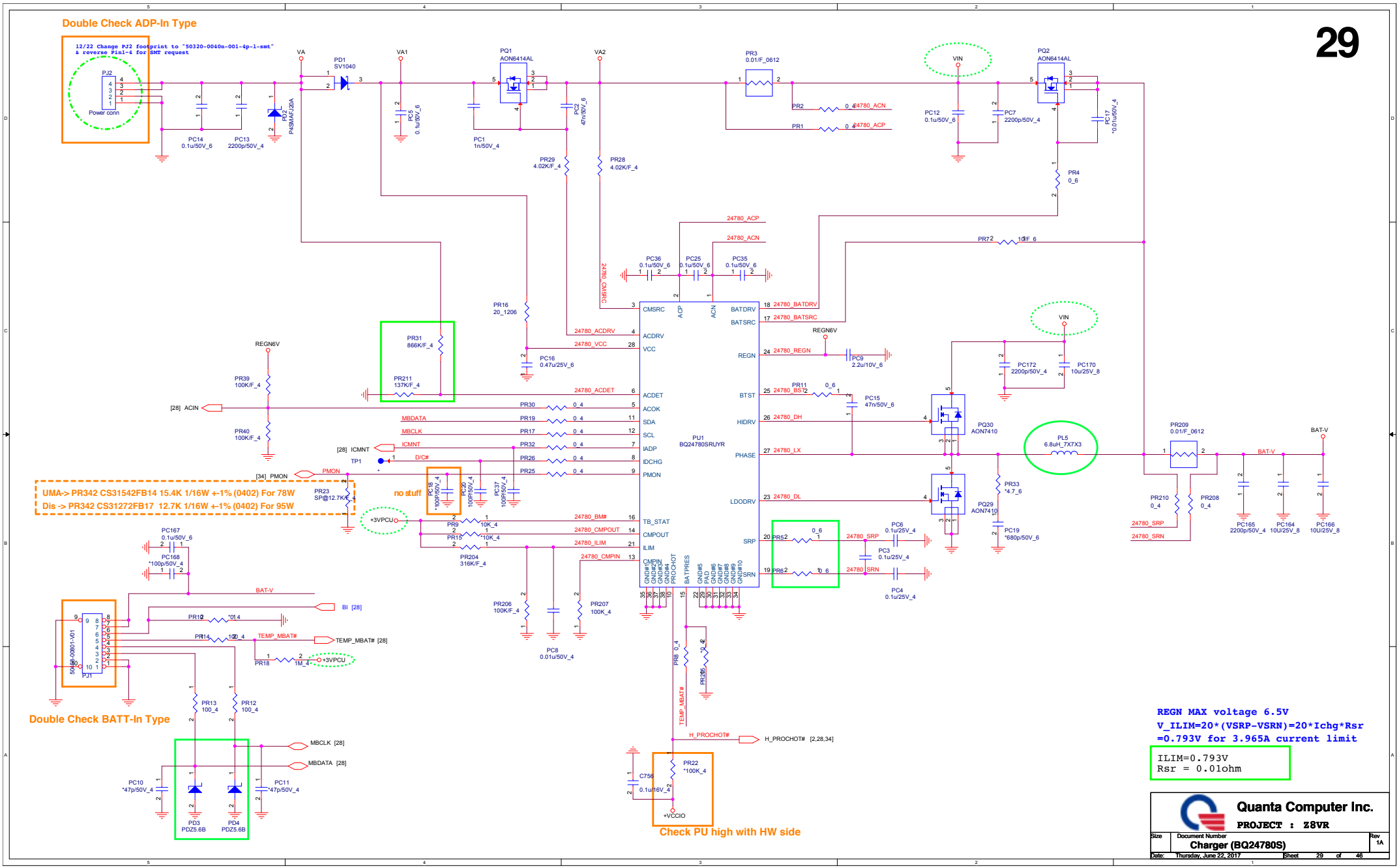
HWPG(KBC)

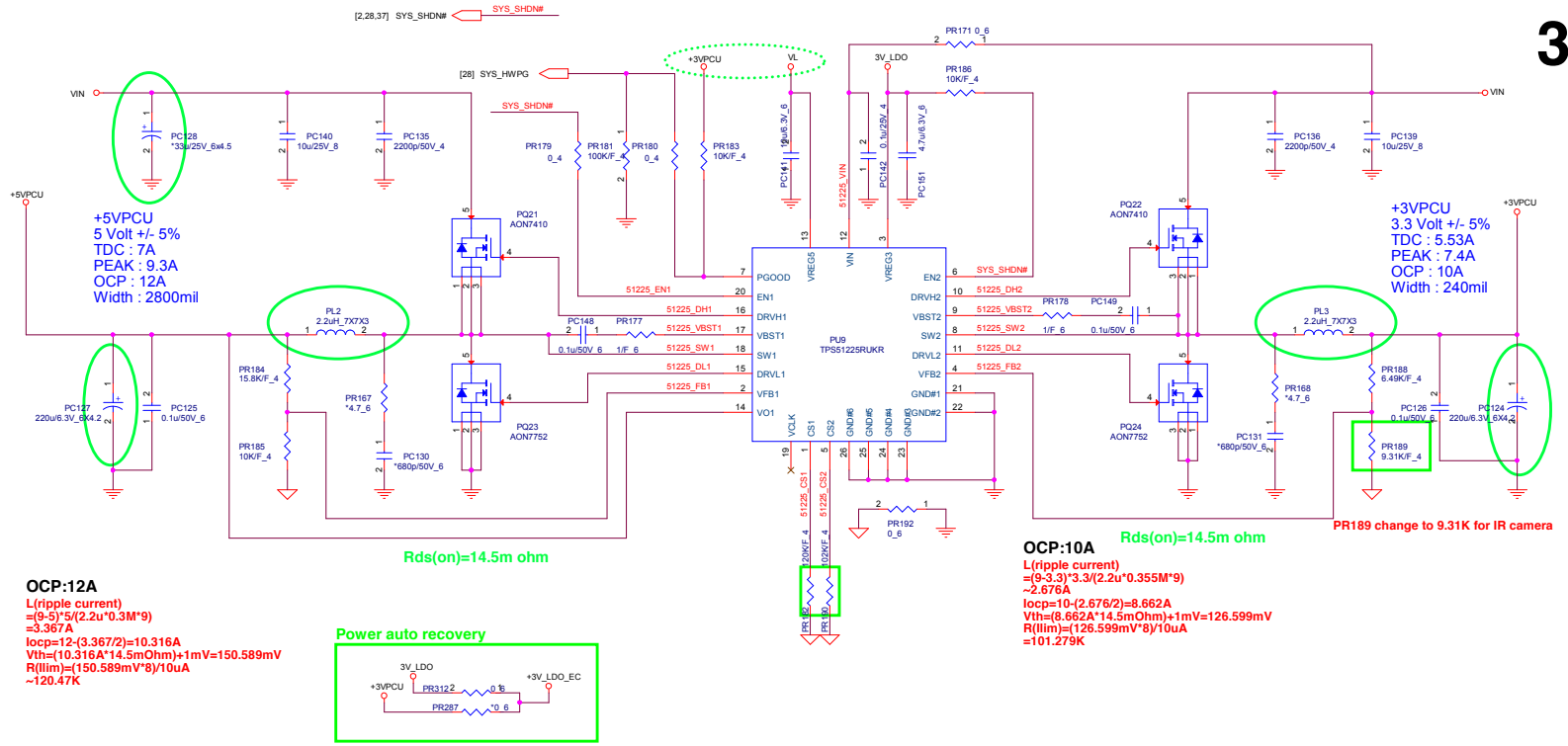


Reset SW (FSW)



Quanta Computer Inc.	
PROJECT : Z8VR	
Size	Document Number: KBC IT8587 — Rev: 1A
Date: Thursday, June 22, 2017	Sheet 28 of 46


Double Check ADP-In Type
12/22 Change PJ2 footprint to "50320-0040n-001-4p-l-smt" & reverse Pin1~4 for SMT request
PJ2
Power conn
PD1 SV1040
PD2 P4SMAJ7.0A
PQ1 AON6414AL
PQ2 AON6414AL
PR3 0.01/F_0612
PR2 0_4780_ACN
PR1 0_4780_ACP
PR4 0_6
PR29 4.02K/F_4
PR28 4.02K/F_4
PR16 20_1206
PR31 866K/F_4
PR211 137K/F_4
PR39 100K/F_4
PR40 100K/F_4
PR23 SP@12.7K/F
UMA-> PR342 CS31542FB14 15.4K 1/16W +-1% (0402) For 78W
Dis -> PR342 CS31272FB17 12.7K 1/16W +-1% (0402) For 95W
no stuff
PU1 BQ24780SRUYR
CMSRC
ACDRV
VCC
ACDET
ACOK
SDA
SCL
IADP
IDCHG
PMON
TB_STAT
CMPOUT
ILIM
CMPIN
PROCHOT
BATPRES
BATDRV
BATSRC
REGN
BTST
HIDRV
PHASE
LODRV
SRP
SRN
PQ30 AON7410
PQ29 AON7410
PL5 6.8uH_7X7X3
PR33 *4.7_6
PC19 *680p/50V_6
PR209 0.01/F_0612
PR210 0_4
PR208 0_4
PC165 2200p/50V_4
PC164 10U/25V_8
PC166 10U/25V_8
PC167 0.1u/50V_6
PC168 *100p/50V_4
PJ1
Double Check BATT-In Type
PR13 100_4
PR12 100_4
PC10 *47p/50V_4
PC11 *47p/50V_4
PD3 PDZ5.6B
PD4 PDZ5.6B
PR206 100K/F_4
PR207 100K_4
PC8 0.01u/50V_4
PR8 0_4
PR22 *100K_4
C756 0.1u/16V_4
+VCCIO
Check PU high with HW side
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
Quanta Computer Inc.
PROJECT : Z8VR
Charger (BQ24780S)
Rev 1A
Thursday, June 22, 2017
Sheet 29 of 46



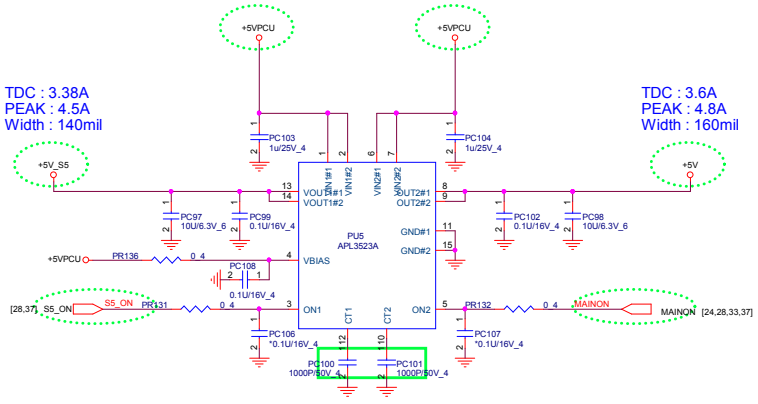
OCP:12A

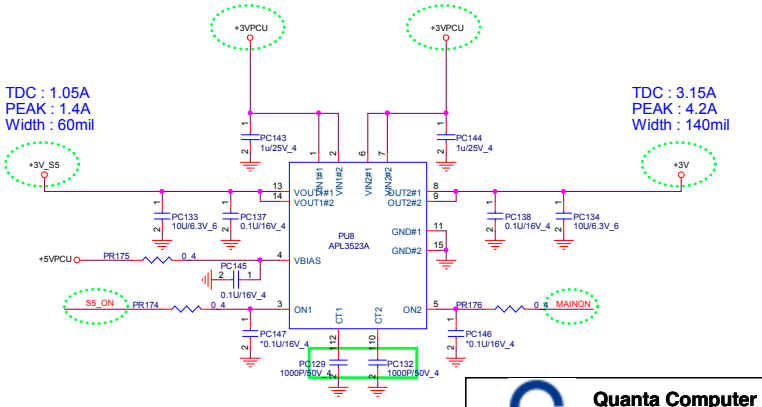
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=12-(3.367/2)=10.316A
Vth=(10.316A*14.5mOhm)+1mV=150.589mV
R(Ilim)=(150.589mV*8)/10uA
~120.47K

OCP:10A

L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=10-(2.676/2)=8.662A
Vth=(8.662A*14.5mOhm)+1mV=126.599mV
R(Ilim)=(126.599mV*8)/10uA
=101.279K

Power auto recovery

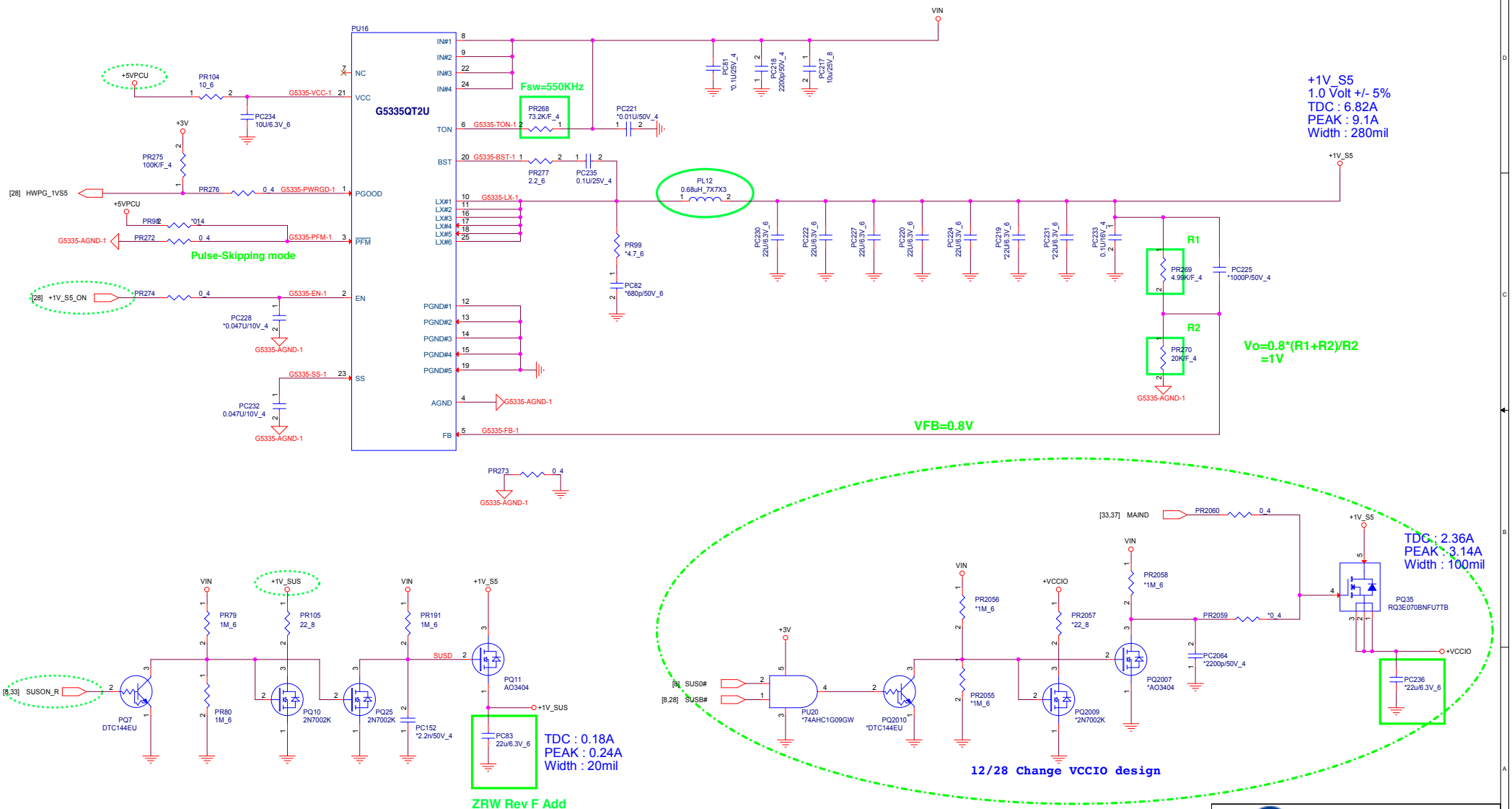


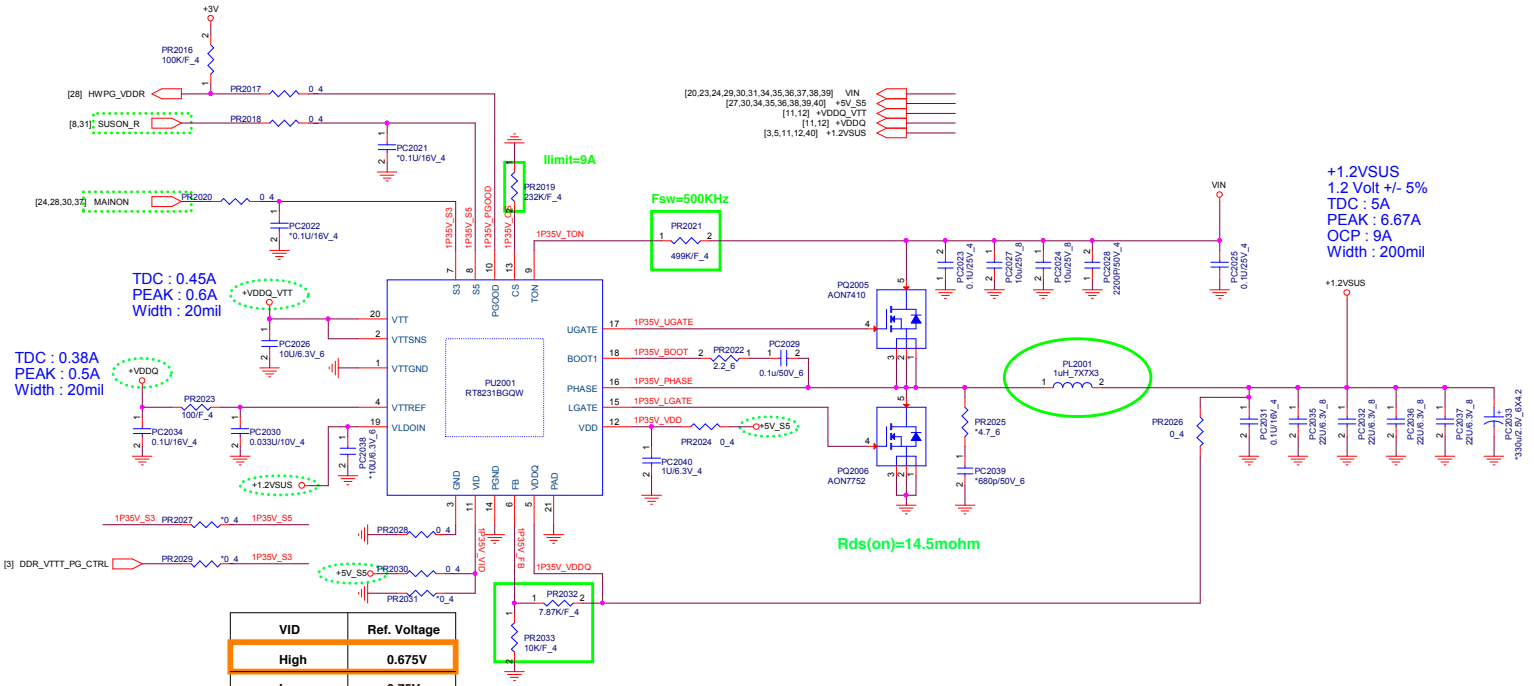


Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	SYSTEM 5V/3V (TPS51225R)	1A

Date: Thursday, June 22, 2017 Sheet 30 of 46


PU16
G5335QT2U
Fsw=550KHz
Pulse-Skipping mode
VFB=0.8V
+1V_S5
1.0 Volt +/- 5%
TDC : 6.82A
PEAK : 9.1A
Width : 280mil
Vo=0.8*(R1+R2)/R2
=1V
R1
R2
TDC : 0.18A
PEAK : 0.24A
Width : 20mil
ZRW Rev F Add
TDC : 2.36A
PEAK : 3.14A
Width : 100mil
12/28 Change VCCIO design



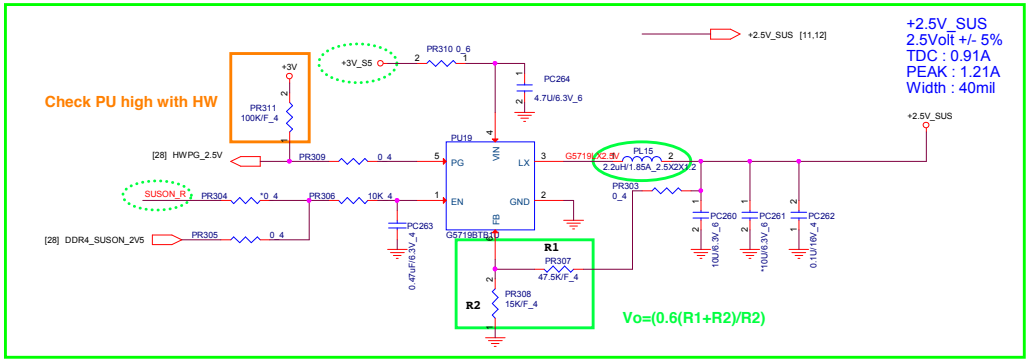
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=9A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=9-(2.248/2)*14.5mohm
=114.202mV
Rlimit=114.202mV/5uA*10=228.4Kohm

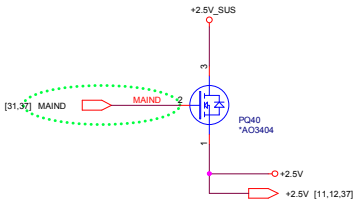
DDR=1.2V
PR2032=7.87K/F_4
PR2033=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

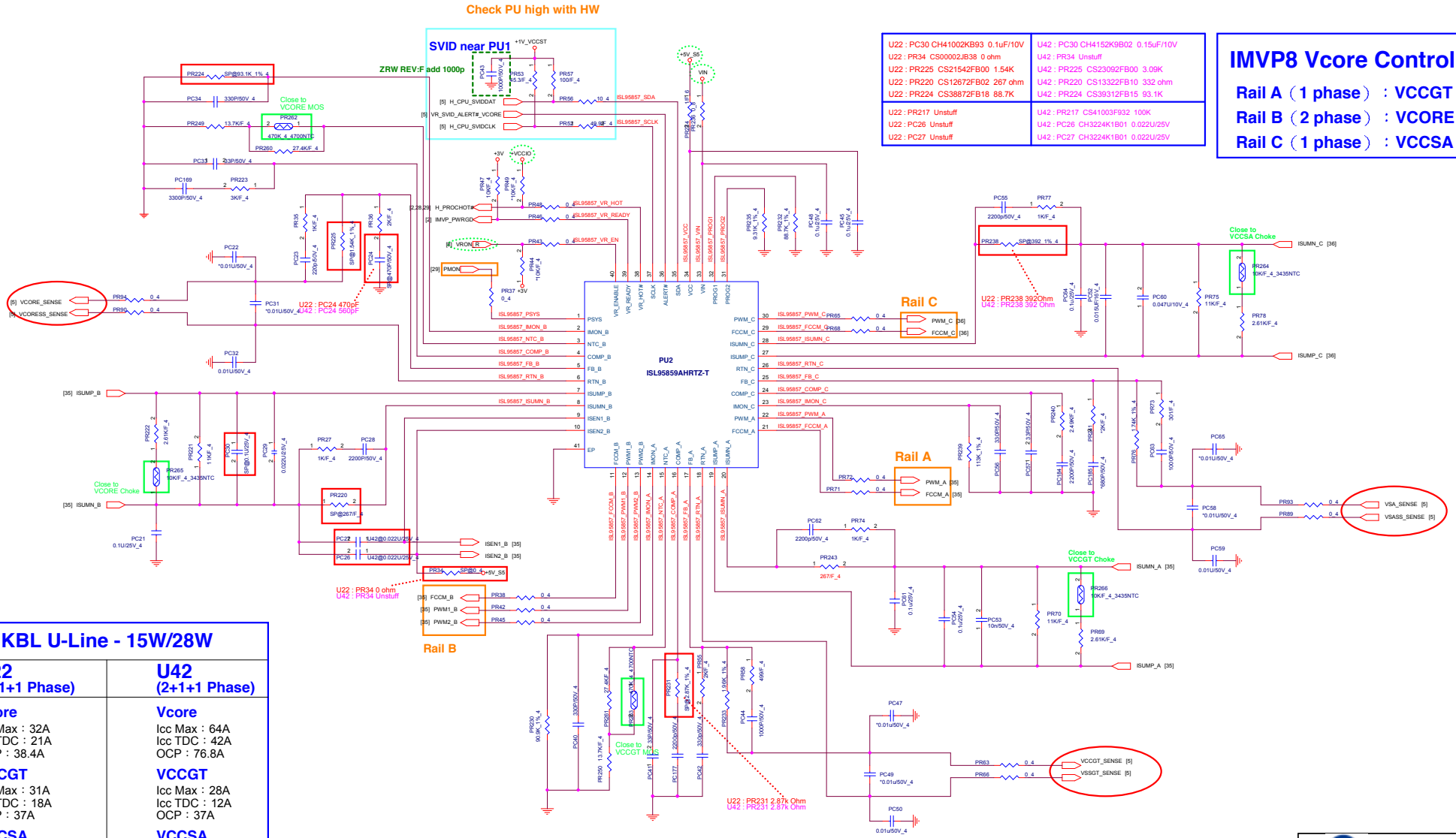
+2.5VSUS Power Rail For DDR4



10/26 Reserve +2.5V for DDR4 VDDSPD



Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number: DDR4_+1.2VSUS (G5316RZ1D) | Rev 1A
Date: Thursday, June 22, 2017 | Sheet 33 of 46



U22	U42
U22 : PC30 CH41002KB93 0.1uF/10V	U42 : PC30 CH4152K9B02 0.15uF/10V
U22 : PR34 CS00002JB38 0 ohm	U42 : PR34 Unstuff
U22 : PR225 CS21542FB00 1.54K	U42 : PR225 CS23092FB00 3.09K
U22 : PR220 CS12672FB02 267 ohm	U42 : PR220 CS13322FB10 332 ohm
U22 : PR224 CS38872FB18 88.7K	U42 : PR224 CS39312FB15 93.1K
U22 : PR217 Unstuff	U42 : PR217 CS41003F932 100K
U22 : PC26 Unstuff	U42 : PC26 CH3224K1B01 0.022U/25V
U22 : PC27 Unstuff	U42 : PC27 CH3224K1B01 0.022U/25V

IMVP8 Vcore Controller

- Rail A（1 phase）：VCCGT
- Rail B（2 phase）：VCORE
- Rail C（1 phase）：VCCSA

KBL U-Line - 15W/28W

U22 (1+1+1 Phase)	U42 (2+1+1 Phase)
Vcore	**Vcore**
Icc Max：32A	Icc Max：64A
Icc TDC：21A	Icc TDC：42A
OCP：38.4A	OCP：76.8A
VCCGT	**VCCGT**
Icc Max：31A	Icc Max：28A
Icc TDC：18A	Icc TDC：12A
OCP：37A	OCP：37A
VCCSA	**VCCSA**
Icc Max：4.5A	Icc Max：5A
OCP：10A	OCP：10A

Quanta Computer Inc.
PROJECT : Z8VR

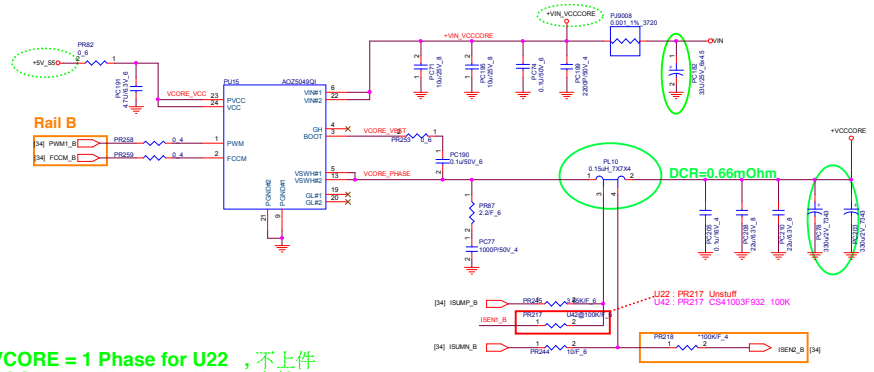
Size	Document Number	Rev
	CPU_CORE (ISL95859HRTZ-T)	1A

Date: Thursday, June 22, 2017 Sheet 34 of 46

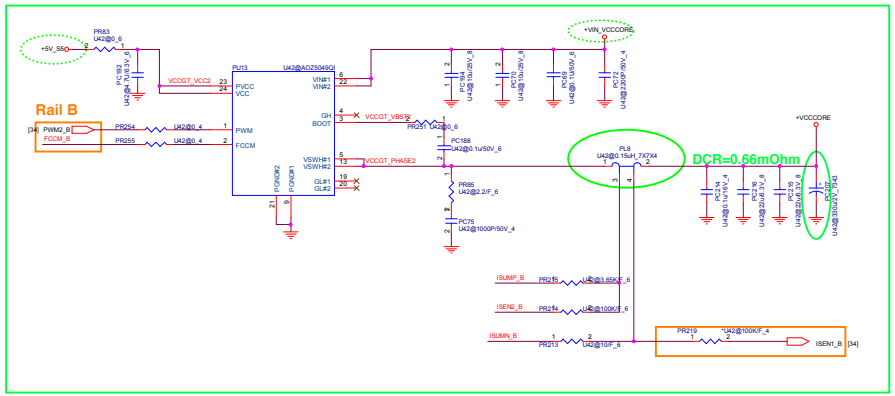
[20,23,24,29,30,31,33,34,36,37,38,39] VIN
[5] +VCCORE
[5] +VCCGT
[27,30,33,34,36,38,39,40] +5V_S5

U22 : PR217 Unstuff	U42 : PR217 CS41003F932 100K

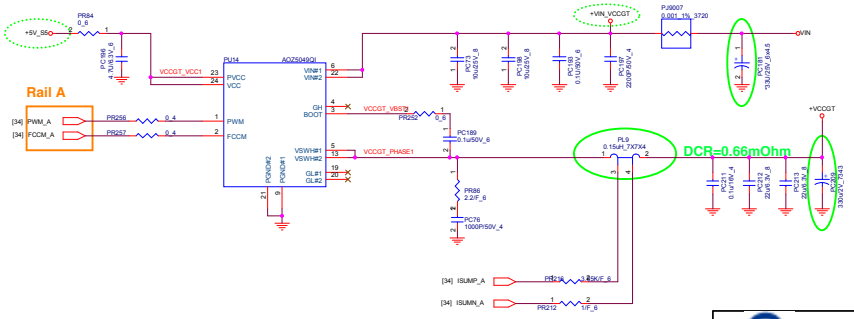
VCORE



VCORE = 1 Phase for U22 ，不上件
VCORE = 2 Phase for U42 ，上件



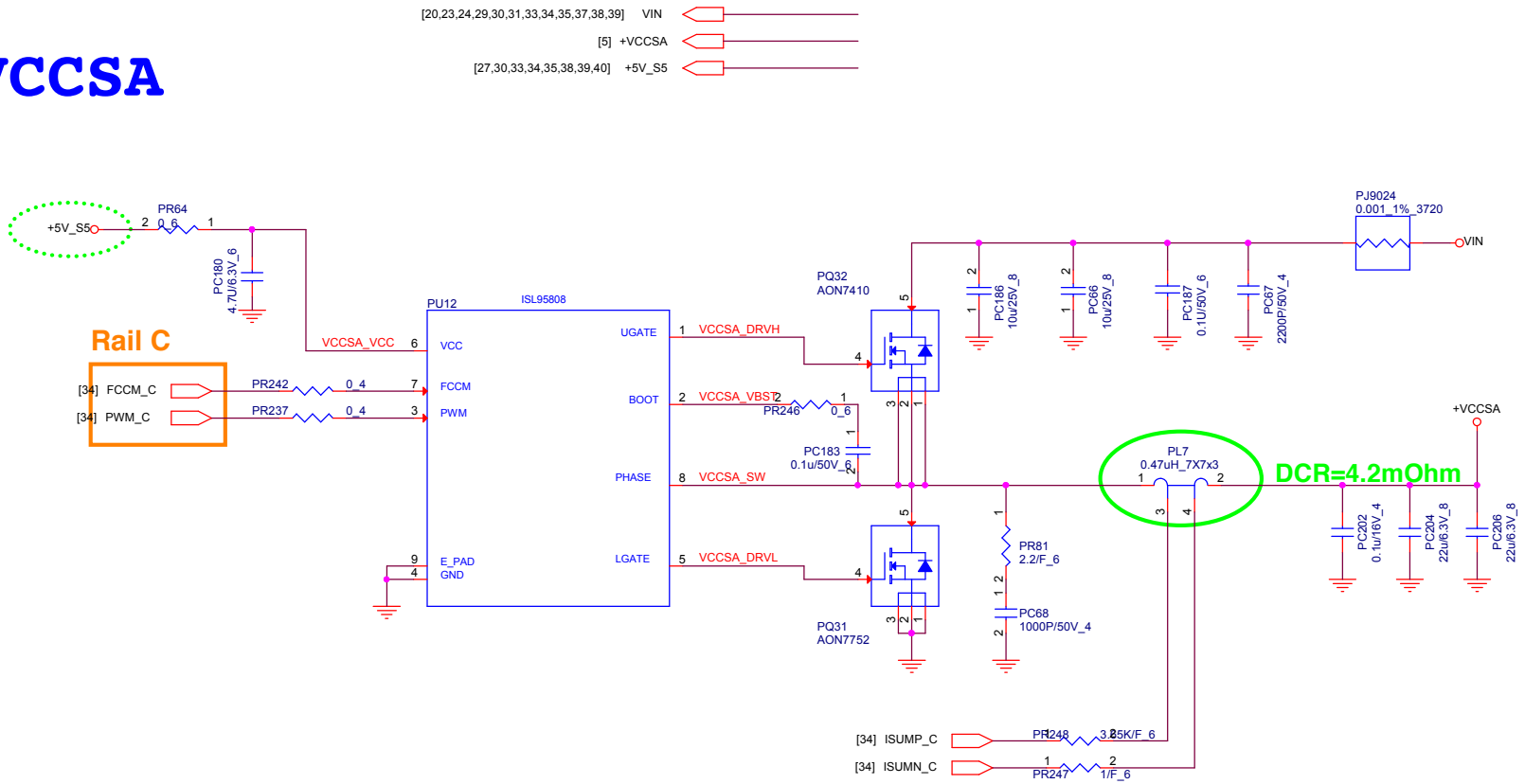
VCCGT



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	VCORE/VCCGT (ISL95808HRZ-T)	1A
Date: Thursday, June 22, 2017	Sheet 35 of 46	

VCCSA



VCCSA

Icc TDC PL2：5A

Icc Max：5A

OCP：6A

Fsw：800KHz

VCCSA L/L：

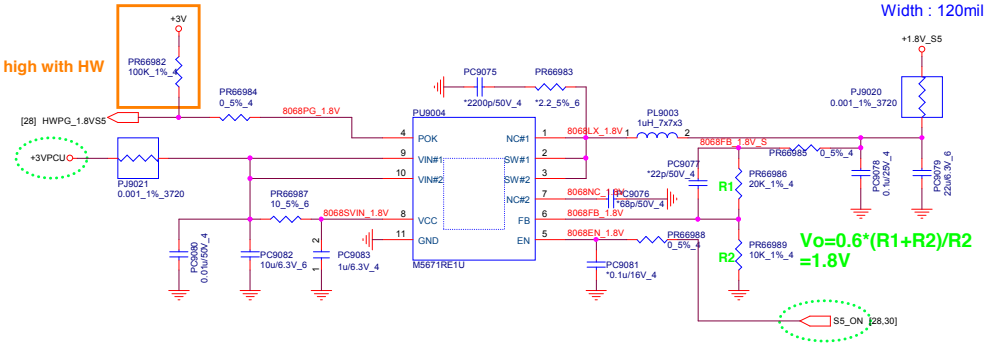
R_DC_LL：10.3mV/A

R_AC_LL：10.3mV/A

Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: VCCSA (ISL95808HRZ-T)	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 36 of 46	

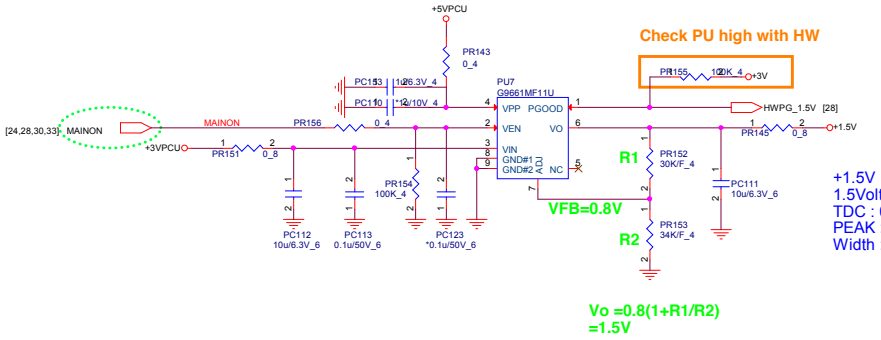
+1.8V_S5
1.8Volt +/- 5%
TDC : 2.61A
PEAK : 3.48A
Width : 120mil

Check PU high with HW



Vo=0.6*(R1+R2)/R2
=1.8V

Check PU high with HW



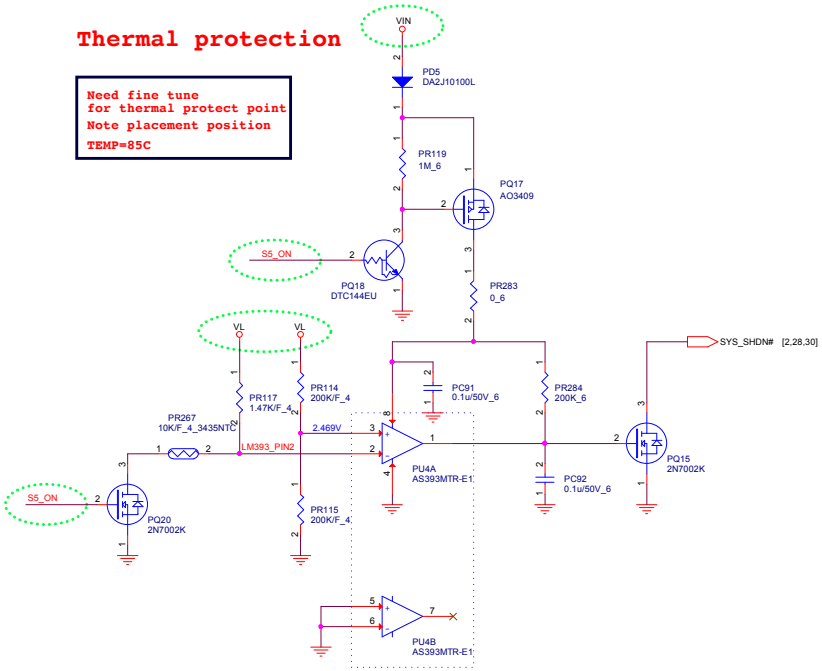
+1.5V
1.5Volt +/- 5%
TDC : 0.49A
PEAK : 0.66A
Width : 20mil

Vo =0.8(1+R1/R2)
=1.5V

Thermal protection

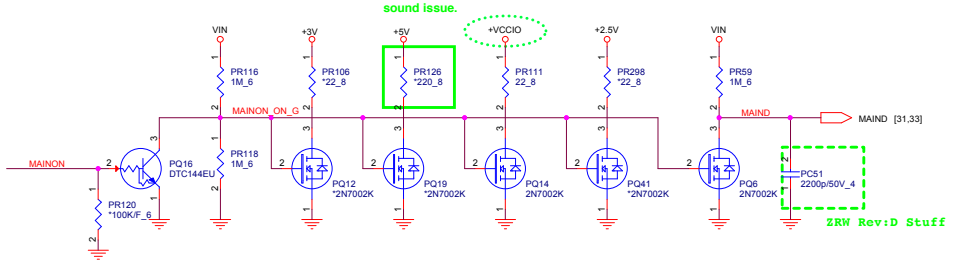
Need fine tune
for thermal protect point
Note placement position

TEMP=85C



For EC control thermal protection (output 3.3V)

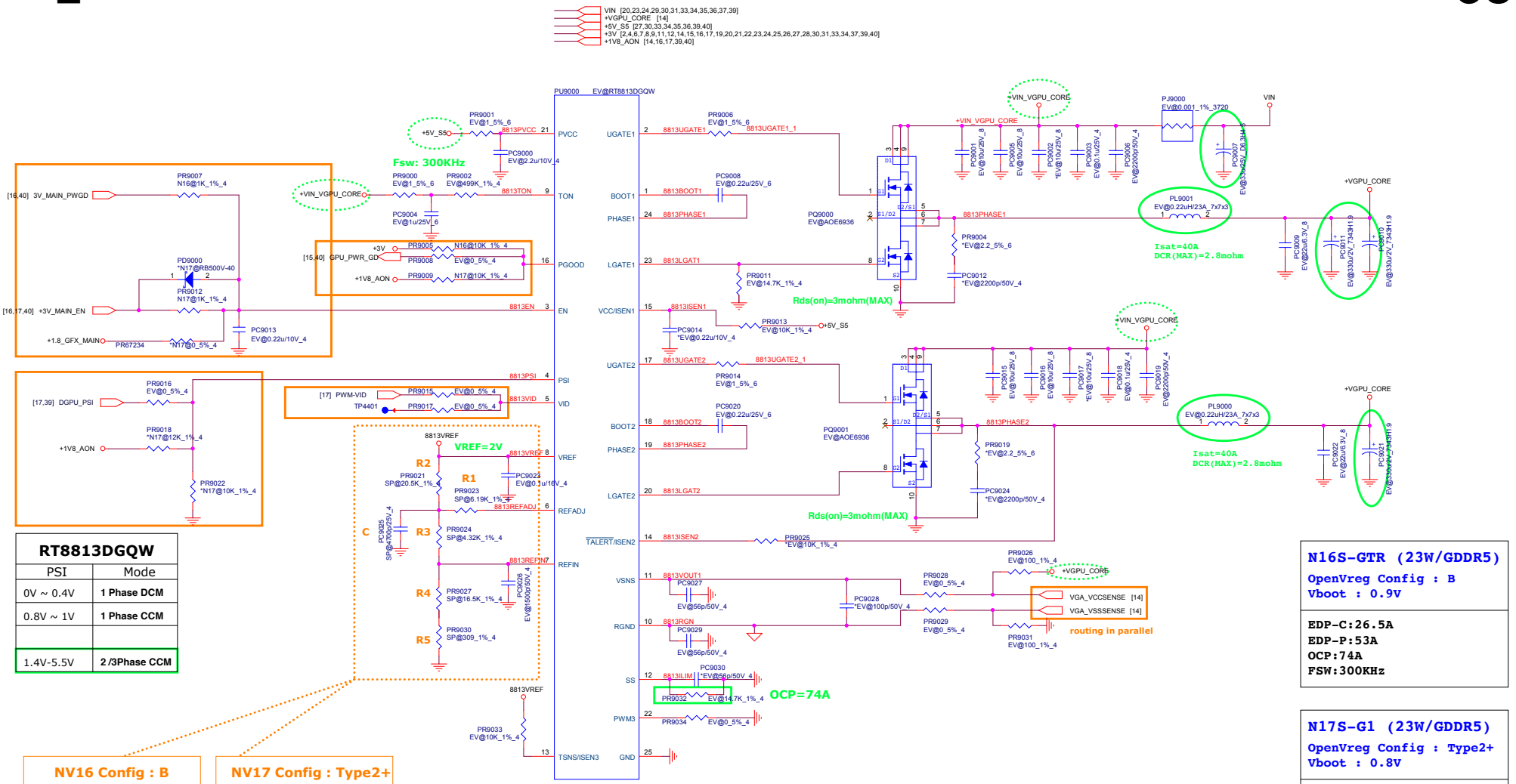
PR153 Change to
220 ohm for bo bo
sound issue.



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A
Date: Thursday, June 22, 2017	Sheet 37 of 46	

VGPU_CORE



RT8813DGQW	
PSI	Mode
0V ~ 0.4V	**1 Phase DCM**
0.8V ~ 1V	**1 Phase CCM**
1.4V-5.5V	**2 /3Phase CCM**

NV16 Config : B	
R1	20K
R2	20K
R3	2K
R4	18K
R5	0 ohm
C	2.7nF

NV17 Config : Type2+	
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	0.309K
C	4.7nF

N16S-GTR (23W/GDDR5)

OpenVreg Config : B
Vboot : 0.9V

EDP-C:26.5A
EDP-P:53A
OCP:74A
FSW:300KHz

N17S-G1 (23W/GDDR5)

OpenVreg Config : Type2+
Vboot : 0.8V

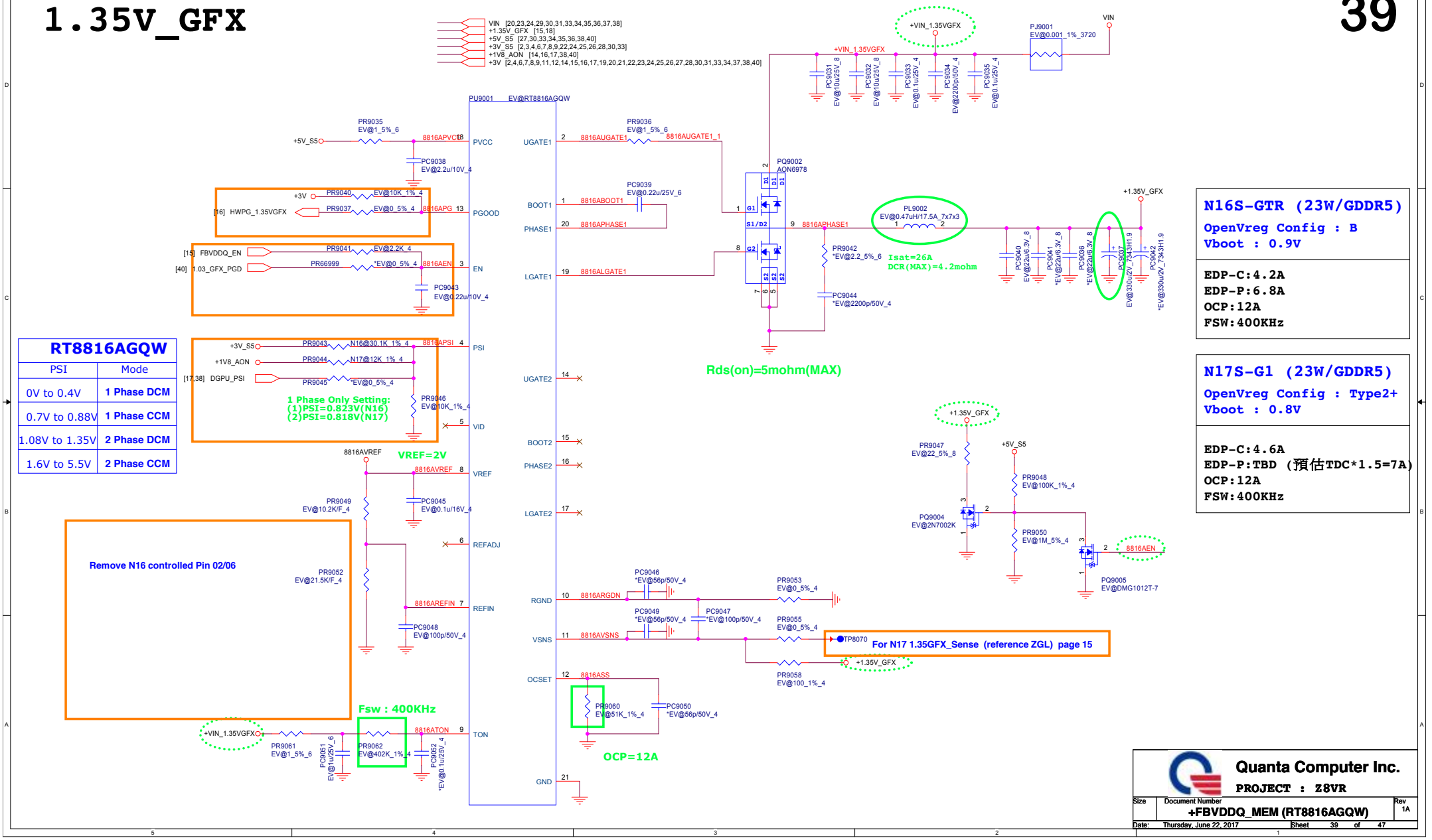
EDP-C:27.9A
EDP-P:62.2A
OCP:74A
FSW:300KHz

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+NVDD (RT8813DGQW)	1A

Date: Thursday, June 22, 2017 Sheet 38 of 47

1.35V_GFX



RT8816AGQW	
PSI	Mode
0V to 0.4V	1 Phase DCM
0.7V to 0.88V	1 Phase CCM
1.08V to 1.35V	2 Phase DCM
1.6V to 5.5V	2 Phase CCM

N16S-GTR (23W/GDDR5)

OpenVreg Config : B
Vboot : 0.9V

EDP-C:4.2A
EDP-P:6.8A
OCP:12A
FSW:400KHz

N17S-G1 (23W/GDDR5)

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:4.6A
EDP-P:TBD (預估TDC*1.5=7A)
OCP:12A
FSW:400KHz

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+FBVDDQ_MEM (RT8816AGQW)	1A
Date: Thursday, June 22, 2017	Sheet 39 of 47	

+1.8V_S5 [8,9,10,37]
+1.8_GFX_MAIN [14,15,16]
+1V8_AON [14,16,17,38,39]

+5VPCU [27,30,31,37]
+1.2VSUS [3,5,11,12,33]
+1.03_GFX [14,15,16]
+5V_S5 [27,30,33,34,35,36,38,39]
+3V [2,4,6,7,8,9,11,12,14,15,16,17,19,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39]

N16S-GTR
+3V_GFX TDC : 0.06A Width : 20mil

PR9084 For N17 use only

N17S-G1
+1.8V_MAIN TDC : 1.13A PEAK : 1.5A Width : 60mil

N17S-G1
+1.8V_AON TDC : 1.13A PEAK : 1.5A Width : 60mil

PJ9002 EV@AOZ1331DI

[4] DGPU_PWR_EN
[16,17,38] +3V_MAIN_EN

A2

N16S-GTR	N17S-G1
+1.05V TDC : 0.8A PEAK : 2.1A Width : 80mil	+1V TDC : 0.9A PEAK : 1.1A Width : 40mil

Check N16 Power Good

Check PU high with HW

PU9003 EV@G9336ADJTP1U

N16S:Vo=(1+R1/R2)*0.5=1.03V
N17S:Vo=(1+R1/R2)*0.5=1.03V

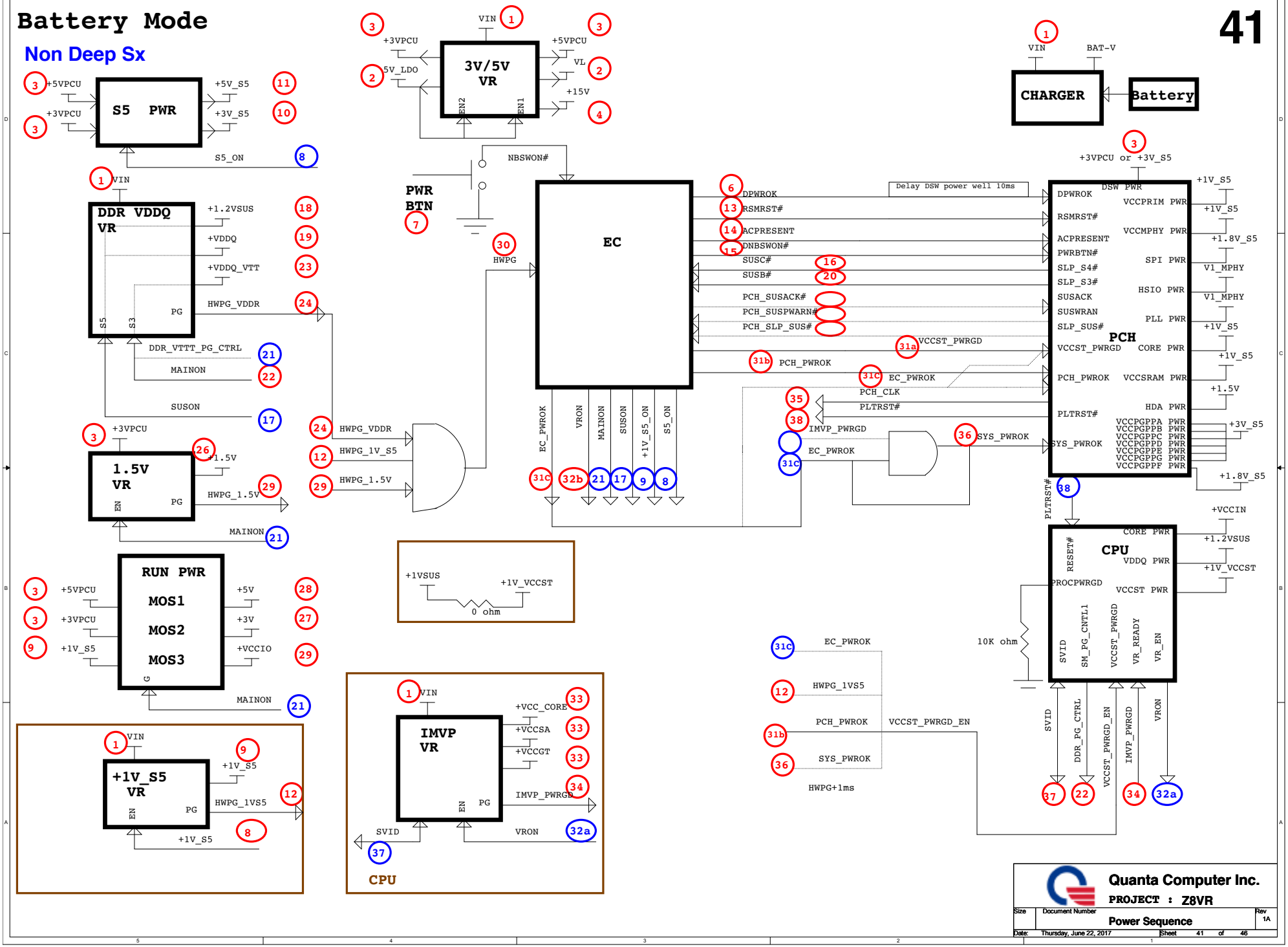
	R1	R2
N16S	133 ohm	124 ohm
N17S	133 ohm	124 ohm

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+1.8V_AON (AOZ1331DI)	1A
Date: Thursday, June 22, 2017	Sheet 40 of 47	

Battery Mode

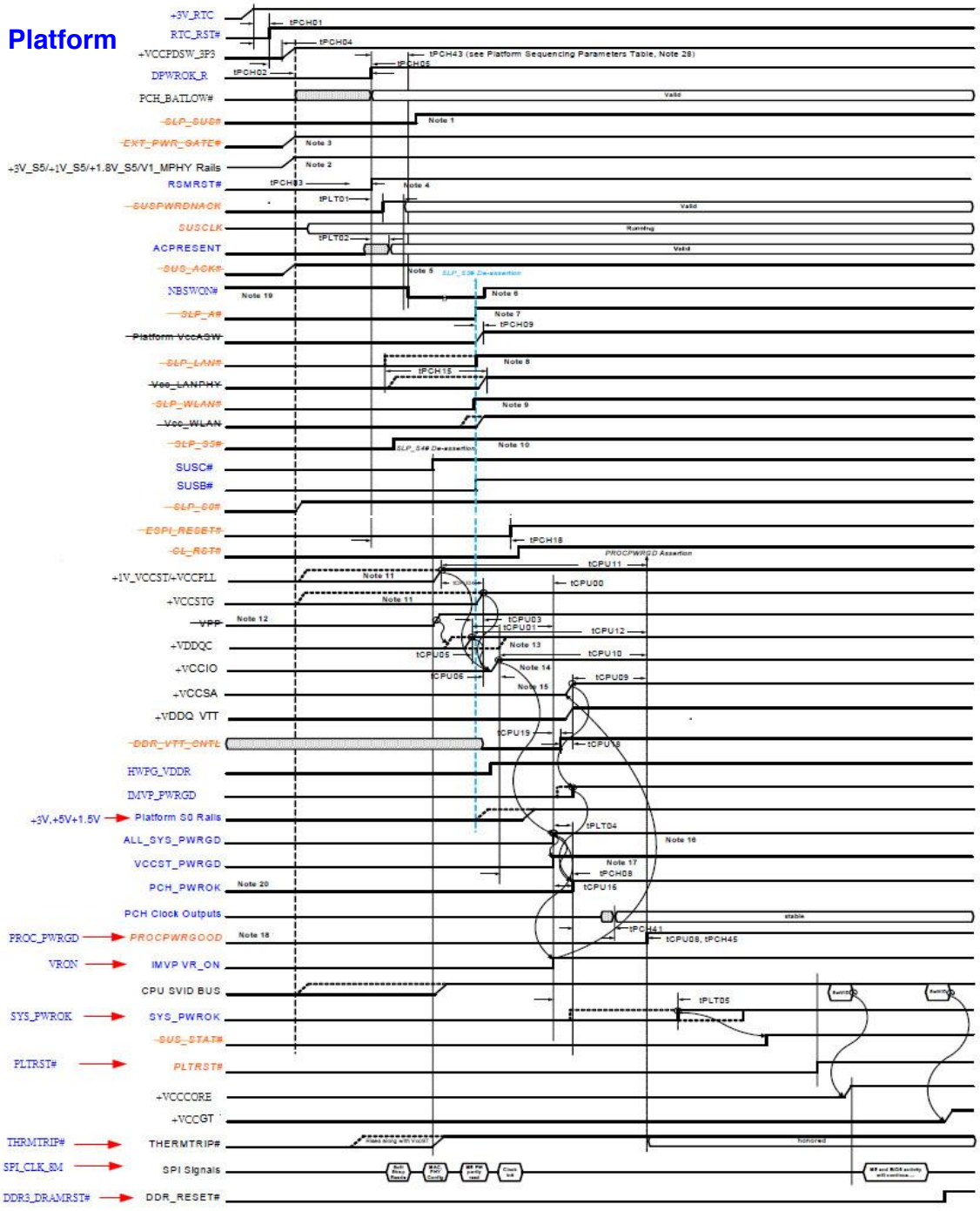
Non Deep Sx



Quanta Computer Inc.
PROJECT : Z8VR

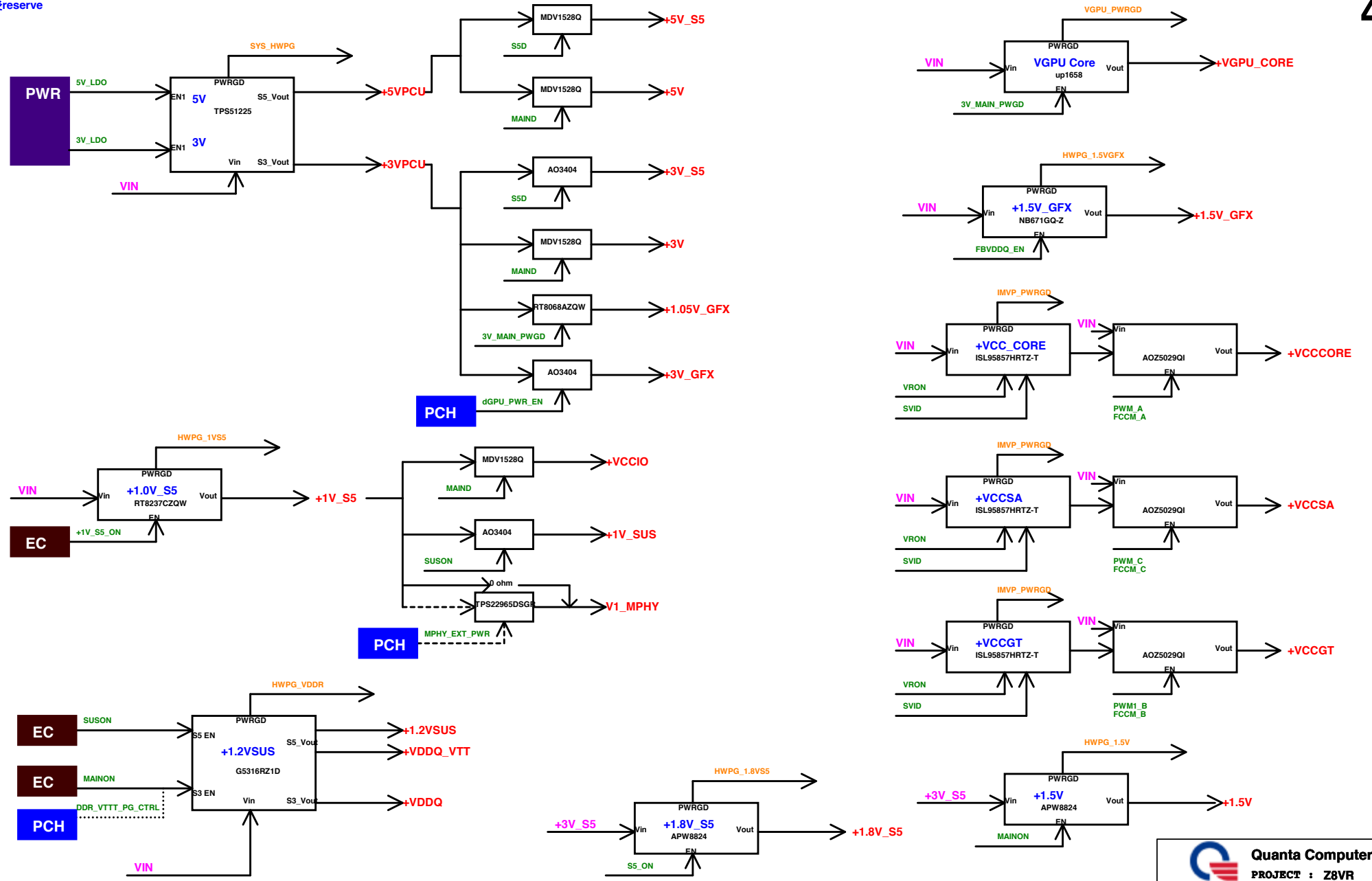
Size	Document Number	Rev
	Power Sequence	1A
Date: Thursday, June 22, 2017	Sheet 41 of 46	

Skylake U Non-Deep Sx Platform Power on sequence



Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: Power on Sequence	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 42 of 46	

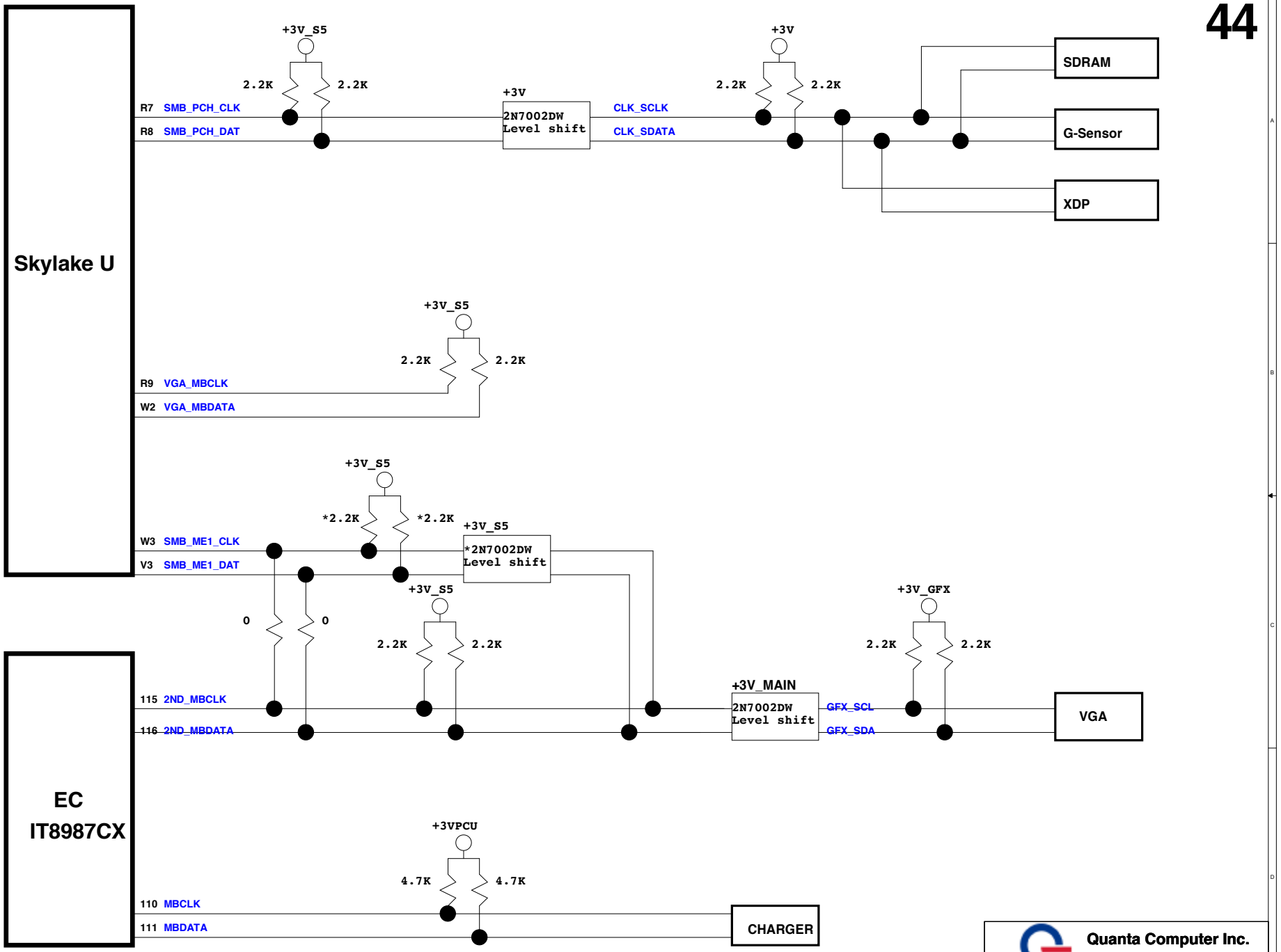
實線表defult
虛線表reserve



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	SKL PCH PWR CONTROL	1A

Date: Thursday, June 22, 2017 Sheet 43 of 46



Quanta Computer Inc.

PROJECT : Z8VR

Size	Document Number	Rev
	SMBUS Block Diagram	1A

Date: Thursday, June 22, 2017 Sheet 44 of 46

Model	Date	CHANGE LIST
Z8VR REV:A	03/14	First release
Z8VR REV:B	03/16	Change SW3 Footprint to Sw-ds-a40e-4p-smt for SMT issue Remove C460/C461 for 16G memory module can't power on issue Change SPI ROM GGD 16M P/N to GD25B127DSIGR, original PN is EOL
	03/28	according to Intel DG to unstuff R8748,R8749 and R417.
	04/28	label PR23 as sp@(UMA and DIS value are different)
Z8VR REV:C	05/15	Change 0 Ohm to shortpad add EV@ for PQ9002 value that no need to stuff on UMA SKU
	06/01	Change for Power Noise issue 1.Add PC181 with 33uF in +VIN_VCCGT net 2.Change PC210,PC216 from 22 uF to 47 uF 3.Change PC208,PC212 from 22uF to no stuff

Quanta Computer Inc. PROJECT : Z8VR Size: Document Number: Change list; Rev: 1A Date: Thursday, June 22, 2017; Sheet 45 of 46	DOC NO.	PROJECT MODEL :	Z8VR	APPROVED BY:	DATE:
		PART NUMBER:		DRAWING BY:	REVISON:

Model	Date	CHANGE LIST

Quanta Computer Inc. PROJECT : Z8VR	DOC NO.	PROJECT MODEL :	Z8VR	APPROVED BY:	DATE:
Size: Document Number: Change list Rev: 1A		PART NUMBER:		DRAWING BY:	REVISON:
Date: Thursday, June 22, 2017 Sheet 46 of 46					