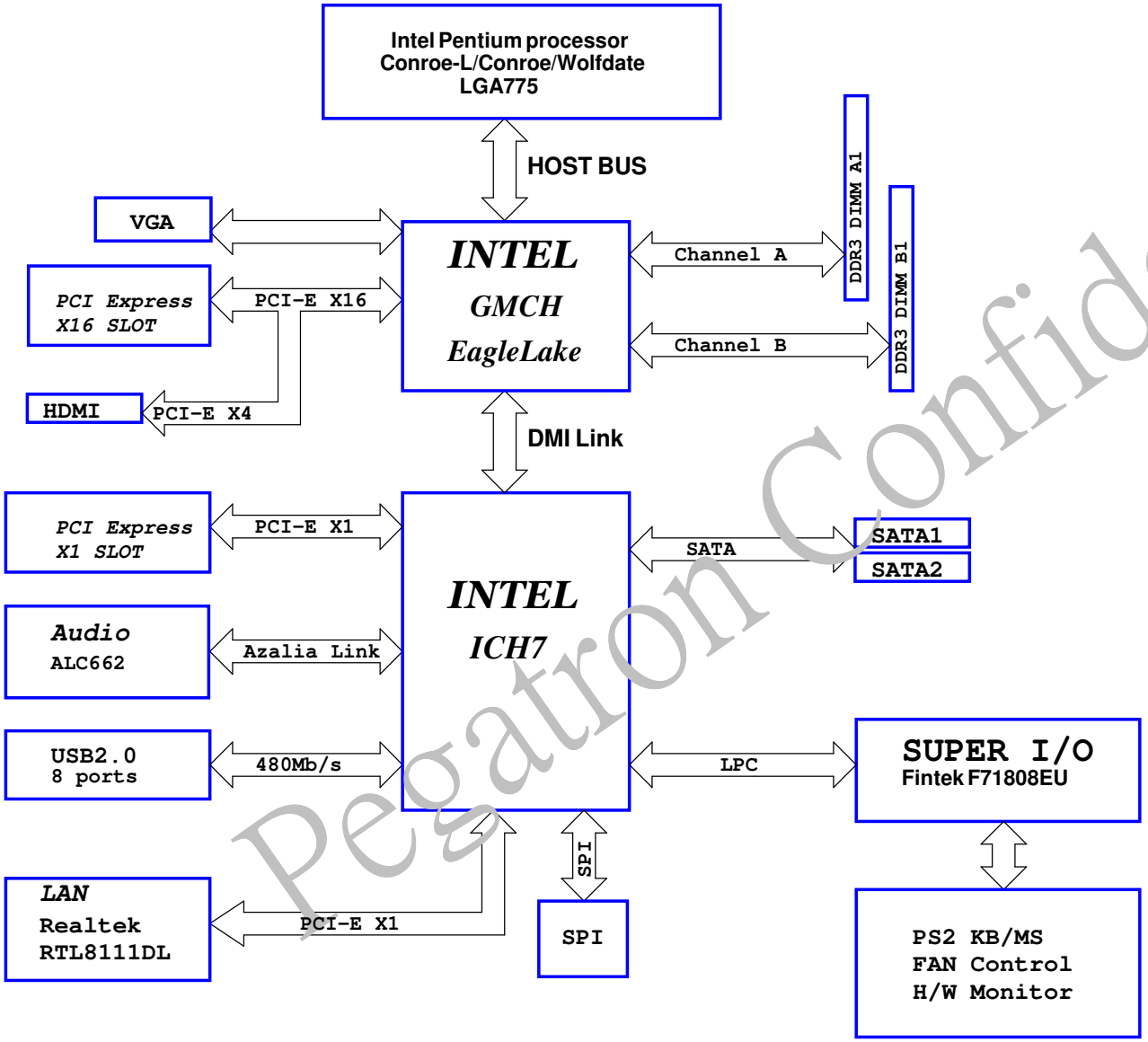
IPX41-D3

Revision:1.02



53	53.+5V_DUAL
54	54.+3P3V_PCIE&+3P3V_LAN
55	
56	

<Variant Name>

PEGATRON Title : Block Diagram

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 1 of 54

ECN Control Table

ECN No.	DATE	Subject	Schematics Revision	BOM Part Number	PCBA Revision	PCB Revision

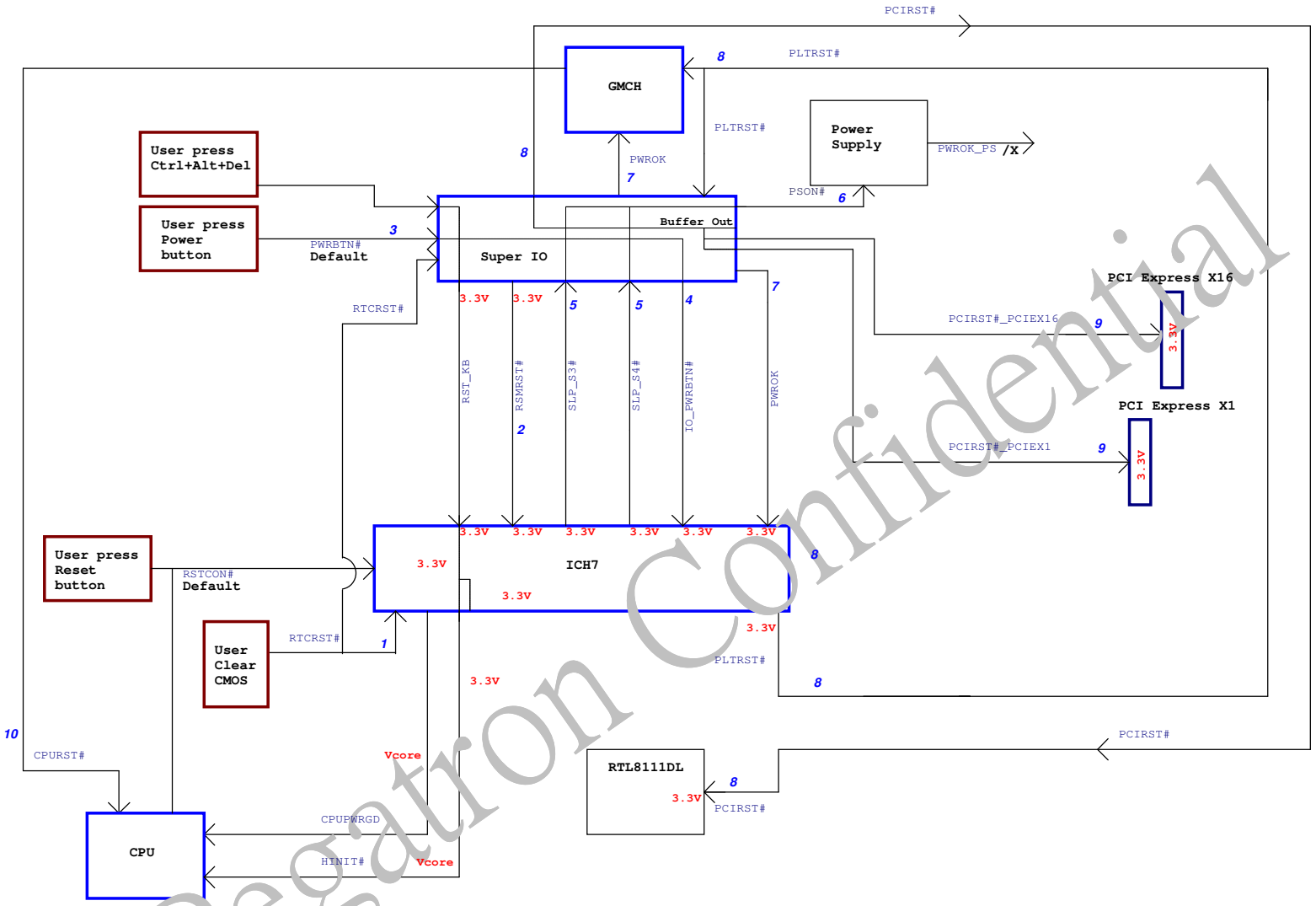
<Variant Name>

PEGATRON Title : ECN

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 2 of 54



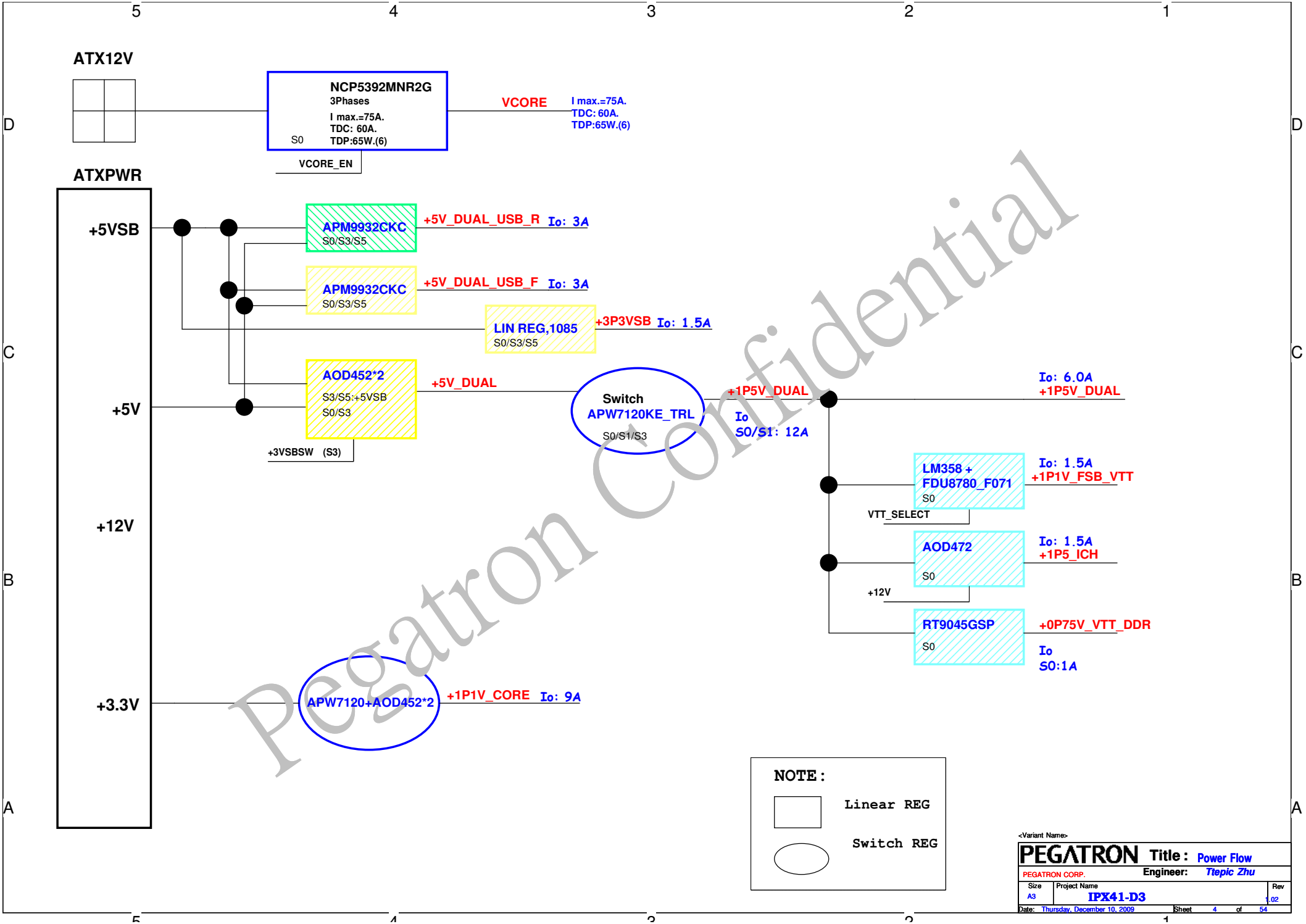
<Variant Name>

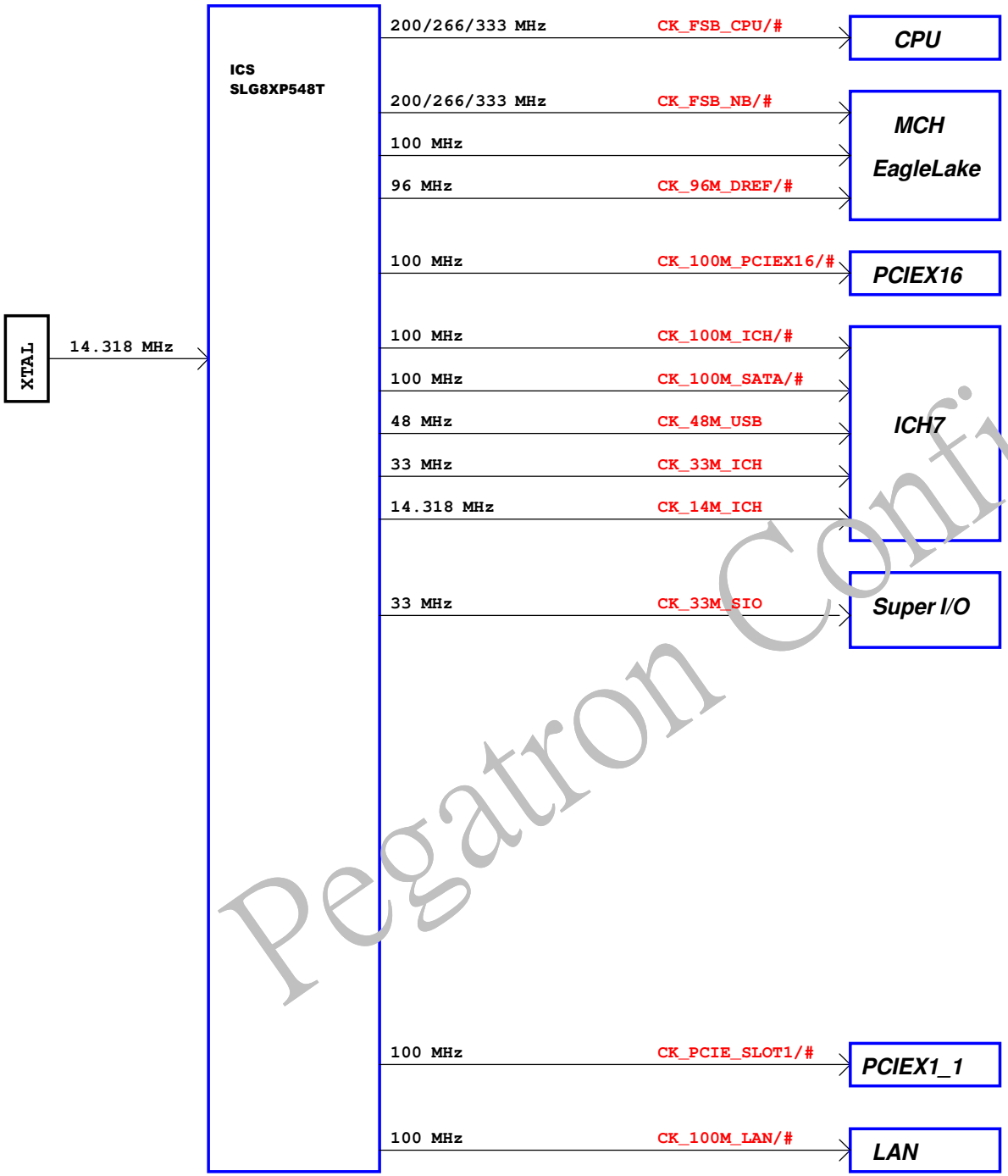
PEGATRON Title : Power Sequence

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 3 of 54





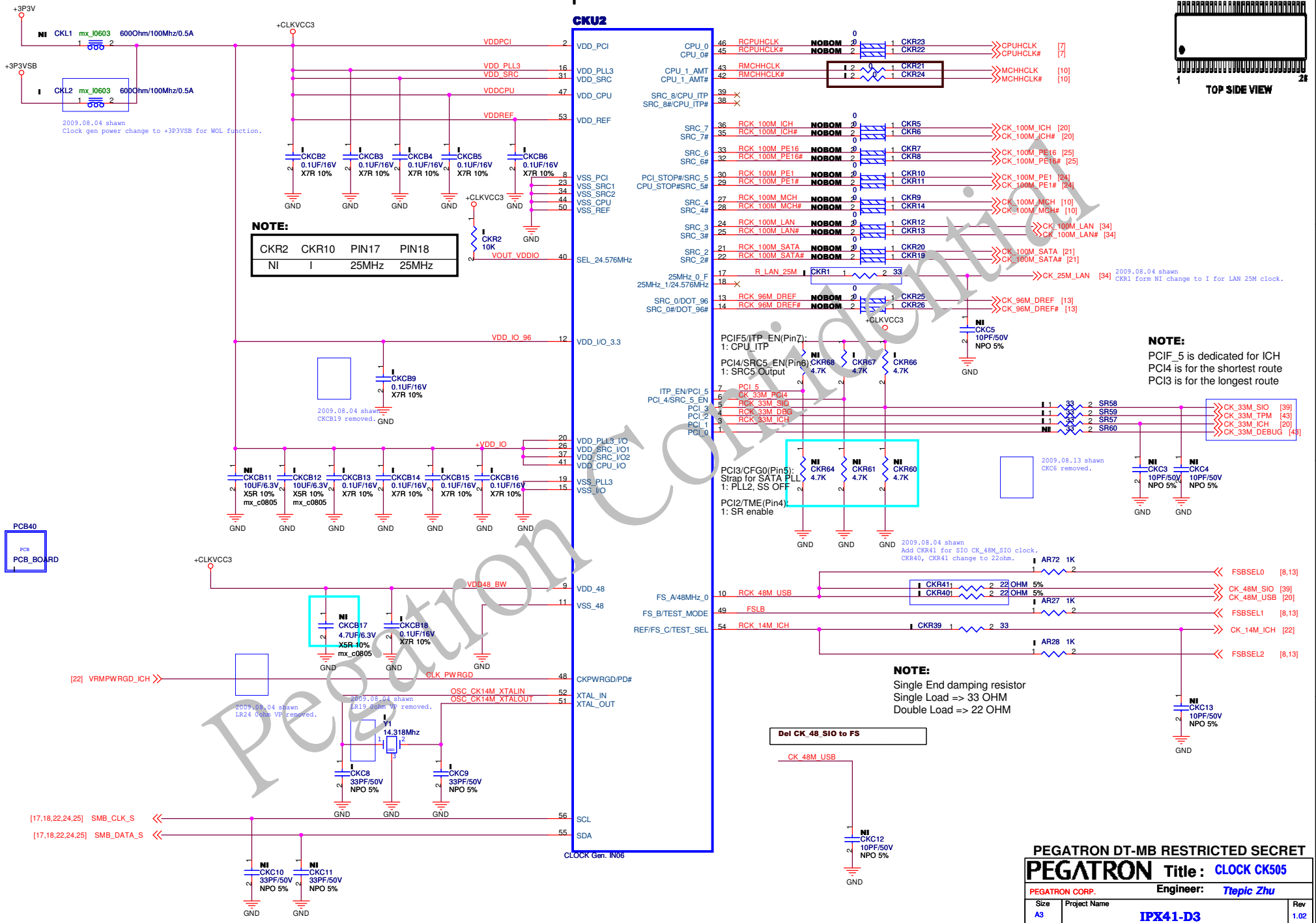
<Variant Name>

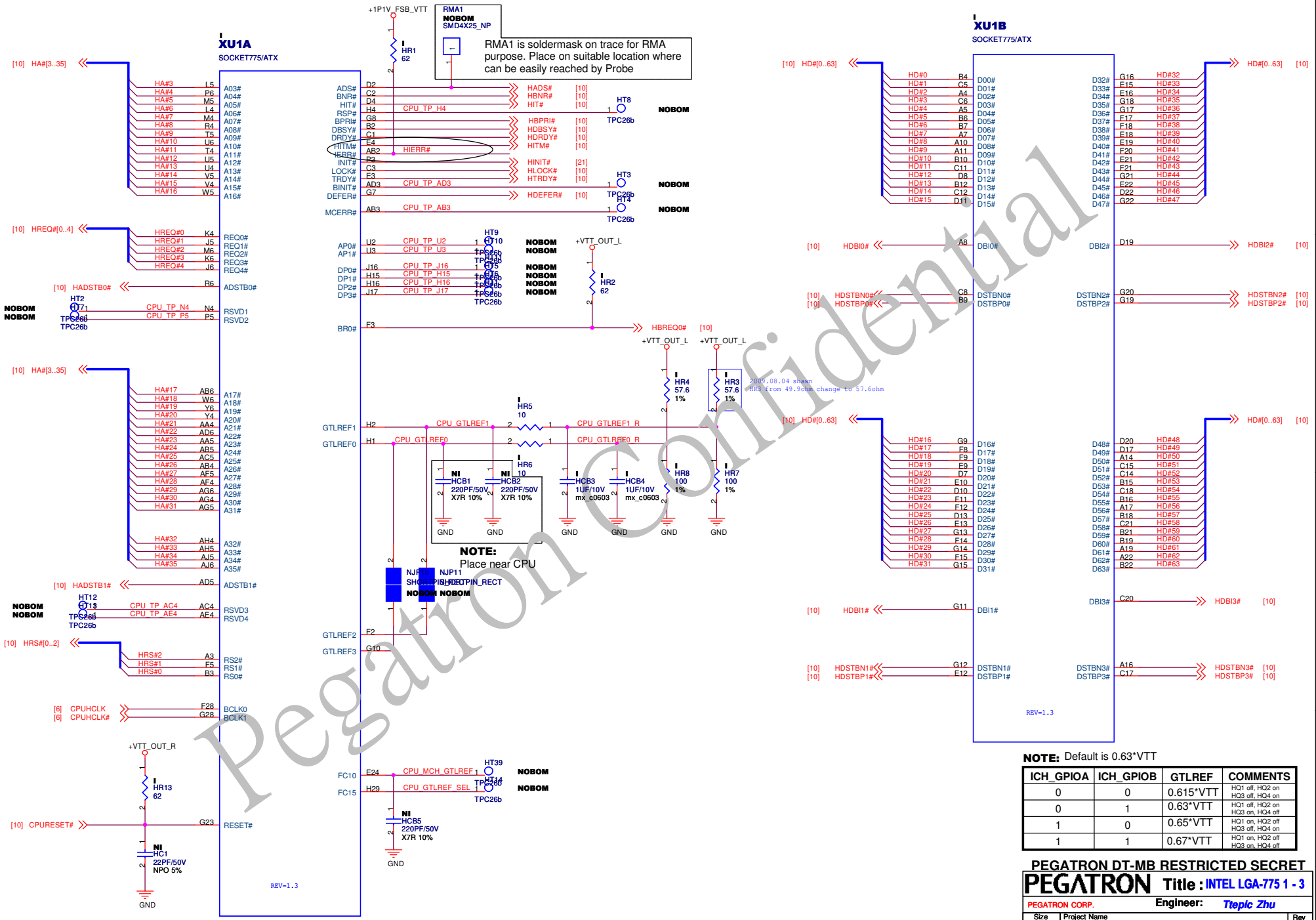
PEGATRON Title : Clock Distribution

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 5 of 54





PLACE NEAR SB

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO CPU SOCKET. THE TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12 MIL.

Note:	If NOT support C3/ C4, these 4 signals can be NC with a PU resistor
PM_SLP# (CPU_SLP)	Install HR24 for pin: L2
DPSLP#	Install HR22 for pin: P1
CPU_PSI	Install HR36 for pin: Y3
DPRSTP#	Install HR37 for pin: T2

NOTE:
FSB_VTT Net Name changed

NOTE:
The VCCIO PLL Filter Circuit is no longer needed since Conroe CPU

BOOTSELECT:
Install PD resistor to prevent PSC SMF CDM PSI CPU from booting

THERMALTRIP# NEED A PULL UP RESISTOR NEAR SB

2009.10.22 shawn
+CPU_VCCPLL floating, change power net name to +1P5V_ICH.

2009.08.14 shawn
HR57, HR58, HR59 from 470 5% change to 470 1%.

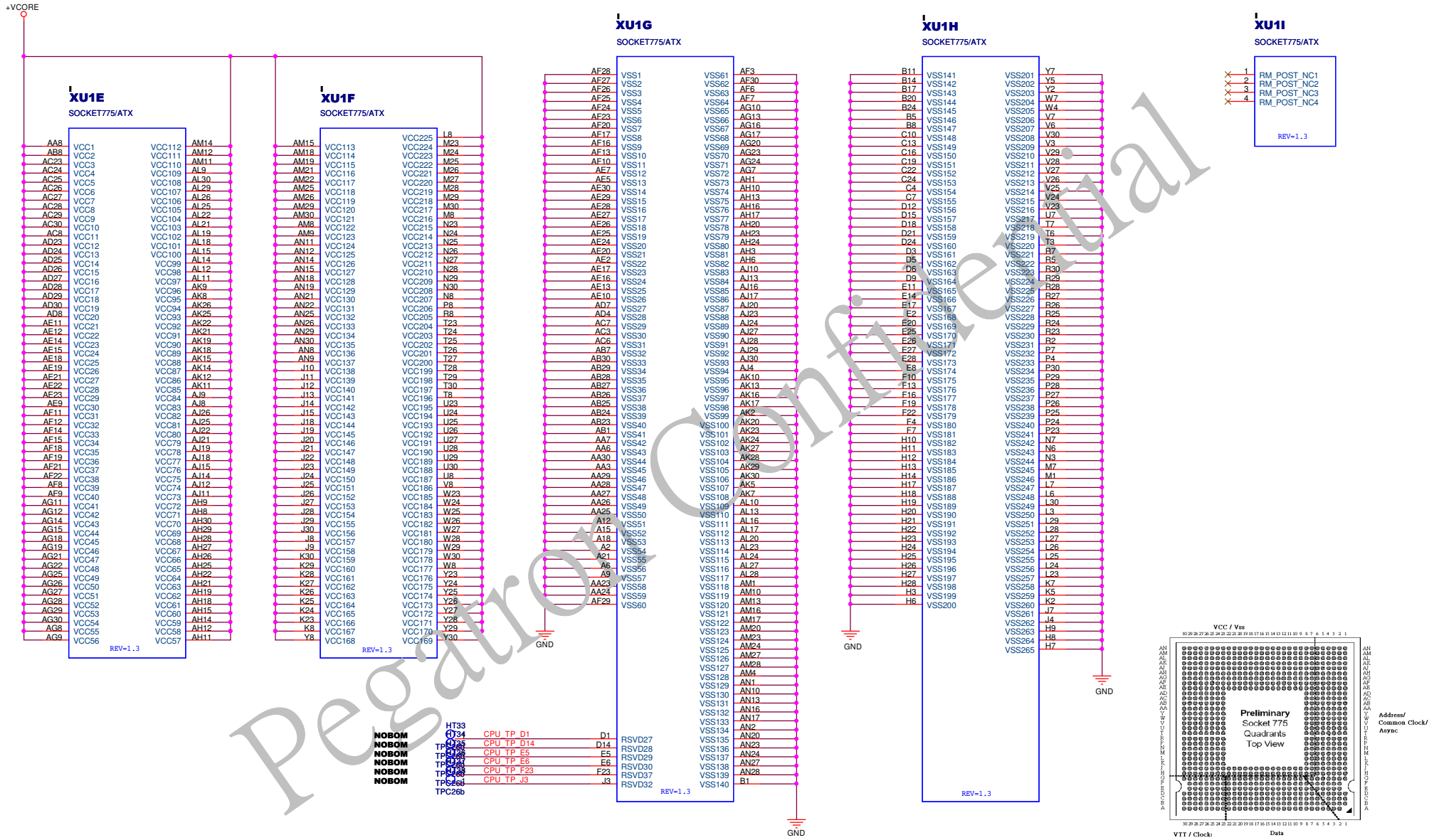
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL LGA-775 2 - 3

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 8 of 54



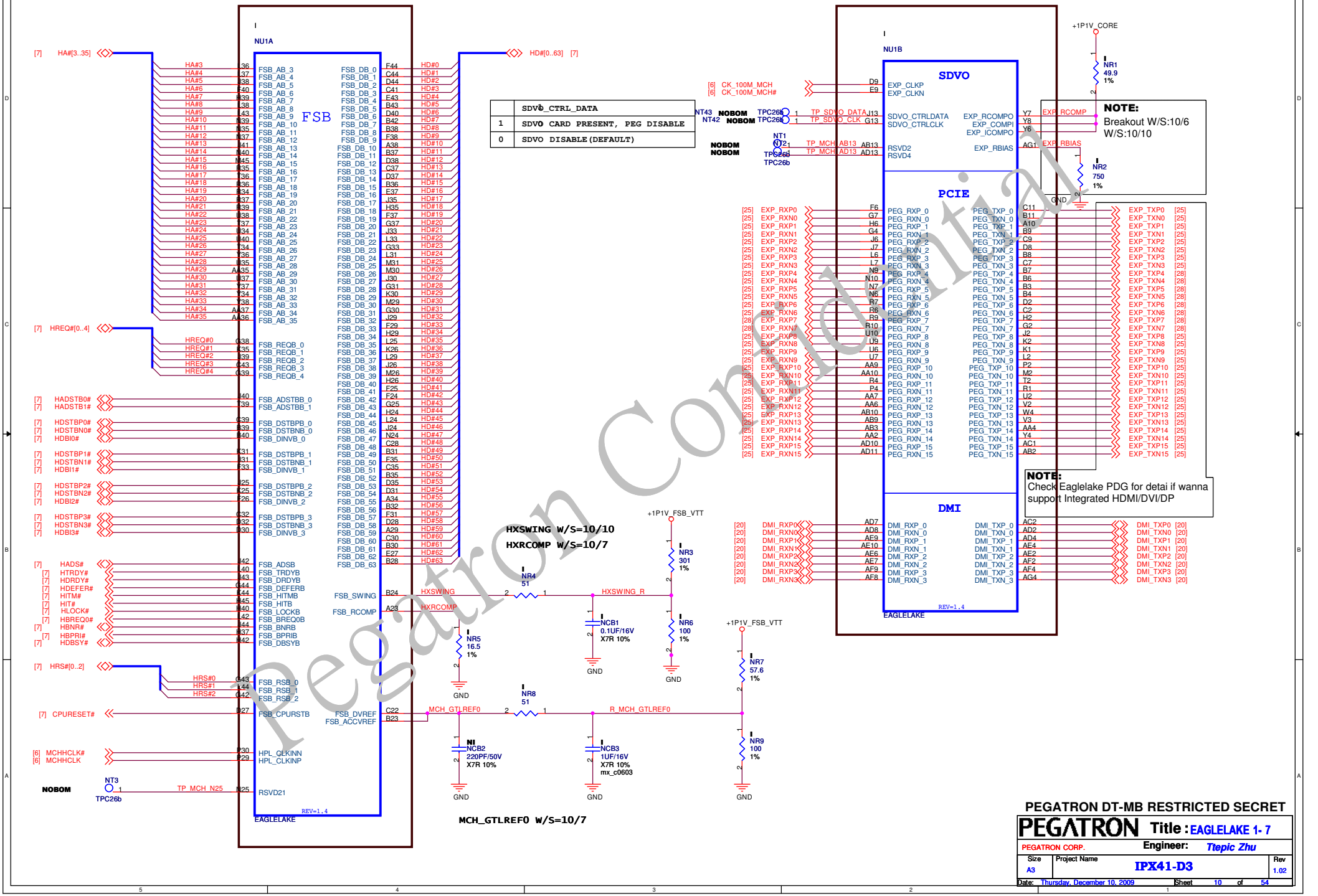
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL LGA-775 3 - 3

PEGATRON CORP. Engineer: Ttepic Zhu

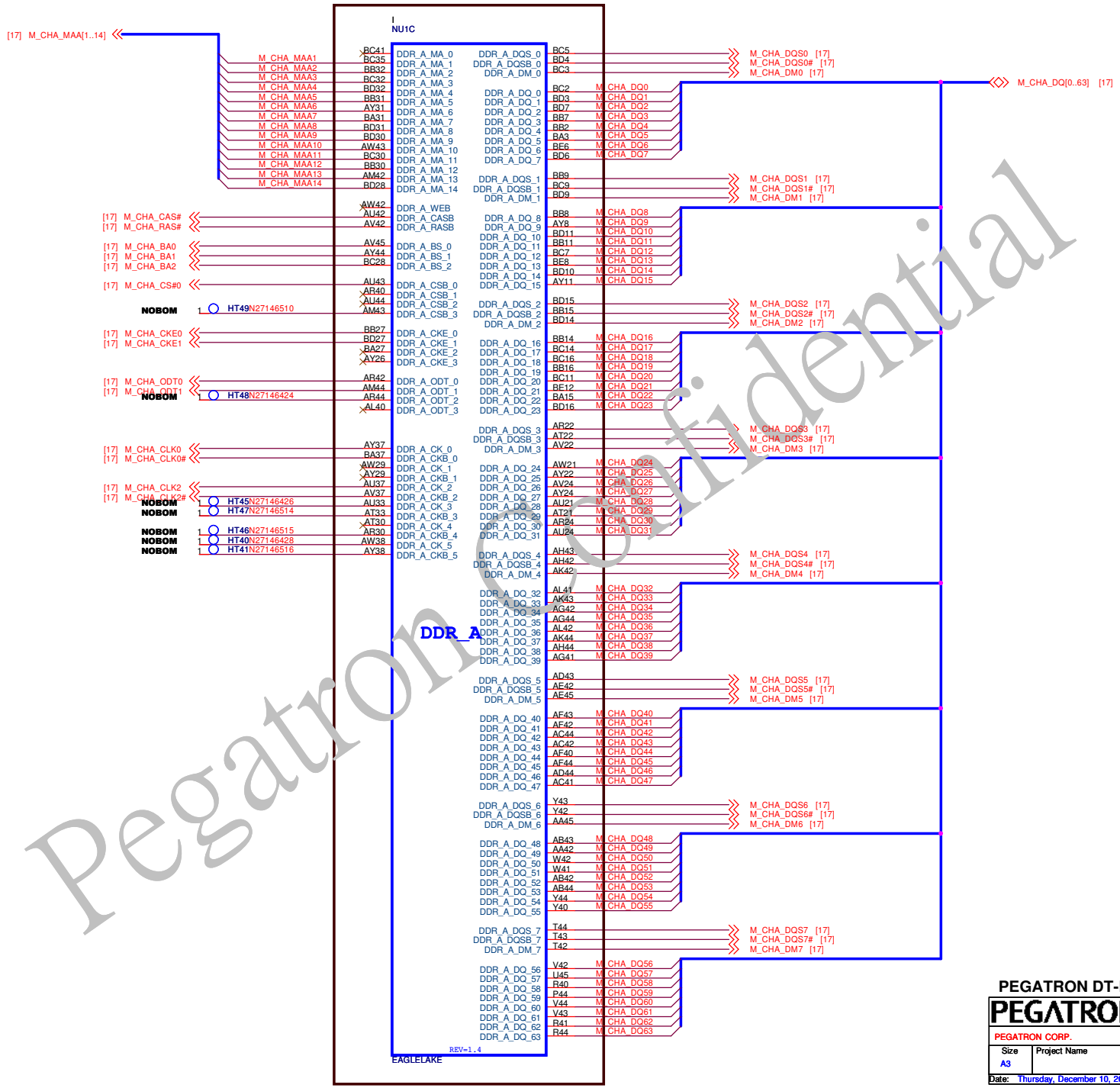
Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 9 of 54



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : EAGLELAKE 1- 7		
PEGATRON CORP.	Engineer: Ttepic Zhu		
Size: A3	Project Name: IPX41-D3		Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 10 of 54		



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : EAGELLAKE 2 - 7		
PEGATRON CORP.	Engineer: Titepic Zhu		
Size: A3	Project Name: IPX41-D3		Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 11 of 54		

Add DIMM B to FS

NU1D

[18] M_CHB_MAA[0..14]

M_CHB_MAA0 BD24 DDR_B_MA_0
M_CHB_MAA1 BB23 DDR_B_MA_1
M_CHB_MAA2 BB24 DDR_B_MA_2
M_CHB_MAA3 BD23 DDR_B_MA_3
M_CHB_MAA4 BB22 DDR_B_MA_4
M_CHB_MAA5 BD22 DDR_B_MA_5
M_CHB_MAA6 BC22 DDR_B_MA_6
M_CHB_MAA7 BC20 DDR_B_MA_7
M_CHB_MAA8 BB20 DDR_B_MA_8
M_CHB_MAA9 BD20 DDR_B_MA_9
M_CHB_MAA10 BC26 DDR_B_MA_10
M_CHB_MAA11 BD19 DDR_B_MA_11
M_CHB_MAA12 BB19 DDR_B_MA_12
M_CHB_MAA13 BE38 DDR_B_MA_13
M_CHB_MAA14 BA19 DDR_B_MA_14

[18] M_CHB_WE# BD36 DDR_B_WEB
[18] M_CHB_CAS# BC37 DDR_B_CASB
[18] M_CHB_RAS# BD35 DDR_B_RASB

[18] M_CHB_BA0 BD26 DDR_B_BS_0
[18] M_CHB_BA1 BB26 DDR_B_BS_1
[18] M_CHB_BA2 BD18 DDR_B_BS_2

[18] M_CHB_CS#0 BB35 DDR_B_CSB_0
[18] M_CHB_CS#1 BD39 DDR_B_CSB_1
BB37 DDR_B_CSB_2
BD40 DDR_B_CSB_3
NOBOM 1 HT53 N27146430

[18] M_CHB_CKE0 BC18 DDR_B_CKE_0
[18] M_CHB_CKE1 AY20 DDR_B_CKE_1
NOBOM 1 HT55 N27146431 BE17 DDR_B_CKE_2
NOBOM 1 HT58 N27146432 BB18 DDR_B_CKE_3

[18] M_CHB_ODT0 BD37 DDR_B_ODT_0
[18] M_CHB_ODT1 BC39 DDR_B_ODT_1
BB38 DDR_B_ODT_2
NOBOM 1 HT61 N27146434 BD42 DDR_B_ODT_3

[18] M_CHB_CLK0 AY33 DDR_B_CK_0
[18] M_CHB_CLK0# AW33 DDR_B_CKB_0
NOBOM 1 HT50 N27146435 AV31 DDR_B_CK_1
NOBOM 1 HT54 N27146436 AW31 DDR_B_CKB_1
[18] M_CHB_CLK2 AW35 DDR_B_CK_2
[18] M_CHB_CLK2# AY35 DDR_B_CKB_2
NOBOM 1 HT57 N27146437 AT31 DDR_B_CK_3
NOBOM 1 HT60 N27146438 AU31 DDR_B_CKB_3
NOBOM 1 HT62 N27146439 AP31 DDR_B_CK_4
NOBOM 1 HT51 N27146440 AP30 DDR_B_CKB_4
AW37 DDR_B_CK_5
NOBOM 1 HT59 N27146442 AV35 DDR_B_CKB_5

[17] M_CHA_CS#1 AR43 DDR3_A_CSB1
[17] M_CHA_MAA0 BB40 DDR3_A_MA0
[17] M_CHA_WE# AT44 DDR3_A_WEB
AV40 DDR3_B_ODT3
[19] DDR3_DRAM_PWROK AR6 DDR3_DRAM_PWROK
[17,18] DDR3_DRAMRST# BC24 DDR3_DRAMRSTB

AN29 RSVD7
NOBOM 1 HT52 N27146445 AN30 RSVD8
NOBOM 1 HT56 N27146446 AJ33 RSVD5
AK33 RSVD6

DDR_VREF BB44 DDR_VREF

MCH_DDR_RPU BA43 DDR_RPU
MCH_DDR_RPD AY42 DDR_RPD

MCH_DDR_SPU BC44 DDR_SPU
MCH_DDR_SPD BC43 DDR_SPD

DDR_B

REV=1.4

EAGLELAKE

M_CHB_DQS0 [18]
M_CHB_DQS0# [18]
M_CHB_DM0 [18]
M_CHB_DQ[0..63] [18]

AW8 DDR_B_DQS_0
AW9 DDR_B_DQSB_0
AY6 DDR_B_DM_0
AV7 M_CHB_DQ0 DDR_B_DQ_0
AW4 M_CHB_DQ1 DDR_B_DQ_1
BA9 M_CHB_DQ2 DDR_B_DQ_2
AU11 M_CHB_DQ3 DDR_B_DQ_3
AU7 M_CHB_DQ4 DDR_B_DQ_4
AU8 M_CHB_DQ5 DDR_B_DQ_5
AW7 M_CHB_DQ6 DDR_B_DQ_6
AY9 M_CHB_DQ7 DDR_B_DQ_7

M_CHB_DQS1 [18]
M_CHB_DQS1# [18]
M_CHB_DM1 [18]
AT15 DDR_B_DQS_1
AU15 DDR_B_DQSB_1
AR15 DDR_B_DM_1
AY13 M_CHB_DQ8 DDR_B_DQ_8
AP15 M_CHB_DQ9 DDR_B_DQ_9
AW15 M_CHB_DQ10 DDR_B_DQ_10
AT16 M_CHB_DQ11 DDR_B_DQ_11
AU13 M_CHB_DQ12 DDR_B_DQ_12
AW13 M_CHB_DQ13 DDR_B_DQ_13
AP16 M_CHB_DQ14 DDR_B_DQ_14
AU16 M_CHB_DQ15 DDR_B_DQ_15

M_CHB_DQS2 [18]
M_CHB_DQS2# [18]
M_CHB_DM2 [18]
AR20 DDR_B_DQS_2
AR17 DDR_B_DQSB_2
AU17 DDR_B_DM_2
AY17 M_CHB_DQ16 DDR_B_DQ_16
AV17 M_CHB_DQ17 DDR_B_DQ_17
AR21 M_CHB_DQ18 DDR_B_DQ_18
AV20 M_CHB_DQ19 DDR_B_DQ_19
AP17 M_CHB_DQ20 DDR_B_DQ_20
AW16 M_CHB_DQ21 DDR_B_DQ_21
AT20 M_CHB_DQ22 DDR_B_DQ_22
AN20 M_CHB_DQ23 DDR_B_DQ_23

M_CHB_DQS3 [18]
M_CHB_DQS3# [18]
M_CHB_DM3 [18]
AU26 DDR_B_DQS_3
AT26 DDR_B_DQSB_3
AV25 DDR_B_DM_3
AT25 M_CHB_DQ24 DDR_B_DQ_24
AV26 M_CHB_DQ25 DDR_B_DQ_25
AU29 M_CHB_DQ26 DDR_B_DQ_26
AV29 M_CHB_DQ27 DDR_B_DQ_27
AW25 M_CHB_DQ28 DDR_B_DQ_28
AR25 M_CHB_DQ29 DDR_B_DQ_29
AP26 M_CHB_DQ30 DDR_B_DQ_30
AR29 M_CHB_DQ31 DDR_B_DQ_31

M_CHB_DQS4 [18]
M_CHB_DQS4# [18]
M_CHB_DM4 [18]
AR38 DDR_B_DQS_4
AR37 DDR_B_DQSB_4
AU39 DDR_B_DM_4
AR36 M_CHB_DQ32 DDR_B_DQ_32
AU38 M_CHB_DQ33 DDR_B_DQ_33
AN35 M_CHB_DQ34 DDR_B_DQ_34
AN37 M_CHB_DQ35 DDR_B_DQ_35
AV39 M_CHB_DQ36 DDR_B_DQ_36
AW39 M_CHB_DQ37 DDR_B_DQ_37
AU40 M_CHB_DQ38 DDR_B_DQ_38
AU41 M_CHB_DQ39 DDR_B_DQ_39

M_CHB_DQS5 [18]
M_CHB_DQS5# [18]
M_CHB_DM5 [18]
AK34 DDR_B_DQS_5
AL34 DDR_B_DQSB_5
AL37 DDR_B_DM_5
AL35 M_CHB_DQ40 DDR_B_DQ_40
AL36 M_CHB_DQ41 DDR_B_DQ_41
AK36 M_CHB_DQ42 DDR_B_DQ_42
AJ34 M_CHB_DQ43 DDR_B_DQ_43
AN39 M_CHB_DQ44 DDR_B_DQ_44
AN40 M_CHB_DQ45 DDR_B_DQ_45
AK37 M_CHB_DQ46 DDR_B_DQ_46
AL39 M_CHB_DQ47 DDR_B_DQ_47

M_CHB_DQS6 [18]
M_CHB_DQS6# [18]
M_CHB_DM6 [18]
AF37 DDR_B_DQS_6
AF36 DDR_B_DQSB_6
AJ35 DDR_B_DM_6
AJ38 M_CHB_DQ48 DDR_B_DQ_48
AJ37 M_CHB_DQ49 DDR_B_DQ_49
AF38 M_CHB_DQ50 DDR_B_DQ_50
AE37 M_CHB_DQ51 DDR_B_DQ_51
AK40 M_CHB_DQ52 DDR_B_DQ_52
AJ40 M_CHB_DQ53 DDR_B_DQ_53
AF34 M_CHB_DQ54 DDR_B_DQ_54
AE35 M_CHB_DQ55 DDR_B_DQ_55

M_CHB_DQS7 [18]
M_CHB_DQS7# [18]
M_CHB_DM7 [18]
AB35 DDR_B_DQS_7
AD35 DDR_B_DQSB_7
AD37 DDR_B_DM_7
AD40 M_CHB_DQ56 DDR_B_DQ_56
AD38 M_CHB_DQ57 DDR_B_DQ_57
AB40 M_CHB_DQ58 DDR_B_DQ_58
AA39 M_CHB_DQ59 DDR_B_DQ_59
AE36 M_CHB_DQ60 DDR_B_DQ_60
AE39 M_CHB_DQ61 DDR_B_DQ_61
AB37 M_CHB_DQ62 DDR_B_DQ_62
AB38 M_CHB_DQ63 DDR_B_DQ_63

DDR_REF NEED ROUTING
Width/Spacing: 12/12 mils

+1P5V_DUAL
NCB4 0.1UF/16V
NR11 1K 1%
GND
NR12 1K 1%
NCB5 0.1UF/16V
NCB115 1UF/10V mx_c0603
090420 add by ESL

MCH_DDR_RPU, MCH_DDR_RPD, MCH_DDR_SPU, MCH_DDR_SPD
NEED ROUTING LESS THEN 1000MIL LENGTH.
WIDTH/SPACING = 10/10 MIL

+1P5V_DUAL
NR13 80.6 1%
NCB6 0.1UF/16V
NR17 80.6 1%

+1P5V_DUAL
NR15 80.6 1%
NCB7 0.1UF/16V
NR16 249 1%

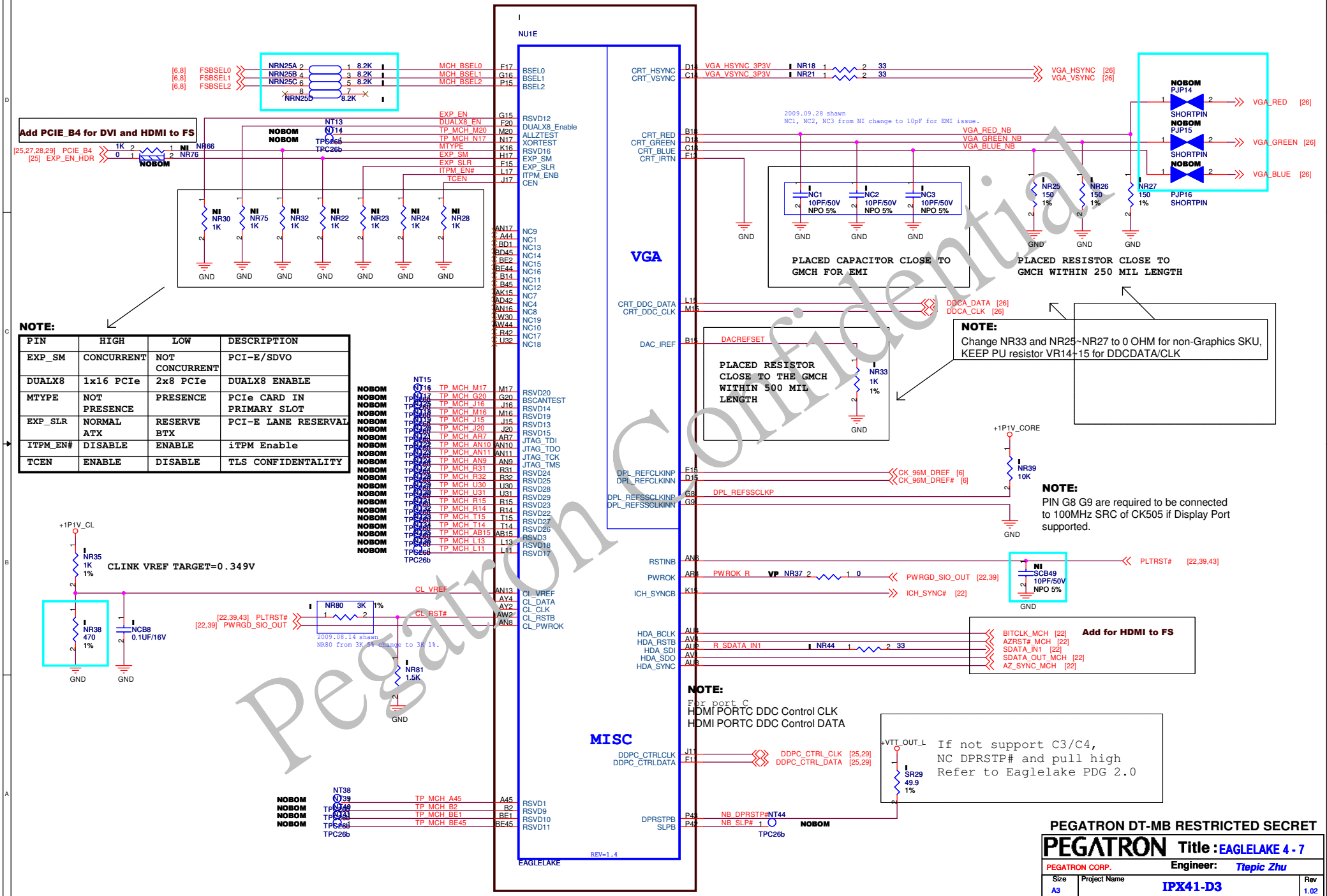
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : EAGLELAKE 3 - 7

Pegatron Corp. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 12 of 54



NOTE:

PIN	HIGH	LOW	DESCRIPTION
EXP_SM	CONCURRENT	NOT CONCURRENT	PCI-E/SDVO
DUALX8	1x16 PCIe	2x8 PCIe	DUALX8 ENABLE
MTYPE	NOT PRESENCE	PRESENCE	PCIe CARD IN PRIMARY SLOT
EXP_SLR	NORMAL ATX	RESERVE BTX	PCI-E LANE RESERVAL
ITPM_EN#	DISABLE	ENABLE	iTPM Enable
TCEN	ENABLE	DISABLE	TLS CONFIDENTALITY

NOTE:
Change NR33 and NR25~NR27 to 0 OHM for non-Graphics SKU, KEEP PU resistor VR14~15 for DDCDATA/CLK

NOTE:
PIN G8 G9 are required to be connected to 100MHz SRC of CK505 if Display Port supported.

NOTE:
For port C
HDMI PORTC DDC Control CLK
HDMI PORTC DDC Control DATA

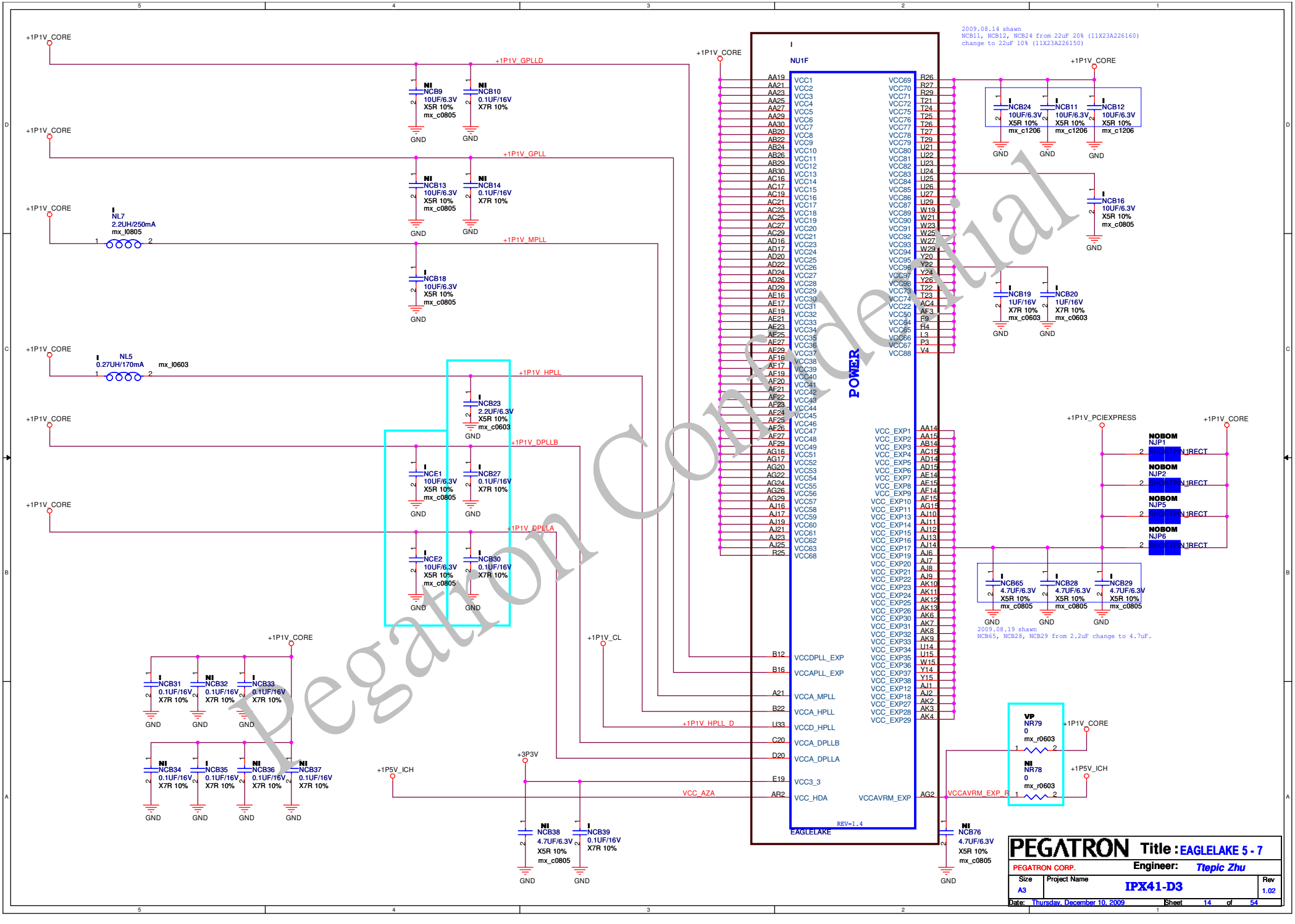
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : EAGLELAKE 4 - 7

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 13 of 54

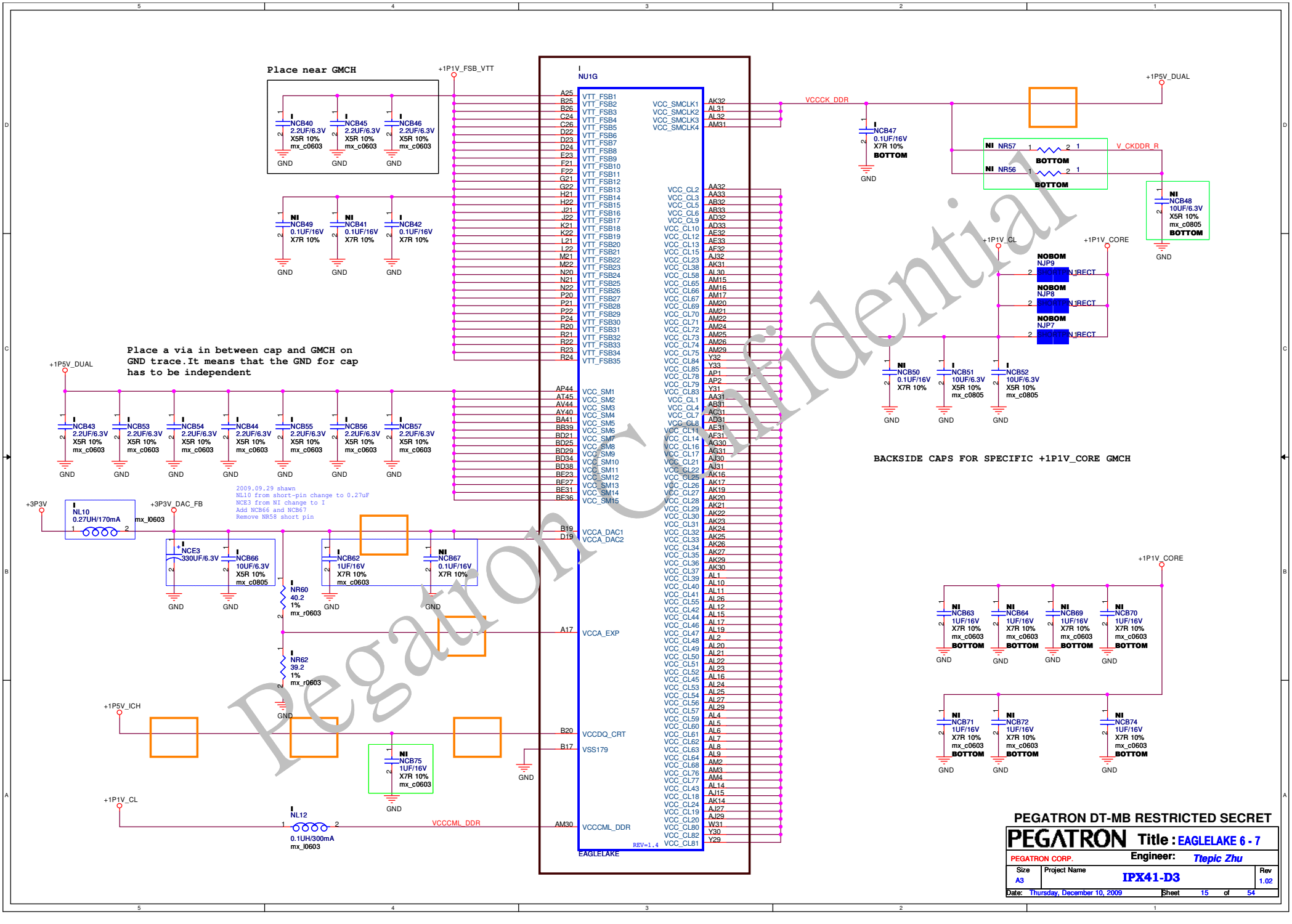


PEGATRON Title : EAGLELAKE 5 - 7

PEGATRON CORP. Engineer: Ttepic Zhu

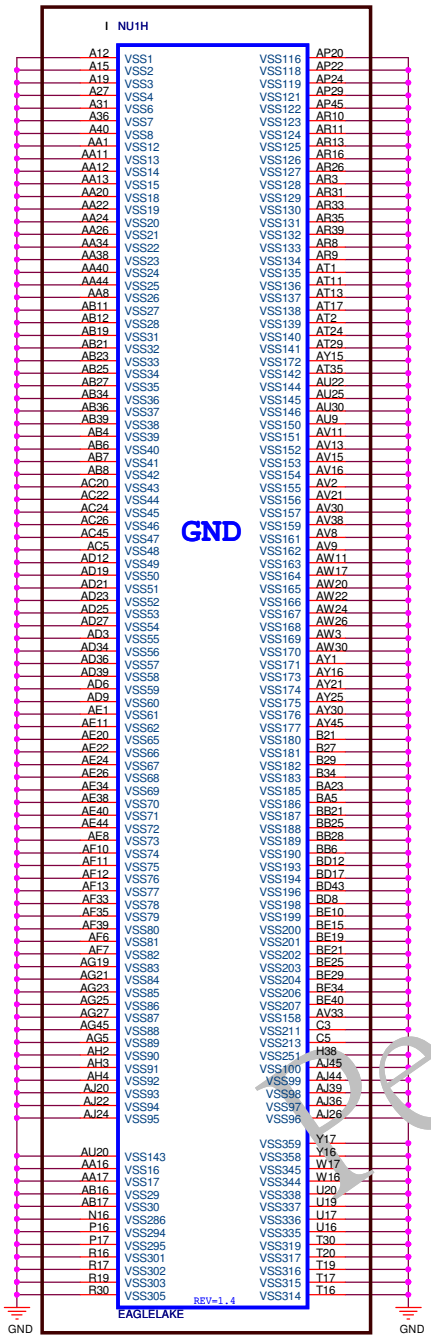
Size	Project Name	Rev
A3	IPX41-D3	1.02

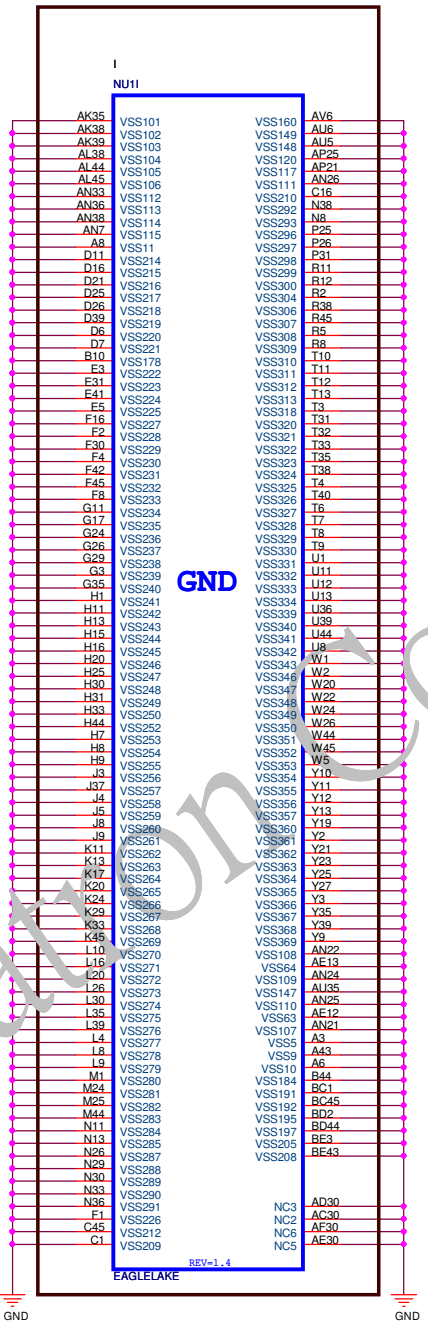
Date: Thursday, December 10, 2009 Sheet 14 of 54



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : EAGLELAKE 6 - 7	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 15 of 54	



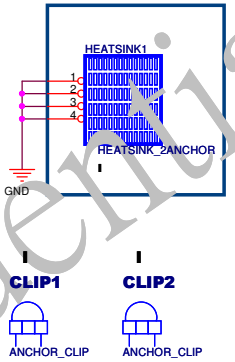


EAGLELAKE-P/Q/G

13G070110360 HEATSINK 42.2*42.2*30mm SILVER

13G070183000 HEATSINK 42.3*42.3*30mm GLUE

13G070308012 HEATSINK 42.3*42.3*30mm SILVER



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : EAGLELAKE 7 - 7

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 16 of 54

NOTE:
Below 4 signals are different connection in Eaglelake platform
Channel A : CS1/WE/MA0
Channel B : ODT3 (G41 No ODT3)

XMM1 COLOR: BLUE

M_CHA_DQ[0..63] [11]
M_CHA_MAA[1..14] [11]
M_CHA_MAA0 [12]

DIMMA0A

NOTE:
Check clock source if Eaglelake implemented

[11] M_CHA_CLK0
[11] M_CHA_CLK0#
[11] M_CHA_CLK2
[11] M_CHA_CLK2#
06/03 Important! follow Intel MRC code, only DIMMA need.

[12] M_CHA_CS#1
[11] M_CHA_CS#0

[11] M_CHA_CKE1
[11] M_CHA_CKE0

[11] M_CHA_BA2
[11] M_CHA_BA1
[11] M_CHA_BA0

[6,18,22,24,25] SMB_DATA_S
[6,18,22,24,25] SMB_CLK_S

[12] M_CHA_WE#
[11] M_CHA_RAS#
[11] M_CHA_CAS#

[11] M_CHA_ODT1
[11] M_CHA_ODT0

[12,18] DDR3_DRAMRST#

[11] M_CHA_DM7
[11] M_CHA_DM6
[11] M_CHA_DM5
[11] M_CHA_DM4
[11] M_CHA_DM3
[11] M_CHA_DM2
[11] M_CHA_DM1
[11] M_CHA_DM0

SWAP DATA signal

DDR3_DIMM_240P

DIMMA0B

+1P5V_DUAL
+0P75V_VTT_DDR
D3CB17 4.7UF/6.3V X5R 10% mx_c0805
D3CB18 0.1UF/16V X7R 10%
GND

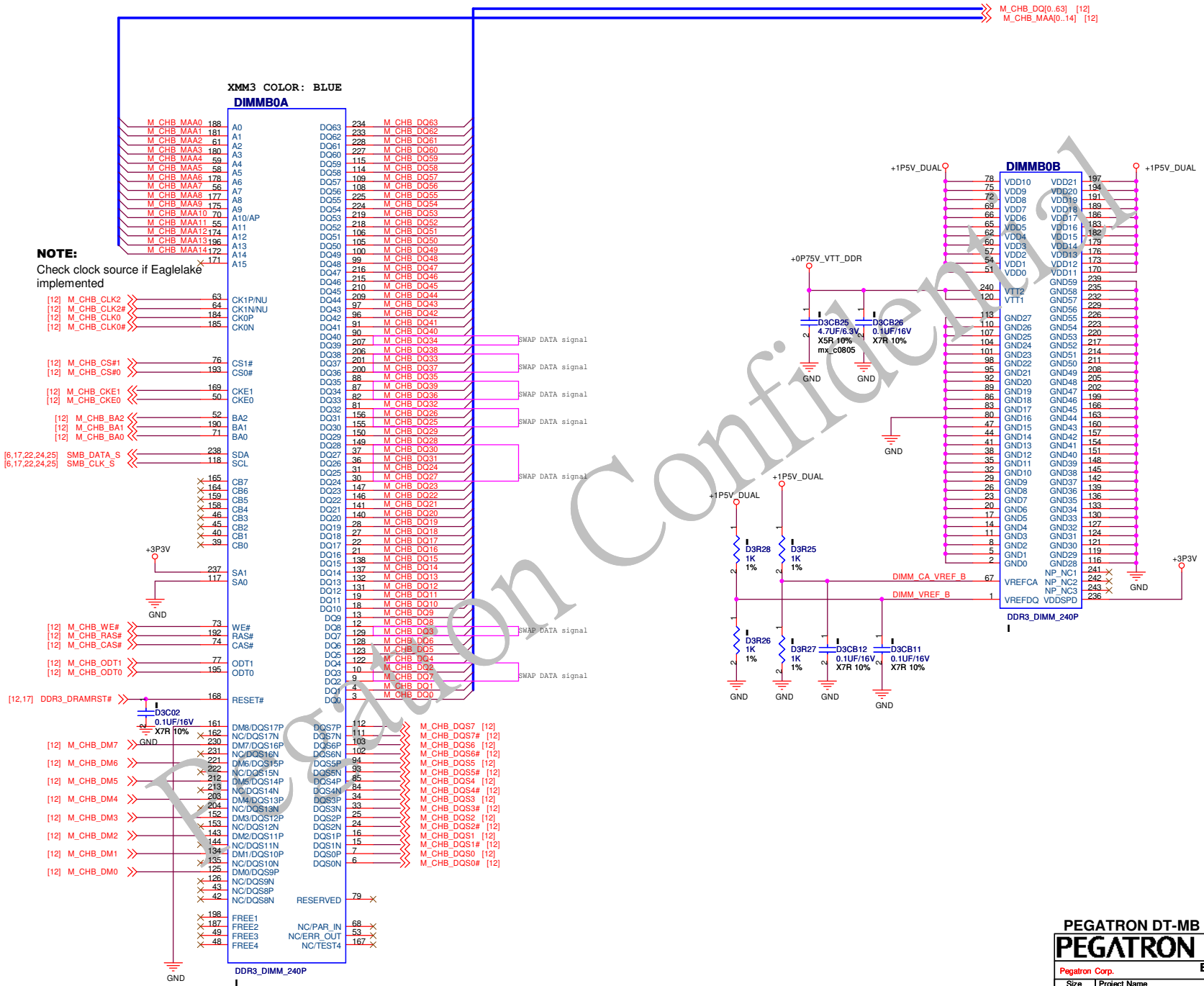
+1P5V_DUAL +1P5V_DUAL
D3R17 1K 1%
D3R15 1K 1%
DIMM_CA_VREF_A
DIMM_VREF_A
D3R18 1K 1%
D3R16 1K 1%
D3CB6 0.1UF/16V X7R 10%
D3CB5 0.1UF/16V X7R 10%

+3P3V

DDR3_DIMM_240P

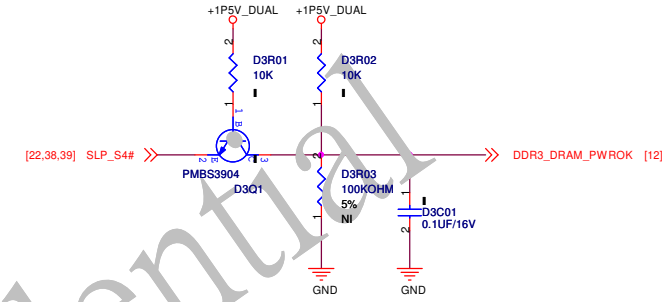
PEGATRON DT-MB RESTRICTED SECRET

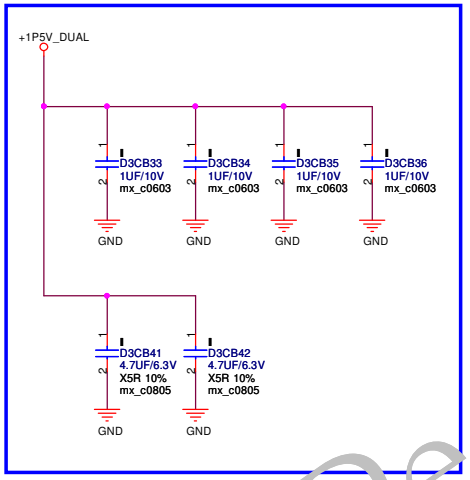
PEGATRON	Title : DDR3 DIMMA	
Pegatron Corp.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 17 of 54	



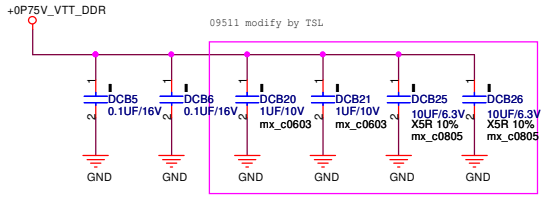
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3 DIMMB		
Pegatron Corp.	Engineer: Ttepic Zhu		
Size: A3	Project Name: IPX41-D3		Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 18 of 54		



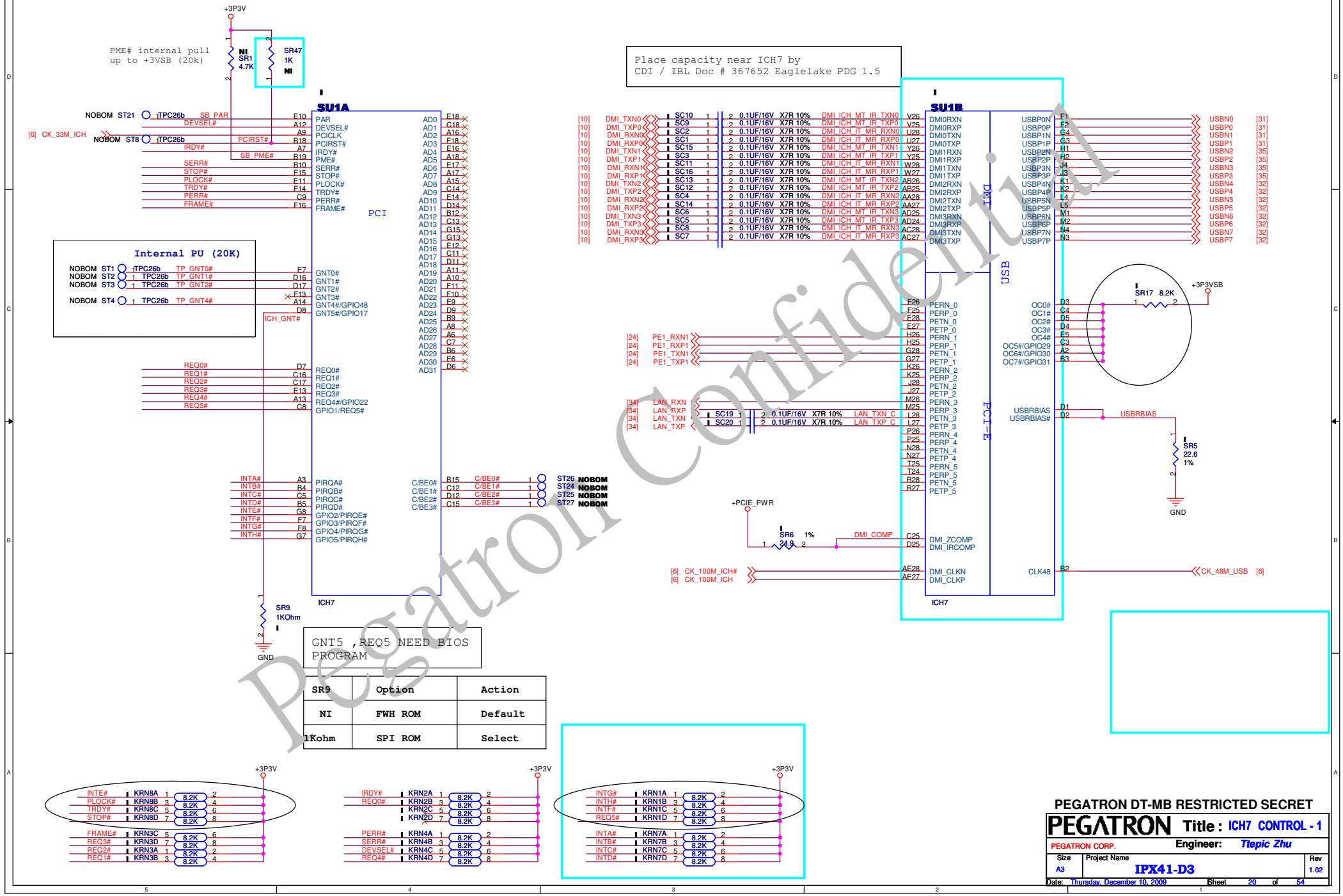


09511 modify by TSL

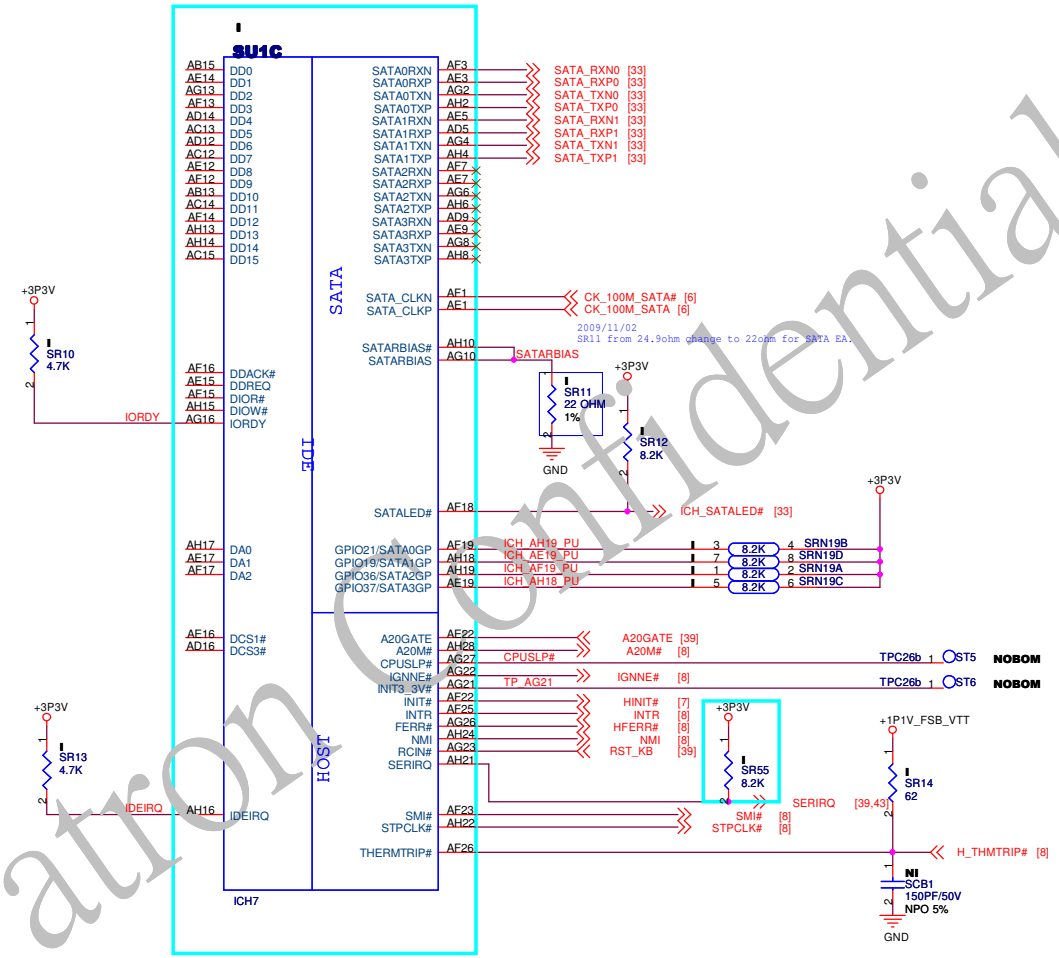


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3 Termination A&B	
Pegatron Corp.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 19 of 54	

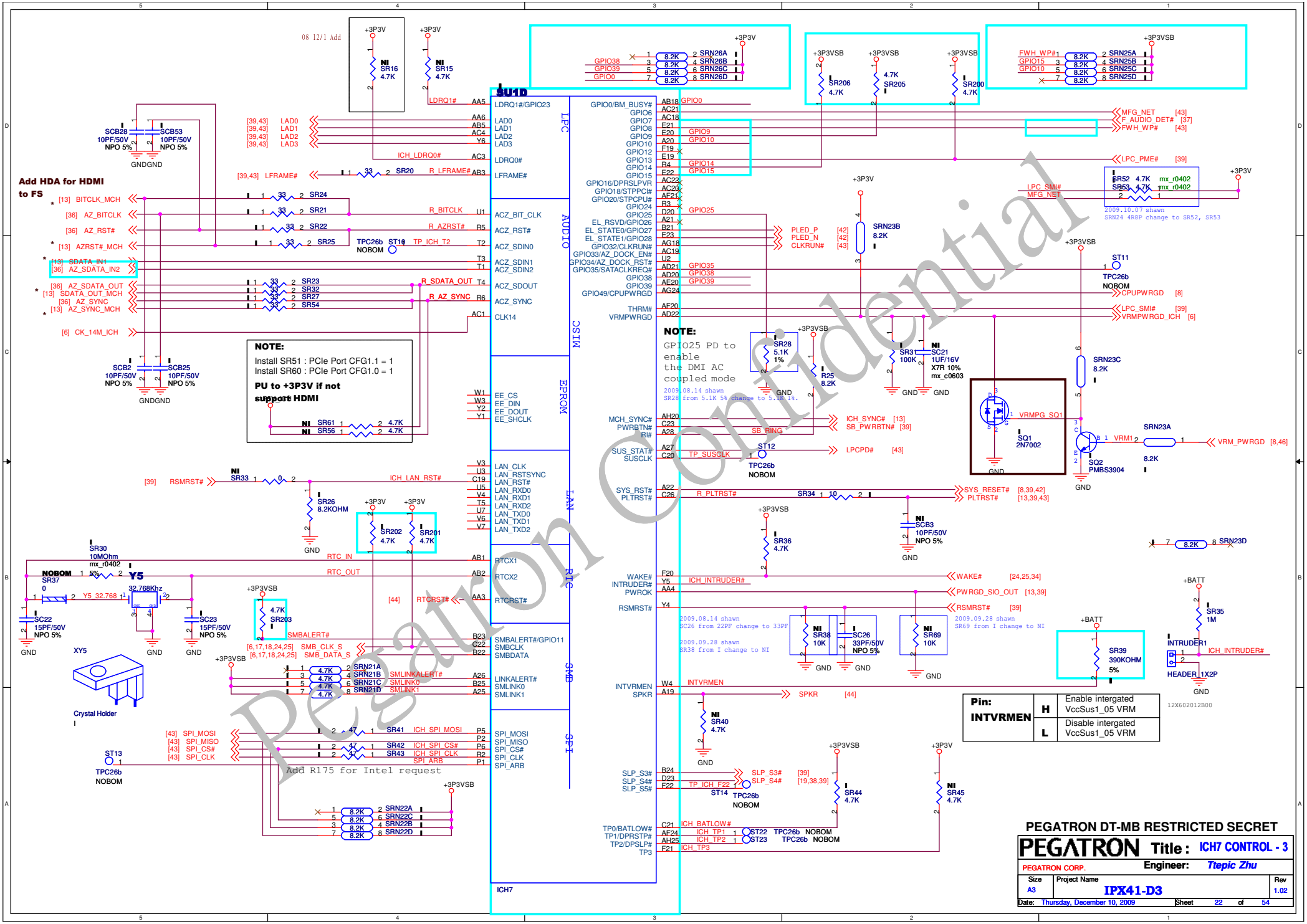


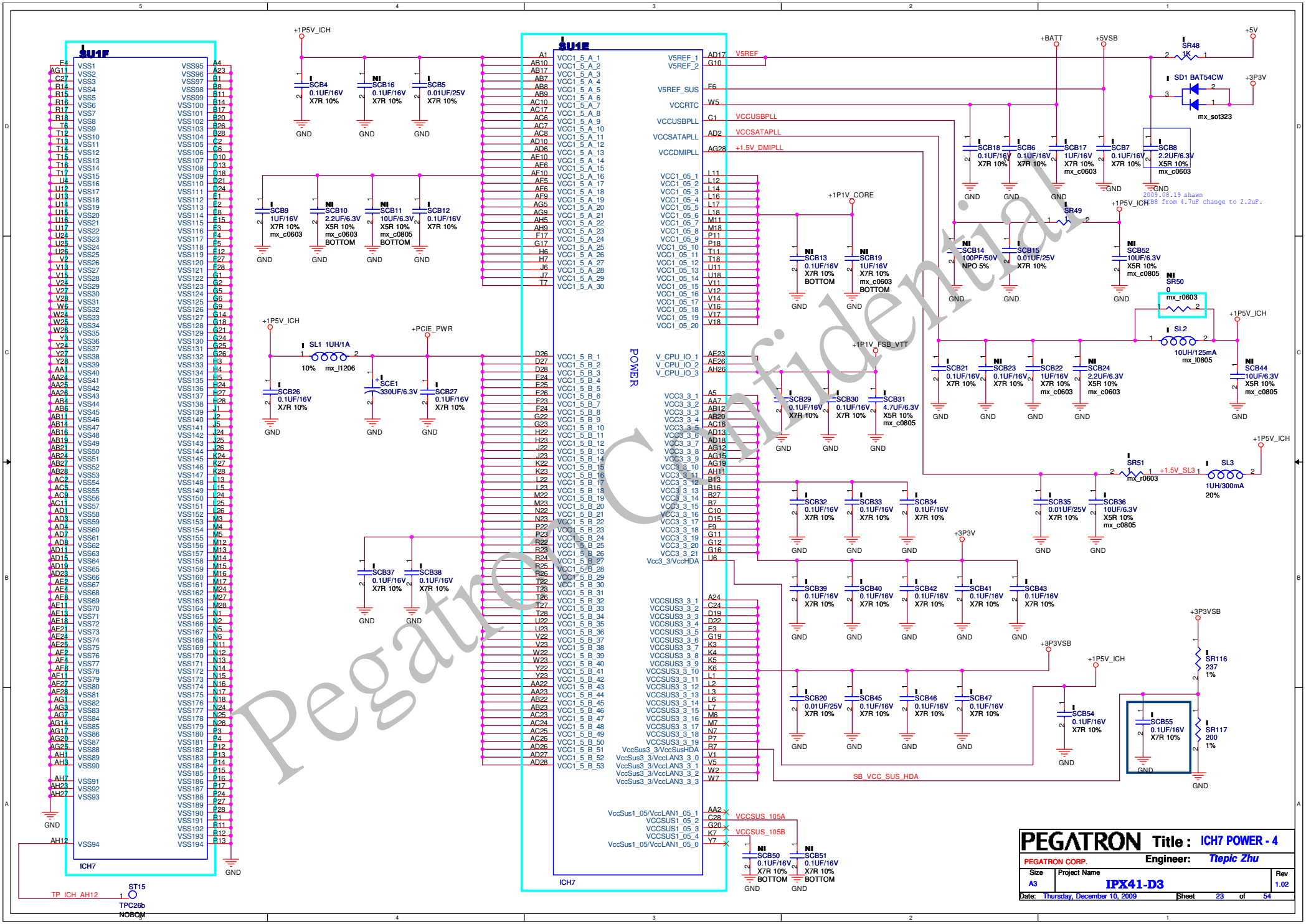
SR9	Option	Action
NI	FWH ROM	Default
1Kohm	SPI ROM	Select



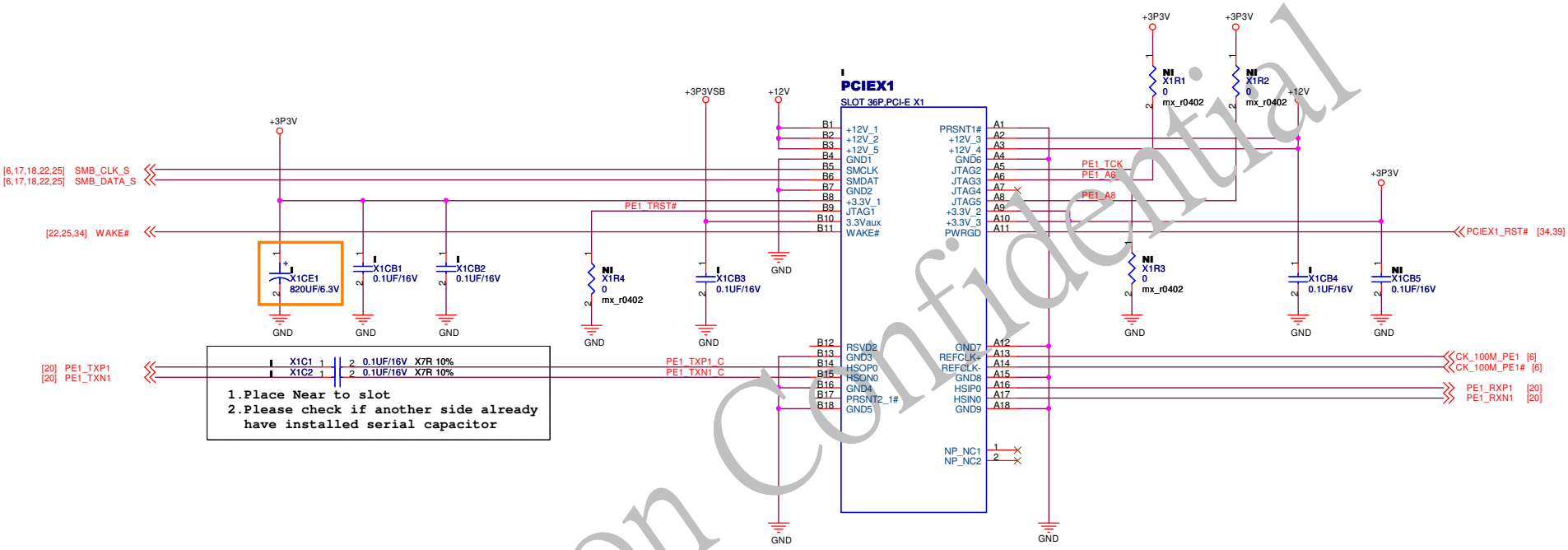
PEGATRON DT-MB RESTRICTED SECRET

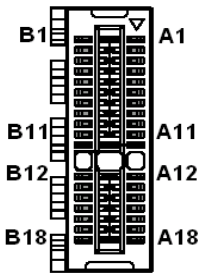
PEGATRON	Title : ICH7 CONTROL - 2	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 21 of 54	


SU1D
LPC
AUDIO
MISC
EEPROM
LAN
RTC
SMB
SPI
ICH7
Add HDA for HDMI to FS
NOTE:
Install SR51 : PCIe Port CFG1.1 = 1
Install SR60 : PCIe Port CFG1.0 = 1
PU to +3P3V if not support HDMI
NOTE:
GPIO25 PD to enable the DMI AC coupled mode
2009.08.14 shawn SR28 from 5.1K 5% change to 5.1K 1%.
2009.10.07 shawn SRN24 4R8P change to SR52, SR53
2009.08.14 shawn SC26 from 22PF change to 33PF
2009.09.28 shawn SR38 from I change to NI
2009.09.28 shawn SR69 from I change to NI
Add R175 for Intel request
Pin: INTVRMEN
H Enable intergated VccSus1_05 VRM
L Disable intergated VccSus1_05 VRM
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : ICH7 CONTROL - 3
PEGATRON CORP. Engineer: Tiepic Zhu
Size A3 Project Name IPX41-D3 Rev 1.02
Date: Thursday, December 10, 2009 Sheet 22 of 54
Pegatron Confidential

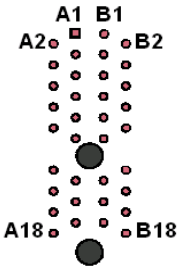

SU1F
ICH7
SU1E
ICH7
POWER
+1P5V_ICH
+PCIE_PWR
+1P1V_CORE
+1P1V_FSB_VTT
+BATT
+5VSB
+5V
+3P3V
+3P3VSB
V5REF
VCCUSBPLL
VCCSATAPLL
+1.5V_DMIPLL
SB_VCC_SUS_HDA
VCCSUS_105A
VCCSUS_105B
+1.5V_SL3
TP_ICH_AH12
ST15
TPC26b
NOBOM
PEGATRON
Title : ICH7 POWER - 4
PEGATRON CORP.
Engineer: Ttepic Zhu
Size A3
Project Name IPX41-D3
Rev 1.02
Date: Thursday, December 10, 2009
Sheet 23 of 54
2009.08.19 shawn
SB8 from 4.7uF change to 2.2uF.
Pegatron Confidential

PCI Express x1 SLOT





TOP SIDE VIEW

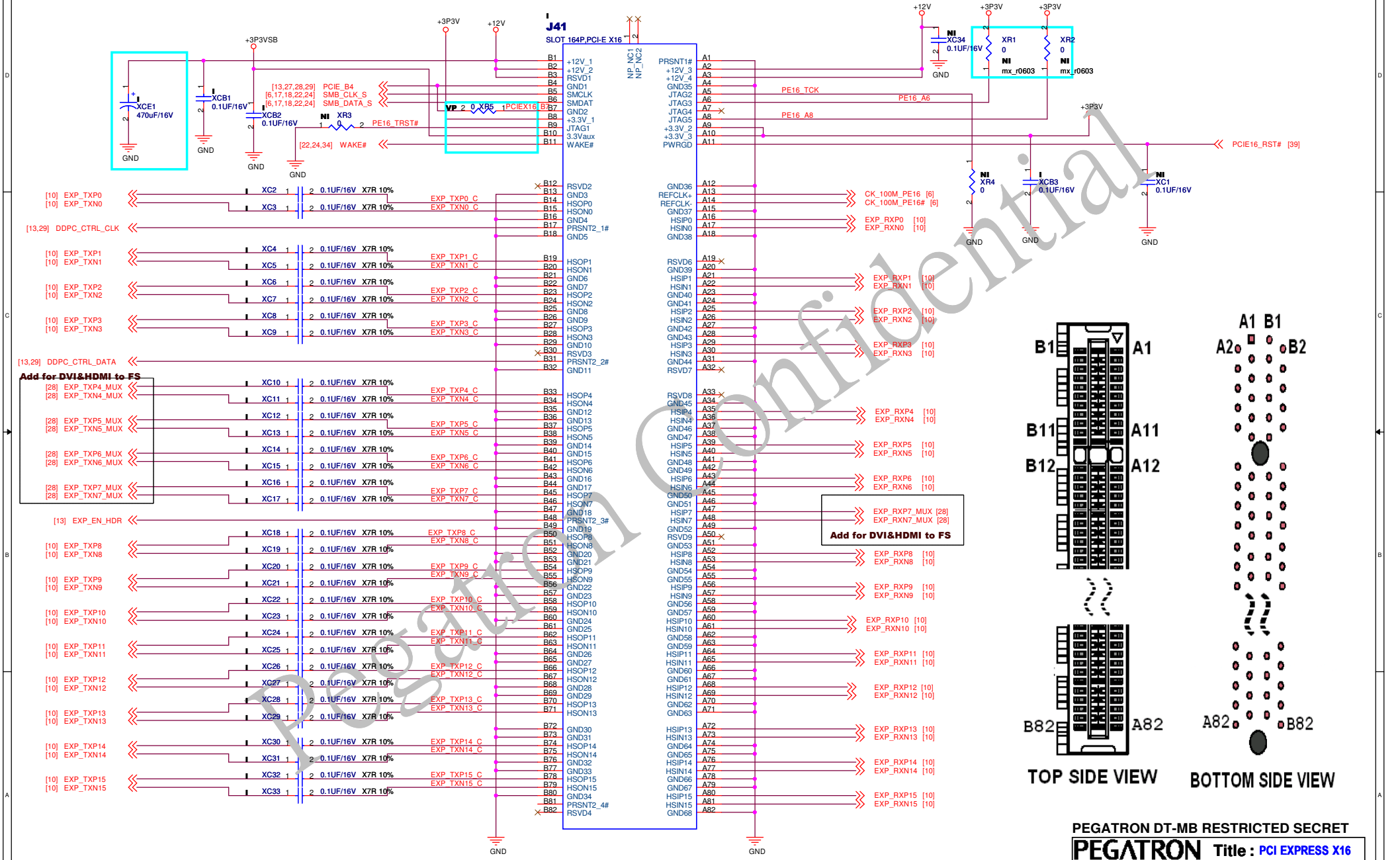


BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

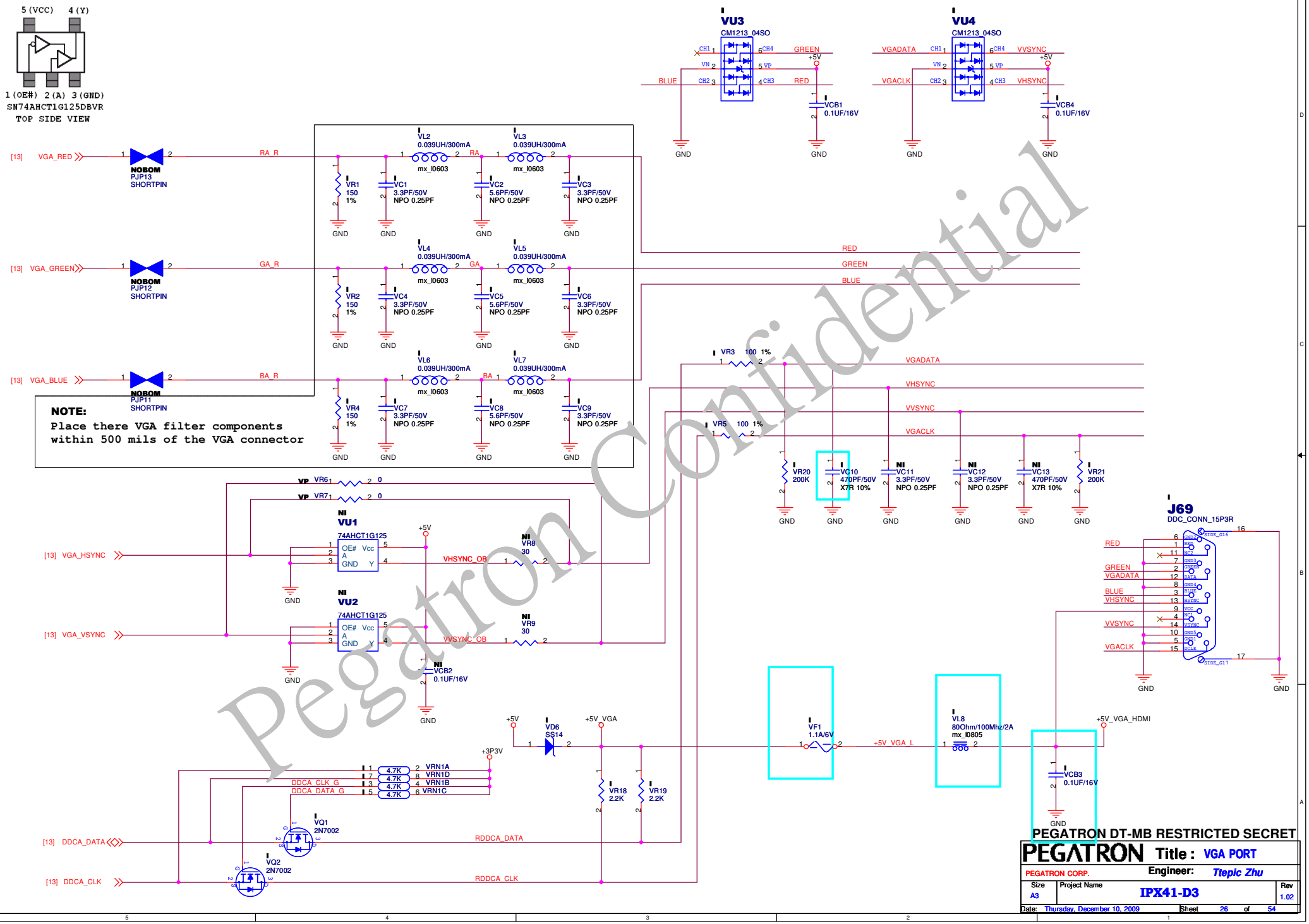
PEGATRON	Title : PCI EXPRESS X1	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 24 of 54	

PCI EXPRESS X16 Graphics Card Slot



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCI EXPRESS X16	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 25 of 54	

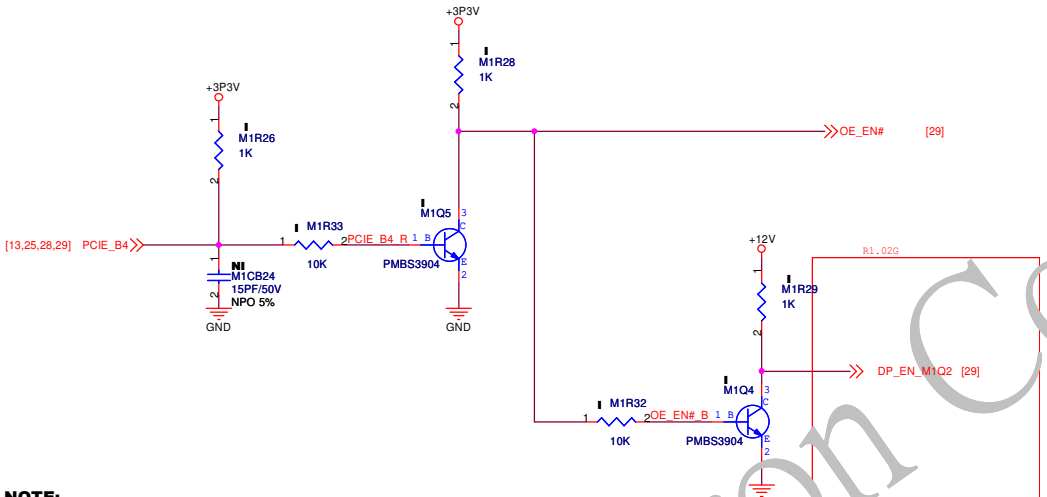


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VGA PORT	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 26 of 54	

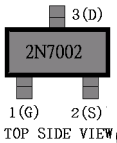
Add HDMI CONTROL to FS

Digital Port Switch Control Logic



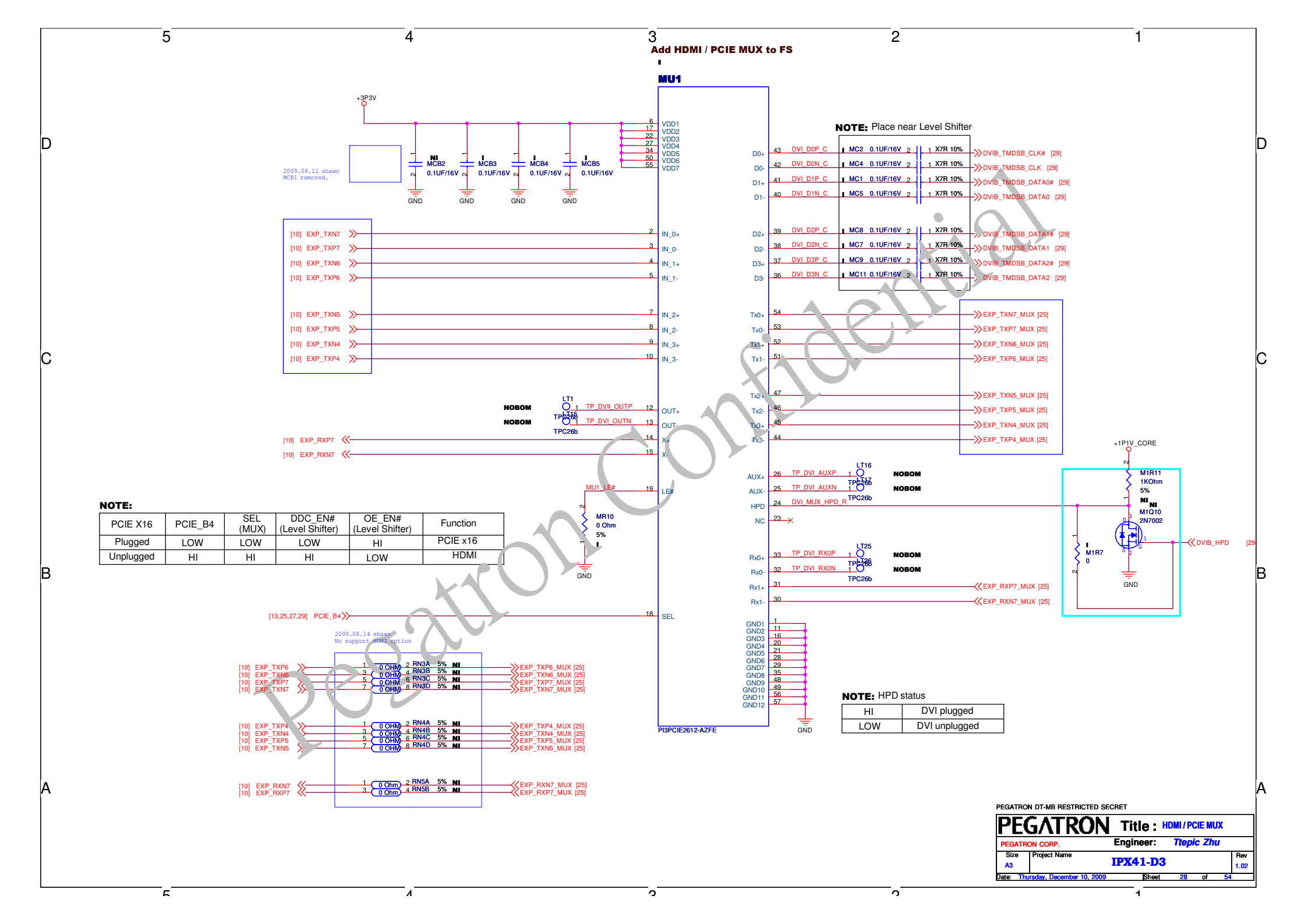
NOTE:

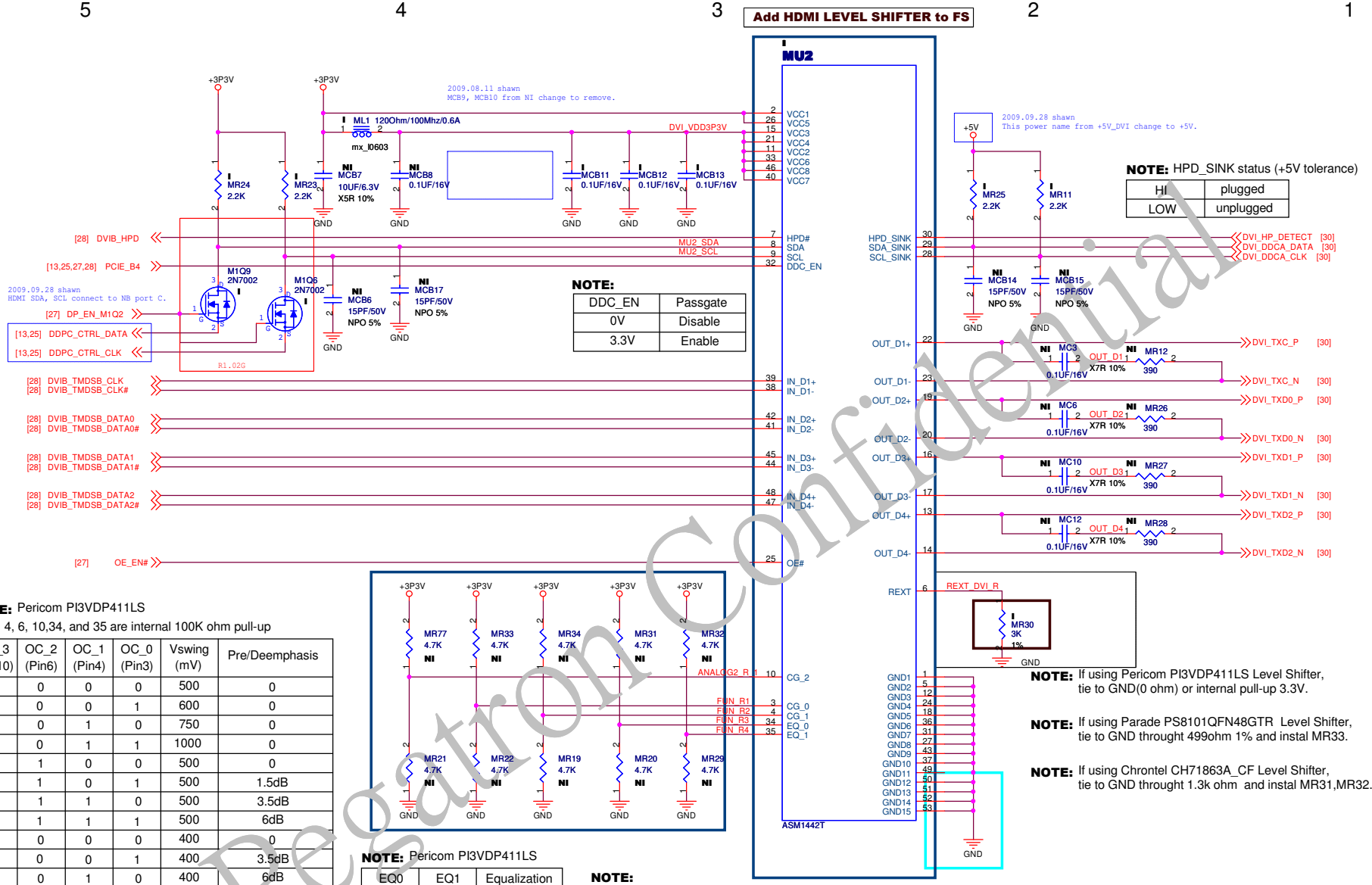
PCIE X16	PCIE_B4	SEL (MUX)	DDC_EN# (Level Shifter)	OE_EN# (Level Shifter)	Function
Plugged	LOW	LOW	LOW	HI	PCIE x16
Unplugged	HI	HI	HI	LOW	HDMI



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : HDMI CONTROL	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 27 of 54	


Add HDMI / PCIE MUX to FS
MU1
PI3PCIE2612-AZFE
NOTE: Place near Level Shifter
NOTE:
NOTE: HPD status
HI DVI plugged
LOW DVI unplugged
PCIE X16 | PCIE_B4 | SEL (MUX) | DDC_EN# (Level Shifter) | OE_EN# (Level Shifter) | Function
Plugged | LOW | LOW | LOW | HI | PCIE x16
Unplugged | HI | HI | HI | LOW | HDMI
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : HDMI / PCIE MUX
PEGATRON CORP.
Engineer: Ttepic Zhu
Size A3
Project Name IPX41-D3
Rev 1.02
Date: Thursday, December 10, 2009
Sheet 28 of 54
Pegatron Confidential



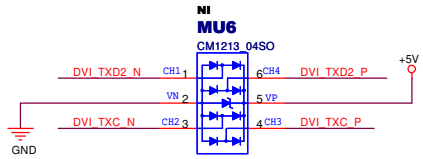
PEGATRON DT-MB RESTRICTED SECRET

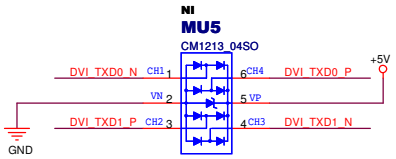
PEGATRON Title : HDMI LEVEL SHIFTER

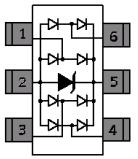
PEGATRON CORP. Engineer: Ttepic Zhu

Size: A3 | Project Name: IPX41-D3 | Rev: 1.02

Date: Thursday, December 10, 2009 | Sheet 29 of 54



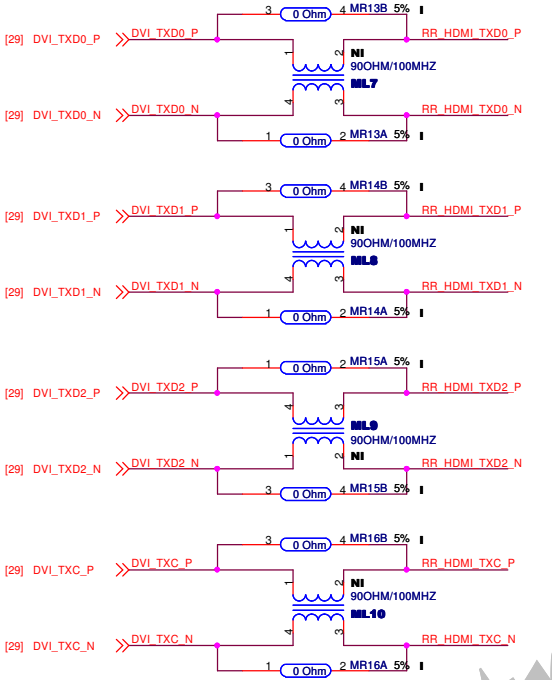


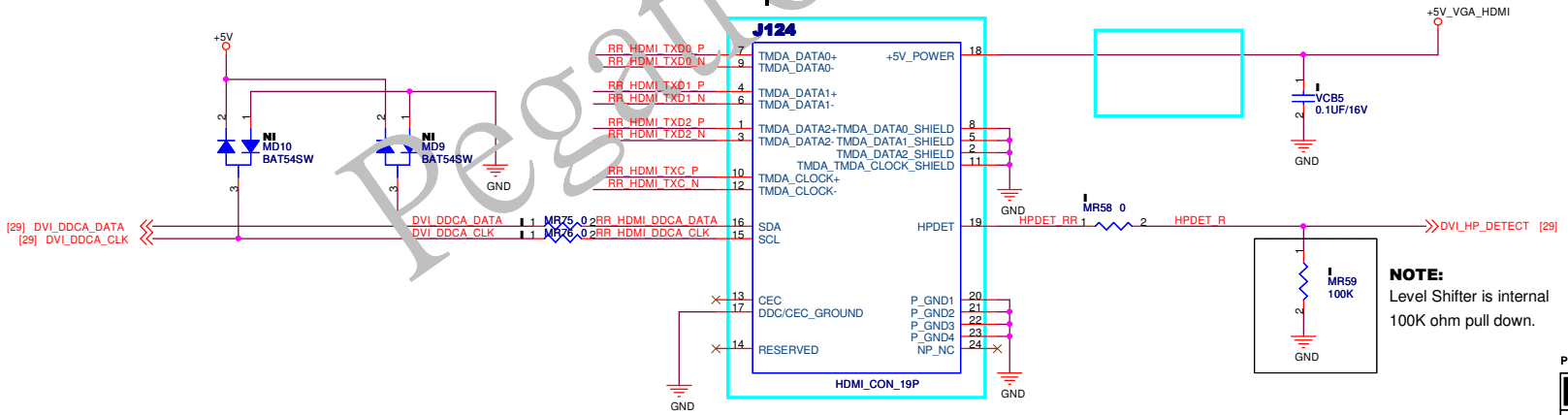


NOTE:
Level Shifter is internal 100K ohm pull down.

NOTE: HPDET status

High	Plugged
Low	Unplugged





NOTE:
Level Shifter is internal
100K ohm pull down.

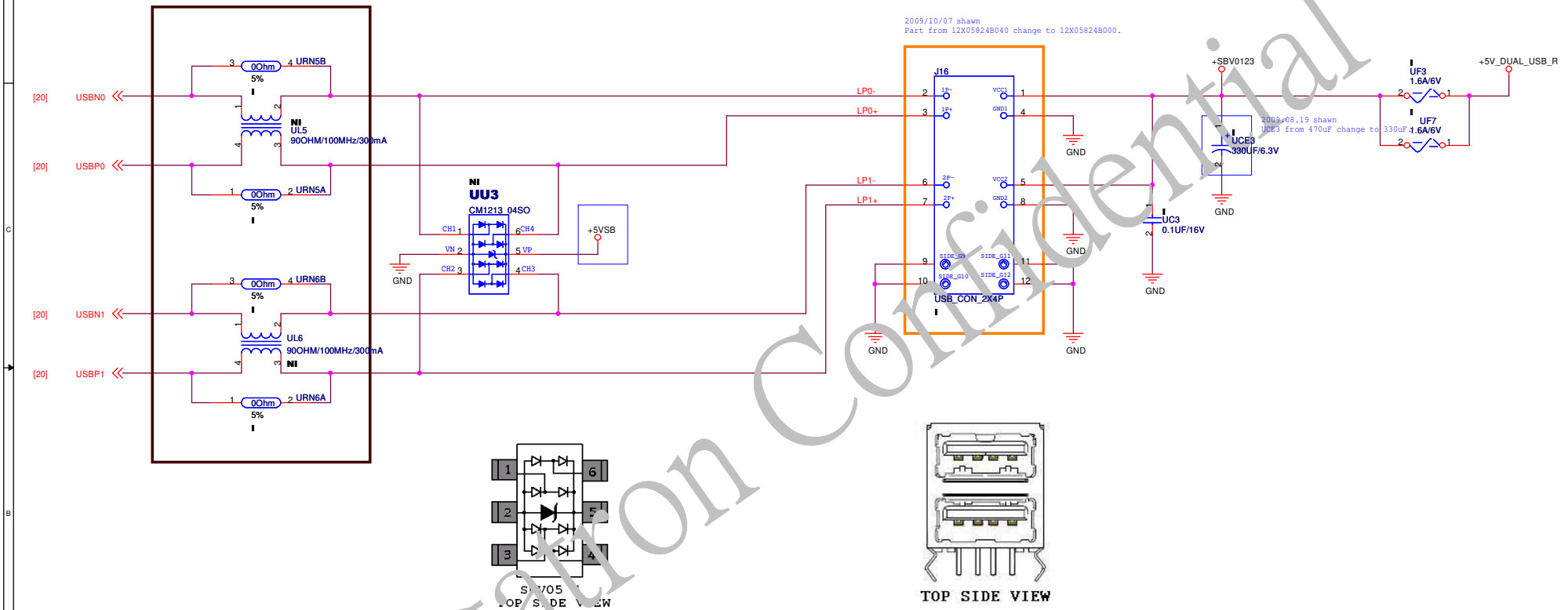
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : HDMI PORT

PEGATRON CORP. Engineer: Ttepic Zhu

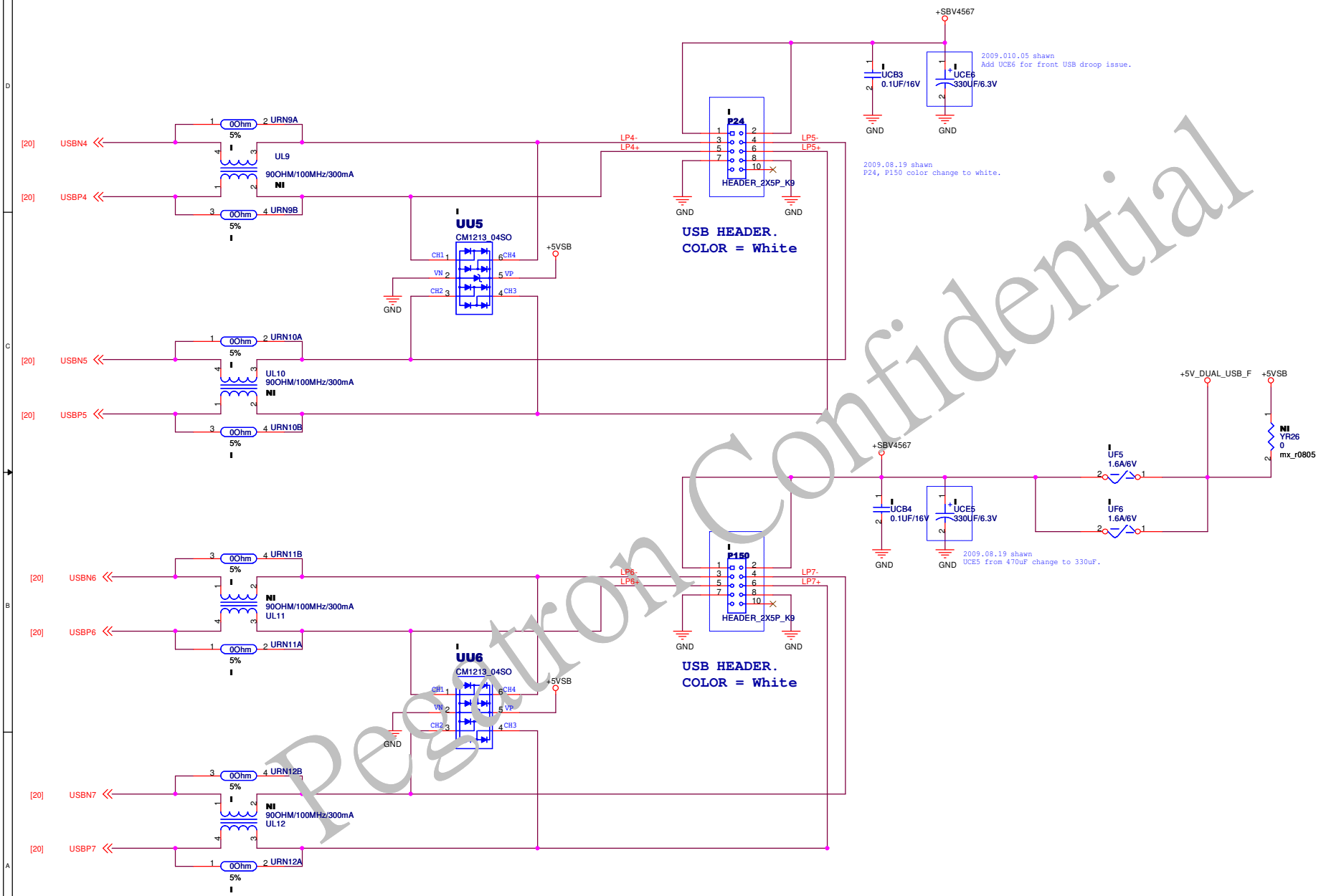
Size	Project Name	Rev
A3	IPX41-D3	1.02

Date: Thursday, December 10, 2009 Sheet 30 of 54



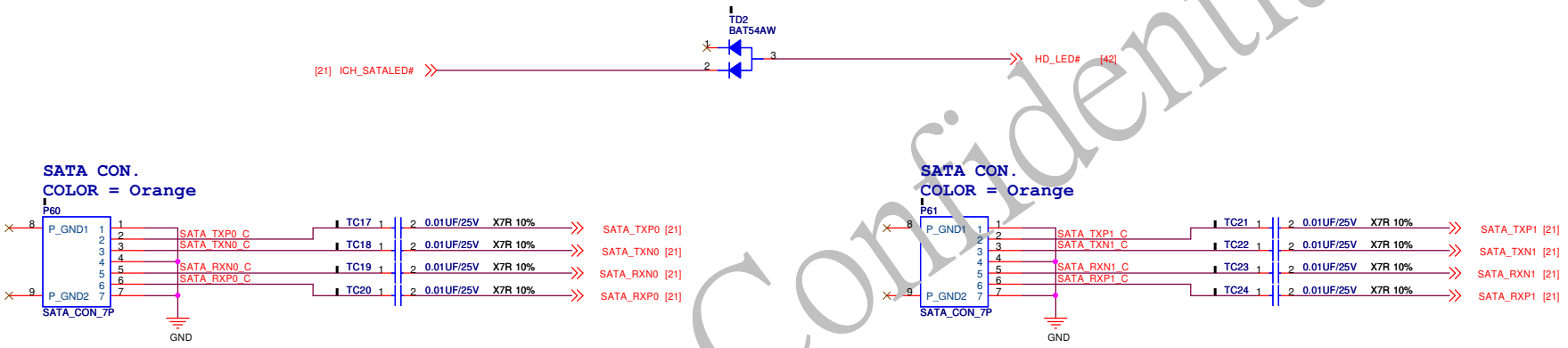
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DOUBLE USB CON.	
Pegatron Corp.	Engineer: Tiepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 31 of 54	



PEGATRON	Title :	USB HEADER CON.
PEGATRON CORP.	Engineer:	Ttepic Zhu
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 32 of 54	

SATA CONNECTOR FOR CPC



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SATA2 FOR CPC	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 33 of 54	

RTL8111DL Switching regulator

PIN	PIN NAME	I/O	Function
48	REG_OUT	O	*Regulator output*
4	FB12	I	*Feedback pin*
43	ENSWREG	I	*3.3V : Enable ; 0V : disable*
44,45	VDDREG	P	*3.3V power pin*

8103EL	Pin
DVDD3.3V	29,37
AVDD3.3V	1
DVDD1.2V	10,13,30,36
+1.2V_OUT	19,45,48

8111DL	Pin
DVDD3.3V	29,37
AVDD3.3V	1,40
DVDD1.2V	13,36
AVDD1.2V	10,30,39
EVDD1.2V	19
+1.0V_OUT	48

Layout Guide: +3P3VSB wider than 40mil
LC2~LC5 place near 200mil to LAN

Layout Guide:
+1P2V_OUT & +1P2OUT wider than 60mil
LL1&LR18 place near 200mil to LAN
LCB6&LCB7 place near 300mil to LAN

2009.08.14 shawn
LCB17 from 22uF 20% (11X23A226160)
change to 22uF 10% (11X23A226150)

LU2

RTL8111DL_GR

NOTE:
If using eFuse funtion,
NI LU2 directly

NOTE: LED MODE
(LEDS1, LEDS0) = (1, 1) DEFAULT
(LEDS1, LEDS0) = (0, 1) ==> For this schematic

NOTE: 8111DL[PIN43]
3.3V enable internal regulator
0V disable internal regulator

Symbol	Type	Pin No (64-pin)	Pin No (48-pin)	Description				
LED0	O	57	38	LEDS1-0	00	01	10	11
LED1	O	56	35	LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ ACT
LED2	O	55	34	LED1	LINK100	LINK10/ 100/1000	LINK	LINK100/ ACT
LED3	O	54	33	LED2	LINK10	LINK10/ 100	Rx	FULL
				LED3	LINK1000	LINK1000	FULL	LINK1000 /ACT

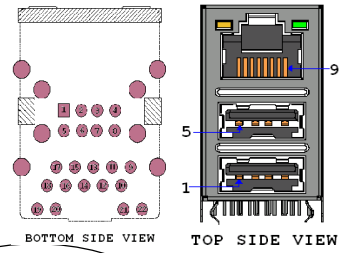
PEGATRON Title : AR8121 CONTROLLER
Pegatron Corp. Engineer: Ttepic Zhu
Size A3 | Project Name IPX41-D3 | Rev 1.02
Date: Thursday, December 10, 2009 | Sheet 34 of 54

LAN + Dual USB CONNECTOR

12XA05MYJG40

giga LAN connector

/Change to 12XA070YG040 for 10/100



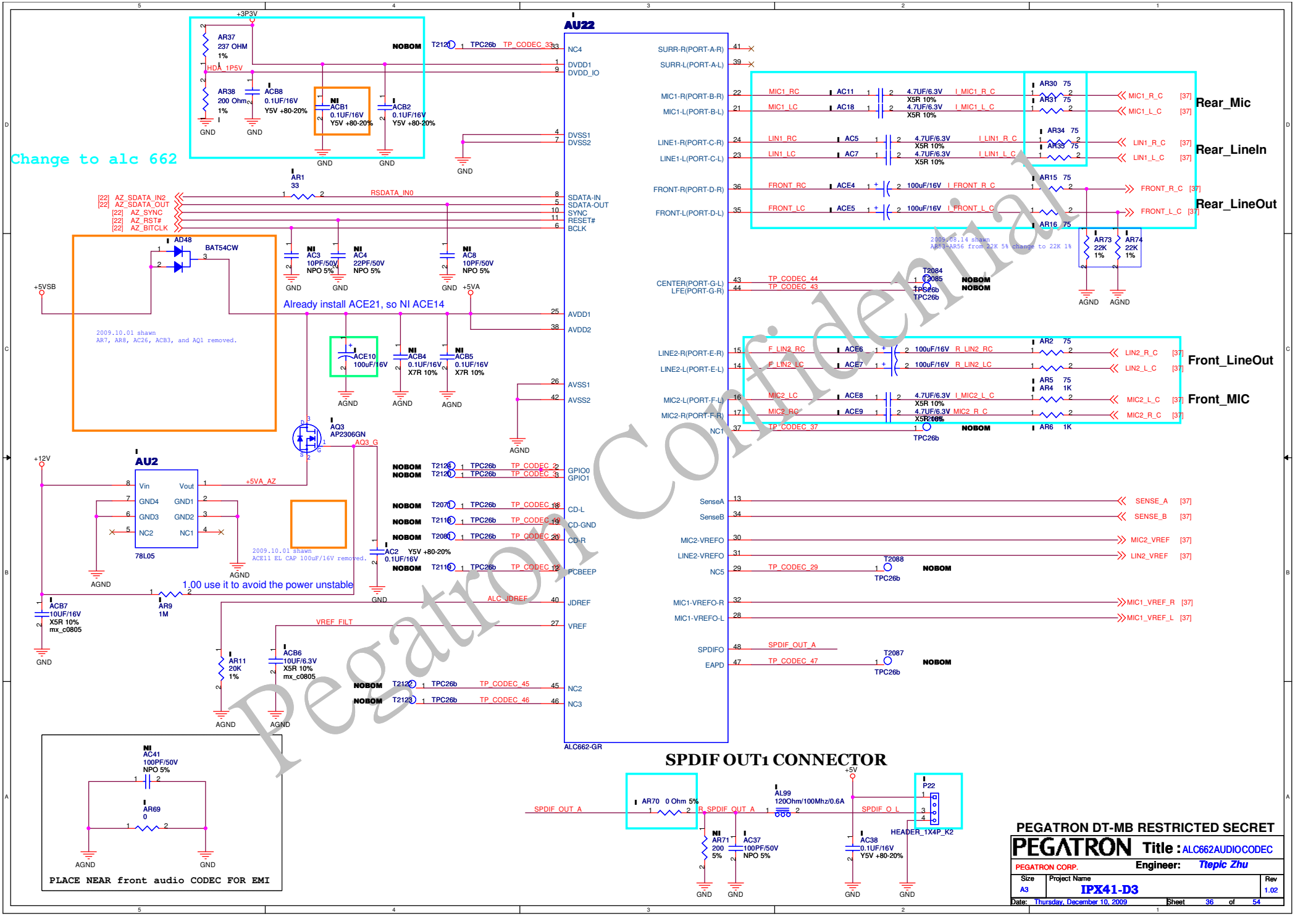
PEGATRON DT-MB RESTRICTED SECRET

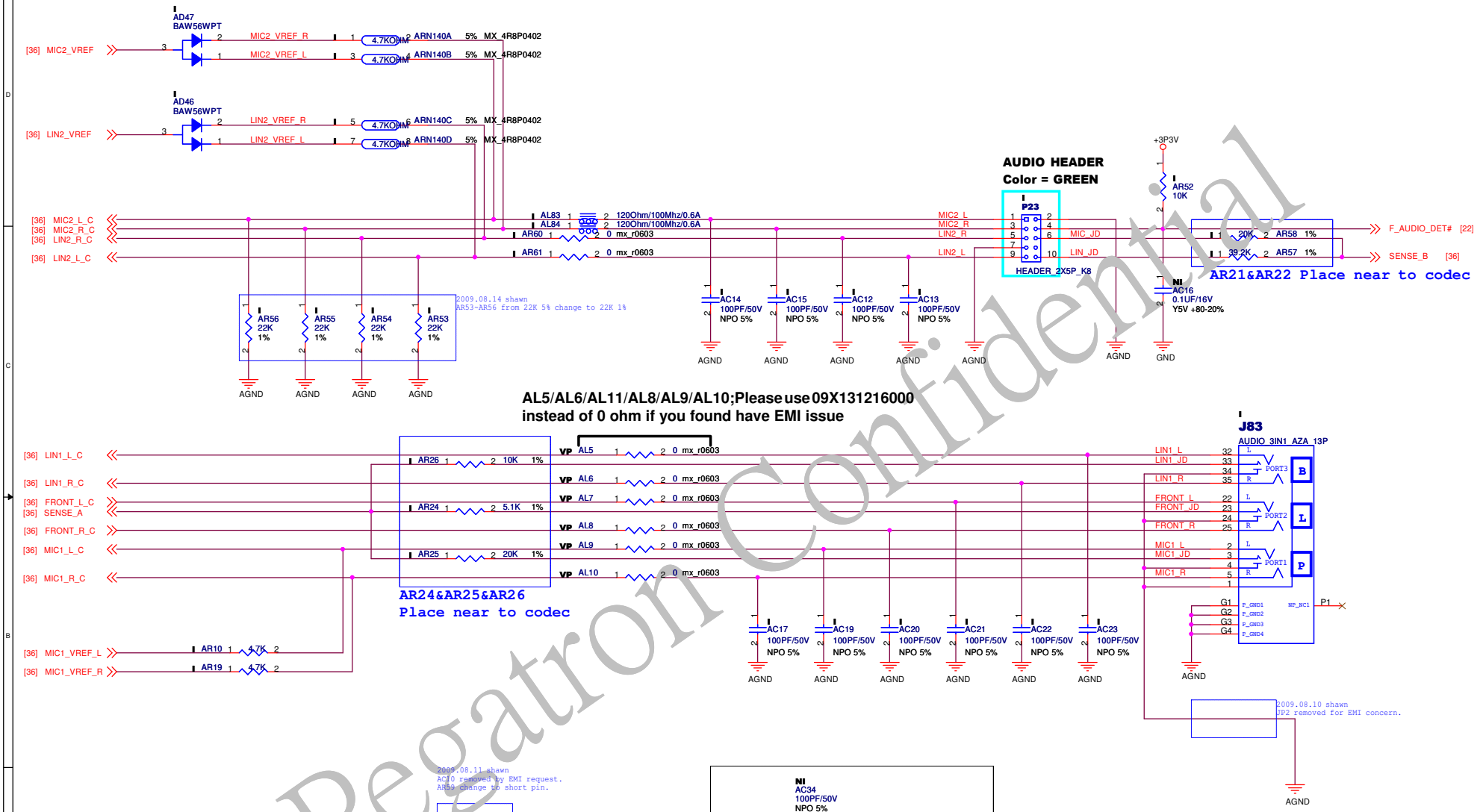
PEGATRON Title : RJ45+USB CONN.

PEGATRON CORP. Engineer: Ttepic Zhu

Size	Project Name	Rev
A3	IPX41-D3	1.02

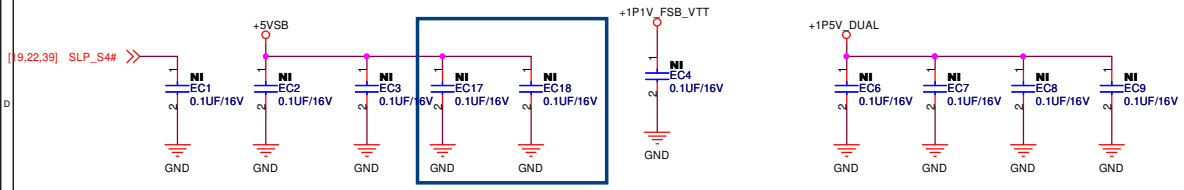
Date: Thursday, December 10, 2009 Sheet 35 of 54


Change to alc 662
AU22
ALC662-GR
Already install ACE21, so NI ACE14
1.00 use it to avoid the power unstable
Rear_Mic
Rear_LineIn
Rear_LineOut
Front_LineOut
Front_MIC
SPDIF OUT1 CONNECTOR
PLACE NEAR front audio CODEC FOR EMI
Pegatron Confidential
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : ALC662AUDIOCODEC
PEGATRON CORP. Engineer: Ttepic Zhu
Size A3 Project Name IPX41-D3 Rev 1.02
Date: Thursday, December 10, 2009 Sheet 36 of 54

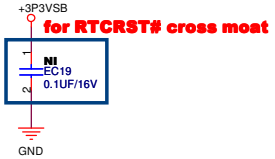


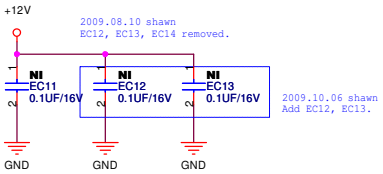
PEGATRON DT-MB RESTRICTED SECRET

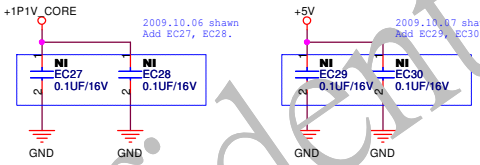
PEGATRON	Title :	AUDIOCONN
PEGATRON CORP.	Engineer:	Ttepic Zhu
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 37 of 54	

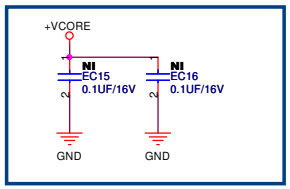


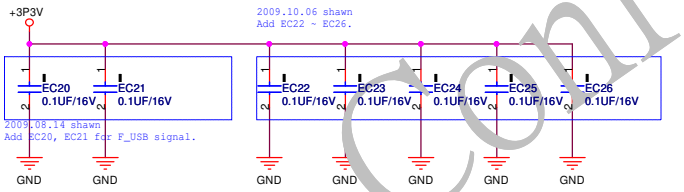
2009.08.10 shawn
EC10 removed.





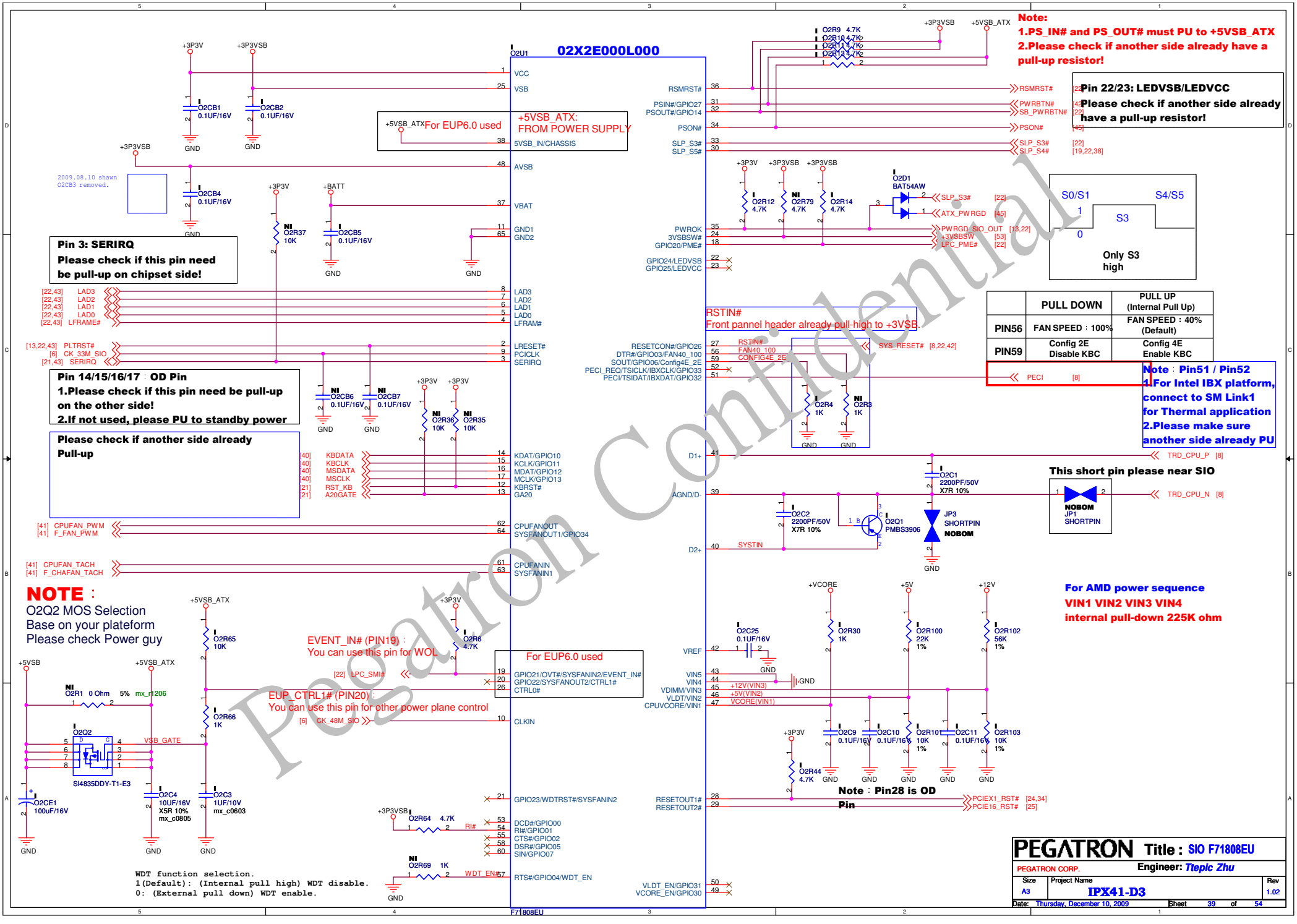






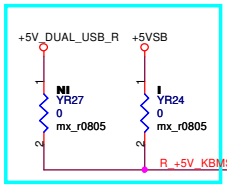
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : EMICAP	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 38 of 54	

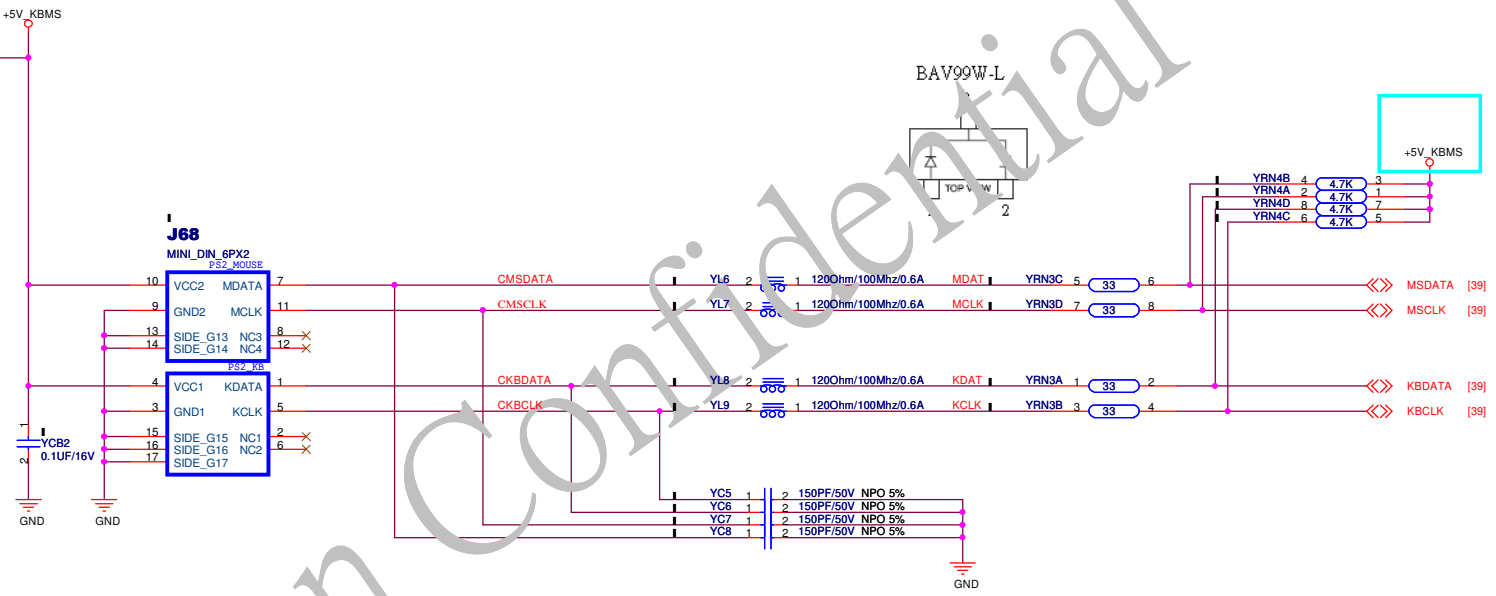


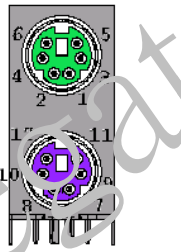
ADD FOR PS/2 WAKE ON IN S5

PS/2 KEYBOARD & MOUSE FOR CPC

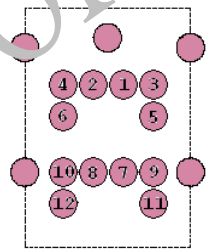


Note:
The +5V_DUAL_USB_B power trace width must have 40 mils or more





TOP SIDE VIEW

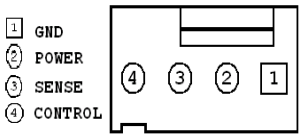


BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

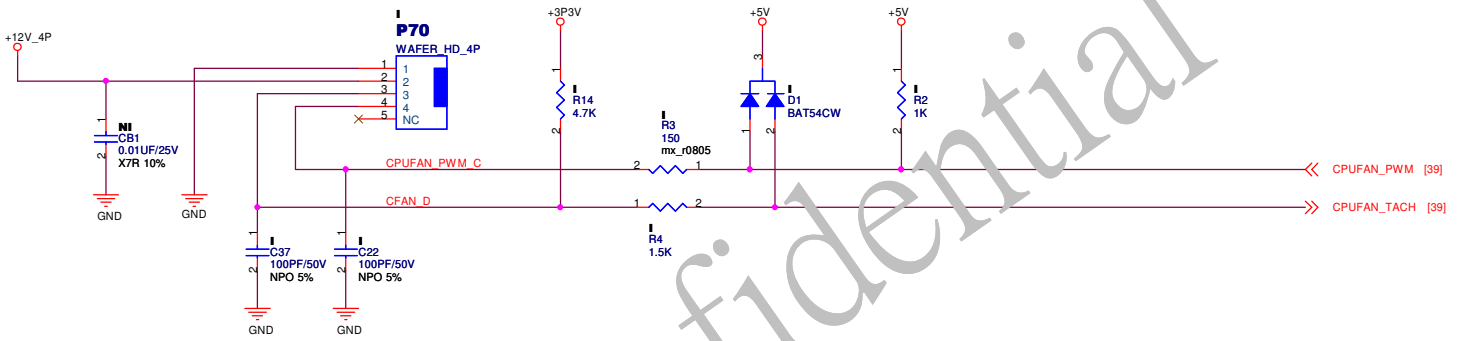
PEGATRON	Title : KB & MS FOR CPC	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 40 of 54	

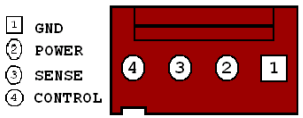
BOTTOM SIDE VIEW



TOP SIDE VIEW

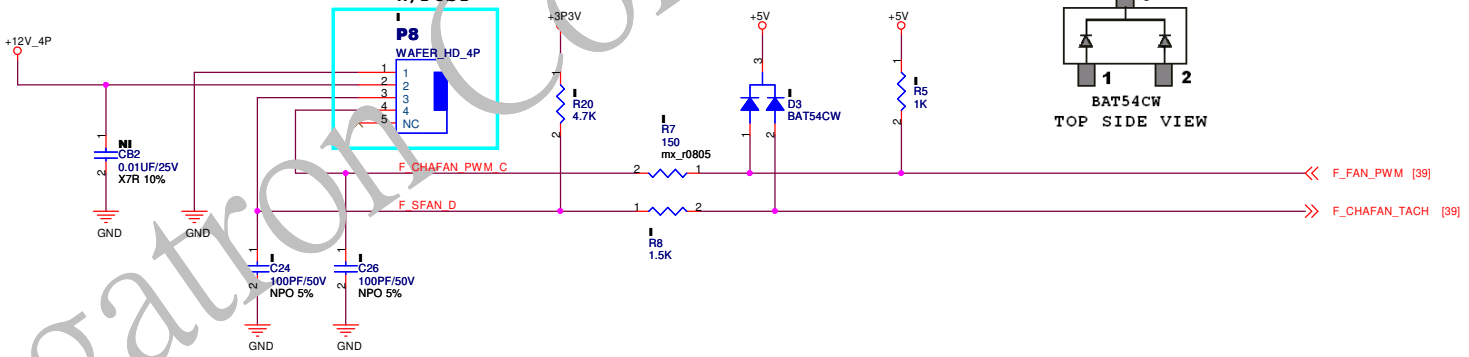
CPU FAN CON.
COLOR = White
W/POST





TOP SIDE VIEW

CHASSIS FAN CON.
COLOR = White
W/POST



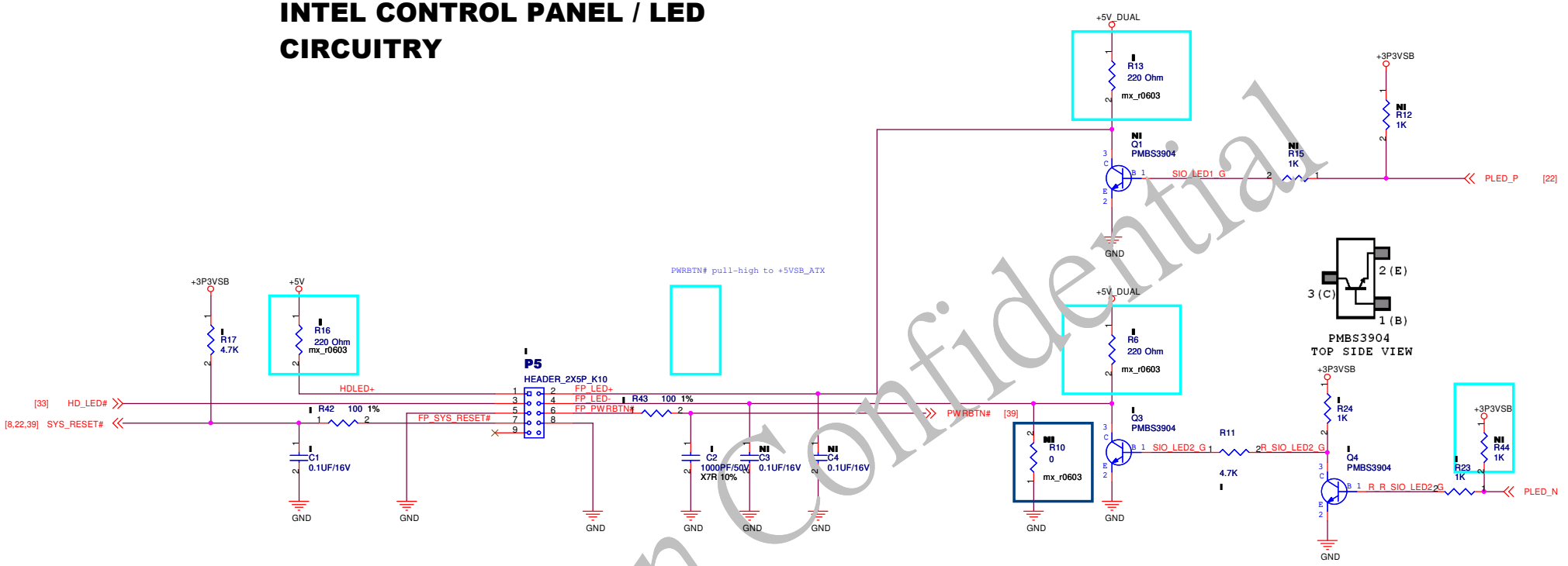
BAT54CW
TOP SIDE VIEW

BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : FAN CIRCUIT	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 41 of 54	

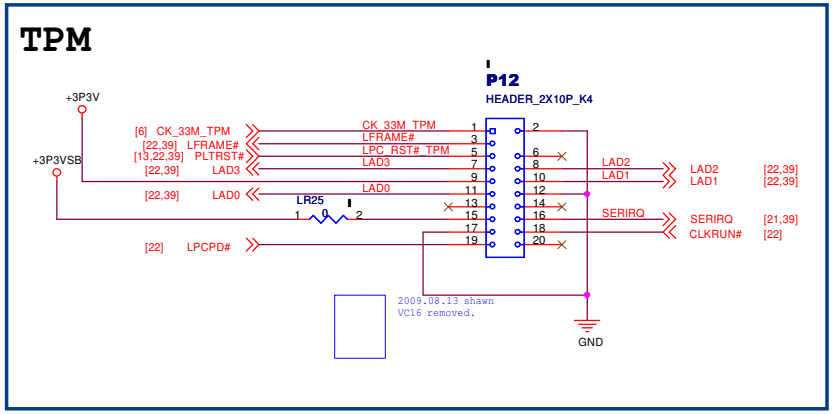
INTEL CONTROL PANEL / LED CIRCUITRY

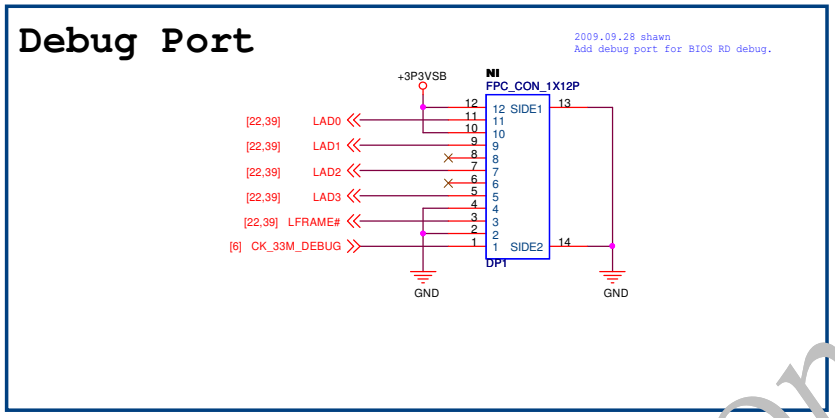


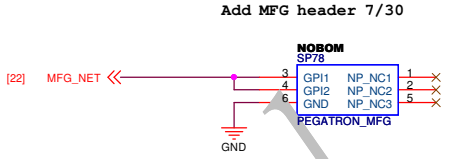
FRONT POWER LED COLOR SUPPORT	R10	Q2	R6	R11
SINGLE COLOR	I	NI	NI	NI
DUAL COLOR	NI	I	I	I

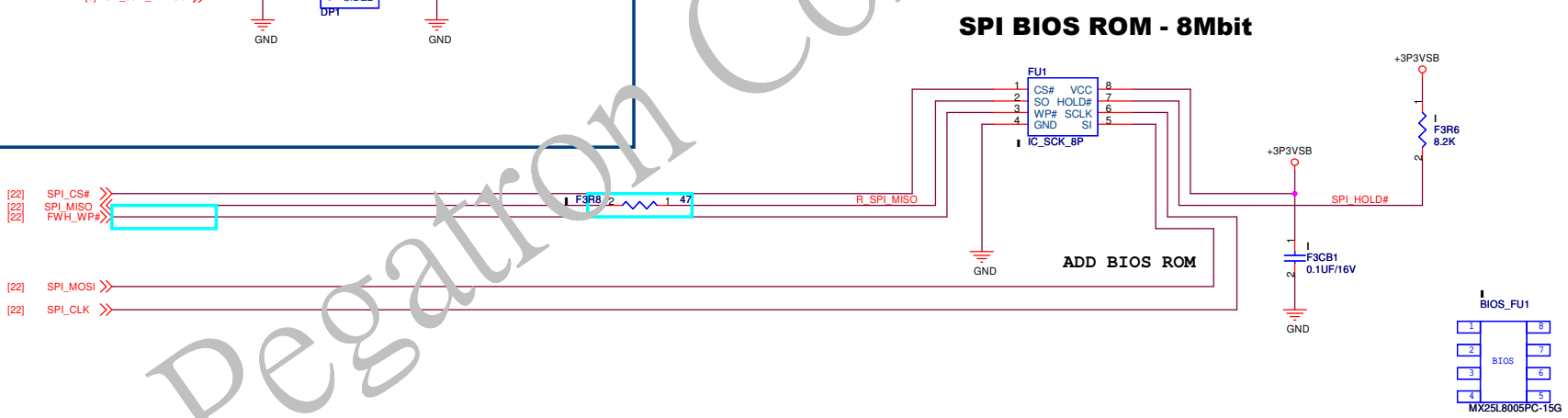
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : FRONT_PANEL	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 42 of 54	





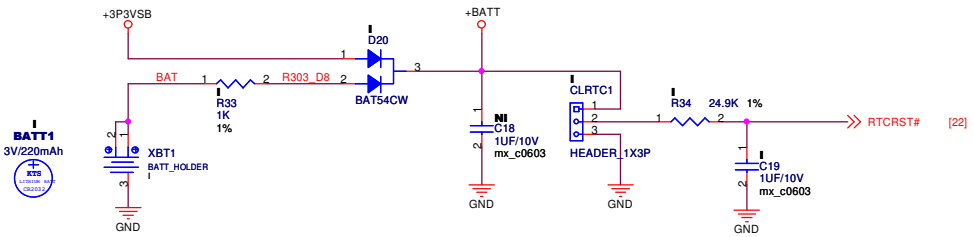




PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SPI FLASH - 8M	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 43 of 54	

External RTC Circuitry



Battery Socket

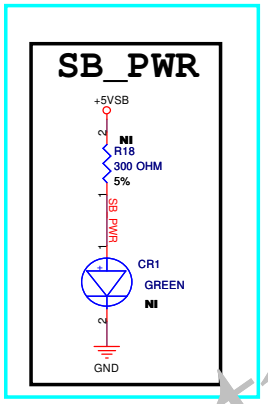
CLEAR CMOS

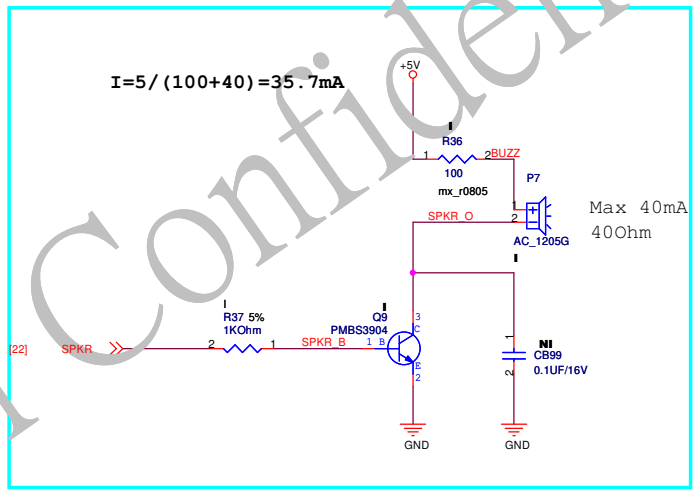
CLRTC1:12

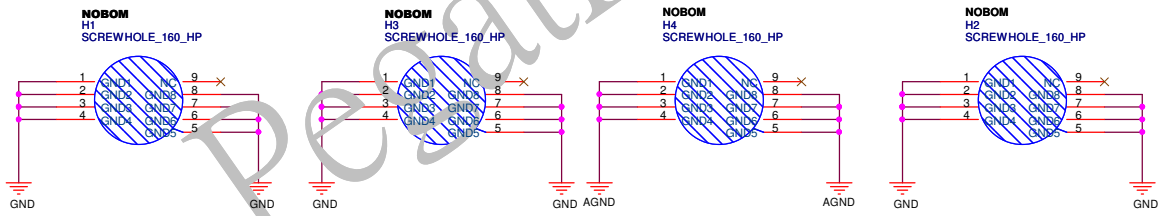
MINI_JUMPER

	CMOS RTC
1-2	Default
2-3	CLEAR

SPEAKER







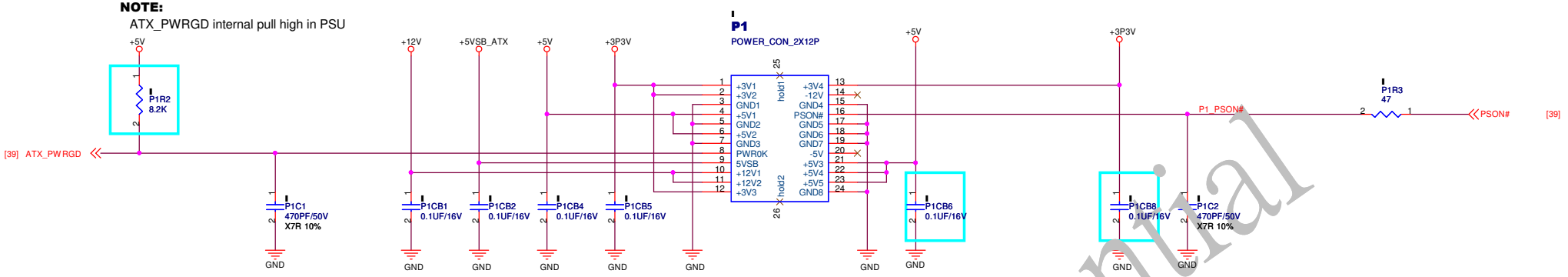
ONLY FOR SCREW HOLE

PEGATRON DT-MB RESTRICTED SECRET

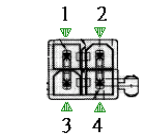
PEGATRON	Title : RTC / CMOS / SPKR	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 44 of 54	

ATX POWER_24P SUPPLY CONNECTOR

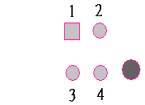
NOTE:
ATX_PWRGD internal pull high in PSU



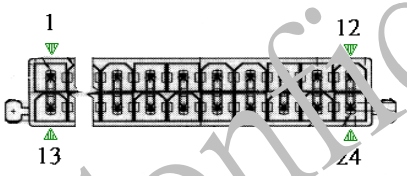
All of the Caps Around the ATX Power Connector



TOP SIDE VIEW



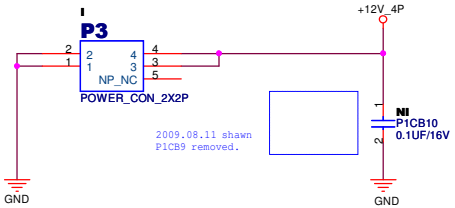
BOTTOM SIDE VIEW



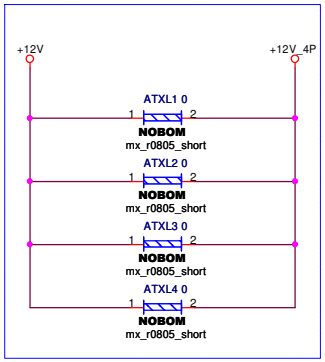
TOP SIDE VIEW

BOTTOM SIDE VIEW

VRM POWER_4P SUPPLY CONNECTOR

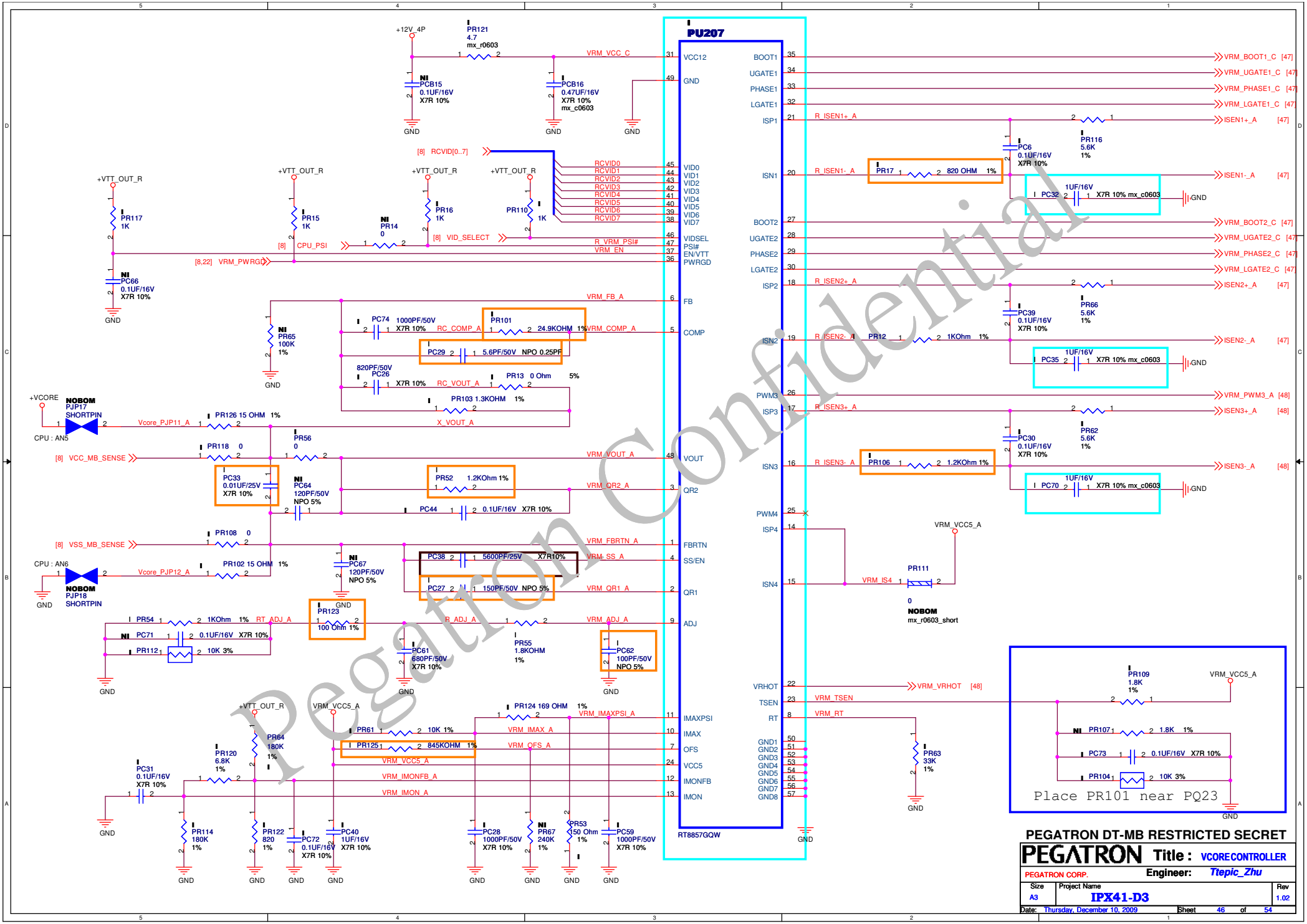


2009.08.04 shawn
→ Remove E70, E71 header and jumper
→ Add ATXL1 ~ 4 0805 short pin for keep the +12V trace width.



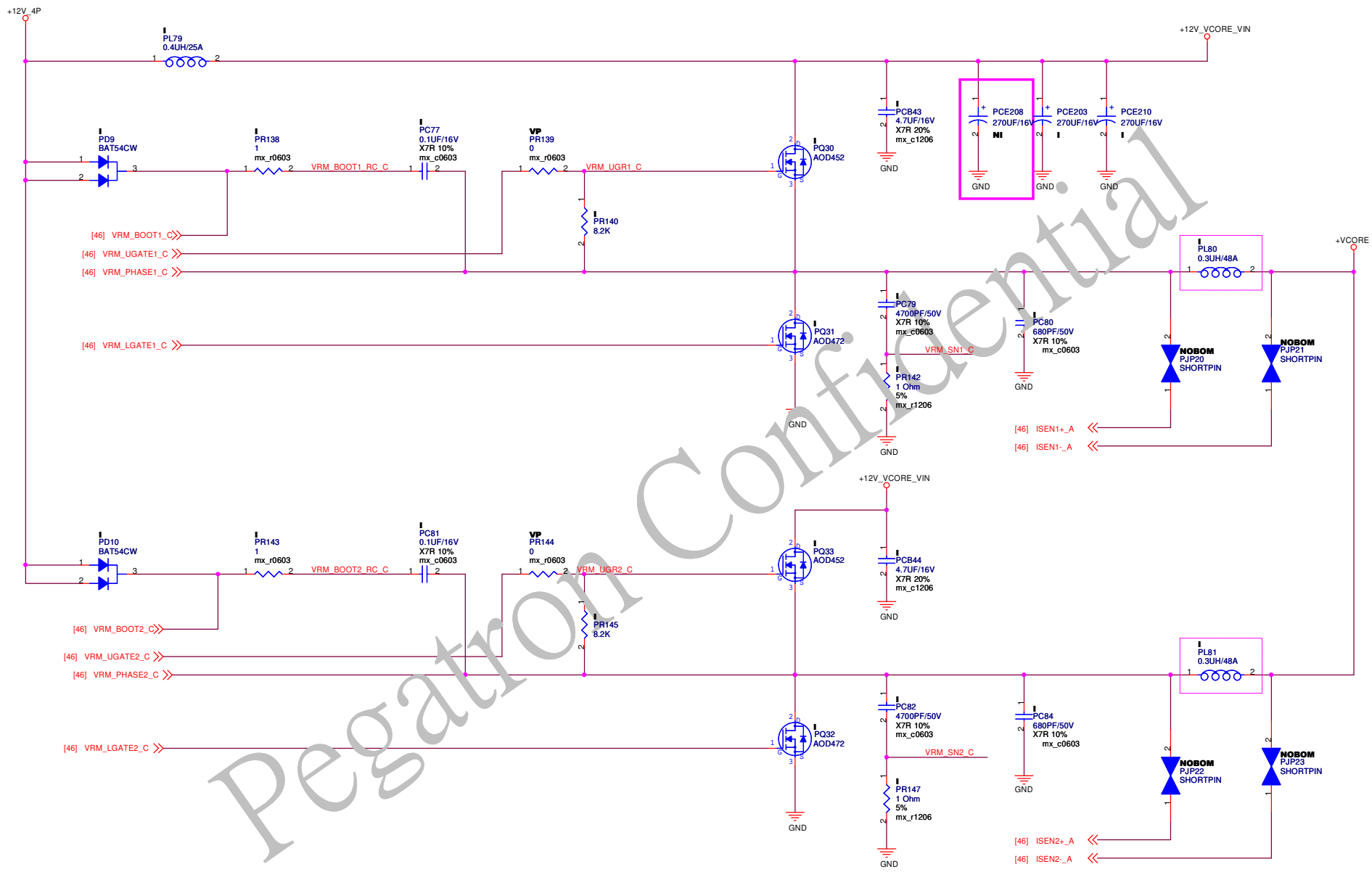
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : ATX POWER	
PEGATRON CORP.	Engineer: Ttepic Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 45 of 54	



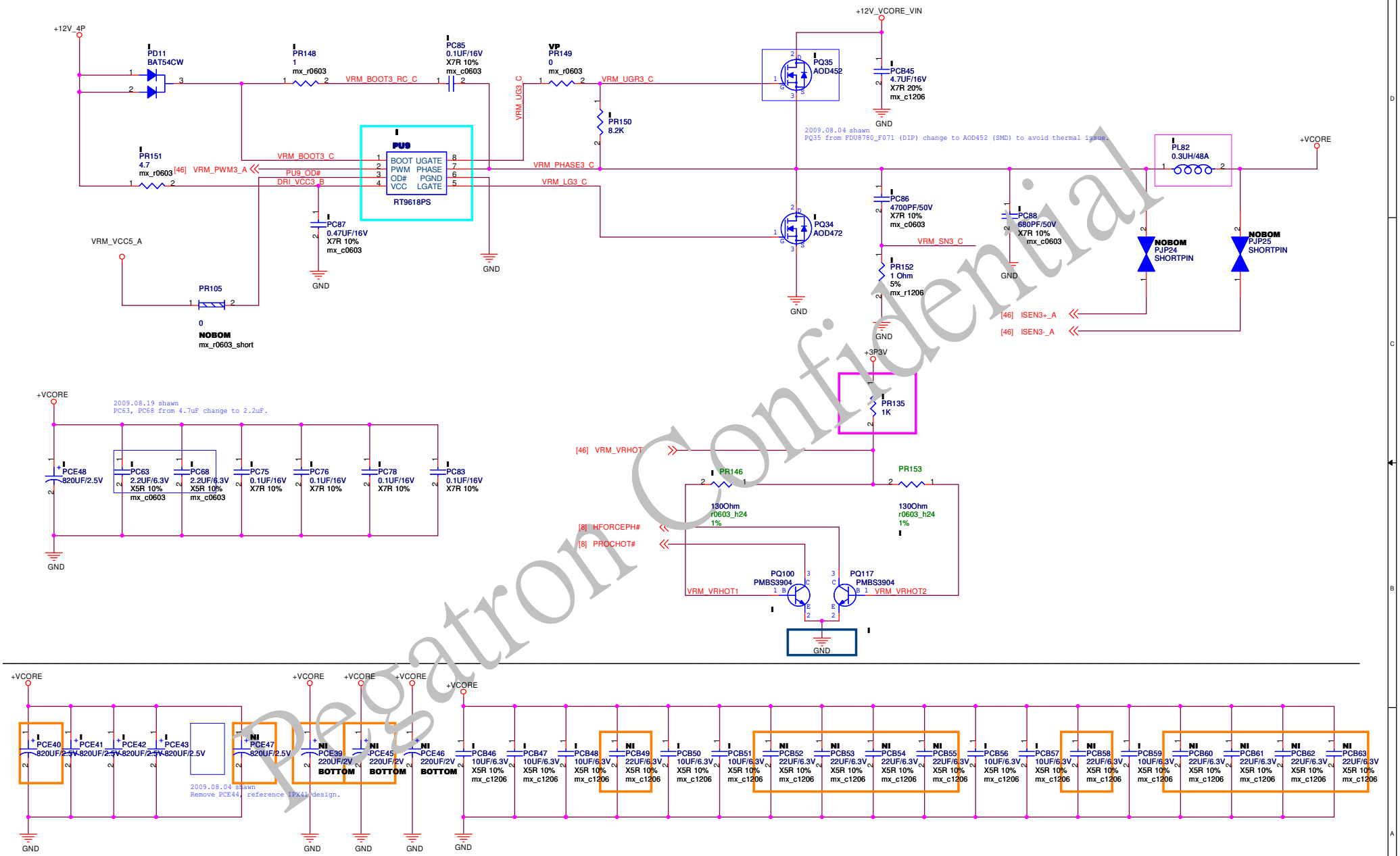
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VCORECONTROLLER	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 46 of 54	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VCOREDRIVER-1	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 47 of 54	



+CPU VCORE OUTPUT CAPs

11X23A106150

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VCOREDRIVER-2	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 48 of 54	

+3P3V ==> +1P1V_CORE (10A)

2009.08.04 shawn
Remove input voltage +12V option.

+3P3V
PL7
1UH/22A 0.2
+3P3V_VIN
PCB39
0.1UF/16V
X7R 10%
GND
PC52
X5R 10%
10UF/6.3V
mx_c0805
PCE25
560UF/6.3V
2009.08.11 shawn
PCE25 from EL CAP 1800u/6.3V change to PL CAP 560u/6.3V for layout space issue.

1P1V_HG_D
NOBOM
PR93
0
mx_r0603_short
1P1V_HGR_D
PQ25
AOD452
2009.08.04 shawn
PQ25 from FDU8780_F071 (DIP) change to AOD452 (SMD)
PR94
8.2K

Please this shortpin close to
low-side MOSFET drain pin

+1.1V
+1P1V_CORE
PL8
1.2UH/29A
PC53
4700PF/50V
X7R 10%
mx_c0603
NI
PC54
680PF/50V
X7R 10%
PCE27
1500UF/6.3V
PCE28
1500UF/6.3V
PC55
10UF/6.3V
X5R 10%
mx_c0805

NOBOM
PJP9
SHORTPIN
1P1V_OCSET_R
2009.08.04 shawn
PQ27 from IPS06N03LAG (DIP) removed
+1P1V_SN_C
PQ26
AOD452
2009.08.04 shawn
PQ26 from IPS06N03LAG (DIP) change to AOD452 (SMD)
modify 8/1
PJP10
SHORTPIN
NOBOM

+12V
PR95
4.7
mx_r0603
PR96
8.2K
PR97
1
mx_r1206
PD8
BAT54CW
1P1V_VCC_C
PR98
17.4KOHM
1%
OCP Point: 49.8A
PC56
0.1UF/16V
X7R 10%
mx_c0603

PU8
APW7120
1P1V_BST_C
1P1V_HG_D
1P1V_LG_D
BOOT PHASE
UGATE OCSET
GND FB
LGATE VCC
1P1V_PHASE_C
1P1V_OCSET_A
1P1V_FB_C
1P1V_VCC_C

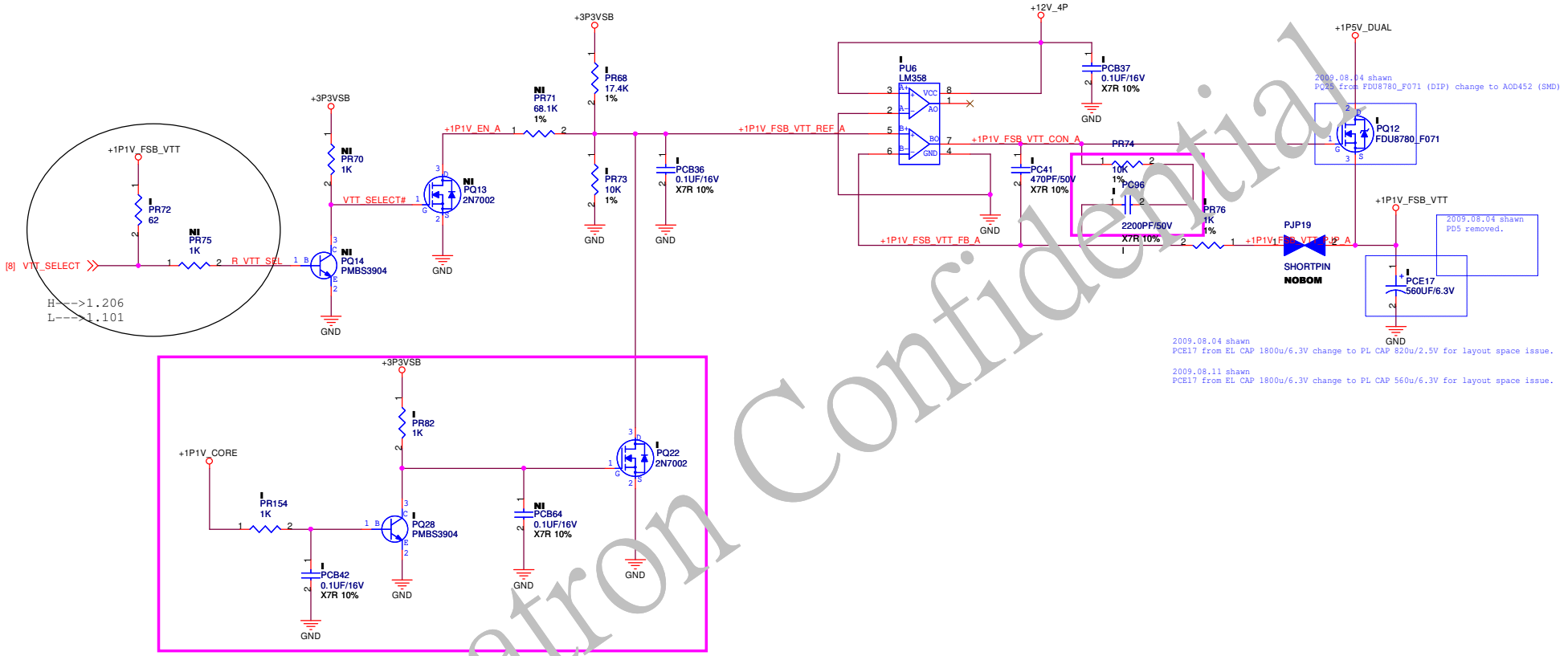
PR99
750 OHM
1%
1P1V_FB1_C
PC57
0.47UF/16V
mx_c0603
X7R 10%
PR100
1.96K
1%
NI
PC58
0.47UF/16V
X7R 10%
mx_c0603

+5VSB
PR130
1K
1P1V_OCSET_A
+3P3V
PR158
1K
PQ40
PMBS3904
PQ41
PMBS3904
NI
PCB71
0.1UF/16V
X7R 10%
PR157
619 OHM
1%
PCB70
0.1UF/16V
X7R 10%

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +1P1V_CORE	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 49 of 54	

+1P5V_DUAL ==> +1P1V_FSB_VTT (1.5A)

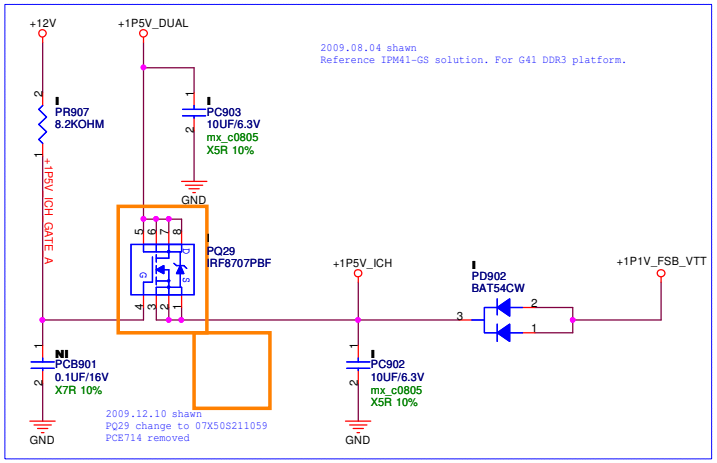


PEGATRON DT-MB RESTRICTED SECRET

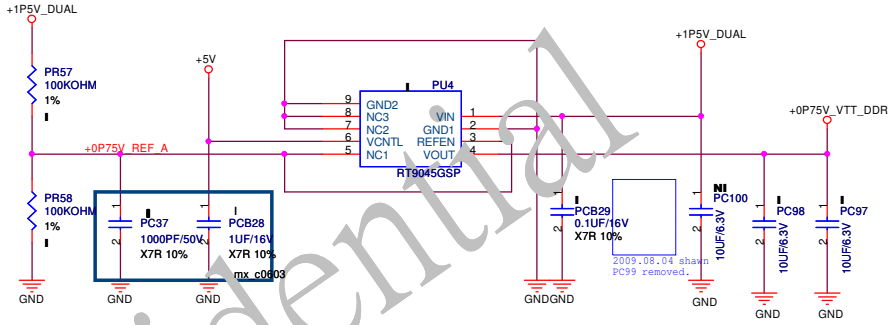
PEGATRON	Title : +1P1V_FSB_VTT_LDO	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 50 of 54	

+1P5V_DUAL ==> +1P5V_ICH (2A)

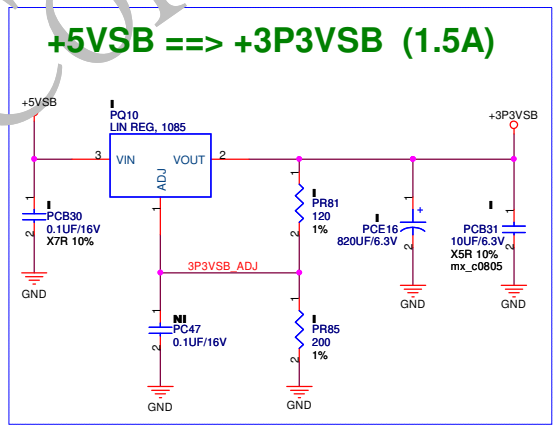
+1P5V_ICH (2A) For G41 DDR3 Platform



+1P5V_DUAL ==> +0P75V_VTT_DDR (2A)



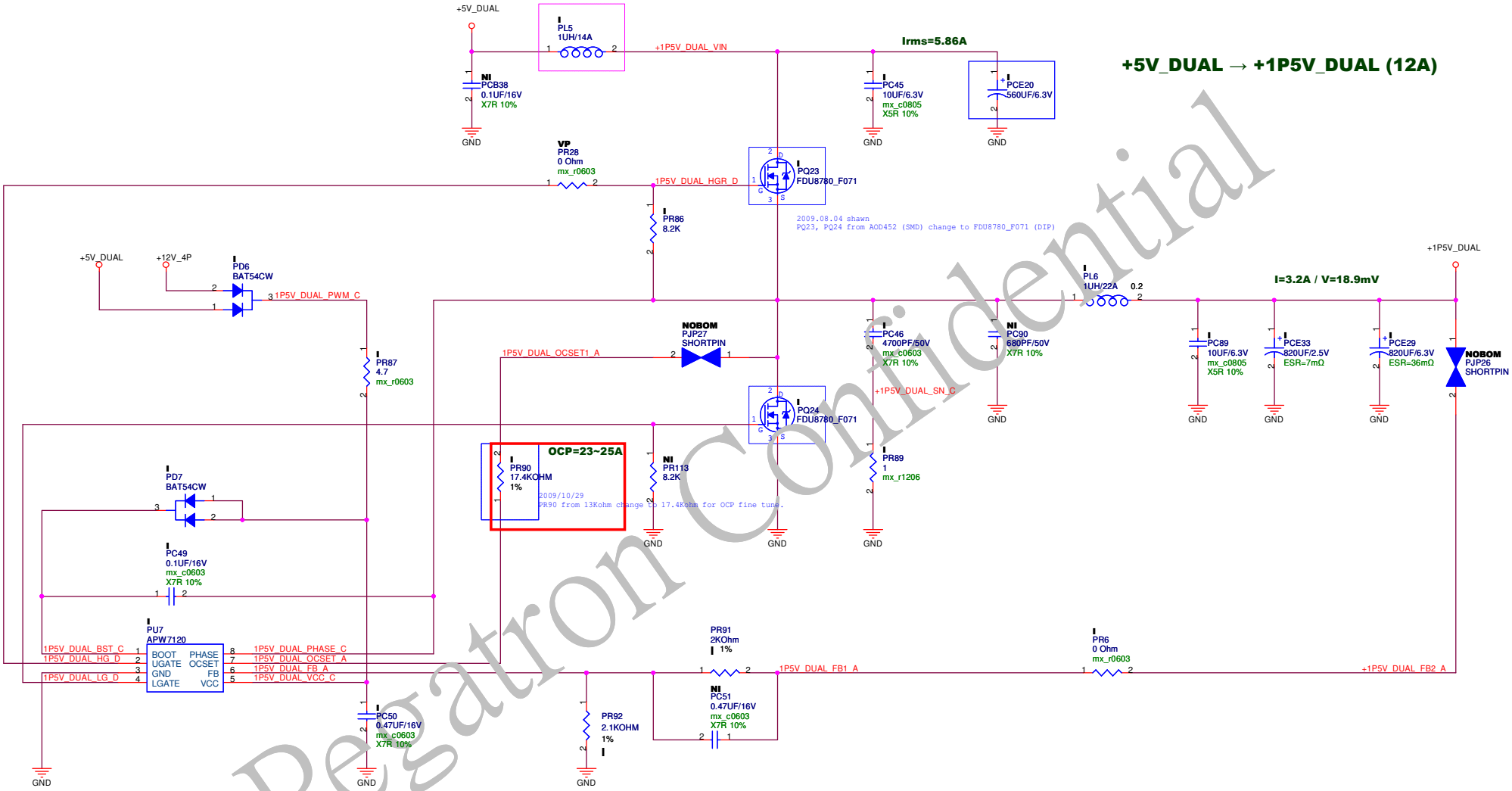
+5VSB ==> +3P3VSB (1.5A)



2009.08.04 shawn
→ Removed switch regulator solution.
→ Add Linear regulator solution.

PEGATRON DT-MB RESTRICTED SECRET

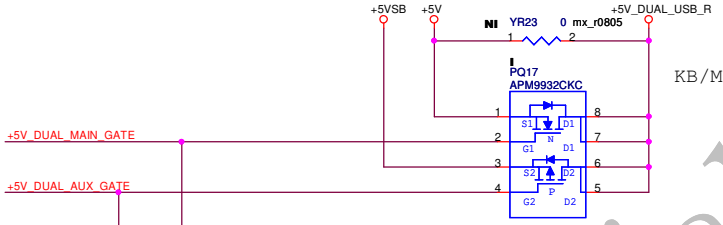
PEGATRON	Title : +0P9V_VTT_DDR_LDO	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 51 of 54	



PEGATRON DT-MB RESTRICTED SECRET

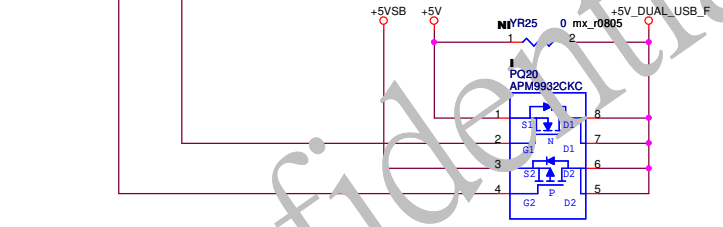
PEGATRON	Title : +1P5V_DUAL_SW	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 52 of 54	

+5V_DUAL_USB_R.....3A



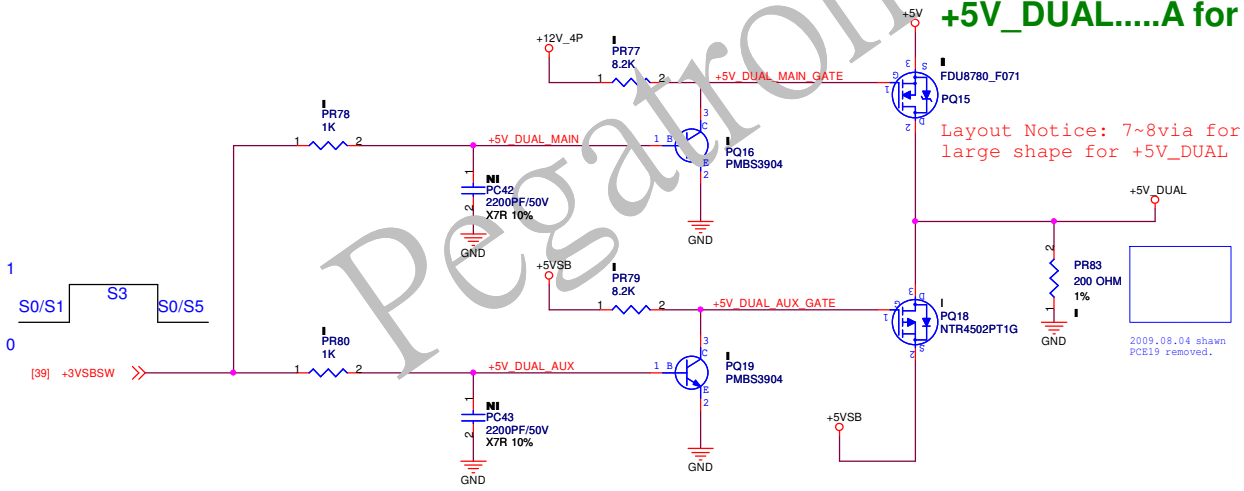
KB/MS connect to +5V_DUAL_USB_R

+5V_DUAL_USB_F.....3A



Layout Notice: 3~4via for +5V, 2via for +5VSB,
large shape for +5V_DUAL

+5V_DUAL.....A for DRAM



Layout Notice: 7~8via for +5V, 2via for +5VSB,
large shape for +5V_DUAL

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +1P1V_FSB_VTT_LDO	
PEGATRON CORP.	Engineer: Ttepic_Zhu	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 53 of 54	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +3P3V_PCIE&+3P3V_LAN	
PEGATRON COMPUTER INC	Engineer: Hemine_He	
Size: A3	Project Name: IPX41-D3	Rev: 1.02
Date: Thursday, December 10, 2009	Sheet 54 of 54	