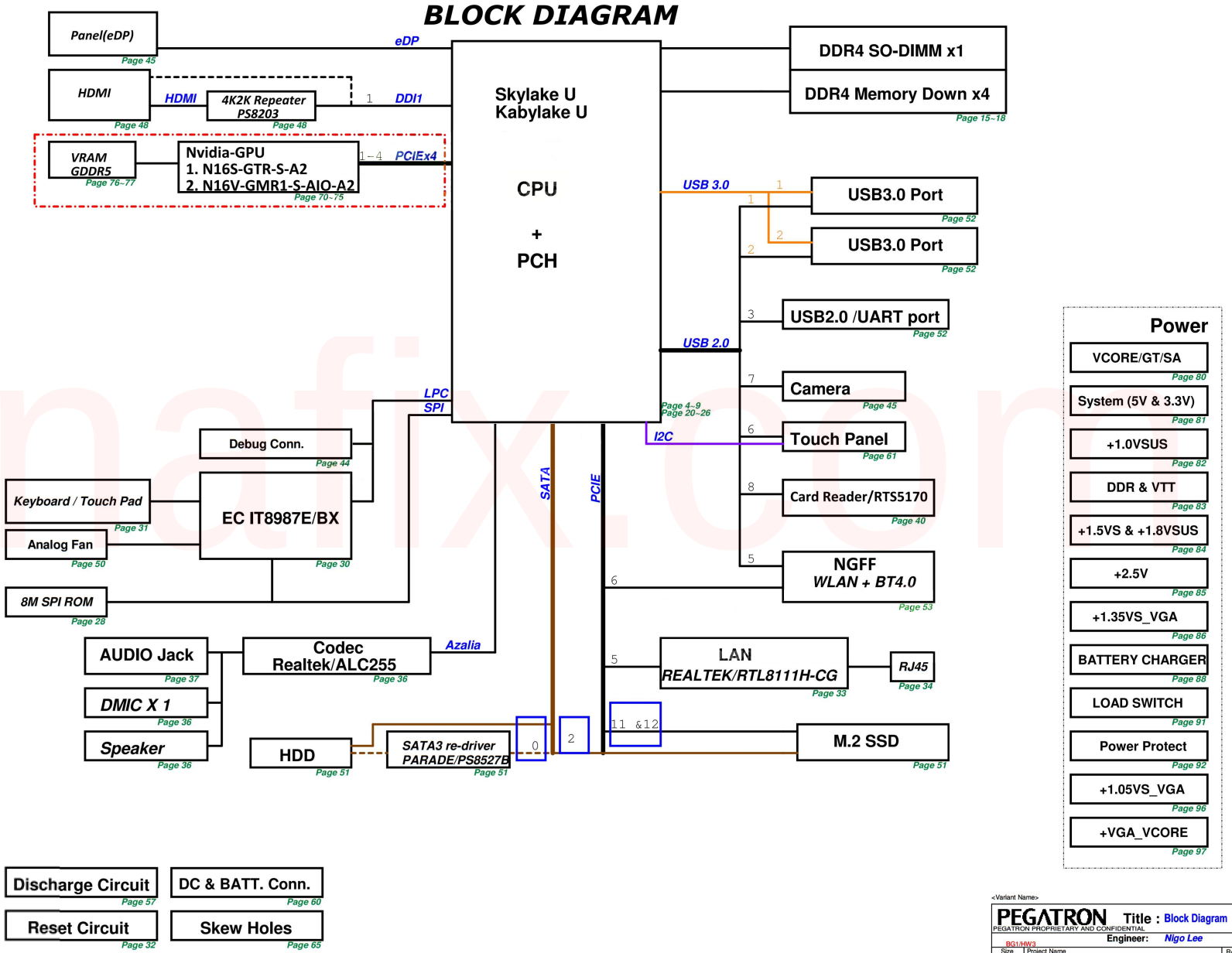
EJ4DA Skylake U / EJRDA Kabylake U

(2+2) Rev2.0 2016/09/02

SYSTEM PAGE REF.

BLOCK DIAGRAM



<Variant Name>

PEGATRON Title : Block Diagram

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Engineer: Nigo Lee

BG1/HW3

Size	Project Name	Rev
Custom	EJ14	1.3

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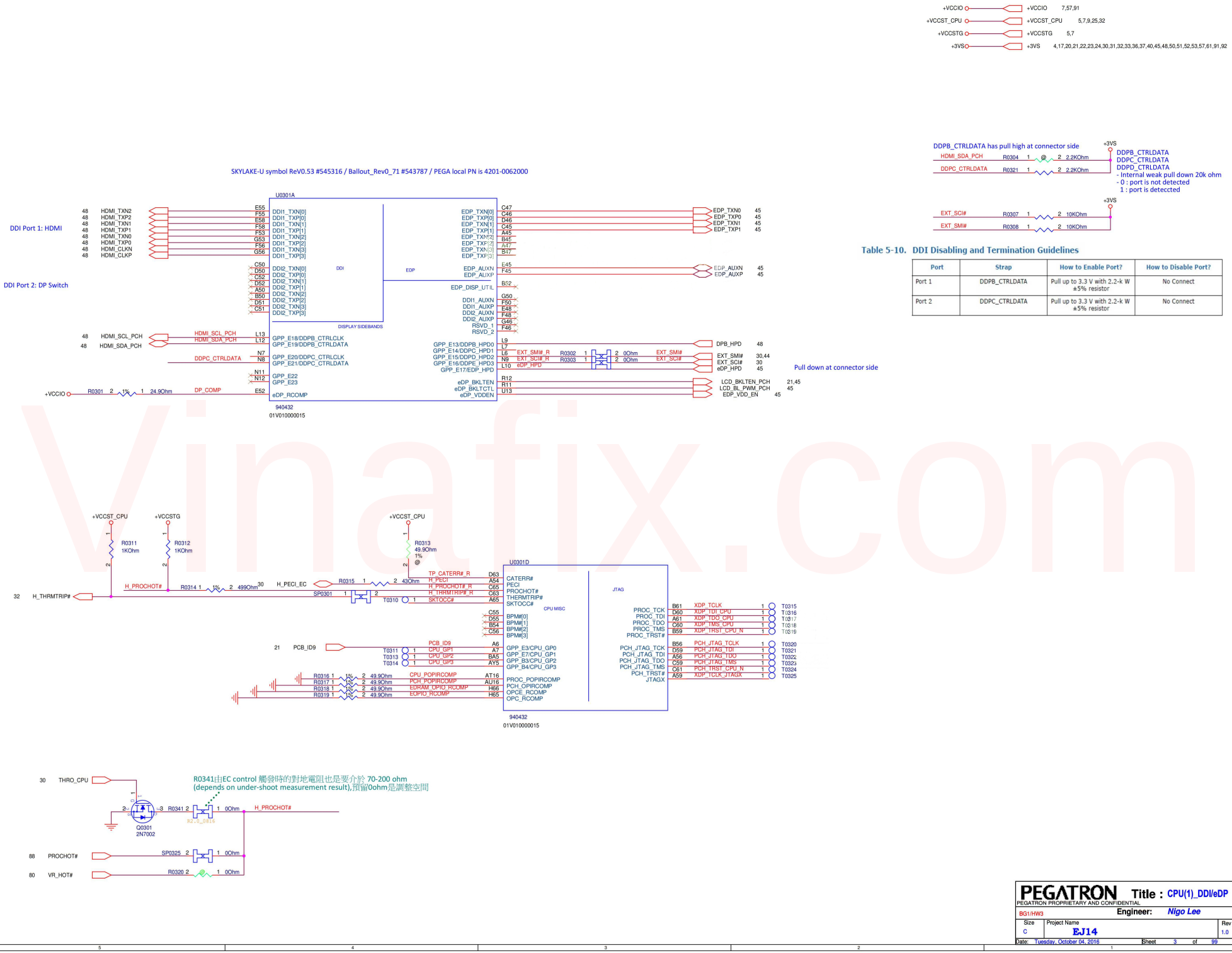

Table 5-10. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect

PEGATRON
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Title : CPU(1)_DDI/eDP
BG1/HW3
Engineer: Nigo Lee
Size C | Project Name EJ14 | Rev 1.0
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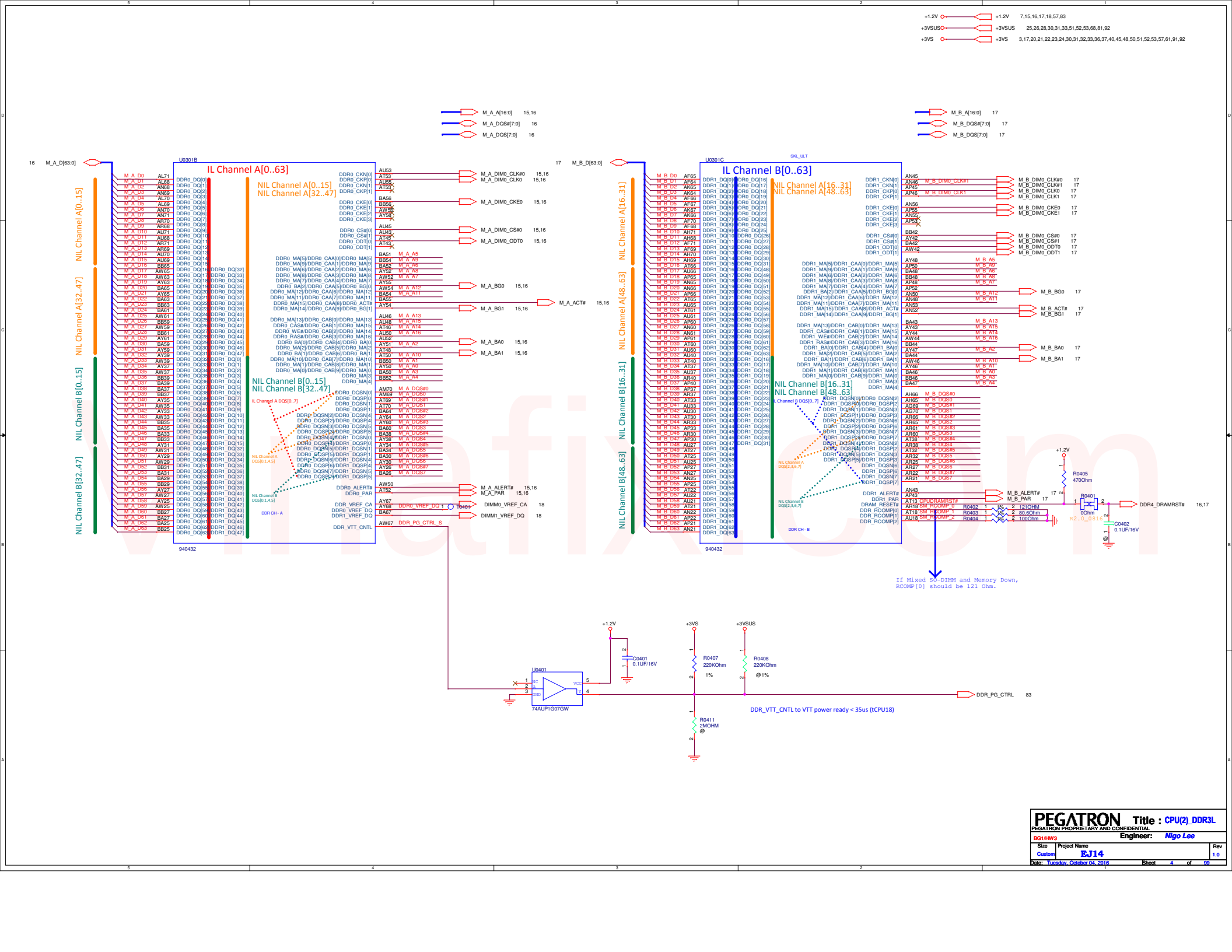

Title : CPU(2)_DDR3L

BG1/HW3

Engineer: Nigo Lee

Size	Project Name	Rev
Custom	EJ14	1.0

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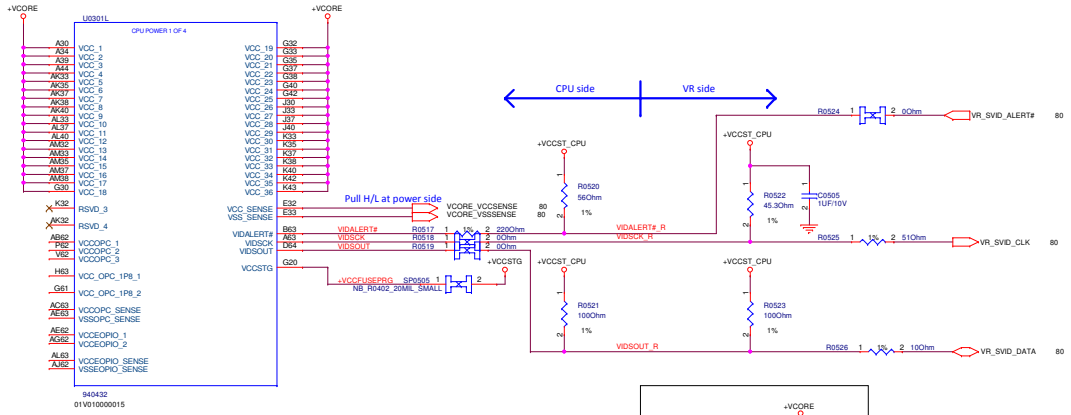
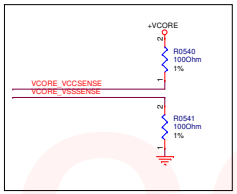
+VCORE +VCORE 57,80

+VCCSTG +VCCSTG 3,7

+VCCST_CPU +VCCST_CPU 3,7,9,25,32





Intel Backside Cap:
9 x 22uF
7 x 10uF
15 x 1uF

Change to Power Side

Intel Primary side Cap:
8 x 47uF
8 x 10uF

Change to Power Side

Vinafix

PEGATRON Title :CPU(3)_+VCCCORE

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1HW3 Engineer: Nigo Lee

Size: Custom | Project Name: EJ14 | Rev: 1.0

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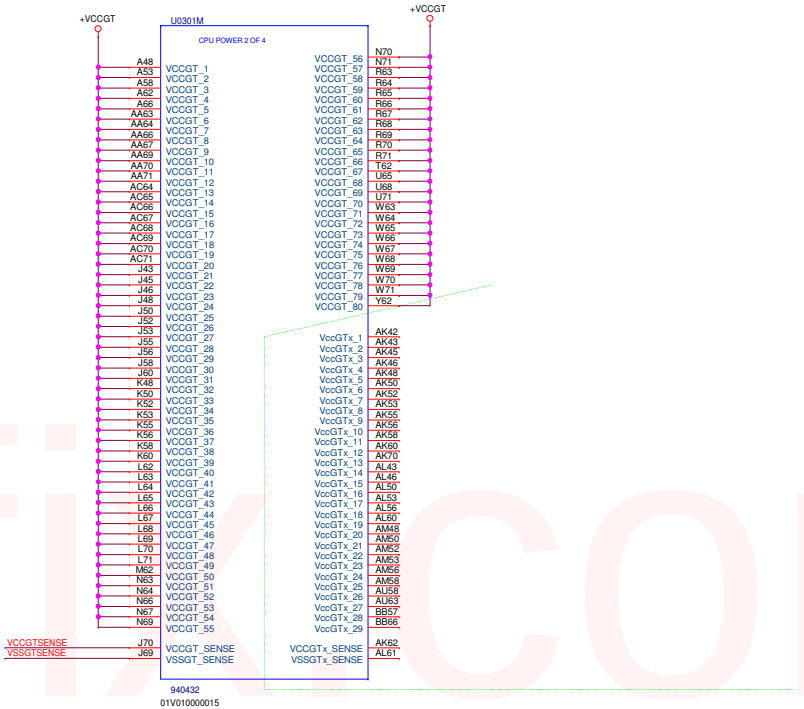
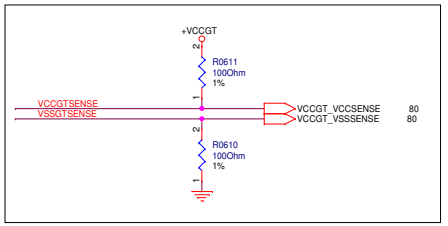
+VCCGT +VCCGT 57,80

Intel :
6 x 47uF
12 x 22uF
10 x 10uF
15 x 1uF

Change to Power Side





PEGATRON Title : CPU(4)_+VCCGT
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3 Engineer: Nigo Lee

Size	Project Name	Rev
C	EJ14	1.0

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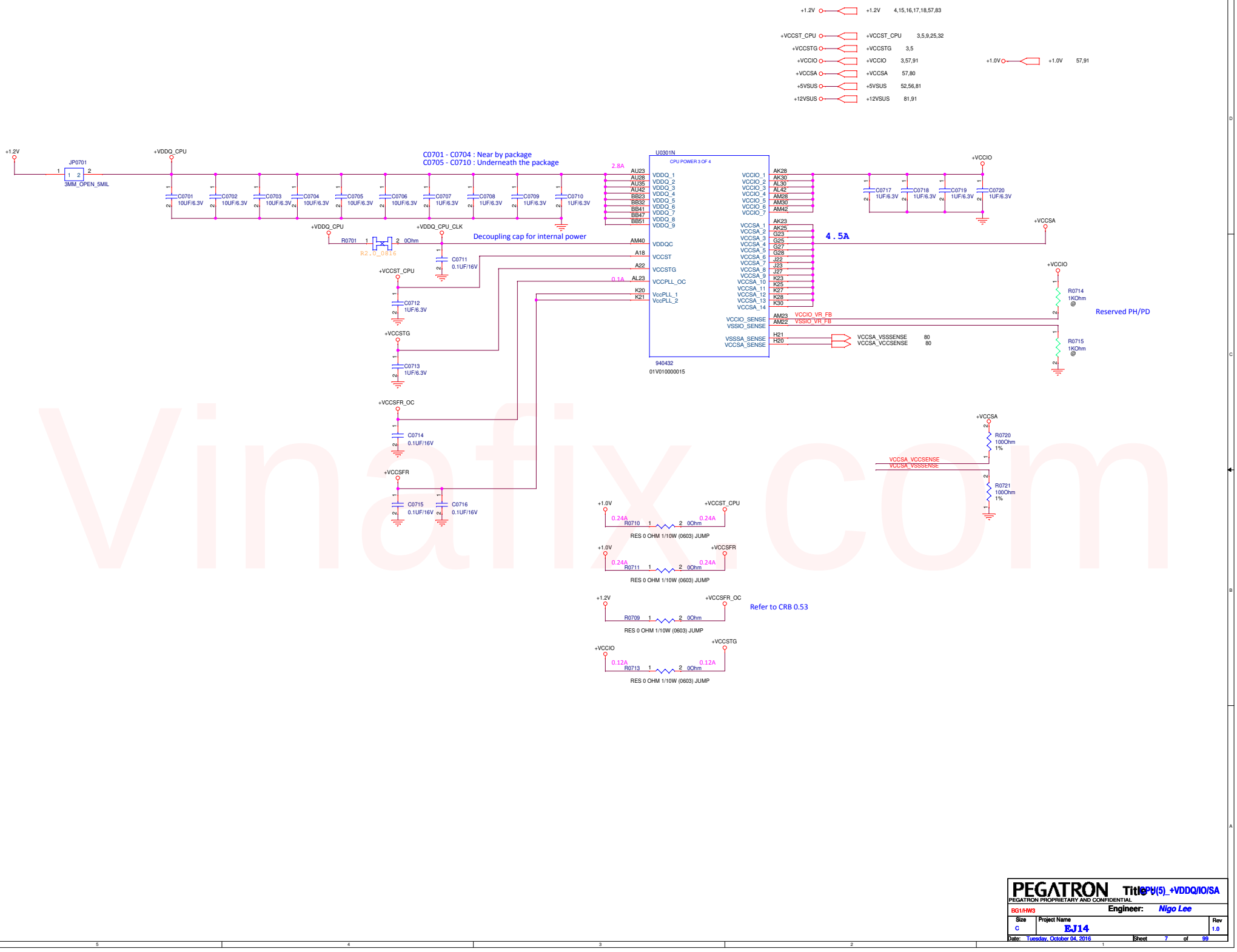

PEGATRON
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Title: PWR(5)_+VDDQ/IO/SA

Engineer: Nigo Lee

BG1/HW3

Size	Project Name	Rev
C	EJ14	1.0

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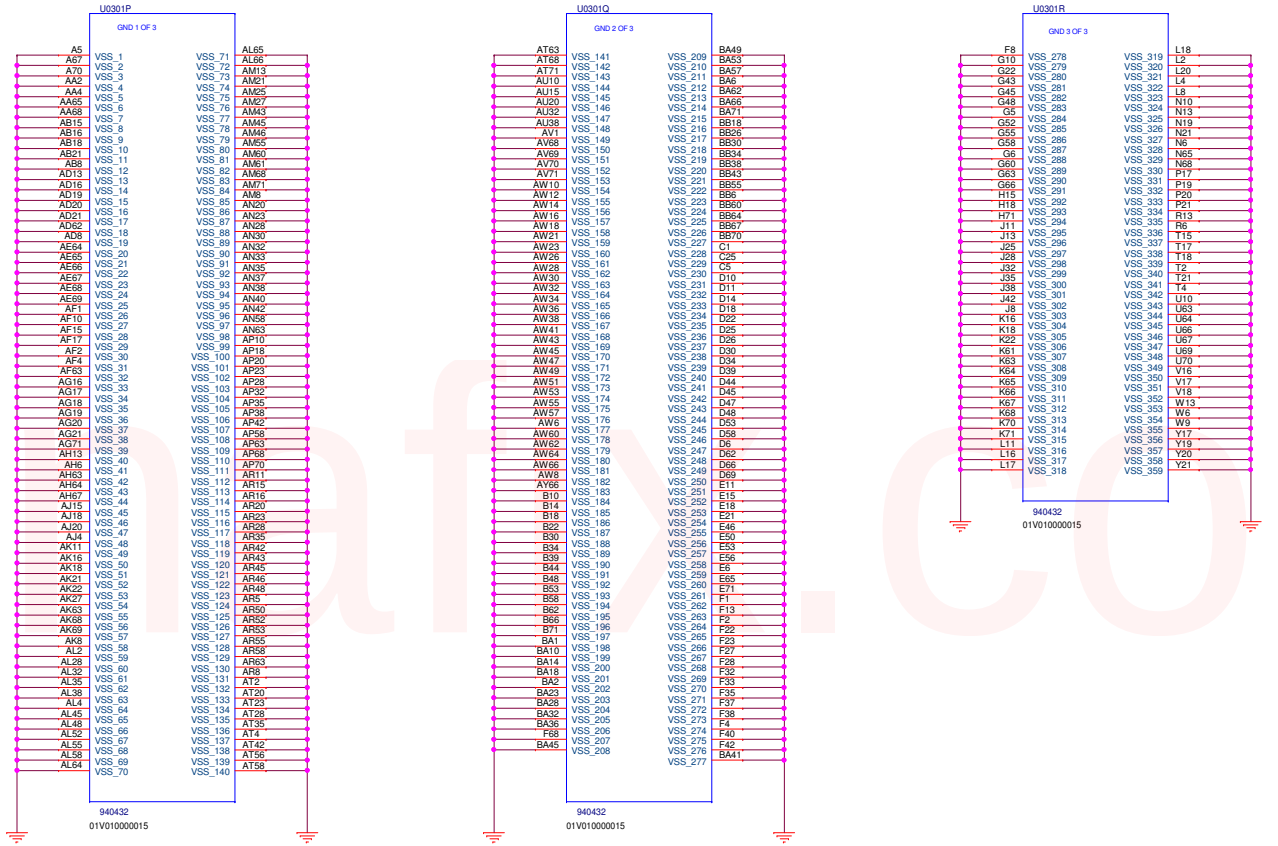

PEGATRON Title : CPU(6)_CPU GND

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Nigo Lee

Size	Project Name	Rev
C	EJ14	1.0

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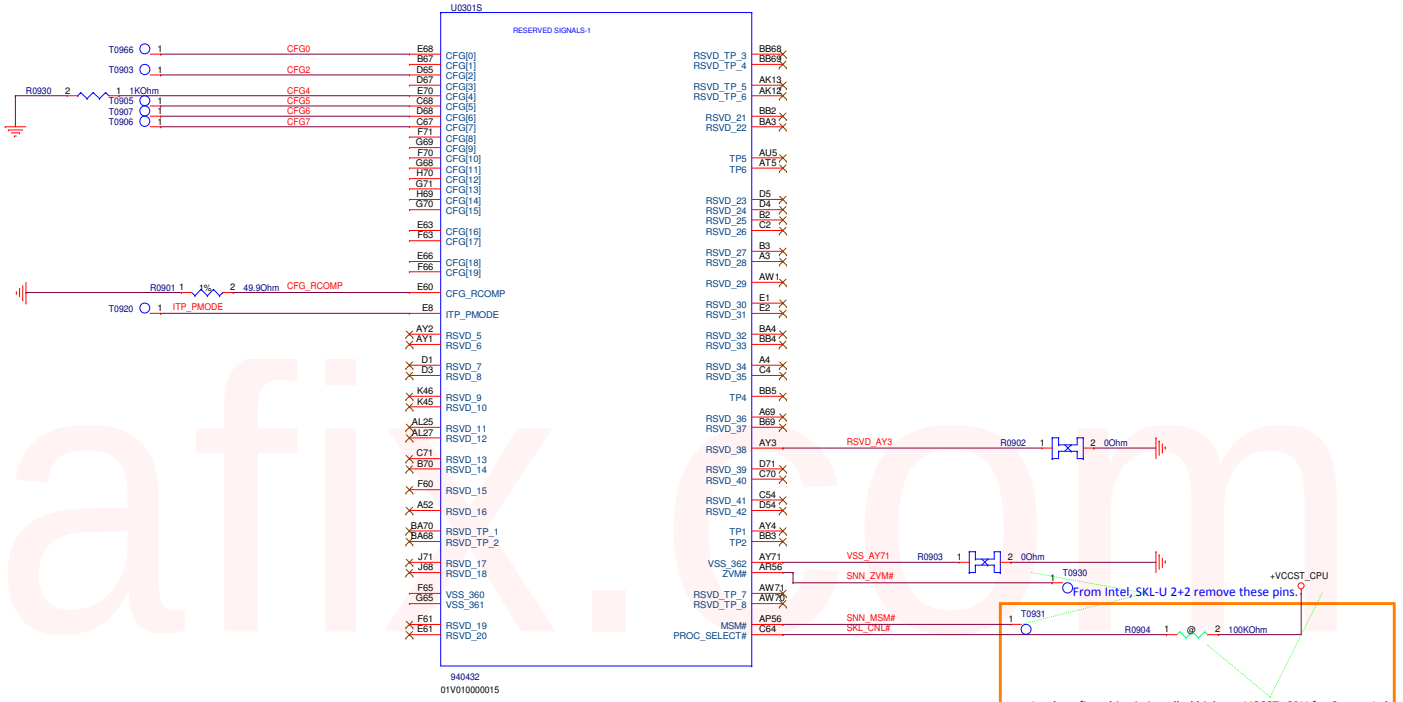
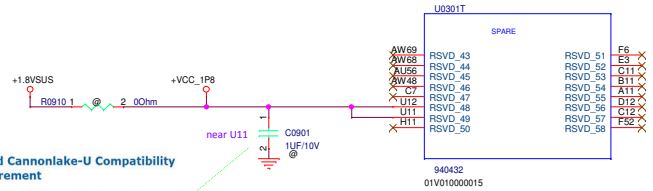
6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.





1.3.2 [U] Skylake-U and Cannonlake-U Compatibility Decoupling Requirement

MOW WW52

Two reserve pins (U11 and U12) for 1.8V were added to Skylake-U PCH to support Cannonlake-U PCH compatibility. For Skylake-U, the following changes will be made to Table 52-8 in the Skylake U/Y Platform Design Guide (IBP#543016).

Table 52-8 – Decoupling and Power Connection Requirement for Skylake-U PCH

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)emeny / (F)ixed	Place capacitor(s) near ball(s)
V1.8A	VccPGPPF	AF16	-	-	-	-	-
	VccATS	AA1	1 uF	0402	1	E (<10 mm)	AA1
	Vcc_1P8	U11, U12	1 uF	0402	1	E (<10 mm)	U11, U12 (Note 1 & 5)

+VCCST_CPU +VCCST_CPU 3,5,7,25,32
+1.8VSUS +1.8VSUS 24,26,84

PEGATRON Title : CPU(7)_CFG/RSVD
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BG1/HW3 Engineer: Nigo Lee
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Title	<Title>	
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Title	<Title>	
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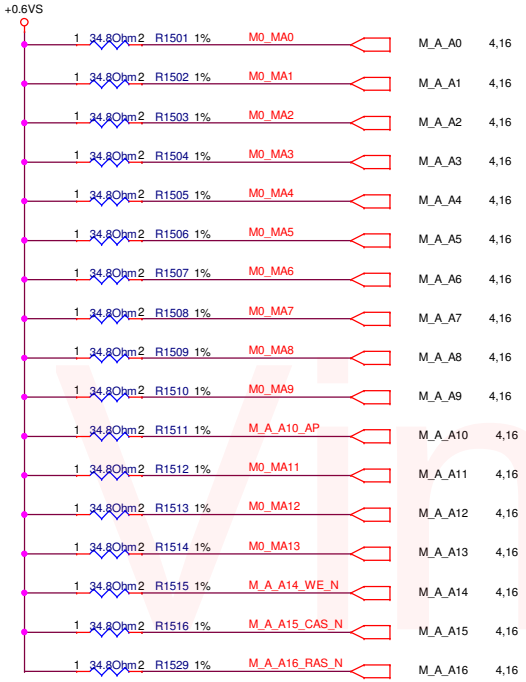
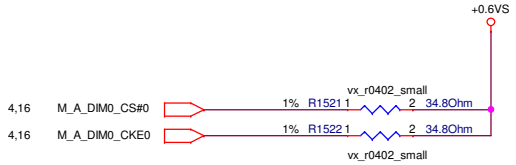
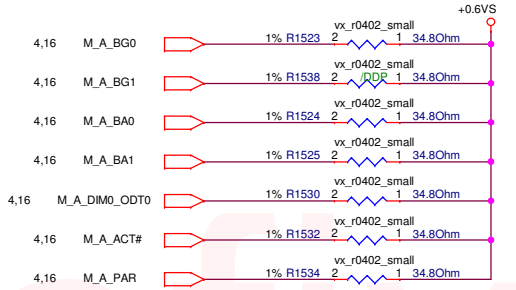
DDR4(0)_Termination

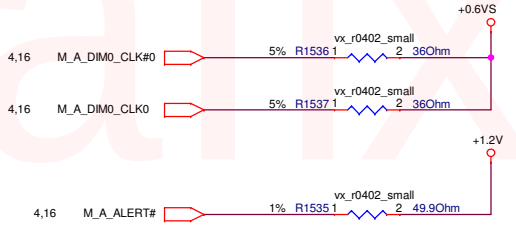
+0.6VS +0.6VS 17,57,83

+1.2V +1.2V 4,7,16,17,18,57,83

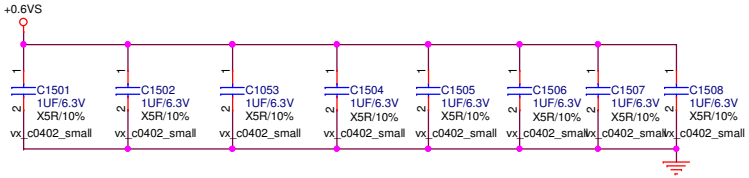


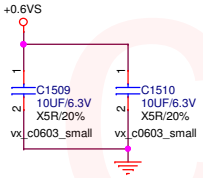






Average placed close to +VDDQ_VTT power plane





PEGATRON Title : DDR4(1)_Termination

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BG1/HW3 Engineer: Nigo Lee

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Custom	EJ14	1.0

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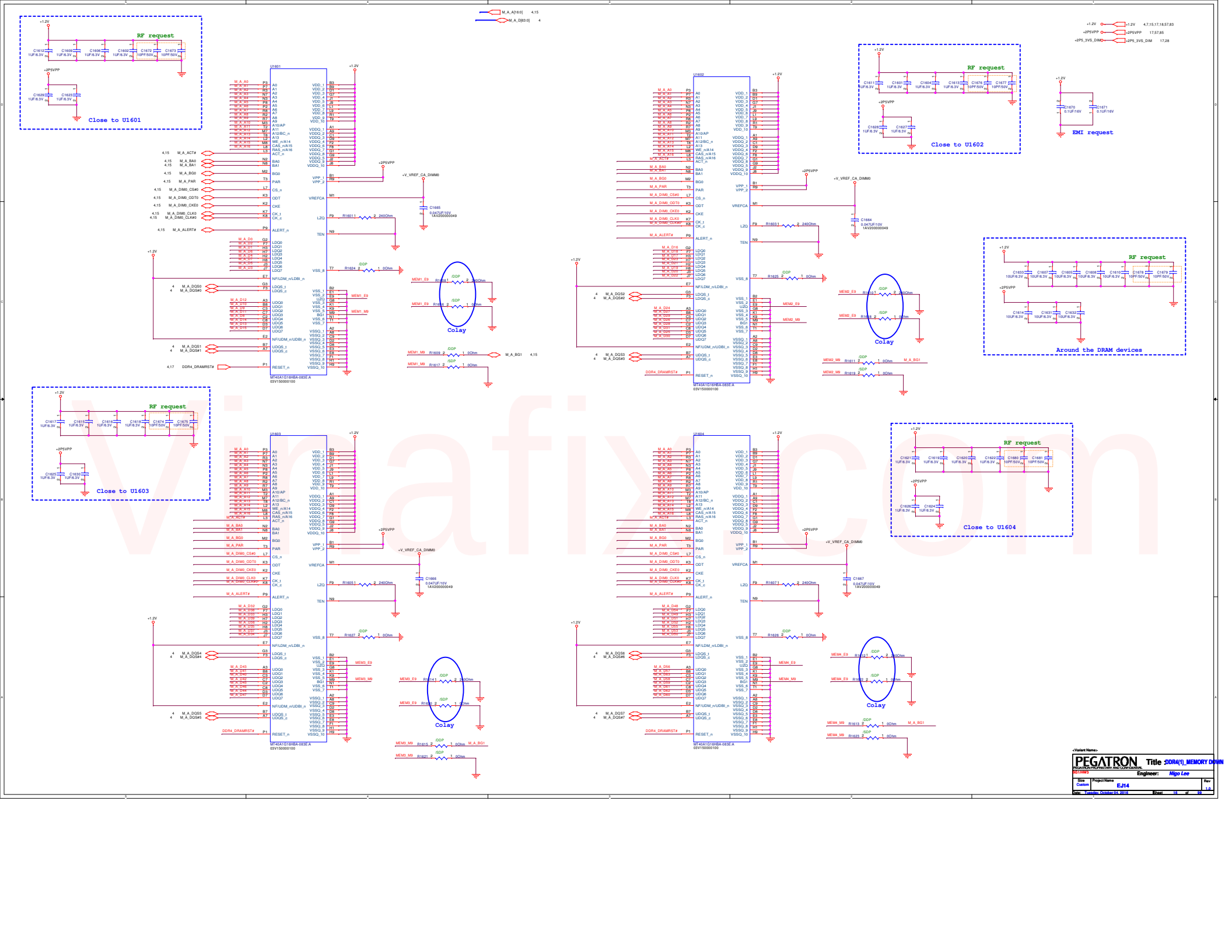
RF request
Close to U1601
Close to U1602
Close to U1603
Close to U1604
EMI request
Around the DRAM devices
Colay
U1601
U1602
U1603
U1604
MT40A1G16HBA-083E:A
03V150000100
+1.2V
+2PSVPP
+V_VREF_CA_DIMM0
DDR4_DRAMRST#
M_A_A[16:0]
M_A_D[63:0]
<Variant Name>
PEGATRON
Title : DDR4(1)_MEMORY DOWN
Engineer: Nigo Lee
Size: Custom
Project Name: EJ14
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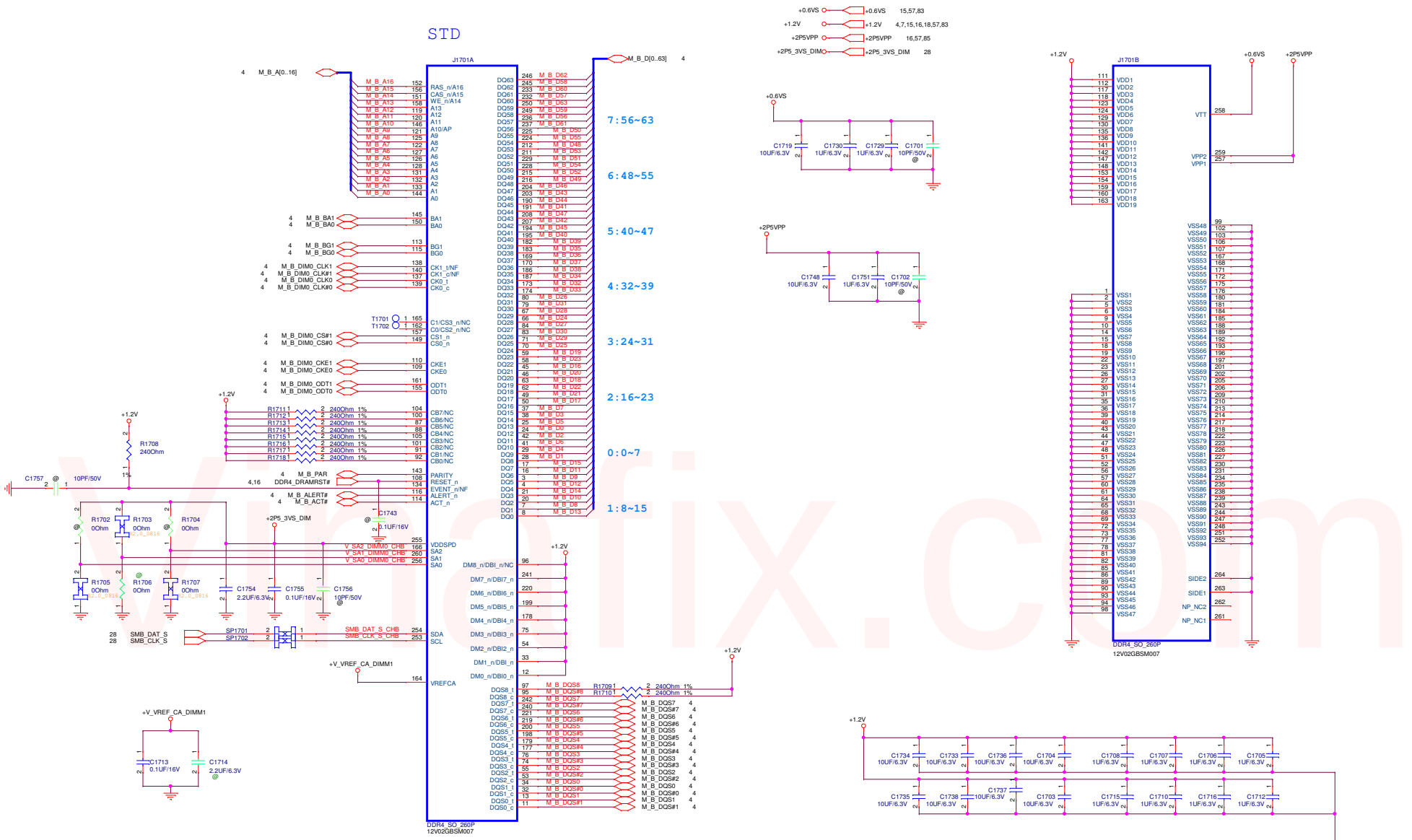

Table 4-52. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

Notes:
1. Total quantity is referring to 2 channels.

<Variant Name>

PEGATRON Title DDR4(1)_SO-DIMM0
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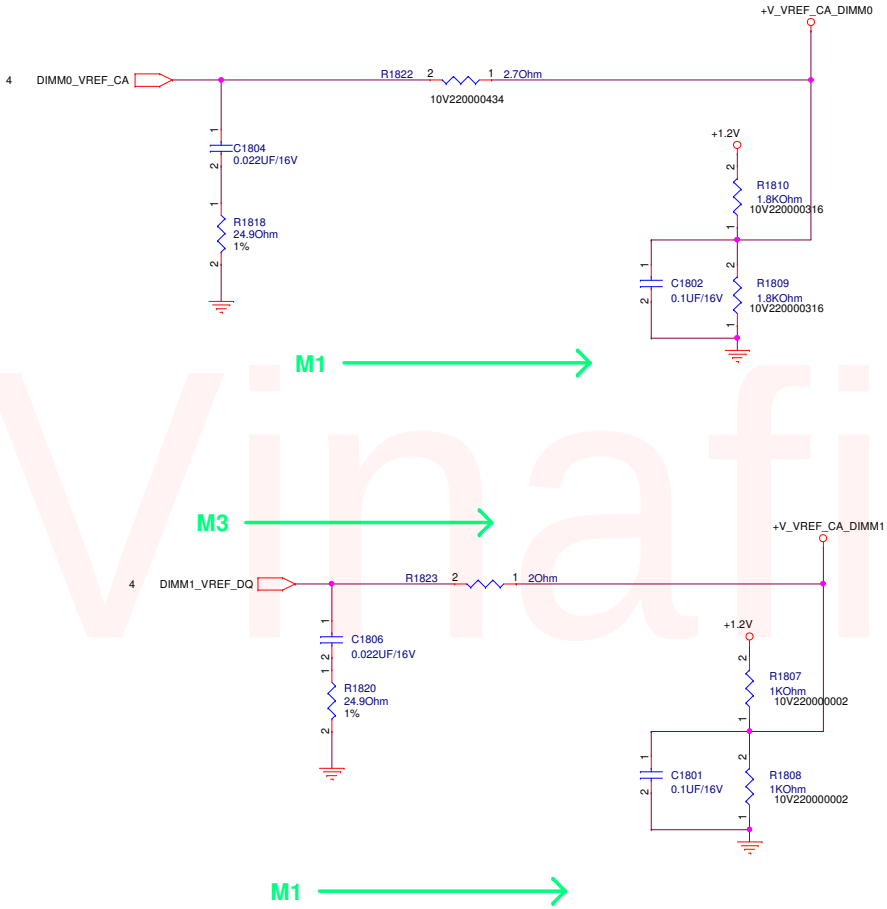
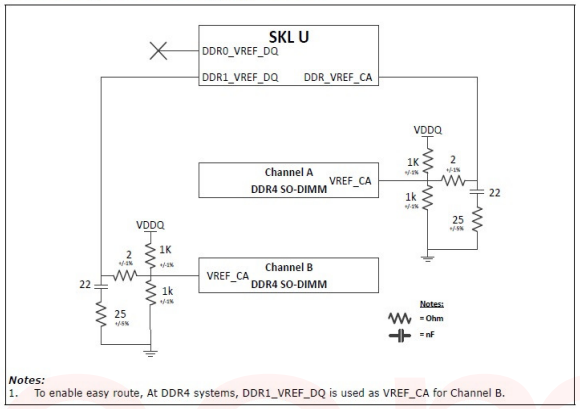
M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



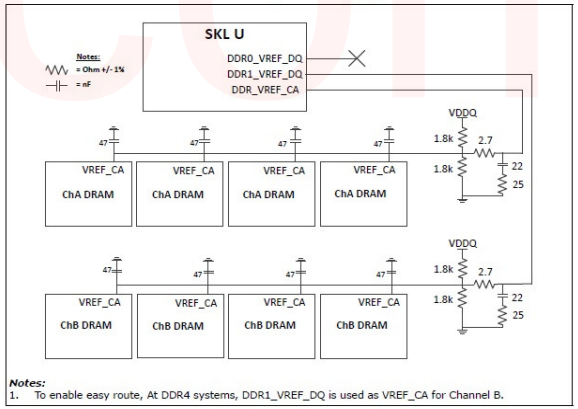
+1.2V		+1.2V	4,7,15,16,17,57,83
+V_VREF_CA_DIMM0		+V_VREF_CA_DIMM0	16
+V_VREF_CA_DIMM1		+V_VREF_CA_DIMM1	17

Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

<Variant Name>

PEGATRON
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Title: DDR3(3)_CA/DQ Voltage
Engineer: Nigo Lee

BG1/HW3
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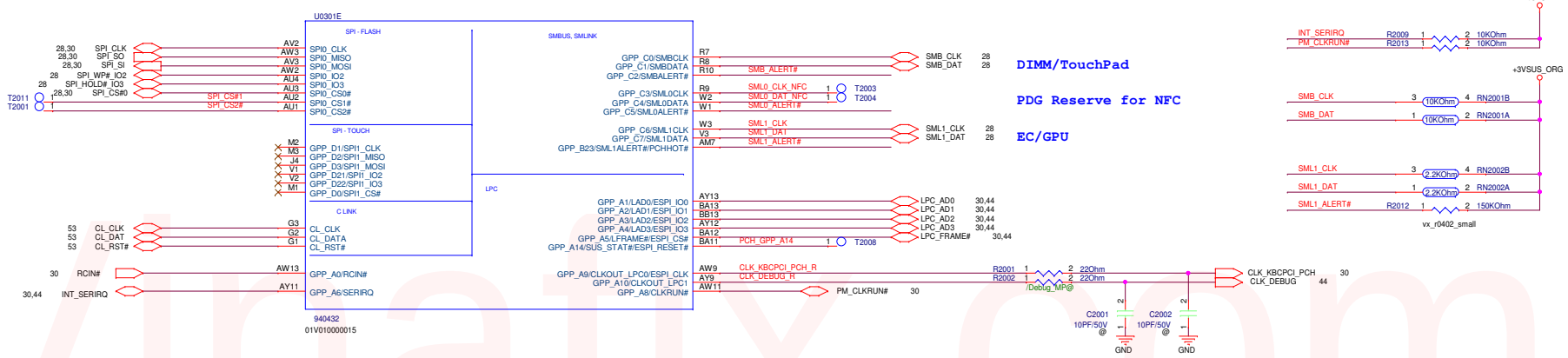

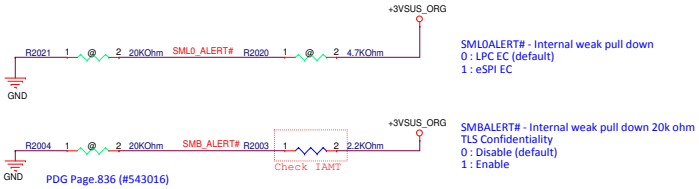

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SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

<Variant Name>

PEGATRON Title : PCH(1)_SMB,LPC

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Engineer: Nigo Lee

BG1/HW3

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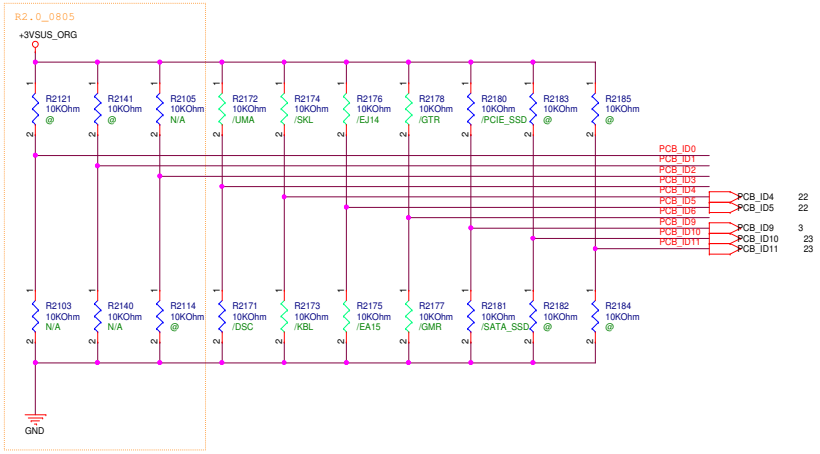
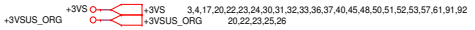
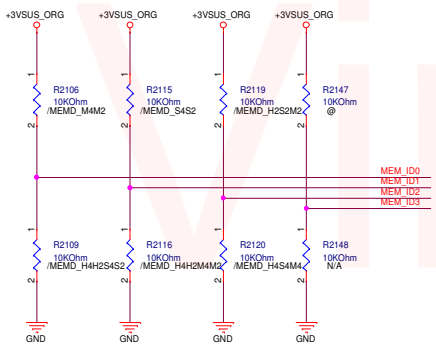


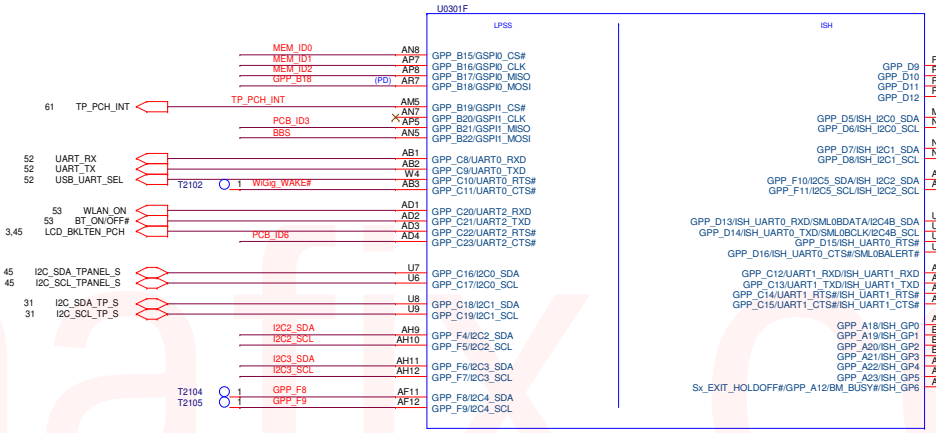
BIOS Rev. SKU

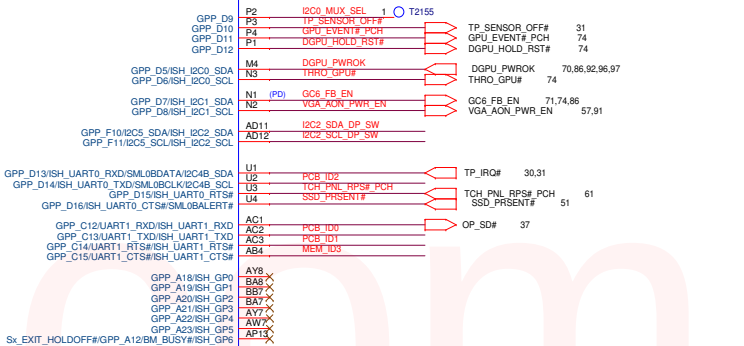
ID2	ID1	ID0	PCB Rev.
0	0	0	R1.0
0	0	1	R1.1
0	1	0	R1.2
0	1	1	R1.3
1	0	0	R2.0
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

SSD_PRSENT#	PCB_ID3	PCB_ID4	PCB_ID5	PCB_ID6	PCB_ID9	PCB_ID10	PCB_ID11
1: SSD	1: UMA	1: SKL	1: EJ14	1: N16S-GTR	1: PCIE_SSD	1: Reserved	1: Reserved
0: No SSD	0: DSC	0: KBL	0: EA15	0: N16V-GMR	0: SATA_SSD	0: Reserved	0: Reserved



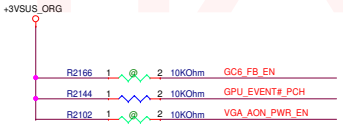


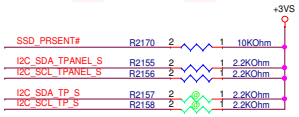




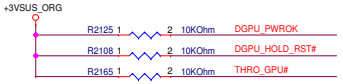
Memory ID

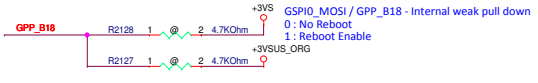
MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	Description		
GPP_B15	GPP_B16	GPP_B17	GPP_C15	Setting	Vendor PN	PEGA PN
0	0	0	0	HYNIX4G	H5AN8G6NAFR-UHC	0315-01W60PB
0	0	1	0	HYNIX 2G	H5AN4G6NAFR-UHC	0315-01EK0PB
0	1	0	0	SAMSUNG 4G	K4A8G165WB-BCRC	0315-01C80PB
0	1	1	0	SAMSUNG2G	K4A4G165WE-BCPB	0315-01WA0PB
1	0	0	0	MICRON 4G	MT40A512M16JY-083E:B	0315-01W90PB
1	0	1	0	MICRON 2G	N/A	N/A
1	1	0	0	Reserved	Reserved	Reserved
1	1	1	0	Reserved	Reserved	Reserved

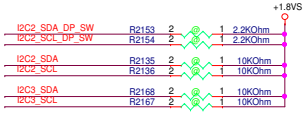


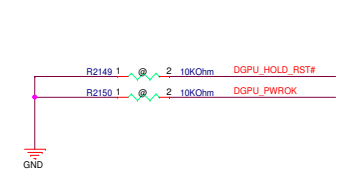


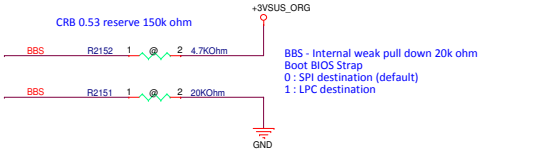
GPIO need to pull high to power with 10Kohm if unused











<Variant Name>

Vinafix

PEGATRON Title : PCH(2) LPSS,ISH

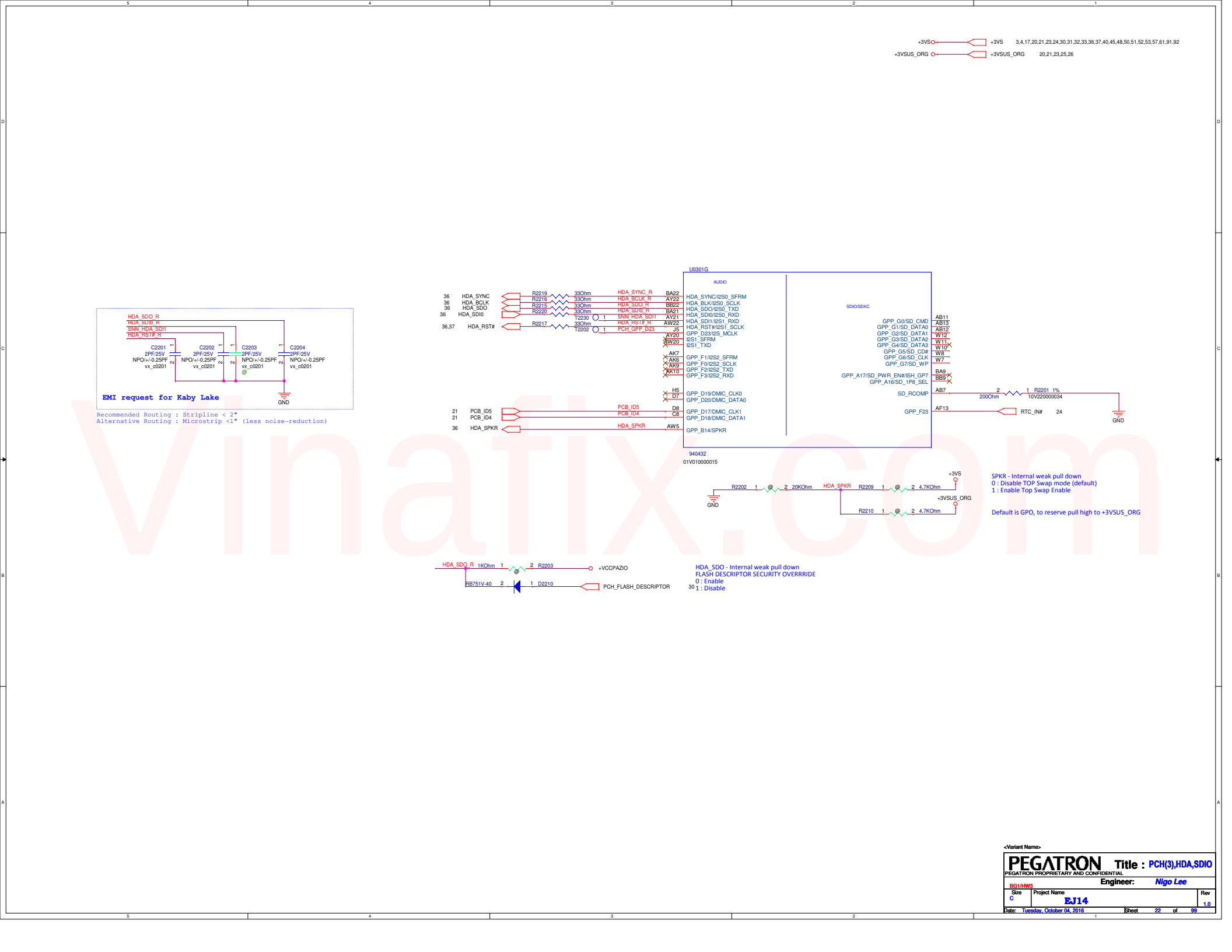
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Nigo Lee

BG1/HW3

Size	Project Name	Rev
C	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 21 of 99



<Variant Name>

PEGATRON Title : PCH(3),HDA,SDIO

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Nigo Lee

BG1/HW3

Size	Project Name	Rev
C	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 22 of 99

+3VS +3VS 3,4,17,20,21,22,24,30,31,32,33,36,37,40,45,48,50,51,52,53,57,61,91,92

+3VSUS_ORG +3VSUS_ORG 20,21,22,25,26

U0301H

PCIE/USB3/SATA

SSIC / USB3

USB2

GPU

LAN

WLAN

HDD

ODD

SSD

70 PCIENB_RXN0
70 PCIENB_RXP0
70 PCIEG_TXN0
70 PCIEG_TXP0
/VGA C2316 1 2 0.22UF/10V PCIEG_TXN0_C
/VGA C2319 1 2 0.22UF/10V PCIEG_TXP0_C
H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP

70 PCIENB_RXN1
70 PCIENB_RXP1
70 PCIEG_TXN1
70 PCIEG_TXP1
/VGA C2310 1 2 0.22UF/10V PCIEG_TXN1_C
/VGA C2312 1 2 0.22UF/10V PCIEG_TXP1_C
G11 PCIE2_RXN/USB3_6_RXN
F11 PCIE2_RXP/USB3_6_RXP
D16 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

70 PCIENB_RXN2
70 PCIENB_RXP2
70 PCIEG_TXN2
70 PCIEG_TXP2
/VGA C2311 1 2 0.22UF/10V PCIEG_TXN2_C
/VGA C2313 1 2 0.22UF/10V PCIEG_TXP2_C
H16 PCIE3_RXN
G16 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP

70 PCIENB_RXN3
70 PCIENB_RXP3
70 PCIEG_TXN3
70 PCIEG_TXP3
/VGA C2314 1 2 0.22UF/10V PCIEG_TXN3_C
/VGA C2315 1 2 0.22UF/10V PCIEG_TXP3_C
G15 PCIE4_RXN
F15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

33 PCIE_RXN_LAN
33 PCIE_RXP_LAN
33 PCIE_TXN_LAN
33 PCIE_TXP_LAN
0.1UF/16V 1 2 C2320 PCIE_TXN_LAN_C
0.1UF/16V 1 2 C2321 PCIE_TXP_LAN_C
F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP

53 PCIE_RXN_WLAN
53 PCIE_RXP_WLAN
53 PCIE_TXN_WLAN
53 PCIE_TXP_WLAN
0.1UF/16V 1 2 C2322 PCIE_TXN_WLAN_C
0.1UF/16V 1 2 C2323 PCIE_TXP_WLAN_C
G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

51 SATA_RXN0
51 SATA_RXP0
51 SATA_TXN0
51 SATA_TXP0
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

F22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP

F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

R2301 1 2 100Ohm 1% PCIE_RCOMPN
PCIE_RCOMPP
F5 PCIE_RCOMPN
E5 PCIE_RCOMPP

D56 PROC_PRDY#
D61 PROC_PREQ#
PIRQA# BB11 GPP_A7/PIRQA#

51 PCIE_RXN11_SSD
51 PCIE_RXP11_SSD
51 PCIE_TXN11_SSD
51 PCIE_TXP11_SSD
51 PCIE_SATA_RXN12_SSD
51 PCIE_SATA_RXP12_SSD
51 PCIE_SATA_TXN12_SSD
51 PCIE_SATA_TXP12_SSD
E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP
E30 PCIE12_RXN/SATA2_RXN
F30 PCIE12_RXP/SATA2_RXP
A25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP

940432
01V010000015

USB3_1_RXN H8
USB3_1_RXP G8
USB3_1_TXN C13
USB3_1_TXP D13
USB3_RXN1 52
USB3_RXP1 52
USB3_TXN1 52
USB3_TXP1 52

USB3_2_RXN/SSIC_RXN J6
USB3_2_RXP/SSIC_RXP H6
USB3_2_TXN/SSIC_TXN B13
USB3_2_TXP/SSIC_TXP A13
USB3_RXN2 52
USB3_RXP2 52
USB3_TXN2 52
USB3_TXP2 52

USB3_3_RXN J10
USB3_3_RXP H10
USB3_3_TXN B15
USB3_3_TXP A15

USB3_4_RXN E10
USB3_4_RXP F10
USB3_4_TXN C15
USB3_4_TXP D15

on MLB USB3.0

on MLB USB3.0

USB2N_1 AB9
USB2P_1 AB10
USB_PN1 52
USB_PP1 52

USB2N_2 AD6
USB2P_2 AD7
USB_PN2 52
USB_PP2 52

USB2N_3 AH3
USB2P_3 AJ3
USB_PN3 52
USB_PP3 52

USB2N_4 AD9
USB2P_4 AD10

USB2N_5 AJ1
USB2P_5 AJ2
USB_PN5 53
USB_PP5 53

USB2N_6 AF6
USB2P_6 AF7
USB_PN6 61
USB_PP6 61

USB2N_7 AH1
USB2P_7 AH2
USB_PN7 45
USB_PP7 45

USB2N_8 AF8
USB2P_8 AF9
USB_PN8 40
USB_PP8 40

USB2N_9 AG1
USB2P_9 AG2

USB2N_10 AH7
USB2P_10 AH8

USB2_COMP AB6 USB2_COMP R2302 1 2 113Ohm 1% GND
USB2_ID AG3 USB2_ID_OTG R2310 1 2 1KOhm GND
USB2_VBUSSENSE AG4 USB2_VBUSSENSE_OTG R2330 1 2 1KOhm

GPP_E9/USB2_OC0# A9 USB_OC0#_PCH
GPP_E10/USB2_OC1# C9 USB_OC1#_PCH
GPP_E11/USB2_OC2# D9 PCB_ID10
GPP_E12/USB2_OC3# B9 PCB_ID11
USB_OC0#_PCH 52 USB3.0
USB_OC1#_PCH 52 USB3.0/USB2.0
PCB_ID10 21
PCB_ID11 21

GPP_E4/DEVSLP0 J1
GPP_E5/DEVSLP1 J2
GPP_E6/DEVSLP2 J3
DEVSLP2 51

GPP_E0/SATAXPCIE0/SATAGP0 H2 SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1 H3 SATA_ODD_PRSNT#
GPP_E2/SATAXPCIE2/SATAGP2 G4 SATA_SSD_PEDET 51

GPP_E8/SATALED# H1

USB_PN1 Finger Print
USB_PP1 M.2 BT
USB_PN2 Touch Panel
USB_PP2 Camera
USB_PN3 Card Reader
USB_PP3

USB_OC0#_PCH 1 10KOhm 2 RN2310A
USB_OC1#_PCH 3 10KOhm 4 RN2310B
+3VSUS_ORG

DEVSLP2 R2324 1 @ 2 10KOhm
+3VS

SATAGP0 R2320 1 @ 2 10KOhm
SATA_ODD_PRSNT# R2305 1 @ 2 10KOhm
PIRQA# R2318 1 2 10KOhm
+3VS

PCH	PCIe* Link Config	Flexible HSIO Lanes											
		5	6	7	8	9	10	11	12	13	14	15	16
		PCIe* Controller 1				PCIe* Controller 2				PCIe* Controller 3			
		PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
PCH-U	1x4	P1				P5				P9			
	2x2	P1		P3		P5		P7		P9		P11	
	1x2 + 2x1	P1		P3	P4	P5		P7	P8	P9		P11	P12
	2x1 + 1x2	P4	P3	P1		P8	P7	P5		P12	P11	P9	
	4x1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12

Table 1-2. PCH SKUs

Features	Base-U	Premium-U	Premium-Y
Intel® Rapid Storage Technology (Intel® RST)	AHCI Mode	AHCI and RAID Mode	AHCI and RAID Mode
Total USB 3.0 Ports	4	6	6
Total USB 2.0 Ports	8[1]	10[2]	6[3]
Total SATA 3.0 Ports (Max. 6Gb/s)	2	3	2
Total PCI Express* Lanes (Gen)	10 (2.0)	12 (3.0)	10 (3.0)
Total Intel® RST for PCIe* Storage and SATA Express* Storage Devices	0	2[5]	2[5]
Total CSI2 lanes	8 lanes	12 lanes	12 lanes

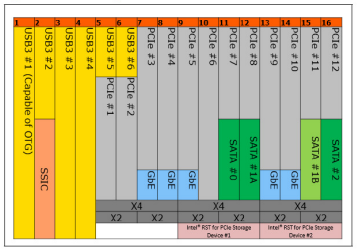
Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)
5. Intel® RST PCIe supports RAID configuration 0/1

Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



<Variant Name>

PEGATRON Title PCH(4) _PCIE,SATA,USB,

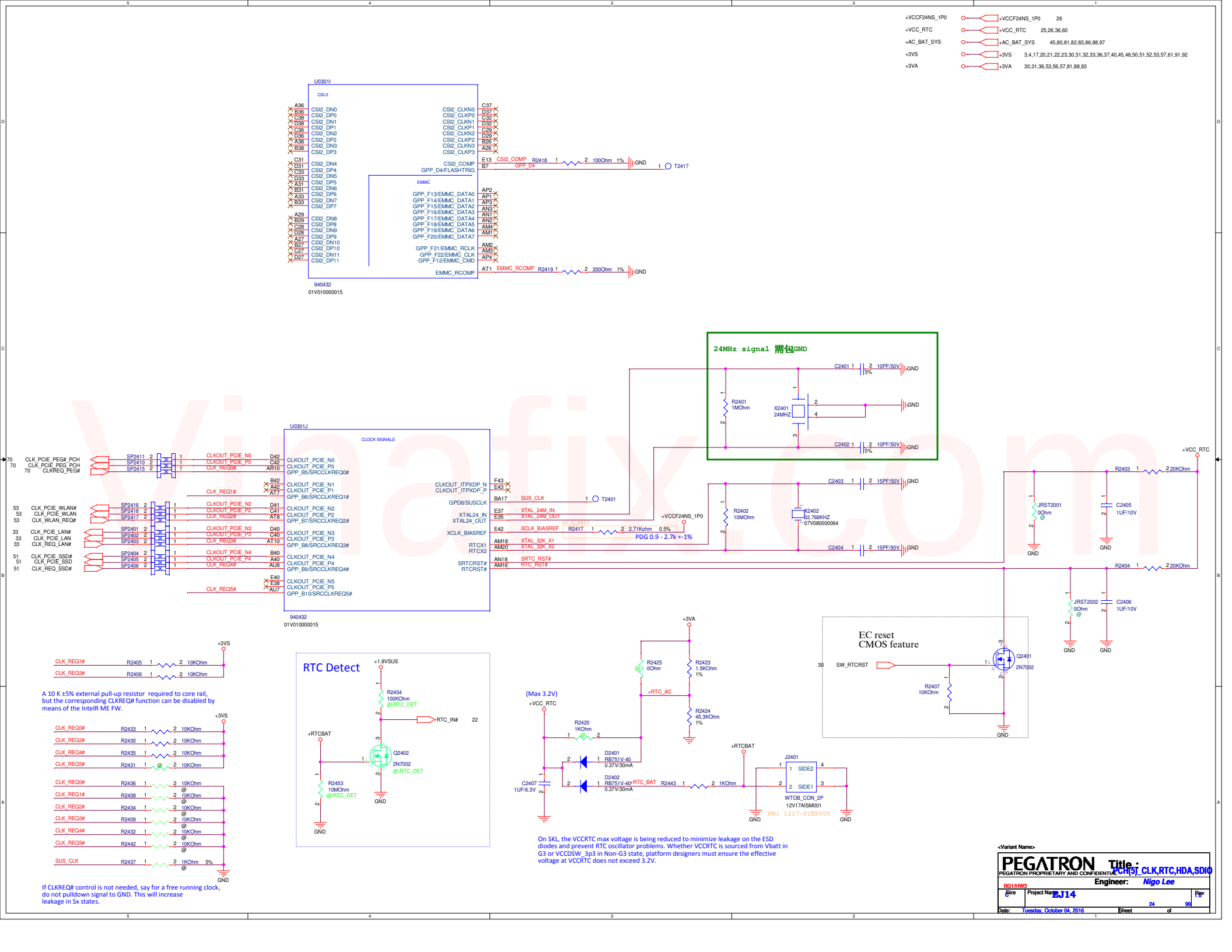
PEGATRON PROPRIETARY AND CONFIDENTIAL

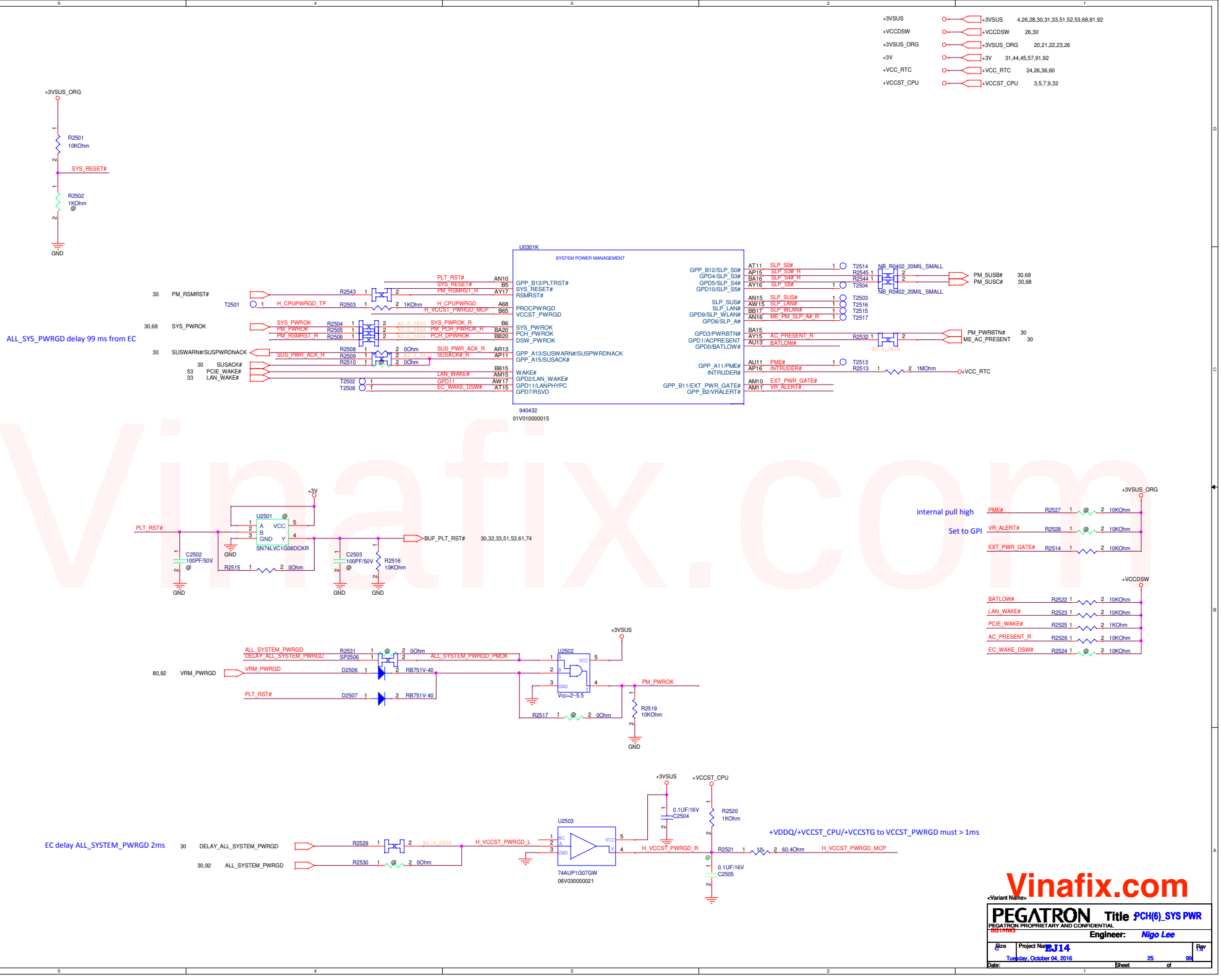
Engineer: Nigo Lee

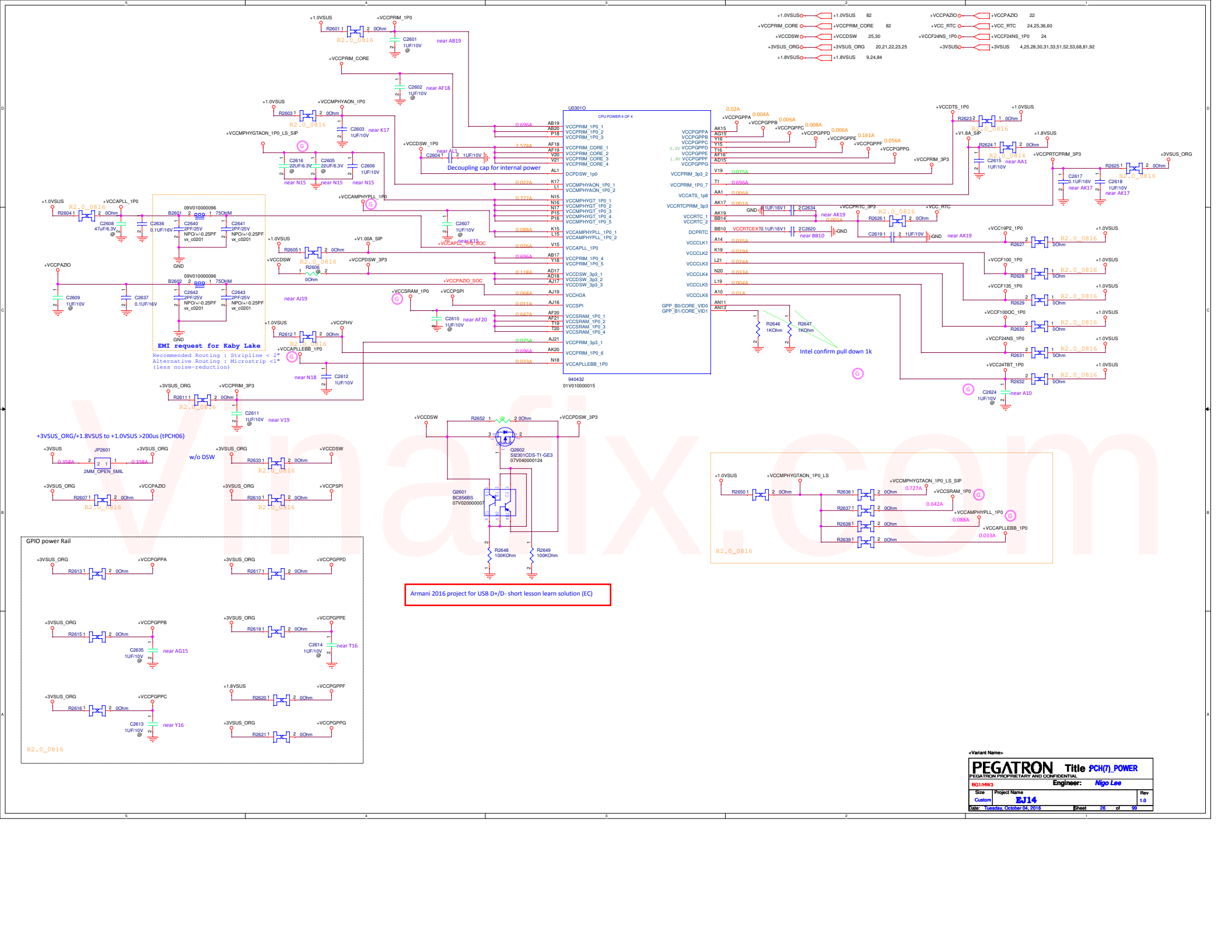
BG1/HW3

Size	Project Name	Rev
C	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 23 of 99

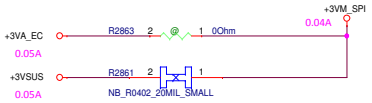

+VCCF24NS_1P0 +VCCF24NS_1P0 26
+VCC_RTC +VCC_RTC 25,26,36,60
+AC_BAT_SYS +AC_BAT_SYS 45,80,81,82,83,86,88,97
+3VS +3VS 3,4,17,20,21,22,23,30,31,32,33,36,37,40,45,48,50,51,52,53,57,61,91,92
+3VA +3VA 30,31,36,53,56,57,81,88,93
U0301I
CSI-2
CSI2_DN0 CSI2_DP0 CSI2_DN1 CSI2_DP1 CSI2_DN2 CSI2_DP2 CSI2_DN3 CSI2_DP3
CSI2_DN4 CSI2_DP4 CSI2_DN5 CSI2_DP5 CSI2_DN6 CSI2_DP6 CSI2_DN7 CSI2_DP7
CSI2_DN8 CSI2_DP8 CSI2_DN9 CSI2_DP9 CSI2_DN10 CSI2_DP10 CSI2_DN11 CSI2_DP11
CSI2_CLKN0 CSI2_CLKP0 CSI2_CLKN1 CSI2_CLKP1 CSI2_CLKN2 CSI2_CLKP2 CSI2_CLKN3 CSI2_CLKP3
CSI2_COMP
GPP_D4/FLASHTRIG
CSI2_COMP R2418 100Ohm 1% GPP_D4 T2417
EMMC
GPP_F13/EMMC_DATA0 GPP_F14/EMMC_DATA1 GPP_F15/EMMC_DATA2 GPP_F16/EMMC_DATA3 GPP_F17/EMMC_DATA4 GPP_F18/EMMC_DATA5 GPP_F19/EMMC_DATA6 GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK GPP_F22/EMMC_CLK GPP_F12/EMMC_CMD
EMMC_RCOMP EMMC_RCOMP R2419 200Ohm 1%
940432
01V010000015
24MHz signal 需包GND
C2401 10PF/50V 5%
R2401 1MOhm
X2401 24MHZ
C2402 10PF/50V 5%
U0301J
CLOCK SIGNALS
CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P
GPD8/SUSCLK SUS_CLK T2401
XTAL24_IN XTAL24_OUT
XCLK_BIASREF R2417 2.71Kohm 0.5% PDG 0.9 - 2.7k +-1%
RTCX1 RTCX2 XTAL_32K_X1 XTAL_32K_X2
SRTCRST# RTCRST# SRTC_RST# RTC_RST#
+VCCF24NS_1P0
R2402 10MOhm
X2402 32.768KHZ 07V080000064
C2403 15PF/50V
C2404 15PF/50V
+VCC_RTC
R2403 20KOhm
R2404 20KOhm
JRST2001 0Ohm
JRST2002 0Ohm
C2405 1UF/10V
C2406 1UF/10V
CLK_PCIE_PEG# CLK_PCIE_PEG_PCH CLKREQ_PEG#
CLK_PCIE_WLAN# CLK_PCIE_WLAN CLK_WLAN_REQ#
CLK_PCIE_LAN# CLK_PCIE_LAN CLK_REQ_LAN#
CLK_PCIE_SSD# CLK_PCIE_SSD CLK_REQ_SSD#
CLK_REQ1# CLK_REQ2# CLK_REQ3# CLK_REQ4# CLK_REQ5#
SP2411 SP2410 SP2415 SP2416 SP2418 SP2417 SP2401 SP2402 SP2403 SP2404 SP2405 SP2406
940432
01V010000015
+3VS
CLK_REQ1# R2405 10KOhm
CLK_REQ3# R2406 10KOhm
A 10 K ±5% external pull-up resistor required to core rail, but the corresponding CLKREQ# function can be disabled by means of the IntelR ME FW.
+3VS
CLK_REQ0# R2433 10KOhm
CLK_REQ2# R2430 10KOhm
CLK_REQ4# R2435 10KOhm
CLK_REQ5# R2431 10KOhm
CLK_REQ0# R2436 10KOhm @
CLK_REQ1# R2408 10KOhm @
CLK_REQ2# R2434 10KOhm @
CLK_REQ3# R2409 10KOhm @
CLK_REQ4# R2432 10KOhm @
CLK_REQ5# R2442 10KOhm @
SUS_CLK R2437 1KOhm 5% @
GND
If CLKREQ# control is not needed, say for a free running clock, do not pulldown signal to GND. This will increase leakage in Sx states.
RTC Detect
+1.8VSUS
R2454 100KOhm @/RTC_DET
RTC_IN# 22
+RTCBAT
Q2402 2N7002 @/RTC_DET
R2453 10MOhm @/RTC_DET
GND
+3VA
(Max 3.2V)
+VCC_RTC
R2425 0Ohm @
R2423 1.5KOhm 1%
+RTC_AC
R2424 45.3KOhm 1%
R2420 1KOhm @
D2401 RB751V-40 0.37V/30mA
D2402 RB751V-40 0.37V/30mA
RTC_BAT
R2443 1KOhm
C2407 1UF/6.3V
+RTCBAT
J2401 SIDE2 SIDE1
WTOB_CON_2P 12V17AISM001
PN: 1217-01EP000
GND
On SKL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V.
EC reset
CMOS feature
SW_RTCRST
Q2401 2N7002
R2407 10KOhm
GND
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PCH(5)_CLK,RTC,HDA,SDIO
Engineer: Nigo Lee
BG1/HW3
Size C
Project Name EJ14
Rev 1.0
Date: Tuesday, October 04, 2016
Sheet 24 of 99

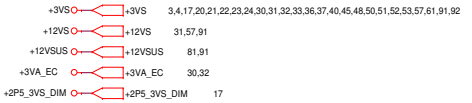

+3VSUS +3VSUS 4,26,28,30,31,33,51,52,53,68,81,92
+VCCDSW +VCCDSW 26,30
+3VSUS_ORG +3VSUS_ORG 20,21,22,23,26
+3V +3V 31,44,45,57,91,92
+VCC_RTC +VCC_RTC 24,26,36,60
+VCCST_CPU +VCCST_CPU 3,5,7,9,32
+3VSUS_ORG
R2501 10KOhm
SYS_RESET#
R2502 1KOhm @
GND
U0301K
SYSTEM POWER MANAGEMENT
940432
01V010000015
ALL_SYS_PWRGD delay 99 ms from EC
30 PM_RSMRST#
T2501 H_CPUPWRGD_TP
30,68 SYS_PWROK
30 SUSWARN#/SUSPWRDNACK
30 SUSACK#
53 PCIE_WAKE#
33 LAN_WAKE#
PLT_RST#
SYS_RESET#
PM_RSMRST_R
H_CPUPWRGD
H_VCCST_PWRGD_MCP
SYS_PWROK_R
PM_PCH_PWROK_R
PCH_DPWROK
SUS_PWR_ACK_R
SUSACK#_R
LAN_WAKE#
EC_WAKE_DSW#
GPP_B13/PLTRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
SLP_S0#
SLP_S3#_R
SLP_S4#_R
SLP_S5#
SLP_SUS#
SLP_LAN#
SLP_WLAN#
ME_PM_SLP_A#_R
AC_PRESENT_R
BATLOW#
PME#
INTRUDER#
EXT_PWR_GATE#
VR_ALERT#
PM_SUSB# 30,68
PM_SUSC# 30,68
PM_PWRBTN# 30
ME_AC_PRESENT 30
+VCC_RTC
+3V
U2501
SN74LVC1G08DCKR
PLT_RST#
BUF_PLT_RST# 30,32,33,51,53,61,74
C2502 100PF/50V @
C2503 100PF/50V @
R2515 0Ohm
R2516 10KOhm
internal pull high
Set to GPI
+3VSUS_ORG
PME# R2527 10KOhm
VR_ALERT# R2528 10KOhm
EXT_PWR_GATE# R2514 10KOhm
+VCCDSW
BATLOW# R2522 10KOhm
LAN_WAKE# R2523 10KOhm
PCIE_WAKE# R2525 1KOhm
AC_PRESENT_R R2526 10KOhm
EC_WAKE_DSW# R2524 10KOhm
ALL_SYSTEM_PWRGD R2531 0Ohm
DELAY_ALL_SYSTEM_PWRGD SP2506
ALL_SYSTEM_PWRGD_PMOK
80,92 VRM_PWRGD
VRM_PWRGD D2506 RB751V-40
PLT_RST# D2507 RB751V-40
U2502
Vcc=2~5.5
PM_PWROK
R2519 10KOhm
R2517 0Ohm
+3VSUS
GND
EC delay ALL_SYSTEM_PWRGD 2ms
30 DELAY_ALL_SYSTEM_PWRGD
30,92 ALL_SYSTEM_PWRGD
R2529
R2530 0Ohm
H_VCCST_PWRGD_L
U2503
74AUP1G07GW
06V030000021
+3VSUS
+VCCST_CPU
0.1UF/16V C2504
R2520 1KOhm
H_VCCST_PWRGD_R
R2521 60.4Ohm
H_VCCST_PWRGD_MCP
0.1UF/16V C2505
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms
Vinafix.com
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title PCH(6)_SYS PWR
Engineer: Nigo Lee
Size D
Project Name E714
Rev 1.0
Date: Tuesday, October 04, 2016
Sheet 25 of 99

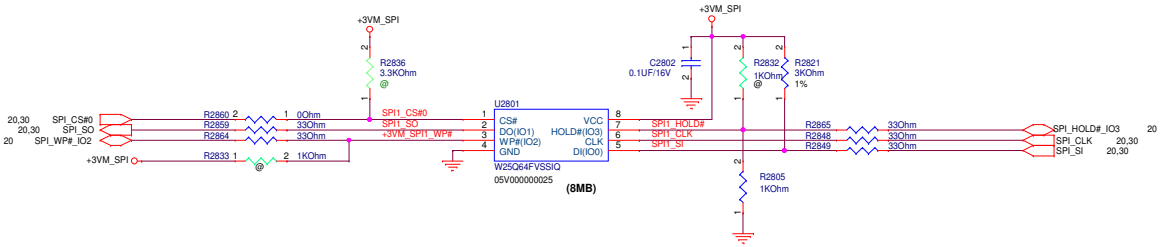

+1.0VSUS
+VCCPRIM_1P0
R2601 1 2 0Ohm
R2.0_0816
C2601 1UF/10V @
near AB19
+VCCPRIM_CORE
C2602 near AF18 1UF/10V @
+1.0VSUS
+VCCMPHYAON_1P0
R2603 1 2 0Ohm
R2.0_0816
C2603 near K17 1UF/10V
+VCCMPHYGTAON_1P0_LS_SIP
C2616 22UF/6.3V @
C2605 22UF/6.3V @
C2606 1UF/10V @
near N15
near N15
near N15
+VCCDSW_1P0
C2604 1 2 1UF/10V
near AL1
Decoupling cap for internal power
+VCCAMPHYPLL_1P0
C2607 1UF/10V @
near K15
+VCCAPLL_1P0_SOC
+1.0VSUS
+VCCAPLL_1P0
R2604 1 2 0Ohm
R2.0_0816
C2608 47uF/6.3V @
C2636 0.1UF/16V
B2601 09V010000096 2 1 75OHM
C2640 2PF/25V NPO/+/-0.25PF vx_c0201
C2641 2PF/25V NPO/+/-0.25PF vx_c0201
GND
+1.0VSUS
R26051 2 0Ohm
R2.0_0816
R2606 0Ohm
+V1.00A_SIP
+VCCDSW
+VCCPDSW_3P3
+VCCPAZIO
B2602 09V010000096 2 1 75OHM
C2609 1UF/10V @
C2637 0.1UF/16V
C2642 2PF/25V NPO/+/-0.25PF vx_c0201
C2643 2PF/25V NPO/+/-0.25PF vx_c0201
GND
near AJ19
+VCCPAZIO_SOC
+VCCSRAM_1P0
+VCCPSPI
C2610 near AF20 1UF/10V @
+1.0VSUS
+VCCFHV
R2612 1 2 0Ohm
R2.0_0816
+VCCAPLLEBB_1P0
near N18
C2612 1UF/10V @
EMI request for Kaby Lake
Recommended Routing : Stripline < 2"
Alternative Routing : Microstrip <1"
(less noise-reduction)
+3VSUS_ORG
+VCCPRIM_3P3
R2611 1 2 0Ohm
R2.0_0816
C2611 1UF/10V @ near V19
U0301O
CPU POWER 4 OF 4
0.696A AB19 VCCPRIM_1P0_1
AB20 VCCPRIM_1P0_2
P18 VCCPRIM_1P0_3
2.574A AF18 VCCPRIM_CORE_1
AF19 VCCPRIM_CORE_2
V20 VCCPRIM_CORE_3
V21 VCCPRIM_CORE_4
AL1 DCPDSW_1p0
0.022A K17 VCCMPHYAON_1P0_1
L1 VCCMPHYAON_1P0_2
0.727A N15 VCCMPHYGT_1P0_1
N16 VCCMPHYGT_1P0_2
N17 VCCMPHYGT_1P0_3
P15 VCCMPHYGT_1P0_4
P16 VCCMPHYGT_1P0_5
0.088A K15 VCCAMPHYPLL_1P0_1
L15 VCCAMPHYPLL_1P0_2
0.026A V15 VCCAPLL_1P0
0.696A AB17 VCCPRIM_1P0_4
Y18 VCCPRIM_1P0_5
0.118A AD17 VCCDSW_3p3_1
AD18 VCCDSW_3p3_2
AJ17 VCCDSW_3p3_3
0.068A AJ19 VCCHDA
0.011A AJ16 VCCSPI
0.642A AF20 VCCSRAM_1P0_1
AF21 VCCSRAM_1P0_2
T19 VCCSRAM_1P0_3
T20 VCCSRAM_1P0_4
0.075A AJ21 VCCPRIM_3p3_1
0.696A AK20 VCCPRIM_1P0_6
0.033A N18 VCCAPLLEBB_1P0
940432
01V010000015
VCCPGPPA
VCCPGPPB
VCCPGPPC
VCCPGPPD
VCCPGPPE
VCCPGPPF
VCCPGPPG
VCCPRIM_3p3_2
VCCPRIM_1P0_7
VCCATS_1p8
VCCRTCPRIM_3p3
VCCRTC_1
VCCRTC_2
DCPRTC
VCCCLK1
VCCCLK2
VCCCLK3
VCCCLK4
VCCCLK5
VCCCLK6
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
AK15 0.02A
AG15 0.004A
Y16 0.006A
Y15 0.008A
3.3V T16 0.006A
AF18 0.161A
1.8V AD15 0.056A
V19 0.075A
T1 0.696A
AA1 0.006A
AK17 0.001A
AK19 0.001A
BB14 0.001A
BB10 0.035A
A14 0.029A
K19 0.024A
L21 0.033A
N20 0.004A
L19 0.001A
A10
AN11
AN13
+VCCPGPPA
+VCCPGPPB
+VCCPGPPC
+VCCPGPPD
+VCCPGPPE
+VCCPGPPF
+VCCPGPPG
+VCCPRIM_3P3
+VCCDTS_1P0
+1.0VSUS
R2623 2 1 0Ohm
R2.0_0816
+V1.8A_SIP
+1.8VSUS
R2624 1 2 0Ohm
R2.0_0816
C2615 near AA1 1UF/10V
+VCCPRTCPRIM_3P3
+3VSUS_ORG
R2625 1 2 0Ohm
R2.0_0816
C2617 0.1UF/16V near AK17
C2618 1UF/10V near AK17
GND
0.1UF/16V
2 C2634
near AK19
+VCCPRTC_3P3
R2626 1 2 0Ohm
R2.0_0816
+VCC_RTC
VCCRTCEXT
0.1UF/16V
2 C2620
near BB10
GND
C2619 1 2 1UF/10V
GND
near AK19
+VCC19P2_1P0
+1.0VSUS
R2627 2 1 0Ohm
R2.0_0816
+VCCF100_1P0
R2628 2 1 0Ohm
R2.0_0816
+VCCF135_1P0
R2629 2 1 0Ohm
R2.0_0816
+VCCF100OC_1P0
R2630 2 1 0Ohm
R2.0_0816
+VCCF24NS_1P0
R2631 2 1 0Ohm
R2.0_0816
+VCC24TBT_1P0
R2632 2 1 0Ohm
R2.0_0816
C2624 1UF/10V @
near A10
R2646 1KOhm
R2647 1KOhm
Intel confirm pull down 1k
+1.0VSUS +1.0VSUS 82
+VCCPRIM_CORE +VCCPRIM_CORE 82
+VCCDSW +VCCDSW 25,30
+3VSUS_ORG +3VSUS_ORG 20,21,22,23,25
+1.8VSUS +1.8VSUS 9,24,84
+VCCPAZIO +VCCPAZIO 22
+VCC_RTC +VCC_RTC 24,25,36,60
+VCCF24NS_1P0 +VCCF24NS_1P0 24
+3VSUS +3VSUS 4,25,28,30,31,33,51,52,53,68,81,92
+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)
+3VSUS
JP2601
+3VSUS_ORG
0.358A
0.358A
2MM_OPEN_5MIL
w/o DSW
+3VSUS_ORG
R2633 1 2 0Ohm
R2.0_0816
+VCCDSW
+3VSUS_ORG
R2607 1 2 0Ohm
+VCCPAZIO
+3VSUS_ORG
R2610 1 2 0Ohm
R2.0_0816
+VCCPSPI
+VCCDSW
R2652 1 2 0Ohm
+VCCPDSW_3P3
Q2602
SI2301CDS-T1-GE3
07V040000124
Q2601
BC856BS
07V020000007
R2648 100KOhm
R2649 100KOhm
Armani 2016 project for USB D+/D- short lesson learn solution (EC)
+1.0VSUS
+VCCMPHYGTAON_1P0_LS
R2650 1 2 0Ohm
R2636 1 2 0Ohm
+VCCMPHYGTAON_1P0_LS_SIP
0.727A
+VCCSRAM_1P0
0.642A
R2637 1 2 0Ohm
R2638 1 2 0Ohm
+VCCAMPHYPLL_1P0
0.088A
R2639 1 2 0Ohm
+VCCAPLLEBB_1P0
0.033A
R2.0_0816
GPIO power Rail
+3VSUS_ORG
R2613 1 2 0Ohm
+VCCPGPPA
+3VSUS_ORG
R2617 1 2 0Ohm
+VCCPGPPD
+3VSUS_ORG
R2615 1 2 0Ohm
+VCCPGPPB
C2635 1UF/10V @
near AG15
+3VSUS_ORG
R2619 1 2 0Ohm
+VCCPGPPE
C2614 1UF/10V @
near T16
+3VSUS_ORG
R2616 1 2 0Ohm
+VCCPGPPC
C2613 1UF/10V @
near Y16
+1.8VSUS
R2620 1 2 0Ohm
+VCCPGPPF
+3VSUS_ORG
R2621 1 2 0Ohm
+VCCPGPPG
R2.0_0816
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title PCH(7)_POWER
BG1/HW3
Engineer: Ngo Lee
Size Custom
Project Name EJ14
Rev 1.0
Date: Tuesday, October 04, 2016
Sheet 28 of 99

Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 27 of 99	

PCH SPI ROM







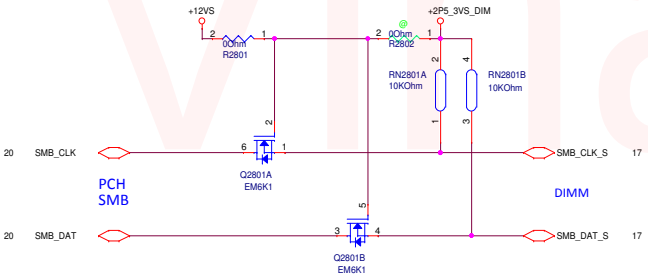
PCH

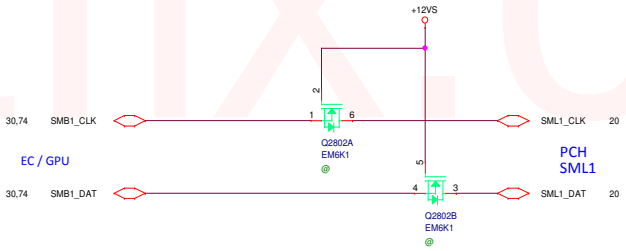
SPI_CLK/SO/SI/CS#0
SPI_WP#_IO2/SPI_HOLD#_IO3

EC

ROM 8MB

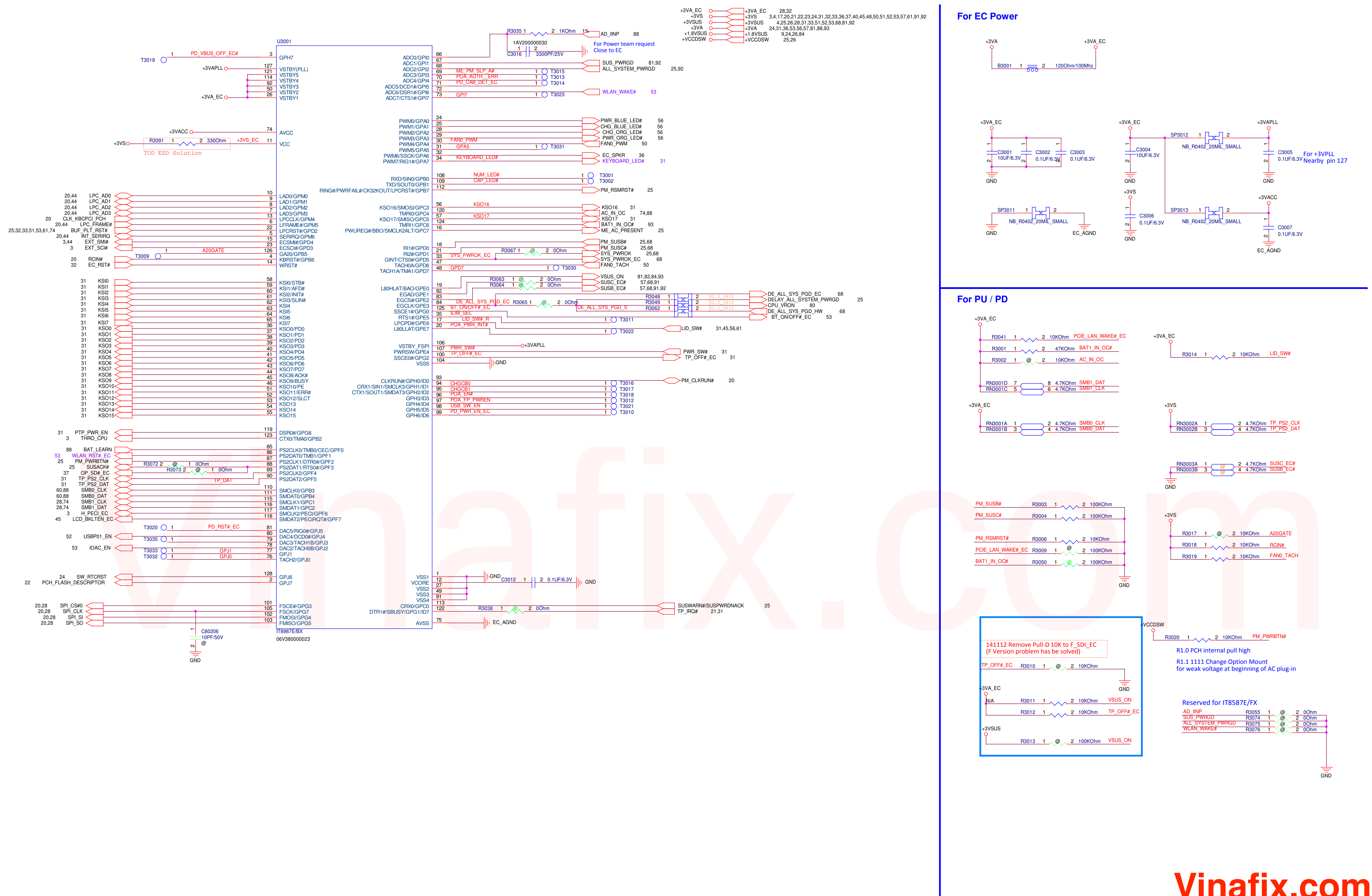
PCH SMBus





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: PCH(8)_SPI,SMB
BG1/HW3
Engineer: Nigo Lee
Size: Custom
Project Name: EJ14
Rev: 1.0
Date: Tuesday, October 04, 2016
Sheet 28 of 99

Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 29 of 99	



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : EC_IT8987E/BX

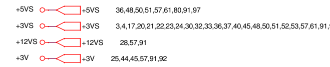
Engineer: Nigo Lee

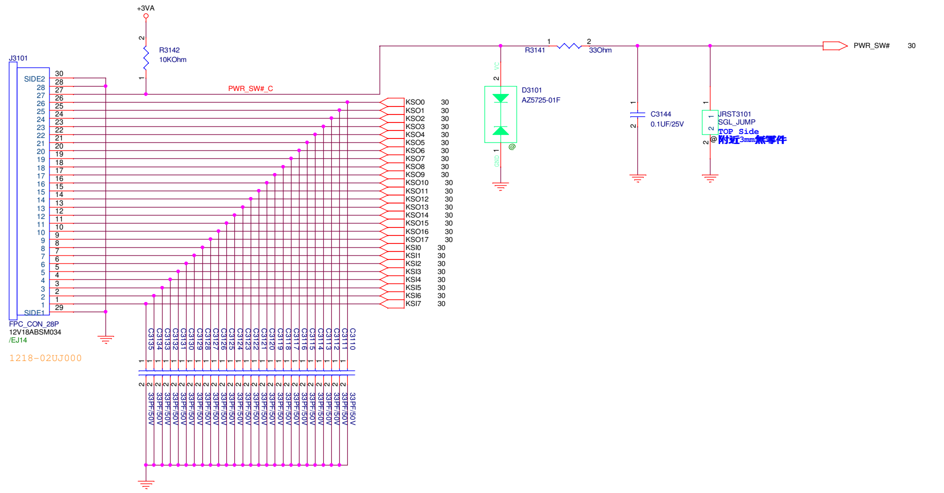
BG1/HW3

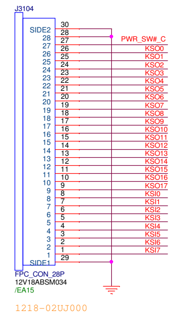
Size	Project Name	Rev
Custom	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 30 of 99

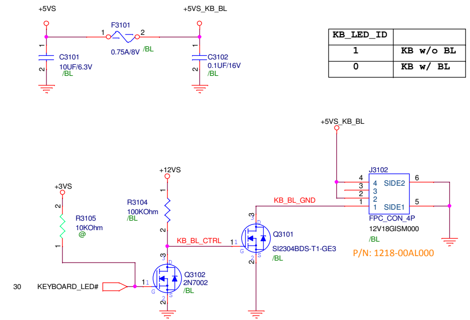
Keyboard





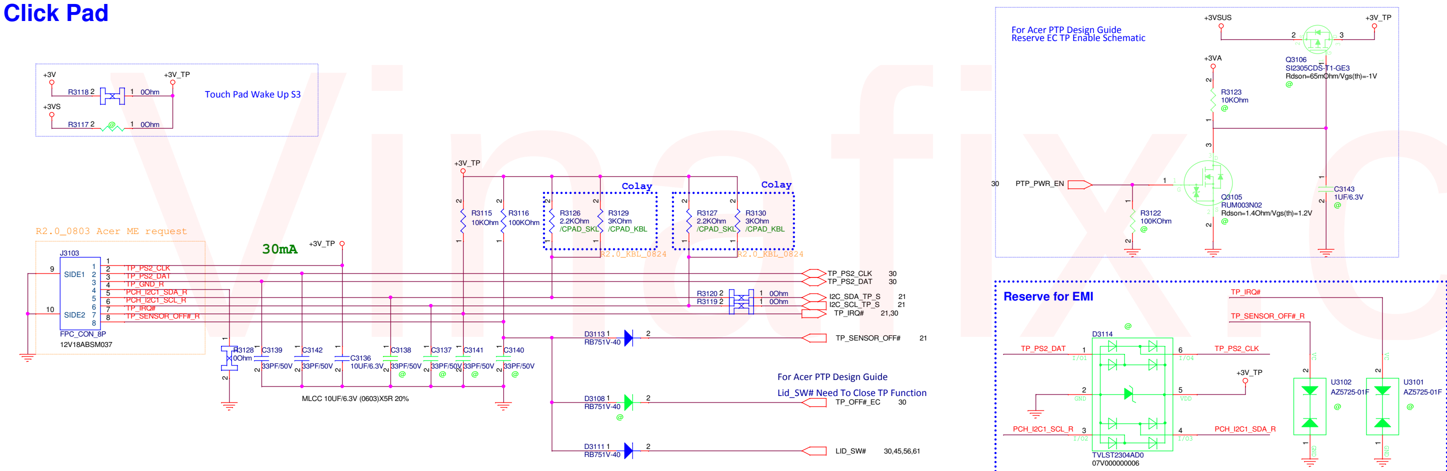


Keyboard LED



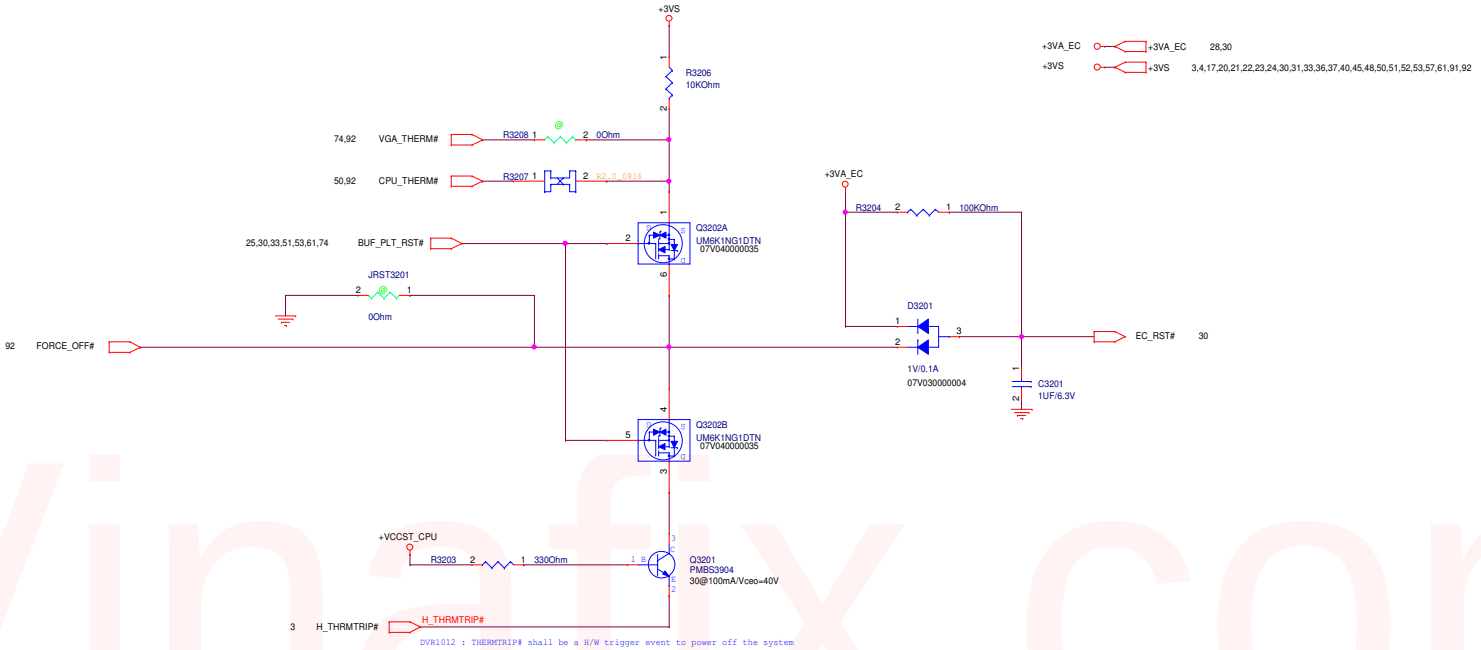
KB_LED_ID	
1	KB w/o BL
0	KB w/ BL

Click Pad


Touch Pad Wake Up S3
R3118
R3117
0Ohm
R2.0_0803 Acer ME request
30mA
J3103
FPC_CON_8P
12V18ABSM037
TP_PS2_CLK
TP_PS2_DAT
TP_GND_R
PCH_I2C1_SDA_R
PCH_I2C1_SCL_R
TP_IRQ#
TP_SENSOR_OFF#_R
Colay
R3115
10KOhm
R3116
100KOhm
R3126
2.2KOhm
R3129
3KOhm
R3127
R3130
/CPAD_SKL
/CPAD_KBL
R2.0_KBL_0824
I2C_SDA_TP_S
I2C_SCL_TP_S
TP_SENSOR_OFF#
MLCC 10UF/6.3V (0603)X5R 20%
For Acer PTP Design Guide
Lid_SW# Need To Close TP Function
TP_OFF#_EC
LID_SW#
RB751V-40
For Acer PTP Design Guide
Reserve EC TP Enable Schematic
+3VSUS
+3V_TP
Q3106
SI2305CDS-T1-GE3
Rdson=65mOhm/Vgs(th)=-1V
R3123
10KOhm
PTP_PWR_EN
Q3105
RUM003N02
Rdson=1.4Ohm/Vgs(th)=1.2V
R3122
100KOhm
C3143
1UF/6.3V
Reserve for EMI
D3114
TVLST2304AD0
07V000000006
U3102
U3101
AZ5725-01F

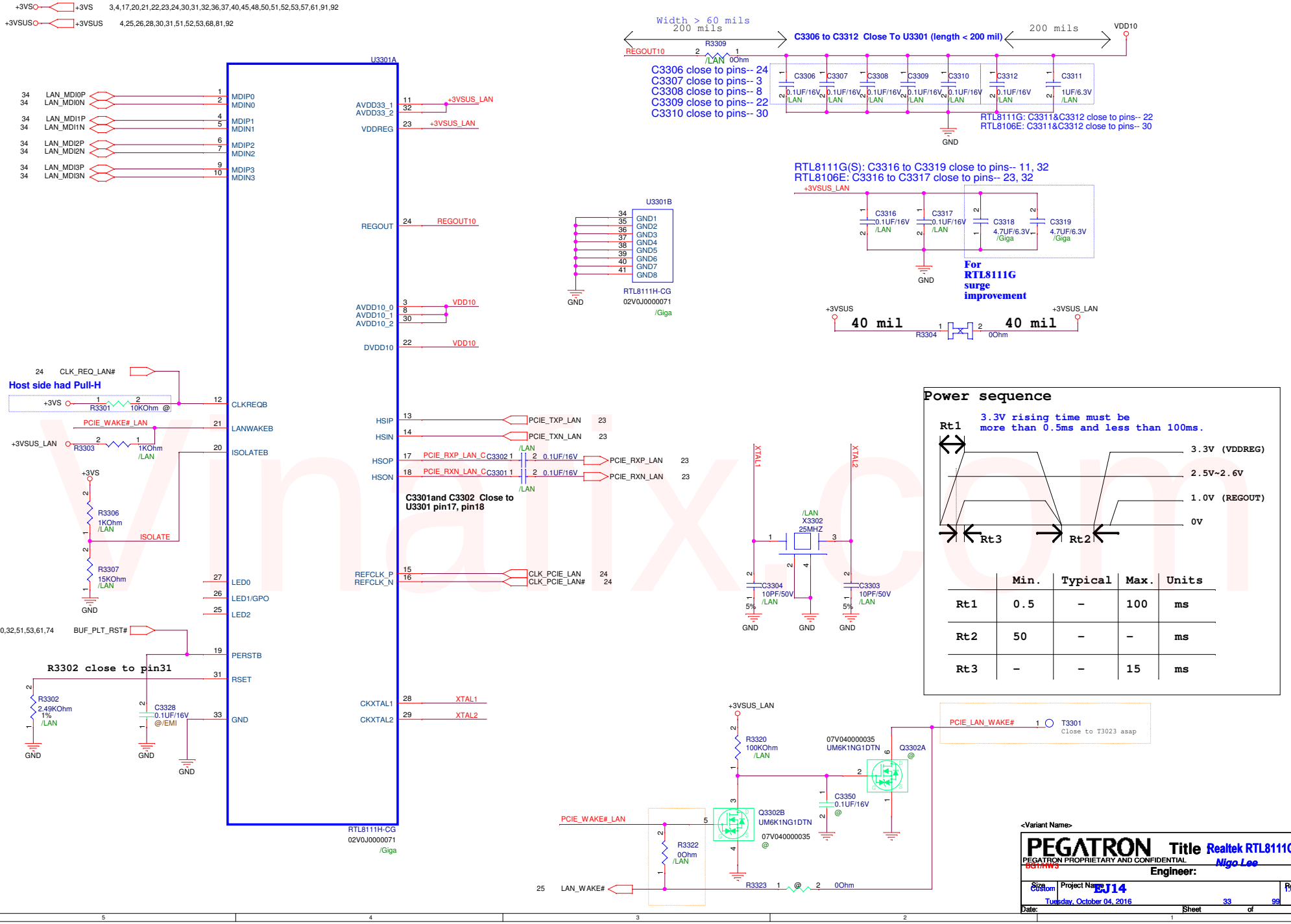
Finger Print

RST_Reset Circuit



Remove 10s RTC reset

PEGATRON	Title : RST_Reset Circuit		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3	Engineer: Nigo Lee		
Size: C	Project Name: EJ14		Rev: 1.0
Date: Tuesday, October 04, 2016	Sheet 32 of 99		


+3VS +3VS 3,4,17,20,21,22,23,24,30,31,32,36,37,40,45,48,50,51,52,53,57,61,91,92
+3VSUS +3VSUS 4,25,26,28,30,31,51,52,53,68,81,92
U3301A
RTL8111H-CG
02V0J0000071
/Giga
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
AVDD33_1
AVDD33_2
VDDREG
REGOUT
AVDD10_0
AVDD10_1
AVDD10_2
DVDD10
CLKREQB
LANWAKEB
ISOLATEB
LED0
LED1/GPO
LED2
PERSTB
RSET
GND
HSIP
HSIN
HSOP
HSON
REFCLK_P
REFCLK_N
CKXTAL1
CKXTAL2
U3301B
RTL8111H-CG
02V0J0000071
/Giga
Width > 60 mils
200 mils
200 mils
VDD10
REGOUT10
R3309
/LAN 0Ohm
C3306 to C3312 Close To U3301 (length < 200 mil)
C3306 close to pins-- 24
C3307 close to pins-- 3
C3308 close to pins-- 8
C3309 close to pins-- 22
C3310 close to pins-- 30
C3306 C3307 C3308 C3309 C3310 C3312 C3311
0.1UF/16V /LAN
1UF/6.3V /LAN
RTL8111G: C3311&C3312 close to pins-- 22
RTL8106E: C3311&C3312 close to pins-- 30
RTL8111G(S): C3316 to C3319 close to pins-- 11, 32
RTL8106E: C3316 to C3317 close to pins-- 23, 32
C3316 C3317 C3318 C3319
0.1UF/16V /LAN
4.7UF/6.3V /Giga
For RTL8111G surge improvement
40 mil
R3304 0Ohm
40 mil
Host side had Pull-H
CLK_REQ_LAN#
R3301 10KOhm @
PCIE_WAKE#_LAN
R3303 1KOhm /LAN
R3306 1KOhm /LAN
R3307 15KOhm /LAN
ISOLATE
BUF_PLT_RST#
R3302 close to pin31
R3302 2.49KOhm 1% /LAN
C3328 0.1UF/16V @/EMI
C3301and C3302 Close to U3301 pin17, pin18
C3302 C3301 0.1UF/16V /LAN
PCIE_TXP_LAN
PCIE_TXN_LAN
PCIE_RXP_LAN_C
PCIE_RXN_LAN_C
PCIE_RXP_LAN
PCIE_RXN_LAN
CLK_PCIE_LAN
CLK_PCIE_LAN#
XTAL1
XTAL2
X3302 25MHZ /LAN
C3304 10PF/50V /LAN
C3303 10PF/50V /LAN
5%
Power sequence
3.3V rising time must be more than 0.5ms and less than 100ms.
Rt1
Rt2
Rt3
3.3V (VDDREG)
2.5V~2.6V
1.0V (REGOUT)
0V
Min. Typical Max. Units
Rt1 0.5 - 100 ms
Rt2 50 - - ms
Rt3 - - 15 ms
+3VSUS_LAN
R3320 100KOhm /LAN
07V040000035 UM6K1NG1DTN
Q3302A @
Q3302B UM6K1NG1DTN
07V040000035 @
C3350 0.1UF/16V @
PCIE_WAKE#_LAN
R3322 0Ohm /LAN
LAN_WAKE#
R3323 1 @ 2 0Ohm
PCIE_LAN_WAKE#
T3301
Close to T3023 asap
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title Realtek RTL8111G
Engineer: Nigo Lee
Size Custom
Project Name LJ14
Rev 1.0
Date: Tuesday, October 04, 2016
Sheet 33 of 99

+3VSUS +3VSUS 4,25,26,28,30,31,33,51,52,53,68,81,92

L3401
NA0069R
/LAN
09V120000009
GIGA

33 LAN_MDI0P — TCT0 — 22/24 — 1CT:1CT — 3/1 — LAN_CT0 / LAN_MDI0P_T
33 LAN_MDI0N — 23 — 2 — LAN_MDI0N_T
33 LAN_MDI2P — TCT2 — 21/20 — 1CT:1CT — 4/5 — LAN_CT2 / LAN_MDI2P_T
33 LAN_MDI2N — 19 — 6 — LAN_MDI2N_T
33 LAN_MDI3P — TCT3 — 16/18 — 1CT:1CT — 9/7 — LAN_CT3 / LAN_MDI3P_T
33 LAN_MDI3N — 17 — 8 — LAN_MDI3N_T
33 LAN_MDI1P — TCT1 — 15/14 — 1CT:1CT — 10/11 — LAN_CT1 / LAN_MDITP_T
33 LAN_MDI1N — 13 — 12 — LAN_MDI1N_T

/LAN 1 2 C3403 0.01UF/100V
TCT0
TCT2
TCT3
TCT1
GND

RN3401B: LAN_MDI0P_T 3 — 0Ohm — 4 LAN_MDI0P_TR
RN3401A: LAN_MDI0N_T 1 — 0Ohm — 2 LAN_MDI0N_TR
90Ohm/100MHz LX3401 @

RN3403B: LAN_MDI2P_T 3 — 0Ohm — 4 LAN_MDI2P_TR
RN3403A: LAN_MDI2N_T 1 — 0Ohm — 2 LAN_MDI2N_TR
90Ohm/100MHz LX3403 @

RN3402B: LAN_MDI1P_T 3 — 0Ohm — 4 LAN_MDI1P_TR
RN3402A: LAN_MDI1N_T 1 — 0Ohm — 2 LAN_MDI1N_TR
90Ohm/100MHz LX3402 @

RN3404B: LAN_MDI3P_T 3 — 0Ohm — 4 LAN_MDI3P_TR
RN3404A: LAN_MDI3N_T 1 — 0Ohm — 2 LAN_MDI3N_TR
90Ohm/100MHz LX3404 @

LAN_CT0 — C3409 — 0.01UF/100V — 75Ohm — R3405 /LAN
LAN_CT1 — C3410 — 0.01UF/100V — 75Ohm — R3404 /LAN
LAN_CT2 — C3411 — 0.01UF/100V — 75Ohm — R3403 /LAN
LAN_CT3 — C3412 — 0.01UF/100V — 75Ohm — R3402 /LAN
FGND1S
R3401 0Ohm @ — LAN_GND
C3402 1000PF/2KV /LAN — LAN_GND

J3401
LAN_JACK_8P
12V23GBSD015
/LAN
LAN_MDI0P_TR 1
LAN_MDI0N_TR 2
LAN_MDI1P_TR 3
LAN_MDI2P_TR 4
LAN_MDI2N_TR 5
LAN_MDI1N_TR 6
LAN_MDI3P_TR 7
LAN_MDI3N_TR 8
P_GND1 1
P_GND2 2
P_GND3 7
P_GND4 8
9 11 12 10
LAN_GND
C3408 1 2 10PF/50V /LAN
GND

EMI request

LAN
8 1
P3 M2 P1 P0
M3 M1 P2 M0

D3403
GND 1 — 2 VC
AZ5725-01F
07V180000029
@
C3401 1 2 10PF/50V /LAN
C3407 1 2 10PF/50V /LAN
R3407 1 2 0Ohm /LAN
GND
LAN_GND

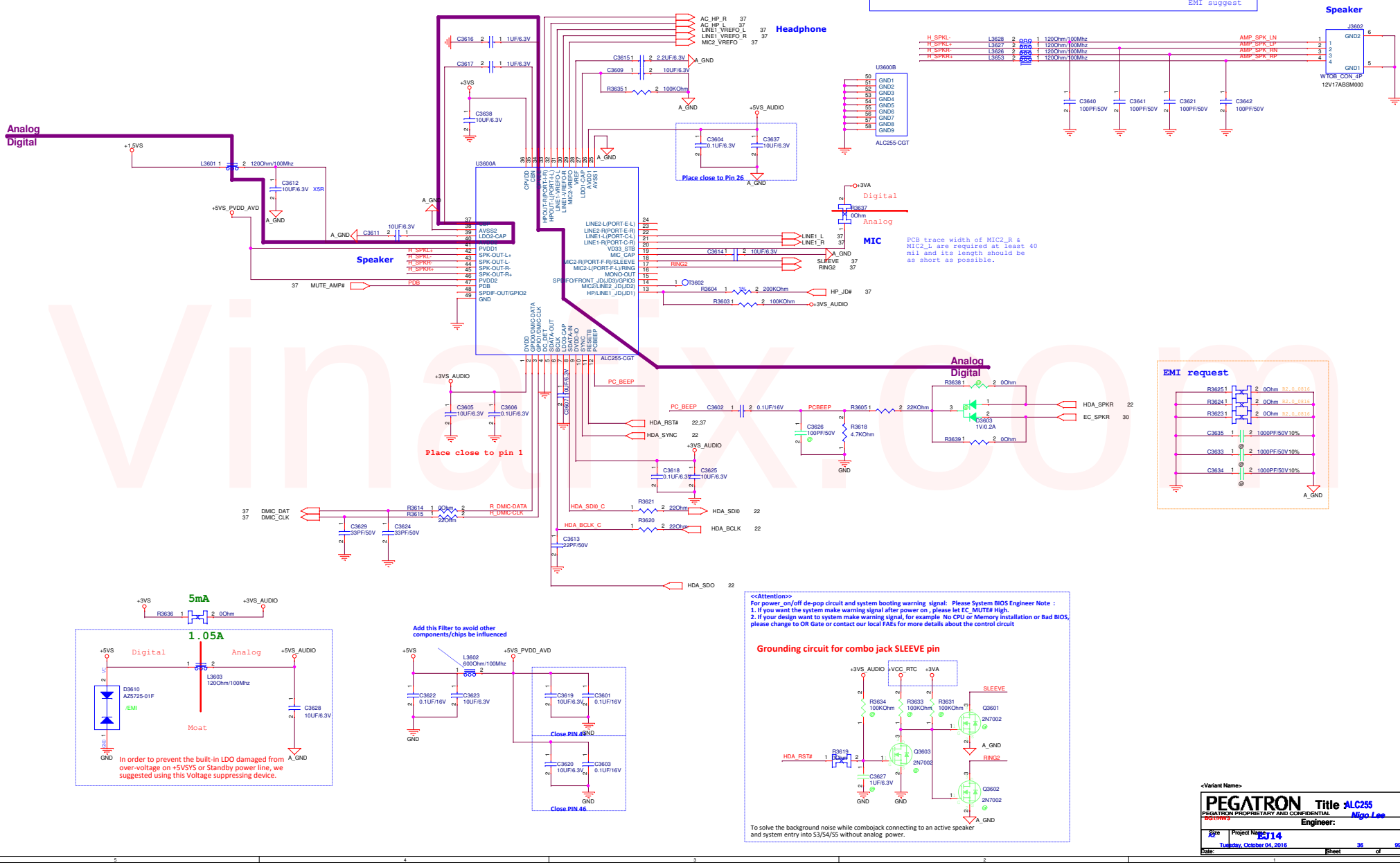
EMI request

Place near chassis GND

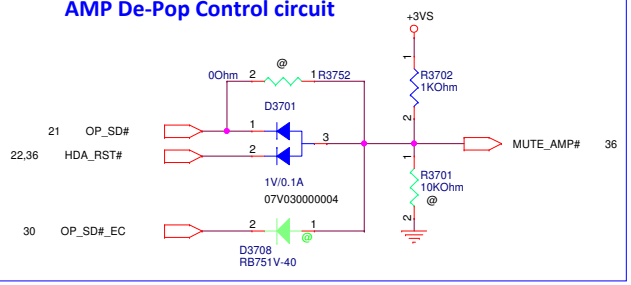
PEGATRON
Title : RJ45
Engineer: Nigo Lee
BG1/HW3
Size: Custom
Project Name: EJ14
P/N
Rev: 1.0
Date: Tuesday, October 04, 2016
Sheet 34 of 99

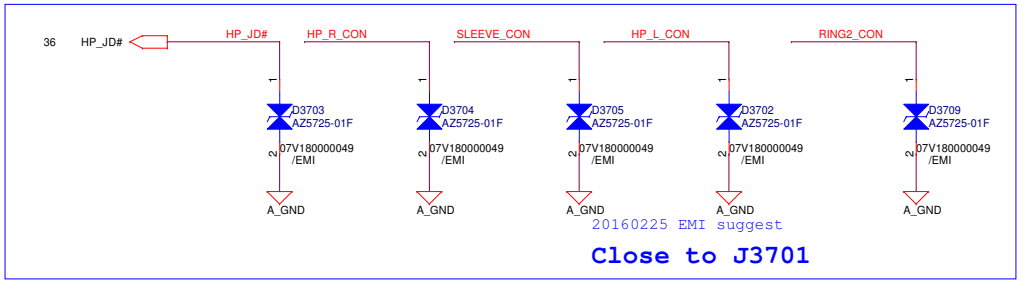
Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 35 of 99	

ALC255 CODEC



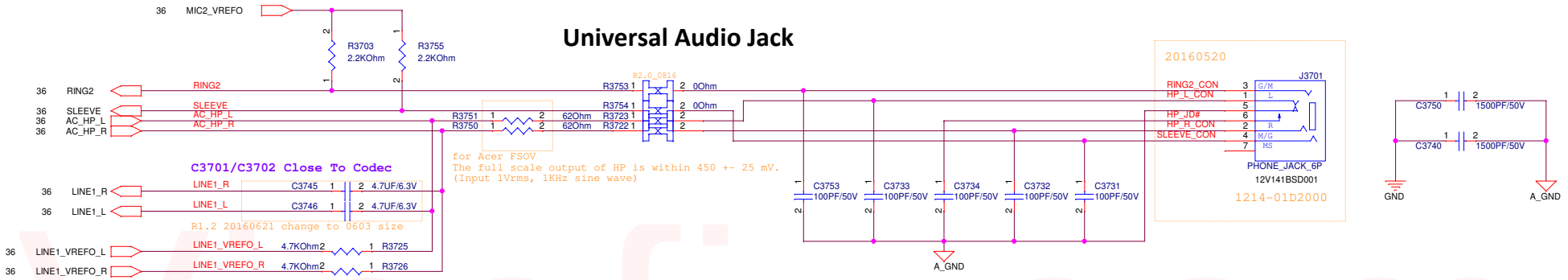
AMP De-Pop Control circuit



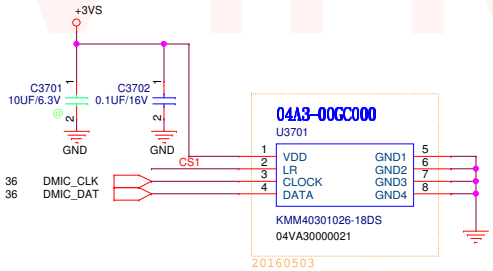


+3VS +3VS 3,4,17,20,21,22,23,24,30,31,32,33,36,40,45,48,50,51,52,53,57,61,91,92

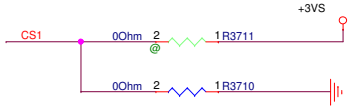
Universal Audio Jack

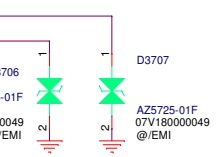


DMIC



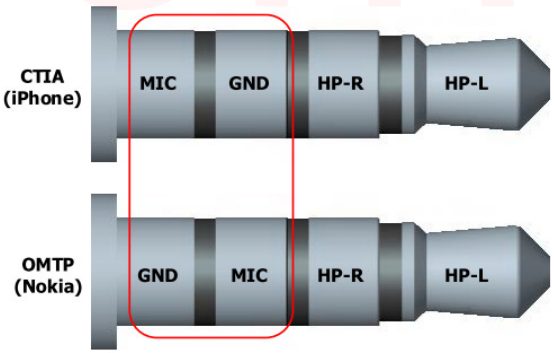
Single MIC	Left Channel	Right Channel
CS Pin	Pull Down	Pull Up





Global Headset

ALC255 embedded hardware auto-switch to switch to switch Microphone signal and reference GND to support OMTP(Nokia type) and CTIA(iPhone type) headset in the same physical phone jack.

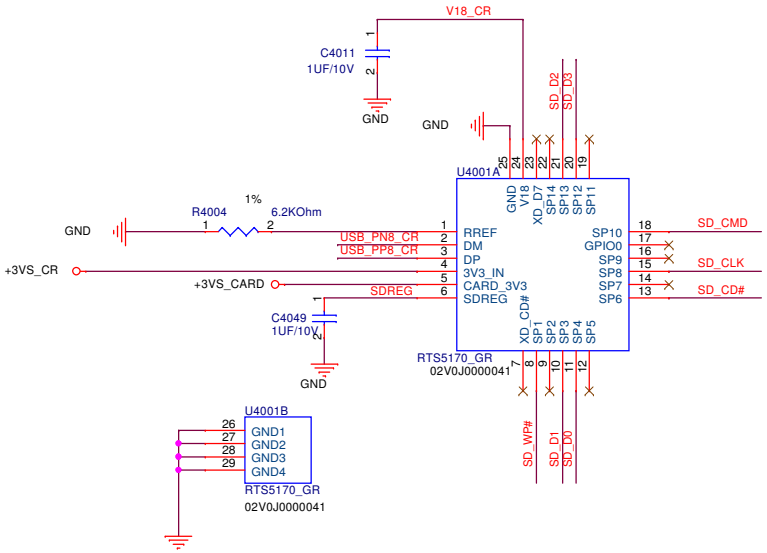


<Variant Name>

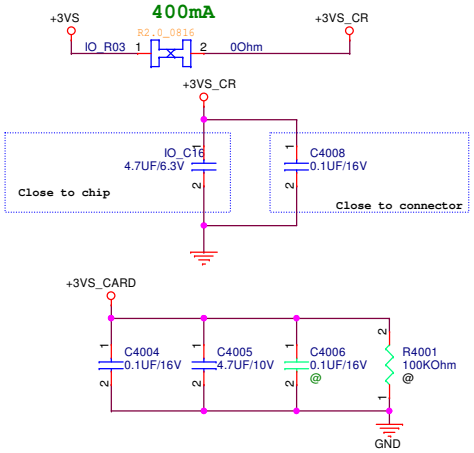
PEGATRON Title COMBO_JACK
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3
Engineer: Nigo Lee
Size: Custom | Project Name: EJ14 | Rev: 1.0
Date: Tuesday, October 04, 2016 | Sheet 37 of 99

Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 38 of 99	

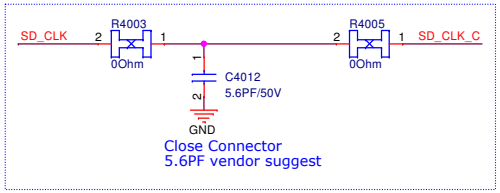
Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 39 of 99	



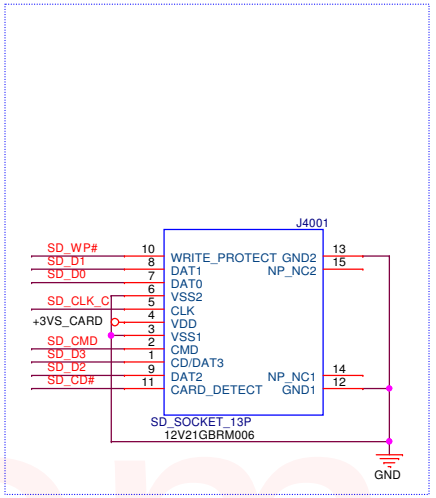
Power Budget is around 400mA.



Card SCLK Slew Rate Control

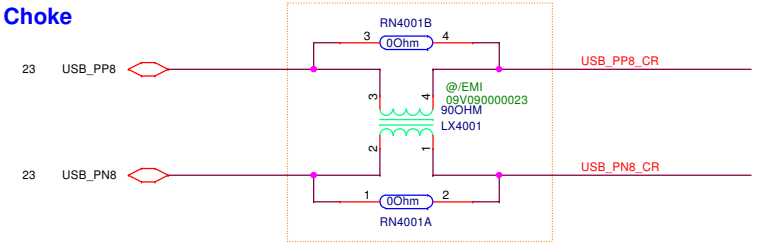


Card Socket



20160519
Swap for layout

Card Reader USB Choke



EMI request

PEGATRON	Title : 40. card reader		
BG1/HW3	Engineer: Nigo Lee		
Size: Custom	Project Name: EJ14		Rev: 1.0
Date: Tuesday, October 04, 2016	Sheet 40 of 99		

<Variant Name>

PEGATRON Title : POWER_FLOWCHART

Engineer: Nigo Lee

Size	Project Name	Rev
C	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 41 of 99

<Variant Name>

PEGATRON Title POWER_FLOWCHART

Engineer: Nigo Lee

Size	Project Name	Rev
D	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 82 of 88

PEGATRON

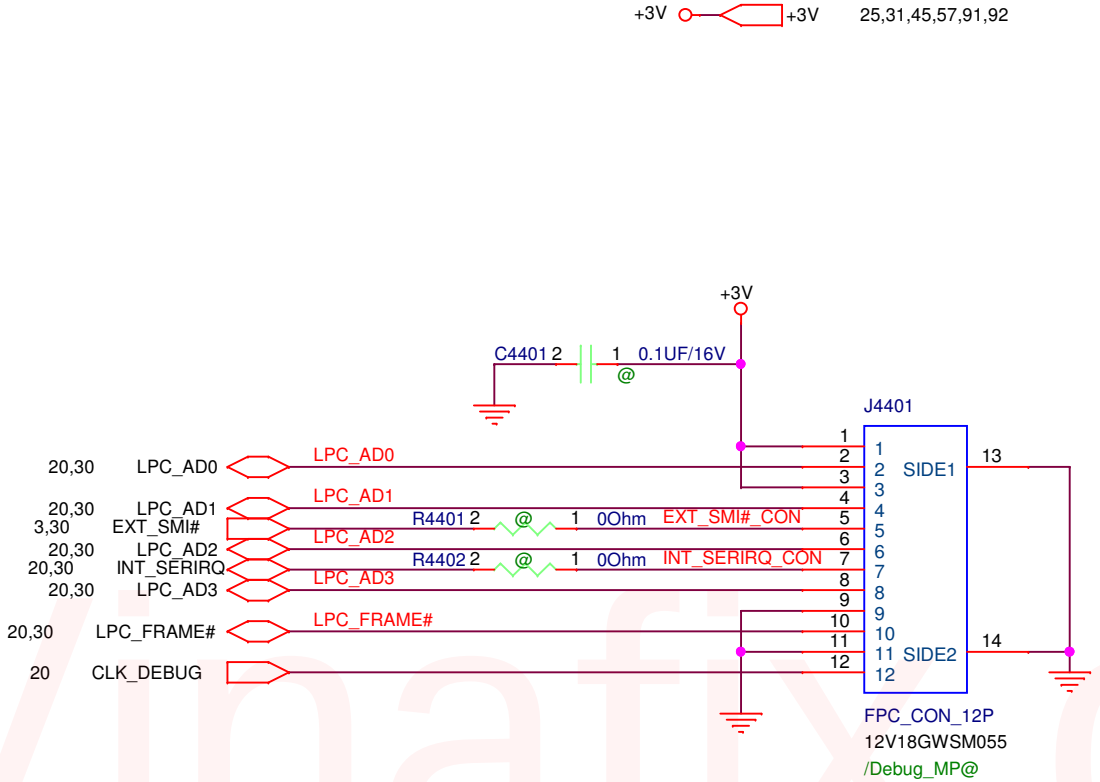
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Dead Battery

Engineer: Nigo Lee

Size	Project Name	Rev
A	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 43 of 99



<Variant Name>

PEGATRON

Title : BUG_Debug

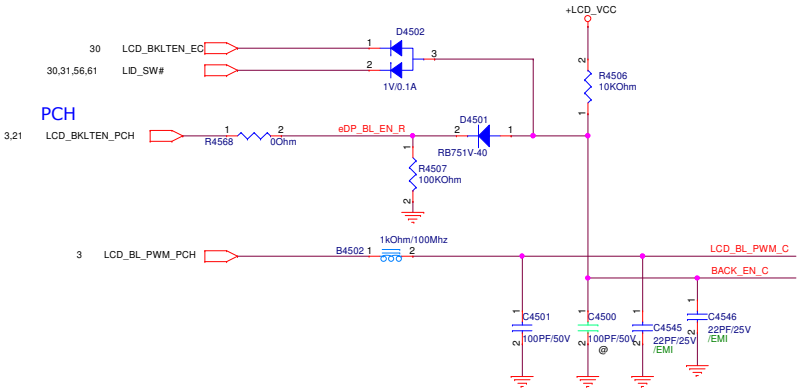
Engineer: Nigo Lee

BG1/HW3

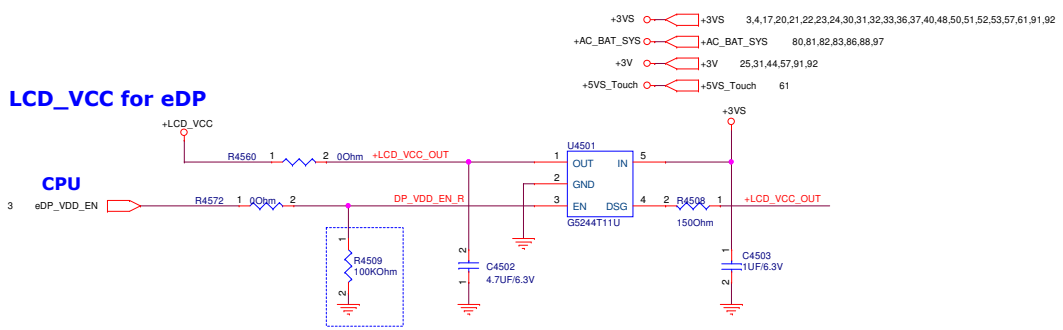
Size	Project Name	Rev
Custom		1.0

Date: Tuesday, October 04, 2016 Sheet 44 of 99

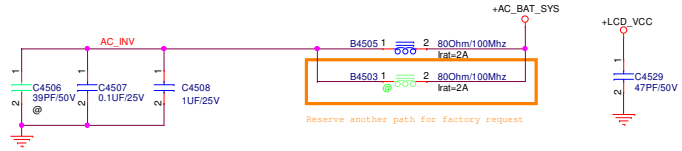
Controller circuit



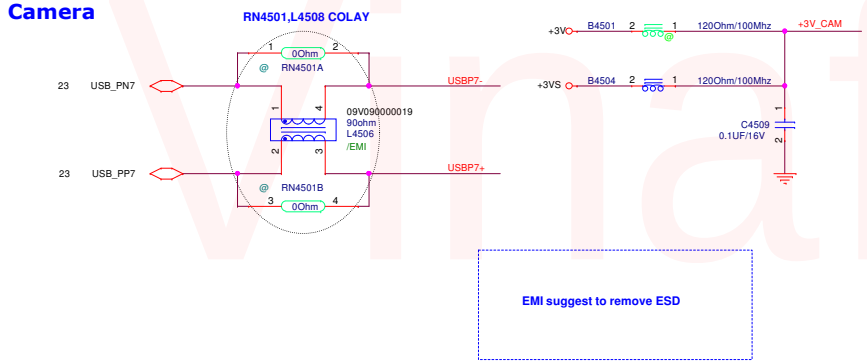
LCD_VCC for eDP



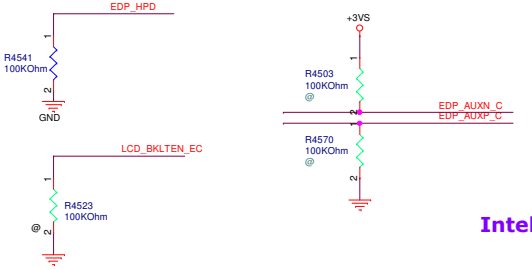
Check PCH/FCH or CPU PD



Camera



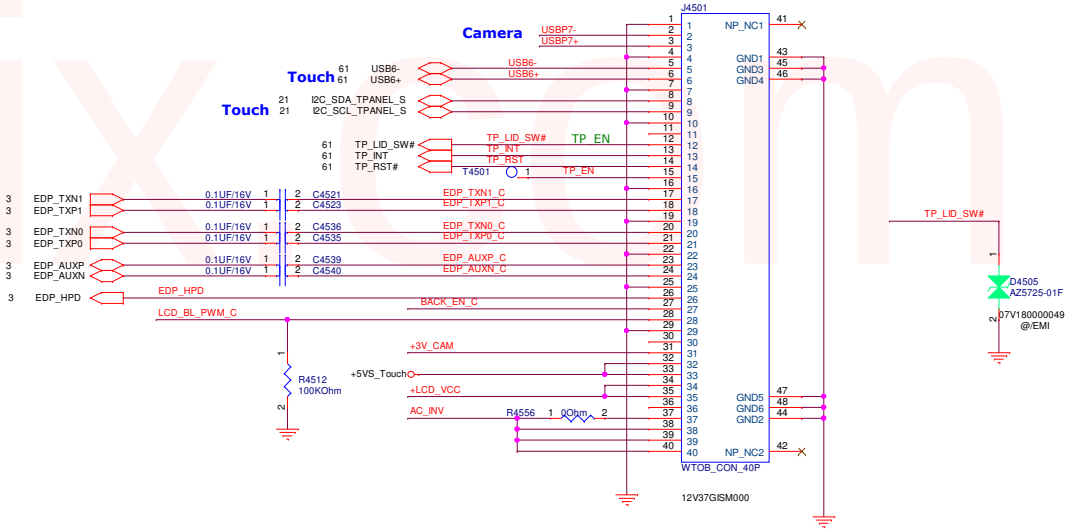
eDP HPD



Intel Solution

eDP Connector

NOTE:
Entire trace of Panel_VCC & LCD_VCC should be wider than 80-mil



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : LVDS Out
BG1/HW3
Engineer: Nigo Lee
Size: Custom | Project Name: EJ14 | Rev: 1.0
Date: Tuesday, October 04, 2016 | Sheet 45 of 99

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : CRT RTD2166

Engineer: Nigo Lee

BG1/HW3

Size	Project Name	Rev
C	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 46 of 99

PEGATRON Title : DP_SWITCH

PEGATRON PROPRIETARY AND CONFIDENTIAL

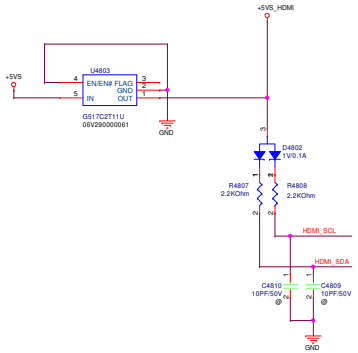
Engineer: Nigo Lee

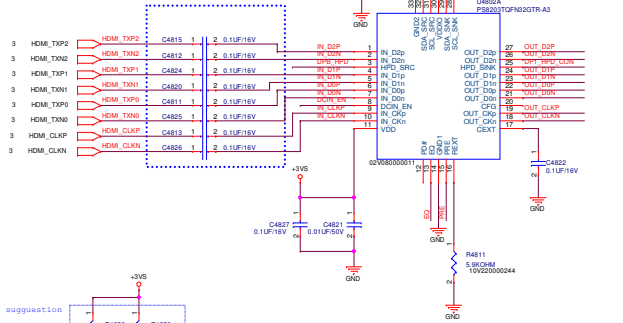
BG1/HW3

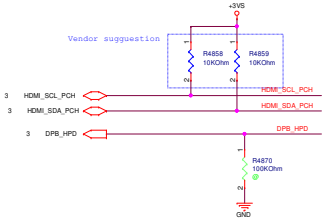
Size	Project Name	Rev
C	EJ14	1.0

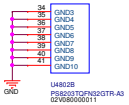
Date: Tuesday, October 04, 2016 Sheet 47 of 99

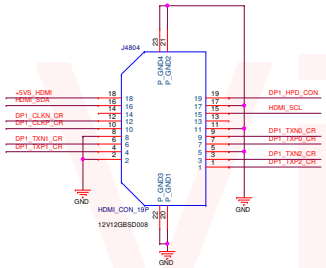
HDMI

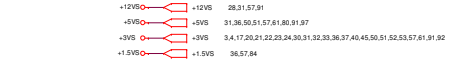


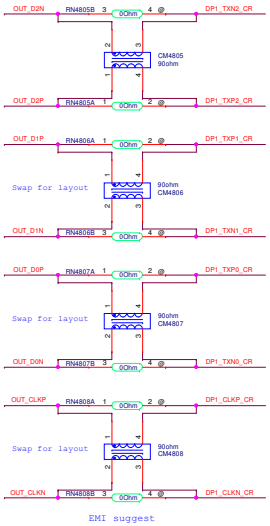








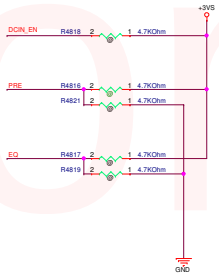




Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 2.5dB pre-emphasis

Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
M: programmable EQ for channel loss up to 8.6dB @ 3Gbps

DC coupling enable; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input



<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : HDMI-4K2K
BG1-HW3
Engineer: Nigo Lee
Size: Custom
Project Name: EJ14
Rev: 1.0
Date: Tuesday, October 04, 2016
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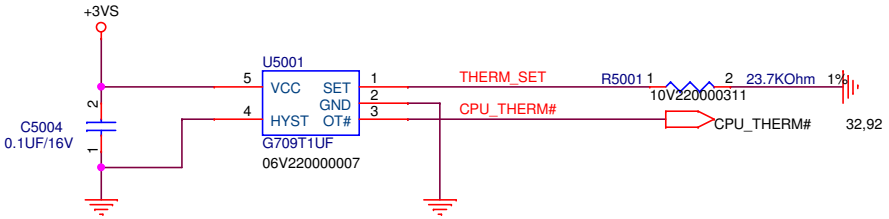
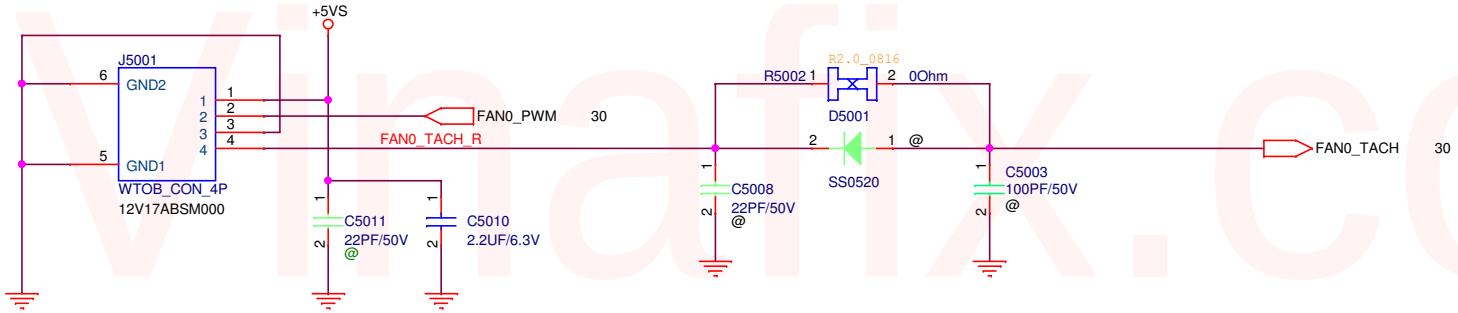
Title	eMMC	
Size B	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 49 of 99	

+3VS +3VS 3,4,17,20,21,22,23,24,30,31,32,33,36,37,40,45,48,51,52,53,57,61,91,92

+5VS +5VS 31,36,48,51,57,61,80,91,97





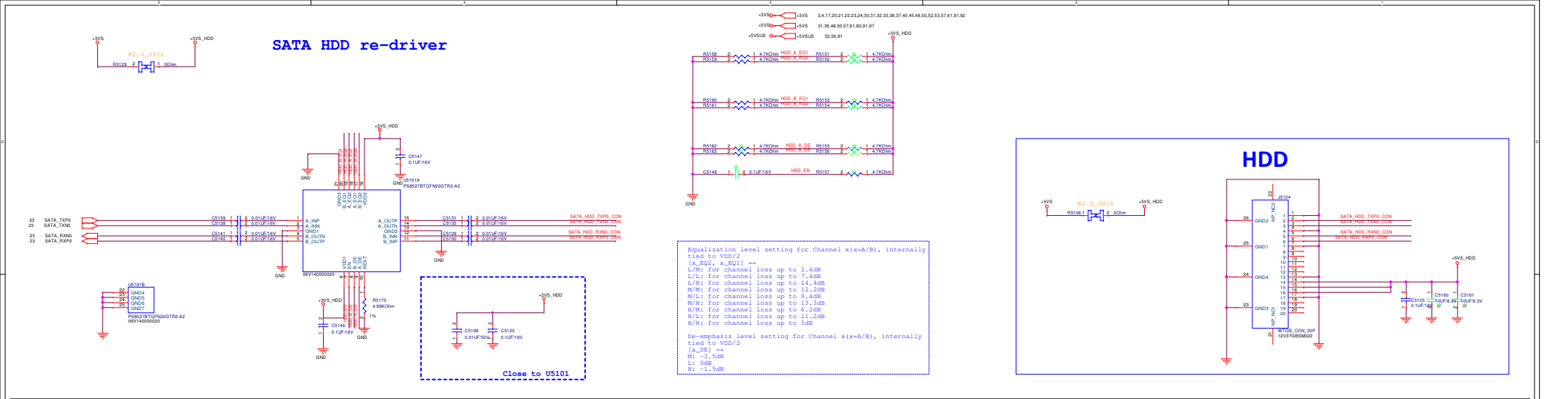
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BGM/HWS

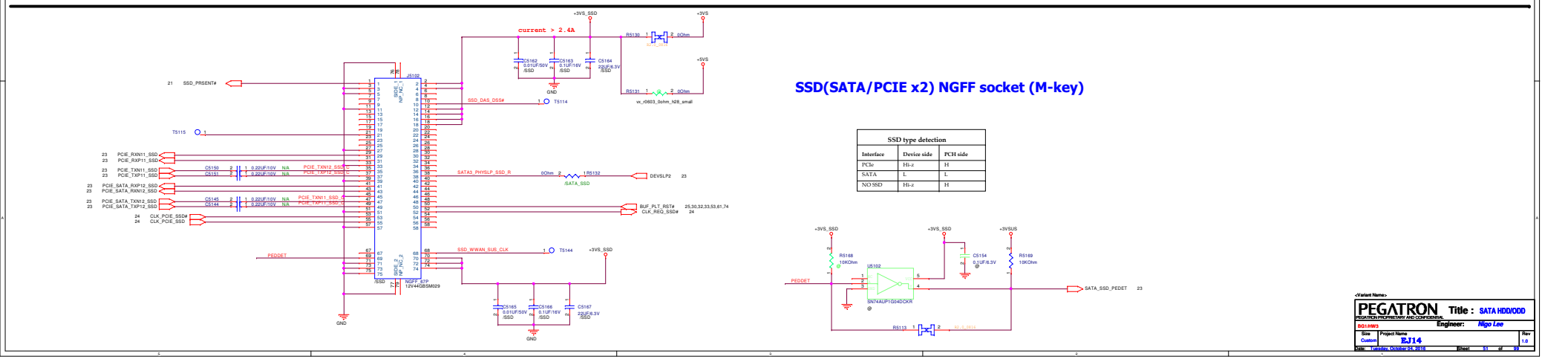
Title: THERMAL/ FAN

Engineer: Nigo Lee

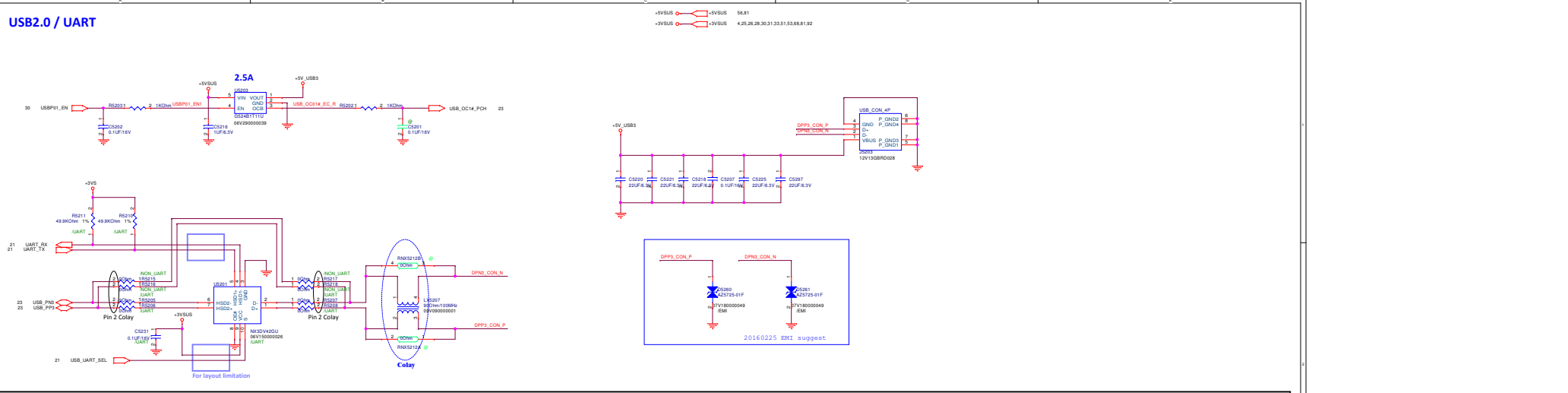
Size	Project Name	Rev
Custom	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 50 of 99

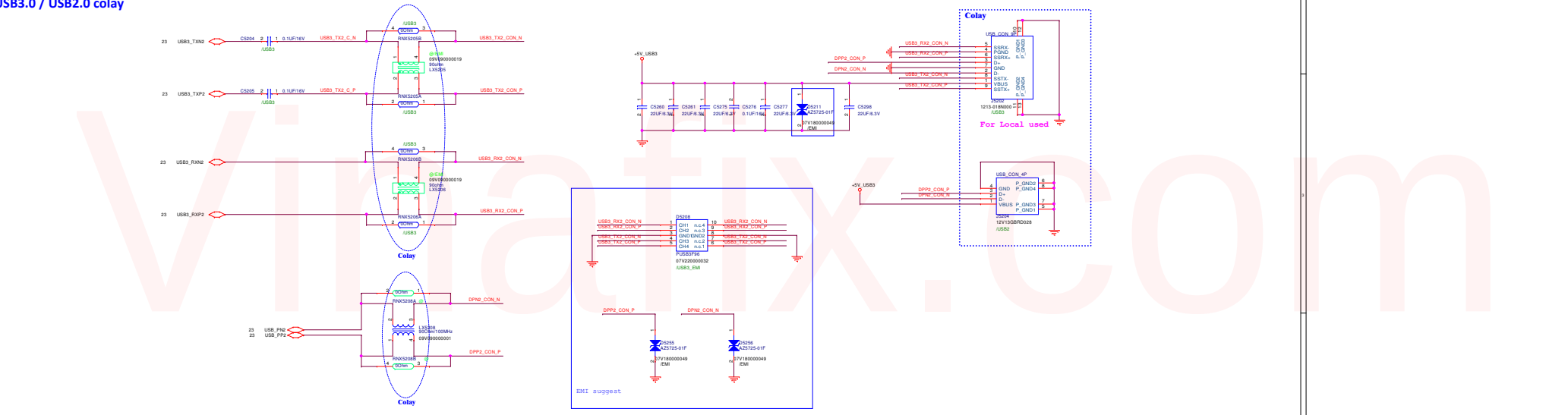

SATA HDD re-driver
HDD
Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
[x_EQ2, x_EQ1] ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB
De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
[X_DE] ==
M: -3.5dB
L: 0dB
H: -1.5dB
Close to U5101


SSD(SATA/PCIE x2) NGFF socket (M-key)
current > 2.4A
SSD type detection
Interface | Device side | PCH side
PCIe | Hi-z | H
SATA | L | L
NO SSD | Hi-z | H

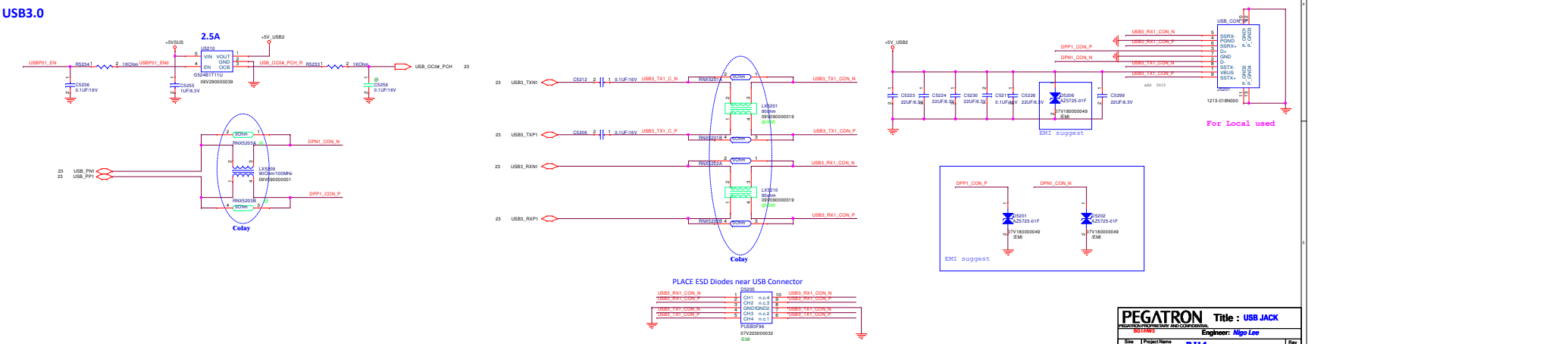
USB2.0 / UART



USB3.0 / USB2.0 colay



USB3.0



Title :	USB JACK
Engineer:	Nigo Lee
Size:	Custom
Project Name:	EJ14
Rev:	1.0
Date:	Tuesday, October 04, 2016
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WLAN / BT

+3V_WLAN_WP1 bypass capactor:
Place 0.1UF near pin 2,4

Place 10UF near +3V_WLAN_WP1 source side.

C5300 10UF/6.3V
C5307 0.1UF/6.3V
C5306 0.01UF/25V
C5303 10PF/50V
C5349 68PF/50V
C5350 82PF/50V
RF request

+3V_WLAN_WP1 bypass capactor:
Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.

C5347 10UF/6.3V
C5345 0.1UF/6.3V
C5348 0.01UF/25V
C5346 10PF/50V
C5351 68PF/50V
C5352 82PF/50V
RF request

J5301
MINI_PCI_67P
12V44GBSM037
R2.0_KBL_0902

C5332 39PF/50V

USBP5_C
USBN5_C
RN5301A 1 0Ohm 2
RN5301B 3 0Ohm 4
09V090000019 90ohm L5301
USB_PP5 23
USB_PN5 23

PCIE_TXP_WLAN 23
PCIE_TXN_WLAN 23
PCIE_RXP_WLAN 23
PCIE_RXN_WLAN 23
CLK_PCIE_WLAN 24
CLK_PCIE_WLAN# 24
PCIE_WAKE#_WLAN

R5334 10KOhm @ R5334 Close To Connector
CLK_WLAN_REQ# 24

R5315 10KOhm
R5316 10KOhm
CL_RST# 20
CL_DAT 20
CL_CLK 20
R5322
R5323
R5324

T5301
T5302
T5303
T5308
T5304
T5305
T5306
T5307

PLT_RST#_WLAN
BT_ON/OFF#_H
WLAN_ON_H

30 BT_ON/OFF#_EC
R5302 @ 0Ohm
21 BT_ON/OFF#
R5341 R2.0_0816
D5301 RB751V-40
BT_ON/OFF#_C
SP5301
SP5302
21 WLAN_ON
R5317 R2.0_0816
D5302 RB751V-40
WLAN_ON_C

PCIE_WAKE# Pull High To +VCCDSW (+3VSUS_ORG)
25 PCIE_WAKE#
30 WLAN_WAKE#
D5305 RB751V-40
Q5311 2N7002
R5391 100KOhm @
R5333 /IOAC 0Ohm

25,30,32,33,51,61,74 BUF_PLT_RST#
0Ohm SP5306
R5343 10KOhm @
PLT_RST#_WLAN
D5304 1.2V/0.1A
30 WLAN_RST#_EC
0Ohm R5344

For USI W0096 Module Card
CL_RST# R5358 @ 0Ohm GND

IOAC Control Schematic

+3VS_WLAN
+3VS
500mA
JP5303 1MM_OPEN_M1M2 /NON_IOAC
+3VSUS
Q5313 SI2305CDS-T1-GE3 Rdson=65mOhm,Vgs(th)=-1V /IOAC
+3VA
R5390 10KOhm /IOAC
Q5312B EM6K1 /IOAC
Soft Start
C5341 1UF/6.3V /IOAC
Q5312A EM6K1 /IOAC
IOAC_EN 30
R5360 100KOhm /IOAC

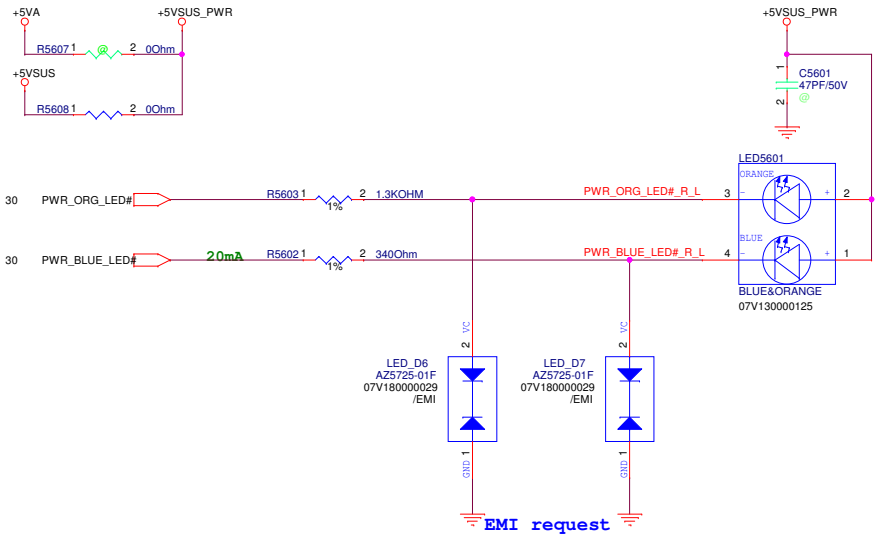
<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : WLAN/ WiGig / BT
Engineer: Nigo Lee
BG1/HW3
Size C | Project Name EJ14 | Rev 1.0
Date: Tuesday, October 04, 2016 | Sheet 53 of 99

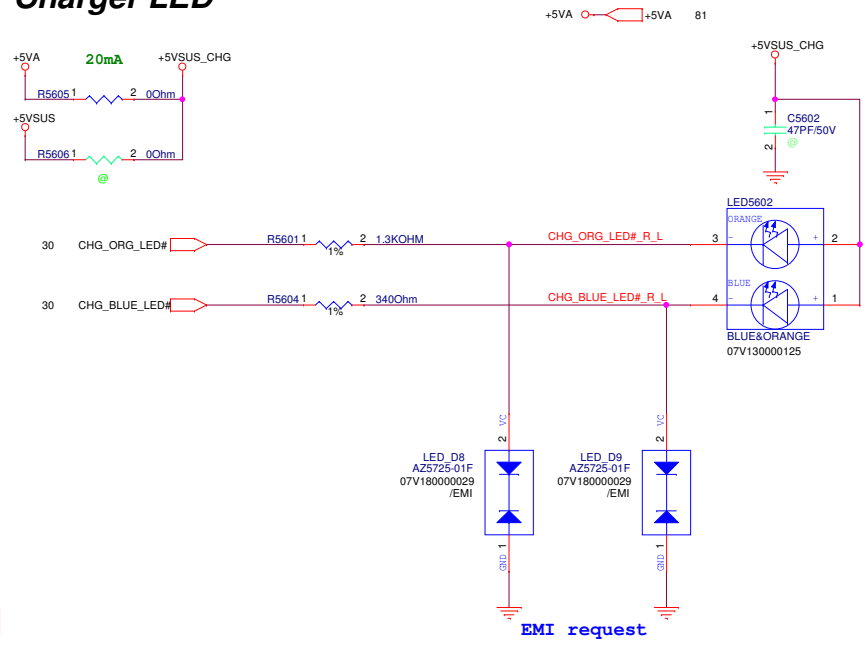
Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 54 of 99	

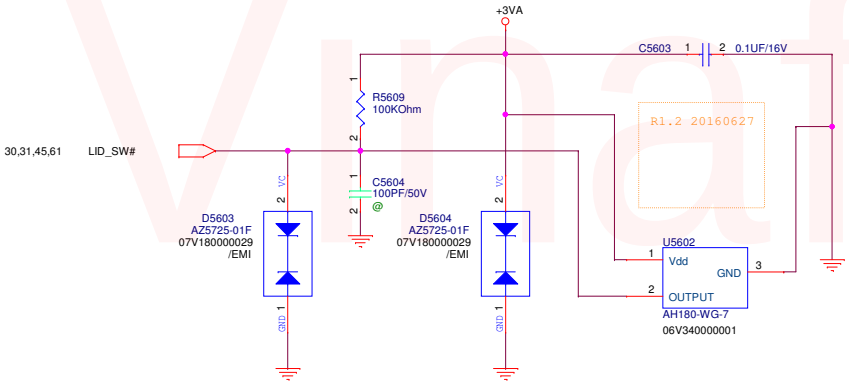
Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 55 of 99	

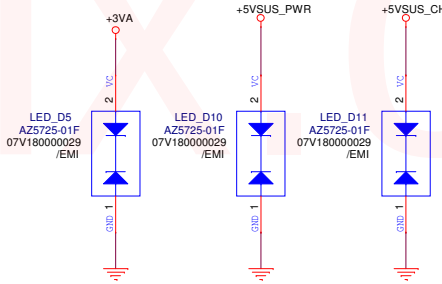
POWER LED



Charger LED







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

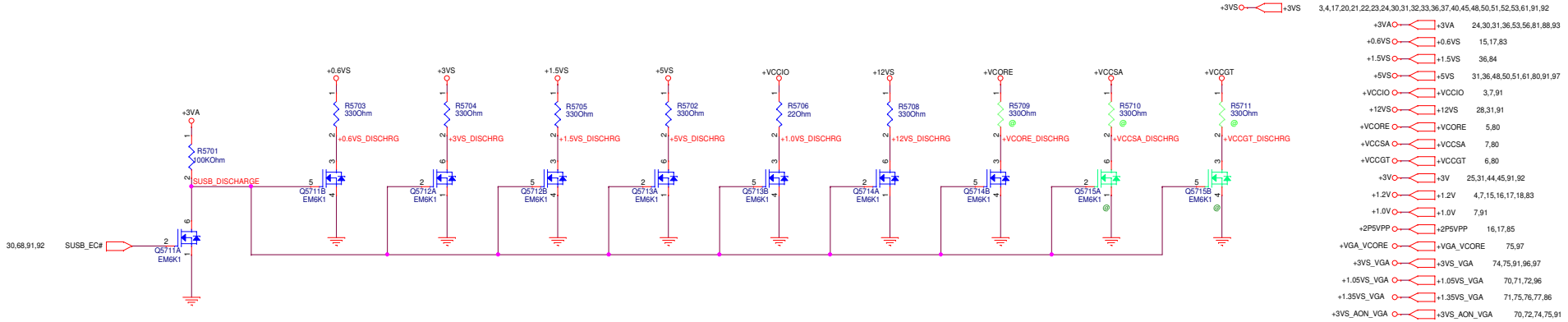
Title : LED

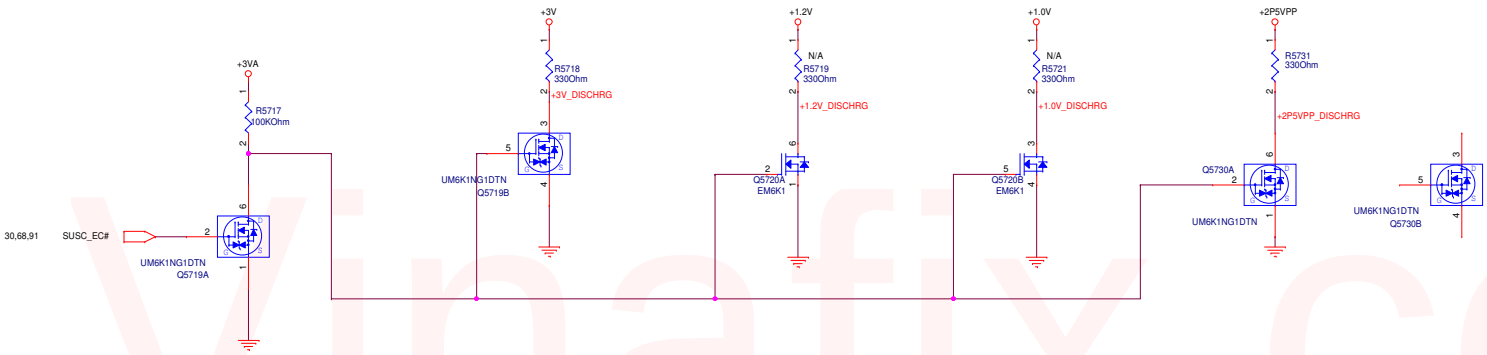
Engineer: Nigo Lee

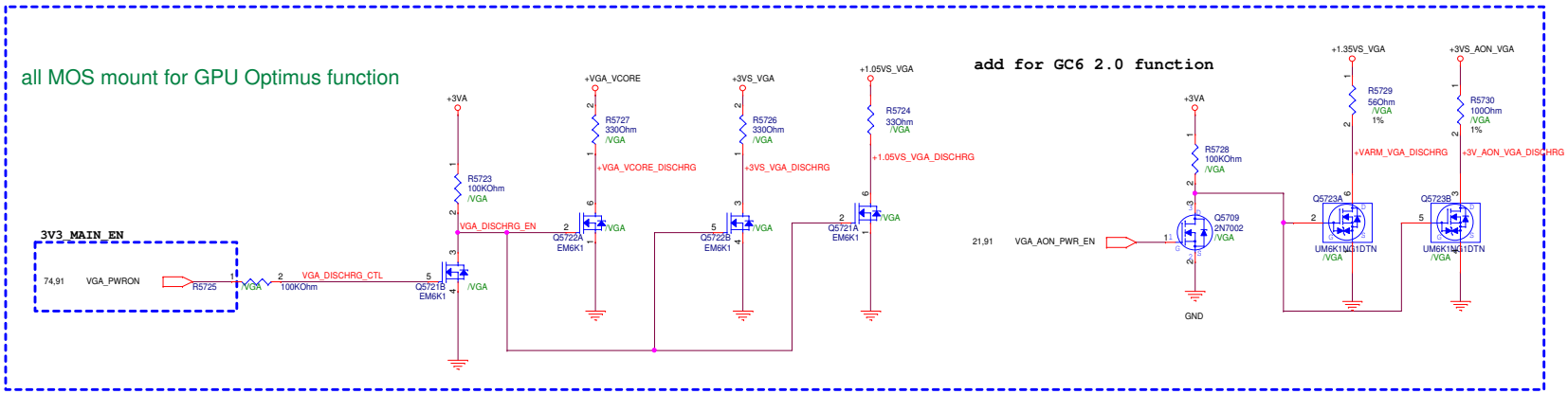
BG1/HW3

Size	Project Name	Rev
Custom	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 56 of 99







PEGATRON Title DSG_Discharge
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Nigo Lee
Size D Project Name EJ14 Rev 1.0
Date: Tuesday, October 04, 2016 Sheet 57 of 99

Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 58 of 99	

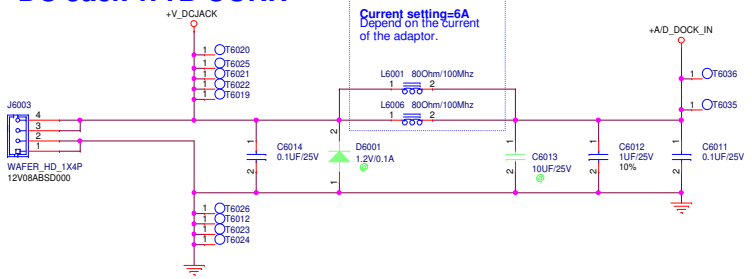
Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 59 of 99	

DC_BAT_CONN

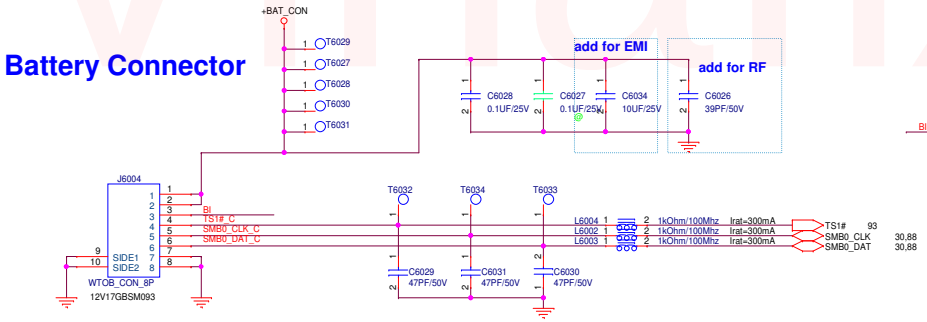
+VCC_RTC +VCC_RTC 24,25,26,36
+3VA_EC +3VA_EC 28,30,32
+3VA +3VA 24,30,31,36,53,56,57,81,88,93
+5VA +5VA 56,81
+1.0VSUS +1.0VSUS 26,82
+1.8VSUS +1.8VSUS 9,24,26,84
+3VSUS +3VSUS 4,25,26,28,30,31,33,51,52,53,68,81,92
+5VSUS +5VSUS 52,56,81
+12VSUS +12VSUS 81,91
+3V +3V 25,31,44,45,57,91,92
+12V +12V 91

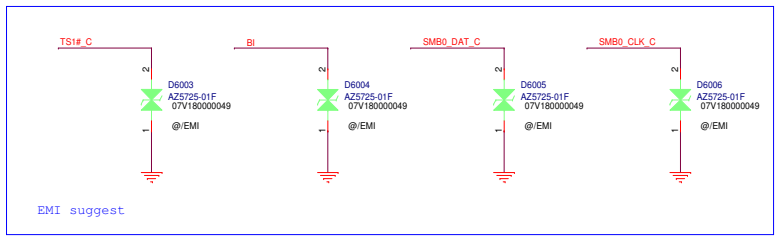
+3VS +3VS 3,4,17,20,21,22,23,24,30,31,32,33,36,37,40,45,48,50,51,52,53,57,61,91,92
+5VS +5VS 31,36,48,50,51,57,61,80,91,97
+12VS +12VS 28,31,57,91
+AC_BAT_SYS +AC_BAT_SYS 45,80,81,82,83,86,88,97
+A/D_DOCK_IN +A/D_DOCK_IN 88
+BAT_CON +BAT_CON 88
+VCORE +VCORE 5,57,80
+VCCGT +VCCGT 6,57,80
+VCCSA +VCCSA 7,57,80
+VCCIO +VCCIO 3,7,57,91
+RTCBAT +RTCBAT 24

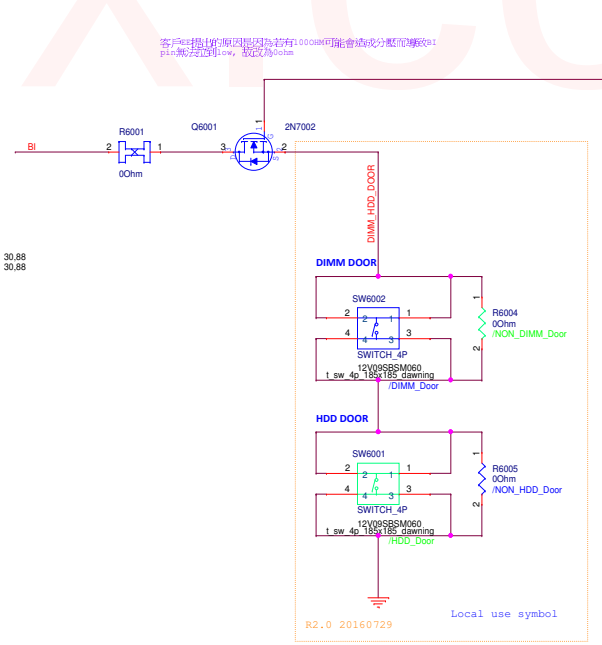
DC Jack WTB CONN

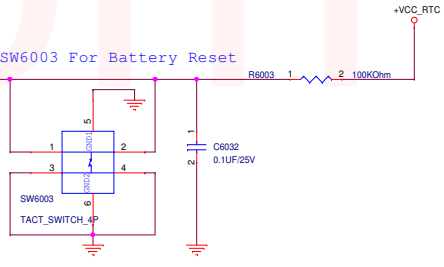


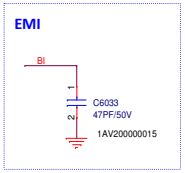
Battery Connector



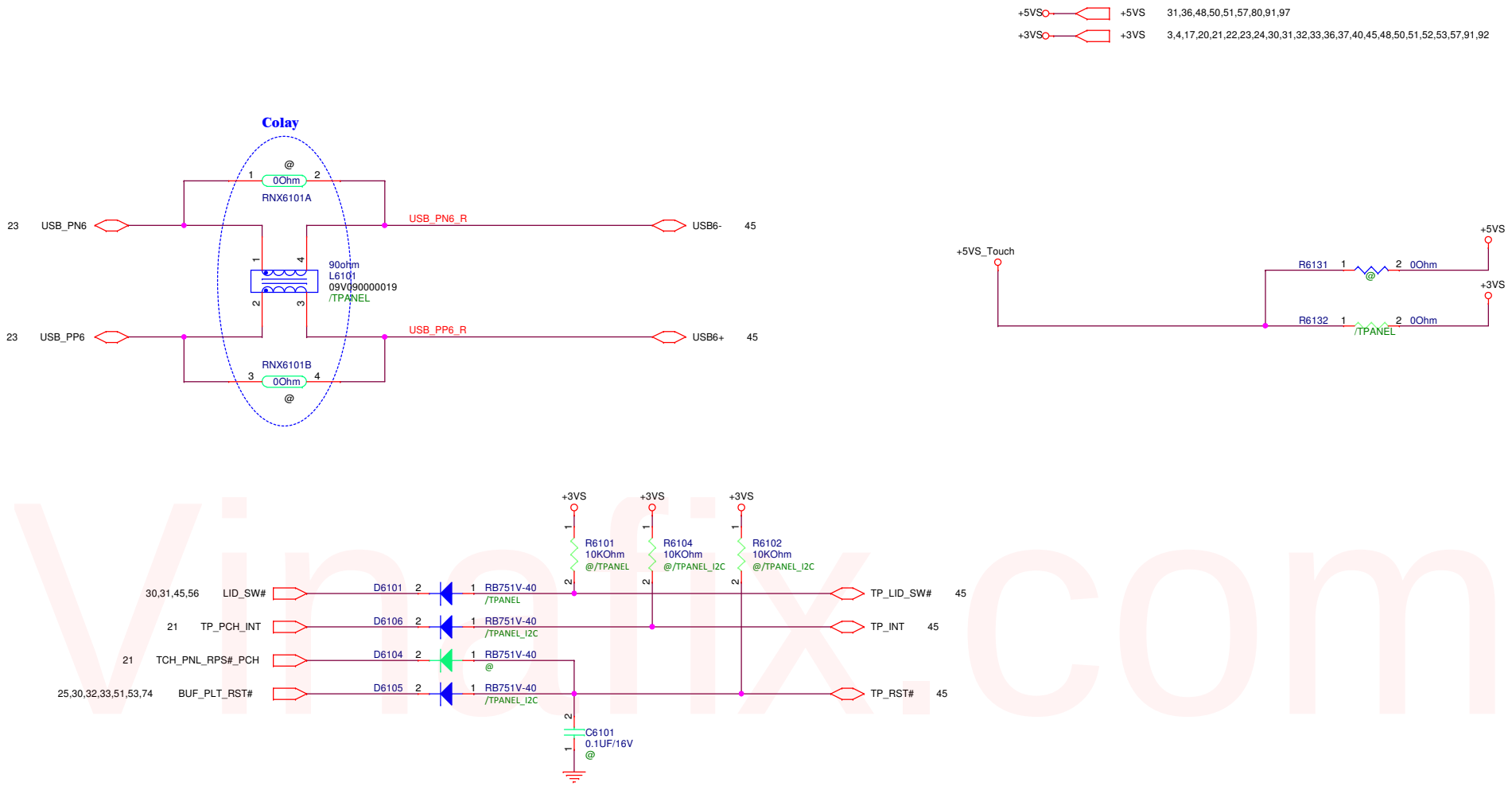








PEGATRON Title : DC_BAT_CONN
BG1/HW3 Engineer: Nigo Lee
Size C | Project Name EJ14 | Rev 1.0
Date: Tuesday, October 04, 2016 | Sheet 60 of 99



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Touch Panel Conn

BG1/HW3

Engineer: Nigo Lee

Size	Project Name	Rev
Custom		1.0

Date: Tuesday, October 04, 2016 Sheet 61 of 99

<Variant Name>

PEGATRON Title :TPM

Engineer: Nigo Lee

BG1/HW3

Size	Project Name	Rev
C	EJ14	1a

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Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 63 of 99	

<Variant Name>

PEGATRON Title : G-Sensor

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Nigo Lee

Size	Project Name	Rev
D	EJ14	1.0

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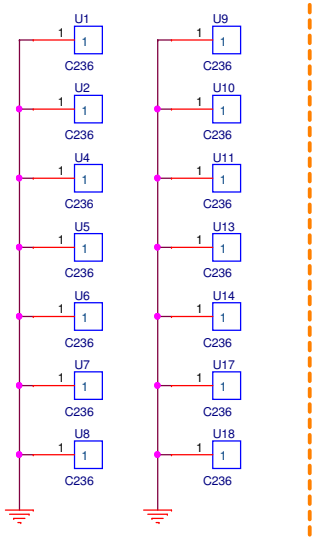
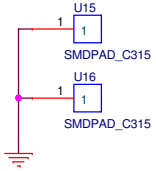
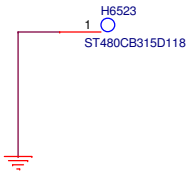
CU





WLAN NUT

A



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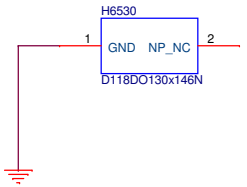

J 定位孔

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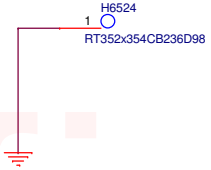

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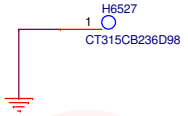
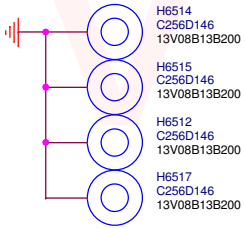
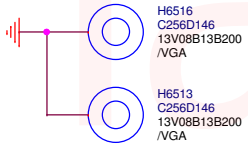


K 定位孔

BGA 1308-00BG000
CPU NUTx4



BGA 1308-00BG000
GPU NUTx2



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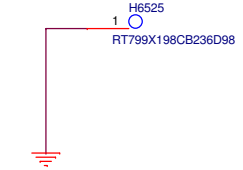

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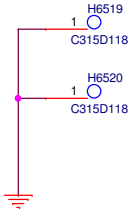

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : ME_CONN,Skew Hole
Engineer: Nigo Lee

Size	Project Name	Rev
B	EJ14	1.0
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PWR BRD

+5VA	+5VA	56,81
+3VA	+3VA	24,30,31,36,53,56,57,81,88,93

PEGATRON Title: PWR BRD/ IO BRD

PEGATRON PROPRIETARY AND CONFIDENTIAL

BGT/HW3

Engineer: Nigo Lee

Size	Project Name	Rev
B	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 66 of 99

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : MLB to IO

Engineer: Nigo Lee

BG1/HW3

Size	Project Name	Rev
Custom	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 67 of 99

+3VSUS +3VSUS 4,25,26,28,30,31,33,51,52,53,81,92

+3VA +3VA 24,30,31,36,53,56,57,81,88,93

25,30 PM_SUSB# R6801 1 2 R2.0_0816 SUSB_EC# 30,57,91,92

25,30 PM_SUSC# R6802 1 2 R2.0_0816 SUSC_EC# 30,57,91

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

Delay By EC(2ms+ EC processing time (3ms~33ms)

30 DE_ALL_SYS_PGD_EC R6809 1 2 R2.0_0816

+3VSUS

U6802
1 A VCC 5
PM_SUSB# 2 B
3 GND Y 4
Vcc=2~5.5

DE_ALL_SYS_PGD_HW 30

For shut down Sequence

R6808 1
@100KOhm
10V240000005 2
GND

C6804 1
0.1UF/16V
@ 2
GND

30 SYS_PWROK_EC SP6802 1 2 SYS_PWROK_EC_G

+3VSUS

U6803
PM_SUSB# 1 A VCC 5
2 B
3 GND Y 4
Vcc=2~5.5

R6804 1 2 R2.0_0816 SYS_PWROK 25,30

For shut down Sequence

R6806 1
@100KOhm
10V240000005 2
GND

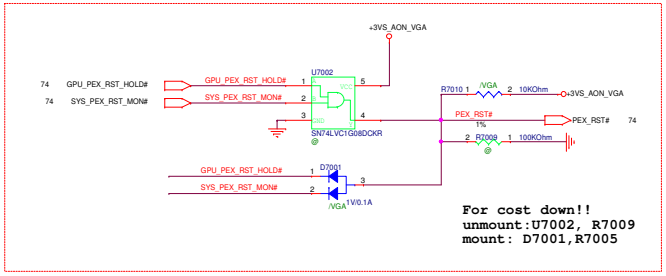
<Variant Name>

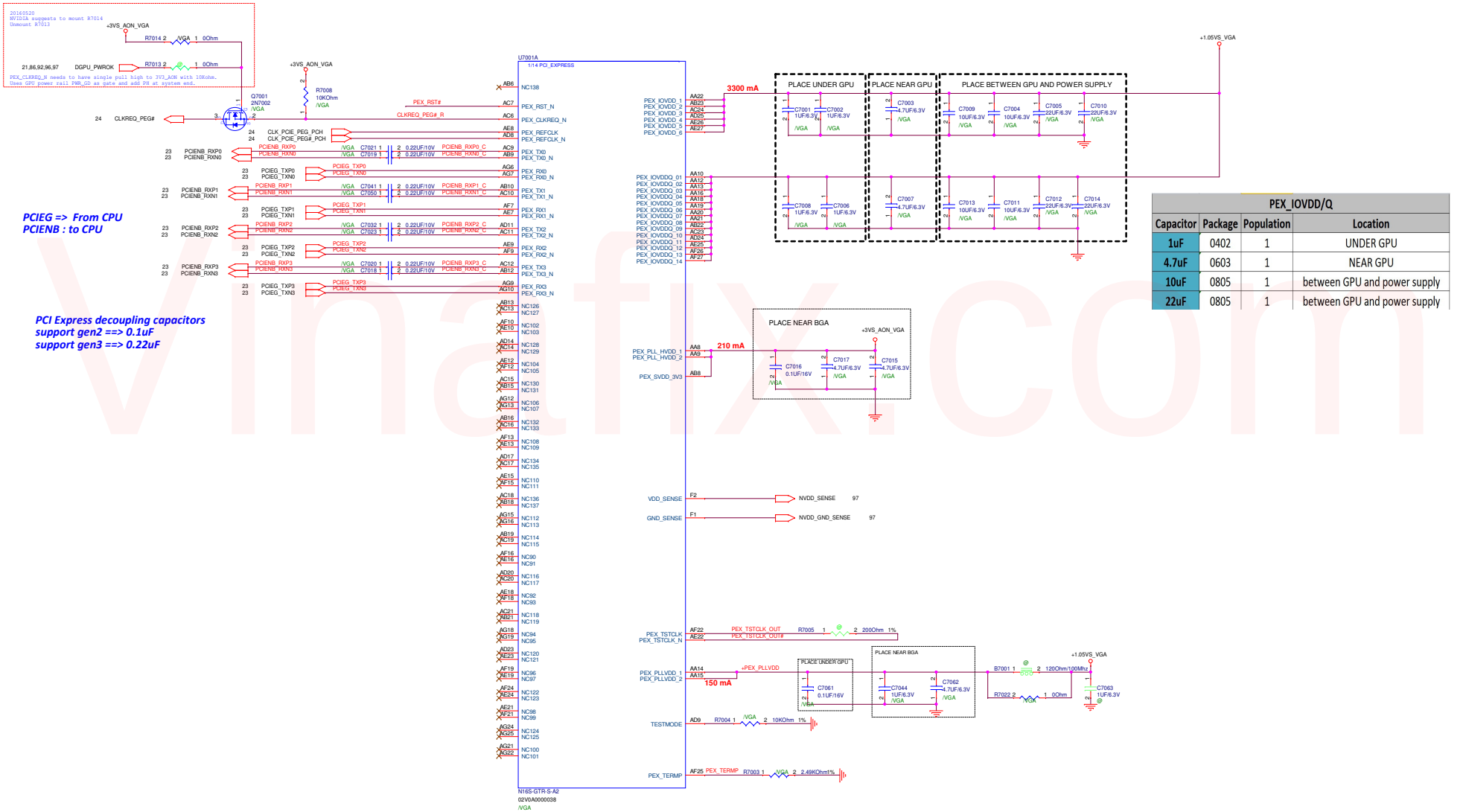
PEGATRON Title :
PEGATRON PROPRIETARY AND CONFIDENTIAL
<Title> Engineer:

Size	Project Name	Rev
B	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 68 of 99

Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
Date: Tuesday, October 04, 2016	Sheet 69 of 99	





PEX_IOVDD/Q			
Capacitor	Package	Population	Location
1uF	0402	1	UNDER GPU
4.7uF	0603	1	NEAR GPU
10uF	0805	1	between GPU and power supply
22uF	0805	1	between GPU and power supply

Title : VGA-PCIE

Engineer: Nigo Lee

Size	Project Name	Rev
Custom	EJ14	1.0

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+1.35VS_VGA → +1.35VS_VGA 57,75,76,77,86

+1.05VS_VGA → +1.05VS_VGA 57,70,72,96

GPU_FB_CLAMP_R R7107 2 — 1 0Ohm — GC6_FB_EN 21,74,86

FB_CLAMP F3 **35 mA** — R7106 2 /VGA 1% — 1 10KOhm

For GM10x / GK10 x GC6K
1. Stuff R7107
2. NO Stuff R7160

For GM10x GC6M (P5HCJ_KBL this mode)
1. NO Stuff R7107
2. Stuff R7106

NVIDIA Design Guide
DG-07158-001_v05 P.117
Table 6-3

	LOWER 0..31	UPPER 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA2	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A9_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA2
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A9_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

U7001B 2/14 FBA

76 FBAD[0..31] — FBAD0 E18 … FBAD63 W25 — FBA_D0 … FBA_D63

77 FBAD[32..63]

76,77 FBA_DBI[0..7] — FBA_DBI0 D19 … FBA_DBI7 U25 — FBA_DQM0 … FBA_DQM7

76,77 FBA_EDC[0..7] — FBA_EDC0 E19 … FBA_EDC7 T26 — FBA_DQS_WP0 … FBA_DQS_WP7

F19, C14, A16, A22, P25, W22, AB27, T27 — FBA_DQS_RN0 … FBA_DQS_RN7

FBA_CMD[0..15] 76 — FBA_CMD0 C27 … FBA_CMD15 J26 — FBA_CMD0 … FBA_CMD15

FBA_CMD[16..31] 77 — FBA_CMD16 M24 … FBA_CMD31 J26 — FBA_CMD16 … FBA_CMD31

B19 FBA_CMD32 — For test/Debug only — +1.35VS_VGA — R7101 1 — 2 60.4Ohm 1% — F22 FBA_CMD34 — R7102 1 — 2 60.4Ohm 1% — J22 FBA_CMD35

FBA_CLK0 D24 / FBA_CLK0_N D25 — FBA_CLK0 76 / FBA_CLK0# 76

FBA_CLK1 N22 / FBA_CLK1_N M22 — FBA_CLK1 77 / FBA_CLK1# 77

FBA_WCK01 D18 / FBA_WCK01_N C18 — FBA_WCK01 76 / FBA_WCK01# 76

FBA_WCK23 D17 / FBA_WCK23_N D16 — FBA_WCK23 76 / FBA_WCK23# 76

FBA_WCK45 T24 / FBA_WCK45_N U24 — FBA_WCK45 77 / FBA_WCK45# 77

FBA_WCK67 V24 / FBA_WCK67_N V25 — FBA_WCK67 77 / FBA_WCK67# 77

FB_PLL_AVDD_1 F16 / FB_PLL_AVDD_2 P22 / FB_DLL_AVDD H22 — **1.05V+-3% 100 mA** — +FB_PLL_AVDD

C7118 0.1UF/16V /VGA — C7104 0.1UF/16V /VGA — C7101 0.1UF/16V /VGA — Place UNDER GPU

B7101 30Ohm/100Mhz /VGA 09V010000029 — C7103 22UF/6.3V /VGA — Place NEAR GPU — +1.05VS_VGA

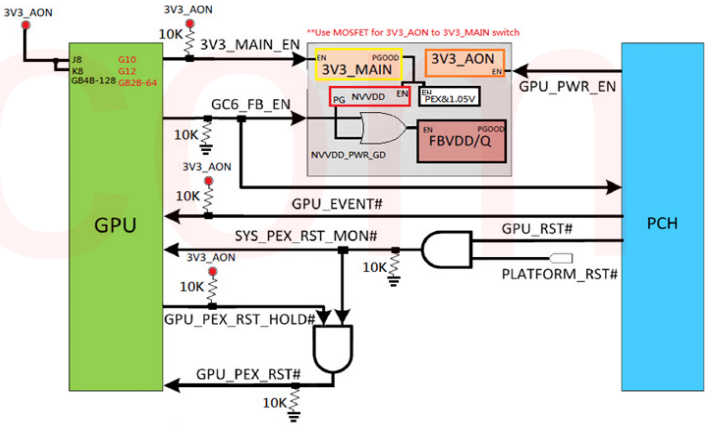
T7101 /VGA — 1 FB_VREF D23 — FB_VREF

N16S-GTR-S-A2
02V0A0000038
/VGA

FBA_CKE — +1.35VS_VGA
FBA_CMD14 R7103 2 /VGA 1 10KOhm 5%
FBA_CMD30 R7104 2 /VGA 1 10KOhm 5%

FBA_RST#
FBA_CMD13 R7154 2 /VGA 1 10KOhm 5%
FBA_CMD29 R7108 2 /VGA 1 10KOhm 5%

VR Complex



GC6 2.0 High-level Signal Connections

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : VGA_N16S-GTR

Engineer: Nigo Lee

Size	Project Name	Rev
C	EJ14	1.0

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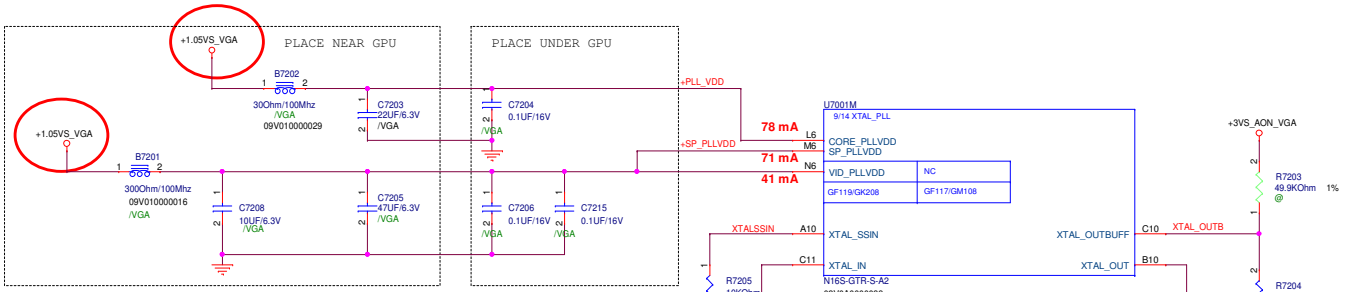
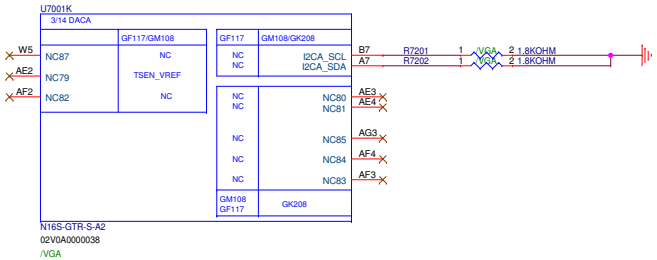
+3VS_AON_VGA → +3VS_AON_VGA 57,70,74,75,91

+1.05VS_VGA → +1.05VS_VGA 57,70,71,96



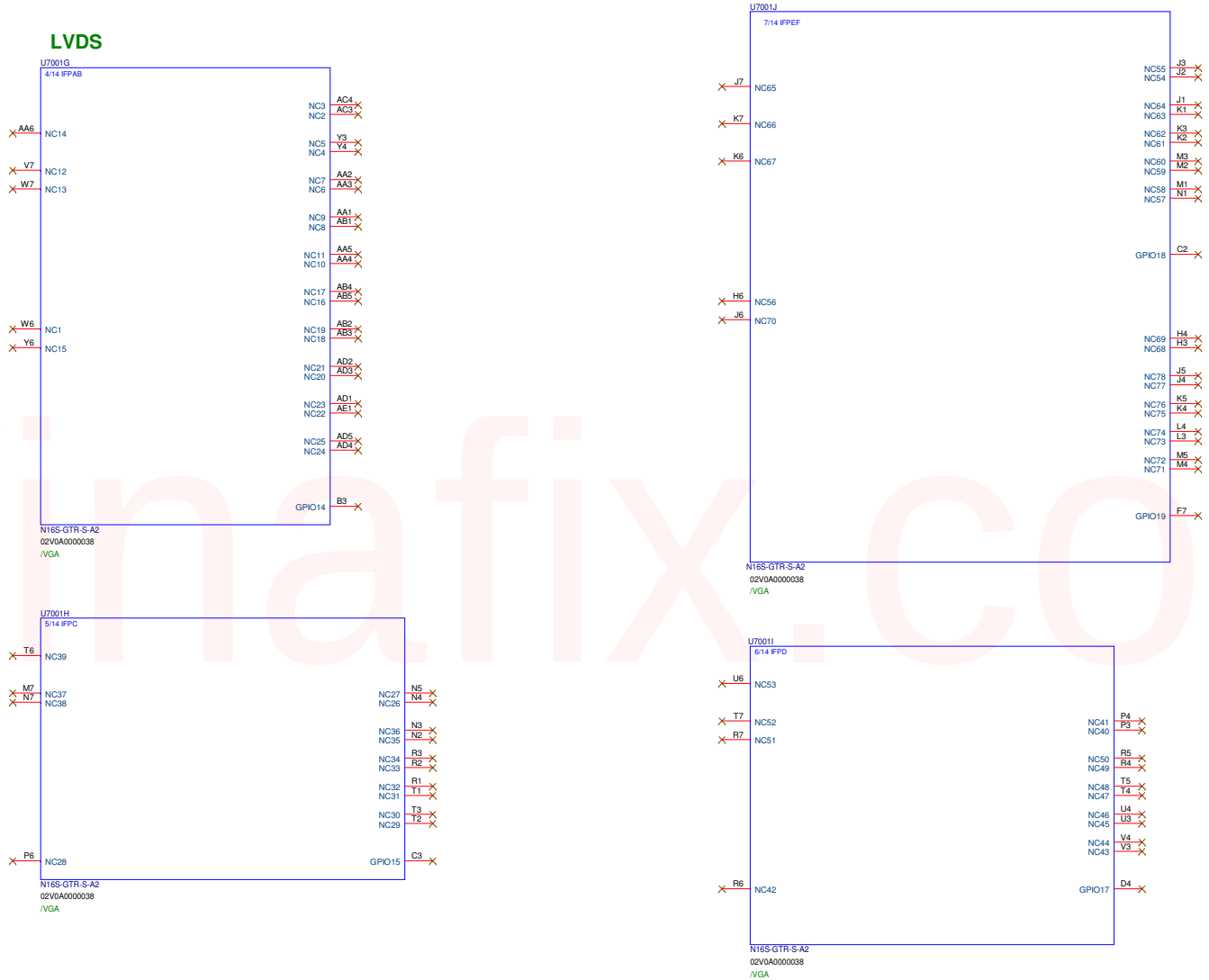
N16x series B7201==> 300ohm bead.



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : VGA_RGB,XTAL
Engineer: Nigo Lee

Size	Project Name	Rev
C	EJ14	1.0

Date: Tuesday, October 04, 2016 Sheet 72 of 99



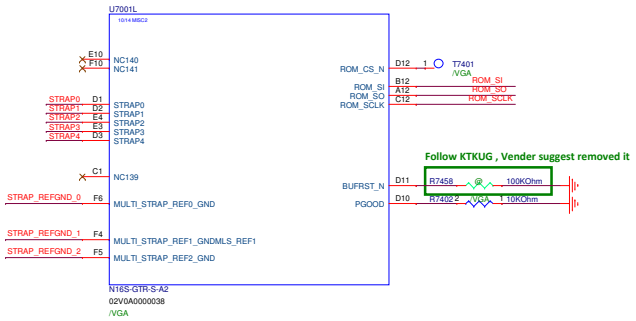
PEGATRON Title : VGA_LVDS,HDMI

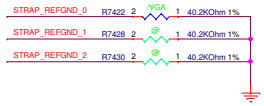
PEGATRON PROPRIETARY AND CONFIDENTIAL

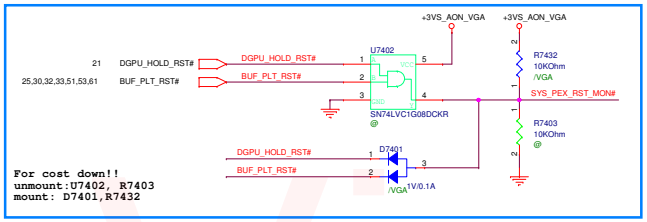
Engineer: Nigo Lee

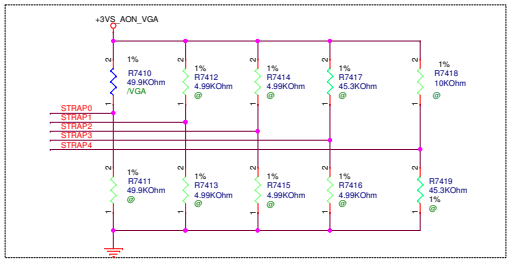
Size	Project Name	Rev
C	EJ14	1.0

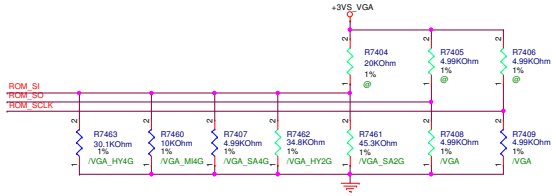
Date: Tuesday, October 04, 2016 Sheet 73 of 99











Hynix 2G	H5GC4H24AJR-T2C	0x6	0110	PD 34.8K
Samsung 2G	K4G41325FE-HC28	0x7	0111	PD 45.3K
Samsung 4G	K4G80325FB-HC03	0x0	0000	PD 4.99K
Micron 4G	MT51J256M32HF-60:A	0x1	0001	PD 10K
Hynix 4G	H5GC8H24MJR-T2C	0x5	0101	PD 30.1K

+3VS_AON_VGA 57,70,72,75,91
+3VS_VGA 57,75,91,96,97

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

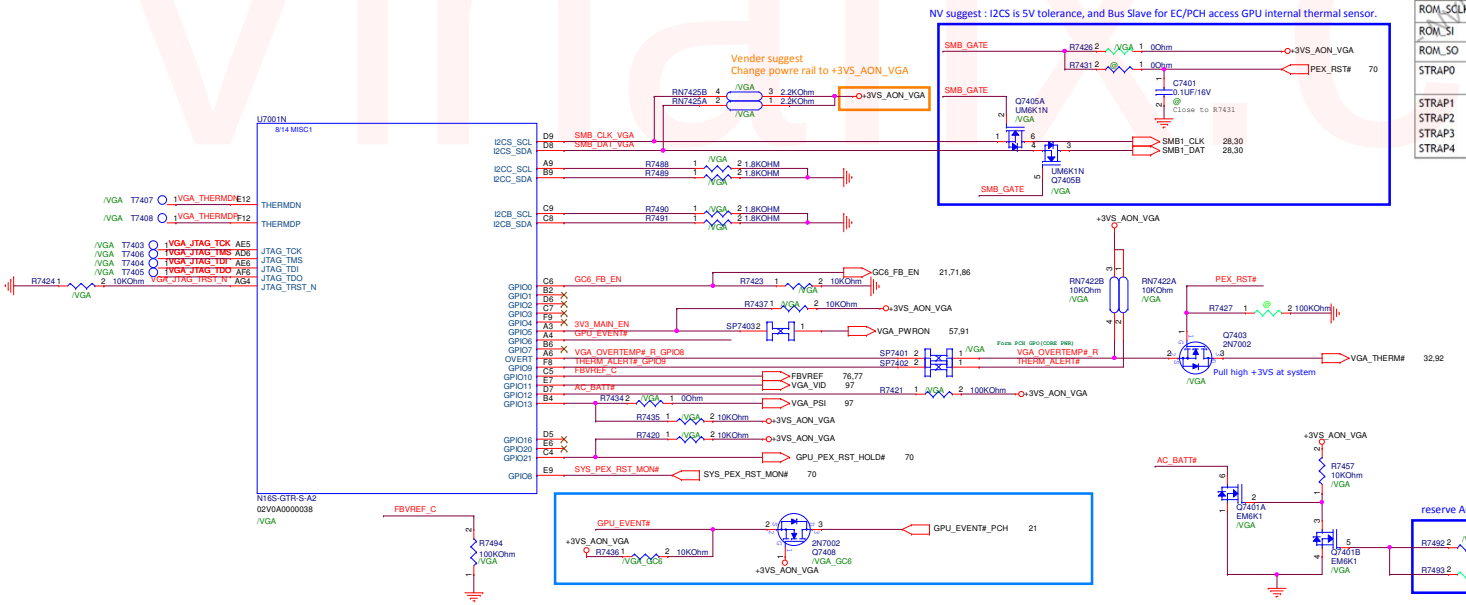
Table 12. N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	256Mx16	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		128Mx32	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
		512Mx16	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready

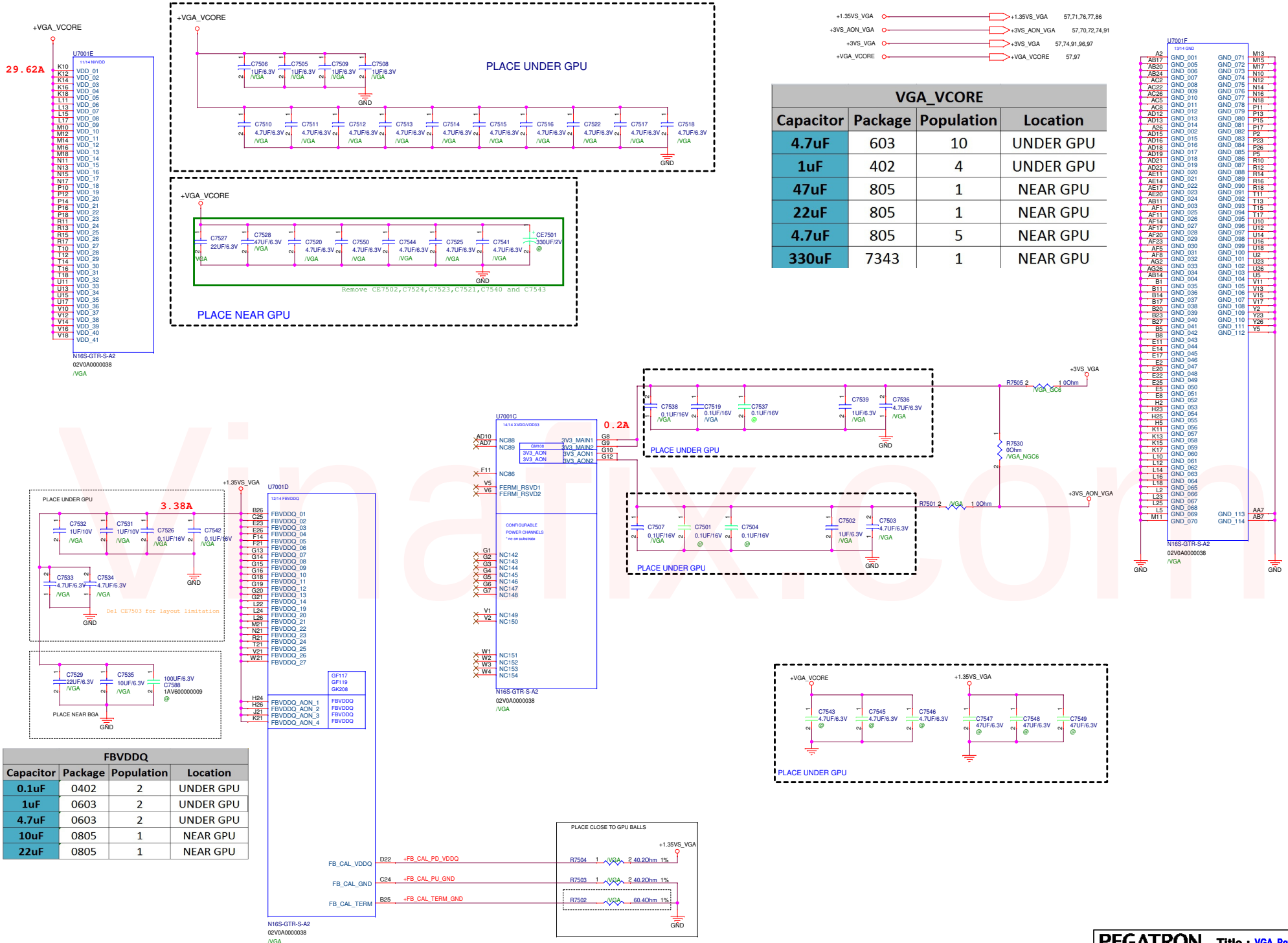
Note: For N16V-GMR1 and N16S-LG/-GMR/-GTR, the maximum allowable memory case temperature is 85 °C.

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			



PEGATRON Title :VGA_GPIO,STRAP
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Nigo Lee
Size: Custom | Project Name: EJ14 | Rev: 1.0
Date: Tuesday, October 04, 2016 | Sheet 74 of 99



+1.35VS_VGA	+1.35VS_VGA	57,71,76,77,86
+3VS_AON_VGA	+3VS_AON_VGA	57,70,72,74,91
+3VS_VGA	+3VS_VGA	57,74,91,96,97
+VGA_VCORE	+VGA_VCORE	57,97

VGA_VCORE			
Capacitor	Package	Population	Location
4.7uF	603	10	UNDER GPU
1uF	402	4	UNDER GPU
47uF	805	1	NEAR GPU
22uF	805	1	NEAR GPU
4.7uF	805	5	NEAR GPU
330uF	7343	1	NEAR GPU

FBVDDQ			
Capacitor	Package	Population	Location
0.1uF	0402	2	UNDER GPU
1uF	0603	2	UNDER GPU
4.7uF	0603	2	UNDER GPU
10uF	0805	1	NEAR GPU
22uF	0805	1	NEAR GPU

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : VGA_Power,GND
Engineer: Nigo Lee
Size: C | Project Name: EJ14 | Rev: 1.0
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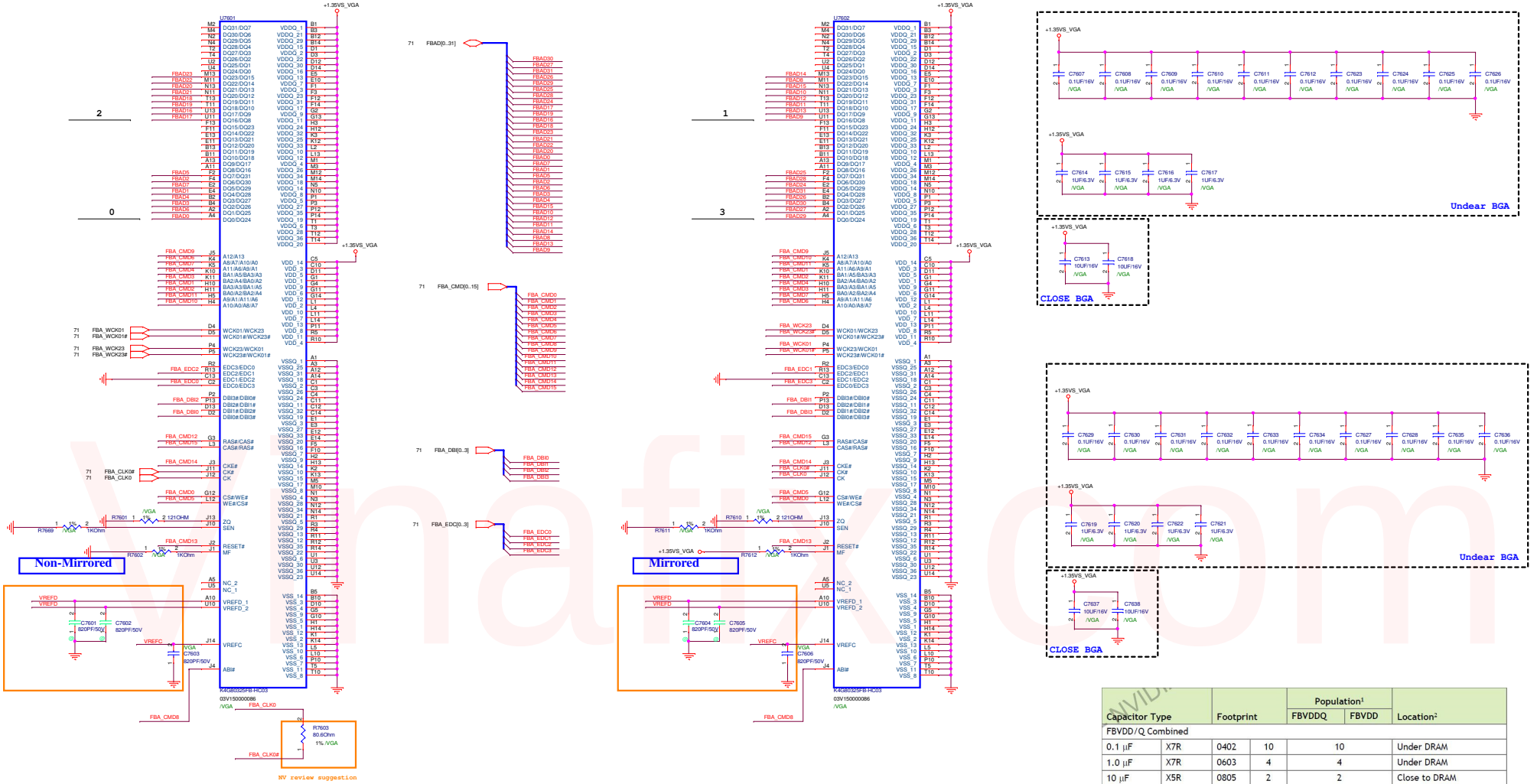

Capacitor Type		Footprint	Population[1] FBVDDQ	Population[1] FBVDD	Location[2]
FBVDD/Q Combined					
0.1 µF	X7R	0402	10	10	Under DRAM
1.0 µF	X7R	0603	4	4	Under DRAM
10 µF	X5R	0805	2	2	Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	6	6	0 Under DRAM
1.0 µF	X7R	0603	8	4	4 Under DRAM
10 µF	X5R	0805	2	1	1 Close to DRAM

Note:
1. Per sub-partition, for example, per two pieces of ×16 DRAM or one piece of ×32 DRAM.
2. Location is close to DRAM for all decoupling with ×16 DRAM.

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Title : VGA_GDDR5,CHA

Engineer: Terry_Pan

Size	Project Name	Rev
Custom	EJ14	1.0

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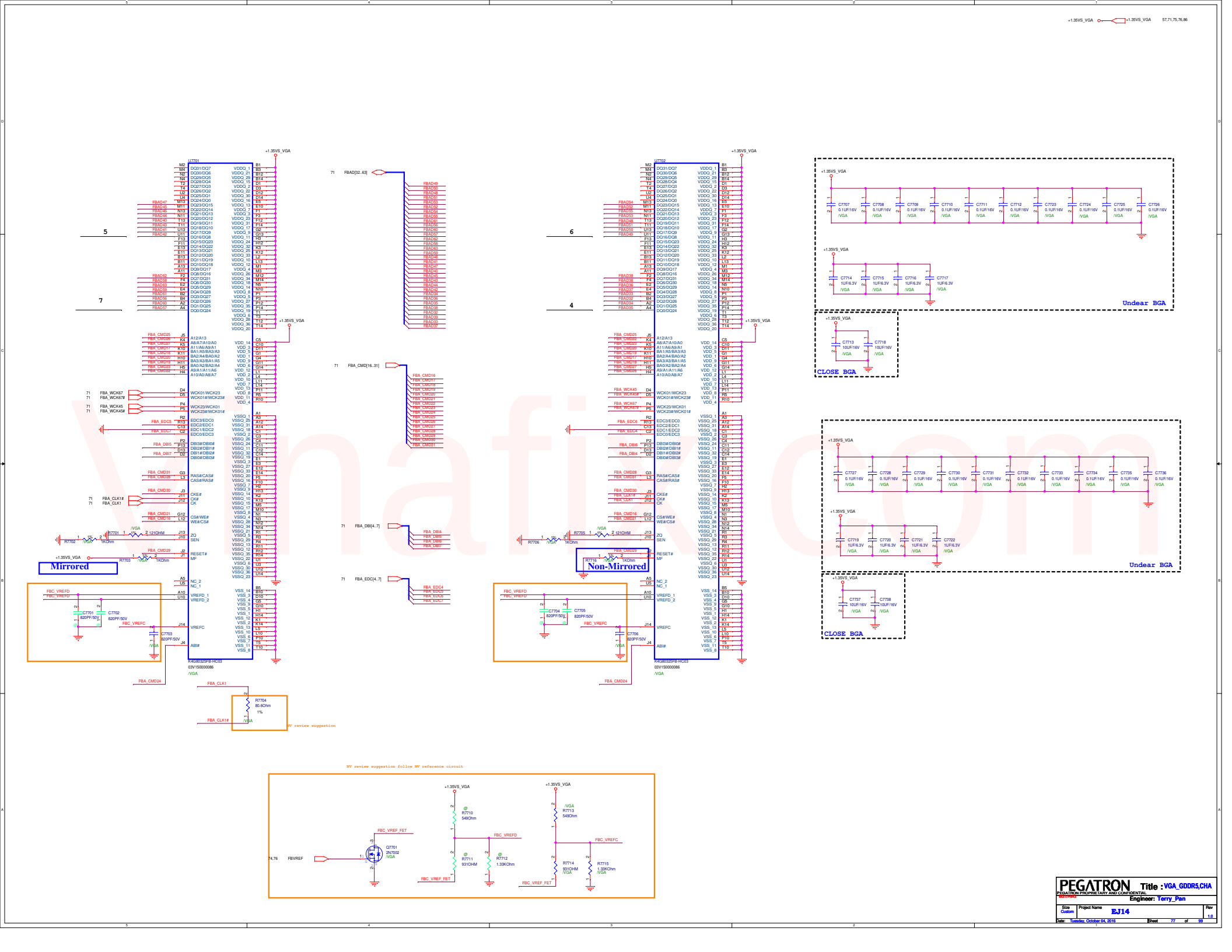
+1.35VS_VGA
+1.35VS_VGA 57,71,75,76,86
U7701
U7702
Mirrored
Non-Mirrored
Undear BGA
CLOSE BGA
Undear BGA
CLOSE BGA
NV review suggestion
NV review suggestion follow NV reference circuit
PEGATRON
Title : VGA_GDDR5,CHA
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Terry_Pan
Project Name
EJ14
Rev
1.0
Date: Tuesday, October 04, 2016
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Title	<Title>		
Size A	Document Number EJ14		Rev 1.0
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Title	<Title>	
Size A	Document Number EJ14	Rev 1.0
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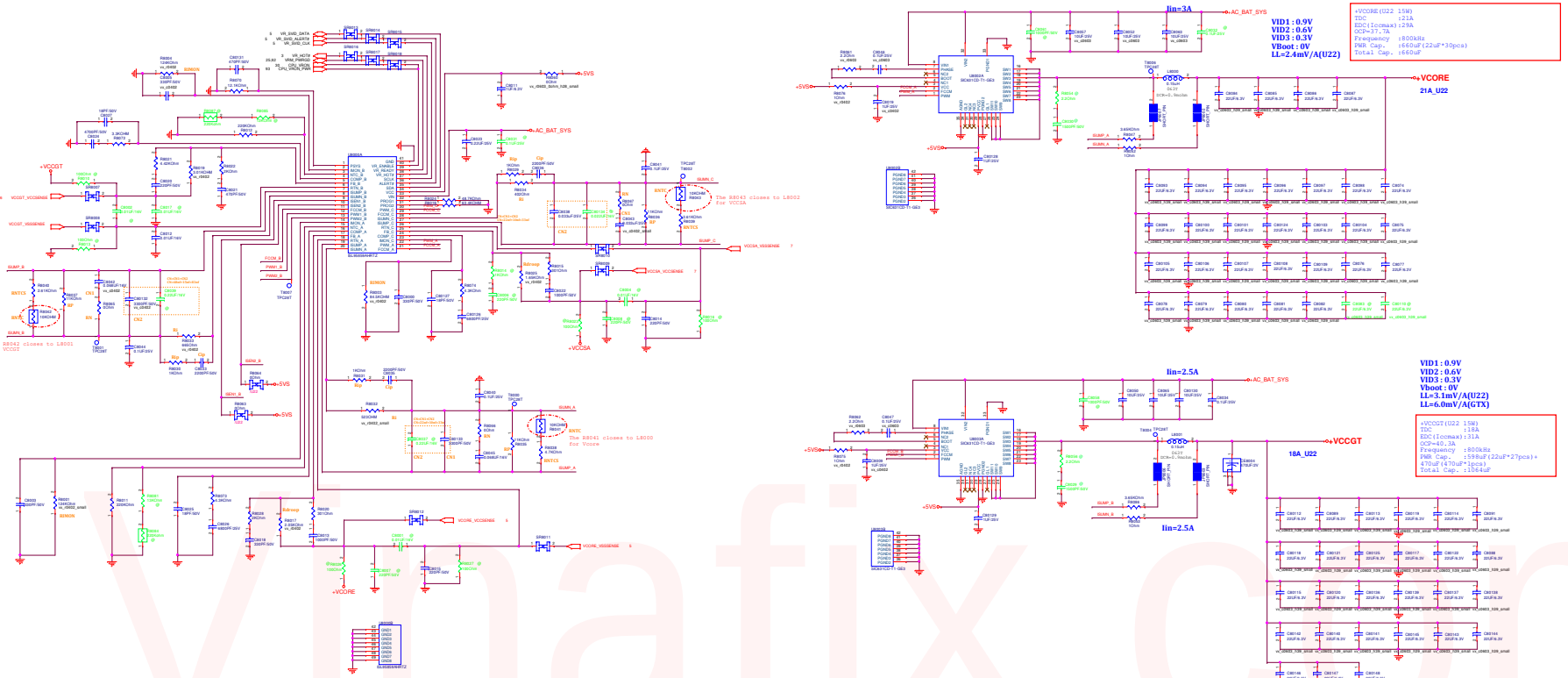
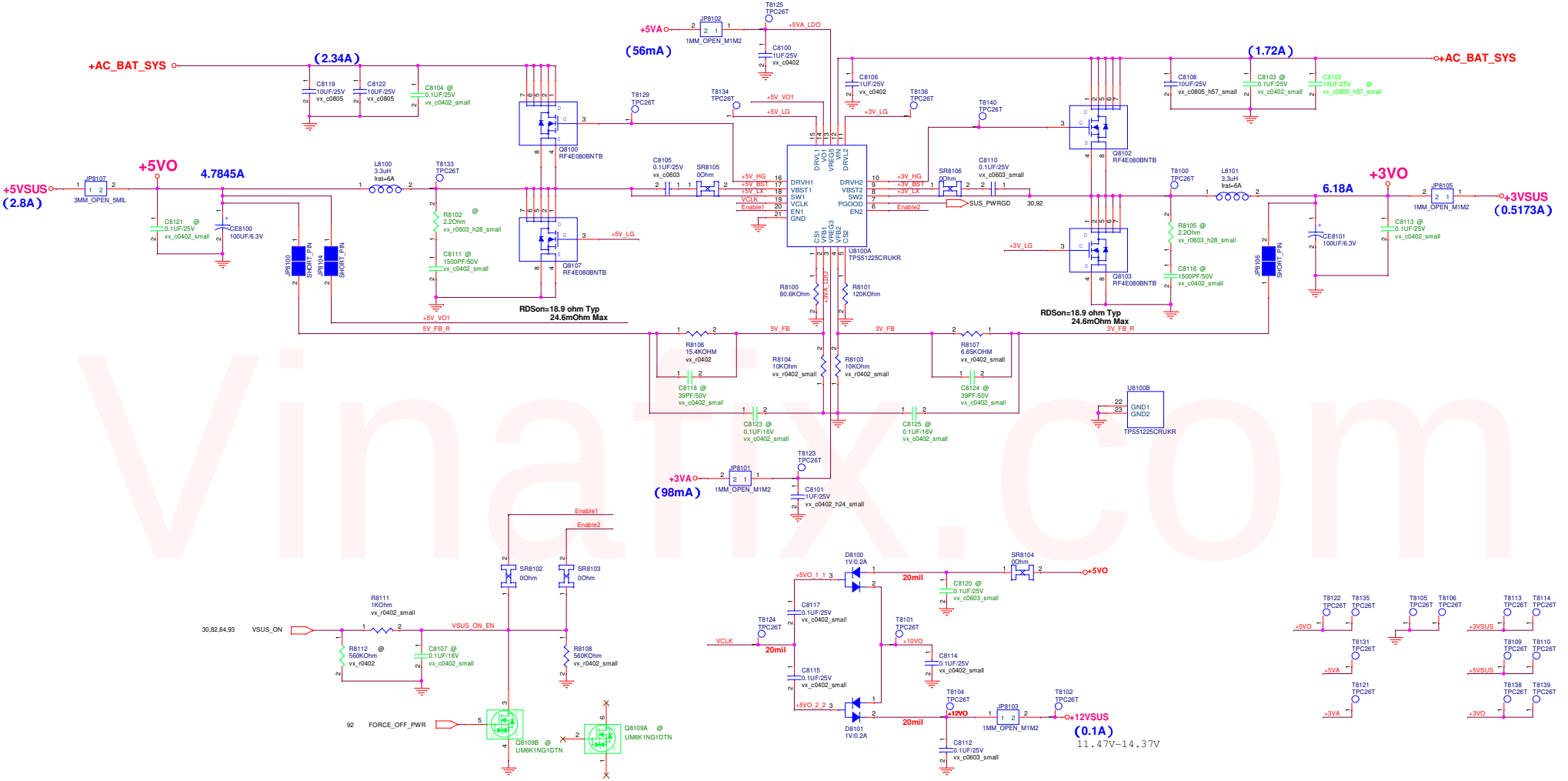
VCORE POWER SUPPLY SKL_U22



PEGATRON Title : POWER_VCORE
Engineer: Mike_Ko
Project Name: EJ14

+5VO & +3VO POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SYSTEM

Engineer: Adams Lin

Size	Project Name	Rev
Custom	EJ14	1.0

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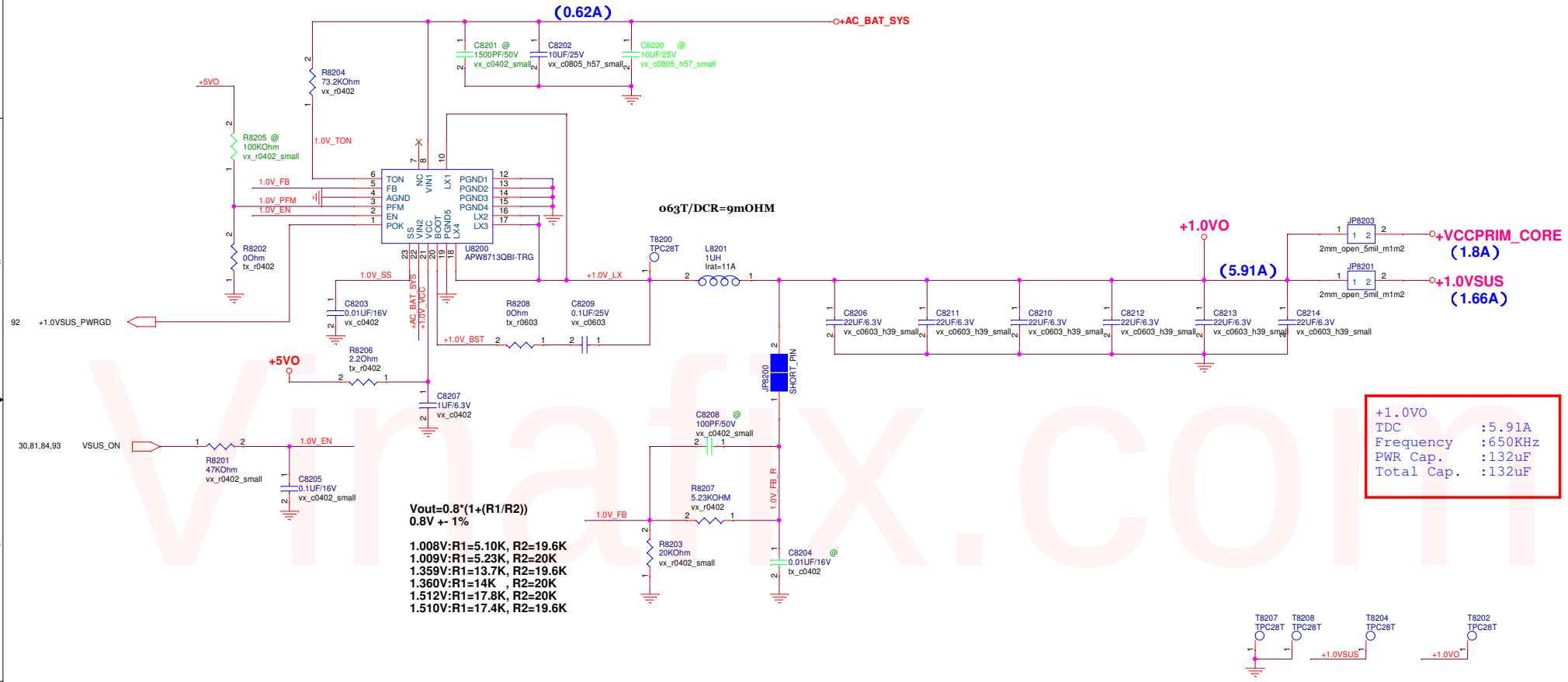
+1.0VSUS POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : P82_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	EJ14	1.0

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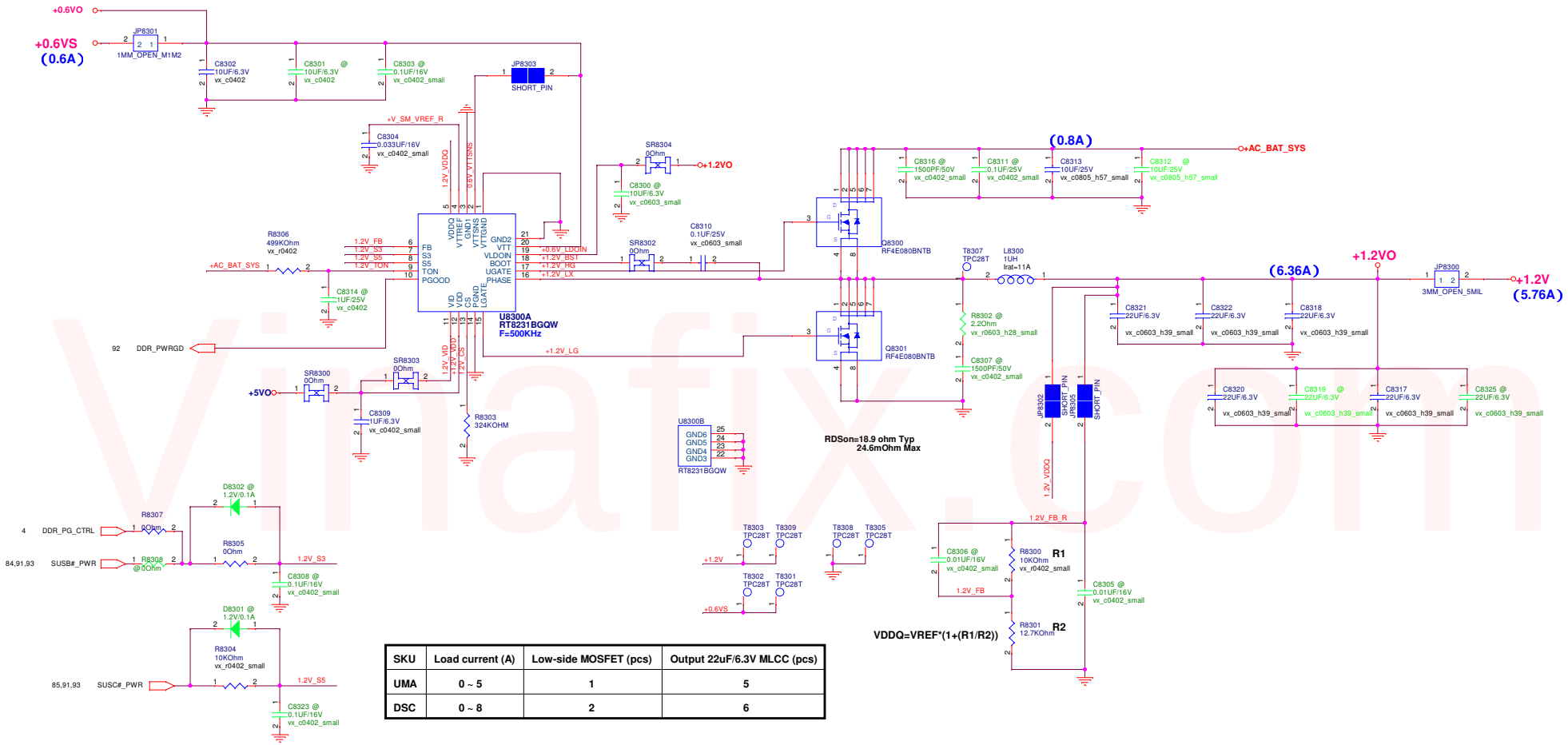
DDR & VTT POWER SUPPLY



SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_DDR & VTT

Engineer: Adams Lin

Size	Project Name	Rev
Custom	EJ14	1.0

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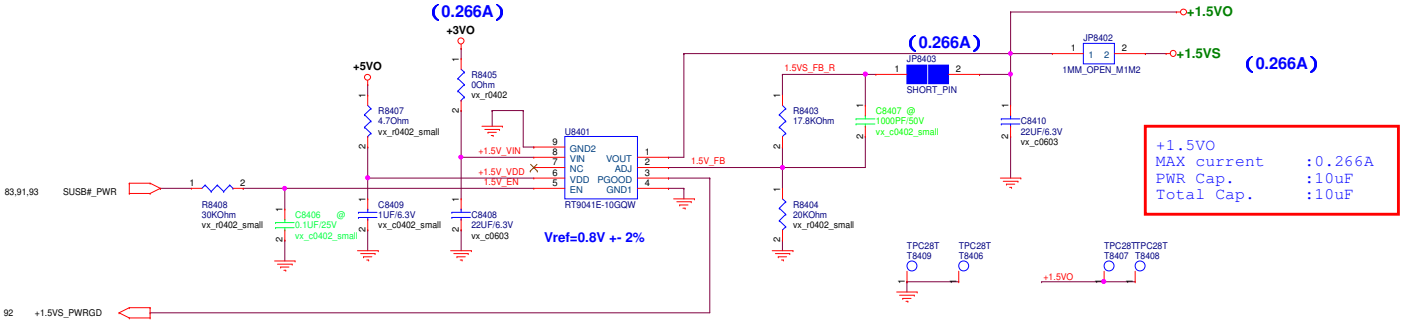
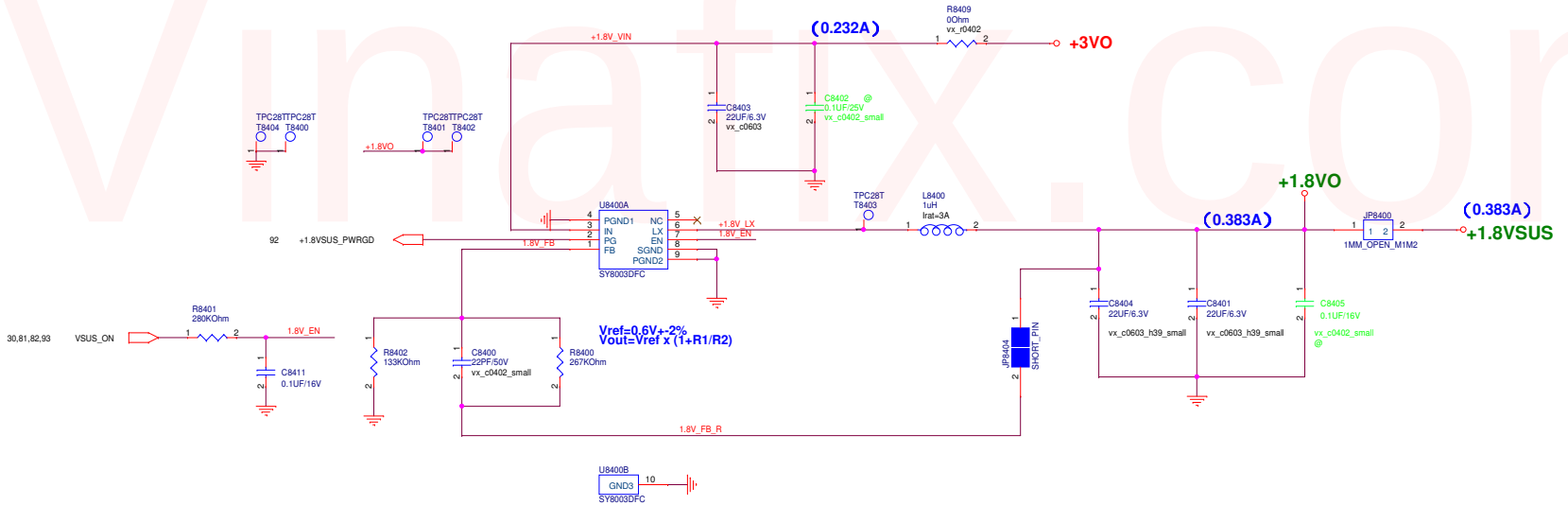
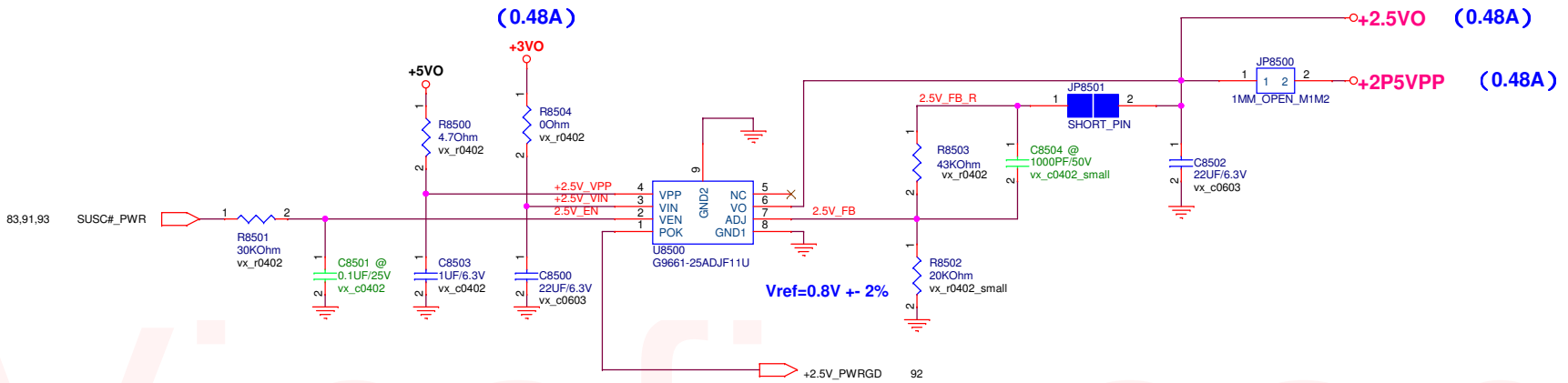
1.5VS POWER SUPPLY



1.8VSUS POWER SUPPLY



2.5V POWER SUPPLY



<Variant Name>

PEGATRON Title : PAGE 85 POWER

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Gene Cheng

Size	Project Name	Rev
B	EJ14	1.0

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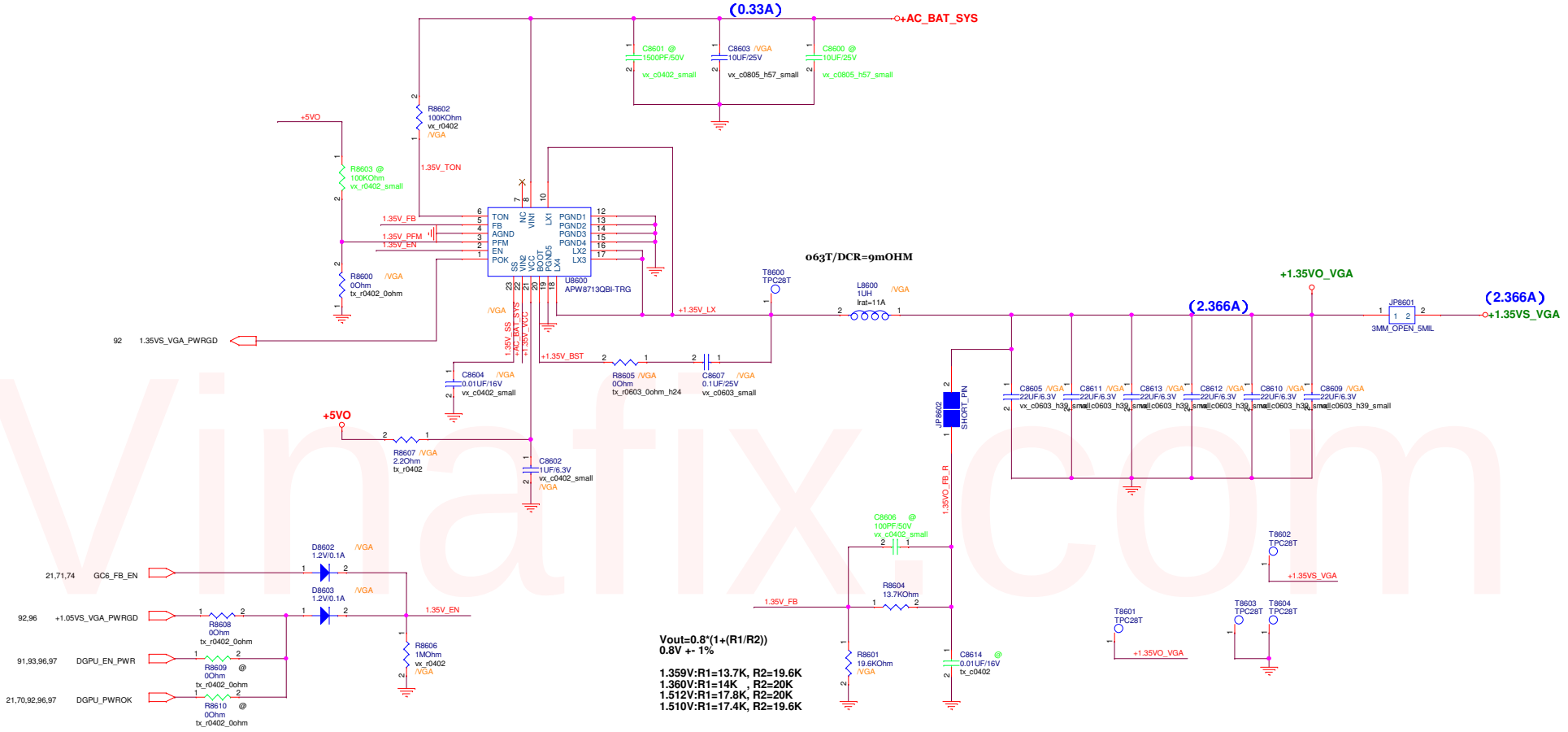
+VRAM_VGA(+1.35V) POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+1.35VS_VGA

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	EJ14	1.0

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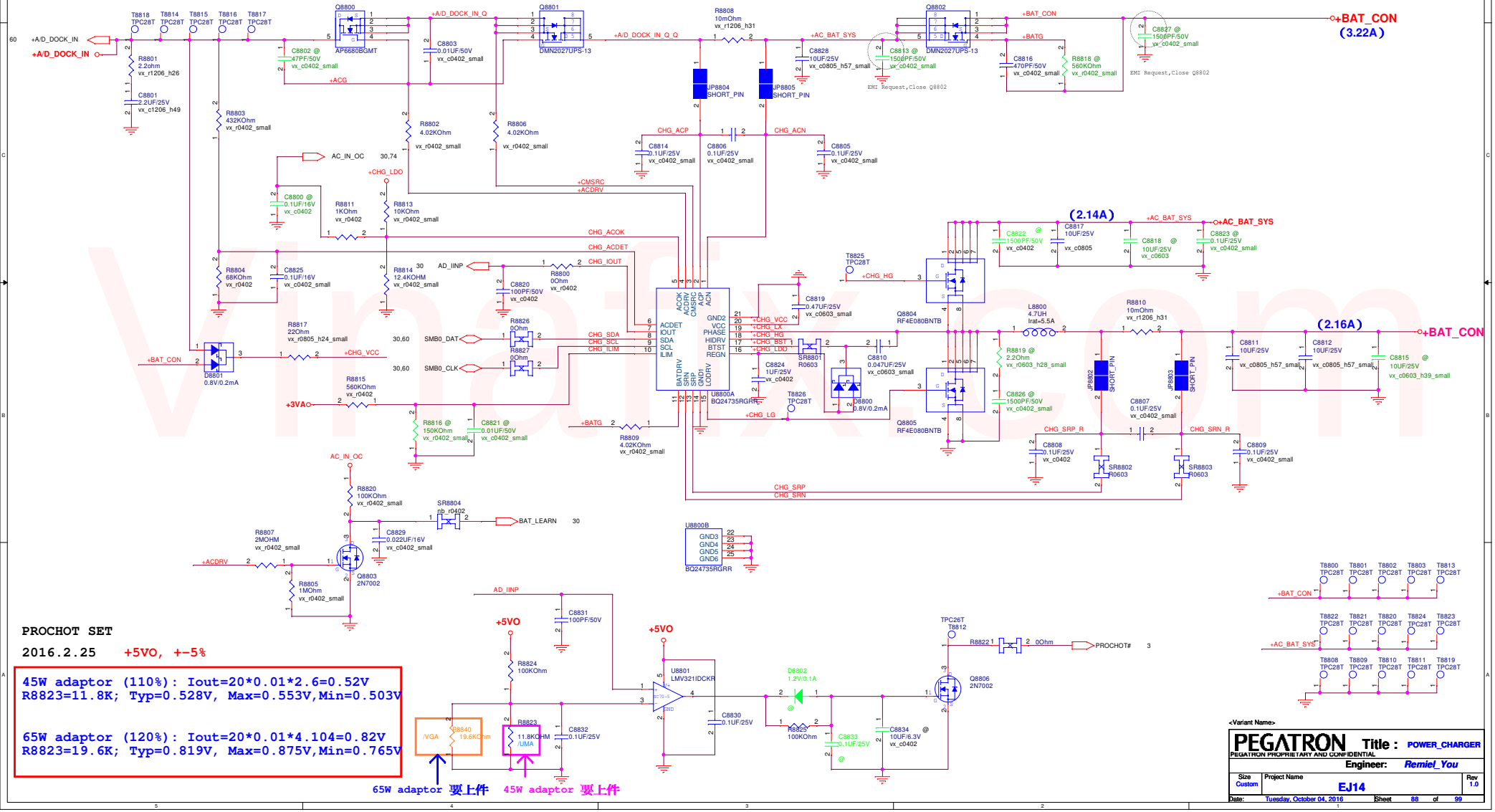
BATTERY CHARGER

Adapter 90W=4.5A
Adapter 65W=3.42A
Adapter 45W=2.37A



PROCHOT SET

2016.2.25 +5VO, +-5%

45W adaptor (110%): Iout=20*0.01*2.6=0.52V
R8823=11.8K; Typ=0.528V, Max=0.553V,Min=0.503V

65W adaptor (120%): Iout=20*0.01*4.104=0.82V
R8823=19.6K; Typ=0.819V, Max=0.875V,Min=0.765V

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : POWER_CHARGER		
	Engineer: Remiel_You		
Size: Custom	Project Name: EJ14		Rev: 1.0
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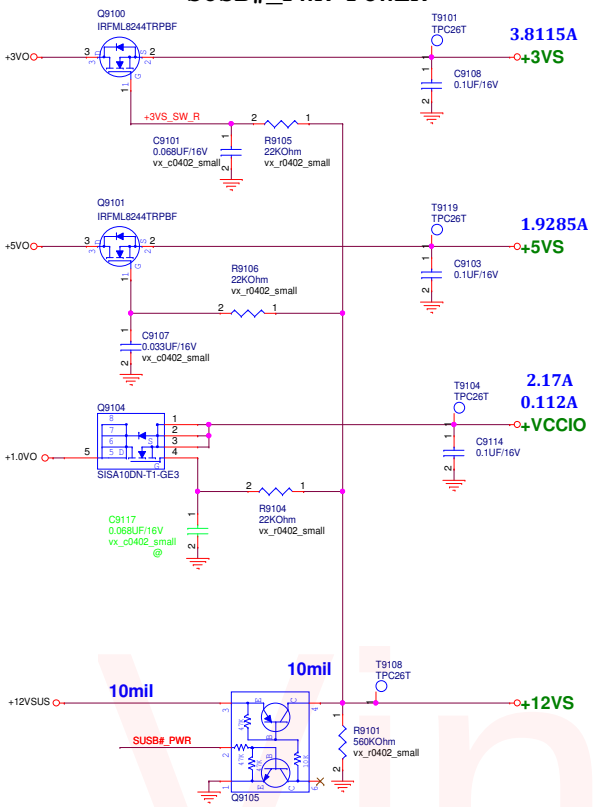
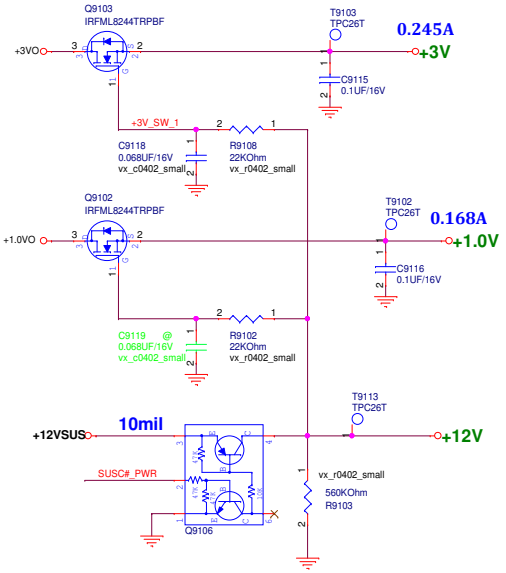
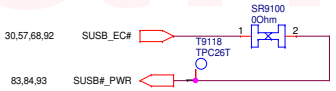
SUSB#_PWR POWER



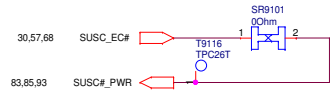
SUSC#_PWR POWER

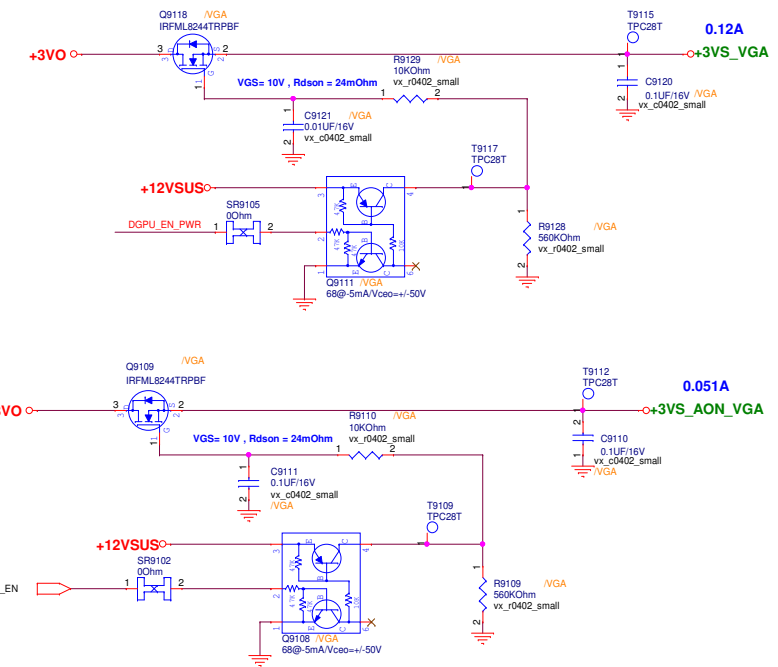


SUSB#_PWR POWER Control



SUSC#_PWR POWER Control





DSC_VGA_PWR POWER Control

<Variant Name>

PEGATRON
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Title : POWER_LOAD SWITCH

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	EJ14	1.0

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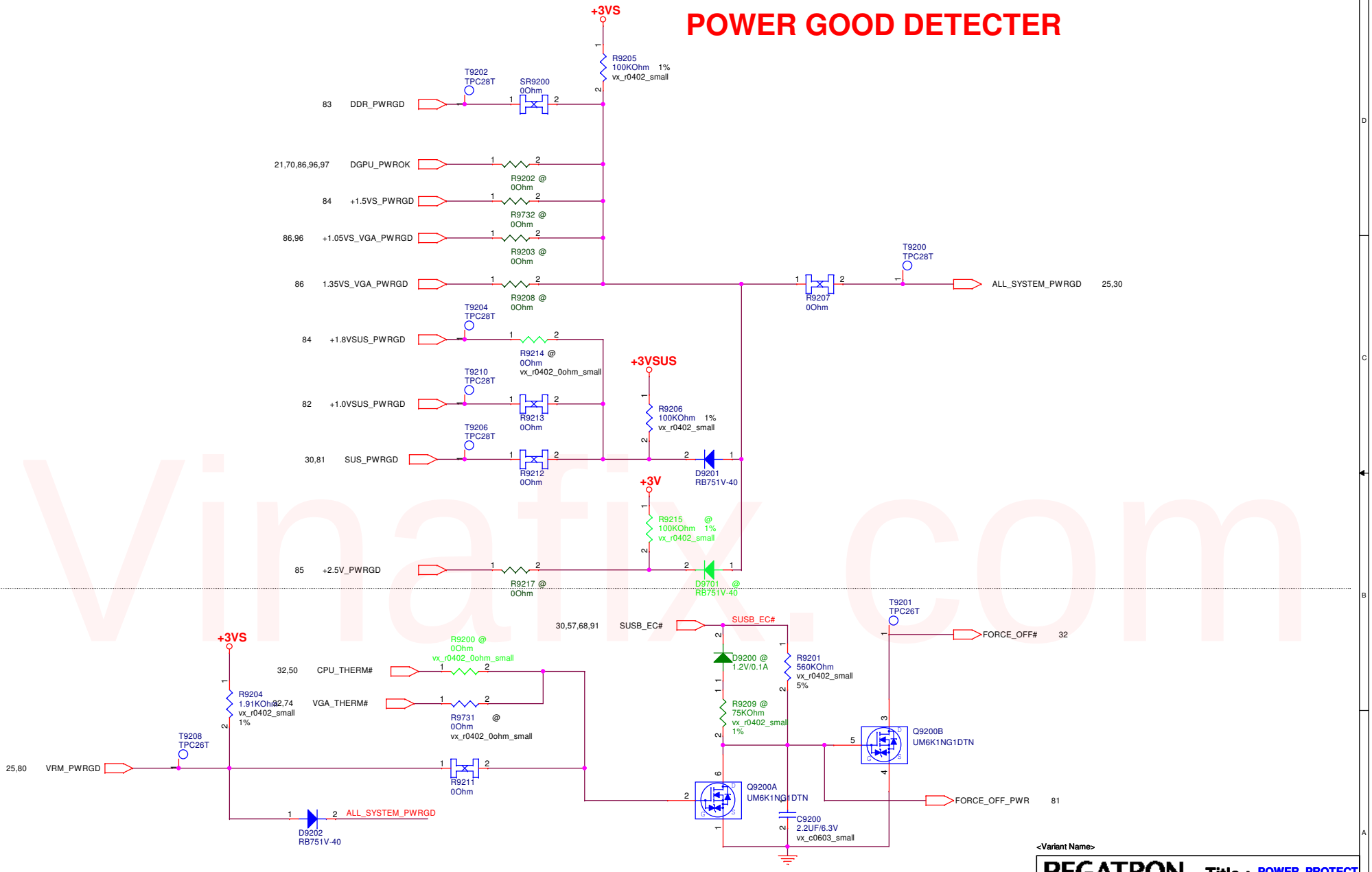
POWER GOOD DETECTER



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Adams Lin

Size	Project Name	Rev
Custom	EJ14	1.0

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+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,86,88,97

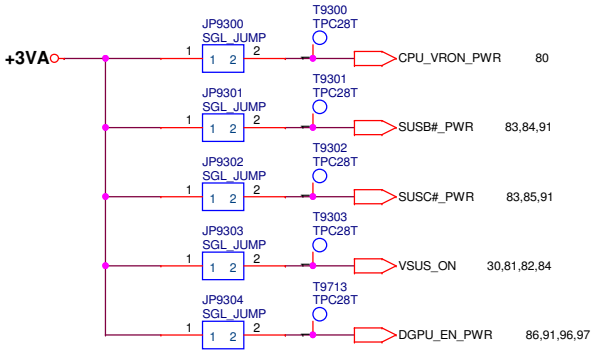
+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 56,81
+3VA → +3VA 24,30,31,36,53,56,57,81,88
+5VO → +5VO 81,82,83,84,85,86,88,91
+3VO → +3VO 81,84,85,91,96
+1.8VO → +1.8VO 84
+1.5VO → +1.5VO 84
+1.2VO → +1.2VO 83
+1.0VO → +1.0VO 82,91
+0.6VO → +0.6VO 83
+12VSUS → +12VSUS 81,91
+5VSUS → +5VSUS 52,56,81
+3VSUS → +3VSUS 4,25,26,28,30,31,33,51,52,53,68,81,92
+1.8VSUS → +1.8VSUS 9,24,26,84
+1.0VSUS → +1.0VSUS 26,82
+12V → +12V 91
+3V → +3V 25,31,44,45,57,91,92
+1.2V → +1.2V 4,7,15,16,17,18,57,83
+1.0V → +1.0V 7,57,91
+12VS → +12VS 28,31,57,91
+5VS → +5VS 31,36,48,50,51,57,61,80,91,97
+3VS → +3VS 3,4,17,20,21,22,23,24,30,31,32,33,36,37,40,45,48,50,51,52,53,57,61,91,92

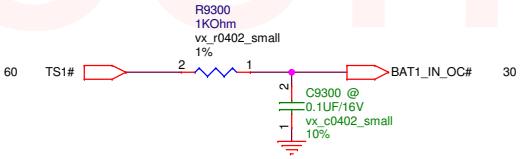
+1.5VS → +1.5VS 36,57,84

+0.6VS → +0.6VS 15,17,57,83
+VCORE → +VCORE 5,57,80
+VCCGT → +VCCGT 6,57,80
+VCCIO → +VCCIO 3,7,57,91
+VCCSA → +VCCSA 7,57,80
+VCCPRIM_CORE → +VCCPRIM_CORE 26,82

FOR POWER TEST

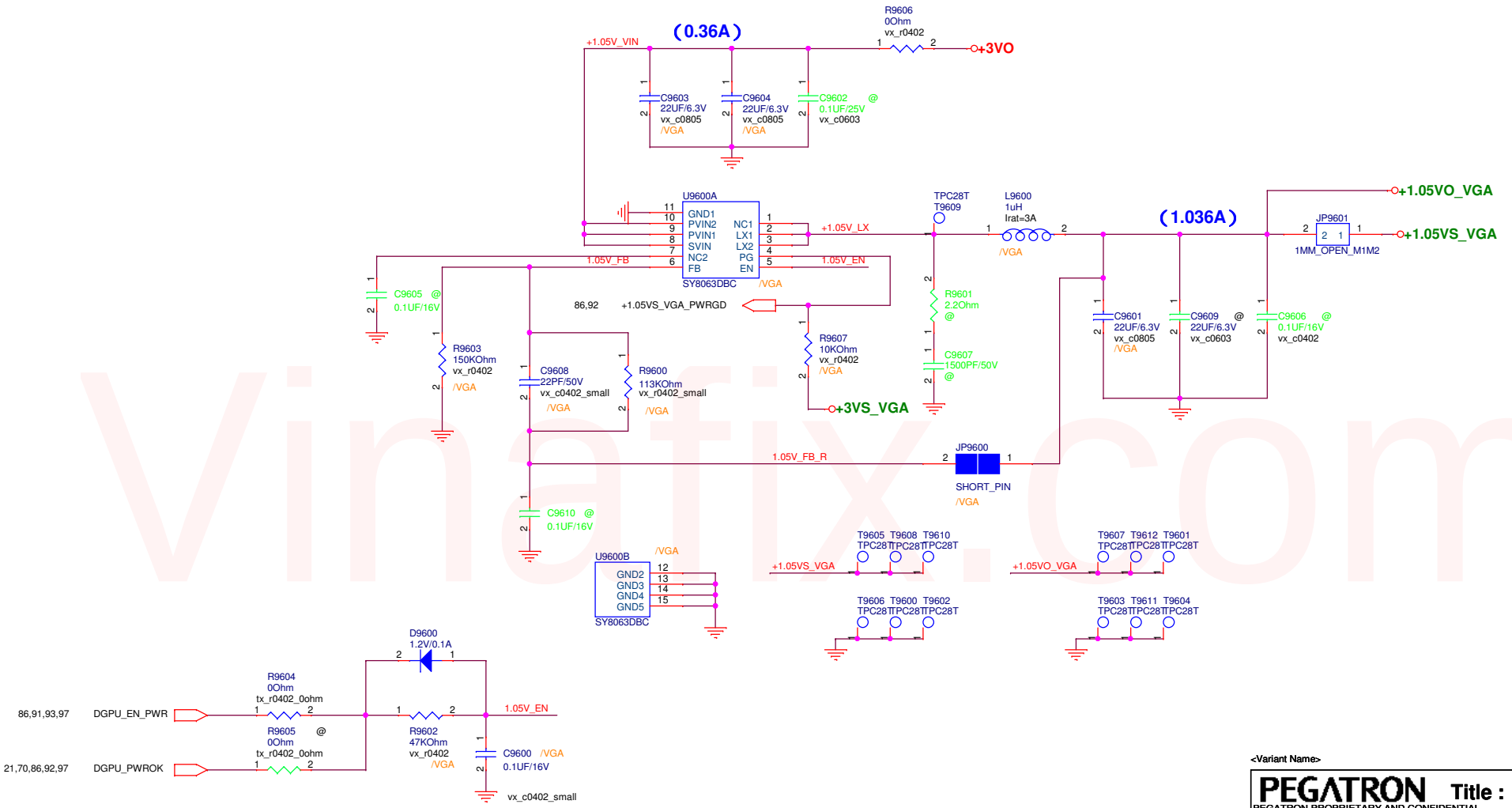


BATTERY IN DETECT



PEGATRON Title : POWER_SIGNAL
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3 Engineer: Mike_Ke
Size B | Project Name EJ14 | Rev 1.0
Date: Tuesday, October 04, 2016 Sheet 93 of 99

1.05VS_VGA POWER SUPPLY



<Variant Name>

PEGATRON Title : PAGE 96 POWER

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Neil_Lin

Size	Project Name	Rev
B	EJ14	1.0

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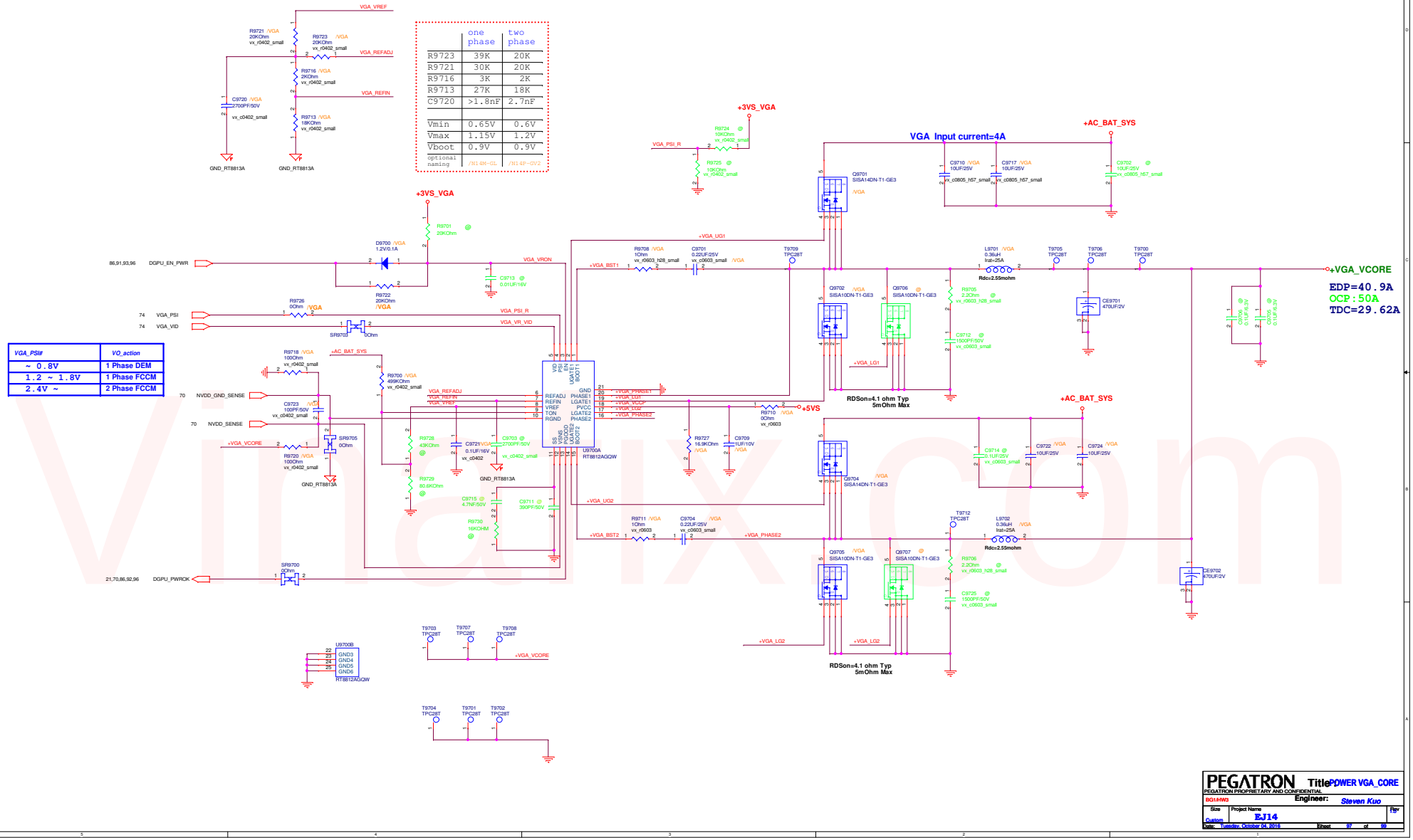
VGA_CORE POWER SUPPLY



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER VGA_CORE

BG1.HW3

Engineer: Steven Kuo

Size: Custom | Project Name: EJ14 | Rev:

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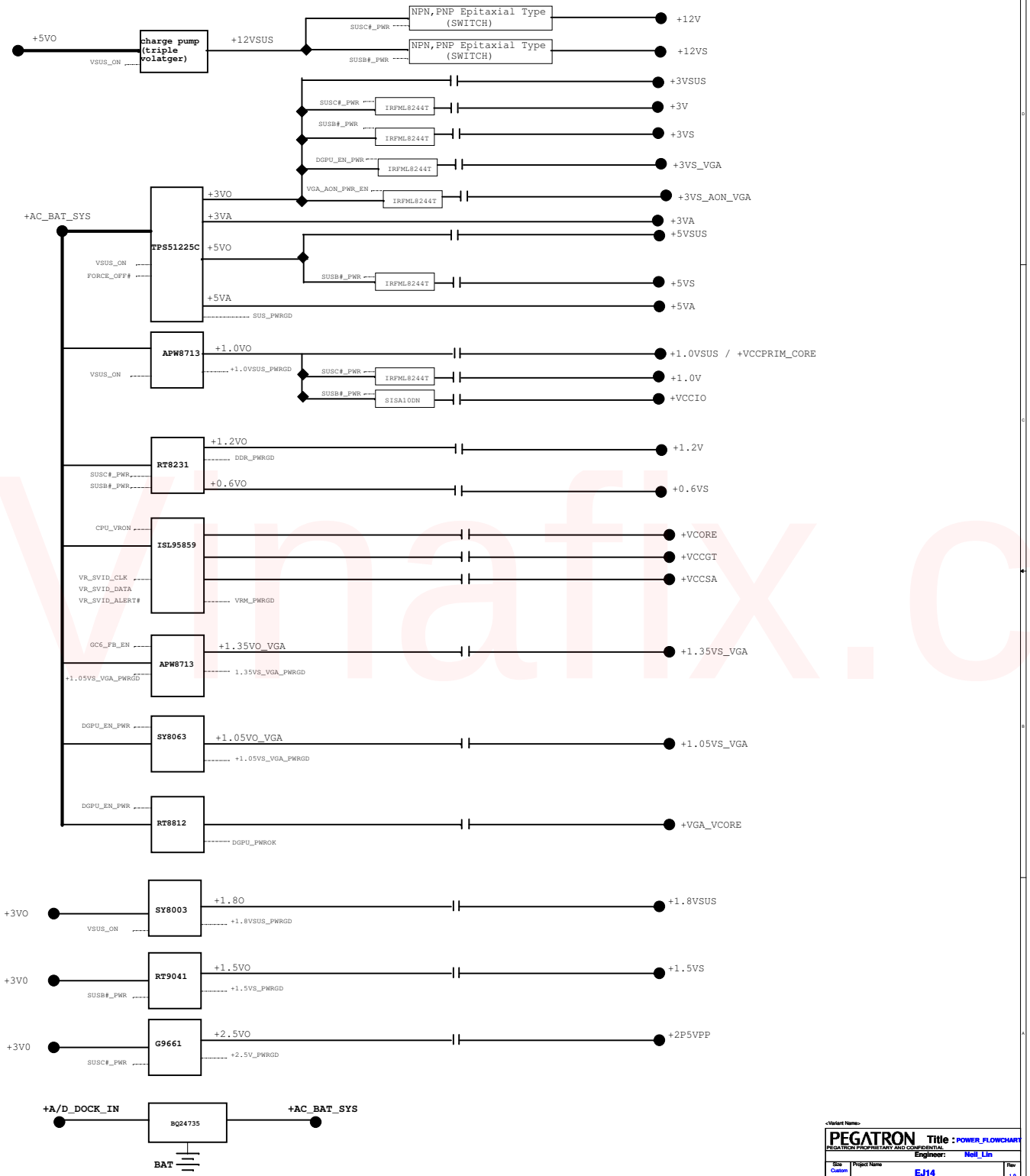
+5VO
charge pump (triple volatger)
VSUS_ON
+12VSUS
NPN,PNP Epitaxial Type (SWITCH)
SUSC#_PWR
+12V
NPN,PNP Epitaxial Type (SWITCH)
SUSB#_PWR
+12VS
+3VSUS
IRFML8244T
SUSC#_PWR
+3V
SUSB#_PWR
+3VS
DGPU_EN_PWR
+3VS_VGA
VGA_AON_PWR_EN
+3VS_AON_VGA
+AC_BAT_SYS
TPS51225C
+3VO
+3VA
+3VA
+5VSUS
+5VO
VSUS_ON
FORCE_OFF#
SUSB#_PWR
+5VS
+5VA
+5VA
SUS_PWRGD
APW8713
+1.0VO
+1.0VSUS / +VCCPRIM_CORE
VSUS_ON
+1.0VSUS_PWRGD
SUSC#_PWR
+1.0V
SUSB#_PWR
SISA10DN
+VCCIO
RT8231
+1.2VO
+1.2V
DDR_PWRGD
SUSC#_PWR
SUSB#_PWR
+0.6VO
+0.6VS
ISL95859
CPU_VRON
+VCORE
+VCCGT
VR_SVID_CLK
VR_SVID_DATA
VR_SVID_ALERT#
+VCCSA
VRM_PWRGD
APW8713
GC6_FB_EN
+1.35VO_VGA
+1.35VS_VGA
+1.05VS_VGA_PWRGD
1.35VS_VGA_PWRGD
SY8063
DGPU_EN_PWR
+1.05VO_VGA
+1.05VS_VGA
+1.05VS_VGA_PWRGD
RT8812
DGPU_EN_PWR
+VGA_VCORE
DGPU_PWROK
SY8003
+3VO
+1.8O
+1.8VSUS
VSUS_ON
+1.8VSUS_PWRGD
RT9041
+3V0
+1.5VO
+1.5VS
SUSB#_PWR
+1.5VS_PWRGD
G9661
+3V0
+2.5VO
+2P5VPP
SUSC#_PWR
+2.5V_PWRGD
+A/D_DOCK_IN
BQ24735
+AC_BAT_SYS
BAT