MS-1782

Ver:2.0 Skylake platform

Tuesday, July 07, 2015

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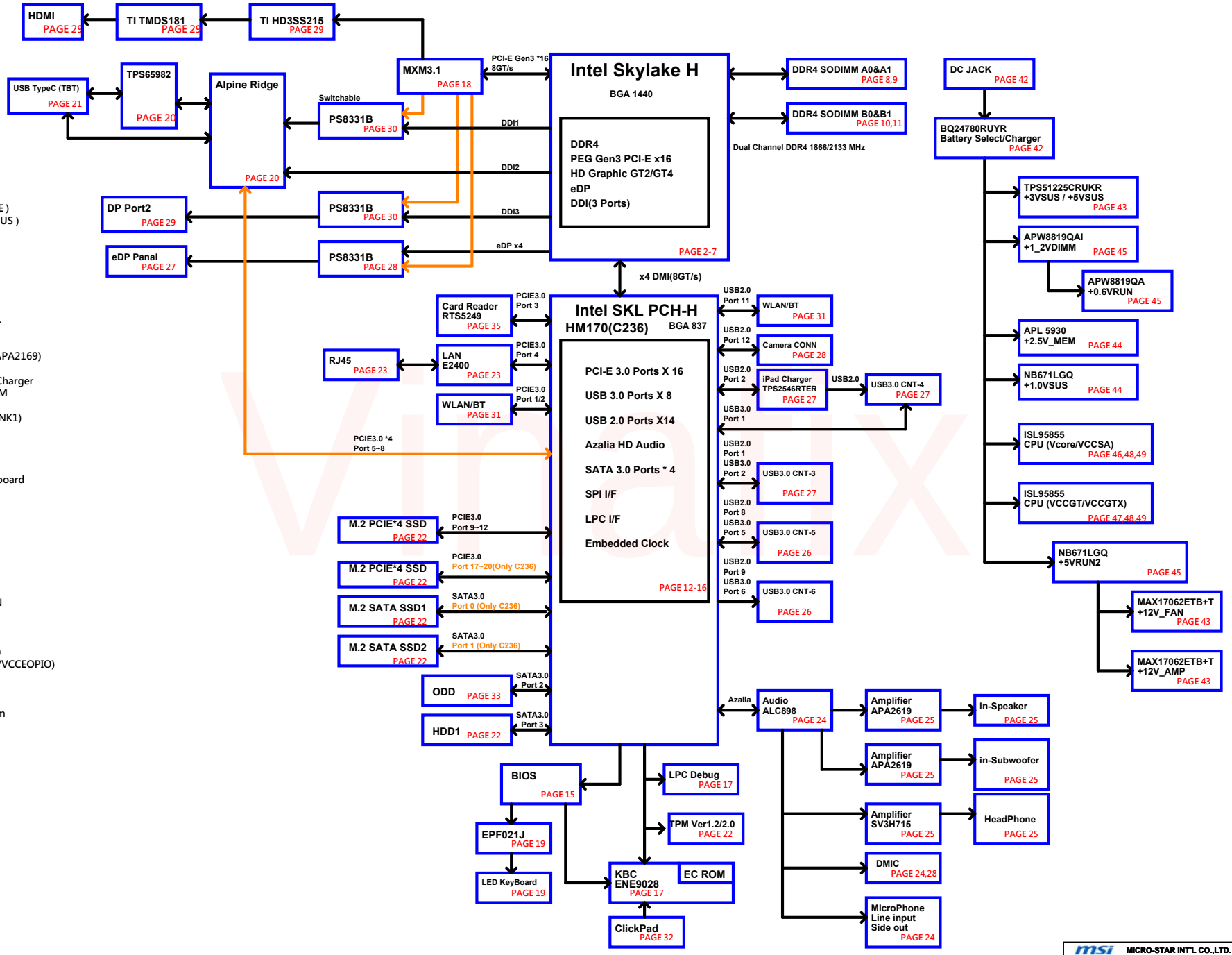
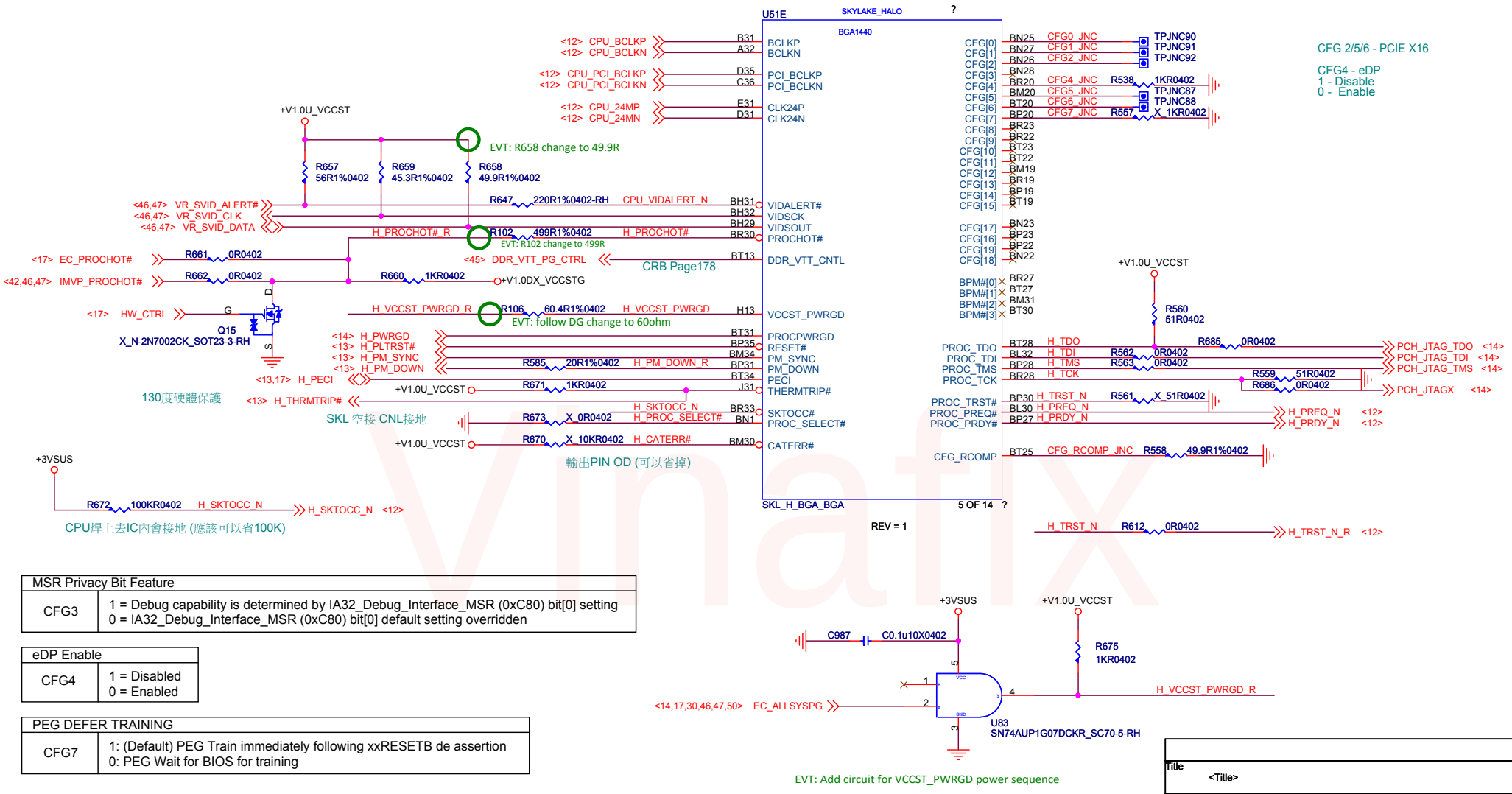


MICRO-STAR INT'L CO.,LTD.

Block Diagram

MS-1782

2.0



MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Title	<Title>		
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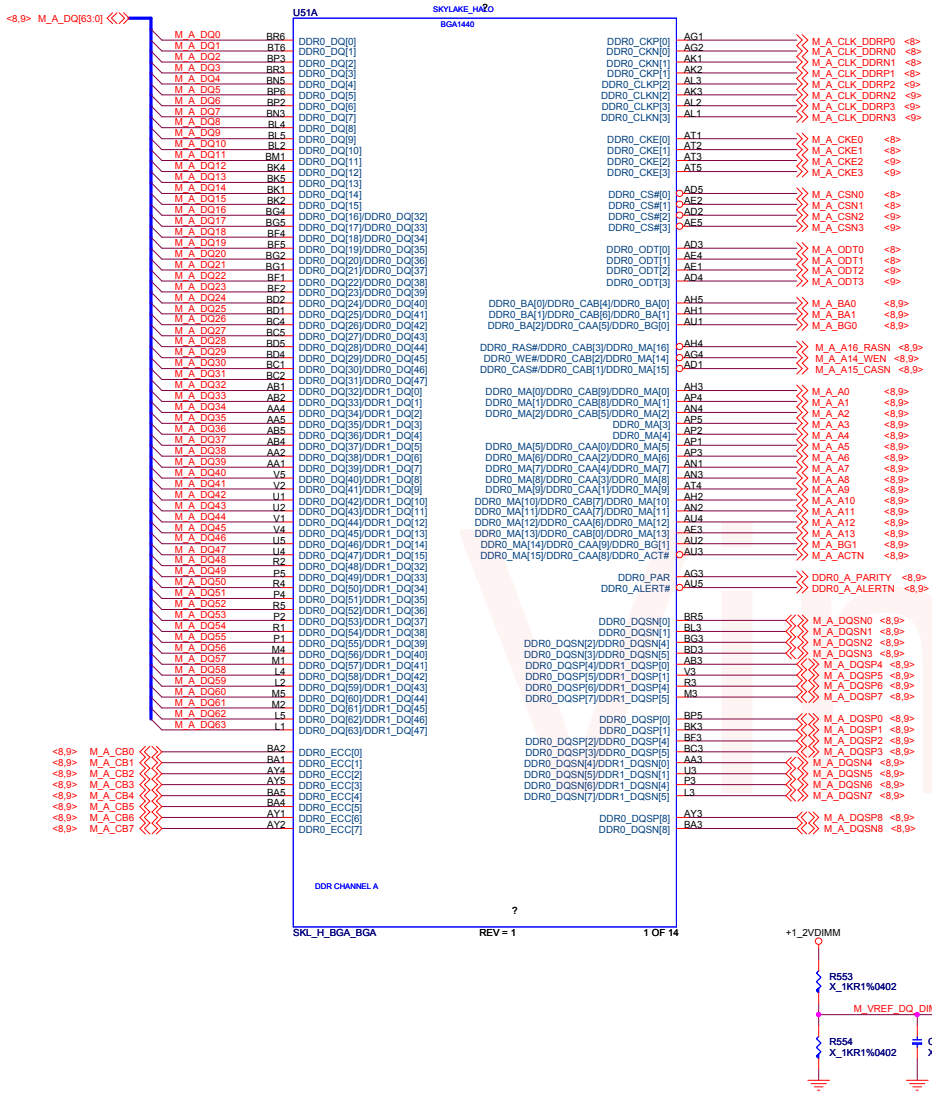
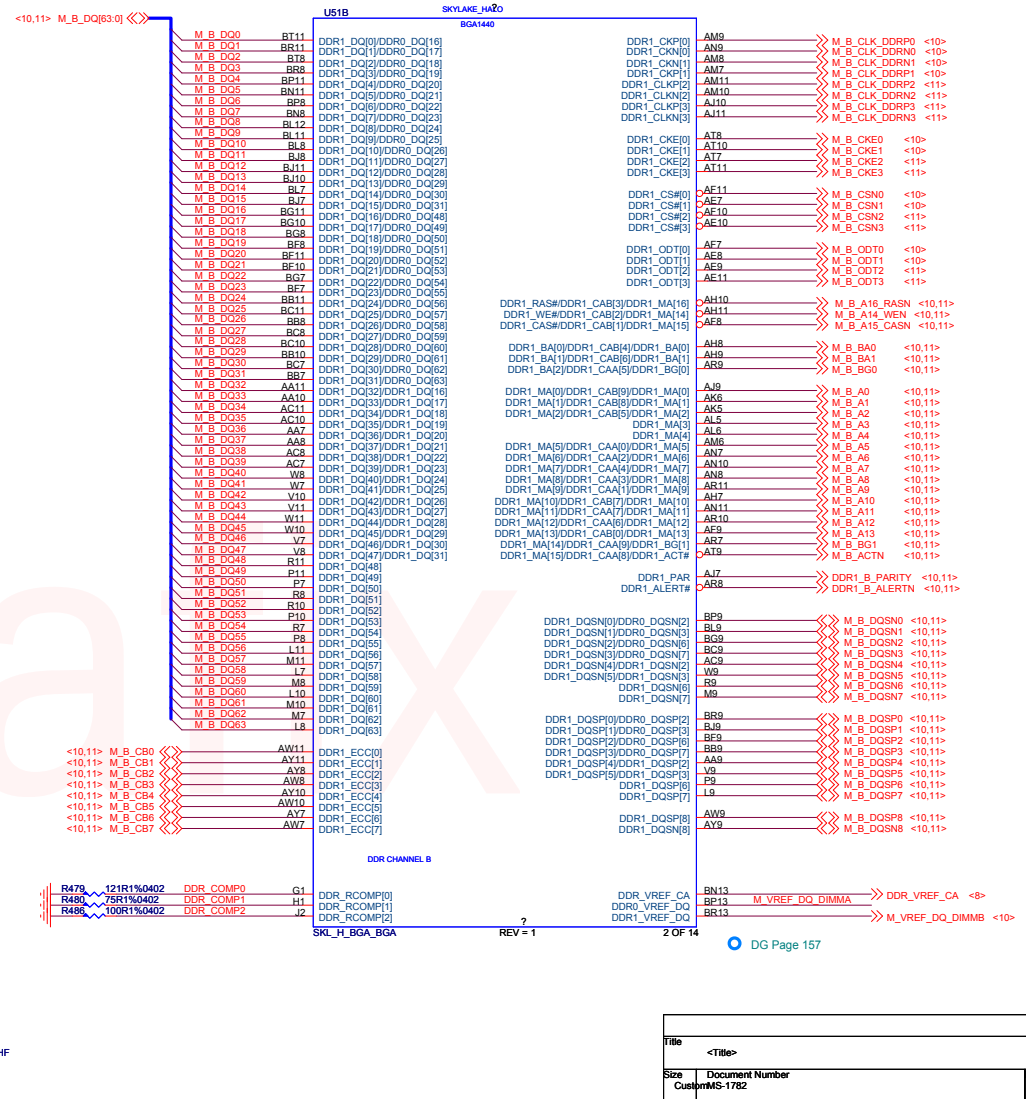
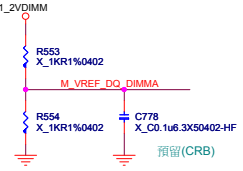
DDR Channel A



DDR Channel B



DG Page 157



Title	<Title>		
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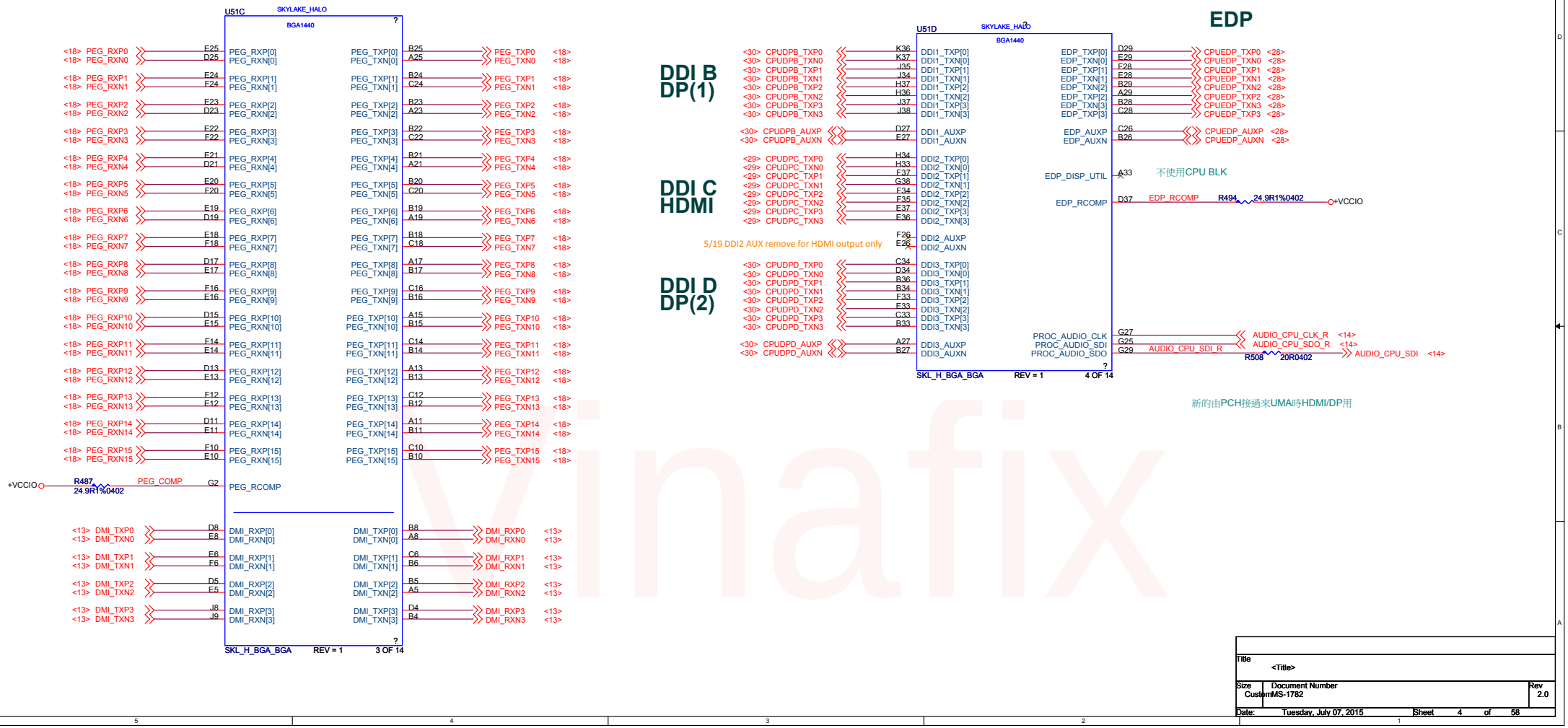
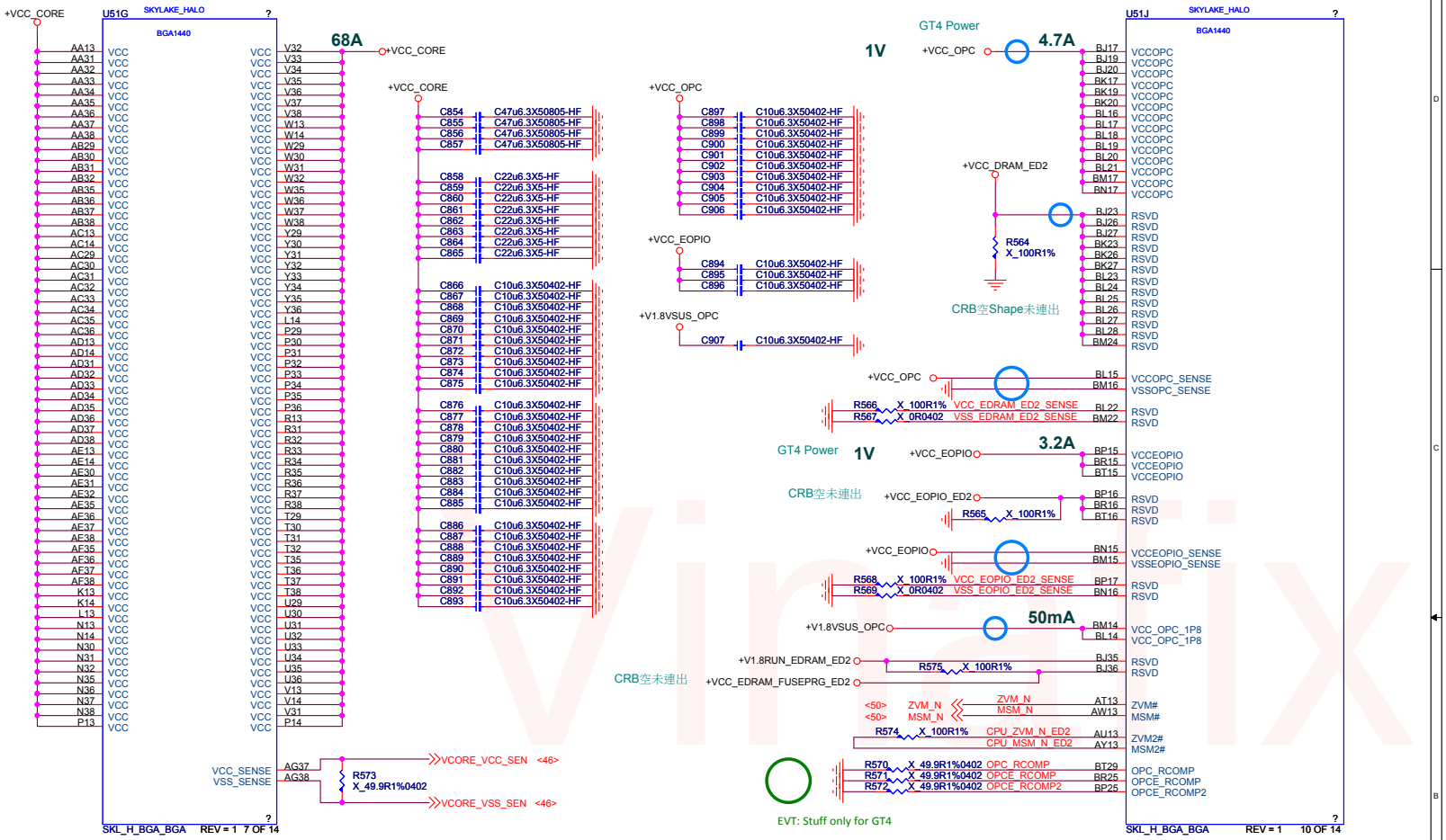
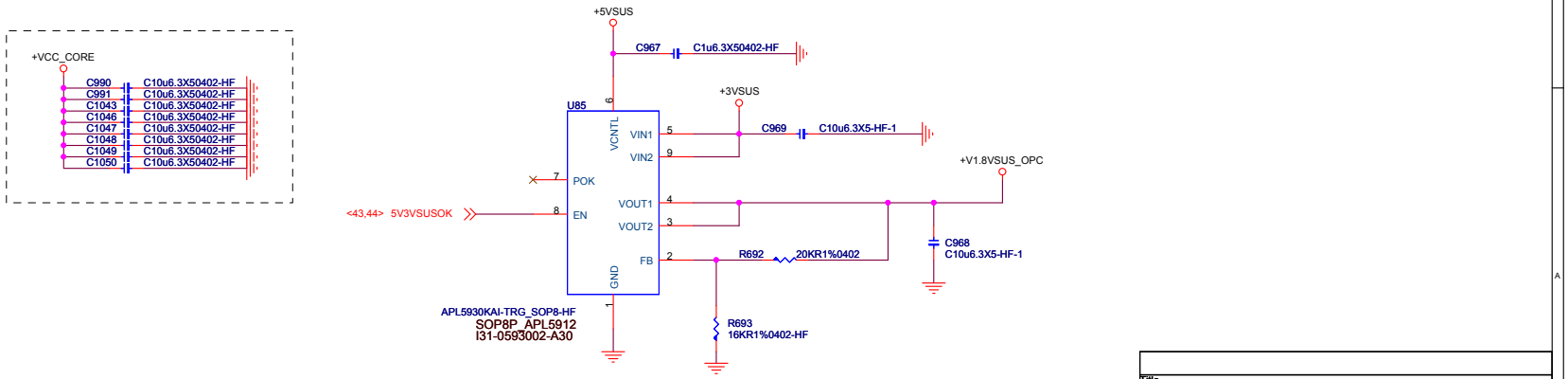


Title	<Title>	
Size: Custom	Document Number: MS-1782	Rev: 2.0
Date: Tuesday, July 07, 2015	Sheet 4 of 58	





Title	<Title>	
Size: Custom	Document Number: MS-1782	Rev: 2.0
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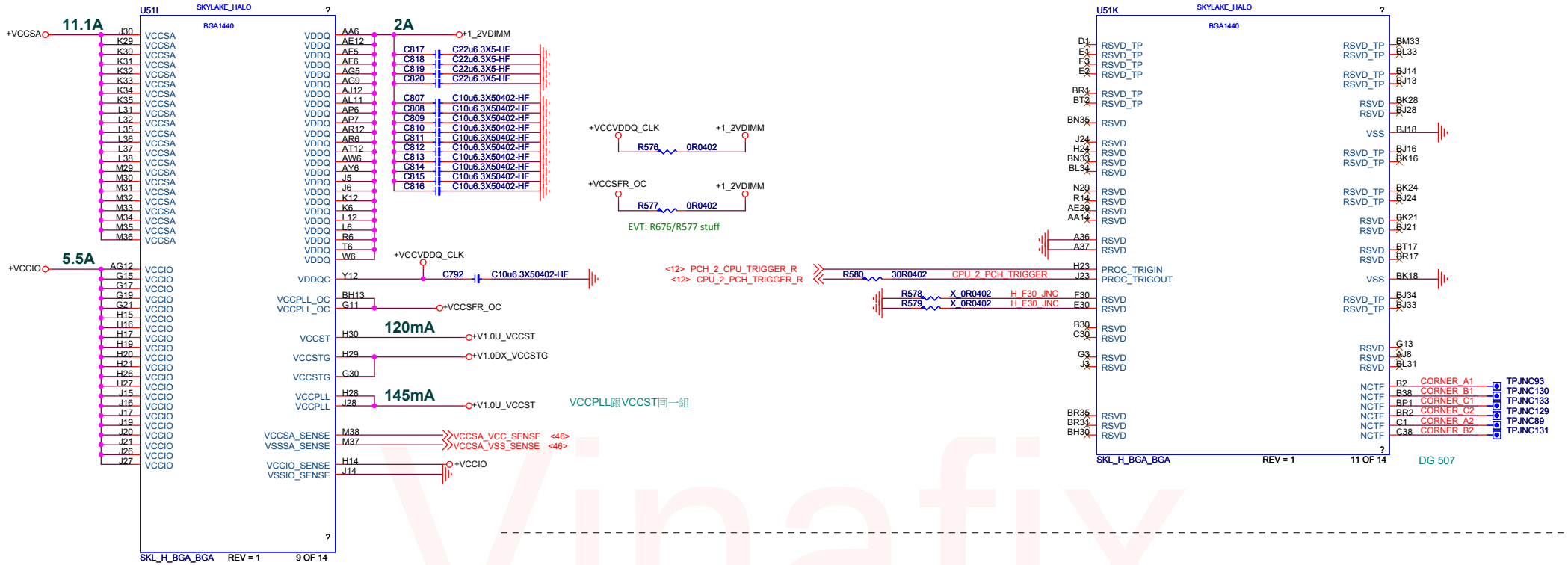

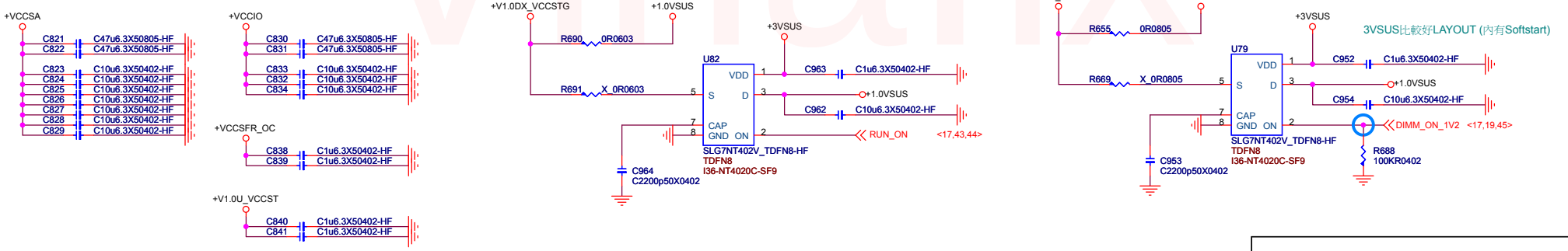

Title	<Title>		
Size	Document Number		Rev
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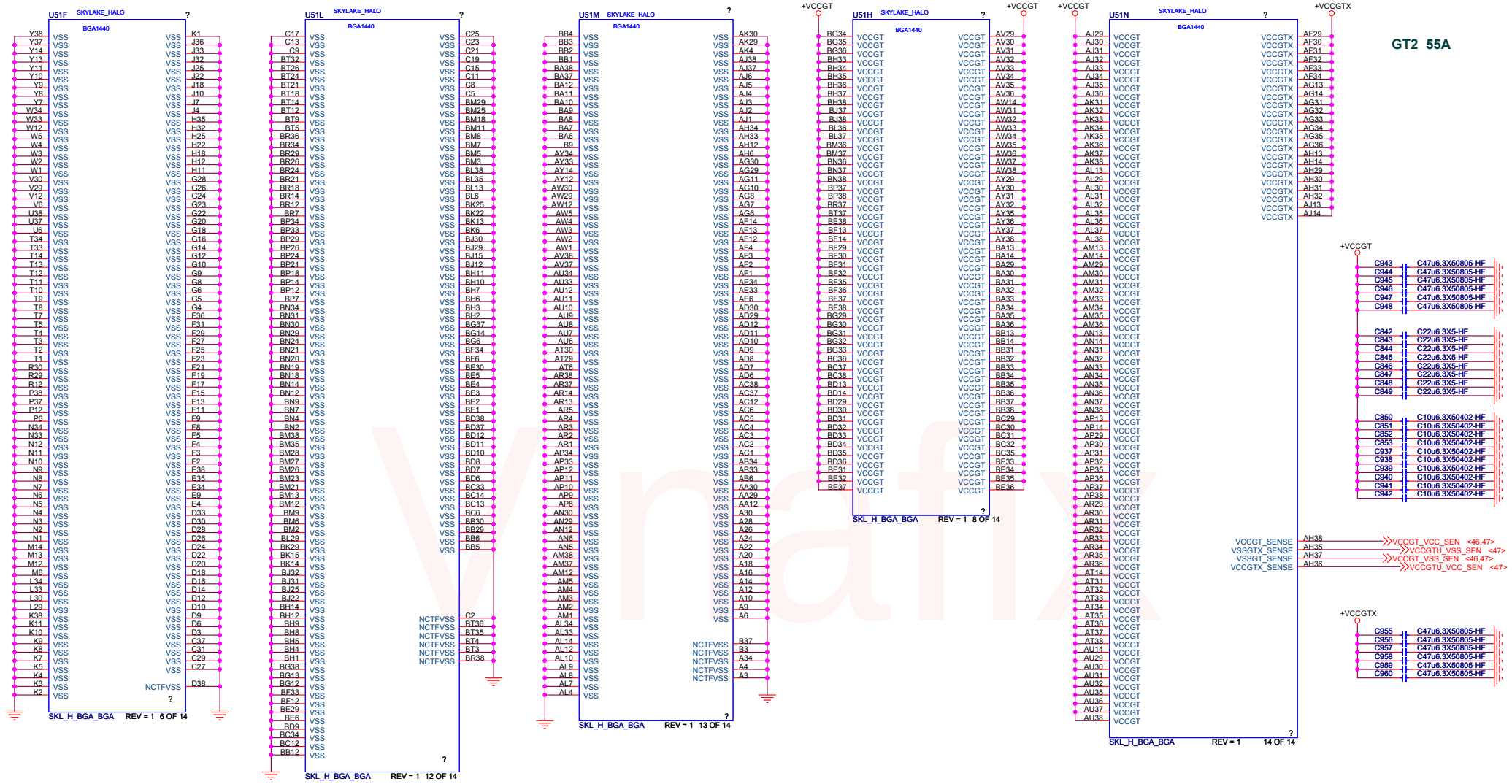

Title	<Title>		
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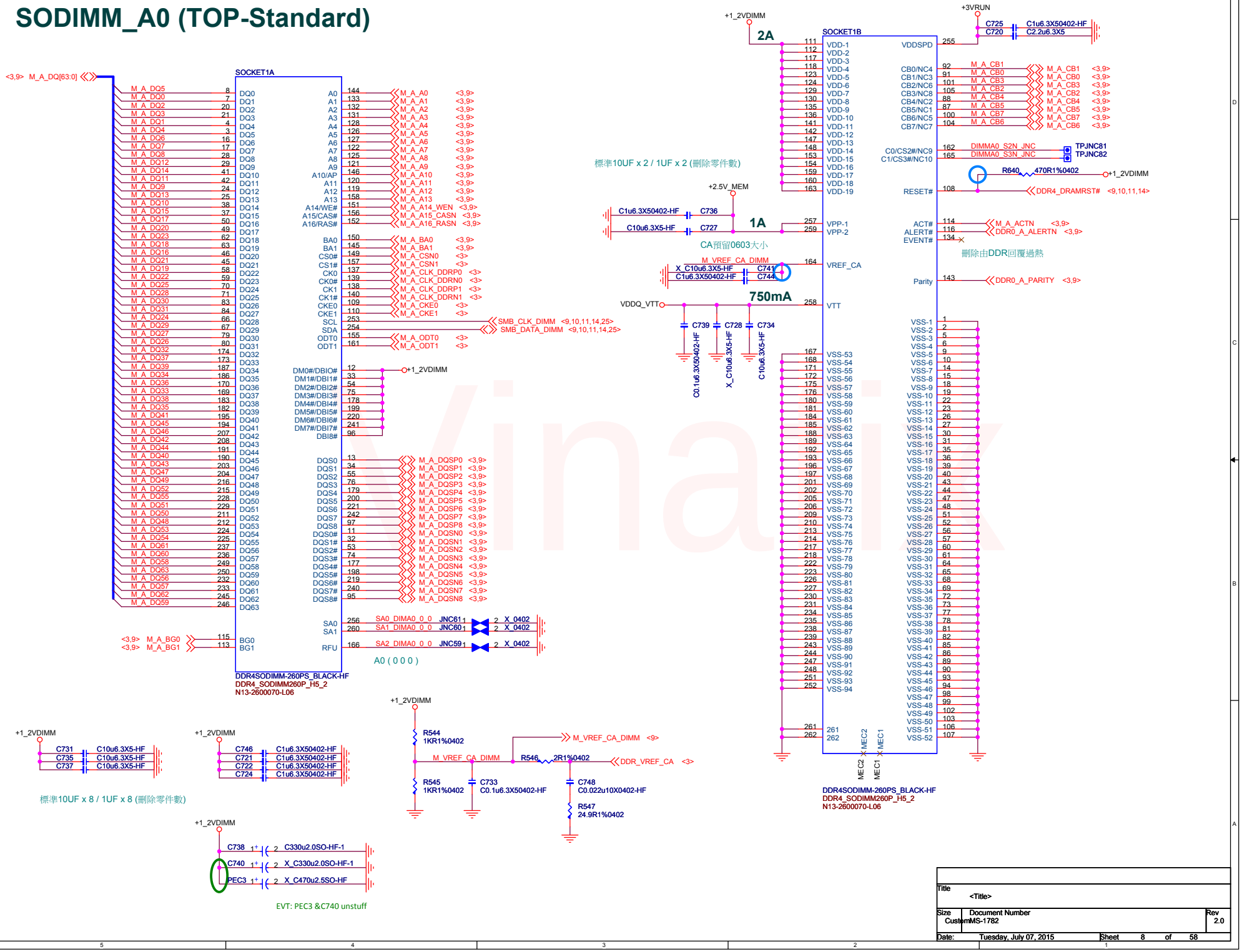
SODIMM_A0 (TOP-Standard)



Title	<Title>	
Size: Custom	Document Number: MS-1782	Rev: 2.0
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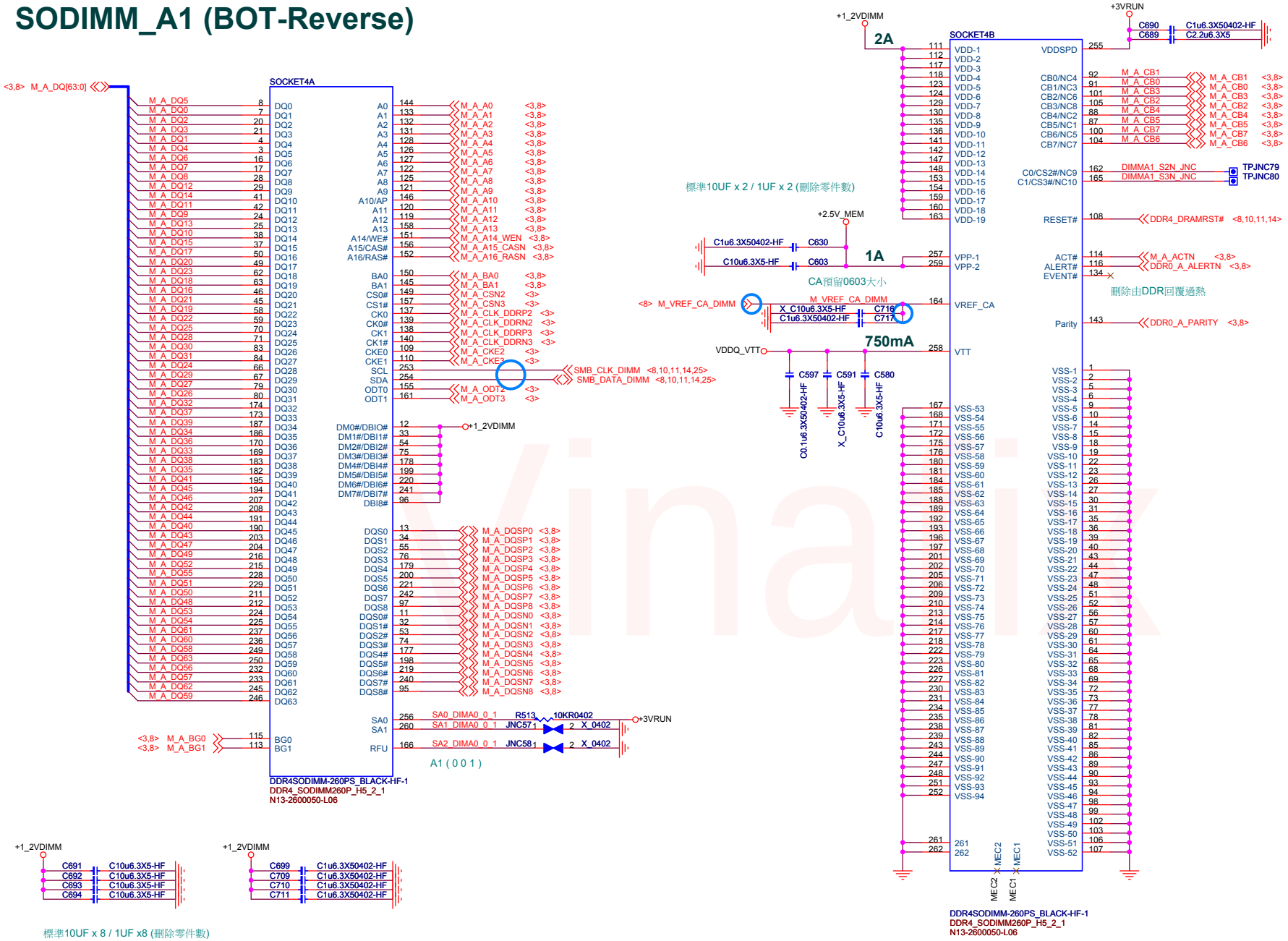
SODIMM_A1 (BOT-Reverse)



Title	<Title>		
Size: Custom	Document Number: MS-1782	Rev: 2.0	
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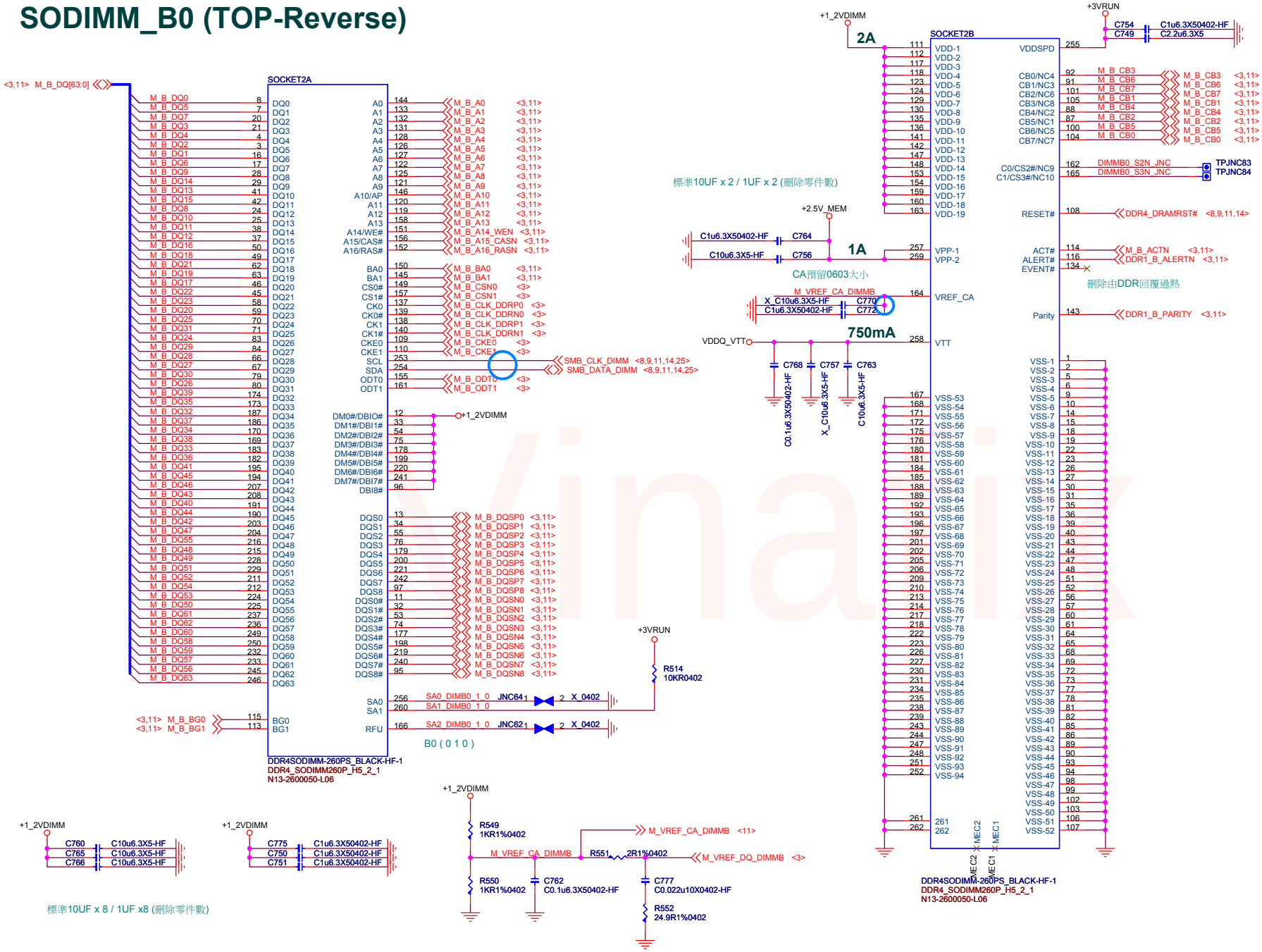
SODIMM_B0 (TOP-Reverse)



Title	<Title>
Size	Custom
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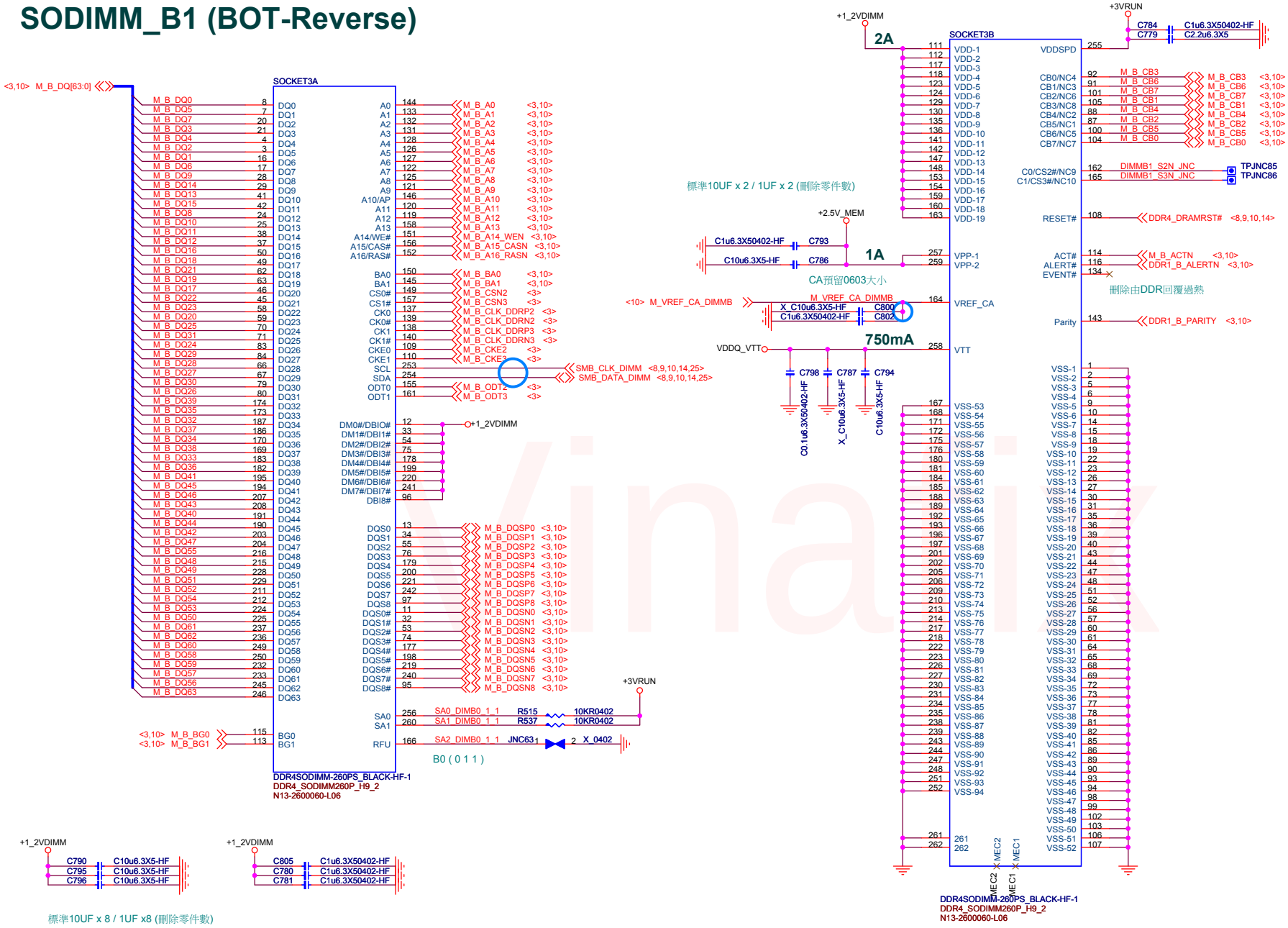
SODIMM_B1 (BOT-Reverse)



Title	<Title>		
Size: Custom	Document Number: MS-1782		Rev: 2.0
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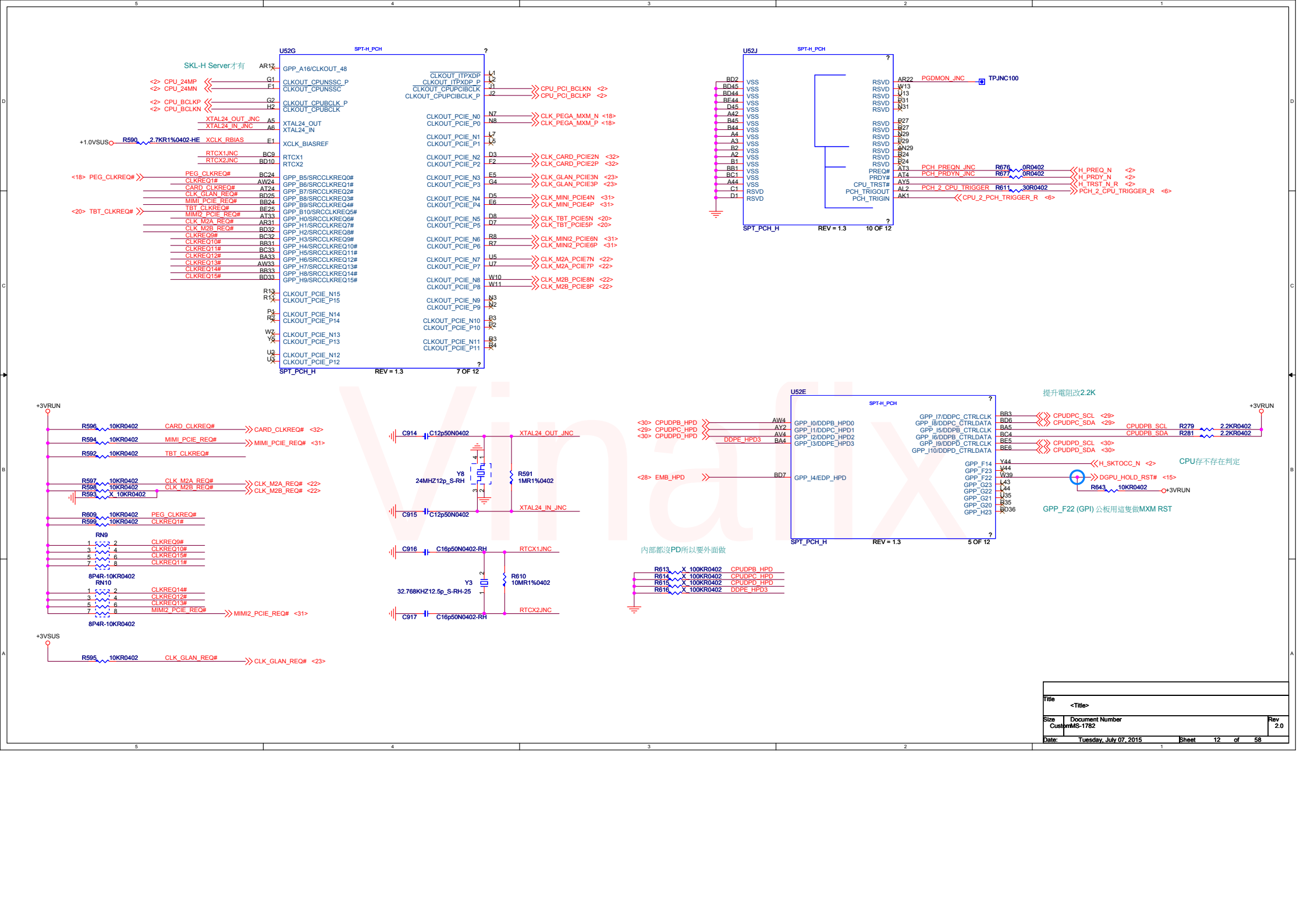
U52G
SPT-H_PCH
SKL-H Server才有
GPP_A16/CLKOUT_48
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK
XTAL24_OUT
XTAL24_IN
XCLK_BIASREF
RTCX1
RTCX2
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK
CLKOUT_CPUPCIBCLK_P
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
SPT_PCH_H
REV = 1.3
7 OF 12
U52J
SPT-H_PCH
VSS
RSVD
PGDMON_JNC
TPJNC100
PREQ#
PRDY#
CPU_TRST#
PCH_TRIGOUT
PCH_TRIGIN
PCH_PREON_JNC
PCH_PRDYN_JNC
PCH_2_CPU_TRIGGER
CPU_2_PCH_TRIGGER_R
SPT_PCH_H
REV = 1.3
10 OF 12
+1.0VSUS
R590 2.7KR1%0402-HE
+3VRUN
+3VSUS
R596 10KR0402 CARD_CLKREQ#
R594 10KR0402 MIMI_PCIE_REQ#
R592 10KR0402 TBT_CLKREQ#
R597 10KR0402 CLK_M2A_REQ#
R598 10KR0402 CLK_M2B_REQ#
R593 X_10KR0402
R609 10KR0402 PEG_CLKREQ#
R599 10KR0402 CLKREQ1#
RN9
RN10
8P4R-10KR0402
MIMI2_PCIE_REQ#
R595 10KR0402 CLK_GLAN_REQ#
C914 C12p50N0402
C915 C12p50N0402
Y8 24MHZ12p_S-RH
R591 1MR1%0402
XTAL24_OUT_JNC
XTAL24_IN_JNC
C916 C16p50N0402-RH
C917 C16p50N0402-RH
Y3 32.768KHZ12.5p_S-RH-25
R610 10MR1%0402
RTCX1JNC
RTCX2JNC
U52E
SPT-H_PCH
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_I4/EDP_HPD
GPP_I7/DDPC_CTRLCLK
GPP_I6/DDPC_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
CPUDPB_SCL
CPUDPB_SDA
CPUDPC_SCL
CPUDPC_SDA
CPUDPD_SCL
CPUDPD_SDA
R279 2.2KR0402
R281 2.2KR0402
提升電阻改2.2K
H_SKTOCC_N
CPU存不存在判定
DGPU_HOLD_RST#
R643 10KR0402
GPP_F22 (GPI) 公板用這隻做MXM RST
SPT_PCH_H
REV = 1.3
5 OF 12
內部都沒PD所以要外面做
R613 X_100KR0402 CPUDPB_HPD
R614 X_100KR0402 CPUDPC_HPD
R615 X_100KR0402 CPUDPD_HPD
R616 X_100KR0402 DDPE_HPD3
Title
<Title>
Size Custom
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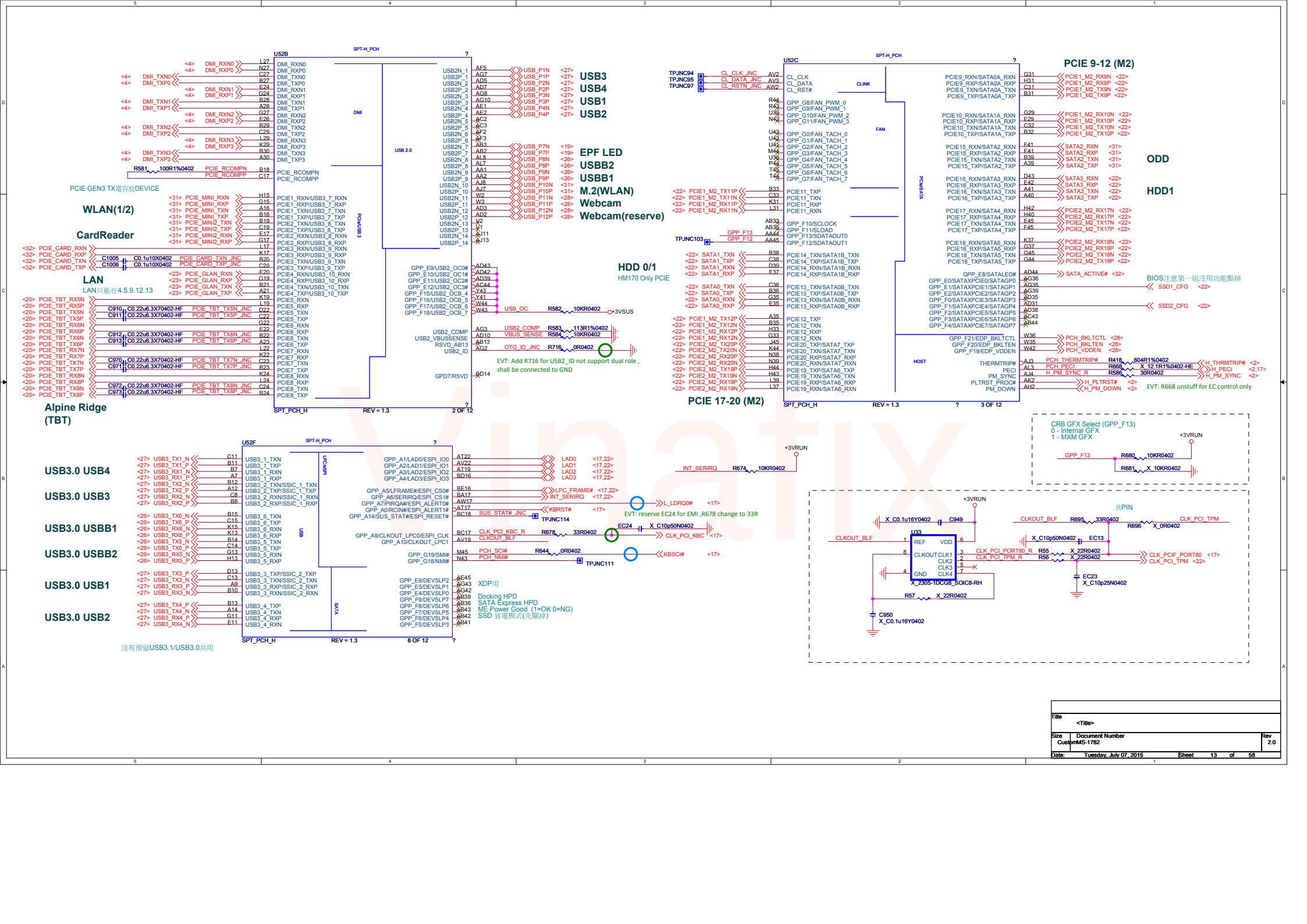
SPT-H_PCH
U52B
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI
USB 2.0
PCIe/USB 3
R581 100R1%0402
PCIE_RCOMPN
PCIE_RCOMPP
PCIE GEN3 TX電容放DEVICE
WLAN(1/2)
CardReader
LAN
LAN只能在4.5.9.12.13
Alpine Ridge
(TBT)
USB3
USB4
USB1
USB2
EPF LED
USBB2
USBB1
M.2(WLAN)
Webcam
Webcam(reserve)
HDD 0/1
HM170 Only PCIE
USB_OC
R582 10KR0402
+3VSUS
USB2_COMP
VBUS_SENSE
R583 113R1%0402
R584 10KR0402
OTG_ID_JNC
R716 0R0402
EVT: Add R716 for USB2_ID not support dual role ,
shall be connected to GND
SPT_PCH_H
REV = 1.3
2 OF 12
U52C
CL_CLK
CL_DATA
CL_RST#
CLINK
FAN
PCIe/SATA
HOST
TPJNC94 CL_CLK_JNC
TPJNC95 CL_DATA_JNC
TPJNC97 CL_RSTN_JNC
TPJNC103
PCIE 17-20 (M2)
PCIE 9-12 (M2)
ODD
HDD1
BIOS注意第一組沒用功能點掉
SSD1_CFG
SSD2_CFG
PCH_BKLTCTL
PCH_BKLTEN
PCH_VDDEN
PCH_THERMTRIP#
PCH_PECI
H_PM_SYNC_R
R418 604R1%0402
R668 X_12.1R1%0402-HE
R586 30R0402
H_THRMTRIP#
H_PECI
H_PM_SYNC
H_PLTRST#
H_PM_DOWN
EVT: R668 unstuff for EC control only
SPT_PCH_H
REV = 1.3
3 OF 12
USB3.0 USB4
USB3.0 USB3
USB3.0 USBB1
USB3.0 USBB2
USB3.0 USB1
USB3.0 USB2
USB3
USB2
SATA
XDP用
Docking HPD
SATA Express HPD
ME Power Good (1=OK 0=NG)
SSD 省電模式(先關掉)
沒有預留USB3.1/USB3.0共用
SPT_PCH_H
REV = 1.3
6 OF 12
INT_SERIRQ
R674 10KR0402
+3VRUN
KBRST#
TPJNC114
EVT: reserve EC24 for EMI ,R678 change to 33R
EC24 X_C10p50N0402
CLK_PCI_KBC
KBSCI#
TPJNC111
CRB GFX Select (GPP_F13)
0 - Internal GFX
1 - MXM GFX
GPP_F13
R680 10KR0402
R681 X_10KR0402
共PIN
X_C0.1u16Y0402
C949
CLKOUT_BLF
U33
X_2305-1DCG8_SOIC8-RH
R695 33R0402
R696 X_0R0402
CLK_PCI_TPM
X_C10p50N0402
EC13
CLK_PCI_PORT80_R
R55 X_22R0402
R56 X_22R0402
CLK_PCIF_PORT80
CLK_PCI_TPM
EC23
X_C10p25N0402
R57 X_22R0402
C950
X_C0.1u16Y0402
Title
<Title>
Size Custom
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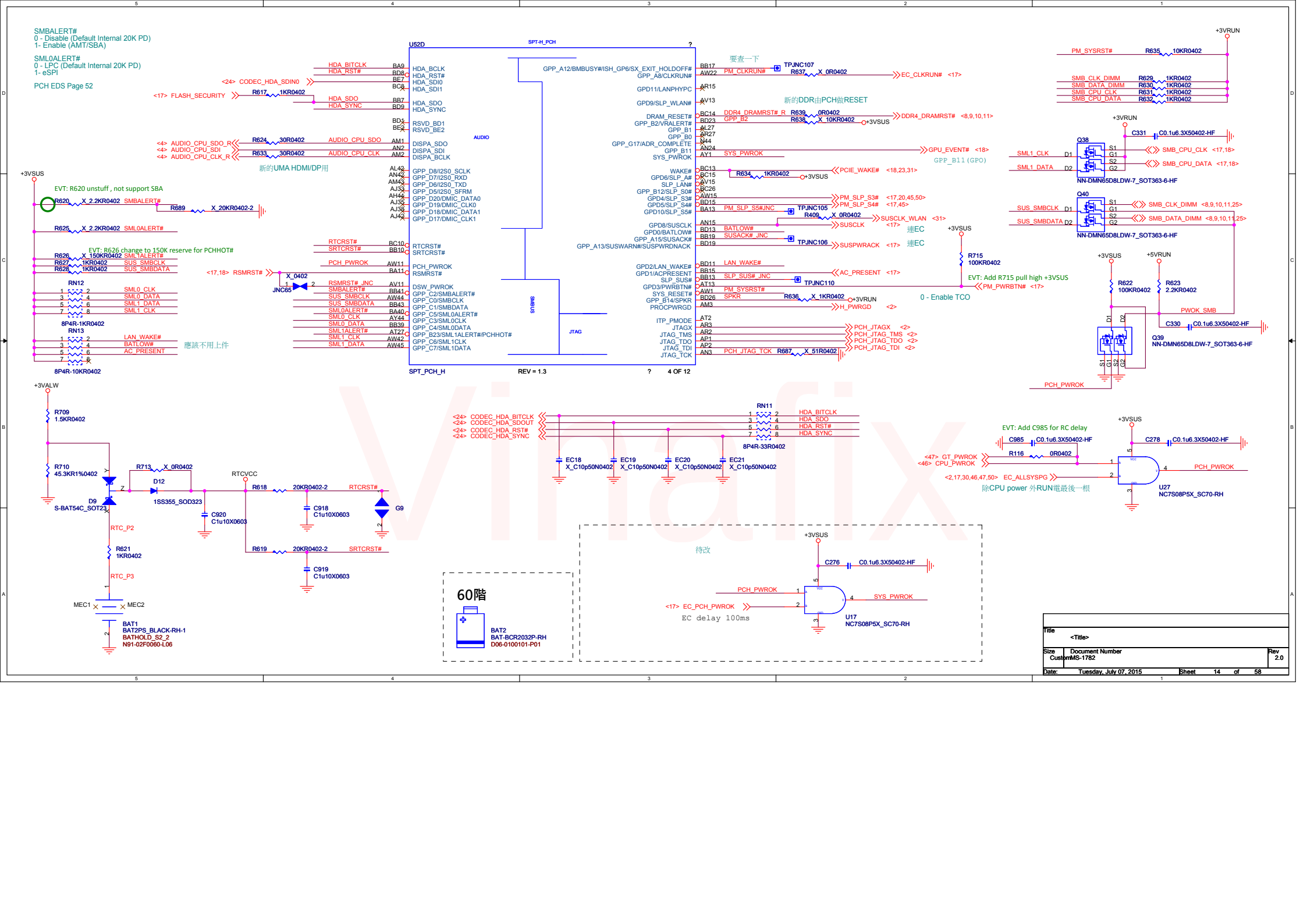
SMBALERT#
0 - Disable (Default Internal 20K PD)
1- Enable (AMT/SBA)
SML0ALERT#
0 - LPC (Default Internal 20K PD)
1- eSPI
PCH EDS Page 52
U52D
SPT-H_PCH
SPT_PCH_H
REV = 1.3
4 OF 12
AUDIO
SMBUS
JTAG
HDA_BITCLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_SYNC
RSVD_BD1
RSVD_BE2
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8/I2S0_SCLK
GPP_D7/I2S0_RXD
GPP_D6/I2S0_TXD
GPP_D5/I2S0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_A12/BMBUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
要查一下
新的DDR由PCH做RESET
新的UMA HDMI/DP用
EVT: R620 unstuff , not support SBA
EVT: R626 change to 150K reserve for PCHHOT#
應該不用上件
連EC
連EC
EVT: Add R715 pull high +3VSUS
0 - Enable TCO
GPP_B11 (GPO)
EVT: Add C985 for RC delay
除CPU power 外RUN電最後一根
待改
60階
BAT2
BAT-BCR2032P-RH
D06-0100101-P01
BAT1
BAT2PS_BLACK-RH-1
BATHOLD_S2_2
N91-02F0060-L06
NN-DMN65D8LDW-7_SOT363-6-HF
8P4R-1KR0402
8P4R-10KR0402
8P4R-33R0402
S-BAT54C_SOT23
1SS355_SOD323
NC7S08P5X_SC70-RH
Title
<Title>
Size
Custom
Document Number
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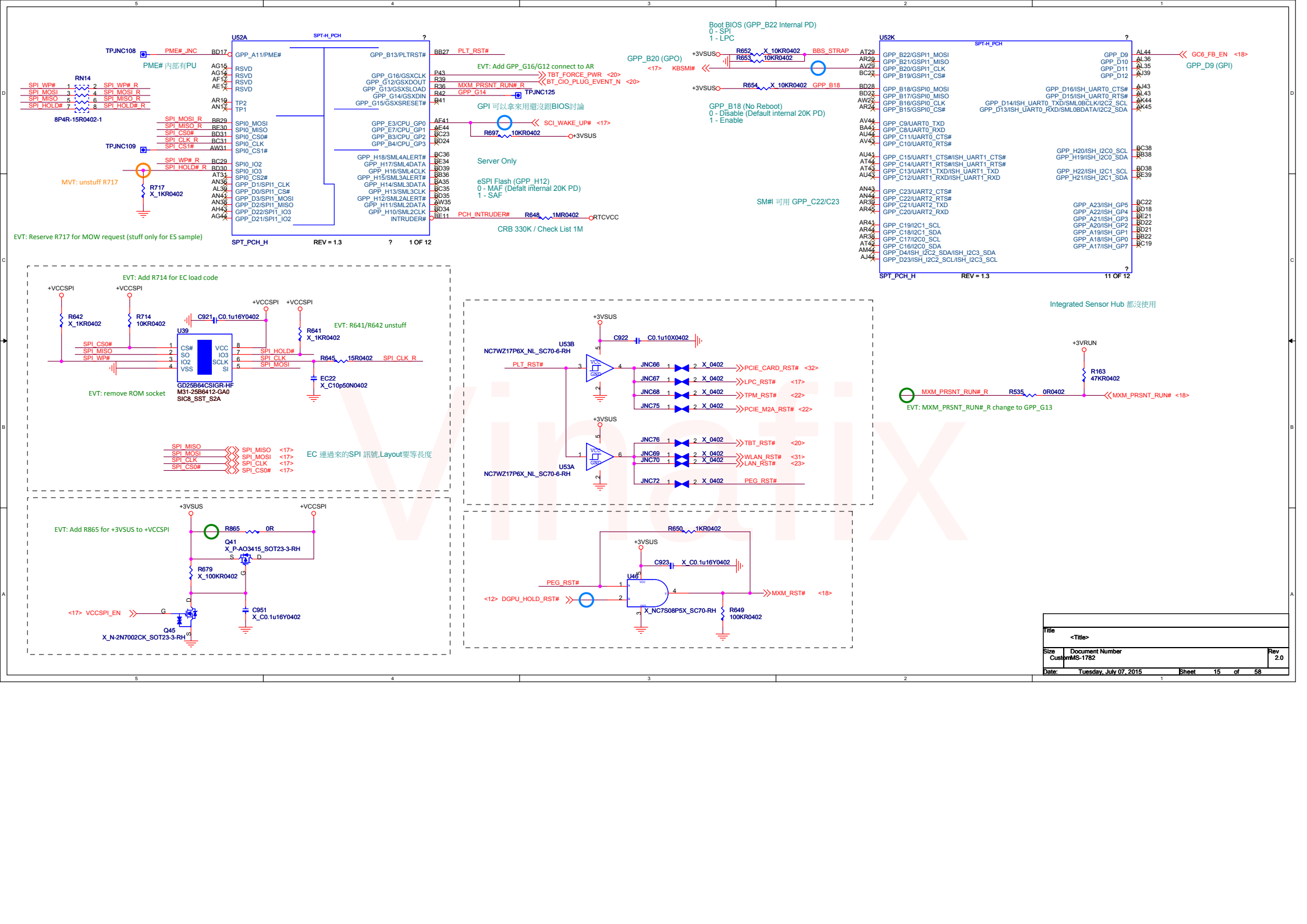
U52A
SPT-H_PCH
TPJNC108
PME#_JNC
PME# 內部有PU
RN14
SPI_WP#
SPI_MOSI
SPI_MISO
SPI_HOLD#
8P4R-15R0402-1
TPJNC109
MVT: unstuff R717
R717
X_1KR0402
EVT: Reserve R717 for MOW request (stuff only for ES sample)
GPP_A11/PME#
RSVD
TP2
TP1
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPD_D1/SPI1_CLK
GPD_D0/SPI1_CS#
GPD_D3/SPI1_MOSI
GPD_D2/SPI1_MISO
GPD_D22/SPI1_IO3
GPD_D21/SPI1_IO2
GPP_B13/PLTRST#
PLT_RST#
EVT: Add GPP_G16/G12 connect to AR
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXSRESET#
TBT_FORCE_PWR
BT_CIO_PLUG_EVENT_N
MXM_PRSNT_RUN#_R
GPP_G14
TPJNC125
GPI 可以拿來用還沒跟BIOS討論
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
SCI_WAKE_UP#
R697
10KR0402
+3VSUS
Server Only
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
PCH_INTRUDER#
R648
1MR0402
RTCVCC
CRB 330K / Check List 1M
SPT_PCH_H
REV = 1.3
1 OF 12
GPP_B20 (GPO)
KBSMI#
Boot BIOS (GPP_B22 Internal PD)
0 - SPI
1 - LPC
R652
X_10KR0402
R653
10KR0402
BBS_STRAP
R654
GPP_B18
GPP_B18 (No Reboot)
0 - Disable (Default internal 20K PD)
1 - Enable
SM# 可用 GPP_C22/C23
U52K
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA
GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL
GPP_D9
GPP_D10
GPP_D11
GPP_D12
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C2_SCL
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C2_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/ISH_GP7
GC6_FB_EN
GPP_D9 (GPI)
EVT: Add R714 for EC load code
+VCCSPI
R642
X_1KR0402
R714
10KR0402
C921
C0.1u16Y0402
U39
CS#
SO
IO2
VSS
VCC
IO3
SCLK
SI
GD25B64CSIGR-HF
M31-25B6412-GA0
SIC8_SST_S2A
EVT: remove ROM socket
R641
X_1KR0402
EVT: R641/R642 unstuff
R645
15R0402
SPI_CLK_R
EC22
X_C10p50N0402
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_CS0#
EC 連過來的SPI 訊號,Layout要等長度
U53B
NC7WZ17P6X_NL_SC70-6-RH
U53A
C922
C0.1u10X0402
PLT_RST#
JNC66
JNC67
JNC68
JNC75
JNC76
JNC69
JNC70
JNC72
X_0402
PCIE_CARD_RST#
LPC_RST#
TPM_RST#
PCIE_M2A_RST#
TBT_RST#
WLAN_RST#
LAN_RST#
PEG_RST#
Integrated Sensor Hub 都沒使用
+3VRUN
R163
47KR0402
MXM_PRSNT_RUN#_R
R535
0R0402
MXM_PRSNT_RUN#
EVT: MXM_PRSNT_RUN#_R change to GPP_G13
EVT: Add R865 for +3VSUS to +VCCSPI
R865
0R
Q41
X_P-AO3415_SOT23-3-RH
R679
X_100KR0402
VCCSPI_EN
Q45
X_N-2N7002CK_SOT23-3-RH
C951
X_C0.1u16Y0402
R650
1KR0402
C923
X_C0.1u16Y0402
U46
X_NC7S08P5X_SC70-RH
DGPU_HOLD_RST#
MXM_RST#
R649
100KR0402
Title
<Title>
Size
Custom
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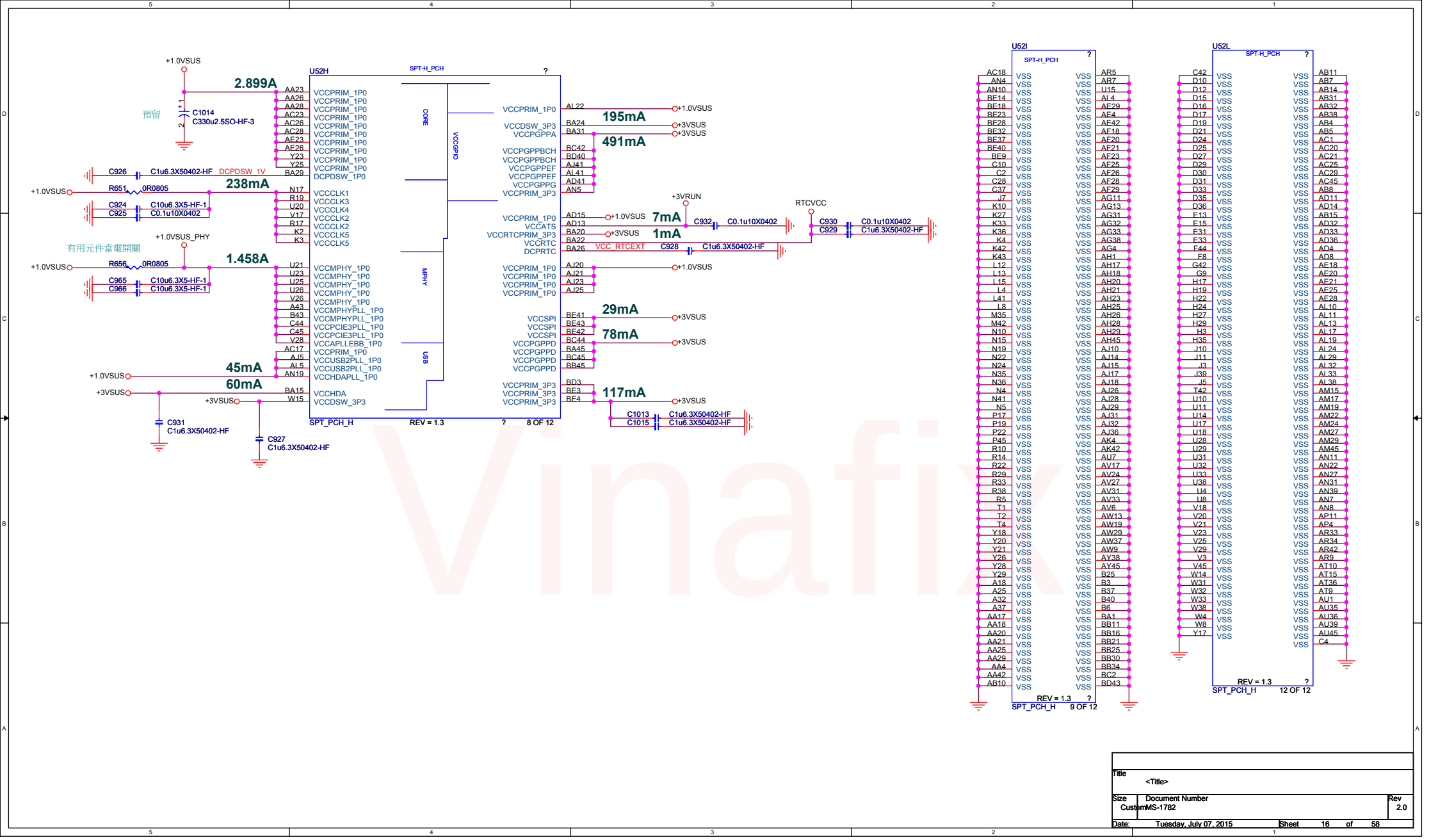

Vinafix

Title	<Title>	
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RSMRST# follow DG modify to 10K

KBC/EC/uP (ENE9028)

PU/PD

+3VRUN
R509 X 10KR0402 KBSMI#
R491 X 10KR0402 KBSCI#
R492 X 10KR0402 EC_GA20
R453 X 10KR0402 KBRST#
R461 X 100KR0402 EC_CLKRUN#
R445 47KR0402 RSMRST#
R460 100KR0402 KBRST#

EC Reset

<32> ECRST_SW# R528 33R0402 EC_RST#

LID pull hi 10K

+3VSUS
R345 10KR0402 LID#

+3VSUS
R202 47KR0402 MXM_PRSNT#

+3VALW
R495 4.7KR0402 BATCLK_M
R489 4.7KR0402 BATDATA_M

MB Power SW

+3VALW
R299 10KR0402
PWR_SW#
SW1
C360 X_C0.1u16Y0402
SW-TACTB1S-HF
SWTA_S6_5_2X6_3
N71-0101630-D02

Debug Port

LPC_FRAME# LAD3 LAD2 LAD1 LAD0
<13> L_LDRQ0#
<13> CLK_PCIF_PORT80
INT_SERIRQ LPC_RST#
+5VRUN +3VRUN
FWH_ID0
R534 X_10KR0402
CON11
BH1X14HS-1.25PITCH_WHITE-RH
53398_14
N32-1140060-H06

U37 KB9028Q-C-RH

LPC I/F

<13,22> INT_SERIRQ
<13,22> LPC_FRAME#
<13> CLK_PCI_KBC
<14> EC_CLKRUN#
<13,22> LAD0
<13,22> LAD1
<13,22> LAD2
<13,22> LAD3

SERIRQ
LFRAME#
PCICLK
CLKRUN#/GPIO1D
LAD0
LAD1
LAD2
LAD3

ESB

<32> ESB_CLK
<32> ESB_DATA
R488 22R0402 ESB_CLK_JNC
GPIO0B/ESB_CLK
GPIO0C/ESB_DAT_O

CIR

原DIMM_ON
KBIN6
KBIN7
<44> DIMM_ON_2V5
<18> MXM_PWRSR_EN
GPIO40/AD6
GPIO41/CIR_RLC_TX/AD7
GPIO0A/OWM
GPIO0D/RLC_TX2

SPI FLASH

<15> SPI_MISO
<15> SPI_MOSI
<15> SPI_CLK
<15> SPI_CS0#
MISO/GPIO5B
MOSI/GPIO5C
SPICLK/GPIO58
SPICS#/GPIO5A

PS2 I/F

<32> TP_CLK
<32> TP_DATA
<31> WLAN_PWR_ON
<27> CTL3_EC
<19,42> BATCLK_M
<19,42> BATDATA_M
PSCLK3/GPIO4E
PSDAT3/GPIO4F
PSCLK2/GPIO4C/SCL3
PSDAT2/GPIO4D/SDA3
PSCLK1/GPIO4A/SCL2/SMBD_CLK
PSDAT1/GPIO4B/SDA2/SMBD_DAT

UART

JNC73 X_0402 E51TXD_JNC
JNC74 X_0402 E51CLK_JNC
<19> EPF021_RST
<19> EPF021_OPMODE
E51TXD/GPIO16
E51CLK/GPIO17
GPIO5D
GPIO5E

POWER/GROUND

VCC_LPC
VCC
VCC-1
VCC-2
VCC-3
VCC0
VCC_IO2
AVCC
AGND
GND
GND-1
GND-2
GND-3
GND-4

C632 C0.1u10X0402
C572 C0.1u10X0402
C596 C0.1u10X0402
C550 C0.1u10X0402
C609 C0.1u10X0402
+3VALW

FAN&PWM

hybrid power boost mode
BM#_JNC 改名TB_STAR#
<42> TB_STAR#
<14> FLASH_SECURITY
<28> PANEL_ON
<42> AC_CTL
<15> LPC_RST#
<31> BT_PWR_ON
<28> CAMERA_ON
<31> CPUFAN_FB
<31> MXMFAN_FB
TPJNC123 EC_RST#
<13> KBRST#
<13> KBSCI#
EC_GA20
PWM0/GPIO0F
PWM1/GPIO10
PWM2/GPIO11
PWM3/GPIO19
FANPWM0/GPIO12
FANPWM1/GPIO13
FANFB0/GPIO14
FANFB1/GPIO15

SMBUS

SDA0/GPIO45
SCL0/GPIO44
IEDI_SDA/SDA1/GPIO47
IEDI_SCL/SCL1/GPIO46
EC_SDA
EC_SCL
SMB_CPU_DATA <14,18>
SMB_CPU_CLK <14,18>

AD/DA

DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
AD4/GPI42
AD5/GPI43
KBIN0
KBIN1
KBIN2
KBIN3
KBIN4
KBIN5
CPUFAN_PWM <31>
MXMFAN_PWM <31>
SUSPWRACK <14>

IKB

KBOUT0 KBOUT1 KBOUT2 KBOUT3 KBOUT4 KBOUT5 KBOUT6 KBOUT7 KBOUT16 KBOUT17
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25/UART_SOUT
KSO6/GPIO26
KSO7/GPIO27/SERIRQ(LPC_Bypass)UART_RTS
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B/LAD3(LPC_Bypass)
KSO12/GPIO2C/LAD2(LPC_Bypass)UART_DTR
KSO13/GPIO2D/LAD1(LPC_Bypass)
KSO14/GPIO2E/LAD0(LPC_Bypass)
KSO15/GPIO2F
KSO16/GPIO48/UART_SOUT2
KSO17/GPIO49
<18> MXM_PRSNT#
<27> CTL1_EC
<42> BATT_EN
<42> BAT_IN#
<28,32> LID#
<44> SUSPWROK
TPJNC121 EC_SDA
TPJNC122 EC_SCL

SDI

GPXIOA09/GPIO60/SHICS#
GPXIOA01/GPIO61/SHICLK
GPXIOA02/GPIO62/SHIDO
EC_MUTE# <24>
MUTE# <25>
HDMI_HPD_DET <29>

KSI/KSO

KBOUT8 KBOUT9 KBOUT10 KBOUT11 KBOUT12 KBOUT13 KBOUT14 KBOUT15
KSI0/GPIO30/E51TXD
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37/EDI_DO

POWER_FAIL0

POWER_FAIL0/GPIO63/GPXIOA03
GPIO64/GPXIOA04
GPIO65/GPXIOA05
VCOUT1/GPIO66/GPXIOA06
VCOUT0/GPIO67/GPXIOA07
GPIO68/GPXIOA08
GPIO69/GPXIOA09
GPIO6A/GPXIOA10
GWG/GPIO6B/GPXIOA11
SDIDO/GPIO78/GPXIOD00
GPIO79/GPXIOD01
EC_EN#/GPIO7A/GPXIOD02
GPIO7B/GPXIOD03
GPIO7C/GPXIOD04
GPIO7D/GPXIOD05
GPIO7E/GPXIOD06
GPIO7F/PECI
VCCSPI_EN
MB_ID
SUS_ON <43>
VCCSPI_EN <15>
DIMM_ON_1V2 <6,19,45>
EC_PROCHOT# <2>
LED_WLAN# <32>
LED_CHARGE# <32>
LED_BATLOW# <32>
AC_PRESENT <14>
ADP_ICC <42>
AC_OK <42>
AC_OK改成High AC Adapter
MXM_ACOK_EC
PWR_SW# <32>
EC_ALLSYSPG
RUN_ON <6,43,44>
H_PECI_R R443 33R0402
PM_PWRBTN# <14>
H_PECI <2,13>
KBSMI# <15>
i_clk_8051/GPIO07
PROCHOT#/i_clk_pei/GPIO08
POWER_FAIL1/GPIO18
MXM_RUN_EN# <18,28,29,30>
SCI_WAKE_UP# <15>
EC_PCH_PWROK <14>
GPIO50
GPIO52
WDT_LED#/GPIO54
GPIO56
XCLK32K/GPIO57
GPIO59
USB_ENABLE <26,27>
LED_PWR# <32>
RSMRST# <14,18>
PM_SLP_S3# <14,20,45,50>
PM_SLP_S4# <14,45>

LED

GPIO1A/NUMLED#
GPIO53/CAPSLED#
GPIO55/SCROLED#
LED_NUM# <26>
LED_CAP# <19>

CLOCK

R442 0R0402 EC_XIN_JNC EC_XOUT_JNC
<14> SUSCLK
ER1 X_22R0402
Y7 X_32.768KHZ12.5p_S-RH-21
R437 680KR0402-HE
C546 X_C22p50N0402
C548 X_C16p50N0402-RH
C547 X_C16p50N0402-RH

CON9

KBOUT17 KBOUT16 KBIN0 KBIN1 KBIN2 KBIN3 KBIN4 KBIN5 KBIN6 KBIN7 KBOUT15 KBOUT14 KBOUT13 KBOUT12 KBOUT11 KBOUT10 KBOUT9 KBOUT8 KBOUT7 KBOUT6 KBOUT5 KBOUT4 KBOUT3 KBOUT2 KBOUT1 KBOUT0
CON9
FPC26P-B-1PITCH_BLACK-RH
FPC_S26_7
N5A-26F0340-H06

For EMI

KBOUT17 EC8 C100p16N0402
KBOUT16 EC9 C100p16N0402
EC15 8p4C-100p50N0402-RH
EC14 8p4C-100p50N0402-RH
EC16 8p4C-100p50N0402-RH
EC17 8p4C-100p50N0402-RH

MotherBoard ID

+3VALW
R520 10KR0402
MB_ID
R519 X_10KR0402
EVT: default pull high

AC_OK#	MXM_ACOK_EC	Mode
0	0	AC
0	1	AC
1	0	AC
1	1	DC

+3VRUN
R511 X_10KR0402
C635 X_C0.1u16Y0402
R524 X_10KR0402
<42> AC_INTERRUPT
HW_CTRL <2>
U42 X_74AHC1G09GV_SC74A5-HF
C660 X_C0.1u16Y0402

+3VRUN
R444 10KR0402
<44> +1_1VRUN_PWRGD
<50> VCCIO_PWRGD
R118 0R0402
R115 0R0402
<18> MXM_PWROK
R72 X_0R0402
EC_ALLSYSPG <2,14,30,46,47,50>
C636 X_C10p50N0402
5/15 reserve C636

+3VALW
R682 100KR0402
AC_OK
Q17 N-2N7002CK_SOT23-3-RH

+3VRUN_MXM
R683 X_100KR0402
MXM_ACOK <18>
MXM internal PU 100K
Q42 NN-DMN65D8LDW-7_SOT363-6-HF
MXM_ACOK_EC
AC_OK#
R684 X_0R0402

+3VALW
RN16 8P4R-10KR0402
RN17 8P4R-10KR0402
KBIN3 KBIN2 KBIN1 KBIN0
KBIN5 KBIN7 KBIN6 KBIN4
EVT: KBIN add 10K pull high to +3VALW for EC request

MICRO-STAR INT'L CO.,LTD.

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MXM 3.1 (x16 PEG Gen 3)

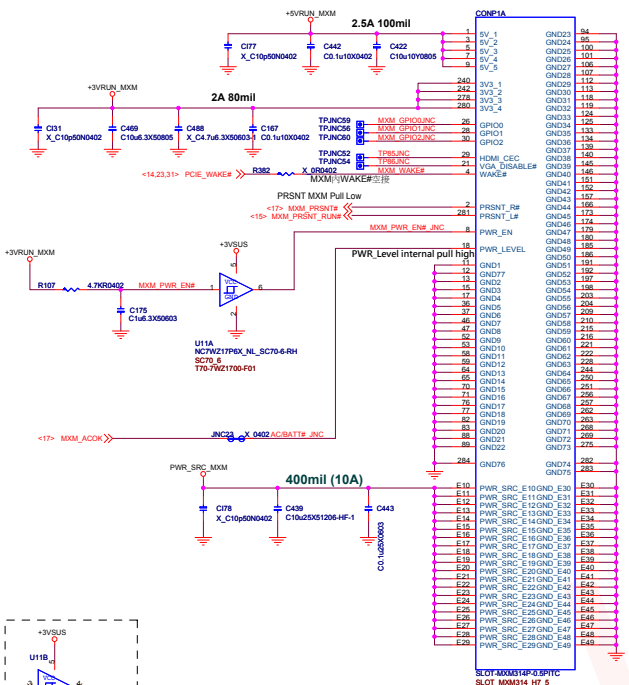
GB3-256 Split Mode EF	
Link AB	Not Connected
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link)
Link F	DisplayPort/eDP, DVI (Single Link)

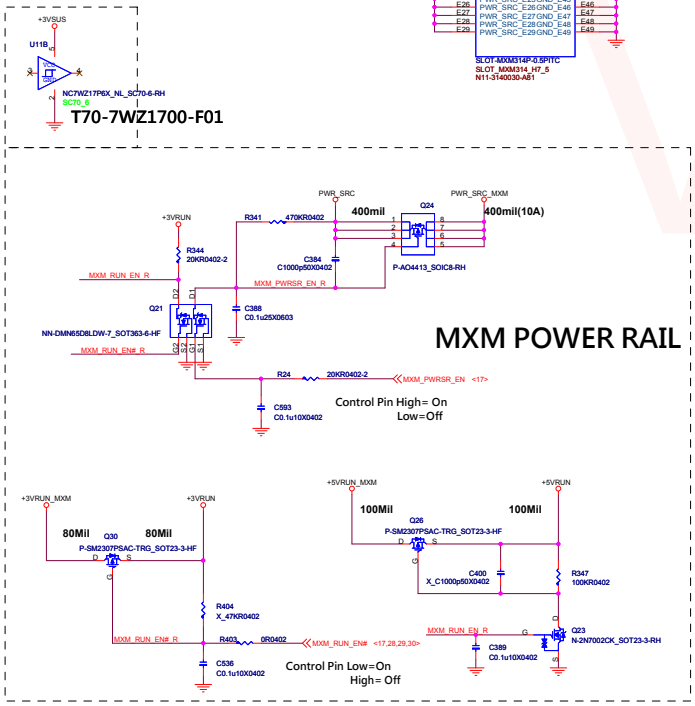
External DP1=Link E

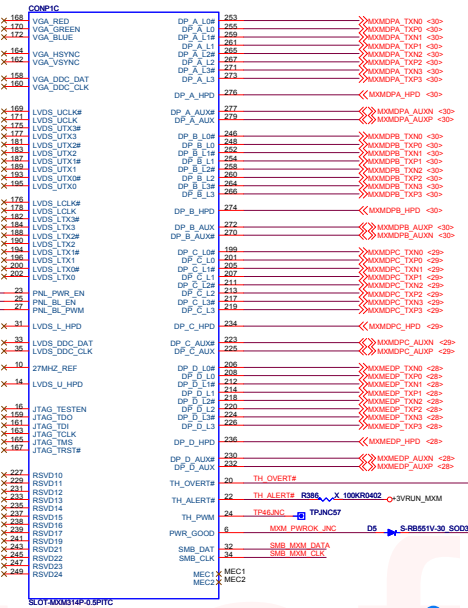
External DP2=Link F

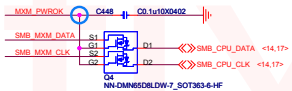
External HDMI=Link C

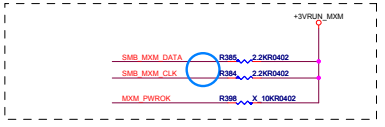
eDP=Link D

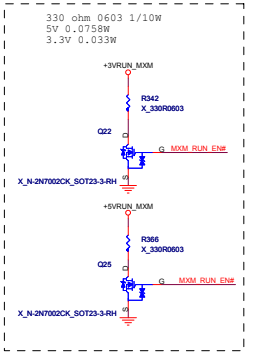




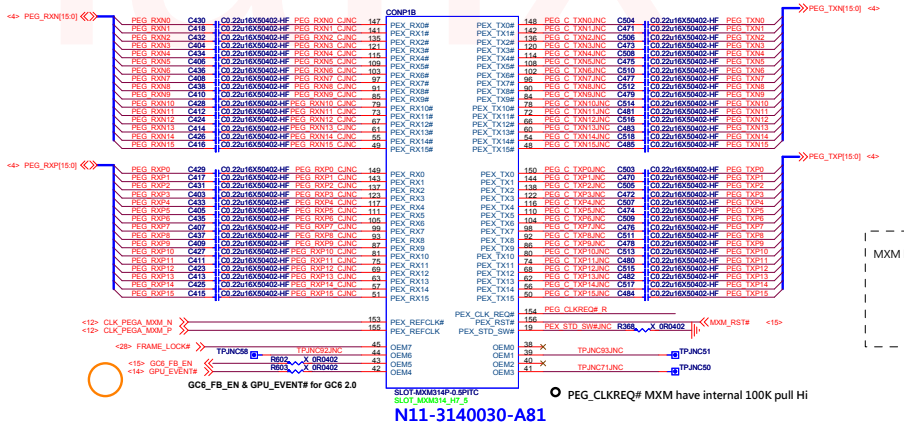


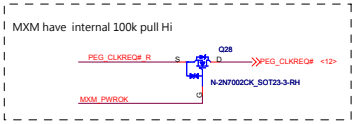






The change in AC capacitor value from 0.1uf to 0.22uf is to enable compatibility with futrue platforms having PCIE GEN3(8GT/s)





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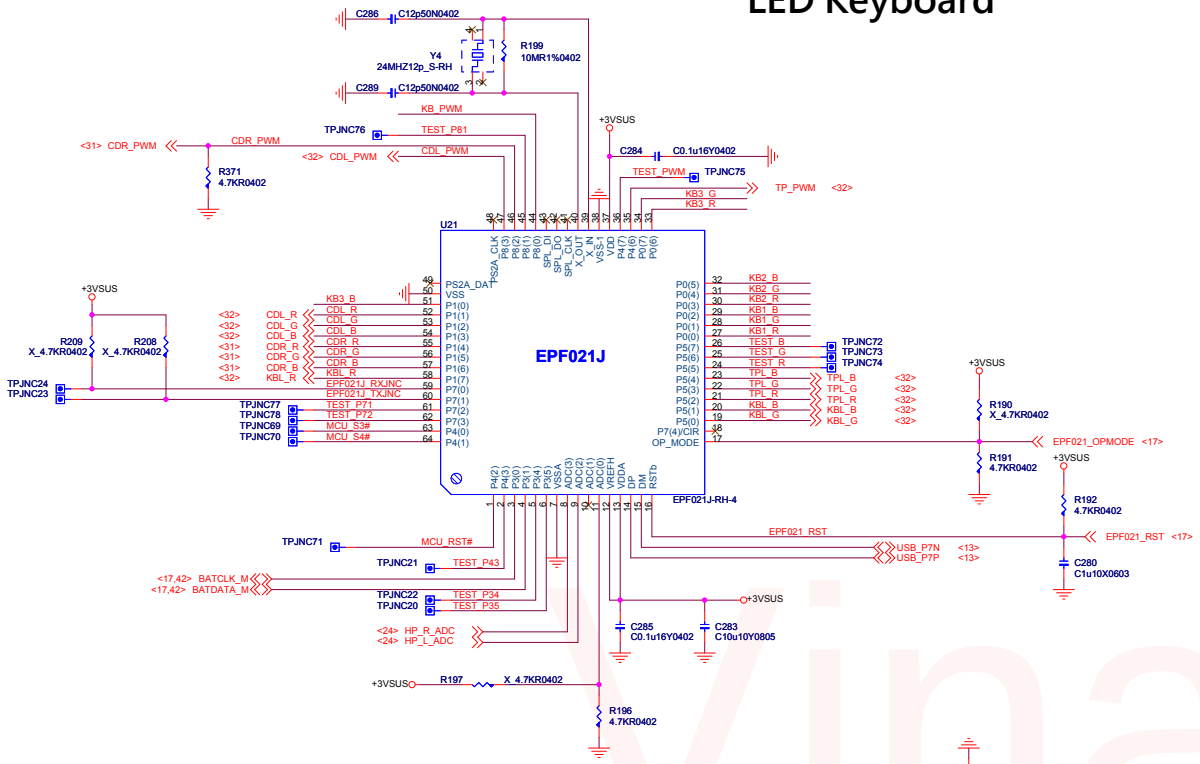
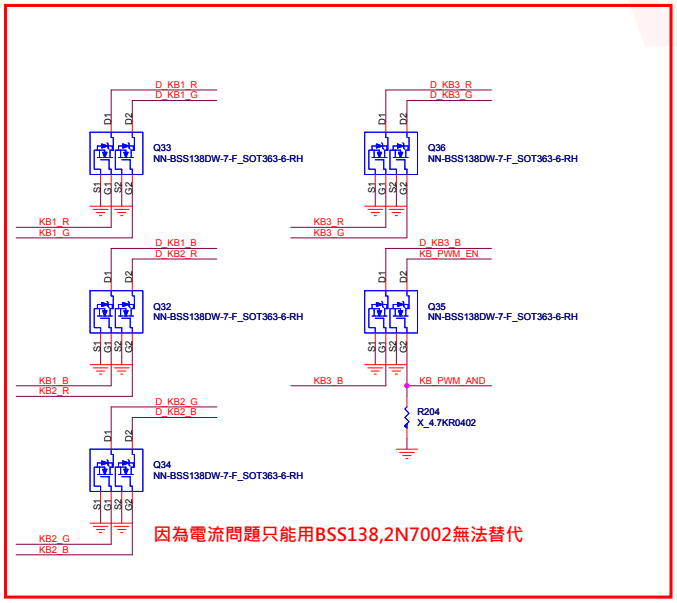
LED 8051 Controller

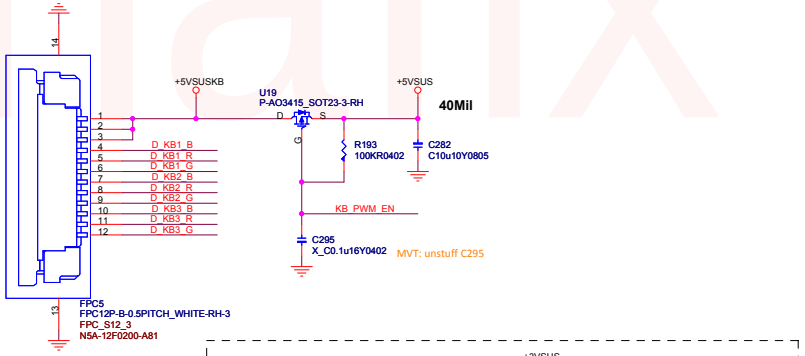
LED Keyboard

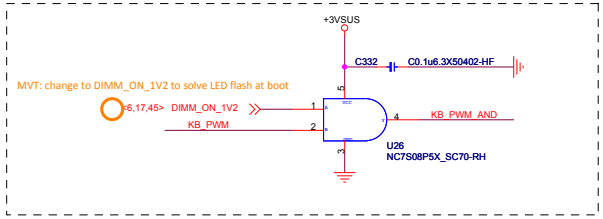


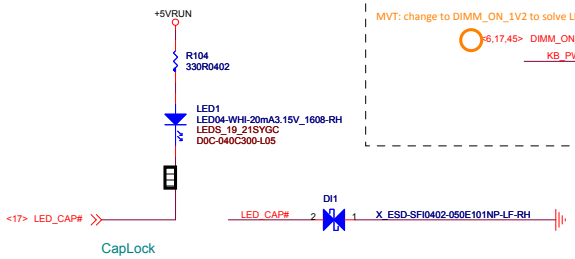
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

PIN1 要接 CON 的 PIN1









msi	MICRO-STAR INT'L CO.,LTD.
Title	LED Driver IC/ LED 8051
Size	Document Number: MS-1782
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Date:	Tuesday, July 07, 2015
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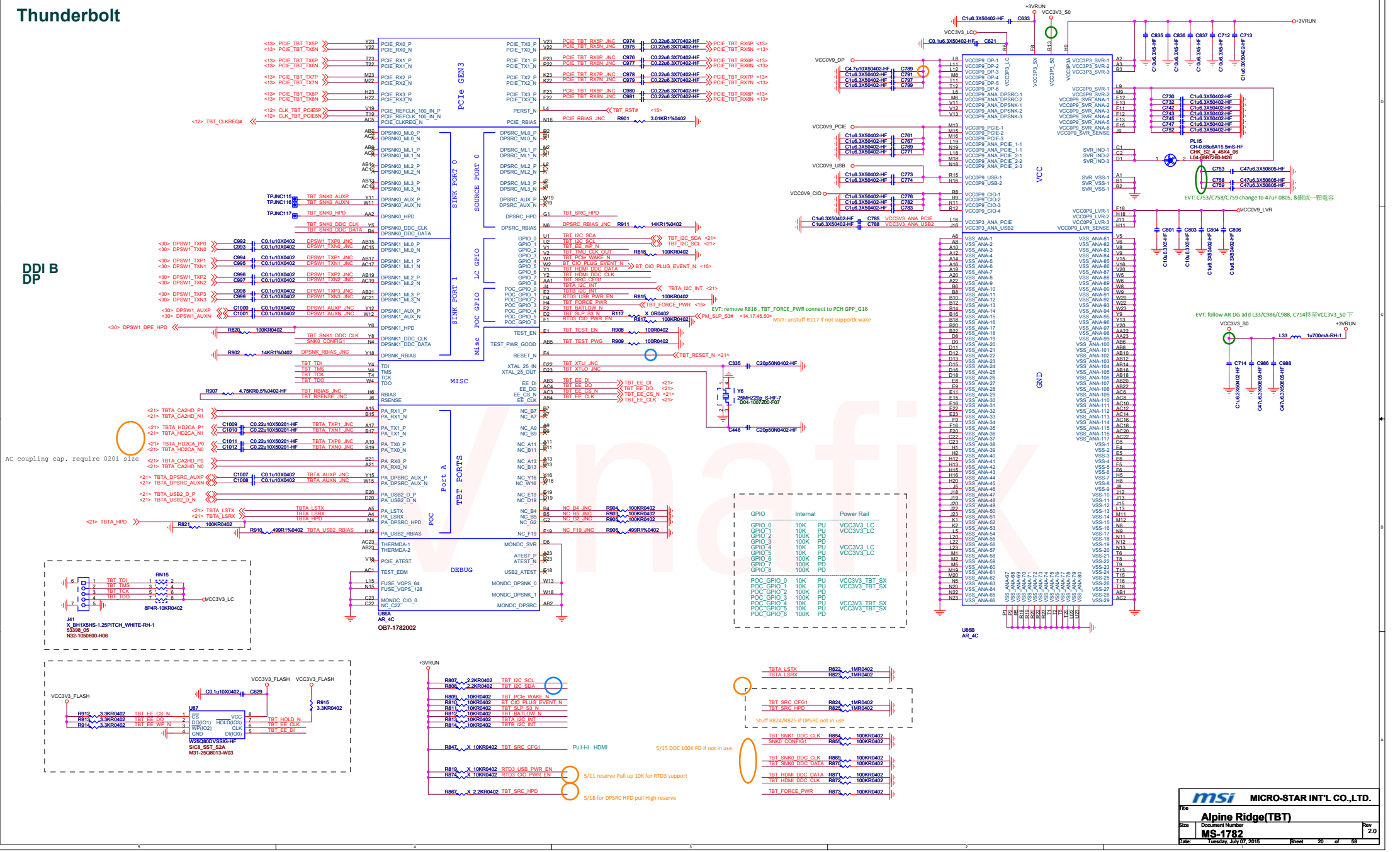
Thunderbolt

DDI B DP



GPIO	Internal		Power Rail
GPIO_0	10K	PU	VCC3V3_LC
GPIO_1	10K	PU	VCC3V3_LC
GPIO_2	100K	PD	
GPIO_3	100K	PD	
GPIO_4	10K	PU	VCC3V3_LC
GPIO_5	10K	PU	VCC3V3_LC
GPIO_6	100K	PD	
GPIO_7	100K	PD	
GPIO_8	100K	PD	
POC_GPIO_0	10K	PU	VCC3V3_TBT_SX
POC_GPIO_1	10K	PU	VCC3V3_TBT_SX
POC_GPIO_2	100K	PD	
POC_GPIO_3	100K	PD	
POC_GPIO_4	10K	PU	VCC3V3_TBT_SX
POC_GPIO_5	10K	PU	VCC3V3_TBT_SX
POC_GPIO_6	100K	PD	

Title	Alpine Ridge(TBT)
Size	Document Number: MS-1782
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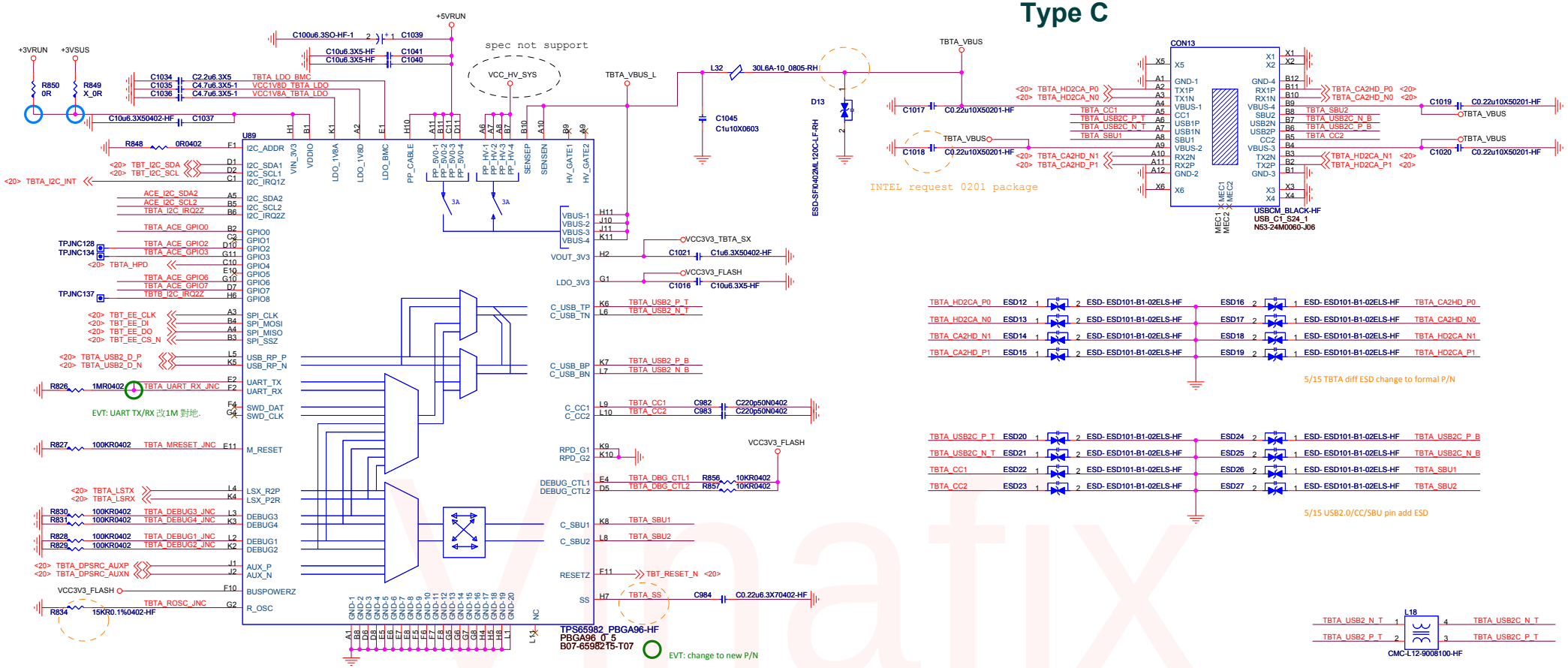
MICRO-STAR INT'L CO.,LTD.

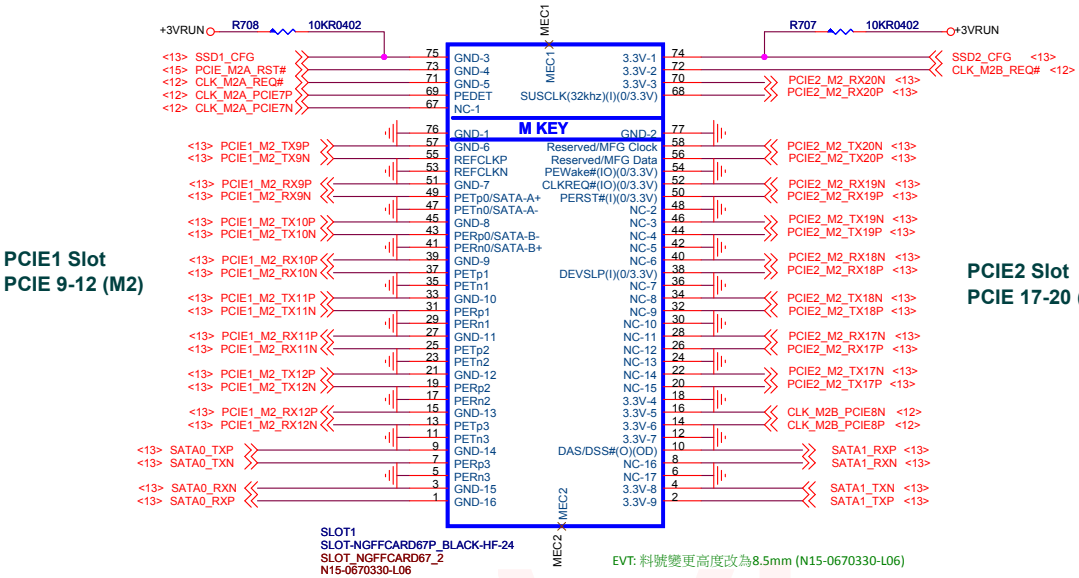
Type C

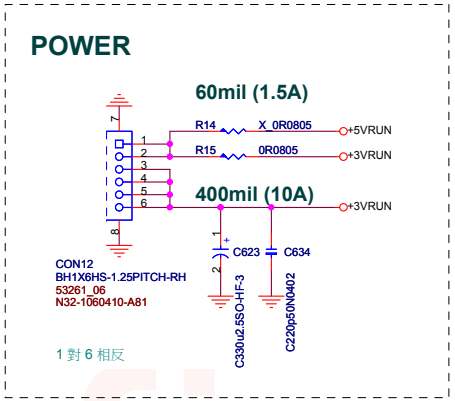


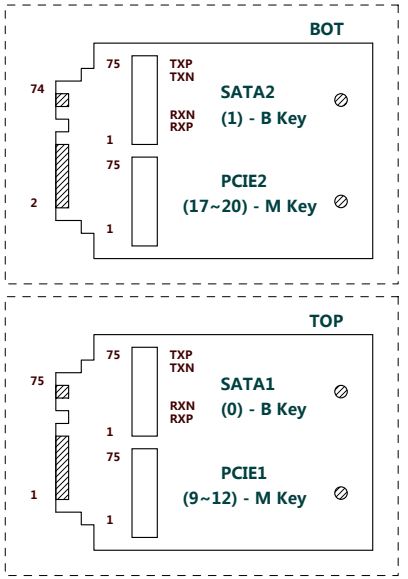
Wistron

Title	<Title>	
Size: Custom	Document Number: MS-1782	Rev: 2.0
Date: Tuesday, July 07, 2015	Sheet 21 of 58	

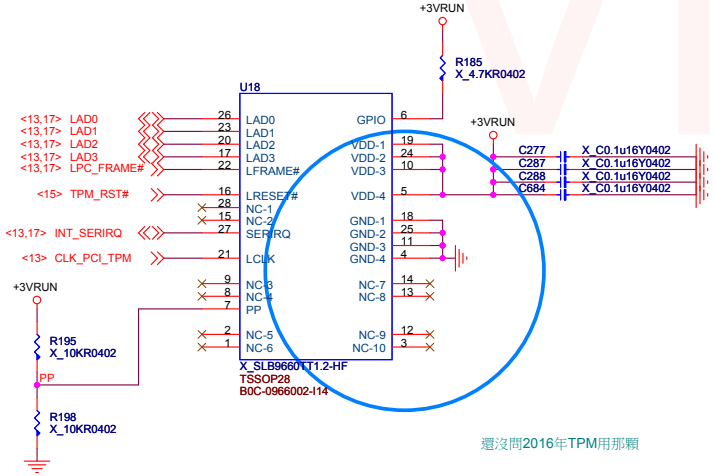
M.2/PCIE/SATA BTB



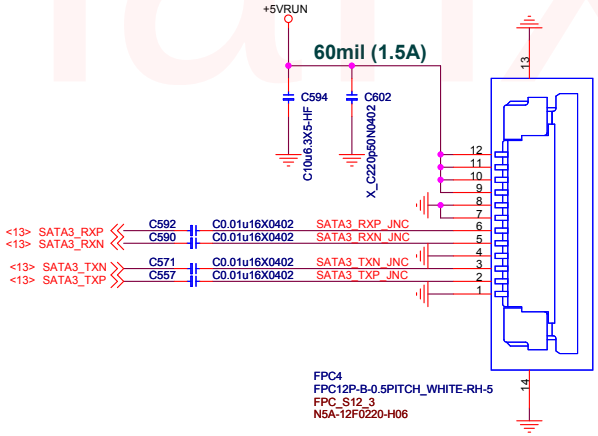


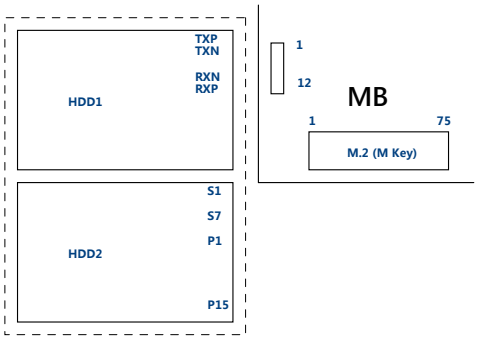


TPM



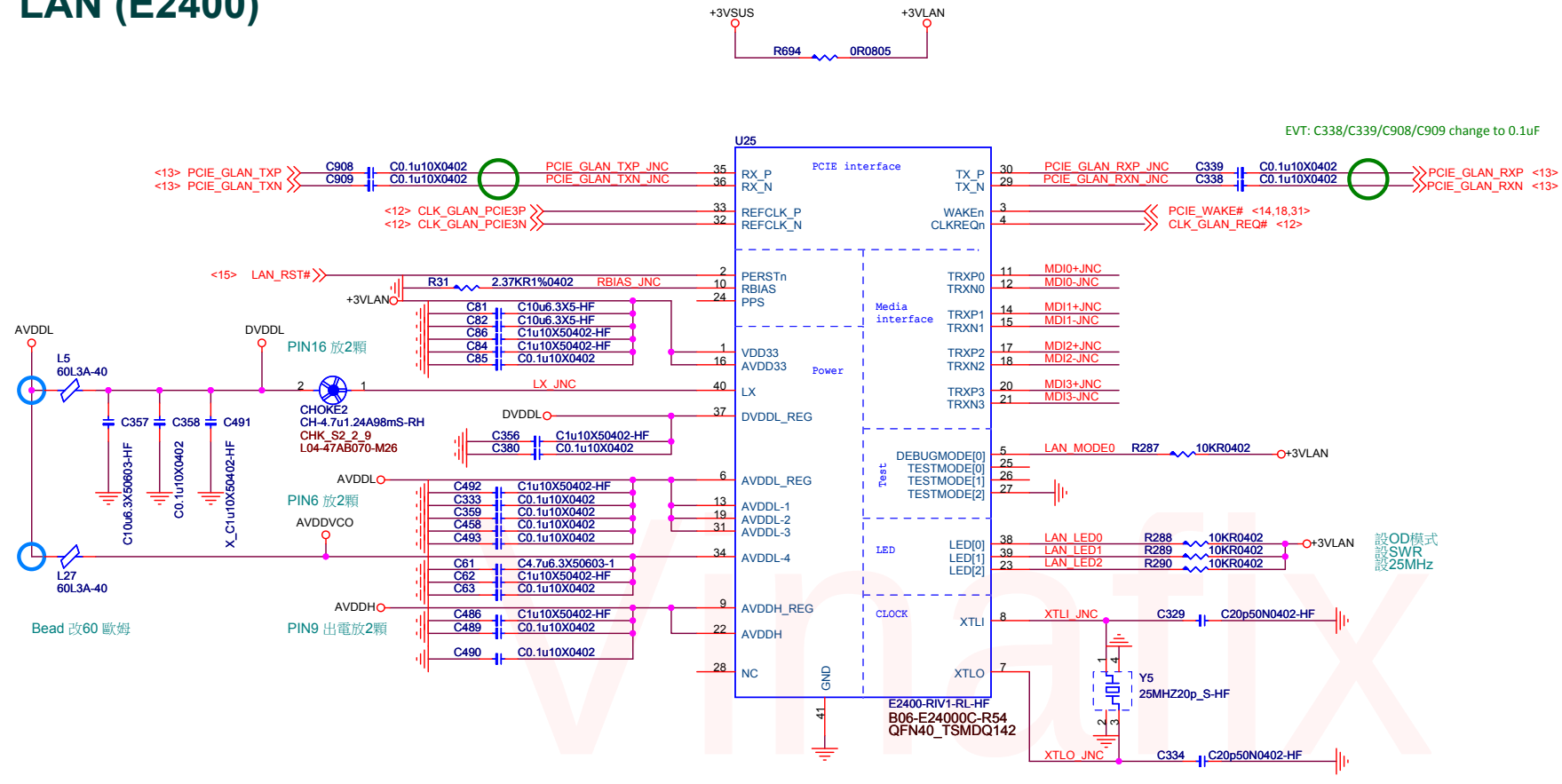
HDD2



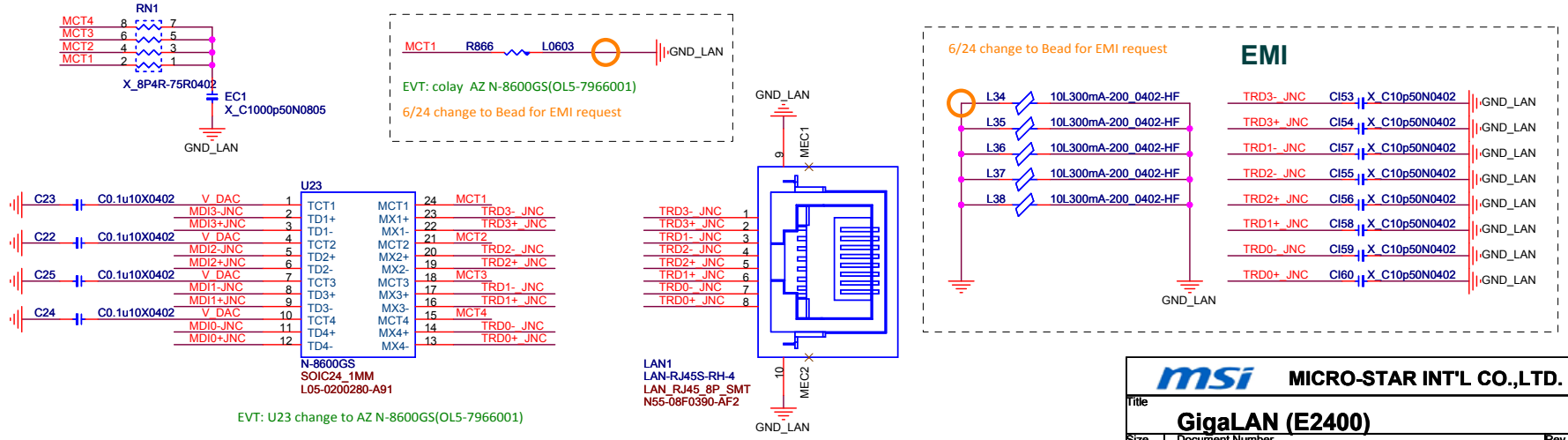


MICRO-STAR INT'L CO.,LTD.		
Title: TPM/HDD2/HDD Conn.		
Size: Custom	Document Number: MS-1782	Rev: 2.0
Date: Tuesday, July 07, 2015	Sheet 22 of 58	

LAN (E2400)



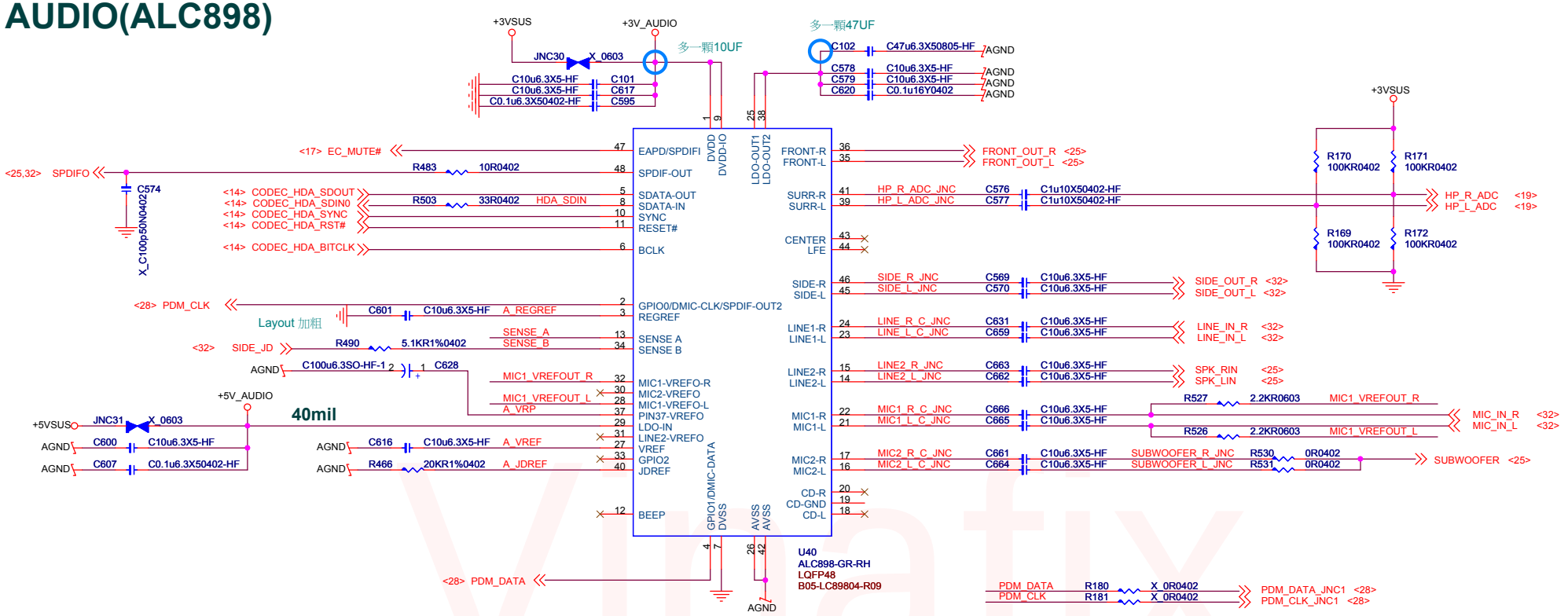
EVT: change U25 to E2400 正式料號

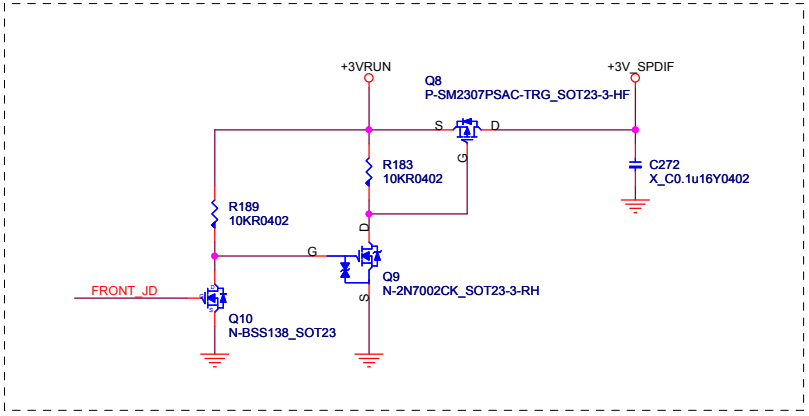


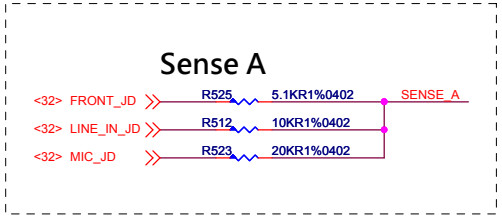
EVT: U23 change to AZ N-8600GS(OL5-7966001)

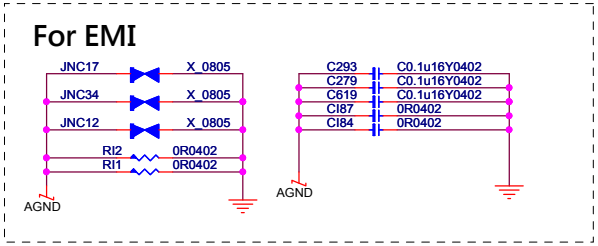
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	GigaLAN (E2400)	
Size: Custom	Document Number: MS-1782	Rev: 2.0
Date: Tuesday, July 07, 2015	Sheet 23 of 58	

AUDIO(ALC898)

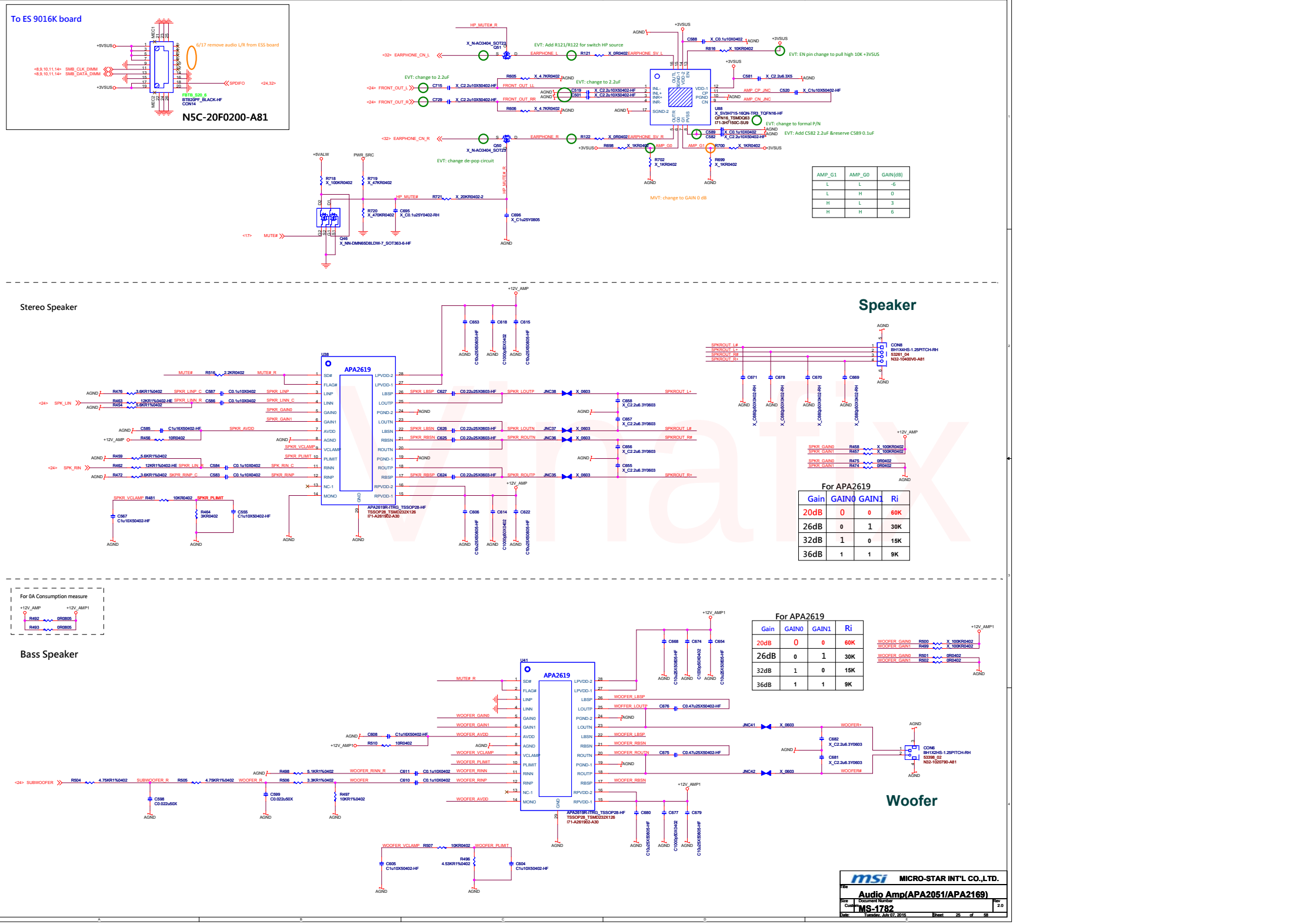




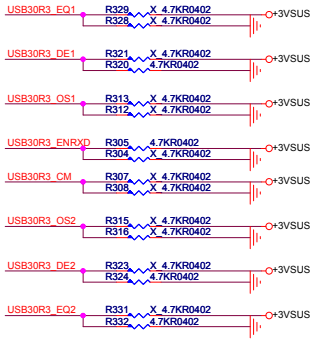




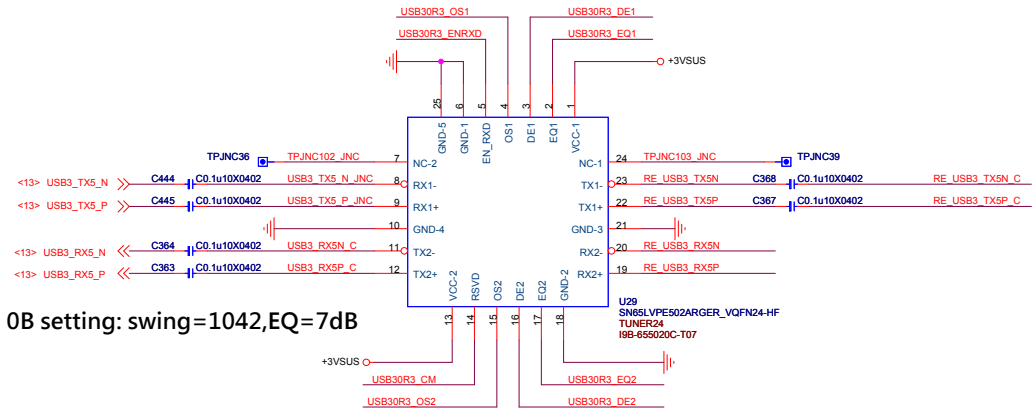
MICRO-STAR INT'L CO.,LTD.			
Title: Audio(ALC898)			
Size: Custom	Document Number: MS-1782		Rev: 2.0
Date: Tuesday, July 07, 2015		Sheet 24 of 58	


To ES 9016K board
6/17 remove audio L/R from ESS board
N5C-20F0200-A81
Stereo Speaker
Speaker
Bass Speaker
Woofer
For 0A Consumption measure
For APA2619
Gain GAIN0 GAIN1 Ri
20dB 0 0 60K
26dB 0 1 30K
32dB 1 0 15K
36dB 1 1 9K
AMP_G1 AMP_G0 GAIN(dB)
L L -6
L H 0
H L 3
H H 6
MICRO-STAR INT'L CO.,LTD.
Audio Amp(APA2051/APA2169)
MS-1782
Tuesday, July 07, 2015

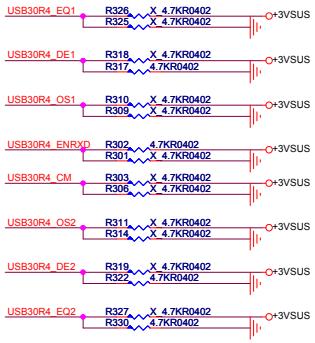
Daughter Board USB



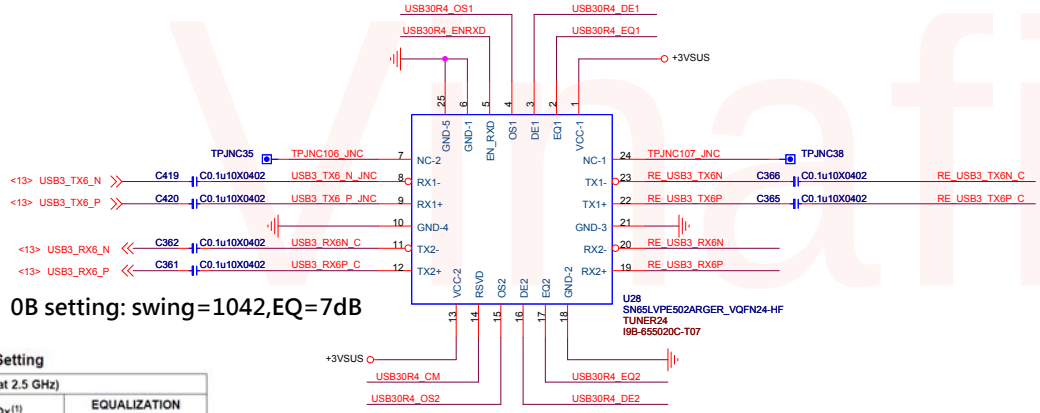
USB3.0 Port 5 Redriver



0B setting: swing=1042,EQ=7dB



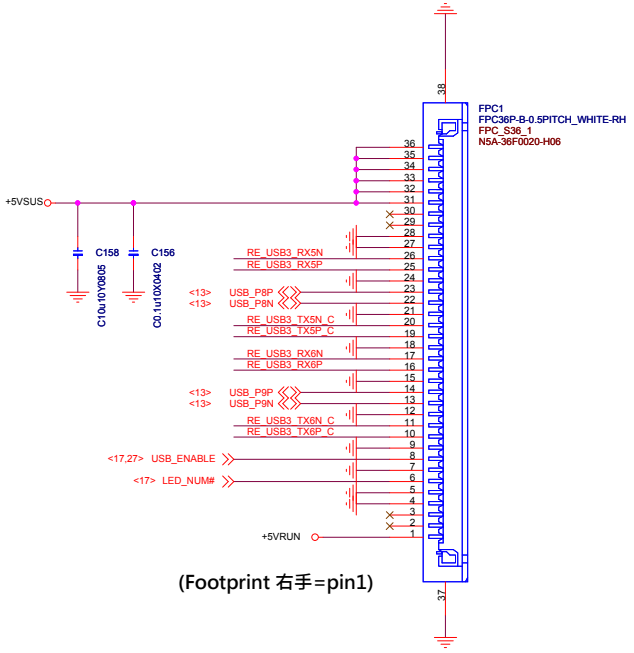
USB3.0 Port 6 Redriver



0B setting: swing=1042,EQ=7dB

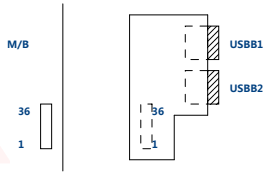
Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx(1)	TRANSISTION BIT AMPLITUDE (TYP mVpp)	EQx(1)	EQUALIZATION (dB)
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DEx(1)	OSx(1) = NC	OSx(1) = 0	OSx(1) = 1
NC (default)	0 dB	0 dB	0 dB
0	–3.5 dB	–2.2 dB	–4.4 dB
1	–6.0 dB	–5.2 dB	–6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION		
1 (default)	Normal Operation		
0	Sleep Mode		



(Footprint 右手=pin1)

Connec to USB board (sheet 38)



Vinafix

MICRO-STAR INT'L CO.,LTD.

Title: USB3.0/Redriver

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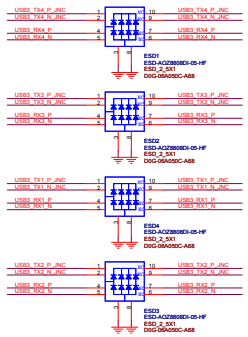
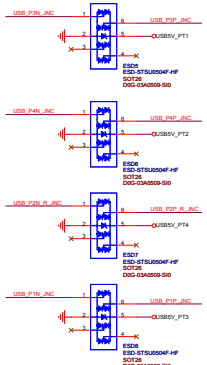
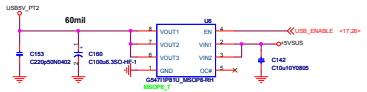
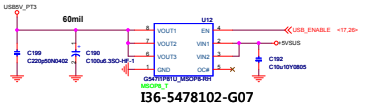
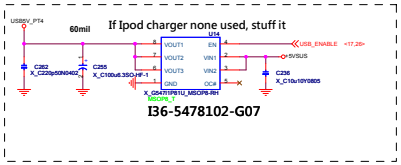


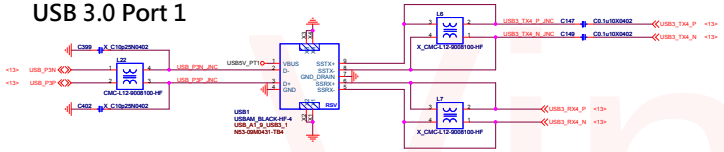




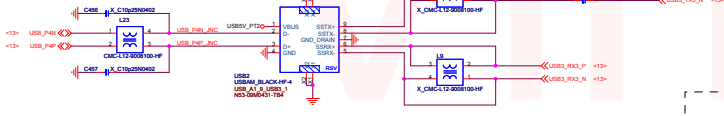




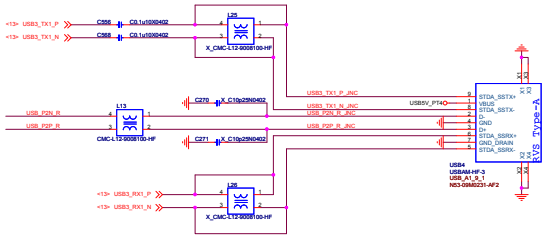
USB 3.0 Port 1

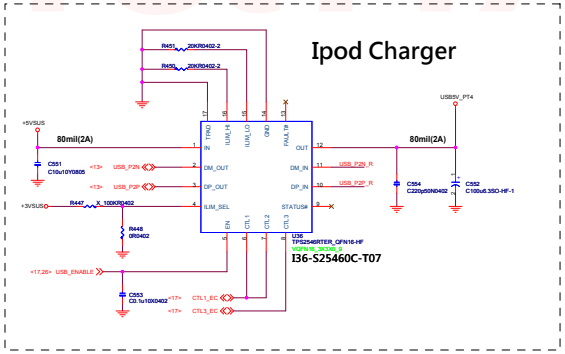


USB 3.0 Port 2

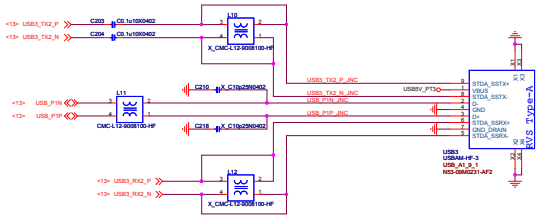


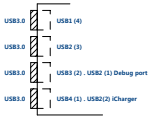
USB 3.0 Port 4(Ipod Charger)





USB 3.0 Port 3(Debug port)





MICRO-STAR INT'L CO.,LTD.		
Title	USB3.0/USB3.1 Conn/iCharger	
Size	Document Number MS-1782	Rev 2.0
Date: Tuesday, July 07, 2015	Sheet 27 of 58	

MXM_PWRSR_EN#	Low	High
Output Select	MXM(Default)	IGPU

Port switching control configuration; Internal pull down at ~150Kohm, 3.3V I/O.
L: Input port1 is selected (default)
H: Input port2 is selected

Programmable inout equalization levels; Internal pull down at 150K ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 11.5 dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

Auto test enable! Internal pull down at ~150Kohm, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

Automatic EQ disable!; Internal pull down 150Kohm, 3.3V I/O.
L: Automatic EQ enable (default)
H: Automatic EQ disable

AUX interception diable for prot y (y=1,2). Internal pull down ~150Kohm, 3.3V I/O;
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception diable, driver output with fixed 800mv and 0dB
M: AUX interception diable, driver output with fixed 400mv and 0dB

Outout swing adjustment for port y(y=1,2). Internal pull down ~150Kohm, 3.3V I/O;
L:default
H:+20%
M:-16.7%

PS8331B
PS8331BQFN60GTR-A1-HF
QFN60_T118X278
B0B-8331B0C-P97

PD pin signal reversal

eDP Panel Signal 2in 1out switch
Default set S1 output

Inputs		INPUT/OUTPUT D	FUNCTION
EN#	MXM_PWRSR_EN#		
L	L	S1	D PORT=S1 PORT
L	H	S2	D PORT= S2 PORT
H	X	Z	DISCONNECT

FPC3
FPC40P-B-0.5PITCH_WHITE-HF-1
FPC_540_5
N5A-40F0130-A81

TS5V330DBQR_SSOP16-RH
QSOP16
I98-5V33002-T07

Camera_ON:
High= On
Low=Off

For 0A consumption measure

For Vendor suggestion camera modify to 5V

reserve for Nvidia G-sync

EMI

CON2
X_BH1X10HS-1.25PITCH-RH
FPC_CONN_12P
N32-1100230-A81

For 4K*2K panel used MVTmodify no stuff

Panel Logic power

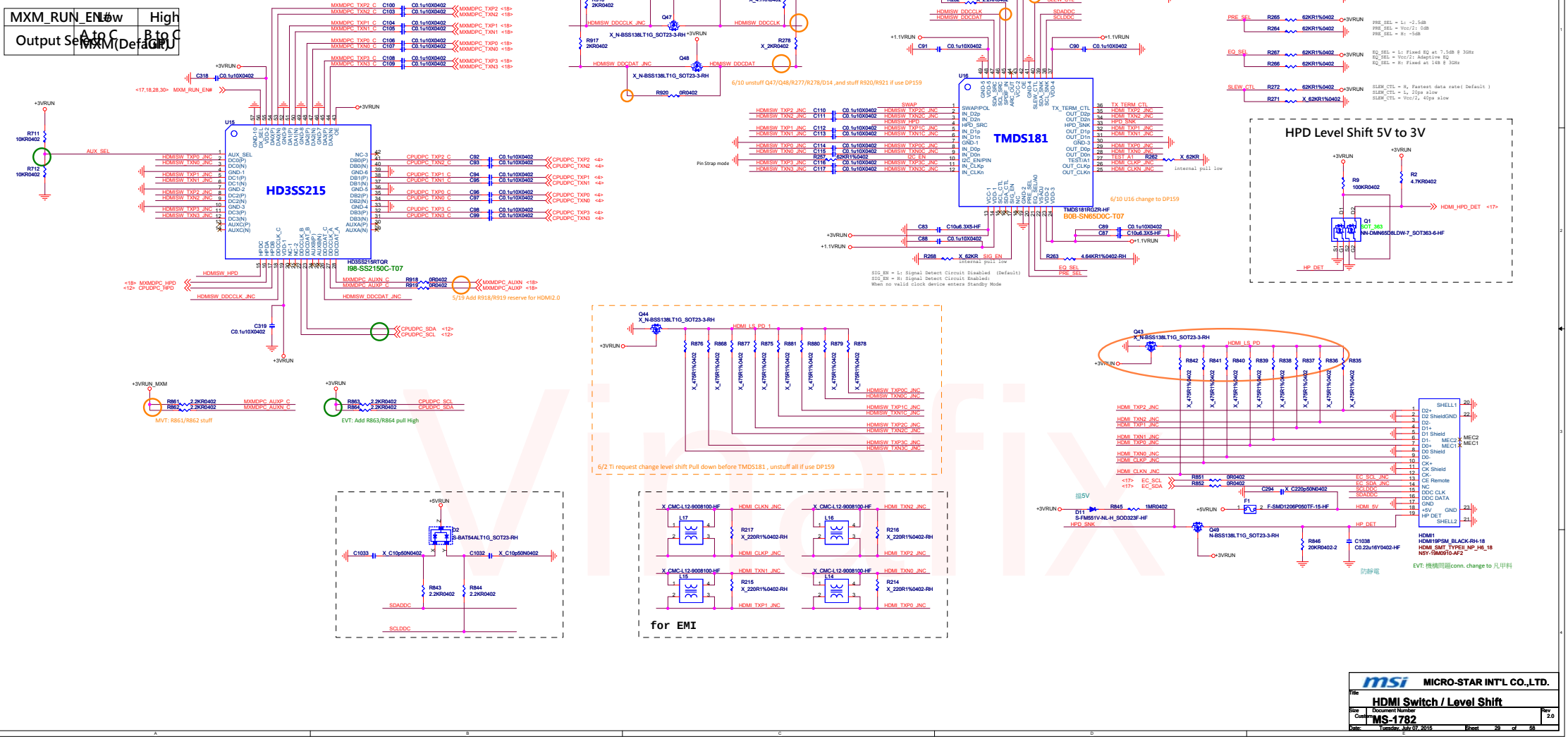
APL3512ABI-TRG_SOT23-5-HF
SOT23_5_NPC30X
I36-3512A09-A30

MICRO-STAR INT'L CO.,LTD.

Title: eDP switch & Conn/CAM/Lid
Size: Custom | Document Number: MS-1782 | Rev: 2.0
Date: Tuesday, July 07, 2015 | Sheet 28 of 58

HDMI SWITCH

MXM_RUN_EN#	Low	High
Output Select	A to C	B to C
	MXM(Default)	GPU



DP 2in 1 out Switch

MXM_PWRSR_EN#	Low	High
Output Select	MXM(Default)	IGPU

Programmable inout equalization levels; Internal pull down at 150K ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 11.5 dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

Auto test enablel Internal pull down at ~150Kohm, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

Automatic EQ disablel; Internal pull down 150Kohm, 3.3V I/O.
L: Automatic EQ enable (default)
H: Automatic EQ disable

AUX interception diable for prot y (y=1,2). Internal pull down ~150Kohm, 3.3V I/O;
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception diable, driver output with fixed 800mv and 0dB
M: AUX interception diable, driver output with fixed 400mv and 0dB

Outout swing adjustment for port y(y=1,2). Internal pull down ~150Kohm, 3.3V I/O;
L:default
H:+20%
M:-16.7%

Port switching control configuration; Internal pull down at ~150Kohm, 3.3V I/O.
L: Input port1 is selected (default)
H: Input port2 is selected

MVT Modify Common choke PN

For Dual Mode switch to DDC

Avoid DP connector Leakage to IC

TBT-SINK1

MXM_RUN_EN#	Low	High
Output Select	MXM(Default)	IGPU

Programmable inout equalization levels; Internal pull down at 150K ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 11.5 dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

Auto test enablel Internal pull down at ~150Kohm, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

Automatic EQ disablel; Internal pull down 150Kohm, 3.3V I/O.
L: Automatic EQ enable (default)
H: Automatic EQ disable

AUX interception diable for prot y (y=1,2). Internal pull down ~150Kohm, 3.3V I/O;
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception diable, driver output with fixed 800mv and 0dB
M: AUX interception diable, driver output with fixed 400mv and 0dB

Outout swing adjustment for port y(y=1,2). Internal pull down ~150Kohm, 3.3V I/O;
L:default
H:+20%
M:-16.7%

MICRO-STAR INT'L CO.,LTD.		
Title: DP Switch		
Size: Custom	Document Number: MS-1782	Rev: 2.0
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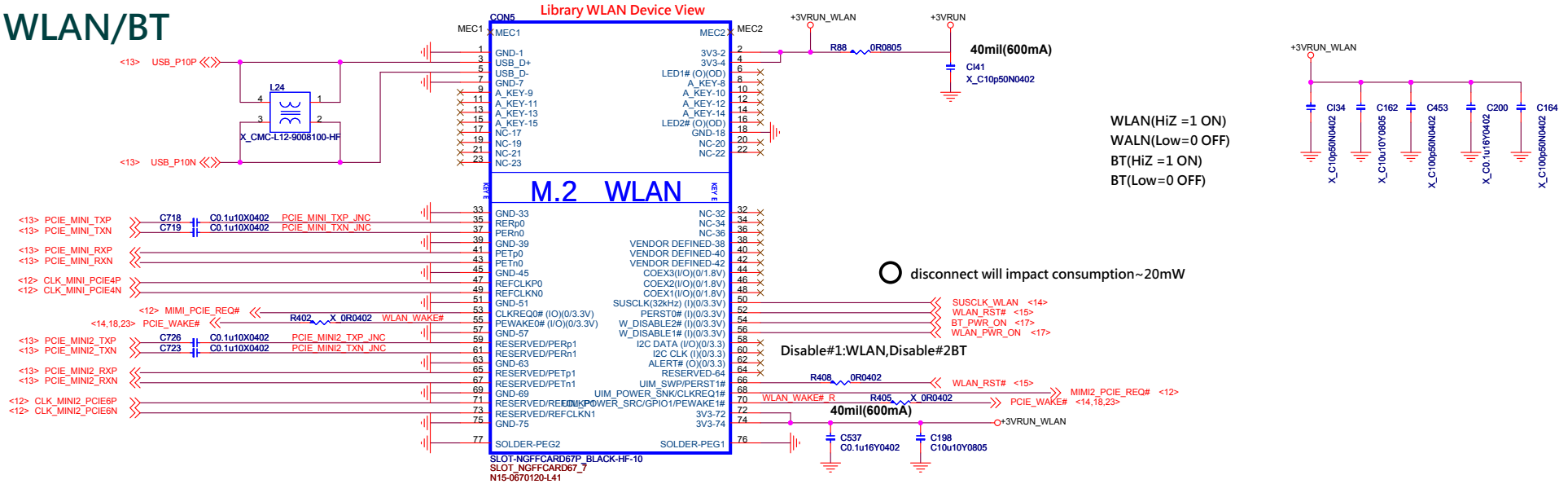
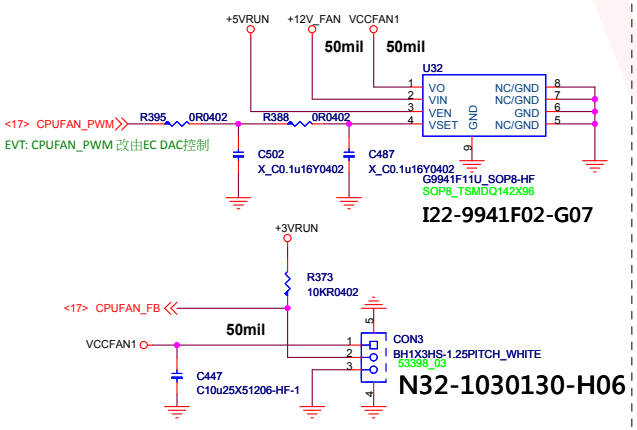
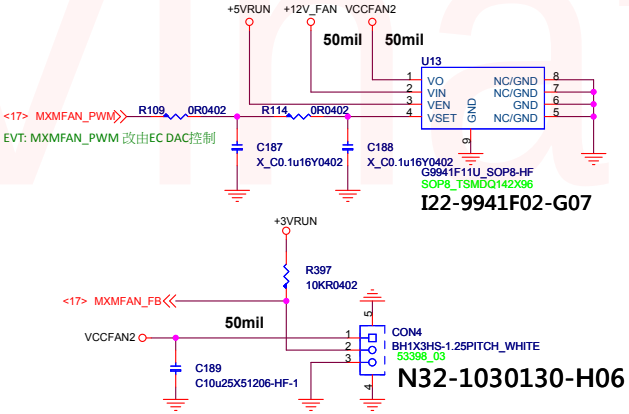
M.2 WLAN/BT



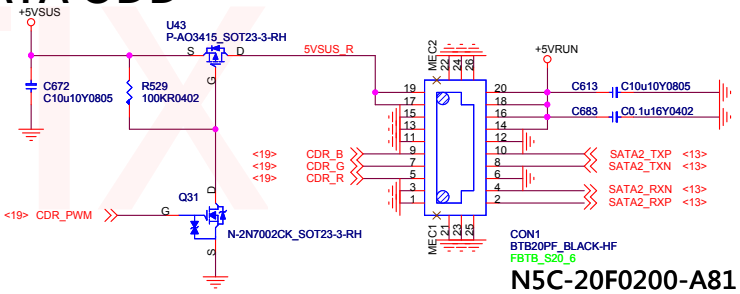
CPU FAN



MXM FAN



SATA ODD



Library用自定義，不online更新(footprint與online相同)

MICRO-STAR INT'L CO.,LTD.		
Title: WLAN/FAN/ODD Conn		
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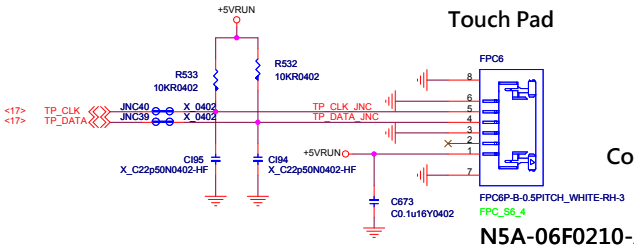
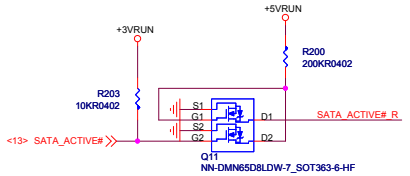
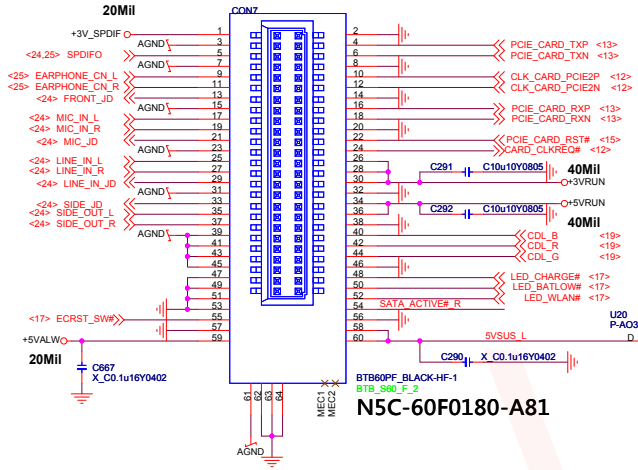
Touch Pad



Connect Touch Board (sheet 40)

N5A-06F0210-A81

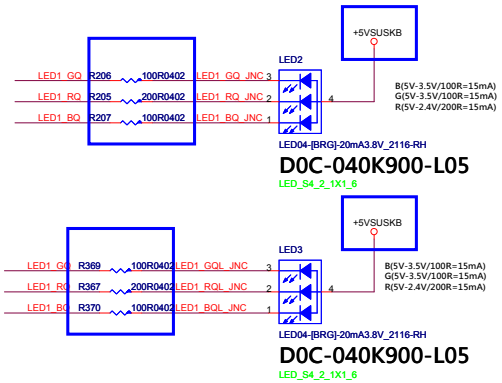




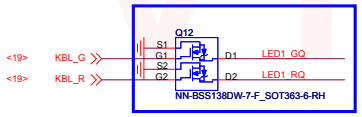
BTB to Audio Board

N5C-60F0180-A81

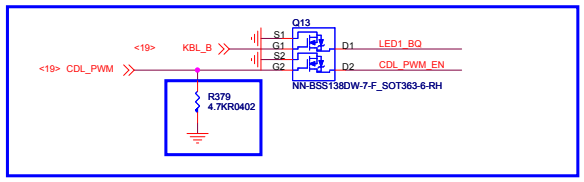
Connec to Audio board (sheet 40)

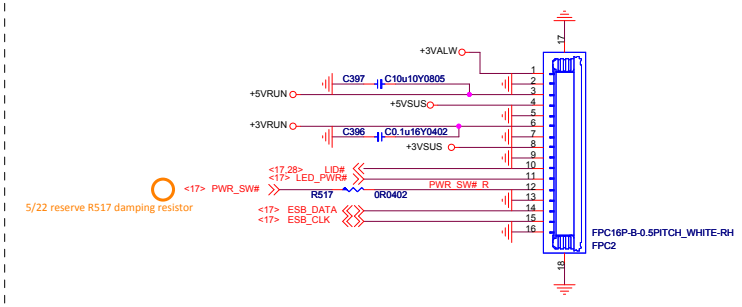


LED亮度電流15mA B=100R,G=100R,R=200R



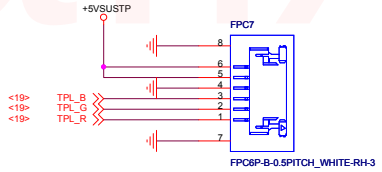
PN :D03-138DW19-D07



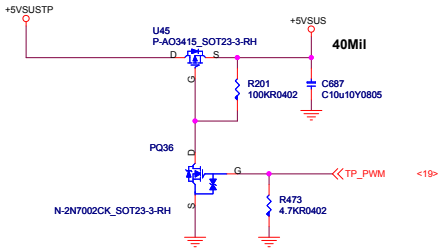


Connec to Switch board (sheet 42)

Connec to TP Light Bar Board(sheet 45)



N5A-06F0210-A81



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Title: Audio BTB/TP Conn		
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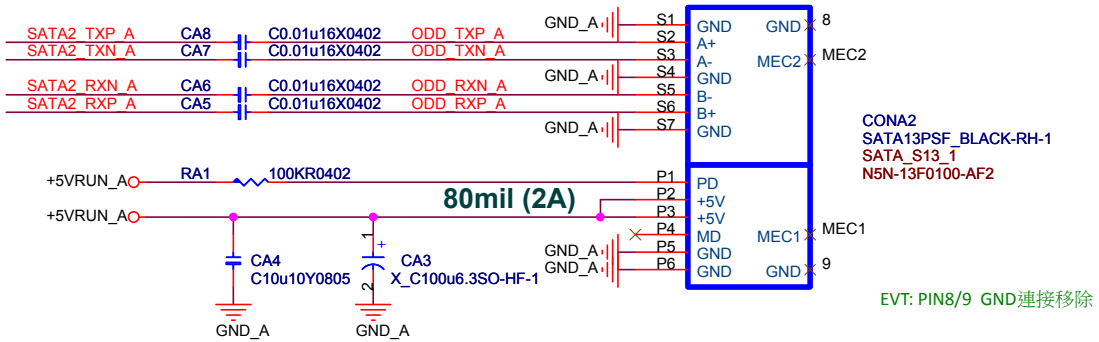
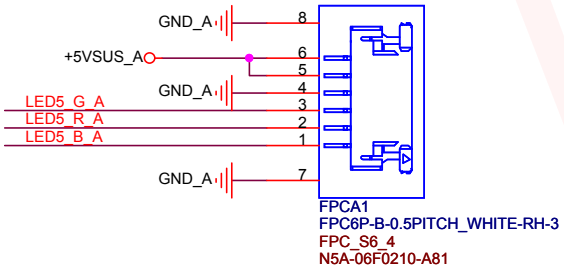
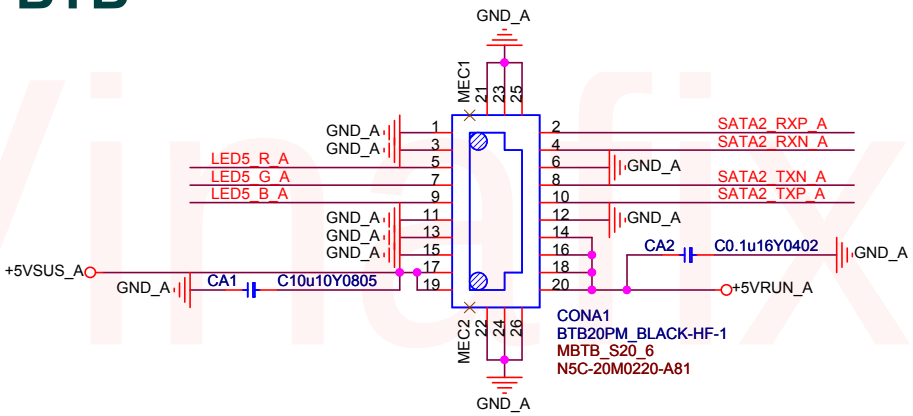
ODD



Right LED FPC



BTB



Connec to MB board (sheet 35)

Library用自定義，不online更新(footprint與online相同)

HA2 — GND_A — H_R276D118_PT — X_H_R276D118_PT

HA1 — GND_A — HOLES_R197D91_PT — X_HOLES_R197D91_PT

HA3 — NPTH_98 — X_NPTH_98

SCREWA1 — 60 — E43-1205003-H29

SCREWA2 — 60 — E43-1205003-H29

PCBA1 — P30-1782A20-H73

MICRO-STAR INT'L CO.,LTD.			
Title: [A]ODD Board			
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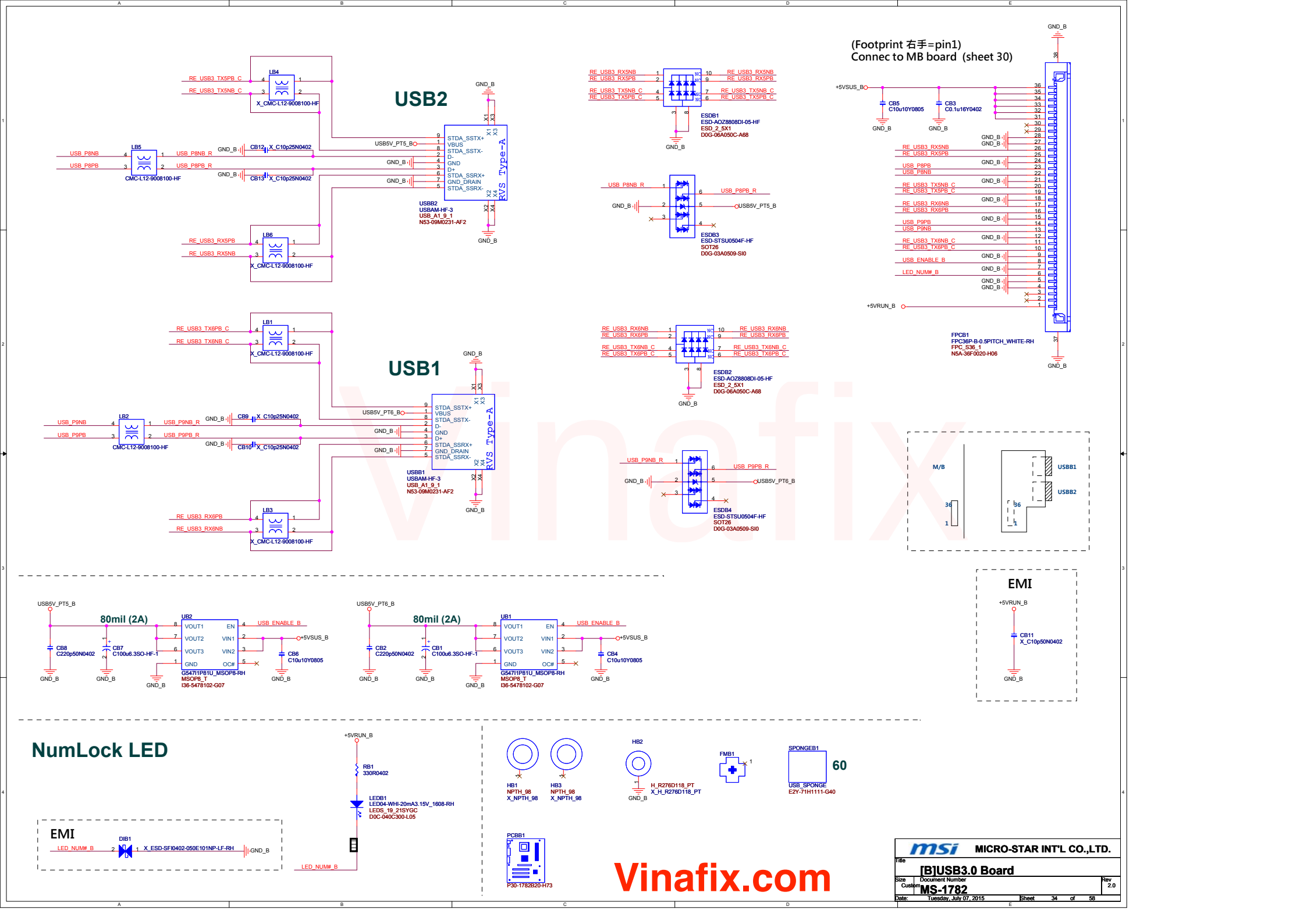
USB2
USB1
(Footprint 右手=pin1)
Connec to MB board (sheet 30)
LB4
LB5
LB6
LB1
LB2
LB3
CMC-L12-9008100-HF
X_CMC-L12-9008100-HF
USBB2
USBAM-HF-3
USB_A1_9_1
N53-09M0231-AF2
USBB1
ESDB1
ESD-AOZ8808DI-05-HF
ESD_2_5X1
D0G-06A050C-A68
ESDB2
ESDB3
ESD-STSU0504F-HF
SOT26
D0G-03A0509-SI0
ESDB4
FPCB1
FPC36P-B-0.5PITCH_WHITE-RH
FPC_S36_1
N5A-36F0020-H06
M/B
USBB1
USBB2
EMI
80mil (2A)
UB2
UB1
G54711P81U_MSOP8-RH
MSOP8_T
I36-5478102-G07
NumLock LED
LEDB1
LED04-WHI-20mA3.15V_1608-RH
LEDS_19_21SYGC
D0C-040C300-L05
DIB1
X_ESD-SFI0402-050E101NP-LF-RH
HB1
HB3
NPTH_98
X_NPTH_98
HB2
H_R276D118_PT
X_H_R276D118_PT
FMB1
SPONGEB1
USB_SPONGE
E2Y-71H1111-G40
60
PCBB1
P30-1782B20-H73
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[B]USB3.0 Board
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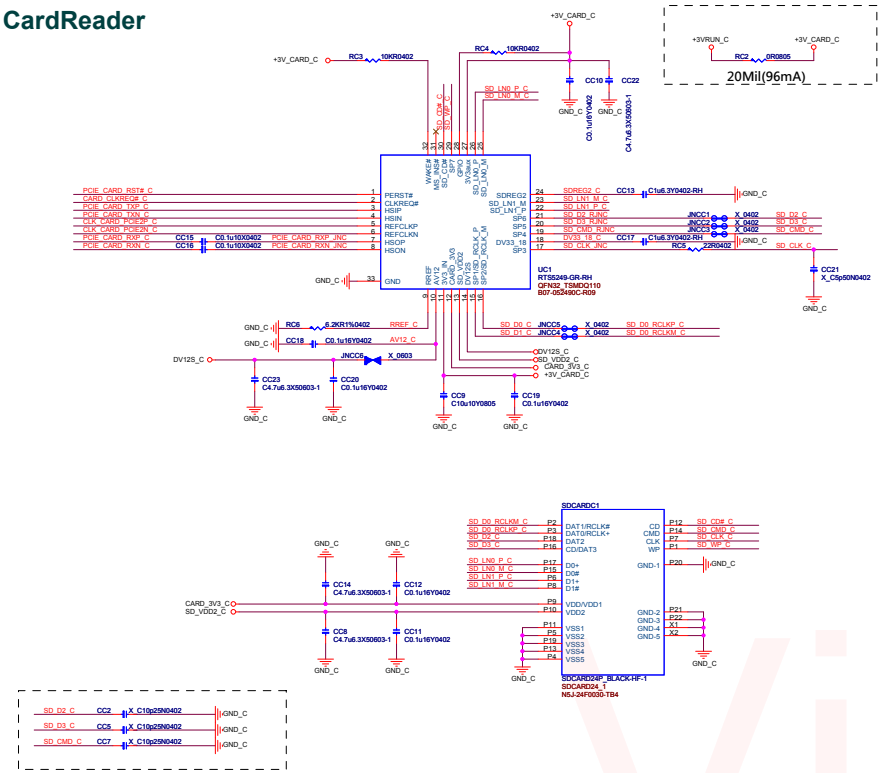
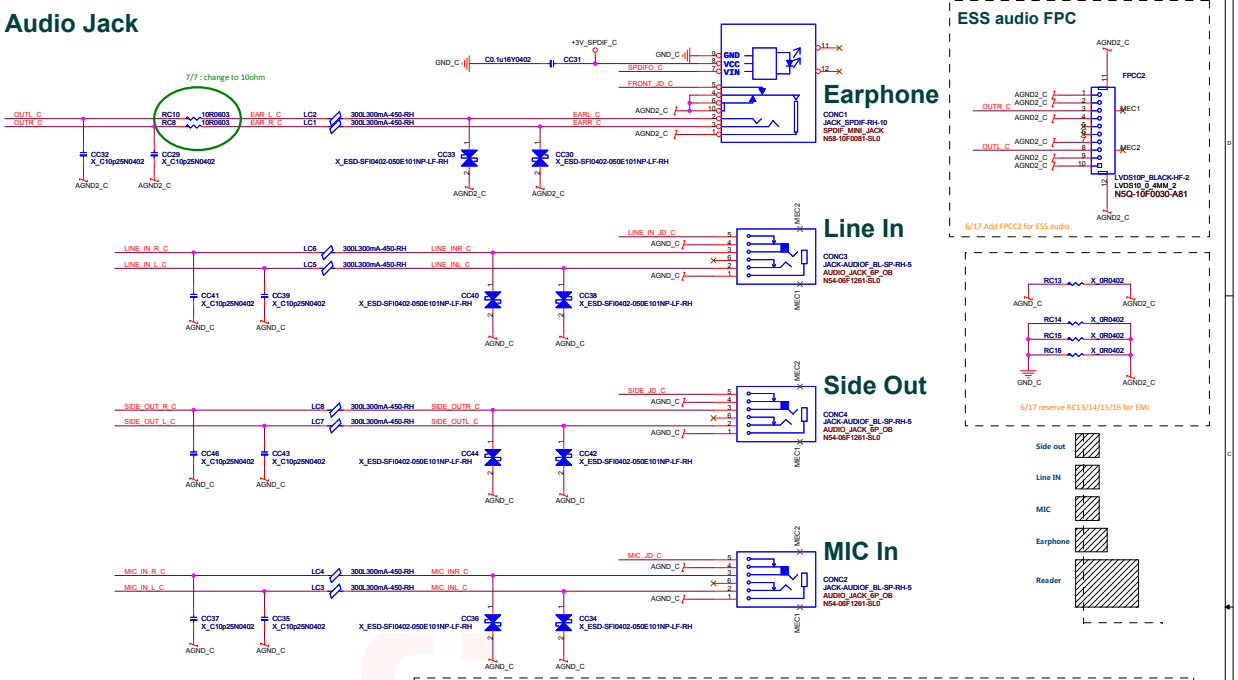
CardReader



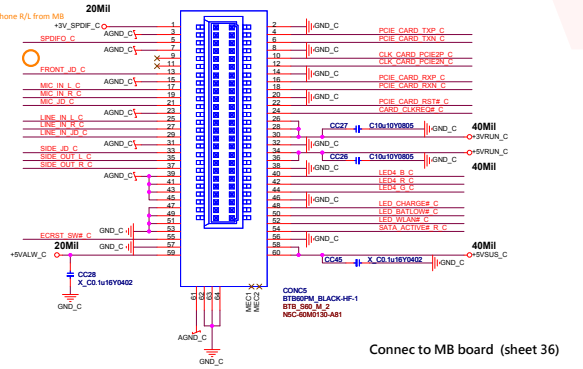
Audio Jack



ESS audio FPC

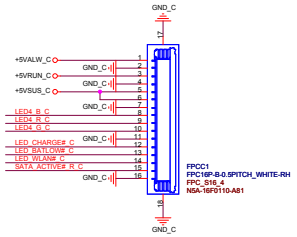
BTB

6/17 Ver2.0 remove headphone R/L from MB



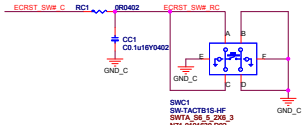
Connect to MB board (sheet 36)

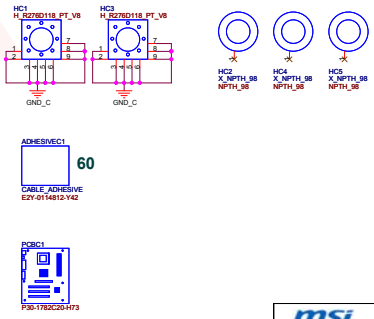
Left LED FPC



Connect to Light Left board (sheet 42)

Reset Key





msi	MICRO-STAR INT'L CO.,LTD.	
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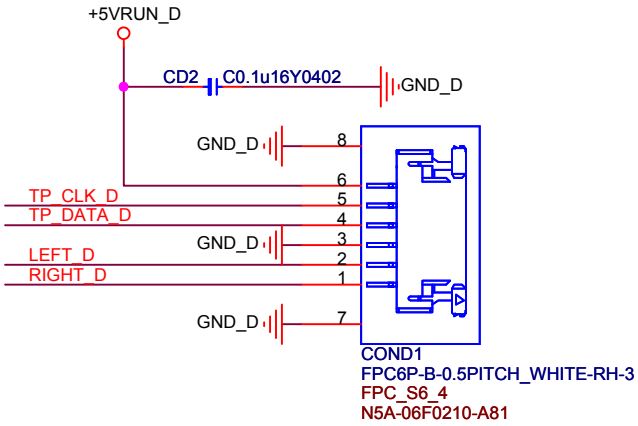
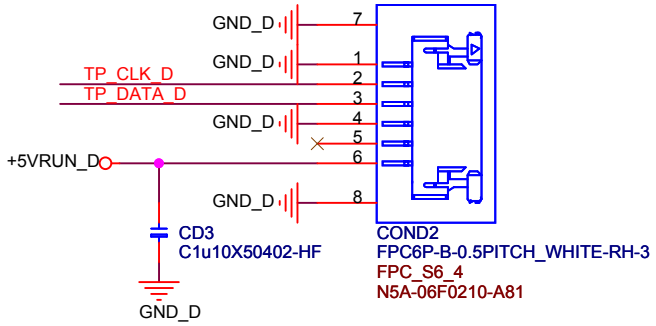
Vinafix

TP Pad FPC

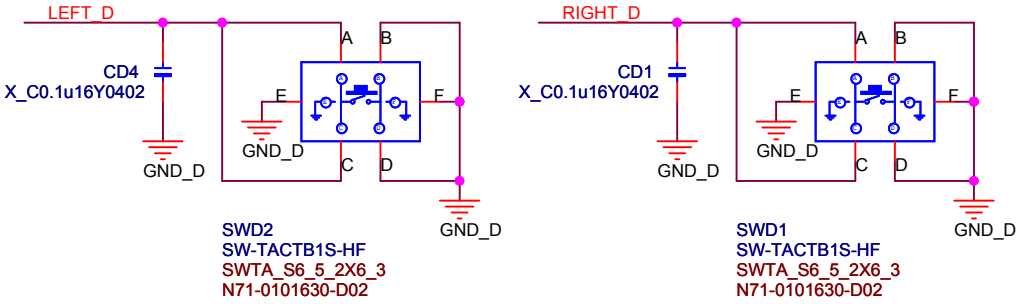


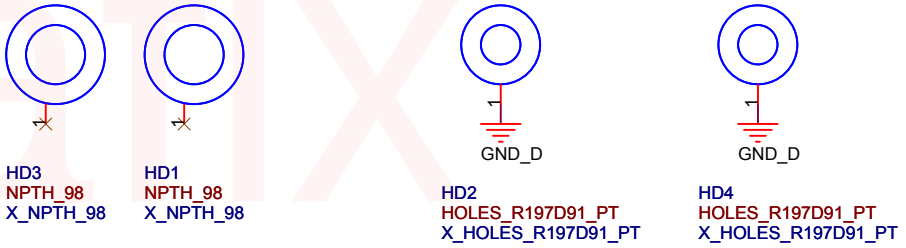
MB FPC

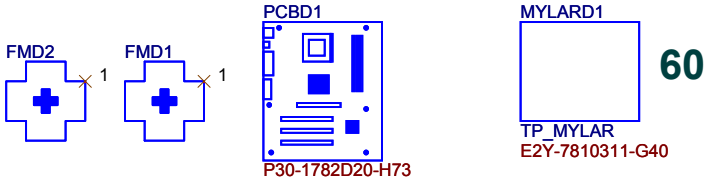


Connec to MB board (sheet 36)

TP L/R Key







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Title: [D]TP/LED BOARD

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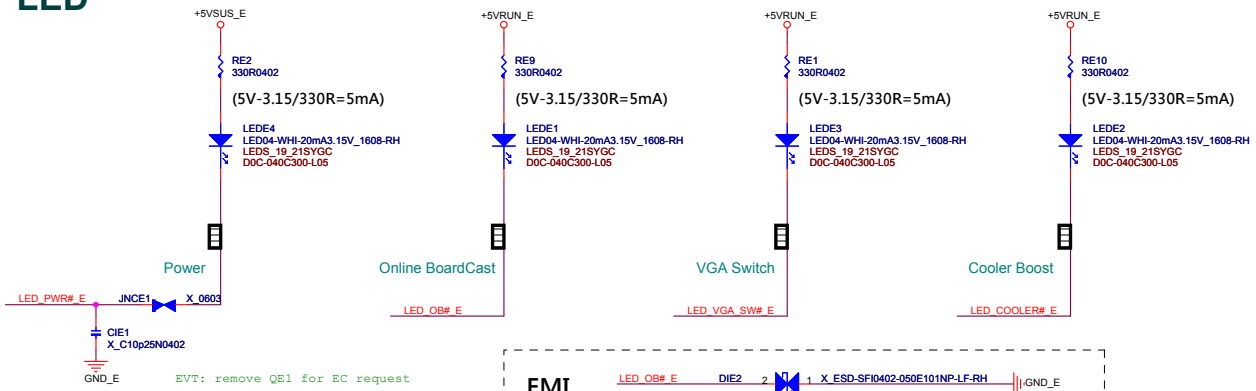
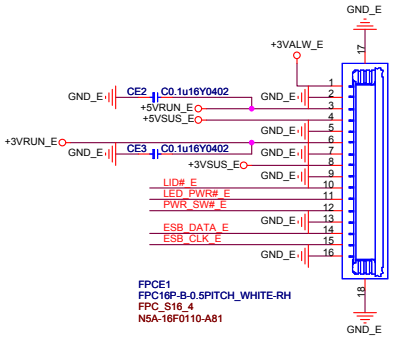
LED

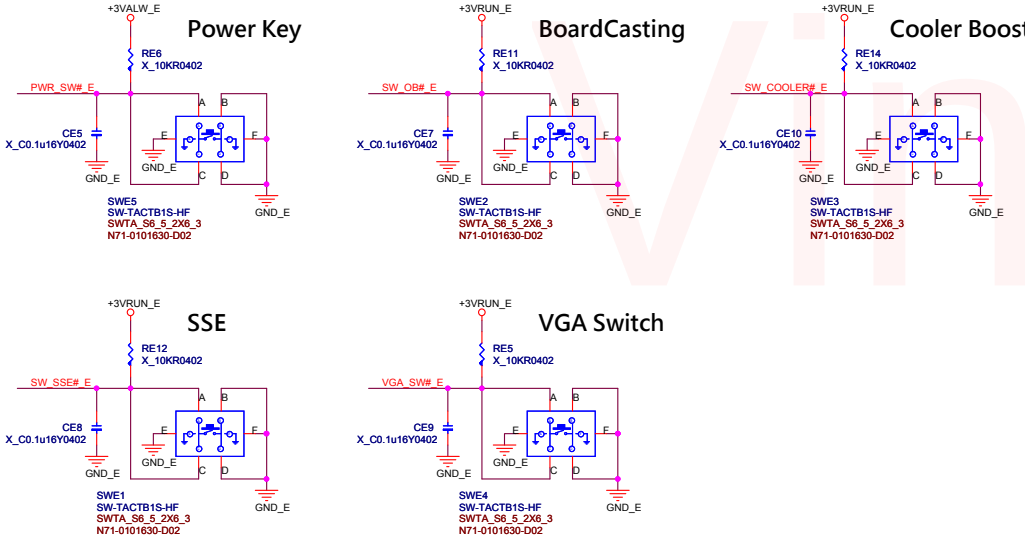


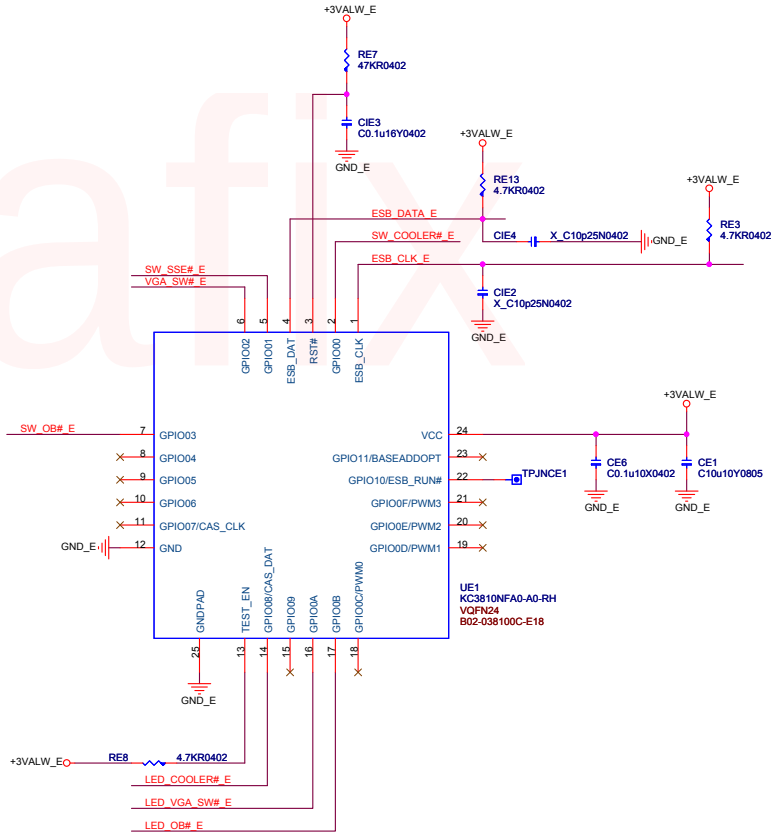
EMI



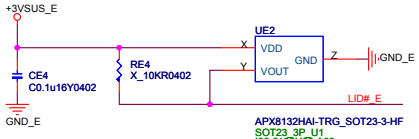
Connec to MB board (sheet 36)

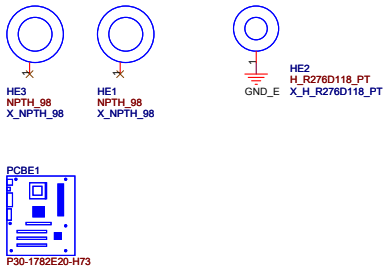
Function Key





Hall Sensor





Vinafix

msi MICRO-STAR INT'L CO.,LTD.		
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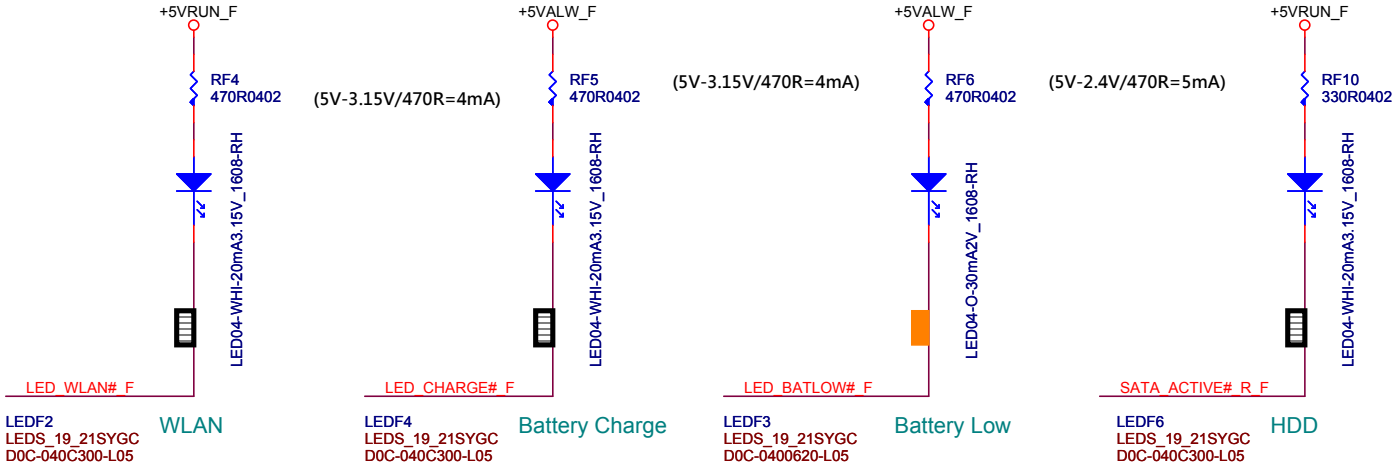
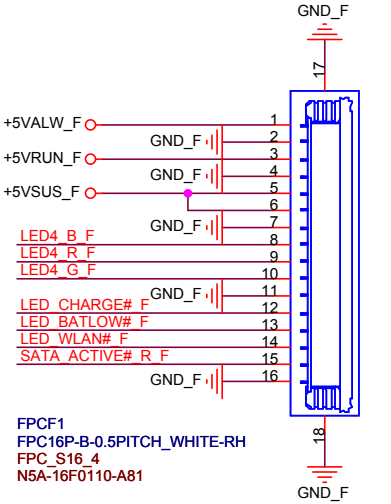
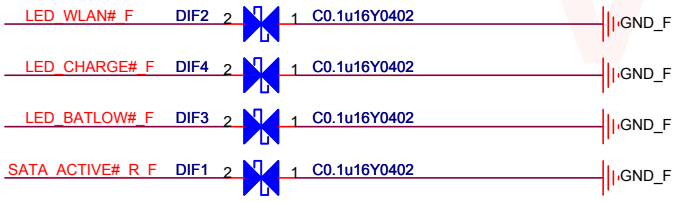
LED Board

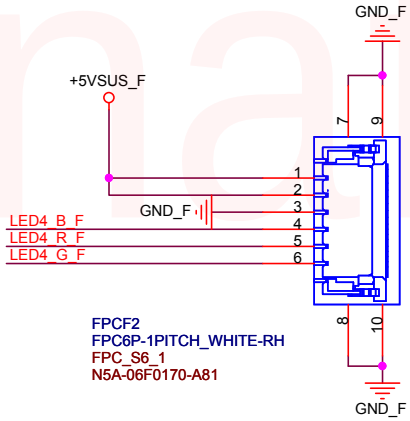




Connec to Audio board (sheet 40)

EMI





HF2
X_NPTH_98
NPTH_98

HF1
X_NPTH_98
NPTH_98

PCBF1
P30-1782F20-H73

MYLARF1
60
INDICATOR_MYLAR
E2P-7813112-G40

MICRO-STAR INT'L CO.,LTD.

Title: [F]LED Board

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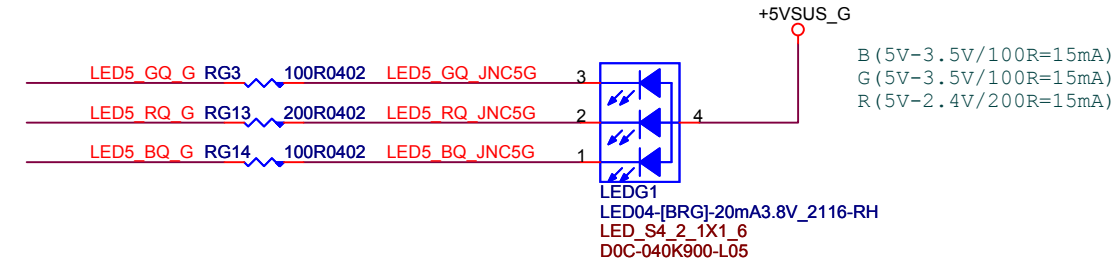
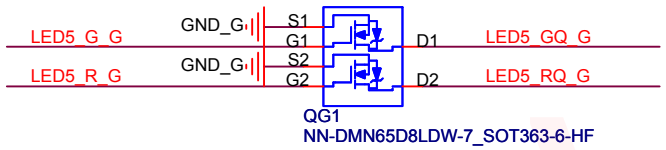
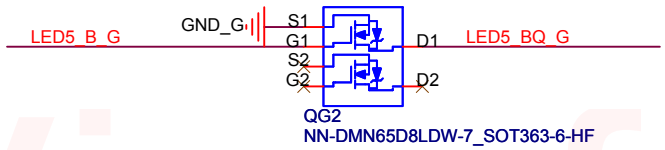
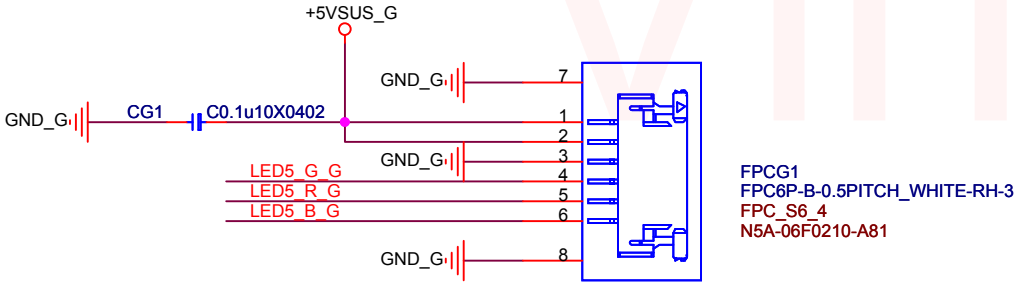
LED Light Bar (Right)

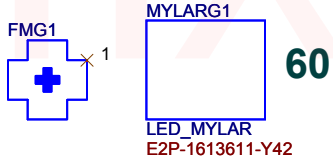


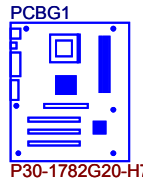
ESD protect



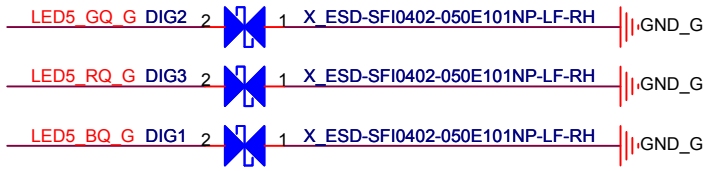








EMI



MICRO-STAR INT'L CO.,LTD.

Title	Light Bar Right	
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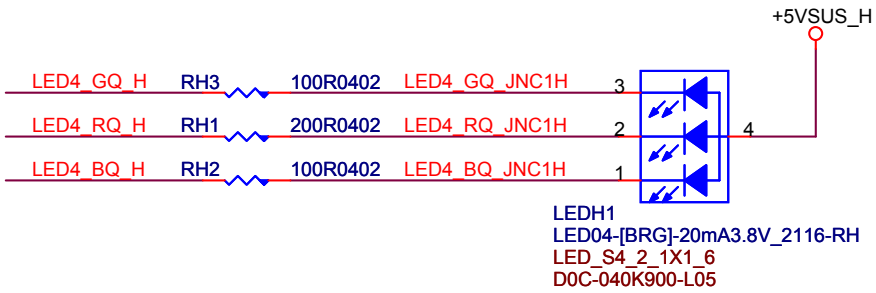
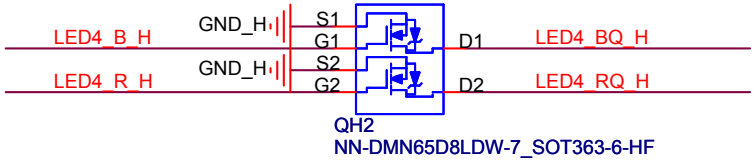
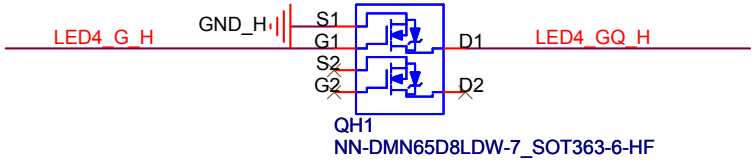
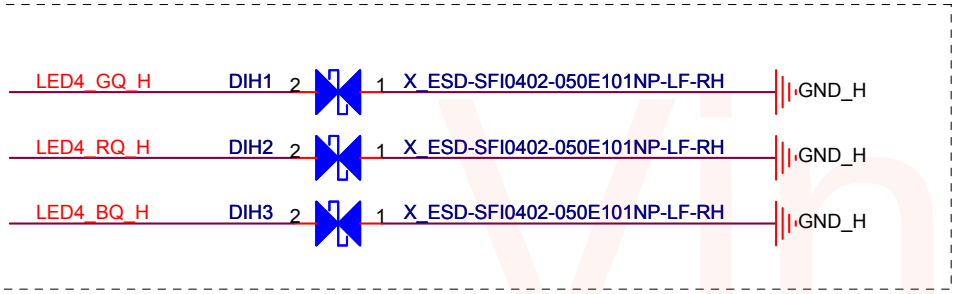
LED Light Bar (Left)

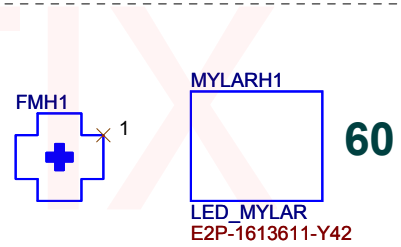


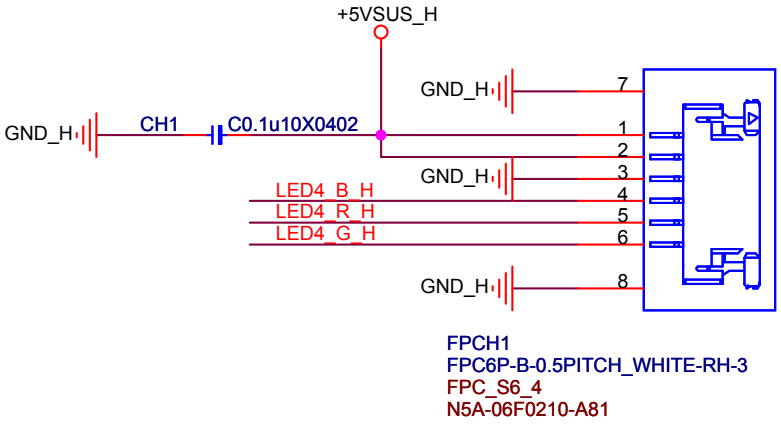




ESD protect







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Title: [H]Light Bar Left

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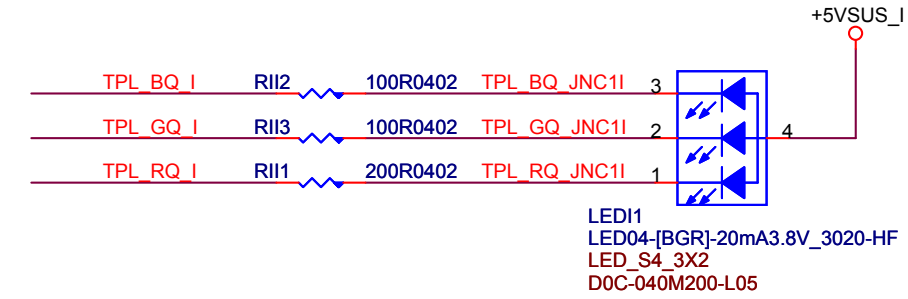
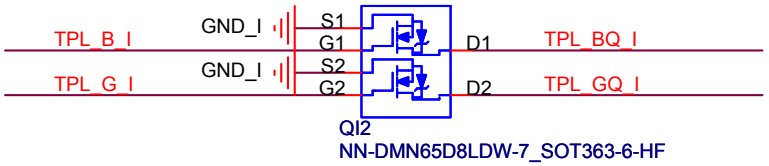
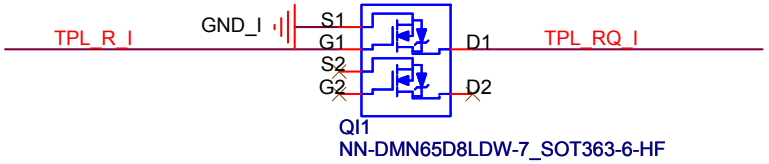
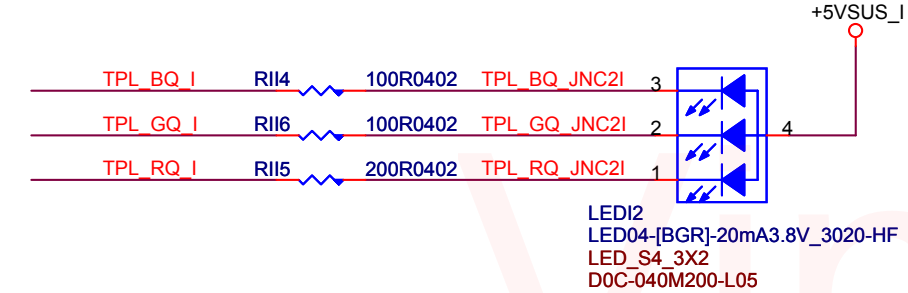
Touch Light Bar

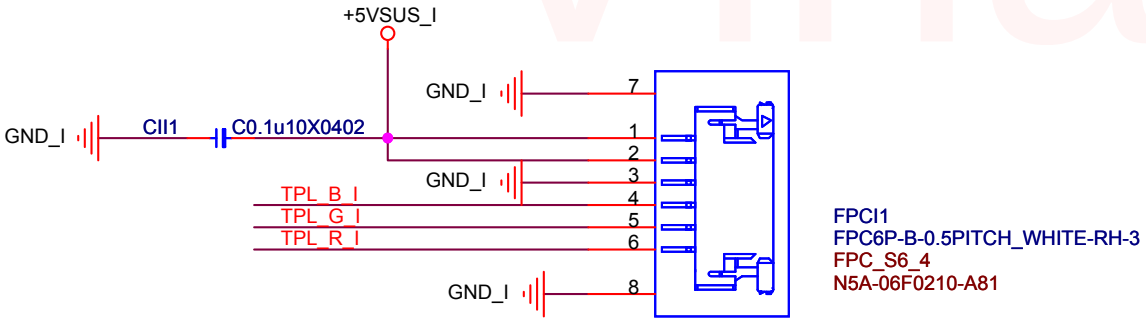


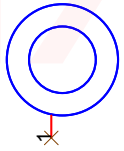


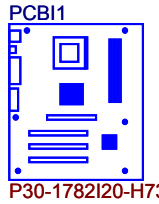




ESD protect







MICRO-STAR INT'L CO.,LTD.

Title: [I]Touch Light Bar

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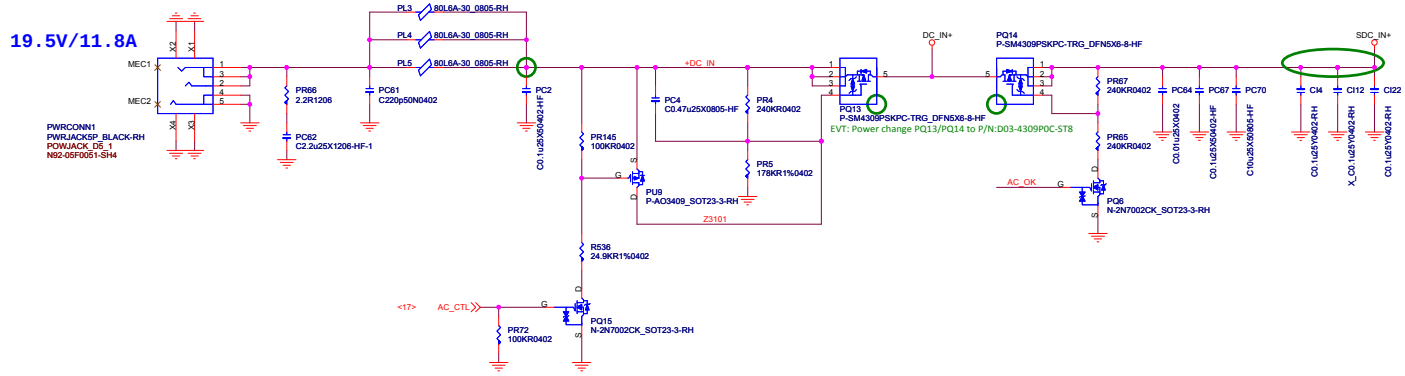
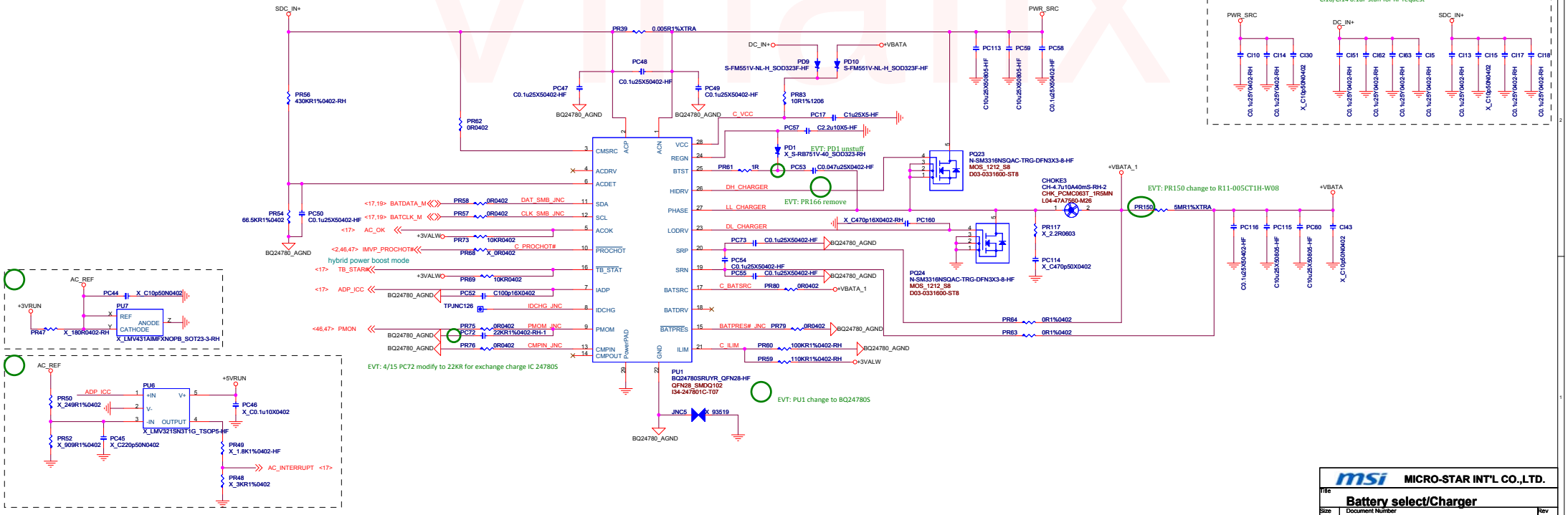


Battery Charger



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msi	MICRO-STAR INT'L CO.,LTD.		
Title	Battery select/Charger		
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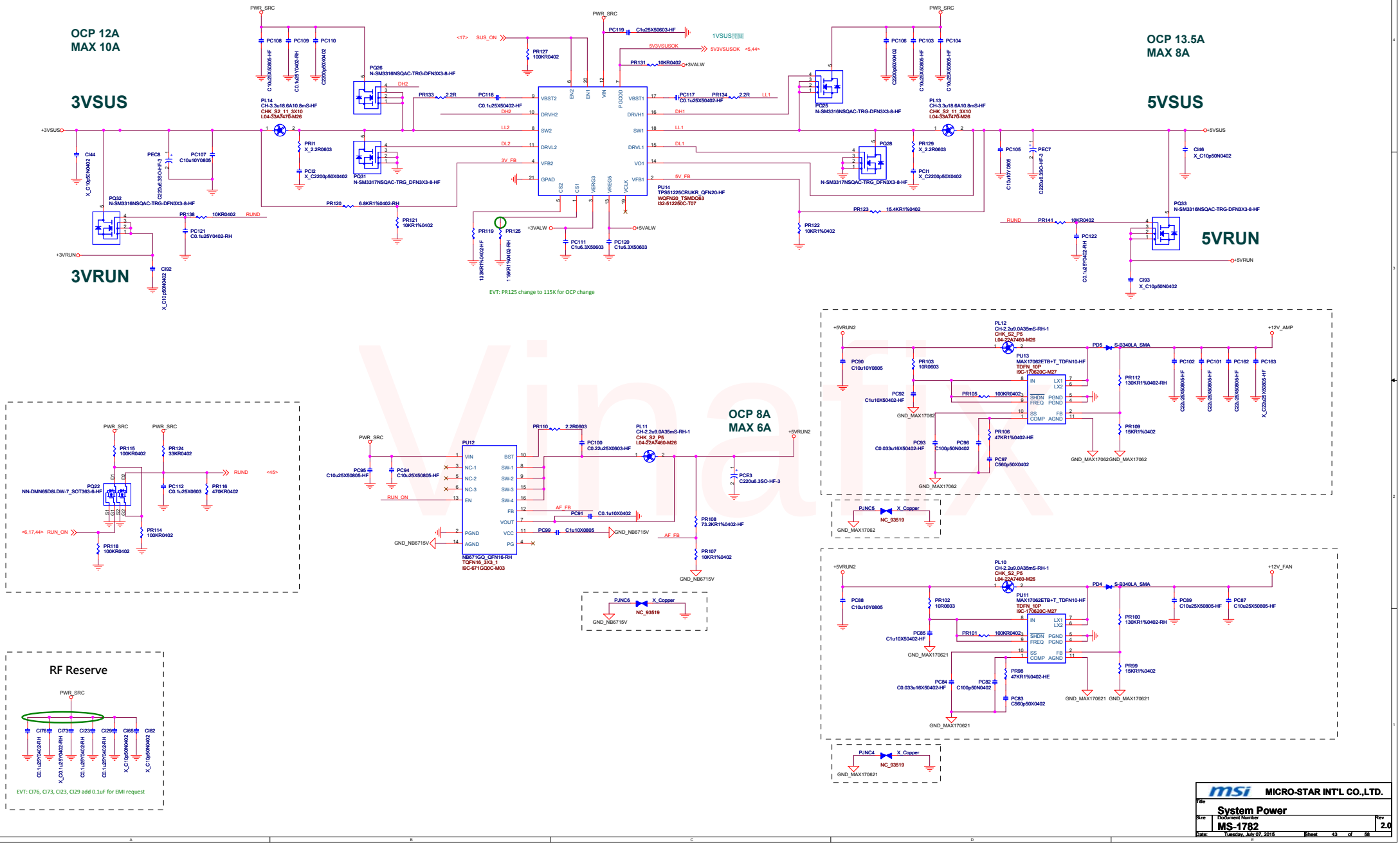
System Power



Vinafix

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	System Power		
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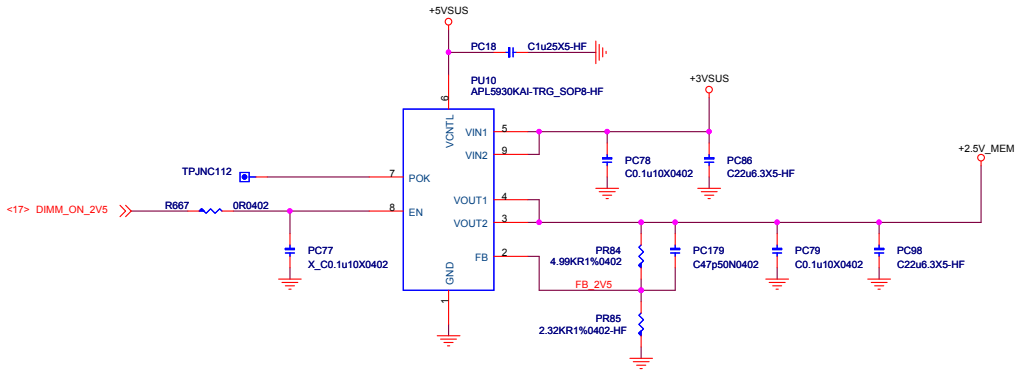
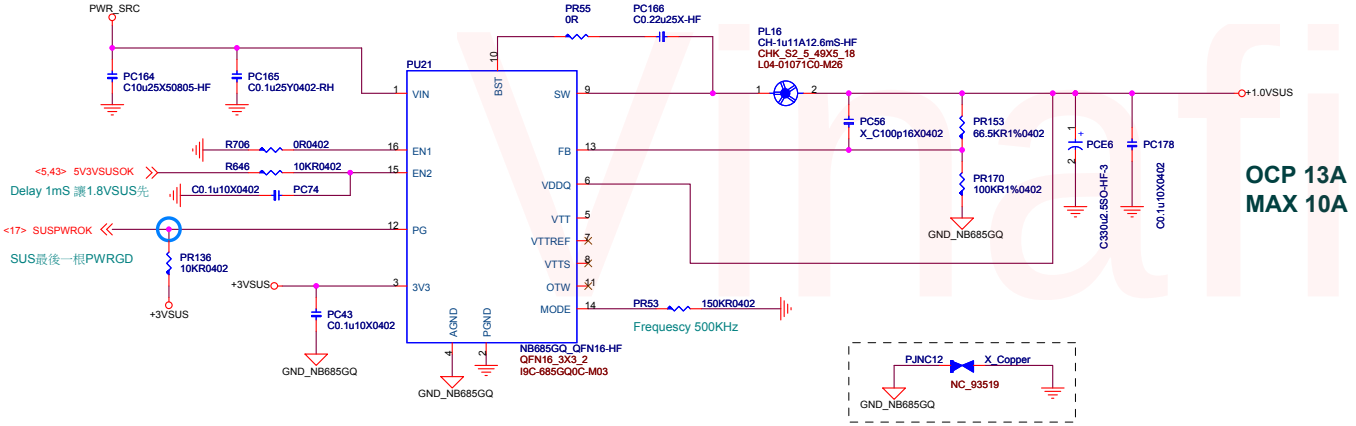
+2.5V_MEM



OCP 4.2A
MAX 1A

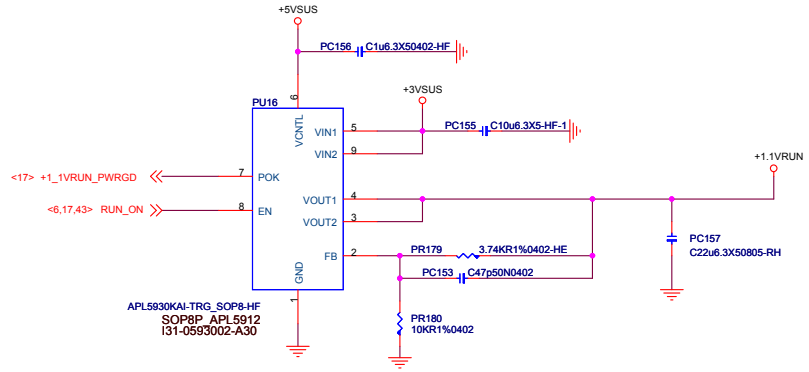
EVT: Change to LDO circuit

+1.0VSUS



OCP 13A
MAX 10A

+1.1VRUN



msi	MICRO-STAR INT'L CO.,LTD.	
Title	2.5VMEM/1VSUS/+1_1VRUN	
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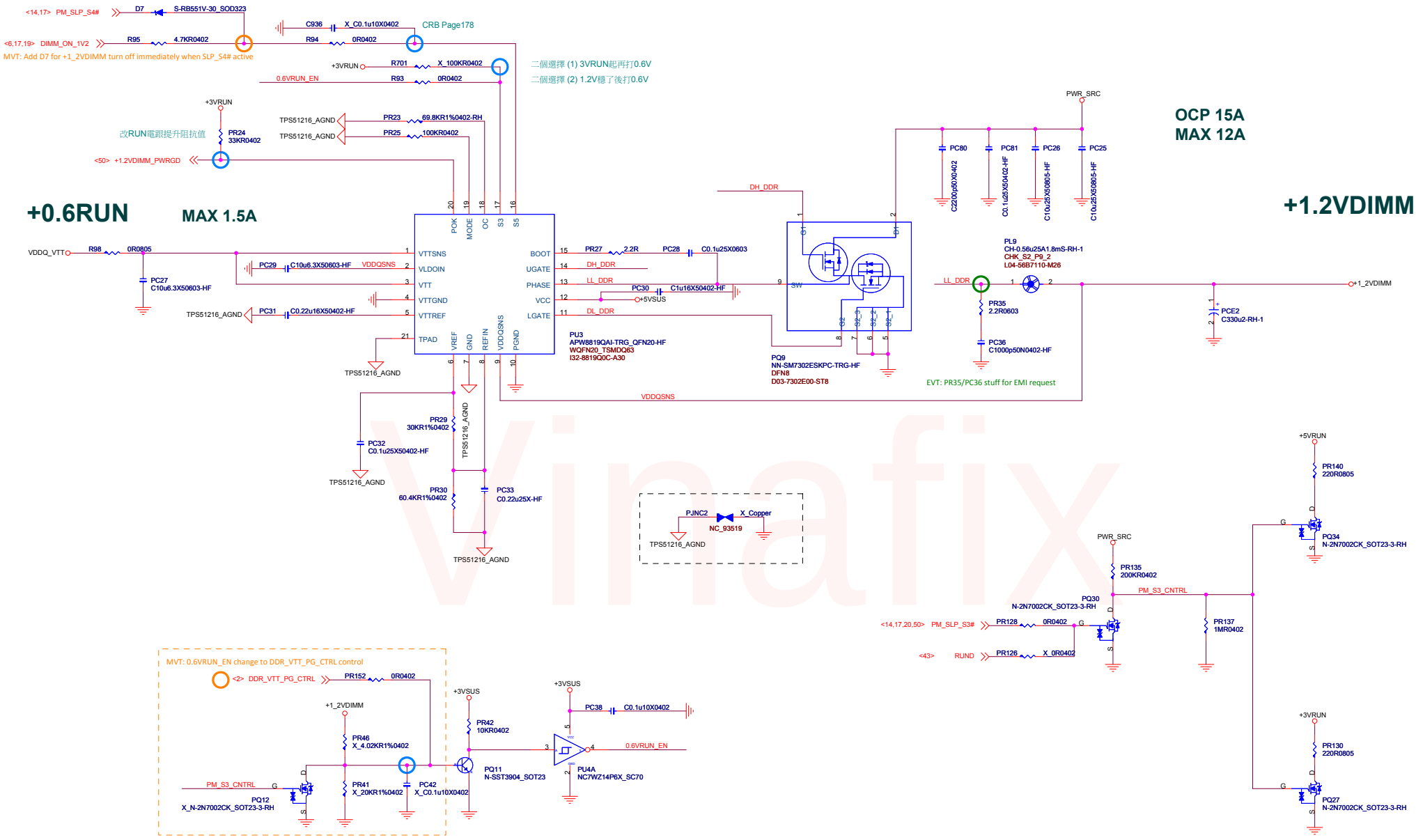
+0.6RUN
MAX 1.5A
+1.2VDIMM
OCP 15A
MAX 12A
<14,17> PM_SLP_S4#
D7
S-RB551V-30_SOD323
<6,17,19> DIMM_ON_1V2
R95 4.7KR0402
MVT: Add D7 for +1_2VDIMM turn off immediately when SLP_S4# active
C936 X_C0.1u10X0402
R94 0R0402
CRB Page178
+3VRUN
R701 X_100KR0402
0.6VRUN_EN
R93 0R0402
二個選擇 (1) 3VRUN起再打0.6V
二個選擇 (2) 1.2V穩了後打0.6V
改RUN電跟提升阻抗值
PR24 33KR0402
<50> +1.2VDIMM_PWRGD
TPS51216_AGND
PR23 69.8KR1%0402-RH
PR25 100KR0402
VDDQ_VTT
R98 0R0805
PC27 C10u6.3X50603-HF
PC29 C10u6.3X50603-HF
VDDQSNS
PC31 C0.22u16X50402-HF
VTTSNS
VLDOIN
VTT
VTTGND
VTTREF
TPAD
POK
MODE
OC
S3
S5
BOOT
UGATE
PHASE
VCC
LGATE
VREF
GND
REFIN
VDDQSNS
PGND
PR27 2.2R
PC28 C0.1u25X0603
DH_DDR
LL_DDR
PC30 C1u16X50402-HF
+5VSUS
DL_DDR
PU3
APW8819QAI-TRG_QFN20-HF
WQFN20_TSMDQ63
I32-8819Q0C-A30
PR29 30KR1%0402
PC32 C0.1u25X50402-HF
PR30 60.4KR1%0402
PC33 C0.22u25X-HF
PJNC2 X_Copper
NC_93519
PWR_SRC
PC80 C2200p50X0402
PC81 C0.1u25X50402-HF
PC26 C10u25X50805-HF
PC25 C10u25X50805-HF
PL9
CH-0.56u25A1.8mS-RH-1
CHK_S2_P9_2
L04-56B7110-M26
PR35 2.2R0603
PC36 C1000p50N0402-HF
PCE2 C330u2-RH-1
+1_2VDIMM
PQ9
NN-SM7302ESKPC-TRG-HF
DFN8
D03-7302E00-ST8
EVT: PR35/PC36 stuff for EMI request
MVT: 0.6VRUN_EN change to DDR_VTT_PG_CTRL control
<2> DDR_VTT_PG_CTRL
PR152 0R0402
PR46 X_4.02KR1%0402
PR41 X_20KR1%0402
PC42 X_C0.1u10X0402
PM_S3_CNTRL
PQ12
X_N-2N7002CK_SOT23-3-RH
PR42 10KR0402
PQ11
N-SST3904_SOT23
PC38 C0.1u10X0402
PU4A
NC7WZ14P6X_SC70
PR135 200KR0402
PQ30
N-2N7002CK_SOT23-3-RH
<14,17,20,50> PM_SLP_S3#
PR128 0R0402
<43> RUND
PR126 X_0R0402
PR137 1MR0402
PR140 220R0805
PQ34
N-2N7002CK_SOT23-3-RH
PR130 220R0805
PQ27
N-2N7002CK_SOT23-3-RH
MICRO-STAR INT'L CO.,LTD.
Title
+1.35VDIMM/+0.675VRUN
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EVT: power change list (H4+2)
CPU-core
PR157 改2.2R (0603 R11-022A013-W08)
PR613 改2.43K (R11-2431T12-W08)
PC199 改1000P (C11-1027612-M09)
PR608 改4.7K (R11-0472T12-W08)
PR615 改86.6K (R11-8662T12-W08)
PC194 改0.22uF (C11-2242312-W08)
PC193 改47nF (C11-4732012-W08)
Add PC288 10nF (C11-1032052-T34)

EVT: power change list (H4+2)
GT-core
PR667 改383R (0603 PN:R11-3830T13-W08)
PR662 改2.94K (R11-2941T12-W08)
PC227 改820P (C11-8212822-Y01)
PR664 改1.4K (R11-0142T12-W08)
PC287 改220P (C11-2212812-W08)
PR663 改 1K (-R11-0102T12-W08)
PR671 改86.6K (R11-8662T12-W08)
PC234 改100P (C11-1012812-W08)
PC232 改0.22u (C11-2242312-T04)
PR668 改5.49K (R11-5491T22-W08)

EVT: power change list (H4+2)
SA-core
PR621改2.26K (R11-2261T12-W08)
PC207改1.2nF (C11-1222832-W08)
PR618改2.87K (R11-2871T12-W08)
PR626改71.5K (R11-7152T22-W08)

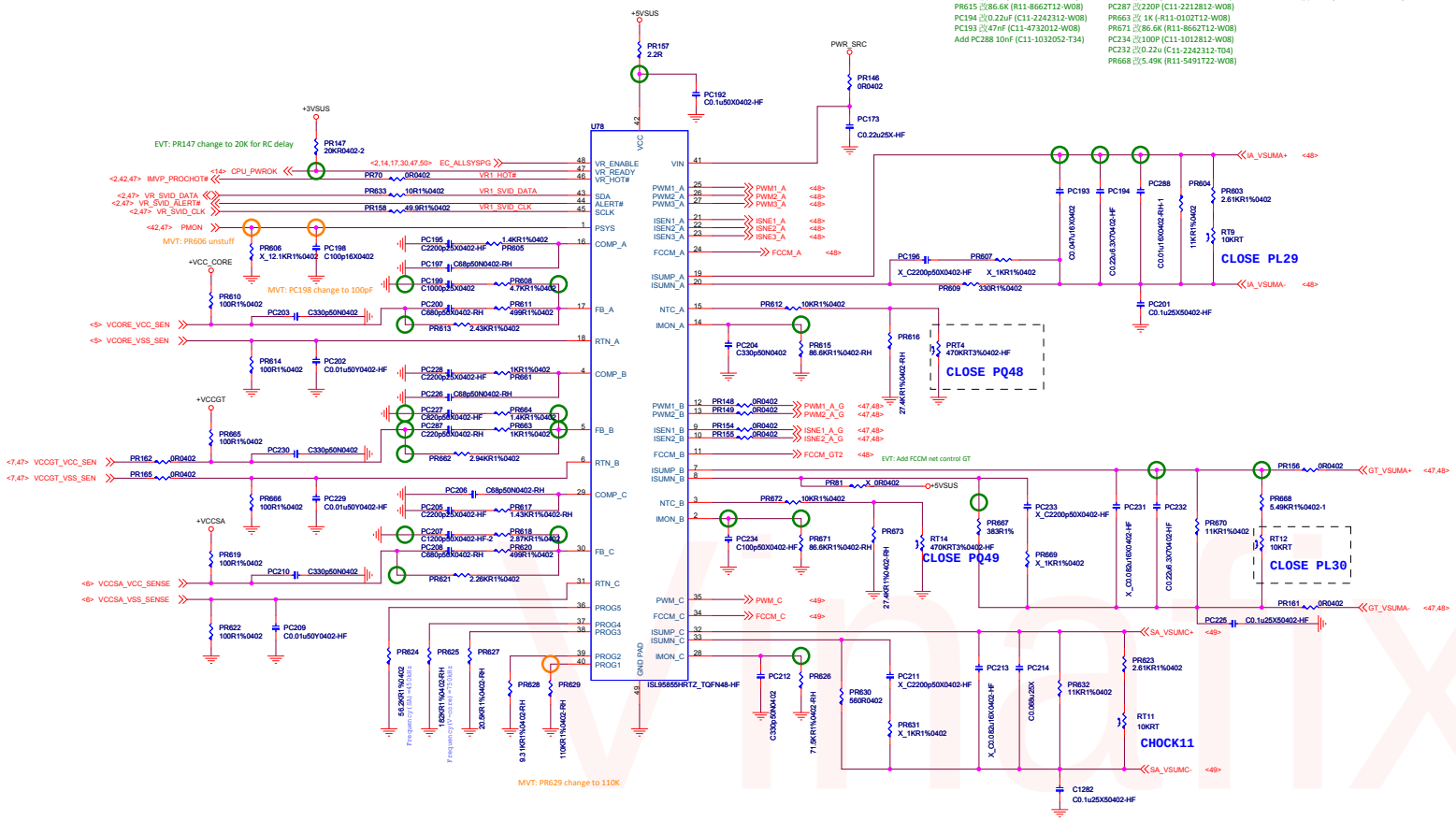

TABLE 4. PROG1 PROGRAMMING TABLE

TYPICAL PROG1 RESISTOR (±1%, kΩ)	VR A + VR B + VR C (GTUS) VBoot (V)	SLEW RATE ALL VRs (mV/μs)	ADDRESS SELECTION VR A	VR B	VR C
1.87	1.05	30	GT[01h]	GTUS [03h]	SA [02h]
5.62	1.05	30	GT[01h]	IA [00h]	GTUS [03h]
9.31	1.05	30	GT[01h]	IA [00h]	SA [02h]
13.3	1.05	30	IA [00h]	GTUS [03h	SA [02h]
16.9	1.05	30	IA [00h]	GT[01h]	GTUS [03h]
20.5	1.05	30	IA [00h]	GT[01h]	SA [02h]
24.3	1.05	10	GT[01h]	GTUS [03h]	SA [02h]
28.0	1.05	10	GT[01h]	IA [00h]	GTUS [03h]
34.0	1.05	10	GT[01h]	IA [00h]	SA [02h]
41.2	1.05	10	IA [00h]	GTUS [03h	SA [02h]
48.7	1.05	10	IA [00h]	GT[01h]	GTUS [03h]
56.2	1.05	10	IA [00h]	GT[01h]	SA [02h]
63.4	0	30	GT[01h]	GTUS [03h]	SA [02h]
71.5	0	30	GT[01h]	IA [00h]	GTUS [03h]
78.7	0	30	GT[01h]	IA [00h]	SA [02h]
88.7	0	30	IA [00h]	GTUS [03h	SA [02h]
100	0	30	IA [00h]	GT[01h]	GTUS [03h]
110	0	30	IA [00h]	GT[01h]	SA [02h]
121	0	10	GT[01h]	GTUS [03h]	SA [02h]
137	0	10	GT[01h]	IA [00h]	GTUS [03h]
150	0	10	GT[01h]	IA [00h]	SA [02h]
165	0	10	IA [00h]	GTUS [03h	SA [02h]
182	0	10	IA [00h]	GT[01h]	GTUS [03h]
215	0	10	IA [00h]	GT[01h]	SA [02h]

TABLE 5. PROG2 PROGRAMMING TABLE

TYPICAL PROG2 RESISTOR (±1%, kΩ)	IMAX VR A 3-PH (A)	2-PH (A)	1-PH (A)	VR A PS1L PHASE REDUCTION
1.87	67	35	7	2-Phase
5.62	70	40	10	2-Phase
9.31	75	45	15	2-Phase
13.3	80	50	18	2-Phase
16.9	85	55	20	2-Phase
20.5	91	60	25	2-Phase
24.3	95	65	27	2-Phase
28.0	100	67	30	2-Phase
34.0	105	70	33	2-Phase
41.2	110	75	35	2-Phase
48.7	115	80	40	2-Phase
56.2	120	85	45	2-Phase
63.4	67	35	7	1-Phase
71.5	70	40	10	1-Phase
78.7	75	45	15	1-Phase
88.7	80	50	18	1-Phase
100	85	55	20	1-Phase
110	91	60	25	1-Phase
121	95	65	27	1-Phase
137	100	67	30	1-Phase
150	105	70	33	1-Phase
165	110	75	35	1-Phase
182	115	80	40	1-Phase
215	120	85	45	1-Phase

TABLE 6. PROG3 PROGRAMMING TABLE

TYPICAL PROG3 RESISTOR (±1%, kΩ)	IMAX VR B 2-PH (A)	1-PH (A)	DROOP VR B
1.87	35	7	Active
5.62	40	10	Active
9.31	45	15	Active
13.3	50	18	Active
16.9	55	20	Active
20.5	60	25	Active
24.3	65	27	Active
28.0	67	30	Active
34.0	70	33	Active
41.2	75	35	Active
48.7	80	40	Active
56.2	85	45	Active
63.4	35	7	Disabled
71.5	40	10	Disabled
78.7	45	15	Disabled
88.7	50	18	Disabled
100	55	20	Disabled
110	60	25	Disabled
121	65	27	Disabled
137	67	30	Disabled
150	70	33	Disabled
165	75	35	Disabled
182	80	40	Disabled
215	85	45	Disabled

TABLE 7. PROG4 PROGRAMMING TABLE

TYPICAL PROG4 RESISTOR (±1%, kΩ)	DROOP VR A	DROOP VR C	VR A and VR B SWITCHING FREQUENCY (kHz)
1.87	Disabled	Disabled	300
5.62	Disabled	Disabled	350
9.31	Disabled	Disabled	450
13.3	Disabled	Disabled	583
16.9	Disabled	Disabled	750
20.5	Disabled	Disabled	1000
24.3	Disabled	Active	300
28.0	Disabled	Active	350
34.0	Disabled	Active	450
41.2	Disabled	Active	583
48.7	Disabled	Active	750
56.2	Disabled	Active	1000
63.4	Active	Disabled	300
71.5	Active	Disabled	350
78.7	Active	Disabled	450
88.7	Active	Disabled	583
100	Active	Disabled	750
110	Active	Disabled	1000
121	Active	Active	300
137	Active	Active	350
150	Active	Active	450
165	Active	Active	583
182	Active	Active	750
215	Active	Active	1000

TABLE 8. PROG5 PIN

TYPICAL PROG5 RESISTOR (±1%, kΩ)	VR C IMAX (A) SA	GTUS	VR C SWITCHING FREQUENCY (kHz)
1.87	7	17	300
5.62	9	20	300
9.31	12	25	300
13.3	15	27	300
16.9	7	17	350
20.5	9	20	350
24.3	12	25	350
28.0	15	27	350
34.0	7	17	450
41.2	9	20	450
48.7	12	25	450
56.2	15	27	450
63.4	7	17	583
71.5	9	20	583
78.7	12	25	583
88.7	15	27	583
100	7	17	750
110	9	20	750
121	12	25	750
137	15	27	750
150	7	17	1000
165	9	20	1000
182	12	25	1000
215	15	27	1000

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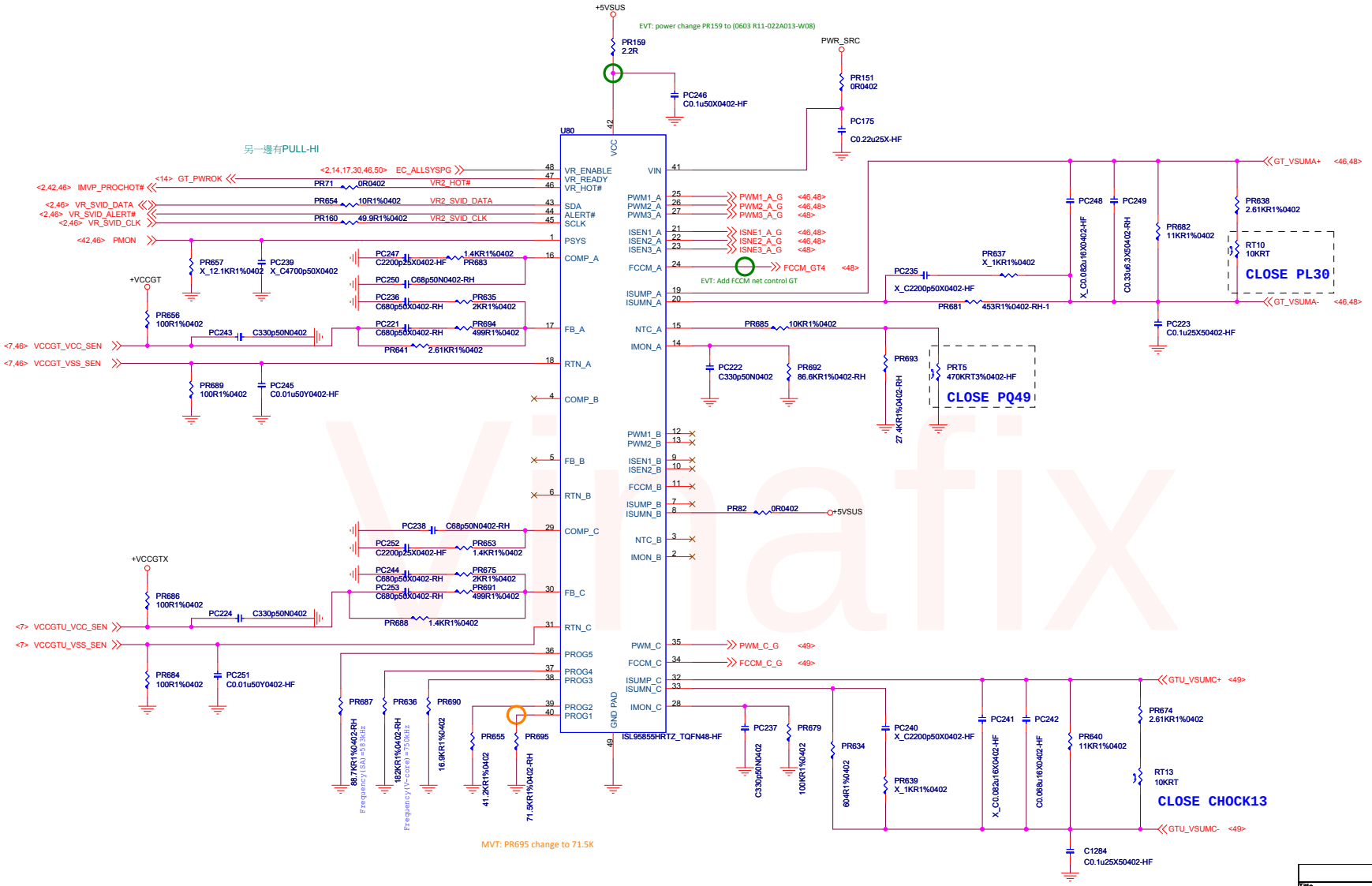
Skylake H-line 44e 45W ISL95855



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EVT power change
1. PR278,PR286,PR294, PR303, PR314, PR324 change to 0603 package
2. PQ48,PQ50,PQ53,PQ51,PQ54,PQ49 change P/N to I33-F30350C-F01
3. U49/US1/US4 add FCCM control GT power

OCP 81A
MAX 68A

+VCC_CORE

this phase for GT4 only

H-42
OCP 66A
MAX 55A

H-44e
OCP 112A
MAX 104A

+VCCGT

EVT: change to C11-1067610-M09(架高型MLCC)

EVT: PC330 unstuff (H4+2)

EVT: PC333 stuff (H4+2)

EVT: PC343 unstuff (H4+2)

Spec Page18

EVT: Add FCCM_A control

EVT: Add FCCM control

Title: <Title>
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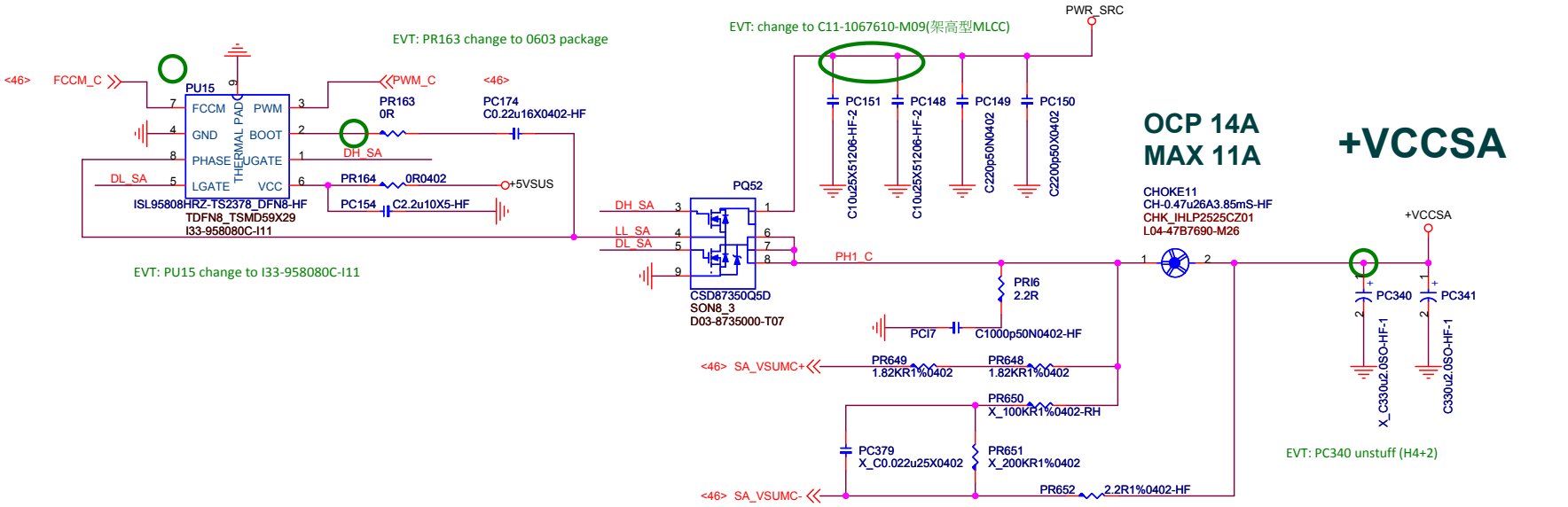

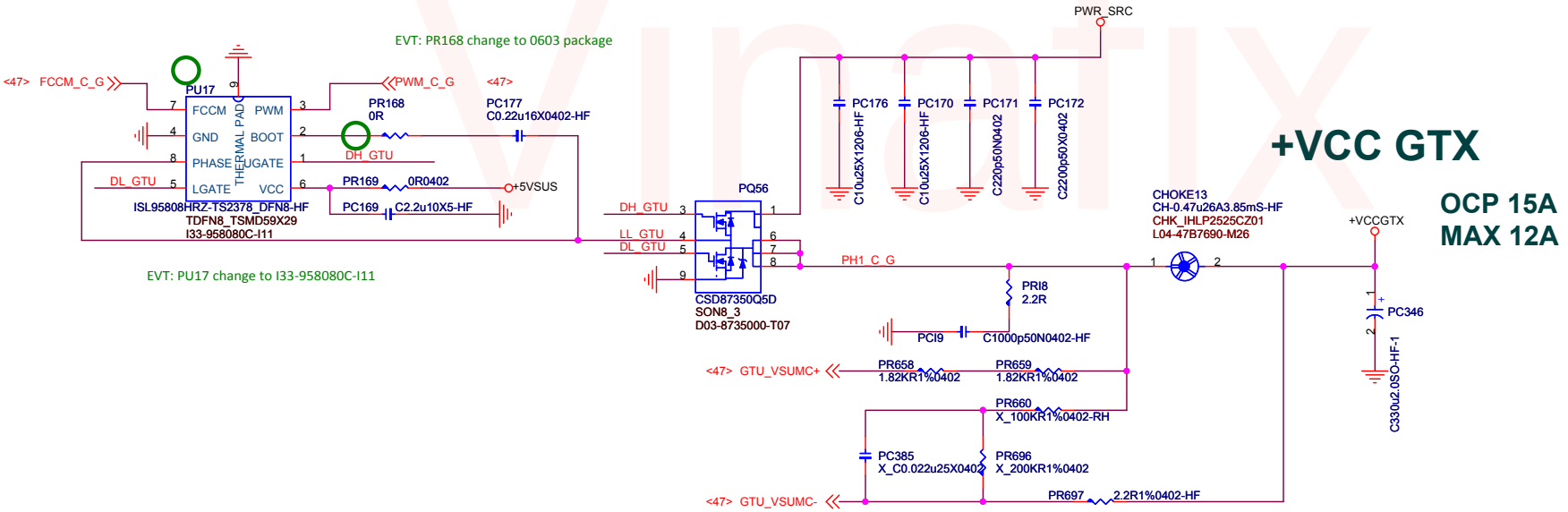

Title	<Title>	
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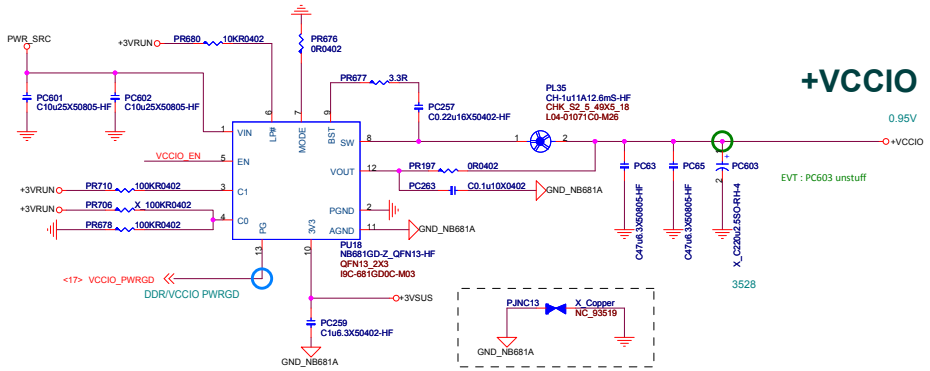
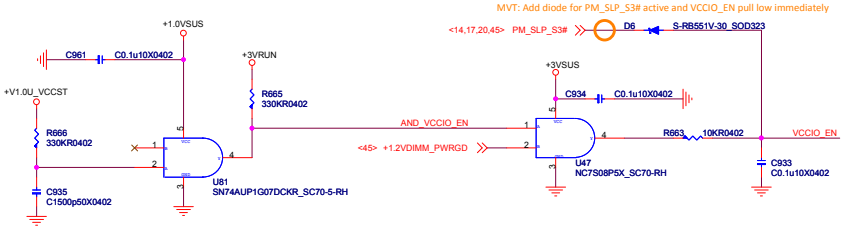
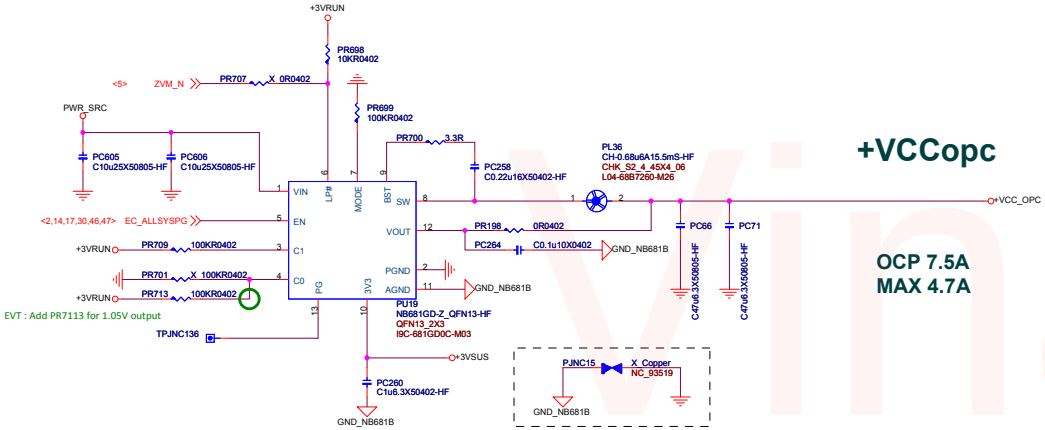


+VCCIO

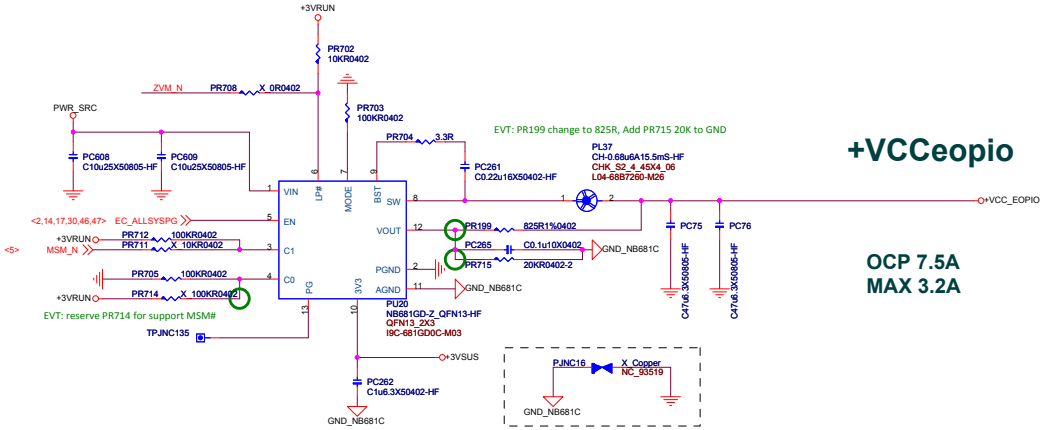
OCP 7.5A
MAX 5.5A





+VCCopc

OCP 7.5A
MAX 4.7A



+VCCeopio

OCP 7.5A
MAX 3.2A

Title	<Title>		
Size: Custom	Document Number: MS-1782		Rev: 2.0
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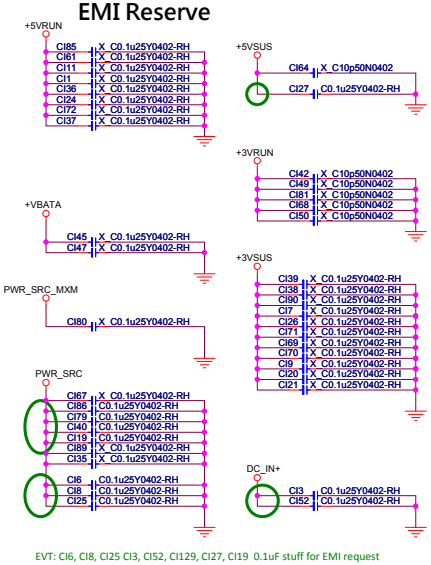
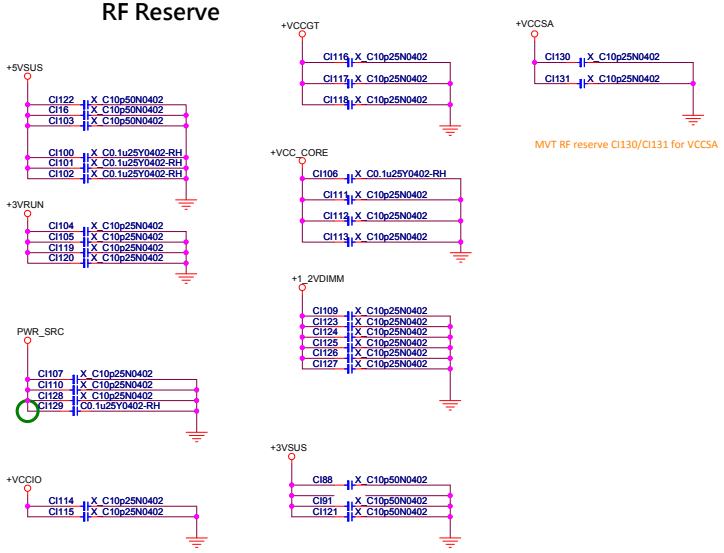
EMI Reserve



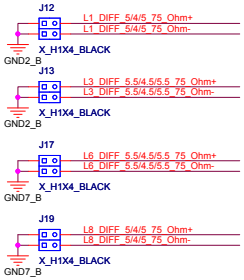
EVT: CI6, CI8, CI25 CI3, CI52, CI129, CI27, CI19 0.1uF stuff for EMI request
CI40, CI79, CI86 0.1uF stuff for RF request

RF Reserve

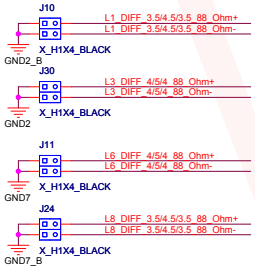


MVT RF reserve CI130/CI131 for VCCSA

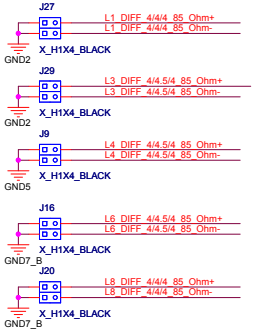
75 OHM / DDR3 DQS



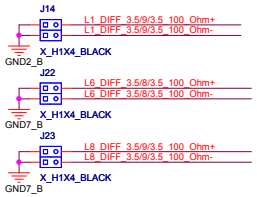
88 OHM / DDR3L (CLK)



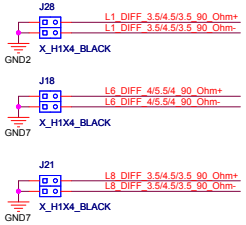
85 OHM /SATA /PCH PCIE/ EDP USB /HDMI/DP/DMI/CLK/PEG



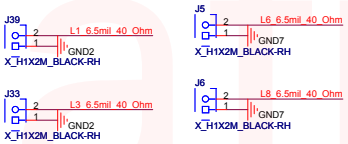
100 OHM / LAN



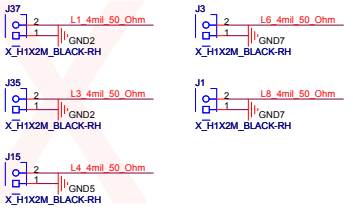
90 OHM /Alpine Ridge



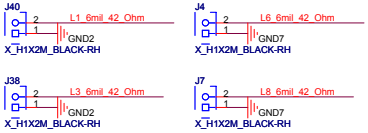
40 OHM / DDR3 CTRL



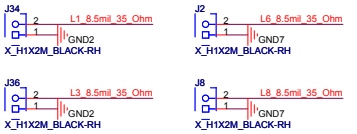
50 OHM / NORMAL



42 OHM / DDR3 DQ



35 OHM / DDR3 CMD



MICRO-STAR INT'L CO.,LTD.		
Title: EMI		
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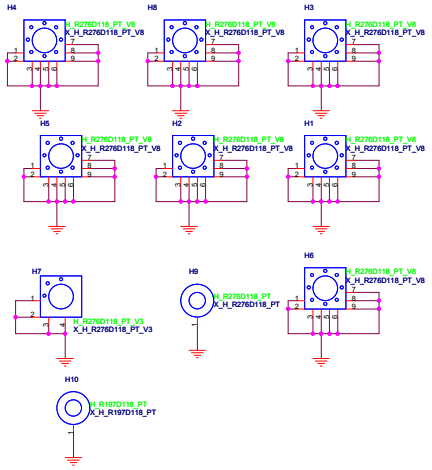
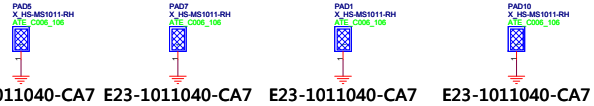
Board Corner



Top Spring



E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7

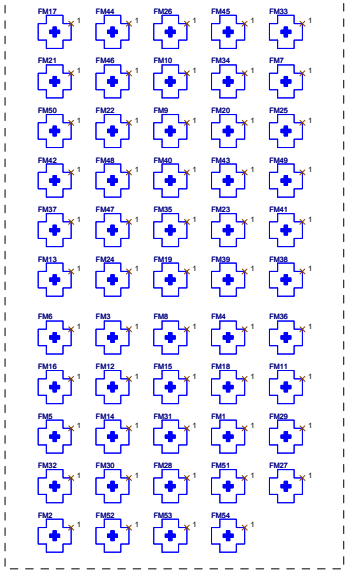
E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7

BOT Spring

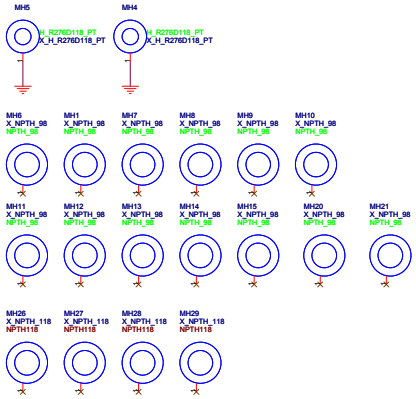
E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7

E23-1011040-CA7 E23-1011040-CA7

EVT: add BOT Spring *3 (PAD11/PAD12/PAD13)



Board Inside

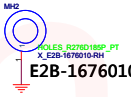


ESS board stand off

EVT: add stand off for ESS board

E2B-1634020-L63 E2B-1634020-L63

Board Stand off



E2B-1676010-L63

Bracket

60階

EVT新增 CPU Bracket

E2M-7820111-A89

MYLAR

60階

E2P-7813011-G40

USB_SPONGE

E2Y-7812211-Y42

USB_TAPE

E2Y-6F12511-G40

THERMAL_SPONGE

E2Y-6330511-G40

LABEL

60階

MVT Stuff

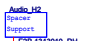
Y01-RHDMI03-000

60階

G51-LA01678-A09

Audio Stand off

E2B-1351010-L63



E2B-1313010-L63

SPONGE

LED遮光泡棉

60階

E2Y-71H1111-G40

MYLAR

60階

E2P-4312611-G40

RUBBER

60階

E2Y-6F11711-Y40

RUBBER

60階

E2Y-6F11711-Y40

MXM Rubber

ODD Stand off

E2B-1634020-L63

ESS RUBBER

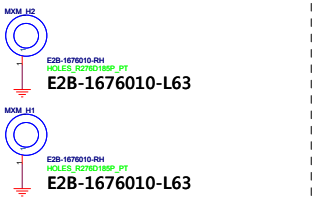
60階

E2Y-6111911-Y40

WLAN_H1

E2B-1781010-A89

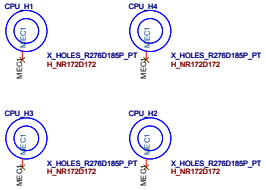
MXM Stand Off



E2B-1676010-L63

E2B-1676010-L63

CPU Hole



PCH Stand off

E2B-163B010-L63 E2B-163B010-L63

PCH Thermal Sink

60階

E31-0403231-TA9

SCREW

60階 60階

E43-1203003-H29 E43-1203003-H29

PCB

P30-1782120-H73 (翰宇博德)

P30-1782120-T53 (健鼎無錫)

CPU_MYLAR

60階

E2P-6F40412-Y42

MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME

Size: Document Number: MS-1782 Rev: 2.0

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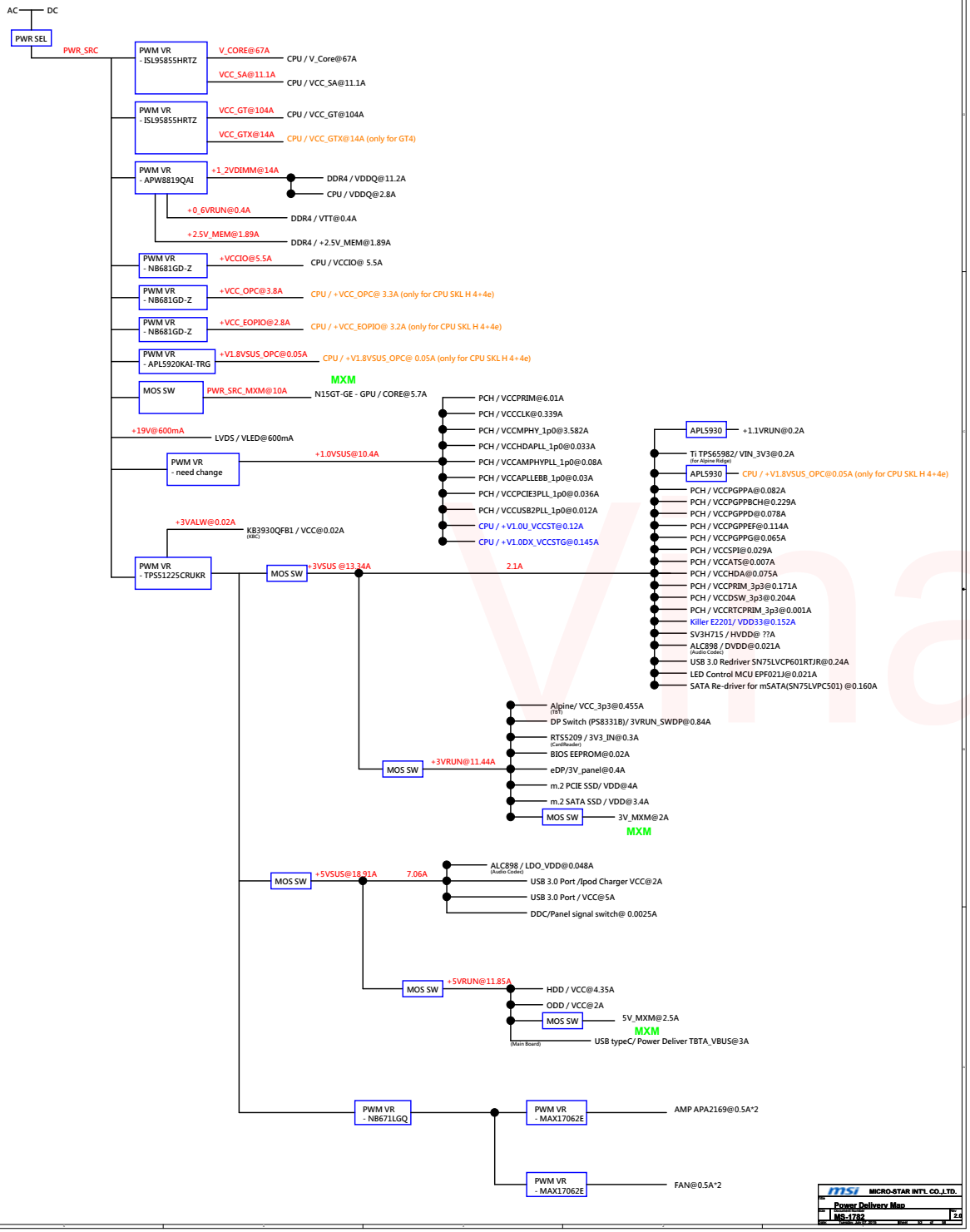
MS-1782 Power Delivery Chart



Vinafix

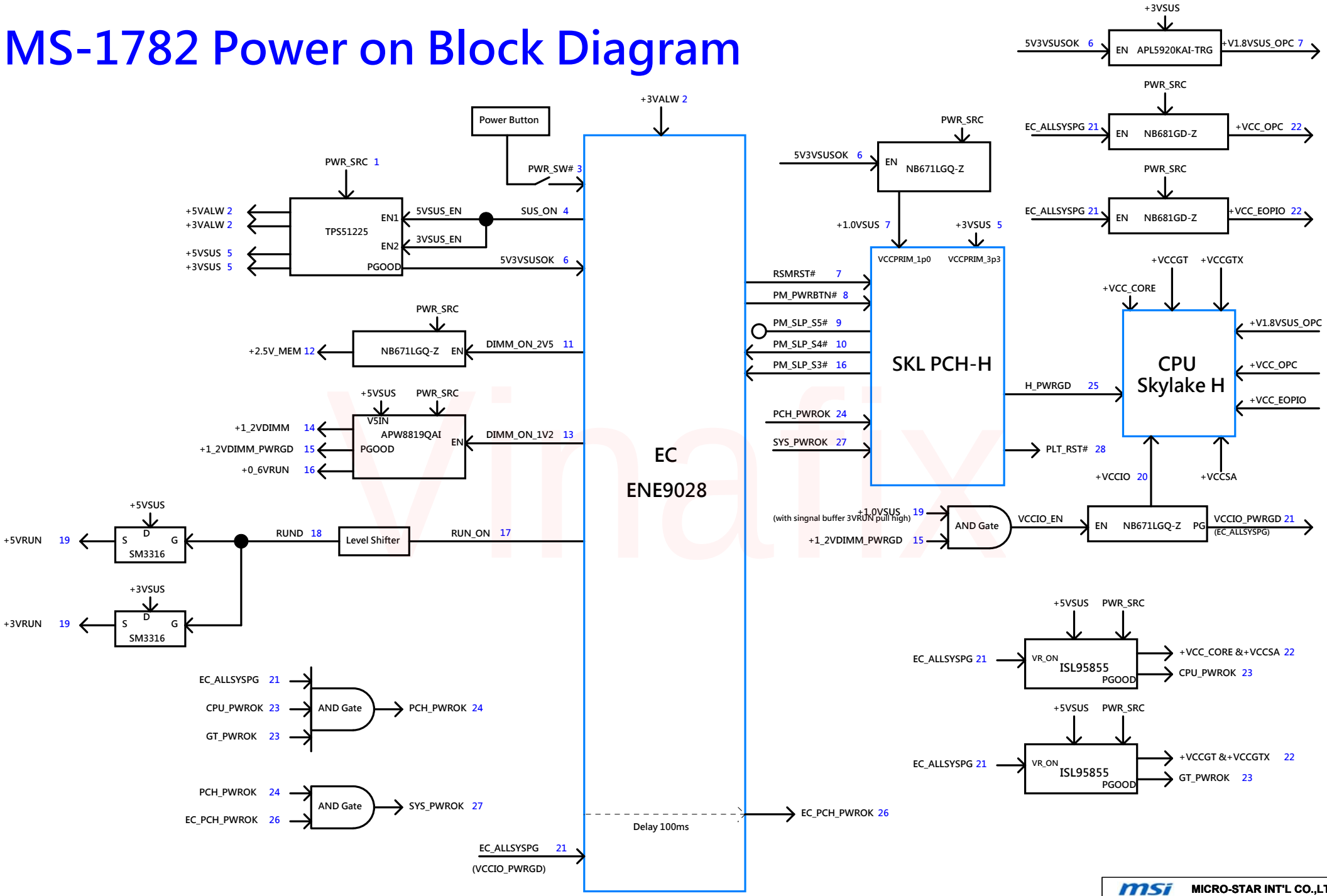
MICRO-STAR INT'L CO.,LTD.

Power Delivery Map

MS-1782

2.0

MS-1782 Power on Block Diagram



Vinafix

msi MICRO-STAR INT'L CO.,LTD.			
Title: Power on Block Diagram			
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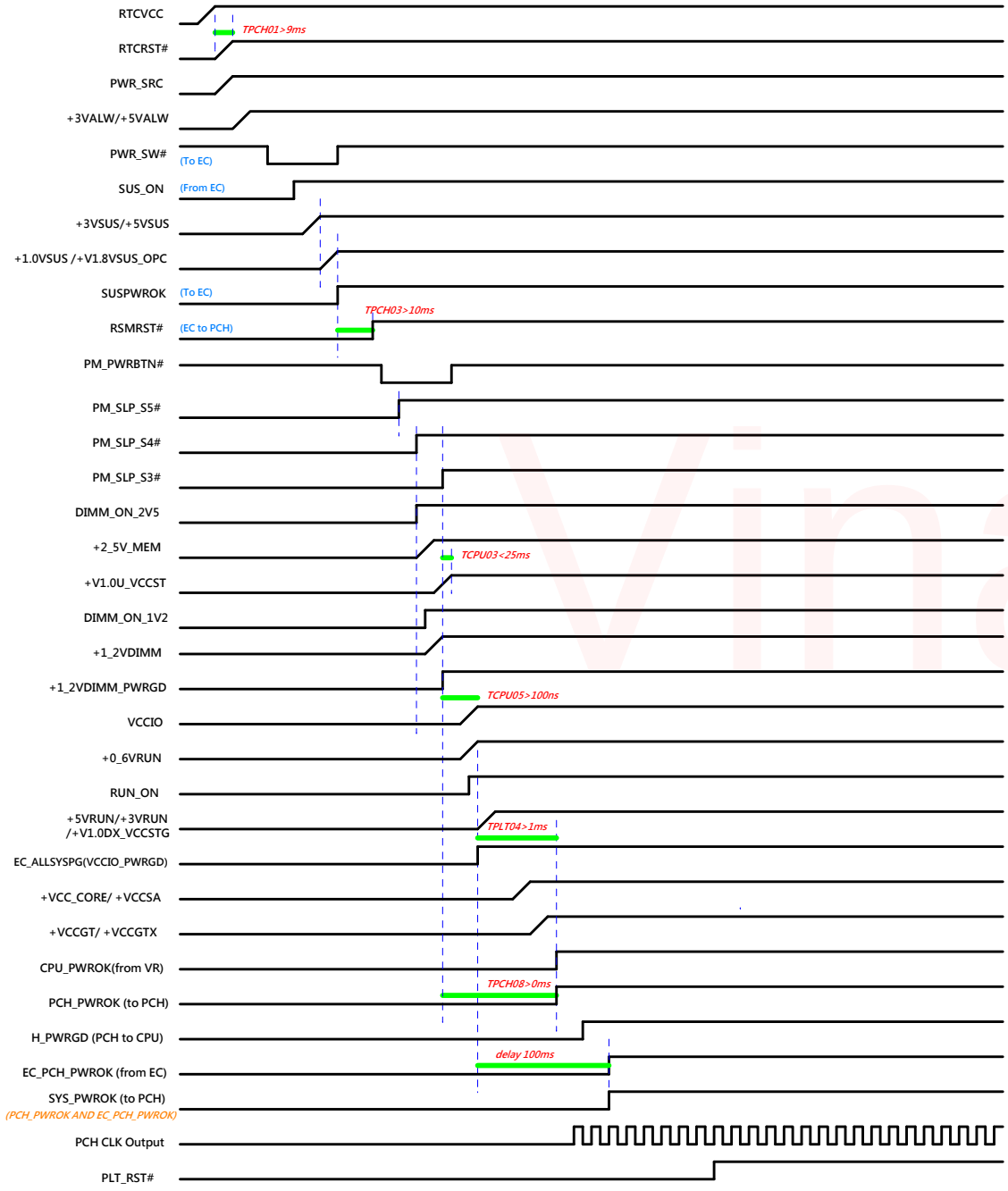
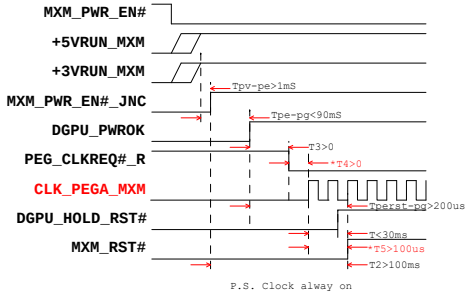
Power on Sequence

G3 -> S0

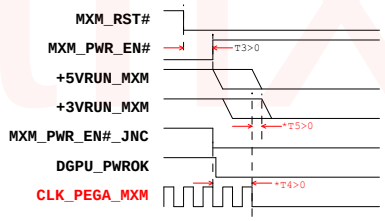


Power-Up Sequence For Optimus On MXM



P.S. Clock alway on

Power-Down Sequence For Optimus On MXM



P.S. Clock alway on

Vinafix

msi	MICRO-STAR INT'L CO.,LTD.	
Title	Power on Sequence	
Size	Document Number MS-1782	Rev 2.0
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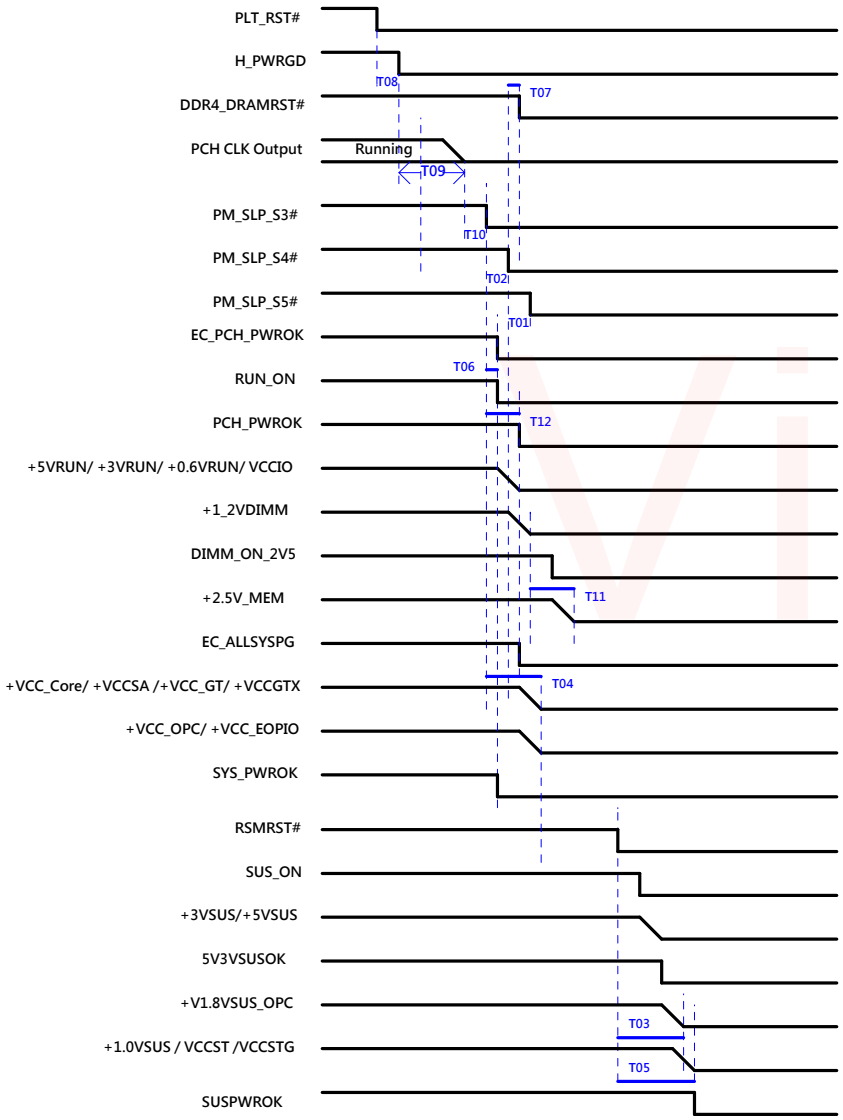
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

Wistron

MICRO-STAR INT'L CO.,LTD.

Title: Power down Sequence

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Change List

DVT to EVT modify

2015.03.10

1. p.37 Remove QE1 for EC request
2. p.17 R520 stuff for EC request
3. p.15 Add R714 for EC load code
4. p.13 R668 unstuff for EC control only
5. p.20 Y6 change main source to D04-1007200-F07
6. p.12 R591 change to R11-0105T12-W08
7. p.17 KBIN add 10K pull high to +3VALW for EC request
8. p.14 R626 change to 150K reserve for PCHHOT#
9. p.15 R641/R642 unstuff
10. p.14 R639 stuff
11. p.6 R576/R577 stuff
12. p.29 R257/R258/R259/R260/R261/R264/R265/R266/R267/R271/R272 change to 0402 package
13. p.27 ESD5/6/7/8 stuff
14. p.14 Add R715 pull high +3VSUS
15. p.14 Add C985 for CPU_PWROK RC delay
16. p.20 R811 unstuff
17. p.2 add circuit for H_VCCST_PWRGD_R power sequence , R106 follow DG change to 60ohm.
18. p.29 HDMI1 因機構問題conn. change to 凡甲料(N5Y-19M0910-AF2)
19. p.15 Add TBT_FORCE_PWR connect to GPP_G16
20. p.15 Add BT_CIO_PLUG_EVENT_N connec to GPP_G12
21. p.15 MXM_PRSNT_RUN#_R change to GPP_G13
22. remove R816 , TBT_FORCE_PWR connect to PCH GPP_G16
23. Add R117 connect to PCH PM_SLP_S3#
24. p.46 PR147 change to 20K for RC delay
25. p.25 ~~Add R816/C636 for MUTE# RC delay~~ EN pin change to pull high 10K +3VSUS

2015.03.16

26. p.13 Add R716 for USB2_ID not support dual role ,shall be connected to GND
27. p.13 R668 unstuff for EC control only (PECI)
28. p.15 Reserve R717 for MOW WW09 request (stuff only for ES sample)

2015.03.17

POWER modify

29. p.43 PR125 change to 115K for OCP change
30. p. 44+2.5V_MEM change to LDO circuit
31. p.8 PEC3 &C740 unstuff
32. p.42 PR150 change to R11-005CT1H-W08 ,PR166 delete
33. 全GAP 取消
34. p.46,
    power change list (H4+2)
    CPU-core
    PR157 改2.2R (0603 R11-022A013-W08)
    PR613 改2.43K (R11-2431T12-W08)
    PC199 改1000P (C11-1027612-M09)
    PR608 改4.7K (R11-0472T12-W08)
    PR615 改86.6K (R11-8662T12-W08)
    PC194 改0.22uF (C11-2242312-W08)
    PC193 改47nF (C11-4732012-W08)
    Add PC288 10nF (C11-1032052-T34)
35. p.46
    power change list (H4+2)
    GT-core
    PR667 改383R (0603 PN:R11-3830T13-W08)
    PR662 改2.94K (R11-2941T12-W08)
    PC227 改820P (C11-8212822-Y01)
    PR664 改1.4K (R11-0142T12-W08)
    PC287 改220P (C11-2212812-W08)
    PR663 改 1K (-R11-0102T12-W08)
    PR671 改86.6K (R11-8662T12-W08)
    PC234 改100P (C11-1012812-W08)
    PC232 改0.22u (C11-2242312-T04)
    PR668 改5.49K (R11-5491T22-W08)
36. p.46
    power change list (H4+2)
    SA-core
    PR621改2.26K (R11-2261T12-W08)
    PC207改1.2nF (C11-1222832-W08)
    PR618改2.87K (R11-2871T12-W08)
    PR626改71.5K (R11-7152T22-W08)
37. p.47 power change PR159 to (0603 R11-022A013-W08)
38. p.48 PC330/PC340 unstuff , PC333 stuff (H4+2)
39. PR163/PR168 change to 0603 package
40. p.15 U39 remove ROM socket ,and reserve R717 for MOW request
41. .46 CPUFAN_PWM &MXMFAN_PWM 改由EC DAC control ,電阻先改0R, 電容不上件
42. p.25 change to GAIN 6 dB, add C582 2.2uF 對地電容, reserve C589 0.1uF
43. p.49 PU15/PU17 change to I33-958080C-I11
44. C11-1067312-M09 footprint 修改, 由C0402 改為C0402_EXTRA_T
45. p.22 SLOT1 料號變更高度改為N15-0670330-L06
46. p.25 add HP_MUTE# circuit for de-pop ,C519/C501/C715/C729 change to 2.2uF
47. p.35 RC8/RC10 change to 75ohm
48. p.23 GLAN chip change to E2400
49. p.21 UART TX/RX 改1M 對地 ,TBTA_ACE_GPIO6 change to 10K pull GND.
50. All D03-7002D10-D07 change to D03-65D8L09-D07 for ESD protect

2015.03.25

51. p.33 CONA2 pin8/9 GND連接移除
52. p.14 SLP_S0 測點移除
53. p.6 delete TPJNC132
54. p.13 reserve EC24 for EMI ,R678 change to 33R, R695 change to 33R
55. p.42 PC2, CI4, CI14, CI12, CI22, CI13, CI17,CI18,CI15,CI51,CI63 ,CI62 add 0.1uF for EMI request
56. p.43 CI76, CI73, CI23, CI29 add 0.1uF for EMI request
57. p.51 CI6, CI8, CI25 CI3, CI52, CI129 ,CI79 0.1uF stuff for EMI request
58. p.45 PR35/PC36 stuff for EMI request

2015.03.26

59. p.21 L18/L21 stuff, R219/R221 delete for EMI request
60. p.20&p.29 modify U15 circuit to U86 (Switch改放置在AR SINK0 前, SINK0 改為DP++ mode input)
61. p.29 R805/R806/R861/R862 unstuff ,stuff circuit component for DGPU DDC function
62. p.50 PC603 unstuff, add PR7113 for 1.05V output
63. p.50 EVT: reserve PR714 for support MSM# , PR199 change to 825R, Add PR715 20K to GND
64. p.48
    a. PR278,PR286,PR294, PR303, PR314, PR324 change to 0603 package
    b. PQ48,PQ50,PQ53,PQ51,PQ54,PQ49 change P/N to I33-F30350C-F01
    c. U49/U51/U54 pin2改接V-core(U78)(U80) FCCM
65. p.42 PD1 unstuff
66. p.5 R570/R571/R572 unstuff , stuff only for GT4
67. p.23 change U25 to E2400 正式料號, C338/C339/C908/C909 change to 0.1uF
68. ~~p.20 C837 change to 47uF 0805 ,add L33 0.1uH,~~ C753/C758/C759 change to 47uF 0805

2015.03.27

69. p.52 add BOT Spring *3
70. p.51 add CI27 0.1uF for EMI request
71. p.15 add R865 for +3VSUS to +VCCSPI
72. p.20 Add VCC3V3_S0 power for U86 PIN R13
73. , follow AR DG add L33/C986/C988 for VCC3V3_S0, C714移至VCC3V3_S0 下
74. p.14 R620 unstuff , not support SBA

2015.03.30

75. Power change PQ13/PQ14 to P/N:D03-4309P0C-ST8
76. p.46, p.48 Add FCCM_A control for VCC_Core
77. p.48, p.49 PC140/PC143/PC147/PC145/PC161/PC168/PC128/PC131/PC132/PC135/PC139 /PC136/PC148/PC151 change to C11-1067610-M09(架高型MLCC)
78. p.21 TPS65982 change to new P/N B07-6598205-T07
79. p.25 U88 SV3H715 change to formal P/N

2015.04.01

80. p.25 Add conn. from ES9016 &modify HP circuit
81. p.32 change Earphone net name
82. p.52 add stand off ESS_H1 &ESS_H2 for ESS board

2015.04.08

~~83. p.42 PC72 modify to 11KR for exchange charge IC 24780S~~

2015.04.09

84. p.23 U23 LAN transformer change to AZ N-8600GS(OL5-7966001)
85. p.42 PU1 change to BQ24780S(I34-247801C-T07)

2015.04.10

86. p.2 R658 change to 49.9R ,R102 change to 499R follow DG.

2015.04.15

87. p.42 PC72 modify to 22KR for exchange charge IC 24780S

EVT to MVT modify

2015.05.15

1. p.19 unstuff C295 for LED flash issue
2. p.19 U26 input DIMM_ON_2V5 change to DIMM_ON_1V2 for solve KB flash issue
~~3. p.20 unstuff R815/R817 &add R819/R874 for RTD3 support~~
4. p.20 add R869/R870/R871/R872 100K pull GND if DDC not in use
5. p.20 TBT_FORCE_PWR follow AR DG add 100K pull GND
6. p.20 TBT_SRC_HPD add 2.2K pull high for SINK0 occupy
7. p.20 AR SINK0 HDMI circuit remove
8. p.4 DDI2 AUX remove for HDMI output only.
9. p.20,p29 HDMI 更改架構, 線路不經過AR 改為獨立出來
~~10. p.20 R277 change from 47KR to 2KR.~~

2015.05.19

11. 刪減HDMI1.4/HDMI2.0 切換線路, 新增R918/R919 0R for HDMI2.0 support BOM modify
12. p.20 AR SINK0 AUX &HPD 新增測點
13. Add CI130/ CI131 for RF request

2015.05.22

14. p.32 Add R517 damping resistor (reserve)
15. p.17 C636 reserve

POWER modify

16. p.46, p.47 PR606,PR657,PC239不上件
17. p.46 PC198 改100pF
18. p.46 PR629 GT2 PR629=110k, ~~GT4 PR629=71.5k~~
19. p.47 PR695 change to 71.5K
20. p.45 0.6VRUN change to DDR_VTT_PG_CTRL control
21. p.45 Add R95 &D7 for +1_2VDIMM turn off immediately when SLP_S4# active

2015.06.04

22. p.15 R717 unstuff for QS sample
23. p.29 R277 change to 4.7KR

1.0 -> 2.0 Modify for ESS solution

2015.06.17

1. p.25 remove headphone L/R from ESS audio Board
2. p.35 新增FPCC2 from ESS小板飛線至C小板, 並刪除原主板過來的Headphone L/R
3. p.35 reserve RC13/RC14 for EMI
4. p.23 R866 change from 0R to Bead for EMI request
5. p.23 GND_LAN to GND change from copper to Bead

Winafix

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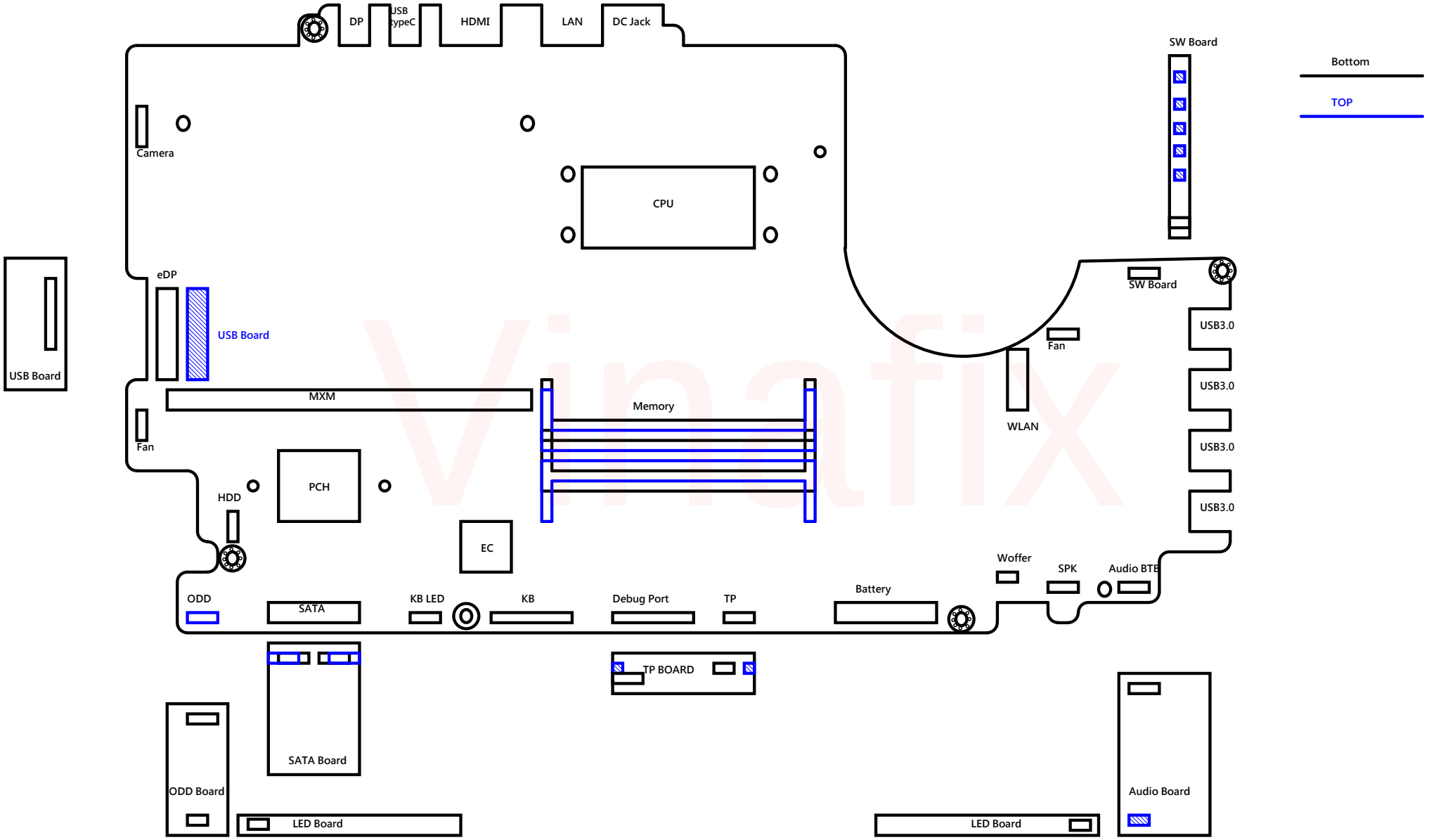
MS-1782 Board View



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