MS-7592

Version 5.2

CPU:

Intel Conroe (95W Dual core)

System Chipset:

Intel G41 - MCH (North Bridge)
Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI
HD --VT1708S
LPC Super I/O -- F718829G
LAN Atheros AR8132M co-lay AR8131M
CLOCK -- RTM875-605

Main Memory:

DDR III *2 (Max 4GB)

Expansion Slots:

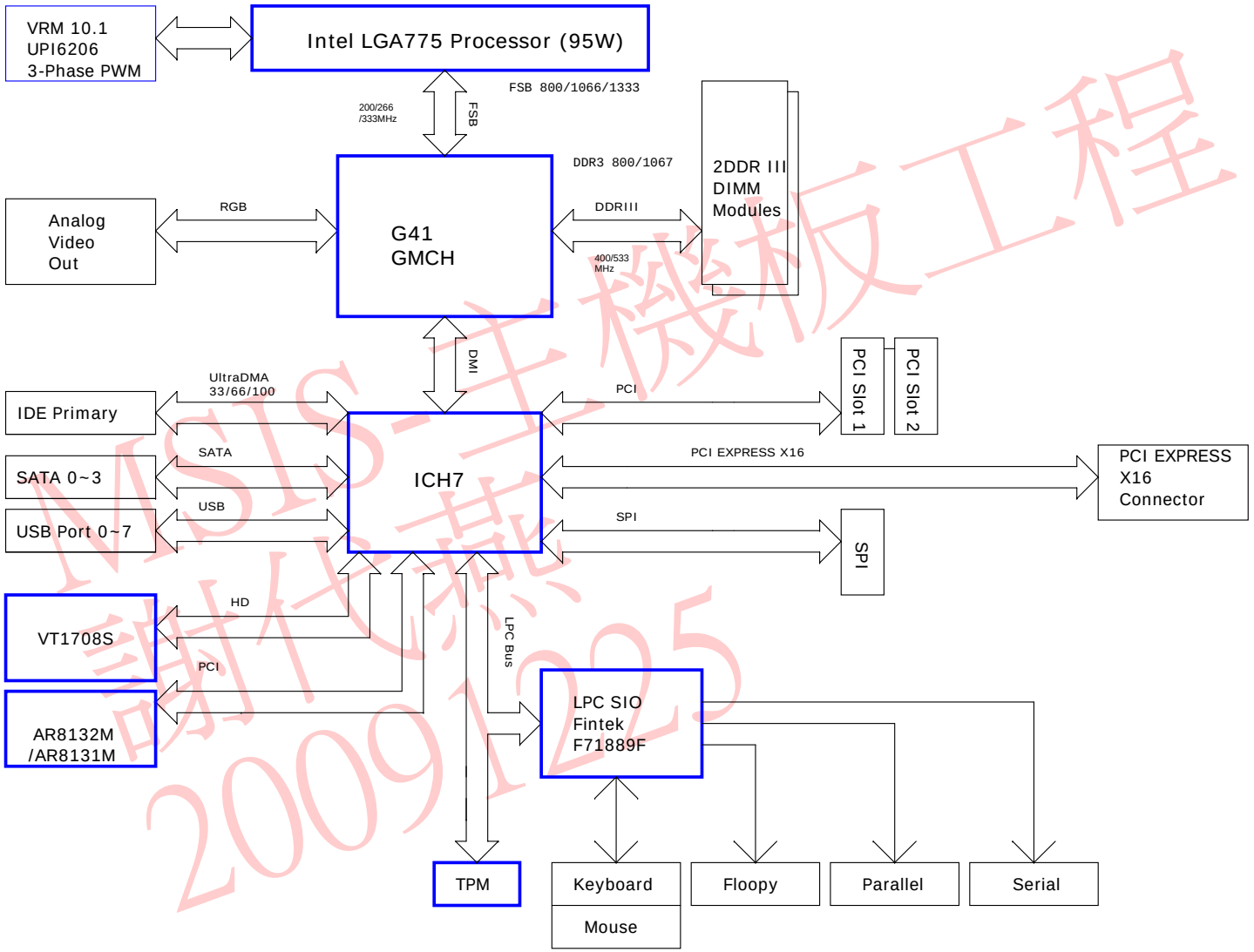
PCI2.3 SLOT * 2

PCI EXPRESS X16 SLOT

ST PWM:

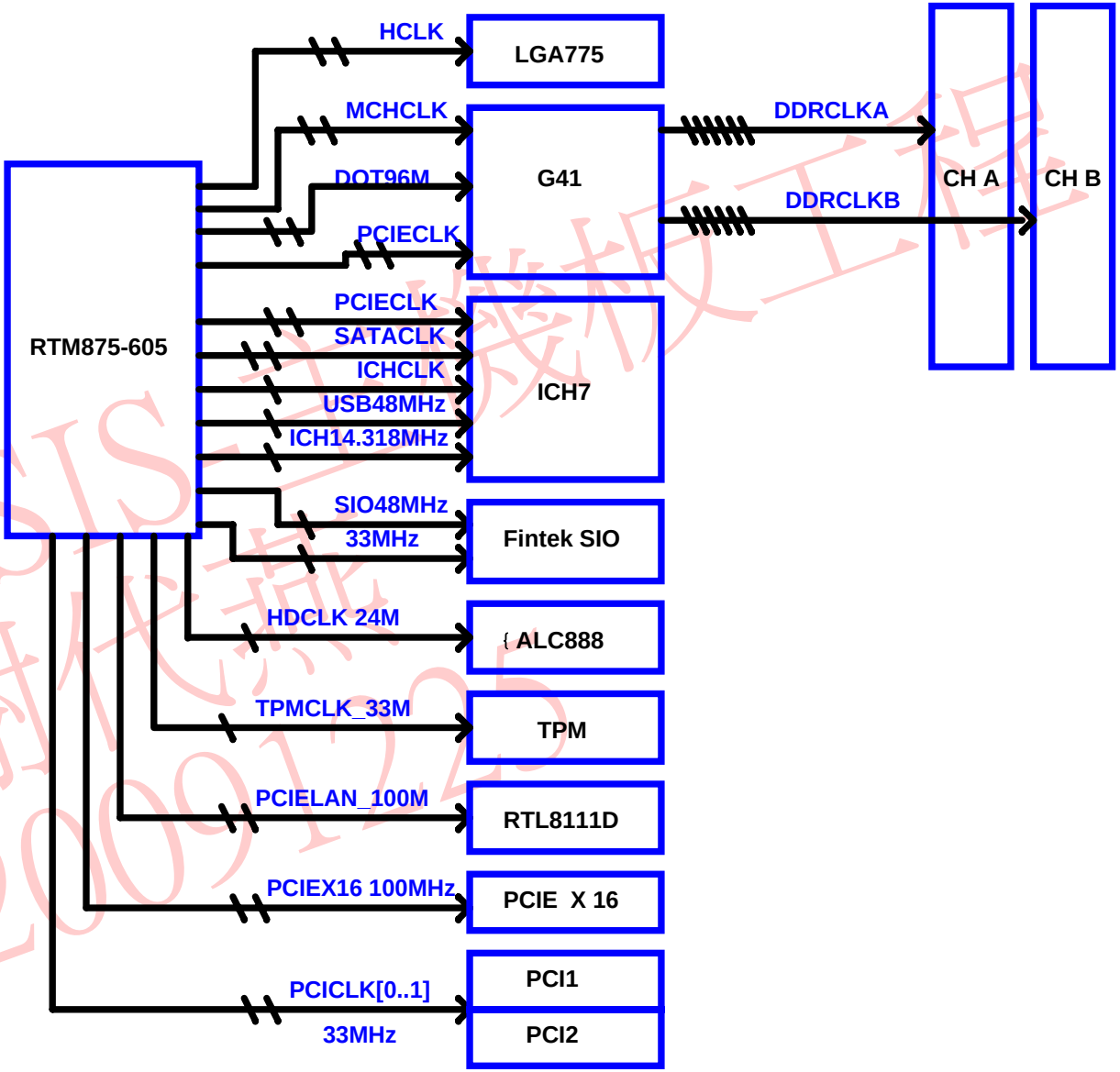
Controller: 3 PHASES

Block Diagram

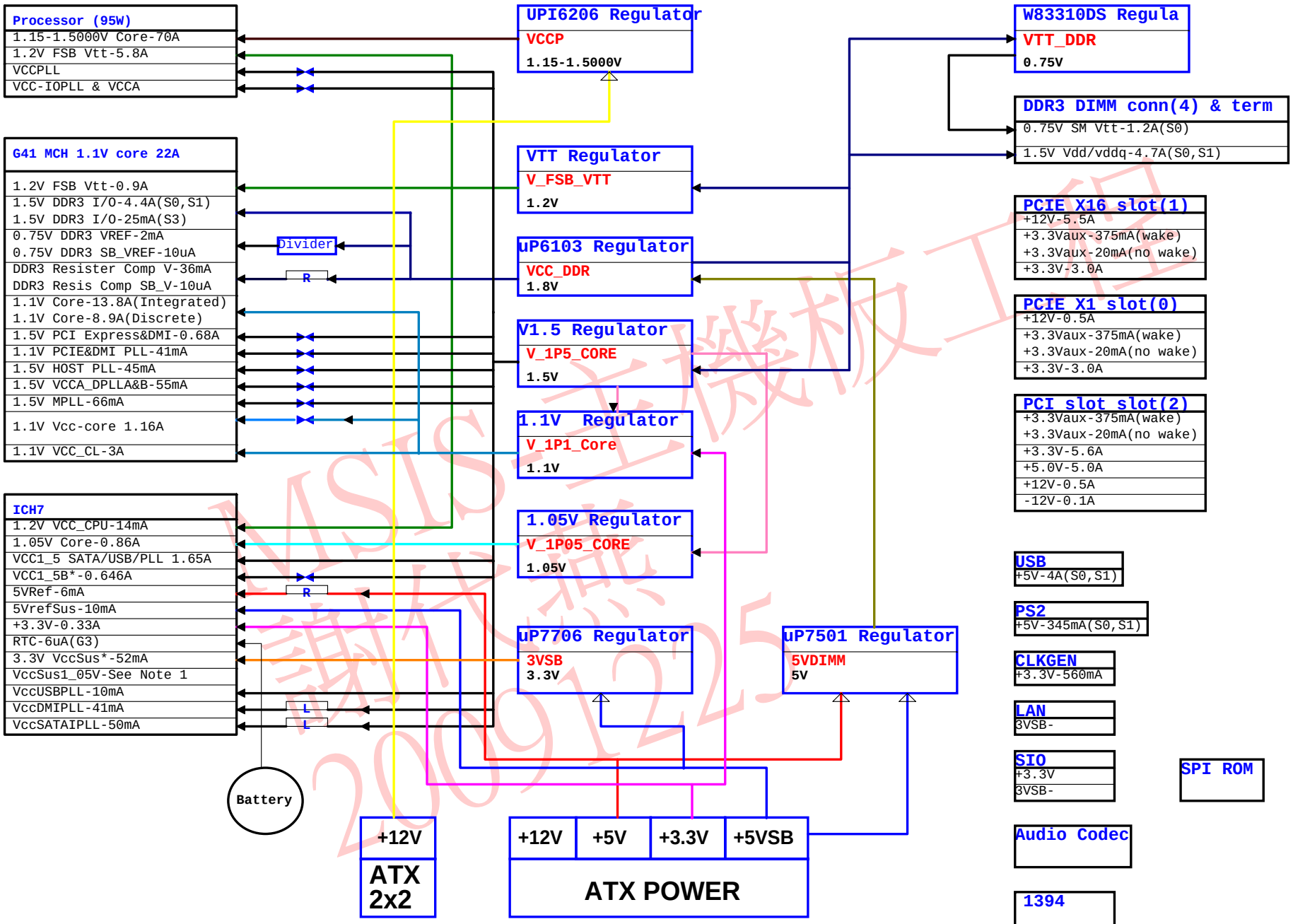


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7592	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 5.2
Date: Thursday, December 10, 2009	Sheet 2 of 33	

CLOCK MAP



MICRO-STAR INT'L CO.,LTD		
MS-7592		
Size: Custom	Document Description: CLOCK MAP	Rev: 5.2
Date: Thursday, December 10, 2009	Sheet 3 of 33	

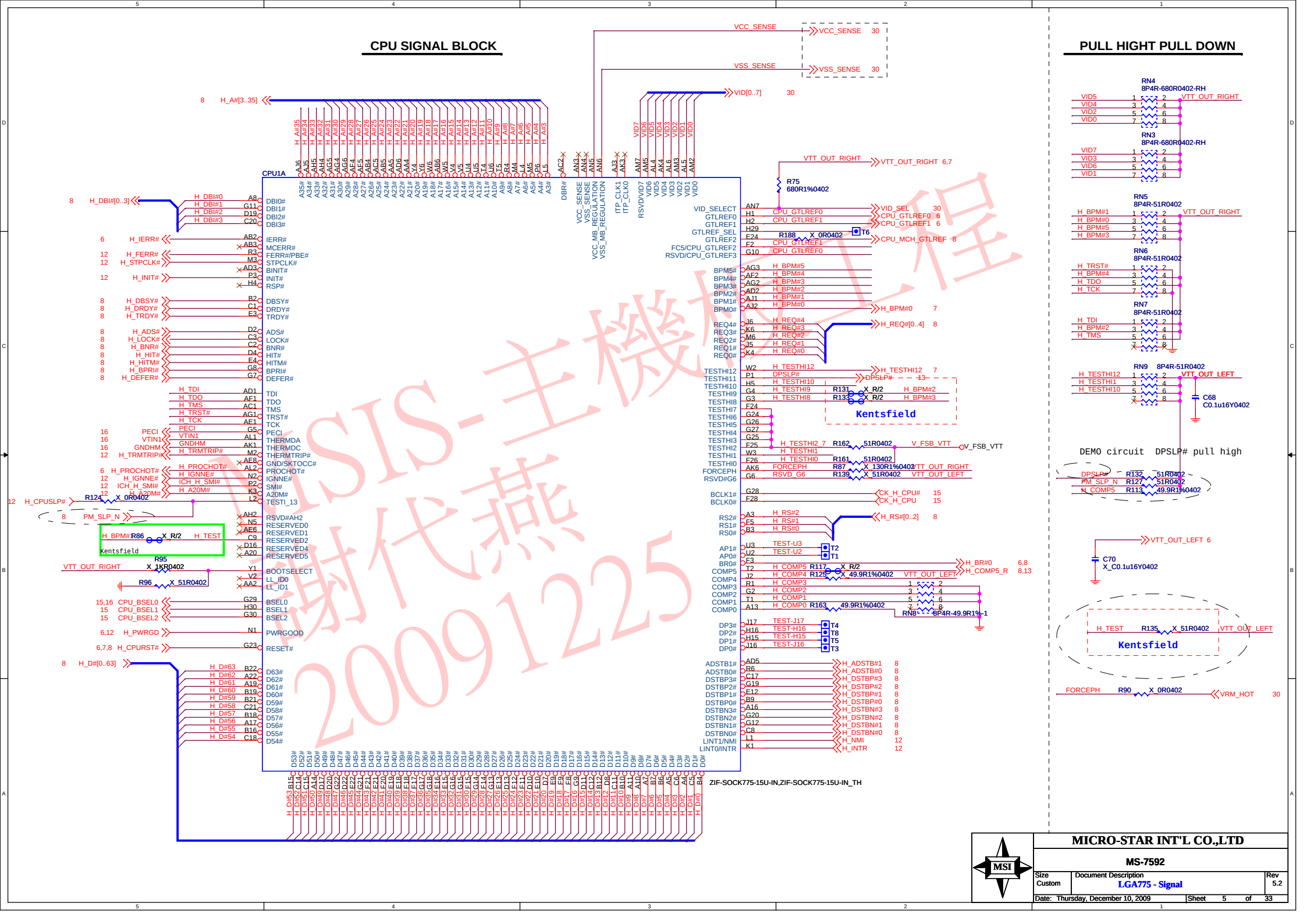


MICRO-STAR INT'L CO.,LTD

MS-7592

Size	Document Description	Rev
Custom	LGA775 - Signal	5.2

Date: Thursday, December 10, 2009 Sheet 4 of 33


CPU SIGNAL BLOCK
PULL HIGHT PULL DOWN
CPU1A
VCC_SENSE
VSS_SENSE
VID[0..7]
H_A#[3..35]
H_DBI#[0..3]
H_D#[0..63]
VTT_OUT_RIGHT
R75
680R1%0402
R188
X_0R0402
T6
CPU_MCH_GTLREF
H_BPM#0
H_REQ#[0..4]
H_TESTHI12
DPSLP#
H_TESTHI10
H_TESTHI9
H_TESTHI8
R131
R133
Kentsfield
H_TESTHI2
R162
51R0402
V_FSB_VTT
H_TESTHI1
H_TESTHI0
R161
FORCEPH
R87
X_130R1%0402
VTT_OUT_RIGHT
RSVD_G6
R139
X_51R0402
VTT_OUT_LEFT
CK_H_CPU#
CK_H_CPU
H_RS#[0..2]
TEST-U3
TEST-U2
T2
T1
H_BR#0
H_COMP5
R117
H_COMP5_R
H_COMP4
R125
X_49.9R1%0402
H_COMP3
H_COMP2
H_COMP1
H_COMP0
R163
49.9R1%0402
RN8
8P4R-49.9R1%-1
TEST-J17
TEST-H16
TEST-H15
TEST-J16
T4
T8
T5
T3
H_ADSTB#1
H_ADSTB#0
H_DSTBP#3
H_DSTBP#2
H_DSTBP#1
H_DSTBP#0
H_DSTBN#3
H_DSTBN#2
H_DSTBN#1
H_DSTBN#0
H_NMI
H_INTR
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
R124
X_0R0402
R86
X_R/2
H_TEST
R95
X_1KR0402
R96
X_51R0402
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
H_PWRGD
H_CPURST#
H_CPUSLP#
PM_SLP_N
H_PROCHOT#
H_IGNNE#
ICH_H_SMI#
H_A20M#
H_IERR#
H_FERR#
H_STPCLK#
H_INIT#
H_DBSY#
H_DRDY#
H_TRDY#
H_ADS#
H_LOCK#
H_BNR#
H_HIT#
H_HITM#
H_BPRI#
H_DEFER#
H_TDI
H_TDO
H_TMS
H_TRST#
H_TCK
PECI
VTIN1
GNDHM
H_TRMTRIP#
RN4
8P4R-680R0402-RH
RN3
8P4R-680R0402-RH
RN5
8P4R-51R0402
RN6
8P4R-51R0402
RN7
8P4R-51R0402
RN9
8P4R-51R0402
C68
C0.1u16Y0402
C70
X_C0.1u16Y0402
DEMO circuit DPSLP# pull high
R132
51R0402
R127
51R0402
R113
49.9R1%0402
H_TEST
R135
X_51R0402
VTT_OUT_LEFT
FORCEPH
R90
X_0R0402
VRM_HOT
MICRO-STAR INT'L CO.,LTD
MS-7592
LGA775 - Signal
Rev 5.2
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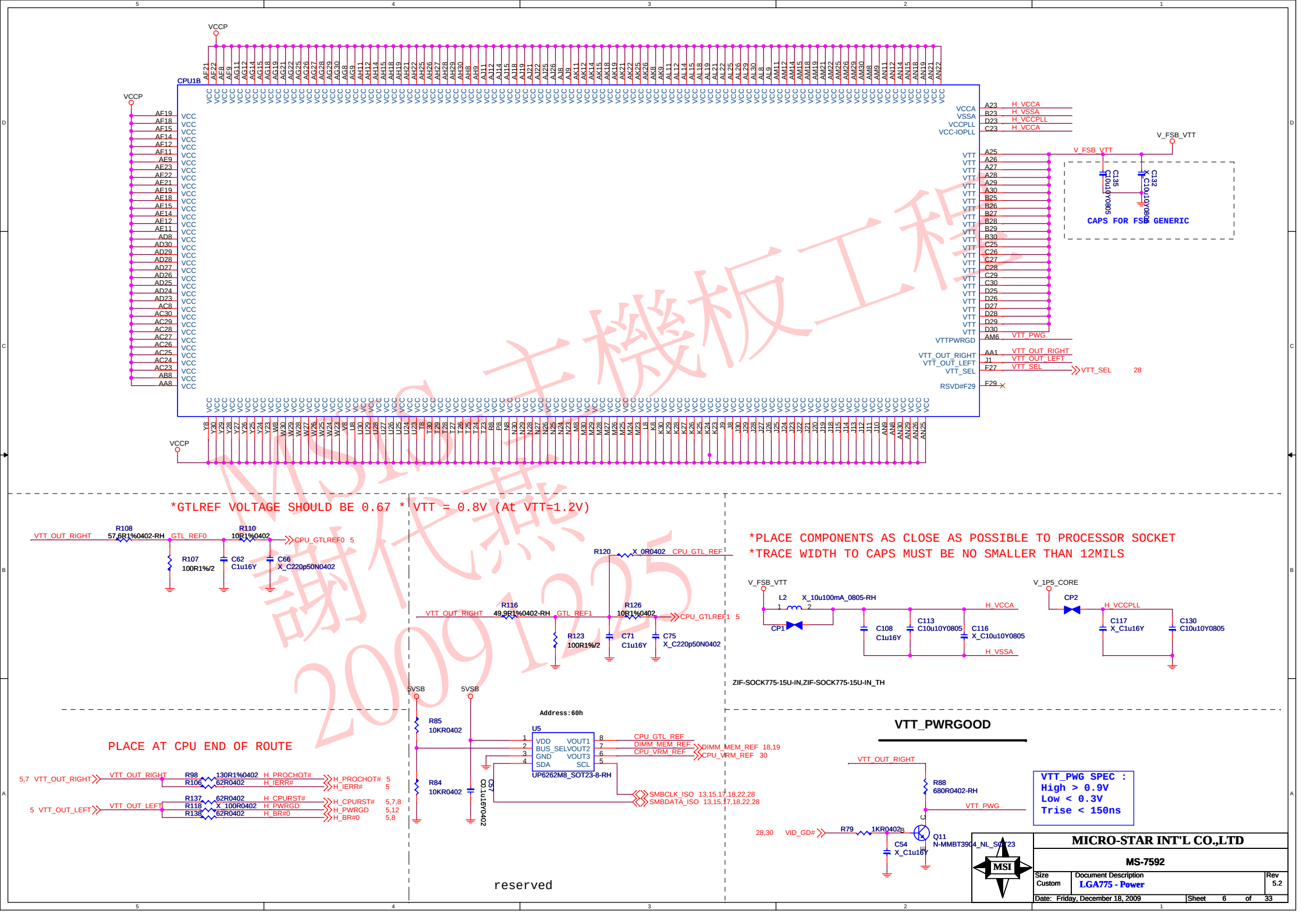
CPU1B
VCCP
VCCA
VSSA
VCCPLL
VCC-IOPLL
VTTPWRGD
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
RSVD#F29
H_VCCA
H_VSSA
H_VCCPLL
V_FSB_VTT
VTT_PWG
CAPS FOR FSB GENERIC
*GTLREF VOLTAGE SHOULD BE 0.67 * VTT = 0.8V (At VTT=1.2V)
R108 57.6R1%0402-RH
R110 10R1%0402
R107 100R1%/2
C62 C1u16Y
C66 X_C220p50N0402
CPU_GTLREF0
R120 X_0R0402
CPU_GTL_REF
R116 49.9R1%0402-RH
R126 10R1%0402
R123 100R1%/2
C71 C1u16Y
C75 X_C220p50N0402
CPU_GTLREF1
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS
L2 X_10u100mA_0805-RH
CP1
C108 C1u16Y
C113 C10u10Y0805
C116 X_C10u10Y0805
CP2
C117 X_C1u16Y
C130 C10u10Y0805
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
PLACE AT CPU END OF ROUTE
R98 130R1%0402
R106 62R0402
R137 62R0402
R118 X_100R0402
R138 62R0402
H_PROCHOT#
H_IERR#
H_CPURST#
H_PWRGD
H_BR#0
5VSB
R85 10KR0402
R84 10KR0402
C57 C0.1u16Y0402
Address:60h
U5
UP6262M8_SOT23-8-RH
DIMM_MEM_REF
CPU_VRM_REF
SMBCLK_ISO
SMBDATA_ISO
reserved
VTT_PWRGOOD
R88 680R0402-RH
R79 1KR0402
C54 X_C1u16Y
Q11 N-MMBT3904_NL_SOT23
VID_GD#
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
MICRO-STAR INT'L CO.,LTD
MS-7592
LGA775 - Power
Rev 5.2
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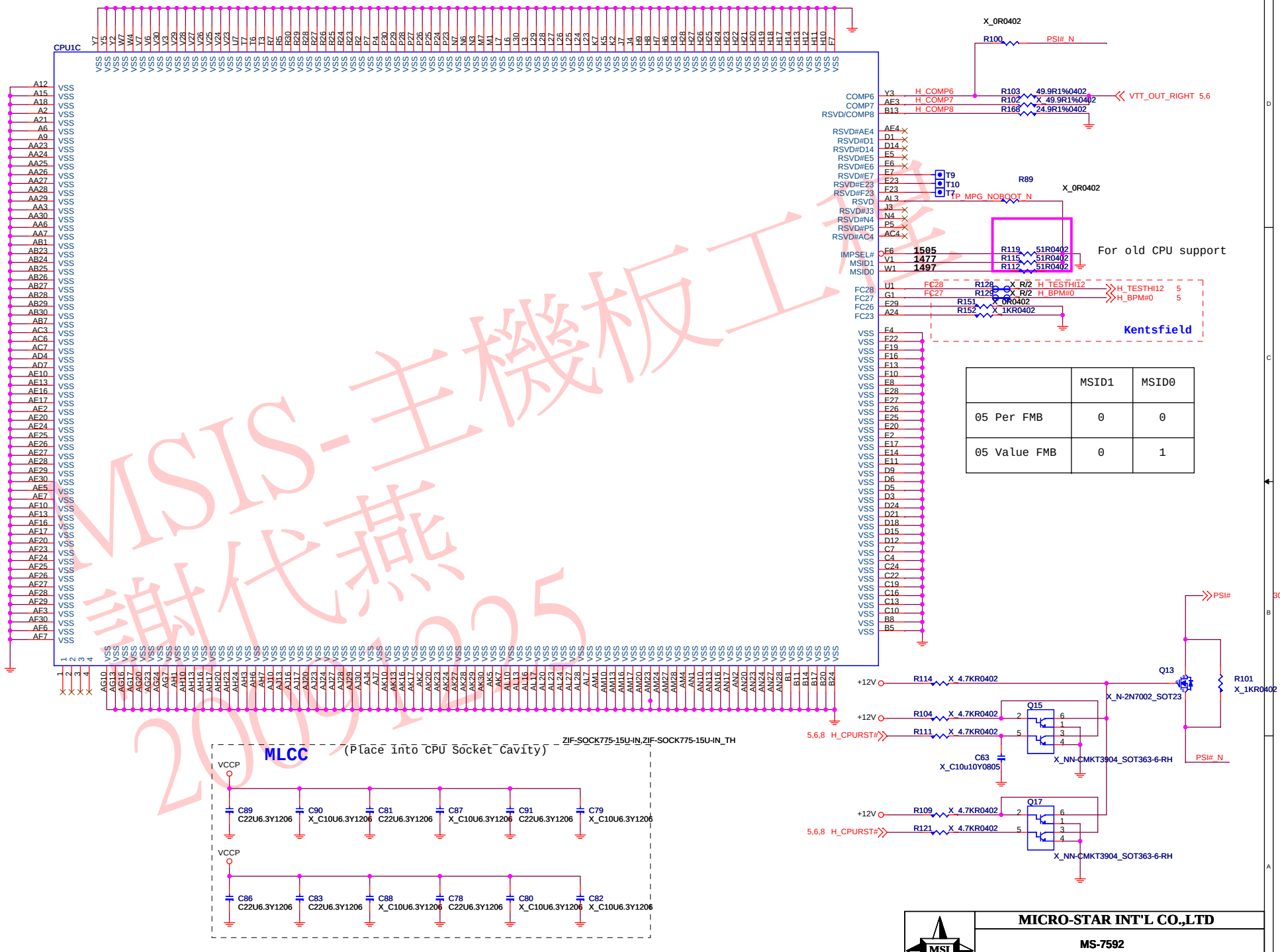

	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1

MICRO-STAR INT'L CO.,LTD

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Custom	LGA775 - GND	5.2

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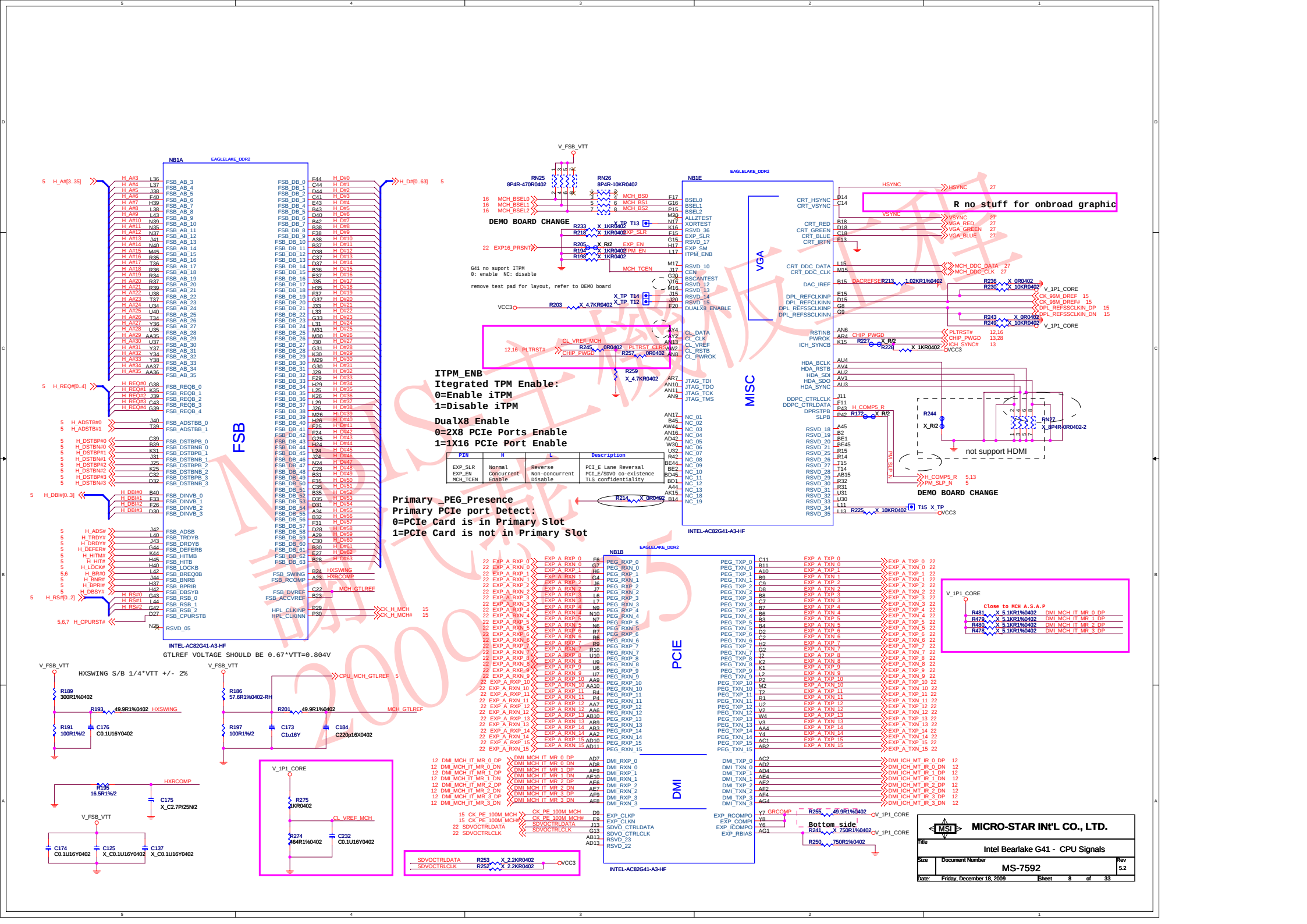
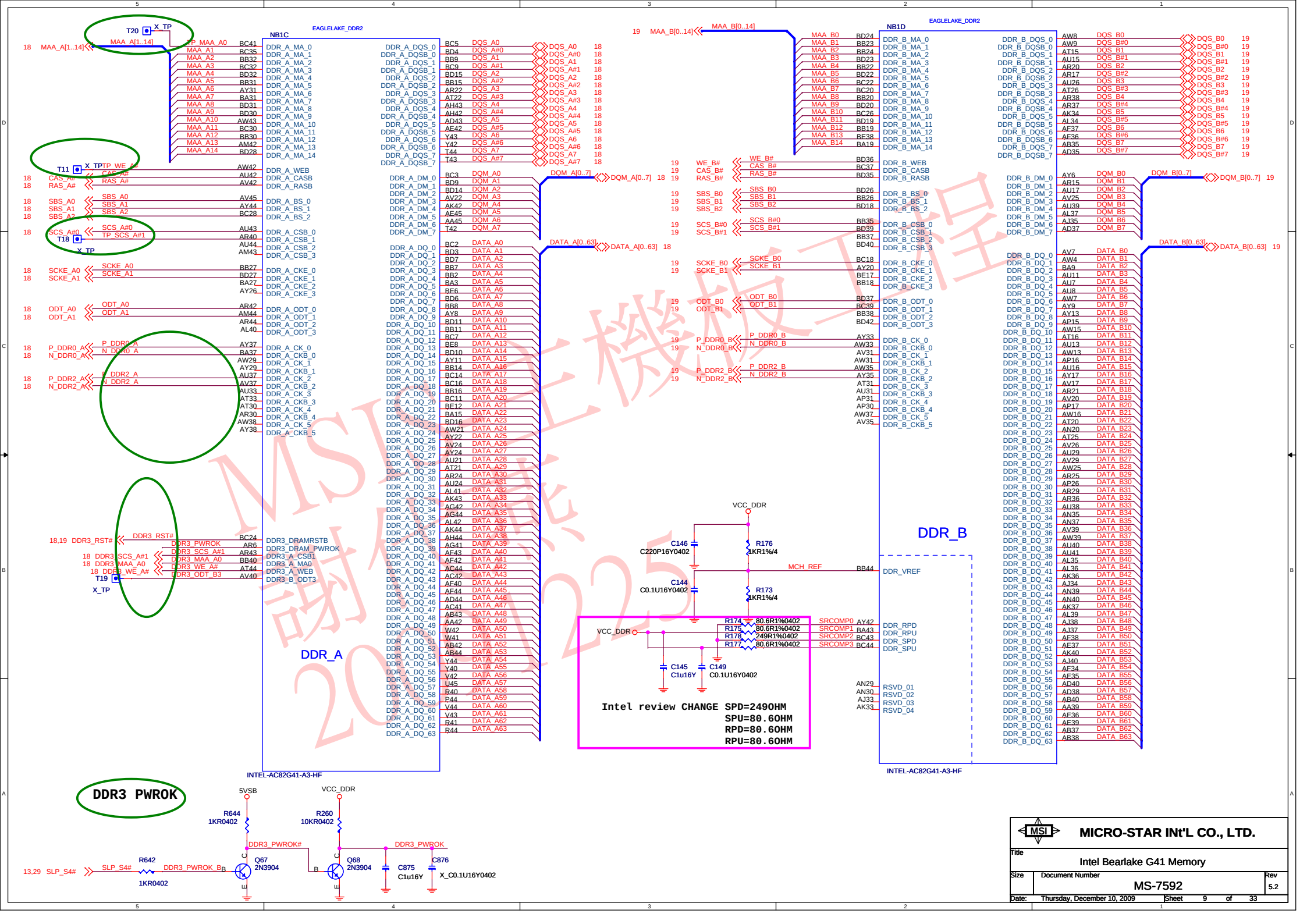
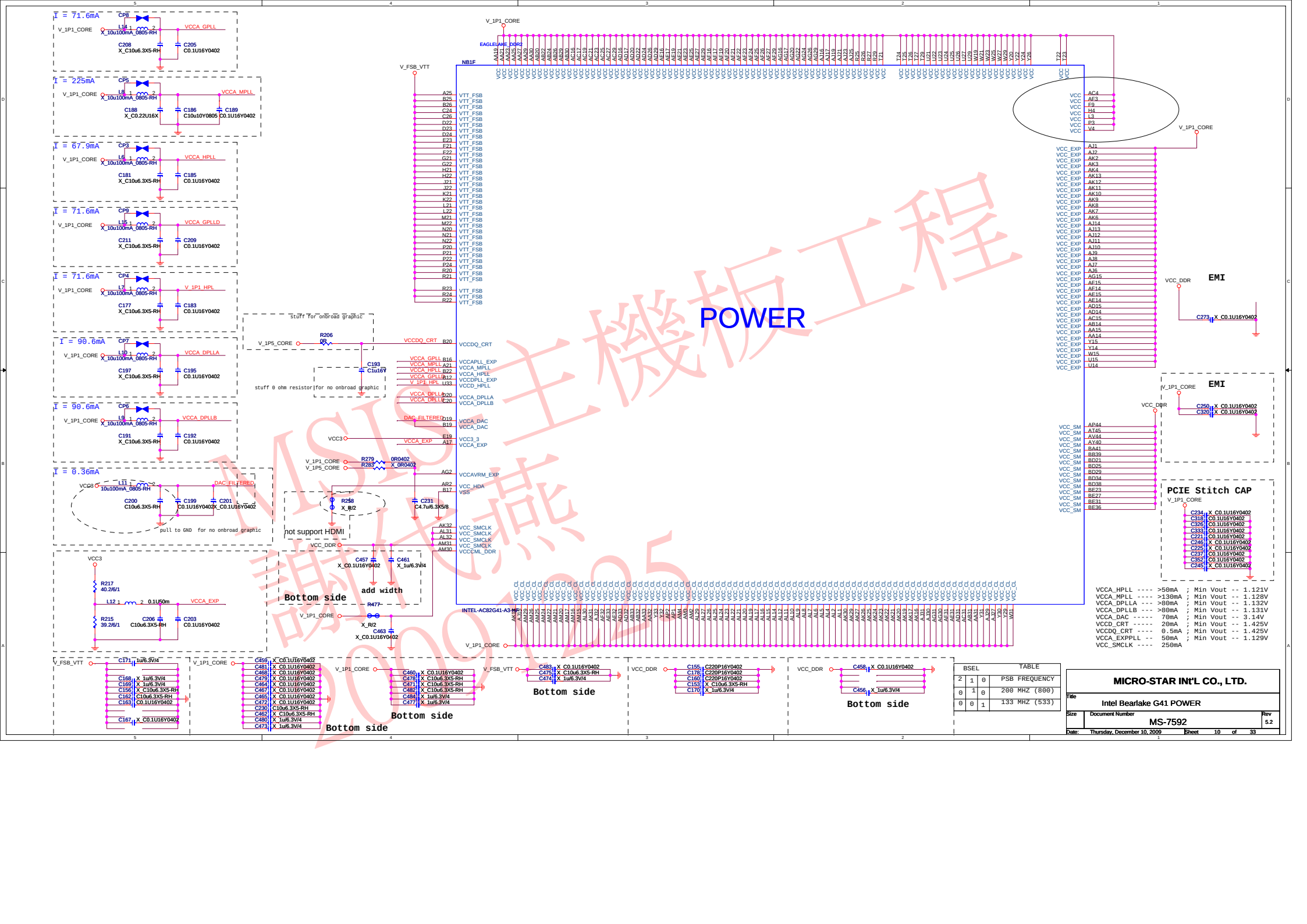

NB1A
EAGLELAKE_DDR2
FSB
INTEL-AC82G41-A3-HF
GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.804V
HXSWING S/B 1/4*VTT +/- 2%
V_FSB_VTT
DEMO BOARD CHANGE
ITPM_ENB
Itegrated TPM Enable:
0=Enable iTPM
1=Disable iTPM
DualX8_Enable
0=2X8 PCIe Ports Enable
1=1X16 PCIe Port Enable
Primary _PEG_Presence
Primary PCIe port Detect:
0=PCIe Card is in Primary Slot
1=PCIe Card is not in Primary Slot
NB1E
MISC
VGA
NB1B
PCIE
DMI
R no stuff for onbroad graphic
not support HDMI
Close to MCH A.S.A.P
Bottom side
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G41 - CPU Signals
MS-7592
Friday, December 18, 2009


NB1C
EAGLELAKE_DDR2
NB1D
EAGLELAKE_DDR2
DDR_A
DDR_B
INTEL-AC82G41-A3-HF
INTEL-AC82G41-A3-HF
Intel review CHANGE SPD=249OHM
SPU=80.6OHM
RPD=80.6OHM
RPU=80.6OHM
DDR3 PWROK
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G41 Memory
MS-7592
Thursday, December 10, 2009


POWER
I = 71.6mA
I = 225mA
I = 67.9mA
I = 71.6mA
I = 71.6mA
I = 90.6mA
I = 90.6mA
I = 0.36mA
V_1P1_CORE
V_FSB_VTT
V_1P5_CORE
VCC3
VCC_DDR
EAGLELAKE_DDR2
NB1F
INTEL-AC82G41-A3-HF
stuff for onbroad graphic
stuff 0 ohm resistor for no onbroad graphic
not support HDMI
add width
Bottom side
EMI
PCIE Stitch CAP
VCCA_HPLL ---- >50mA ; Min Vout -- 1.121V
VCCA_MPLL ---- >130mA ; Min Vout -- 1.128V
VCCA_DPLLA --- >80mA ; Min Vout -- 1.132V
VCCA_DPLLB --- >80mA ; Min Vout -- 1.131V
VCCA_DAC ----- 70mA ; Min Vout -- 3.14V
VCCD_CRT ----- 20mA ; Min Vout -- 1.425V
VCCDQ_CRT ---- 0.5mA ; Min Vout -- 1.425V
VCCA_EXPPLL -- 50mA ; Min Vout -- 1.129V
VCC_SMCLK ---- 250mA
BSEL TABLE
2 1 0 PSB FREQUENCY
0 1 0 200 MHZ (800)
0 0 1 133 MHZ (533)
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G41 POWER
MS-7592
Rev 5.2
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MSI	MICRO-STAR INt'L CO., LTD.		
Title	Intel Bearlake G41 GND		
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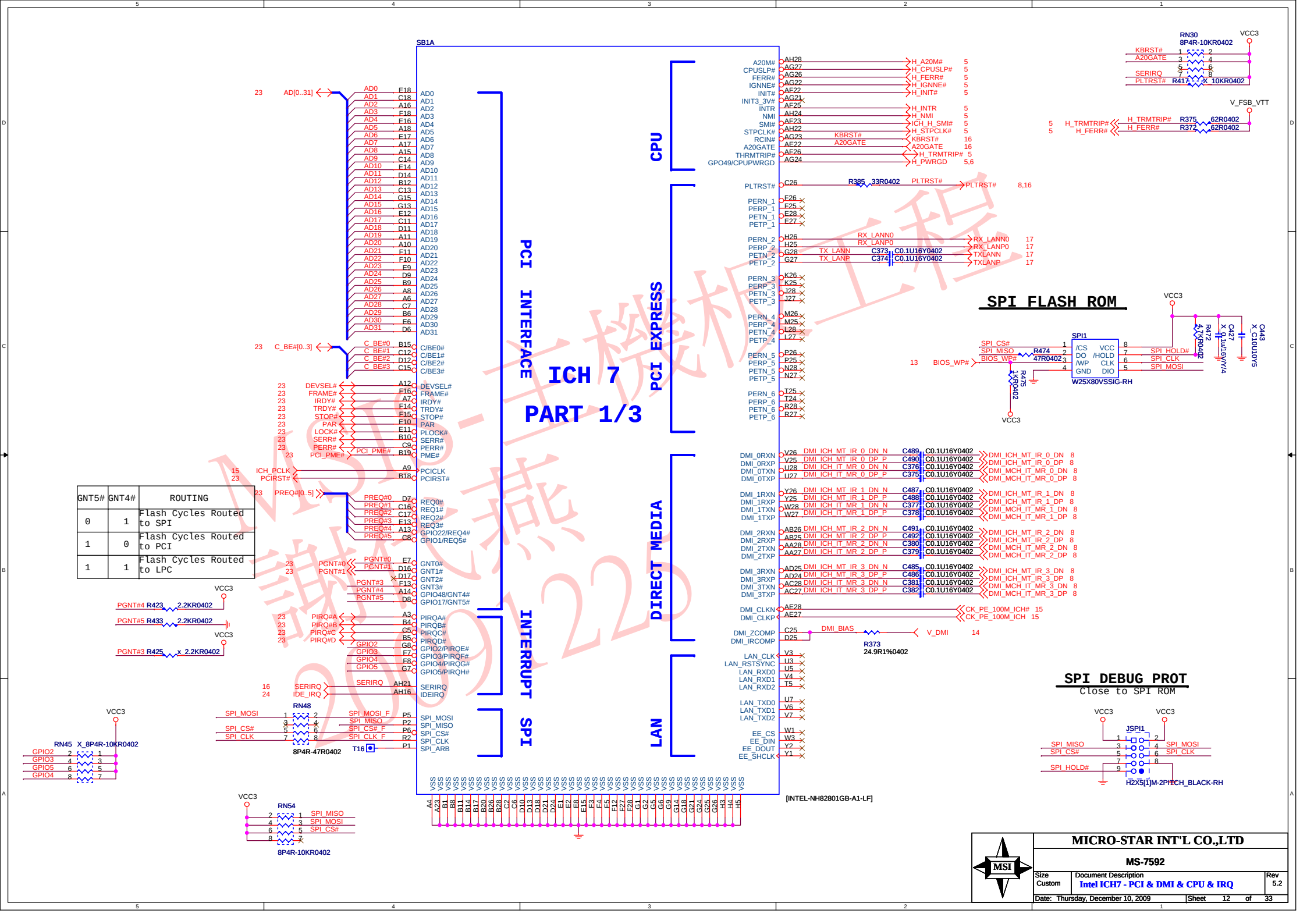
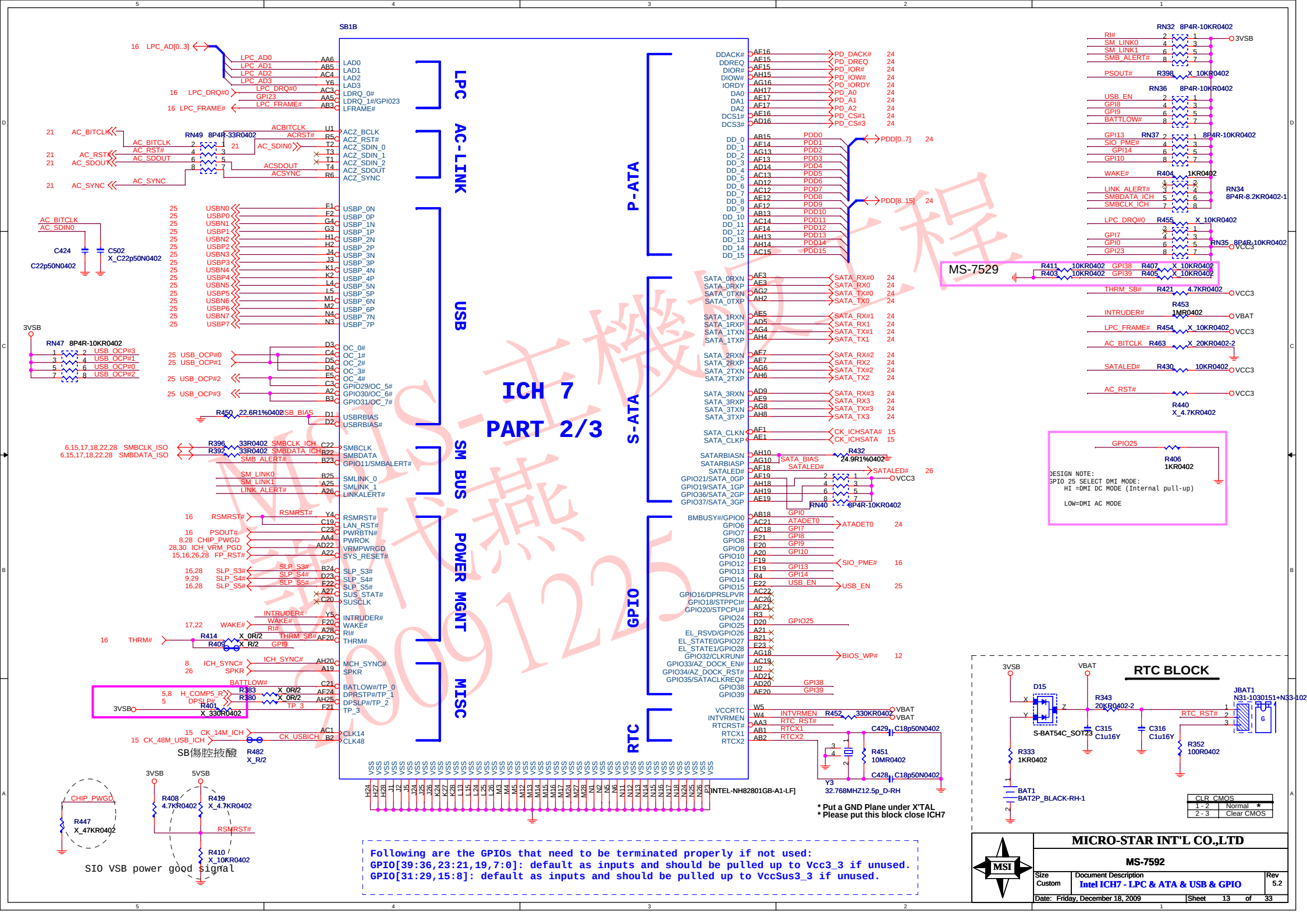
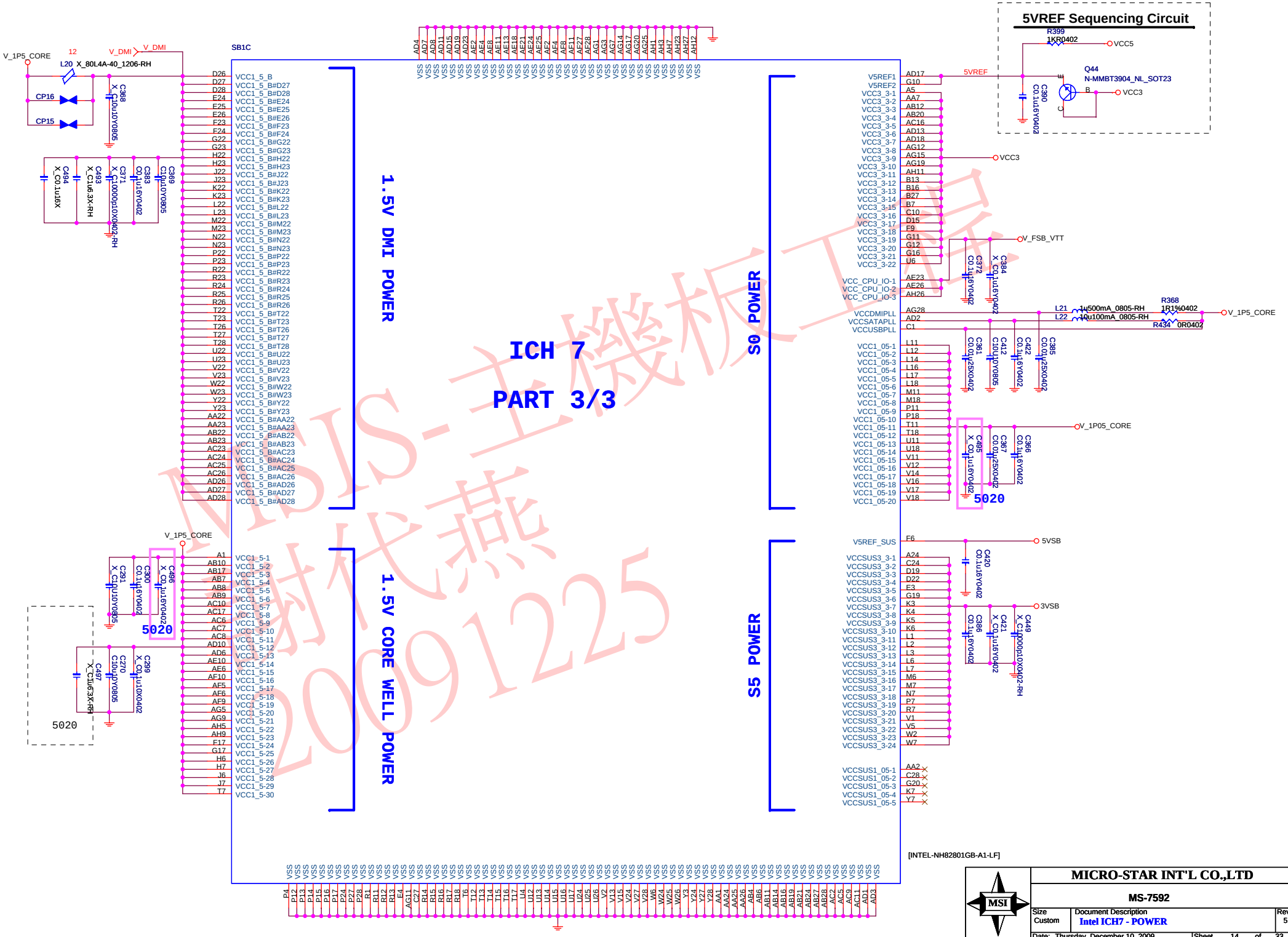


GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC


ICH 7
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
SB1B
MS-7529
RTC BLOCK
SB傷腔掖醱
SIO VSB power good signal
[INTEL-NH82801GB-A1-LF]
* Put a GND Plane under X'TAL
* Please put this block close ICH7
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
MICRO-STAR INT'L CO.,LTD
MS-7592
Intel ICH7 - LPC & ATA & USB & GPIO
Date: Friday, December 18, 2009
Sheet 13 of 33
Rev 5.2


ICH 7
PART 3/3
1.5V DMI POWER
1.5V CORE WELL POWER
S0 POWER
S5 POWER
SB1C
5VREF Sequencing Circuit
[INTEL-NH82801GB-A1-LF]
MICRO-STAR INT'L CO.,LTD
MS-7592
Intel ICH7 - POWER
Rev 5.2
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Clock Generator - RTM875T-605

U12

RTM875T-605

TSSOP56

RTM875T-605-VD-GR_TSSOP56-RH

RN28 8P4R-33R0402

Close to chip

L18 X_10u125mA_0805-RH-1

CP11 X_Copper

CKVDD

C284 X_1u16Y0402 C288 X_1u16Y0402 C240 C_0.1u16Y0402 C256 C_0.1u16Y0402 C255 C_0.1u16Y0402 C279 X_1u16Y0402 C258 C_0.1u16Y0402 C278 C_0.1u16Y0402 C257 X_1u16Y0402 C281 C_0.1u16Y0402 C287 X_1u16Y0402

STRAPPING RESISTOR

	0	1
TME_OC	Normal Run	No Overclocking
SRC5_EN	Pin29/30 is PCI STOP/CPU STOP	Pin29/30 is SRC 5
27M_SEL	Pin17/18 is SRC 1	Pin17/18 is 27MHz
ITP_EN	Pin38/39 is SRC 8	Pin38/39 is CPUITP

Close to chip

L17 X_10u125mA_0805-RH-1

CP10 X_Copper

Clock Generator Power Good Block

CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid

RTL demo board circuit: BSEL BIASING RES(cowork EMI 10P to GND)

For 400MHz CPU Support

X_SW-DIPP3-RH

MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: CLK-RTM 875T-605
Rev: 5.2	
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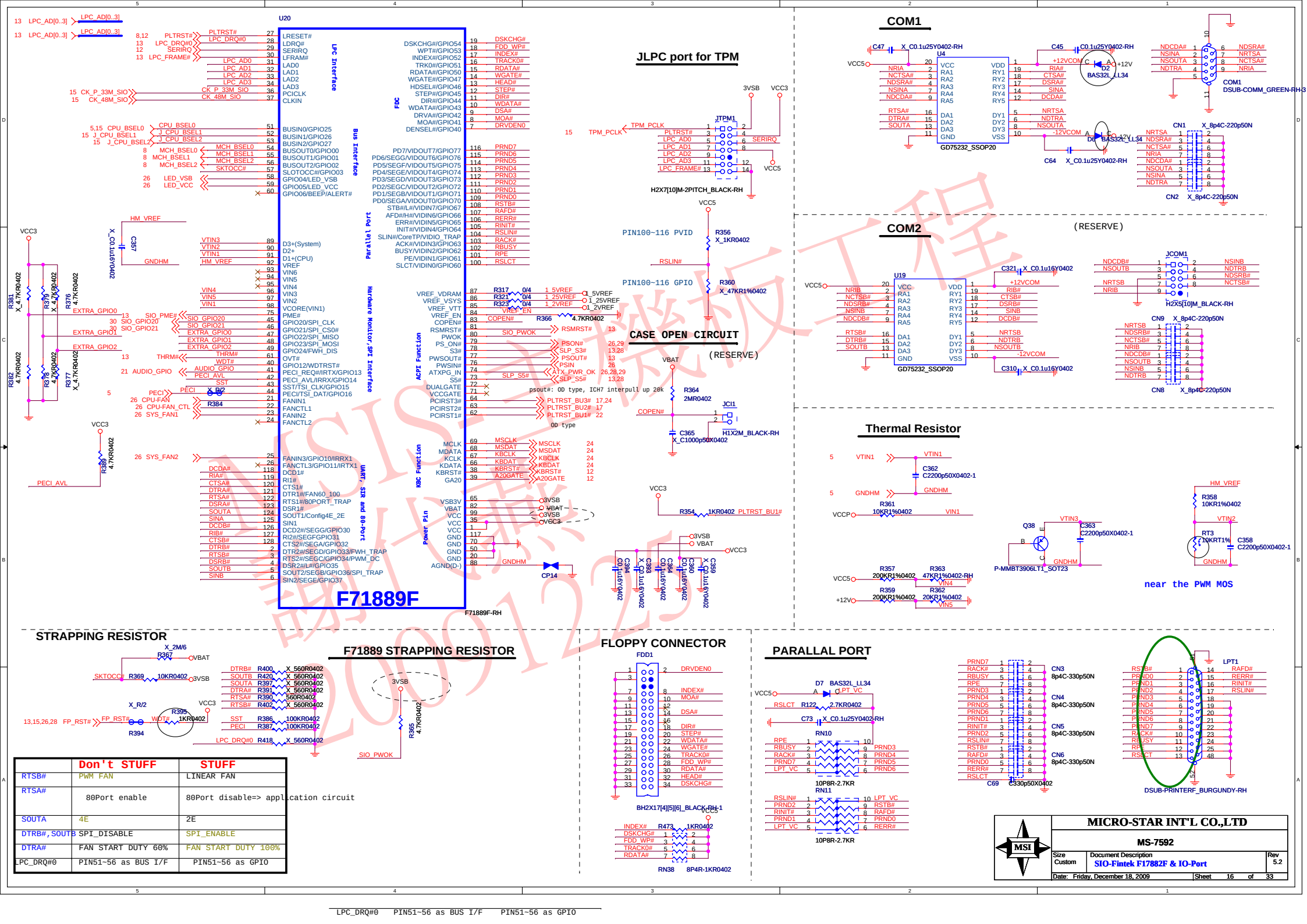
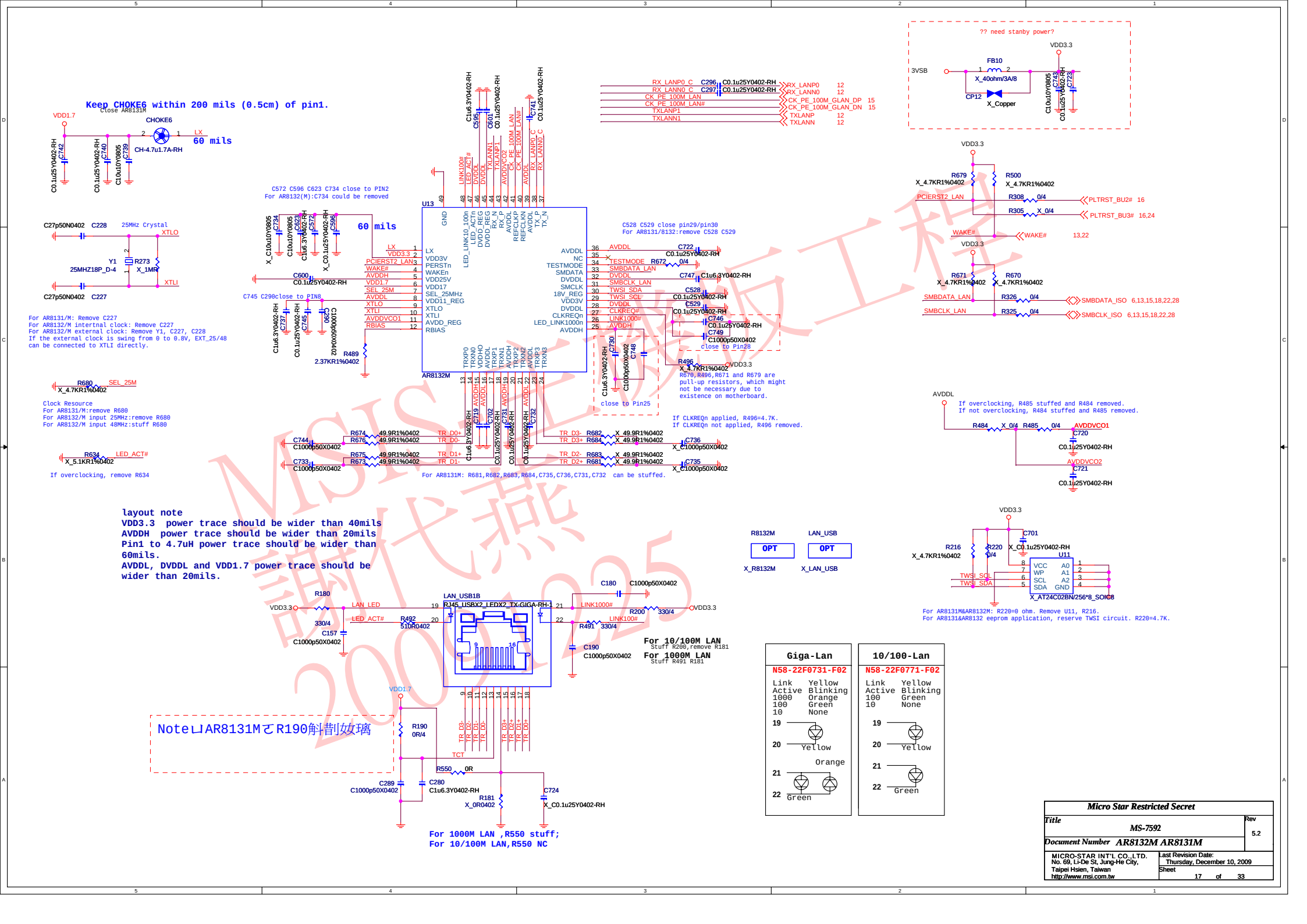


	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80Port enable	80Port disable=> application circuit
SOUTA	4E	2E
DTRB#, SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LPC_DRQ#0	PIN51~56 as BUS I/F	PIN51~56 as GPIO

LPC_DRQ#0 PIN51~56 as BUS I/F PIN51~56 as GPIO


Keep CHOKE6 within 200 mils (0.5cm) of pin1.
Close AR8131M
CHOKE6
60 mils
CH-4.7u1.7A-RH
25MHz Crystal
25MHZ18P_D-4
For AR8131/M: Remove C227
For AR8132/M internal clock: Remove C227
For AR8132/M external clock: Remove Y1, C227, C228
If the external clock is swing from 0 to 0.8V, EXT_25/48 can be connected to XTLI directly.
C572 C596 C623 C734 close to PIN2
For AR8132(M):C734 could be removed
C528 C529 close pin29/pin30
For AR8131/8132:remove C528 C529
R680 SEL_25M
Clock Resource
For AR8131/M:remove R680
For AR8132/M input 25MHz:remove R680
For AR8132/M input 48MHz:stuff R680
R634 LED_ACT#
If overclocking, remove R634
AR8132M
C745 C290close to PIN8
close to Pin25
close to Pin28
R489 2.37KR1%0402
R496 X_4.7KR1%0402
R670,R496,R671 and R679 are pull-up resistors, which might not be necessary due to existence on motherboard.
If CLKREQn applied, R496=4.7K.
If CLKREQn not applied, R496 removed.
For AR8131M: R681,R682,R683,R684,C735,C736,C731,C732 can be stuffed.
?? need stanby power?
FB10
X_40ohm/3A/8
CP12
X_Copper
R679 X_4.7KR1%0402
R500 X_4.7KR1%0402
R671 X_4.7KR1%0402
R670 X_4.7KR1%0402
If overclocking, R485 stuffed and R484 removed.
If not overclocking, R484 stuffed and R485 removed.
R8132M
LAN_USB
OPT
X_R8132M
X_LAN_USB
X_AT24C02BN/256*8_SOIC8
For AR8131M&AR8132M: R220=0 ohm. Remove U11, R216.
For AR8131&AR8132 eeprom application, reserve TWSI circuit. R220=4.7K.
layout note
VDD3.3 power trace should be wider than 40mils
AVDDH power trace should be wider than 20mils
Pin1 to 4.7uH power trace should be wider than 60mils.
AVDDL, DVDDL and VDD1.7 power trace should be wider than 20mils.
LAN_USB1B
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
For 10/100M LAN
Stuff R200,remove R181
For 1000M LAN
Stuff R491 R181
Note：AR8131M之R190斛削妓璃
For 1000M LAN ,R550 stuff;
For 10/100M LAN,R550 NC
Giga-Lan
N58-22F0731-F02
Link Yellow
Active Blinking
1000 Orange
100 Green
10 None
10/100-Lan
N58-22F0771-F02
Link Yellow
Active Blinking
100 Green
10 None
Micro Star Restricted Secret
Title
MS-7592
Rev
5.2
Document Number
AR8132M AR8131M
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
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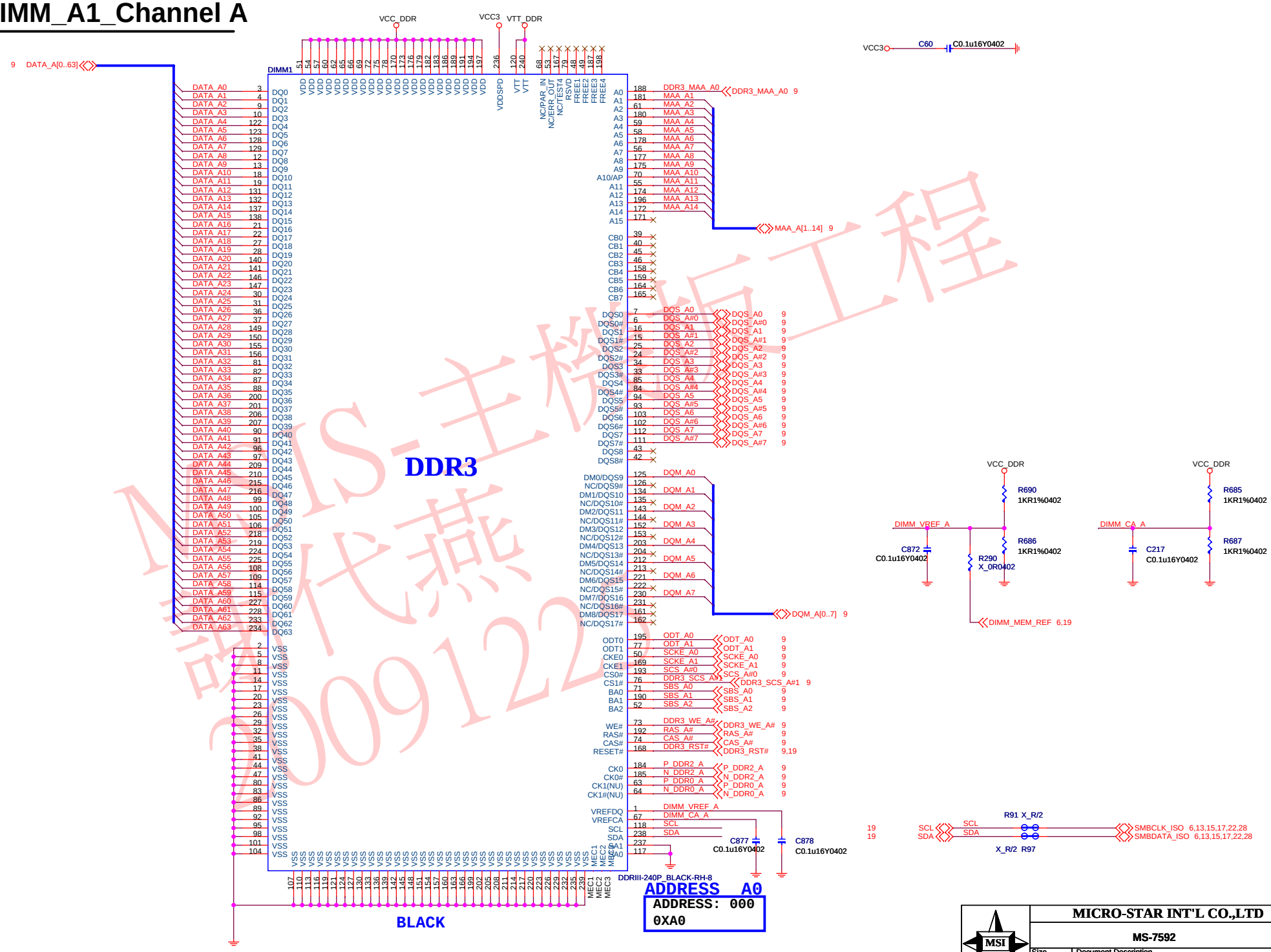
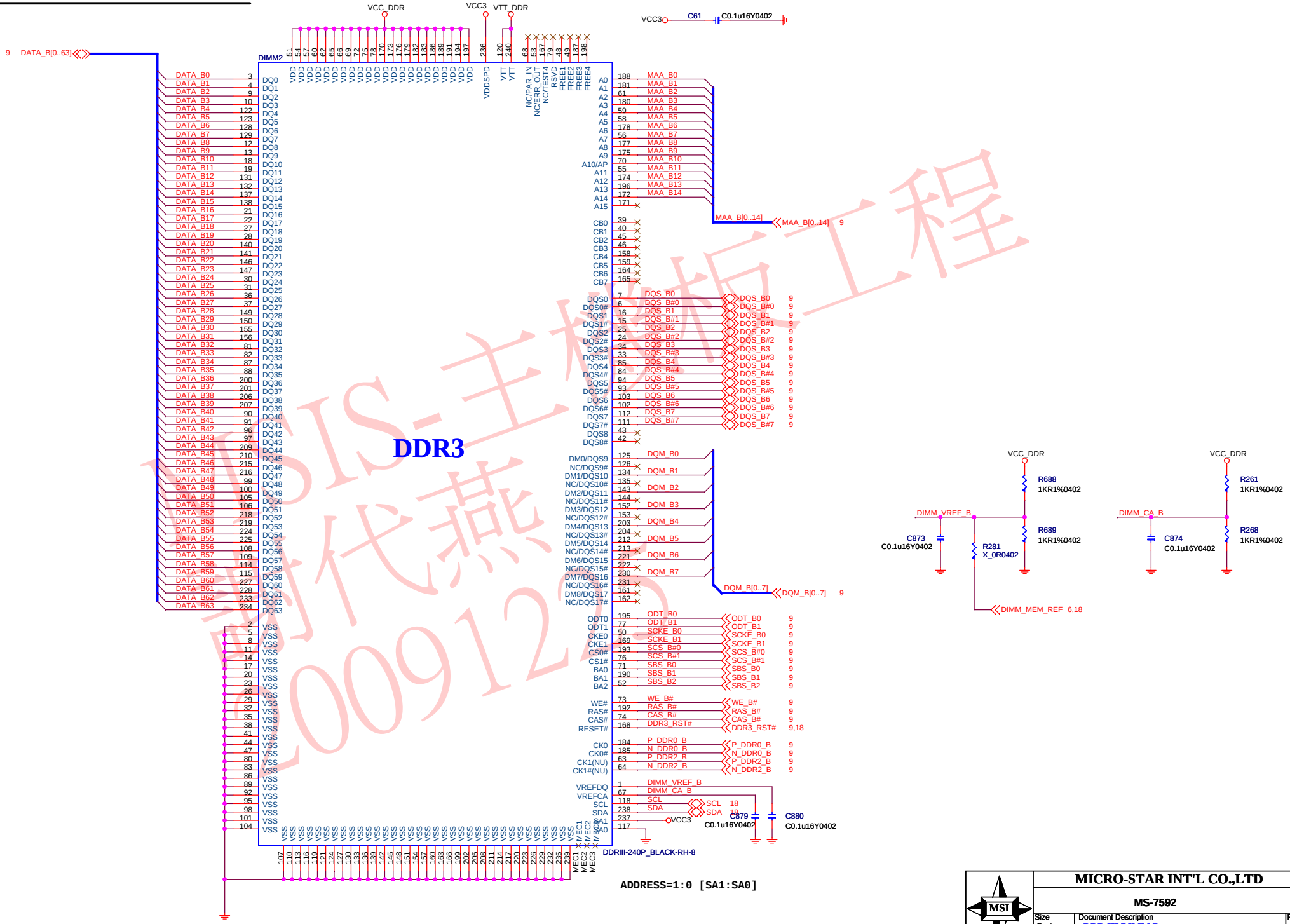
DDRII DIMM_A1_Channel A

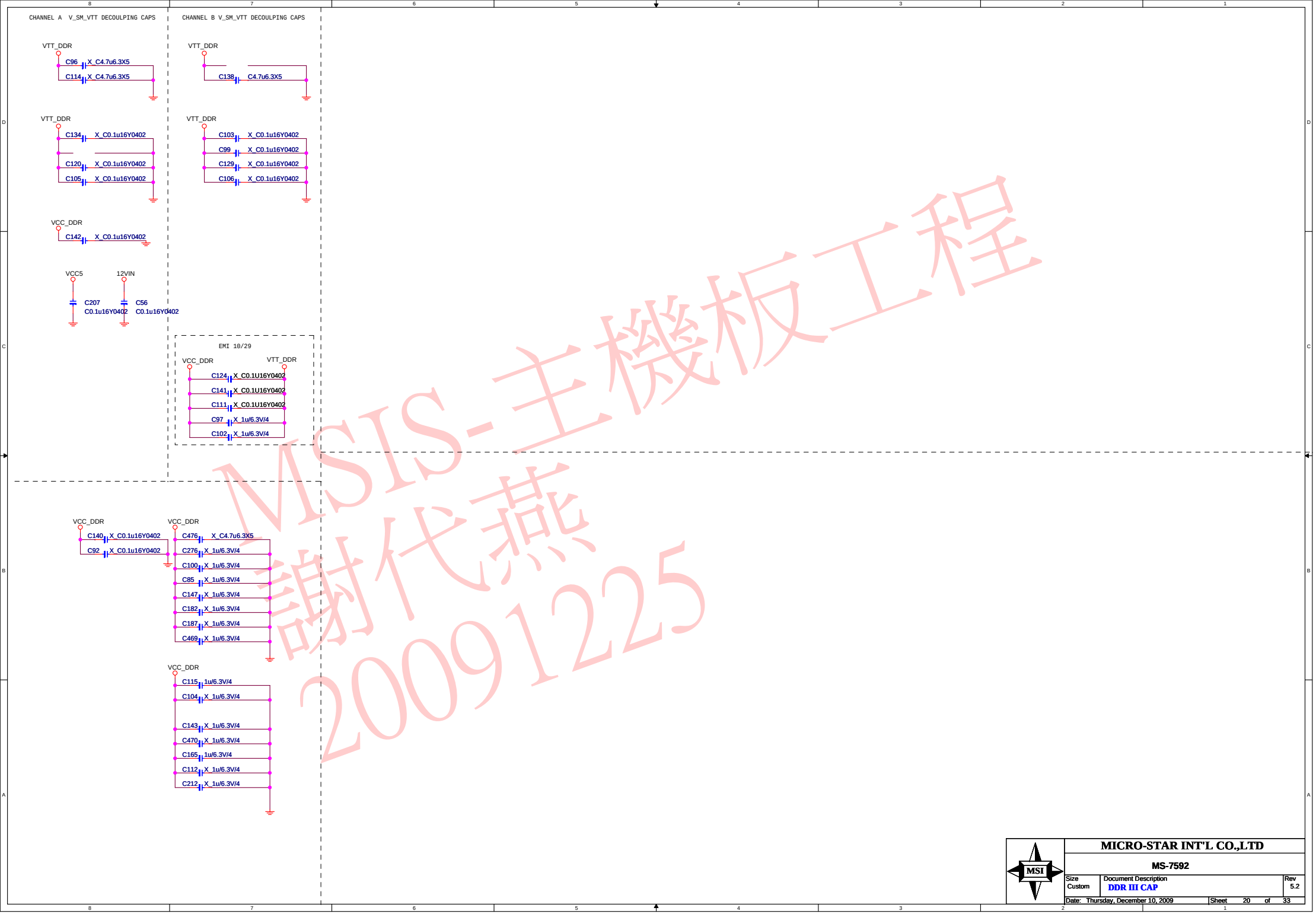


MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: DDR III DIMM A
Rev: 5.2	
Date: Thursday, December 10, 2009	Sheet 18 of 33

DDRII DIMM_B1_Channel B



MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: DDR III DIMM B
Rev: 5.2	
Date: Thursday, December 10, 2009	Sheet 19 of 33



MICRO-STAR INT'L CO.,LTD

MS-7592

Size	Document Description	Rev
Custom	DDR III CAP	5.2

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VT1708S CODEC

FOR 6 Port

FOR 6 Port

Trace Width 20mils.

modify

U22 VT1708S

CD/IN HEADERS

JCD1 BH1X4_BLACK-RH

RN53 8P4R-330R0402

RN51 8P4R-100KR0402

Azalia Front Audio Connector

D23 S-BAT54A_SOT23

D22 S-BAT54A_SOT23

RN50 8P4R-3.3KR0402

RN55 8P4R-22R

JAUD1 H2X5[8]M_BLACK-RH

CN10 8p4C-100p50N

Place those component close to audio connector.

VT1708S JACK

RN58 8P4R-75R

RN57 8P4R-75R

RN56 8P4R-75R

AUDIO1A (Upper)

X_JACK-AUDIOX6-26P_L-pbg_R-obl

AUDIO1B(Middle)

AUDIO1C (Down)

100P

AUDIO2A (Upper)

JACK-AUDIOX6-26P_L-pbg_R-obl

AUDIO2B(Middle)

AUDIO2C (Down)

VT1708S

OPT

X_VT1708S

FOR 6 Port

VT1708S JACK DETECT

SPDIF OUT

JSP1 BH1X3_BLACK-RH

For EMI

AUDIO CODE REGULATORS

U23 LT1087S_SOT89

Trace Width 30mils.

MICRO-STAR INT'L CO.,LTD

MS-7592

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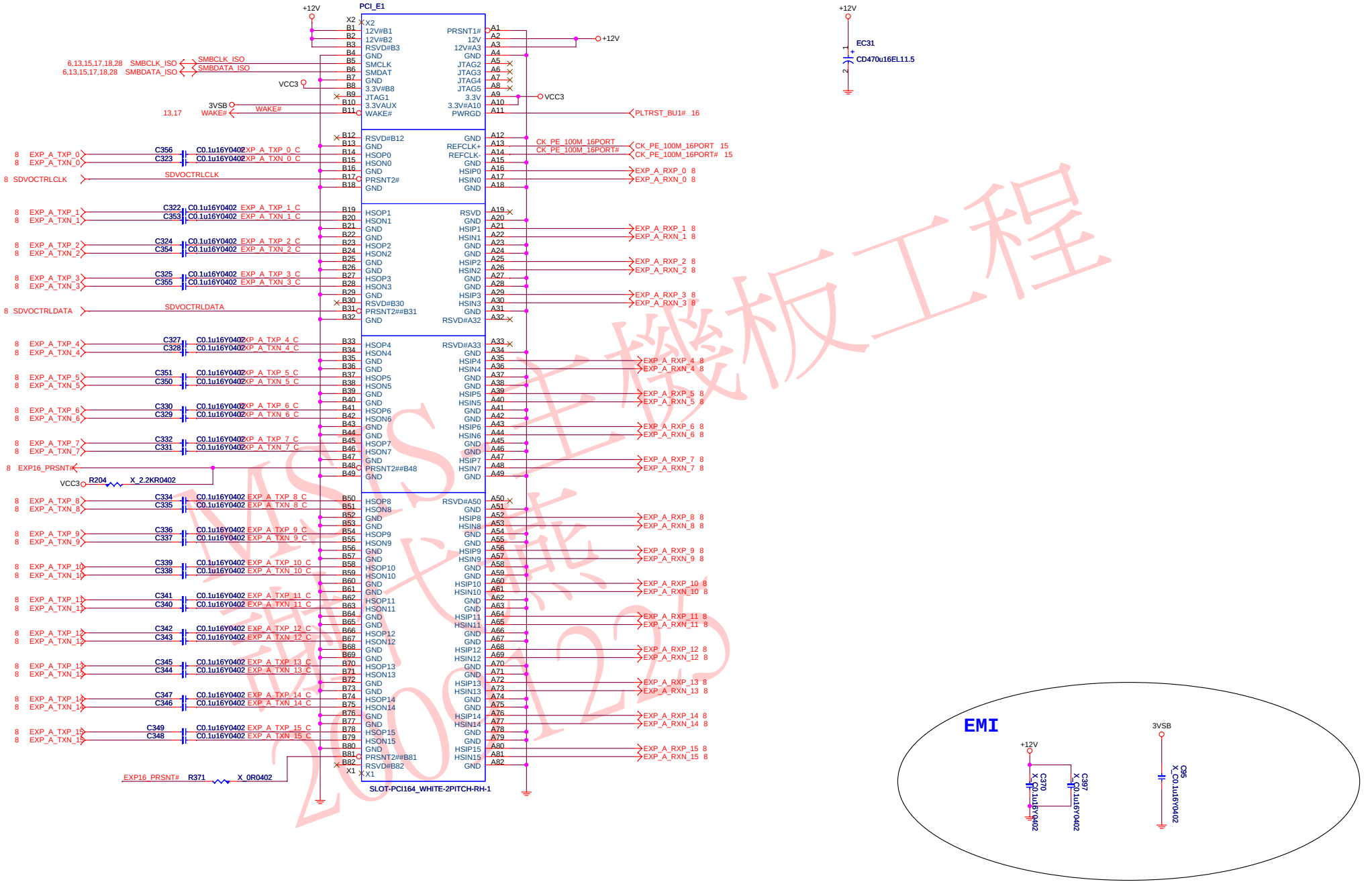
PCIE X16 PORT



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Size: Custom	Document Description: PCI EXPRESSX16&X1
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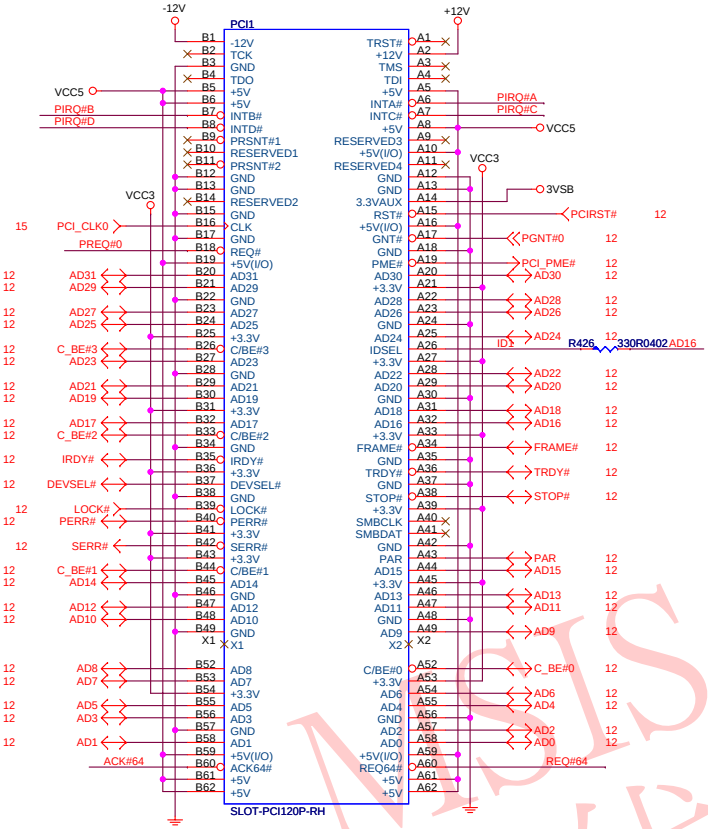
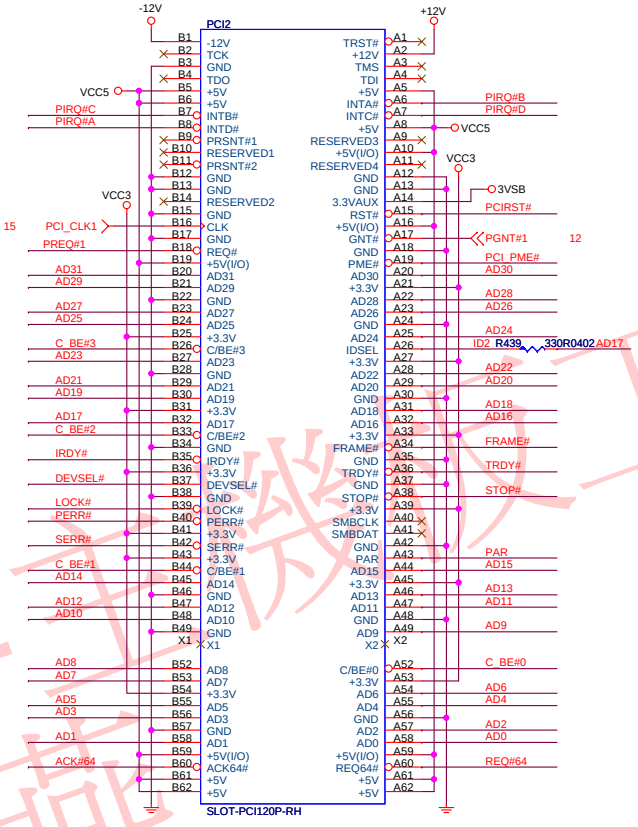
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



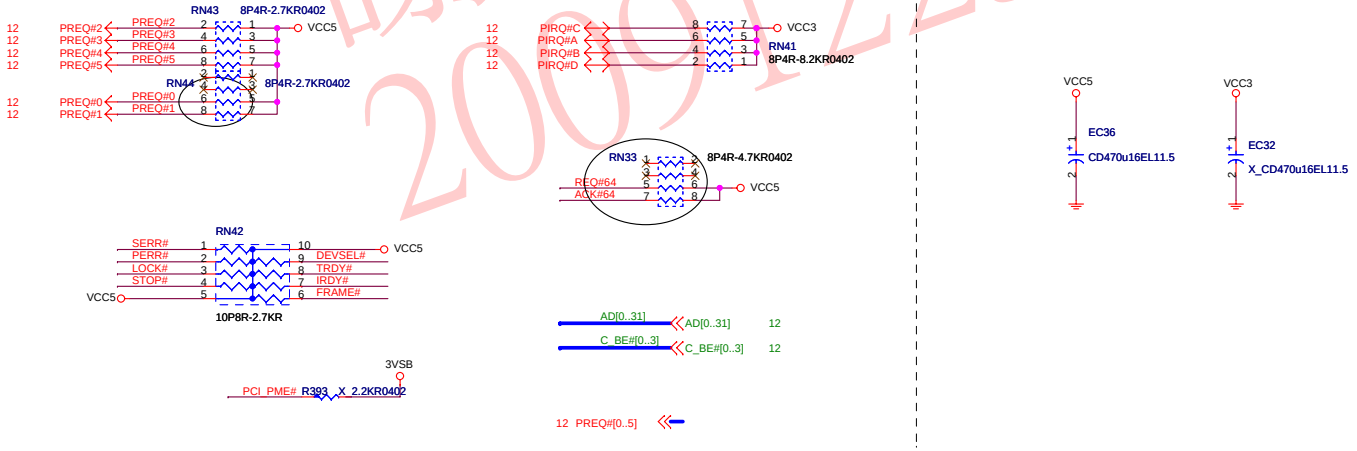
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



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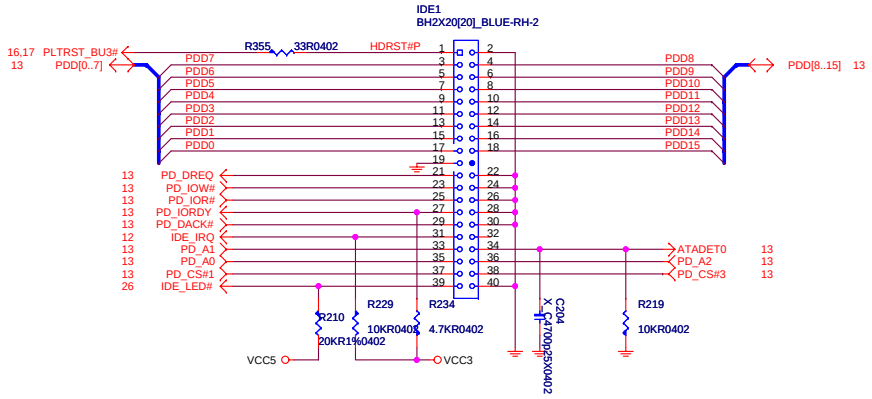
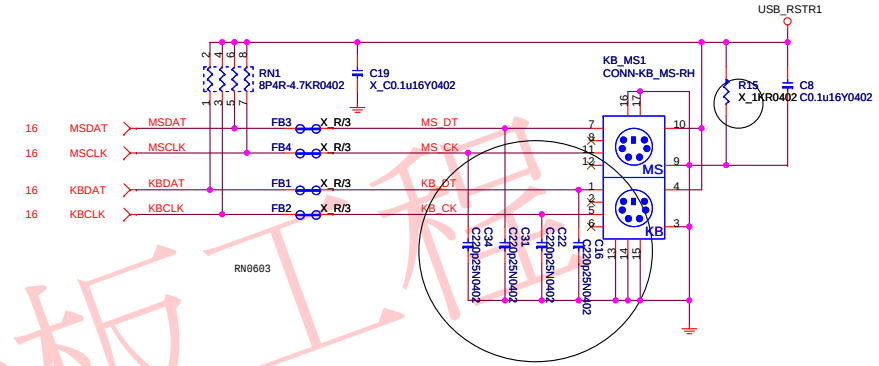
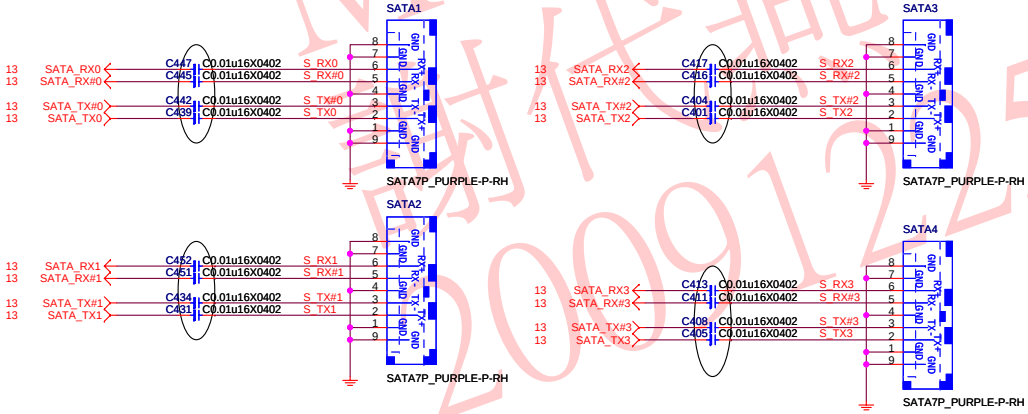
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK



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Custom	IDE & SATA Connectors	5.2

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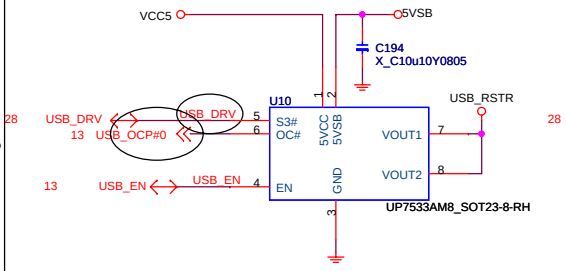
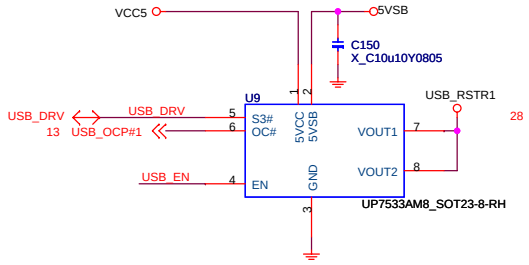
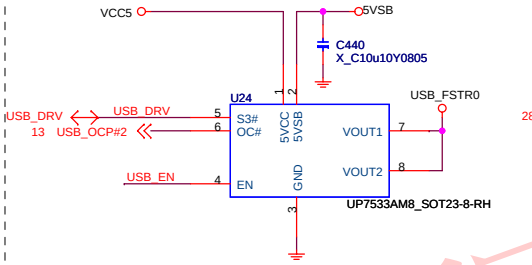
POWER CIRCUIT FOR USB PORT 0,1



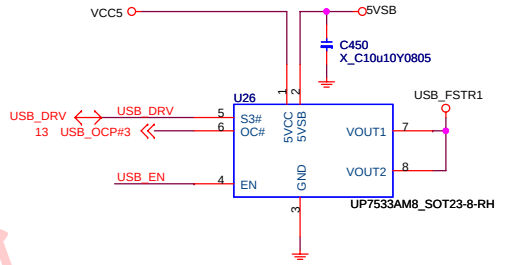
POWER CIRCUIT FOR USB PORT 2,3



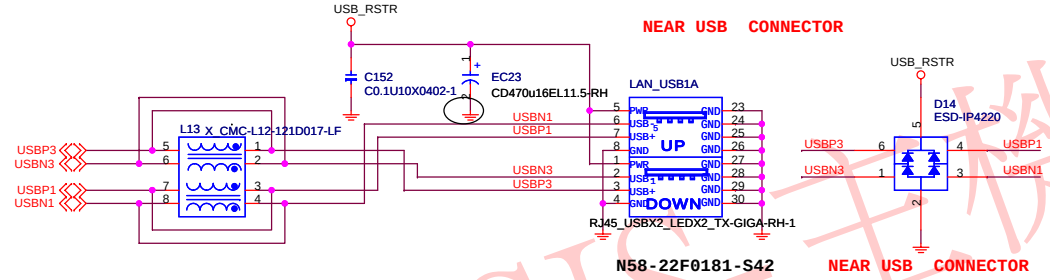
POWER CIRCUIT FOR USB PORT 4,5



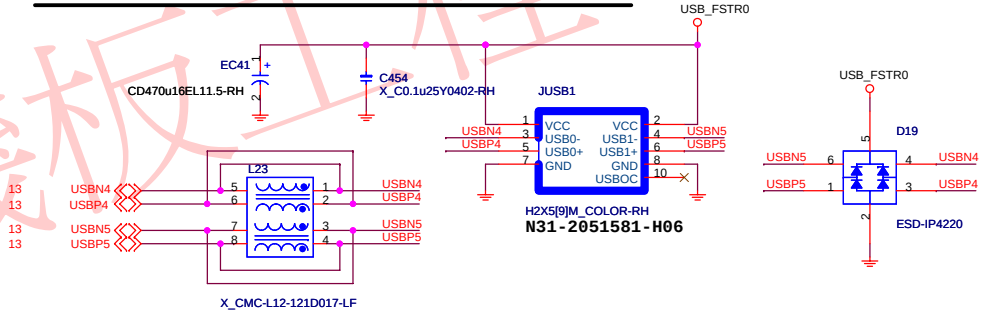
POWER CIRCUIT FOR USB PORT 6,7



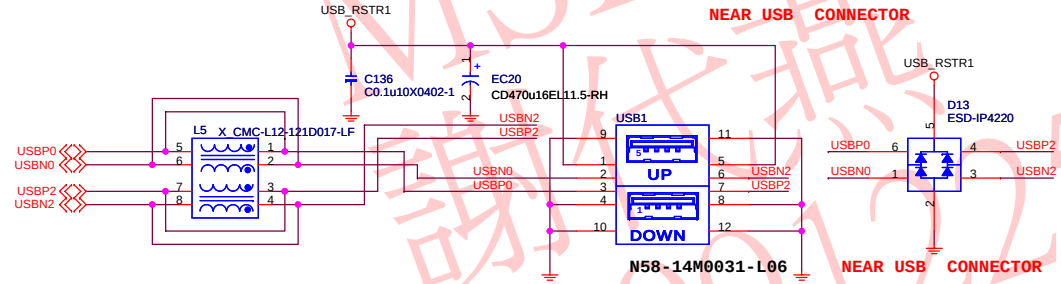
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



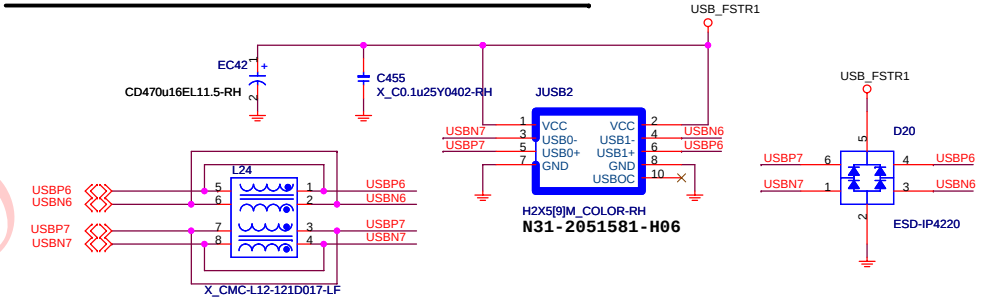
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



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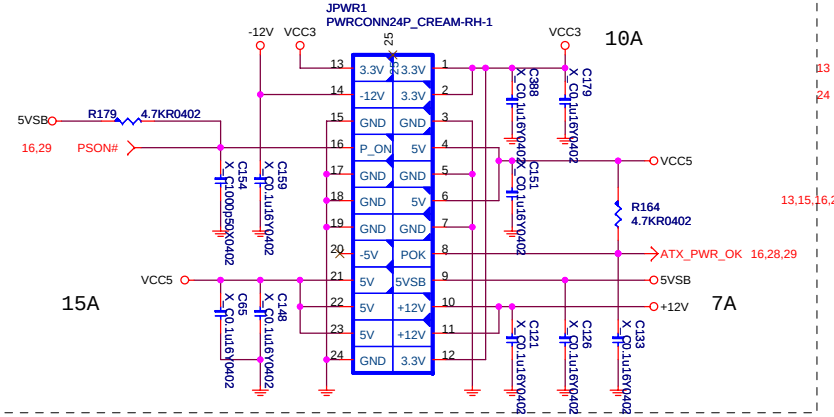
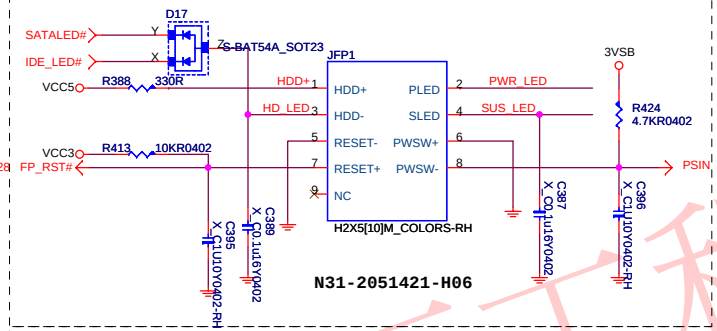
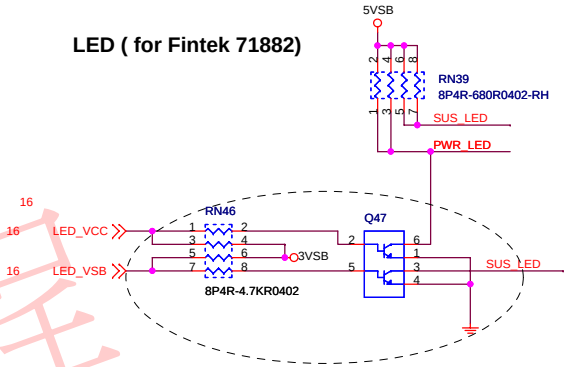
ATX Connector



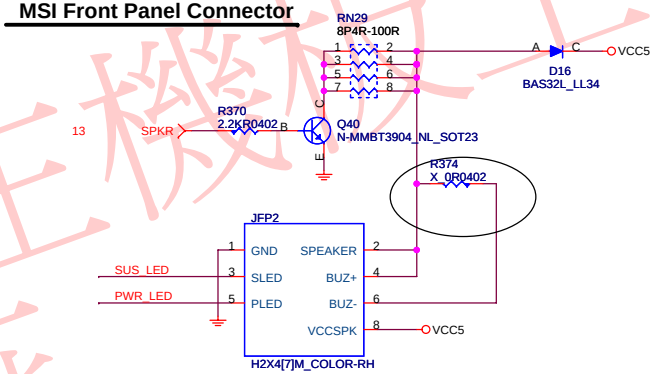
INTEL/PB Front Panel Connector



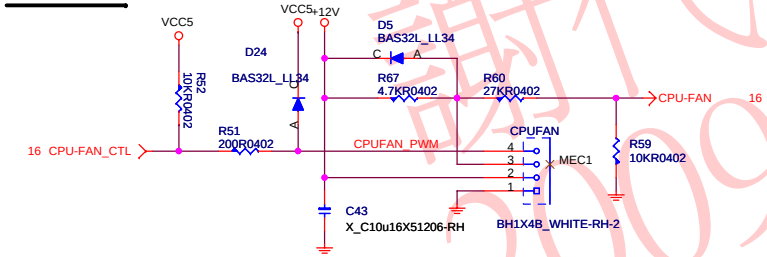
LED (for Fintek 71882)



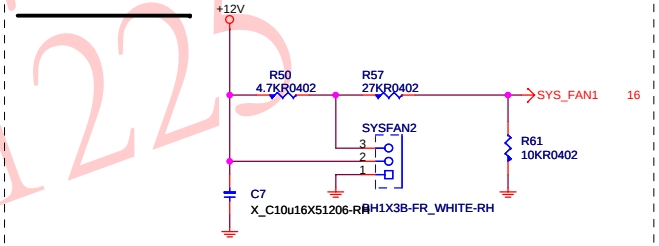
MSI Front Panel Connector



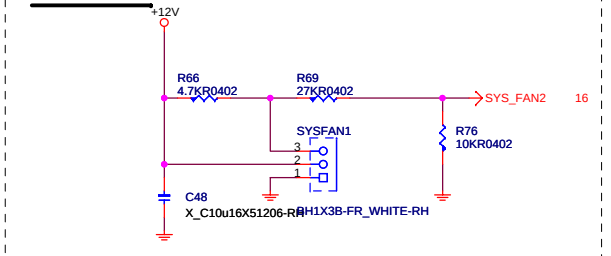
CPU FAN

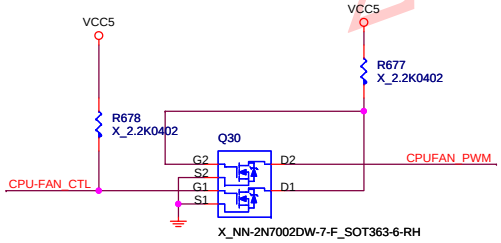


SYSTEM FAN



PWR FAN





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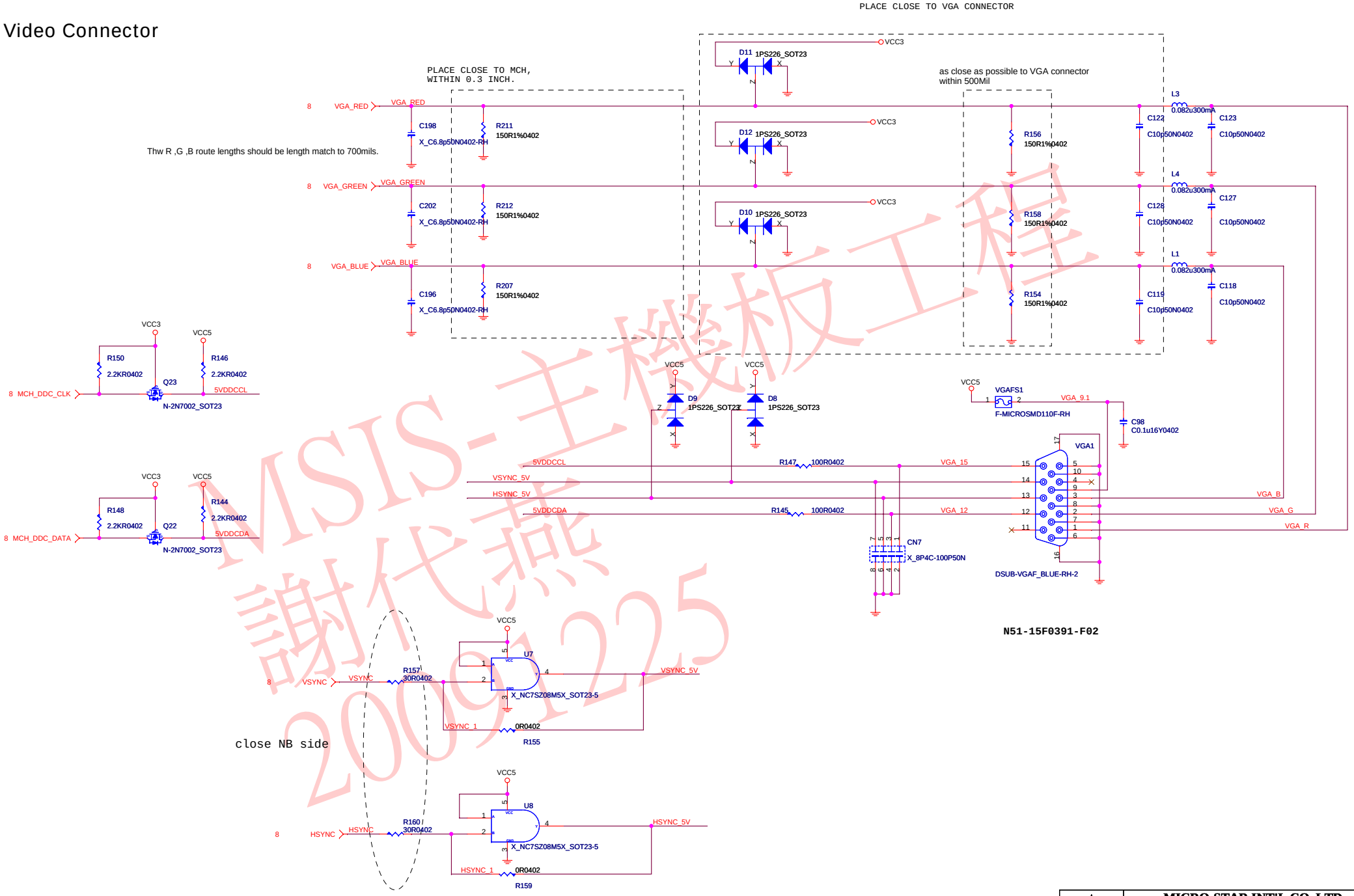
Video Connector



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Size: Custom	Document Description: VGA Connector	Rev: 5.2
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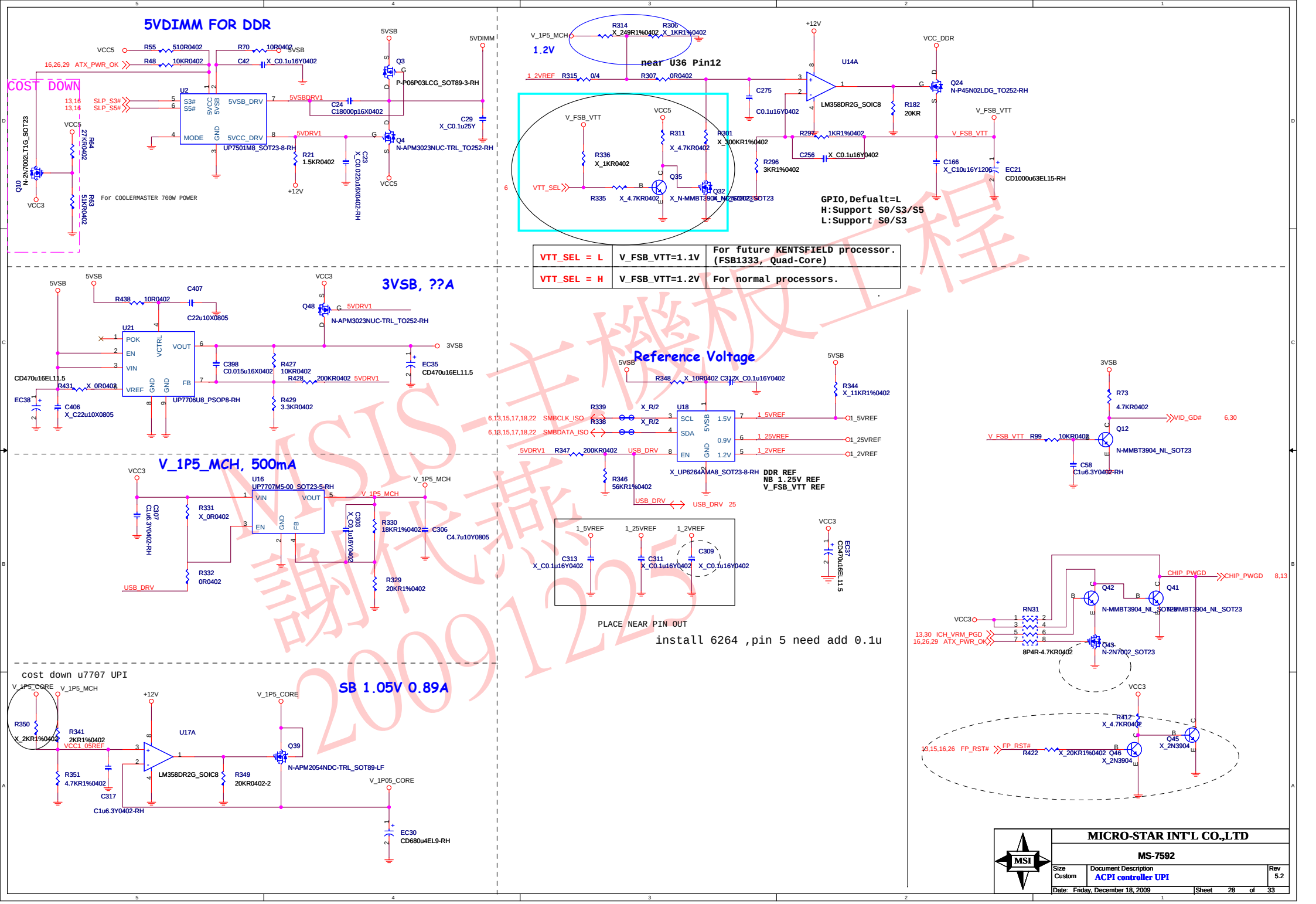
5VDIMM FOR DDR
COST DOWN
For COOLERMASTER 700W POWER
1.2V
near U36 Pin12
GPIO,Defualt=L
H:Support S0/S3/S5
L:Support S0/S3
VTT_SEL = L
V_FSB_VTT=1.1V
For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H
V_FSB_VTT=1.2V
For normal processors.
3VSB, ??A
Reference Voltage
DDR_REF
NB 1.25V REF
V_FSB_VTT REF
V_1P5_MCH, 500mA
PLACE NEAR PIN OUT
install 6264 ,pin 5 need add 0.1u
cost down u7707 UPI
SB 1.05V 0.89A
MICRO-STAR INT'L CO.,LTD
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ACPI controller UPI
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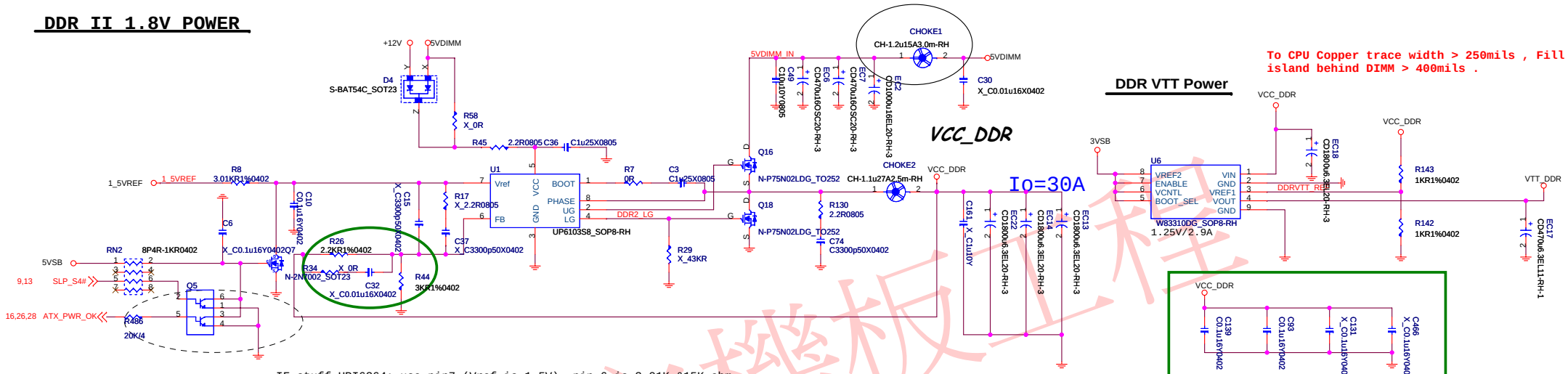
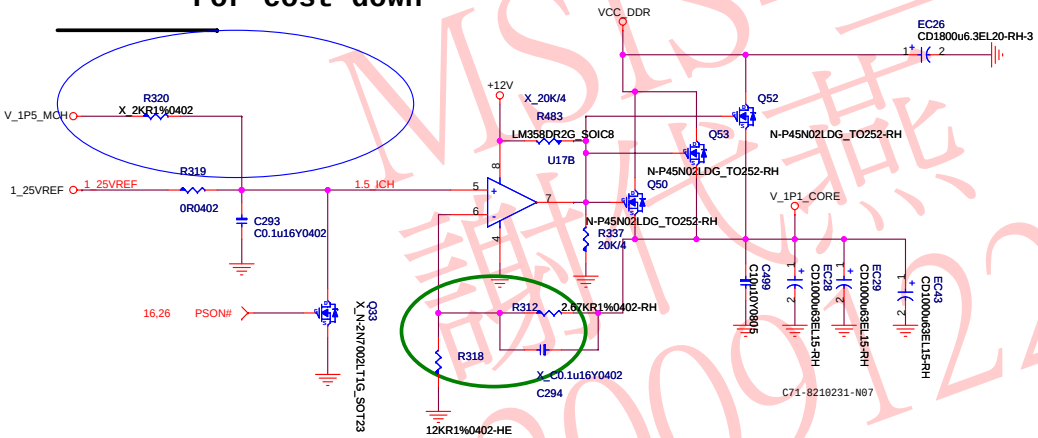
DDR II 1.8V POWER



IF stuff UPI6264: use pin7 (Vref is 1.5V), pin 6 is 3.01K &15K ohm

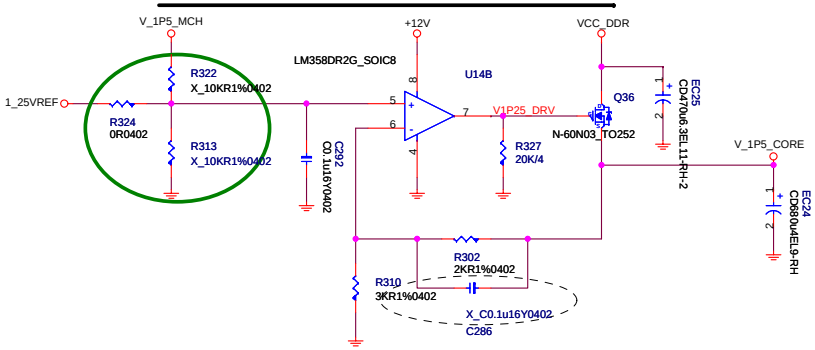
For cost down



V_1P1_CORE 18.1A+2.47A+2.94A

? value=> 1.1V 1.5V=> 1.1V 3.6K /10K

1.5V Core
1.4A



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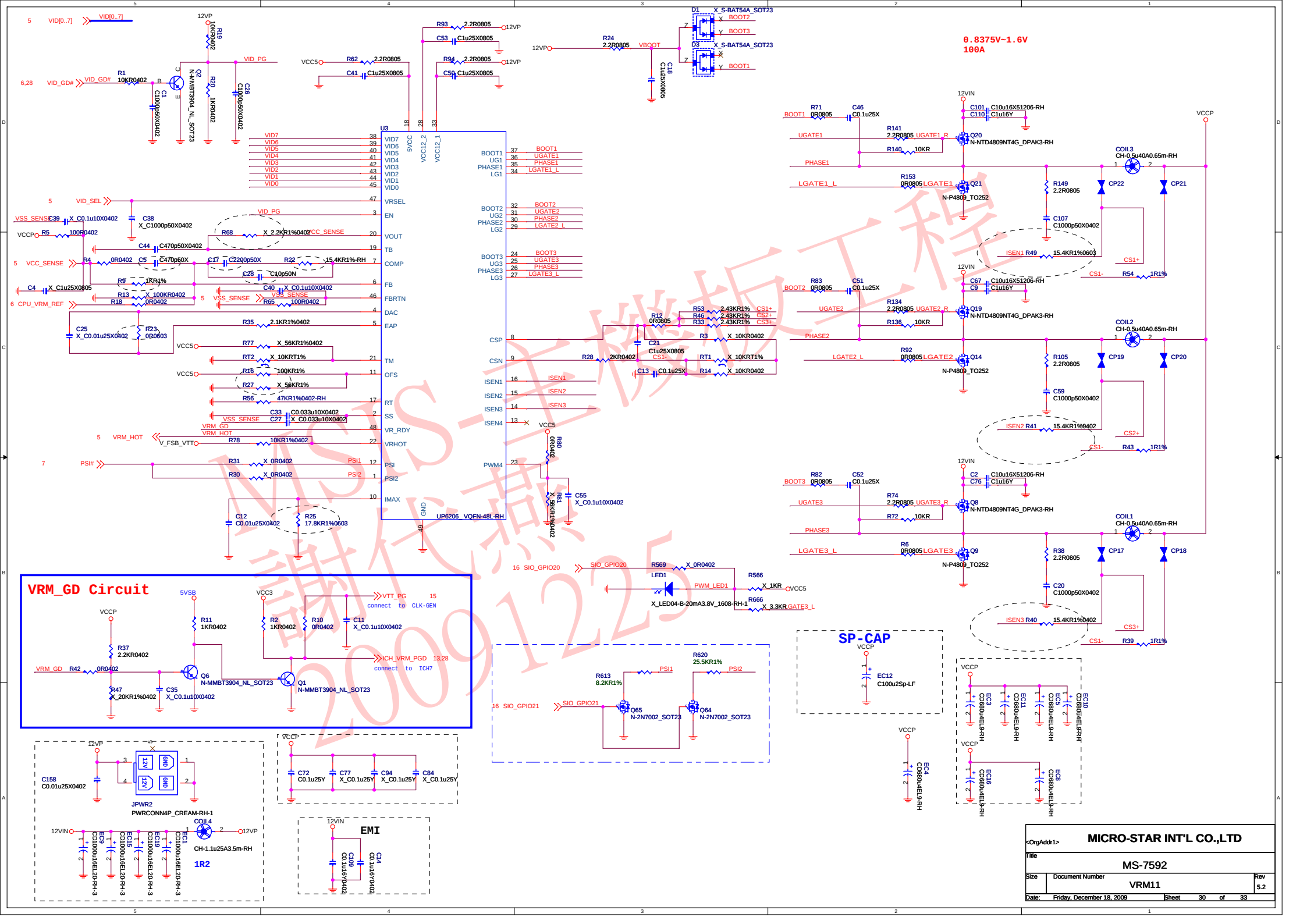
0.8375V~1.6V
100A
VRM_GD Circuit
SP-CAP
EMI
U3
UP6206_VQFN-48L-RH
JPWR2
PWRCONN4P_CREAM-RH-1
COIL4
CH-1.1u25A3.5m-RH
1R2
COIL3
CH-0.5u40A0.65m-RH
COIL2
CH-0.5u40A0.65m-RH
COIL1
CH-0.5u40A0.65m-RH
Q20
N-NTD4809NT4G_DPAK3-RH
Q21
N-P4809_TO252
Q19
N-NTD4809NT4G_DPAK3-RH
Q14
N-P4809_TO252
Q8
N-NTD4809NT4G_DPAK3-RH
Q9
N-P4809_TO252
Q6
N-MMBT3904_NL_SOT23
Q1
N-MMBT3904_NL_SOT23
Q65
N-2N7002_SOT23
Q64
N-2N7002_SOT23
D1
X_S-BAT54A_SOT23
D3
X_S-BAT54A_SOT23
LED1
X_LED04-B-20mA3.8V_1608-RH-1
connect to CLK-GEN
connect to ICH7
MICRO-STAR INT'L CO.,LTD
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VRM11
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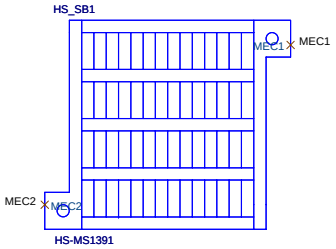
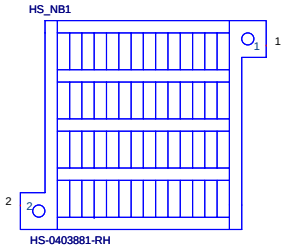
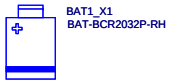
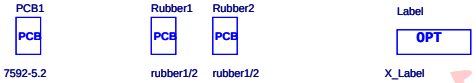
ICH7 HEATSINK



MCH HEATSINK



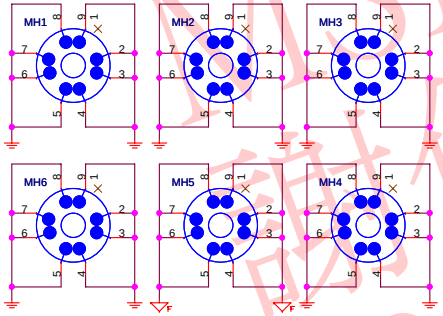




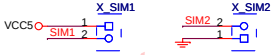
PK0-0759252-G37,精成,23,寶安恩斯邁廠(MSIS) 4,Coffee

PK0-0759252-E48,競華,23,寶安恩斯邁廠(MSIS)4,Coffee

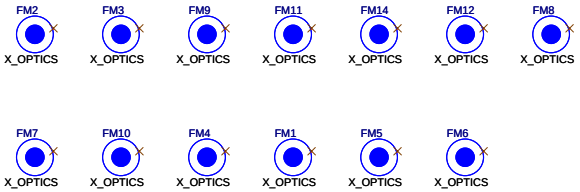
Mounting Holes



Simulation



Optics Orientation Holes



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ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPI0(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OOD12t	
GPIO6	SLOTOCC#	55	GPO	I/OOD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OOD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OOD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OOD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OOD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OOD12t	

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JCI1	*Chassis Intrusion*
Open	Normal
(1-2)	Chassis Open

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

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0A Change list:

1. Add DMI Audio net name
2. Change LED Power pull high to 680 Change r20 to 1.5K
3. Change D10 D11 Power pull VCC5, Q20 Pull up VCC3
4. Delet R252 R254 C132 R22 C60,change U5 to I95-7523212-T07
5. Modify footprint : C_P3_5_D8_H9 NC_0402_6 NC_0603_10 C0805MSB C0603MS_BOT
6. Swap RN65 RN61 RN23 RN64 RN63 RN24 RN28 RN25 RN66 ; Delet EC20,
7. Add 5VCC TO 3VCC sequence
8. change TESTPIN30 to TPC20B
9. RENAME ,Swap RN37, X_J1 Change to GND , Change C300 C301 to 0.22UF
10. Modify V_1P25_CORE to G31

7592 Change list:

1. modify G31 to G41; LAN=> TRL8111DL; ALC888 - > change to ALC888S VC2;
SIO: I/O Fintek 882 - > Change to 889;
LAN : 8111C /8101E > Change to 8111DL / 8101E ;
Vcore ST6703   > Change to UPI 6206   2008/10/13

2.reserved 0 ohm to GND for ALC888s pin4
change DDR to quar choke (ckhoke1/2) 10/15
change Q27 to N7002 from 3904, change 2pcs N3904 to Q36 ;
chage LAN circuit => modify EL cap to MLCC for +3VSB; add 2n3904 for link100/1000 ;10/16
install copper to instand LXX :10/17

3. modify TPM footprint;=JLPC1_TPM 10/20
4. remove H/VSYNC to GND resistor, (only onboard VGA) 10/21
5:Pin 23 is GPO pin for8111DL. It is used forDSM function. 10/22
6. reserved SIO PECI_REQ# to ICH7 BMbusy# 10/23
7. reserved ITPM die to resistor (G41 no support ITPM 10/23
8, delect錨璃赻論(錨璃赻) 10/24
9 ,reserved PSI function circuit, reserved PGNT#3 to Vcc3 for ICH Top Block-swap issue
reserved LPC_DRQ#0 pull high resistor (ICH7 &SIO interpull high) 10/24
10. H_VCCPLL 迵VCCDQ_CRT煦羲眙轎layout奀掩耽誑補   10/24
11.H_COMP4 reserved Pul up R(DEMO board reserved); ICH7 pinAF24/AH25 for desttop is test pint,
for mobile is DPRSTP#/DPSLP#=> 0 ohm R to ICH7 no stuff , stuff CPU side pull high R to VTT; 10/26
12. PCIE slot footprint chage to SLOT_PCIEXP164_2(嫉諶砑妓厘CPU源砑)
Clock part: cange 2 pcs 3904 to 1 2n3904 for layout size;10/27
13. reserved a DDR DIMM input EL cap ;
change VRM part some RC to 0603 footprint, reserved a SP_cap10/28
14. remove some NB TXX(test pad) for layout , 10/30
15: reserved RNXX for HDMI (RNXX intershort) P8; del TPM CONN TPMCLK 10P EMI cap; SWap RN64 .6&8 (CPUSEL2) 10/31
16: Swap RN15.1&3 , update NB_sink/EC36/37/R380 tol CIS library 11/03
17, modify some 0805 to 0603 cap for layout and reserved 1.1_core cap for cost (p8) ; change H/VSYNC_1 location for cost; 11/04
18: update NB ci library; change Audio 100uf cap to EL cap 11/05
19: modify test point footprint from tcp20B to testpin25
change VRM CS1/2/3+ to 1.5K ohm, reserved C8; 11/06
20 PLTRST_BU1# pull high from 220 ohm to 1K (VCC3) ==test signal 11/07
21: reservec SATALED# & AC_RST# pull high resistor 11/08
22 Footprint update凵 OSCC_MS 峈 N_OSCC_MS 11/10
add rubber 6010: P/N:E25-7530010-C81 11/12
23 R40/R41 change 0402 value 11/21

7592 1.0 Change list:

1. SIO Version:B change to Version: C; SIO pin99(VCC) modify to 3VSB, pwok(pin80) modify to 3VSB ;
DMI CAP change to 0510 for SMT process ; update LAN_usb footprint, R181 for 8111DL, 8103E no install;1202
2> modify NB core and NB_sink P/N ;c211 chage to 0603;C359 chage to 3vsb for SIO Pin99 from Vcc3;
R158 R160 place NB side for SI bug,; add R486 for intel seq; 1212
3> build BOM for osc cap (audio/VRM/DDR input) 12/16

7592 5.1 Change list:

1.0 Change list:

1. U11 EN(pin3)change to USB_DRV
2. Add SIO pin55 SKTOCC# pull up to 3vsb
3. Swap RN26
4. add Control UP7501 power seqence

1.1 Change list:

09/07/22

1. Printport chane to pin header
2凵add APS LED(ONE LED);
3凵change Y3 footprint to OSCC_MS;
4凵change SIO PN to B02-7188934-F34
5凵change JPW1 to JPWR2
6凵change ATX1 to JPWR1
7凵Change NB &SB heatsink to HS_NB1&HS_SB1
8凵Change LAN to AR8132M/AR8131M
9凵change audio codec to VT1708S;

09/07/23

1. page 30 ,del R616,R550
chagne R80 to 0ohm
change R54,R43,R39 to 1ohm;
add Q64,Q65,R613,R620;
2. page 21 ,change CN10 to 100p
change 470p cap to 100p;
3凵page 15乙add OC Switch

09/07/24

1凵page 17乙change 3VDUAL to 3VSB
add C724 for EMI;

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