MS-7592

Version 20

CPU:

Intel Conroe (95W Dual core)

System Chipset:

Intel G41 - MCH (North Bridge)
Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI
HD -- ALC888S
LPC Super I/O -- F71889
LAN-- REALTEK RTL8111D Co-lay RTL8103E
CLOCK -- RTM875-605

Main Memory:

DDR II *2 (Max 4GB)

Expansion Slots:

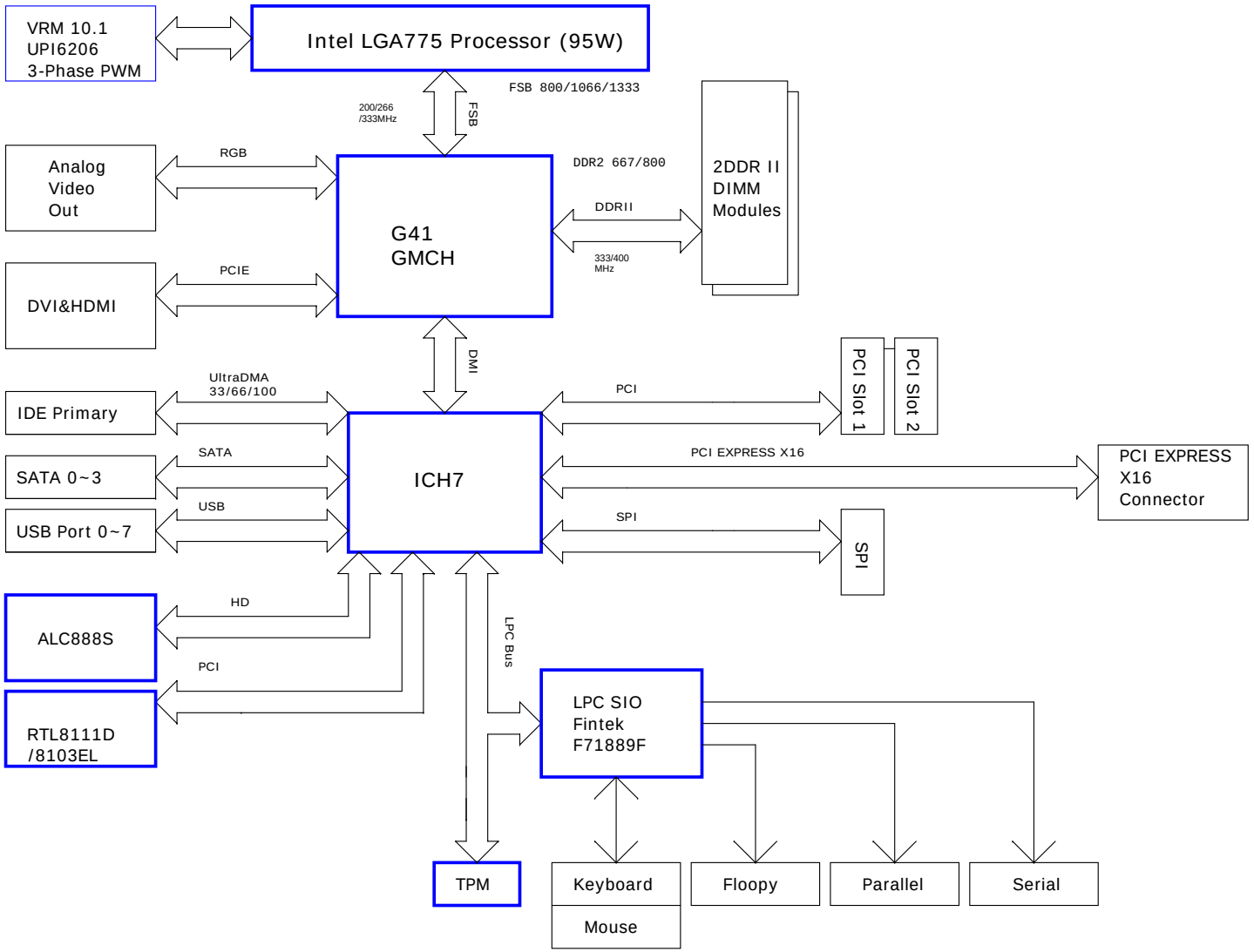
PCI2.3 SLOT * 2

PCI EXPRESS X16 SLOT

ST PWM:

Controller: 3 PHASES

Block Diagram



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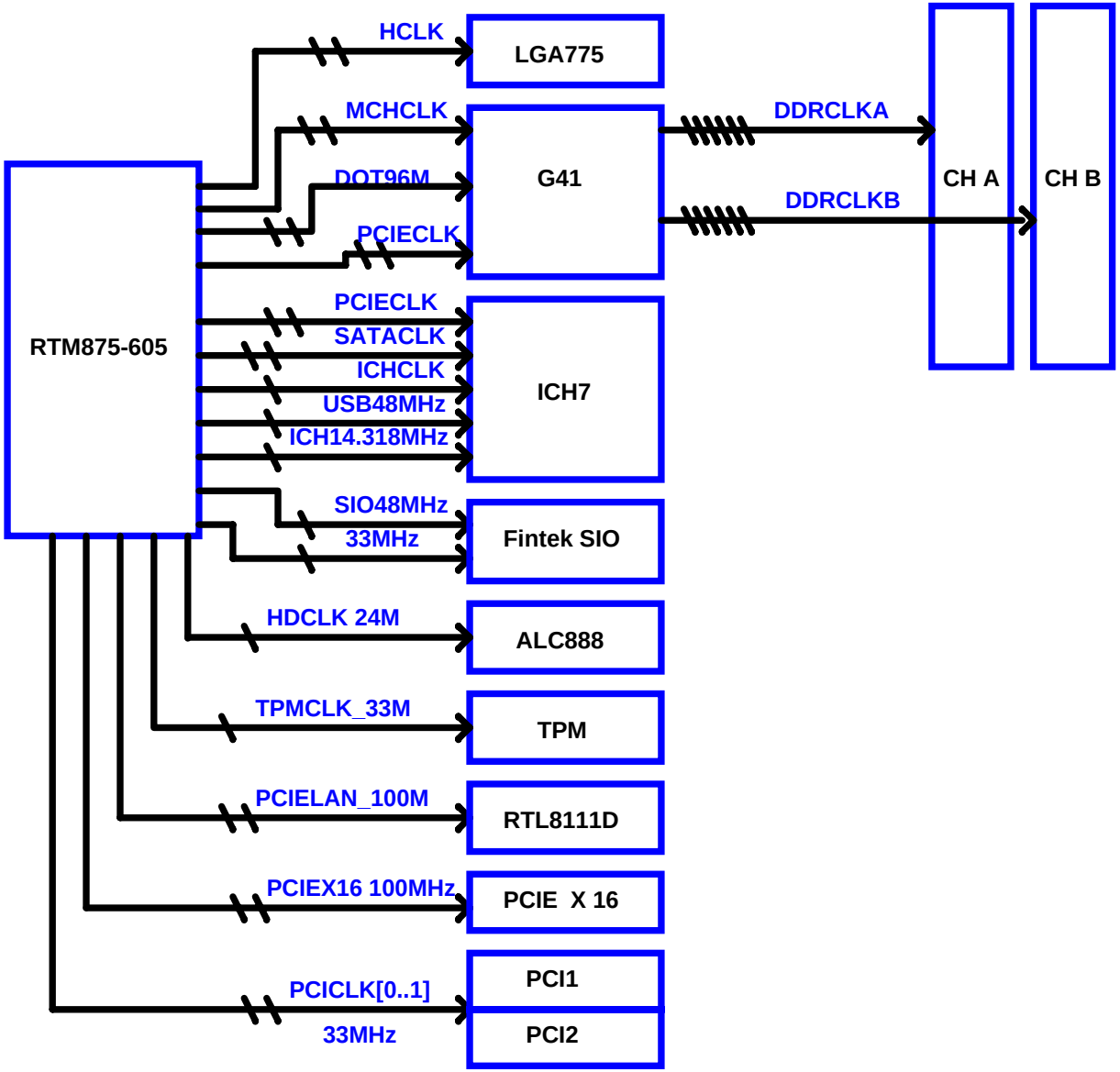
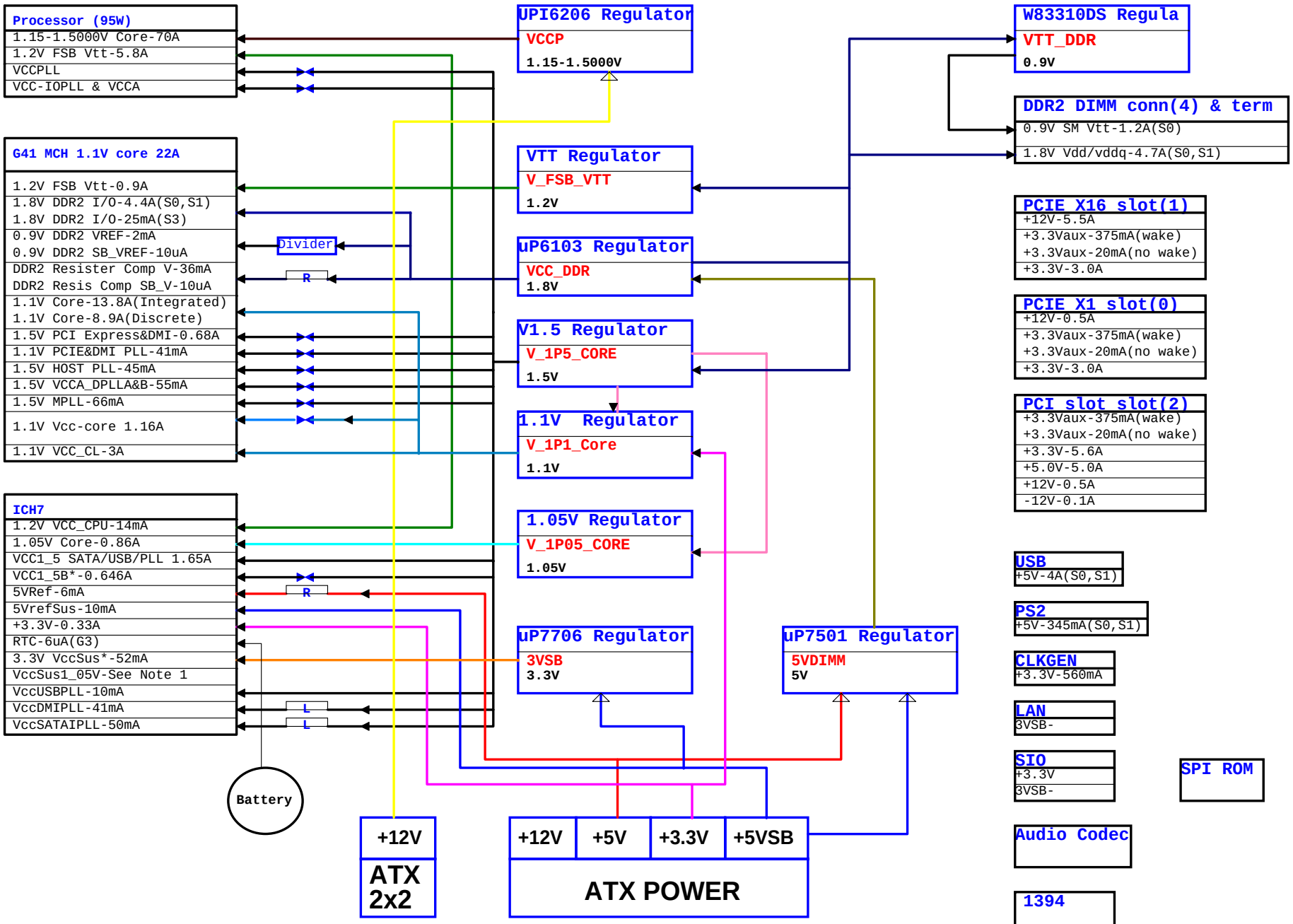
	MS-7592	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 2.0
Date: Sunday, January 04, 2009	Sheet 2 of 35	

CLOCK MAP



MICRO-STAR INT'L CO.,LTD		
MS-7592		
Size: Custom	Document Description: CLOCK MAP	Rev: 2.0
Date: Sunday, January 04, 2009	Sheet 3 of 35	



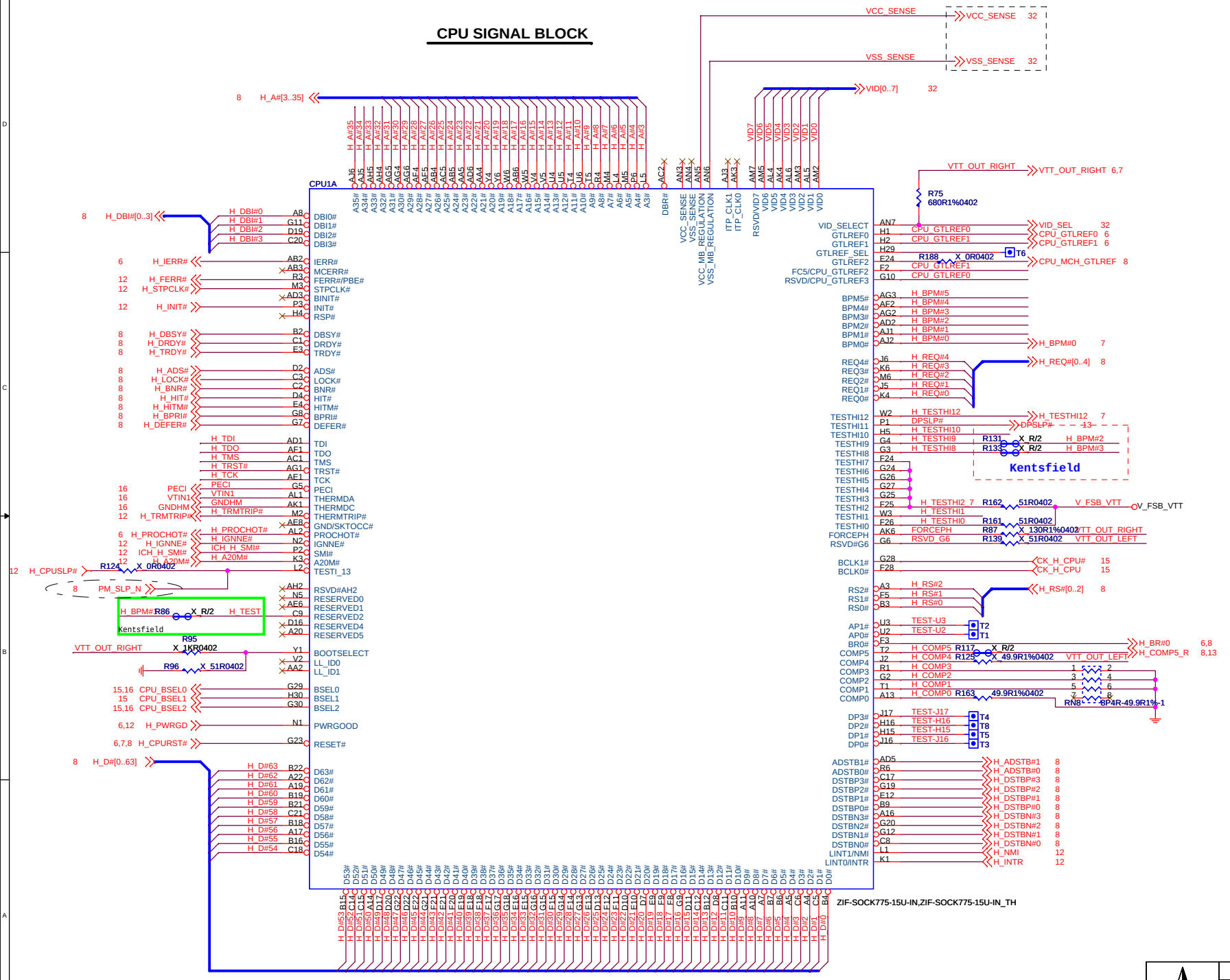
MICRO-STAR INT'L CO.,LTD

MS-7592

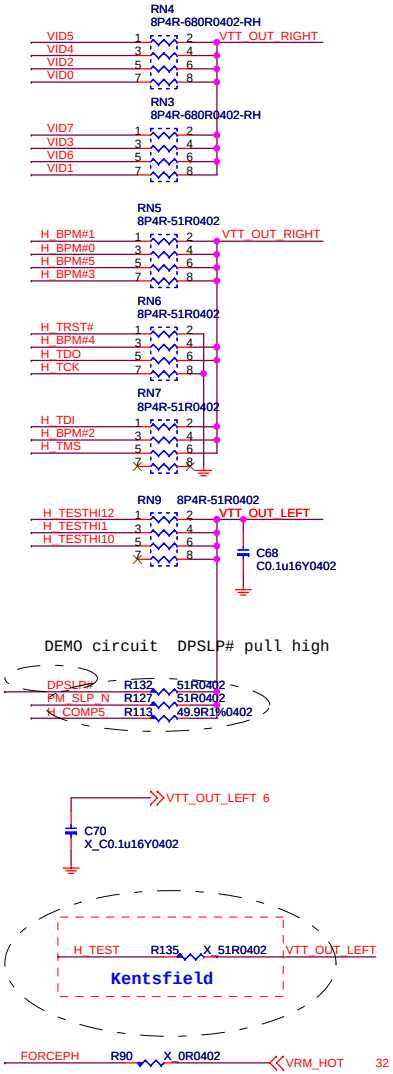
Size	Document Description	Rev
Custom	LGA775 - Signal	2.0

Date: Sunday, January 04, 2009 Sheet 4 of 35

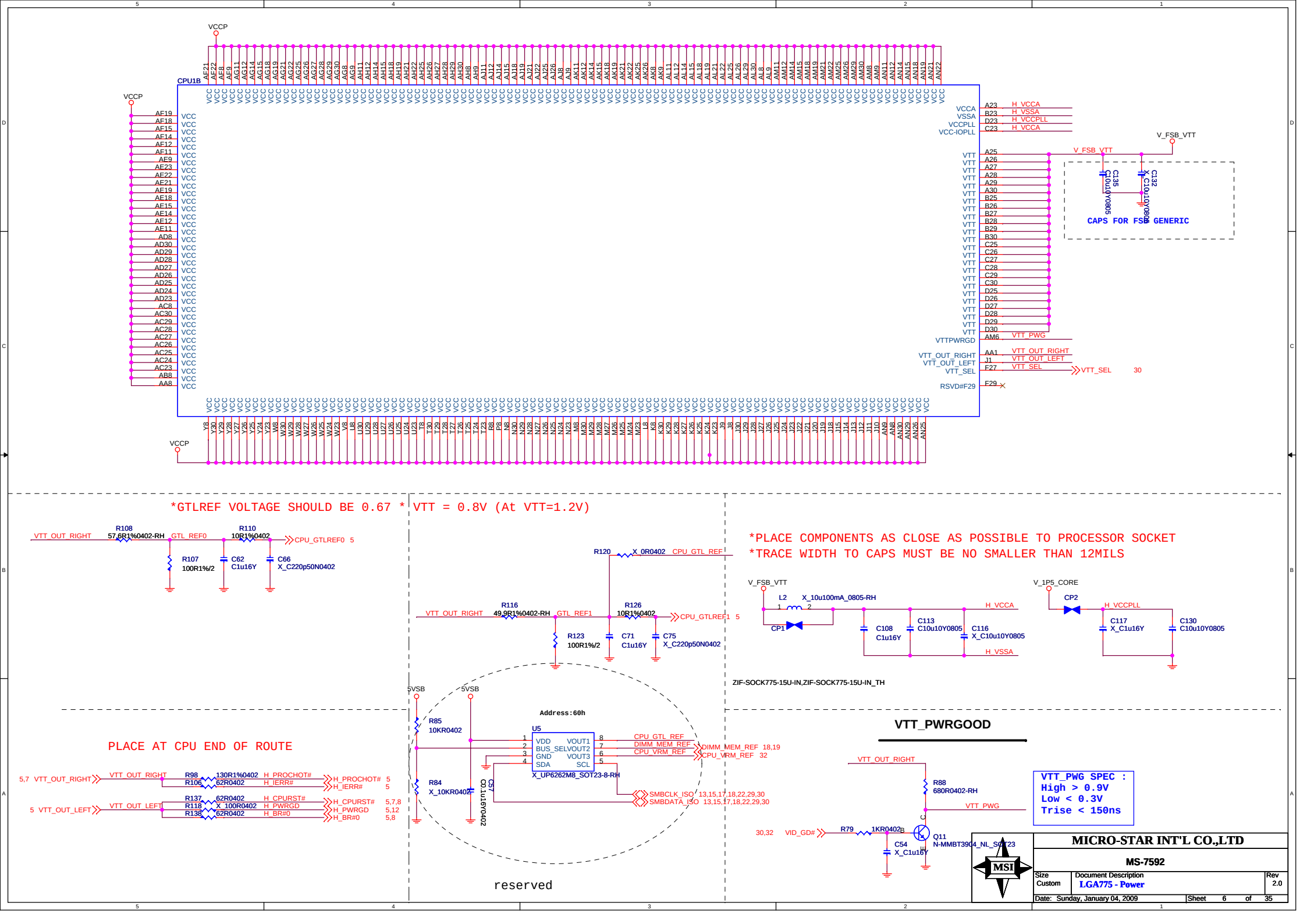
CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN



MICRO-STAR INT'L CO.,LTD			
MS-7592			
Size: Custom	Document Description: LGA775 - Signal		Rev: 2.0
Date: Sunday, January 04, 2009		Sheet 5 of 35	


CPU1B
VCCP
VCCA
VSSA
VCCPLL
VCC-IOPLL
VTTPWRGD
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
RSVD#F29
V_FSB_VTT
CAPS FOR FSB GENERIC
*GTLREF VOLTAGE SHOULD BE 0.67 * VTT = 0.8V (At VTT=1.2V)
R108 57.6R1%0402-RH
R110 10R1%0402
R107 100R1%/2
C62 C1u16Y
C66 X_C220p50N0402
CPU_GTLREF0
R120 X_0R0402 CPU_GTL_REF
R116 49.9R1%0402-RH
R126 10R1%0402
R123 100R1%/2
C71 C1u16Y
C75 X_C220p50N0402
CPU_GTLREF1
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS
L2 X_10u100mA_0805-RH
CP1
C108 C1u16Y
C113 C10u10Y0805
C116 X_C10u10Y0805
H_VCCA
H_VSSA
V_1P5_CORE
CP2
H_VCCPLL
C117 X_C1u16Y
C130 C10u10Y0805
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
PLACE AT CPU END OF ROUTE
R98 130R1%0402 H_PROCHOT#
R106 62R0402 H_IERR#
R137 62R0402 H_CPURST#
R118 X_100R0402 H_PWRGD
R138 62R0402 H_BR#0
H_CPURST# 5,7,8
H_PWRGD 5,12
H_BR#0 5,8
5VSB
R85 10KR0402
R84 X_10KR0402
C57 C0.1u16Y0402
Address:60h
U5
VDD VOUT1
BUS_SEL VOUT2
GND VOUT3
SDA SCL
X_UP6262M8_SOT23-8-RH
CPU_GTL_REF
DIMM_MEM_REF
CPU_VRM_REF
DIMM_MEM_REF 18,19
CPU_VRM_REF 32
SMBCLK_ISO 13,15,17,18,22,29,30
SMBDATA_ISO 13,15,17,18,22,29,30
reserved
VTT_PWRGOOD
R88 680R0402-RH
VTT_PWG
R79 1KR0402
Q11 N-MMBT3904_NL_SOT23
C54 X_C1u16Y
VID_GD#
30,32
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
MICRO-STAR INT'L CO.,LTD
MS-7592
Size Custom
Document Description LGA775 - Power
Rev 2.0
Date: Sunday, January 04, 2009
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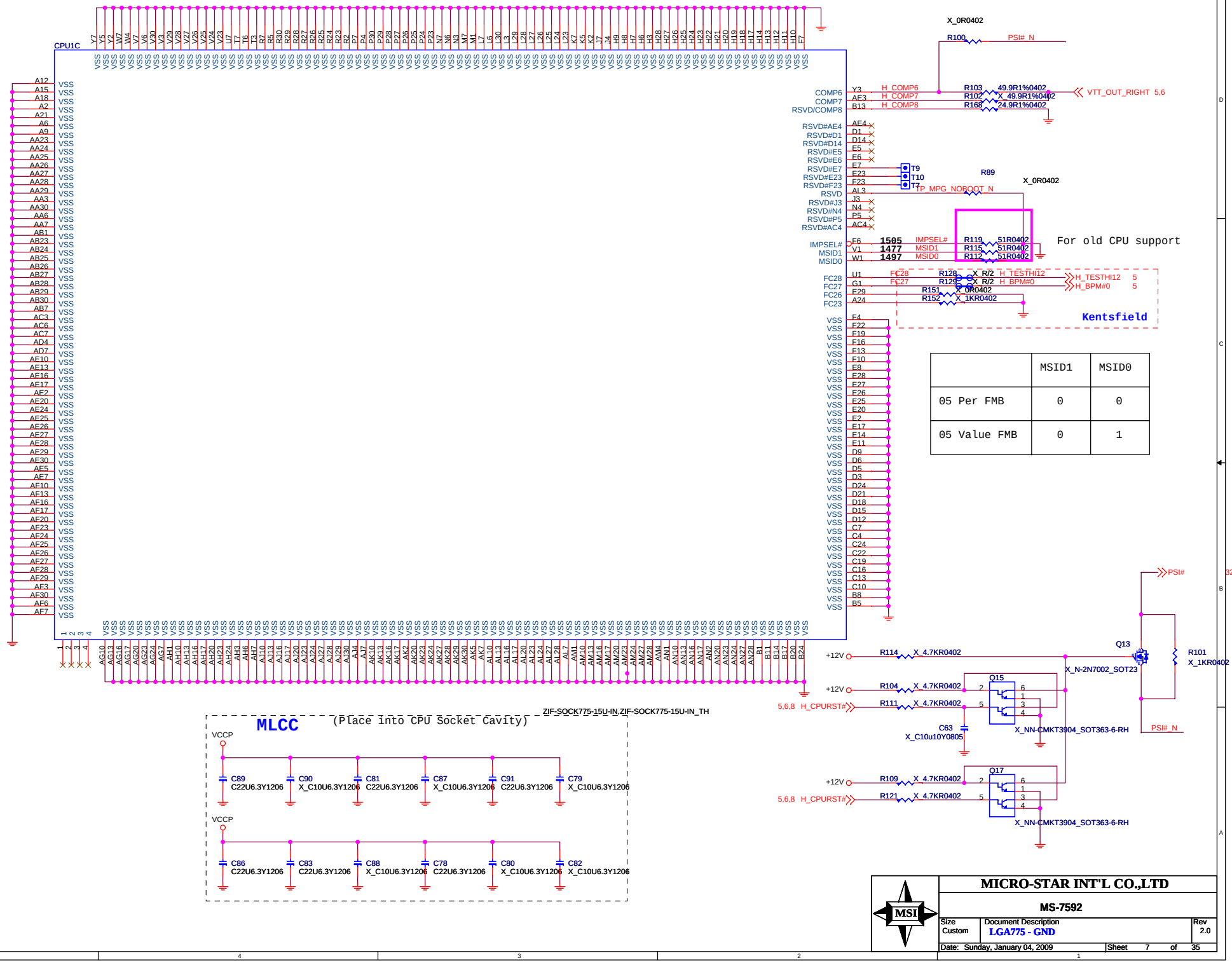

	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1

MICRO-STAR INT'L CO.,LTD

MS-7592

Size: Custom | Document Description: LGA775 - GND | Rev: 2.0

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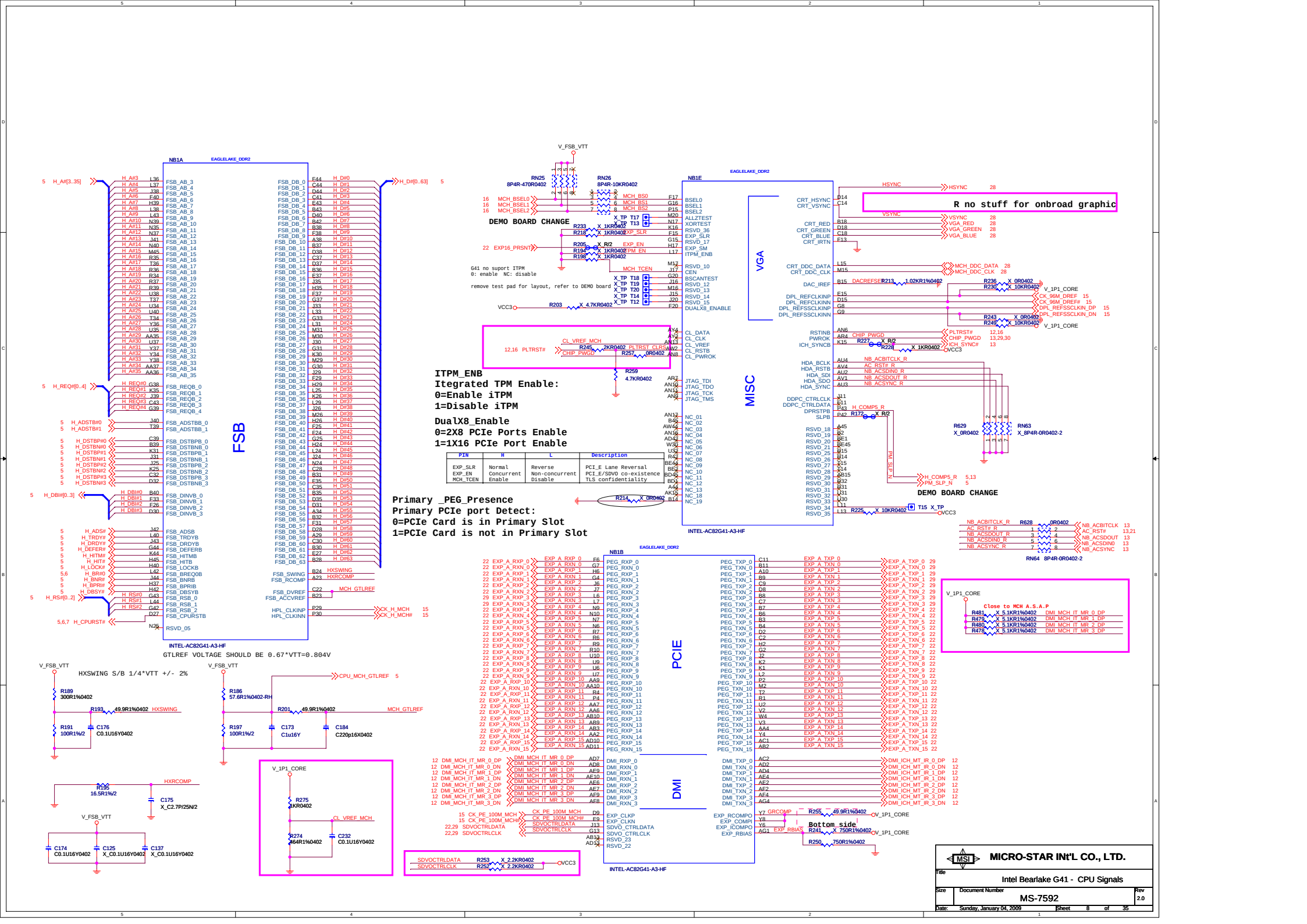
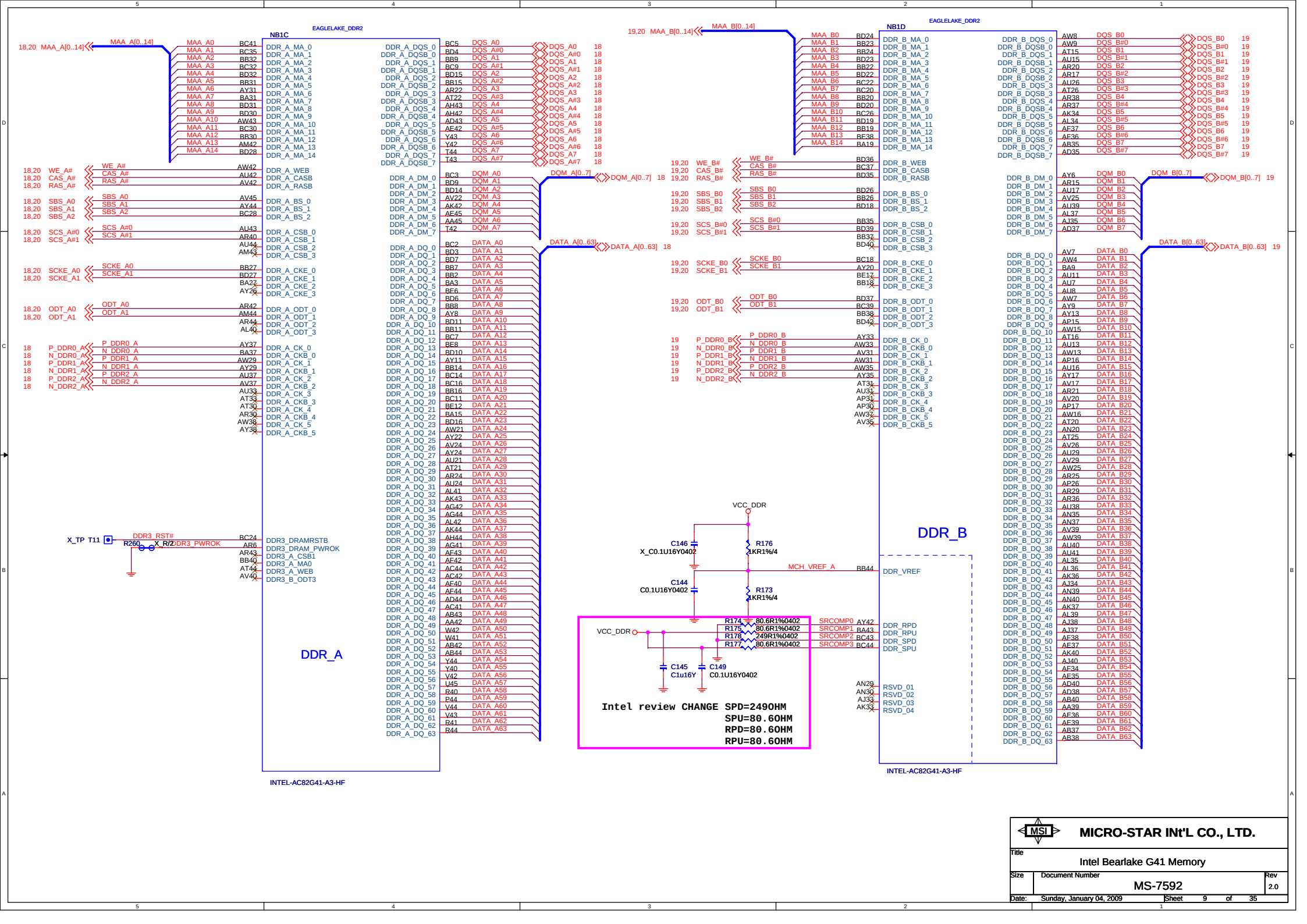
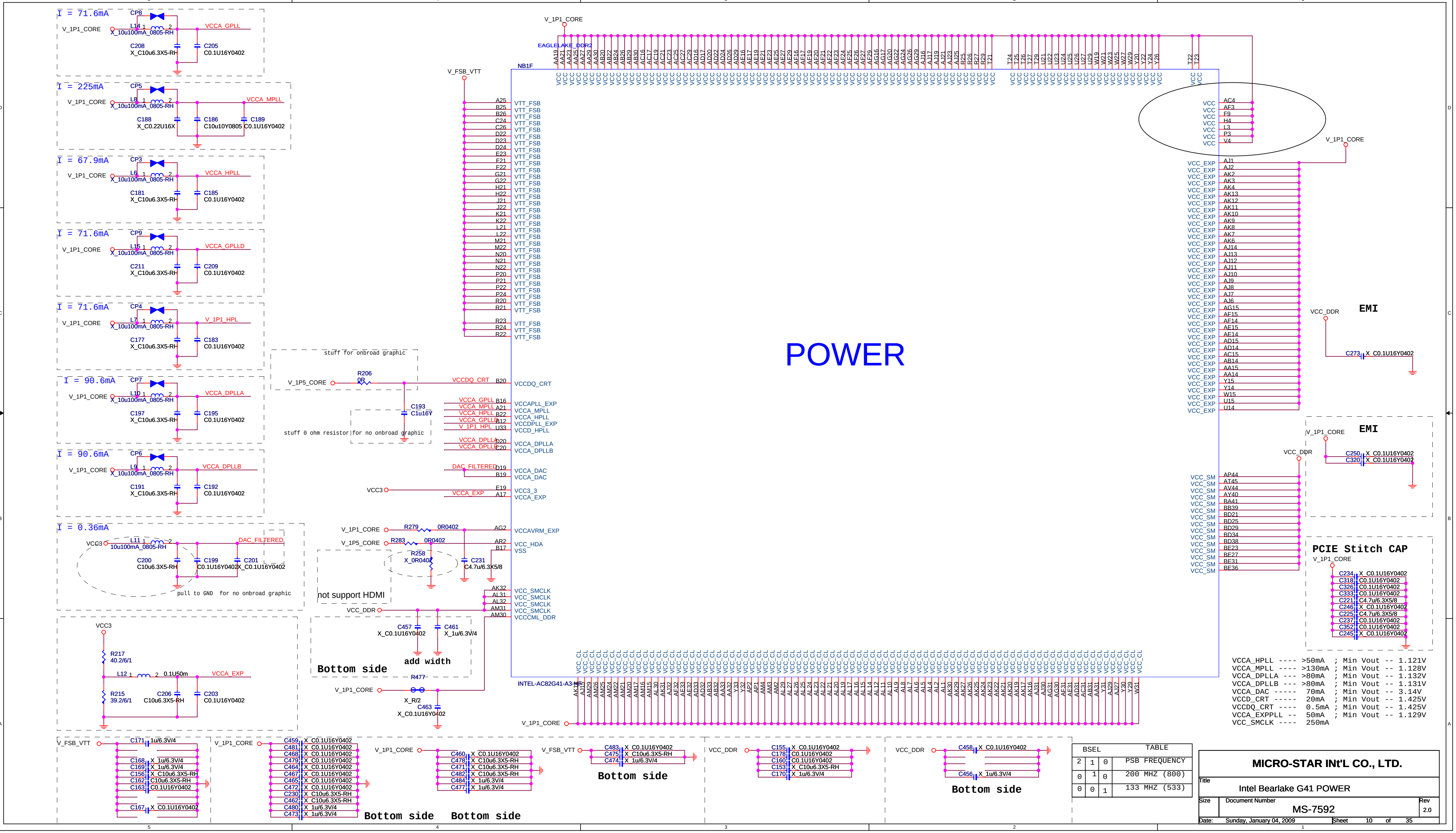

NB1A
EAGLELAKE_DDR2
FSB
INTEL-AC82G41-A3-HF
GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.804V
HXSWING S/B 1/4*VTT +/- 2%
V_FSB_VTT
DEMO BOARD CHANGE
ITPM_ENB
Itegrated TPM Enable:
0=Enable iTPM
1=Disable iTPM
DualX8_Enable
0=2X8 PCIe Ports Enable
1=1X16 PCIe Port Enable
Primary _PEG_Presence
Primary PCIe port Detect:
0=PCIe Card is in Primary Slot
1=PCIe Card is not in Primary Slot
NB1E
VGA
MISC
R no stuff for onbroad graphic
NB1B
PCIE
DMI
Bottom_side
Close to MCH A.S.A.P
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G41 - CPU Signals
MS-7592
Sunday, January 04, 2009


EAGLELAKE_DDR2
NB1C
DDR_A
INTEL-AC82G41-A3-HF
EAGLELAKE_DDR2
NB1D
DDR_B
INTEL-AC82G41-A3-HF
Intel review CHANGE SPD=249OHM
SPU=80.6OHM
RPD=80.6OHM
RPU=80.6OHM
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G41 Memory
MS-7592
Rev 2.0
Sunday, January 04, 2009
Sheet 9 of 35



VCCA_HPLL ---- >50mA ; Min Vout -- 1.121V
VCCA_MPLL ---- >130mA ; Min Vout -- 1.128V
VCCA_DPLLA --- >80mA ; Min Vout -- 1.132V
VCCA_DPLLB --- >80mA ; Min Vout -- 1.131V
VCCA_DAC ----- 70mA ; Min Vout -- 3.14V
VCCD_CRT ----- 20mA ; Min Vout -- 1.425V
VCCDQ_CRT ---- 0.5mA ; Min Vout -- 1.425V
VCCA_EXPPLL -- 50mA ; Min Vout -- 1.129V
VCC_SMCLK ---- 250mA

BSEL			TABLE PSB FREQUENCY
2	1	0	PSB FREQUENCY
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

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Title: Intel Bearlake G41 POWER

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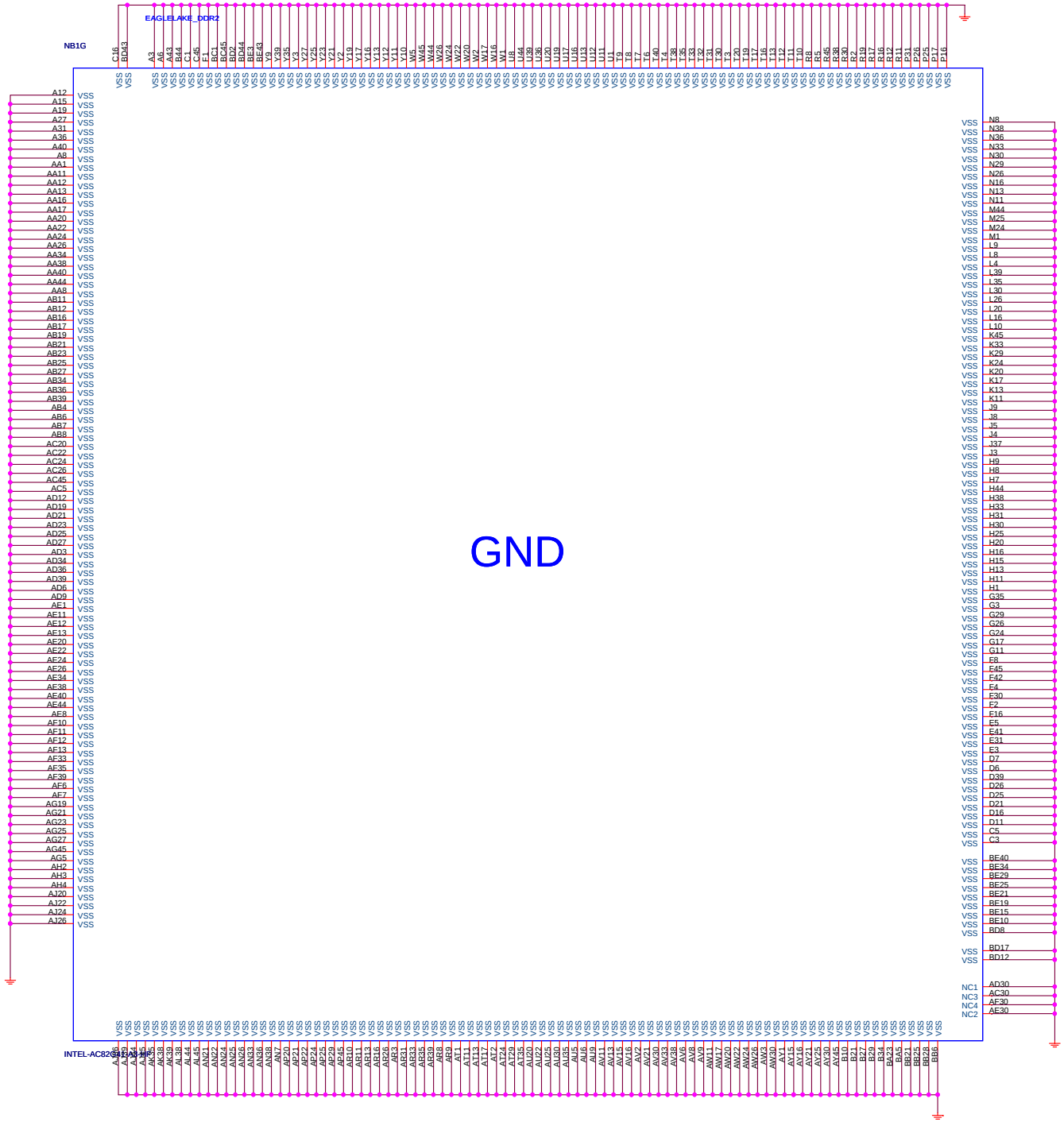
Date: Sunday, January 04, 2009 | Sheet 10 of 35



MSI	MICRO-STAR INt'L CO., LTD.
Title	Intel Bearlake G41 GND
Size	Document Number: MS-7592
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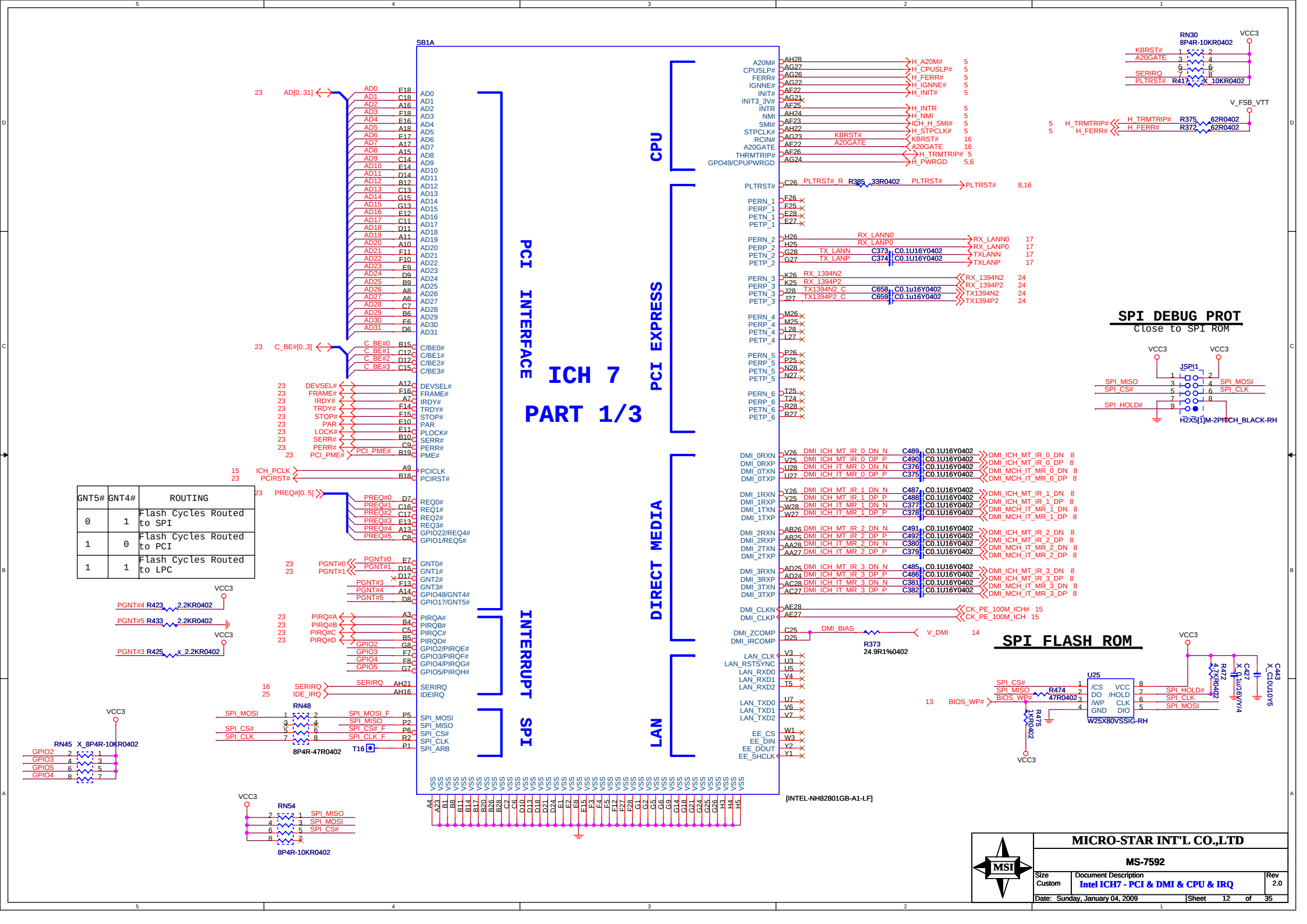
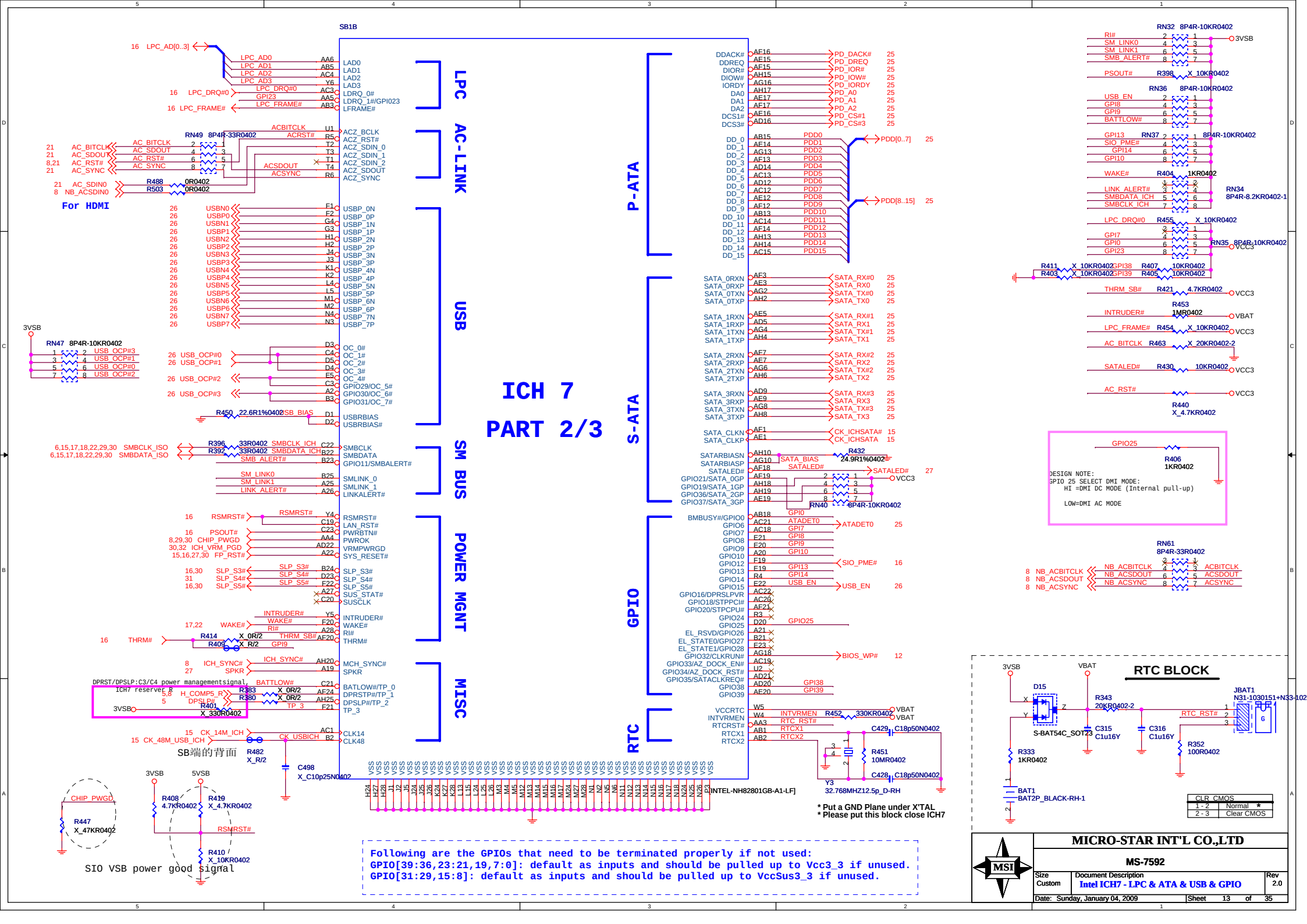


GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC


SB1B
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-SATA
GPIO
RTC
ICH 7
PART 2/3
For HDMI
SB端的背面
SIO VSB power good signal
[INTEL-NH82801GB-A1-LF]
* Put a GND Plane under X'TAL
* Please put this block close ICH7
RTC BLOCK
CLR_CMOS
1 - 2 Normal *
2 - 3 Clear CMOS
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
MICRO-STAR INT'L CO.,LTD
MS-7592
Intel ICH7 - LPC & ATA & USB & GPIO
Rev 2.0
Date: Sunday, January 04, 2009
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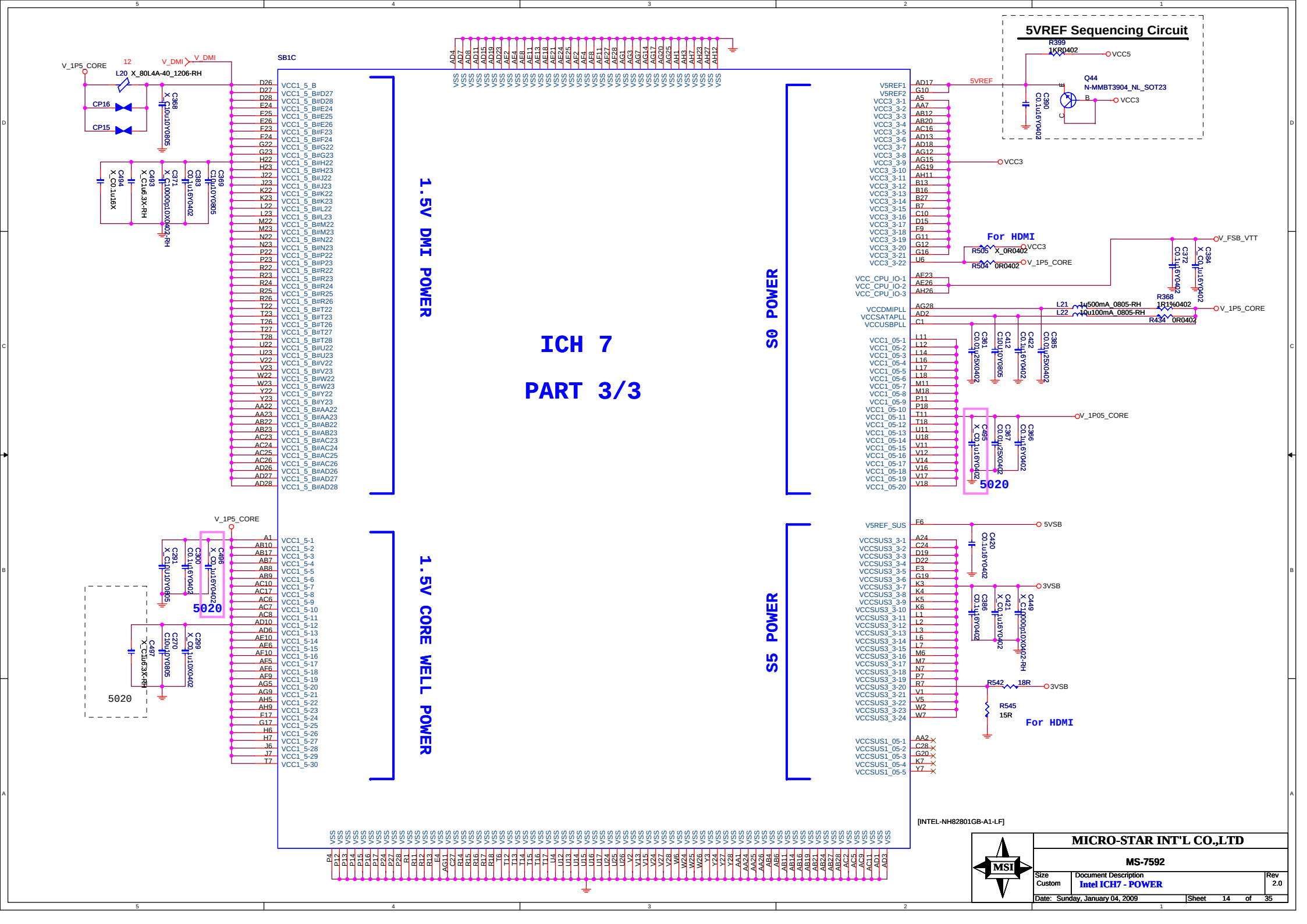
ICH 7
PART 3/3
1.5V DMI POWER
1.5V CORE WELL POWER
S0 POWER
S5 POWER
SB1C
5VREF Sequencing Circuit
For HDMI
For HDMI
5020
5020
[INTEL-NH82801GB-A1-LF]
MICRO-STAR INT'L CO.,LTD
MS-7592
Intel ICH7 - POWER
Size Custom
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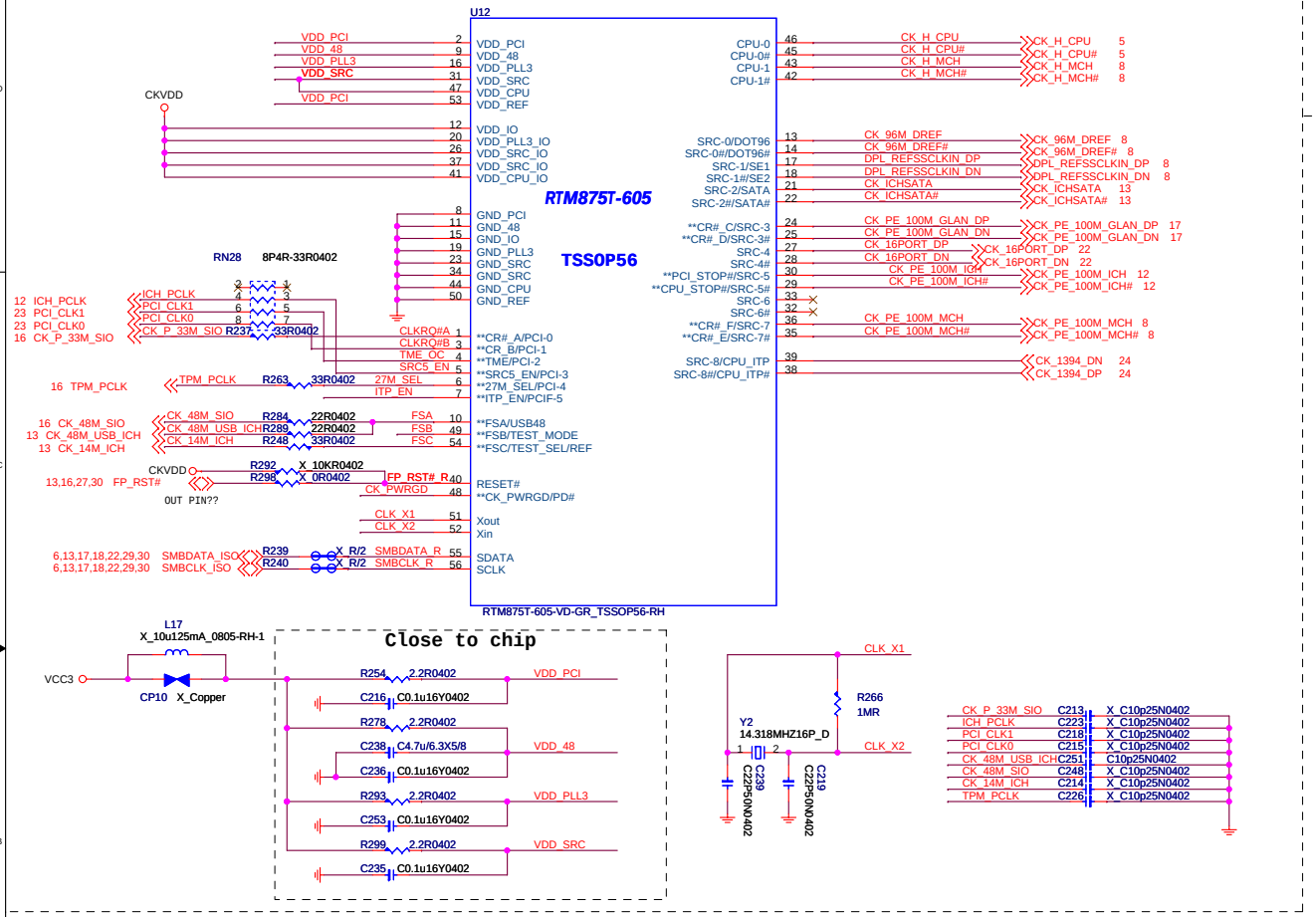
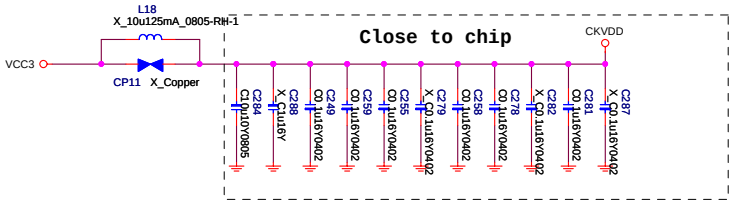
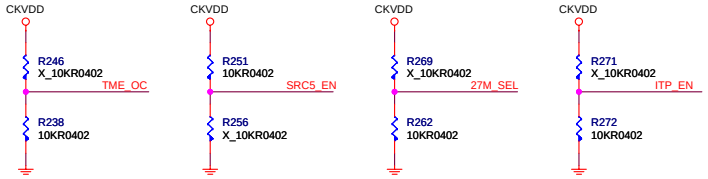
Clock Generator - RTM875T-605

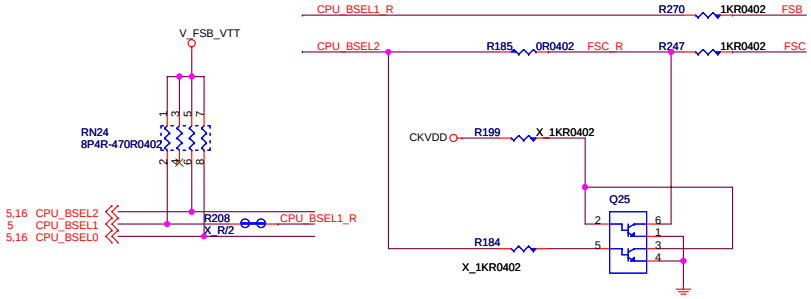




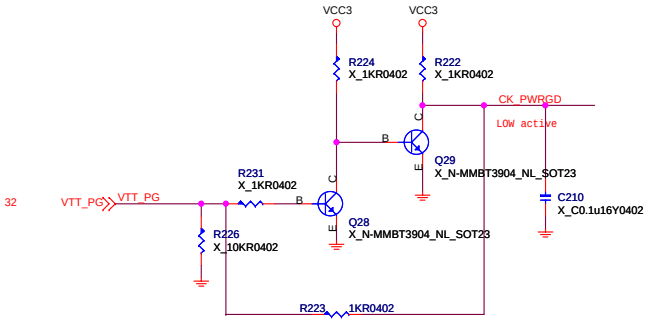
STRAPPING RESISTOR

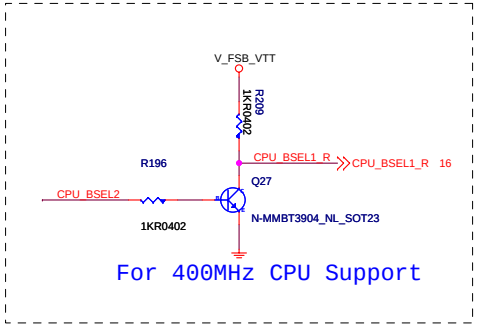


	0	1
TME_OC	Normal Run	No Overclocking
SRC5_EN	Pin29/30 is PCI STOP/CPU STOP	Pin29/30 is SRC 5
27M_SEL	Pin17/18 is SRC 1	Pin17/18 is 27MHz
ITP_EN	Pin38/39 is SRC 8	Pin38/39 is CPUITP



Clock Generator Power Good Block

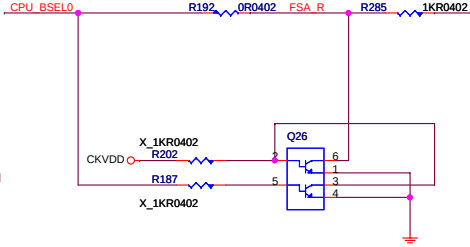


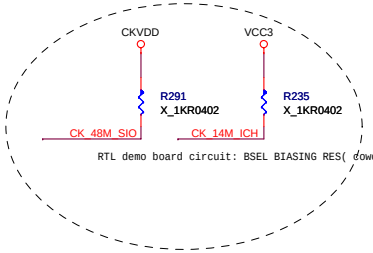


CPU Frequency Selection

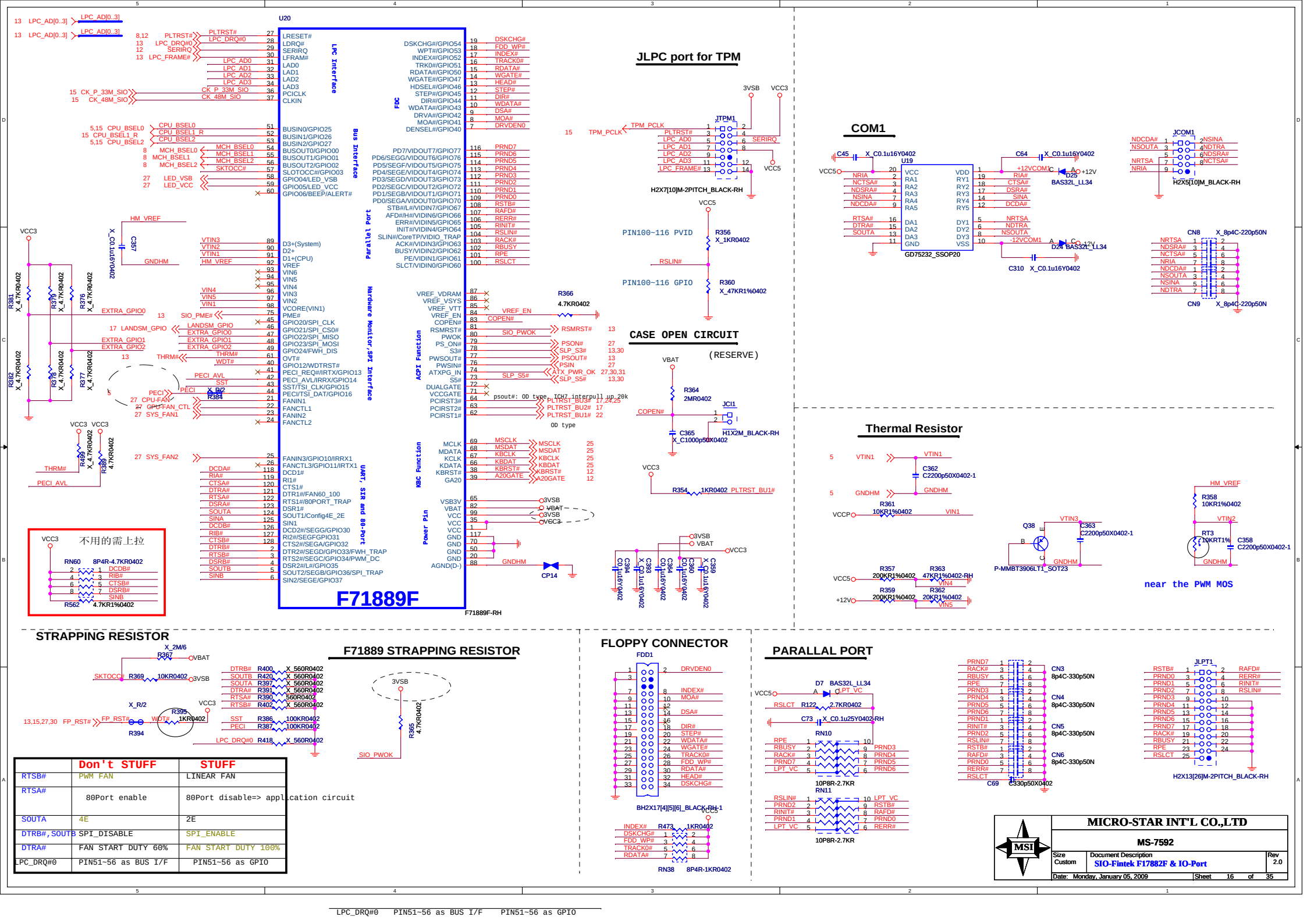
FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid





MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7592		
	Size: Custom	Document Description: CLK-RTM 875T-605	Rev: 2.0
	Date: Sunday, January 04, 2009	Sheet 15 of 35	



	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80Port enable	80Port disable=> application circuit
SOUTA	4E	2E
DTRB#,SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LPC_DRQ#0	PIN51~56 as BUS I/F	PIN51~56 as GPIO

LPC_DRQ#0 PIN51~56 as BUS I/F PIN51~56 as GPIO

MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: SIO-Fintek F71882F & IO-Port
Rev: 2.0	
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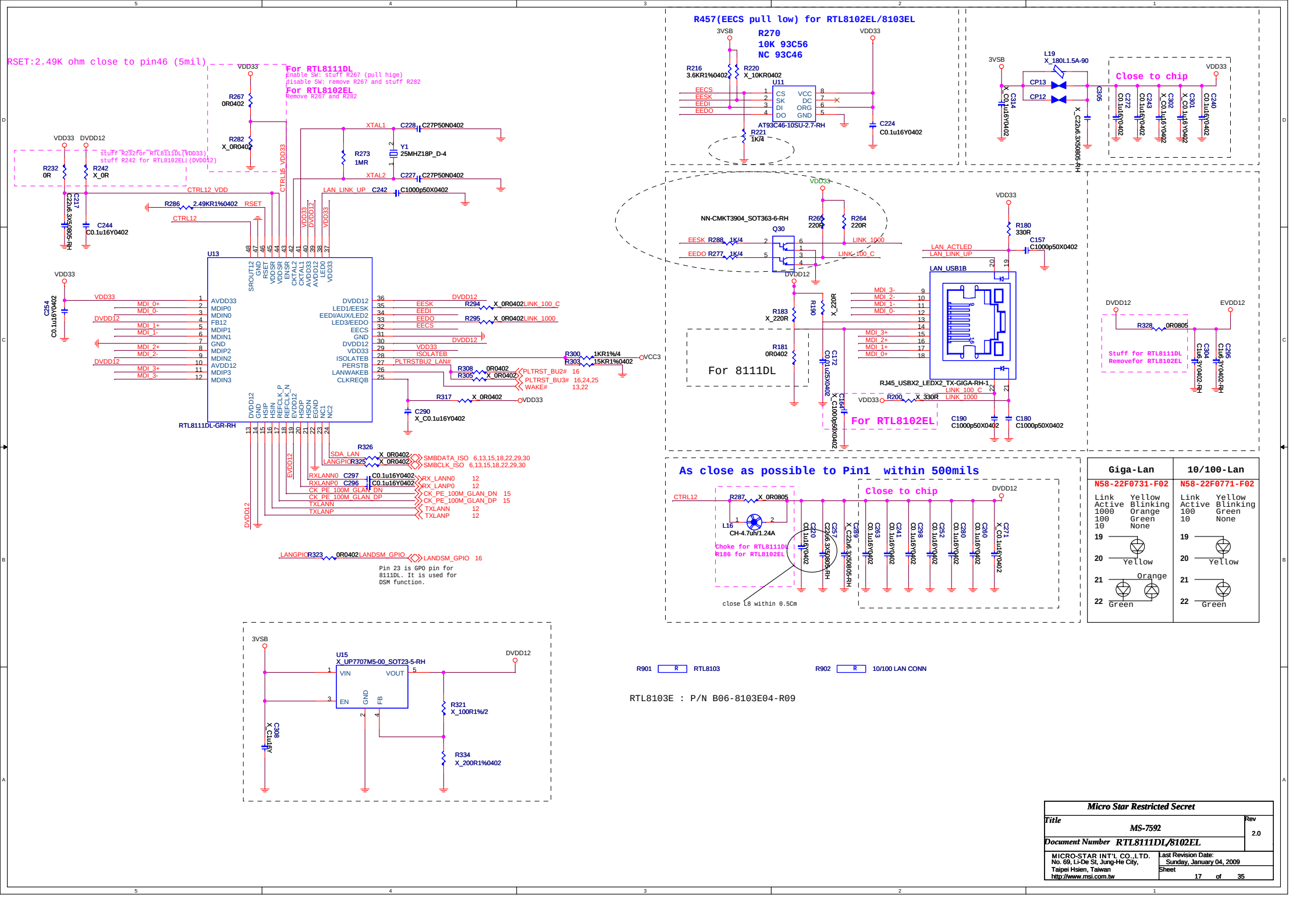
RSET:2.49K ohm close to pin46 (5mil)
For RTL8111DL
Enable SW: stuff R267 (pull hige)
disable SW: remove R267 and stuff R282
For RTL8102EL
Remove R267 and R282
stuff R232for RTL8111DL(VDD33)
stuff R242 for RTL8102EL(DVDD12)
U13
RTL8111DL-GR-RH
R457(EECS pull low) for RTL8102EL/8103EL
R270
10K 93C56
NC 93C46
AT93C46-10SU-2.7-RH
Close to chip
LAN_USB1B
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
For 8111DL
For RTL8102EL
Stuff for RTL8111DL
Removefor RTL8102EL
As close as possible to Pin1 within 500mils
Choke for RTL8111DL
R186 for RTL8102EL
close L8 within 0.5Cm
Pin 23 is GPO pin for
8111DL. It is used for
DSM function.
U15
X_UP7707M5-00_SOT23-5-RH
Giga-Lan
N58-22F0731-F02
10/100-Lan
N58-22F0771-F02
R901 R RTL8103
R902 R 10/100 LAN CONN
RTL8103E : P/N B06-8103E04-R09
Micro Star Restricted Secret
Title MS-7592
Rev 2.0
Document Number RTL8111DL/8102EL
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Sunday, January 04, 2009
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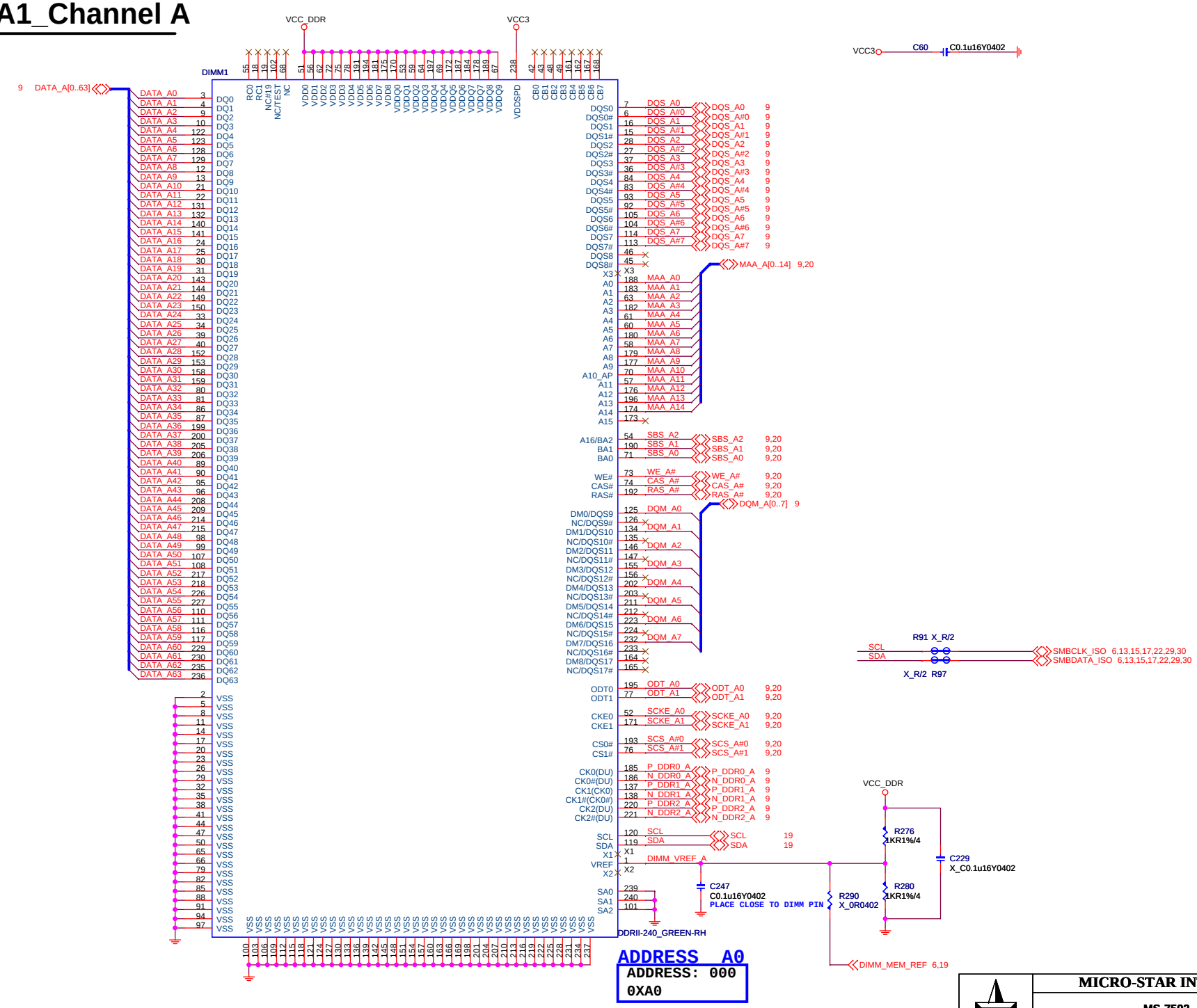
DDRII DIMM_A1_Channel A



ADDRESS A0

ADDRESS: 000
0XA0

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR II DIMM A
Rev: 2.0	
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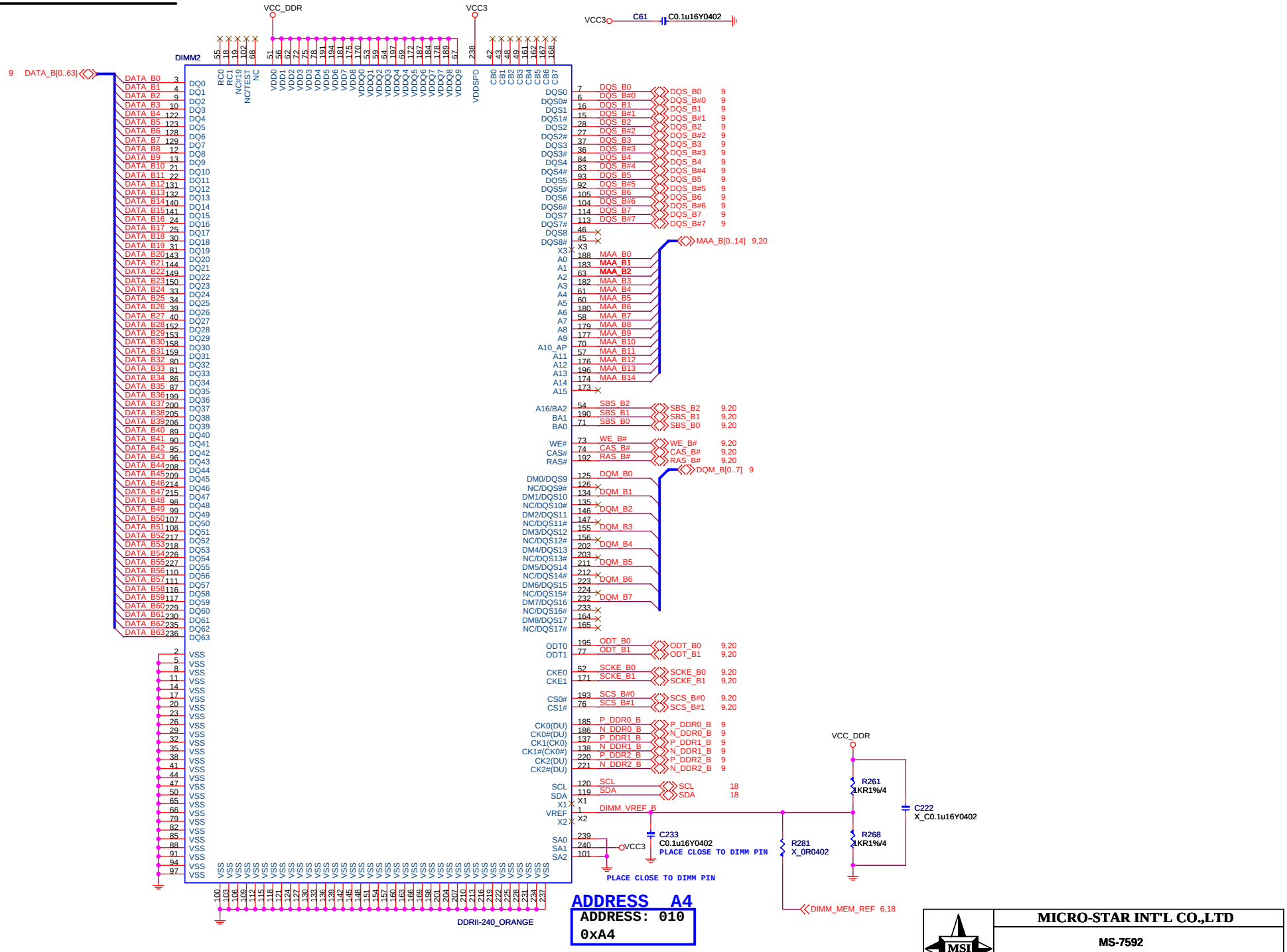
DDRII DIMM_B1_Channel B



MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: DDR II DIMM B
Rev: 2.0	
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CHANNEL A V_SM_VTT DECOUPLING CAPS

VTT_DDR
C96 X_C4.7u6.3X5
C114 X_C4.7u6.3X5

VTT_DDR
C134 X_C0.1u16Y0402
C120 X_C0.1u16Y0402
C105 X_C0.1u16Y0402

VCC_DDR
C142 X_C0.1u16Y0402

VCC5 12VIN
C207 X_C0.1u16Y0402
C56 C0.1u16Y0402

CHANNEL B V_SM_VTT DECOUPLING CAPS

VTT_DDR
C138 C4.7u6.3X5

VTT_DDR
C103 X_C0.1u16Y0402
C99 X_C0.1u16Y0402
C129 X_C0.1u16Y0402
C106 X_C0.1u16Y0402

EMI 10/29

VCC_DDR VTT_DDR
C124 X_C0.1U16Y0402
C141 X_C0.1U16Y0402
C111 X_C0.1U16Y0402
C97 X_1u/6.3V/4
C102 X_1u/6.3V/4

VTT_DDR

RN18 8P4R-33R0402
MAA_A4 MAA_A3 MAA_A2 MAA_A1

RN20 8P4R-33R0402
MAA_A7 MAA_A8 MAA_A5 MAA_A6

RN22 8P4R-33R0402
9,18 SBS_A2
MAA_A12 MAA_A11 MAA_A9 RAS_A#

RN15 8P4R-33R0402
9,18 RAS_A#
9,18 WE_A#
9,18 CAS_A#
WE_A# CAS_A# MAA_A13

MAA_A14 R165 33R0402

RN17 8P4R-33R0402
MAA_A0 SBS_A1 MAA_A10 SBS_A0
9,18 SBS_A1
9,18 SBS_A0

RN13 8P4R-43R0402
ODT_A1 SCS_A#1 ODT_A0 SCS_A#0
9,18 ODT_A1
9,18 SCS_A#1
9,18 ODT_A0
9,18 SCS_A#0

SCKE_A0 R167 43R0402
SCKE_A1 R170 43R0402
9,18 SCKE_A0
9,18 SCKE_A1

change RN

9,18 MAA_A[0..14]

VTT_DDR

RN19 8P4R-33R0402
MAA_B4 MAA_B3 MAA_B1 MAA_B2

RN21 8P4R-33R0402
MAA_B7 MAA_B8 MAA_B6 MAA_B5

RN23 8P4R-33R0402
9,19 SBS_B2
SBS_B2 MAA_B12 MAA_B11 MAA_B9

RN14 8P4R-33R0402
9,19 RAS_B#
9,19 WE_B#
9,19 CAS_B#
RAS_B# WE_B# CAS_B# MAA_B13

MAA_B14 R166 33R0402

RN16 8P4R-33R0402
MAA_B0 SBS_B1 MAA_B10 SBS_B0
9,19 SBS_B1
9,19 SBS_B0

RN12 8P4R-43R0402
ODT_B1 SCS_B#1 SCS_B#0 ODT_B0
9,19 ODT_B1
9,19 SCS_B#1
9,19 SCS_B#0
9,19 ODT_B0

SCKE_B0 R171 43R0402
SCKE_B1 R169 43R0402
9,19 SCKE_B0
9,19 SCKE_B1

change RN

9,19 MAA_B[0..14]

VCC_DDR VCC_DDR
C140 X_C0.1u16Y0402
C92 X_C0.1u16Y0402
C476 X_C4.7u6.3X5
C276 X_1u/6.3V/4
C100 X_1u/6.3V/4
C85 X_1u/6.3V/4
C147 X_1u/6.3V/4
C182 X_1u/6.3V/4
C187 X_1u/6.3V/4
C469 X_1u/6.3V/4

VCC_DDR
C115 1u/6.3V/4
C104 X_1u/6.3V/4
C143 X_1u/6.3V/4
C470 X_1u/6.3V/4
C165 1u/6.3V/4
C112 X_1u/6.3V/4
C212 X_1u/6.3V/4

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ALC888 CODEC

FOR 6 Port

FOR 6 Port

Trace Width 20mils.

Pin4 : stuff for ALC888-VC2
Pin4 : remove for ALC888S-VC2

U22 ALC888-GR-A2-RH

R458 20KR1%0402

R457 X_10KR0402 ; only for ALC 883

CD/IN HEADERS

CD_IN1 BH1X4_BLACK-RH

RN53 8P4R-10KR0402

RN51 8P4R-47KR0402

Azalia Front Audio Connector

D23 S-BAT54A_SOT23

D22 S-BAT54A_SOT23

RN52 8P4R-75R

RN50 8P4R-4.7KR0402

JAUD1 H2X5[8]M_BLACK-RH

CN10 8p4C-470p50N

Place those component close to audio connector.

ALC888 JACK

3 hole : line1/Mic1 change to 75 ohm

R903 R 3hole

AUDIO1A (Upper)

X_JACK-AUDIOX6-26P_L-pbg_R-obl AUDIO1B(Middle)

X_JACK-AUDIOX6-26P_L-pbg_R-obl AUDIO1C (Down)

X_JACK-AUDIOX6-26P_L-pbg_R-obl

470P

AUDIO2A (Upper)

JACK-AUDIOX6-26P_L-pbg_R-obl AUDIO2B(Middle)

JACK-AUDIOX6-26P_L-pbg_R-obl AUDIO2C (Down)

JACK-AUDIOX6-26P_L-pbg_R-obl

470P

FOR 6 Port

ALC883 JACK DETECT

SPDIF OUT

JSPD1 BH1X3_BLACK-RH

AUDIO CODE REGULATORS

FOR 6 Port

Trace Width 30mils.

U23 LT1087S_SOT89

For EMI

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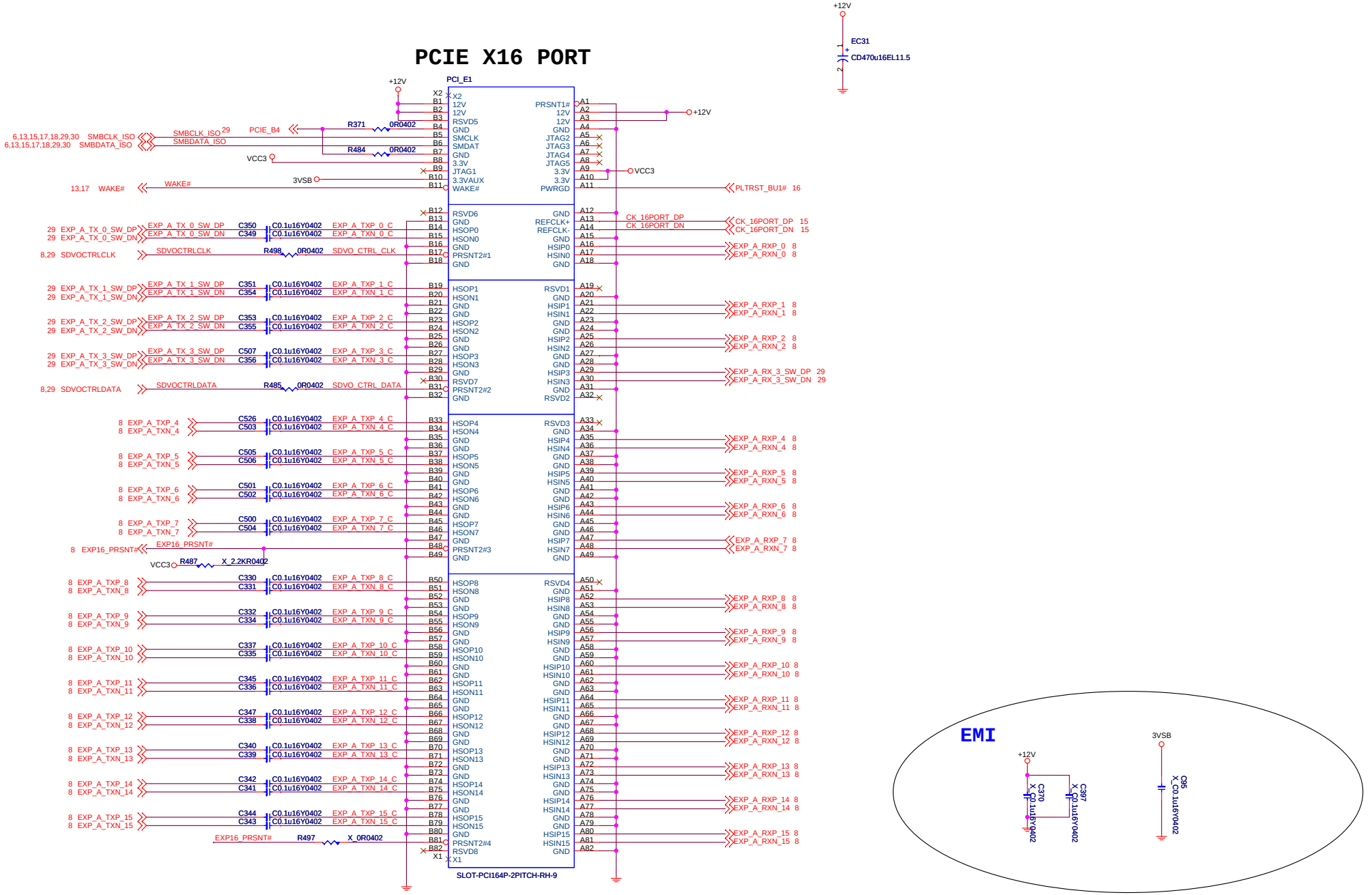
PCIE X16 PORT



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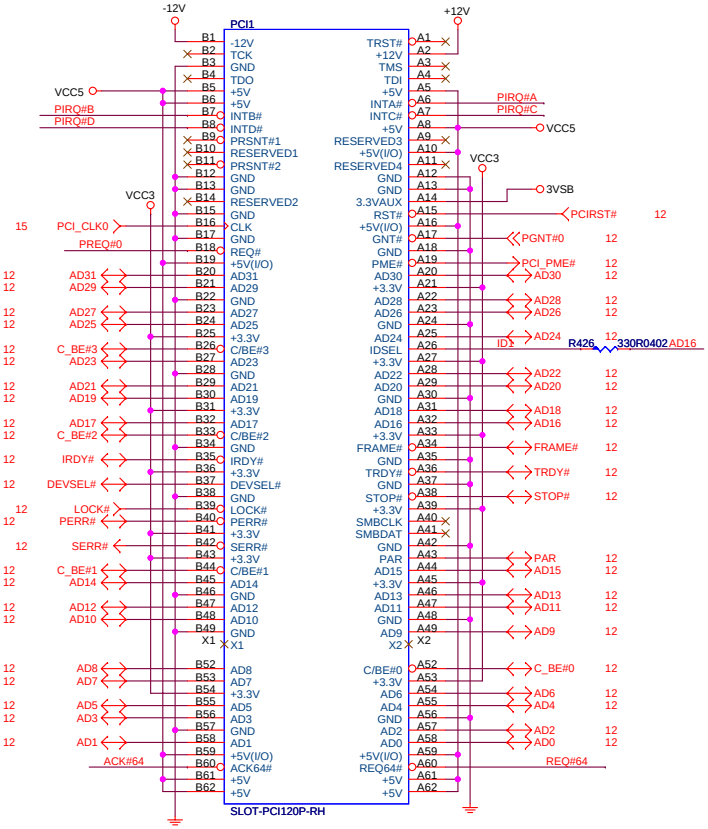
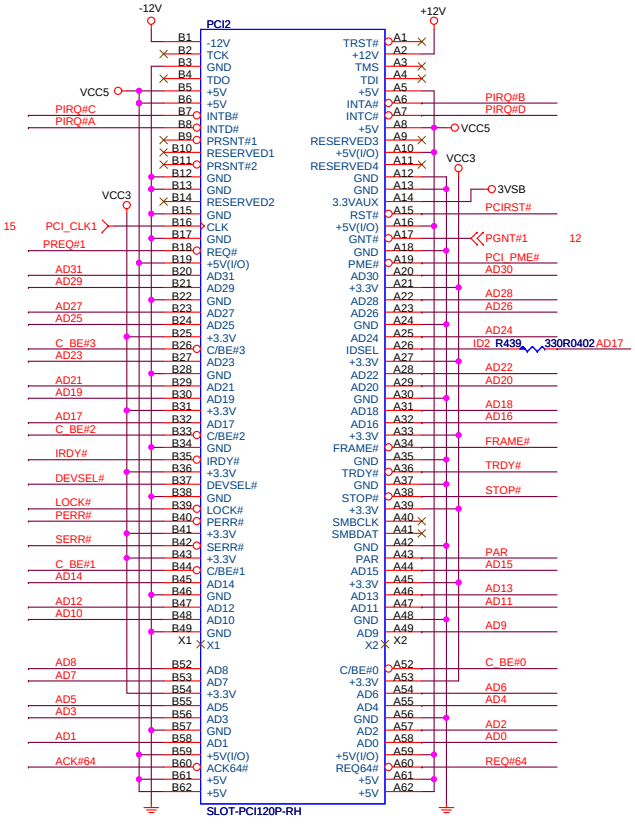
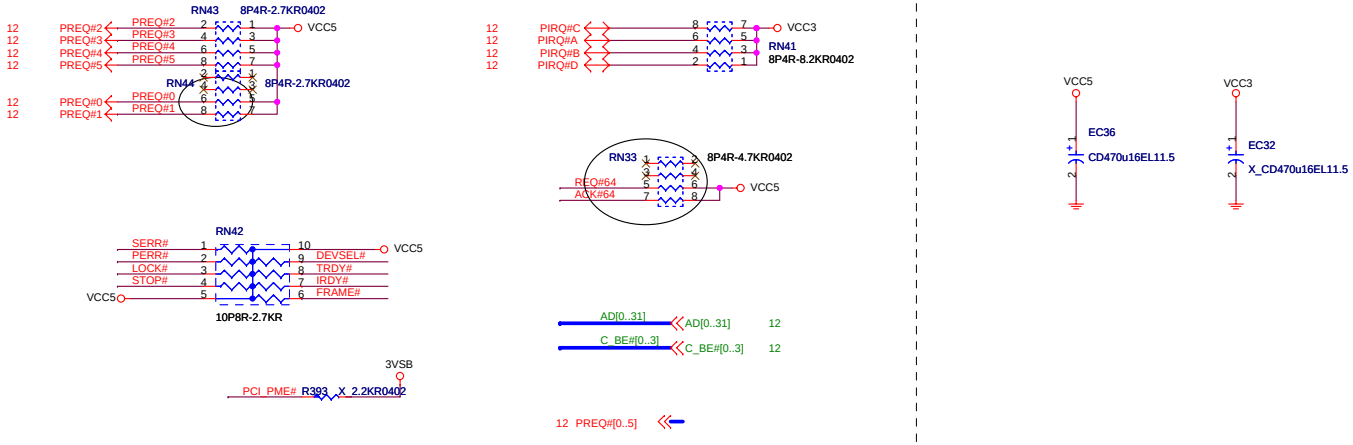
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



PCI PULL-UP / DOWN RESISTORS



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Size: Custom	Document Description: PCI Slot 1 &2	Rev: 2.0
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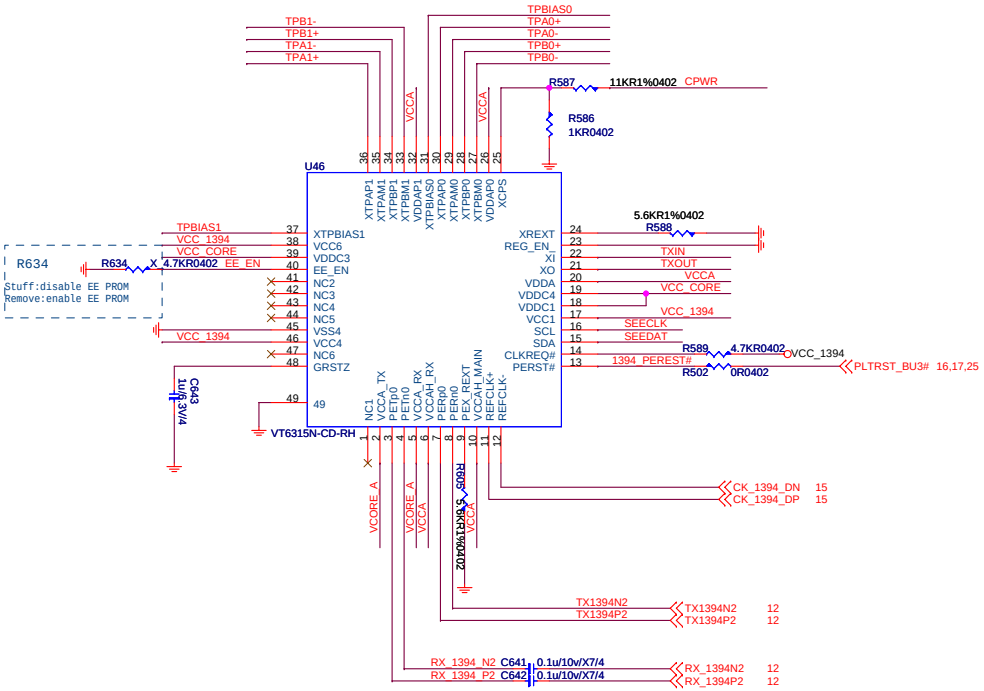
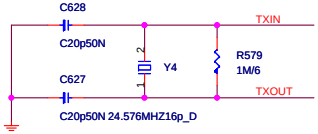
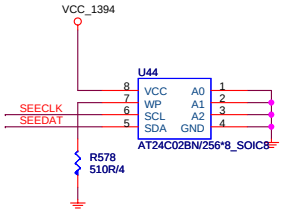
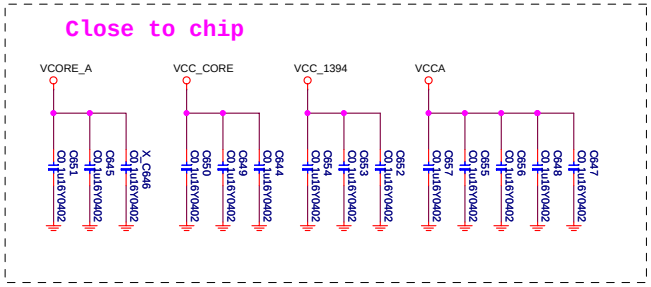
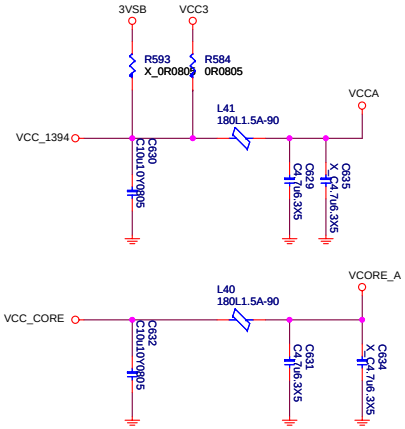
1394 CONTROLLER



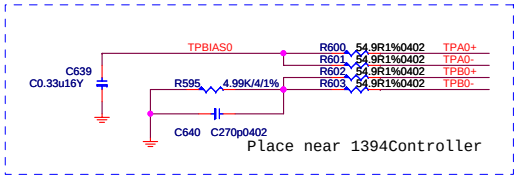


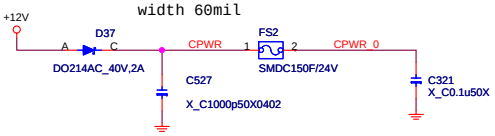


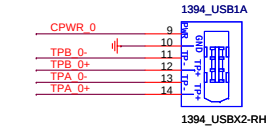




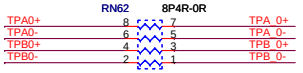
Rear 1394 port

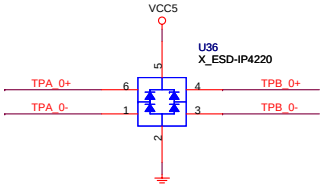




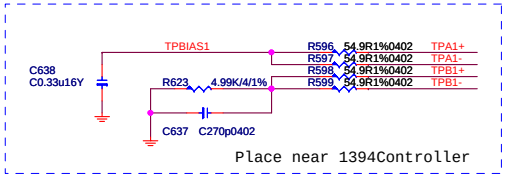


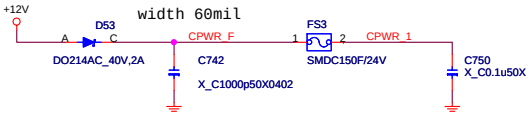
N58-14M0031-L06

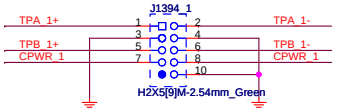




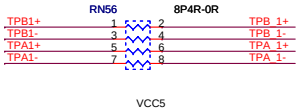
Front 1394 pin header

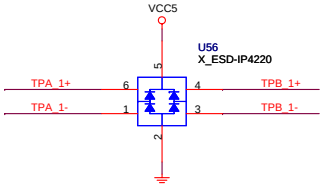






N31-2051551-H06





VT6315N

Power domain chart

PIN Name	PIN NO.	Description
VCC	*17,46,38*	PCIE power 3.3V
VCC_A	*6,10,20,26,32*	Analog power 3.3V
VCORE	*18,19,39*	Core power 1.2V
EVDD12	*2,5*	Analog core power 1.2V

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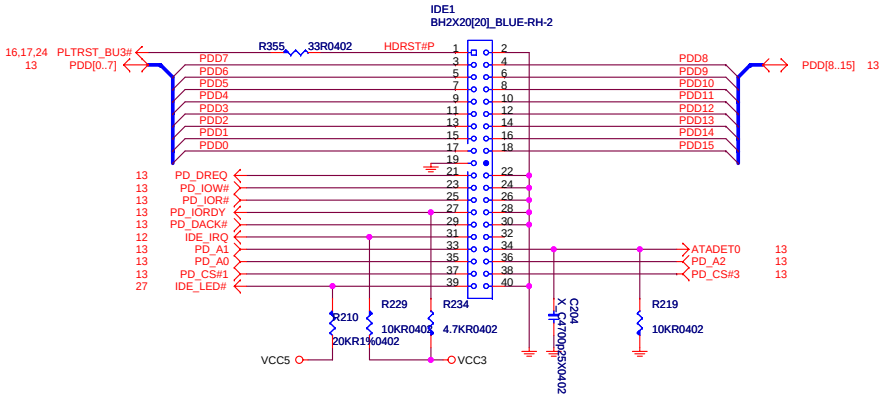
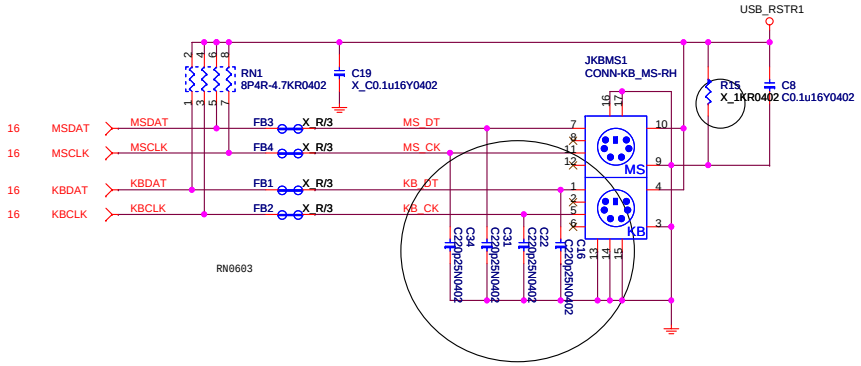
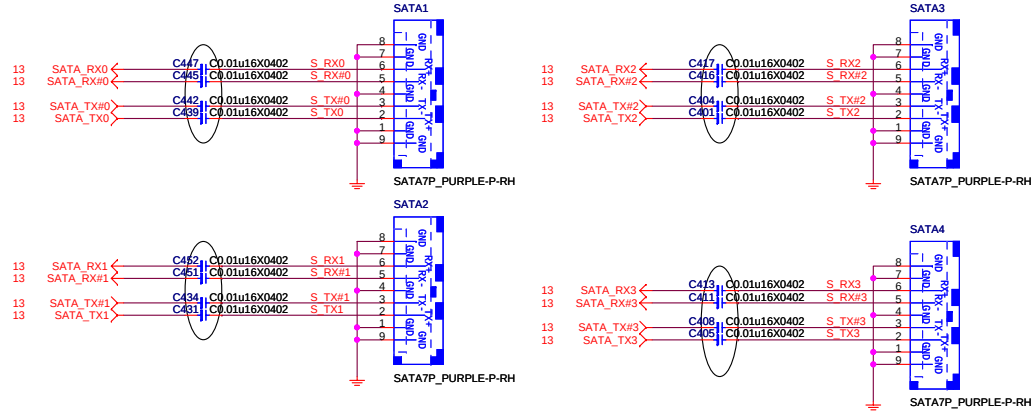
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK



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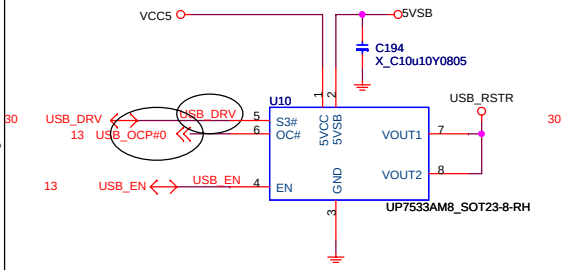
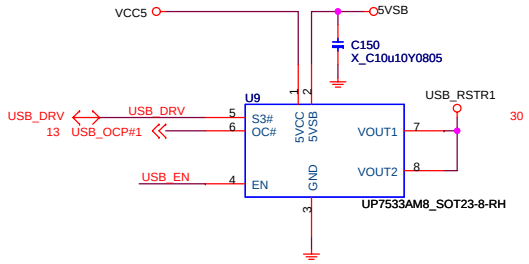
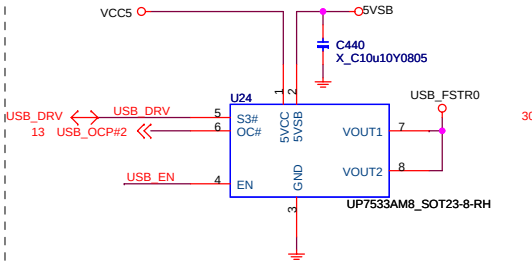
POWER CIRCUIT FOR USB PORT 0,1



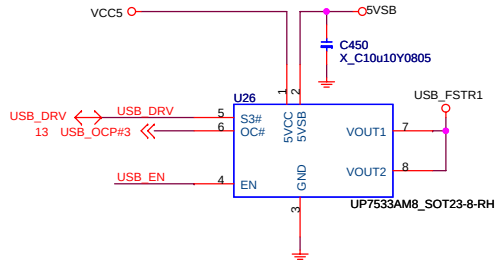
POWER CIRCUIT FOR USB PORT 2,3



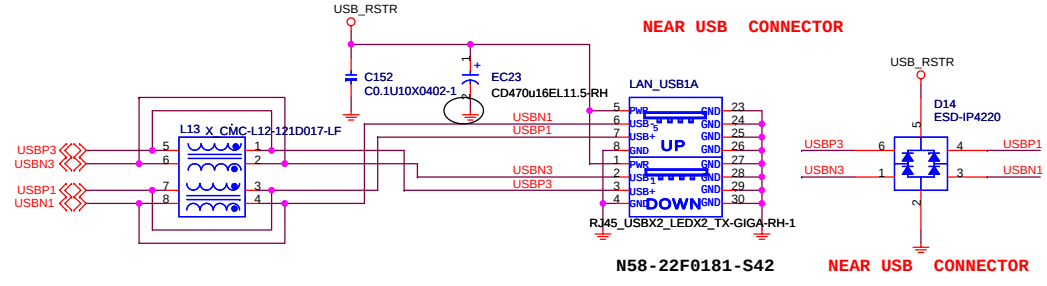
POWER CIRCUIT FOR USB PORT 4,5



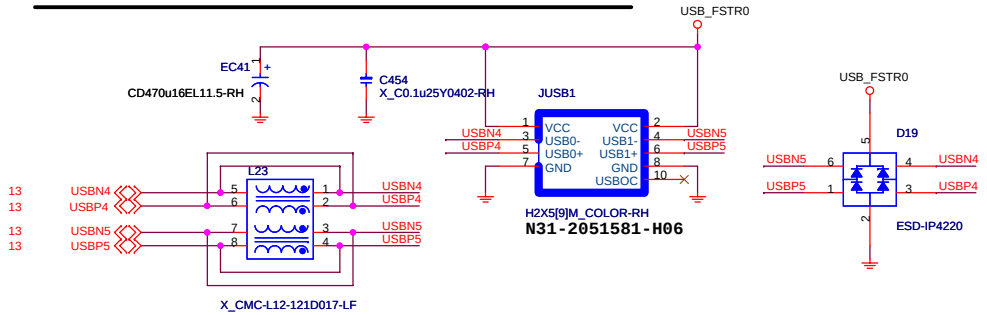
POWER CIRCUIT FOR USB PORT 6,7



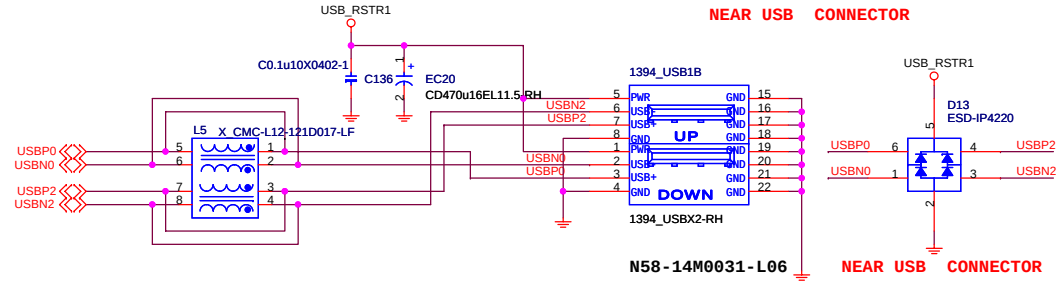
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



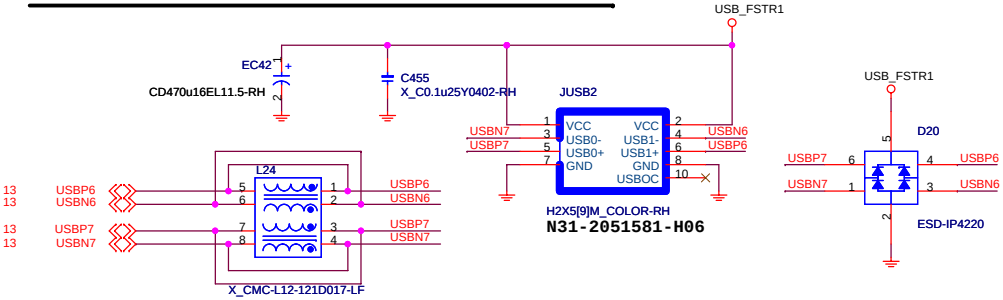
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



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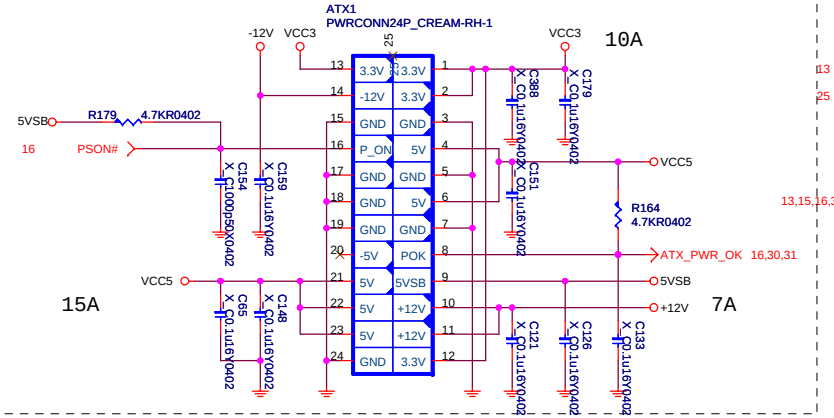
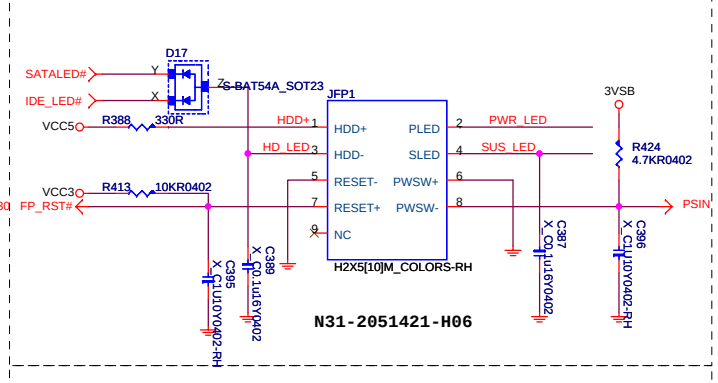
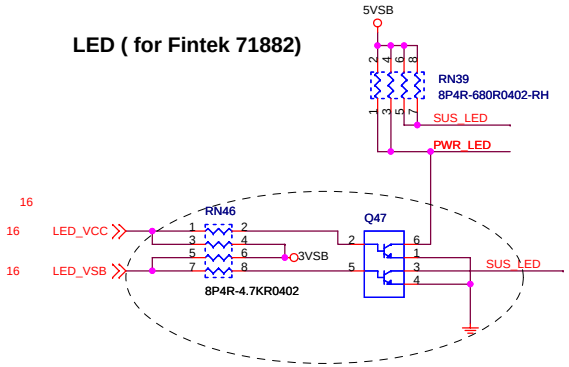
ATX Connector



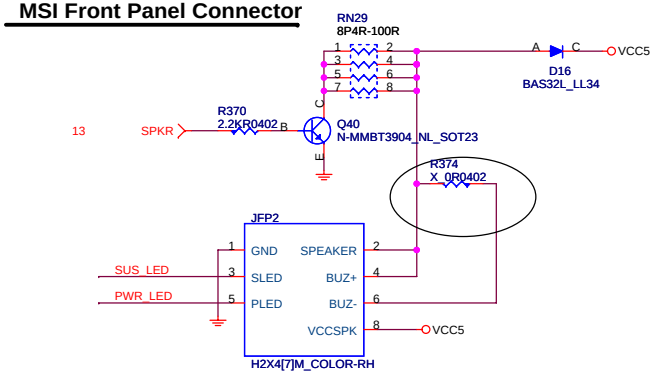
INTEL/PB Front Panel Connector



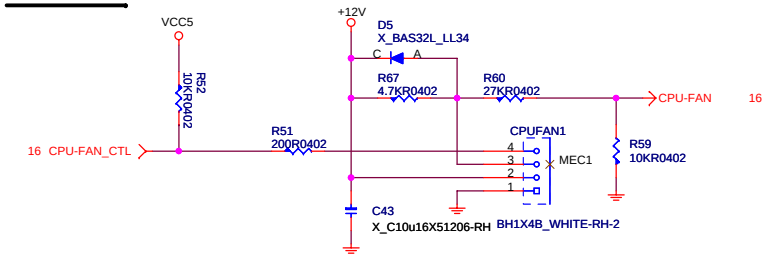
LED (for Fintek 71882)



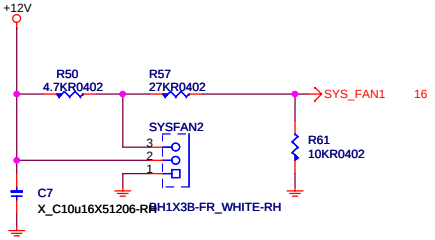
MSI Front Panel Connector



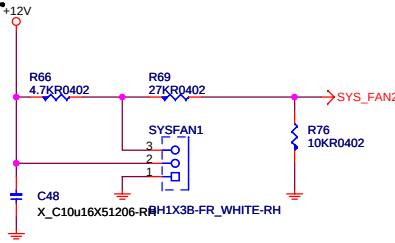
CPU FAN



SYSTEM FAN



PWR FAN



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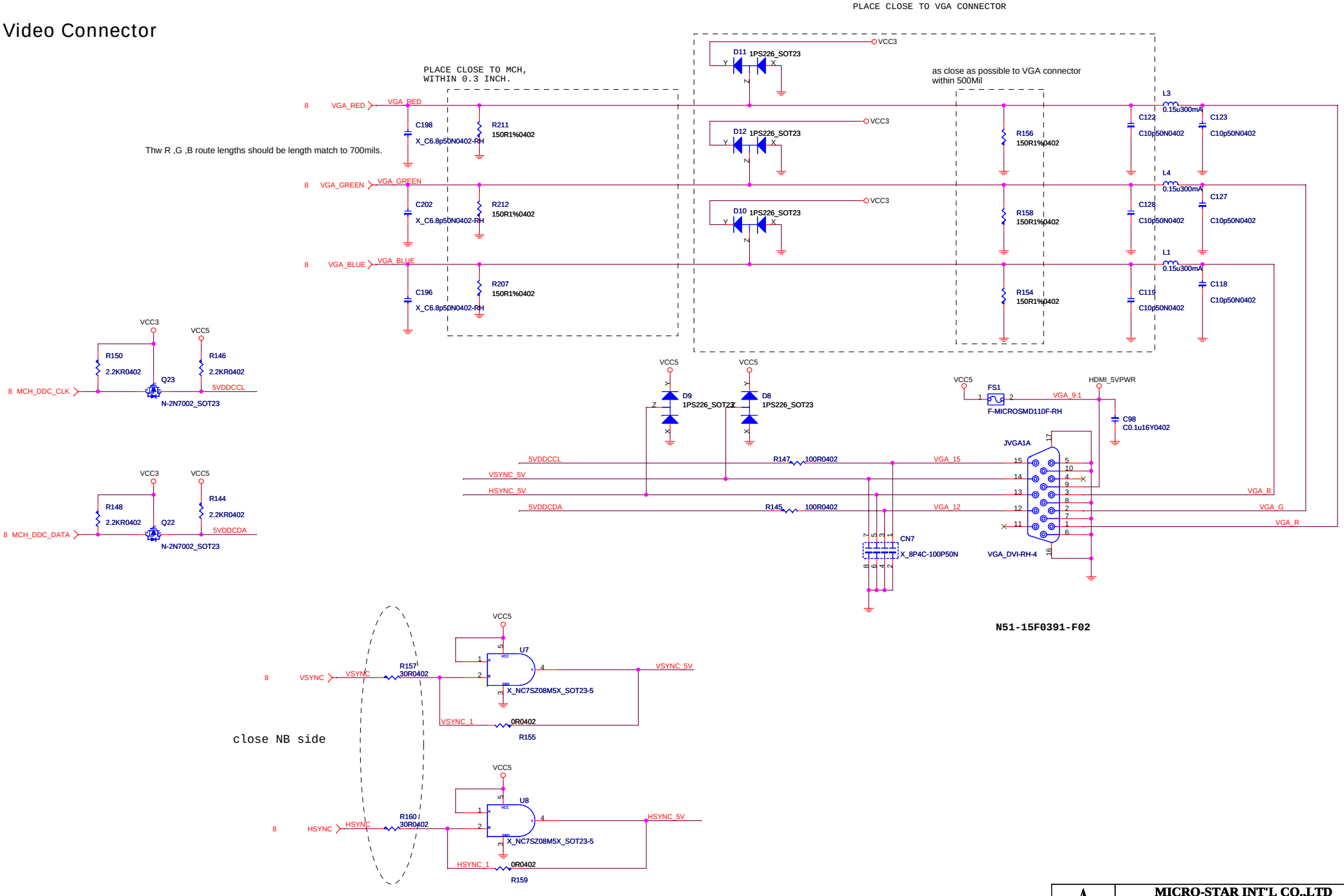
Video Connector



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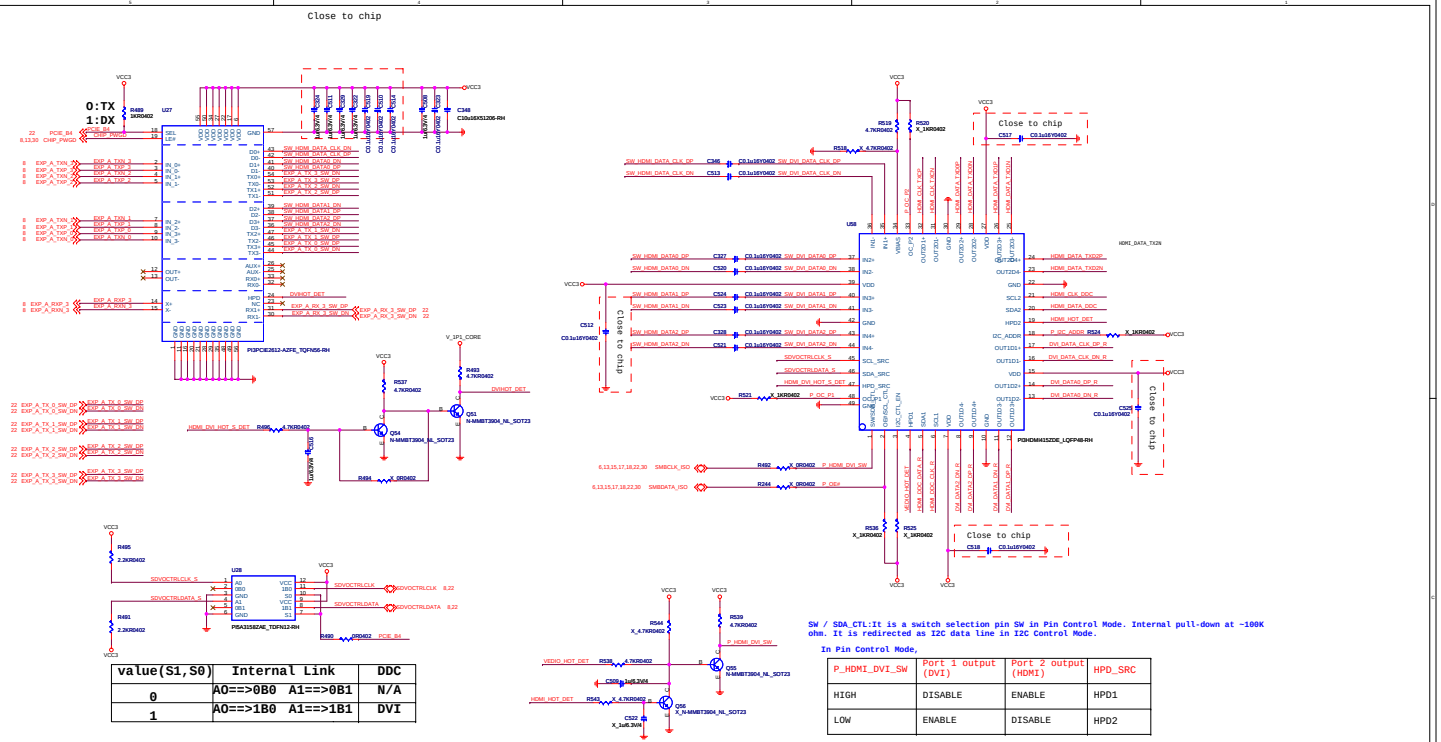
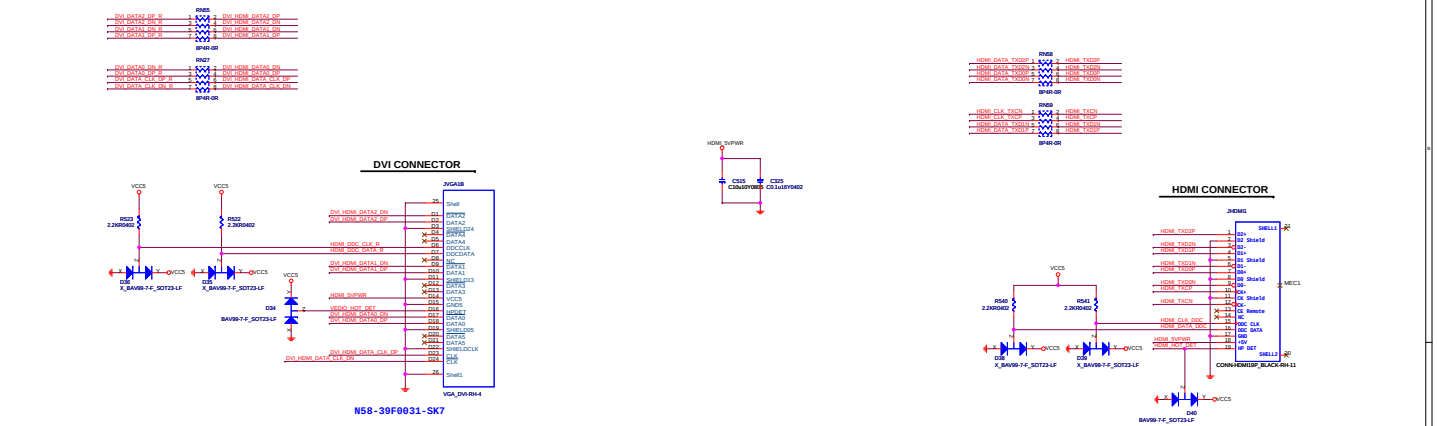


value(S1,S0)	Internal Link	DDC
0	AO==>0B0 A1==>0B1	N/A
1	AO==>1B0 A1==>1B1	DVI

P_HDMI_DVI_SW	Port 1 output (DVI)	Port 2 output (HDMI)	HPD_SRC
HIGH	DISABLE	ENABLE	HPD1
LOW	ENABLE	DISABLE	HPD2



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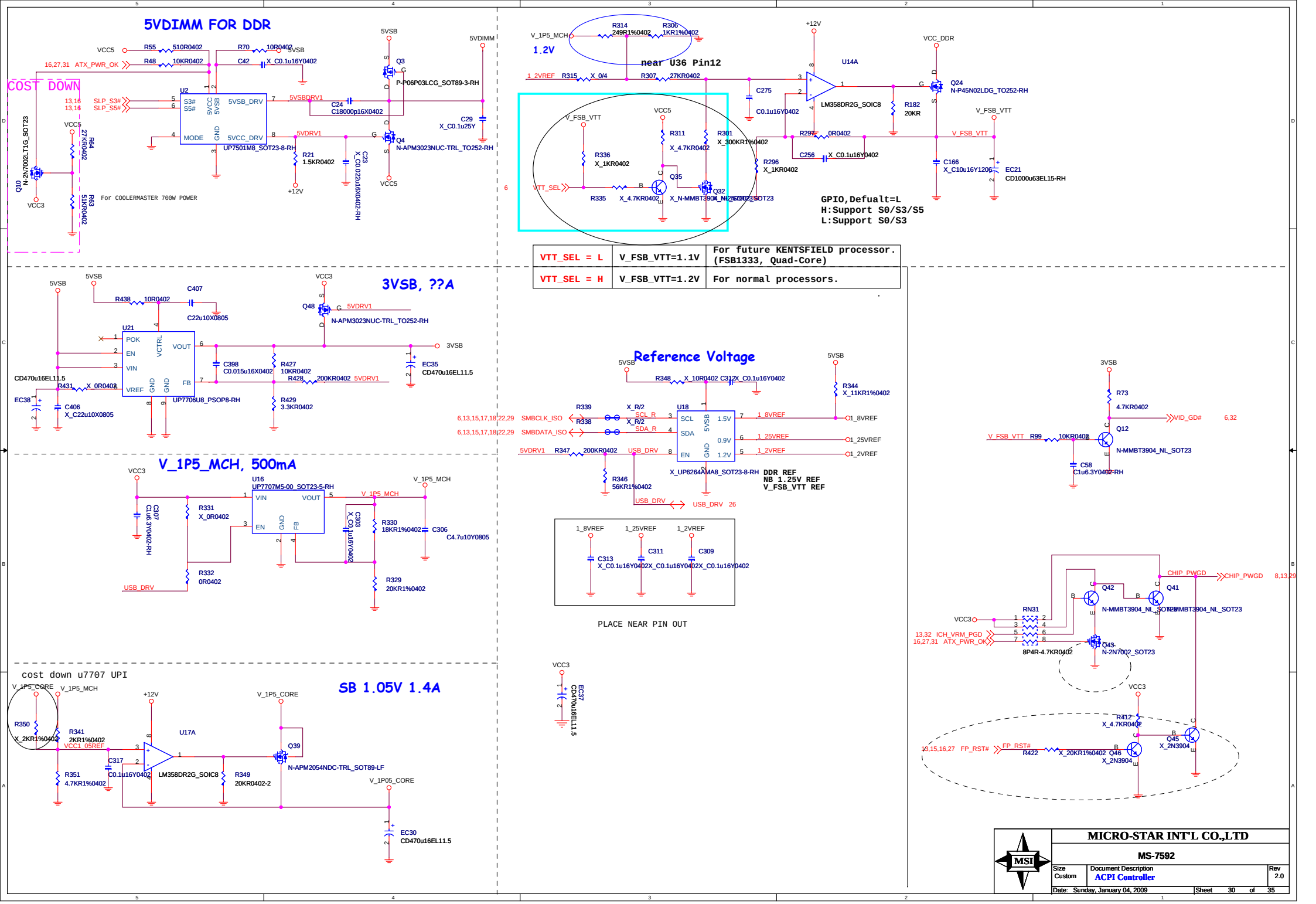
5VDIMM FOR DDR
COST DOWN
U2
UP7501M8_SOT23-8-RH
Q3
P-P06P03LCG_SOT89-3-RH
Q4
N-APM3023NUC-TRL_TO252-RH
Q10
N-2N7002LT1G_SOT23
For COOLERMASTER 700W POWER
1.2V
near U36 Pin12
U14A
LM358DR2G_SOIC8
Q24
N-P45N02LDG_TO252-RH
GPIO,Defualt=L
H:Support S0/S3/S5
L:Support S0/S3
VTT_SEL = L
V_FSB_VTT=1.1V
For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H
V_FSB_VTT=1.2V
For normal processors.
3VSB, ??A
U21
UP7706U8_PSOP8-RH
Q48
N-APM3023NUC-TRL_TO252-RH
Reference Voltage
U18
X_UP6264AMA8_SOT23-8-RH
DDR_REF
NB 1.25V REF
V_FSB_VTT REF
PLACE NEAR PIN OUT
V_1P5_MCH, 500mA
U16
UP7707M5-00_SOT23-5-RH
cost down u7707 UPI
SB 1.05V 1.4A
U17A
Q39
N-APM2054NDC-TRL_SOT89-LF
Q12
N-MMBT3904_NL_SOT23
Q41
Q42
Q43
N-2N7002_SOT23
Q45
X_2N3904
Q46
X_2N3904
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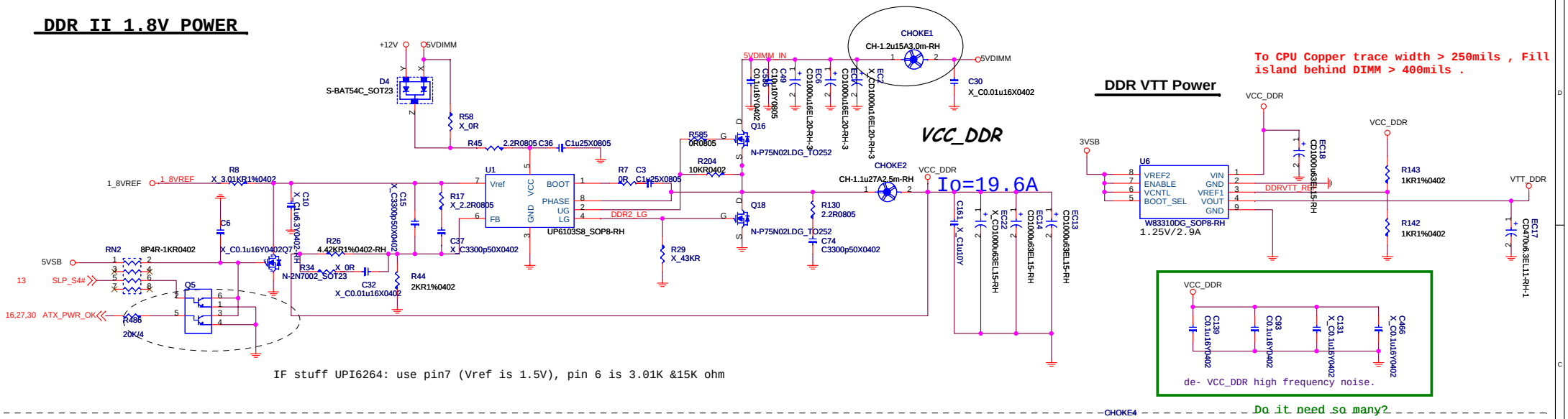
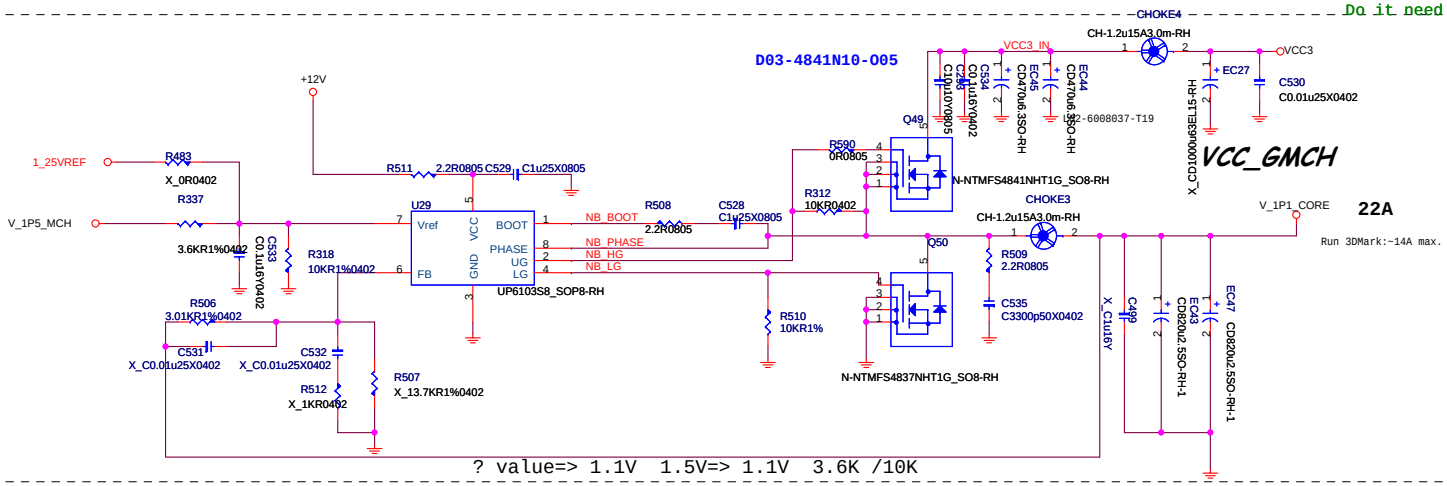
DDR II 1.8V POWER



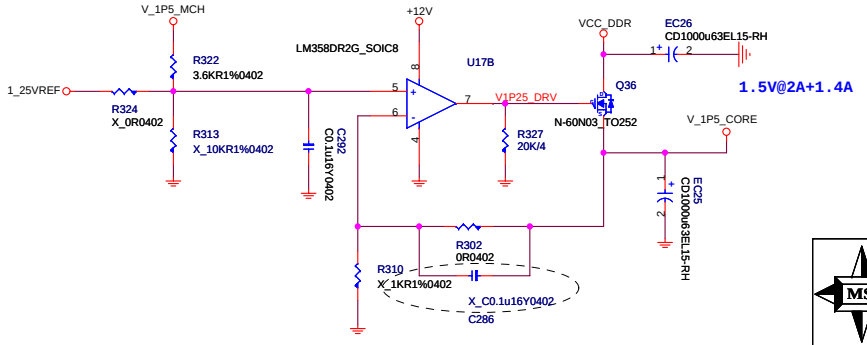
IF stuff UPI6264: use pin7 (Vref is 1.5V), pin 6 is 3.01K &15K ohm

MCH-G41 1.1V Core Power



? value=> 1.1V 1.5V=> 1.1V 3.6K /10K

ICH-ICH7 1.5V Core Power



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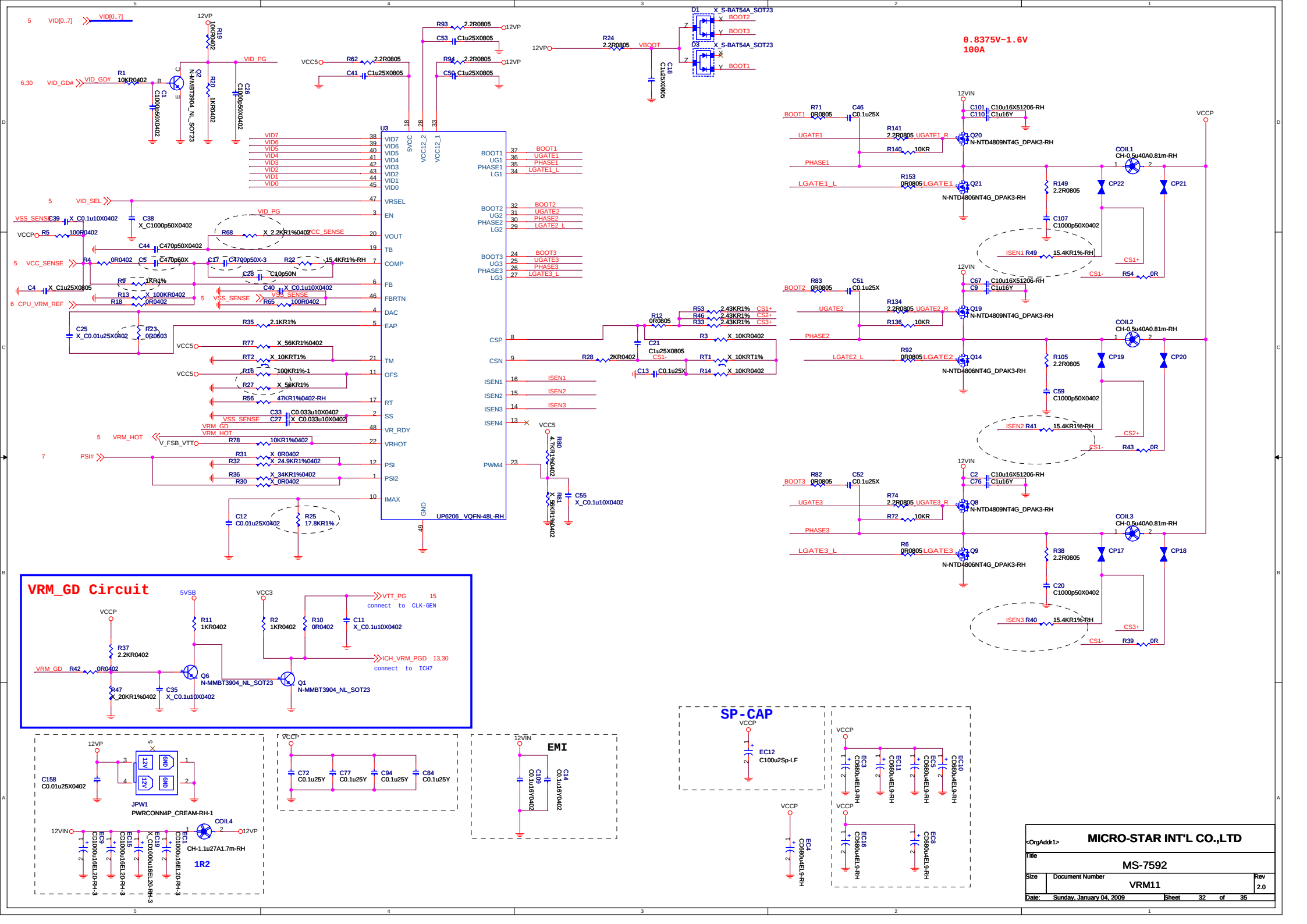
0.8375V~1.6V
100A
U3
UP6206_VQFN-48L-RH
VRM_GD Circuit
SP-CAP
EMI
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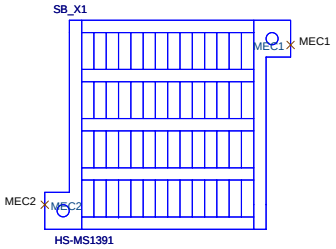
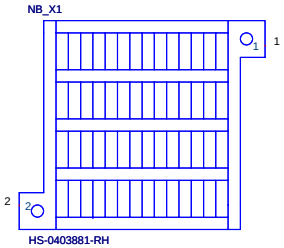
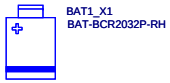
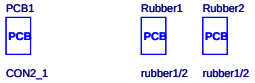
ICH7 HEATSINK



MCH HEATSINK

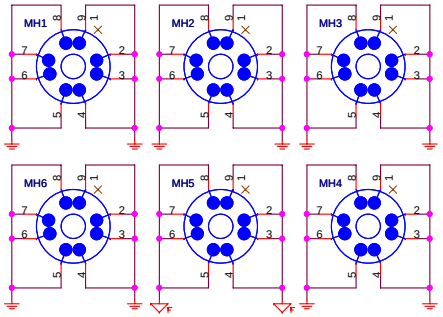




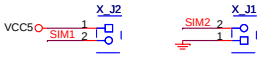


P80-075920A-E48
P80-075920A-G37

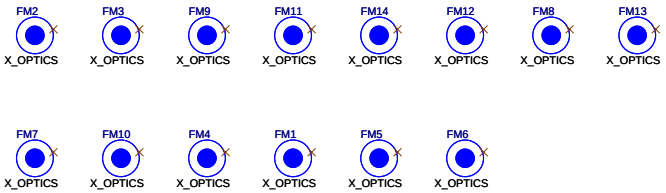
Mounting Holes



Simulation



Optics Orientation Holes



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ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPI0(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OOD12t	
GPIO6	SLOTOCC#	55	GPO	I/OOD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OOD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OOD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OOD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OOD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OOD12t	

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JCI1	*Chassis Intrusion*
Open	Normal
(1-2)	Chassis Open

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

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2.0 Change list:

1.LPT and COM : reserve by Pin header (default on board)
2.Add DVI and HDMI function,add R505 R504 R542 R545
3.Change R245 R259 value
4.Change R22 C17 R49 R41 R40 C28 R35 R16 R25 R53 R46 R33 COIL3 COIL2 COIL1 value
5.Delete C635 C633 reserver C646 ,change R593 R584 footrpint to R0805

2008/12/25

1.swap CK_PE_100M_ICH/CK_PE_100M_ICH# and CK_1394_DN/CK_1394_DP
2.Swap RN58 RN59 RN55 RN27
3.For EMI require,delete L30 L31 L32 L33 L34 L35 L36 L37
4.Swap RN27 RN55 RN59
5.delete RN70 RN69,add R596-R603

2008/12/29

1.swap RN49 RN63 RN64
2.For power,change R40、R54、R43、R39、R35 footprint
3.For power,change coil4 footprint&PN.
4.Change G41 pin AR2 AG2 power,modify C225 C221 cap

2009/01/04

1.add R585 R204 R590 R312 C536 C293 EC27

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