

P50CA0 Schematics : Revision : B2 LF

82GP50105-B2 SMT+MI M/B ASSY P50CA0 REV.B2 LF

(37GP50100-B2 PCB MAIN BD FOR P50CA0 REV:B2)

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9. K8T890 - HOST -1
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24. IT8510E - 1
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26. +3.3V,+5V & +12V
27. +2.6V,+1.3V & +1.8V(LDO)
28. +1.5V,+1.2V & +2.5V(LDO)
29. VCC_CORE (ISL6559)
30. INPUT & BATTERY CHARGER
31. VCC_MOSFET

Power Rail

| | |
|-------------|---|
| +VCC_CORE | Core voltage for Processor(off in S3-S5) |
| +V2.6 | 2.6V rail for Processor DDR VDDIO(off in S4-S5) |
| +V1.3 | 1.3V rail for Processor DDR VTT(off in S4-S5) |
| +V2.5S | 2.5V switched power rail (off in S3-S5) |
| +V2.5 | 2.5V switched power rail (off in S4-S5) |
| +V1.2S | 1.2V rail for Processor VLDT(off in S3-S5) |
| +V1.5S | 1.5V switched power rail (off in S3-S5) |
| +V1.5 | 1.5V power rail (off in S4-S5) |
| +V1.8S | 1.8V switched power rail (off in S3-S5) |
| +V3.3ALWAYS | 3.3V always on power rail |
| +V3.3S | 3.3V switched power rail (off in S3-S5) |
| +V3.3 | 3.3V power rail (off in S4-S5) |
| +V5ALWAYS | 5V always on power rail |
| +V5S | 5V switched power rail (off in S3-S5) |
| +V5 | 5V power rail (off in S4-S5) |
| +V12ALWAYS | 12V always on power rail |

+V□□ALWAYS

Always on power rail

+V□□

Switched power rail (off in S4 - S5)

+V□□S

Switched power rail (off in S3 - S5)

PCI Resure Allocation

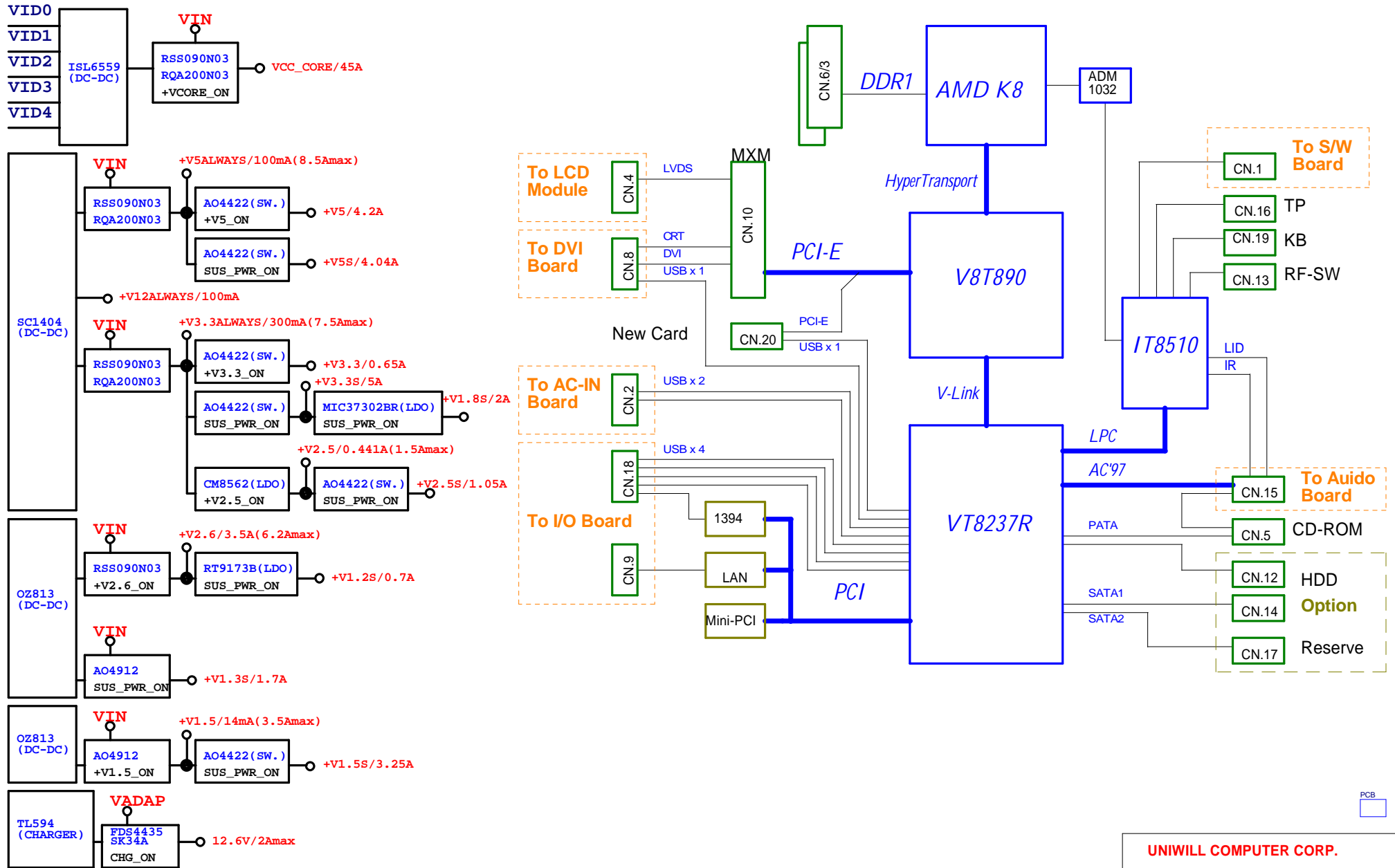
| Device | IDSEL | REQ/GNT# | INT |
|-----------|-------|----------|-----|
| IEEE 1394 | AD19 | 0 0 | A |
| GIGA LAN | AD20 | 1 1 | B |
| MINI PCI | AD21 | 2 2 | C |
| NB | | | D |

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|-------|-------------------------|---------------|
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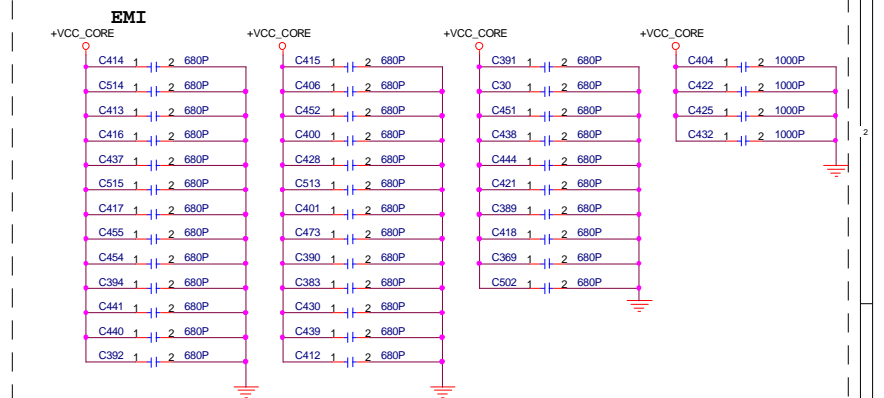
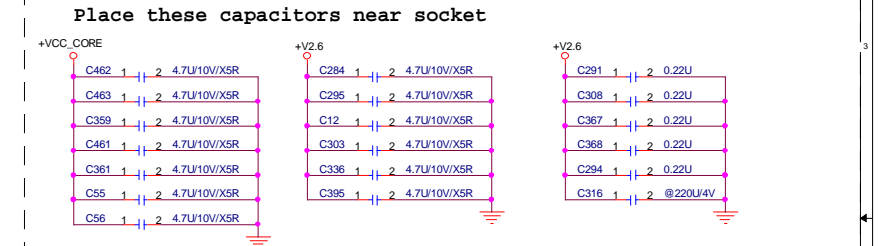
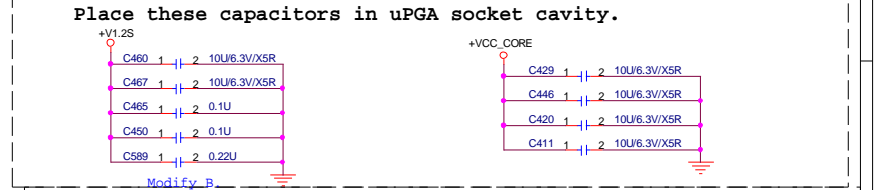
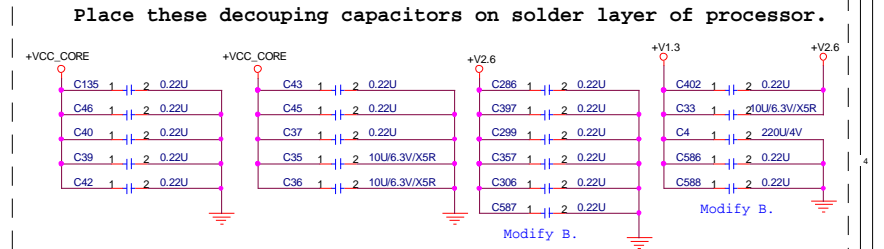
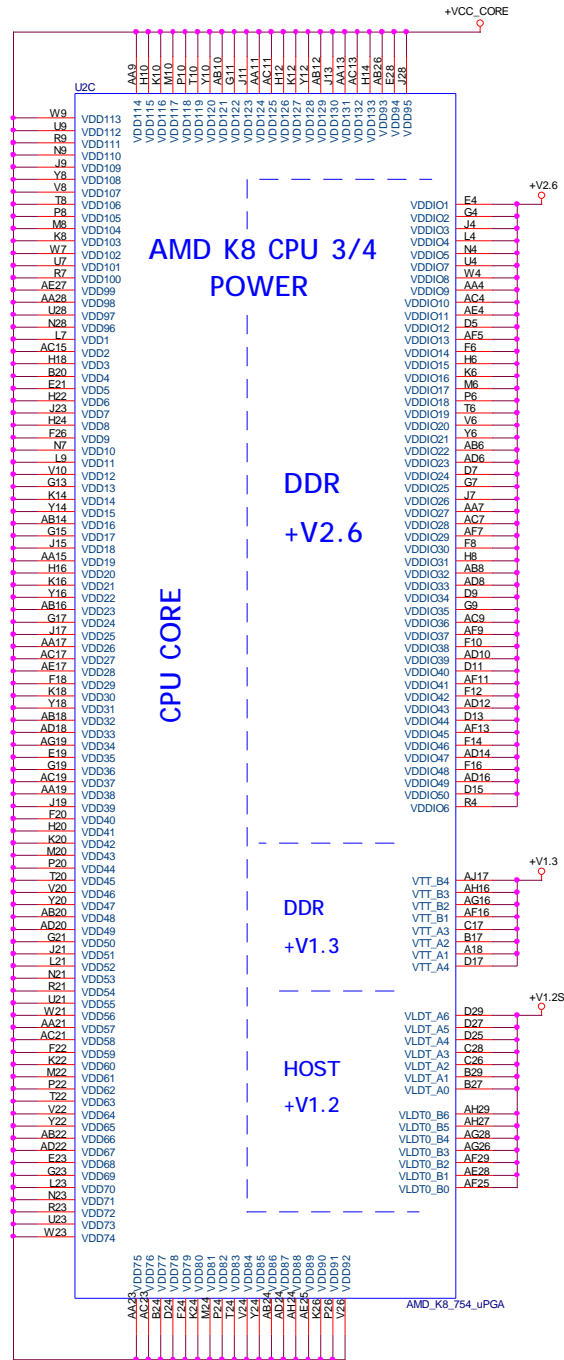
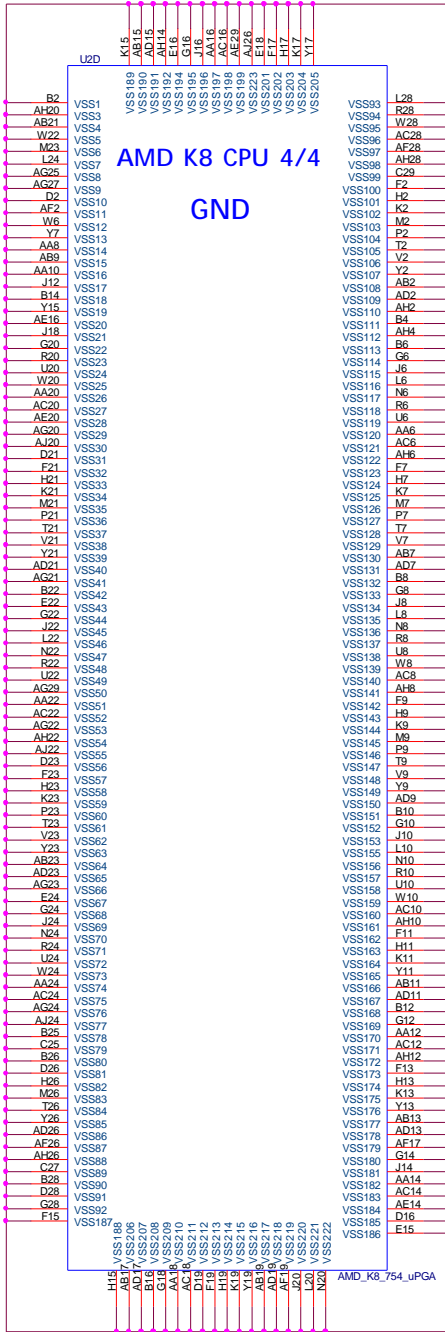
POWER BLOCK DIAGRAM



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| | | |
|-------|--|---------------|
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RN3 10R-8P4R
M_D0M0 8 1 M_D0M0_R_0
M_D6 7 2 M_D_R_6
M_D2 6 3 M_D_R_2
M_D0S0 5 4 M_D0S_R_0

RN5 10R-8P4R
M_D9 5 4 M_D_R_9
M_D0S1 6 3 M_D0S_R_1
M_D0M1 7 2 M_D0M1_R_1
M_D13 8 1 M_D_R_13

RN4 10R-8P4R
M_D12 8 1 M_D_R_12
M_D8 7 2 M_D_R_8
M_D7 6 3 M_D_R_7
M_D3 5 4 M_D_R_3

RN7 10R-8P4R
M_D16 8 1 M_D_R_16
M_D17 6 3 M_D_R_17
M_D20 7 2 M_D_R_20
M_D21 8 1 M_D_R_21

RN9 10R-8P4R
M_D24 8 1 M_D_R_24
M_D28 7 2 M_D_R_28
M_D23 6 3 M_D_R_23
M_D19 5 4 M_D_R_19

RN8 10R-8P4R
M_D0S2 5 4 M_D0S_R_2
M_D18 6 3 M_D_R_18
M_D0M2 7 2 M_D0M2_R_2
M_D22 8 1 M_D_R_22

RN11 10R-8P4R
M_D30 8 1 M_D_R_30
M_D31 7 2 M_D_R_31
M_D27 6 3 M_D_R_27
M_D26 5 4 M_D_R_26

RN10 10R-8P4R
M_D25 5 4 M_D_R_25
M_D29 6 3 M_D_R_29
M_D0S3 7 2 M_D0S_R_3
M_D0M3 8 1 M_D0M3_R_3

RN14 10R-8P4R
M_D40 8 1 M_D_R_40
M_D44 7 2 M_D_R_44
M_D39 6 3 M_D_R_39
M_D38 5 4 M_D_R_38

RN12 10R-8P4R
M_D32 5 4 M_D_R_32
M_D33 6 3 M_D_R_33
M_D36 7 2 M_D_R_36
M_D37 8 1 M_D_R_37

RN13 10R-8P4R
M_D35 8 1 M_D_R_35
M_D0M4 7 2 M_D0M4_R_4
M_D34 6 3 M_D_R_34
M_D0S4 5 4 M_D0S_R_4

RN15 10R-8P4R
M_D41 5 4 M_D_R_41
M_D0S5 6 3 M_D0S_R_5
M_D45 7 2 M_D_R_45
M_D0M5 8 1 M_D0M5_R_5

RN17 10R-8P4R
M_D53 8 1 M_D_R_53
M_D52 7 2 M_D_R_52
M_D49 6 3 M_D_R_49
M_D48 5 4 M_D_R_48

RN2 10R-8P4R
M_D63 8 1 M_D_R_63
M_D62 7 2 M_D_R_62
M_D59 6 3 M_D_R_59
M_D58 5 4 M_D_R_58

RN1 10R-8P4R
M_D4 8 1 M_D_R_4
M_D5 7 2 M_D_R_5
M_D1 6 3 M_D_R_1
M_D0 5 4 M_D_R_0

RN18 10R-8P4R
M_D0M6 5 4 M_D0M6_R_6
M_D0S6 6 3 M_D0S_R_6
M_D50 7 2 M_D_R_50
M_D54 8 1 M_D_R_54

RN19 10R-8P4R
M_D56 8 1 M_D_R_56
M_D60 7 2 M_D_R_60
M_D51 6 3 M_D_R_51
M_D55 5 4 M_D_R_55

RN20 10R-8P4R
M_D57 5 4 M_D_R_57
M_D0S7 6 3 M_D0S_R_7
M_D61 7 2 M_D_R_61
M_D0M7 8 1 M_D0M7_R_7

RN16 10R-8P4R
M_D47 8 1 M_D_R_47
M_D46 7 2 M_D_R_46
M_D43 6 3 M_D_R_43
M_D42 5 4 M_D_R_42

RN6 10R-8P4R
M_D15 8 1 M_D_R_15
M_D11 7 2 M_D_R_11
M_D14 6 3 M_D_R_14
M_D10 5 4 M_D_R_10

+V1.3
R252 1 2 47R M_AB8
R253 1 2 47R M_AB11
R254 1 2 68R M_D_R_23
R255 1 2 68R M_D_R_28
R250 1 2 68R M_D_R_5
R251 1 2 68R M_D_R_4

RN40 68R-8P4R
1 2 8 M_D_R_8
2 7 M_D_R_3
3 6 M_D_R_2
4 5 M_D0S_R_0

RN36 68R-8P4R
4 5 M_D_R_12
3 6 M_D_R_7
2 7 M_D_R_6
1 8 M_D0M0_R_0

RN39 68R-8P4R
1 2 8 M_D_R_10
2 7 M_D_R_11
3 6 M_D_R_9
4 5 M_D0S_R_1

RN33 68R-8P4R
4 5 M_D_R_30
3 6 M_D_R_31
2 7 M_D_R_29
1 8 M_D0M0_R_3

RN35 68R-8P4R
1 2 8 M_D0M0_R_1
2 7 M_D_R_13
3 6 M_D_R_15
4 5 M_D_R_14

RN37 68R-8P4R
1 2 8 M_D_R_26
2 7 M_D0S_R_3
3 6 M_D_R_25
4 5 M_D_R_24

RN28 68R-8P4R
4 5 M_D_R_53
3 6 M_D_R_52
2 7 M_D_R_46
1 8 M_D_R_47

RN30 68R-8P4R
1 2 8 M_D_R_36
2 7 M_D_R_37
3 6 M_D0M0_R_4
4 5 M_D_R_38

RN43 68R-8P4R
4 5 M_D_R_50
3 6 M_D0S_R_6
2 7 M_D_R_51
1 8 M_D_R_56

RN27 68R-8P4R
1 2 8 M_D0M0_R_6
2 7 M_D_R_54
3 6 M_D_R_55
4 5 M_D_R_60

RN29 68R-8P4R
1 2 8 M_D_R_39
2 7 M_D_R_44
3 6 M_D_R_45
4 5 M_D0M0_R_5

RN32 47R-8P4R
1 2 8 M_AB6
2 7 M_AB4
3 6 M_AB2
4 5 M_AB0

RN47 47R-8P4R
1 2 8 M_AB3
2 7 M_AB1
3 6 M_AB7
4 5 M_AB5

+V1.3
R264 1 2 47R M_AB9
R267 1 2 47R M_AB12
R271 1 2 68R M_D_R_27
R263 1 2 68R M_D_R_16
R268 1 2 68R M_D_R_0
R269 1 2 68R M_D_R_1

RN48 47R-8P4R
1 2 8 M_A11
2 7 M_AB
3 6 M_AB
4 5 M_A4

RN51 47R-8P4R
1 2 8 M_BAA0
2 7 M_WE#
3 6 M_CS0_R#
4 5 M_A0_131

RN34 68R-8P4R
4 5 M_D_R_22
3 6 M_D0M0_R_2
2 7 M_D_R_21
1 8 M_D_R_20

RN42 68R-8P4R
1 2 8 M_D_R_59
2 7 M_D_R_58
3 6 M_D_R_57
4 5 M_D0S_R_7

RN44 68R-8P4R
1 2 8 M_D_R_49
2 7 M_D_R_48
3 6 M_D_R_42
4 5 M_D_R_43

RN49 47R-8P4R
1 2 8 M_A13
2 7 M_AB
3 6 M_A12
4 5 M_A5

RN46 68R-8P4R
4 5 M_D_R_33
3 6 M_D_R_32
2 7 M_D_R_34
1 8 M_D0S_R_4

RN50 47R-8P4R
1 2 8 M_A7
2 7 M_A1
3 6 M_A3
4 5 M_A10

RN41 47R-8P4R
1 2 8 M_BAB0
2 7 M_WEB#
3 6 M_CS2_R#
4 5 M_CS2_R#

R270 1 2 47R M_AB10
R279 1 2 47R M_CKE0_R
R266 1 2 47R M_CKE1_R

RN45 68R-8P4R
1 2 8 M_D_R_41
2 7 M_D0S_R_5
3 6 M_D_R_40
4 5 M_D_R_35

R277 1 2 47R M_A2
R276 1 2 47R M_A0
R274 1 2 47R M_BAA1
R275 1 2 47R M_RAS#

RN38 68R-8P4R
1 2 8 M_D_R_19
2 7 M_D_R_18
3 6 M_D0S_R_2
4 5 M_D_R_17

RN26 68R-8P4R
1 2 8 M_D_R_61
2 7 M_D0M0_R_7
3 6 M_D_R_62
4 5 M_D_R_63

RN31 47R-8P4R
1 2 8 M_BAB1
2 7 M_RAS#
3 6 M_CASB#
4 5 M_CS3_R#

R273 1 2 47R M_CS1_R#
R272 1 2 47R M_CAS#
R265 1 2 47R M_AB13

4.7 M_BAA0
4.7 M_BAA1
4.7 M_BAB0
4.7 M_BAB1
4.7 M_RAS#
4.7 M_CAS#
4.7 M_WE#

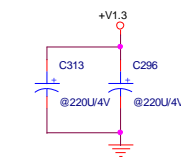
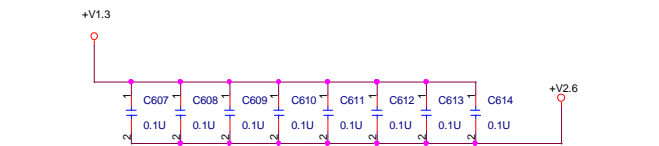
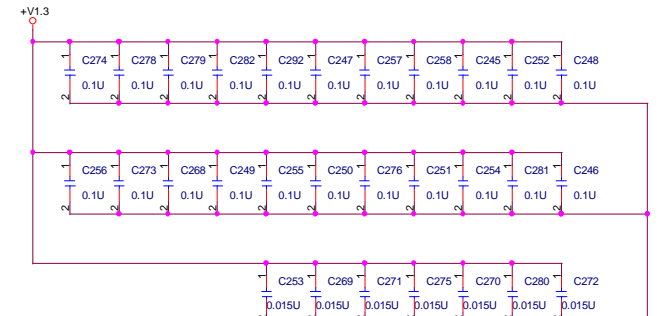
4.7 M_RASB#
4.7 M_CASB#
4.7 M_WEB#

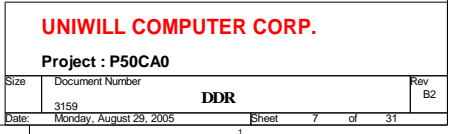
4 M_D0S[0..7] M_D0S_R[0..7] 7
4 M_D[0..63] M_D_R[0..63] 7

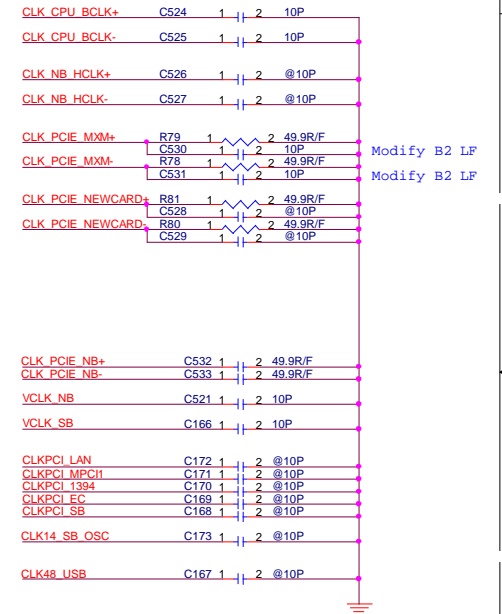
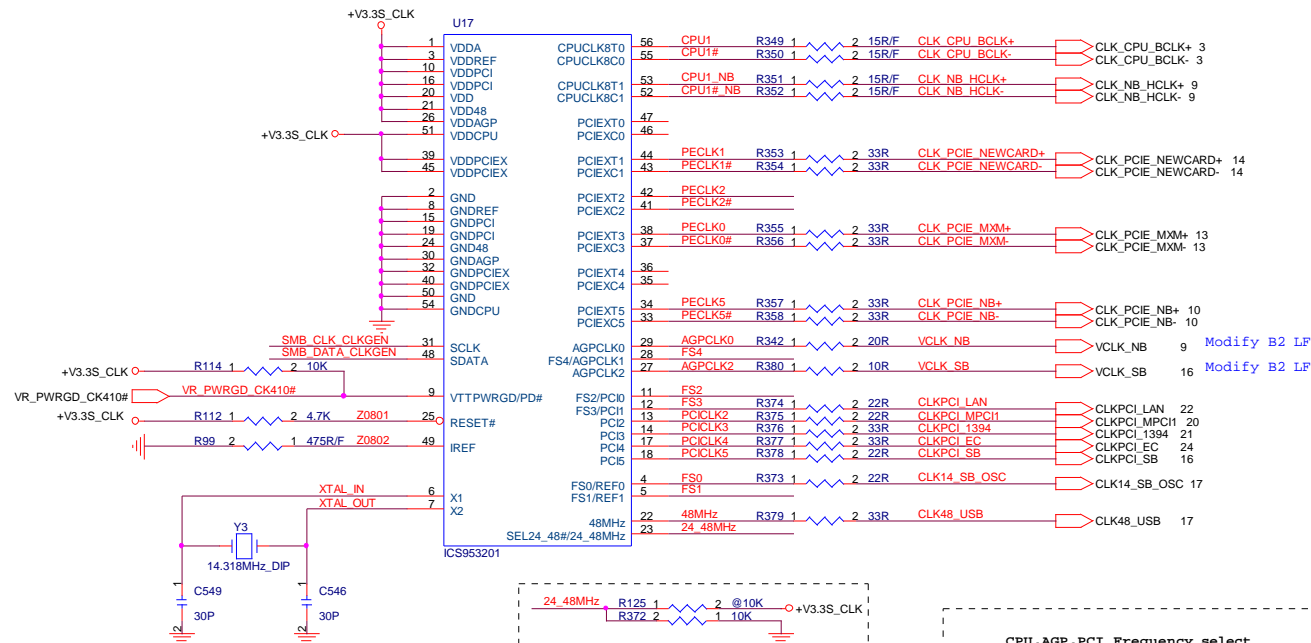
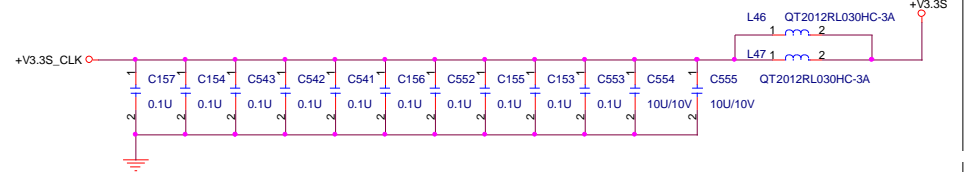
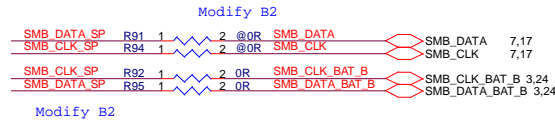
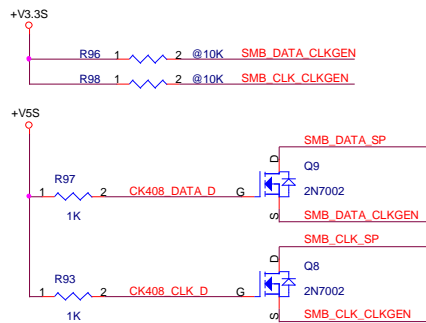
4.7 M_A[0..13] M_A0_131
4.7 M_AB[0..13] M_AB0_131
4 M_D0M0[0..7] M_D0M0_R[0..7] 7

4.7 M_CS0_R#
4.7 M_CS1_R#
4.7 M_CS2_R#
4.7 M_CS3_R#

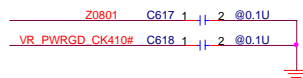
4.7 M_CKE0_R
4.7 M_CKE1_R



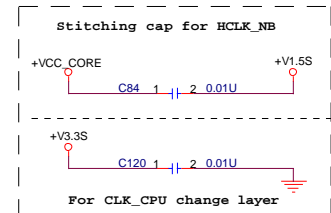




Modify B:Place at Top side

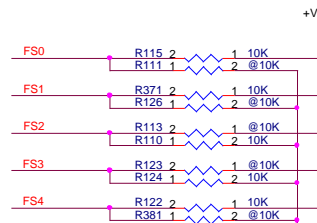


Pin 23 Output Frequency select
0 : 48MHz / 1 : 24MHz



CPU,AGP,PCI Frequency select

| FS_[4:0] | CPU | PCIEX | AGP | PCI |
|----------|--------|--------|-------|-------|
| 10011 | 200.00 | 100.00 | 66.67 | 33.33 |



Modify B2 LF :
Add RW1 which is 10P near by NB(K8T890)
at "VCLK_NB".

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| | CLK Generator | B2 |
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Ground

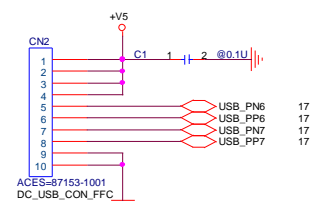
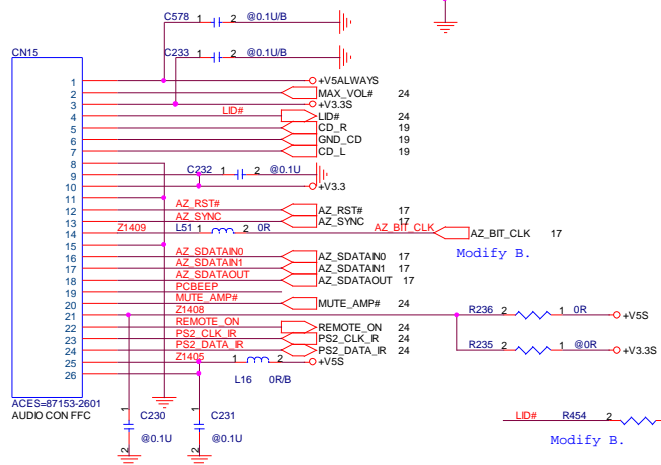
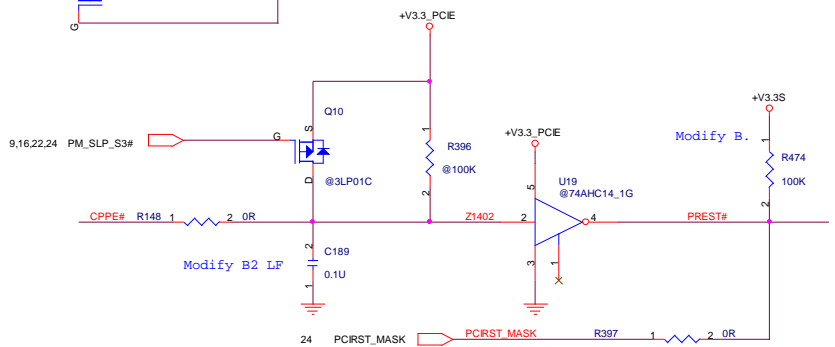
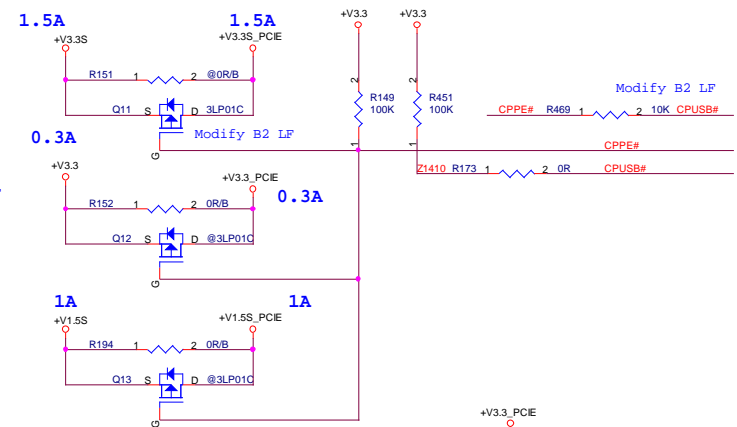
VIA K8T890CE 4/5

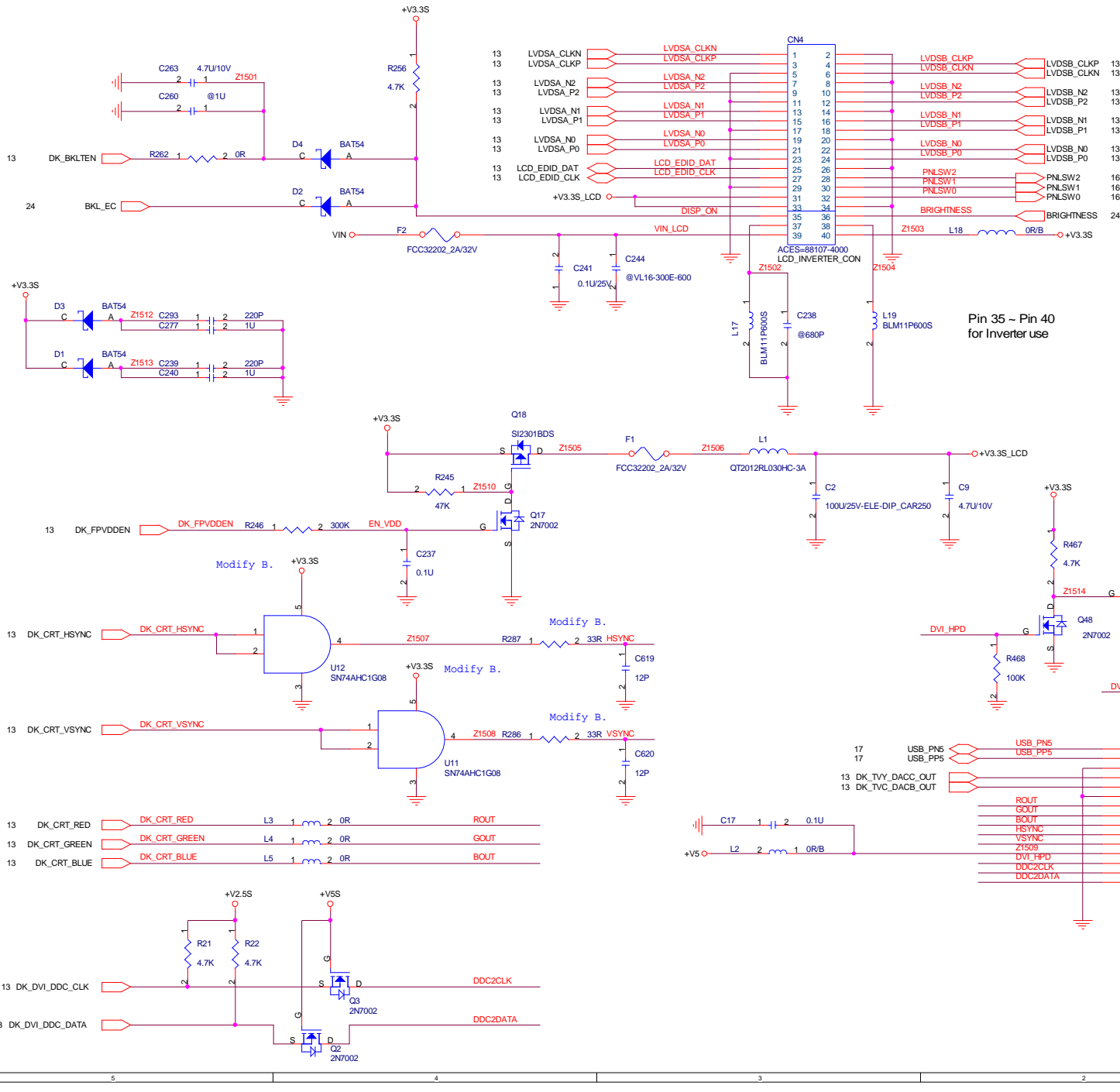
3.3V
(PCIE)

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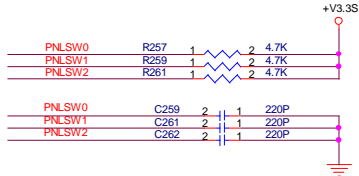
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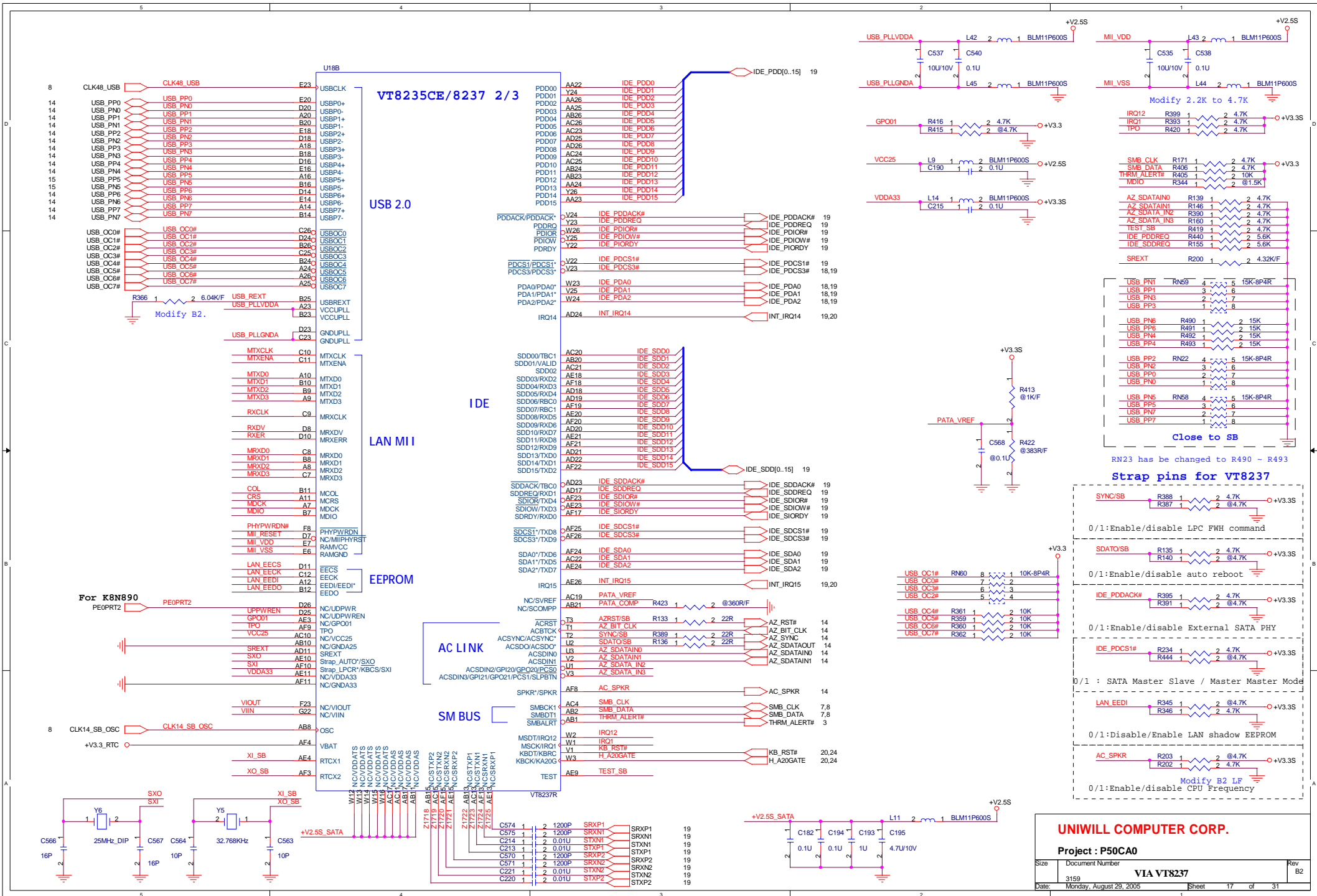
| | | | | |
|-------|-------------------------|------------------------|-----|-------|
| Size | Document Number | K8T890CE - POWER & GND | Rev | B2 |
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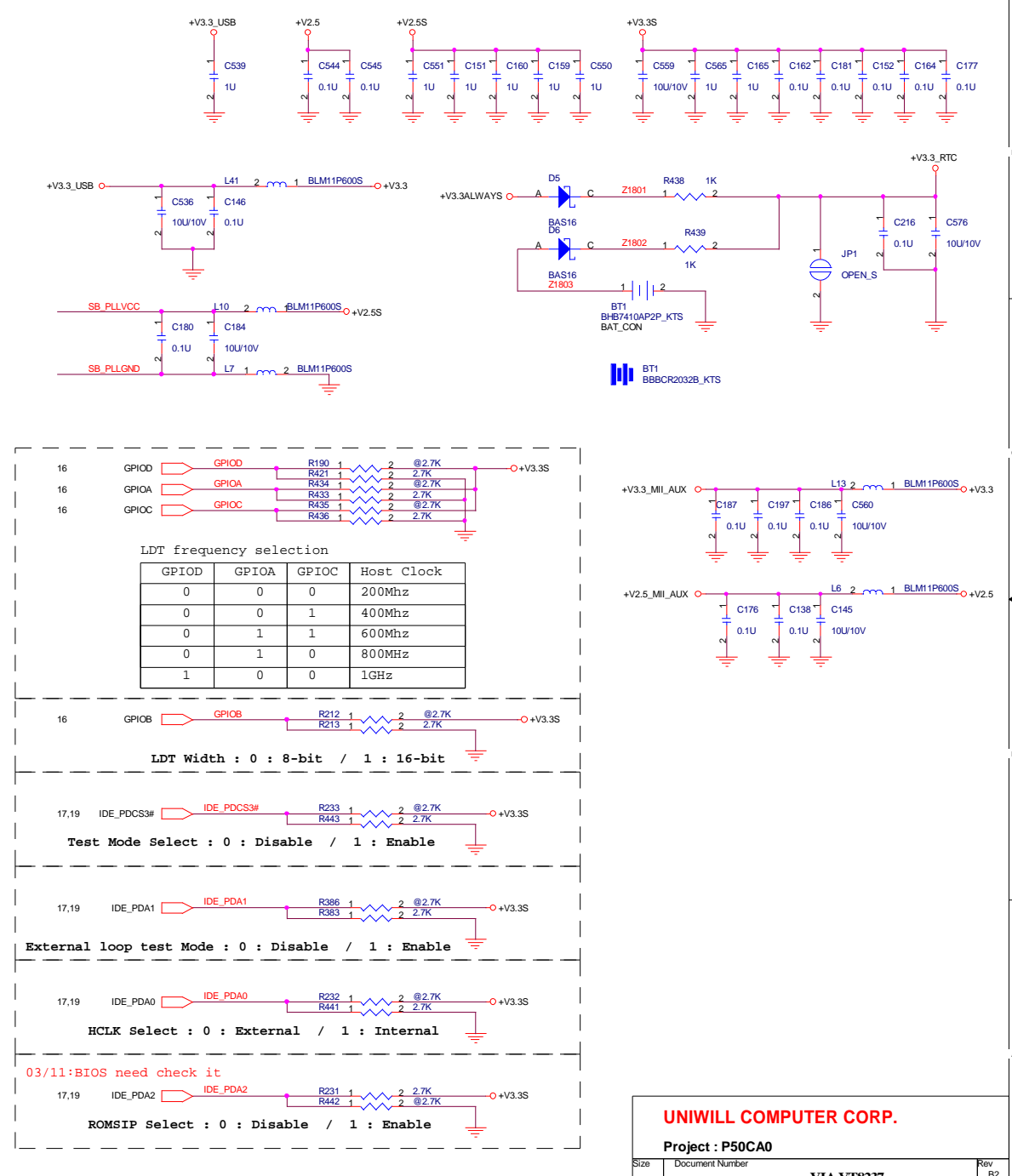
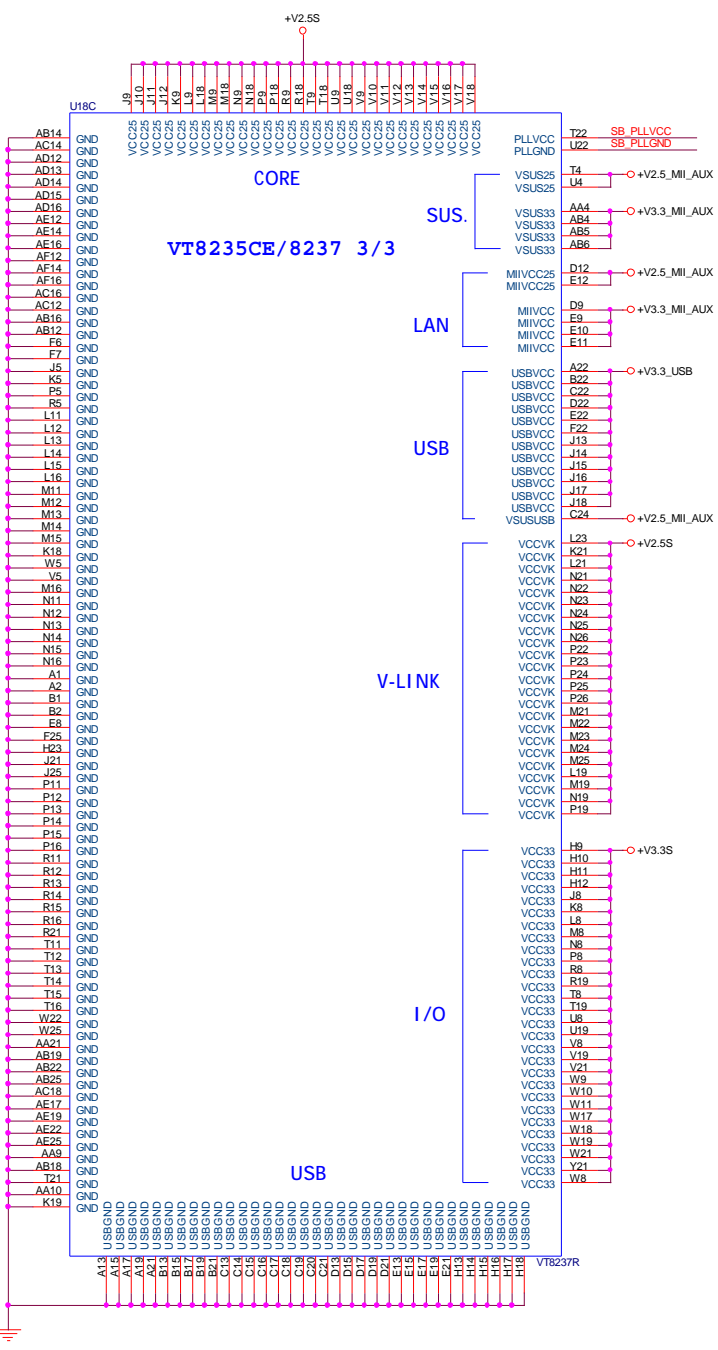


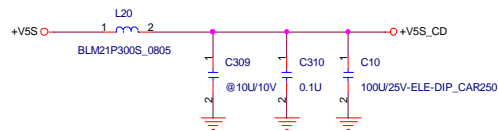


| LCD Panel ID Table | | | |
|--------------------|--------|--------|------------|
| PNLSW2 | PNLSW1 | PNLSW0 | Resolution |
| 0 | 0 | 0 | reserved |
| 0 | 0 | 1 | reserved |
| 0 | 1 | 0 | reserved |
| 0 | 1 | 1 | 1280x800 |
| 1 | 0 | 0 | 1440x900 |
| 1 | 0 | 1 | 1680X1050 |
| 1 | 1 | 0 | 1920X1200 |
| 1 | 1 | 1 | reserved |



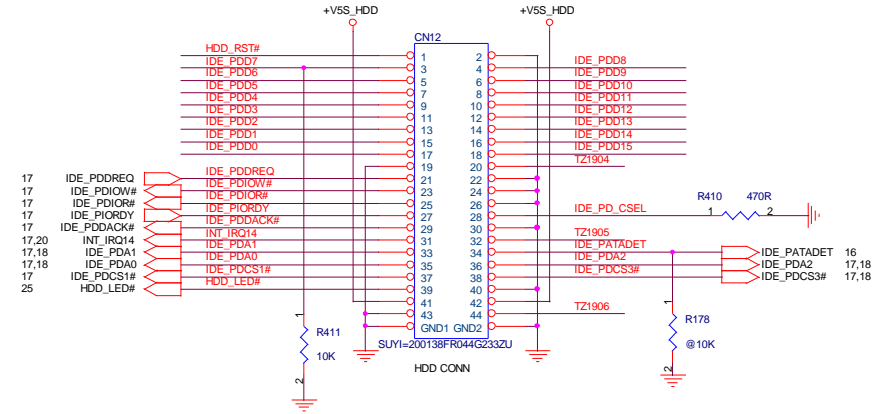
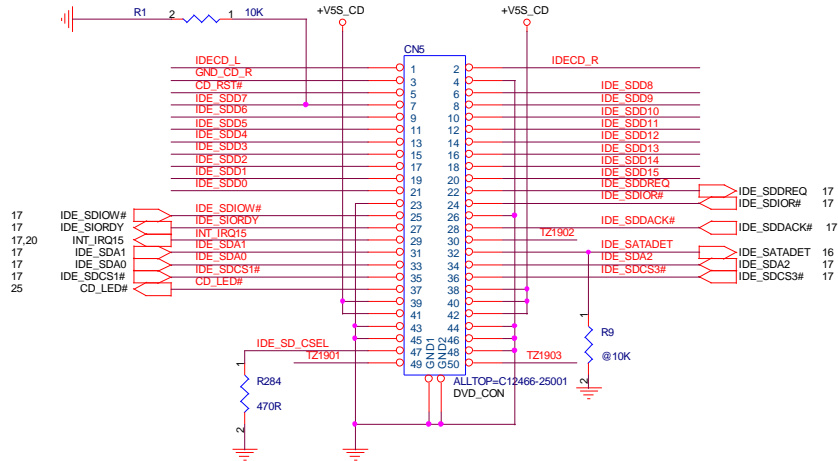
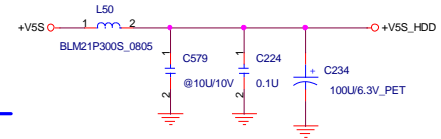




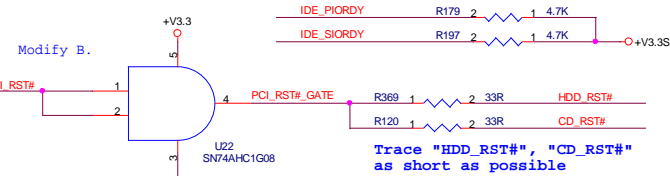


17 IDE_SDD[0..15] IDE_SDD[0..15]

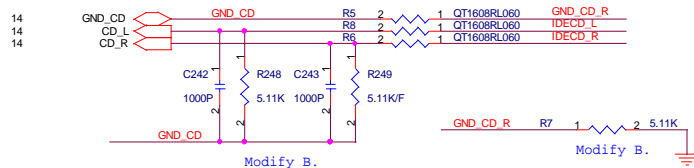
17 IDE_PDD[0..15] IDE_PDD[0..15]



Secondary Channel

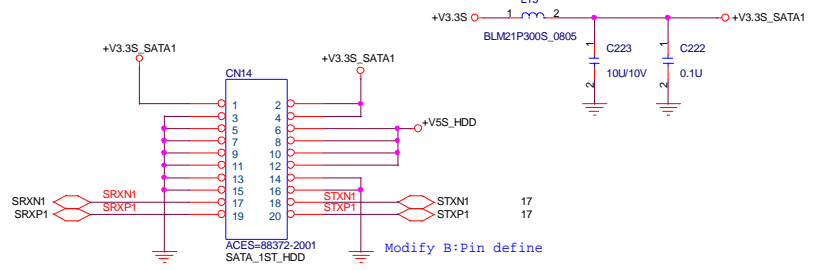
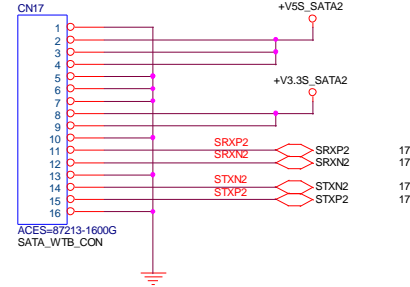
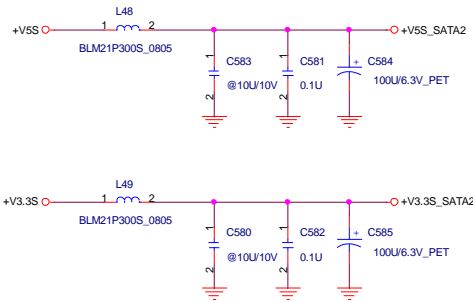


Trace "HDD_RST#", "CD_RST#" as short as possible



3,9,13,16,20,21,22,24

Modify B.

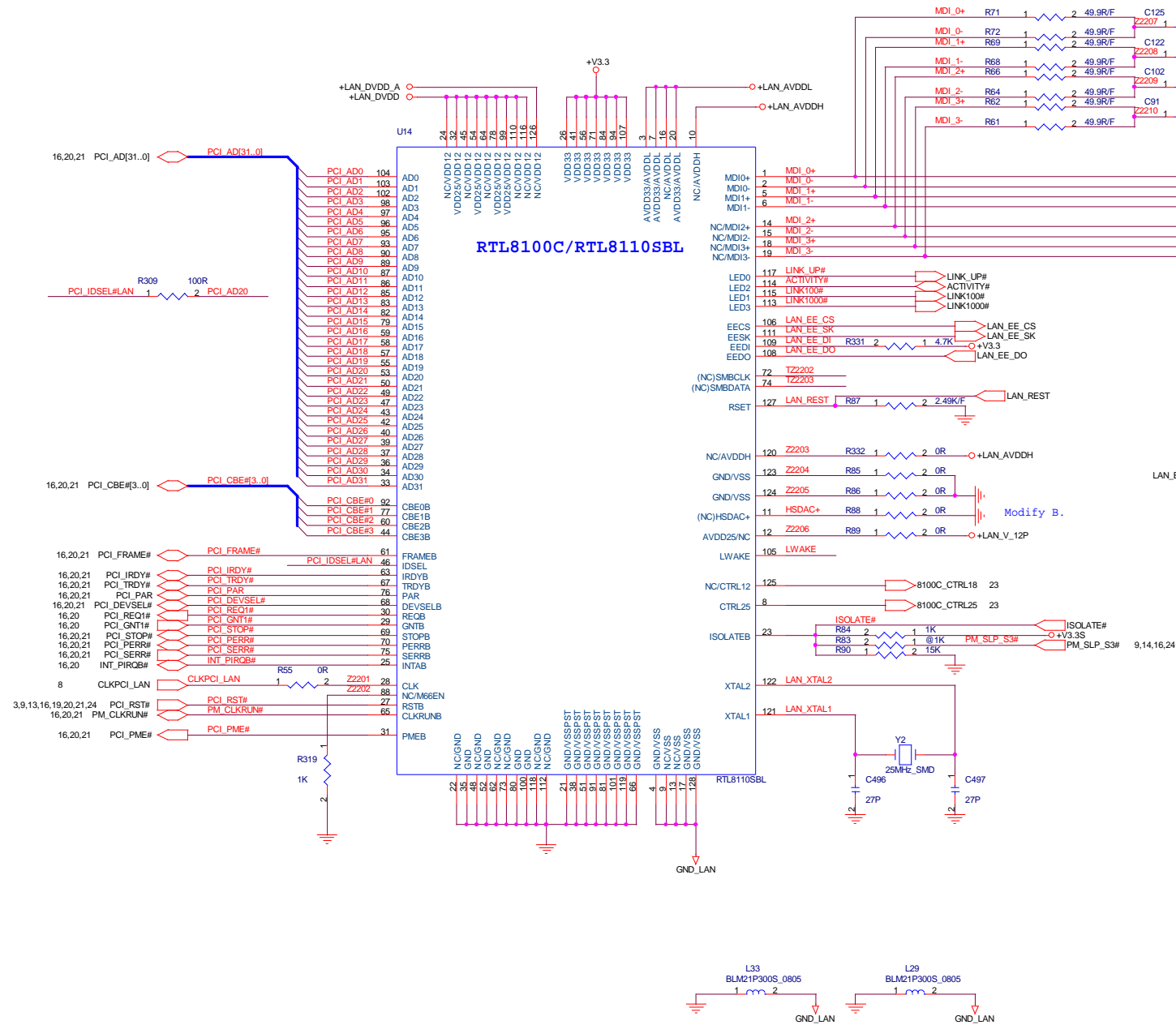


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| | | |
|------|-------------------------|----------------|
| Size | Document Number | Rev |
| | 3159 | B2 |
| Date | Monday, August 29, 2005 | Sheet 19 of 31 |

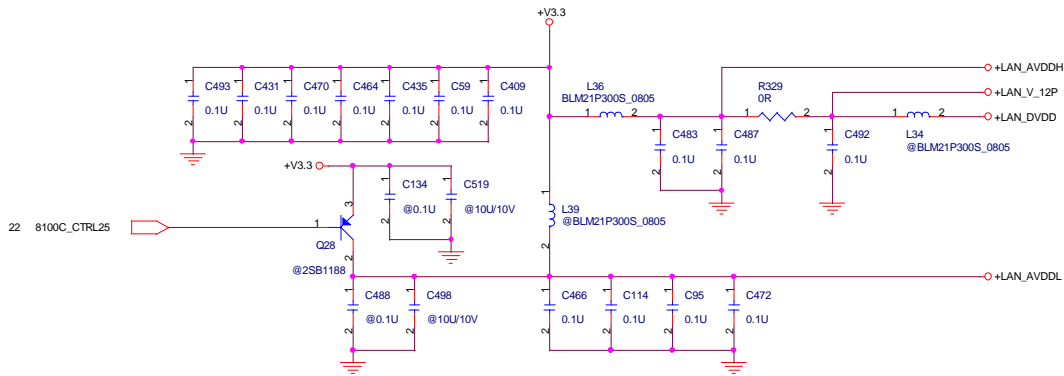
IDE & SATA HDD CDROM



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Project : P50CA0

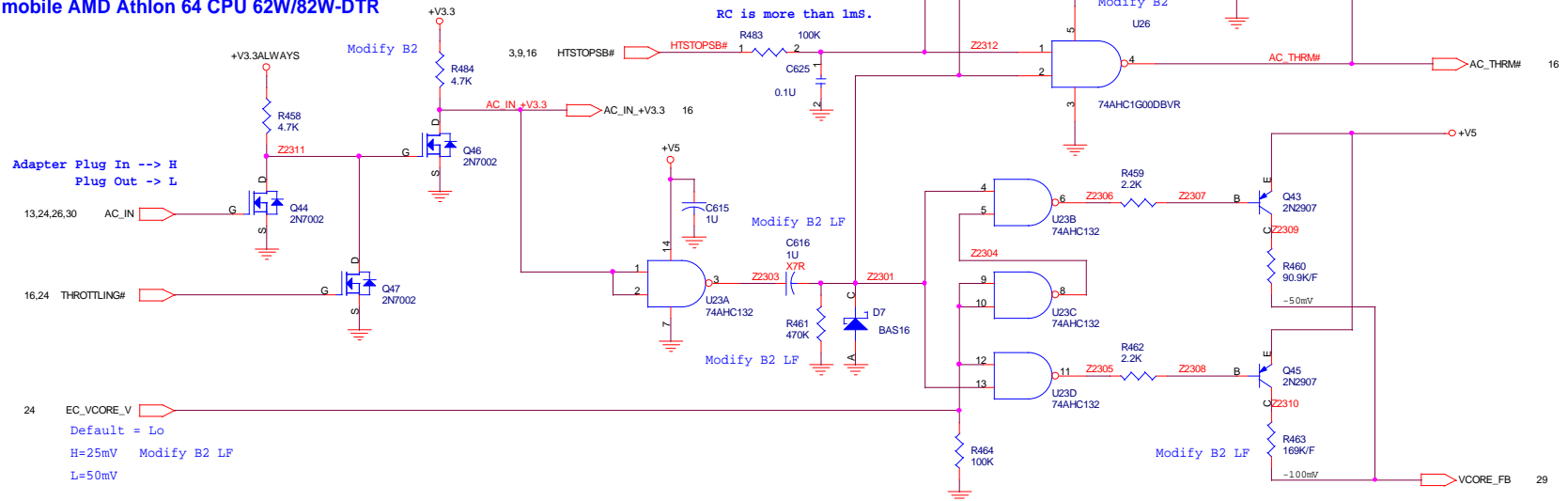
| | | |
|-------|-------------------------|----------------|
| Size | Document Number | Rev |
| | IEEE1394 | B2 |
| Date: | Monday, August 29, 2005 | Sheet 22 of 31 |



| | RTL8100C | RTL8110SB |
|------|----------|-----------|
| R313 | X | O |
| L38 | X | O |
| L36 | O | X |
| L41 | O | X |
| L37 | X | O |
| L40 | X | O |
| Q24 | X | O |
| Q26 | X | O |
| R72 | X | O |
| R73 | X | O |
| Q25 | O | X |

| | RTL8100C | RTL8110SB |
|--------|----------|-----------|
| AVDDH | N/A | 3.3AVDD |
| V_12P | 2.5AVDD | 3.3AVDD |
| AVDDL | 3.3AVDD | 2.5AVDD |
| V_DAC | N/A | 2.5AVDD |
| DVDD | 2.5VDD | 1.2VDD |
| DVDD_A | N/A | 1.2AVDD |

Vcore Stop-Down Circuit support mobile AMD Athlon 64 CPU 62W/82W-DTR

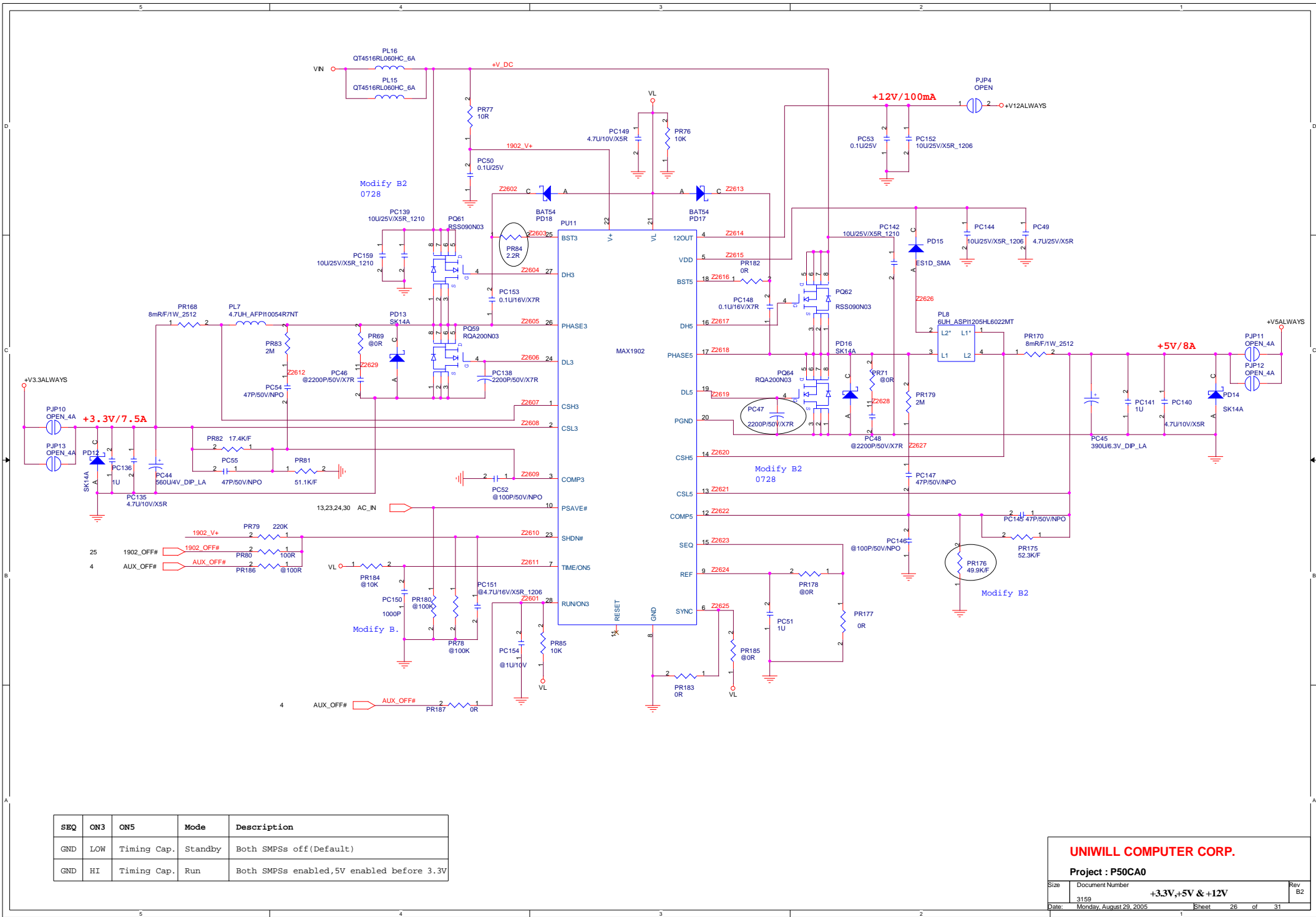


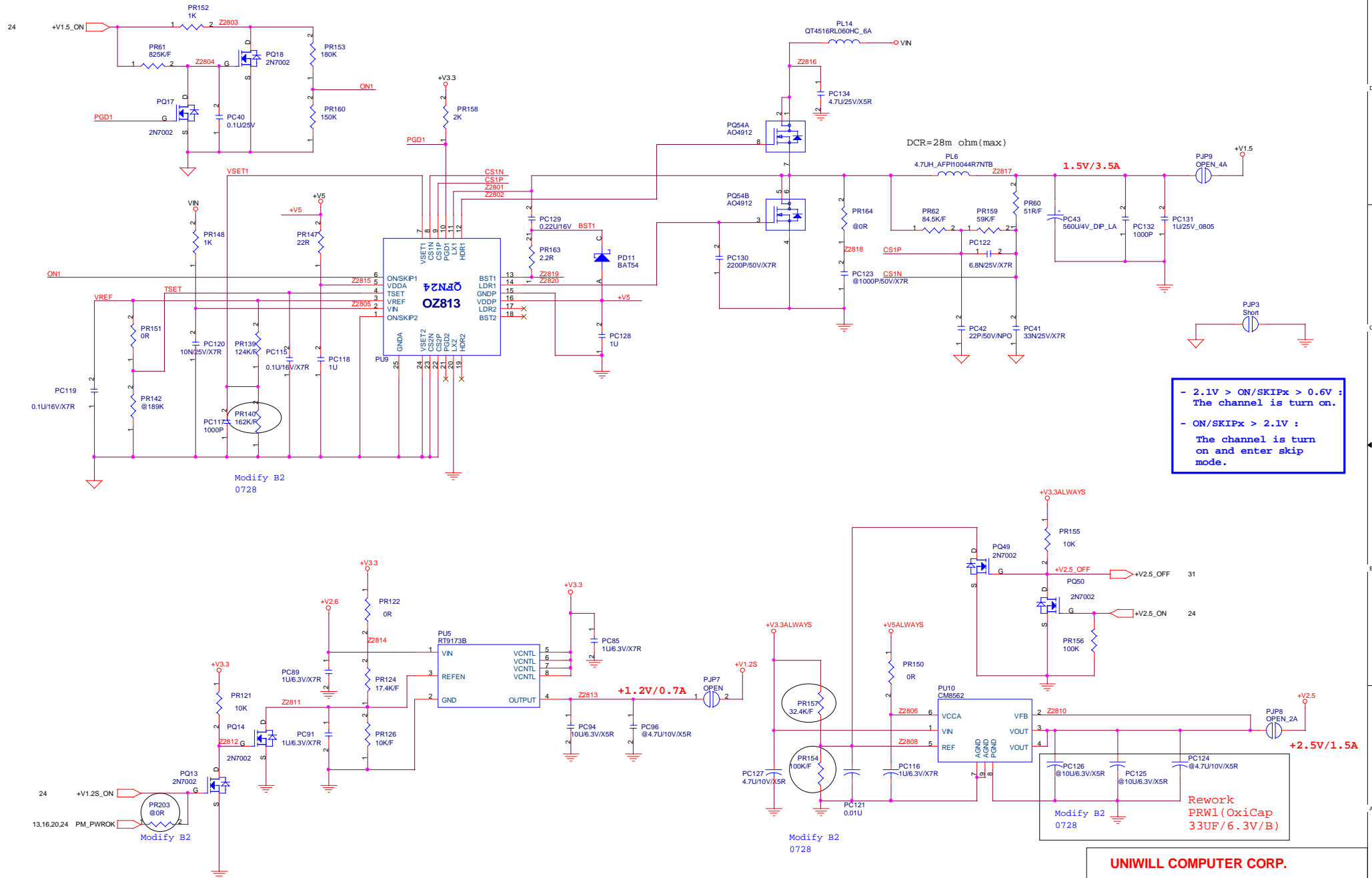
259Klx Change List
Delete Vcore stop-down circuit the above material

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| | | |
|------|---|----------------|
| Size | Document Number | Rev |
| 155 | LAN - RTL8100C/RTL8110S-2&Vcore Stop-Down | B2 |
| Date | Monday, August 29, 2005 | Sheet 23 of 31 |





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| Size | Document Number | Rev |
|-------|--------------------------|----------------|
| 3159 | +1.5V,+1.2V & +2.5V(LDO) | B2 |
| Date: | Monday, August 29, 2005 | Sheet 28 of 31 |

PSW1 Switch Table

| | AMD K8 | 62W | 35W | 25W |
|----------------|--------|-----|-----|-----|
| Low-Power Mode | PSW1_1 | OFF | ON | ON |
| Load-Line | PSW1_2 | OFF | ON | ON |

Switch Table

| | AMD K8 | 62W | 35W | 25W |
|----------------|------------|-----|-----|-----|
| Low-Power Mode | K8_OFFSET | LOW | HI | HI |
| Load-Line | LOAD_LINE# | HI | LOW | LOW |

