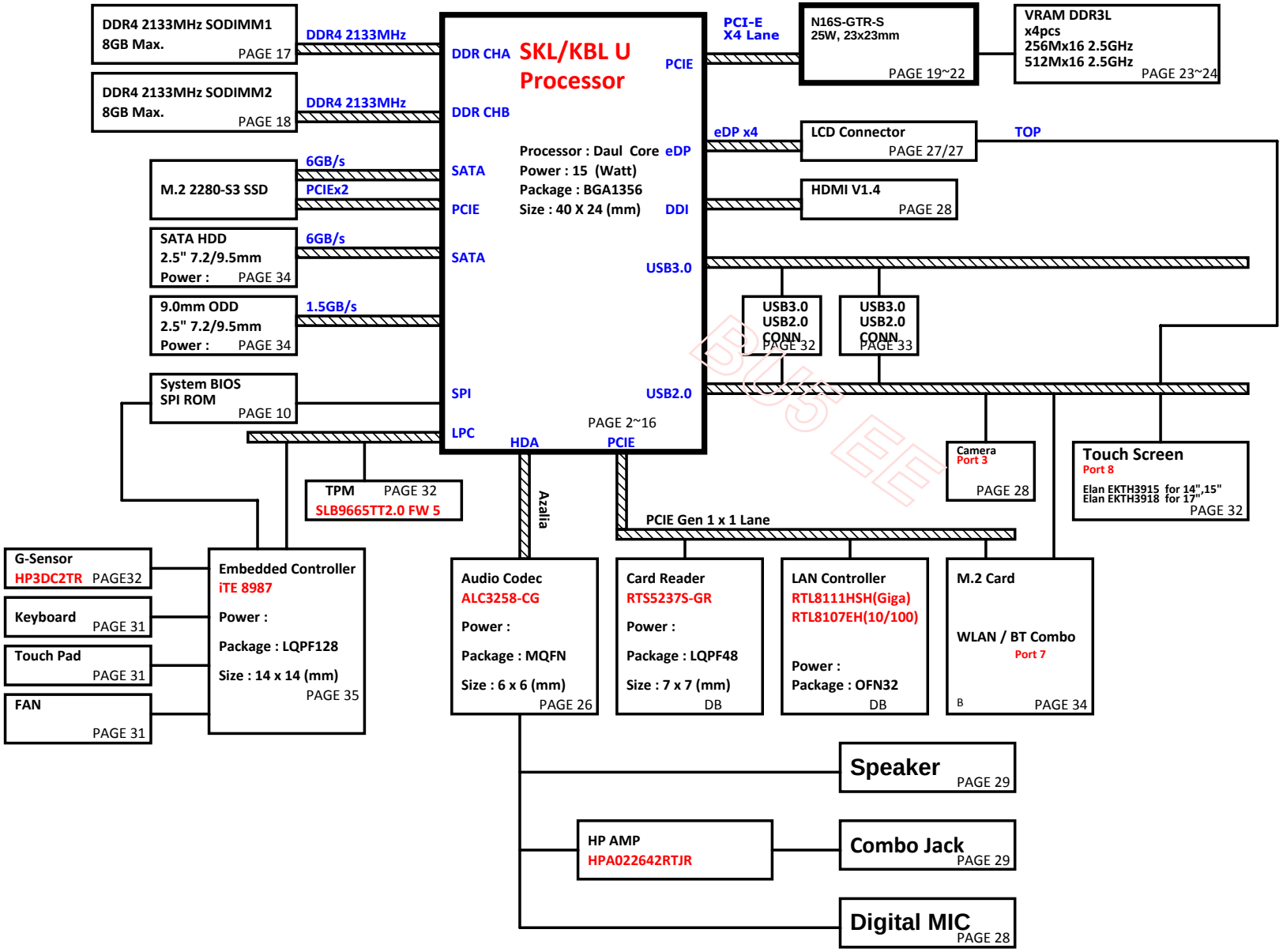
Dessert DIS (15")
Intel SKL/KBL ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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need surport to UHD 3840x2160

02

+3V [4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]
+1.0V [4,6,16,33,38]
+VCCSTPLL [4,5,6,9,38,39]

HDMI

U1A SKL_ULT ? Need apply PN

[27] IN_D2# → IN_D2# E55 DDI1_TXN[0]
[27] IN_D2 → IN_D2 F55 DDI1_TXP[0]
[27] IN_D1# → IN_D1# E58 DDI1_TXN[1]
[27] IN_D1 → IN_D1 F58 DDI1_TXP[1]
[27] IN_D0# → IN_D0# F53 DDI1_TXN[2]
[27] IN_D0 → IN_D0 G53 DDI1_TXP[2]
[27] IN_CLK# → IN_CLK# F56 DDI1_TXN[3]
[27] IN_CLK → IN_CLK G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI → EDP

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 [25]
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 [25]
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 [25]
EDP_TXP[1] C45 INT_EDP_TXP1 → INT_EDP_TXP1 [25]
EDP_TXN[2] A45 INT_EDP_TXN2 → INT_EDP_TXN2 [25]
EDP_TXP[2] B45 INT_EDP_TXP2 → INT_EDP_TXP2 [25]
EDP_TXN[3] A47 INT_EDP_TXN3 → INT_EDP_TXN3 [25]
EDP_TXP[3] B47 INT_EDP_TXP3 → INT_EDP_TXP3 [25]

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN [25]
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP [25]
EDP_DISP_UTIL B52 EDP_DISP_UTIL → TP1

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN F48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E13/DDPB_HPD0 L9 HDMI_HPD_CON → HDMI_HPD_CON [27]
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L5
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 ULT_EDP_HPD → ULT_EDP_HPD [25]

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON [25]
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM [25]
EDP_VDDEN U13 PCH_DISP_ON → PCH_DISP_ON [25]

DISPLAY SIDEBANDS

[27] SDVO_CLK L13 GPP_E18/DDPB_CTRLCLK
[27] SDVO_DATA L12 GPP_E19/DDPB_CTRLDATA

TP2 DDPC_CTRLDATA N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA

TP3 DDPD_CTRLDATA N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO R3 24.9/F_4 EDP_RCOMP E52 EDP_RCOMP

*SKL_ULT
REV = 1
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?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R1 *10K/F_4
ULT_EDP_HPD
R2 100K_4

U1D SKL_ULT ? Need apply PN

[33,39,47] H_PROCHOT# R4 499/F_4 [33] EC_PECI
[33] PM_THRMTRIP#

CATERR# D63
EC_PECI A51 PECI
PROCHOT# C55 PROCHOT#
PM_THRMTRIP# C57 THERMTRIP#
A61 SKTOCC#

CPU MISC

[16] XDP_BPM0 C55 BPM#[0]
[16] XDP_BPM1 D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

JTAG

PROC_TCK B61 XDP_TCK0 → XDP_TCK0 [16]
PROC_TDI D60 XDP_TDI_CPU → XDP_TDI_CPU [16]
PROC_TDO A61 XDP_TDO_CPU → XDP_TDO_CPU [16]
PROC_TMS C60 XDP_TMS_CPU → XDP_TMS_CPU [16]
PROC_TRST# B59 XDP_TRST#_CPU → XDP_TRST#_CPU [2,16]

PCH_JTAG_TCK B56 JTAG_TCK_PCH → JTAG_TCK_PCH [16]
PCH_JTAG_TDI D59 JTAG_TDI_PCH → JTAG_TDI_PCH [16]
PCH_JTAG_TDO A56 JTAG_TDO_PCH → JTAG_TDO_PCH [16]
PCH_JTAG_TMS C59 JTAG_TMS_PCH → JTAG_TMS_PCH [16]
PCH_TRST# C61 XDP_TRST#_CPU → XDP_TRST#_CPU [2,16]
JTAGX A59 JTAGX_PCH → JTAGX_PCH [16]

TP113 3D_FW_GPIO_R A6 GPP_E3/CPU_GP0
TP4 CPU_GP1 A7 GPP_E7/CPU_GP1
TP5 CPU_GP2 BA5 GPP_B3/CPU_GP2
TP6 CPU_GP3 AY5 GPP_B4/CPU_GP3

R8 49.9/F_4 PROC_POPIRCOMP AT16 PROC_POPIRCOMP
R11 49.9/F_4 PCH_OPI_RCOMP AU16 PCH_OPIRCOMP
R12 49.9/F_4 EDRAM_OPIO_RCOMP H66 OPCE_RCOMP
R14 49.9/F_4 EOPIO_RCOMP H65 OPC_RCOMP

*SKL_ULT
REV = 1
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+VCCSTPLL
R6 *49.9/F_4 CATERR#

+1.0V
R9 0_4
R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

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PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
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SkyLake ULT Processor (DDR4)

[17] M_A_DQSN[7:0]
[17] M_A_DQSP[7:0]
[18] M_B_DQSN[7:0]
[18] M_B_DQSP[7:0]
[17] M_A_DQ[63:0]
[18] M_B_DQ[63:0]

+1.2VSUS [6,17,18,36,38,46]

Need apply PN

U1B — SKL_ULT — *SKL_ULT REV = 1 — 2 OF 20

M_A_DQ0	AL71	DDR0_DQ[0]	DDR0_CKN[0]	AU53	M_A_CLKN0 [17]
M_A_DQ1	AL68	DDR0_DQ[1]	DDR0_CKP[0]	AT53	M_A_CLKP0 [17]
M_A_DQ2	AN68	DDR0_DQ[2]	DDR0_CKN[1]	AU55	M_A_CLKN1 [17]
M_A_DQ3	AN69	DDR0_DQ[3]	DDR0_CKP[1]	AT55	M_A_CLKP1 [17]
M_A_DQ4	AL70	DDR0_DQ[4]	DDR0_CKE[0]	BA56	
M_A_DQ5	AL69	DDR0_DQ[5]	DDR0_CKE[1]	BB56	M_A_CKE0 [17]
M_A_DQ6	AN70	DDR0_DQ[6]	DDR0_CKE[2]	AW56	M_A_CKE1 [17]
M_A_DQ7	AN71	DDR0_DQ[7]	DDR0_CKE[3]	AY56	
M_A_DQ8	AR70	DDR0_DQ[8]			
M_A_DQ9	AR68	DDR0_DQ[9]	DDR0_CS#[0]	AU45	
M_A_DQ10	AU71	DDR0_DQ[10]	DDR0_CS#[1]	AU43	M_A_CS#0 [17]
M_A_DQ11	AU68	DDR0_DQ[11]	DDR0_ODT[0]	AT45	M_A_CS#1 [17]
M_A_DQ12	AR71	DDR0_DQ[12]	DDR0_ODT[1]	AT43	M_A_DIM0_ODT0 [17]
M_A_DQ13	AR69	DDR0_DQ[13]			M_A_DIM0_ODT1 [17]
M_A_DQ14	AU70	DDR0_DQ[14]	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BA51	M_A_A5
M_A_DQ15	AU69	DDR0_DQ[15]	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BB54	M_A_A9 [17]
M_B_DQ0	AF65	DDR1_DQ[0]/DDR0_DQ[16]	DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	BA52	M_A_A6 [17]
M_B_DQ1	AF64	DDR1_DQ[1]/DDR0_DQ[17]	DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AY52	M_A_A8 [17]
M_B_DQ2	AK65	DDR1_DQ[2]/DDR0_DQ[18]	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AW52	M_A_A7 [17]
M_B_DQ3	AK64	DDR1_DQ[3]/DDR0_DQ[19]	DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AY55	M_A_BG#0 [17]
M_B_DQ4	AF66	DDR1_DQ[4]/DDR0_DQ[20]	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	AW54	M_A_A12 [17]
M_B_DQ5	AF67	DDR1_DQ[5]/DDR0_DQ[21]	DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA54	M_A_A11 [17]
M_B_DQ6	AK67	DDR1_DQ[6]/DDR0_DQ[22]	DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	BA55	
M_B_DQ7	AK66	DDR1_DQ[7]/DDR0_DQ[23]	DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]	AY54	M_A_ACT# [17]
M_B_DQ8	AF70	DDR1_DQ[8]/DDR0_DQ[24]			M_A_BG#1 [17]
M_B_DQ9	AF68	DDR1_DQ[9]/DDR0_DQ[25]	DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU46	M_A_A13 [17]
M_B_DQ10	AH71	DDR1_DQ[10]/DDR0_DQ[26]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AU48	M_A_CAS# [17]
M_B_DQ11	AH68	DDR1_DQ[11]/DDR0_DQ[27]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AT46	M_A_WE# [17]
M_B_DQ12	AF71	DDR1_DQ[12]/DDR0_DQ[28]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU50	M_A_RAS# [17]
M_B_DQ13	AF69	DDR1_DQ[13]/DDR0_DQ[29]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AU52	M_A_BS#0 [17]
M_B_DQ14	AH70	DDR1_DQ[14]/DDR0_DQ[30]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AY51	M_A_A2 [17]
M_B_DQ15	AH69	DDR1_DQ[15]/DDR0_DQ[31]	DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT48	M_A_BS#1 [17]
M_A_DQ16	BB65	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	AT50	M_A_A10 [17]
M_A_DQ17	AW65	DDR0_DQ[17]/DDR0_DQ[33]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	BB50	M_A_A1 [17]
M_A_DQ18	AW63	DDR0_DQ[18]/DDR0_DQ[34]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AY50	M_A_A0 [17]
M_A_DQ19	AY63	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_MA[3]	BA50	M_A_A3 [17]
M_A_DQ20	BA65	DDR0_DQ[20]/DDR0_DQ[36]	DDR0_MA[4]	BB52	M_A_A4 [17]
M_A_DQ21	AY65	DDR0_DQ[21]/DDR0_DQ[37]			
M_A_DQ22	BA63	DDR0_DQ[22]/DDR0_DQ[38]	DDR0_DQSN[0]	AM70	M_A_DQSN0
M_A_DQ23	BB63	DDR0_DQ[23]/DDR0_DQ[39]	DDR0_DQSP[0]	AM69	M_A_DQSP0
M_A_DQ24	BA61	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_DQSN[1]	AT69	M_A_DQSN1
M_A_DQ25	AW61	DDR0_DQ[25]/DDR0_DQ[41]	DDR0_DQSP[1]	AT70	M_A_DQSP1
M_A_DQ26	BB59	DDR0_DQ[26]/DDR0_DQ[42]	DDR1_DQSN[0]/DDR0_DQSN[2]	AH66	M_B_DQSN0
M_A_DQ27	AW59	DDR0_DQ[27]/DDR0_DQ[43]	DDR1_DQSP[0]/DDR0_DQSP[2]	AH65	M_B_DQSP0
M_A_DQ28	BB61	DDR0_DQ[28]/DDR0_DQ[44]	DDR1_DQSN[1]/DDR0_DQSN[3]	AG69	M_B_DQSN1
M_A_DQ29	AY61	DDR0_DQ[29]/DDR0_DQ[45]	DDR1_DQSP[1]/DDR0_DQSP[3]	AG70	M_B_DQSP1
M_A_DQ30	BA59	DDR0_DQ[30]/DDR0_DQ[46]	DDR0_DQSN[2]/DDR0_DQSN[4]	BA64	M_A_DQSN2
M_A_DQ31	AY59	DDR0_DQ[31]/DDR0_DQ[47]	DDR0_DQSP[2]/DDR0_DQSP[4]	AY64	M_A_DQSP2
M_B_DQ16	AT66	DDR1_DQ[16]/DDR0_DQ[48]	DDR0_DQSN[3]/DDR0_DQSN[5]	AY60	M_A_DQSN3
M_B_DQ17	AR66	DDR1_DQ[17]/DDR0_DQ[49]	DDR0_DQSP[3]/DDR0_DQSP[5]	BA60	M_A_DQSP3
M_B_DQ18	AP65	DDR1_DQ[18]/DDR0_DQ[50]	DDR1_DQSN[2]/DDR0_DQSN[6]	AR66	M_B_DQSN2
M_B_DQ19	AN65	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_DQSP[2]/DDR0_DQSP[6]	AR65	M_B_DQSP2
M_B_DQ20	AN66	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_DQSN[3]/DDR0_DQSN[7]	AR61	M_B_DQSN3
M_B_DQ21	AP66	DDR1_DQ[21]/DDR0_DQ[53]	DDR1_DQSP[3]/DDR0_DQSP[7]	AR60	M_B_DQSP3
M_B_DQ22	AT65	DDR1_DQ[22]/DDR0_DQ[54]			
M_B_DQ23	AU65	DDR1_DQ[23]/DDR0_DQ[55]	DDR0_ALERT#	AW50	M_A_ALERT# [17]
M_B_DQ24	AT61	DDR1_DQ[24]/DDR0_DQ[56]	DDR0_PAR	AT52	M_A_PARITY [17]
M_B_DQ25	AU61	DDR1_DQ[25]/DDR0_DQ[57]			
M_B_DQ26	AP60	DDR1_DQ[26]/DDR0_DQ[58]	DDR_VREF_CA	AY67	SM_VREF
M_B_DQ27	AN60	DDR1_DQ[27]/DDR0_DQ[59]	DDR0_VREF_DQ	BA67	SMDDR_VREF_DQ1_M3 [18]
M_B_DQ28	AN61	DDR1_DQ[28]/DDR0_DQ[60]	DDR1_VREF_DQ		
M_B_DQ29	AP61	DDR1_DQ[29]/DDR0_DQ[61]			
M_B_DQ30	AT60	DDR1_DQ[30]/DDR0_DQ[62]	DDR_VTT_CNTL	AW67	DDR_VTT_CNTL [4,18]
M_B_DQ31	AU60	DDR1_DQ[31]/DDR0_DQ[63]			

NIL-DDR CH - A

TP7

20mils width

U1C — SKL_ULT — *SKL_ULT REV = 1 — 3 OF 20

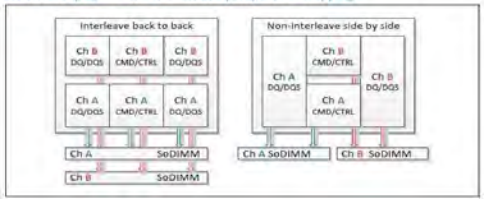
Need apply PN

M_A_DQ32	AY39	DDR0_DQ[32]/DDR1_DQ[0]	DDR1_CKN[0]	AN45	M_B_CLKN0 [18]
M_A_DQ33	AW39	DDR0_DQ[33]/DDR1_DQ[1]	DDR1_CKN[1]	AN46	M_B_CLKN1 [18]
M_A_DQ34	AY37	DDR0_DQ[34]/DDR1_DQ[2]	DDR1_CKP[0]	AP45	M_B_CLKP0 [18]
M_A_DQ35	AW37	DDR0_DQ[35]/DDR1_DQ[3]	DDR1_CKP[1]	AP46	M_B_CLKP1 [18]
M_A_DQ36	BB39	DDR0_DQ[36]/DDR1_DQ[4]			
M_A_DQ37	BA39	DDR0_DQ[37]/DDR1_DQ[5]	DDR1_CKE[0]	AN56	
M_A_DQ38	BA37	DDR0_DQ[38]/DDR1_DQ[6]	DDR1_CKE[1]	AP55	M_B_CKE0 [18]
M_A_DQ39	BB37	DDR0_DQ[39]/DDR1_DQ[7]	DDR1_CKE[2]	AN55	M_B_CKE1 [18]
M_A_DQ40	AY35	DDR0_DQ[40]/DDR1_DQ[8]	DDR1_CKE[3]	AP53	
M_A_DQ41	AW35	DDR0_DQ[41]/DDR1_DQ[9]			
M_A_DQ42	AY33	DDR0_DQ[42]/DDR1_DQ[10]	DDR1_CS#[0]	BB42	
M_A_DQ43	AW33	DDR0_DQ[43]/DDR1_DQ[11]	DDR1_CS#[1]	AY42	M_B_CS#0 [18]
M_A_DQ44	BB35	DDR0_DQ[44]/DDR1_DQ[12]	DDR1_ODT[0]	BA42	M_B_CS#1 [18]
M_A_DQ45	BA35	DDR0_DQ[45]/DDR1_DQ[13]	DDR1_ODT[1]	AW42	M_B_DIM0_ODT0 [18]
M_A_DQ46	BA33	DDR0_DQ[46]/DDR1_DQ[14]			M_B_DIM0_ODT1 [18]
M_A_DQ47	BB33	DDR0_DQ[47]/DDR1_DQ[15]	DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	AY48	M_B_A5
M_B_DQ32	AU40	DDR1_DQ[32]/DDR1_DQ[16]	DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	AP50	M_B_A9 [18]
M_B_DQ33	AT40	DDR1_DQ[33]/DDR1_DQ[17]	DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	BA48	M_B_A6 [18]
M_B_DQ34	AT37	DDR1_DQ[34]/DDR1_DQ[18]	DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	BB48	M_B_A8 [18]
M_B_DQ35	AU37	DDR1_DQ[35]/DDR1_DQ[19]	DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	AP48	M_B_A7 [18]
M_B_DQ36	AR40	DDR1_DQ[36]/DDR1_DQ[20]	DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]	AP52	
M_B_DQ37	AP40	DDR1_DQ[37]/DDR1_DQ[21]	DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	AN50	M_B_BG#0 [18]
M_B_DQ38	AP37	DDR1_DQ[38]/DDR1_DQ[22]	DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	AN48	M_B_A12 [18]
M_B_DQ39	AR37	DDR1_DQ[39]/DDR1_DQ[23]	DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	AN53	M_B_A11 [18]
M_B_DQ40	AT33	DDR1_DQ[40]/DDR1_DQ[24]	DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]	AN52	M_B_ACT# [18]
M_B_DQ41	AU33	DDR1_DQ[41]/DDR1_DQ[25]			M_B_BG#1 [18]
M_B_DQ42	AU30	DDR1_DQ[42]/DDR1_DQ[26]	DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	BA43	M_B_A13
M_B_DQ43	AT30	DDR1_DQ[43]/DDR1_DQ[27]	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AY43	M_B_A13 [18]
M_B_DQ44	AR33	DDR1_DQ[44]/DDR1_DQ[28]	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AY44	M_B_CAS# [18]
M_B_DQ45	AP33	DDR1_DQ[45]/DDR1_DQ[29]	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	AW44	M_B_WE# [18]
M_B_DQ46	AR30	DDR1_DQ[46]/DDR1_DQ[30]	DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	BB44	M_B_RAS# [18]
M_B_DQ47	AP30	DDR1_DQ[47]/DDR1_DQ[31]	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	AY47	M_B_BS#0 [18]
M_A_DQ48	AY31	DDR1_DQ[48]/DDR1_DQ[32]	DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	BA44	M_B_A2 [18]
M_A_DQ49	AW31	DDR1_DQ[49]/DDR1_DQ[33]	DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	AW46	M_B_BS#1 [18]
M_A_DQ50	AY29	DDR1_DQ[50]/DDR1_DQ[34]	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	AY46	M_B_A10 [18]
M_A_DQ51	AW29	DDR1_DQ[51]/DDR1_DQ[35]	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	AY45	M_B_A1 [18]
M_A_DQ52	BB31	DDR1_DQ[52]/DDR1_DQ[36]	DDR1_MA[3]	BB46	M_B_A0 [18]
M_A_DQ53	BA31	DDR1_DQ[53]/DDR1_DQ[37]	DDR1_MA[4]	BA47	M_B_A3 [18]
M_A_DQ54	BA29	DDR1_DQ[54]/DDR1_DQ[38]			M_B_A4 [18]
M_A_DQ55	BB29	DDR1_DQ[55]/DDR1_DQ[39]	DDR0_DQSN[4]/DDR1_DQSN[0]	BA38	M_A_DQSN4
M_A_DQ56	AY27	DDR1_DQ[56]/DDR1_DQ[40]	DDR0_DQSP[4]/DDR1_DQSP[0]	AY38	M_A_DQSP4
M_A_DQ57	AW27	DDR1_DQ[57]/DDR1_DQ[41]	DDR0_DQSN[5]/DDR1_DQSN[1]	AY34	M_A_DQSN5
M_A_DQ58	AY25	DDR1_DQ[58]/DDR1_DQ[42]	DDR0_DQSP[5]/DDR1_DQSP[1]	BA34	M_A_DQSP5
M_A_DQ59	AW25	DDR1_DQ[59]/DDR1_DQ[43]	DDR1_DQSN[4]/DDR1_DQSN[2]	AT38	M_B_DQSN4
M_A_DQ60	BB27	DDR1_DQ[60]/DDR1_DQ[44]	DDR1_DQSP[4]/DDR1_DQSP[2]	AR38	M_B_DQSP4
M_A_DQ61	BA27	DDR1_DQ[61]/DDR1_DQ[45]	DDR1_DQSN[5]/DDR1_DQSN[3]	AT32	M_B_DQSN5
M_A_DQ62	BA25	DDR1_DQ[62]/DDR1_DQ[46]	DDR1_DQSP[5]/DDR1_DQSP[3]	AR32	M_B_DQSP5
M_A_DQ63	BB25	DDR1_DQ[63]/DDR1_DQ[47]	DDR0_DQSN[6]/DDR1_DQSN[4]	BA30	M_A_DQSN6
M_B_DQ48	AU27	DDR1_DQ[48]	DDR0_DQSP[6]/DDR1_DQSP[4]	AY30	M_A_DQSP6
M_B_DQ49	AT27	DDR1_DQ[49]	DDR0_DQSN[7]/DDR1_DQSN[5]	AY26	M_A_DQSN7
M_B_DQ50	AT25	DDR1_DQ[50]	DDR0_DQSP[7]/DDR1_DQSP[5]	BA26	M_A_DQSP7
M_B_DQ51	AU25	DDR1_DQ[51]	DDR1_DQSN[6]	AR25	M_B_DQSN6
M_B_DQ52	AP27	DDR1_DQ[52]	DDR1_DQSP[6]	AR27	M_B_DQSP6
M_B_DQ53	AN27	DDR1_DQ[53]	DDR1_DQSN[7]	AT22	M_B_DQSN7
M_B_DQ54	AN25	DDR1_DQ[54]	DDR1_DQSP[7]	AR21	M_B_DQSP7
M_B_DQ55	AP25	DDR1_DQ[55]			
M_B_DQ56	AT22	DDR1_DQ[56]	DDR1_ALERT#	AN43	M_B_ALERT# [18]
M_B_DQ57	AU22	DDR1_DQ[57]	DDR1_PAR	AP43	M_B_PARITY [18]
M_B_DQ58	AU21	DDR1_DQ[58]	DRAM_RESET#	AT13	SM_DRAMRST#
M_B_DQ59	AT21	DDR1_DQ[59]	DDR_RCOMP[0]	AR18	SM_RCOMP_0 R25 121/F_4
M_B_DQ60	AN22	DDR1_DQ[60]	DDR_RCOMP[1]	AT18	SM_RCOMP_1 R26 80.6/F_4
M_B_DQ61	AP22	DDR1_DQ[61]	DDR_RCOMP[2]	AU18	SM_RCOMP_2 R27 100/F_4
M_B_DQ62	AP21	DDR1_DQ[62]			
M_B_DQ63	AN21	DDR1_DQ[63]			

NIL-DDR CH - B

+1.2VSUS
R24 470/F_4
DDR3_DRAMRST# [17,18]

Interleave (IL) and Non-Interleave (NIL) Modes Mapping



BU5	PROJECT : G34A Quanta Computer Inc.		
Size: Custom	Document Number: 03 -- SKYPAKE 3/20(DDR3-A I/F)		Rev: 1A
Date: Tuesday, January 05, 2016	Sheet 3 of 47		

[10,11,12,14,15,16,18] +3V_DEEP_SUS
[2,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47] +3V
[10,15,16,25,32,33,35,36,37,38,42,43,46,47] +3VS5
[2,5,6,9,38,39] +VCCSTPLL
[2,6,16,33,38] +1.0V
[13,15,29,30,34,47] +BAT_RTC
[13,15] +3V_RTC_2

U1K SKL_ULT ?

SYSTEM POWER MANAGEMENT

Need apply PN

[33] RSMRST#
EC1 *220P/50V_4
R29 *10K_4 PROCPWRGD
C1 *0.1U/16V_4
[16] SYS_PWROK
[16,33] EC_PWROK
SUSWARN# *0_4 R32
[33] SUSACK#_EC 0_4 R34
[33] SUSWARN#_EC R33 0_4
[28,29,32,33] PCIE_WAKE#
[3,18] DDR_VTT_CNTL

PLTRST# AN10
SYS_RESET# B5
RSMRST# AY17
PROCPWRGD A68
H_VCCST_PWRGD B65
SYS_PWROK B6
PCH_PWROK BA20
DSWROK_EC_R BB20
SUSWARN# AR13
SUSACK# AP11
PCIE_WAKE# BB15
LAN_WAKE# AM15
AW17
DDR_VTT_CNTL AT15

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD

GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#

AT11 PCH_SLP_S0_N → PCH_SLP_S0_N [16,33]
AP15 → SUSB# [16,33]
BA16 → SUSC# [16,33]
AY16 → SLP_S5# [16]
AN15 SLP_SUS# → SLP_SUS#_EC [33]
AW15
BB17 GPD9 → TP8
AN16 → SLP_A# [16]
BA15 DNBSWON# → DNBSWON# [33]
AY15 AC_PRESENT_EC → AC_PRESENT_EC [33]
AU13 RF_OFF_PCH → RF_OFF_PCH [32]
AU11
AP16 INTRUDER# R
AM10
AM11 GPP_B2 → TP9

Ra
R36 *1M_4 +BAT_RTC
R305 1M_4 +3V_RTC_2
Rb
Modify 0922

Main BAT -->Ra
Coin BAT -->Rb (default)

1005 Change +3V_RTC to +BAT_RTC

*SKL_ULT
REV = 1
11 OF 20
?

PCH Pull-high/low(CLG)

+3V_DEEP_SUS
SUSWARN# R28 *10K_4
SUSACK# R30 10K_4
RF_OFF_PCH R31 10K_4
+3VS5
PCIE_WAKE# R35 1K_4
AC_PRESENT_EC R37 *10K_4
LAN_WAKE# R38 *10K_4
+3V
SYS_RESET# R39 10K_4
RSMRST# R40 10K_4
DSWROK_EC R41 100K/F_4

For DS3 Sequence

For DS3 -->Ra
Non-DS3 -->Rb

Rb
RSMRST# R42 *0_4
[33] DSWROK_EC R46 0_4 DSWROK_EC_R
Ra

PLTRST#(CLG)

Check Rise/Fall time less than 100ns

PLTRST# [16,19,28,29,31,32,33]
R52 100K/F_4

System PWR_OK(CLG)

SYS_PWROK R53 0_4 EC_PWROK
R54 10K/F_4

+1.0V +VCCSTPLL
R47 1K_4
R48 *1K_4
Ra
[16,33,35,36,37] HWPG
D1 1 2 MEK500V-40
H_VCCST_PWRGD_R R50 60.4/F_4 H_VCCST_PWRGD
C3 *10P/50V_4

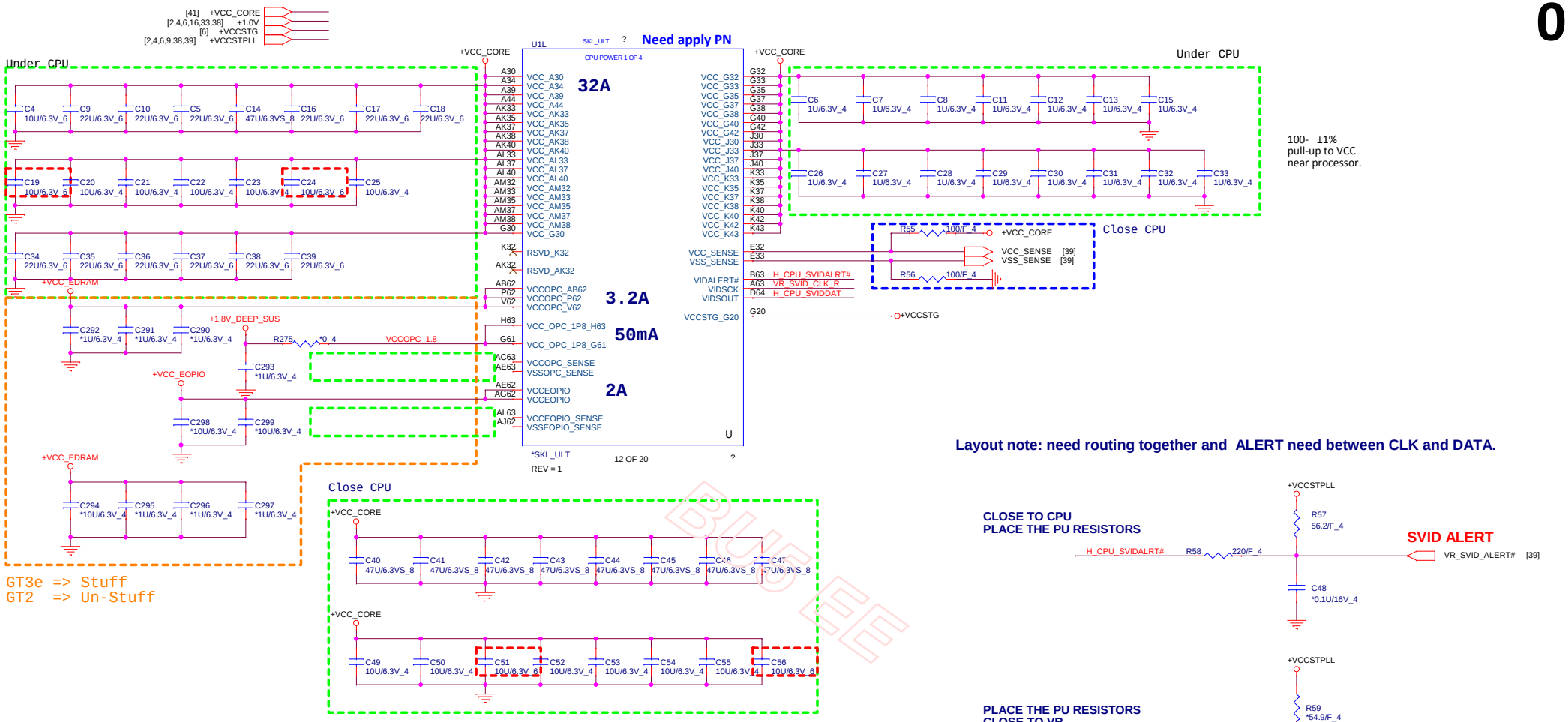
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+1.0V +5VS5 +3VS5
R43 15K/F_4
R44 100K_4
R45 10K_4
HWPG
+1.0V_PWRGD_G2
Q1 2N7002K
R49 100K_4
+1.0V_PWRGD_G1
Q2 METR3904-G
C2 0.1U/16V_4
R51 100K_4

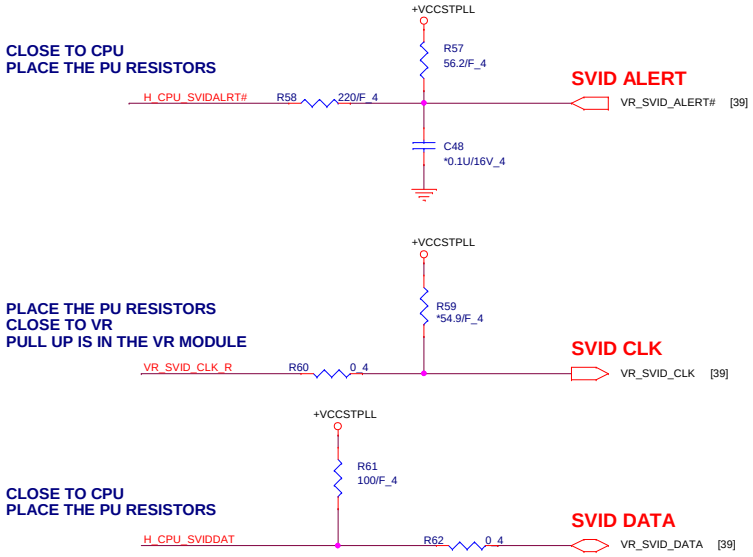
BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 -- SKYPAKE 5/20(Power Manger)	1A
Date: Tuesday, January 05, 2016	Sheet 4 of 47	



Layout note: need routing together and ALERT need between CLK and DATA.

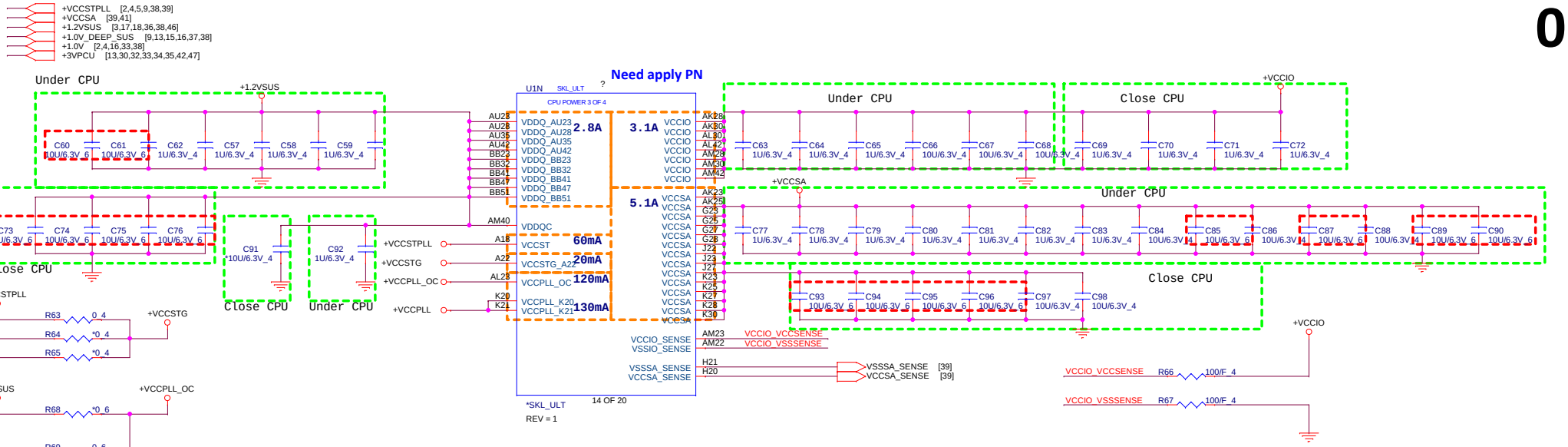


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

BU5

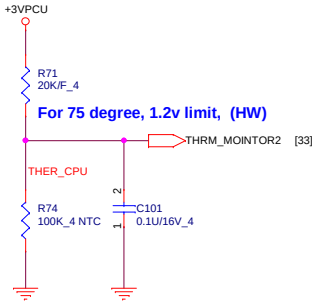
PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYPAKE 6/20 (POWER-1)	1A
Date: Tuesday, January 05, 2016	Sheet 5 of 47	

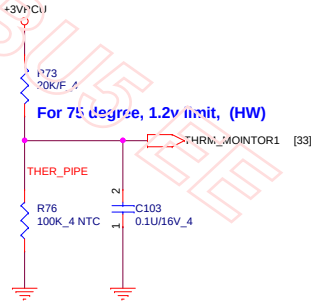


IO Thrm Protect

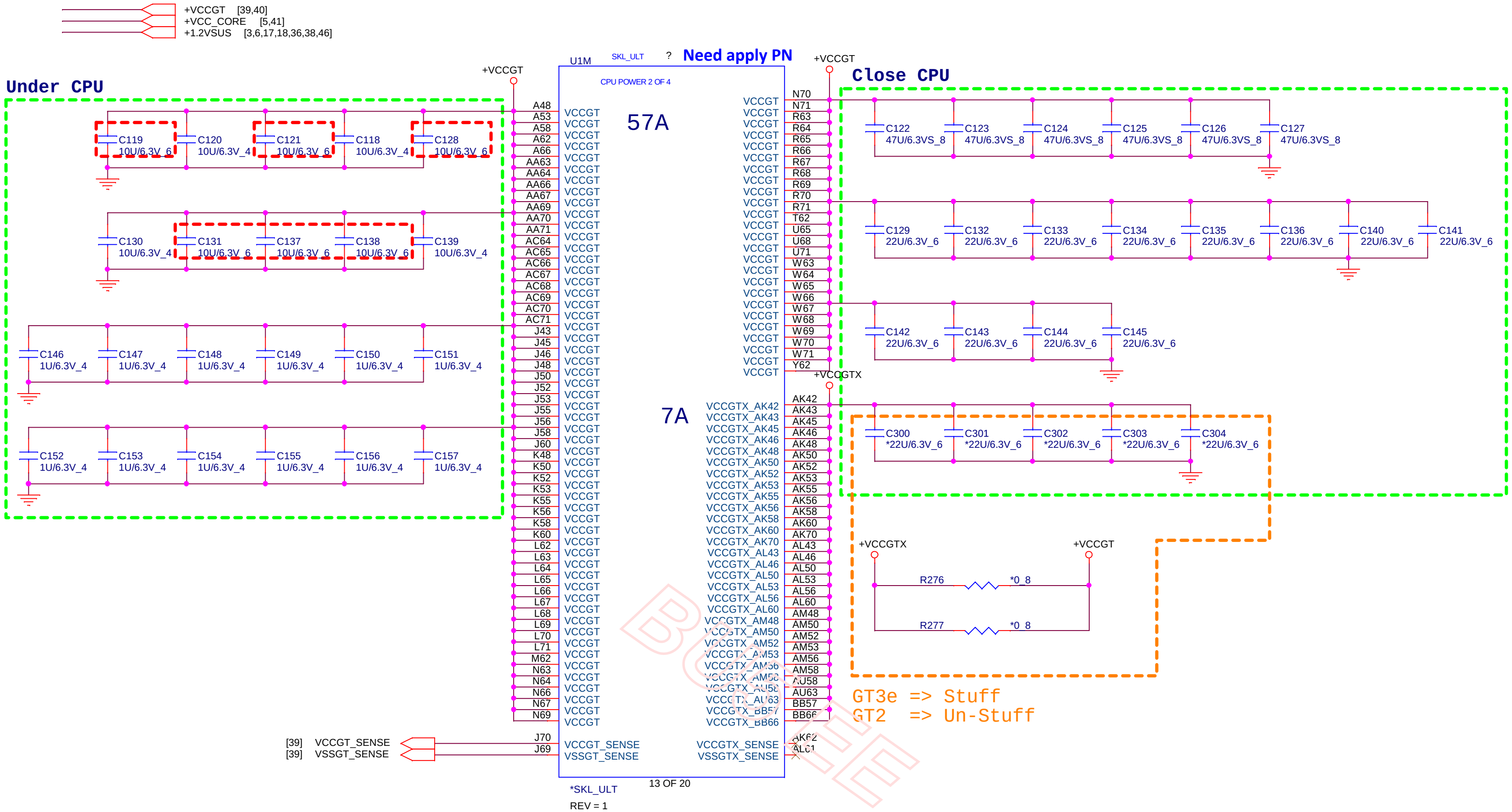
For CPU USE



For PIPE USE



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



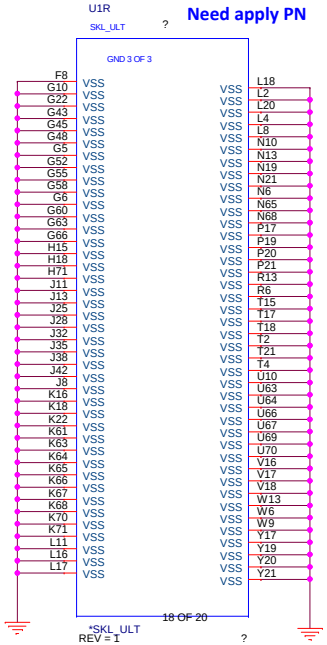
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

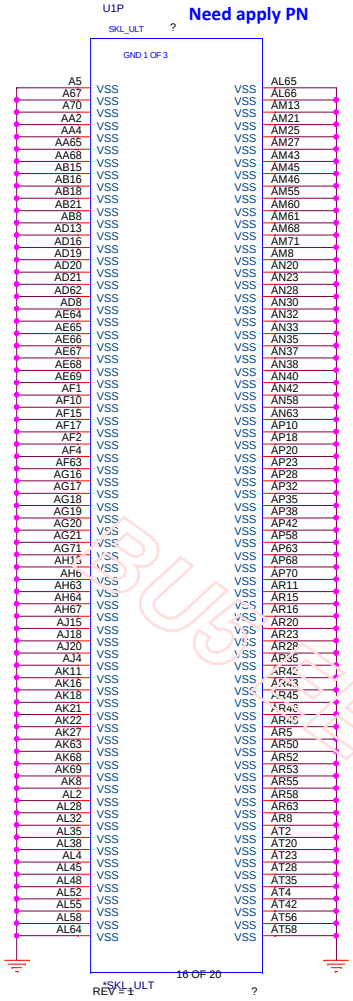
BU5

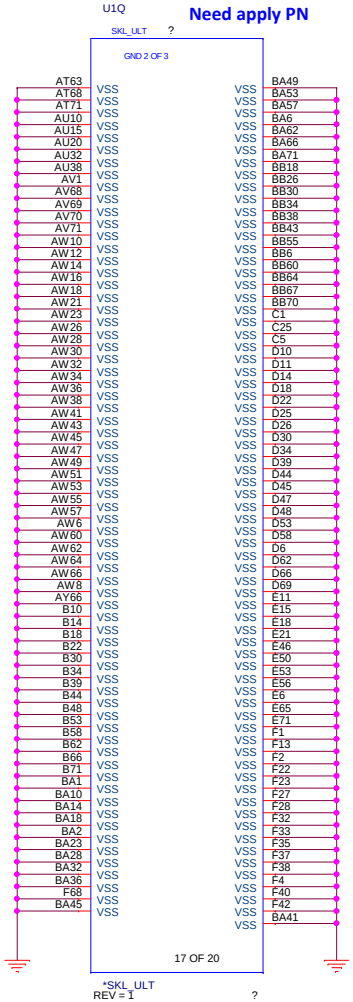
PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 -- SKYPAKE 8/20 (POWER-3)	1A

Date: Tuesday, January 05, 2016 Sheet 7 of 47



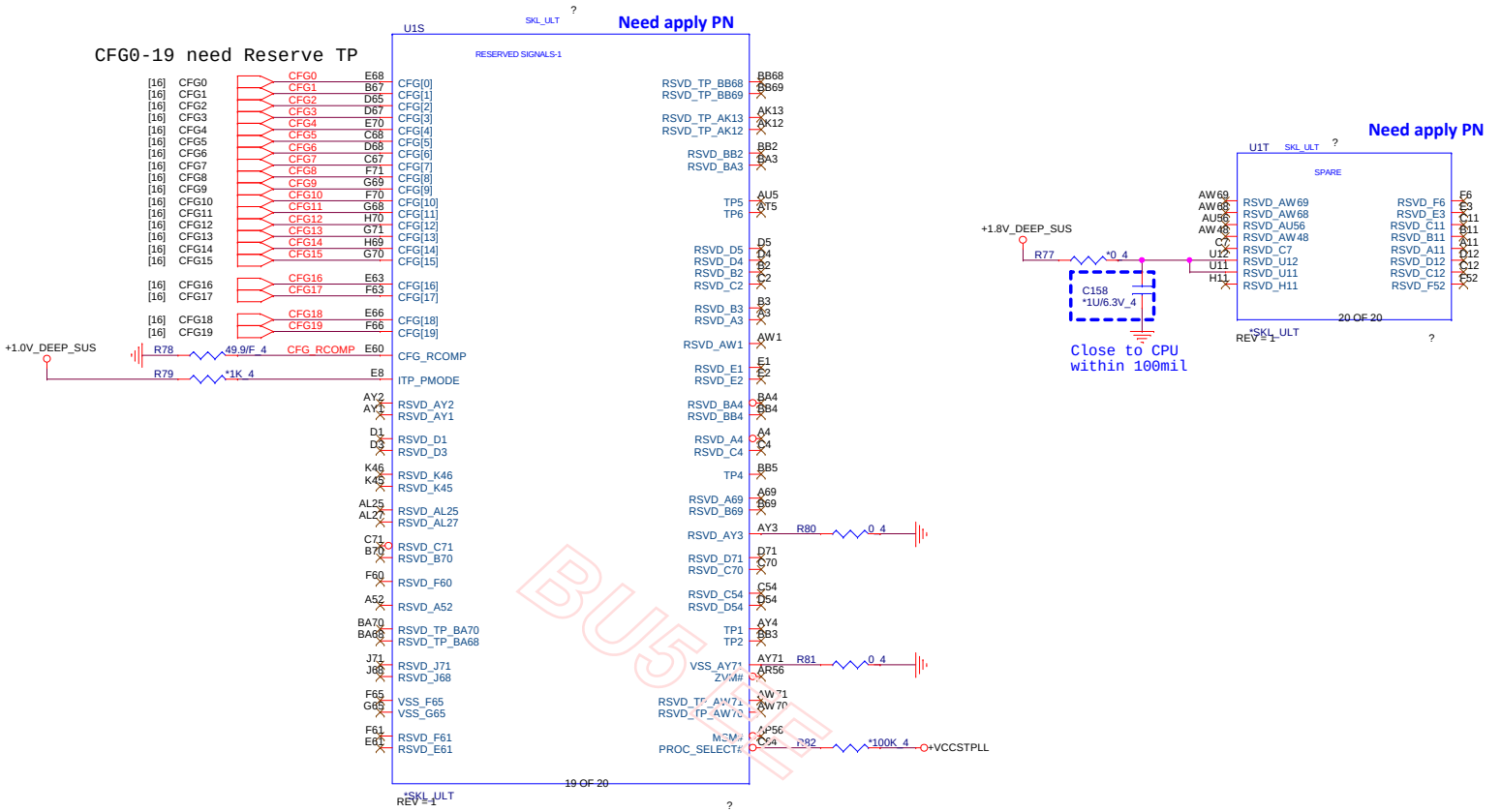




BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	8 – SKYPAKE 9/20 (GND-1)	1A
Date: Tuesday, January 05, 2016	Sheet 8 of 47	



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

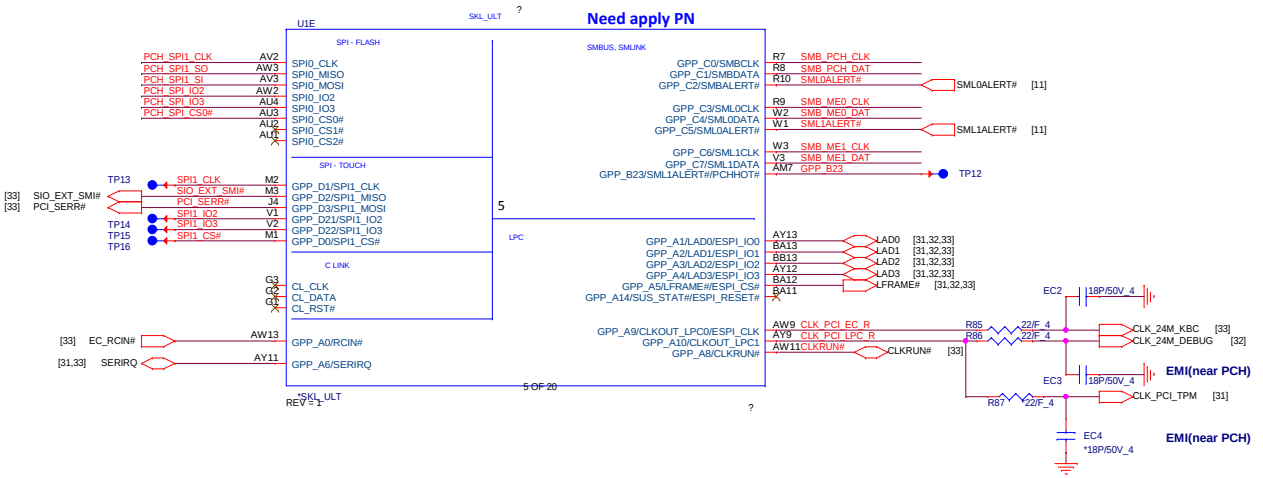
BU5

PROJECT : G34A
Quanta Computer Inc.

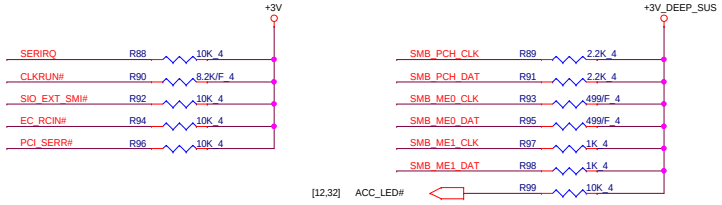
Size	Document Number	Rev
Custom	9 -- SKYPAKE 12/20 (RSV-1)	1A

Date: Tuesday, January 05, 2016 | Sheet 9 of 47

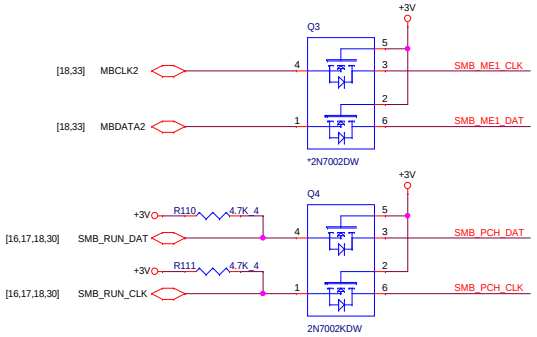
+3V_DEEP_SUS [4,11,12,14,15,16,18]
+3V [2,4,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]
+5V [25,26,27,30,32,43]
+1.0V [2,4,6,16,33,38]
+3VS5 [4,15,16,25,32,33,35,36,37,38,42,43,46,47]



GPIO Pull UP



SMBus/Pull-up(CLG)



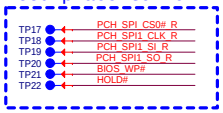
CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

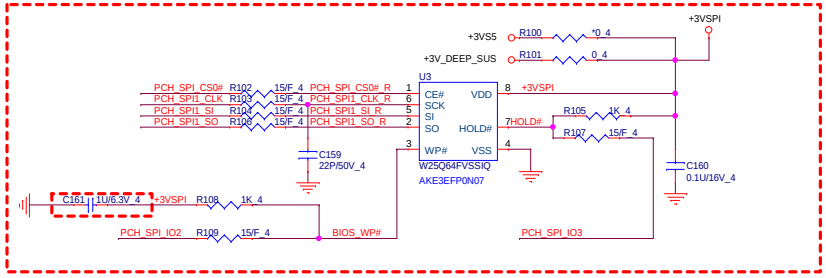
PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

need place to TOP



PCH SPI ROM(CLG)



1005 Change P/N to DFHS08FS023(Socket)

BU5

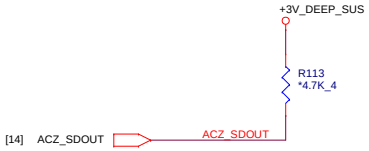
PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)	1A
Date: Tuesday, January 05, 2016	Sheet 10 of 47	

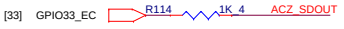
Functional Strap Definitions

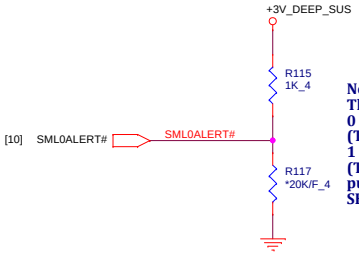
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

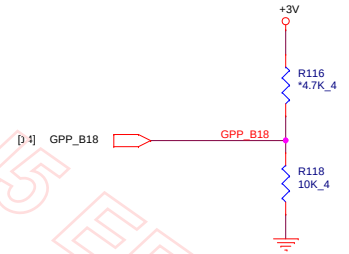


No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

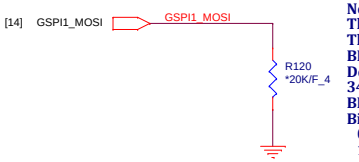




No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

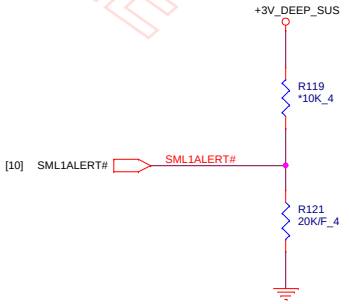


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

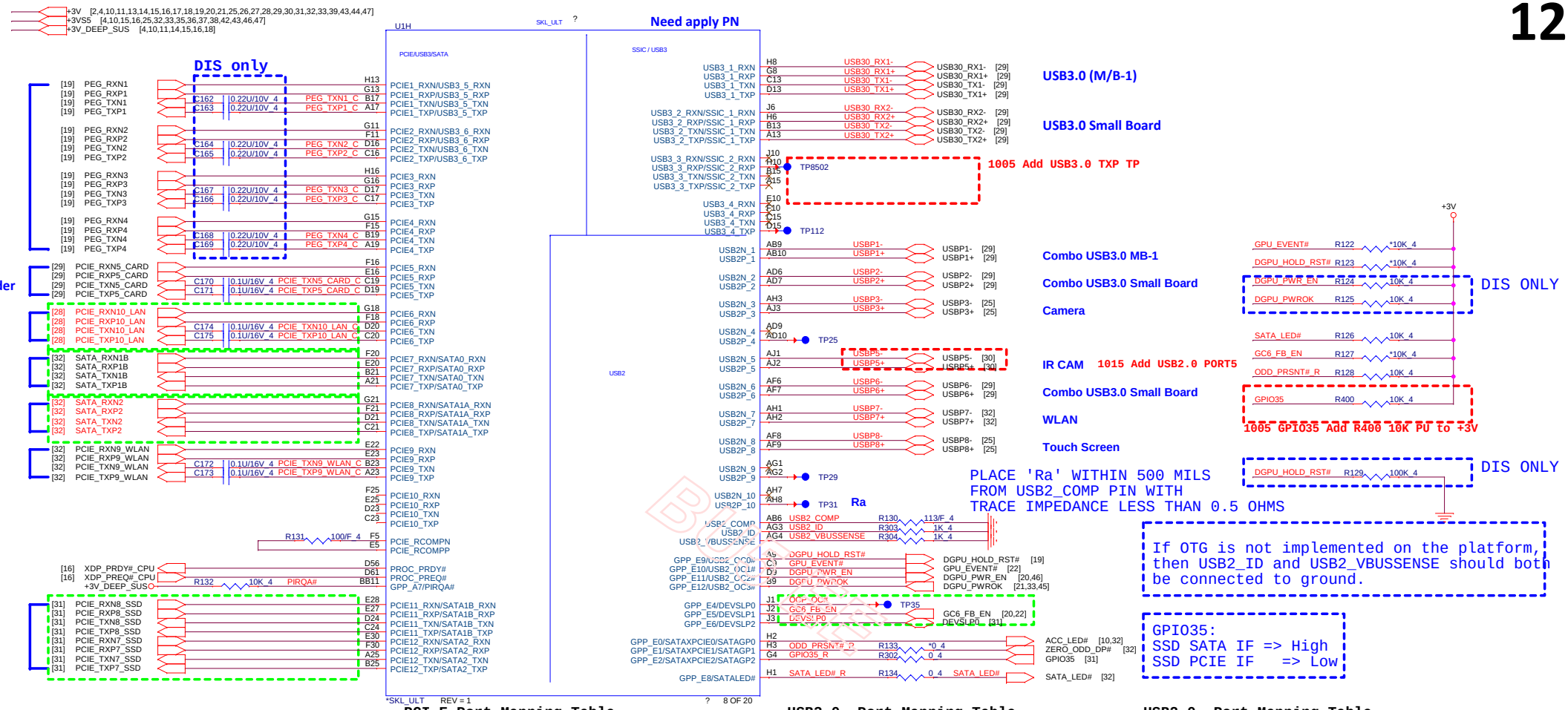


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	CR
Port3	dGPU	Port2	SSD
Port4	dGPU	Port3	WLAN
Port5	CardReader	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	ODD		
Port9	WLAN		
Port10	Un-used		
Port11	SSDx2		
Port12	SSDx2/ SATA2		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	NC
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	Camera
PORT-4	NC
PORT-5	IR CAM
PORT-6	Cobime USB3.0 Small Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- SKYPAKE 16/20 (PCIE/USB)	1A
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BU5

+3V_RTC_2 [4,15]
+BAT_RTC [4,15,29,30,34,47]
+1.8V_DEEP_SUS [5,9,15,37,47]
+3V [2,4,10,11,12,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]

VGA
Cardreader
SSD
WLAN
LAN

1005 SWAP CLK RQ Port

U1J SKL_ULT ? Need apply PN

CLOCK SIGNALS

CLKOUT_PCIE_N0 D42
CLKOUT_PCIE_P0 C42
GPP_B5/SRCCLKREQ0# AR10
CLKOUT_PCIE_N1 B42
CLKOUT_PCIE_P1 A42
GPP_B6/SRCCLKREQ1# AT7
CLKOUT_PCIE_N2 D41
CLKOUT_PCIE_P2 C41
GPP_B7/SRCCLKREQ2# AT8
CLKOUT_PCIE_N3 D40
CLKOUT_PCIE_P3 C40
GPP_B8/SRCCLKREQ3# AT10
CLKOUT_PCIE_N4 B40
CLKOUT_PCIE_P4 A40
GPP_B9/SRCCLKREQ4# AU8
CLKOUT_PCIE_N5 E40
CLKOUT_PCIE_P5 E39
GPP_B10/SRCCLKREQ5# AU7

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17
XTAL24_IN E37
XTAL24_OUT E35
XCLK_BIASREF E42
RTCX1 AM18
RTCX2 AM20
SRTCRST# AN18
RTCRST# AM16

Install for XDP
RP1 *0_4P2R_4
CK_XDP_N_R F43
CK_XDP_P_R E43
CK_XDP_N [16]
CK_XDP_P [16]
+1.0V_DEEP_SUS
R135 2.7K/F_4
R137 *60.4/F_4
XCLK_BIASREF
RTC_X1 AM18
RTC_X2 AM20
TP38
SRTC_RST# AN18
RTC_RST# AM16
RTC_RST# [16]

*SKL_ULT REV = 1
10 OF 20
TBT

CLK_REQ/Strap Pin(CLG)

+3V
PCIE_CLKREQ_VGA# R136 10K_4
PCIE_CLKREQ_WLAN# R138 10K_4
PCIE_CLKREQ_LAN# R139 10K_4
PCIE_CLKREQ_CR# R140 10K_4
PCIE_CLKREQ_SSD# R141 10K_4
PCIE_CLKREQ5# R142 10K_4

U1I SKL_ULT ? Need apply PN

CSI-2

CSI2_DN0 A36
CSI2_DP0 B36
CSI2_DN1 C36
CSI2_DP1 D36
CSI2_DN2 C35
CSI2_DP2 D35
CSI2_DN3 A35
CSI2_DP3 B35
CSI2_DN4 C31
CSI2_DP4 D31
CSI2_DN5 C33
CSI2_DP5 D33
CSI2_DN6 A33
CSI2_DP6 B33
CSI2_DN7 A31
CSI2_DP7 B31
CSI2_DN8 A29
CSI2_DP8 B29
CSI2_DN9 C29
CSI2_DP9 D29
CSI2_DN10 A27
CSI2_DP10 B27
CSI2_DN11 C27
CSI2_DP11 D27

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 C32
CSI2_CLKP1 D32
CSI2_CLKN2 C29
CSI2_CLKP2 D29
CSI2_CLKN3 C26
CSI2_CLKP3 D26
CSI2_COMP E13
GPP_D4/FLASHTRIG B7
R143 100/F_4
TP39

1005 Delete TP

EMMC
GPP_F13/EMMC_DATA0
GPP_F14/EMMC_DATA1
GPP_F15/EMMC_DATA2
GPP_F16/EMMC_DATA3
GPP_F17/EMMC_DATA4
GPP_F18/EMMC_DATA5
GPP_F19/EMMC_DATA6
GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK
GPP_F22/EMMC_CLK
GPP_F12/EMMC_CMD
EMMC_RCOMP AT1
EMMC_RCOMP R144 200/F_4

*SKL_ULT REV = 1
9 OF 20

RTC Clock 32.768KHz

C177 12P/50V_4
Y1 32.768KHZ
C179 12P/50V_4
R147 10M_4
RTC_X1
RTC_X2

RTC Circuitry(RTC)

30mils
+3V_RTC_2
+BAT_RTC
1005 Change +3V_RTC to +BAT_RTC
Main BAT -->Ra
Coin BAT -->Rb (default)
Rb
Ra
R306 0_4
R307 *0_4
R145 *0_6
R146 20K/F_4
RTC_RST#
RTC Power trace width 20mils.
C178 1U/6.3V_4
R149 20K/F_4
SRTC_RST#
C182 1U/6.3V_4
+3V_RTC_0
+3VPCU
R150 1K_4
+3V_RTC_1
D2 BAT54CW-7-F
C181 1U/6.3V_4
CN1 BAT_CONN DFHS02FS027 BAT-23_2-4_2
RTC_RST# R152 *0_6 SRTC_RST#
Q5 2N7002K
EC_RTC_RST [33]
R151 10K_4

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

TP51
C176 27P/50V_4
XTAL24_IN
XTAL24_OUT
R148 1M_4
24MHZ +-20PPM
Y2
C180 27P/50V_4
TP52

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYPAKE 17/20 (CLK)	1A
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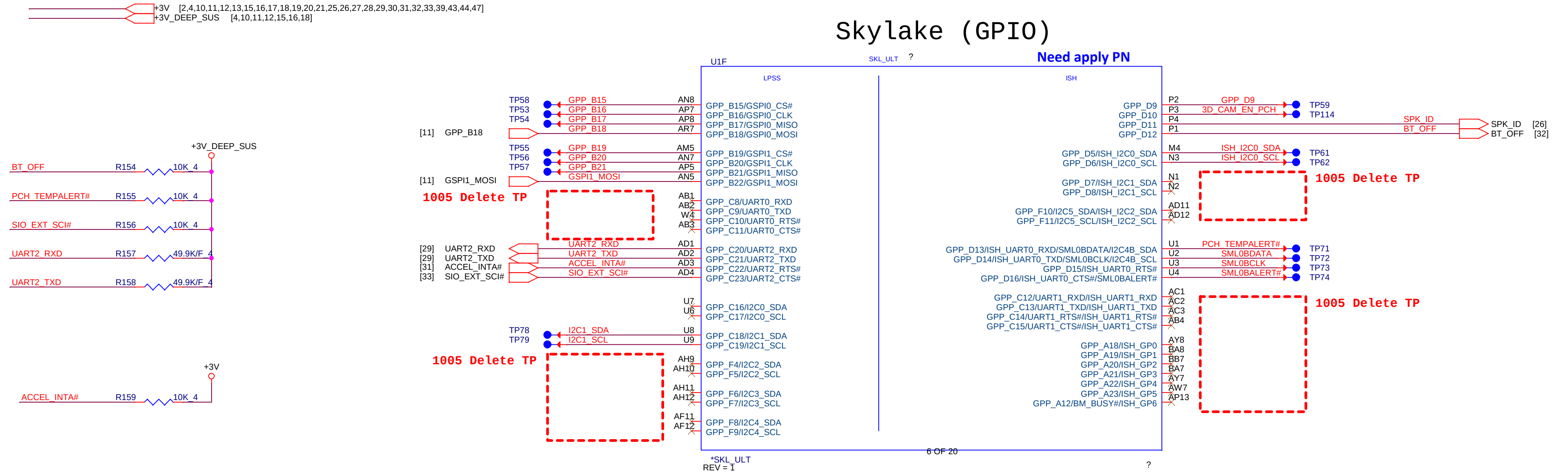
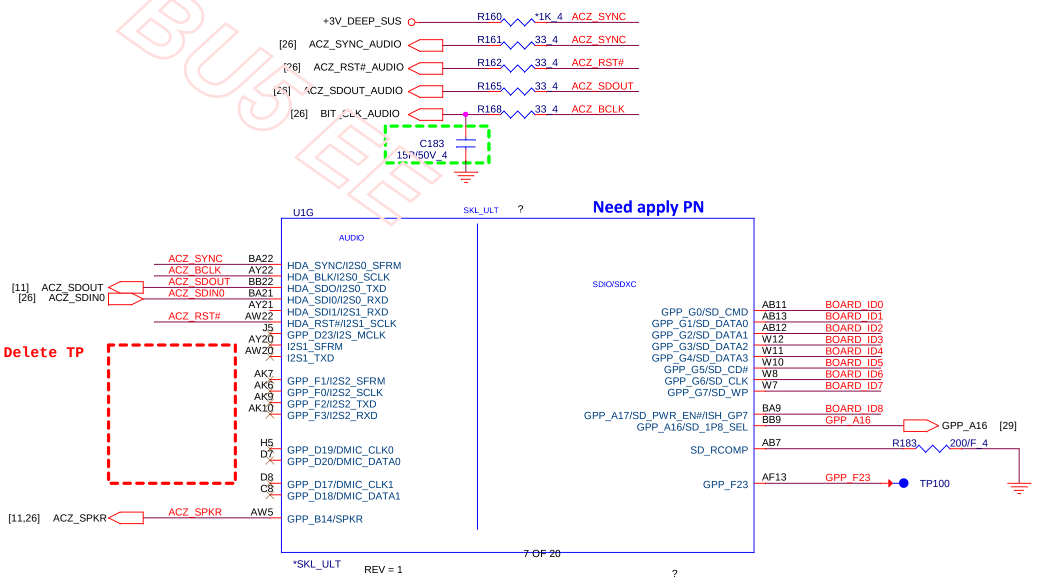
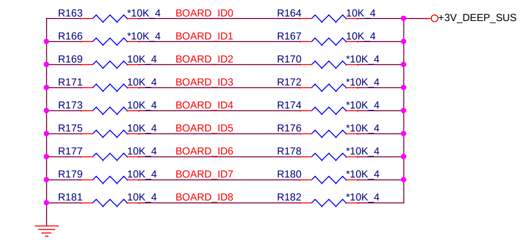
Skylake (GPIO)



HDA Bus(CLG)





Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	Reserve (Default = 00)	00 14" 01 15" 10 Reserve 11 Reserve	0 : UMA 1 : DIS

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 -- SKYPAKE 19/20 (GPIO)	1A

[4,10,11,12,14,16,18] +3V_DEEP_SUS
[9,13,16,37,38] +1.0V_DEEP_SUS
[5,9,37,47] +1.8V_DEEP_SUS
[4,13,29,30,34,47] +BAT_RTC
[4,10,16,25,32,33,35,36,37,38,42,43,46,47] +3VS5

U1O SKL_ULT
CPU POWER 4 OF 4
15 OF 20
*SKL_ULT
REV = 1

Need apply PN

PCH Internal VRM

Ca and Cb close to CPU less then 100 mils

+VCCPRIM → VCCPRIM_1P0 (AB19, AB20, P18) 2.899A
+1.0V_DEEP_SUS → VCCPRIM_CORE (AF18, AF19, V20, V21) 2.57A
+VCCDSW_1.0V → DCPDSW_1P0 (AL1)
+1.0V_DEEP_SUS → VCCMPHYAON_1P0 (K17, L1) via R188 0_6
+1.0V_DEEP_SUS → VCCMPHYGT_1P0 (N15, N16, N17, P15, P16) 1.714A
+1.0V_DEEP_SUS → VCCAMPHYPLL_1P0 (K15, L15) via R194 0_6
+1.0V_DEEP_SUS → VCCAPLL_1P0 (V15) via R196 0_6 0.03A
+1.0V_DEEP_SUS → VCCPRIM_1P0_AB17 (AB17, Y18) via R199 0_6
+3VS5 → VCCDSW_3P3_AD17 (AD17, AD18, AJ17) via R201 0_4 0.09A
+V3.3DX_1.5DX_ADO → VCCHDA (AJ19)
+3V_DEEP_SUS → VCCSPI (AJ16) via R205 0_6
+1.0V_DEEP_SUS → VCCSRAM_1P0 (AF20, AF21, T19, T20) via R206 0_6
+3V_DEEP_SUS → VCCPRIM_3P3_AJ21 via R207 0_6
+1.0V_DEEP_SUS → VCCPRIM_1P0_AK20 via R208 0_6
+1.0V_DEEP_SUS → VCCAPLLEBB (N18) via R209 0_6

C184 1U/6.3V_4 · C185 1U/6.3V_4 · C187 1U/6.3V_4 · C188 1U/6.3V_4 · C189 1U/6.3V_4 · C190 47U/6.3VS_8 · C192 1U/6.3V_4 · C193 1U/6.3V_4 · C194 1U/6.3V_4 · C196 1U/6.3V_4 · C197 1U/6.3V_4

VCCPGPPA (AK15 +VCCPGPPA) · VCCPGPPB (AG15 +VCCPGPPB) · VCCPGPPC (Y16 +VCCPGPPC) · VCCPGPPD (Y15 +VCCPGPPD) · VCCPGPPE (T16 +VCCPGPPE) · VCCPGPPF (AF16 +VCCPGPPF) · VCCPGPPG (AD15 +VCCPGPPG)

VCCPRIM_3P3_V19 (V19) → C186 1U/6.3V_4 → +3V_DEEP_SUS
VCCPRIM_1P0_T1 (T1 +VCCPRIM_1.0V_T1) via R187 0_6 → +1.0V_DEEP_SUS
VCCATS_1P8 (AA1 +VCCATS_1.8V) via R190 0_6 → +1.8V_DEEP_SUS
VCCRTCPRIM_3P3 (AK17 +VCCRTCPRIM_3.3V) via R192 0_6 → +3V_DEEP_SUS
VCCRTC_AK19 (AK19 +VCCRTC) via Ra R308 *0_4
VCCRTC_BB14 (BB14) via Rb R309 0_4 → +BAT_RTC → +3V_RTC_2

Main BAT -->Ra
Coin BAT -->Rb (default)
20mils

DCPRTC (BB10 DCPRTC) Cb C191 0.1U/16V_4 → +1.0V_DEEP_SUS
1005 Change +3V_RTC to +BAT_RTC

VCCCLK1 (A14 +VCCCLK1) via R195 0_6
VCCCLK2 (K19 +VCCCLK2) via R198 0_6
VCCCLK3 (L21 +VCCCLK3) via R200 0_6
VCCCLK4 (N20 +VCCCLK4) via R202 0_6
VCCCLK5 (L19 +VCCCLK5) via R203 0_6
VCCCLK6 (A10 +VCCCLK6) via R204 0_6 C195 1U/6.3V_4 → +1.0V_DEEP_SUS

GPP_B0/CORE_VID0 (AN11 CORE_VID0) → TP102
GPP_B1/CORE_VID1 (AN13 CORE_VID1) → TP103

+3V_DEEP_SUS
+VCCPGPPA R184 0_6
+VCCPGPPB R185 0_6
+VCCPGPPC R186 0_6
+VCCPGPPD R189 0_6
+VCCPGPPE R191 0_6
+VCCPGPPG R193 0_6
+1.8V_DEEP_SUS
+VCCPGPPF R197 0_6

+V3.3DX_1.5DX_ADO → R210 0_4 → +3V
+1.0V_DEEP_SUS → C203 *1U/6.3V_4 · C204 *22U/6.3V_6

for DS3

+3VS5 → R211 100K_4 · C205 1U/6.3V_4
U4 AP2821KTR-G1: IN (5), IN (4), ON/OFF (3), OUT (1), GND (2)
[33,37,38] SLP_SUS_ON → ON/OFF
C210 *10P/50V_4
+3V_DEEP_SUS → C209 0.1U/16V_4

+VCCATS_1.8V → C198 1U/6.3V_4 · C199 0.1U/16V_4
+VCCRTC → C200 1U/6.3V_4
+VCCRTCPRIM_3.3V → C201 1U/6.3V_4 · C202 0.1U/16V_4
+VCCPGPPB → C206 1U/6.3V_4
+VCCPGPPC → C207 1U/6.3V_4
+VCCPGPPE → C208 1U/6.3V_4

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	15 -- SKYPAKE 20/20(PCH POWER)	1A
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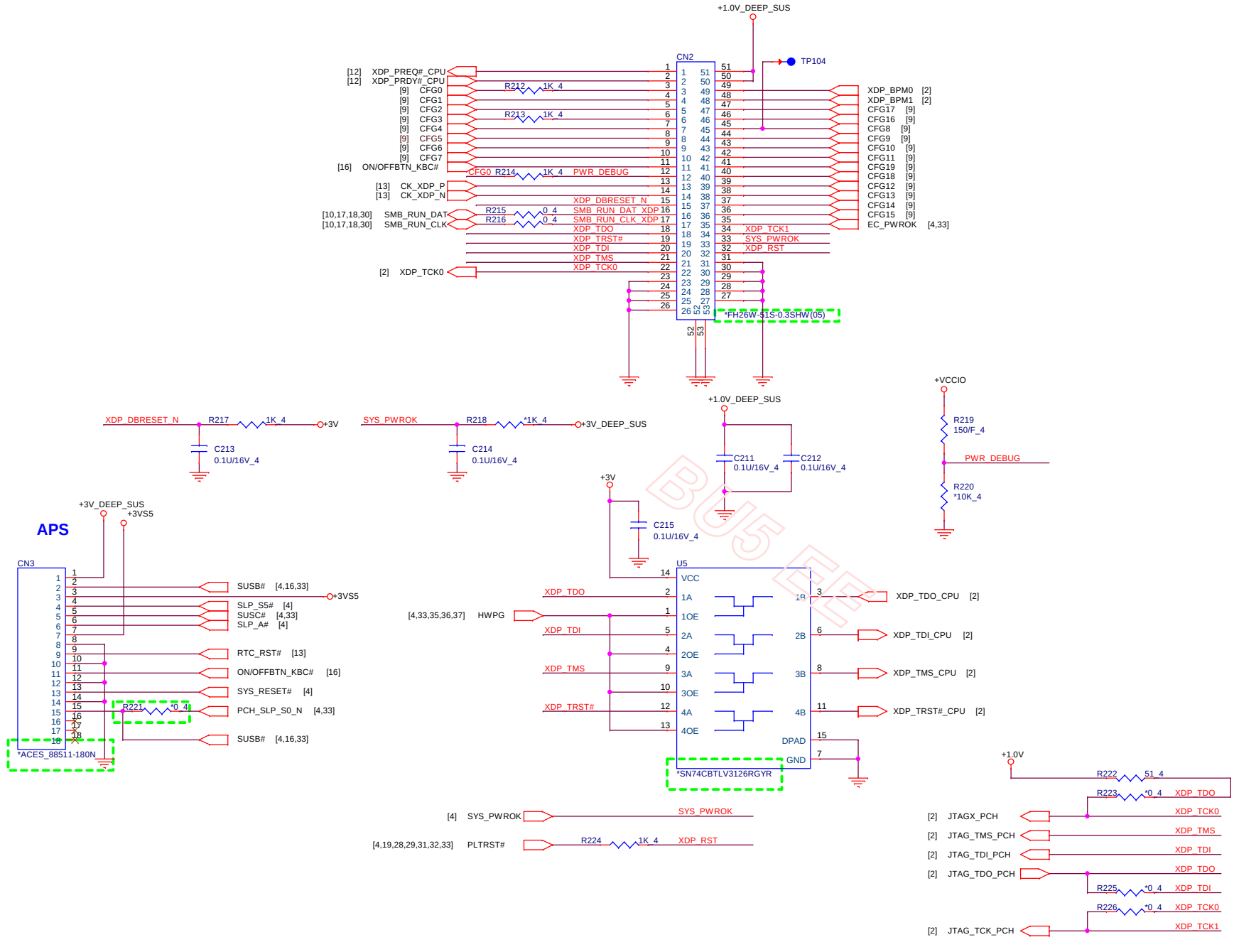
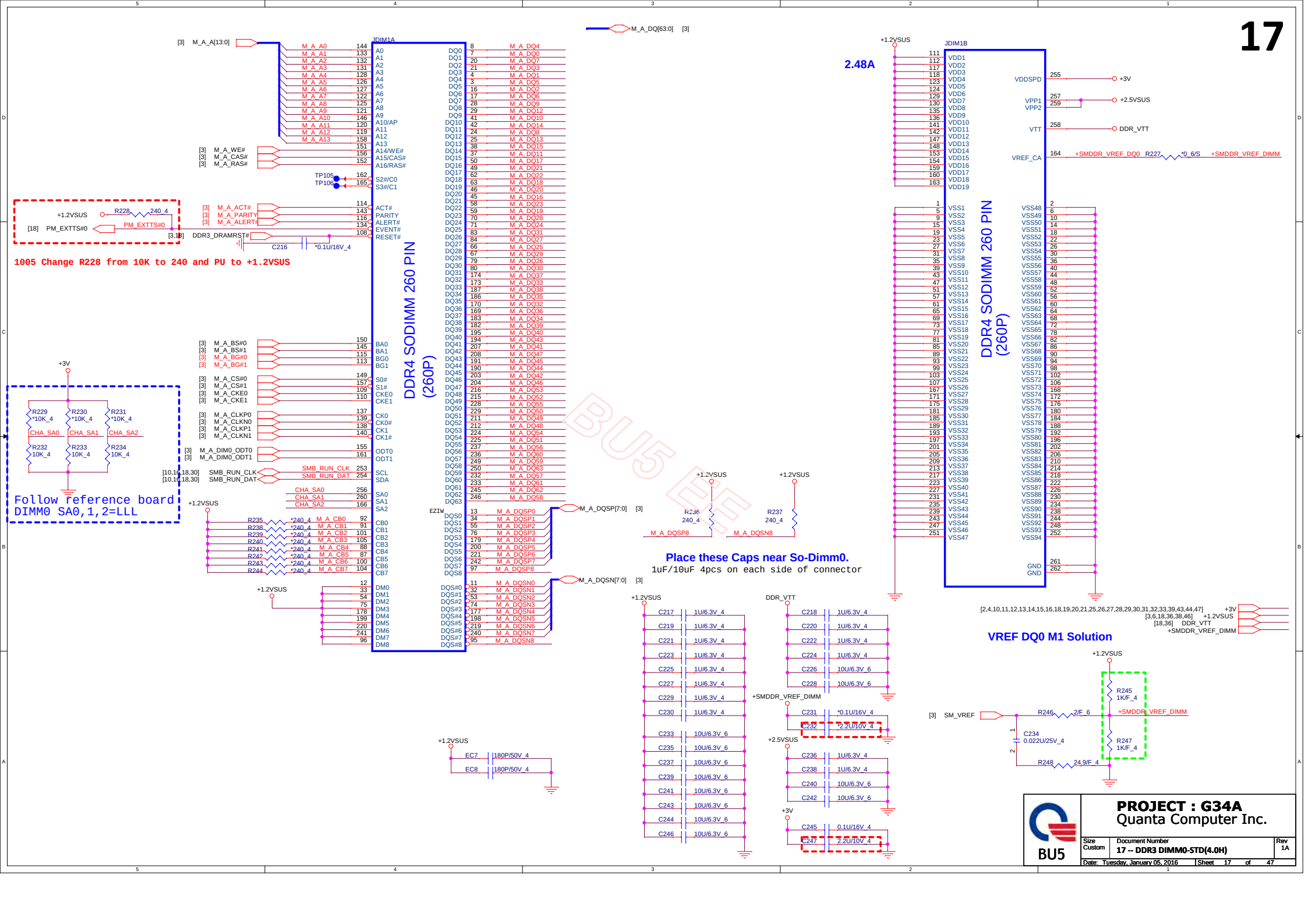


BU5	**PROJECT : G34A** Quanta Computer Inc.	
Size	Document Number **16 -- HSW XDP & APS**	Rev 1A
Date: Tuesday, January 05, 2016	Sheet 16 of 47	


JDIM1A
DDR4 SODIMM 260 PIN (260P)
JDIM1B
DDR4 SODIMM 260 PIN (260P)
2.48A
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : G34A
Quanta Computer Inc.
BU5
Size Custom
Document Number
17 -- DDR3 DIMM0-STD(4.0H)
Rev 1A
Date: Tuesday, January 05, 2016
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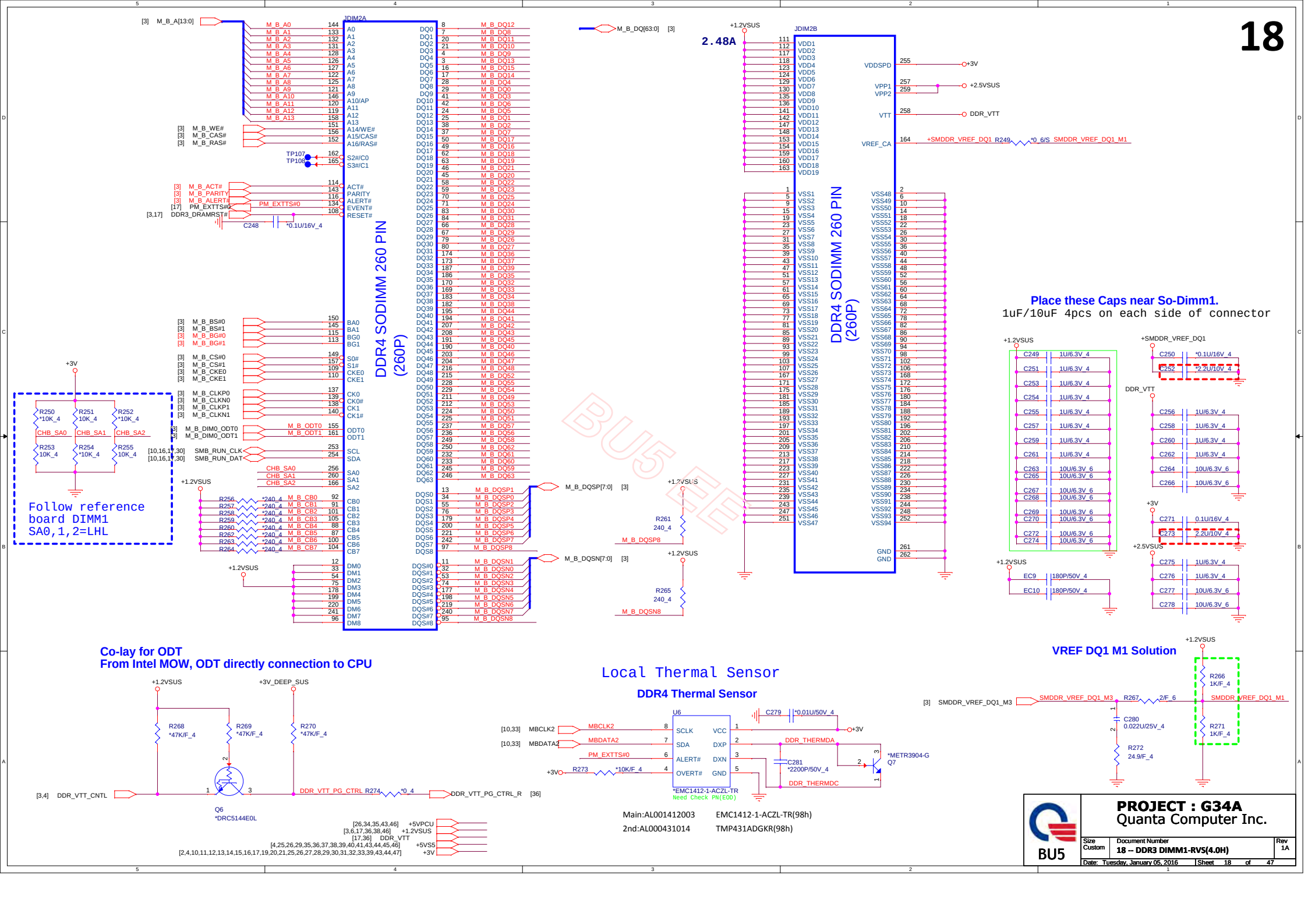
JDIM2A
DDR4 SODIMM 260 PIN (260P)
M_B_A[13:0]
M_B_WE#
M_B_CAS#
M_B_RAS#
TP107
TP108
M_B_ACT#
M_B_PARITY
M_B_ALERT#
PM_EXTTS#0
DDR3_DRAMRST#
C248
*0.1U/16V_4
M_B_BS#0
M_B_BS#1
M_B_BG#0
M_B_BG#1
M_B_CS#0
M_B_CS#1
M_B_CKE0
M_B_CKE1
M_B_CLKP0
M_B_CLKN0
M_B_CLKP1
M_B_CLKN1
M_B_DIM0_ODT0
M_B_DIM0_ODT1
SMB_RUN_CLK
SMB_RUN_DAT
CHB_SA0
CHB_SA1
CHB_SA2
M_B_CB0
M_B_CB1
M_B_CB2
M_B_CB3
M_B_CB4
M_B_CB5
M_B_CB6
M_B_CB7
M_B_DQ[63:0]
M_B_DQSP[7:0]
M_B_DQSN[7:0]
R261
240_4
M_B_DQSP8
R265
M_B_DQSN8
+1.2VSUS
+3V
Follow reference board DIMM1 SA0,1,2=LHL
JDIM2B
DDR4 SODIMM 260 PIN (260P)
2.48A
VDDSPD
VPP1
VPP2
VTT
VREF_CA
+SMDDR_VREF_DQ1 R249
*0_6/S_SMDDR_VREF_DQ1_M1
DDR_VTT
+2.5VSUS
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
+SMDDR_VREF_DQ1
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU
+3V_DEEP_SUS
R268 *47K/F_4
R269 *47K/F_4
R270 *47K/F_4
Q6
*DRC5144E0L
DDR_VTT_CNTL
DDR_VTT_PG_CTRL
R274 *0_4
DDR_VTT_PG_CTRL_R
Local Thermal Sensor
DDR4 Thermal Sensor
U6
MBCLK2
MBDATA2
PM_EXTTS#0
R273 *10K/F_4
C279 *0.01U/50V_4
C281 *2200P/50V_4
DDR_THERMDA
DDR_THERMDC
*METR3904-G
Q7
*EMC1412-1-ACZL-TR
Need Check PN(E0D)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
VREF DQ1 M1 Solution
SMDDR_VREF_DQ1_M3
R266 1K/F_4
R267 2/F_6
R271 1K/F_4
C280 0.022U/25V_4
R272 24.9/F_4
SMDDR_VREF_DQ1_M1
BU5
PROJECT : G34A
Quanta Computer Inc.
Size Custom
Document Number 18 -- DDR3 DIMM1-RVS(4.0H)
Rev 1A
Date: Tuesday, January 05, 2016
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PEX_IOVDD + PEX_IOVDDQ = 1.042A

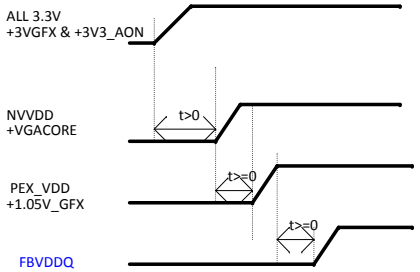
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

NVDD = 32.22 ~ 26.66 A

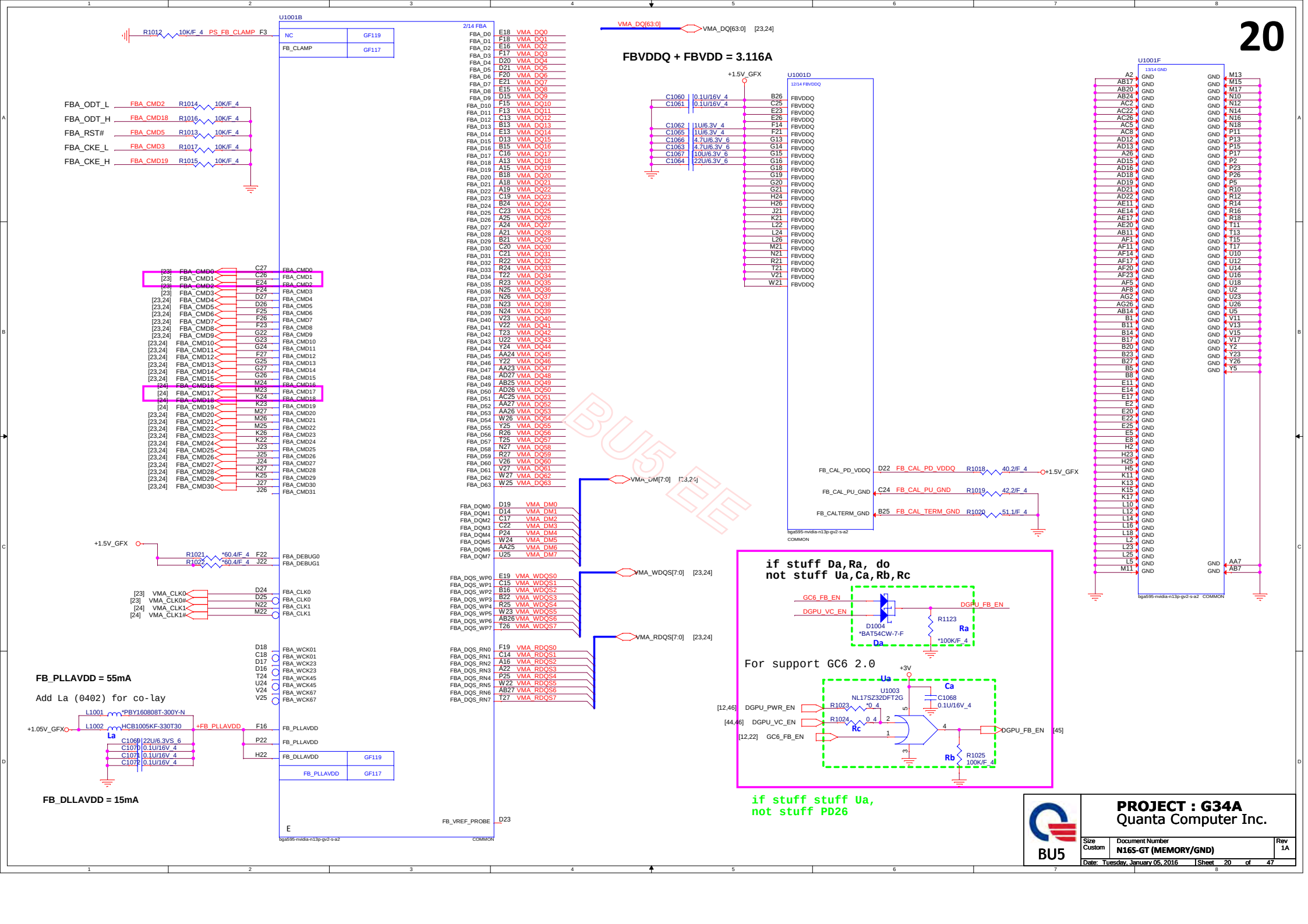
VDD33 = 56mA

Power up sequence



if stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd

BU5	**PROJECT : G34A** Quanta Computer Inc.	
Size Custom	Document Number **N16S-GT (PCIE I/F) /NVDD**	Rev 1A
Date: Tuesday, January 05, 2016	Sheet 19 of 47	


U1001B
2/14 FBA
R1012 10K/F_4 PS_FB_CLAMP F3
NC GF119
FB_CLAMP GF117
FBA_ODT_L FBA_CMD2 R1014 10K/F_4
FBA_ODT_H FBA_CMD18 R1016 10K/F_4
FBA_RST# FBA_CMD5 R1013 10K/F_4
FBA_CKE_L FBA_CMD3 R1017 10K/F_4
FBA_CKE_H FBA_CMD19 R1015 10K/F_4
FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30 FBA_CMD31
+1.5V_GFX
R1021 *60.4/F_4 F22 FBA_DEBUG0
R1022 *60.4/F_4 J22 FBA_DEBUG1
VMA_CLK0 VMA_CLK0# VMA_CLK1 VMA_CLK1#
FBA_CLK0 FBA_CLK0 FBA_CLK1 FBA_CLK1
FBA_WCK01 FBA_WCK01 FBA_WCK23 FBA_WCK23 FBA_WCK45 FBA_WCK45 FBA_WCK67 FBA_WCK67
FB_PLLAVDD = 55mA
Add La (0402) for co-lay
L1001 *PBY160808T-300Y-N
L1002 HCB1005KF-330T30
+1.05V_GFX
+FB_PLLAVDD
La
C1069 22U/6.3VS_6
C1070 0.1U/16V_4
C1071 0.1U/16V_4
C1072 0.1U/16V_4
FB_PLLAVDD F16
FB_PLLAVDD P22
FB_PLLAVDD H22
FB_DLLAVDD GF119
FB_PLLAVDD GF117
FB_DLLAVDD = 15mA
FB_VREF_PROBE D23
bga595-nvidia-n13p-gv2-s-a2 COMMON
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63
VMA_DQ0 VMA_DQ1 VMA_DQ2 VMA_DQ3 VMA_DQ4 VMA_DQ5 VMA_DQ6 VMA_DQ7 VMA_DQ8 VMA_DQ9 VMA_DQ10 VMA_DQ11 VMA_DQ12 VMA_DQ13 VMA_DQ14 VMA_DQ15 VMA_DQ16 VMA_DQ17 VMA_DQ18 VMA_DQ19 VMA_DQ20 VMA_DQ21 VMA_DQ22 VMA_DQ23 VMA_DQ24 VMA_DQ25 VMA_DQ26 VMA_DQ27 VMA_DQ28 VMA_DQ29 VMA_DQ30 VMA_DQ31 VMA_DQ32 VMA_DQ33 VMA_DQ34 VMA_DQ35 VMA_DQ36 VMA_DQ37 VMA_DQ38 VMA_DQ39 VMA_DQ40 VMA_DQ41 VMA_DQ42 VMA_DQ43 VMA_DQ44 VMA_DQ45 VMA_DQ46 VMA_DQ47 VMA_DQ48 VMA_DQ49 VMA_DQ50 VMA_DQ51 VMA_DQ52 VMA_DQ53 VMA_DQ54 VMA_DQ55 VMA_DQ56 VMA_DQ57 VMA_DQ58 VMA_DQ59 VMA_DQ60 VMA_DQ61 VMA_DQ62 VMA_DQ63
FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7
VMA_DM0 VMA_DM1 VMA_DM2 VMA_DM3 VMA_DM4 VMA_DM5 VMA_DM6 VMA_DM7
VMA_DM[7:0] [23,24]
FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7
VMA_WDQS0 VMA_WDQS1 VMA_WDQS2 VMA_WDQS3 VMA_WDQS4 VMA_WDQS5 VMA_WDQS6 VMA_WDQS7
VMA_WDQS[7:0] [23,24]
FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7
VMA_RDQS0 VMA_RDQS1 VMA_RDQS2 VMA_RDQS3 VMA_RDQS4 VMA_RDQS5 VMA_RDQS6 VMA_RDQS7
VMA_RDQS[7:0] [23,24]
VMA_DQ[63:0] VMA_DQ[63:0] [23,24]
FBVDDQ + FBVDD = 3.116A
+1.5V_GFX
U1001D
12/14 FBVDDQ
C1060 0.1U/16V_4
C1061 0.1U/16V_4
C1062 1U/6.3V_4
C1065 1U/6.3V_4
C1066 4.7U/6.3V_6
C1063 4.7U/6.3V_6
C1067 10U/6.3V_6
C1064 22U/6.3V_6
FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1018 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1019 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R1020 51.1/F_4
bga595-nvidia-n13p-gv2-s-a2 COMMON
U1001F
13/14 GND
GND
if stuff Da,Ra, do not stuff Ua,Ca,Rb,Rc
GC6_FB_EN
DGPU_VC_EN
D1004 *BAT54CW-7-F
Da
R1123 *100K/F_4
Ra
DGPU_FB_EN
For support GC6 2.0
+3V
Ua
U1003 NL17SZ32DFT2G
Ca
C1068 0.1U/16V_4
[12,46] DGPU_PWR_EN
[44,46] DGPU_VC_EN
[12,22] GC6_FB_EN
R1023 *0_4
R1024 0_4
Rc
Rb
R1025 100K/F_4
DGPU_FB_EN [45]
if stuff stuff Ua, not stuff PD26
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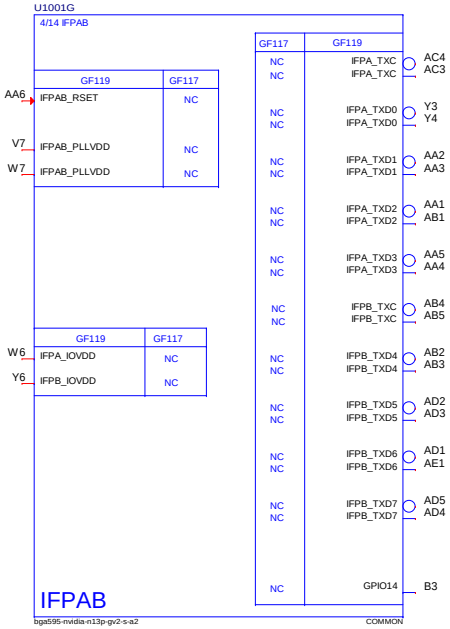

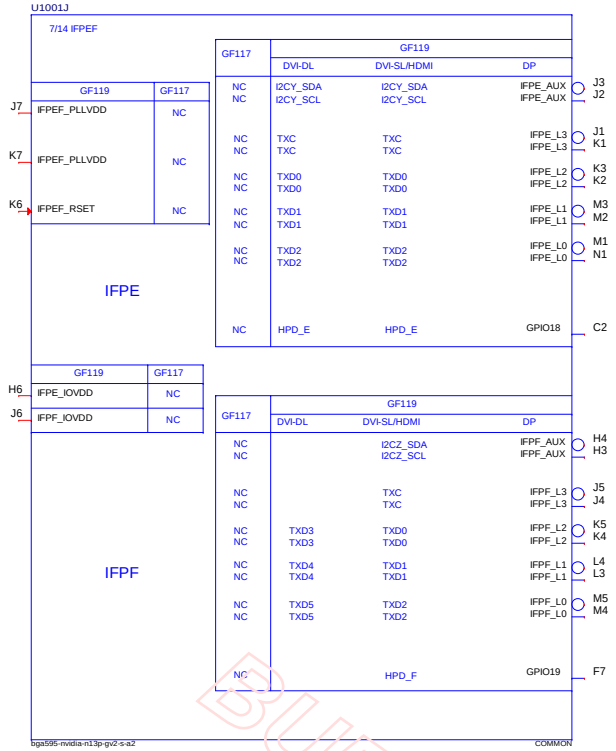

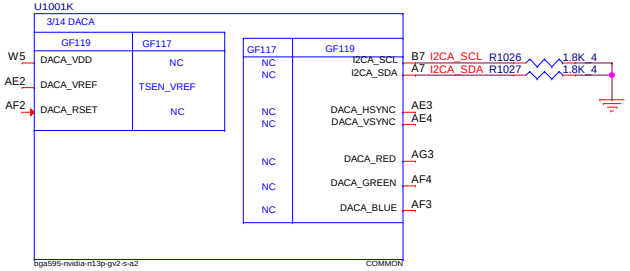

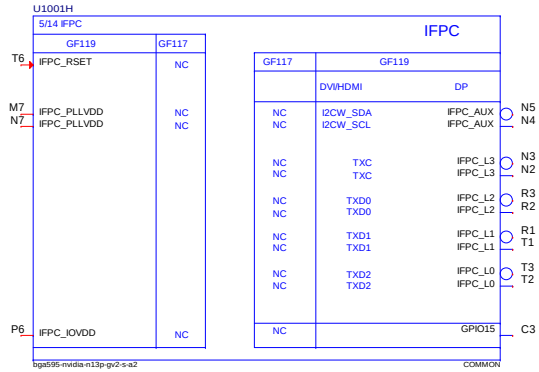

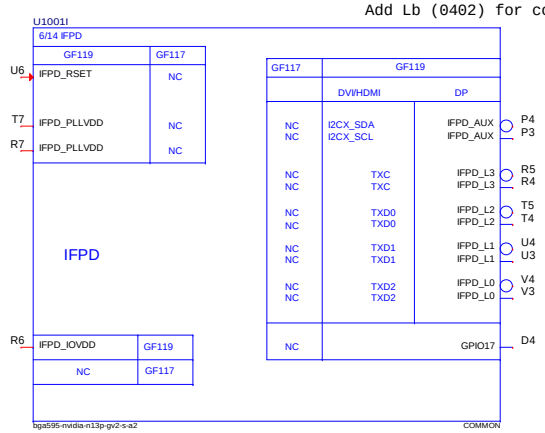

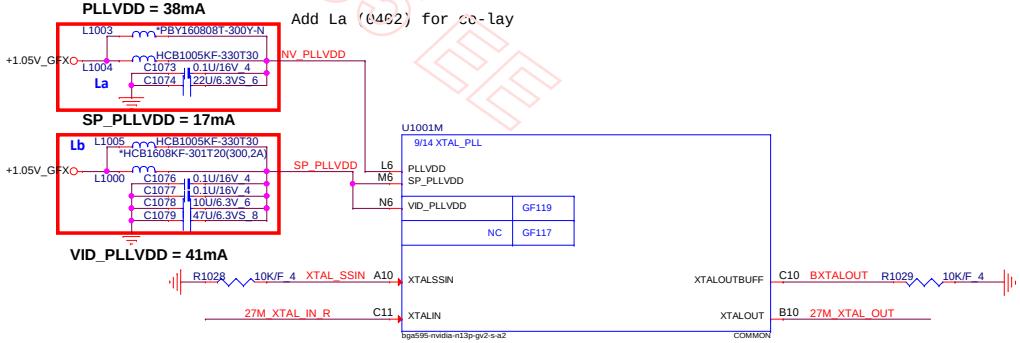

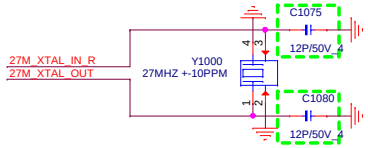

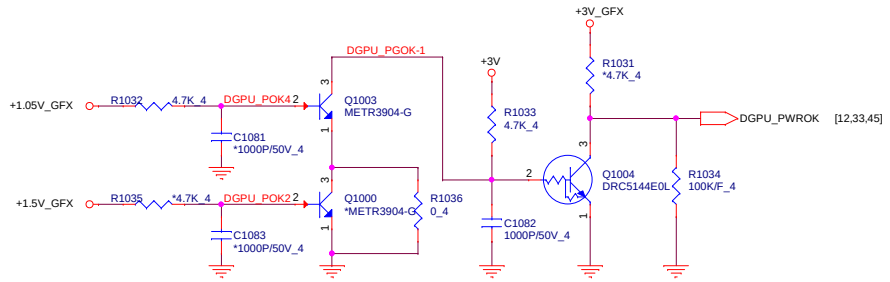

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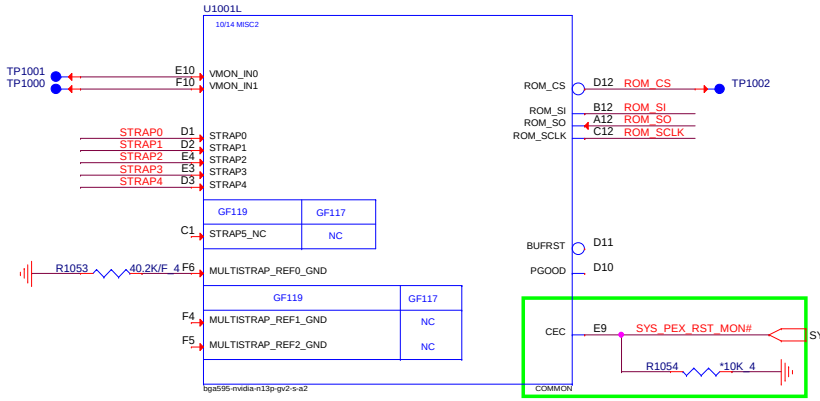
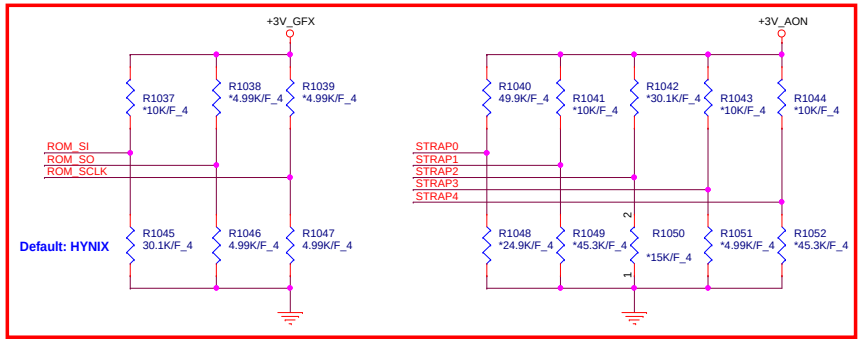
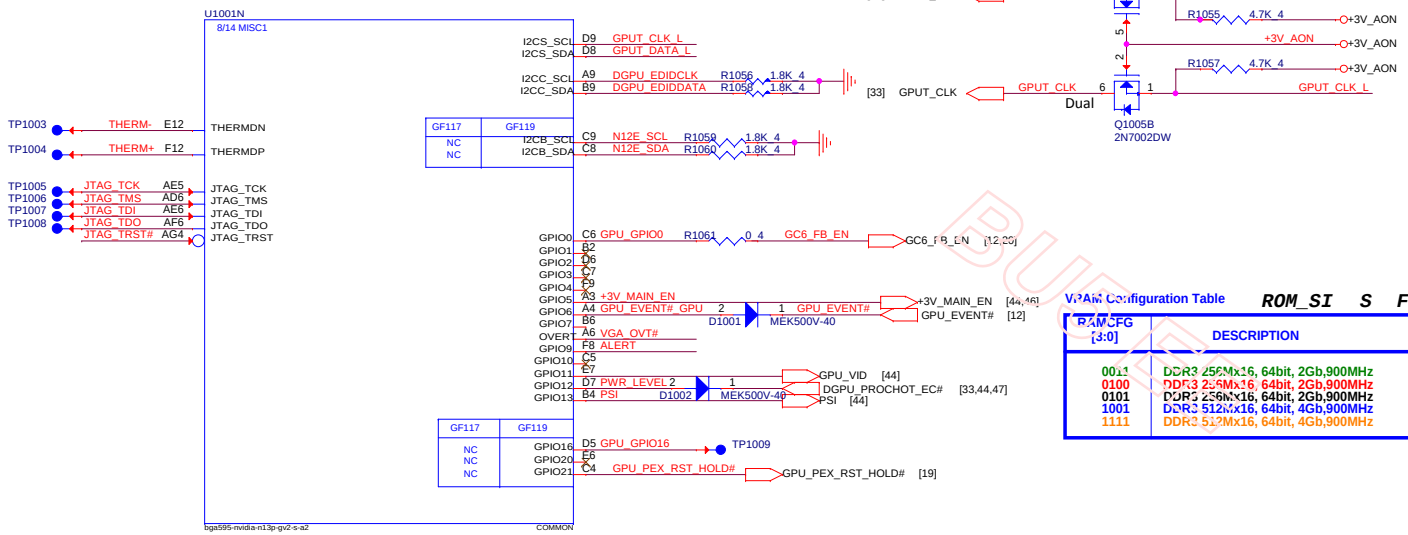
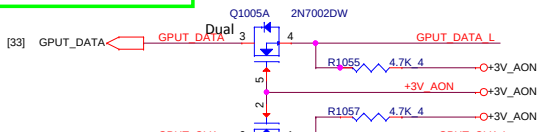




4.99k	CS24992FB26
10k	CS31002FB26
15k	CS31502FB24
20k	CS32002FB29
24.9k	CS32492FB16
30.1k	CS33012FB18
34.8k	CS33482FB06
45.3k	CS34532FB18





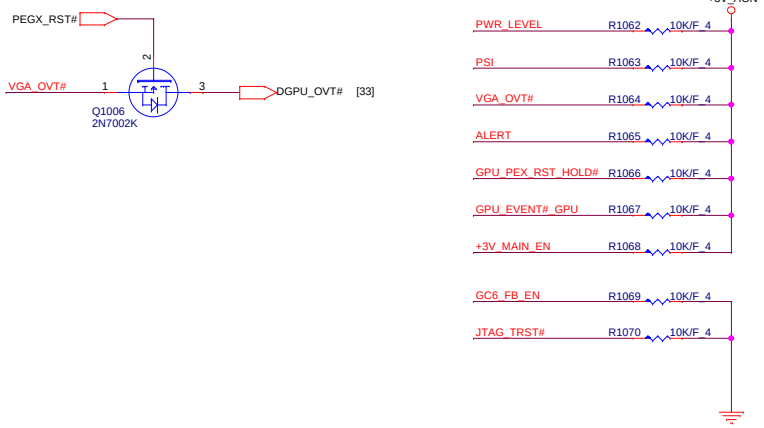


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table

ROM_SI S F

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Straping	*TOP B/S*	QBC
0011	DDR3 256Mx16, 64bit, 2Gb,900MHz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 256Mx16, 64bit, 2Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501
0101	DDR3 256Mx16, 64bit, 2Gb,900MHz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
1001	DDR3 512Mx16, 64bit, 4Gb,900MHz	Micron	MT41K512M16HA-107G:A	0x9	AKD5QGSTL05	AKD5QGSTL09
1111	DDR3 512Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC8G63CMR-11C	0xF	AKD5QFDTW00	AKD5QFDTW01

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

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Rank0

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16LY-091G:N QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

stuff R1124 for
Hynix 8Gb DDP VRAM

stuff R1125 for
Hynix 8Gb DDP VRAM

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN_FBA0_ODT1	J1	NC/ODT1
SNN_FBA0_CKE1	J9	NC/CKE1
SNN_FBA0_CS1	L1	NC/CS1
SNN_FBA0_ZQ1	L9	NC/ZQ1

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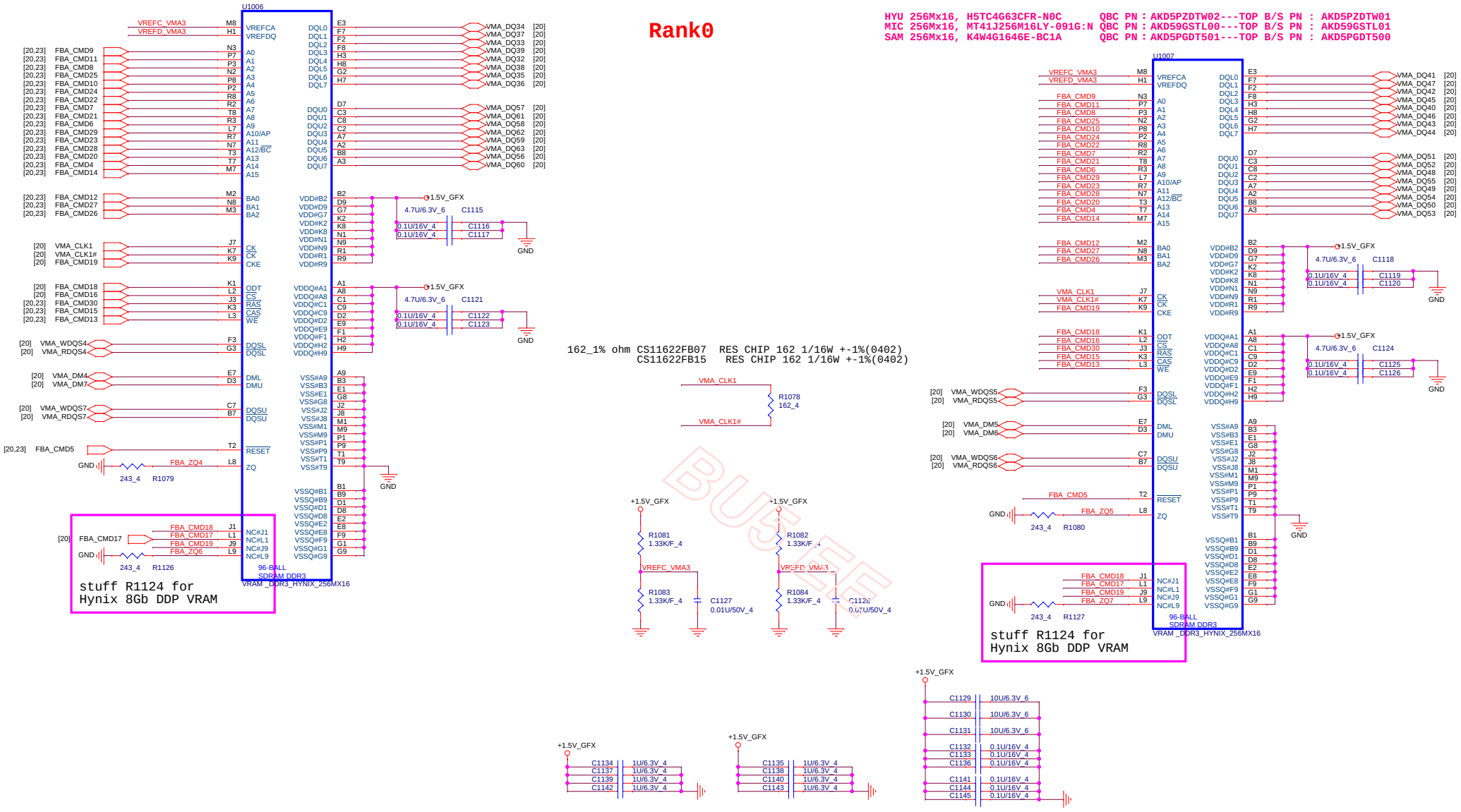
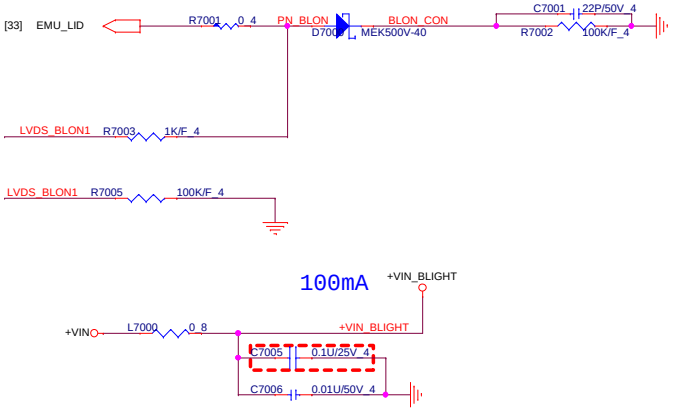
Rank0

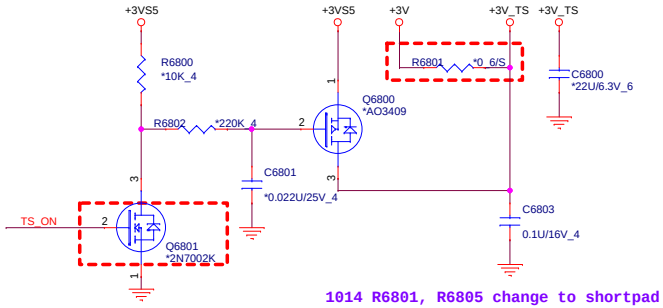
HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16LY-091G:N QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



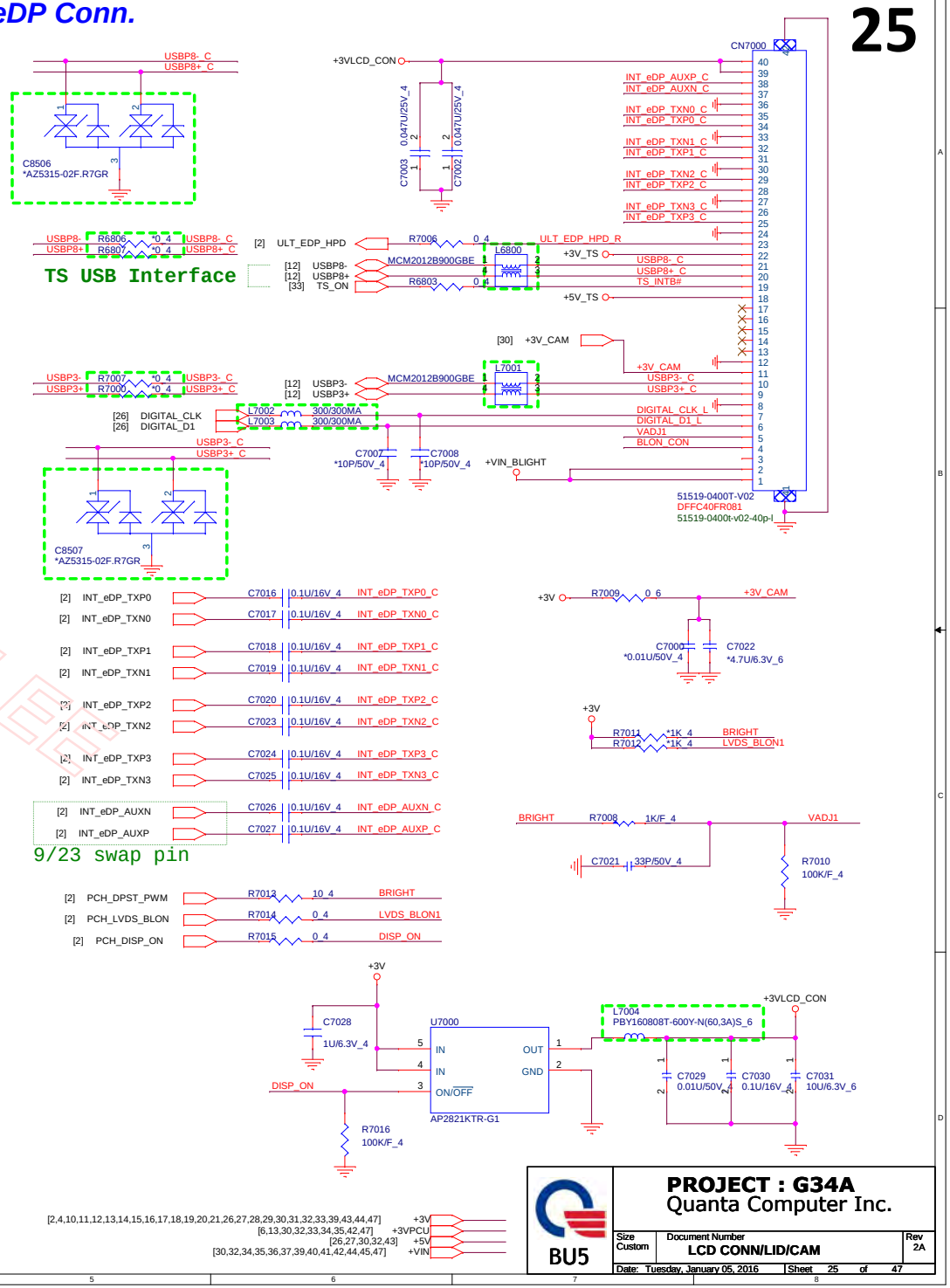
LID Switch



Touch screen



eDP Conn.



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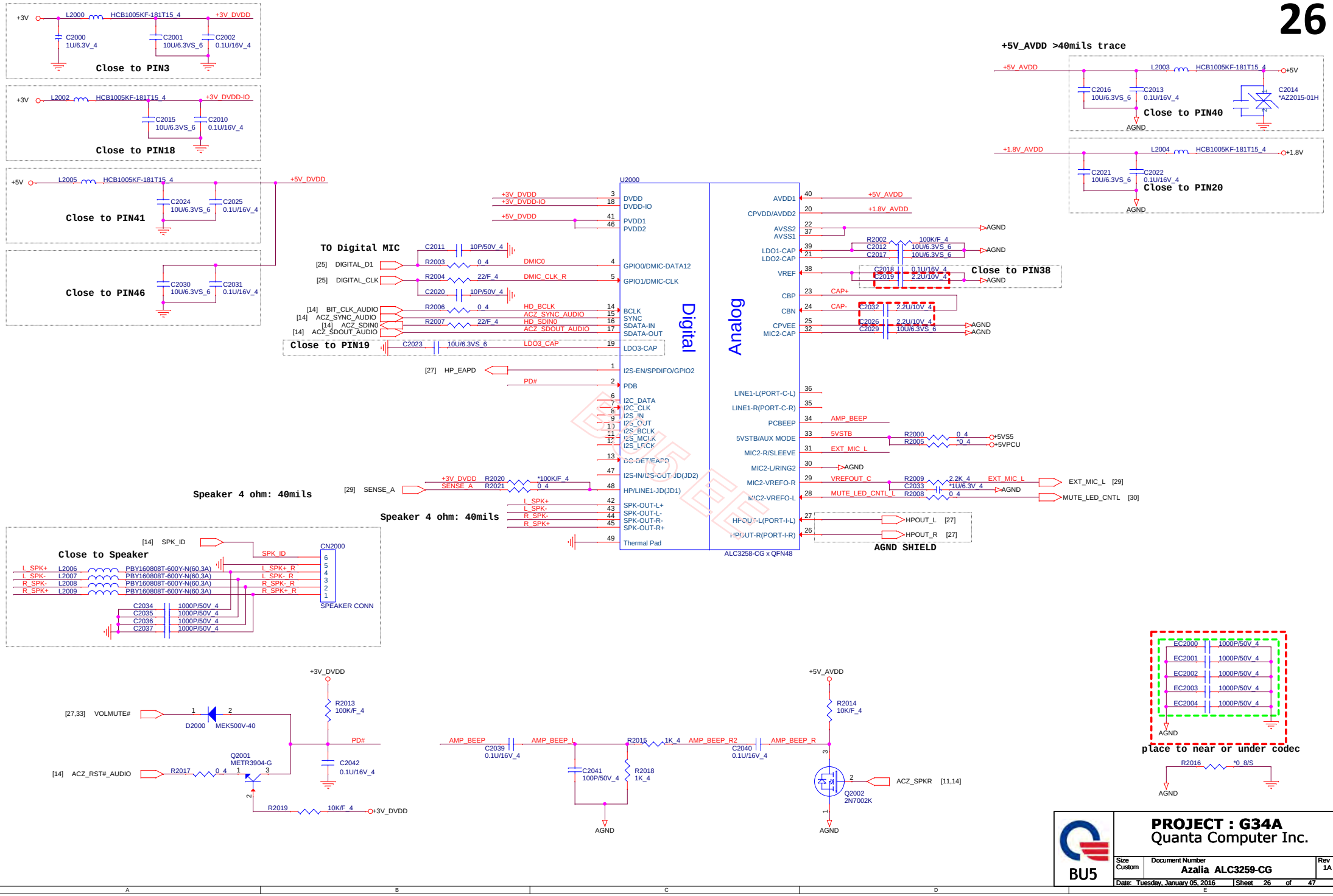
+5V_AVDD >40mils trace
Close to PIN3
Close to PIN18
Close to PIN41
Close to PIN46
Close to PIN40
Close to PIN20
Close to PIN38
Close to PIN19
TO Digital MIC
Speaker 4 ohm: 40mils
Speaker 4 ohm: 40mils
Close to Speaker
AGND SHIELD
place to near or under codec
U2000
Digital
Analog
ALC3258-CG x QFN48
SPEAKER CONN
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Azalia ALC3259-CG
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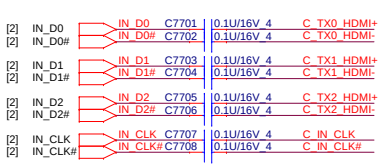
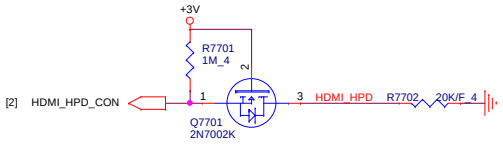
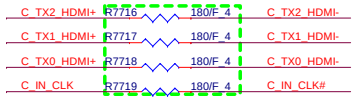
HDMI CONN

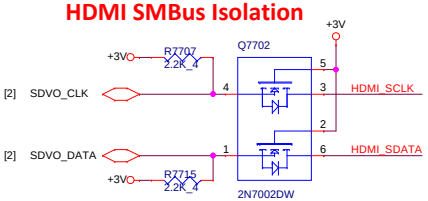




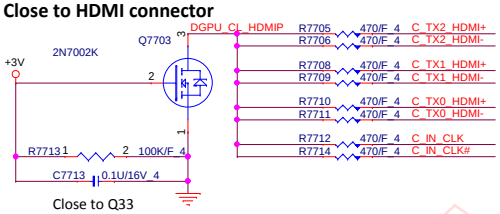
EMI Solution

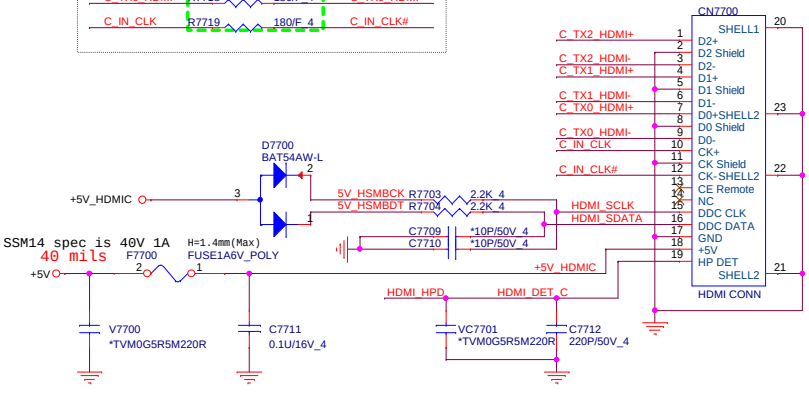


HDMI SMBus Isolation

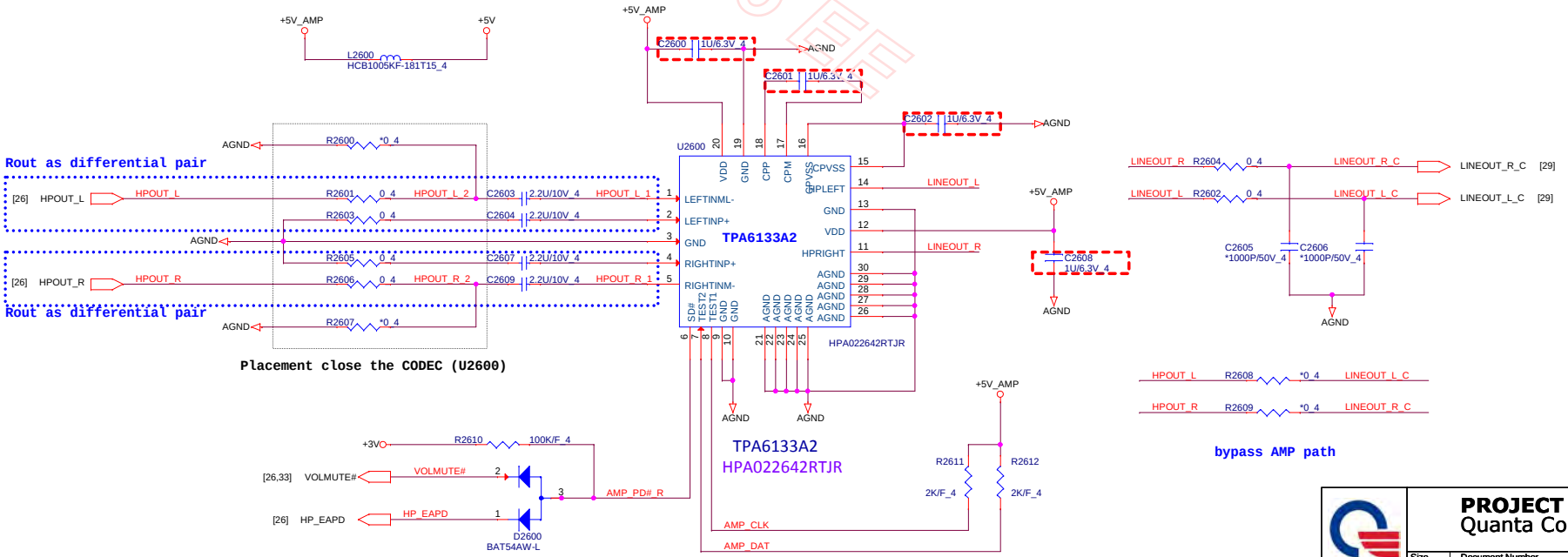


Close to HDMI connector





Head Phone out



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LAN & RJ45

For SWR mode support RTL8111HSH/RTL8107ESH
Stuff La, Ca ,Cb
For LDO mode support RTL8166EH
NA : La, Ca, Cb

* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30
* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)
* Place Cq,Cr for RTL8166EH close to each VDD10 pin-- 30(reserved)
* Place Ce,Cd for RTL8166EH close to each VDD10 pin-- 8 , 30

Power trace Layout 寬度> 60mil
>60mil >60mil

+1.05V_LAN_REGOUT L3000 4.7UH,+-20%,650MA_1210 La
Ca C3004 0.1U/16V_4
Cb C3005 4.7U/6.3VS_4
Cc PIN3 C3006 0.1U/16V_4
Cd PIN8 C3007 *0.1U/16V_4
Ce PIN30 C3008 *0.1U/16V_4
Cf PIN22 C3009 0.1U/16V_4
Cg PIN22 C3010 1U/6.3V_4
Ch PIN22 C3011 0.1U/16V_4
Cq PIN30 C3023 *1U/6.3V_4
Cr PIN30 C3024 *0.1U/16V_4

LAN_XTAL1 R3000 10_4 XTAL1
Y3000 25MHZ +-10PPM
XTAL2
C3000 10P/50V_4
C3001 10P/50V_4
R3001 2.49K/F_4

LAN_AMBLED# TP3000
LAN_LED1 TP3001
LED2 TP3002

+1.05V_LAN
+3V_LAN
LAN_AMBLED# Ra R3003 *0_4 LAN_WLED#
R3004 0_4 LAN_WLED# Rb

+3V R3002 1K_4 ISOLATEB R3005 15K/F_4
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

For GbE
* Place Ra
For 10/100
* Place Rb

U3000
Please add 9 GND VIAs connection with thermal PAD
GND
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2-
MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10
RTL8107ESH-CG
AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED0 LED1/GPO LED2(LED1)
REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP
MDIP3(NC) MDIN3(NC) AVDD33(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N
RTL8107ESH-CG

+1.05V_LAN_REGOUT
+3V_LAN
+1.05V_LAN
PCIE_WAKE# R R3006 0_4 PCIE_WAKE# [4,29,32,33]
ISOLATEB
PLTRST# [4,16,19,29,31,32,33]
PCIE_RXN10_LAN_L C3002 0.1U/16V_4 PCIE_RXN10_LAN [12]
PCIE_RXP10_LAN_L C3003 0.1U/16V_4 PCIE_RXP10_LAN [12]

For GbE
* Place RTL8111HSH-CG
For 10/100
* Place RTL8107ESH-CG/RTL8166EH-CG

MDI3+ MDI3-
+3V_LAN
[13] PCIE_CLKREQ_LAN#
CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN10_LAN PCIE_TXP10_LAN
CLK_PCIE_LANN [13]
CLK_PCIE_LANP [13]
PCIE_TXN10_LAN [12]
PCIE_TXP10_LAN [12]

+3VLANVCC R3017 360_4 LED3000 3P ORANGE LED VC3000 *AVLC5S_4 LAN_AMBLED#
+3VLANVCC R3018 360_4 LED3001 3P WHITE LED VC3001 *AVLC5S_4 LAN_WLED#
C3026 *0.1U/16V_4

For 10/100 stuff only Close RJ45
MDI3-_1 R3007 0_4
MDI3+_1 R3008 0_4
MDI2-_1 R3009 0_4
MDI2+_1 R3010 0_4
C3012 68P/50V_4

* Place Ci and Ck, close to each VDD33 pin-- 23, 32 for RTL8166EH
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

+3VLANVCC +3V_LAN
Ci PIN23 C3025 *0.1U/16V_4
Cj PIN11 C3013 0.1U/16V_4
Ck PIN32 C3014 0.1U/16V_4
Cm PIN11 C3015 *4.7U/6.3VS_4
Cn PIN32 C3016 *4.7U/6.3VS_4

Co PIN23 C3017 4.7U/6.3VS_4
Cp PIN23 C3018 0.1U/16V_4
For SWR mode support RTL8111HSH/RTL8107ESH
Stuff Co, Cp

For 10/100：Ua
For Giga：Ub

Ua U3001
MDI1- 1 MDI1+ 3 LAN_MCTG1 2 MDI0- 6 MDI0+ 8 LAN_MCTG0 7
TD+ TD- CT RD+ RD- CT GND
TX+ CMT TX- RX- CT RX+
16 MDI1- 15 TRA_V_DAC 14 MDI1+ 9 MDI0+ 10 TRA_V_DAC 11 MDI0-
17
NS681684
DB0LE6LAN20
C3022 0.01U/50V_4

1st source：NS681684 DB0LE6LAN20
2nd source：N-3110M DB0Y11LAN00

Ub U3002
MDI0+ 2 MDI0- 3 MDI1+ 5 MDI1- 6 MDI2+ 8 MDI2- 9 MDI3+ 11 MDI3- 12
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-
23 MDI0+_1 22 MDI0-_1 20 MDI1+_1 19 MDI1-_1 17 MDI2+_1 16 MDI2-_1 14 MDI3+_1 13 MDI3-_1
TRA_V_DAC 1 TRA_V_DAC 4 TRA_V_DAC 7 TRA_V_DAC 10 TRA_V_DAC 25
TCT1 TCT2 TCT3 TCT4 GND
MCT1 MCT2 MCT3 MCT4
24 LAN_MCTG0 Ra R3011 75/F_4
21 LAN_MCTG1 Rb R3012 75/F_4
18 LAN_MCTG2 Rc R3014 *75/F_4
15 LAN_MCTG3 Rd R3016 *75/F_4
*GST5009B
C3020 10P/3KV_1808

For GiGA
BOT:GST5009B LF,DB0Z06LAN00

For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd

RJ45
CN3000
MDI3-_1 MDI3+_1 MDI1-_1 MDI2-_1 MDI2+_1 MDI1+_1 MDI0-_1 MDI0+_1
RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+
GND2 GND1
R3013 0_6
R3015 0_6
RJ45_CONN
DFTJ08FR475
rj45-2rj1755-000211f-8p

[2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,29,30,31,32,33,39,43,44,47] +3V
[43] +3VLANVCC

BU5
PROJECT : G34A
Quanta Computer Inc.
Size Custom | Document Number LAN RTL8107ESH-CG/RJ45 | Rev 1A
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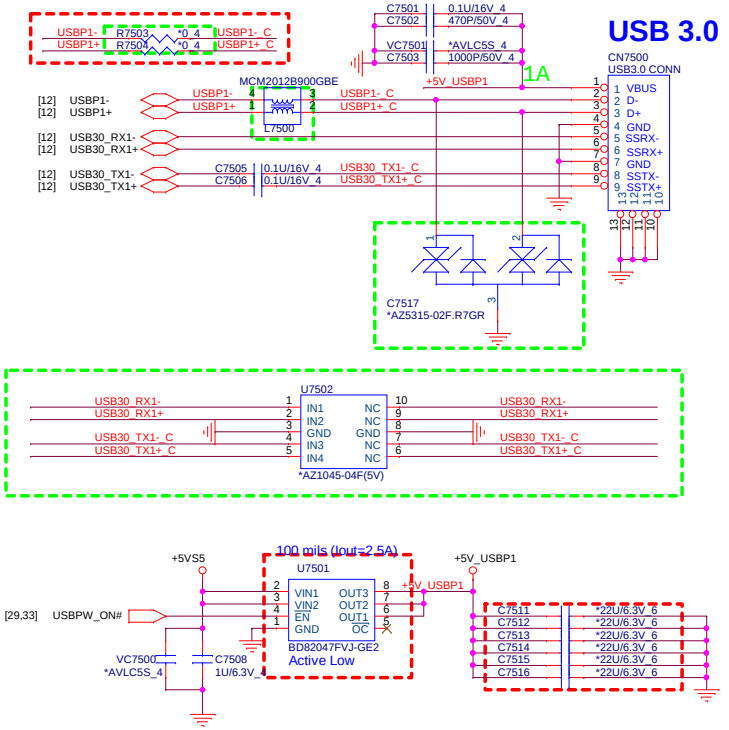
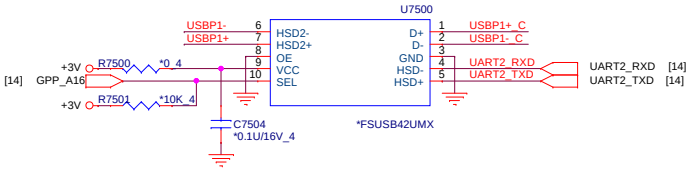
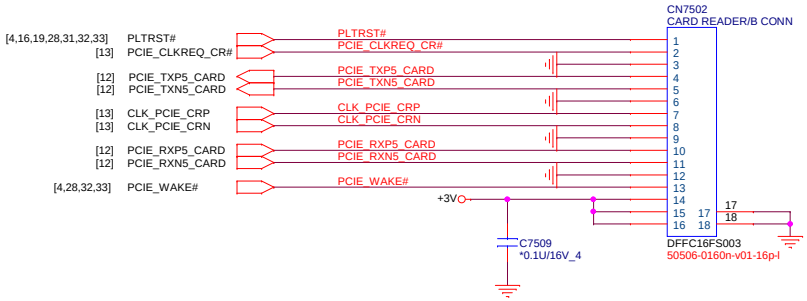
USB 2.0/3.0 Combo



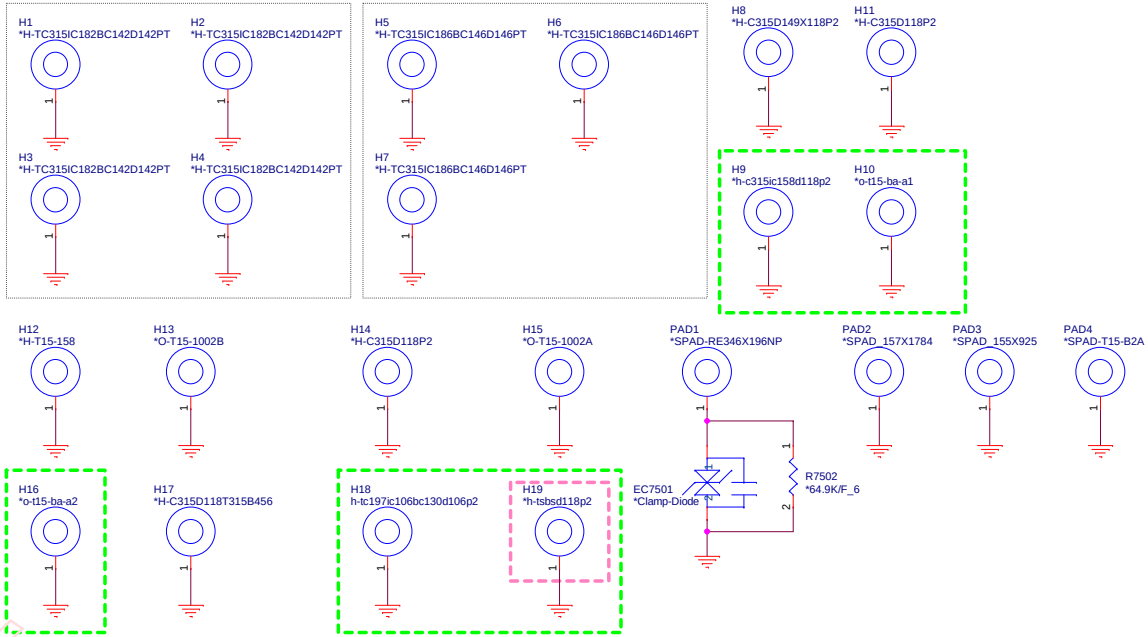
UART for DEBUG



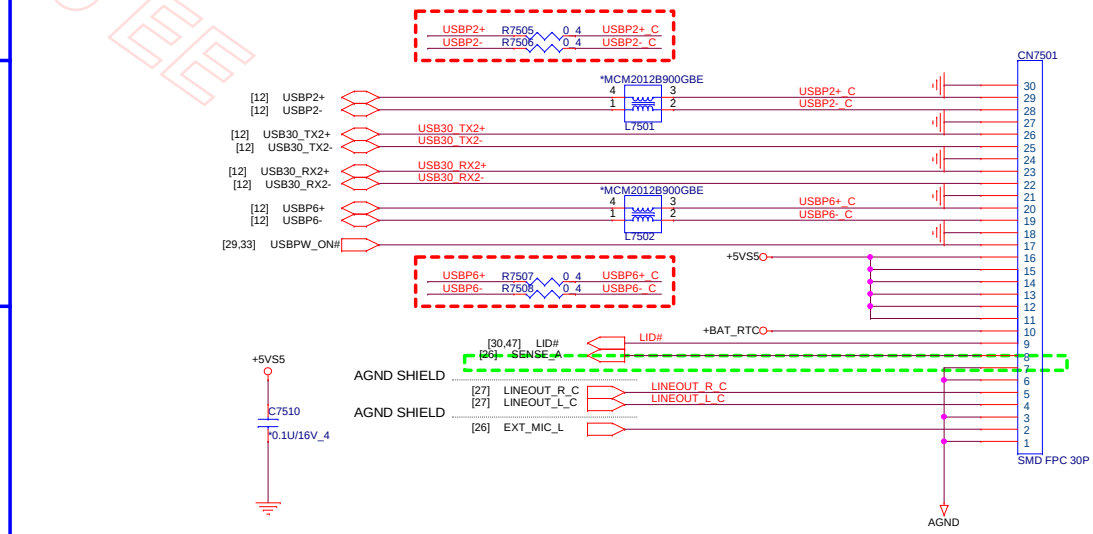
Card Reader Connector



Holes



USB/Phone Jack Connector



+3VPCU [6,13,30,32,33,34,35,42,47]
+5VS5 [4,25,26,35,36,37,38,39,40,41,43,44,45,46]
+BAT_RTC [4,13,15,30,34,47]
+3V [2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,30,31,32,33,39,43,44,47]

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Quanta Computer Inc.

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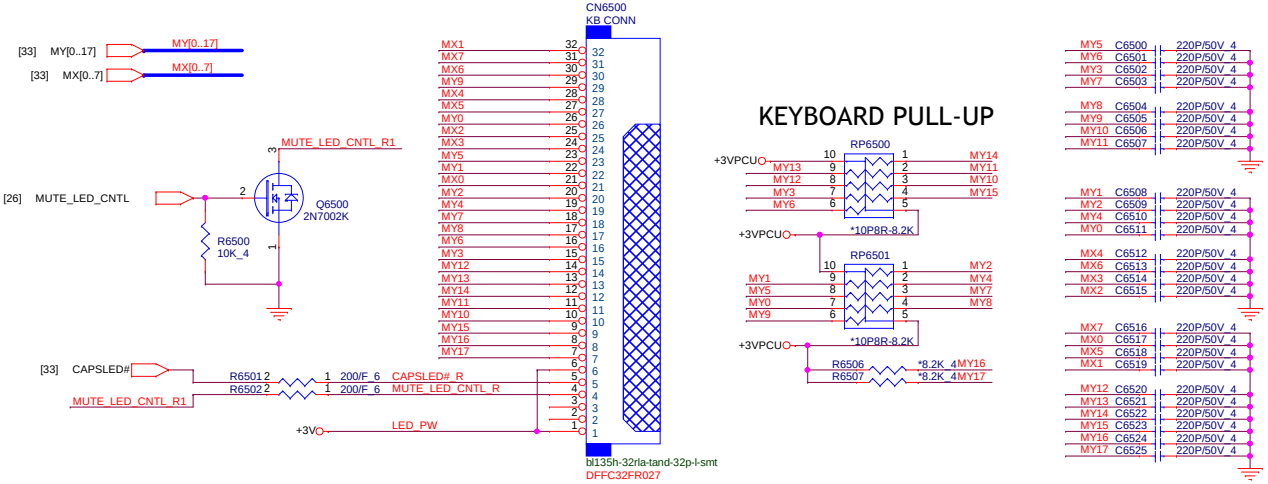
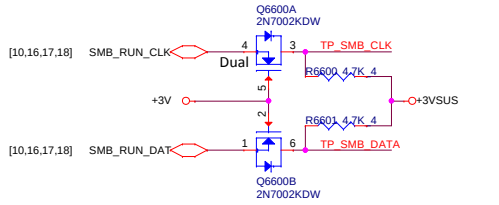
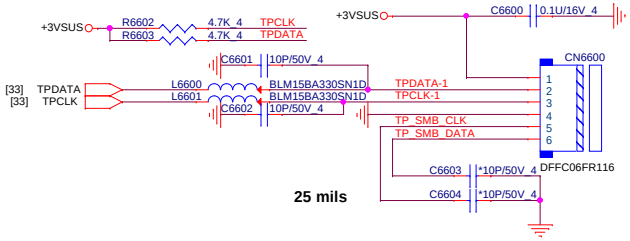
KEYBOARD Con.



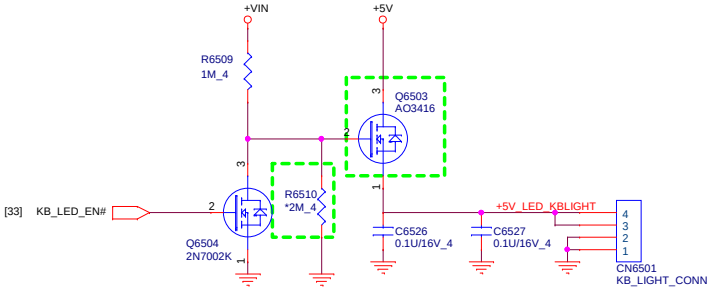
KEYBOARD PULL-UP

Touch Pad Connector

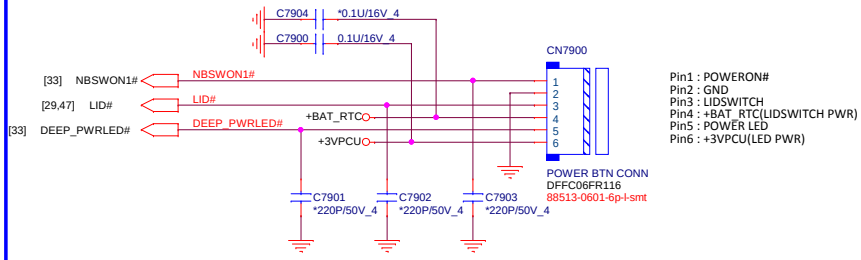




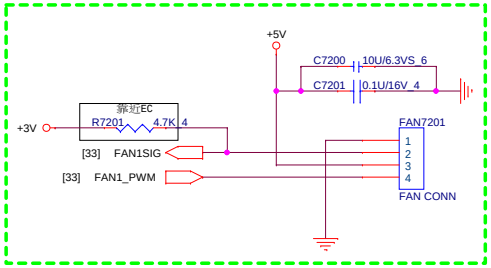
KB LIGHT CONN

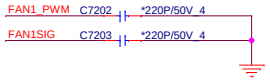


Power Botton Connector

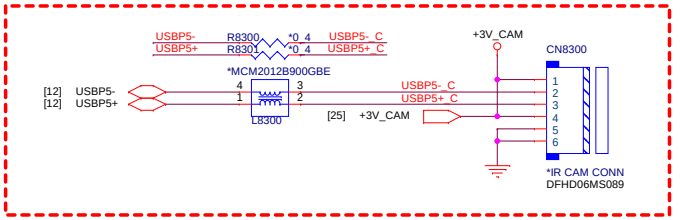


FAN CONN





IR CAM



1015 Add IR CAM circuit

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Quanta Computer Inc.

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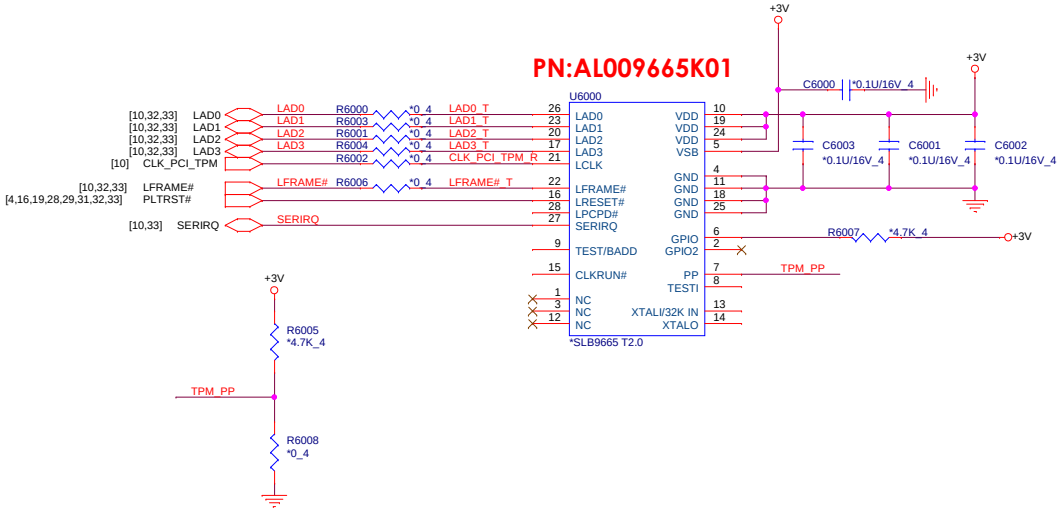
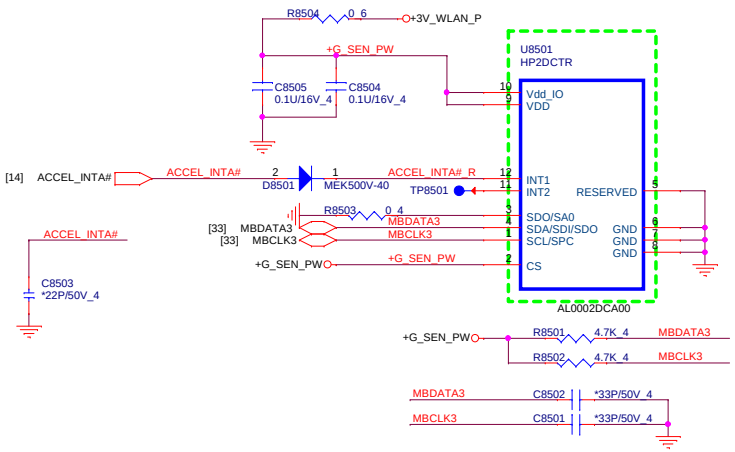
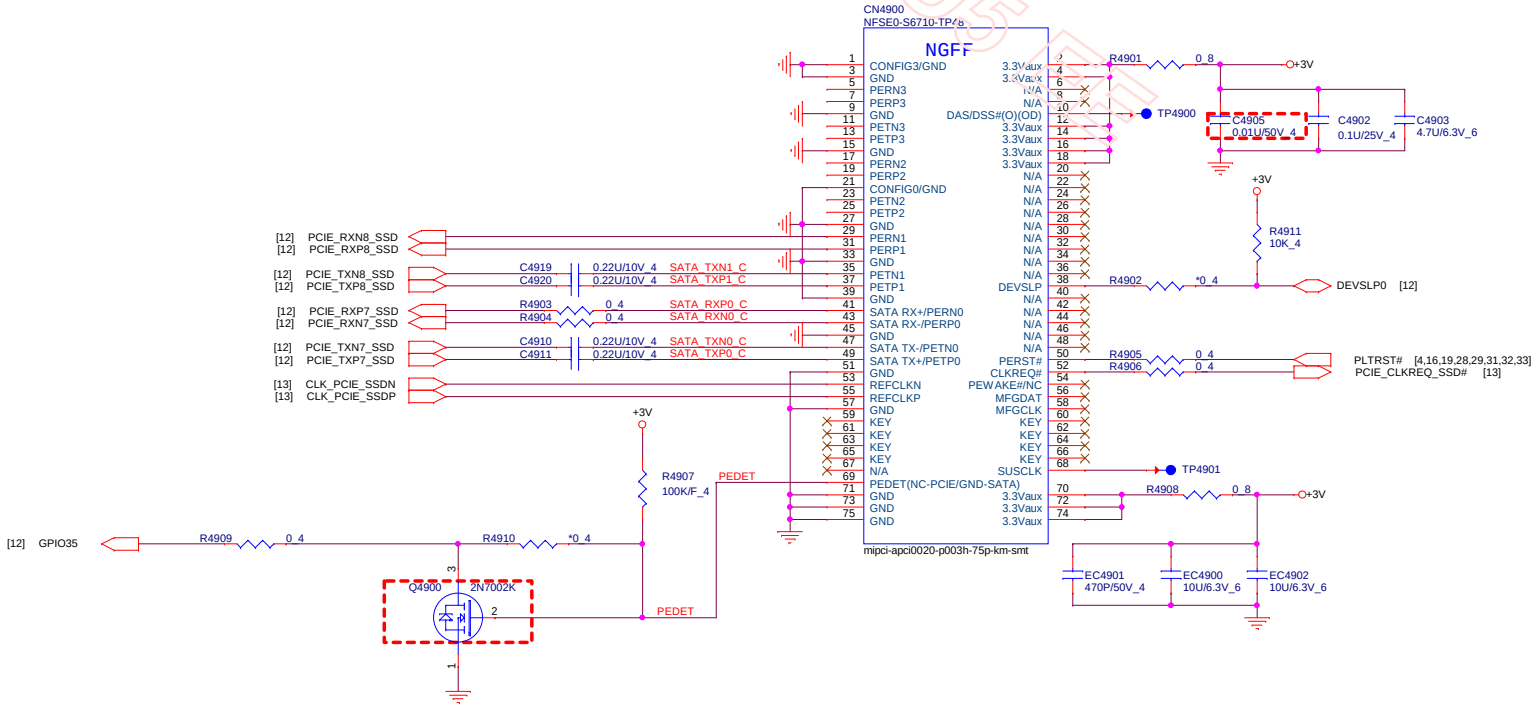
TPM (2.0)



Accelerometer Sensor



SSD



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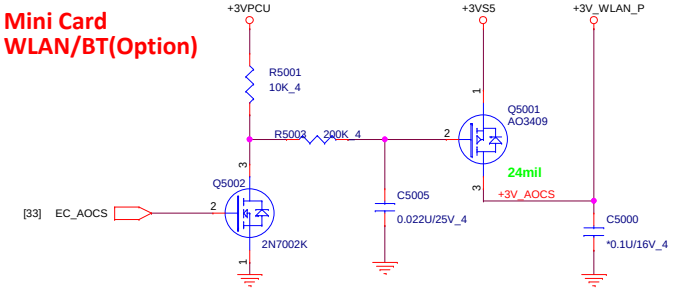
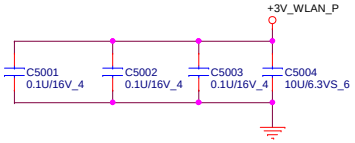
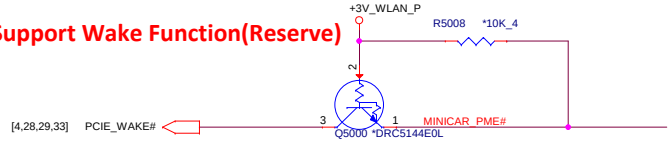
Mini Card WLAN/BT(Option)

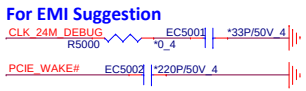


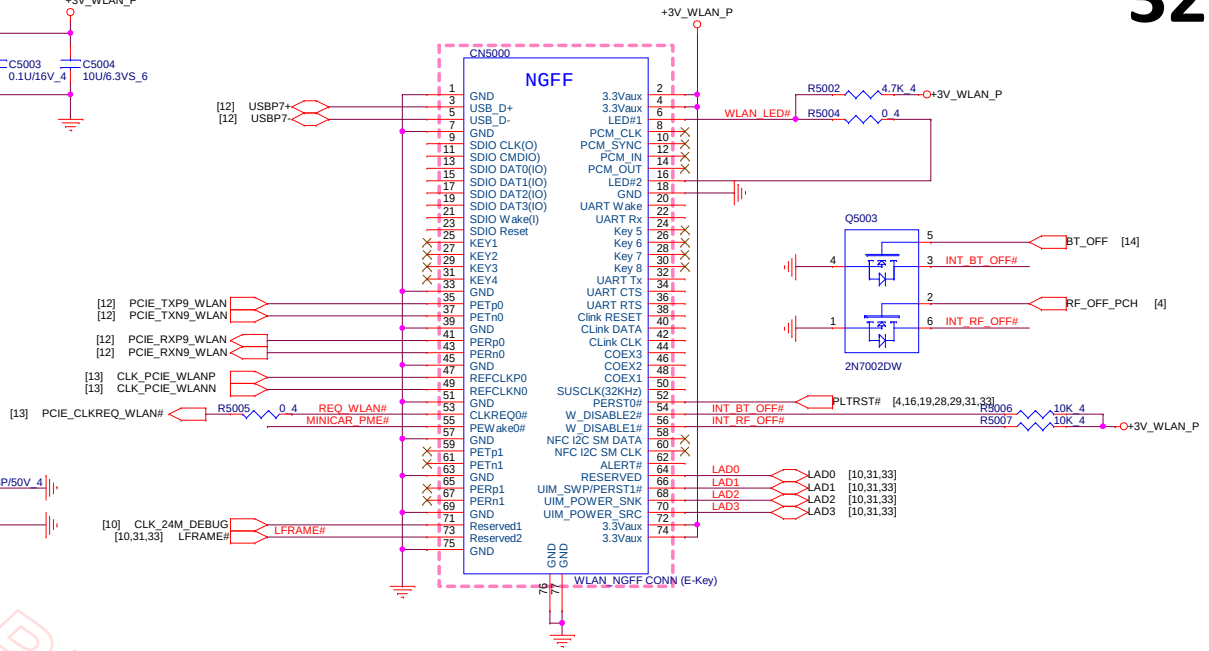


Support Wake Function(Reserve)

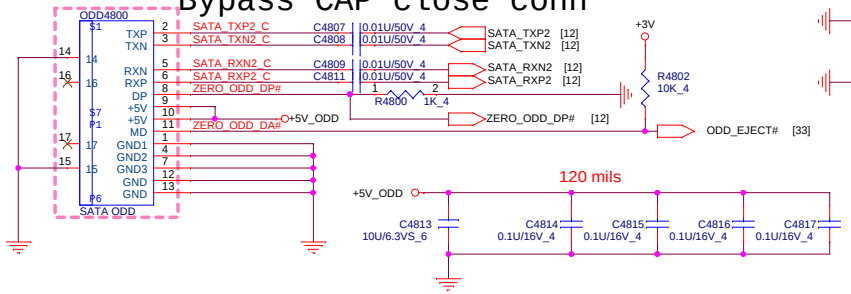


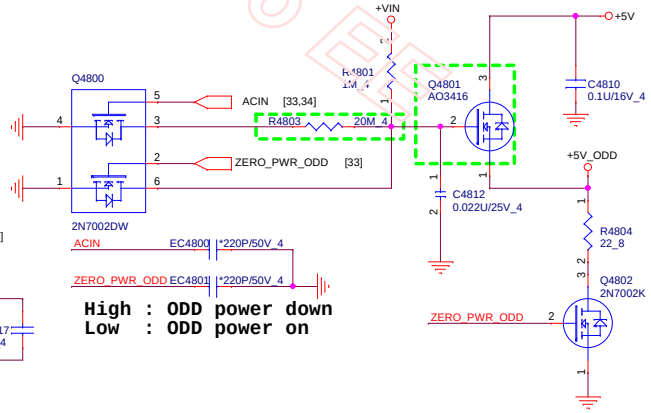
1020 del EC_PCIE_WAKE# circuit

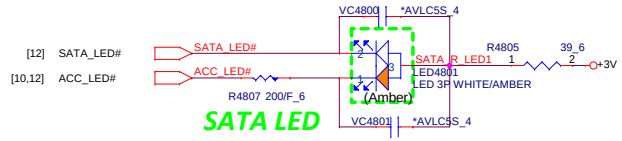




SATA ODD

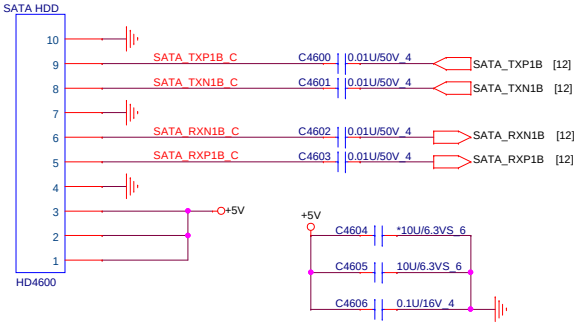






[2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,33,39,43,44,47] +3V
[25,26,27,30,43] +5V
[6,13,30,33,34,35,42,47] +3VPCU

HDD



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Quanta Computer Inc.

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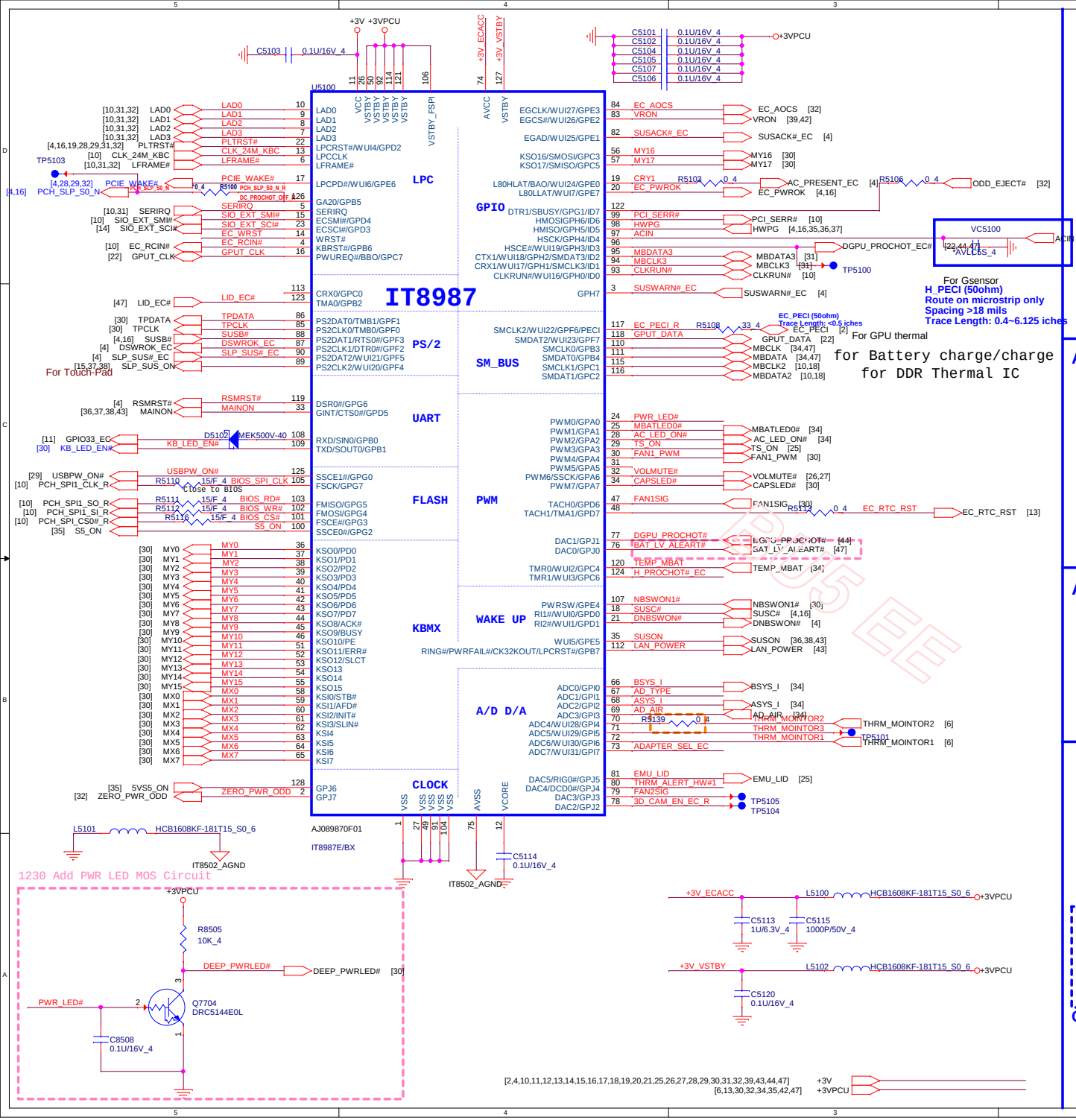
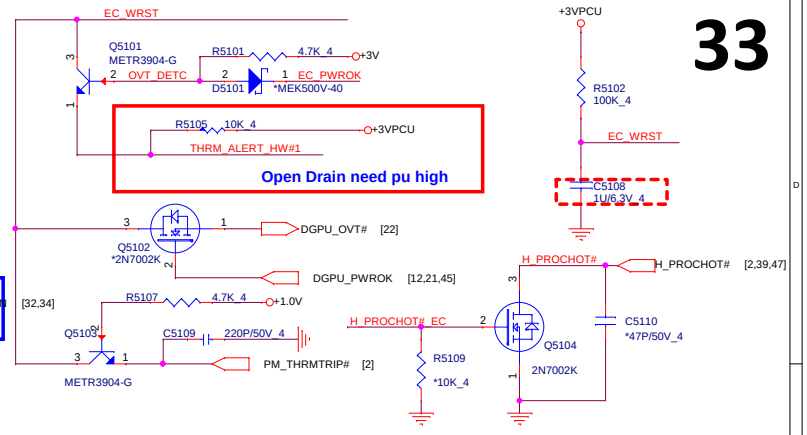
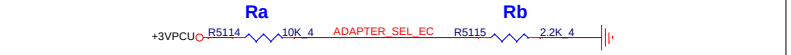


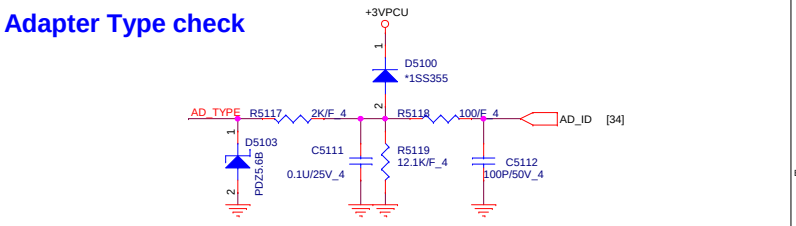


Adapter select for EC

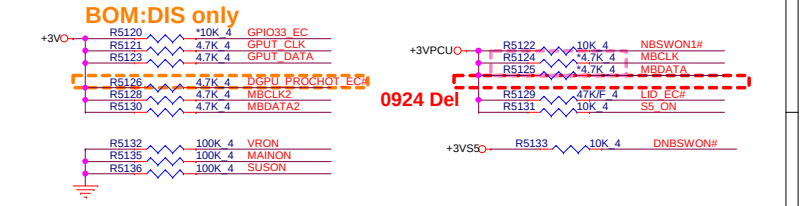


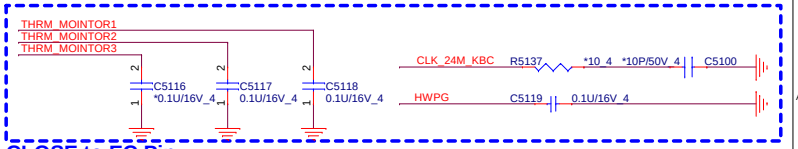
	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002JB28)	100K (CS41002FB28)	3V	
150W	10K(CS31002JB28)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002JB28)	12.1K(CS31212FB28)	1.8V	
90W	10K(CS31002JB28)	6.2K(CS26202FB17)	1.26V	
65W	10K(CS31002JB28)	2.2K(CS22202JB18)	0.59V	DIS
45W	NC	10K(CS31002JB28)	0V	UMA

Adapter Type check



BOM:DIS only





CLOSE to EC Pin

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Quanta Computer Inc.

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Custom	35 -- WLAN/G-Sensor/G-CLK/TS	1A
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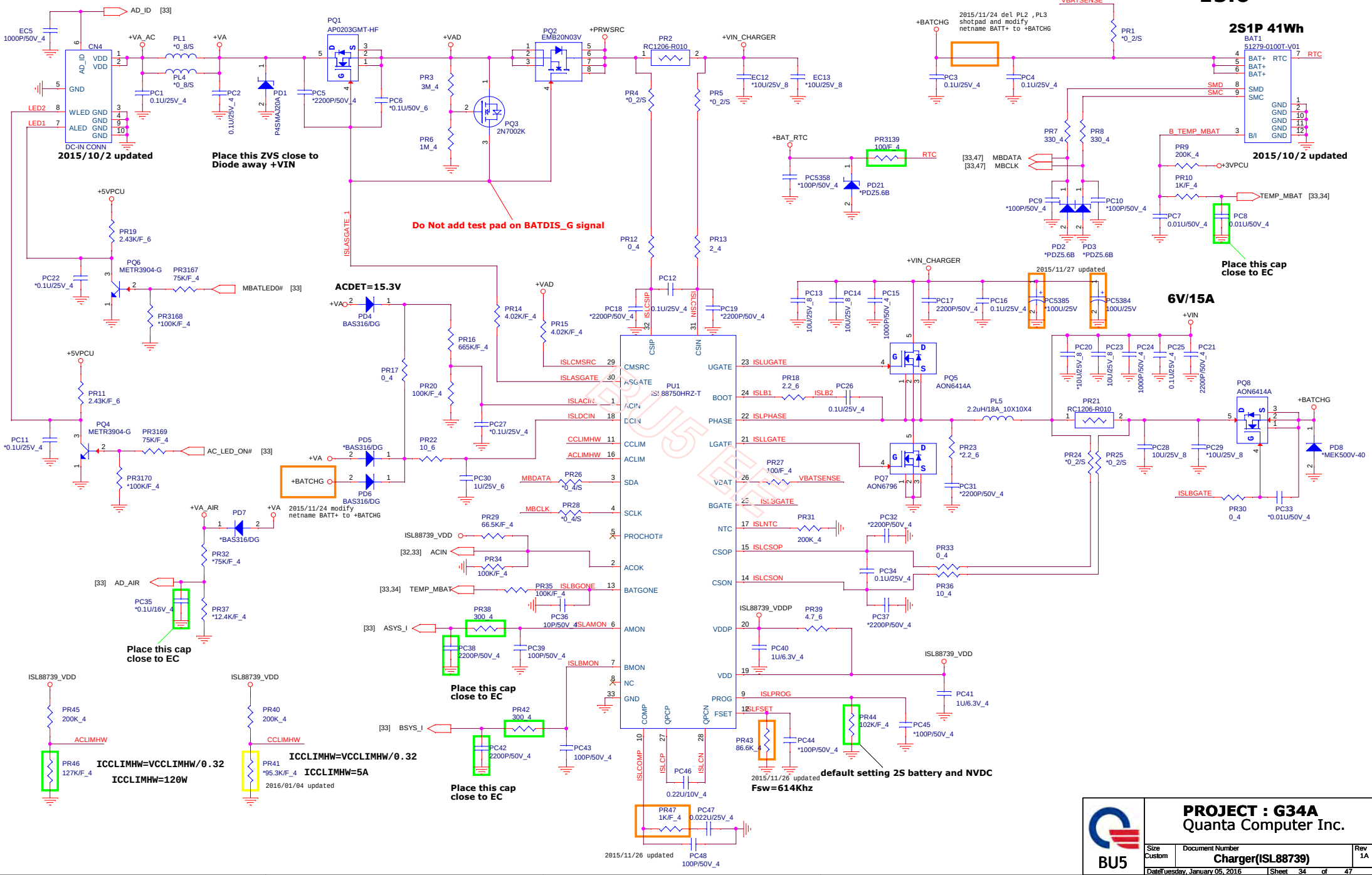
15.6"

DC_JACK 65W

2S1P 41Wh

6V/15A



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Quanta Computer Inc.	
Size: Custom	Document Number: Charger(ISL88739)
Rev: 1A	
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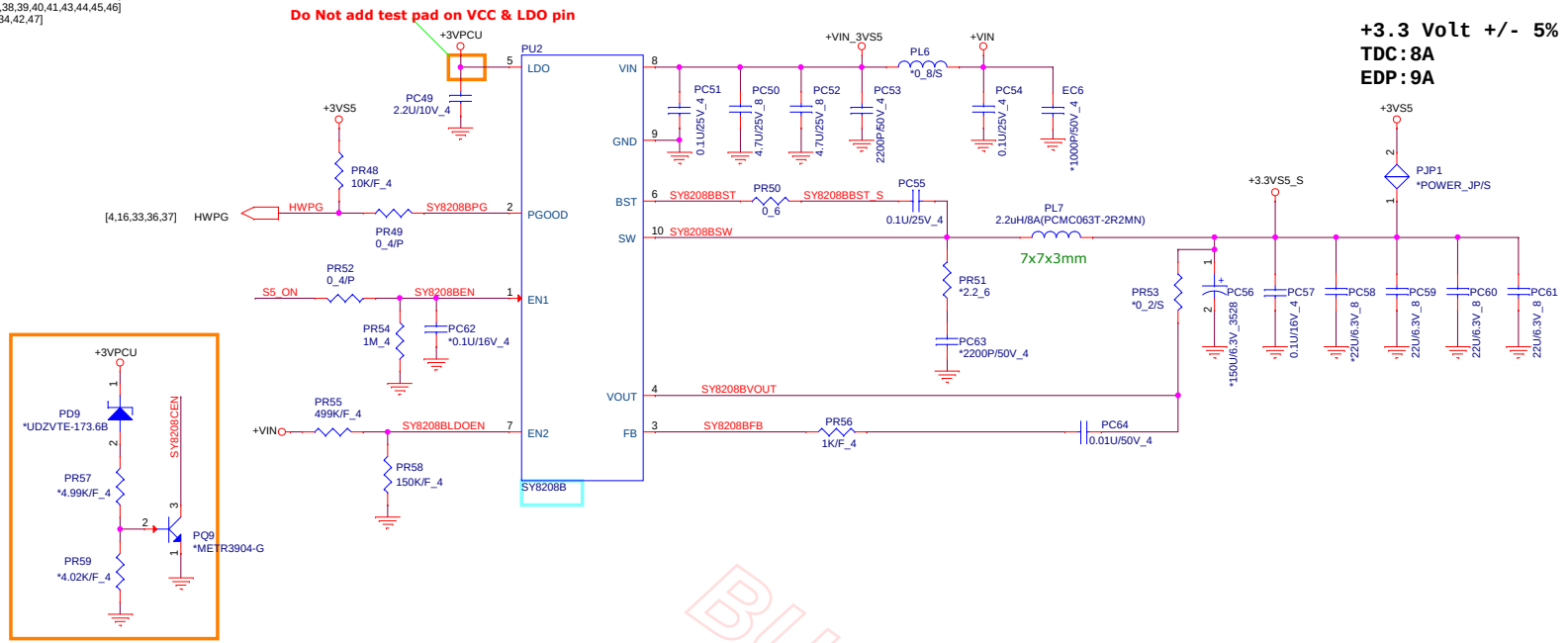
DC/DC +3VS5/+5VS5

+VIN [25,30,32,34,36,37,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,36,37,38,42,43,46,47]
+5VS5 [4,25,26,29,36,37,38,39,40,41,43,44,45,46]
+3VPCU [6,13,30,32,33,34,42,47]
+5VPCU [26,34,43,46]

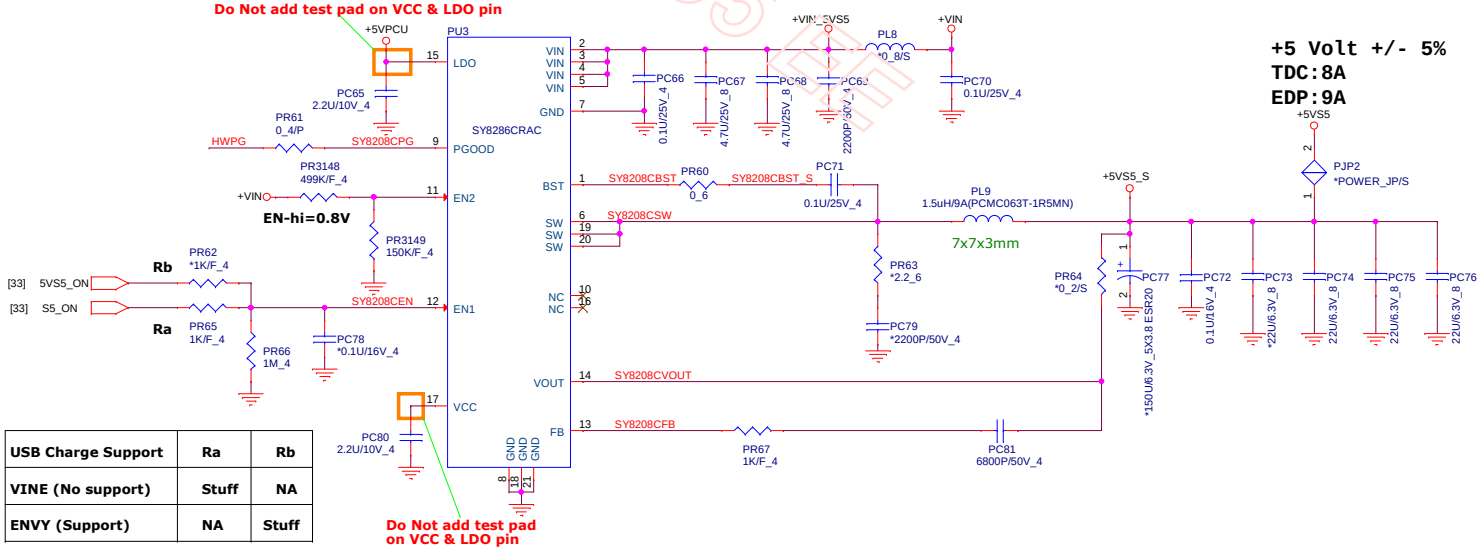
Do Not add test pad on VCC & LDO pin



+3.3 Volt +/- 5%
TDC:8A
EDP:9A

2014/12/12 updated

Do Not add test pad on VCC & LDO pin



+5 Volt +/- 5%
TDC:8A
EDP:9A

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

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Custom	3/5VPCU(RT8243A)	1A
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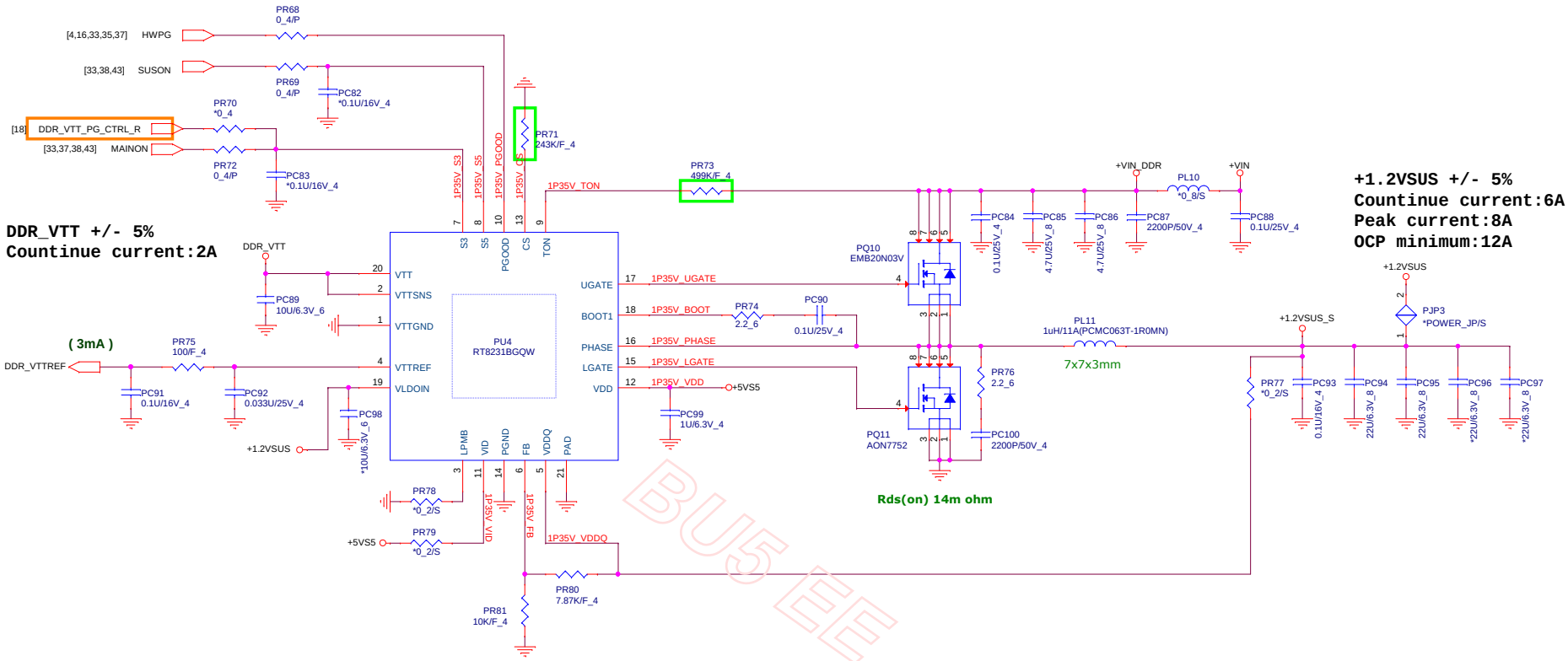
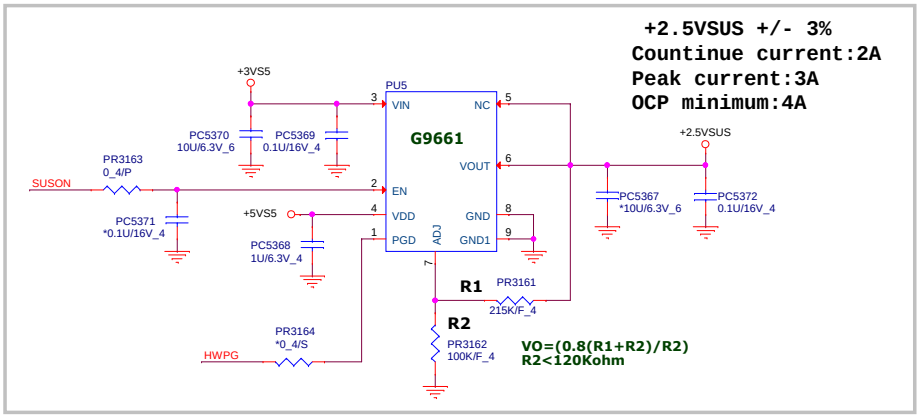
+VIN [25,30,32,34,35,37,39,40,41,42,44,45,47]
+5VS5 [4,25,26,29,35,37,38,39,40,41,43,44,45,46]
+1.2VSUS [3,6,17,18,38,46]
DDR_VTT [17,18]



20151015 updated



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Quanta Computer Inc.

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	DDR3 (RT8231B)/1.8VS5	1A

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+VIN [25,30,32,34,35,36,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,35,36,38,42,43,46,47]
+5VS5 [4,25,26,29,35,36,38,39,40,41,43,44,45,46]
+1.0V_DEEP_SUS [9,13,15,16,38]
+1.8V_DEEP_SUS [5,9,15,47]
+1.8V [26]

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Countinue current:6A
Peak current:9A

PU6 AOZ1236QI-03
2015/11/27 updated
2015/10/27 updated
7x7x3mm

20151015 updated
+1.8V_DEEP_SUS +/- 5%
Countinue current:1.0A
Peak current:3A

PU7 G9661
R1
R2
VO=(0.8(R1+R2)/R2)
R2<120Kohm

PQ46 EMB32N03K **0.05A**
PQ47 *2N7002K
PQ48 2N7002K
PQ49 METR3904-G
For 2S PACK

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Quanta Computer Inc.

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Custom	+1.1VS5 (RT8228)/2.5V	1A
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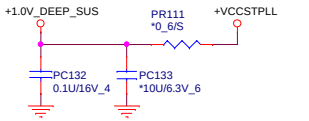
+1.0V [2,4,6,16,33]
+3VS5 [4,10,15,16,25,32,33,35,36,37,42,43,46,47]
+5VS5 [4,25,26,29,35,36,37,39,40,41,43,44,45,46]
+VCCIO [2,6,16]
+1.2VSUS [3,6,17,18,36,46]
+VCCSTPLL [2,4,5,6,9,39]
+1.0V_DEEP_SUS [9,13,15,16,37]
+1.2V_VCCPLL_OC [6]
MAINON [33,36,37,43]

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

Imax:0.24A

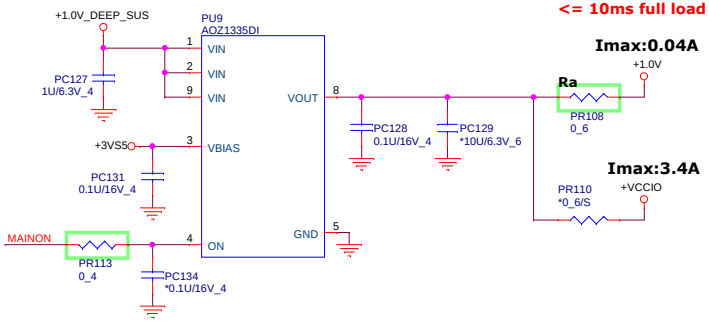


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

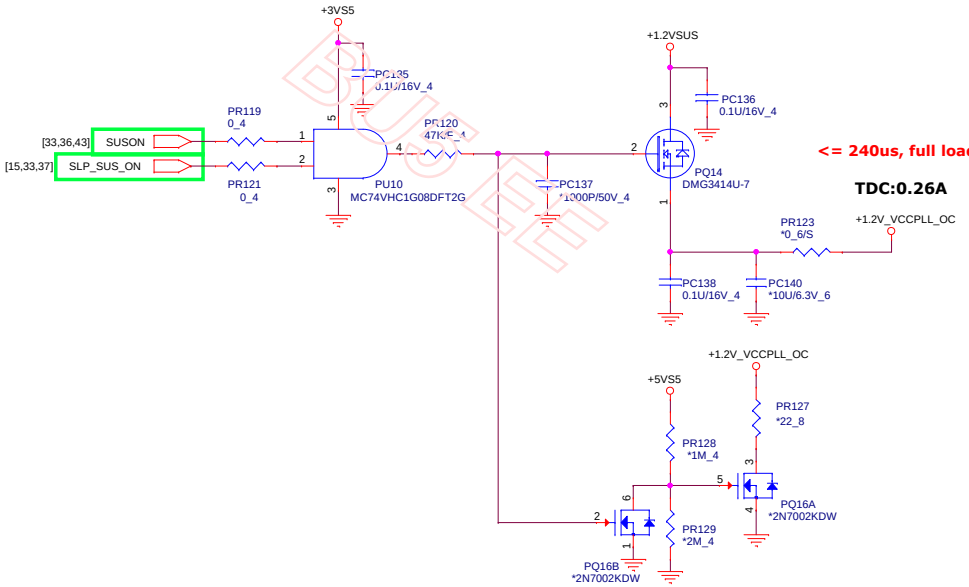
Imax:0.04A

Imax:3.4A



<= 240us, full load ready

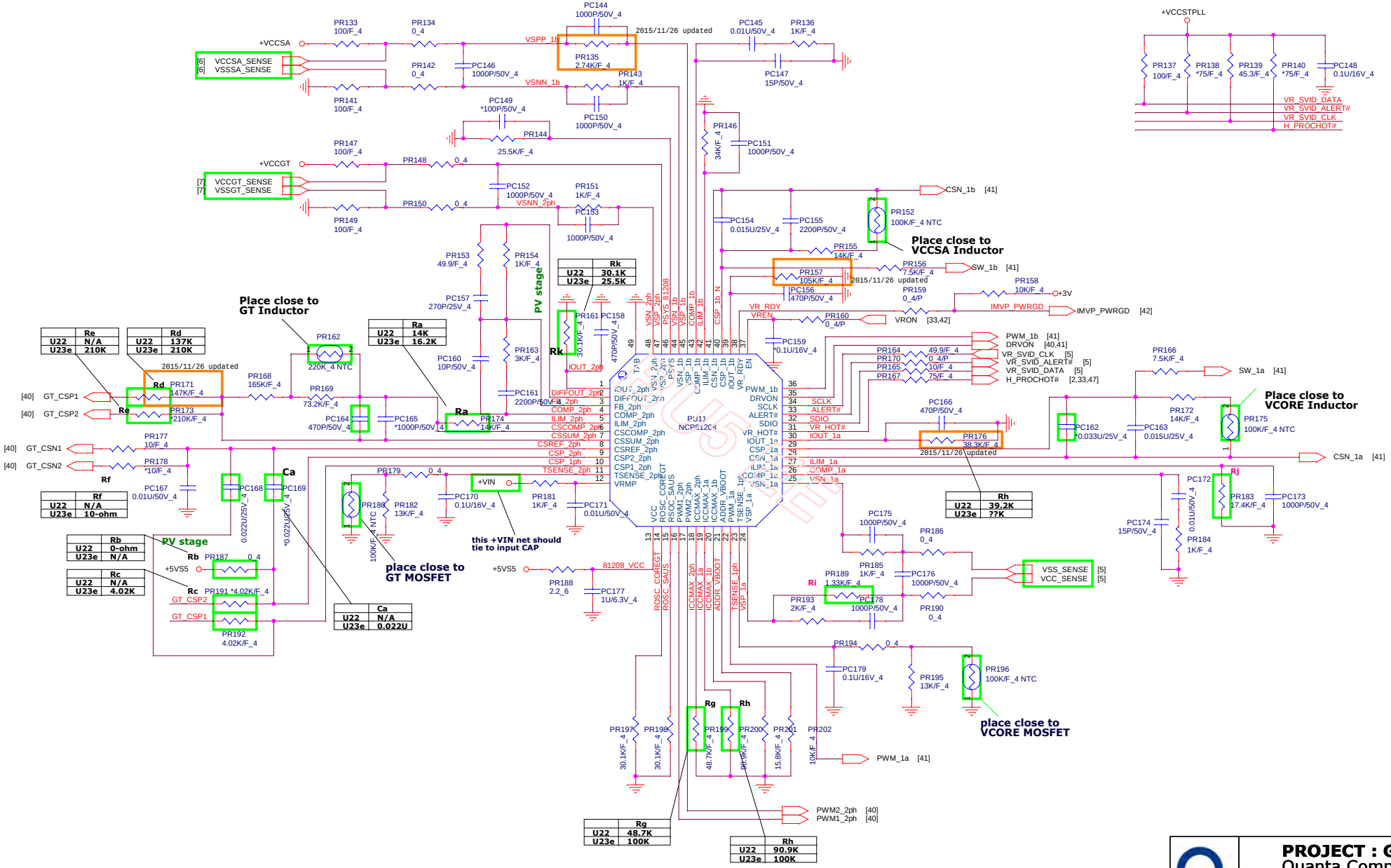
TDC:0.26A



PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
Date: Tuesday, January 05, 2016	Sheet 38 of 47	

+3V [2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,43,44,47]
+5V [25,26,27,30,32,43]
+VIN [25,30,32,34,35,36,37,40,41,42,44,45,47]
+5VPCU [26,34,35,43,46]
+VCCSA [6,41]
+VCCGT [7,40]
+VCCSTPLL [2,4,5,6,9,38]



Re	
U22	N/A
U23e	210K

Rd	
U22	137K
U23e	210K

Ra	
U22	14K
U23e	16.2K

Rk	
U22	30.1K
U23e	25.5K

Rf	
U22	N/A
U23e	10-ohm

Rb	
U22	0-ohm
U23e	N/A

Rc	
U22	N/A
U23e	4.02K

Ca	
U22	N/A
U23e	0.022U

Rg	
U22	48.7K
U23e	100K

Rh	
U22	90.9K
U23e	100K

Rh	
U22	39.2K
U23e	??K

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Size	Document Number	Rev
Custom	CPU VR IC (NCP81206)	2A

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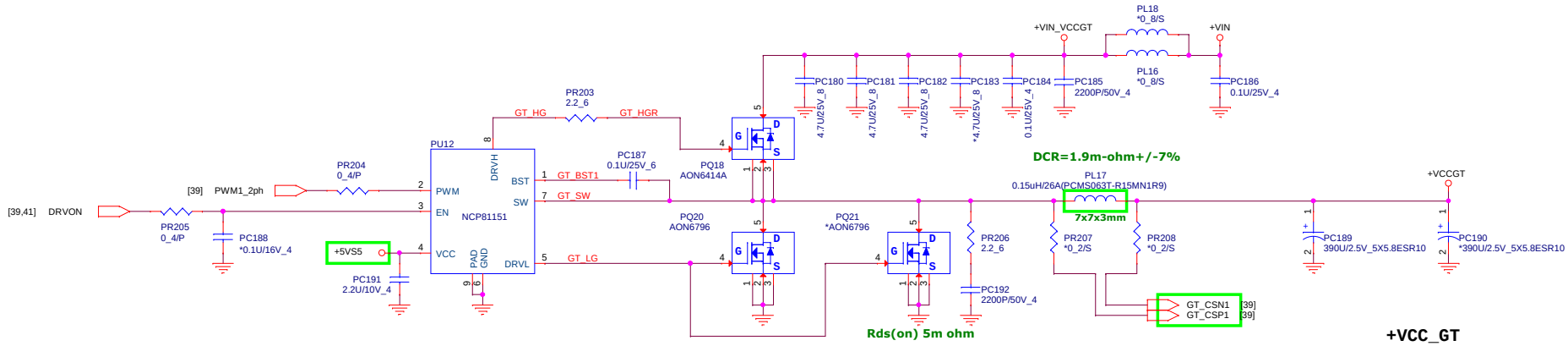
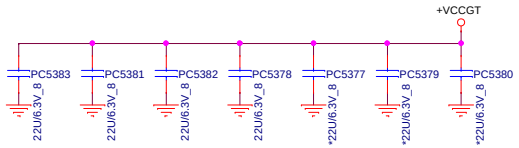
+5V [25,26,27,30,32,43]
+VIN [25,30,32,34,35,36,37,39,41,42,44,45,47]
+5VPCU [26,34,35,43,46]
+VCCGT [7,39]



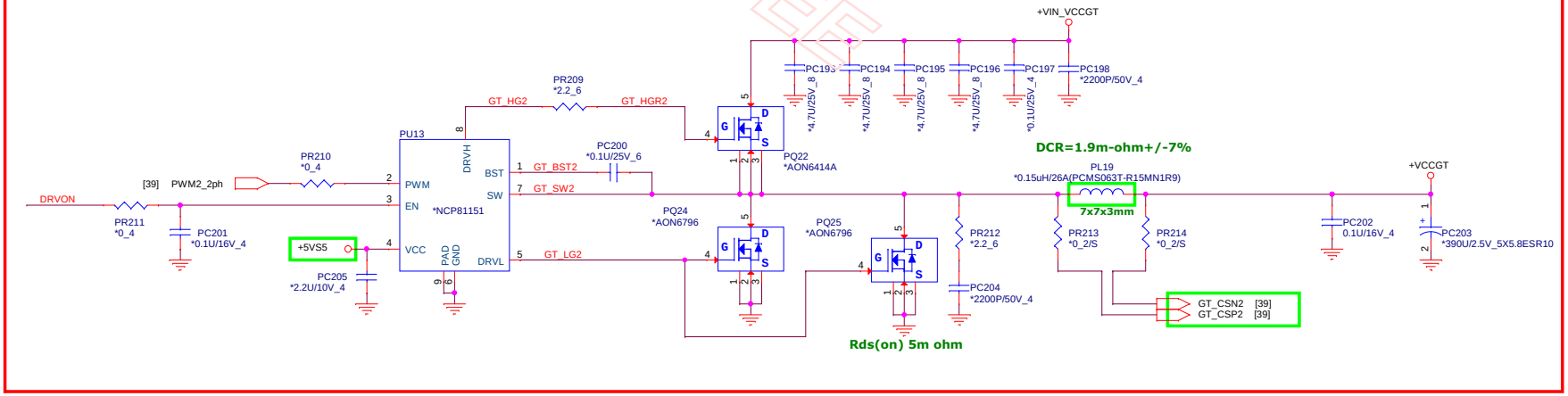


+VCC_GT

U-line 22 (15W)
TDC:18A(22)
Icc max:31A(22)
L/L=3.1mV/A

U-line 23e(28W)
TDC:35A(23e)
Icc max =64A(GT+GTx)
L/L=2mV/A

For U23e --> Add These Components



BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A
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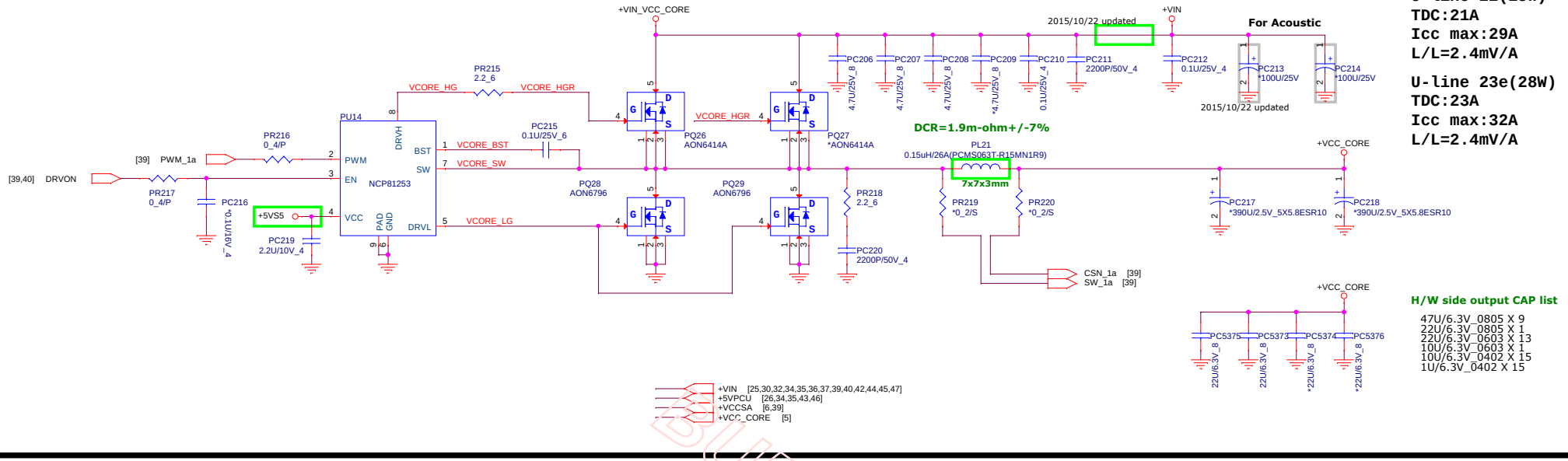
CPU CORE



+VCC_CORE

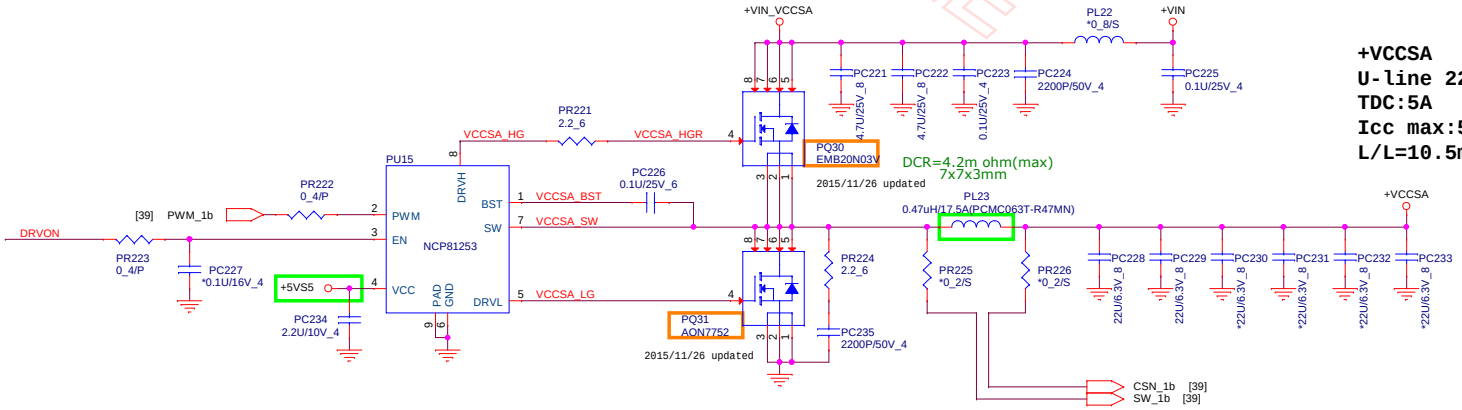
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

U-line 23e(28W)
TDC:23A
Icc max:32A
L/L=2.4mV/A

H/W side output CAP list

47U/6.3V_0805 X 9
22U/6.3V_0805 X 1
22U/6.3V_0603 X 13
10U/6.3V_0603 X 1
10U/6.3V_0402 X 15
1U/6.3V_0402 X 15

VCCSA



+VCCSA
U-line 22&23e
TDC:5A
Icc max:5A
L/L=10.5mV/A

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCORE/VCCSA (NCP81253)	
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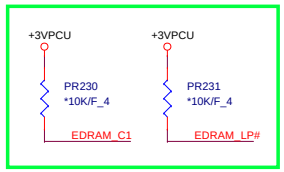
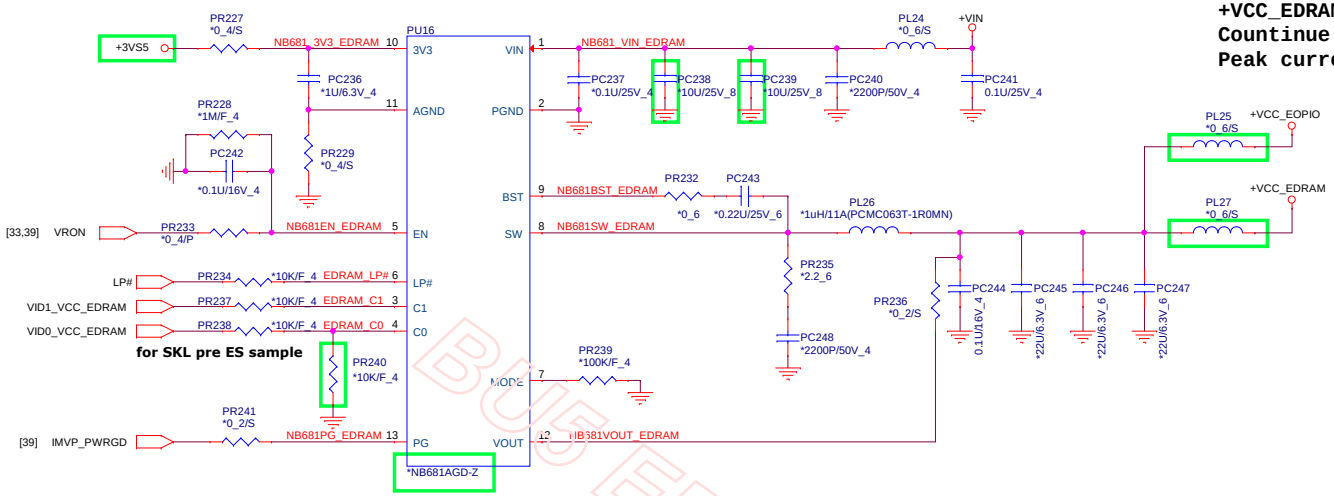
+VIN [25,30,32,34,35,36,37,39,40,41,44,45,47]
+3VPCU [6,13,30,32,33,34,35,47]
+VCC_EOPIO [5]
+VCC_EDRAM [5]





+VCC_EDRAM +/- 5%
Countinue current:4.5A
Peak current:6A

VCC_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

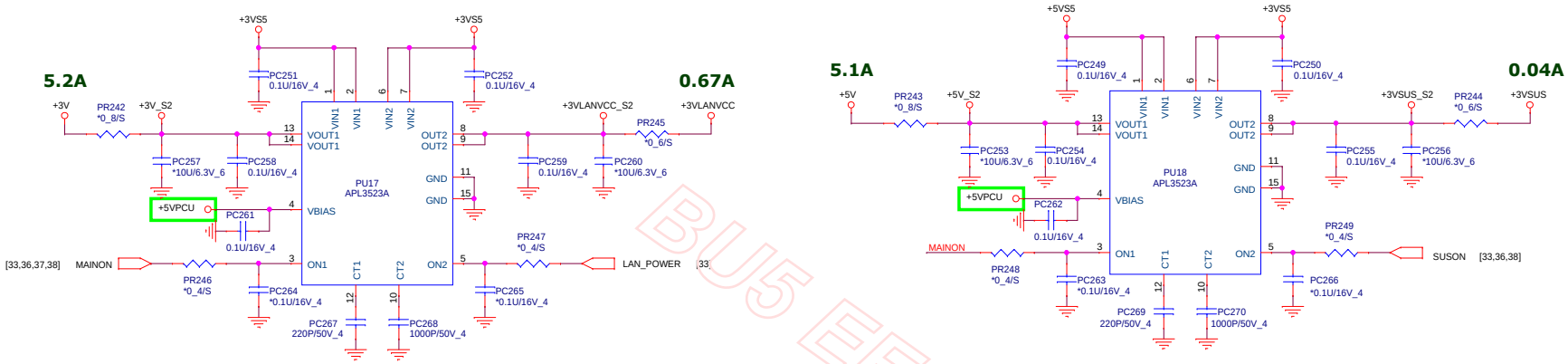
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCC_EDRAM (NB681)_23E	
Date: Tuesday, January 05, 2016	Sheet 42 of 47	

+3V [2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,44,47]
+5V [25,26,27,30,32]
+VIN [25,30,32,34,35,36,37,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,35,36,37,38,42,46,47]
+5VS5 [4,25,26,29,35,36,37,38,39,40,41,44,45,46]
+3VSUS [30]
+5V_CAM
+3VLANVCC [28]



BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A
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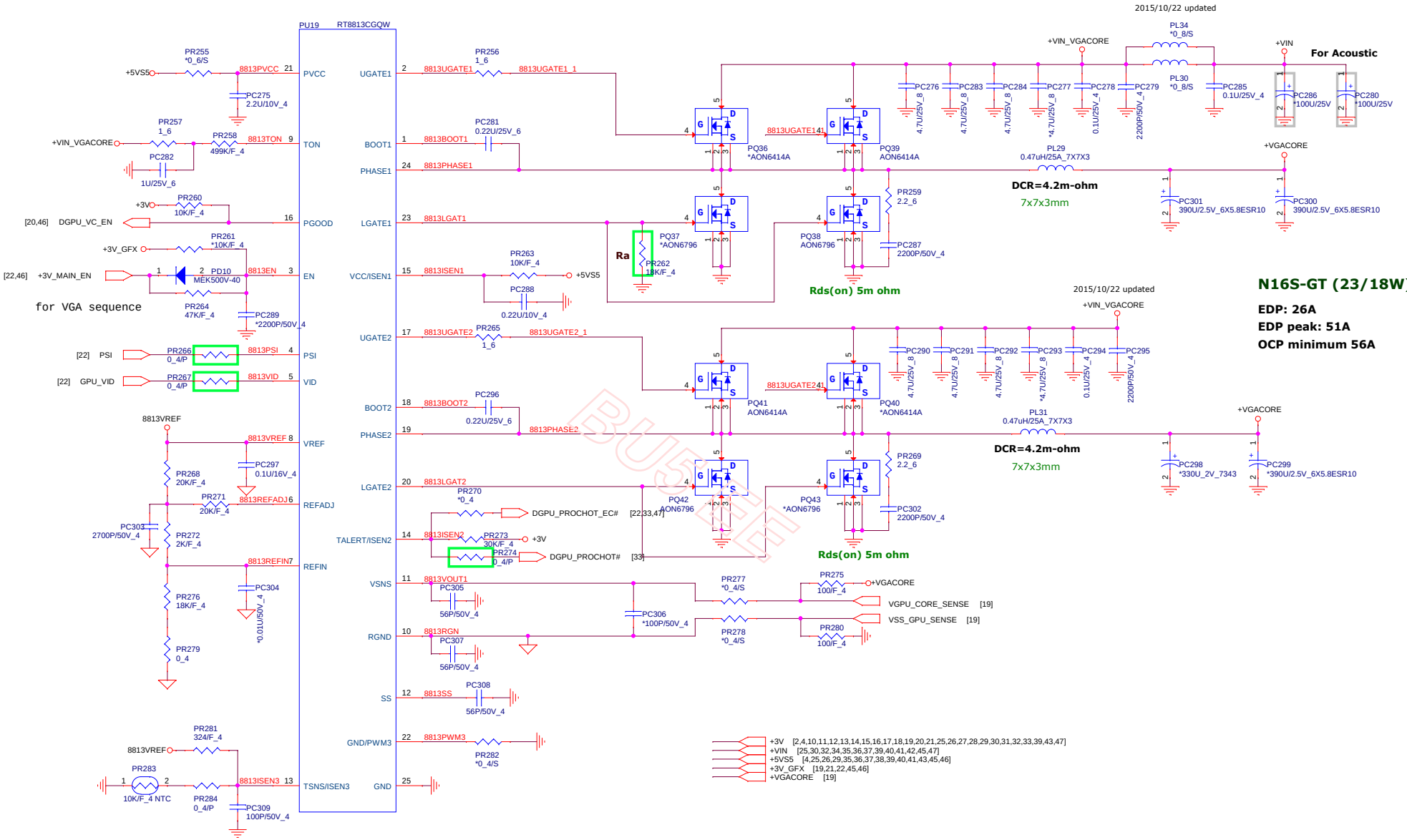
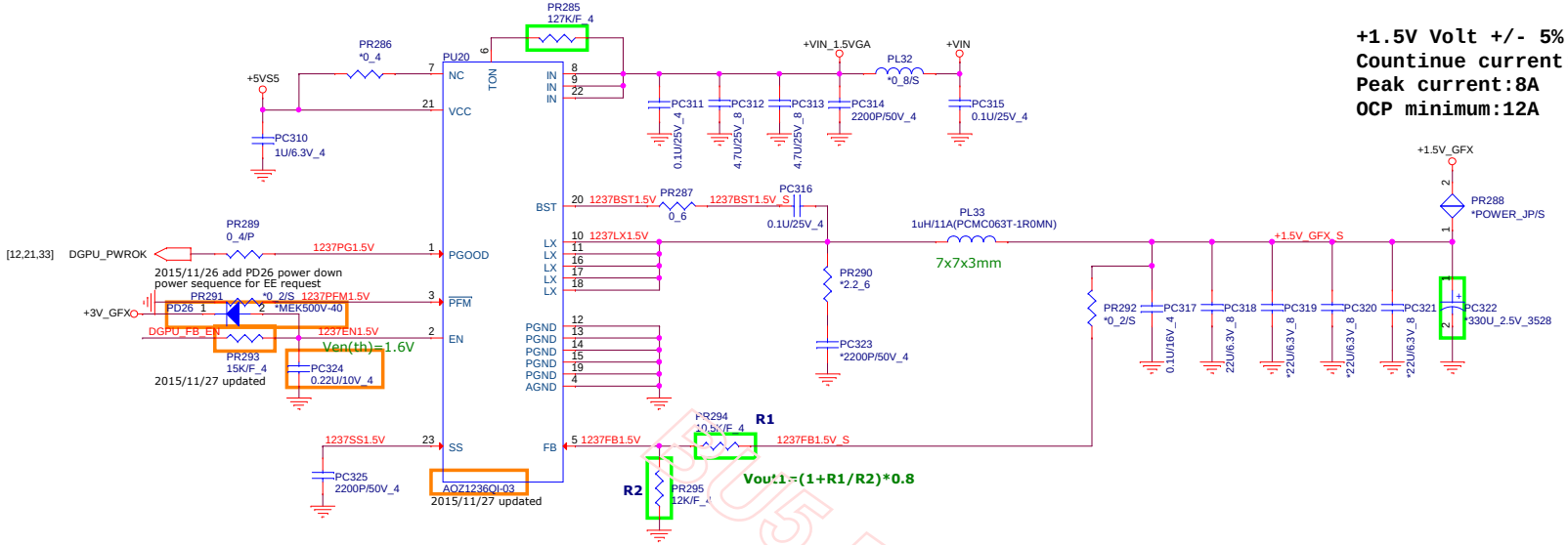
VGA Core

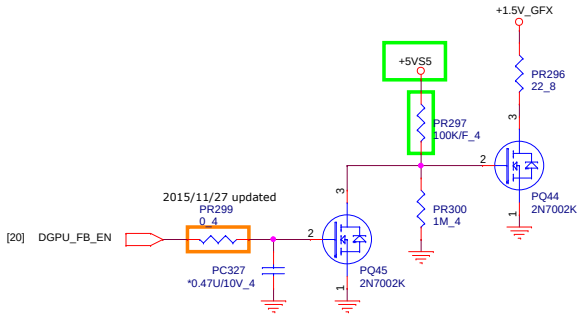


BU5	**PROJECT : G34A** Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE (RT8813A)	Rev: 2A
Date: Tuesday, January 05, 2016	Sheet 44 of 47	

+VIN [25,30,32,34,35,36,37,39,40,41,42,44,47]
+5VS5 [4,25,26,29,35,36,37,38,39,40,41,43,44,46]
+1.5V_GFX [20,21,23,24]

+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



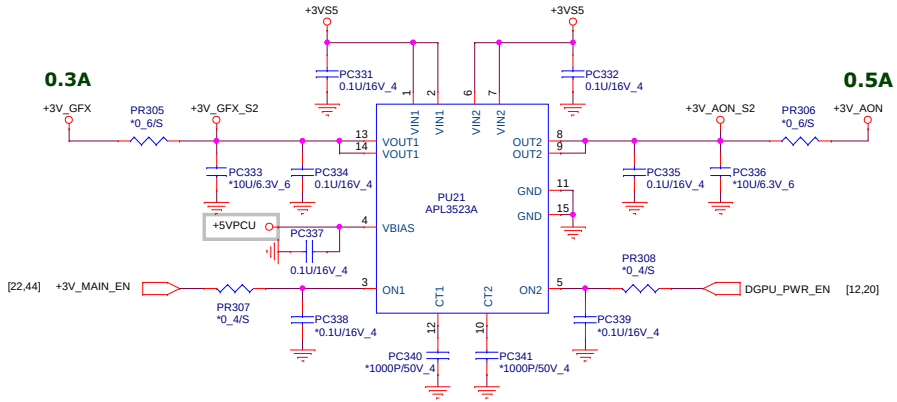


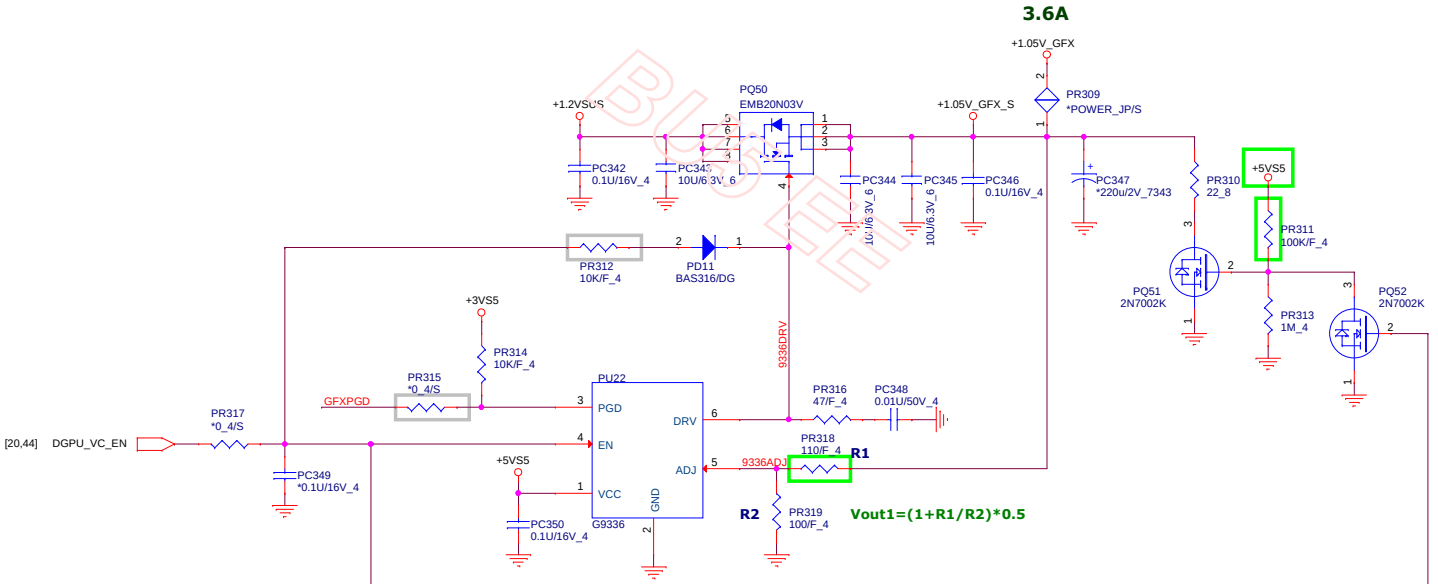
BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_VGA(AOZ1237)	1A
Date: Tuesday, January 05, 2016	Sheet 45 of 47	

+VIN [25,30,32,34,35,36,37,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,35,36,37,38,42,43,47]
+5VS5 [4,25,26,29,35,36,37,38,39,40,41,43,44,45]
+3V_GFX [19,21,22,44,45]
+3V_AON [19,22]
+1.2VSUS [3,6,17,18,36,38]
+1.05V_GFX [19,20,21]

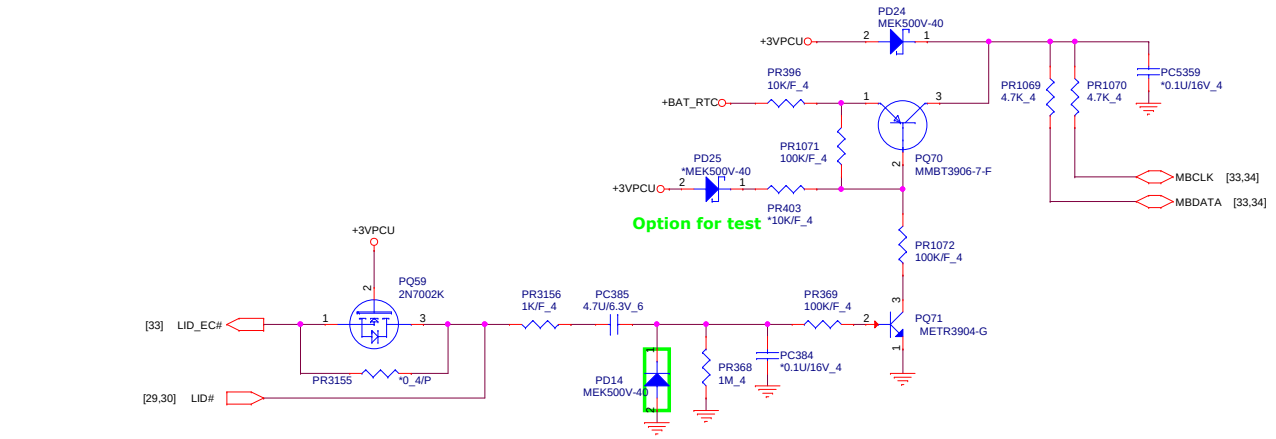




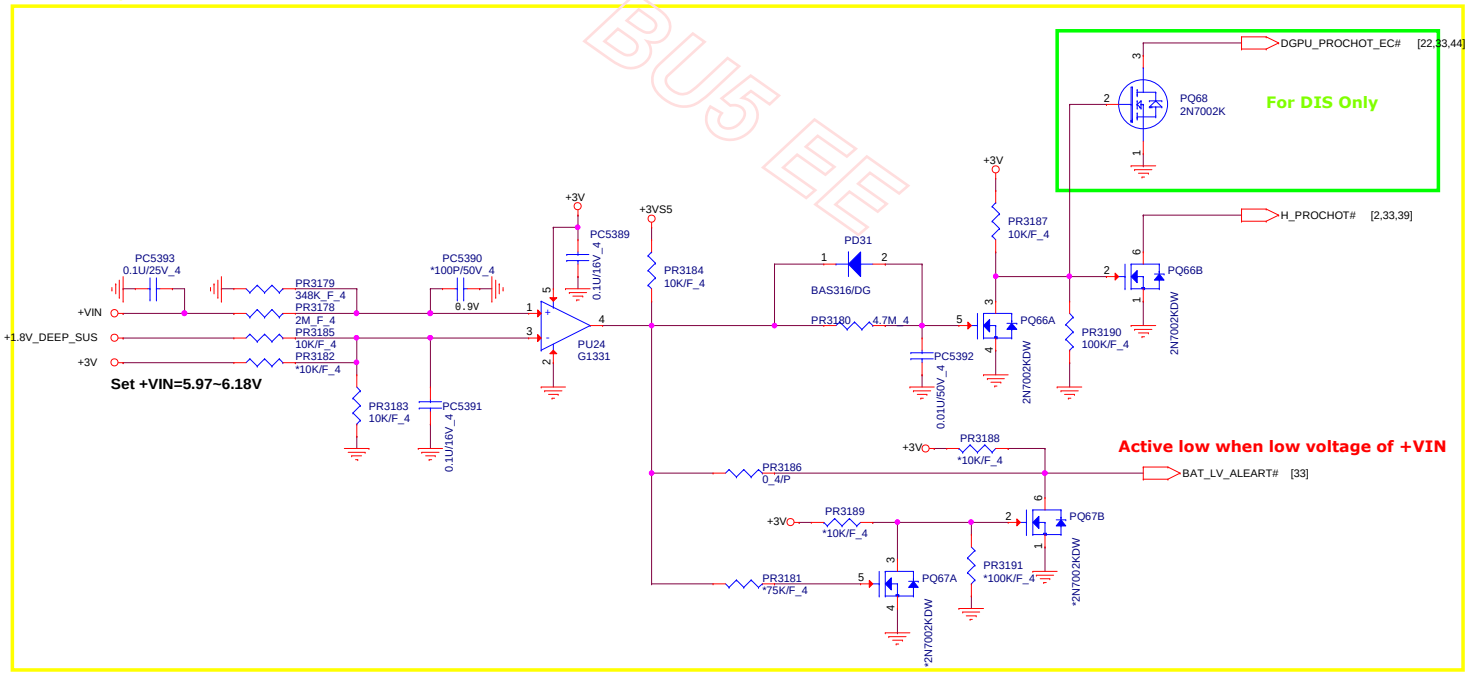
BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V_VGA/3V_VGA	1A
Date: Tuesday, January 05, 2016	Sheet 46 of 47	



20160105 updated



BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LIDS/W for storage mode	1A
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