COMPAL CONFIDENTIAL

MODEL NAME : DAZ20 (SBMLK 12) / DAZ30 (SBMLK 13)

PCB NO : LA-F312P

BOM P/N : 431A8W31L0X (12_NonAR)

Steamboat MLK 12"/13" NonAR

Kabylake-U U22 & Kabylake-R U42

2017-12-29

REV : 2.0 (A01)

@ : Nopop Component
EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CXDP@ : XDP Component
CONN@ : Connector Component
ESPI@ : ESPI interface Component
LPC@ : External ESPI Component (SHD)
U42@ : KBL-R U42 Component
U22@ : KBL-R U22 Component
SB12@ : For SB12 System ID
SB13@ : For SB13 System ID
DS3@ : Deep sleep Component
NDS3@ : Non Deep sleep Component
546@ : TI TUSB546 Component
8743@ : PARADE PS8743 Component

MB PCB

Part Number	Description
DA8001CG010	PCB 263 LA-F312P REV0 MB NAR 1

Layout Dell logo

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REV:A01
PWB: 3DRR6

Power CKT : 0919
GPIO map : 0821

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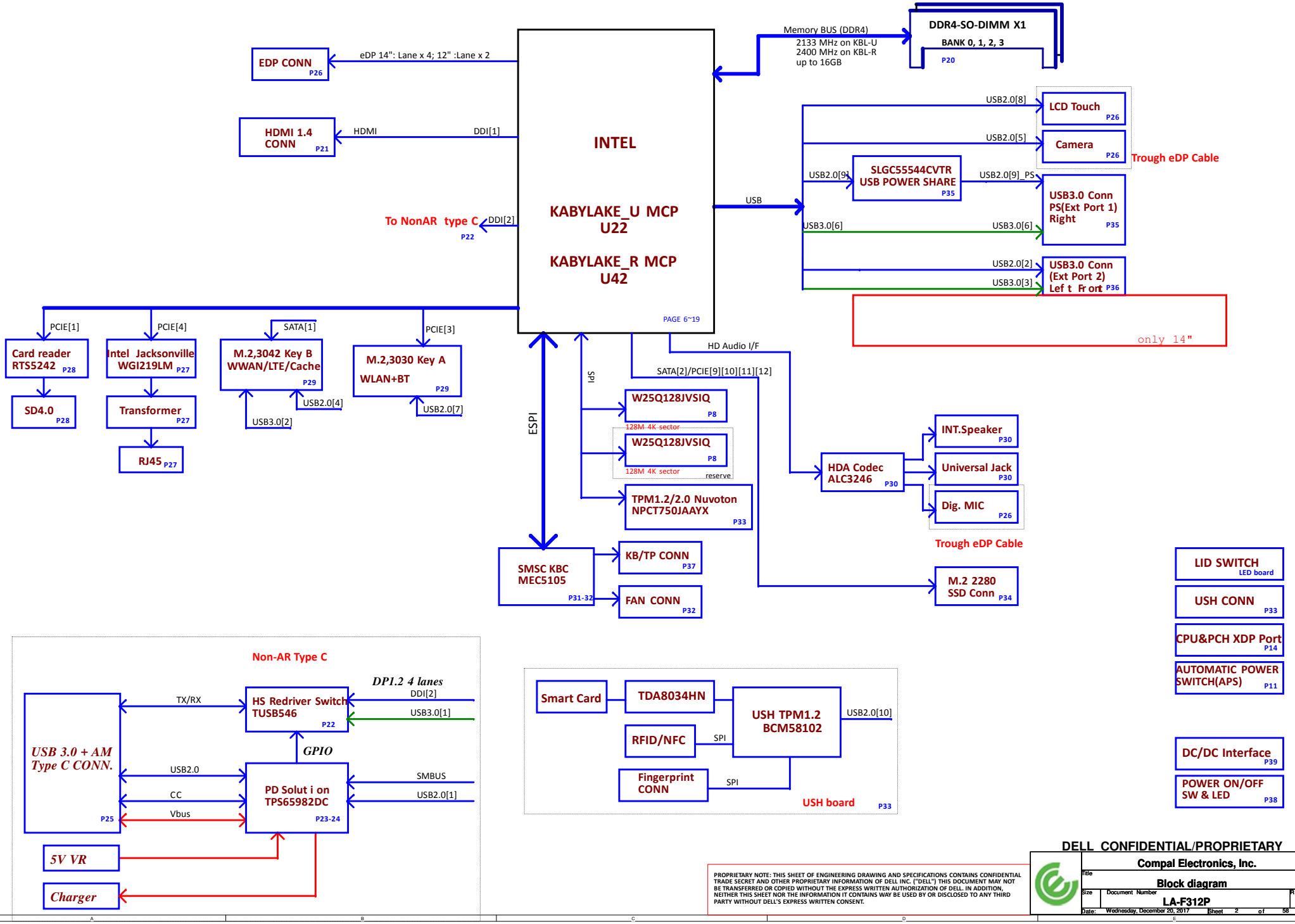
Title: Cover Sheet

Size | Document Number: LA-F312P | Rev: 2.0

Date: Friday, December 29, 2017 Sheet 1 of 58

Steamboat MLK 12&13 w/o AR Block Diagram

Steamboat MLK 12&13 only support one DIMM
Reverse Type



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Title: Block diagram

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 2 of 58

NonAR config

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.0mm ± 10%)			39.4		41.40000

1.05156

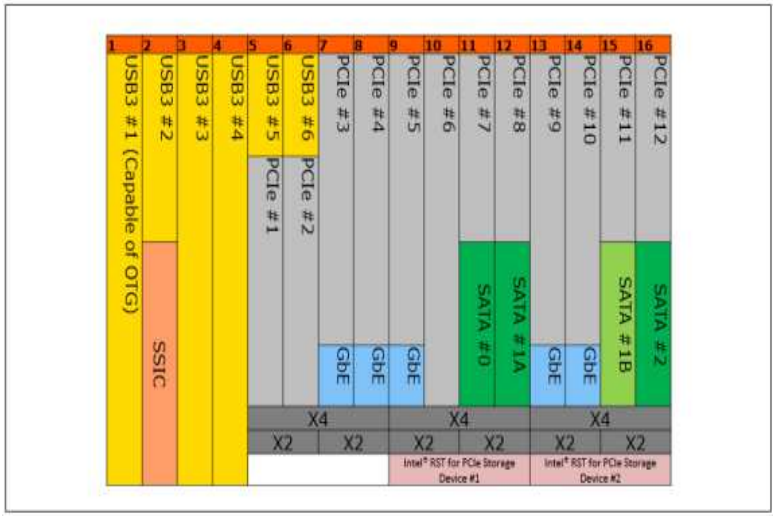
AR use 1086PP (10L)
Non AR use 1080PP (8L)

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				Typce-C(Non AR)
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Lef t Fr ont
USB3.0-4				JUSB3-->Lef t Rear (SB14 onl y)
USB3.0-5		PCIE-1		Card Reader (PCIE)
USB3.0-6		PCIE-2		JUSB1-->Right
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	NA
		PCIE-8	SATA-1	M.2 3042(SATA Cache)
		PCIE-9		M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-1*	
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	Typce-C(Non AR)
2	JUSB2-->Lef t Fr ont
3	JUSB3-->Lef t Rear (SB14 onl y)
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	JUSB1-->Right
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



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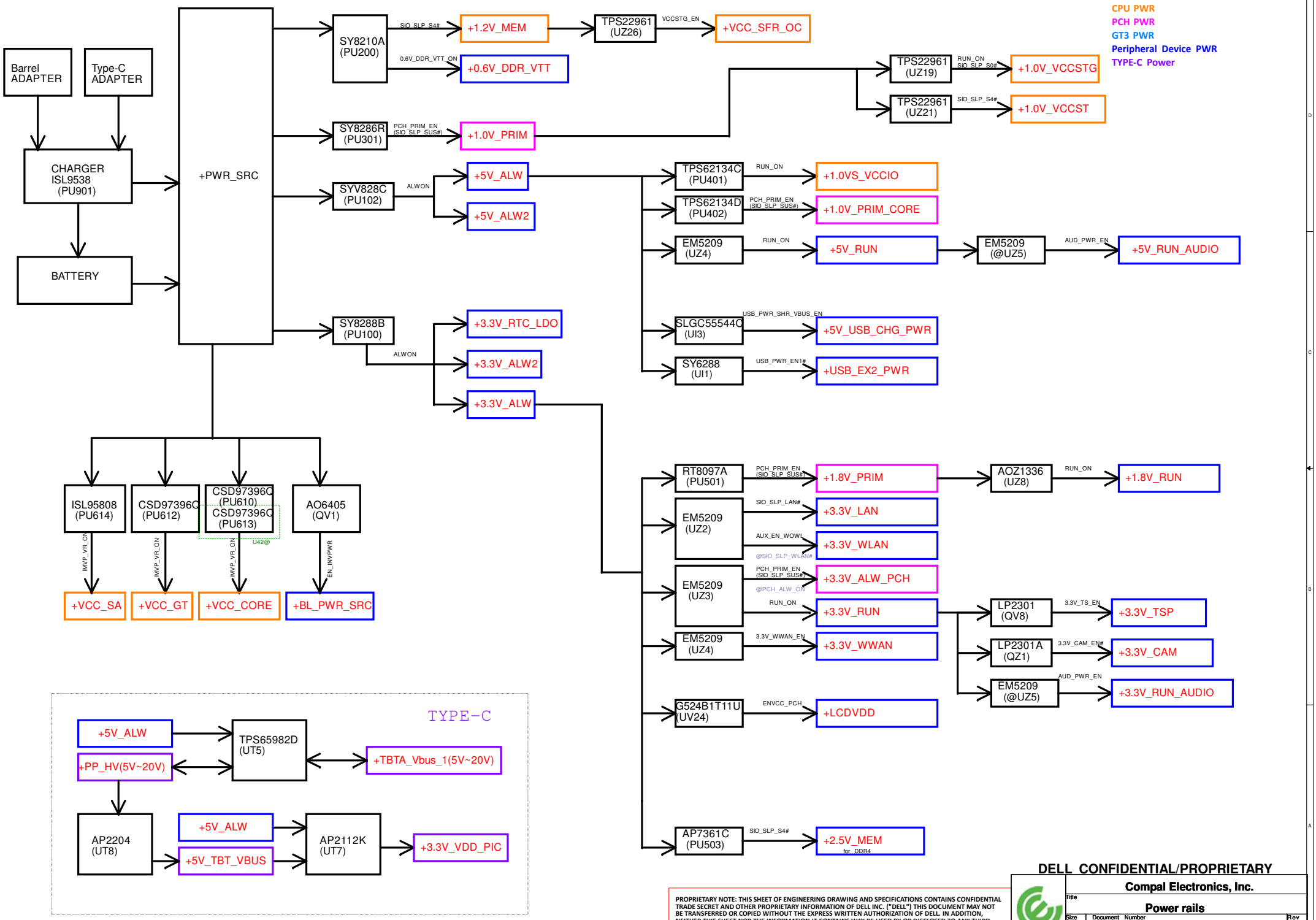
Title: Port assignment

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 3 of 58



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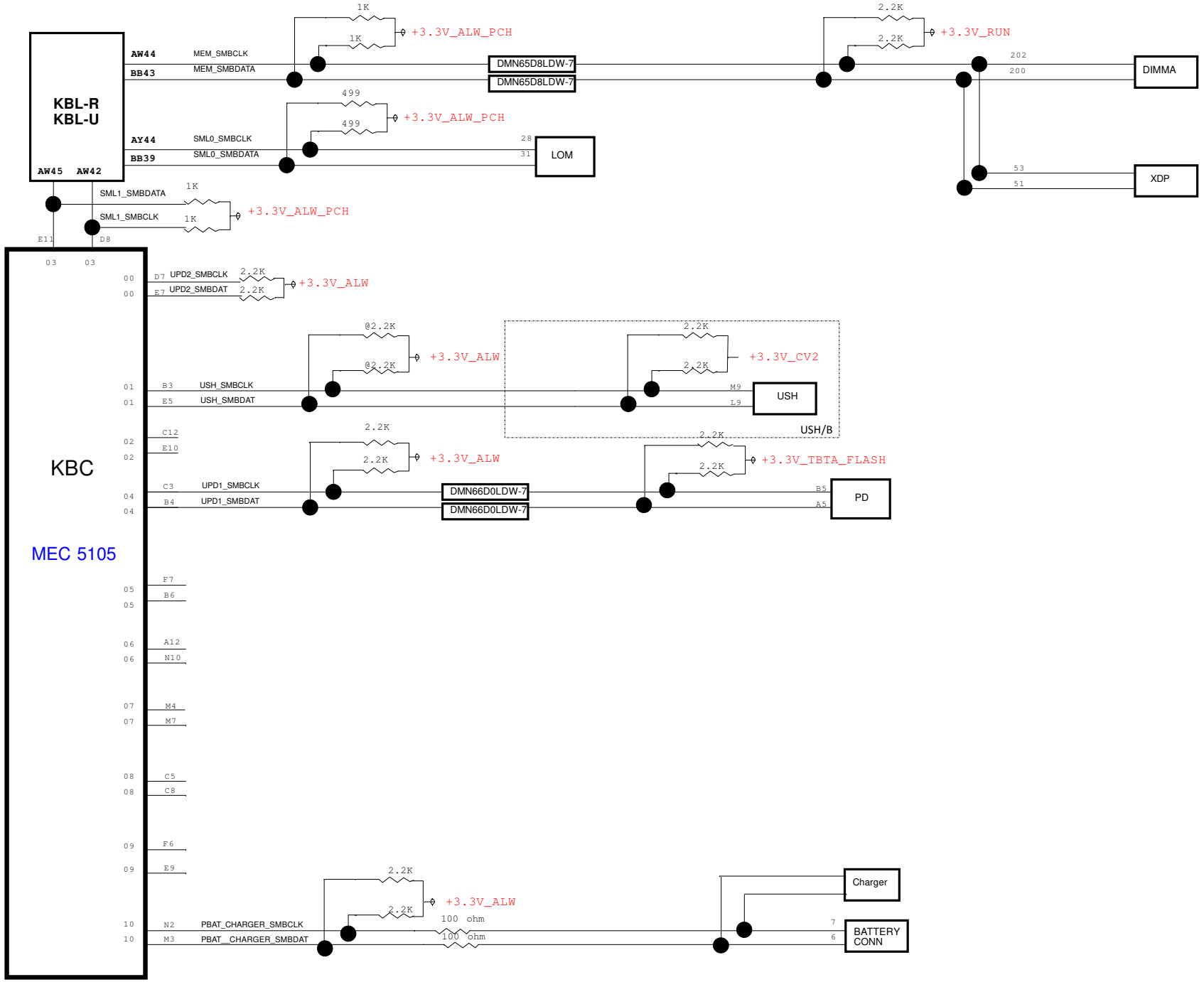
Title: Power rails

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 4 of 58



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Title: Port assignment

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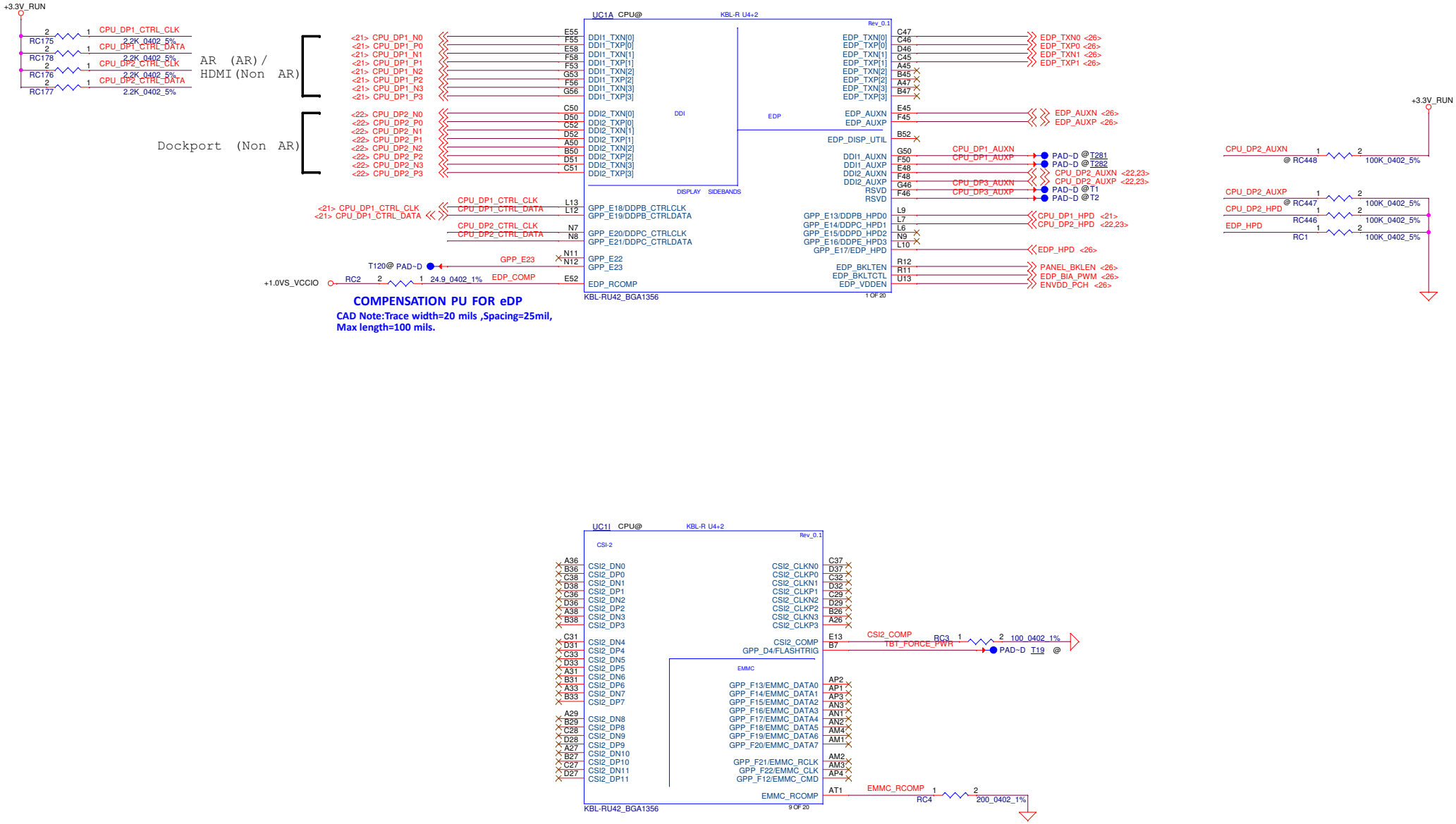
Date: Wednesday, December 20, 2017 | Sheet 5 of 58



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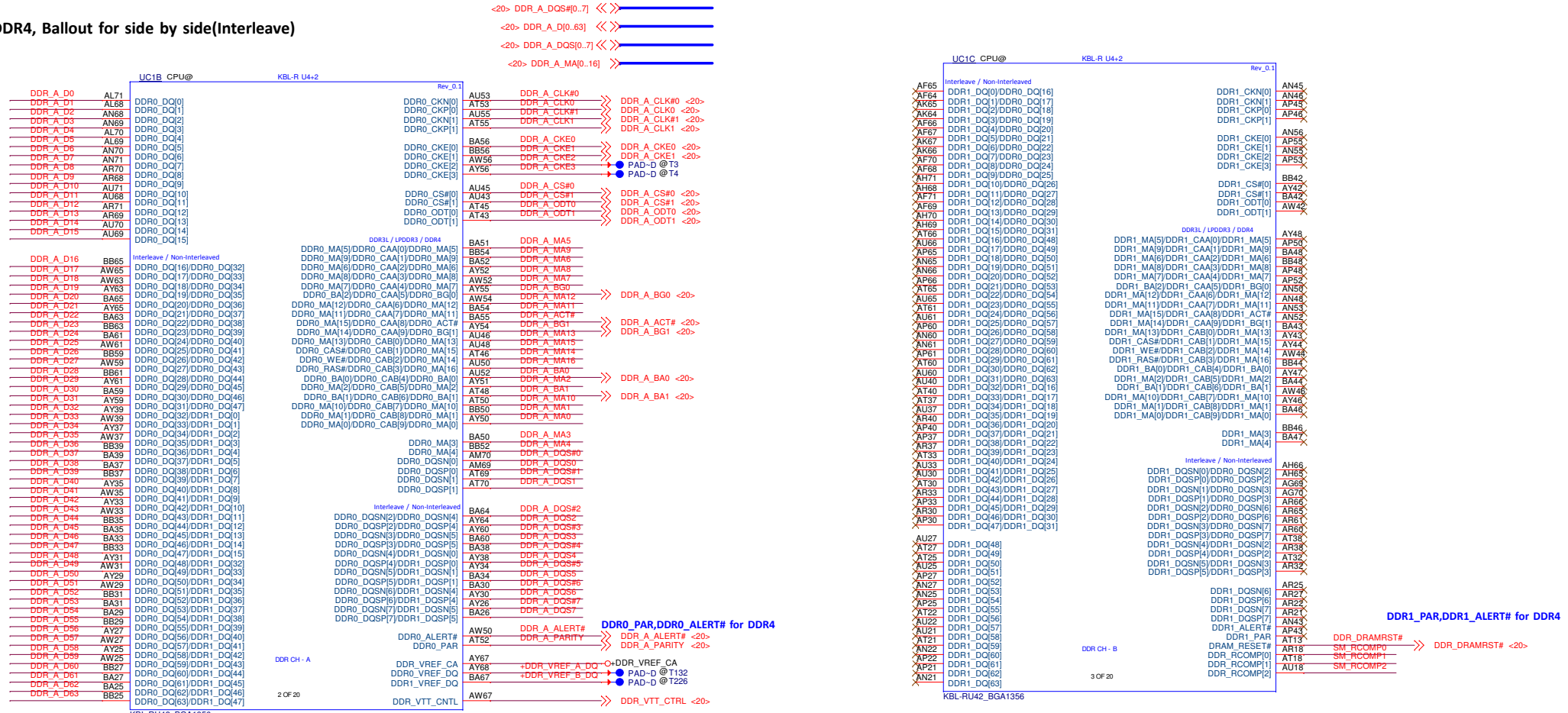
Title: CPU (1/14)

Size | Document Number: LA-F312P | Rev: 2.0

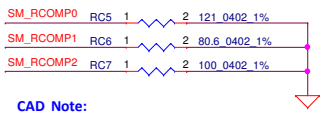
Date: Wednesday, December 20, 2017 | Sheet 6 of 58

For DDR4

DDR4, Ballout for side by side(Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Compal Electronics, Inc.

Title: CPU (2/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 7 of 58

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

UC1E CPU@ KBL-R U4+2

SPI - FLASH

SPI - TOUCH

C LINK

LPC

SMBUS, SMLINK

KBL-RU42_BGA1356

5 OF 20

CHECK LPC_CLK FOR DEBUG CARD?

Reserve

SOFTWARE TAA

RF Request

Place close CPU side

128Mb Flash ROM

W25Q128JVSIQ_SO8

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

WEAK INTERNAL 20K PD

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

WEAK INTERNAL 20k PD

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

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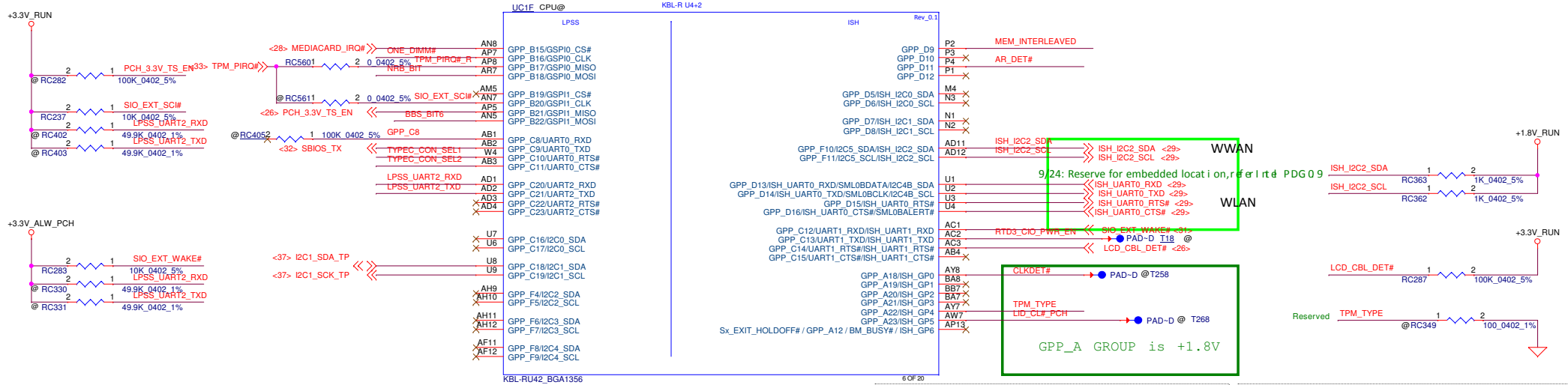
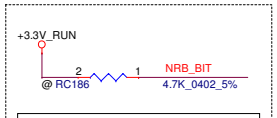
Title: CPU (3/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 8 of 58

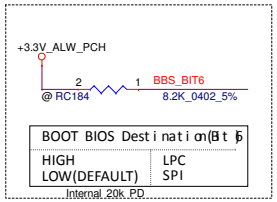
For BR/SB





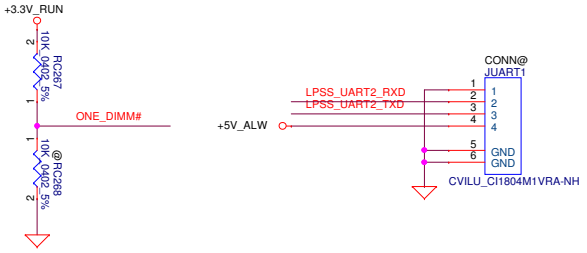
NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Weak IPD

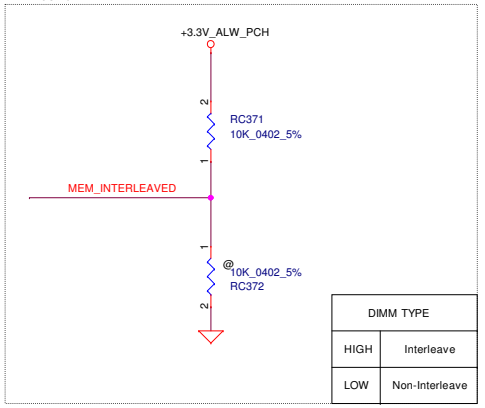


BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI

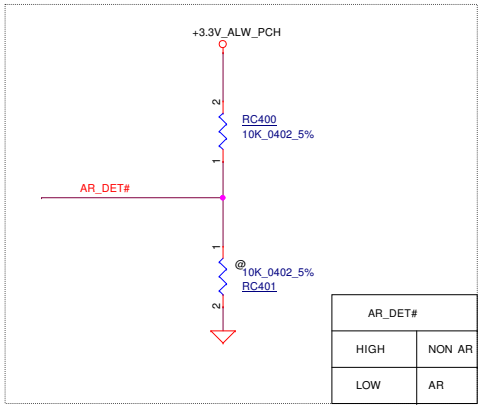
Internal 20k PD



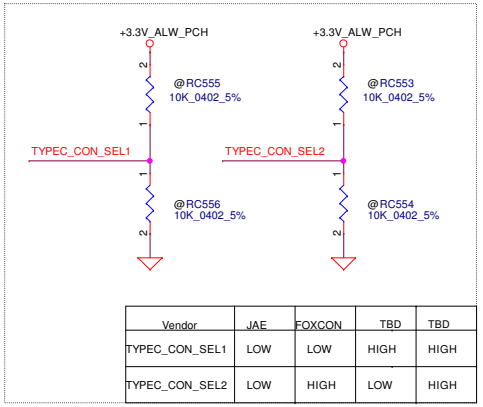
DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM



DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave



AR_DET#	
HIGH	NON AR
LOW	AR



Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

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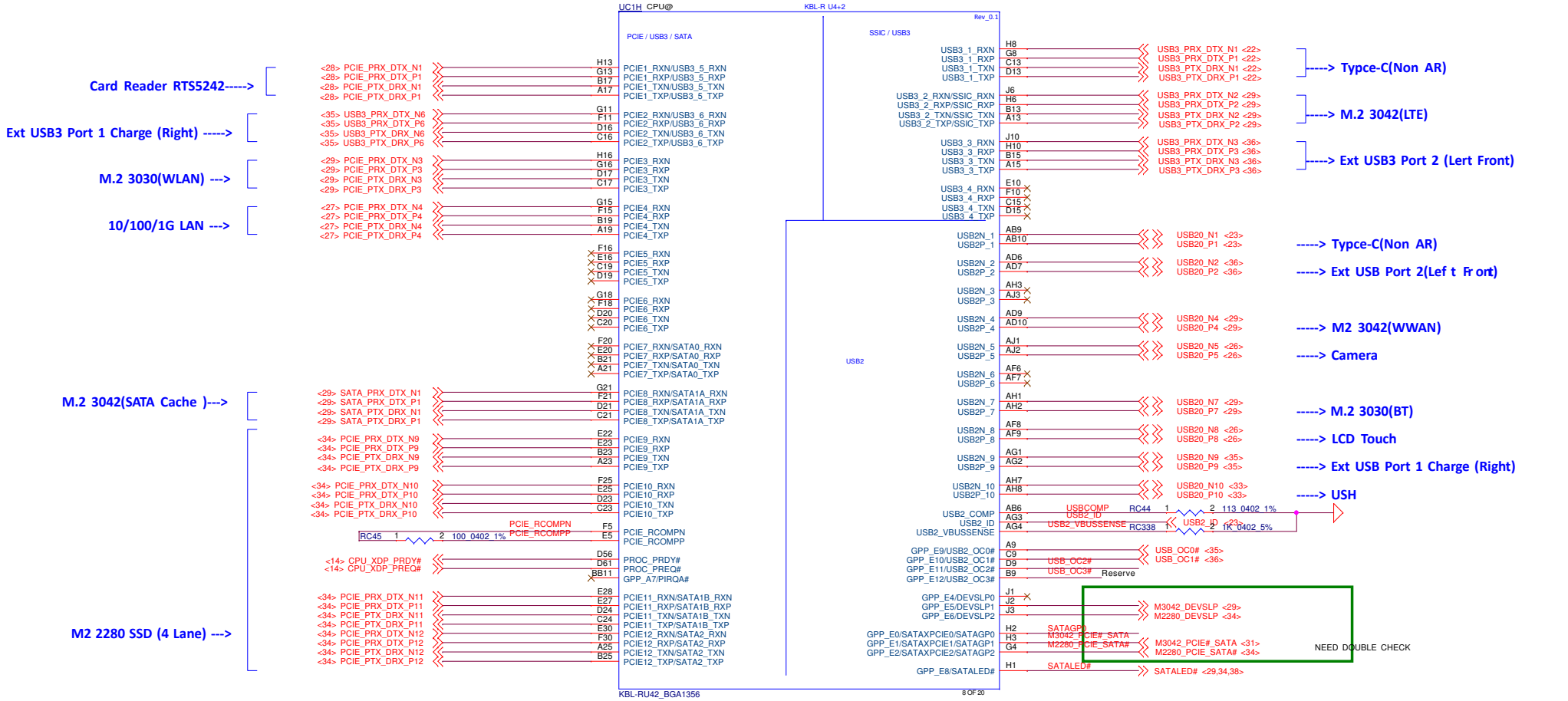
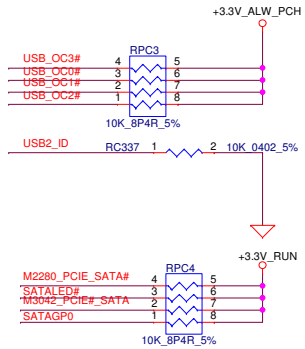
Title: CPU (4/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 9 of 58

Steamboat MLK 12&13 nonAR





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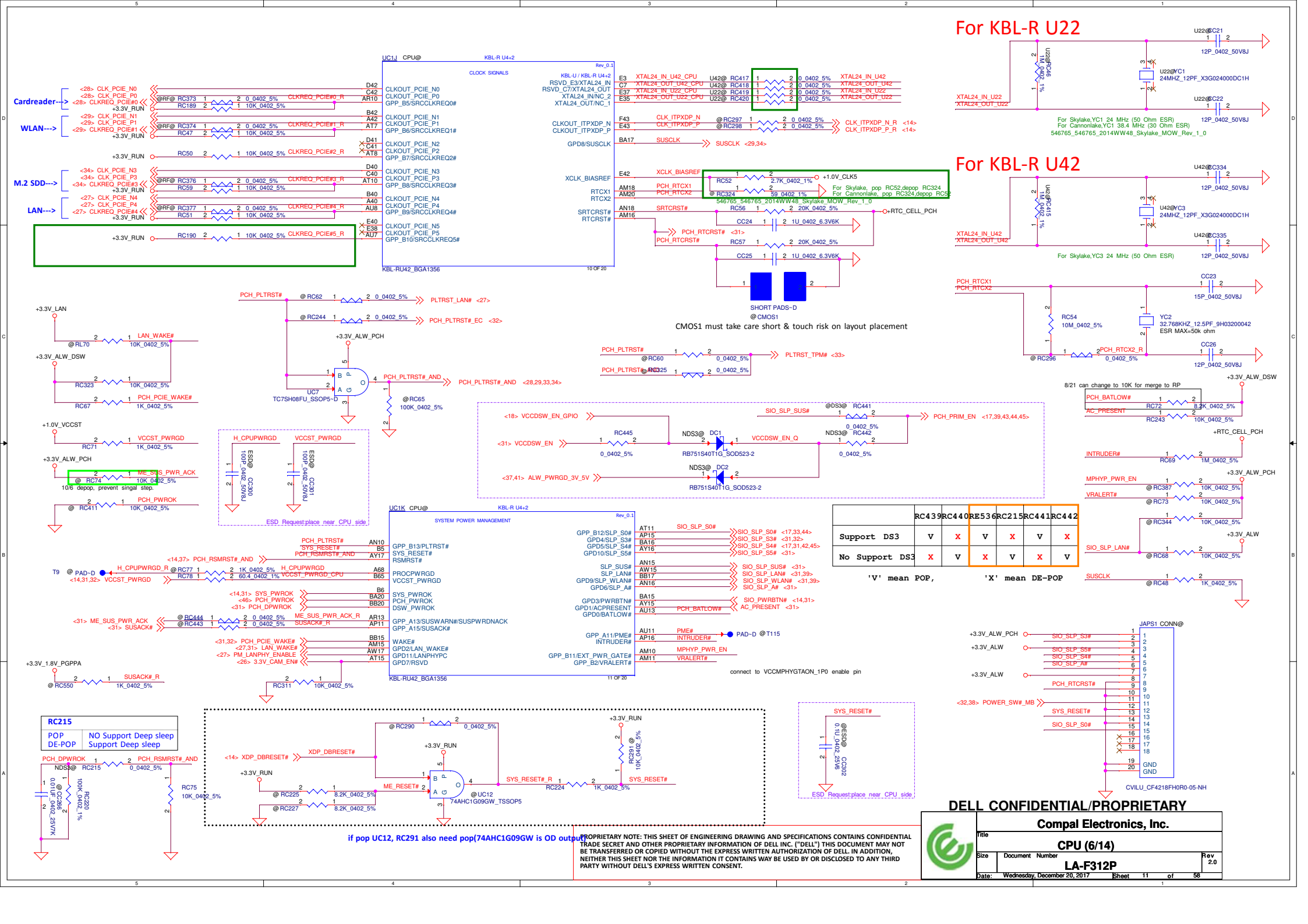
Compal Electronics, Inc.

Title: CPU (5/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 10 of 58



	RC439	RC440	RE536	RC215	RC441	RC442
Support DS3	V	X	V	X	V	X
No Support DS3	X	V	X	V	X	V

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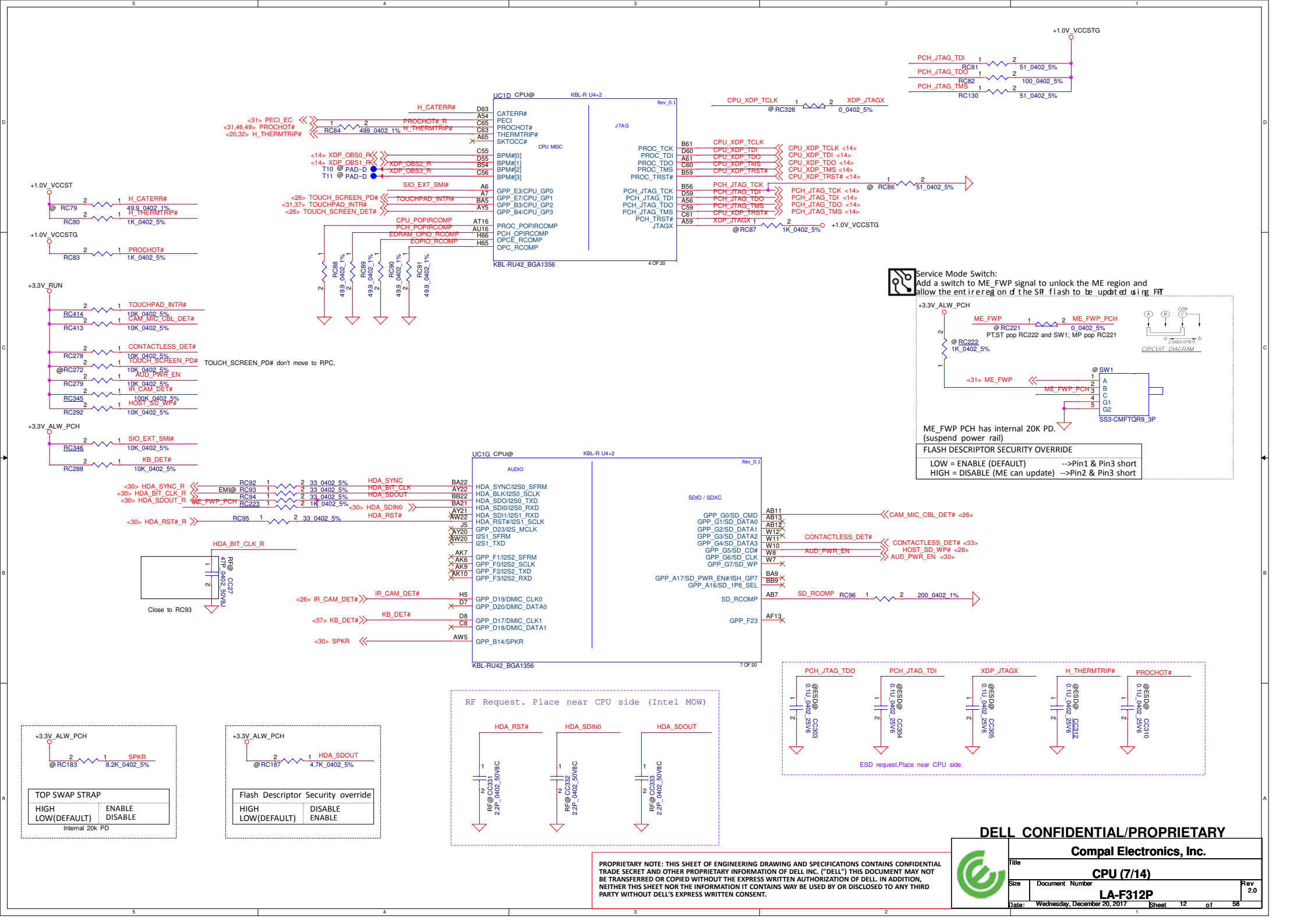
+1.0V_VCCSTG
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
RC81 51_0402_5%
RC82 100_0402_5%
RC130 51_0402_5%
UC1D CPU@
KBL-R U4+2
Rev_0.1
JTAG
CPU MISC
CPU_XDP_TCLK
XDP_JTAGX
@RC328 0_0402_5%
H_CATERR#
<31> PECI_EC
<31,46,49> PROCHOT#
<20,32> H_THERMTRIP#
RC84 499_0402_1%
PROCHOT#_R
H_THERMTRIP#
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
<14> XDP_OBS0_R
<14> XDP_OBS1_R
T10 @ PAD~D
T11 @ PAD~D
XDP_OBS2_R
XDP_OBS3_R
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
SIO_EXT_SMI#
<26> TOUCH_SCREEN_PD#
<31,37> TOUCHPAD_INTR#
<26> TOUCH_SCREEN_DET#
TOUCHPAD_INTR#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
CPU_POPIRCOMP
PCH_POPIRCOMP
EDRAM_OPIO_RCOMP
EOPIO_RCOMP
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
RC88 RC89 RC90 RC91 499_0402_1%
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
JTAGX
CPU_XDP_TDI
CPU_XDP_TDO
CPU_XDP_TMS
CPU_XDP_TRST#
PCH_JTAG_TCK <14>
PCH_JTAG_TDI <14>
PCH_JTAG_TDO <14>
PCH_JTAG_TMS <14>
CPU_XDP_TCLK <14>
CPU_XDP_TDI <14>
CPU_XDP_TDO <14>
CPU_XDP_TMS <14>
CPU_XDP_TRST# <14>
@RC86 51_0402_5%
@RC87 1K_0402_5%
+1.0V_VCCSTG
KBL-RU42_BGA1356
4 OF 20
+1.0V_VCCST
@ RC79 49.9_0402_1%
H_CATERR#
RC80 1K_0402_5%
H_THERMTRIP#
+1.0V_VCCSTG
RC83 1K_0402_5%
PROCHOT#
+3.3V_RUN
RC414 10K_0402_5%
TOUCHPAD_INTR#
RC413 10K_0402_5%
CAM_MIC_CBL_DET#
RC278 10K_0402_5%
CONTACTLESS_DET#
@RC272 10K_0402_5%
TOUCH_SCREEN_PD#
RC279 10K_0402_5%
AUD_PWR_EN
RC345 100K_0402_5%
IR_CAM_DET#
RC292 10K_0402_5%
HOST_SD_WP#
TOUCH_SCREEN_PD# don't move to RPC,
+3.3V_ALW_PCH
RC346 10K_0402_5%
SIO_EXT_SMI#
RC288 10K_0402_5%
KB_DET#
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT
+3.3V_ALW_PCH
ME_FWP
@RC221 0_0402_5%
ME_FWP_PCH
PT,ST pop RC222 and SW1; MP pop RC221
@RC222 1K_0402_5%
CON
CIRCUIT DIAGRAM
<31> ME_FWP
@SW1
A
B
C
G1
G2
SS3-CMFTQR9_3P
ME_FWP PCH has internal 20K PD.
(suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
UC1G CPU@
KBL-R U4+2
Rev_0.1
AUDIO
SDIO / SDXC
<30> HDA_SYNC_R
<30> HDA_BIT_CLK_R
<30> HDA_SDOUT_R
ME_FWP_PCH
EMI@ RC92 RC93 RC94 RC223 33_0402_5% 1K_0402_5%
HDA_SYNC
HDA_BIT_CLK
HDA_SDOUT
<30> HDA_SDIN0
HDA_RST#
<30> HDA_RST#_R
RC95 33_0402_5%
HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
I2S1_SFRM
I2S1_TXD
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_A17/SD_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_RCOMP
GPP_F23
CAM_MIC_CBL_DET# <26>
CONTACTLESS_DET# <33>
HOST_SD_WP# <28>
AUD_PWR_EN <30>
SD_RCOMP RC96 200_0402_1%
HDA_BIT_CLK_R
RF@ CC27 47P_0402_50V8J
Close to RC93
<26> IR_CAM_DET#
IR_CAM_DET#
<37> KB_DET#
KB_DET#
<30> SPKR
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
GPP_B14/SPKR
KBL-RU42_BGA1356
7 OF 20
RF Request. Place near CPU side (Intel MOW)
HDA_RST#
HDA_SDIN0
HDA_SDOUT
RF@ CC331 CC332 CC333 2.2P_0402_50V8C
PCH_JTAG_TDO
PCH_JTAG_TDI
XDP_JTAGX
H_THERMTRIP#
PROCHOT#
@ESD@ CC303 CC304 CC305 CC312 CC310 0.1U_0402_25V6
ESD request,Place near CPU side.
+3.3V_ALW_PCH
@RC183 8.2K_0402_5%
SPKR
TOP SWAP STRAP
HIGH ENABLE
LOW(DEFAULT) DISABLE
Internal 20k PD
+3.3V_ALW_PCH
@RC187 4.7K_0402_5%
HDA_SDOUT
Flash Descriptor Security override
HIGH DISABLE
LOW(DEFAULT) ENABLE
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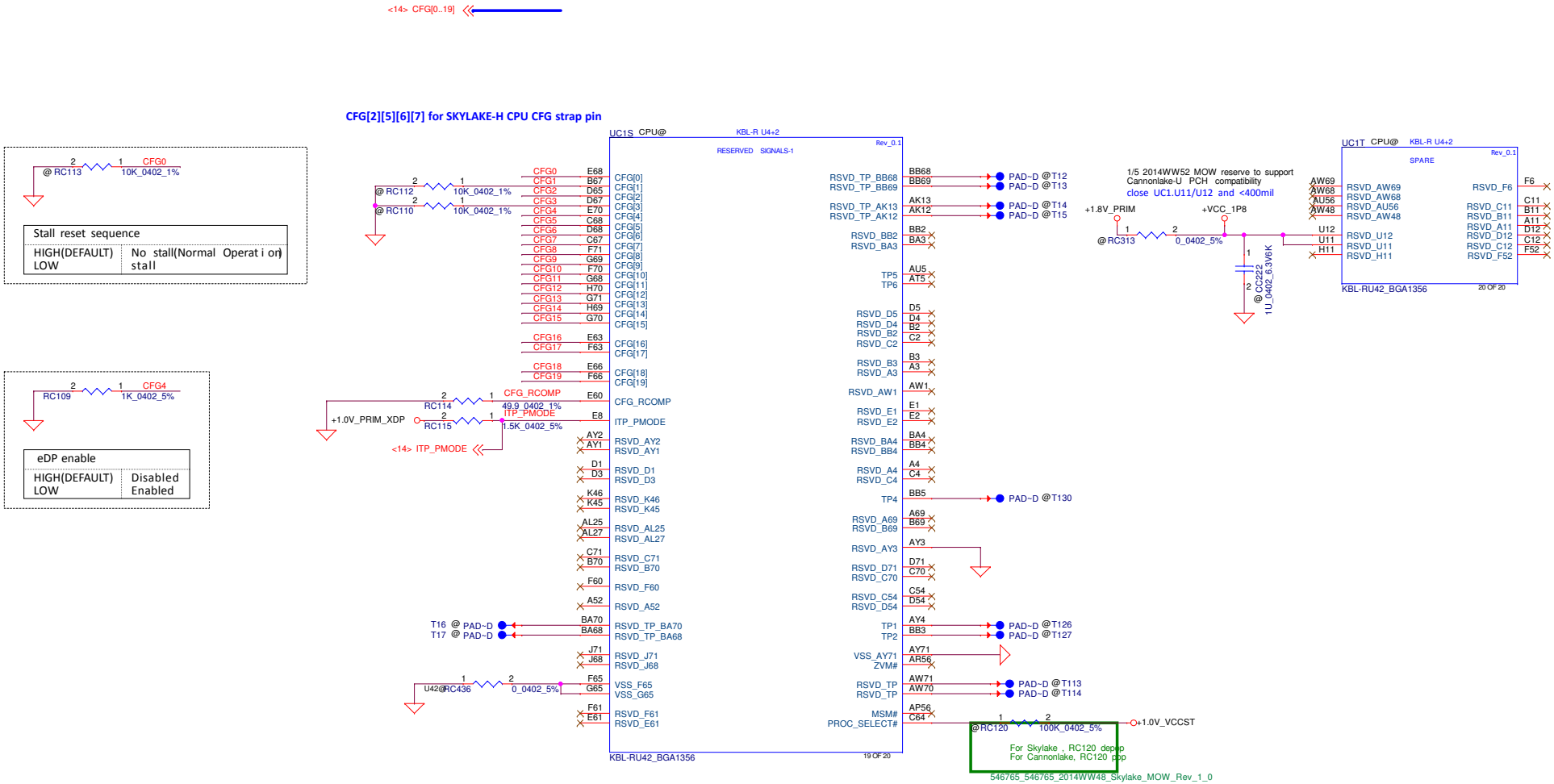
Compal Electronics, Inc.
Title
CPU (7/14)
Size
Document Number
LA-F312P
Rev
2.0
Date: Wednesday, December 20, 2017
Sheet 12 of 58



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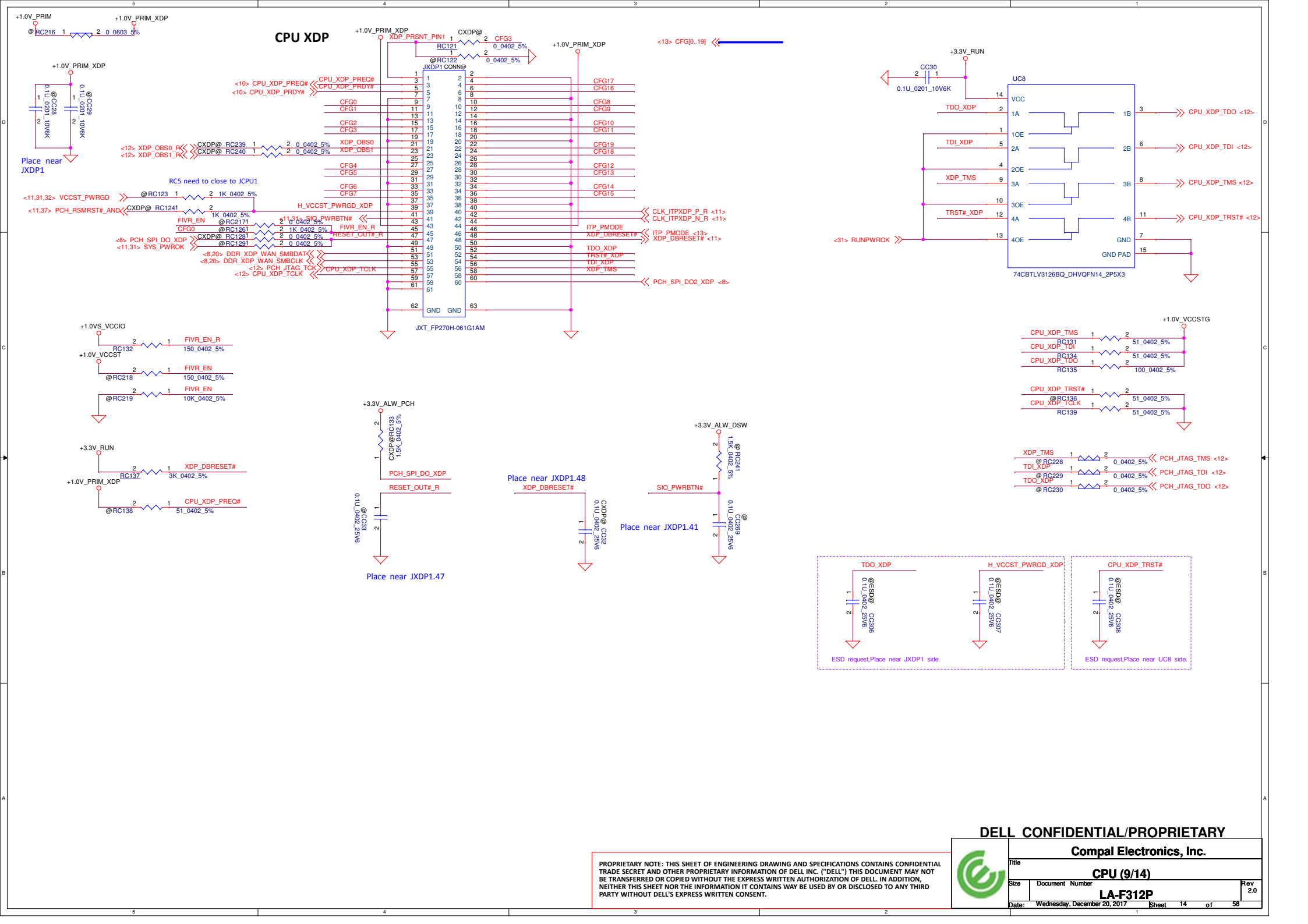
Compal Electronics, Inc.

Title: CPU (8/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 13 of 58



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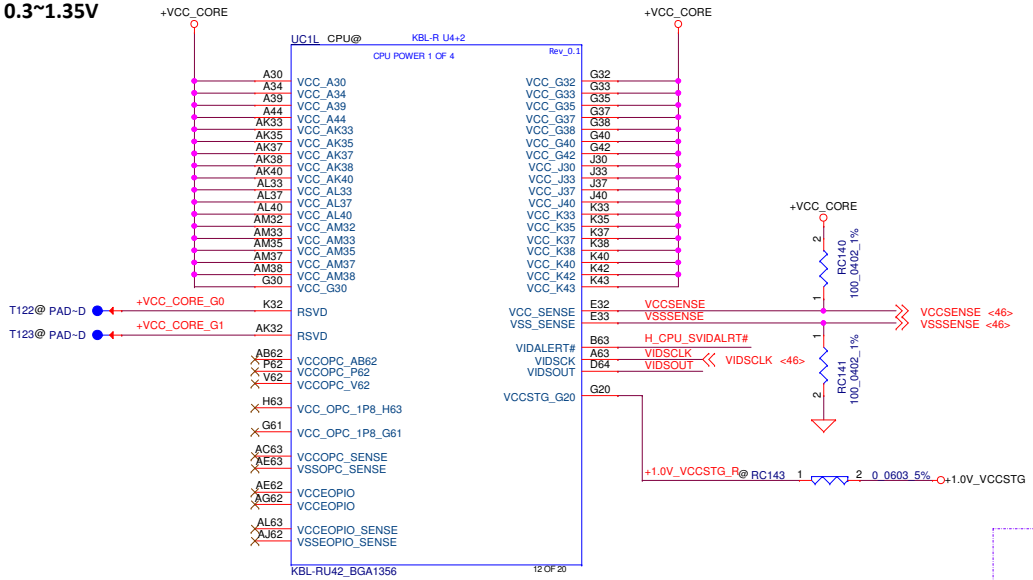
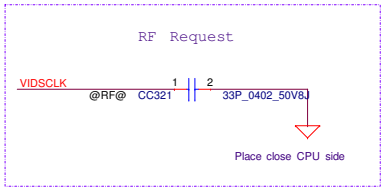
Title	CPU (9/14)
Size	Document Number: LA-F312P
Rev	2.0
Date:	Wednesday, December 20, 2017
Sheet	14 of 58

+VCC_CORE: 0.3~1.35V

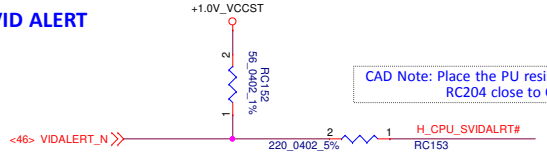


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

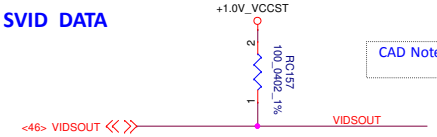


SVID ALERT



CAD Note: Place the PU resistors close to CPU
RC204 close to CPU 300 - 1500mils

SVID DATA



CAD Note: Place the PU resistors close to CPU
RC208close to CPU 300 - 1500mils

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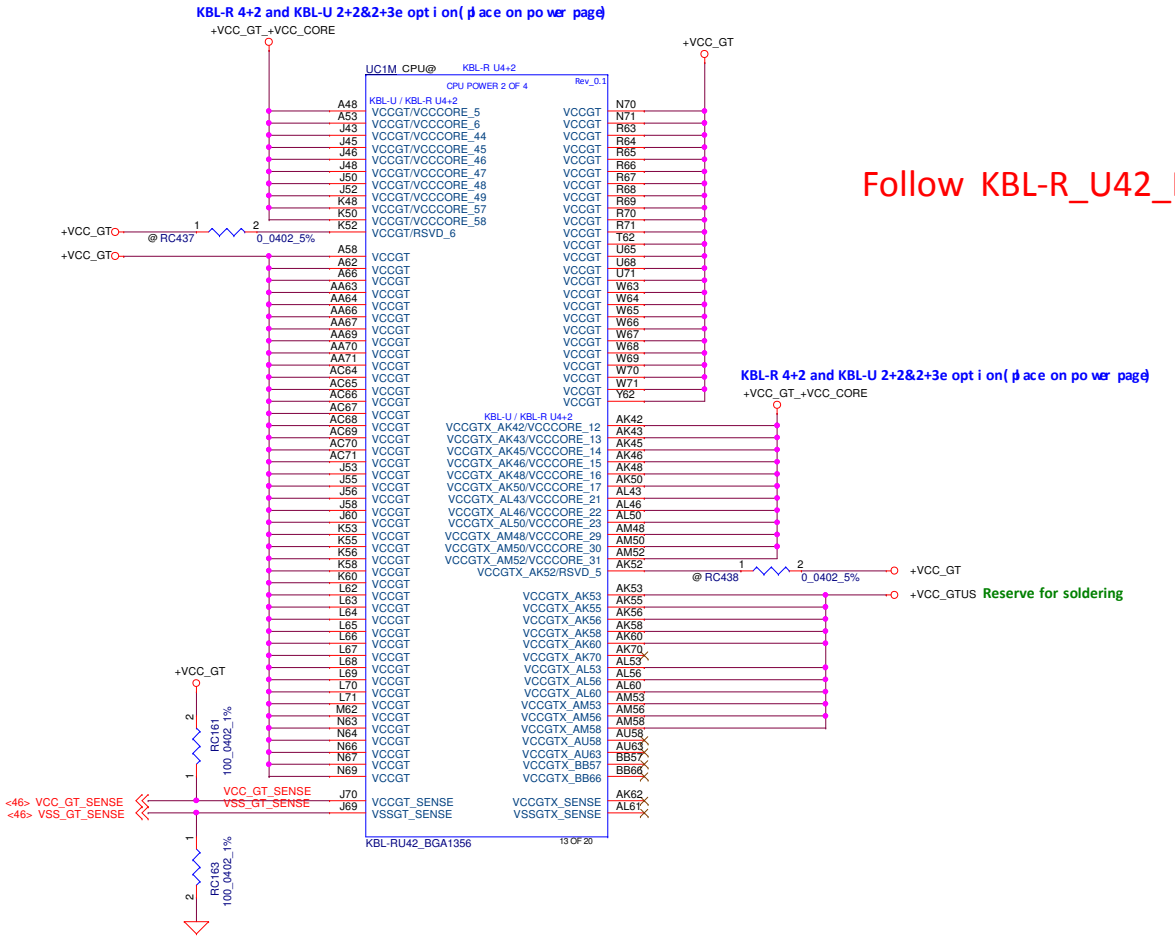
Compal Electronics, Inc.

Title: CPU (10/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 15 of 58

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



Follow KBL-R_U42_Processor_Line_BGA1356_Ballout_Rev1p0

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Title: CPU (11/14)

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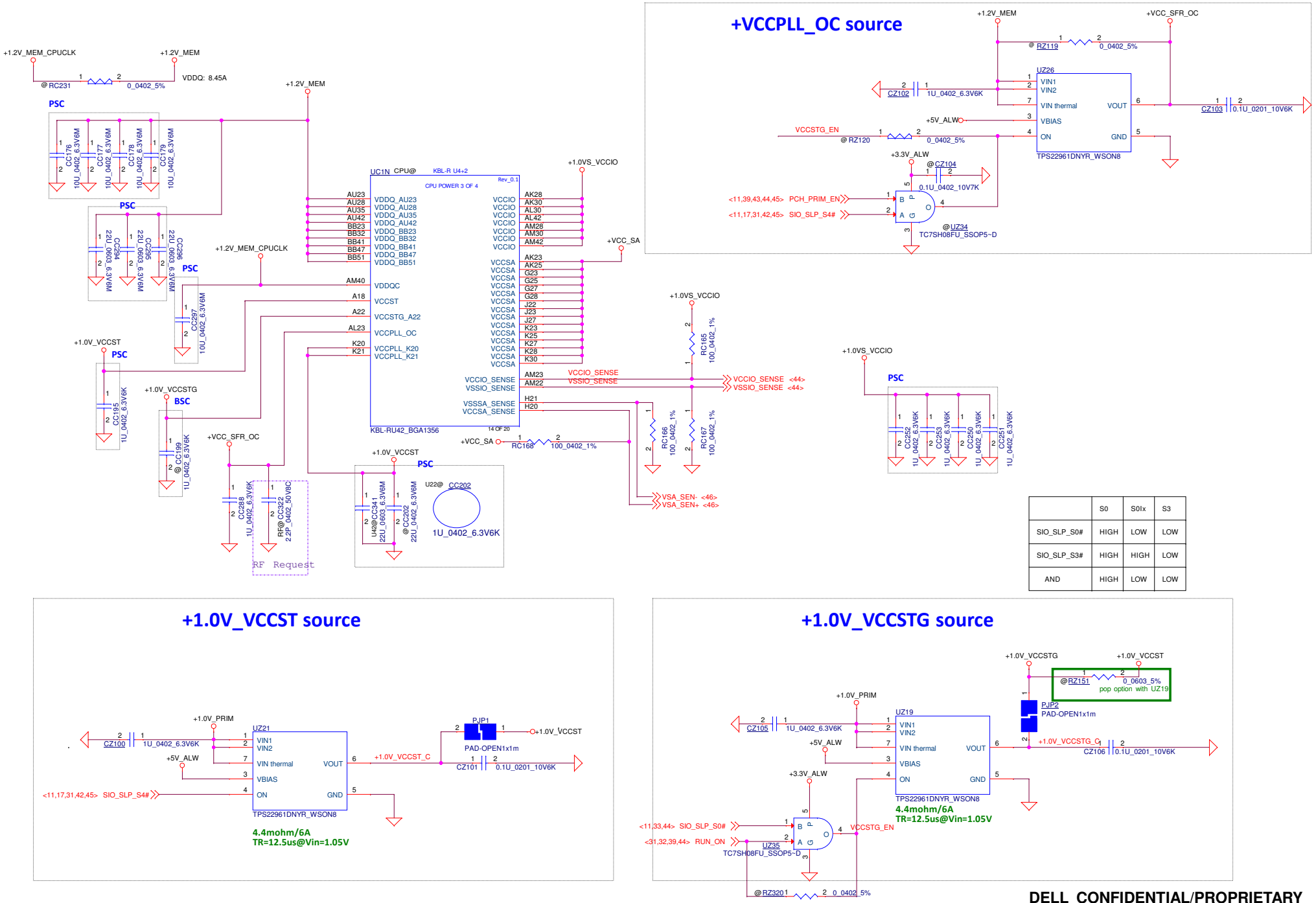
Date: Wednesday, December 20, 2017 | Sheet 16 of 58



	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

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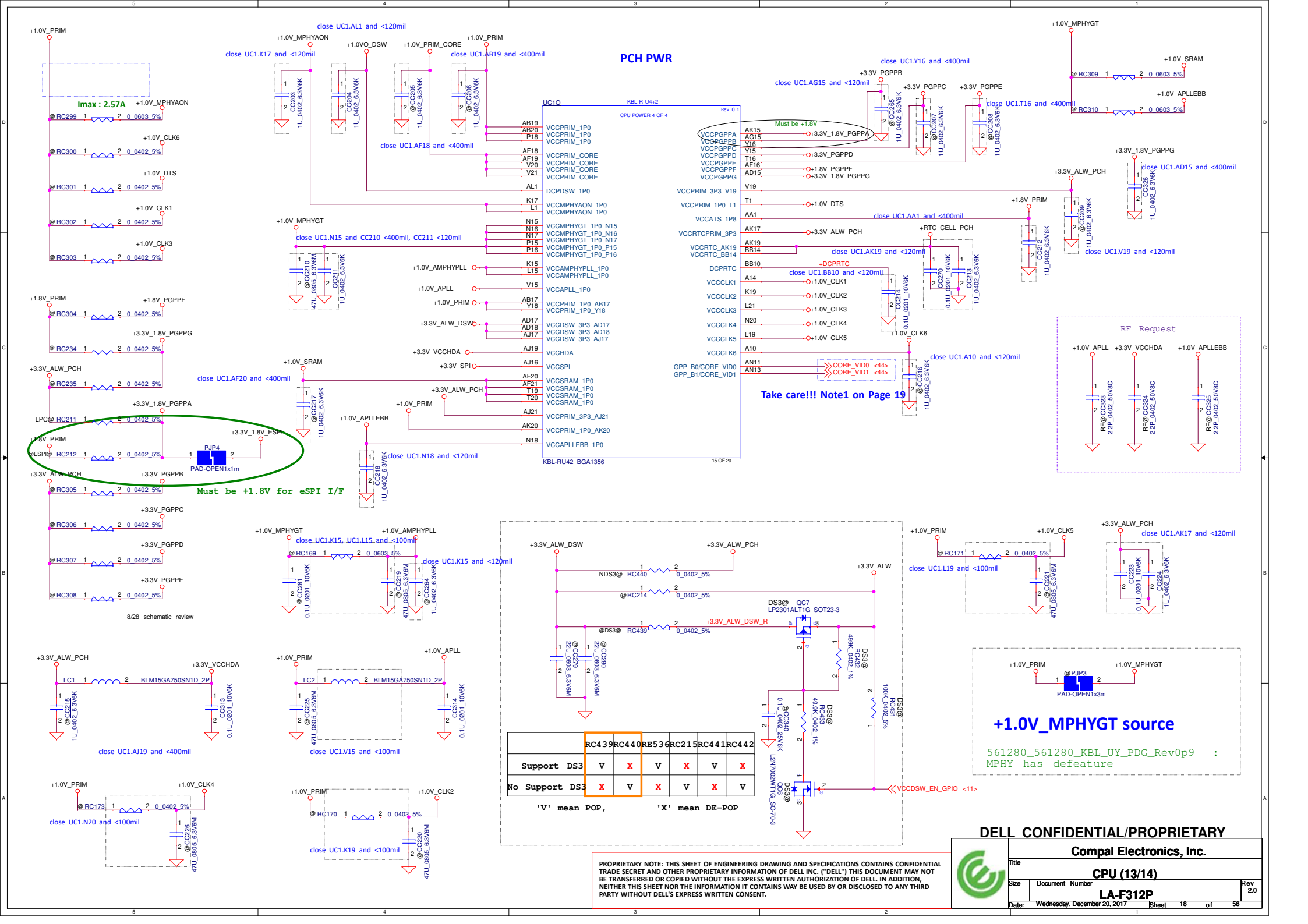
Title: CPU (12/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 17 of 58


PCH PWR
Imax : 2.57A
close UC1.AL1 and <120mil
close UC1.K17 and <120mil
close UC1.AB19 and <400mil
close UC1.AF18 and <400mil
close UC1.Y16 and <400mil
close UC1.AG15 and <120mil
close UC1.T16 and <400mil
close UC1.AD15 and <400mil
close UC1.AA1 and <400mil
close UC1.V19 and <120mil
close UC1.AK19 and <120mil
close UC1.BB10 and <120mil
close UC1.A10 and <120mil
close UC1.N15 and CC210 <400mil, CC211 <120mil
close UC1.AF20 and <400mil
close UC1.N18 and <120mil
close UC1.K15, UC1.L15 and <100mil
close UC1.K15 and <120mil
close UC1.L19 and <100mil
close UC1.AK17 and <120mil
close UC1.AJ19 and <400mil
close UC1.V15 and <100mil
close UC1.N20 and <100mil
close UC1.K19 and <100mil
Must be +1.8V
Must be +1.8V for eSPI I/F
Take care!!! Note1 on Page 19
RF Request
8/28 schematic review
+1.0V_MPHYGT source
561280_561280_KBL_UY_PDG_Rev0p9 : MPHY has defeature
'V' mean POP, 'X' mean DE-POP
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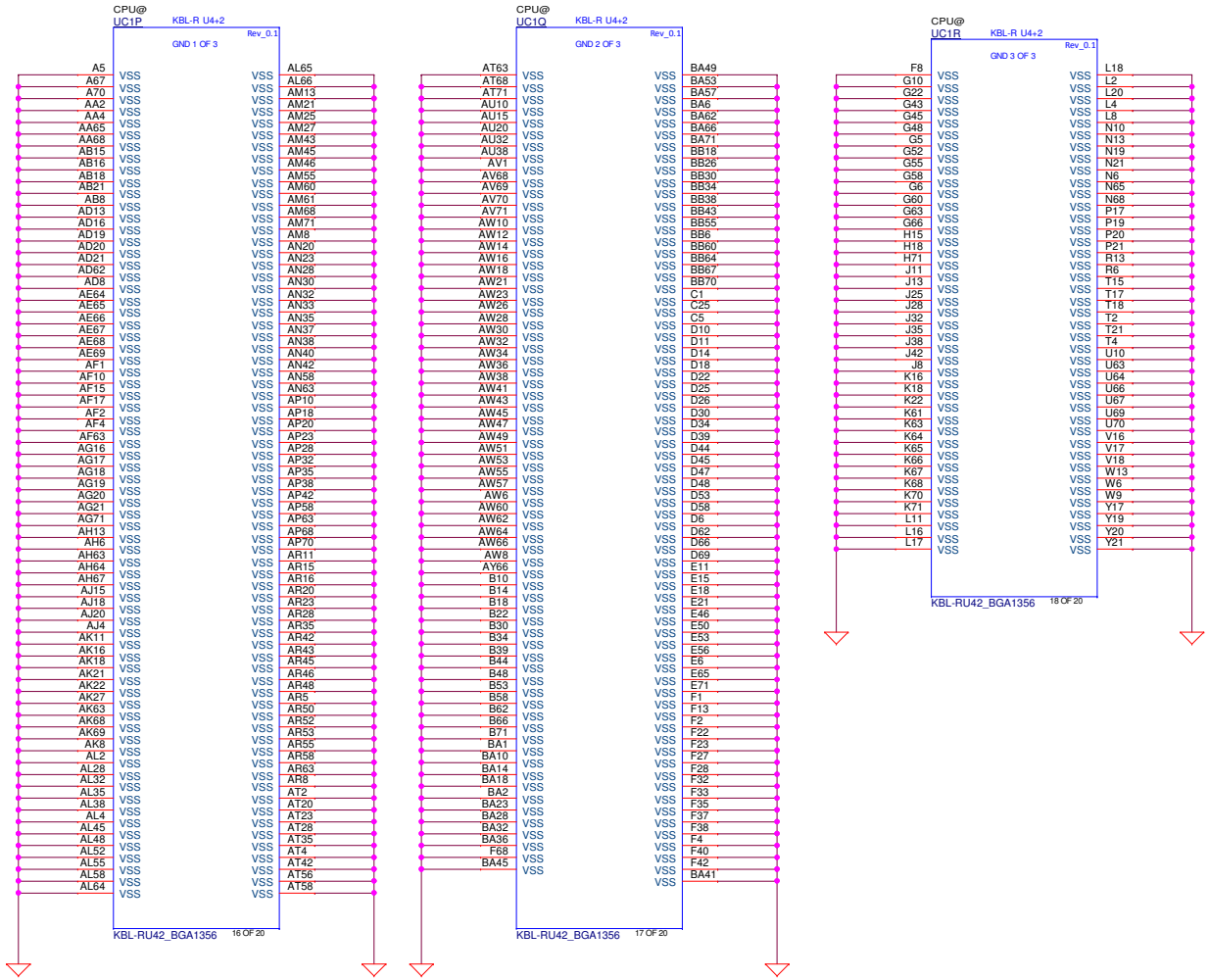
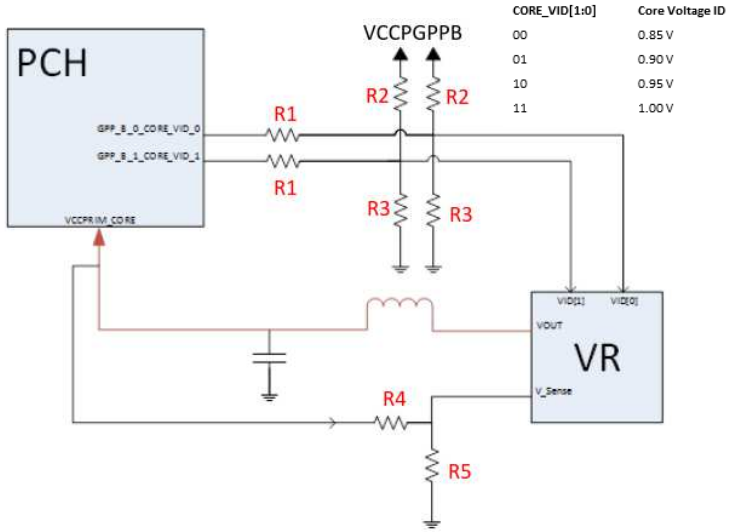
Compal Electronics, Inc.
CPU (13/14)
LA-F312P
Rev 2.0
Wednesday, December 20, 2017
Sheet 18 of 58



Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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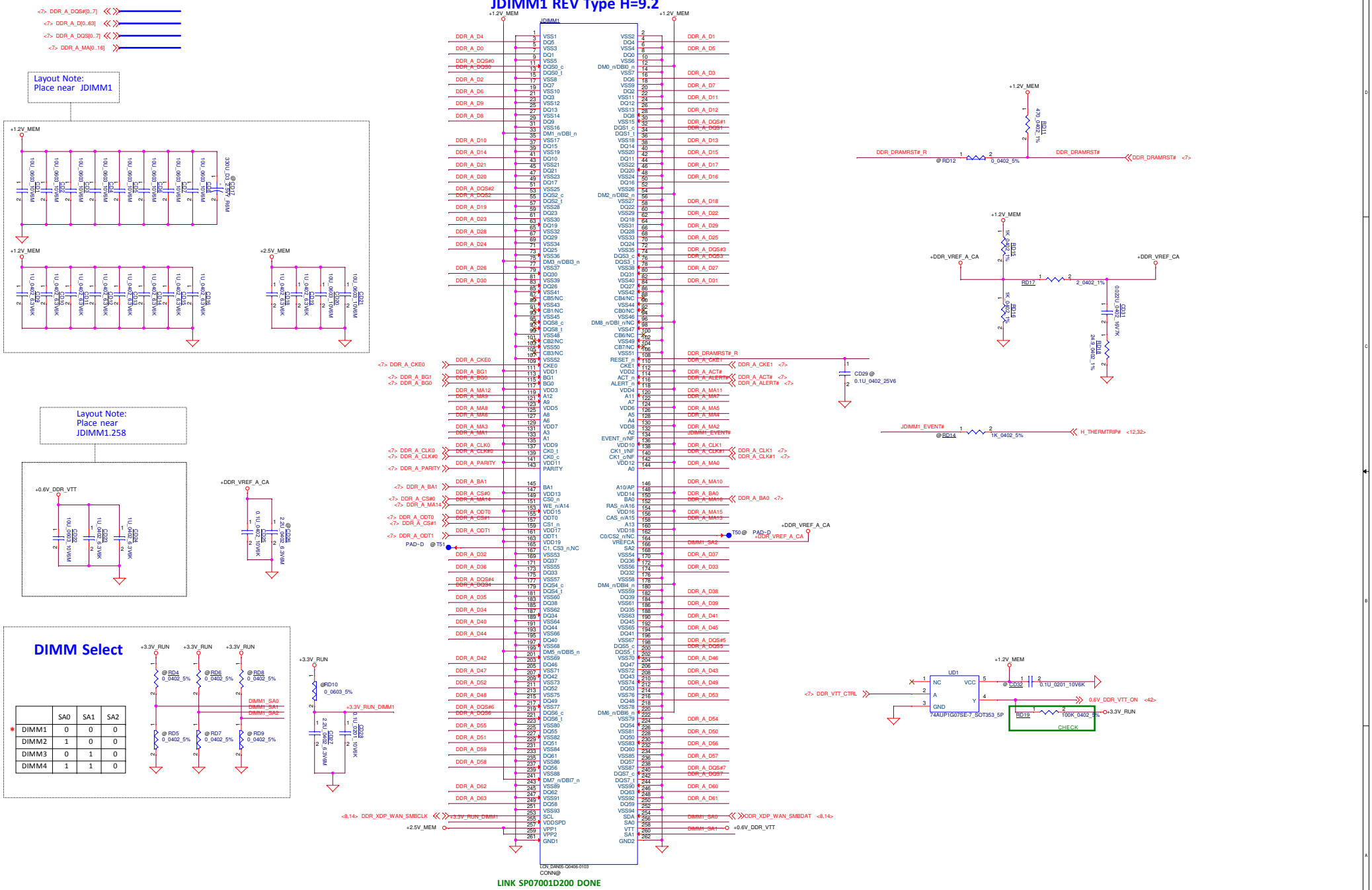
Title: CPU (14/14)

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 19 of 58

For DDR4

JDIMM1 REV Type H=9.2



Layout Note:
Place near JDIMM1

Layout Note:
Place near
JDIMM1.258

DIMM Select

	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

LINK SP07001D200 DONE

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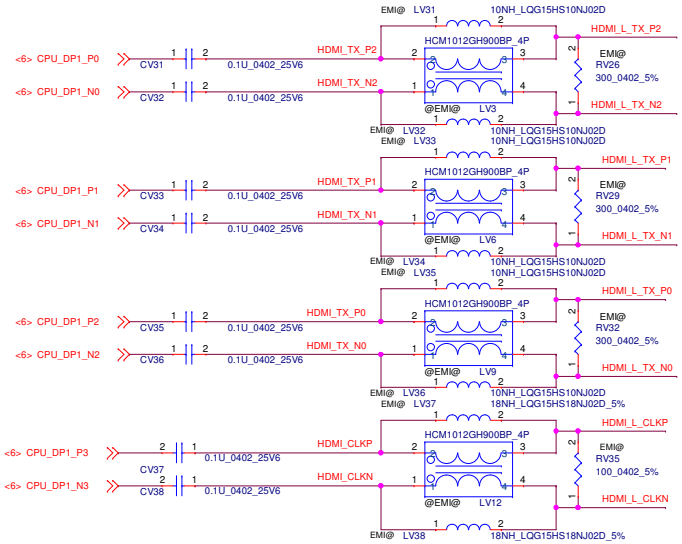
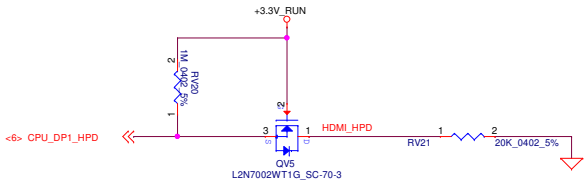
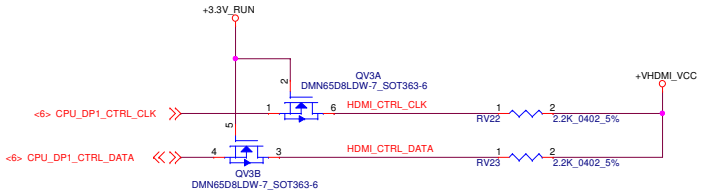
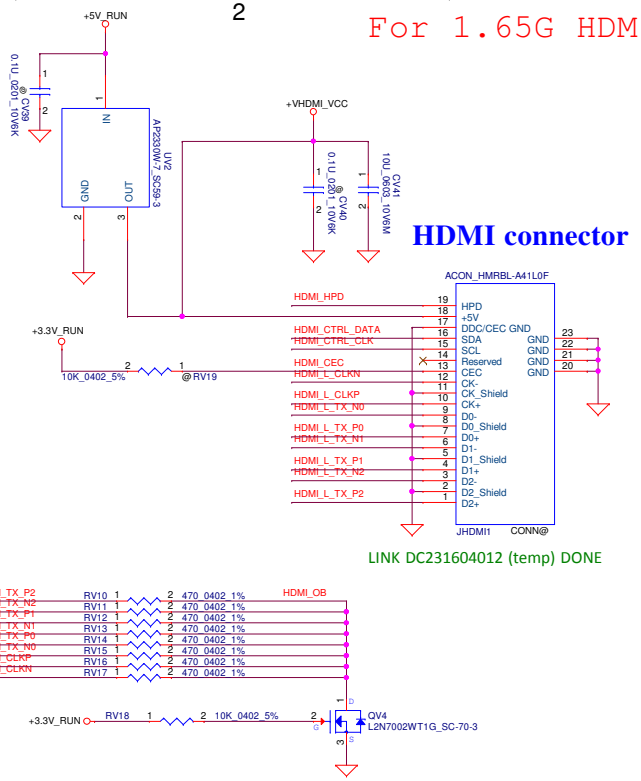
Compal Electronics, Inc.	
Title	DDR4
Size / Document Number	LA-F312P
Rev	2.0
Date: Wednesday, December 20, 2017	Sheet 20 of 58

For 1.65G HDMI from CPU









LINK DC231604012 (temp) DONE

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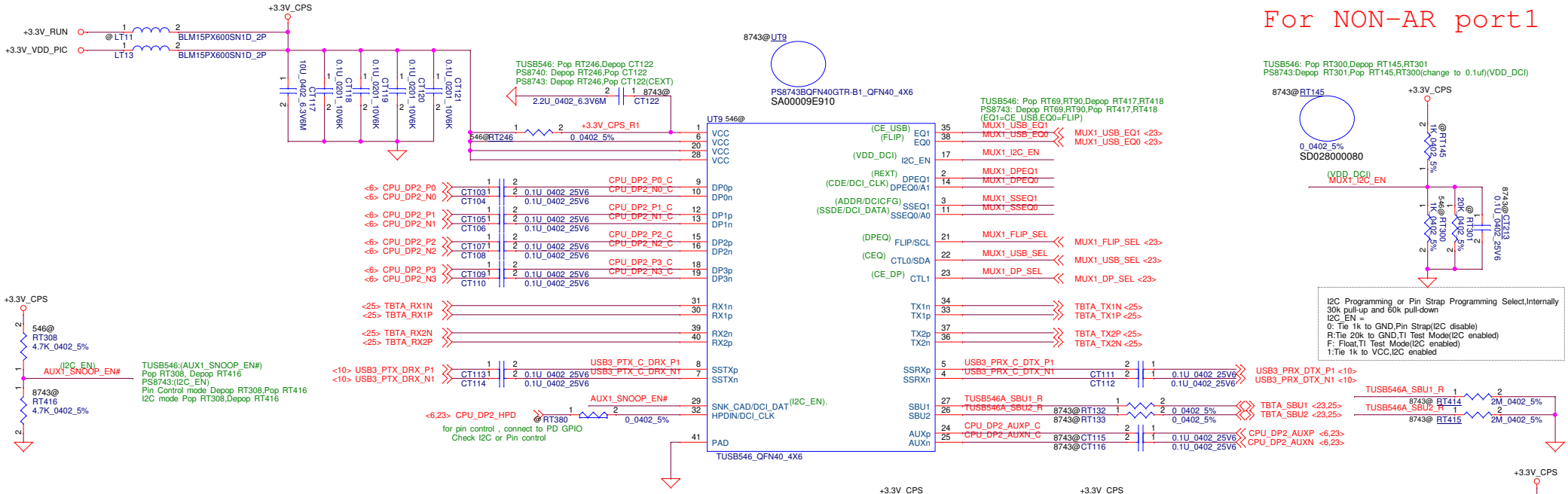
Compal Electronics, Inc.

Title: HDMI CONN

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 21 of 58

For NON-AR port1



PS8743 Mode Selection			
CE_DP	CE_USB	FLIP	
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	USB only on SS1 channels
L	H	H	USB only on SS2 channels
H	L	L	DP only; ML0 on SSRX2
H	L	H	DP only; ML0 on SSRX1
H	H	L	USB+2lanes DP;DP ML0 on SSRX2
H	H	H	USB+2lanes DP;DP ML0 on SSRX1

Table 7. TUSB546-DCI Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	0.2	0	0	-1.6	0	0	1.0
1	0	R	1.2	0	R	-0.5	0	R	3.3
2	0	F	2.2	0	F	0.5	0	F	4.9
3	0	1	3.3	0	1	1.6	0	1	6.5
4	R	0	4.2	R	0	2.4	R	0	7.5
5	R	R	5.1	R	R	3.4	R	R	8.6
6	R	F	5.9	R	F	4.1	R	F	9.5
7	R	1	6.7	R	1	4.9	R	1	10.4
8	F	0	7.4	F	0	5.7	F	0	11.1
9	F	R	8.1	F	R	6.4	F	R	11.7
10	F	F	8.7	F	F	6.9	F	F	12.3
11	F	1	9.3	F	1	7.5	F	1	12.8
12	1	0	9.7	1	0	8.0	1	0	13.2
13	1	R	10.2	1	R	8.5	1	R	13.6
14	1	F	10.6	1	F	8.9	1	F	14.0
15	1	1	11.1	1	1	9.4	1	1	14.4

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Compal Electronics, Inc.

Title: DP/USB3 Repeater SW TUSB546

Size: Document Number: LA-F312P

Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 22 of 58

For NON-AR port1

DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max/" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max/" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Need Link TPS65982D

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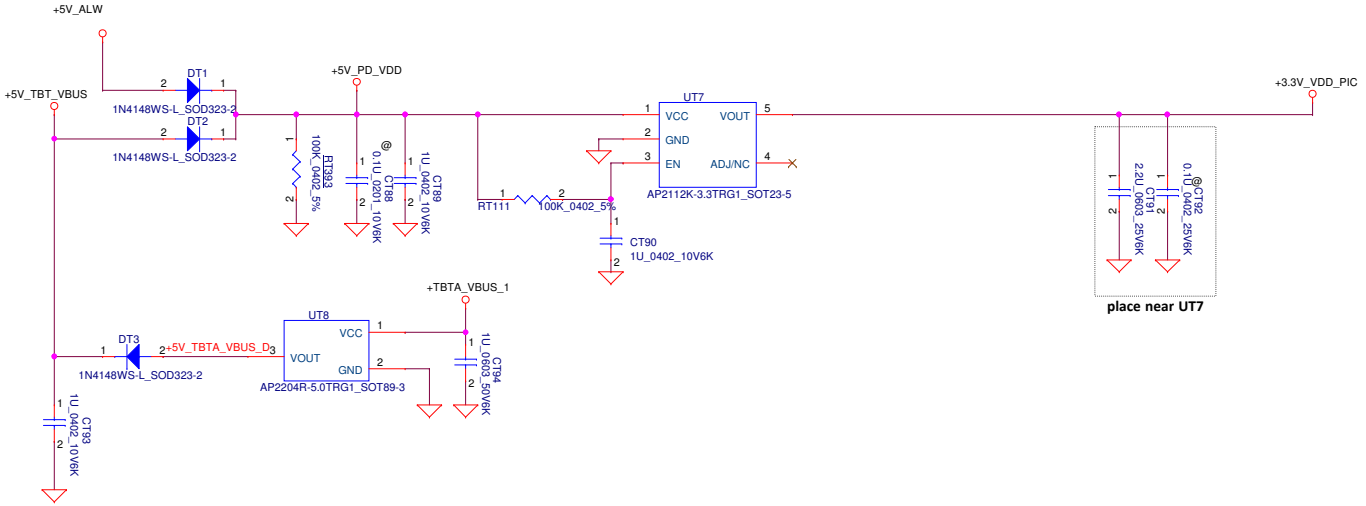
Title: [Type C]PD Controller TI

Size: | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 23 of 58



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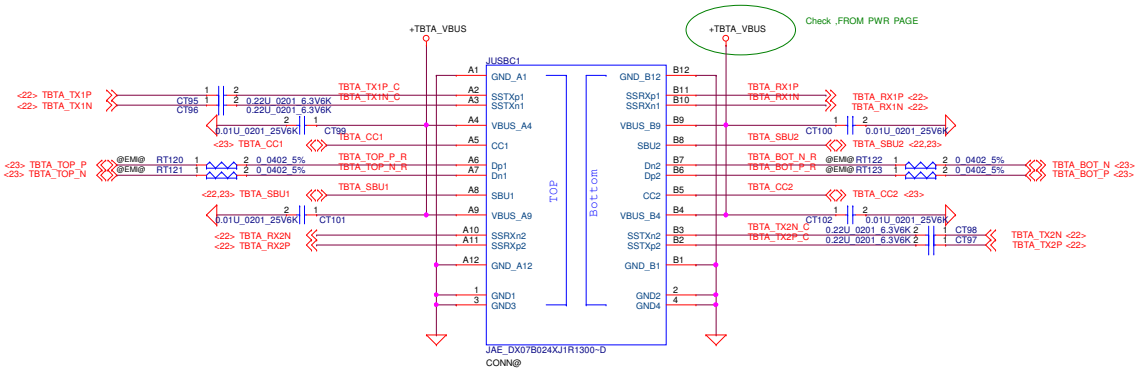
Compal Electronics, Inc.

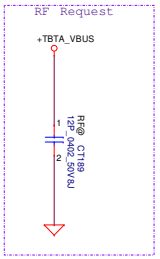
Title: [Type C]PD Power

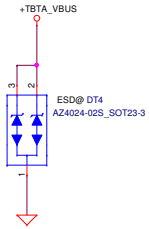
Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 24 of 58

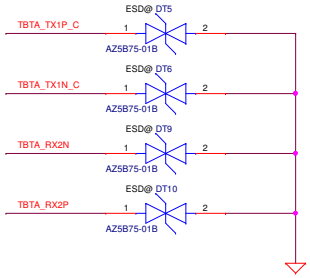
For NON AR Config

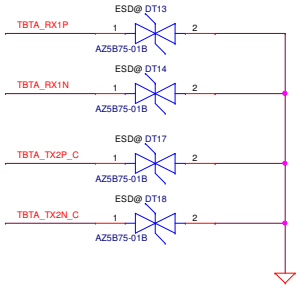


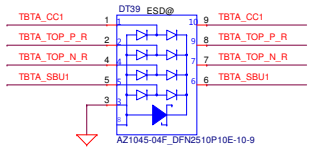


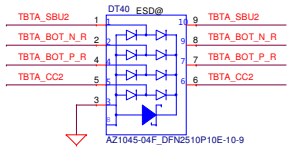


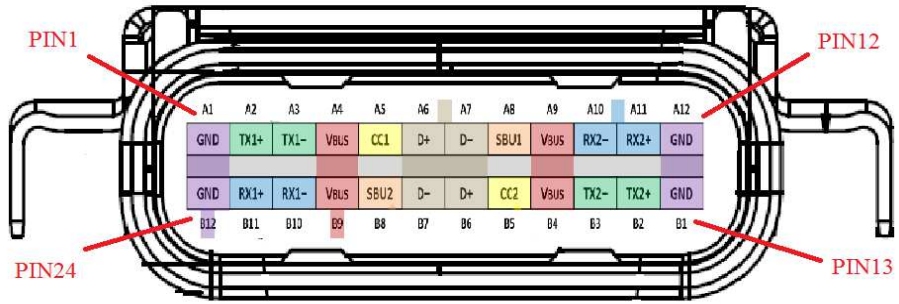
Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done











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Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 25 of 58

LINK 50398-04041-001 DONE

For 2LANE EDP &3.3V_TSP
For Breckenridge&Steamboat 12

JEDP1
ACES_50398-04041-001
CONN@

TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events

EXC24CQ900U_4P
LV27 EMI@

ESD depop location

EMI Request

RF Request

Reserve for EA

Due to SB12/14 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table

CONN@ JIR1
E-T_4251K-F06N-40L

For Touchscreen

LCDVDD POWER

WebCAM

Backlight POWER

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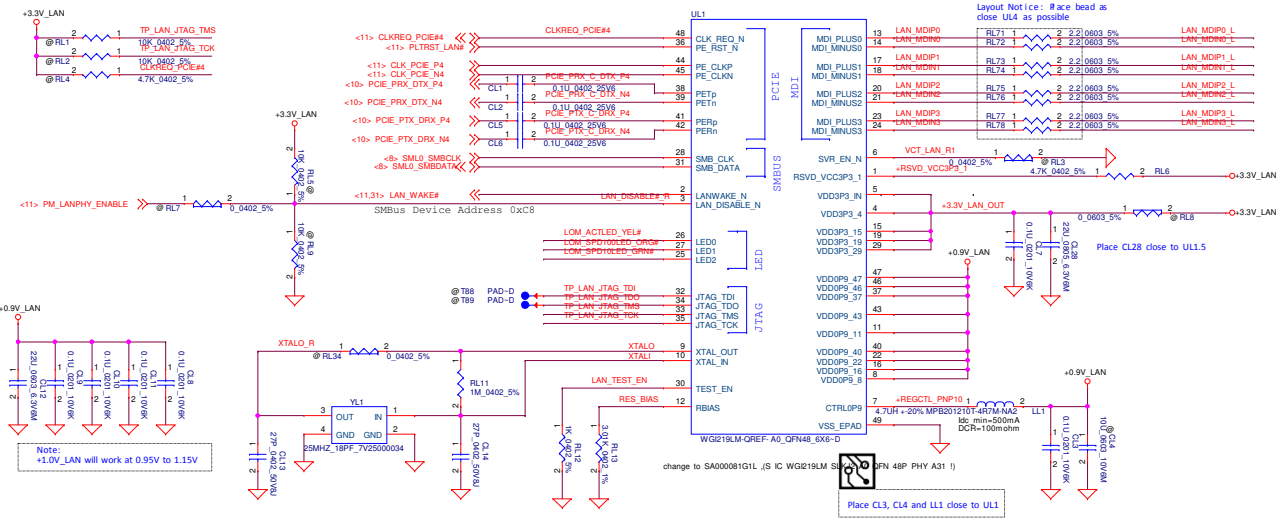
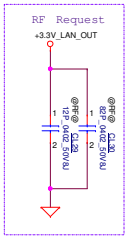
Compal Electronics, Inc.

Title: eDP CONN & Touch screen

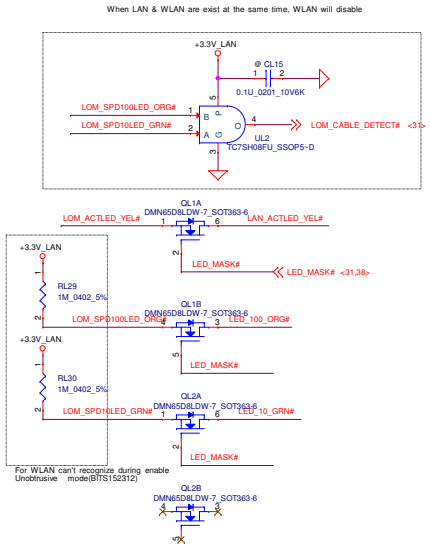
Size | Document Number: LA-F312P | Rev: 2.0

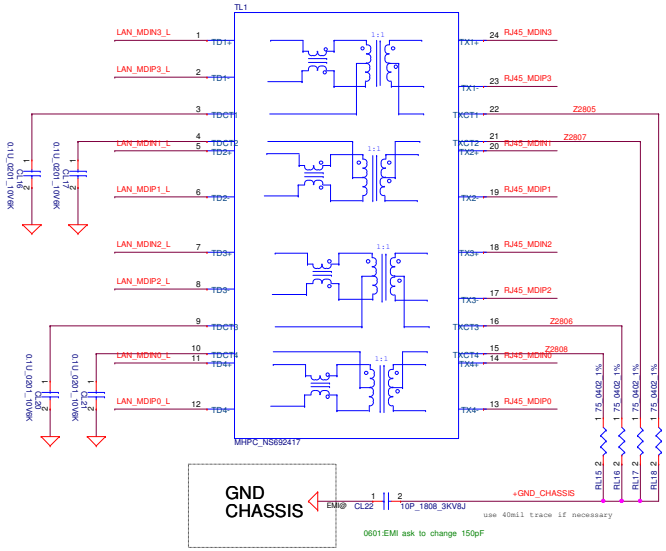
Date: Wednesday, December 20, 2017 | Sheet 26 of 58





Link DC231603220 (temp) DONE





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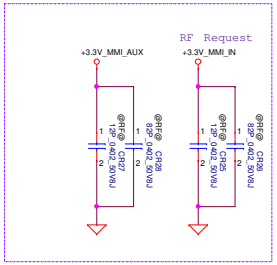
Compal Electronics, Inc.

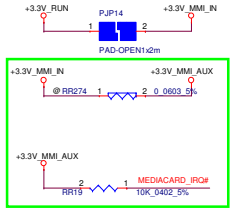
Title: LAN Clarkvillie & RJ45

Size: | Document Number: LA-F312P | Rev: 2.0

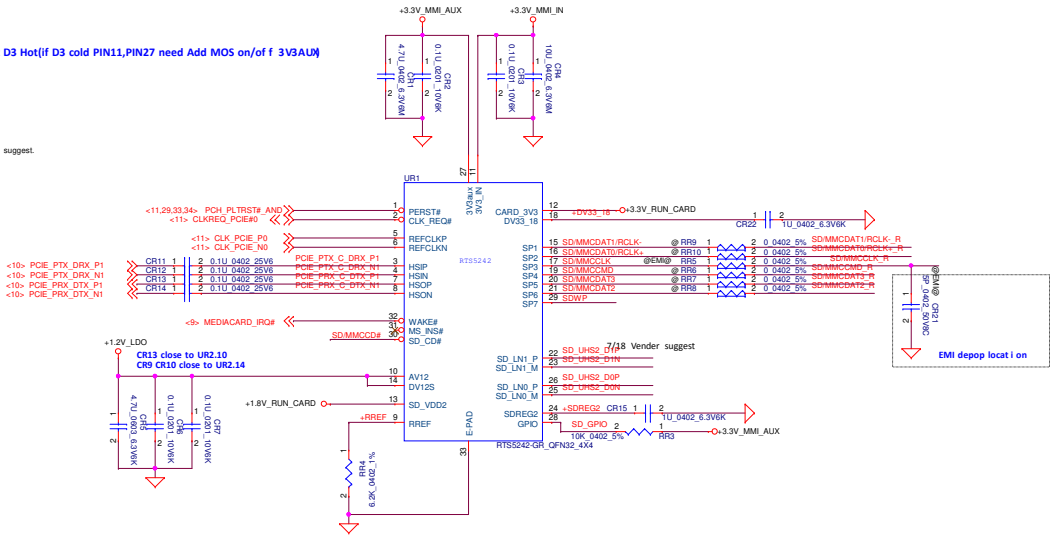
Date: Wednesday, December 20, 2017 | Sheet 27 of 58

For PCIE Interface

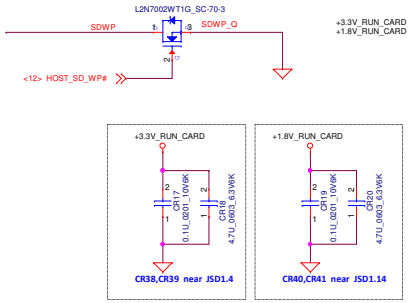


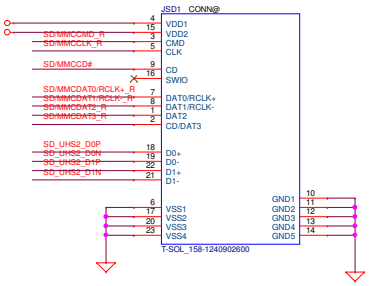


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX)



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	Low	Low	Write Enable
Low	Low	High	Write Protect(FW LOCK)





LINK SP071603151 (temp) DONE

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Compal Electronics, Inc.

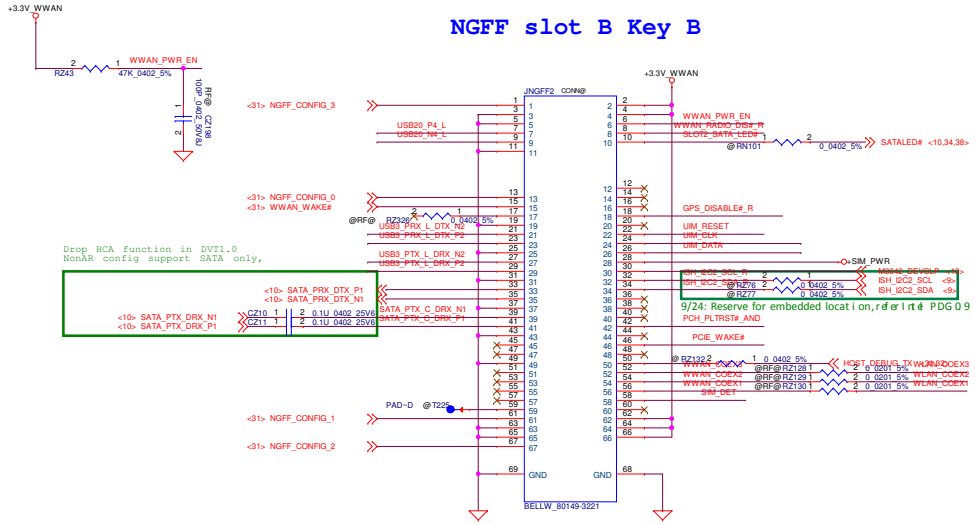
Title: Card Reader RTS5242

Size: Document Number: LA-F312P Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 28 of 58

for no AR,Brekenridge 12/14/15 UMA/Steamboat

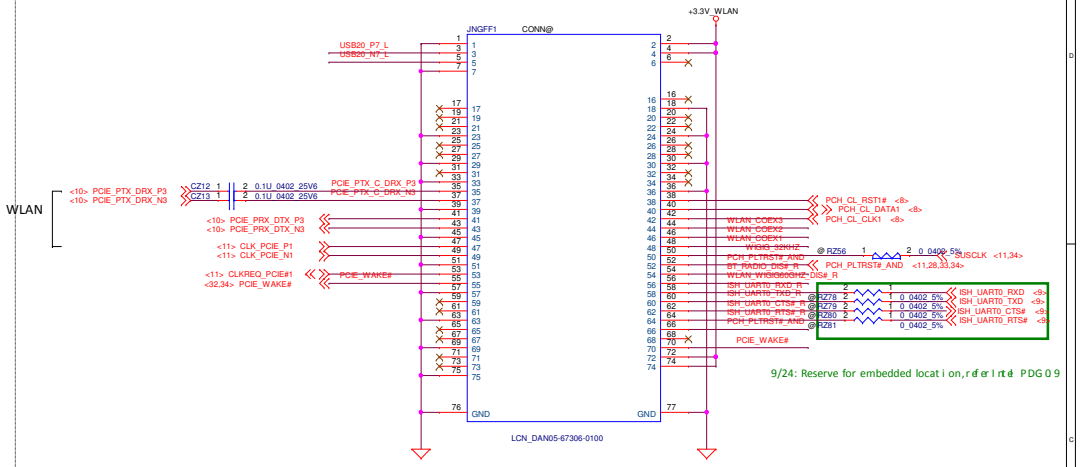
NGFF slot B Key B



9/24: Reserve for embedded locat i on,r e f e r l n t e d P D G 0 9

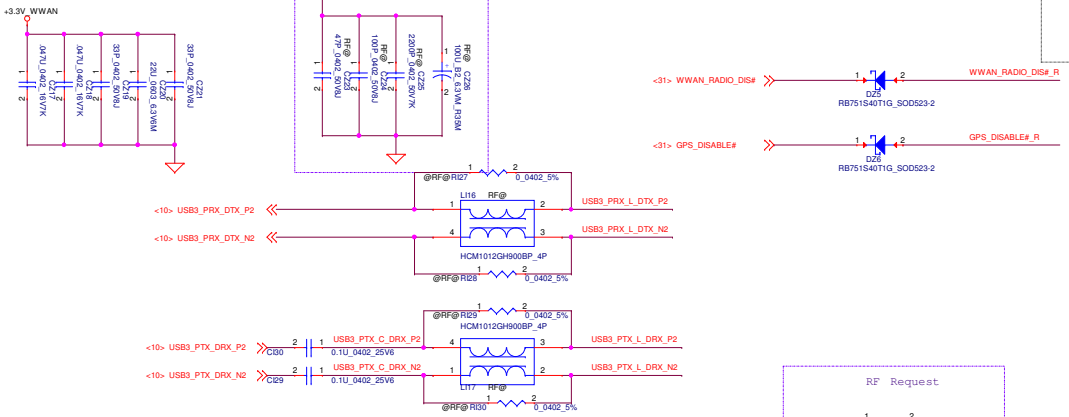
80149-3221 LINK DONE

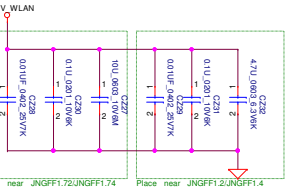
NGFF slot A Key A



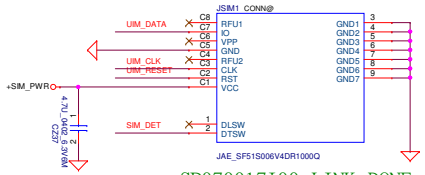
9/24: Reserve for embedded locat i on,r e f e r l n t e d P D G 0 9

SP070019F00 LINK DONE

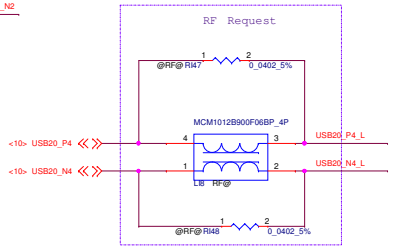


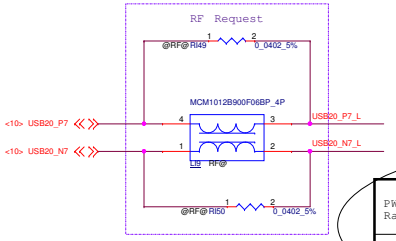


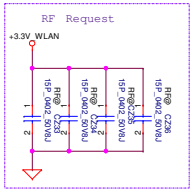
SIM Card Push-Push

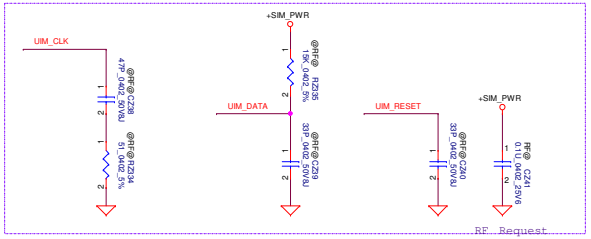


SP070017I00 LINK DONE









STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

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Compal Electronics, Inc.

Title: NGFF Card

Size: Document Number: LA-F312P Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 29 of 58

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

Link SP02001CE00 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 13.

Add for solve pop noise and detect issue

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

Normal

Open

Only BR15U UMA use LA2,LA3,because 6L

Link DC23000DG10 DONE

RF Request

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.			
Title: Codec ALC3246			
Size: C	Document Number: LA-F312P		Rev: 2.0
Date: Wednesday, December 20, 2017		Sheet 30 of 58	

	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

For EVT/DVT1.0 Only,SA00009GL10, S IC MEC5105K-TMP2-TN WFBGA 169P EC
After DVT1.1,SA00009GL00, S IC MEC5105K-D1-TN WFBGA 169P EC

For SB

Deep Sleep support	
non Deep Sleep	1
Deep Sleep	0

	VGA_IDENTIFY
Discrete	0
UMA	1

32 KHz Clock

For EMI request

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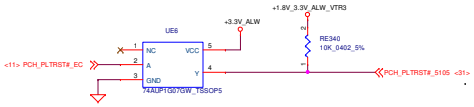
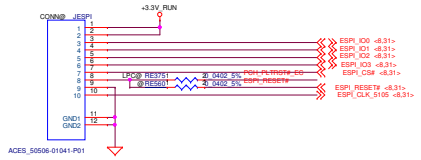
Compal Electronics, Inc.

Title: EC MEC5105

Size: Document Number: LA-F312P Rev: 2.0

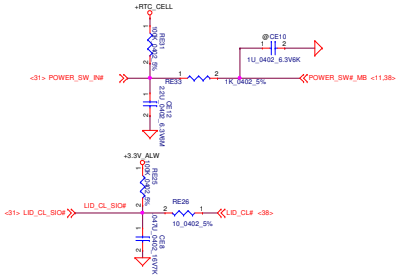
Date: Wednesday, December 20, 2017 Sheet 31 of 58

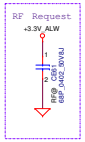


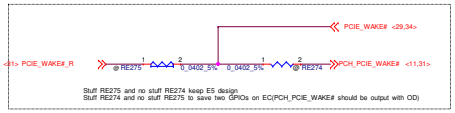


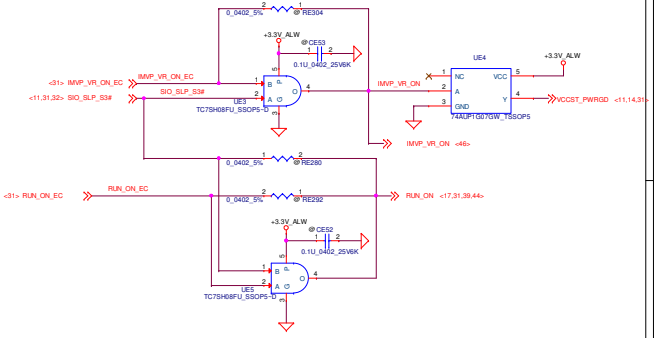
PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

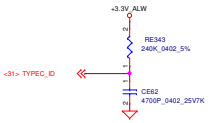
LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK





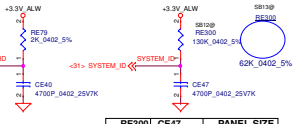






RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

PD_ACE_DET# rise time measured from 5%~68%

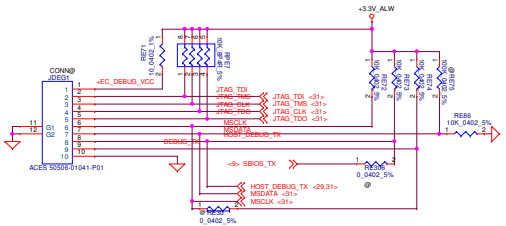


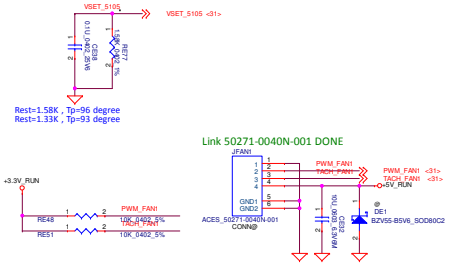
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
* 2K	4700p	A01
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	11"
* 130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	

BOARD_ID rise time measured from 5%~68%

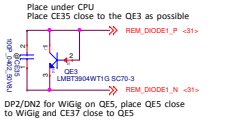
SYSTEM_ID rise time measured from 5%~68%

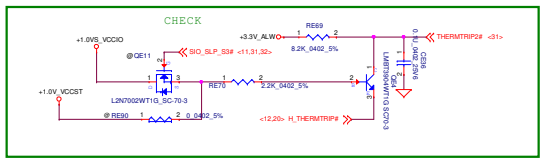


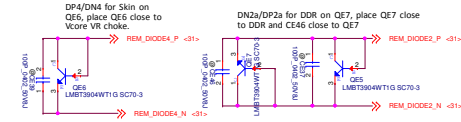


Thermal diode mapping

5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)







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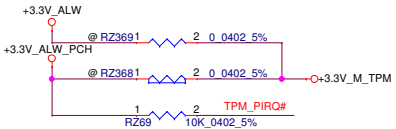
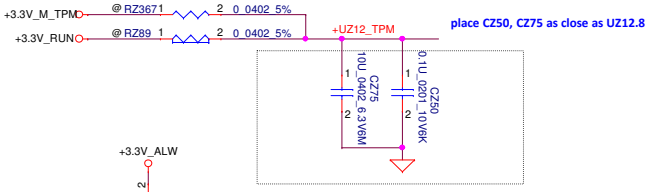
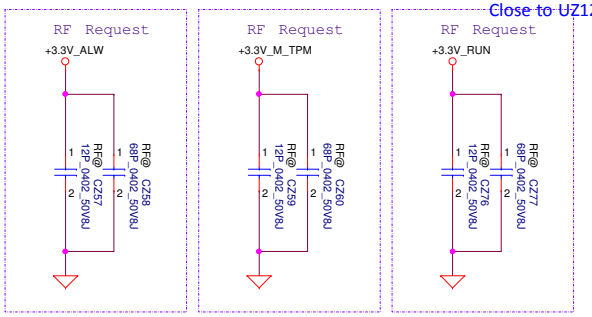
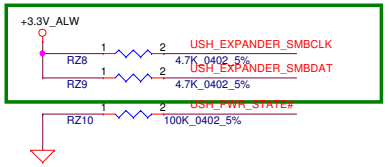
For NUVOTON TPM



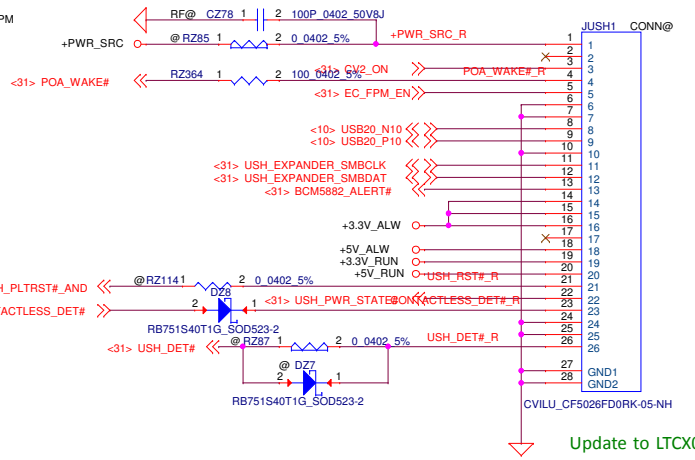


place CZ50, CZ75 as close as UZ12.8

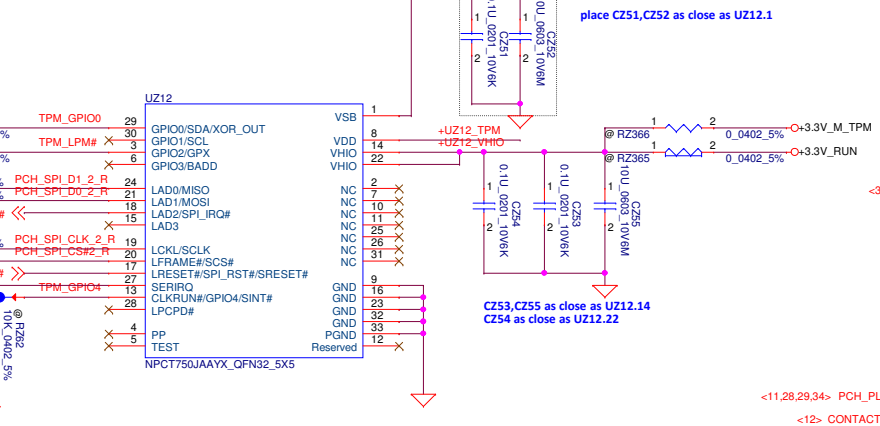




USH CONN



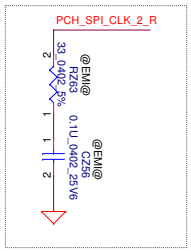
Update to LTCX007Q600 (DVT1.0)

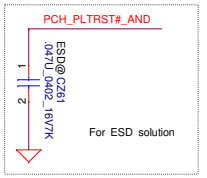


place CZ51,CZ52 as close as UZ12.1

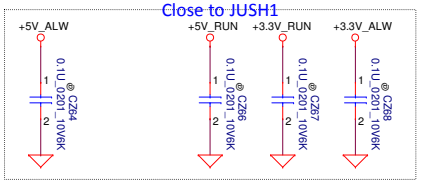
CZ53,CZ55 as close as UZ12.14
CZ54 as close as UZ12.22

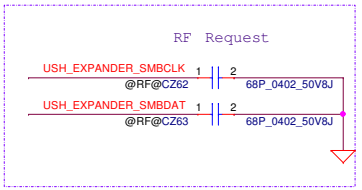
	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V_RUN Power VHIO - V_SPI Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V_RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V_SPI power

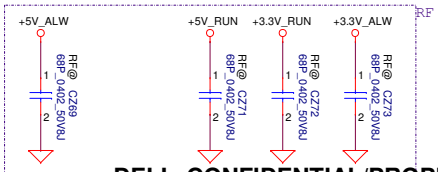




Close to JUSH1







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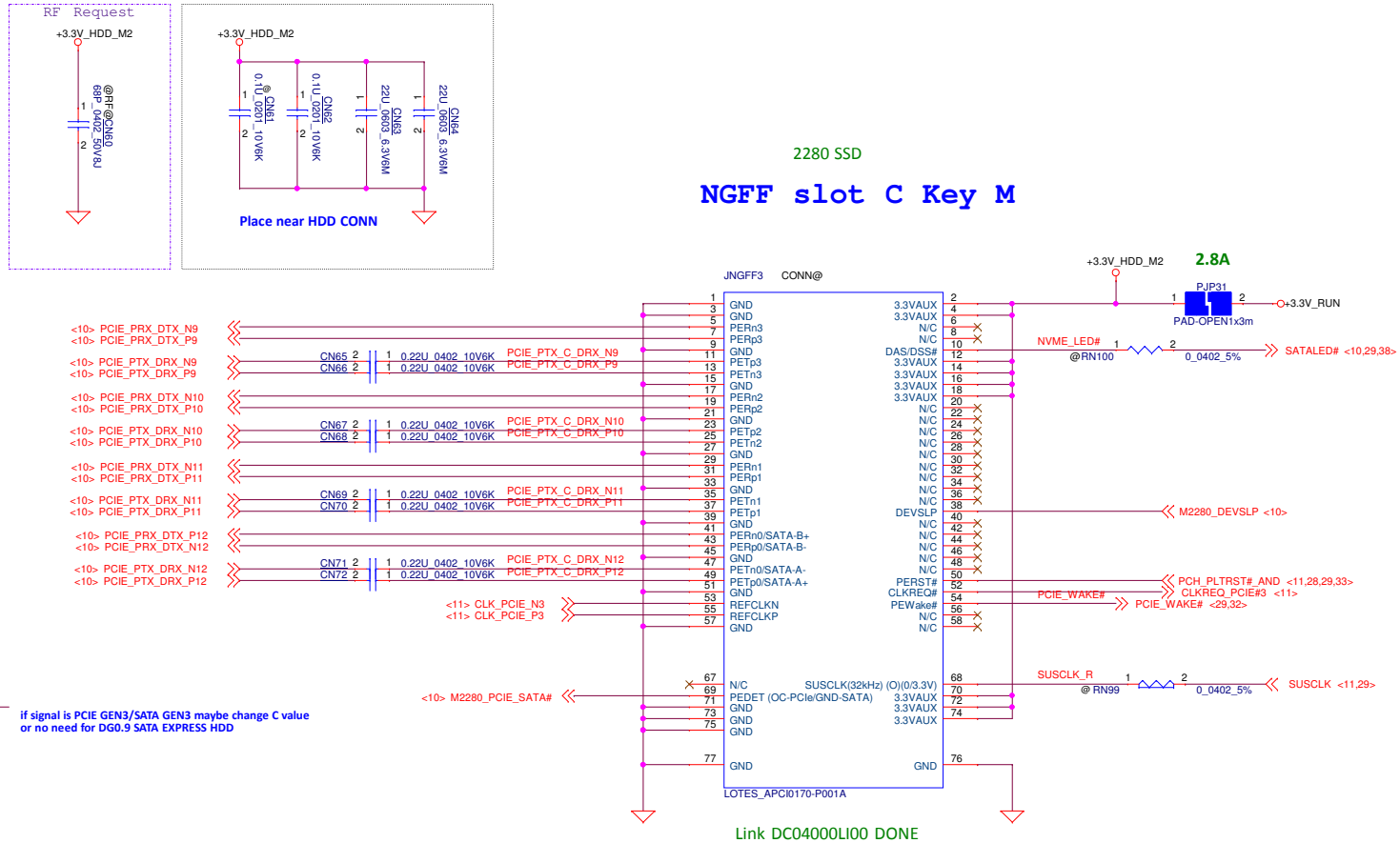
Title: USH & TPM

Size: | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 33 of 58



Link DC04000LI00 DONE

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Compal Electronics, Inc.

Title: M2 2280 Socket

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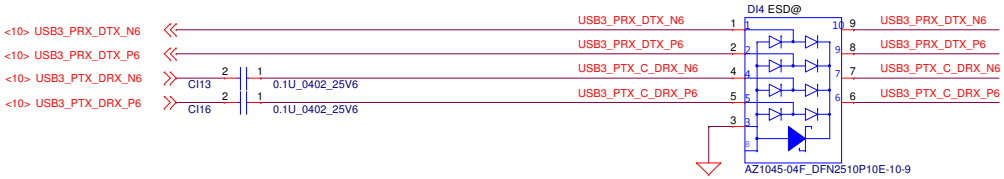
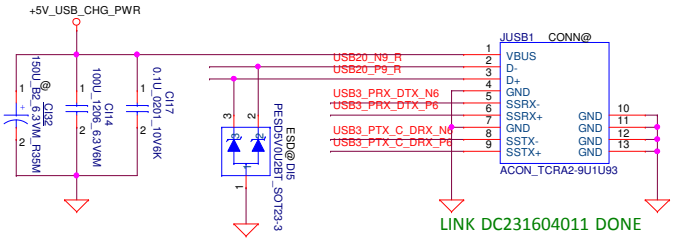
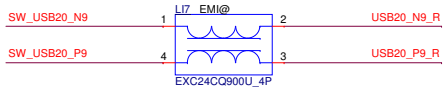
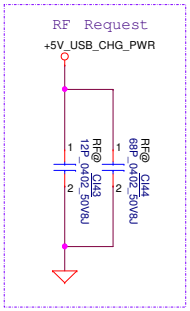
Date: Wednesday, December 20, 2017 | Sheet 34 of 58

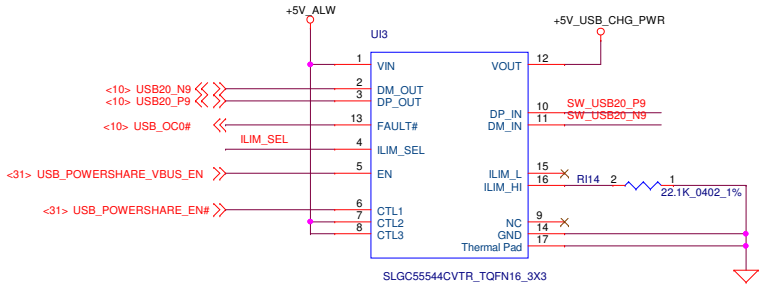




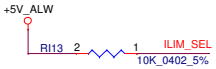
LINK DC231604011 DONE

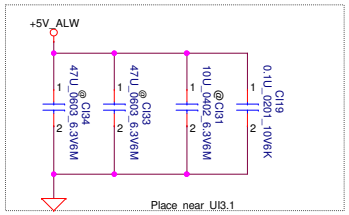






SA000097E10 Link Done





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Compal Electronics, Inc.

Title: JUSB1+PS

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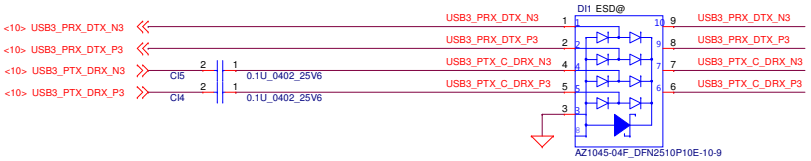
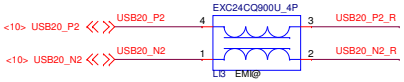
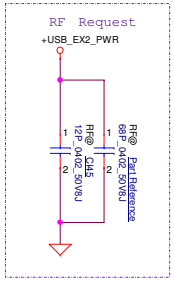
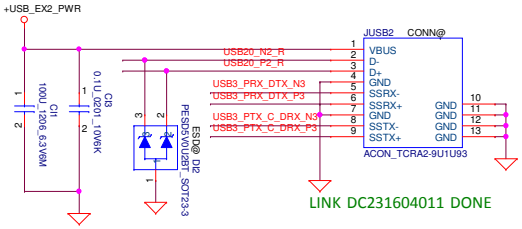
Date: Wednesday, December 20, 2017 | Sheet 35 of 58



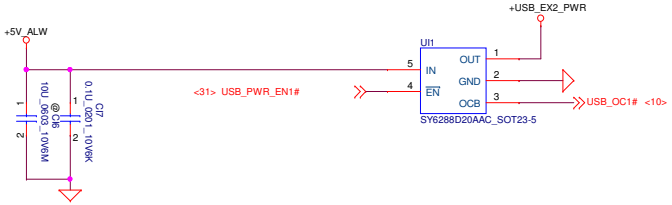


DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm





LINK DC231604011 DONE



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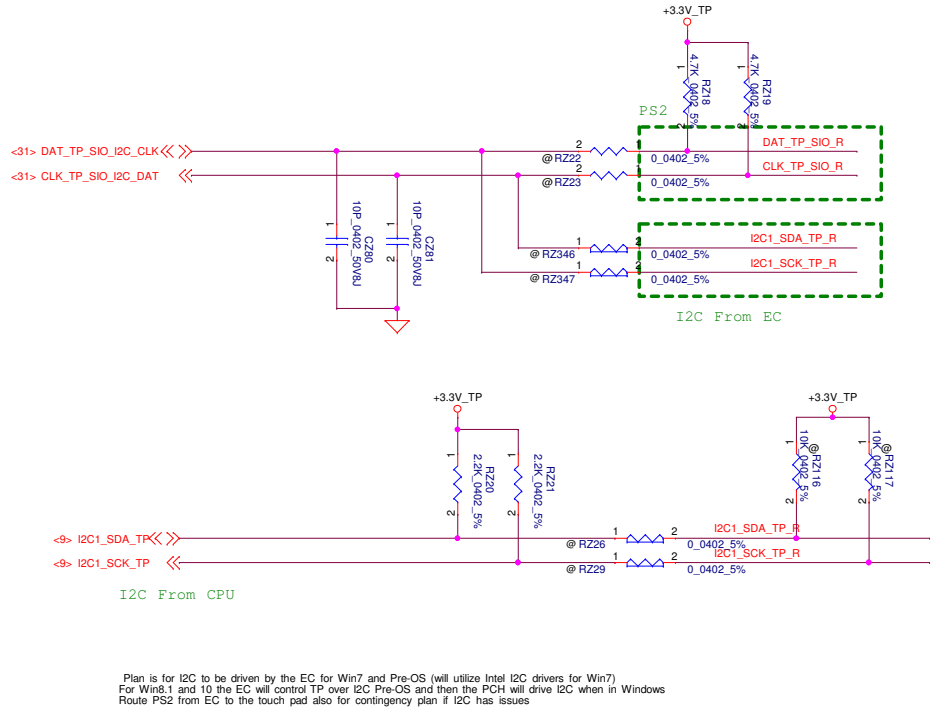
Compal Electronics, Inc.

Title: JUSB2

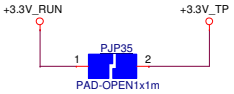
Size | Document Number: LA-F312P | Rev: 2.0

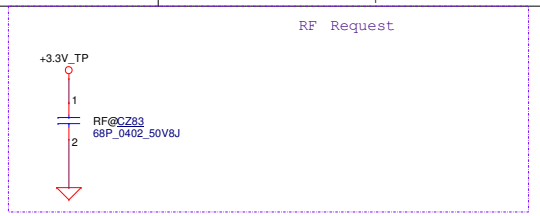
Date: Wednesday, December 20, 2017 | Sheet 36 of 58

Touch Pad

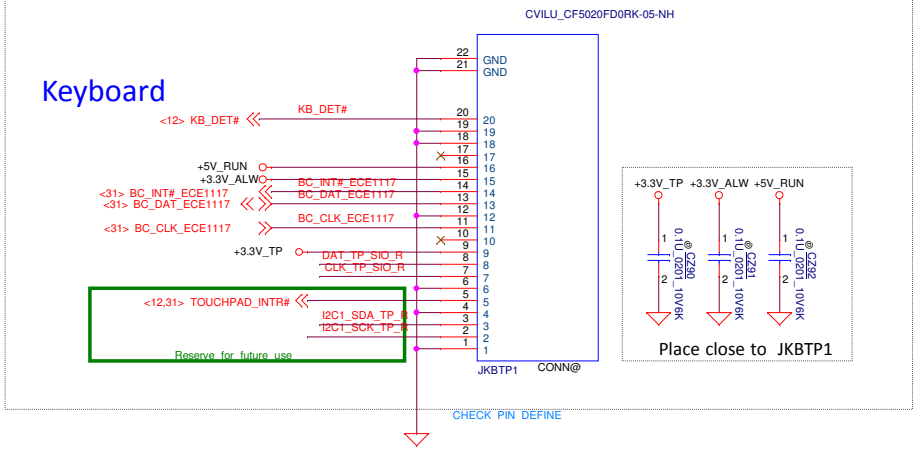


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



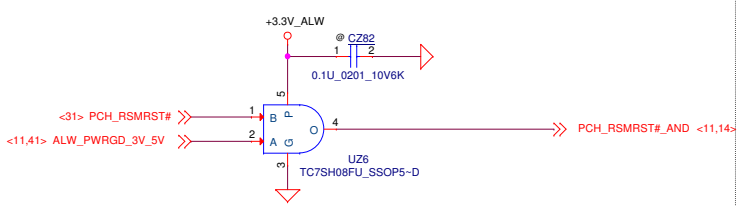


Keyboard



Update to LTCX007Q500 (DVT1.0)

RSMRST circuit



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Compal Electronics, Inc.

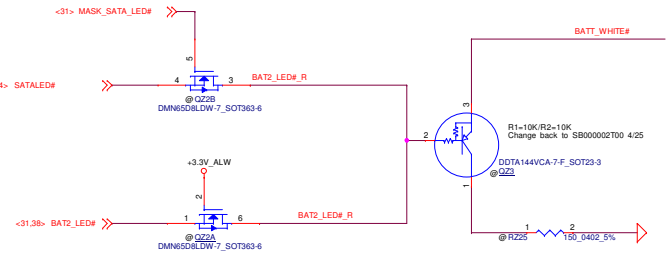
Title: Keyboard

Size | Document Number: LA-F312P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 37 of 58

HDD LED MUX

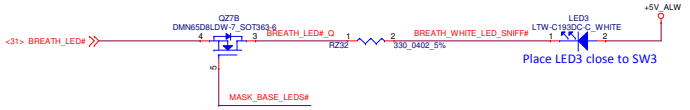
means EC can switch battery white led and HDD LED by hot key " Fn+I"

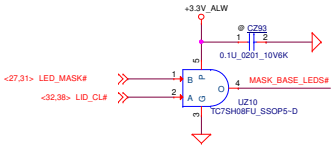


Bat tery LED

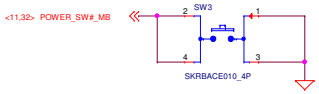
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

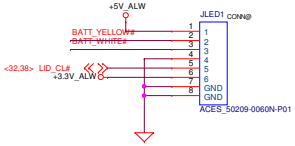




POWER & INSTANT ON SWITCH



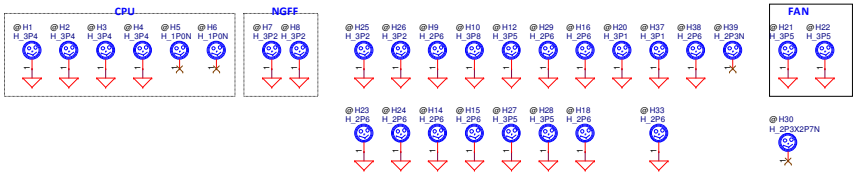
LED board CONN

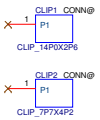


Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





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Title: PAD, LED

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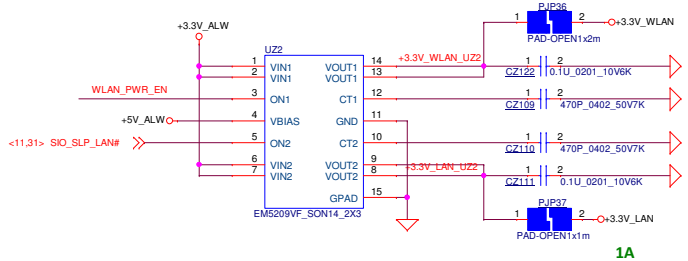
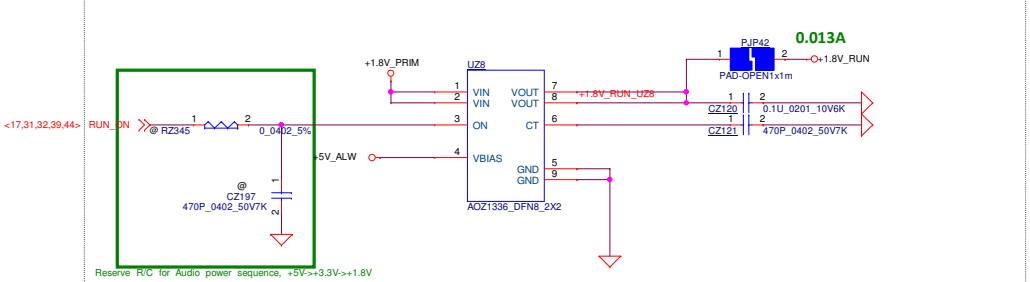
Date: Wednesday, December 20, 2017 | Sheet 38 of 58

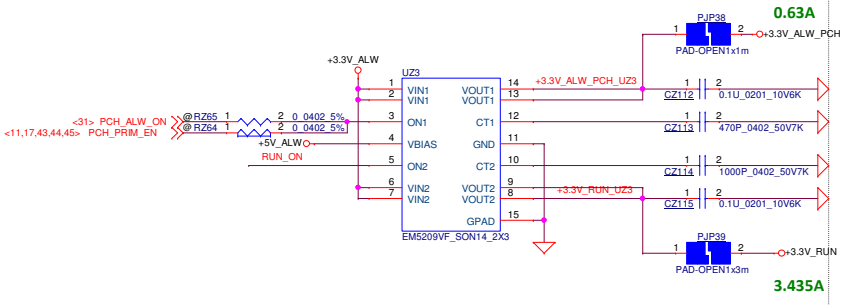
+3.3V_WLAN/+3.3V_LAN source

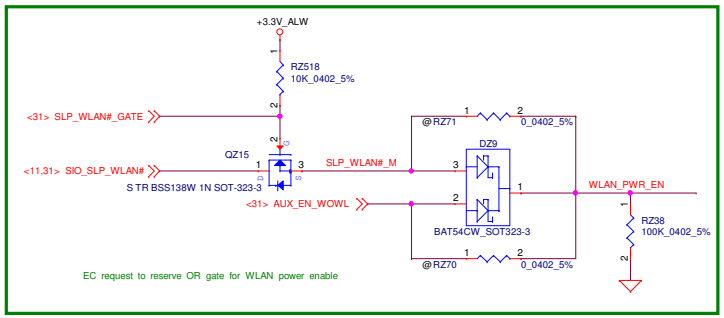


+1.8V_RUN source

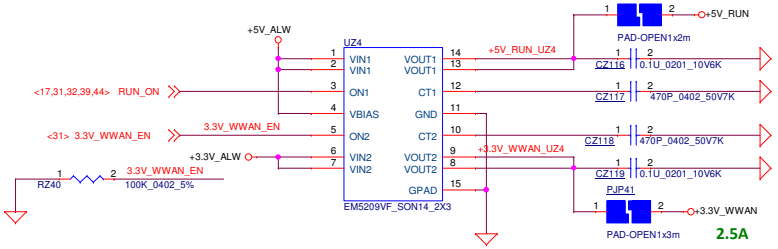


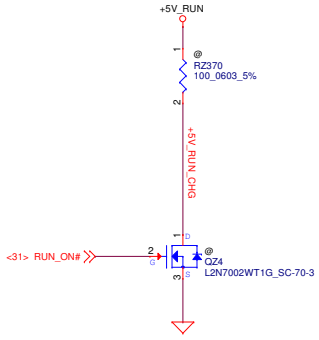
+3.3V_ALW_PCH/+3.3V_RUN source



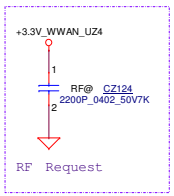


+5V_RUN/+3.3V_WWAN source





Reserve for S3 no power issue (+5V_RUN discharge circuit)



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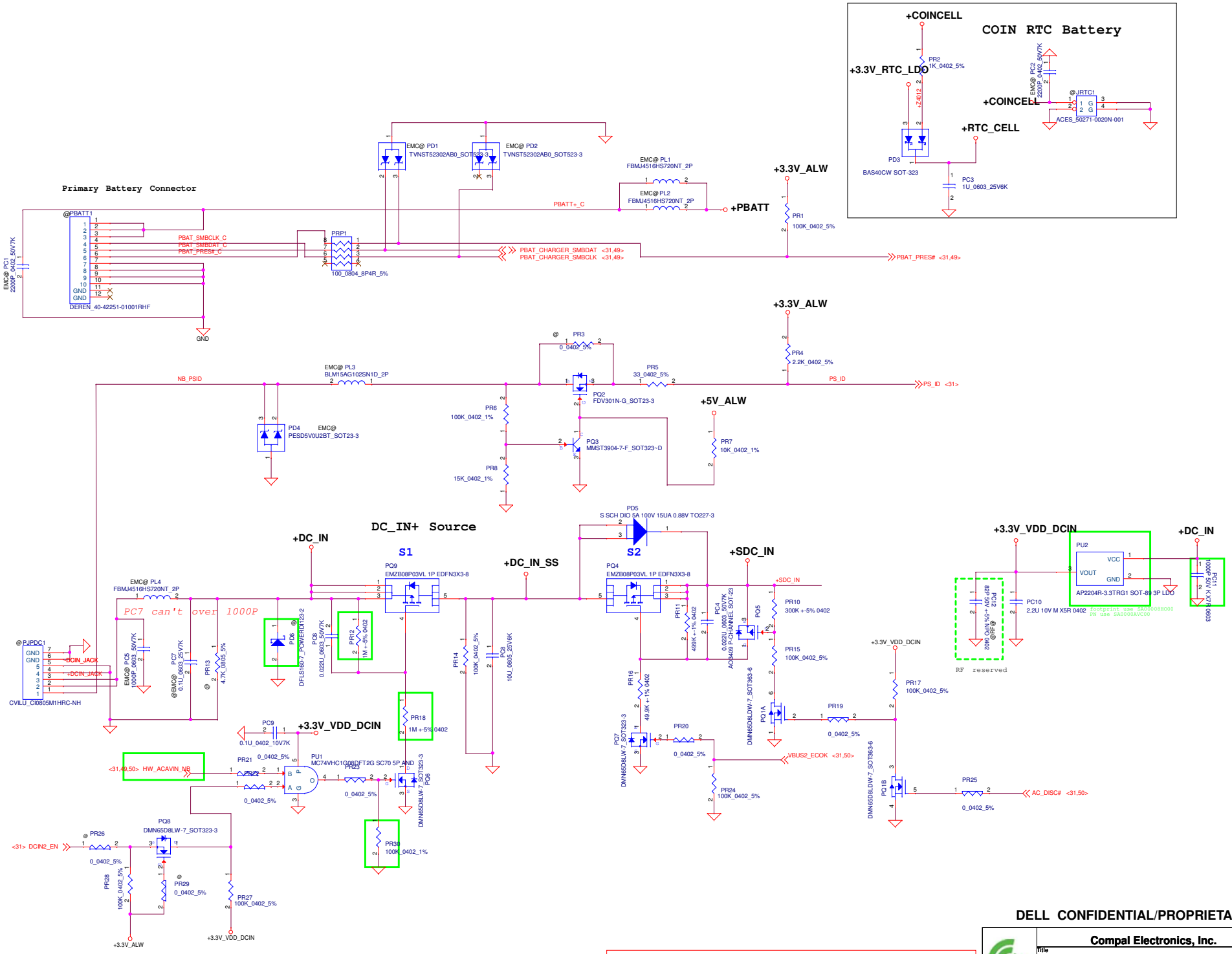
Compal Electronics, Inc.		
Title: Power control		
Size	Document Number: LA-F312P	Rev: 2.0
Date: Wednesday, December 20, 2017	Sheet 39 of 58	



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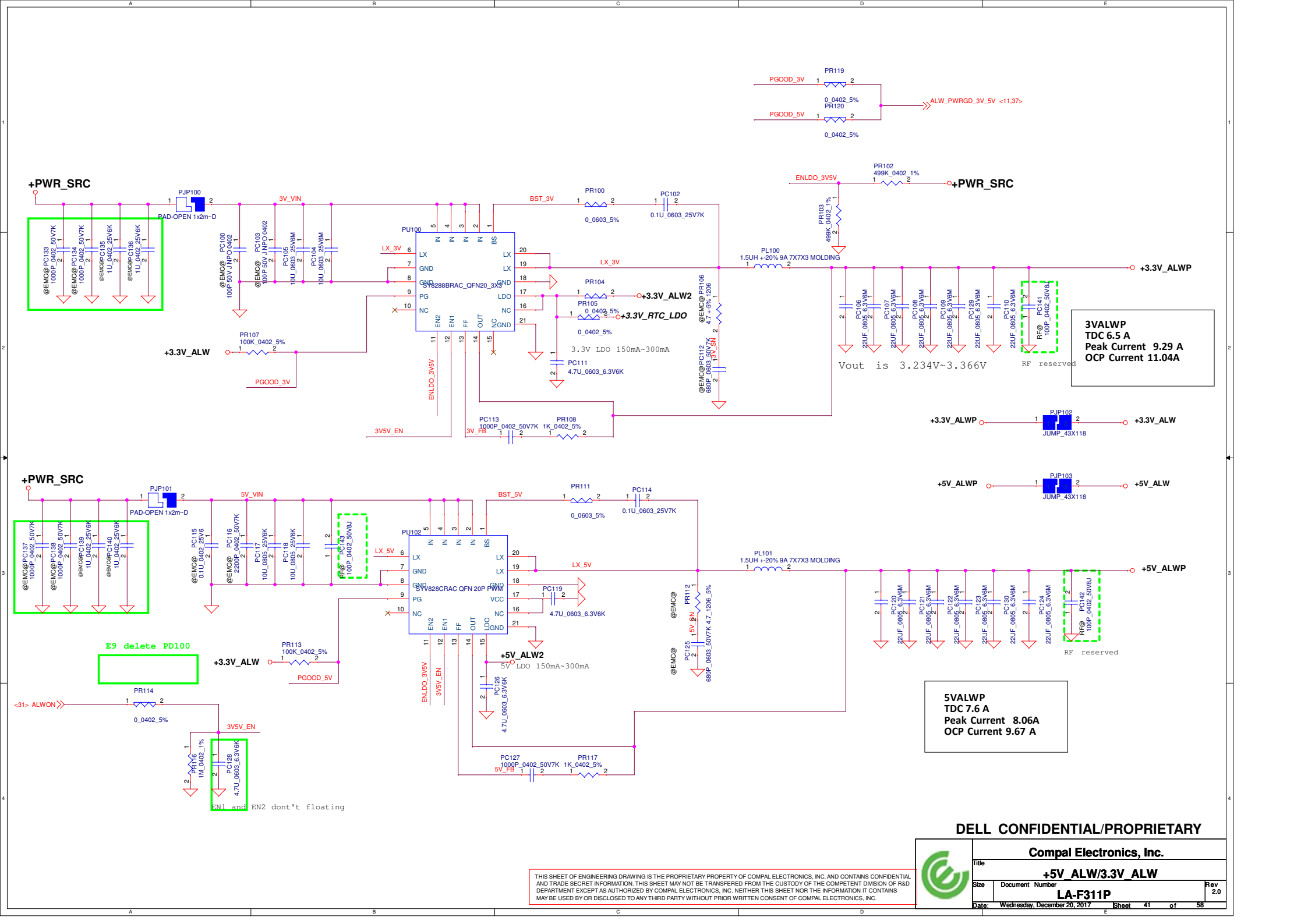
Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-F311P	Rev: 2.0
Date: Wednesday, December 20, 2017	Sheet 40 of 58	



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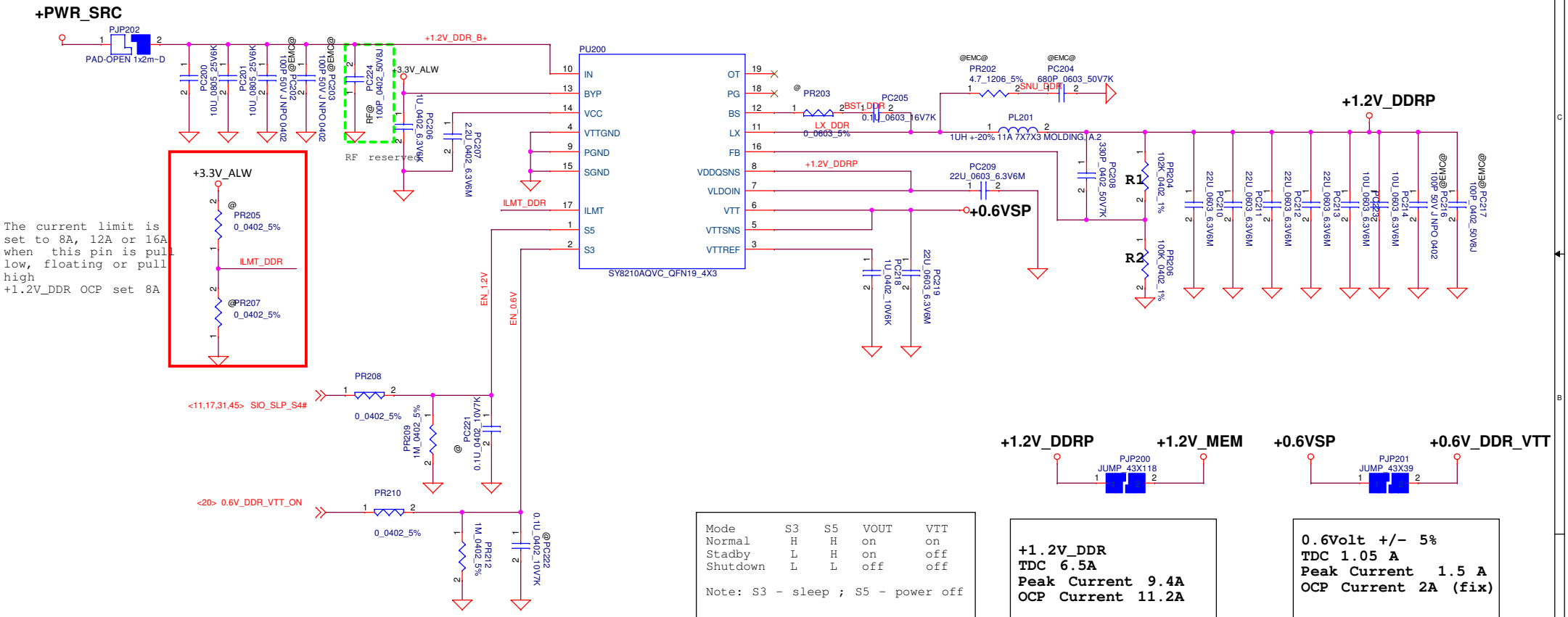

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 6.5A
Peak Current 9.4A
OCP Current 11.2A

0.6Volt +/- 5%
TDC 1.05 A
Peak Current 1.5 A
OCP Current 2A (fix)

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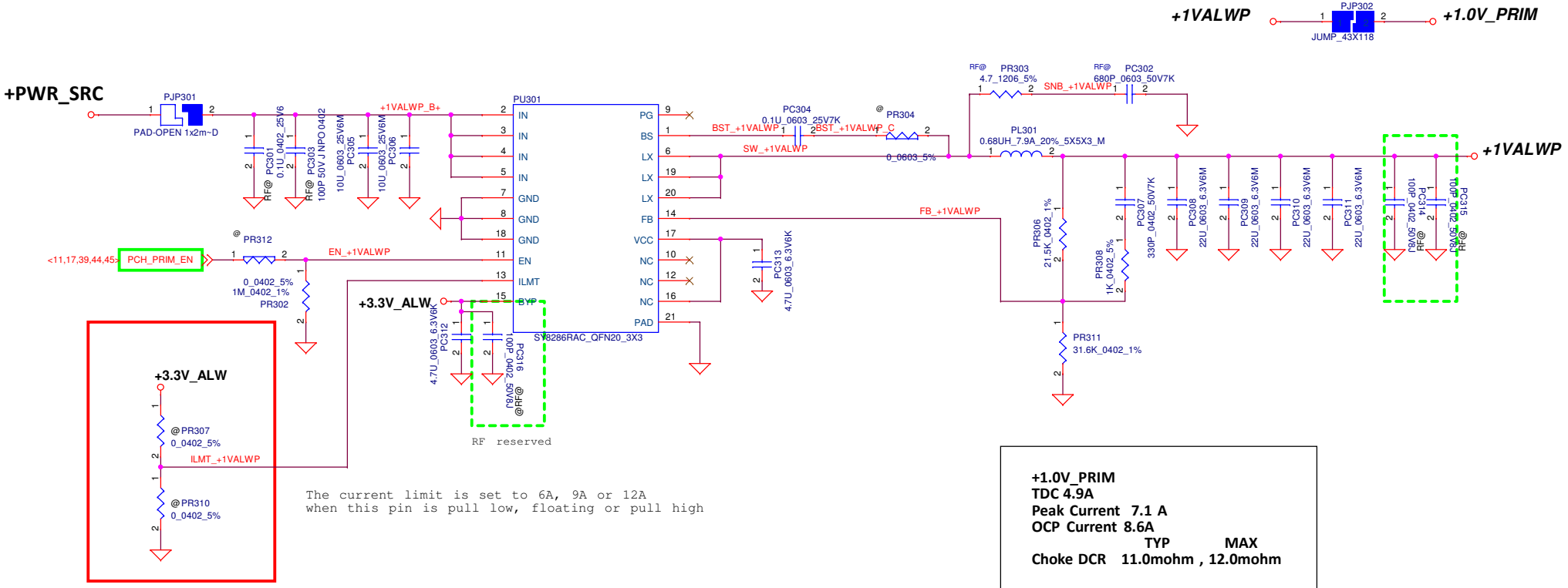
Title: +1.2V_MEN/+0.6V_DDR_VTT

Size | Document Number: LA-F311P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 42 of 58



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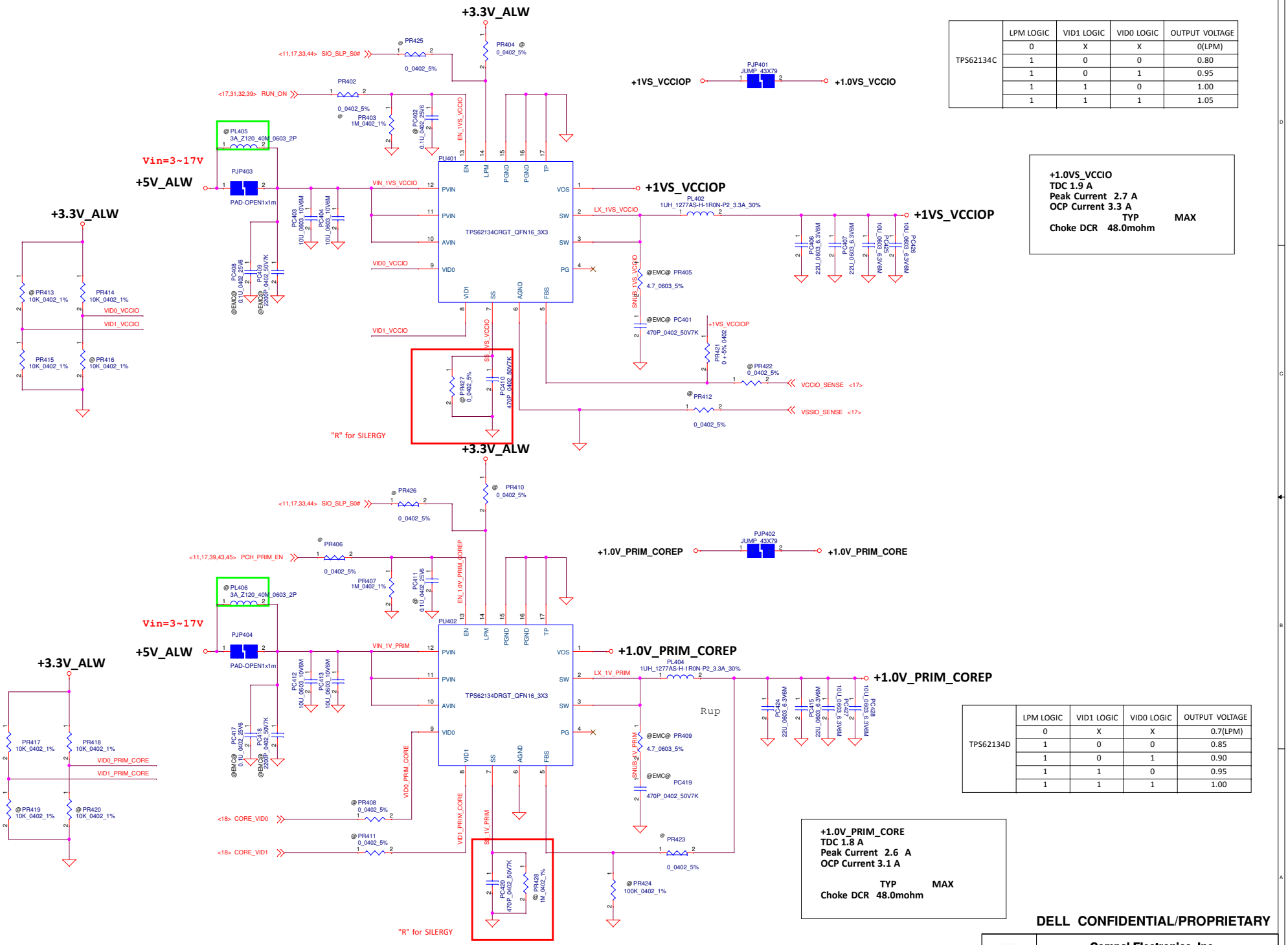
Title: +1VALWP

Size | Document Number: LA-F311P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 43 of 58



TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A

	TYP	MAX
Choke DCR	48.0mohm	

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A

	TYP	MAX
Choke DCR	48.0mohm	

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Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

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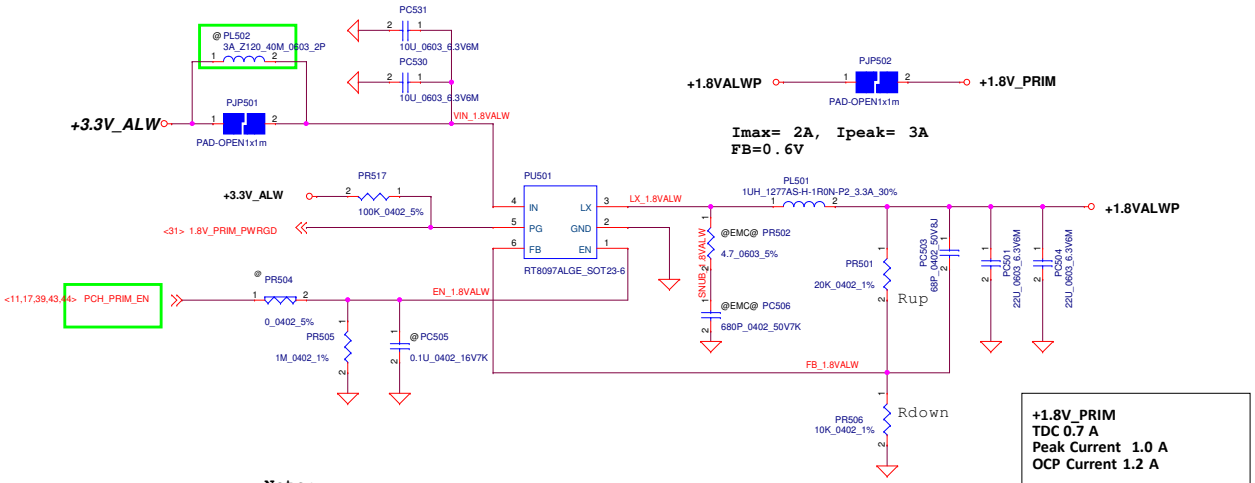
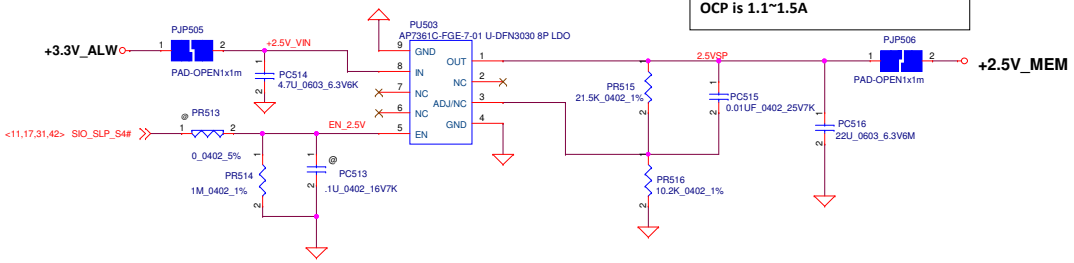
Date: Wednesday, December 20, 2017 | Sheet 44 of 58





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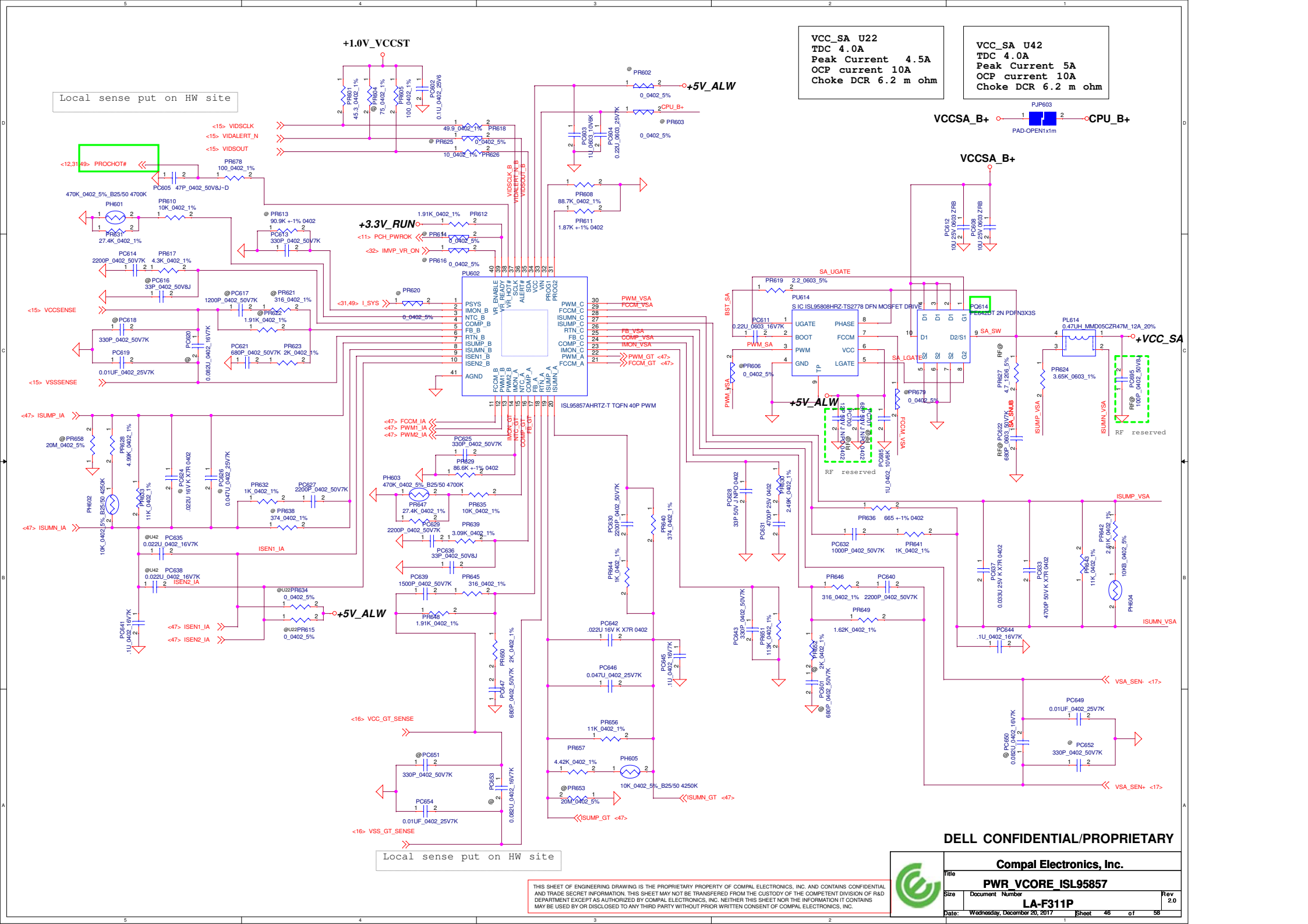
Title: +1.8VALWP/+1.5VSP

Size | Document Number: LA-F311P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 45 of 58



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VCC_core (U22)
TDC 21A
Peak Current 32A
OCP current 38.4A
Choke DCR 0.9 +-5%m ohm

VCC_core (U42)
TDC 42A
Peak Current 64A
OCP current 76.8A
Choke DCR 0.9 +-5%m ohm

For KBL U42 : Pop PR682 and PR684
For KBL U22 : Pop PR683 and PR685

U42

PC626 @U42 0.1U 25V 0402
PR613 @U42 93.1K +-1% 0402
PR621 @U42 1K +-1% 0402
PC624 @U42 0.015U 25V K X7R 0402
PR638 @U42 475 +-1% 0402
PR622 @U42 3.09K_0402_1%
PC616 @U42 68P 50V J 0402
PC617 @U42 220P 50V 0402

U22

PC626 @U22 0.047U_0402_25V7K
PR613 @U22 90.9K +-1% 0402
PR621 @U22 316 +-1% 0402
PC617 @U22 1200P 50V 0402
PR638 @U22 383 +-1% 0402
PR622 @U22 1.5K +-1% 0402
PC616 @U22 33P 50V J 0402
PC624 @U22 .022U 16V K X7R 0402

VCC_GT (U22)
TDC 18A
Peak Current 31A
OCP current 37.2A
Choke DCR 0.9 +-5%m ohm

VCC_GT (U42)
TDC 12A
Peak Current 28A
OCP current 33.6A
Choke DCR 0.9 +-5%m ohm

RF demand

RF reserved

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Compal Electronics, Inc.

Title: PWR_VCORE_ISL95857

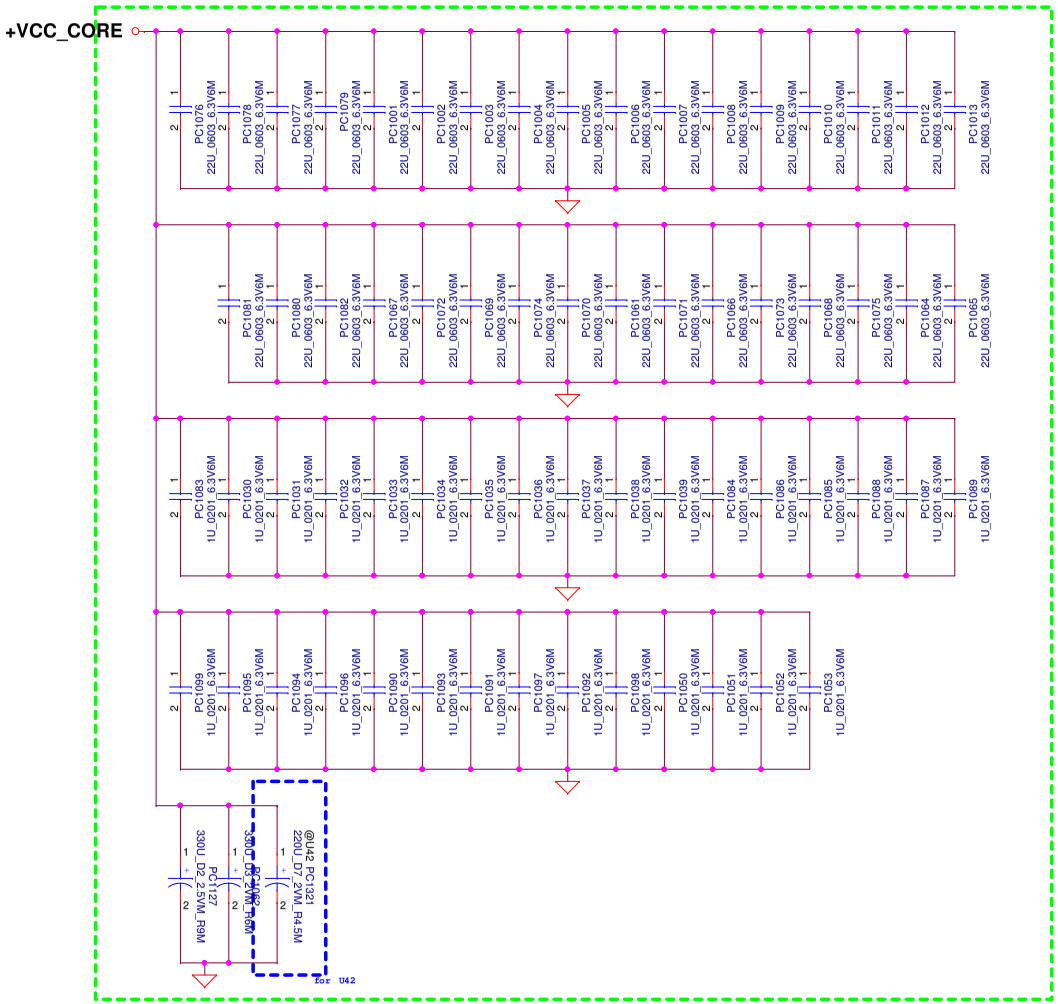
Size: Document Number: LA-F311P Rev: 2.0

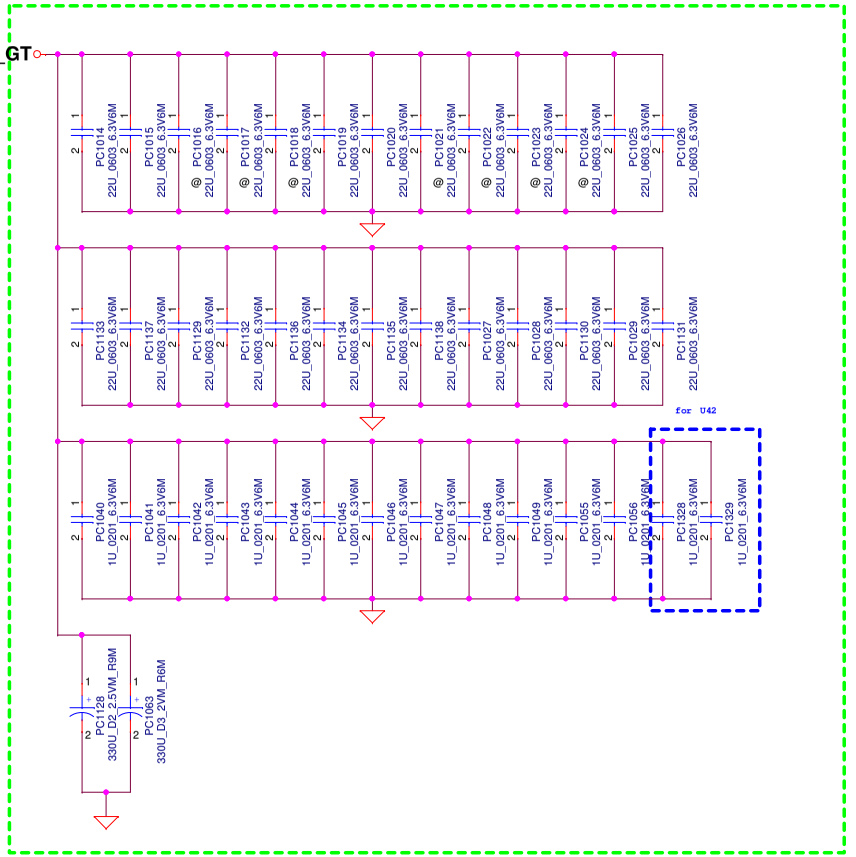
Date: Wednesday, December 20, 2017 Sheet 47 of 58

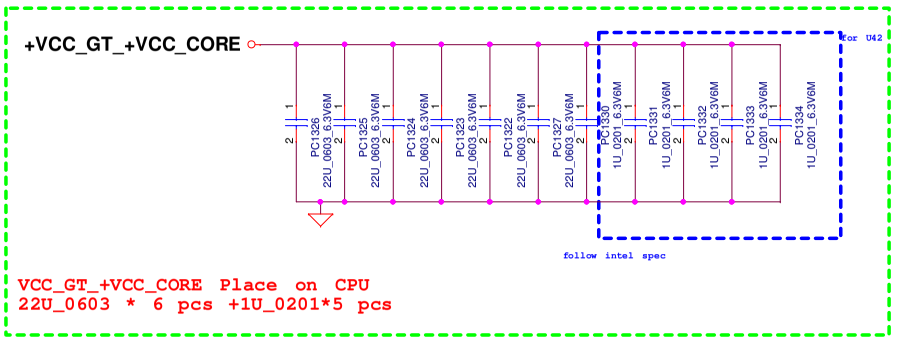
VCC_CORE Place on CPU (U22)
22U_0603 * 33 pcs +1U_0201*31 pcs
+330u_D2*2 pcs

VCC_CORE Place on CPU (U42)
22U_0603 * 33 pcs +1U_0201*31 pcs
+330u_D2*2 pcs+220u_D7*1 pcs

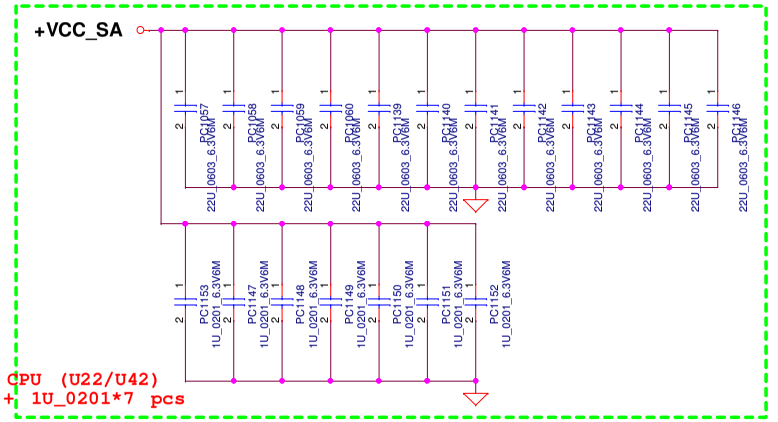
VCC_GT Place on CPU (U22)
22U_0603 * 19 pcs +1U_0201*14 pcs
+330u_D2*2 pcs







VCC_GT_+VCC_CORE Place on CPU
22U_0603 * 6 pcs +1U_0201*5 pcs



VCC_SA Place on CPU (U22/U42)
22U_0603*12 pcs + 1U_0201*7 pcs

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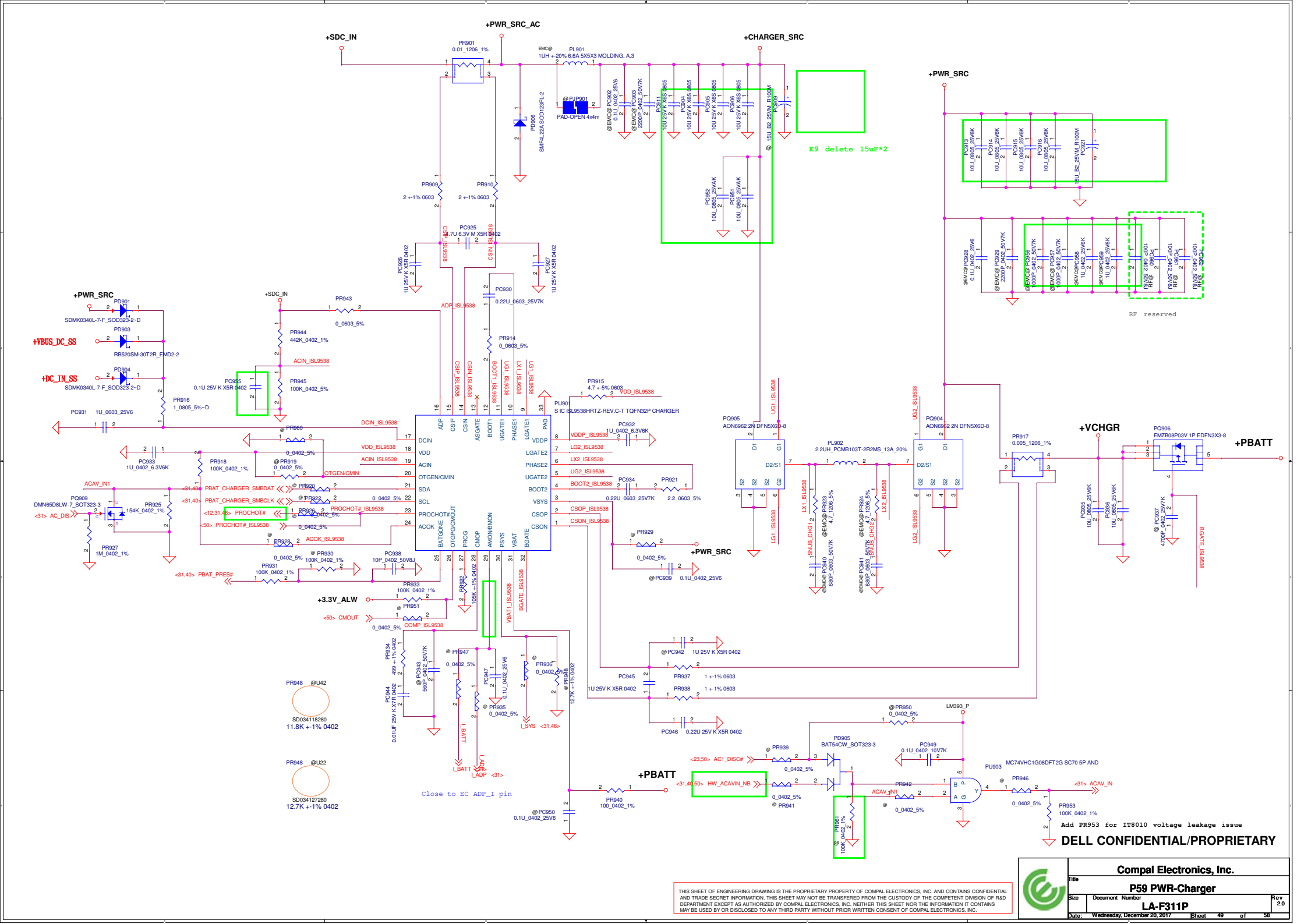
Title: PROCESSOR DECOUPLING

Size: | Document Number: LA-F311P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 48 of 58


+SDC_IN
+PWR_SRC_AC
+CHARGER_SRC
+PWR_SRC
+VBUS_DC_SS
+DC_IN_SS
+3.3V_ALW
+VCHGR
+PBATT
E9 delete 15uF*2
RF reserved
Close to EC ADP_I pin
Add PR953 for IT8010 voltage leakage issue
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Compal Electronics, Inc.
P59 PWR-Charger
LA-F311P
Wednesday, December 20, 2017
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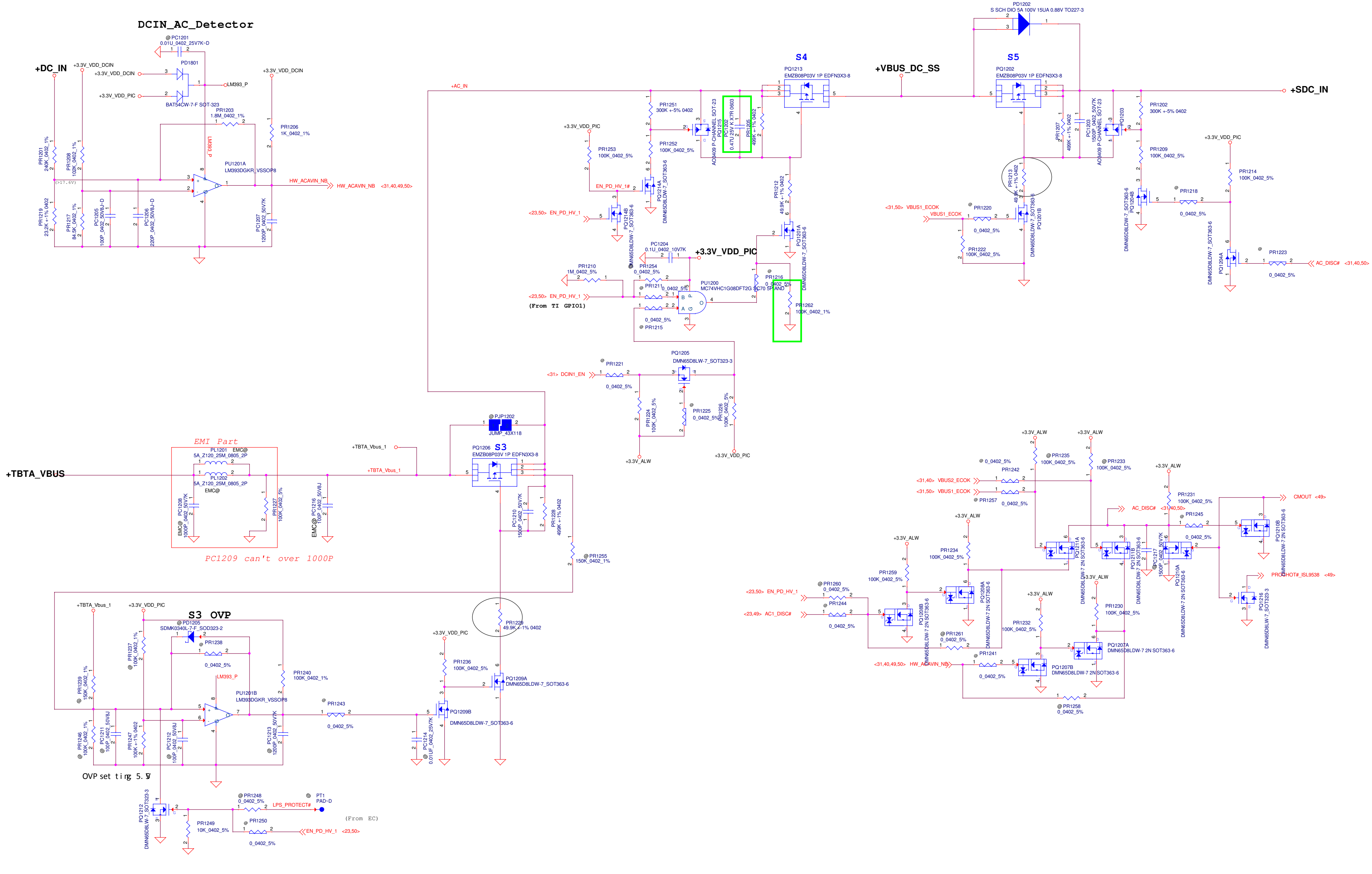

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Title	TypeC_PD
Size / Document Number	LA-F311P
Rev	2.0
Date:	Wednesday, December 20, 2017
Sheet	50 of 58

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	57	VCC_CORE VCORE_VGT,VSA	2017 06/07	Compal	Change DrMOS from TI to Fairlchild	PU610/ PU612/ PU613 change to FDMF3035 (SA0000AHX00)	X01
2	50 51 52 53 56 57 59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Larry	RF team request some item	Add PC315, PC314, PC960, PC961, PC962, PC700, PC701, PC142, PC143, Reserved PC316, PC12, PC702, PC141,PC695, PC696,PC224, PC703	X01
3	51 57 59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Albert	EMI need to modify	1. Depop PC133, PC134, PC135, PC136, PC137, PC138, PC139, PC140, PC689, PC690, PC691, PC692, PC956, PC957, PC958, PC959. 2. Pop PL901.	X01
4	57 59	Charger	2017 06/12	Compal	Change component for acoustic solution	1. CPU input MLCC change to 0603 size and change to low noise MLCC (SE00000X210): PC608, PC612, PC656, PC657, PC658, PC664, PC665, PC672, PC673, PC674, PC675, PC682, PC683, PC684 2. Remove PC917~PC920(10U*4pcs) , add PC921(15U pos cap)	X01
5	57	VCC_CORE VCORE_VGT	2017 06/19	Compal	Add one more bulk for acoustic solution	Pop 2pcs 100uf (PC606,PC607)	X01
7							
8							
12				Compal			
13				Compal			
14				Compal			
15				Compal			
16				Compal			
17				Compal			
18				Compal			
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23							

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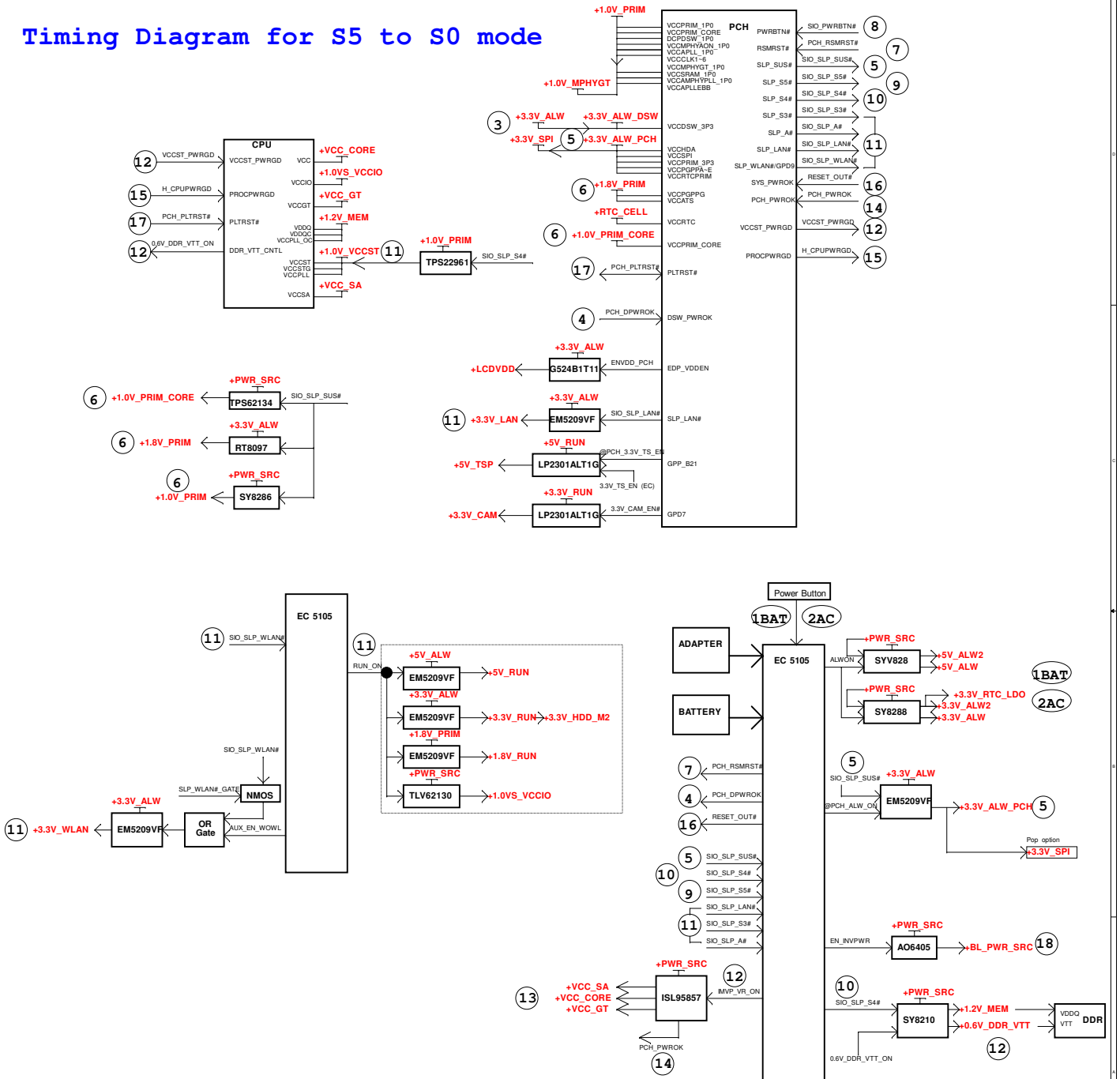
File: PWR P.I.R

Size: Document Number: LA-F311P Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 51 of 58

Timing Diagram for S5 to S0 mode



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Power Sequence

LA-F312P

Rev 2.0

Date: Wednesday, December 20, 2017 Sheet 52 of 58

Version Change List (P. I. R. List) LA-F312P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	8	CPU (3/14)	2017/03/21	EE	Winbond 16MB SPI ROM EOL (change to J-die)	Change UC5, UC6 to SA00005VV20	0.1(X00)
2	8	CPU (3/14)	2017/03/21	ME	JSPI1 connector change vendor	Change JSPI1 to SP010022Q00	0.1(X00)
3	11	CPU (6/14)	2017/03/21	EE	KBL-R U42 X'tal	Add RC415~RC420,CC334,CC335,YC3	0.1(X00)
4	13	CPU (8/14)	2017/03/21	EE	KBL-R CRB schematic	Add RC436 0ohm to GND	0.1(X00)
5	14	CPU (9/14)	2017/03/21	ME	JXDP1 connector change vendor	Change JXDP1 to SP01001VB00	0.1(X00)
6	16	CPU (11/14)	2017/03/21	EE	Follow KBL-R_U42_Processor_Line_BGA1356_ Ballout_Rev1p0	Reserve RC437, RC438	0.1(X00)
7	18	CPU (13/14)	2017/03/21	EE	RTC Power Gate Circuit for +3.3V_DSW	Add RC431~RC433, RC439, RC440, QC6, QC7	0.1(X00)
8	33	EC MEC5105	2017/03/21	EE	RTC Power Gate Circuit for RTCRST	Add QE14~QE17, RE540~RE546, RE551, CE63, RC441, RC442, DC1, DC2, RC445	0.1(X00)
9	34	EC MEC5105 Support	2017/03/21	EE	Remove IO expander	Remove UE2 relating circuit	0.1(X00)
10	28	eDP CONN & Touch screen	2017/03/21	ESD	ESD request	Remove DV7, DV8	0.1(X00)
11	35	USH & TPM	2017/03/21	EE	TPM NPCT65X and NPCT75X schematic colay	UZ12 relating circuit and change UZ12 to SA0000AQ200	0.1(X00)
12	31	NGFF Card	2017/03/21	RF	RF request to align w/ BR MLK	LI8, LI9 change to SM070003Z00, LI16, LI17 change to SM070003V00	0.1(X00)
13	33	EC MEC5105	2017/03/21	EE	RTCRST_ON glitch	Reserve CE64	0.1(X00)
14	All	All	2017/03/21	EE	Port map change	JUSB1 change to USB30_port6 and USB20_port9 USB20_port1 BOM option to Type-C(PD UT5) Delete PS8338 and WIGIG circuit and connect DDI2 to UT1 (Add RC446~RC448 for CPU_DP2_HPD/CPU_DP2_AUXP/CPU_DP2_AUXN)	0.1(X00)
15	23	[Type C]PD Controller TI	2017/03/28	EE	Change PD to PD3.0	Change UT5 to SA0000AP500	0.1(X00)
16	9	CPU (4/14)	2017/03/28	EE	JUART1 reverse	JUART1 pin SWAP	0.1(X00)
17	32	EC MEC5105 Support	2017/03/28	EE	Panel ID define change	RE300 change to 130K ohm for 12" RE300 change to 62K ohm for 13"	0.1(X00)
18	33	USH & TPM	2017/03/28	EE	Prevent POA_WAKE# ESD	Add RZ364 100 ohm to POA_WAKE#	0.1(X00)
19	33	USH & TPM	2017/03/28	EE	Prevent Contactless_det# backdrive	Add DZ8	0.1(X00)
20	25	[Type C]USB3.0 CONN	2017/03/28	ESD	ESD request	Change DT7, DT8, DT11, DT12 to DT39 Change DT15, DT16, DT19, DT20 to DT40	0.1(X00)
21	11	CPU (6/14)	2017/03/28	EE	RTC Power Gate Circuit option	Add RC441, RC442, DC1, DC2, RC445	0.1(X00)

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Version Change List (P. I. R. List) LA-E122P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	All	All	2017/03/28	EE	GPIO map change	PCH_RSMRST#_GPIO204 -> USH_PWR_STATE# (delete RE363) PORT80_DET# -> DCIN1_EN (delete RE512,RE513,RZ131) SHD_IO3 -> VBUS1_ECOK SHD_IO1 -> SATA_LED_EN ENVDD_PCH -> DCIN2_EN SIO_RCIN#_EC -> VBUS2_ECOK and delete RE339/RC13 USH_SMBCLK -> USH_EXPANDER_SMBCLK USH_SMBDAT -> USH_EXPANDER_SMBCLK Delete RTCRST_ON_GPIO141 PRIM_PWRGD_GPIO024 -> RESET_IN# 3.3V_TS_EN rename to PCH_3.3_TS_EN SHD_IO0 change to 3.3V_TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V_TS_EN/PCH_3.3V_TS_EN option	0.1(X00)
23	All	All	2017/03/30	EE	GPIO map change	PANEL_ID -> SYSTEM_ID SHD_IO1 -> SATA_LED_EN -> MASK_SATA_LED# EXPANDER_GPU_SMDAT -> VCCDSW_EN_GPIO and delete RE524 EXPANDER_GPU_SMCLK -> free and delete RE525 THERMATRIP1# -> THERMTRIP1# THERMATRIP2# -> THERMTRIP2# SIO_EXT_SCI#_EC -> free and delete RE341 FAN1_TACH -> TACH_FAN1 LCD_TST -> free WWAN_RADIO_DIS# -> LCD_TST EC GPIO123 (UE1.F12) -> WWAN_RADIO_DIS# DCIN3_EN -> EC GPIO202 (UE1.J6) (SBMLK 12/13 only) FAN1_PWM -> PWM_FAN1 PS_ID -> free SHD_CLK -> PS_ID and delete RE374 AUD_NB_MUTE# -> NB_MUTE#	0.1(X00)
24	All	All	2017/03/30	EE	GPIO map change	UE1.B1 -> add net name 3.3V_ALW2 and depop RE57 (Microchip suggest) RESET_IN# -> Remove RE361 (Microchip suggest) SLOT2_CONFIG_3 -> NGFF_CONFIG_3 ME_FWP -> ME_FWP_PCH ME_FW_EC -> ME_FWP HW_GPS_DISABLE# -> GPS_DISABLE# VGA_ID -> BEEP H_PROCHOT# -> PROCHOT# USB_PWR_SHR_VBUS_EN -> USB_POWERSHARE_VBUS_EN USB_PWR_SHR_LFT_EN# -> USB_POWERSHARE_EN# SIO_EXT_SMI#_EC -> free and delete RE338 CLKRUN#_EC -> ENABLE_DS# and delete RE337 and add RE549, RE550 SHD_IO2 -> 1.8V_PRIM_PWRGD and delete RE360 BEEP -> VGA_IDENTIFY (rename from VGA_ID) SHD_CS# -> PCH_RSMRST# and delete RE364 SLOT2_CONFIG_0 -> NGFF_CONFIG_0 SLOT2_CONFIG_1 -> NGFF_CONFIG_1 SLOT2_CONFIG_2 -> NGFF_CONFIG_2 ACAV_IN_NB -> HW_ACAVIN_NB LID_CL#_NB -> LID_CL_SIO# SYS_PWROK->reserved 0ohm RE548 and add netname to RESET_OUT	0.1(X00)

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Version Change List (P. I. R. List) LA-F312P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	All	All	2017/03/30	EE	Port map change	NGFF3 (SSD 4 Lane) add PCIE port 9 and port 10 LOM change to PCIE port 4	0.1(X00)
26	11 31	CPU (6/14) EC MEC5105	2017/04/05	EE	Intel PDG for DSx and NonDSx	Add RC443, RC444 for SUSACK#, ME_SUS_PWR_ACK Add BOM structure DS3@ for RE349 and RE536	0.1(X00)
27	17 39	CPU (12/14) Power control	2017/04/05	EE	PCH_PRIM_EN net name change	Change net name from SIO_SLP_SUS# to PCH_PRIM_EN	0.1(X00)
28	32	EC MEC5105 Support	2017/04/05	EE	Microchip suggest	Change RE71 to 10 ohm	0.1(X00)
29	39	Power control	2017/04/05	EE	+5V_RUN discharge circuit for S3 no power issue	Add QZ4 and RZ370	0.1(X00)
30	38	PAD, LED	2017/04/05	EE	Add bracket	Add bracket CLIP1 CLIP_14P0X2P6 Add bracket CLIP2 CLIP_7P7X4P2	0.1(X00)
31	32	EC MEC5105 Support	2017/04/11	EE	+5V_RUN for FAN	Change DE1 to SC400002J00	0.1(X00)
32	39	Power control	2017/04/14	EE	EC request to reseve OR gate for WLAN power EN	Reserve DZ9	0.1(X00)
33	32	EC MEC5105 Support	2017/04/14	EE	EC request to reseve ESPI_RESET# for JESPI	Reserve RE560	0.1(X00)
34	31	EC MEC5105	2017/04/14	EE	Schmatic align	Add GPU_SMCLK/GPU_SMDAT PU to RPE12	0.1(X00)
35	11	CPU (6/14)	2017/04/14	EE	WIGIG feature remove	Add back RC50 and depop	0.1(X00)
36	30	CodeC ALC3246	2017/04/14	EE	Realtek request	CA54 change back to 10pf and depop	0.1(X00)
37	31 11	EC MEC5105 CPU (6/14)	2017/04/14	EE	RTC power Gate circuit rev.2 (0411)	Delete RE540, RE542, RE544, RE545, QE14, QE16 Change RE543 to 1M ohm and RE546 to 10K ohm Add DE2, CE65, Reserve CE66 for VCCDSW_EN	0.1(X00)
38	11	CPU (6/14)	2017/04/14	EE	RTC Power Gate Circuit option (0411)	RC445 change to connect to VCCDSW_EN and pop	0.1(X00)
39	10 23	CPU (5/14) [Type C]PD Controller TI	2017/04/14	EE	OTG support	Pop RT74, Depop RC337	0.1(X00)
40	13	CPU (8/14)	2017/04/19	EE	KBL-R CRB schematic	Add BOM structure for RC436 U42@	0.1(X00)
41	All	All	2017/04/19	EE	GPIO map change	RC443 BOM structure change to @ GPIO126->GPU_PWR_LEVEL Add RTCRST_ON_R net neme for QE17.2 Add SIO_SLP_SUS#_R net name and PU RE561 SYS_LED_MASK#->LED_MASK# RC27.2->NC for CLKRUN# HDD_DET#->SATAGP0 Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN	0.1(X00)
42	33	USH & TPM	2017/04/19	EE	TPM change to NPCT650x	Change UZ12 to SA00008EL80 and related resistors	0.1(X00)
43	9	CPU (4/14)	2017/04/19	RF	I2C interface for Active Steering Antenna (SB14 only)	Swap I2C3_SDA and I2C3_SCL	0.1(X00)

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Version Change List (P. I. R. List)
LA-F312P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
43	31	EC MEC5105	2017/04/19	EE	Dell request to add test point for EC free pins	Add test point T141 for UE1.D1->GPIO051 Add test point T142 for UE1.L11->GPIO054 Add test point T264 for UE1.F13->VBUS3_ECOK Add test point T143 for UE1.K7->GPIO011 Add test point T144 for UE1.M1->GPIO100 Add test point T262 for UE1.J6->DCIN3_EN Add test point T147 for UE1.M4->GPIO013	0.1(X00)
44	All	All	2017/04/20	EE	GPIO map change	GPIO013 net name change to DGPU_PWROK UPD1_ALERT#->UPD1_SMBINT# UPD1_SMBUS_ALERT#->UPD1_SMBINT#_R	0.1(X00)
45	11	CPU (6/14)	2017/04/20	EE	Schematic align	INTRUDER# PU change to +RTC_CELL_PCH	0.1(X00)
46	31	EC MEC5105	2017/04/26	EE	GPIO map change	UPD2_ALERT#->UPD2_SMBINT#	0.1(X00)
47	11	CPU (6/14)	2017/05/03	EE	CLKREQ align	Pop RC50 and RC190	0.1(X00)
48	10	CPU (5/14)	2017/05/03	EE	OTG support	RC337 pop and change to 10K ohm	0.1(X00)
49	39	Power control	2017/06/02	EE	EC request to reseve OR gate for WLAN power EN	Add QZ15 and RZ518 Add SLP_WLAN#_GATE net and RE552 to UE1.K10	0.2(X01)
50	23	[Type C]PD Controller TI	2017/06/02	EE	PD ROM main source change	UT6 change to SA000095R10 (GD)	0.2(X01)
51	11	CPU (6/14)	2017/06/02	EE	Schematic align	Reserve RC551 for SUSACK#_R	0.2(X01)
52	33	USH & TPM	2017/06/02	EE	Nuvoton request to change TPM_PIRQ# power rai TPM change to NPCT750	TPM_PIRQ# power rail change to +3.3V_ALW_PCH Change UZ12 to SA0000AQ200 and related resistors and CZ75 change to 10U	0.2(X01)
53	All	All	2017/06/02	ESD	Main source change	DI1,DI4,DT39,DT40,DI6 change to SC300001Y00 DI2,DI3,DI5 change to SCA00000T00 DA2 change to SCA00001A00 DT4 change to SCA00002Q00	0.2(X01)
54	All	All	2017/06/02	EE	DFX request	DA8, DC1, DC2, DE2, DZ1, DZ2, DZ5-DZ8 footprint change to AZ5125-01HPR7G_SOD523-2	0.2(X01)
55	All	All	2017/06/02	EE	Dell request to change cap to L-end P/N	L-end P/N for all cap	0.2(X01)
56	30	CodeC ALC3246	2017/06/12	EE	DFX request	LA13 footprint change to TAI-T_HCB2012KF-121T50_2P	0.2(X01)
57	33	USH & TPM	2017/06/12	RF	RF request	Add CZ76/CZ77 (12pf/68pf) for +3.3V_RUN of UZ12 Add CZ78 (100pf) for +PWR_SRC of JUSH1	0.2(X01)
58	32	EC MEC5105 Support	2017/06/12	EE	Board ID	Change RE79 to 130Kohm (rev. X01)	0.2(X01)
59	9	CPU (4/14)	2017/06/14	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553-RC556 for connector selection	0.2(X01)
60	39	Power control	2017/06/14	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2(X01)
61	22	TUSB546	2017/06/14	EE	PS8743-B1 colay (SA00009E910)	Add RT410, RT411, RT412,RT413, RT414, RT415, RT416,CT213	0.2(X01)
62	23	[Type C]PD Controller TI	2017/06/14	EE	PS8743-B1 colay (SA00009E910)	Add RT405, RT406, RT407, RT417, RT418	0.2(X01)

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Version Change List (P. I. R. List)
LA-F312P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
63	30	CodeC ALC3246	2017/06/15	RF	RF request	Reserve CA78 for +5V_RUN_AUDIO	0.2(X01)
64	23	[Type C]PD Controller TI	2017/06/21	EE	PD change to rer.C	UT5 change to SA0000AX700	0.2(X01)
65	6	CPU (1/14)	2017/06/21	EE	AUX voltage level shift	Depop RC448, RC447	0.2(X01)
66	23	TUSB546	2017/06/21	EE	TUSB546 DPEQ set to level 5	Depop RT248, RT140 and pop RT303 and RT306	0.2(X01)
67	23	[Type C]PD Controller TI	2017/08/02	EE	PS8743-B1 colay (SA00009E910)	Change RT405-RT407 to 10K	0.3(X02)
68	25	[Type C]USB3.0 CONN	2017/08/02	EE	Schematic align	CT99-CT102 change to 0.01uf (SE00000YH00)	0.3(X02)
69	22	TUSB546	2017/08/02	EE	TUSB546 new version IC	UT9 change to SA00009R720	0.3(X02)
70	26 31 13	eDP CONN EC MEC5105 CPU (13/14)	2017/08/04	EE	Reserve soft start solution	Reserve RV400, CV635 for QV8 Reserve CZ200, RZ380 for QZ1 Reserve CC340 for QC7 Reserve RE565 for QE15	0.3(X02)
71	30	CodeC ALC3246	2017/08/04	RF	RF request to pop CA54 for 2MHz/4MHz noise	Change CA54 to 82pf and pop	0.3(X02)
72	21	HDMI Conn	2017/08/04	EMI/EE	HDMI EA for NonAR only	Change RV35 to 100ohn Change LV37, LV38 to SHI0000M500 Change LV31-LV36 to SHI00003F0L	0.3(X02)
73	32	EC MEC5105 Support	2017/08/07	EE	Board ID	Change RE79 to 62Kohm (rev. X02)	0.3(X02)
74	9	CPU (4/14)	2017/08/09	EE	TPM_PIRQ# GPIO map change	Add RC560 and reserve RC561 to TPM_PIRQ#	0.3(X02)
75	32	EC MEC5105 Support	2017/09/15	EE	Board ID	Change RE79 to 4.2Kohm (rev. A00)	1.0(A00)
76	12	CPU (7/14)	2017/09/15	EE	ME SW depop	Depop RC222, SW1, RC221 change to 0 ohm short pad	1.0(A00)
77	33	USH & TPM	2017/09/15	EE	TPM change to MP version	UZ12 change to SA0000AQ220	1.0(A00)
78	9	CPU (4/14)	2017/09/15	EE	GPIO map change	Depop RC330, RC331	1.0(A00)
79	8	CPU (3/14)	2017/09/15	EE	Add solder mask	Add UC6 -NPM	1.0(A00)
80	All	All	2017/09/15	EE	0 ohm change to short pad	0 ohm change to short pad	1.0(A00)
81	All	All	2017/09/15	EE	Only support DS3 (0 ohm change to short pad)	Only support DS3 (0 ohm change to short pad)	1.0(A00)
82	22	TUSB546	2017/09/15	EE	TUSB546 DPEQ set to default	Depop RT303, RT306, Pop RT140, RT248	1.0(A00)
83	20 29	HDMI CONN NGFF card	2017/09/18	EE	DFX request	Add LV3,LV6,LV9,LV12 RI27,RI28,RI29,RI30,RI47,RI48,RI49,RI50 -NPM	1.0(A00)
84	24	[Type C]PD Power	2017/10/03	EE	X1 Code	DT1,DT2,DT3 Change from SC1N4148180 to SC100005500	1.0(A00)
85	27	LAN Clarkvillie & RJ45	2017/10/03	EE	Not completely replaced with DAZ40	LL1 Change from SHI0000IY00 to SHI0000K000	1.0(A00)

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Version Change List (P. I. R. List)
LA-F312P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
86	23	[Type C]PD Controller TI	2017/11/10	EE	Main vendor EOL	CT74,CT83 Change from SE00000OU00 to SE00000QL10	1.0(A00)
87	23	[Type C]PD Controller TI	2017/11/10	EE	PD just change part number	UT5 Change from SA0000AX700 to SA0000BIJ00	1.0(A00)
88	38	PAD, LED	2017/12/08	EE	SW3 main source change	SW3 main source change from SN111005800 to SN100005800	1.0(A00)
89	17	CPU (12/14)	2017/12/08	EE	WHEA BSOD Intel request	CC202 change to 22uf for 4+2 CPU, but keep 1uf for 2+2 CPU	1.0(A00)
90	17	CPU (12/14)	2017/12/20	EE	WHEA BSOD	Add CC341 22uf 0603,Depop CC202 22uf 0402	2.0(A01)
91	32	MEC5105 support	2017/12/29	EE	Board ID	Change RE79 to 2Kohm (rev. A01)	2.0(A01)

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