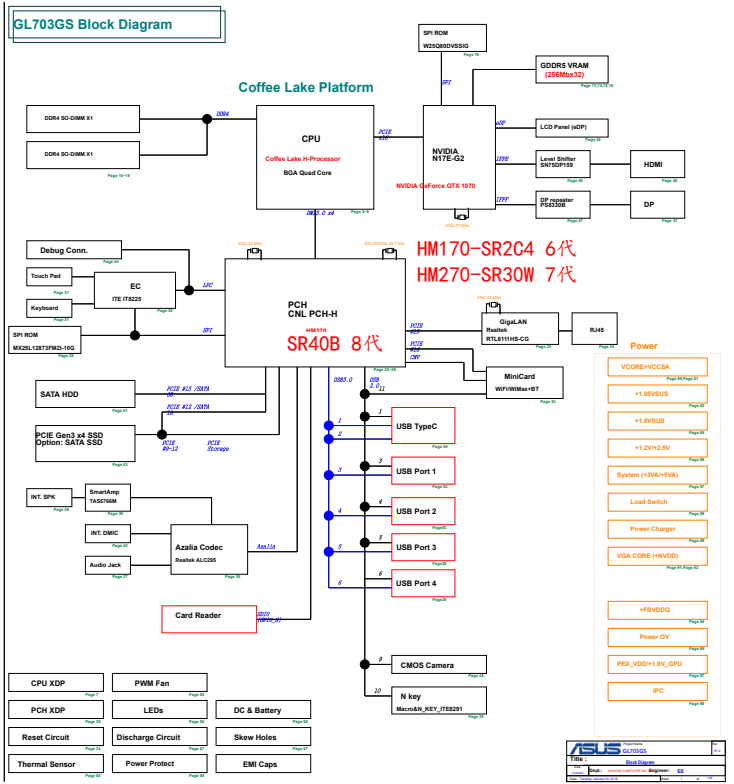
01. Block Diagram
02. System Setting
03. CPU_DMI/PEG/eDP/DDI
04. CPU_DDR4
05. CPU_GND
06. CPU_CFG/RSVD
07. CPU_KEY
08. CPU_PWR
09. CPU_PWR
10. CPU_POWER_CAP
14. DIM_DDR4 SO-DIMM A(0)
15. DIM_DDR4 SO-DIMM B(0)
18. DIM_CA/DQ Voltage
20. PCH-CPF(1)_IHDA/RTC/JTA
21. PCH-CPF(2)_PCIE/USB2/MISC
22. PCH-CPF(3)_CLK/LPC/USB3
23. PCH-CPF(4)_CKT/eSPI/SPI
24. PCH-CPF(5)_SPI, CNV
25. PCH-CPF(6)_GPIO
26. PCH-CPF(7)_POWER/GND
27. PCH-CPF(8)_POWER/GND
28. PCH-SPI ROM/OTH
29. PCH-KEY
30. KBC_ITE225
31. KBC_EN/TP
32. RST_Reset Circuit
33. LAN_RTL8111H-CG
34. LAN_RJ45 CON
35. Macro4N_KEY_ITE8291
36. AUD-ALC295CG
37. AUD-Headphone
38. USB3.0 port
39. AUD-Speaker
40. M2FF_SSD
43. CB_GL3213
44. DEBUG_LPC
45. CRT_eDP
47. Diaport Port
48. HDMI
50. FAN_Thermal Sensor & Fan
52. USB Charger
53. M2FF Type_WLAN&BT
56. LED/Switch
57. DSG_Discharge
58. Power Protect
60. DC/BAT IN
67. screw hold
69. OTH_EMC
70. GPU_PCIE I/F
71. GPU_POWER
72. GPU_FRAME BUFFER
73. VRAM-CHANNEL A
74. VRAM-CHANNEL B
75. VRAM-CHANNEL C
76. VRAM-CHANNEL D
77. VRAM CAP/DQ1905
78. GPU_CLOCK/STRAP/GPIO
79. GPU_LVDS/HDMI/Edp/DP/CRT
80. PW_KABYLAKE (1)
81. PW_KABYLAKE (2)
83. PW_+1.05VSUS
84. PW_+1.8VSUS
86. PW_1.2V/+VTT/2.5V
87. PW_+3VADM/+5VSUS
88. PW_LOAD Switch
89. PW_CHARGER
90. PW_PROTECTION
91. PW_+8VVDD (1)
92. PW_+8VVDD (2)
93. PW_+8VVDDQ
94. PW_+PSVDDQ
96. +12VS_FAN
98. PW_IPC
99. PW_FLOW CHART
100. Power On Timing--AC mode
101. Power On Timing--DC mode
102. History

GL703GS Block Diagram



ASUS	Project Name: GL703GS		Rev:
Title: Block Diagram			
Issued Date: 2017-08-15	Deciphered Date: 2017-08-15	Engineer:	
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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	GPO	(N.C)			
GPP_A12	GPI	GPO	(N.C)			
GPP_A13	SUSWARN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	(N.C)			
GPP_A17	GPI	GPO	GPP_A17_SD_PWREN			
GPP_A18	GPI	GPO	(N.C)			
GPP_A19	GPI	GPO	(N.C)			
GPP_A20	GPI	GPO	(N.C)			
GPP_A21	GPI	GPO	(N.C)			
GPP_A22	GPI	GPO	(N.C)			
GPP_A23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPO	(N.C)			
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K(@)	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K(@)	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLK_REQ5#/		PU 10K	+3VSUS
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	GPI	PCH_GPPB15/KB_LANG_ID0		PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPPB16/KB_LANG_ID1		PU 10K	+3VS
GPP_B17	GPI	GPO	PCH_GPPB17/XBOX_WRST		PD 10K	
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/GPUEVENT#_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/GC6FBEN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2_BT_UART_WAKE_N	PD	PU 4.7K	+3V_NGFF_WLAN
GPP_C3	SML0CLK	Native	SML0_CLK (Reserved)		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT (Reserved)		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	SML1CLK	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	SML1DATA	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	(N.C)			
GPP_C9	GPI	GPO	(N.C)			
GPP_C10	GPI	GPO	(N.C)			
GPP_C11	GPI	GPO	WLAN_ON#		PD 100K	
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NPC_ID		PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS_NV
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPO	(N.C)			
GPP_D3	GPI	GPO	(N.C)			
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	Native3	PCH_GPPD5/M.2_BT_PCMFRM_CRF_RST_N		PD 75K	
GPP_D6	GPI	Native3	PCH_GPPD6/M.2_BT_PCMOUT_CLKREQ0		PD 75K(@)	
GPP_D7	GPI	GPO	PCH_GPPD7/M.2_BT_PCMIN		PD 100K(@)	
GPP_D8	GPI	GPO	PCH_GPPD8/M.2_BT_PCMCLK			
GPP_D9	GPI	GPO	(N.C)			
GPP_D10	GPI	GPO	(N.C)			
GPP_D11	GPI	GPO	(N.C)			
GPP_D12	GPI	GPO	(N.C)			
GPP_D13	GPI	GPO	(N.C)			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	SATAPCIE_DET0		PU 10K(@)	+3VS
GPP_E1	GPI	Native	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	Native	SATAPCIE_DET2		PU 10K(@)	+3VS
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPI	Native	SATA0_HDD1_DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_NGFF3_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	NGFF3_DEVSLP		PU 10K(@)	+3VSUS
GPP_E7	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	Native	SATAPCIE_DET3		PU 10K(@)	+3VS
GPP_F1	GPI	Native	SATAPCIE_DET4		PU 10K	+3VS
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	(N.C)			
GPP_F6	GPI	GPO	(N.C)			
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPO	(N.C)			
GPP_F20	GPI	GPO	(N.C)			
GPP_F21	GPI	GPO	(N.C)			
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	PCH_GPPF23		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPO	(N.C)			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLK_REQ6#/CLKREQ6_NGFF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#/CLKREQ7_NGFF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#/CLKREQ8_NGFF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K(@)	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K(@)	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K(@)	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K(@)	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K(@)	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K(@)	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K(@)	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD	PD 20K(@)	
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	SML3ALERT#		PU 100K	+3VSUS
GPP_H16	GPI	GPI	RBID_0			
GPP_H17	GPI	GPI	RBID_1			
GPP_H18	GPI	GPI	RBID_2			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	(N.C)			
GPP_I1	GPI	GPO	(N.C)			
GPP_I2	GPI	GPO	(N.C)			
GPP_I3	GPI	GPO	(N.C)			
GPP_I4	GPI	GPO	EDP_HPD		PD 100K	
GPP_I5	GPI	GPO	(N.C)			
GPP_I6	GPO	GPO	(N.C)			
GPP_I7	GPI	GPO	(N.C)			
GPP_I8	GPO	GPO	(N.C)			
GPP_I9	GPI	GPO	(N.C)			
GPP_I10	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPI	GPO	(N.C)			
GPP_J1	CPU_VCCIO_PWR_GATE#	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPI	GPO	(N.C)			
GPP_J3	GPI	GPO	(N.C)			
GPP_J4	CNV_BRI_DT	Native	CNV_BRI_DT		PU 4.7K	+1.8VSUS
GPP_J5	CNV_BRI_RSP	Native	CNV_BRI_RSP		PU 20K(@)	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		PD 75K	
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J8	GPI	GPO	(N.C)			
GPP_J9	GPO	GPO	(N.C)			
GPP_J10	GPI	GPO	(N.C)			
GPP_J11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPI	GPO	GPIO_3_FORCE_PWR		PD 100K	
GPP_K1	GPI	GPI	PCB_ID0		PD 10K	
GPP_K2	GPI	GPI	PCB_ID1		PD 10K	
GPP_K3	GPI	GPO	GPP_K3/WLAN_BT_LED		PD 100K	
GPP_K4	GPI	GPO	GPP_K4/WLAN_LED		PD 100K	
GPP_K5	GPI	GPO	VOL_DOWN#(N.C)			
GPP_K6	GPI	GPO	VOL_UP#(N.C)			
GPP_K7	GPI	GPO	(N.C)			
GPP_K8	Reserved	GPO	(N.C)			
GPP_K9	Reserved	GPO	(N.C)			
GPP_K10	Reserved	GPO	(N.C)			
GPP_K11	Reserved	GPO	(N.C)			
GPP_K12	GPI	GPO	(N.C)			
GPP_K13	GPI	GPO	(N.C)			
GPP_K14	GPI	GPO	(N.C)			
GPP_K15	GPI	GPO	(N.C)			
GPP_K16	GPI	GPO	(N.C)			
GPP_K17	GPI	GPO	(N.C)			
GPP_K18	GPI	GPO	(N.C)			
GPP_K19	GPI	GPO	(N.C)			
GPP_K20	Reserved	GPO	(N.C)			
GPP_K21	Reserved	GPO	(N.C)			
GPP_K22	GPI	GPO	(N.C)			
GPP_K23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#(N.C)		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A# (N.C)			
GPD7	GPO	GPO	PCH_GPD7		PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN# (N.C)			
GPD10	SLP_S5#	Native	SLP_S5# (N.C)			
GPD11	LANPHYPC	GPO	LAN_PWREN (N.C)		PU 10K(@)	+3VA_DSW

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	O	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	O	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	EC_GPB5/NKey_WRST	PD 10K	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K(@)	+3VSUS
GPC4	I	GPI	EC_GPC4/PM_SUSB#	PD 100K	
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7/NKEY_PWR_EN	PD 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPO	EC_GPD0/EC_OV_DDR		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN1_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	O	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	CAP_LED#		
GPF1	O	GPO	NUM_LED#		
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PD 10K(@)	
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	O	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#	PD 100K(@)	
GPI1	I	GPI	3VSUS_PWRGD	PU 100K	+3VSUS
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#	PU 10K(@)	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 270K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPO	EC_GPJ0		
GPJ1	O	GPI	GC6FBEN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/TBTA_I2C_INT_EC		
GPJ3	O	GPO	EC_GPJ3/USB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_5VBUS		
GPJ5	O	GPI	EC_GPJ5/MB_DOCK_JACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	NKEY_INT#	PU 10K	+3VA_DSW_NKeyPWR
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

GL703GS Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
GPU INT. Thermal sensor	9Eh, 9Ch
CPU Thermal Sensor	90h
TI_TAS5766M*2	98h, 9Ah
ASM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	7Eh, 7Ch, 7Ah, 78h, 76h

Device Identification

CPU Thermal Sensor		
1st	[illegible]	NCT7717U
2nd		

GPU Thermistor		
1st	[illegible]	[illegible]
2nd		

USB3.0/PCIE/SATA Setting		
1	USB3#1	
2	USB3#2	
3	USB3#3	USB Port1
4	USB3#4	
5	USB3#5	USB Port3
6	USB3#6	USB Port4
7	USB3#7	Card Reader
8	PCIE#2	
9	PCIE#3	
10	PCIE#4	
11	PCIE#5	ThunderBolt x4
12	PCIE#6	
13	PCIE#7	
14	PCIE#8	
15	PCIE#9	PCIE3.0 x 4 SSD
16	PCIE#10	
17	PCIE#11	
18	PCIE#12	
19	PCIE#13(SATA0B)	SATA HDD
20	PCIE#14(SATA1B)	
21	PCIE#15	GLAN
22	PCIE#16	WLAN_11AC
23	PCIE#17	PCIE3.0 x 4 SSD
24	PCIE#18	
25	PCIE#19	
26	PCIE#20	
27	PCIE#21	PCIE3.0 x 4 SSD
28	PCIE#22	
29	PCIE#23	
30	PCIE#24	

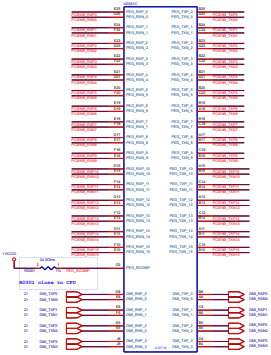
USB2.0 Setting		
1	USB2#1	
2	USB2#2	
3	USB2#3	USB Port1
4	USB2#4	
5	USB2#5	USB Port3
6	USB2#6	USB Port4
7	USB2#7	Card Reader
8	USB2#8	XBOX WLAN
9	USB2#9	Camera
10	USB2#10	N-Key
11	USB2#11	BT
12	USB2#12	Tobii IS4
13	USB2#13	TBT
14	USB2#14	

571391_CFL_H_PDG_Rev0p71, page 230

571182_CNL_PCH_H_EDS_Vol_1_Rev_0_7, page24

GL703GS
System Setting
NB1 RD2 EE1

PCIEG



Refer to CPL-H EDS P.155 (Doc.570825)

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

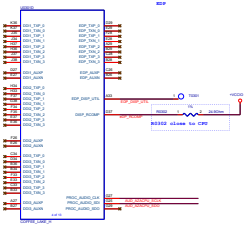
Bifurcation	Link Width			CFG Signals			Lanes													
	0-1-0	0-1-1	0-1-2	CFG [4]	CFG [1]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	F	E	D	C	B	A	9	8
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	B	A	9	8	7	6	5	4	3	2	1	0

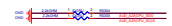
Notes:
1. For CFG bus details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device should use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device should use lanes 0:3, and other 2 lanes device should use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device should use lanes 0:3, two lane device should use lanes 8:9, one lane device should use lane 12.
4. for reversal lanes, for example:
   When using 1x8, the 8 lane device should use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
5. For Basin Falls platform use 1x8+2x4 Bifurcation

Main Board

Display





Refer to CPL-H EDS P.263 (Doc.571391)

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

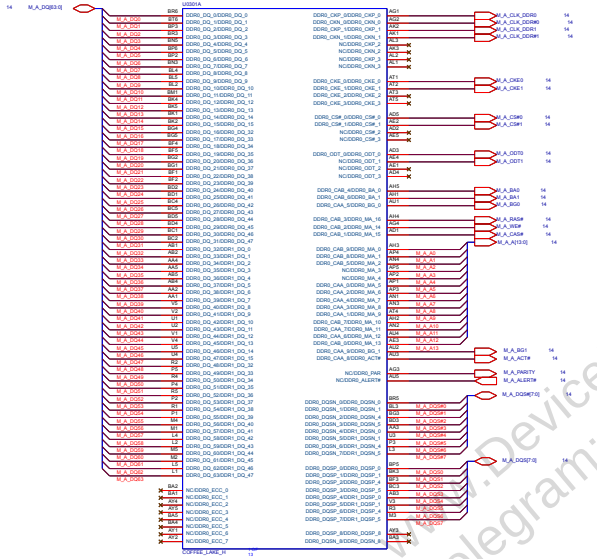
When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

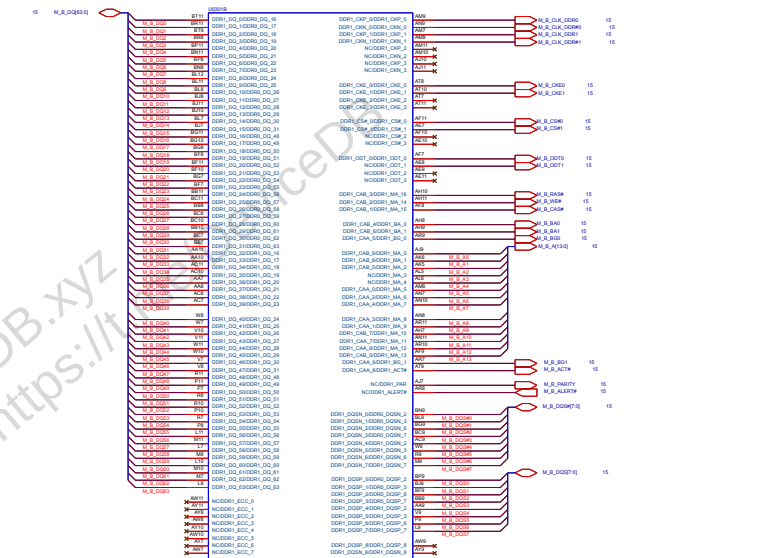
ASUS	Project Name: GL703GS			Rev: 30.0
TITLE :	DVI_SNK/HDMI/eDP/DP			
Size:	Dept.: ASUSTeK COMPUTER	Engineer:	EE	
Date: Tuesday, January 02, 2018		Sheet: 3	of: 100	

Main Board

Memory Channel A

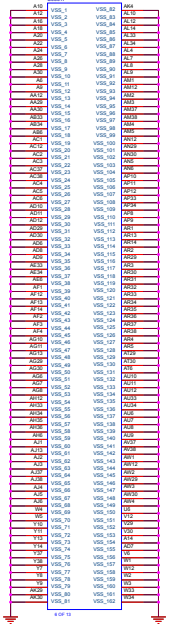


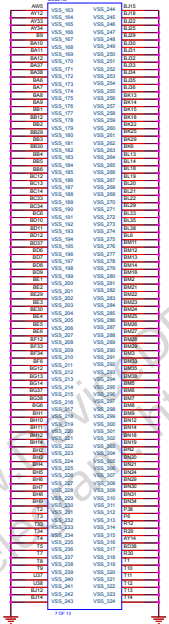
Memory Channel B

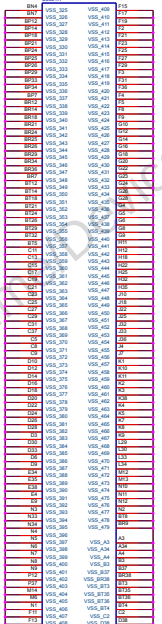


ASUS	Project Name: GL703GS		Rev: R1.4
Title : CPU_DDR4			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, January 30, 2018	Sheet 4 of 101		

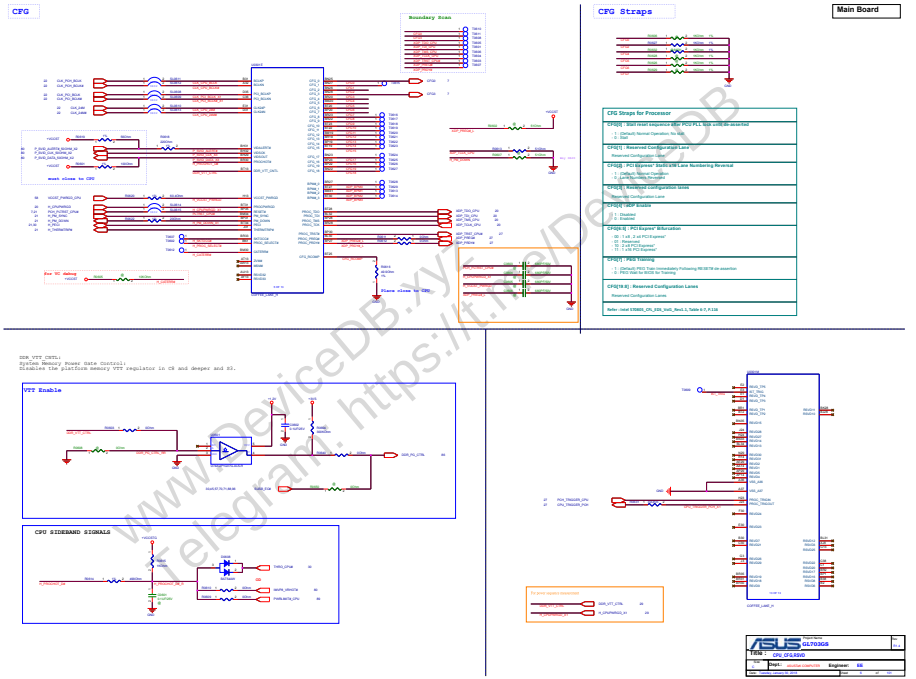
Main Board

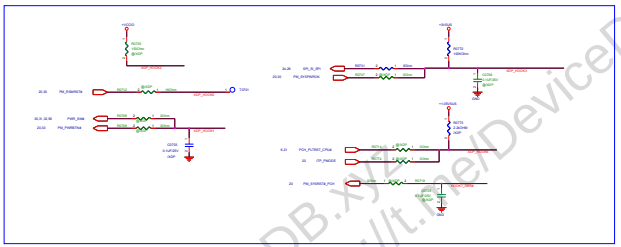






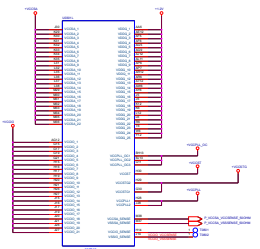
ASUS	Project Name: GL703GS		Rev: R1.4
Title : CPU_GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, January 30, 2018	Sheet: 5	of: 101	

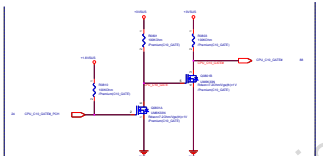




ASUS	Project Name: GL703GS		Rev: 0x1
Title : CPU XDP			
Size:	Dwg.:	Engineer: EE	
Date: Tuesday, January 09, 2018	Sheet 1 of 120		

Main Board



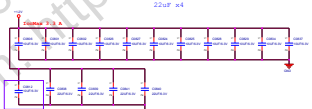


Configuration		Estimated Sst Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	DPL-R
VccST off in S3	On in S3	+28.35mW
VccPLL_OC off in S0/S3	On in S0/S3	+3.15mW
VccPLL_OC off in S5+	On in S5+	+3.15mW

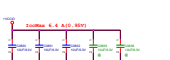
Main Source	1st PWR	2nd PWR	3rd PWR
	+VCCST	+1.05V_VCCST	
+1.05VSPD	+VCCSTG	+1.05V_VCCPLL	
+1.2V	+VDDQ_CPU		
AC_BAT_SYS	+VCCPLL_OC		
+VCCSA			
+VCCIO			

+VCCST/+VCCPLL
DECAPS Place Back Side (TOP)

+VDDQ DECAPS Place Back Side (TOP)



+VCCIO DECAPS Place Back Side (TOP)



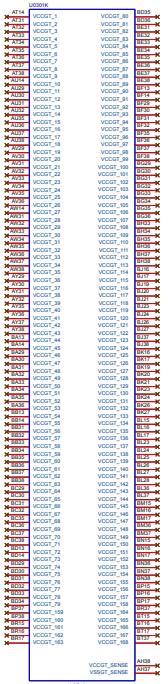
+VCCPLL_OC DECAPS Place Back Side (TOP)

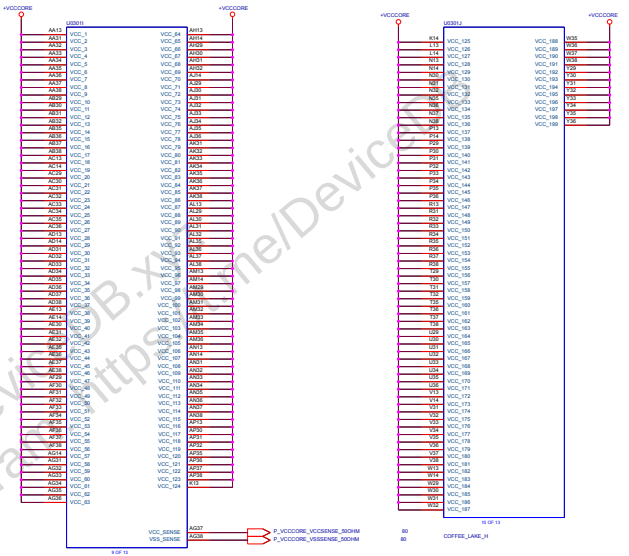
+VCCSA DECAPS Place Back Side (TOP)

+VCCSTG DECAPS Place Back Side (TOP)

+VCCSA cap near CPU

ASUSTeK Computer Inc.
GL703GS
Title : CPU_PWR
Size: Document Number: Rev:
Date: Sheet of
Engineer:

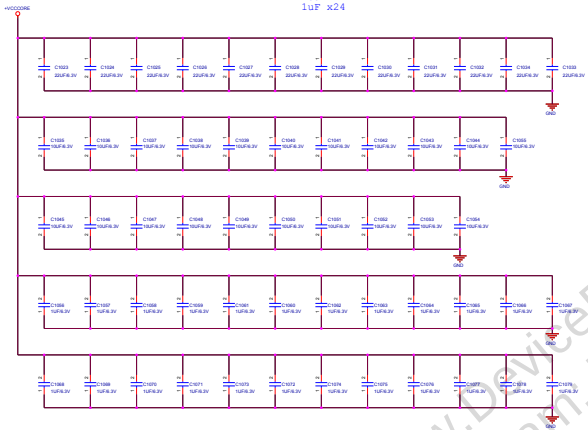




ASUS	Project Name: GL703GS		Rev: R1.4
Title : CPU_PWR			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, January 30, 2018		Sheet 9 of 101	

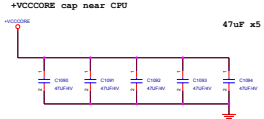
+VCCCORE DECAPS Place Back Side (TOP)

22uF x12
10uF x21
1uF x24



+VCCCORE cap near CPU

47uF x5

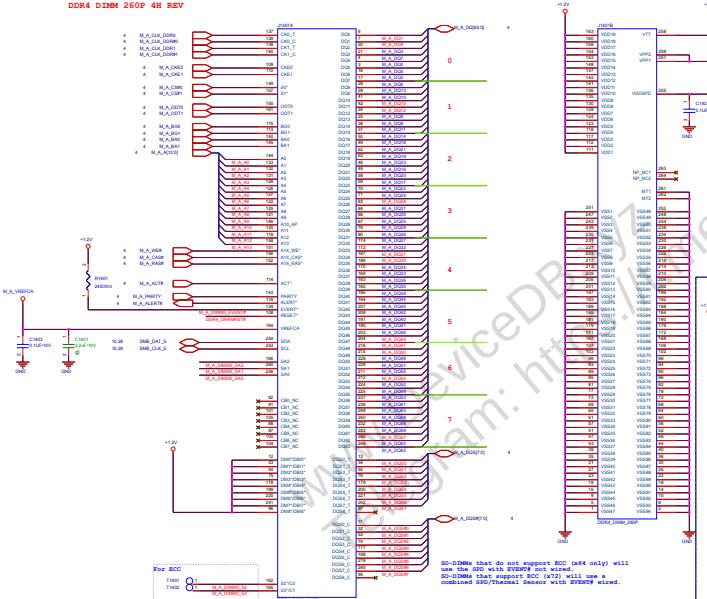


ASUS	Project Name: GL703GS	Rev: R1.4
Title :	010_CPU_POWER_CAP	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Tuesday, January 30, 2018	Sheet 10 of 101	

Main Board

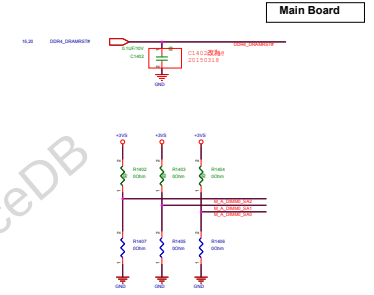
SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

12002-00080600
DDR4 DIMM 260P 4H REV



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT#P not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A POLL UP IF NO PIN IN PCH



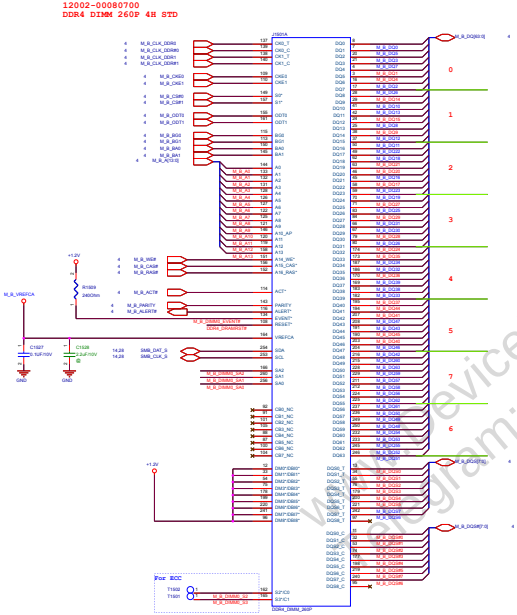
Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

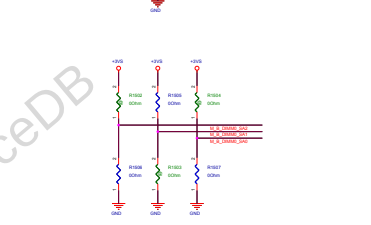
Project Name	GL703GS	Rev: R1A
Title :	DIM_DDR4 SO-DIMM A1	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, January 30, 2018	Sheet 14 of 101	

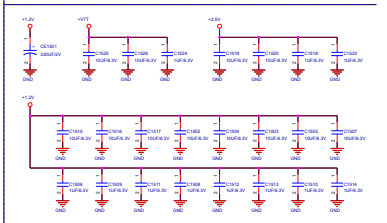
Main Board

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1501)

12002-00080700
DDR4 DIMM 260P 4H STD





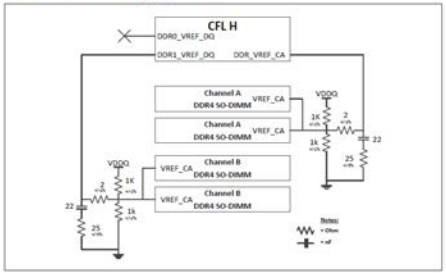


Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

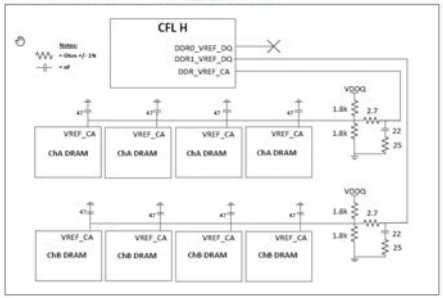
ASUS	Project Name: GL703GS	Rev: 90.4
Title : DIM_DDR4 SO-DIMM B1		
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE
Date: Tuesday, January 30, 2018	Sheet: 19 of 101	

Main Board

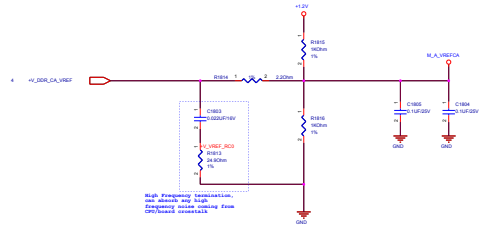
CFL H DDR4 SO-DIMM V_{REF-CA} Overview



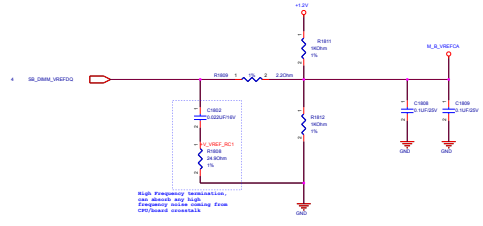
CFL H DDR4 x16 Memory Down V_{REF-CA} Overview



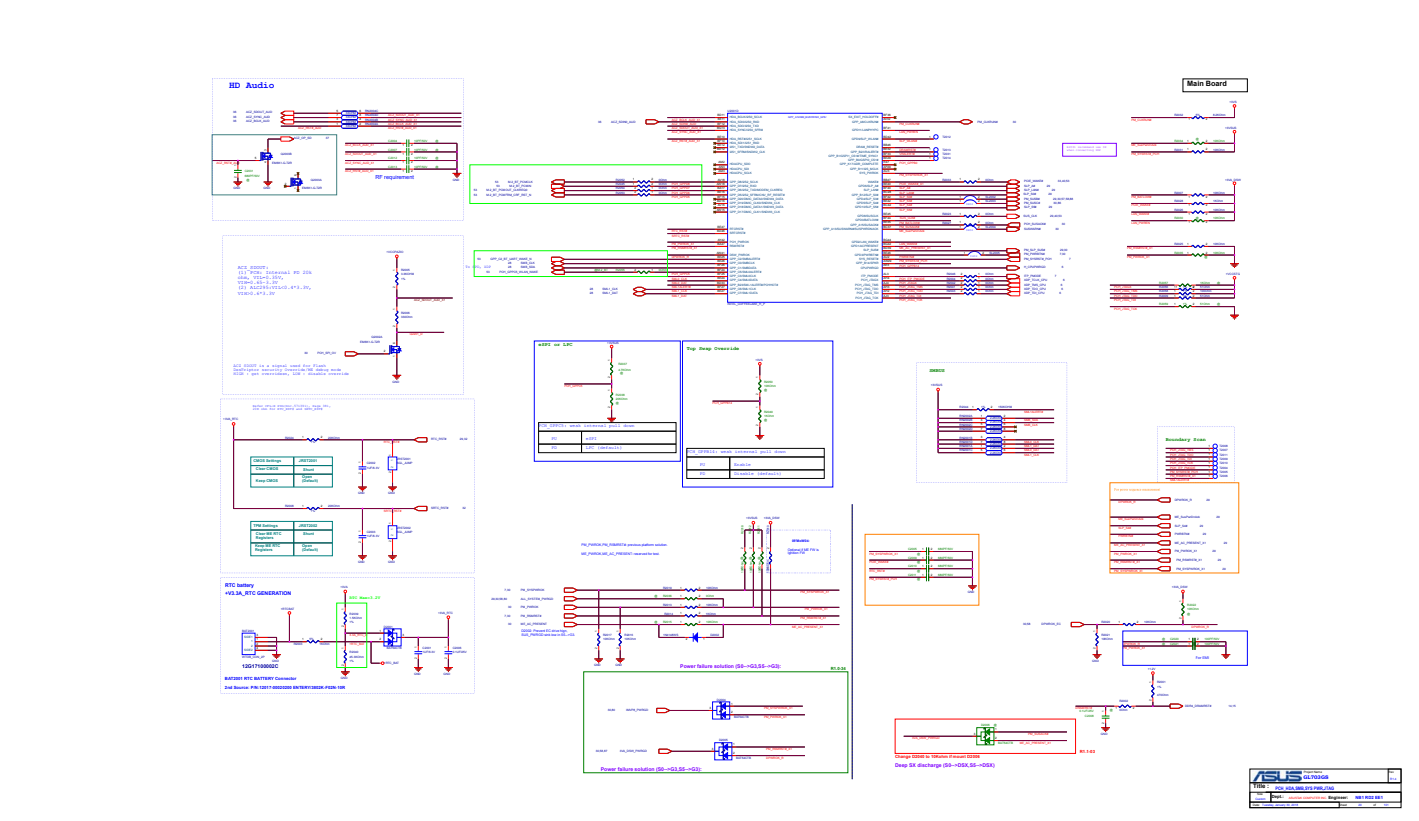
SO-DIMM0 Vref



SO-DIMM1 Vref



ASUS	Project Name: GL703GS		Rev: R1.4
Title : DIM_CA/DQ Voltage			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, January 30, 2018	Sheet 18 of 101		


HD Audio
Main Board
RF requirement
ACE 9320?:
Enable: bidirectional PD 20k
vdig, VIH=1.05V,
VIH=0.45~3.3V
123.8x235.9?1x0.4?3.3V,
vtrans/.4?3.9V
ACE 9320? is a signal used for Flash
ROM to enter recovery mode or debug mode
9320 (get recovery, 120) disable override
eSPI vs LPC
Top Swap Override
Boundary Scan
RTC battery
+V3.3A_RTC GENERATION
12G171000020
BAT3201 RTC BATTERY Connector
2nd Source: P/N:12017-000200000 EINTEK/Y3302K-P2CN-10R
Power failure solution (S0-->G3,S5-->G3):
Power failure solution (S0-->G3,S5-->G3):
Deep S5 discharge (S5-->DSX,S5-->DSX)
Change 22066 to 19Kohm if circuit 22066
Title :
Size :
Project Name :
GL753GE
Rev :
Date :
Sheet
of
Engineer:
Wednesday, October 22, 2014
16:01:19

GL703GS Port Assignment

Main Board

USB Setting

USB 2.0	
USB2_01	USB3.1 type C
USB2_02	
USB2_03	USB3.0 type A
USB2_04	USB3.0 type A
USB2_05	USB3.0 type A
USB2_06	USB3.0 type A
USB2_07	Card Reader
USB2_08	
USB2_09	Camera
USB2_10	N-Key + KB BL control
USB2_11	BT
USB2_12	
USB2_13	
USB2_14	

USB 3.0	
USB3_01	USB3.1 type C
USB3_02	USB3.1 type C
USB3_03	USB3.0 type A
USB3_04	USB3.0 type A
USB3_05	USB3.0 type A
USB3_06	USB3.0 type A
USB3_07	Card Reader
USB3_08	

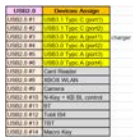
PCIE/SATA Function define

	Funcon	
PCIE-01 (USB3#7)	USB3 Card Reader	
PCIE-02 (USB3#8)		
PCIE-03 (USB3#9)		
PCIE-04 (USB3#10)		
PCIE-05		
PCIE-06		
PCIE-07		
PCIE-08		
PCIE-09		
PCIE-10	PCIE SSD (x4)	
PCIE-11 (SATA-0x)		
PCIE-12 (SATA-1x)		SATA SSD

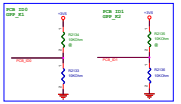
	Funcon
PCIE-13 (SATA-0b)	SATA HDD
PCIE-14 (SATA-1b)	
PCIE-15 (SATA-2)	GLAN
PCIE-16 (SATA-3)	WLAN-AC
PCIE-17 (SATA-4)	
PCIE-18 (SATA-5)	
PCIE-19 (SATA-6)	
PCIE-20 (SATA-7)	
PCIE-21	
PCIE-22	
PCIE-23	
PCIE-24	

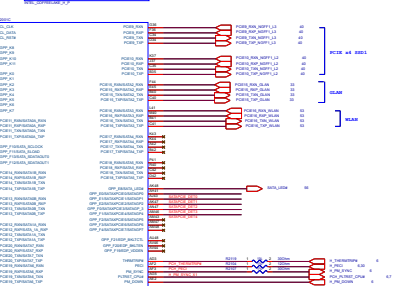
	Funcon
CLKREQ-0	DGPU
CLKREQ-1	
CLKREQ-2	WLAN-AC
CLKREQ-3	
CLKREQ-4	GLAN
CLKREQ-5	
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

Design IP



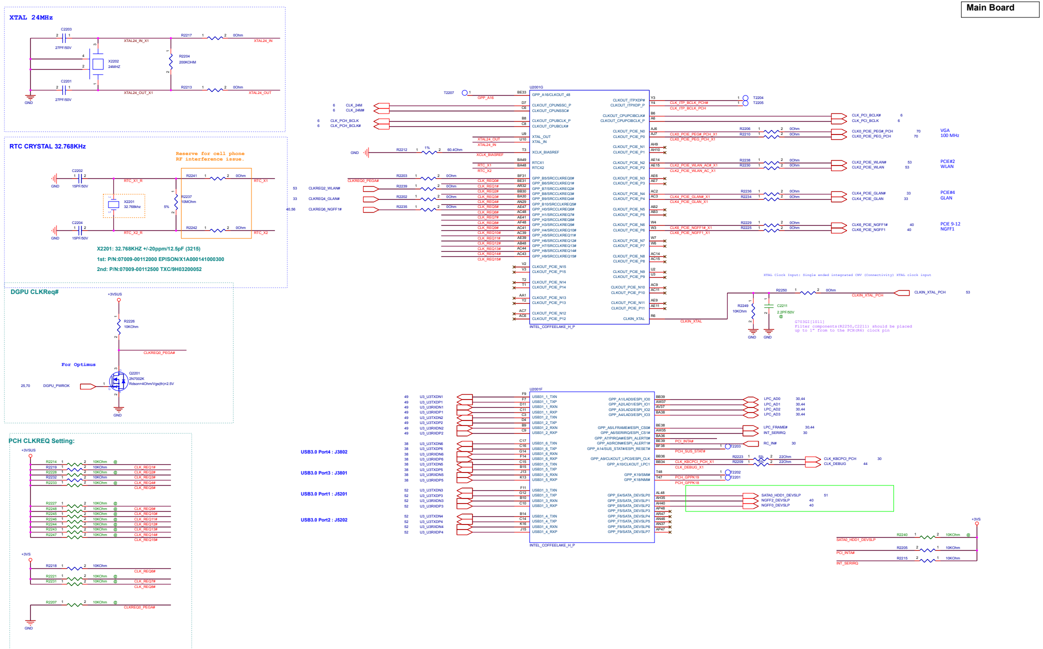
Design IP



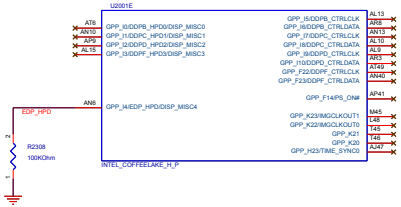


Title :	PCH_PCIE,SATA,USB2,MISC
Size:	Document Number: GL703GS
Date:	Tuesday, January 30, 2018
Sheet	21 of 101
Dept.:	Adv/Sft ComPuTER Inc Engineer:
	NB1 RD2 EE1

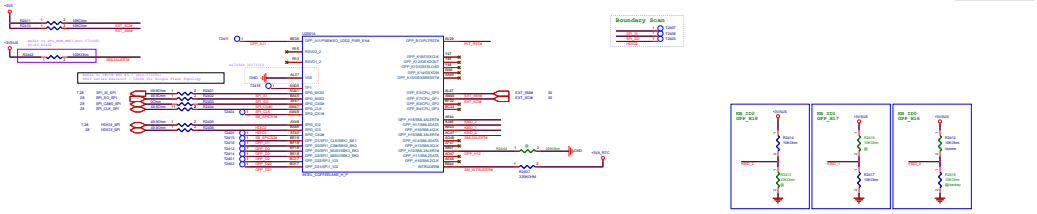
Main Board

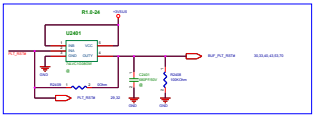


ASUS	Project Name: GL703GS	Rev: R1.4
Title : PCH_CLK,LPC,USB3		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Tuesday, January 30, 2018	Sheet 22 of 101	



Project Name: GL703GS			Rev: R1.4
Title : PCH-CPT(4)_eDP,PCI,DP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, January 30, 2018	Sheet 23 of 101		





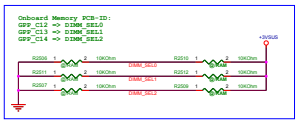
PCH Side (EPK 請依照此表格設計判斷)

Code	ROG RGB KB Type	KBD 2 (GPP_H18)	KBD 1 (GPP_H17)	KBD 0 (GPP_H16)
0x00	Non-RGB	H	H	H
0x01	RGB per Region via CAMERA/WASD modes	H	H	L
0x02	RGB per Region via 4 zones	H	L	H
0x03	RGB per key	H	L	L

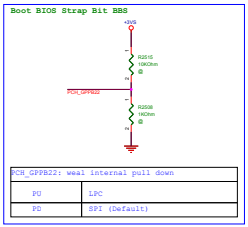
5. 需請 BIOS RD 在 KB ID 讀取的部分，額外加入 Reverse code，以符合第 1 點 table

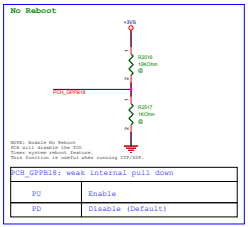
Title :	PCH-CPTS5_LPC3PLSMBUS		
Size:	Project Name: GL703GS	Rev:	
Date:	Sheet: of	Engineer:	EE

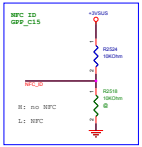
Main Board



	Hynix(2Gb)	XXX (2Gb)	Micron(2Gb)
DIMM_SEL0			
DIMM_SEL1			
DIMM_SEL2			

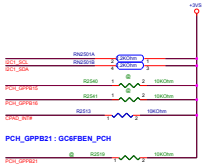


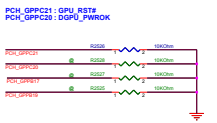




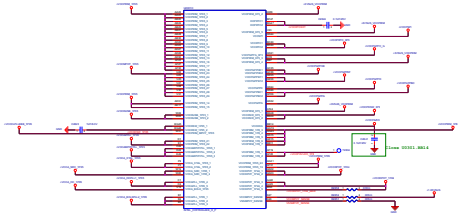
	US	UK	JP
KB_LANG_ID0 (KB pin33)	1	0	0
KB_LANG_ID1 (KB pin34)	0	0	1

US,PIN 33 NC , PIN 34 GND
UK,PIN 33,34 GND
JP,PIN 33 GND , PIN 34 NC



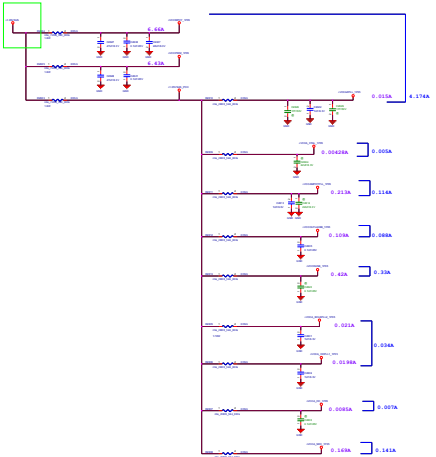


Project Name	GL703GS		Rev 0.1.4
Title :	PCH_GPIO		
Size B	Dept.: ASUSTeK COMPUTER INC	Engineer:	NB1 RD2 EE1
Date: Tuesday, January 30, 2018		Sheet 25	of 101

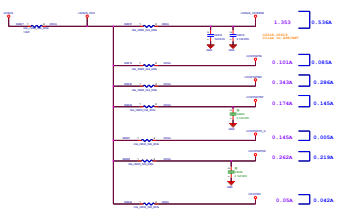


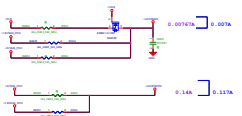
GPIO Voltage Level

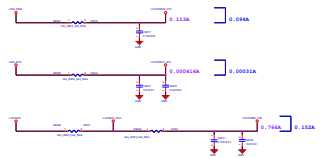
Group	Power pin	Power option	Power plane
GPP_A	VCCGPPA	3.3V	+3VSUS
GPP_B	VCCGPPBC	3.3V	+3VSUS
GPP_C	VCCGPPBC	3.3V	+3VSUS
GPP_D	VCCGPPD	1.8V or 3.3V	+1.8VSUS
GPP_E	VCCGPPEF	3.3V	+3VSUS
GPP_F	VCCGPPEF	3.3V	+3VSUS
GPP_G	VCCSPI, SUS Suswell	Internally tied to Vccspi 1.8/3.3V	+1.8VSUS or +3VSUS
GPP_H	VCCGPPH	3.3V	+3VSUS
GPP_I	VCCDSW_3P3	3.3V Only	+3VSUS
GPP_J	VCCDSW_1P8	1.8V Only	+1.8VSUS
GPP_K	VCCGPPHK	3.3V	+3VSUS
GPD	VCCSUS_3P3	3.3V Only	+3VA_DSW



Purple reference CRB
Blue reference EDS







ASUS	Project Name	UX703GXR	Rev
	Sheet Name	CB_PCH_POWER.DSN	
Size	Project	Engineer	MB1 REV 0X1
Date: Tuesday, June 04, 2019			Sheet of

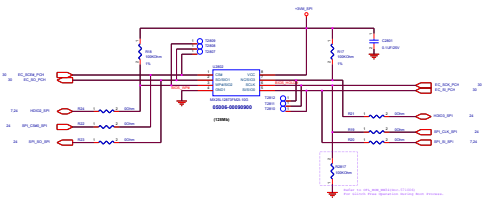
Main Board

Project Name: GL703GS			Rev: R1.4
Title: PCH_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, January 30, 2018	Sheet 27 of 101		

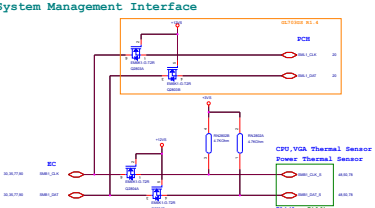
SPI Power

SPI ROM

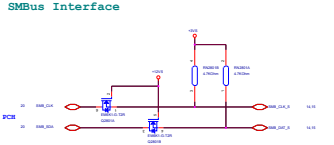
1st: 05006-00090900 FLASH MXIC MX25L12873FMZI-10G 128M SOP-8L

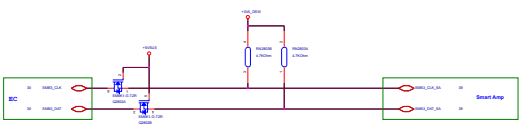


System Management Interface



SMBus Interface





Project Name: GL703GS			Rev: 1.0
Title : PCH-SPI ROM,DTH			
Size: Custom	Dept.: MB/PWR COMPUTER	Engineer: EE	
Date: Tuesday, January 03, 2017	Sheet 23 of 100		

For power sequence measurement

+1.0V_VCCPLL ----------> R0809

H_VCCST_PWRGD ----------> R0620

ASUS	Project Name: GL703GS		Rev: R1.4
Title : PCH-XDP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, January 30, 2018	Sheet 29 of 101		

EC 8225

Only 3V Torlence

GPE[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[3,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPJ5 [0:7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPC0~GPC7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

Power

R1.0-29

+3VS
+5VALW_EC
+3VALW_EC
+1.05VALW
+1.5VALW_EC
+1.8VSDC
+5VALW
+3VSDC
RC_SMAD

C3600 0.1uF/25V
C3601 0.1uF/25V
C3602 0.1uF/25V
C3603 0.1uF/25V
C3604 0.1uF/25V
C3605 0.1uF/25V
C3606 0.1uF/25V
C3607 0.1uF/25V
C3608 0.1uF/25V
C3609 0.1uF/25V
C3610 0.1uF/25V
C3611 0.1uF/25V

PU/PD

R1.0-34

+3VALW_EC
+5VALW
+1.5VALW_EC
+1.8VSDC
+3VSDC
+1.05VALW

for load code

ClickPad Schematic

ITE Version	ASUS P/N
IT8225VG/BX	04037-00260000

Thermal sensor

Battery

2013.08.21 EMI Modify

For EMI

2013.08.21 EMI Modify

For EMI

Close U3201

2013.12.29 EMI Modify

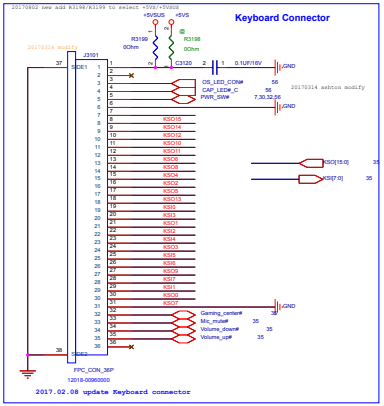
2014.01.15 EMI Modify

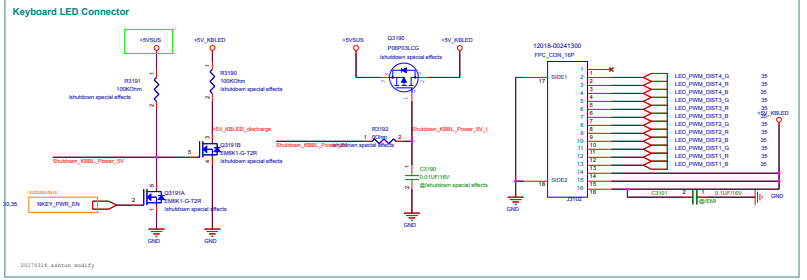
04037-00260300

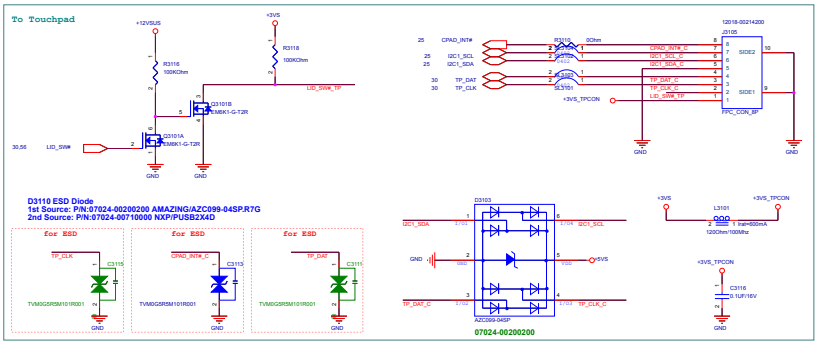
Title :	KBC IT8225		
Size:	Project Name:	GL703GS	Rev: 0.2
Date: Tuesday, January 21, 2014	Dept.: ASUS NB COMPUTER INC.	Engineer:	Sheet 25 of 50

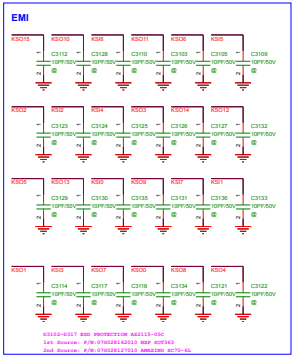
NB1 RD2 ED1

Main Board



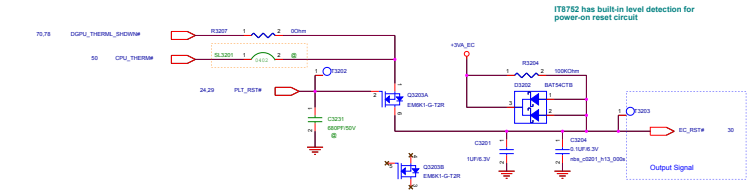




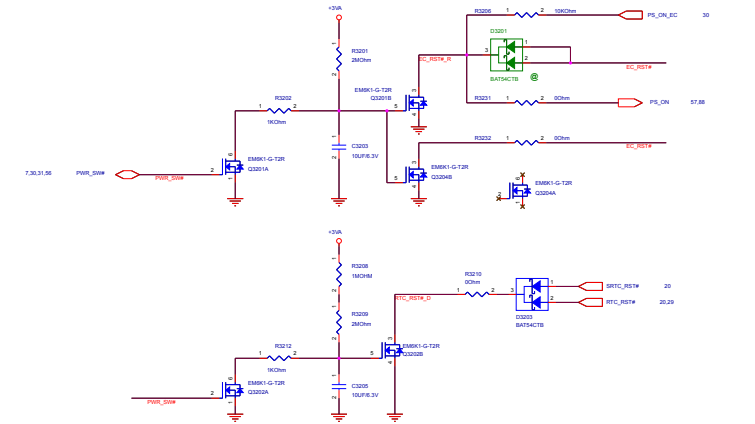


ASUSTeK COMPUTER	Title :	KBC_KB & TP	
	Engineer:	EE	
Size: B	Project Name: GL703GS		Rev: R1.4
Date: Tuesday, January 30, 2018	Sheet: 31 of 101		

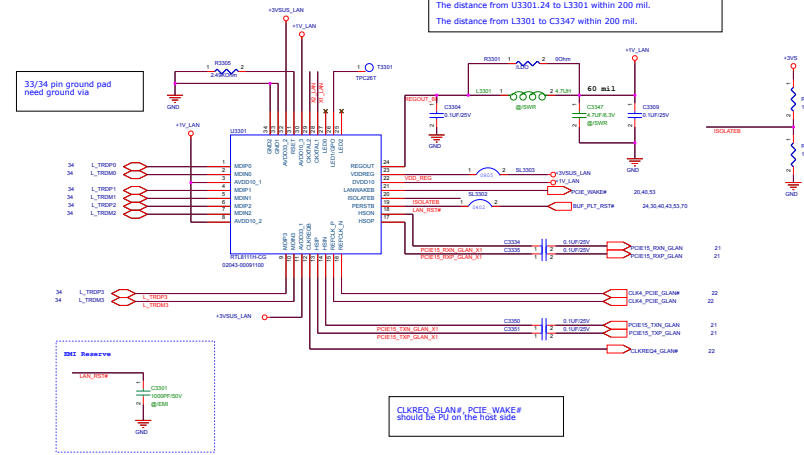
Thermal Policy

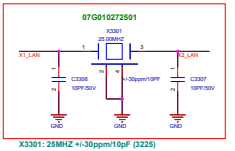


battery embedded (press pwr_sw 10sec, then reset ec)

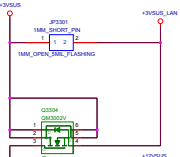


ASUS	Project Name: GL703GS		Rev: R1.4
Title : RST_Reset Circuit			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, January 30, 2018	Sheet: 32	of: 103	





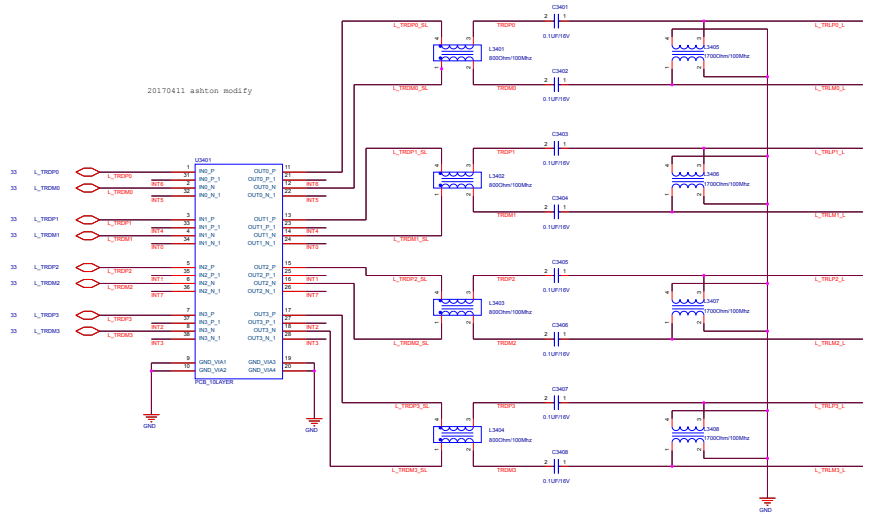
Realtek suggests 3V_LAN raise time >1ms



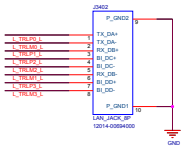
ASUS	Project Name: GL703GS		Rev: R1.4
Title : LAN RTL8111GUX-CG			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, January 30, 2018	Sheet: 33	of: 102	

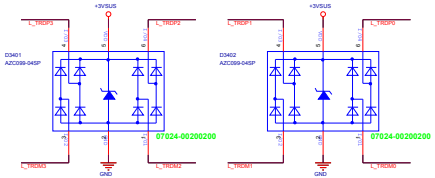
Main Board

Main Board



LAN Connector



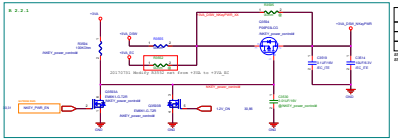


D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

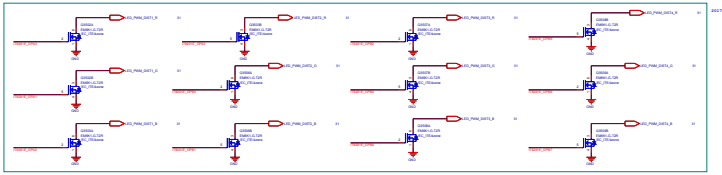
Project Name: GL703GS			Rev: R1.4
Title : LAN RJ45 Conn.			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, January 30, 2018	Sheet 34 of 102		

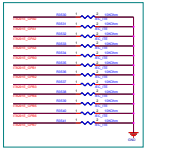


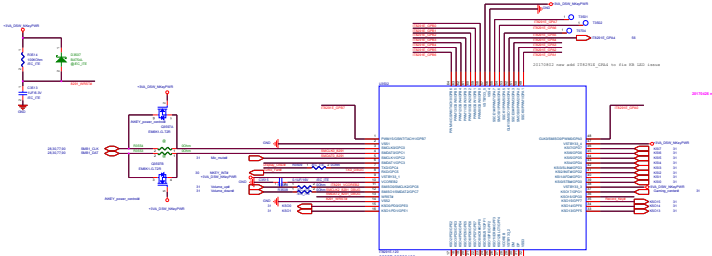
Options	S0	S3	S4/5	S5-	S5
3.3V_CM	1	1	1	0	0
EXT_PWR_EN	1	1	1	1	0
+3VA_CHG_VDby/PWR	1	0	1	1	0

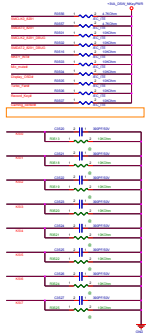
S5-: before shutdown special effects finish
S5: after shutdown special effects finish

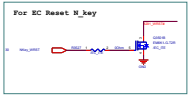
KB RGB LED

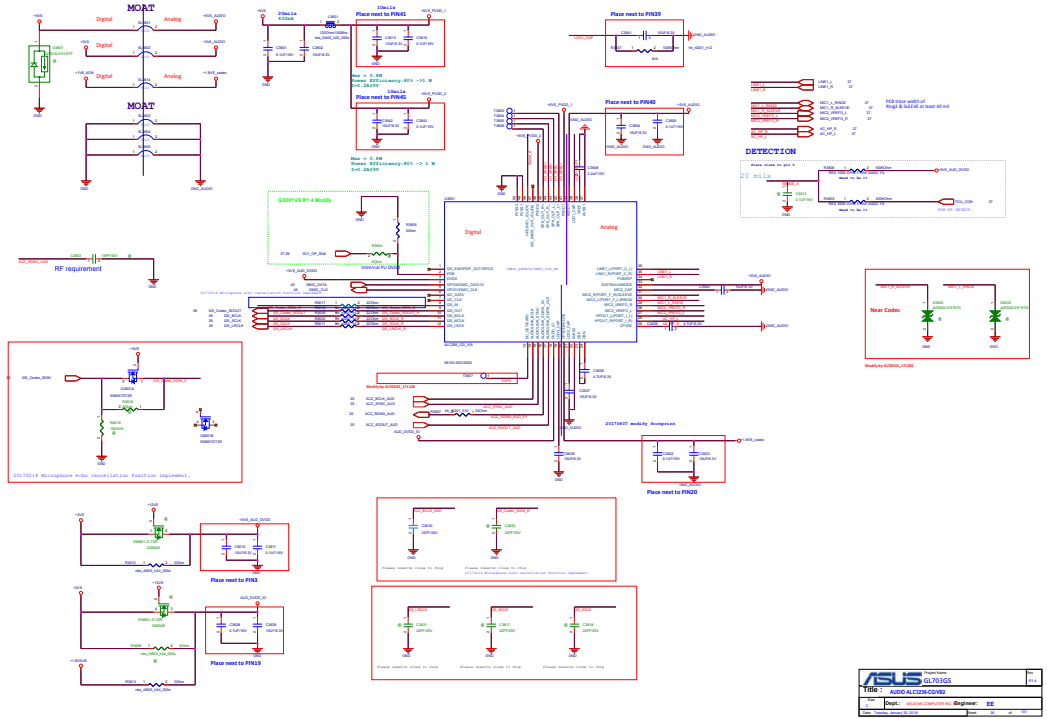






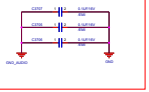


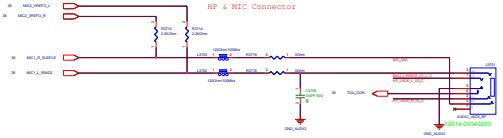



MOAT
Digital
Analog
MOAT
Place next to PIN61
Place next to PIN45
Place next to PIN39
Place next to PIN40
DETECTION
GX30IVS R1.4 Modify
RF requirement
Digital
Analog
Near Codec
Place next to PIN2
Place next to PIN19
Place next to PIN20
20170214 Microphone echo cancellation function implement.
20170607 modify footprint.
Please rewrite close to chip
ASUS
GL703GS
AUDIO AL1325-CGVB2
EE

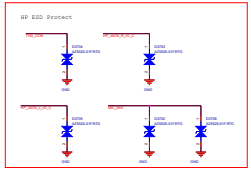
Headphone&MIC

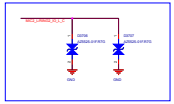
A_GND / GND





Main Board

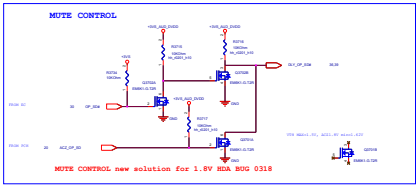




2015.12.16 EMI Reserve

2015.04.14 3 pole mic design and VR2 Reserve

2015.08.07 Realtek Support



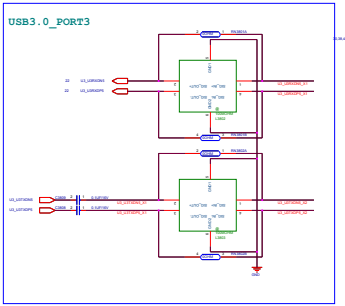
ASUS	Project Name: GL703GS		Rev: 00.A
Title: AUDIO ALC3236-CG/VR2 Jack			
Size:	Project: Skylake_Dis_Quanta_GL703_R1A	Engineer: EE	
Date: Tuesday, January 05, 2016	Sheet 37 of 43		

Main Board

USB3.0_PORT3

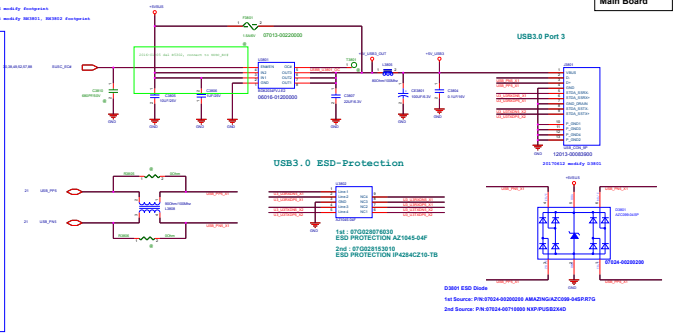
USB3.0 Common choke EMI-Protection

090092090400//090092090305//temp_T_021683



20170406 modify footprint

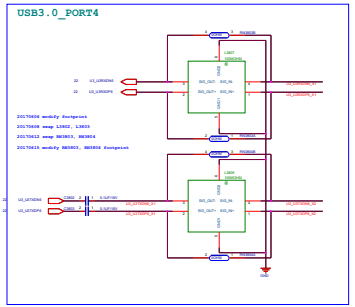
20170413 modify RB301, RB302 footprint



USB3.0_PORT4

USB3.0 Common choke EMI-Protection

090092090400//090092090305//temp_T_021683

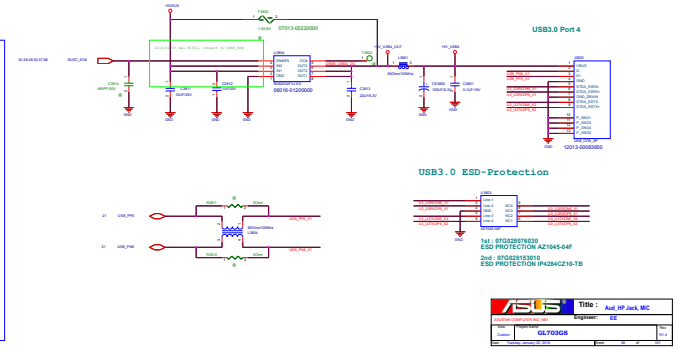


20170606 modify footprint

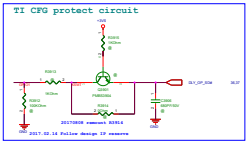
20170608 swap L3802, L3803

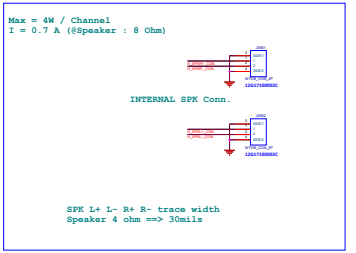
20170612 swap RB3801, RB3804

20170615 modify RB3803, RB3804 footprint



ASUSTeK COMPUTER INC. MB	Title :	Aud_HP Jack, MIC	
Size	Project Name	Engineer:	EE
Custom	GL703GS		Rev. 0U.2
Date: Tuesday, January 02, 2018	Sheet 38 of 47		



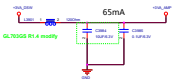


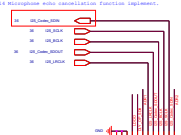
20170214 Microphone echo cancellation function implement.

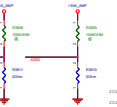
20170801 Modify L3902/L3903/L3904/L3906 P/N:0906-0223003 (103N) (fix EMI issue)

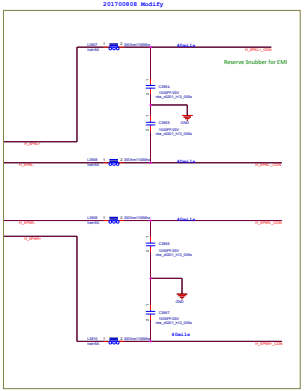
20170803 Modify C3954/C3955/C3956/C3957 type from 0201 to 0402 (满国工作为: 0.22UF/25V (0402))

20170803 remove Snubber for EMI

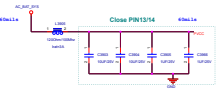


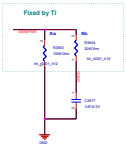


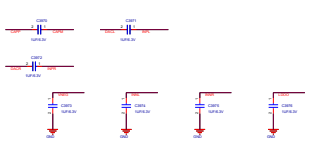




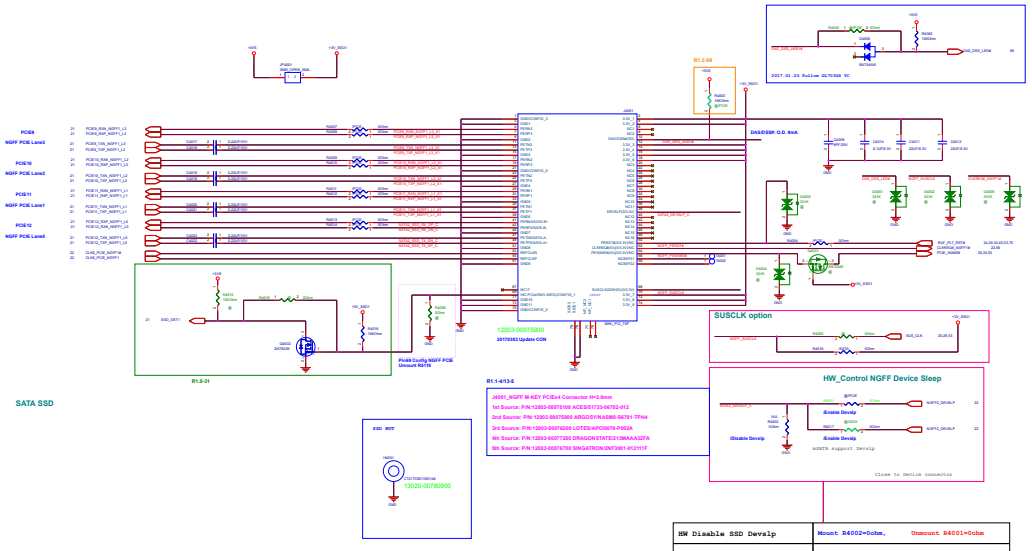
Max = 4W / Channel = 8W
Power Efficiancy:85% -> 9.5 W
I=1.05A@9V 0.8 A@12V 0.5A@19V







NGFF_SSD

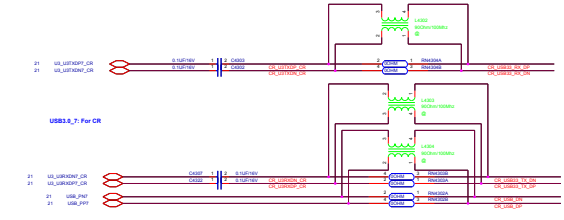


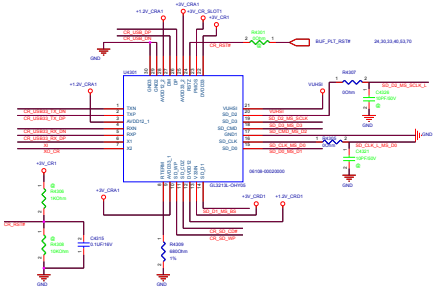
HW Disable SSD Devslp	Mount R4002=0ohm, Unmount R4001=0ohm
HW Enable SSD Devslp	Unmount R4002=0ohm, Mount R4001=0ohm

Title :	MiniCard SSD		
Engineer:	SC		
Size	Project Name		Rev
A	GL703GS		R1.0
Date: Tuesday, January 24, 2017	Sheet 33 of 39		

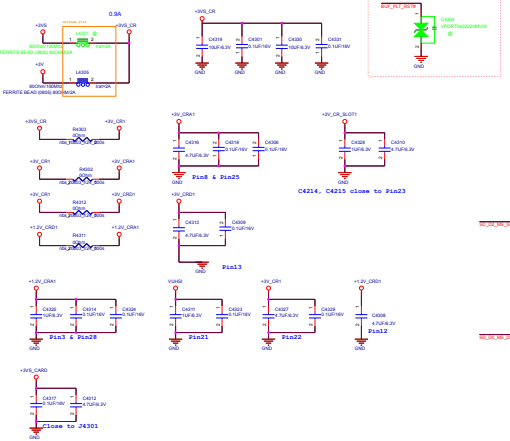
CR I/O Conn. (MB)

Main Board

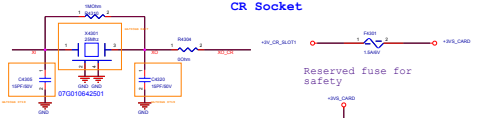




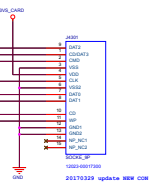
CardReader PWR



CR Socket

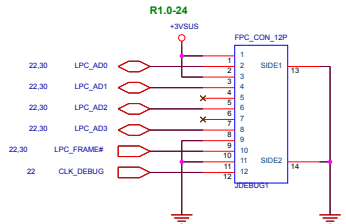


Reserved fuse for safety

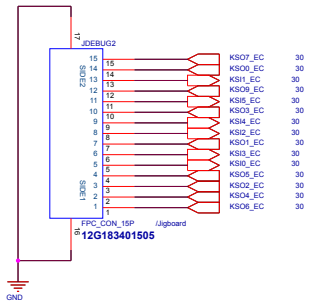


Project Name	GL703GS		Rev. 30.4
Title :	CB_CON		
Size: Custom	Dept.:	Engineer:	EE
Date: Tuesday, January 30, 2018	Sheet	43	of 101

LPC Debug Port



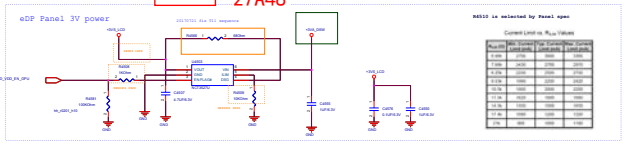
2016/03/21

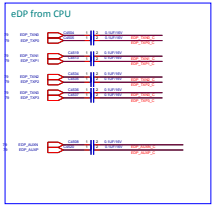


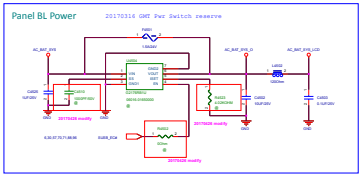
<Variant Name>

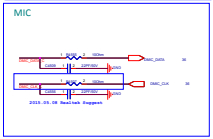
ASUSTeK COMPUTER INC. NB1	Title : DEBUG_LPC Engineer: EE	
Size: A	Project Name: GL703GS	Rev: R1.4
Date: Tuesday, January 30, 2018	Sheet 44 of 101	

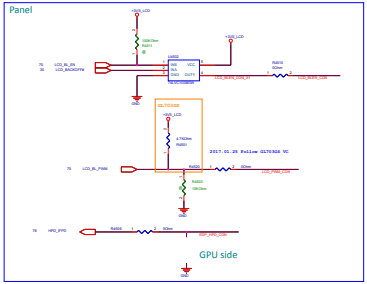
27A88 27A48

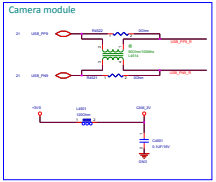


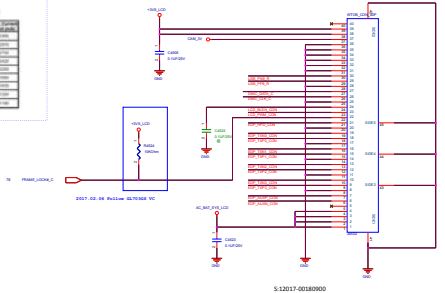


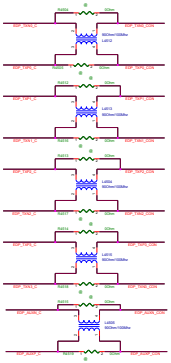


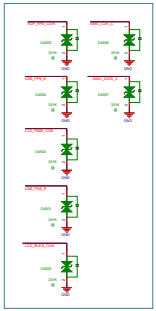












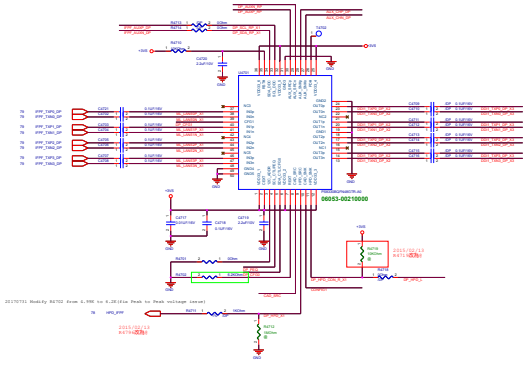
Title : CRT_eDP
Engineer: EE
GL703GS
Tuesday, January 03, 2017

Main Board

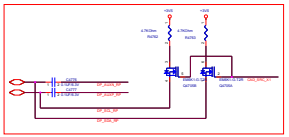
DP Repeater_PS8330B

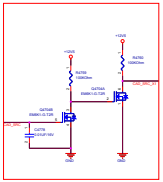
DP Repeater AUX_Sink Input

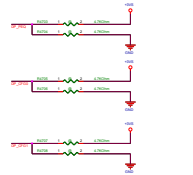
DP Repeater AUX_SRC Output



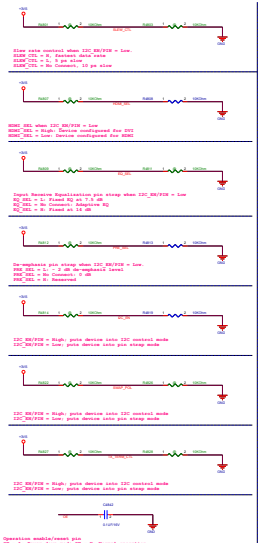
Fix MiniDP to HDMI Dongle No Display Issue



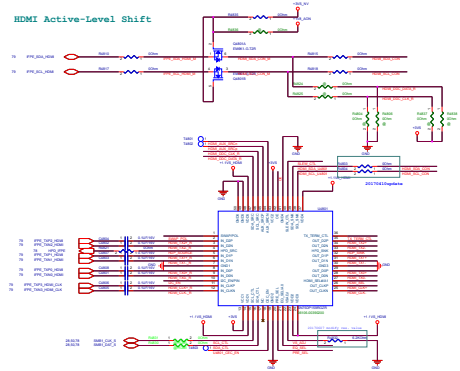


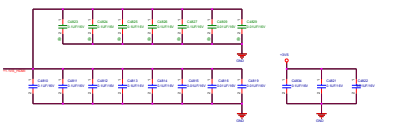


ASUS	Project Name: GL703GS		Rev: 1.0
Title :	Display Port Conn.		
Size: D	Dept.: MOTHER BOARD	Engineer:	
Date: Tuesday, January 30, 2018		Sheet 17 of 101	

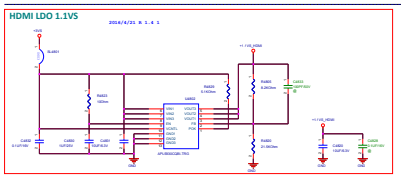


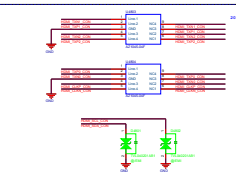
HDMI Active-Level Shift





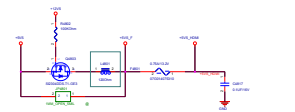
HDMI LDO 1.1VS





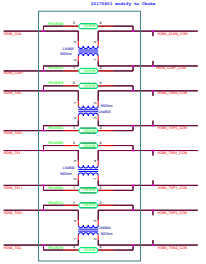
Main Board

HDMI PWR_+5VS_HDMI



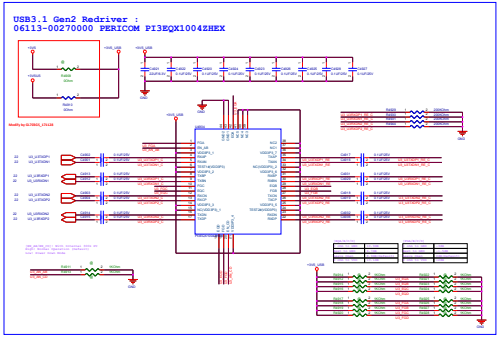
HDMI Conn.

HDMI EMI

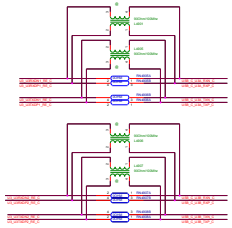


ASUS	Project Name: GL703GS		Rev: R1.1
Title: HDMI			
Size: Custom	Doc#: Wistron GM9YD0.M	Engineer: EE	
Date: Monday, January 30, 2017		Sheet 48 of 50	

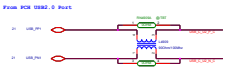
USB3.1 Gen2 Redriver : 06113-00270000 PERICOM PI3EQX1004ZHEX



From PCH USB3.0 EMI-Protection



USB2.0 EMI-Protection With ECMF(PCB 1.25mm_12Layer)



TI CC Logic SN1507044RVCR = TPS25810RVCR, DFP (Host), 5V / 1.5A

(ASUS Only Use)

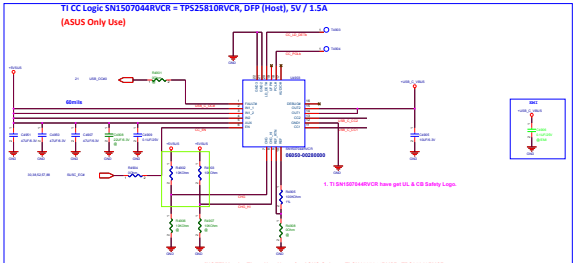
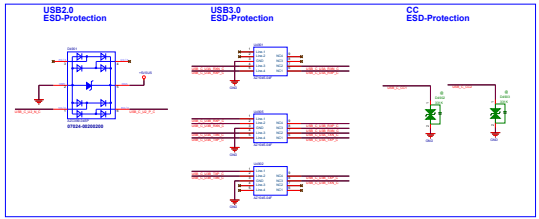


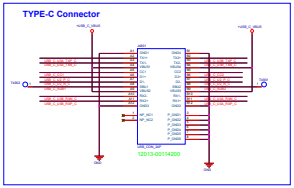
Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

USB2.0 ESD-Protection / USB3.0 ESD-Protection / CC ESD-Protection

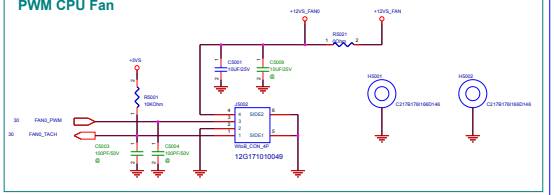


TYPE-C Connector

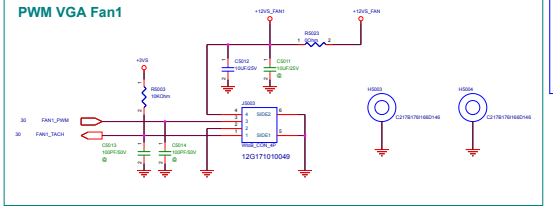


ASUS	Project: GL703GS		Rev:
Title : Type-C Port			
Size:	Dept.: ASUSTeK COMPUTER INC.	Engineer:	RDD_SD3
Date: Tuesday, January 10, 2017		Sheet 1 of 1	

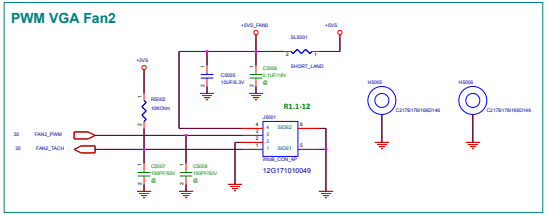
PWM CPU Fan



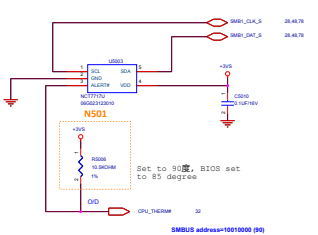
PWM VGA Fan1



PWM VGA Fan2



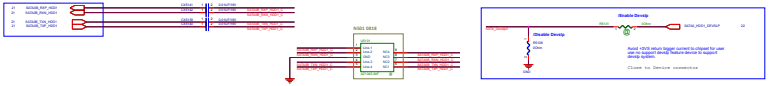
CPU Thermal Sensor

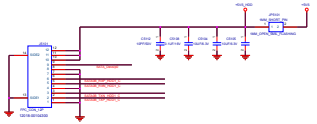


Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for
powr noise

ASUSTeK COMPUTER INC. NBT	Title : FAN_Thermal Sensor & Fan	
	Engineer: EE	
Size: Custom	Project Name: GL703GS	Rev: R1.4
Date: Tuesday, January 30, 2018	Sheet: 66 of 103	





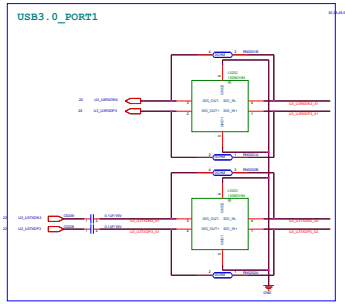
Variant Name:			
Title :	BDD, HDD & ODD CON		
Engineer:			
Size:	Project Name:		Rev:
Custom	GL703GS		0.1
Date:	Monday, January 04, 2016	Sheet	41 of 45

Main Board

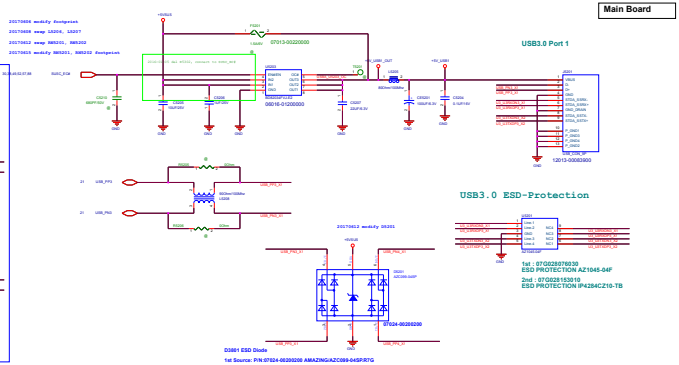
USB3.0_PORT1

USB3.0 Common choke EMI-Protection

DW03Q0360402//DW03Q0360305//temp_T_D21683



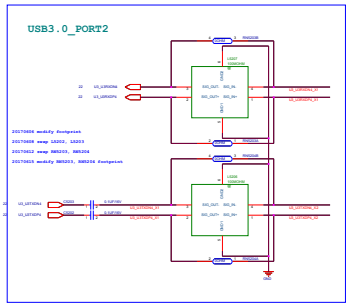
20170806 modify footprint
20170808 swap L8204, L8207
20170812 swap SW8203, SW8202
20170815 modify SW8201, SW8202 footprint



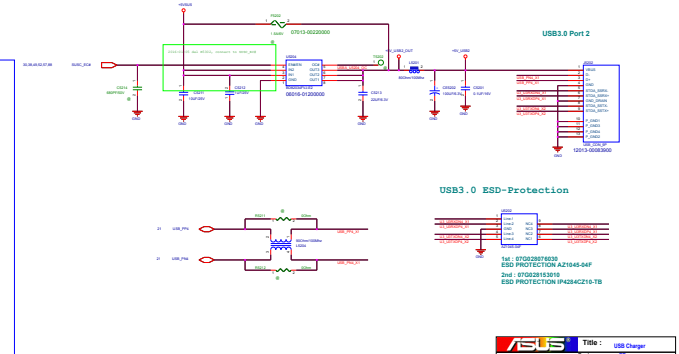
USB3.0_PORT2

USB3.0 Common choke EMI-Protection

DW03Q0360402//DW03Q0360305//temp_T_D21683



20170808 modify footprint
20170808 swap L8202, L8203
20170812 swap SW8203, SW8204
20170815 modify SW8203, SW8204 footprint

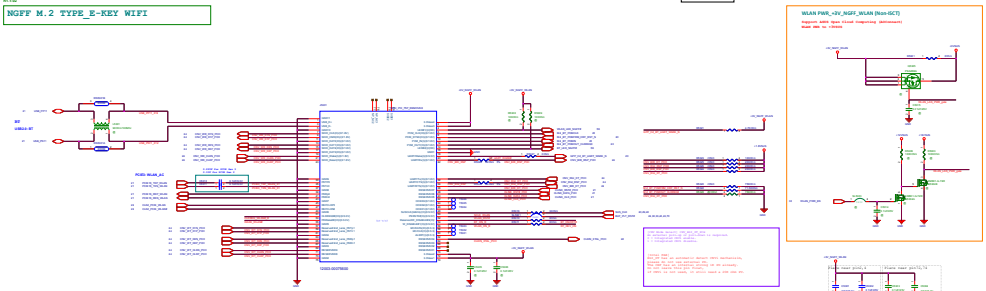


Title : USB Charger			
Engineer: EE			
Size	Project Name		Rev
C	GL703GS		V0.0
Date: Tuesday, January 30, 2018		Sheet 1 of 1	

Rev 1.02

NGFF M.2 TYPE_E-KEY WIFI

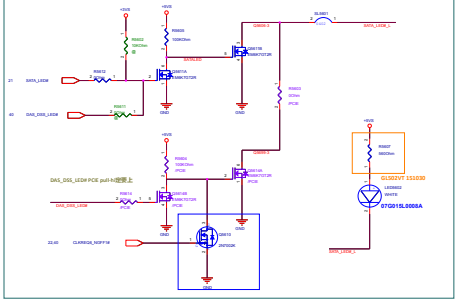
Main Board



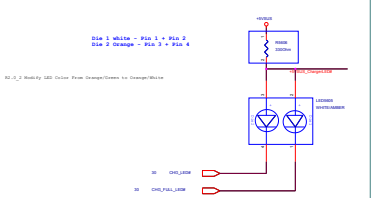
Title	NGFF Type WLAN&BT		
Engineer		Rev	
Size	03170B.00B		
Date	Monday, January 14, 2013	Sheet	1 of 1

Main Board

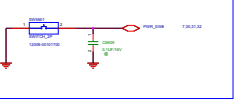
HDD LED & PCIE SSD LED



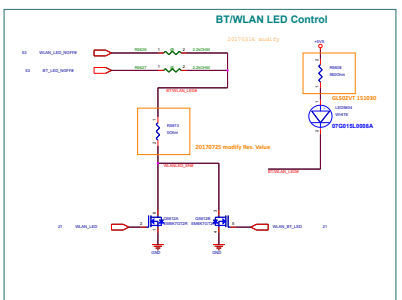
Charger LED



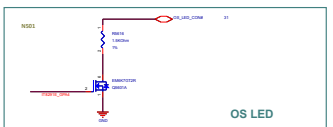
POWER button



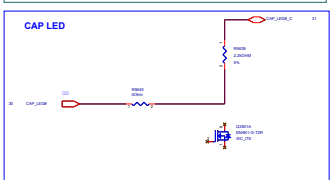
BT/WLAN LED Control



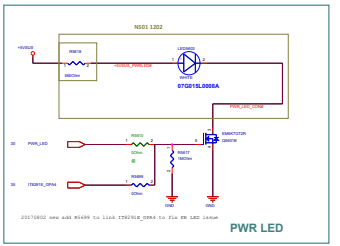
OS LED



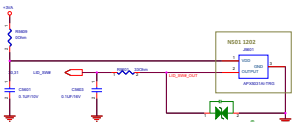
CAP LED



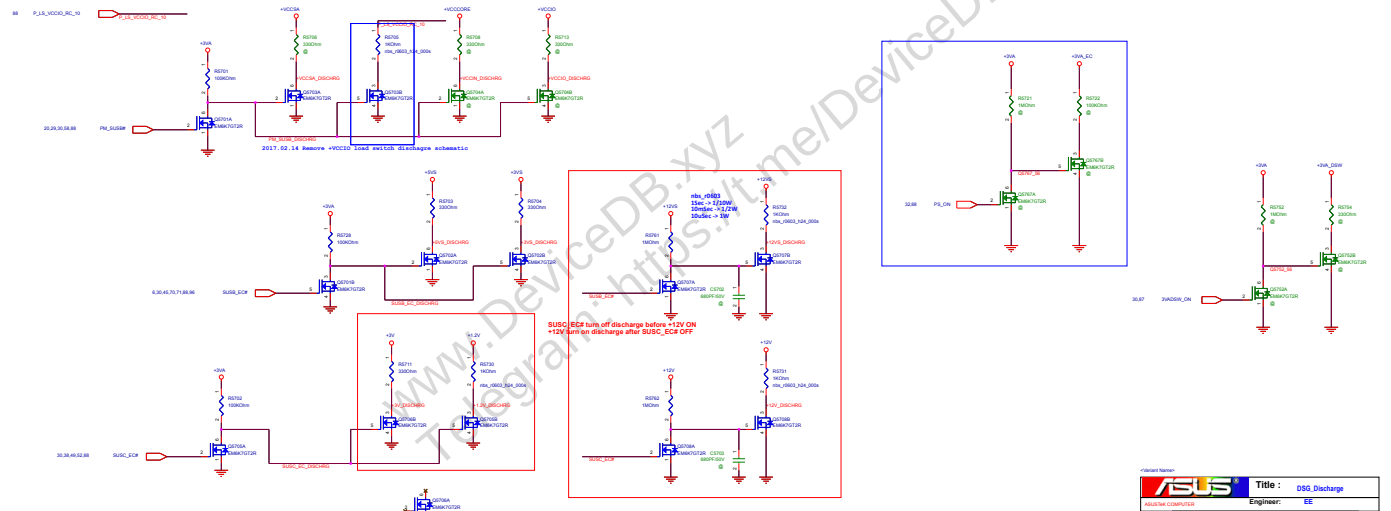
PWR LED



HALL SENSOR 06033-00140000

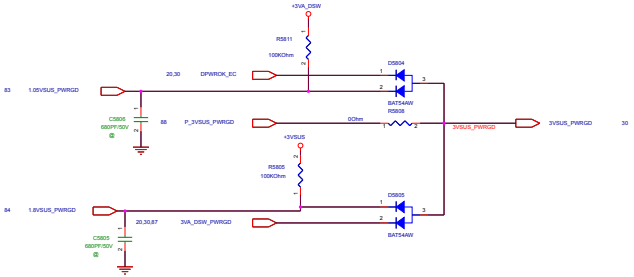


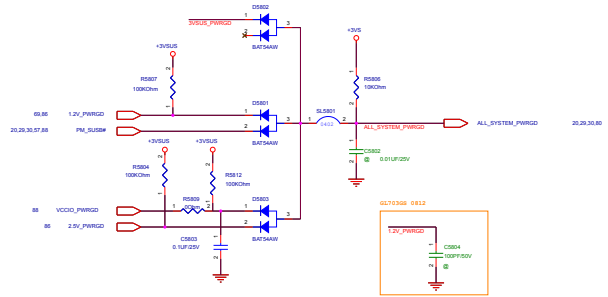
Project Name: GL703GS			Rev: RY-4
Title: LED Indicator			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Tuesday, January 09, 2018	Sheet: 56 of 101		

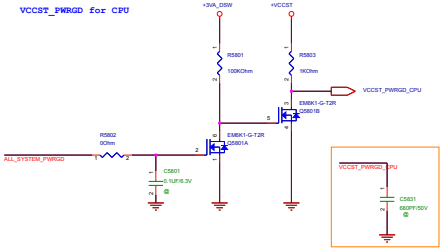


<Variant Name>

ASUSTeK COMPUTER	Title :	DSQ_Discharge
	Engineer:	EE
Size: Custom	Project Name: GL703GS	Rev: X1.x
Date: Tuesday, January 30, 2018	Sheet 37 of 53	

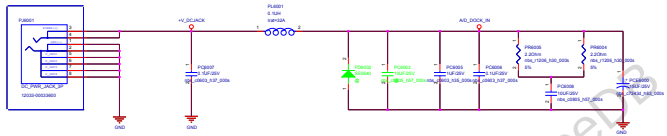






ASUS	Project Name: GL703GS		Rev: R1.4
Title : Power Protect			
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Tuesday, January 30, 2018		Sheet 56 of 101	

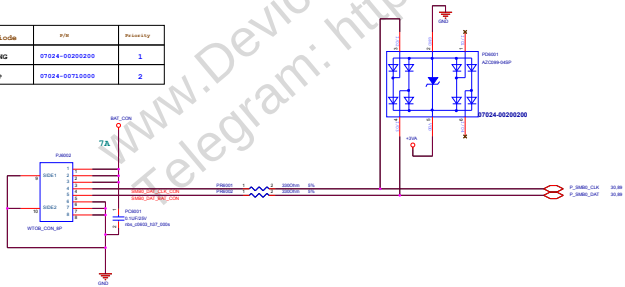
DC-IN Connector



瓦數	P/N (With Cable)	P/N (W/O Cable)	Read 數量
120W	14026-00040000	12033-00031000	5
180W	14026-00040000	12033-00031000	7
230W	TBD	12033-00030400	8
330W	TBD	12033-00050100	09G02X102300

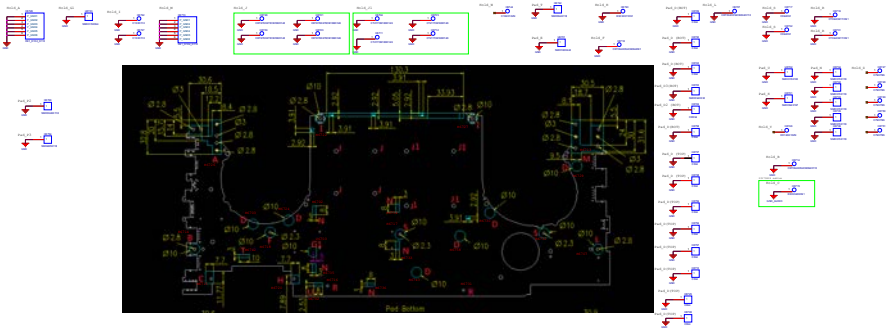
Battery Connector

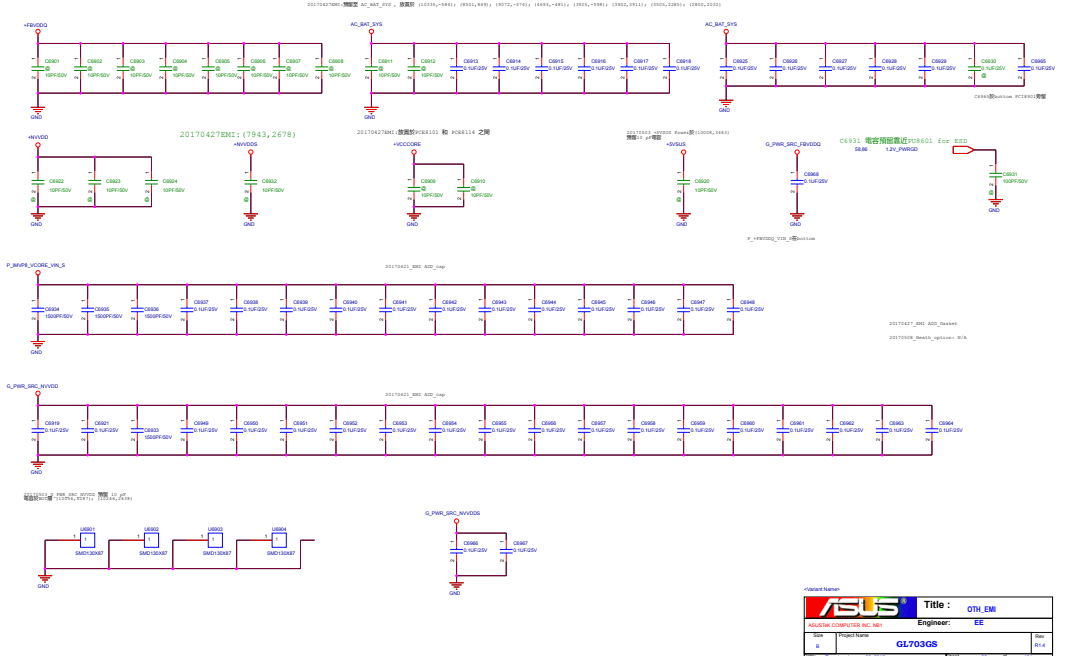
ESD Diode	P/N	Priority
AMAZING	07024-00200200	1
NXP	07024-00710000	2

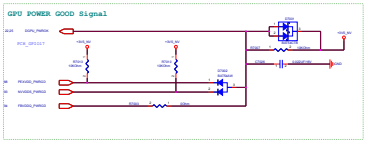


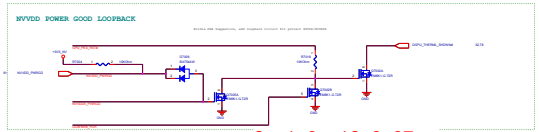
Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

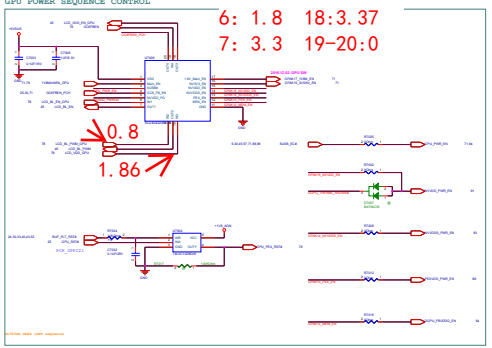
Project Name: GL703GS			Rev: XX.X
Title: DC & BAT IN			
Size: A3	Dept.: MB_Power team	Engineer: Joe	
Date: Thursday, June 15, 2017	Sheet 80 of 103		


Pad_Bottom
Pad_Top

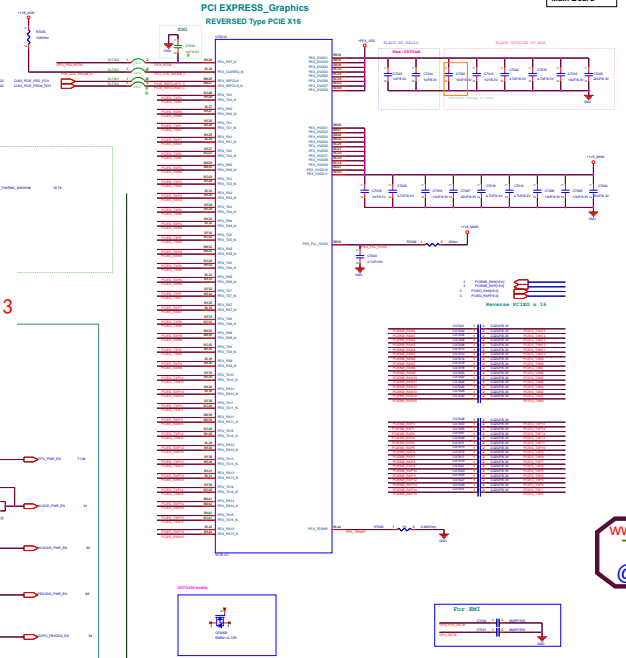

20170427EMI:預留至 AC_BAT_SYS , 放置於 (10335,-584); (8501,849); (9072,-574); (4693,-481); (3925,-598); (3902,3911); (3505,2285); (2800,2032)
+FBVDDQ
C6901 10PF/50V
C6902 10PF/50V
C6903 10PF/50V
C6904 10PF/50V
C6905 10PF/50V
C6906 10PF/50V
C6907 10PF/50V
C6908 10PF/50V
GND
AC_BAT_SYS
C6911 10PF/50V
C6912 10PF/50V
C6913 0.1UF/25V
C6914 0.1UF/25V
C6915 0.1UF/25V
C6916 0.1UF/25V
C6917 0.1UF/25V
C6918 0.1UF/25V
GND
AC_BAT_SYS
C6925 0.1UF/25V
C6926 0.1UF/25V
C6927 0.1UF/25V
C6928 0.1UF/25V
C6929 0.1UF/25V
C6930 0.1UF/25V
C6965 0.1UF/25V
GND
C6965放Position RC1845附近
+NVVDD
C6922 10PF/50V
C6923 10PF/50V
C6924 10PF/50V
GND
20170427EMI:(7943,2678)
+NVVDDS
C6932 10PF/50V
GND
20170427EMI:放置於PCB8101 和 PCB8114 之间
+VCCCORE
C6909 10PF/50V
C6910 10PF/50V
GND
20170503 +5VDDE Power至(13008,5663)
+5VSUS
C6920 10PF/50V
GND
G_PWR_SRC_FBVDDQ
C6968 0.1UF/25V
GND
C6931 100PF/50V
GND
P_+FBVDDQ_VIN_RC
C6931 預留預留靠近PCB601 for ESD
56.86
12V_PWRGD
P_+NVVDDQ_VIN_S
20170421_EMI ADD_cap
C6934 1500PF/50V
C6935 1500PF/50V
C6936 1500PF/50V
C6937 0.1UF/25V
C6938 0.1UF/25V
C6939 0.1UF/25V
C6940 0.1UF/25V
C6941 0.1UF/25V
C6942 0.1UF/25V
C6943 0.1UF/25V
C6944 0.1UF/25V
C6945 0.1UF/25V
C6946 0.1UF/25V
C6947 0.1UF/25V
C6948 0.1UF/25V
GND
20170427_EMI ADD_Gasket
20170508_Reason_options: N/A
G_PWR_SRC_NVVDDS
20170421_EMI ADD_cap
C6919 0.1UF/25V
C6921 0.1UF/25V
C6933 1500PF/50V
C6949 0.1UF/25V
C6950 0.1UF/25V
C6951 0.1UF/25V
C6952 0.1UF/25V
C6953 0.1UF/25V
C6954 0.1UF/25V
C6955 0.1UF/25V
C6956 0.1UF/25V
C6957 0.1UF/25V
C6958 0.1UF/25V
C6959 0.1UF/25V
C6960 0.1UF/25V
C6961 0.1UF/25V
C6962 0.1UF/25V
C6963 0.1UF/25V
C6964 0.1UF/25V
20170512 G_PWR_SRC_NVVDDS 預留 1C pF
U6901 SMD130X87
U6902 SMD130X87
U6903 SMD130X87
U6904 SMD130X87
GND
G_PWR_SRC_NVVDDS
C6966 0.1UF/25V
C6967 0.1UF/25V
GND
<Variant Name>
Title : OTH_EMI
ASUSTeK COMPUTER INC. NB1
Engineer: EE
Size: B
Project Name: GL703GS
Rev: XX.x
Date: Tuesday, January 30, 2018
Sheet 69 of 101

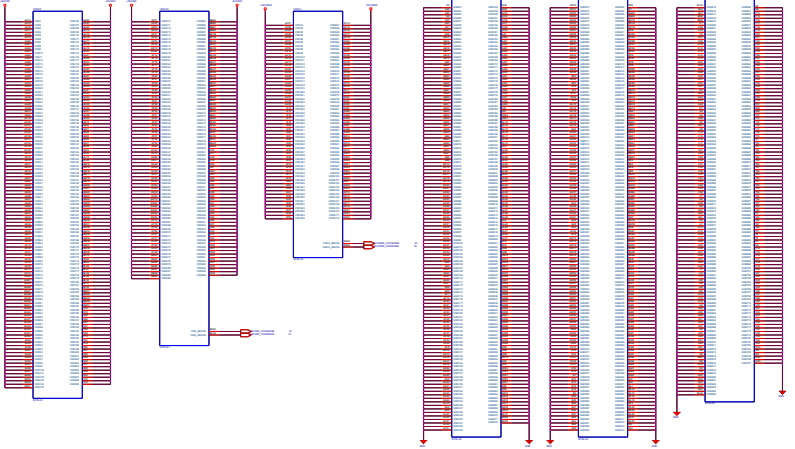


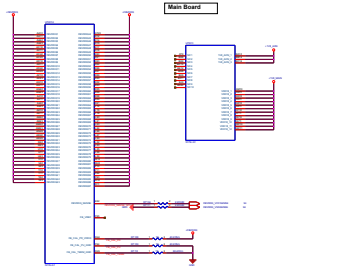


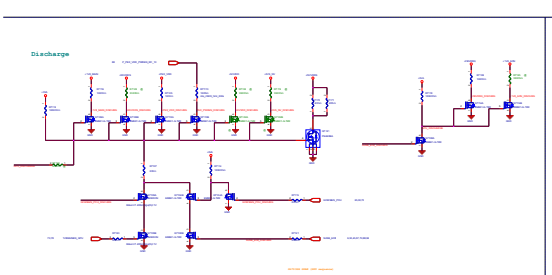


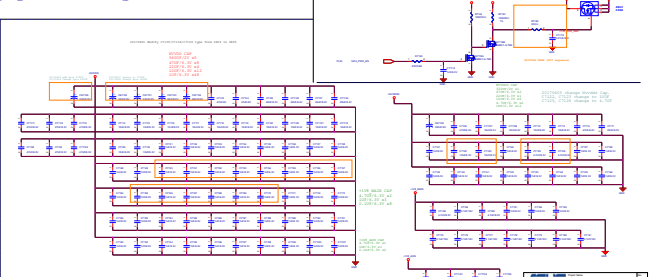
2: 1.8 12:3.37
4: 0 13~17:3.3
6: 1.8 18:3.37
7: 3.3 19~20:0



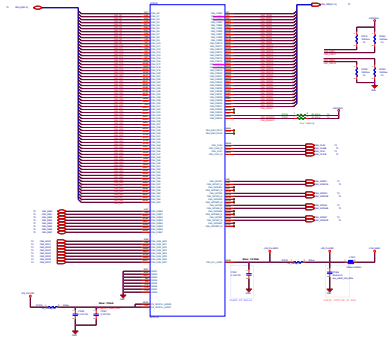



Main Board
1V8 & 3V3 Power Control

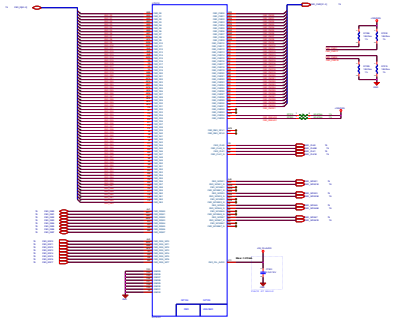

Discharge



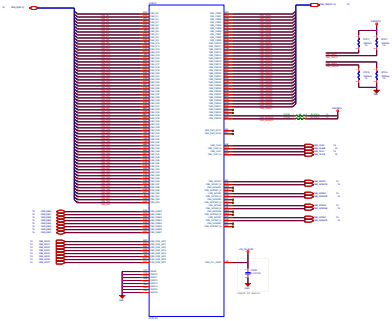
MEMORY: GPU FB Partition A



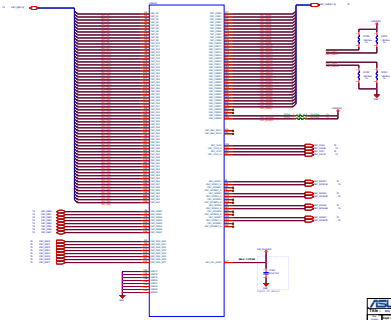
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B

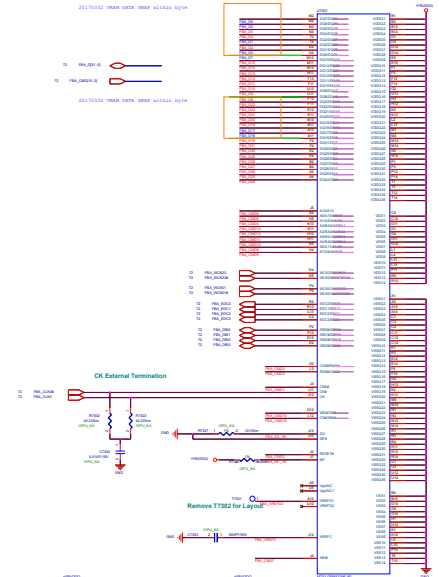


MEMORY: GPU FB Partition C



FBA Partition Memory (1 of 2)

MF=1 Mirror

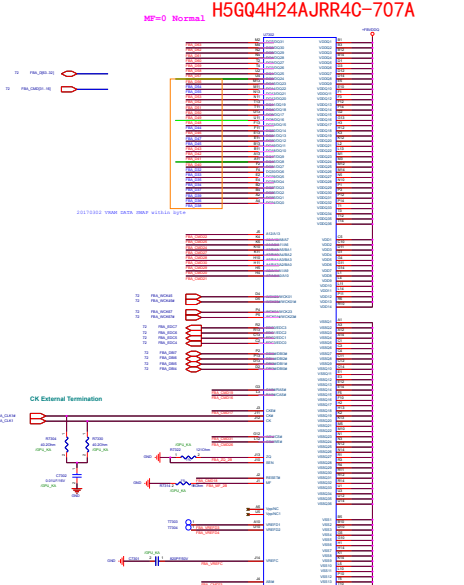


FBA Partition Memory (2 of 2)

Main Board

H5GQ4H24AJRR4C-707A

MF=0 Normal



R1.3-02 R1.2-05

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00020100 HYNIX/H5GC4H24MFR-T2C (M-die) ;Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ;Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW8032A8BG-66-F (B-die) ;Strap: 0x4

GDD5 MODE SELECTION

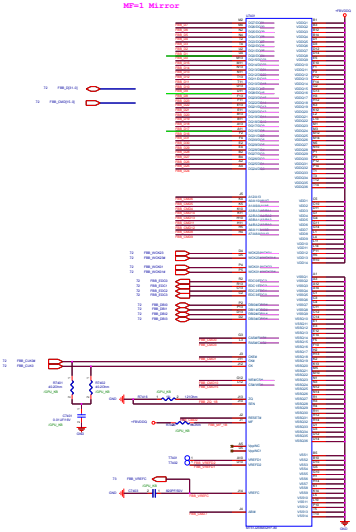
MODE	MF	EDC1	EDC0
x16	0	VDD	VDD
x32	0	VDD	VDD
x16 mirrored	VDD	VDD	0
x32 mirrored	VDD	VDD	VDD

Title :	VRAM-CHANNEL A		
Engineer:	EE		
Size: C	Document Number: GL703GS		Rev: 1.0
Date: Tuesday, January 24, 2017	Sheet: 13	of: 57	

Main Board

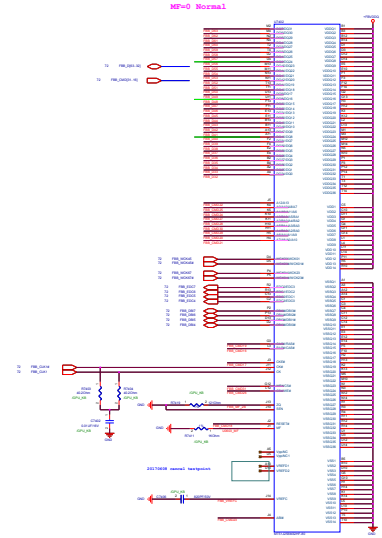
FBB Partition Memory (1 of 2)

MF=1 Mirror



FBB Partition Memory (2 of 2)

MF=0 Normal



RX-342 R1.2-20

USE GDDR3 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00020100 HYNIX(H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG(K4G41325FC-HC03 ,Strap: 0x3

3rd: P/N:03008-00030400 Micron(EDFA8192BABG-60-F (B-die) ,Strap: 0x4

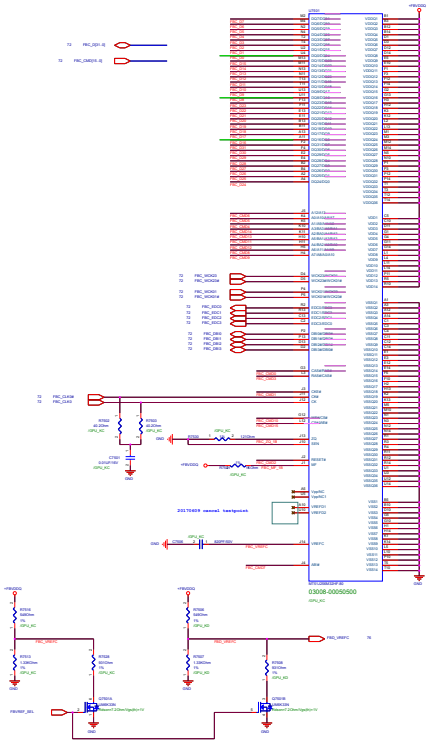
GDD5 MODE SELECTION

MODE	MF	EMC1	EMC2
x32	0	0	VDDQ
x32	0	VDDQ	VDDQ
x32 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

Title :	VRAM-CHANNEL B		
Engineer:	ES		
Size:	Document Number:		Rev:
C	GL703GS		R1.2
Date:	Sheet of		

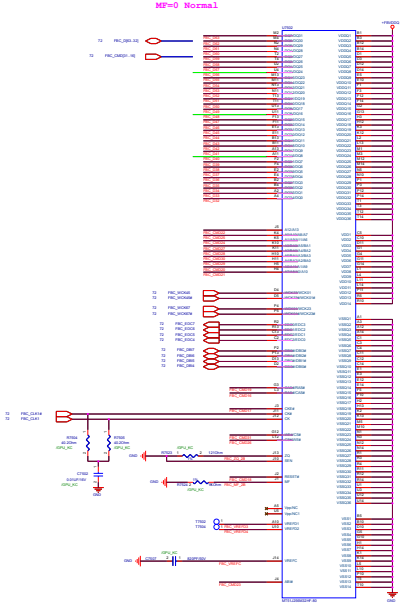
FBC Partition Memory (1 of 2)

MF=1 Mirror



FBC Partition Memory (2 of 2)

MF=0 Normal



R1-3-62 R1-2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00020100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3rd: P/N:03008-00031400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

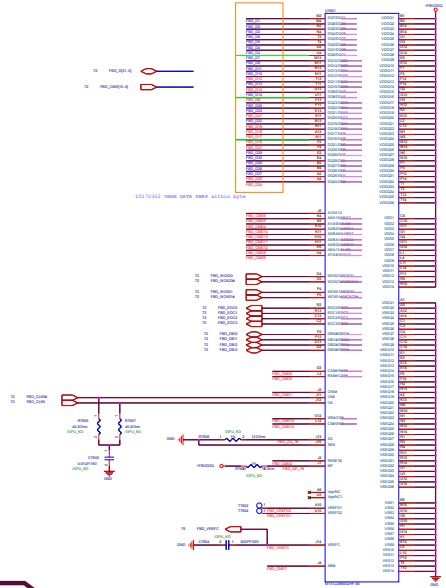
MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

Project Name: GL703GS			Rev: R1.0
Title : VRAM-CHANNEL C			
Size:	Document Number:	Engineer: EE	
Date: Tuesday, January 09, 2018		Sheet 15 of 101	

Main Board

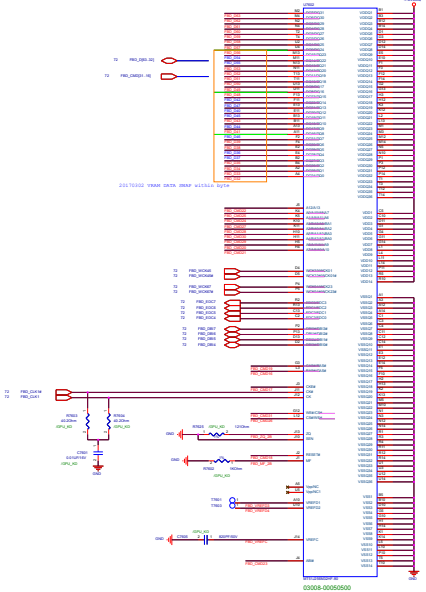
FBD Partition Memory (1 of 2)

MF=1 Mirror



FBD Partition Memory (2 of 2)

MF=0 Normal



R1-3-62 R1-2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G4132BFC-HC03 ,Strap: 0x3

3rd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDC
x32	0	VDDC	VDDC
x16 mirrored	VDDC	VDDC	0
x32 mirrored	VDDC	VDDC	VDDC

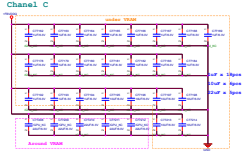
Title :	VRAM-CHANNEL D		
Size:	Document Number:	Rev:	
Date:	Tuesday, January 05, 2010	Sheet:	of

Main Board

Chanel A

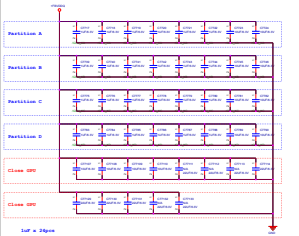
Chanel B

Chanel C

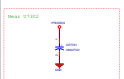


Chanel D

VRAM PWR_FBVDDQ

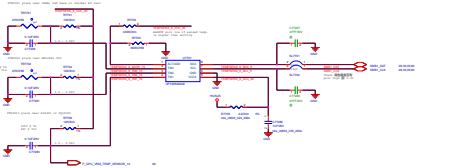


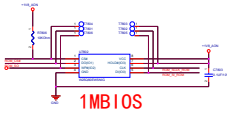
Near ST322

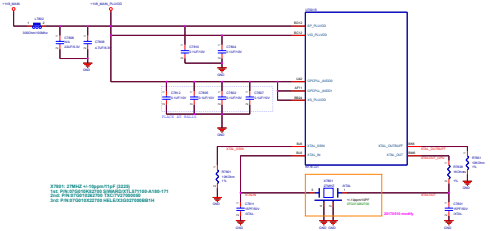


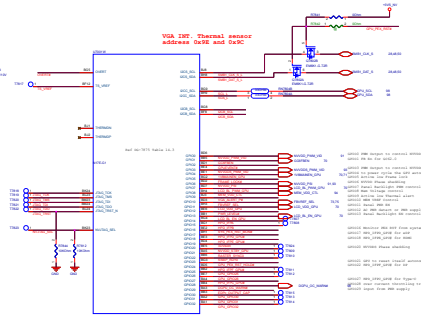
Address Selection Table

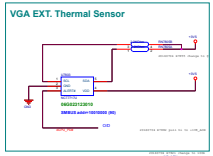
GL703GS UP1905

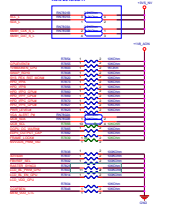


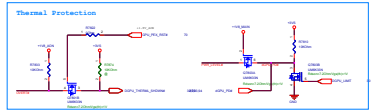


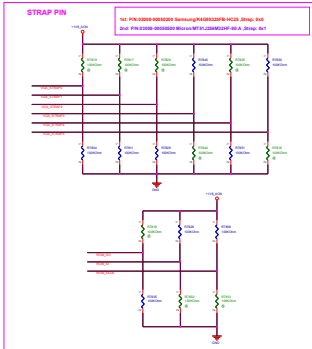


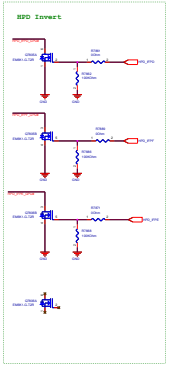




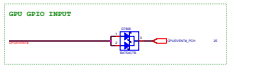






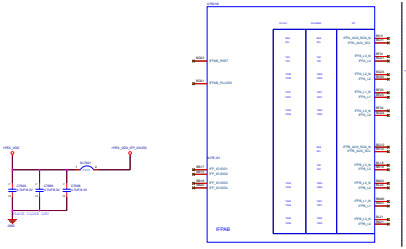


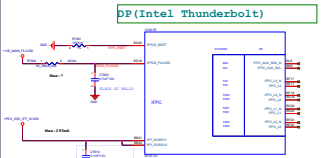
Level shift

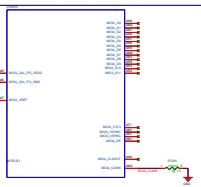


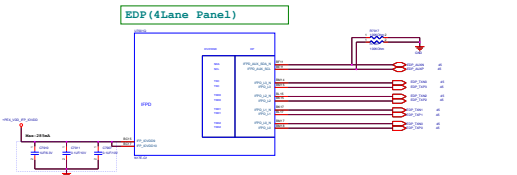
ASUS	Project Name: GL753GS		Rev:
Title:	GPU_GL553GS/GP62G		
Size:	Doc#: ASUSNB_1234-YYY-XX	Engineer: EE	
Date:	Sheet 1 of 1		

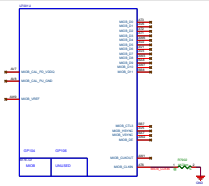
Main Board

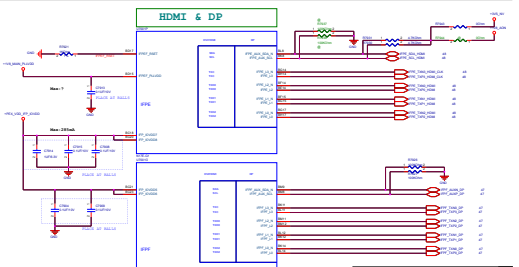






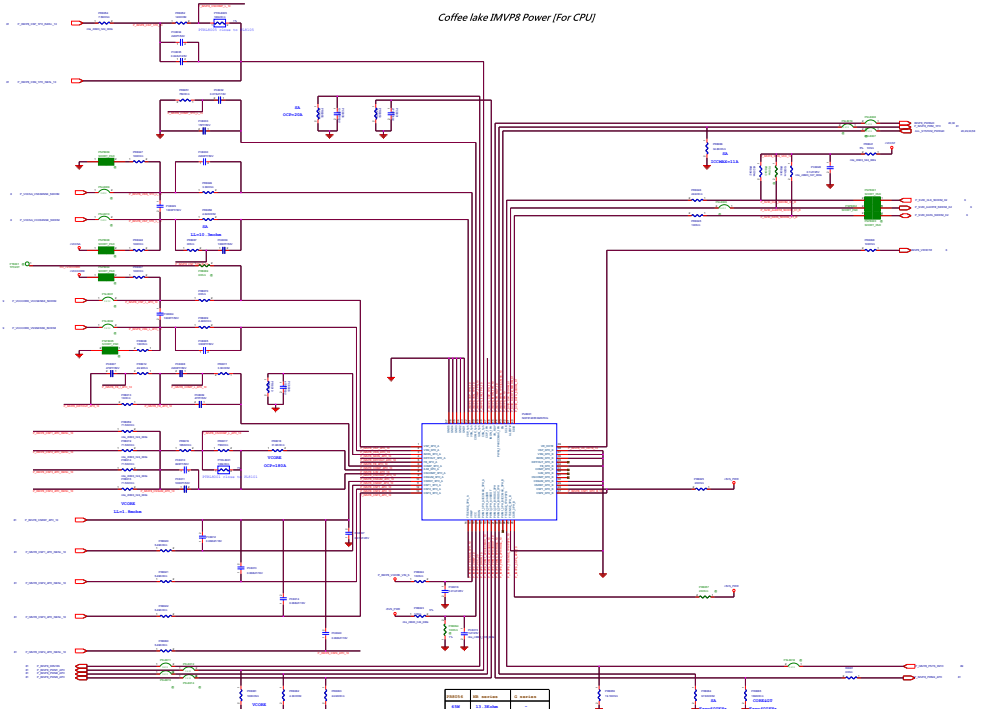






ASUS	Project Name: GL703GS		Rev: 0.1
Title : SYS_DIAGRAM			
Size: Custom	Dwg#:	Engineer:	
Date: Tuesday, January 02, 2018		Sheet 19 of 101	

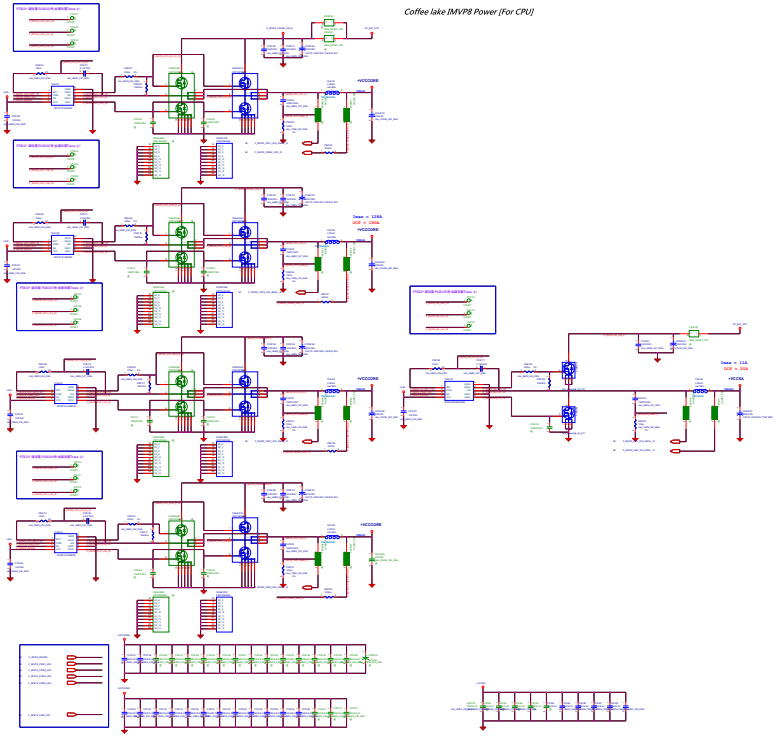
Coffee lake IMVP8 Power [For CPU]



2022/12	EE version	C version
0306	17 - 35ohm	-
0312	1.05ohm	-
1106	1.05ohm	22 - 35ohm
1206	-	28 - 35ohm
2106	-	24 - 35ohm
2306	-	18 - 35ohm

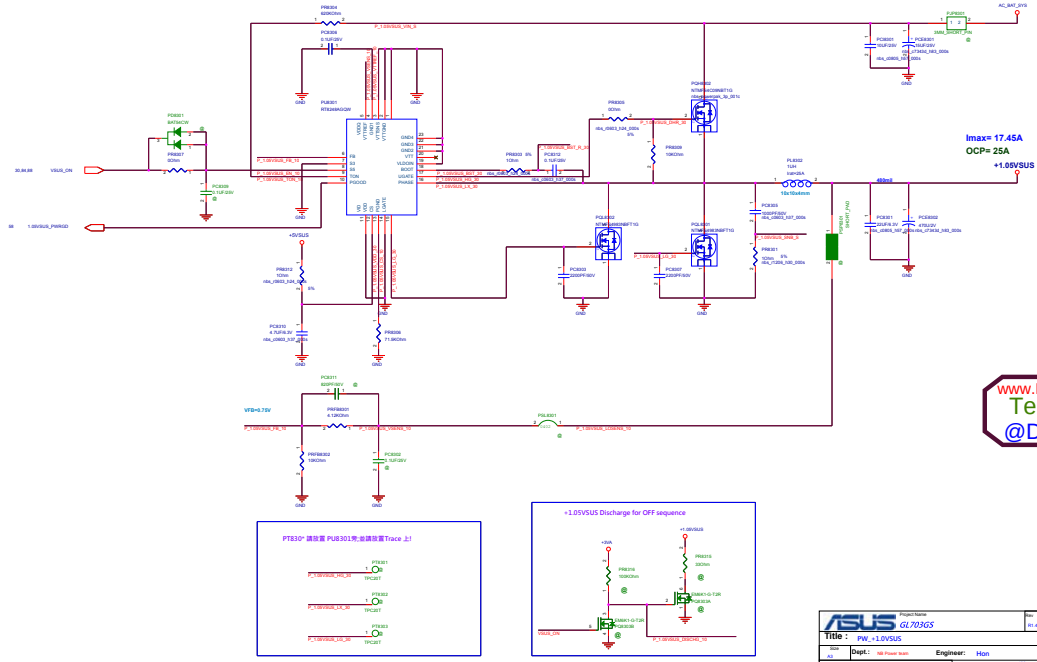
ASUSTeK Computer Inc.
ASUS
Title : /X0 Coffeelake (1)
Size: C | Document Number: | Rev: 2.0
Date: Monday, December 05, 2022 | Sheet: 1 of 1
Engineer: Alan

Coffee lake IMVP8 Power [For CPU]



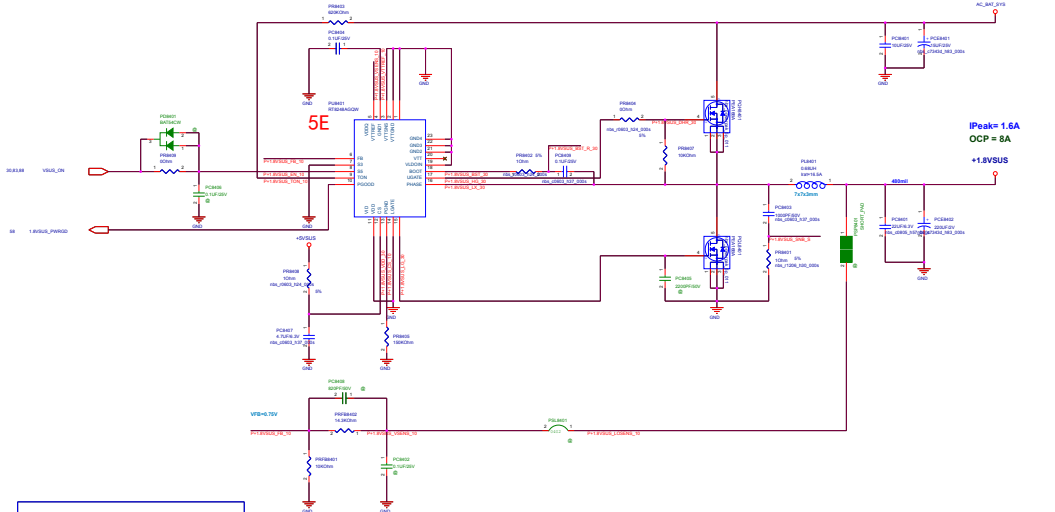
ASUS	Size:	Document Number:	Rev:
Title:			
Date:	Sheet	of	Engineer: Alex

+1.05VSUS [For PCH]



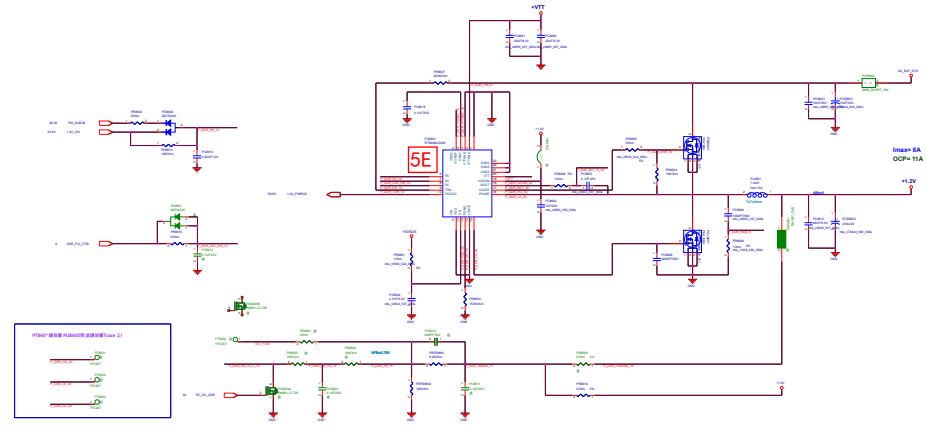
Title :	PW_+1.05VSUS		
Size: A3	Dept.:	MB Power Team	Engineer: Hon
Date: Tuesday, January 30, 2018	Sheet 83 of 103		

+1.8VSUS [For PCH]

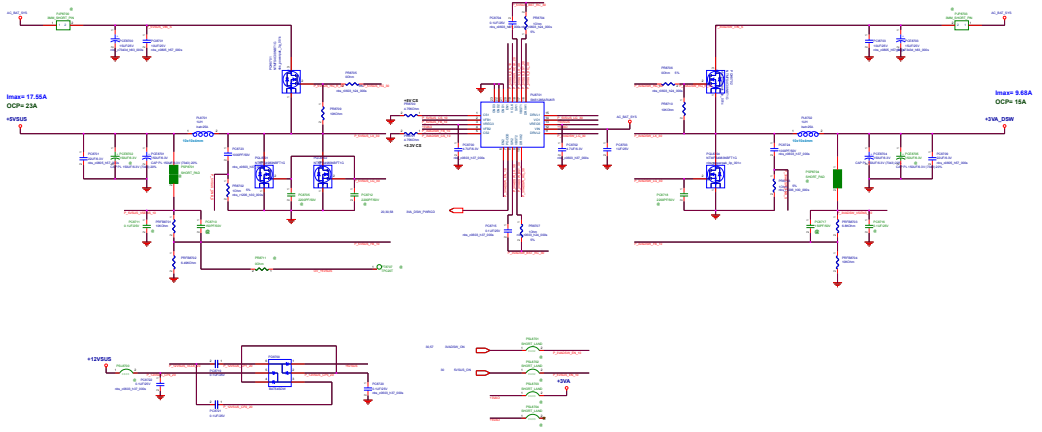


<Variant Name>			
ASUS	Project Name: GL703GS		Rev: XX.X
Title : PW_+1.8VSUS			
Size: A3	Dept.: NB Power Team	Engineer: Hon	
Date: Tuesday, January 30, 2018	Sheet: xx of: 103		

+1.2V / +VTT / +2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]



Adaptor Mode (MAYPA)							
	Vin	S5	S3	S0	Vin_S	BS	BS with USB Charger*
PG_DIN	H	H	H	H	H	H	H
ENABKBK_DIN	H	H	H	H	H	H	H
SYSON_DIN	H	H	H	H	H	H	H
RSMRST_DIN	H	H	H	H	H	H	H
PWRBTN_DIN	H	H	H	H	H	H	H
AUDIO_BIOS	H	H	H	H	H	H	H
BIOSB_BIOS	H	H	H	H	H	H	H

Battery Mode (MAYPA)							
	Vin	S5	S3	S0	Vin_S	BS	BS with USB Charger*
PG_DIN	H	H	H	H	L	H	L
ENABKBK_DIN	H	H	H	H	H	H	H
SYSON_DIN	H	H	H	H	H	H	H
RSMRST_DIN	H	H	H	H	L	H	L
PWRBTN_DIN	H	H	H	H	H	H	H
AUDIO_BIOS	H	H	H	H	H	H	H
BIOSB_BIOS	H	H	H	H	H	H	H

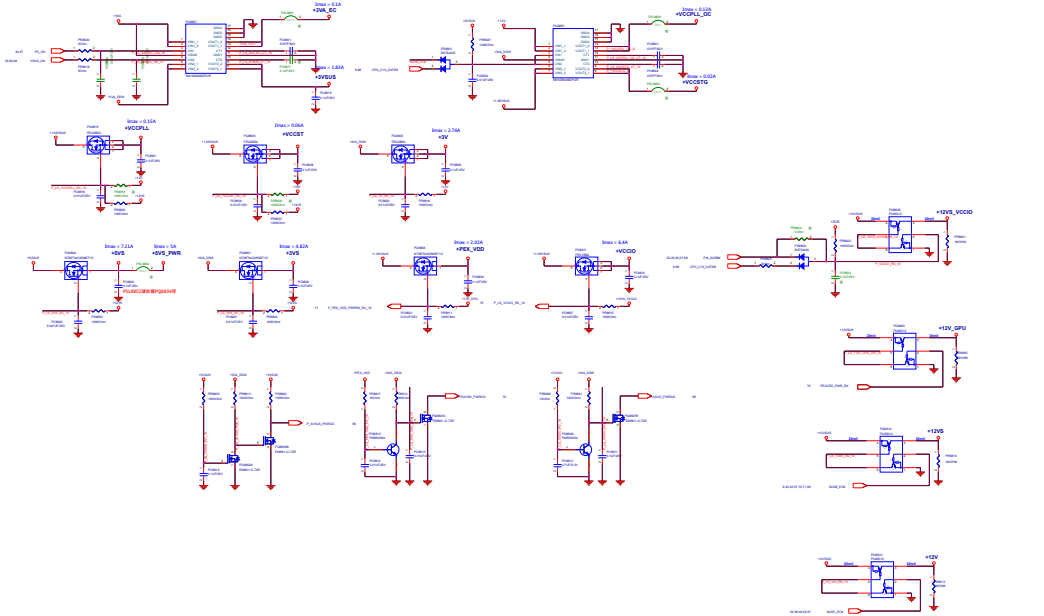
PTS70* 請裝置 PU87505電池請裝置Trace_27

P_PWRBTN_ON_1P	PTS701 PWRBTN	P_PWRBTN_ON_2P	PTS702 PWRBTN
P_PWRBTN_ON_1P	PTS703 PWRBTN	P_PWRBTN_ON_2P	PTS704 PWRBTN
P_PWRBTN_ON_1P	PTS705 PWRBTN	P_PWRBTN_ON_2P	PTS706 PWRBTN

ASUSTeK Computer Inc.				Rev
Title : AW_NHL2N(H)-3050S				
Size	Project	Date	Engineer: Hinn	
Custom	Tuesday, January 08, 2013		Sheet 21 of 50	

Load Switch

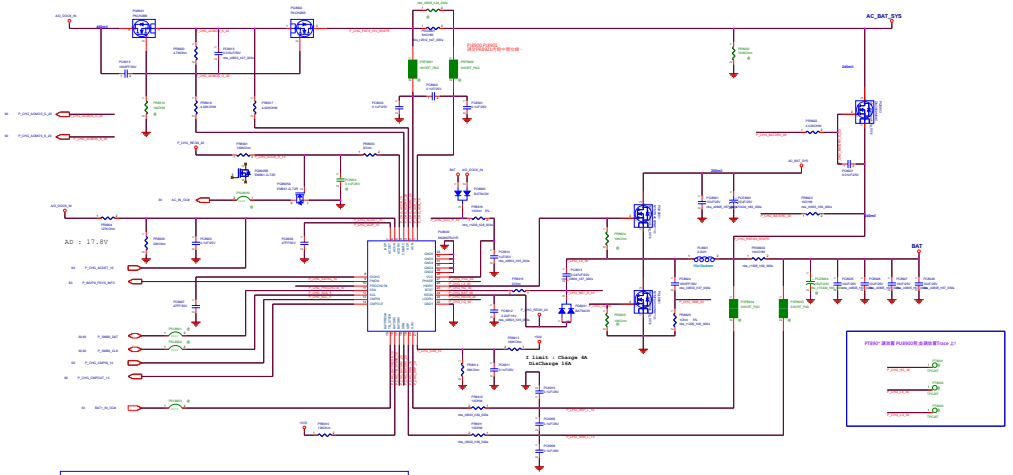
Main Board



ASUS	Project Name: GL703GS		Rev: 0.1
Title:	PA_LOAD SWITCH		
Size: C	Document Number:		
Date: Thursday, January 05, 2017	Sheet: 40 of 53	Engineer:	Hsun

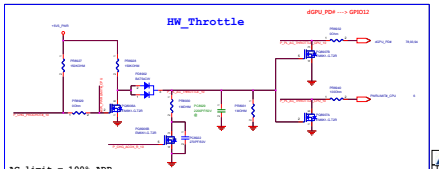
Main Board

PR8901	<=150W	<=230W	>230W	>330W
	10k	5k	2k	1k
	10kΩ±0.5%,3435	5.1kΩ±0.5%,3435	2.01kΩ ±0.5%,3435	1.01kΩ ±0.5%,3435



Adaptor select
total power = 90% ADP

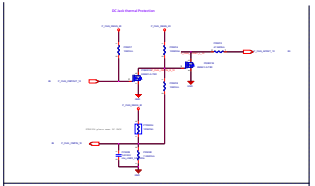
Adaptor select			
	M Series	Q Series	
PR8921	10k	5k	
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	460W

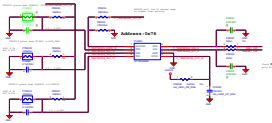


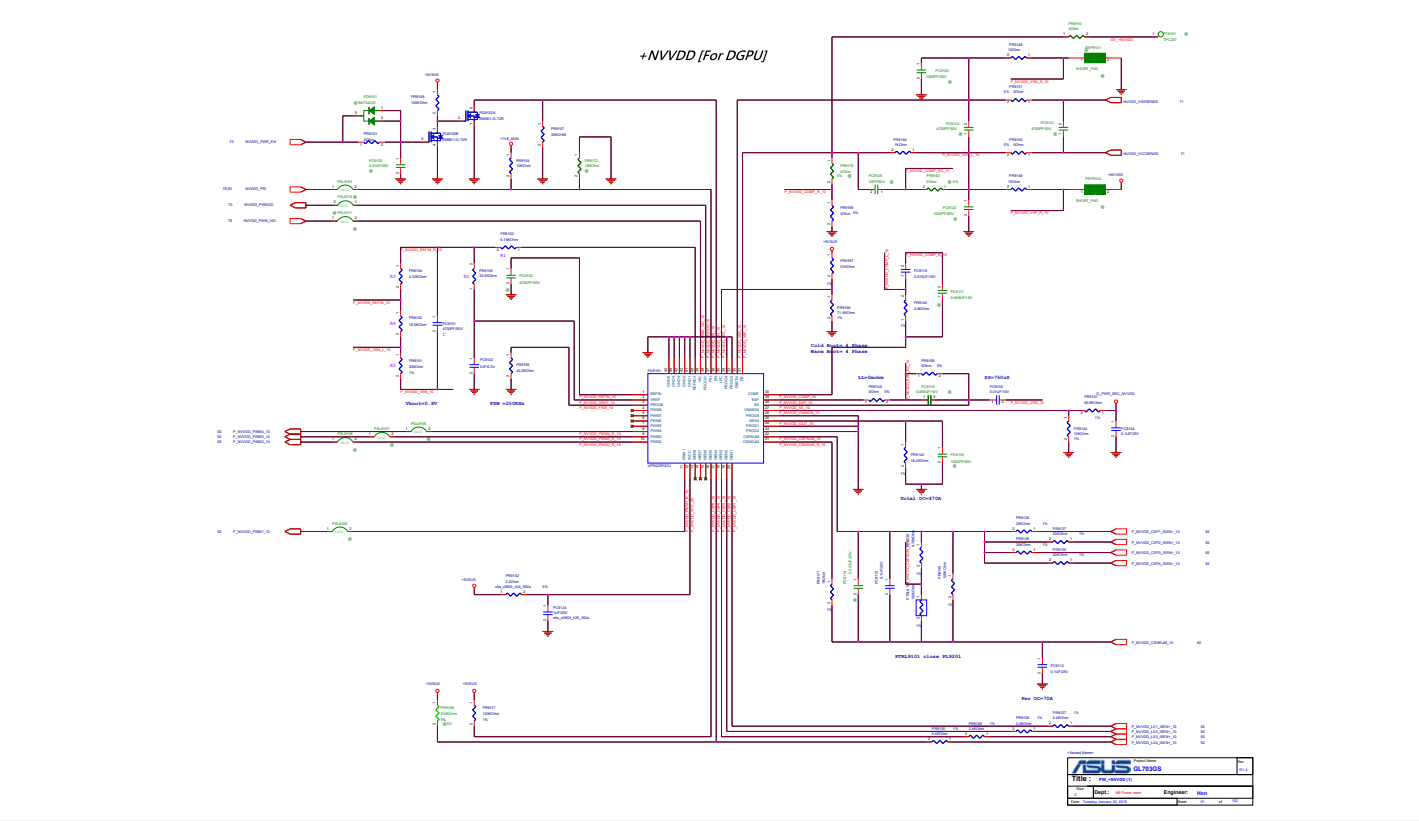
Title :	PW_CHARGER		
Size:	Document Number:		Rev:
A3	UX700GD		0.1
Date:	Sheet of	Engineer:	Hsin
Monday, January 09, 2017			

Address selection Table

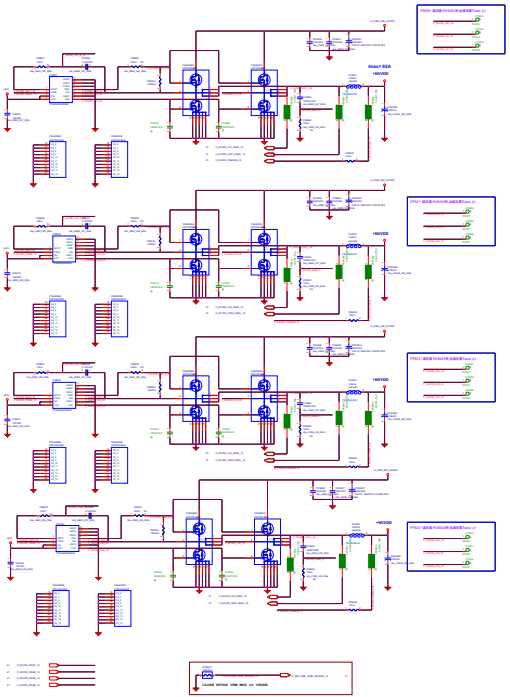
Register Address



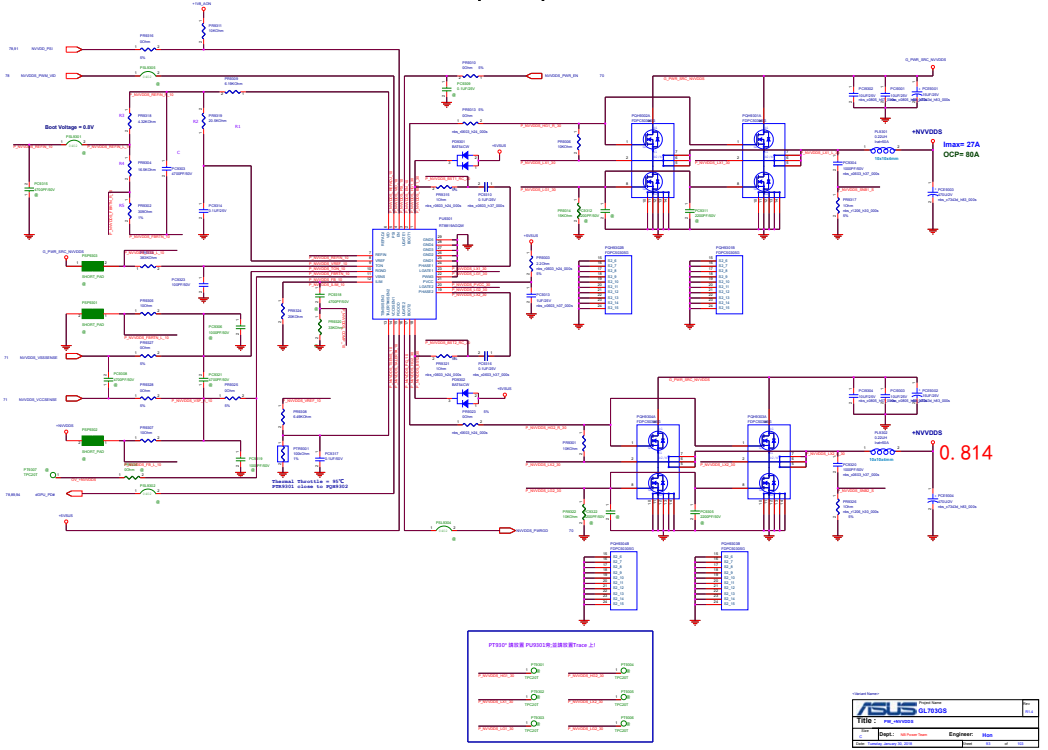



+NVVDD [For DGPU]
Cold Redrip 4 Phase
Warm Redrip 4 Phase
Ydroo1=0.8V
FSW =250KHz
Iin=75Out
Total OCP=470A
Per OCP=75A
PVR1.0/01 close PL0201
GL763GS
Title : PVL_NVVDD(1)
Engineer:
Hsin

+NVVDD [For DGPU]

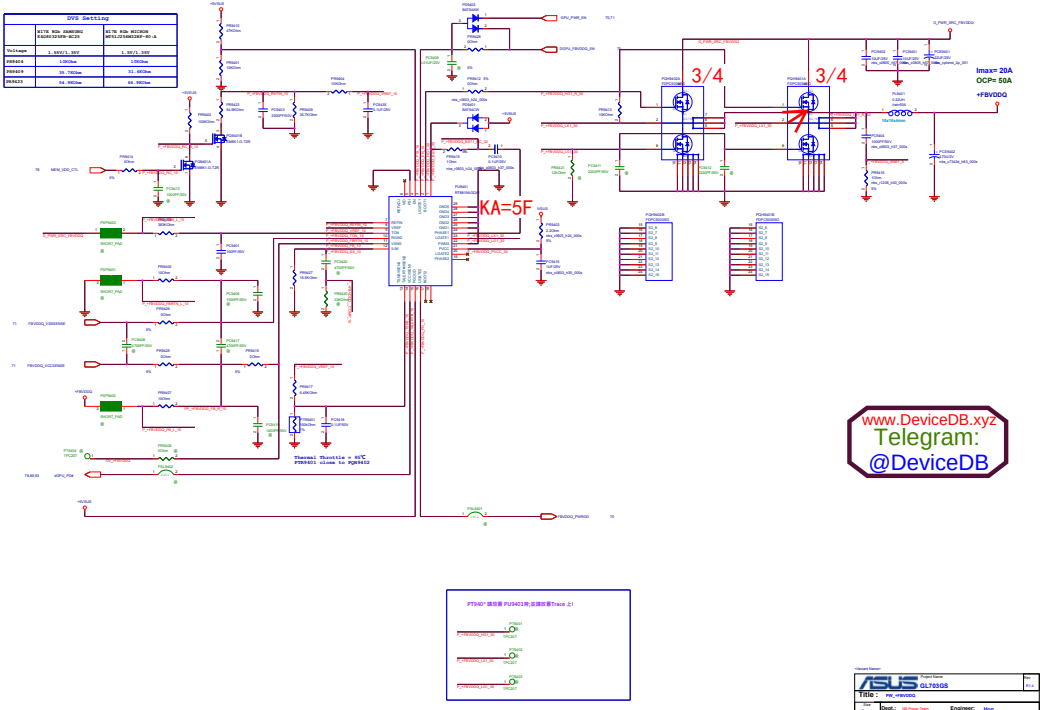


+NVVDDS [For DGPU]

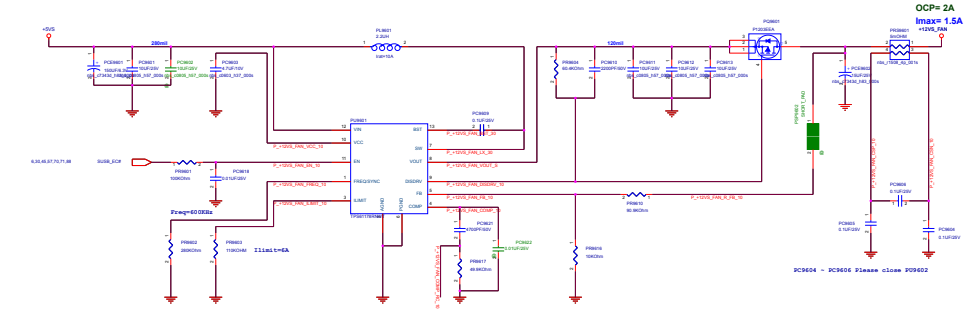


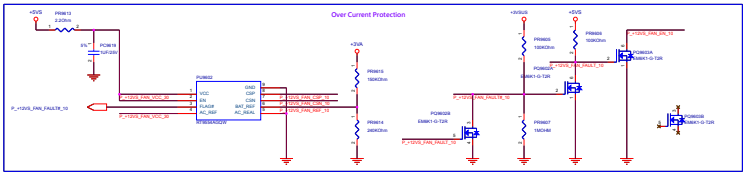
Title :	PM_NVVDDS		
Size	Project Name	GL703GS	Rev
	Dept.	MB Project Team	Engineer: Hsin
Date: Tuesday, January 29, 2019		Sheet 63 of 103	

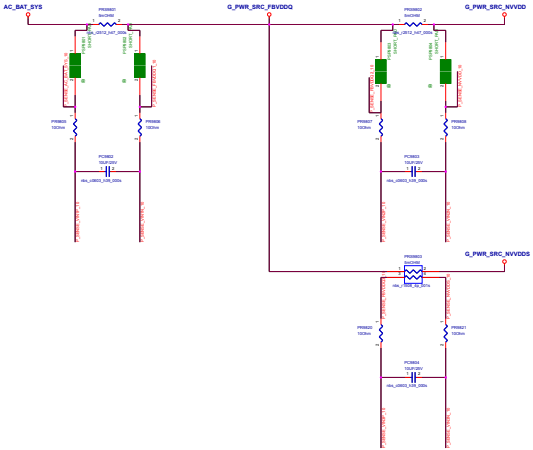
+FBVDDQ [For VRAM]

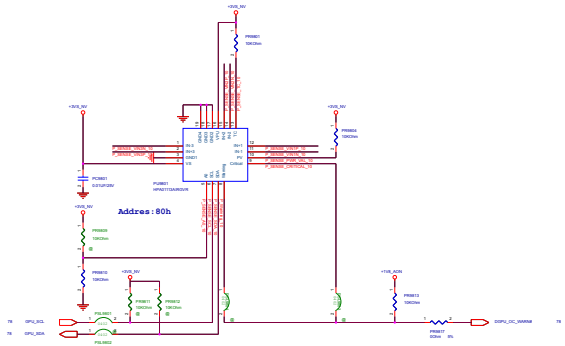


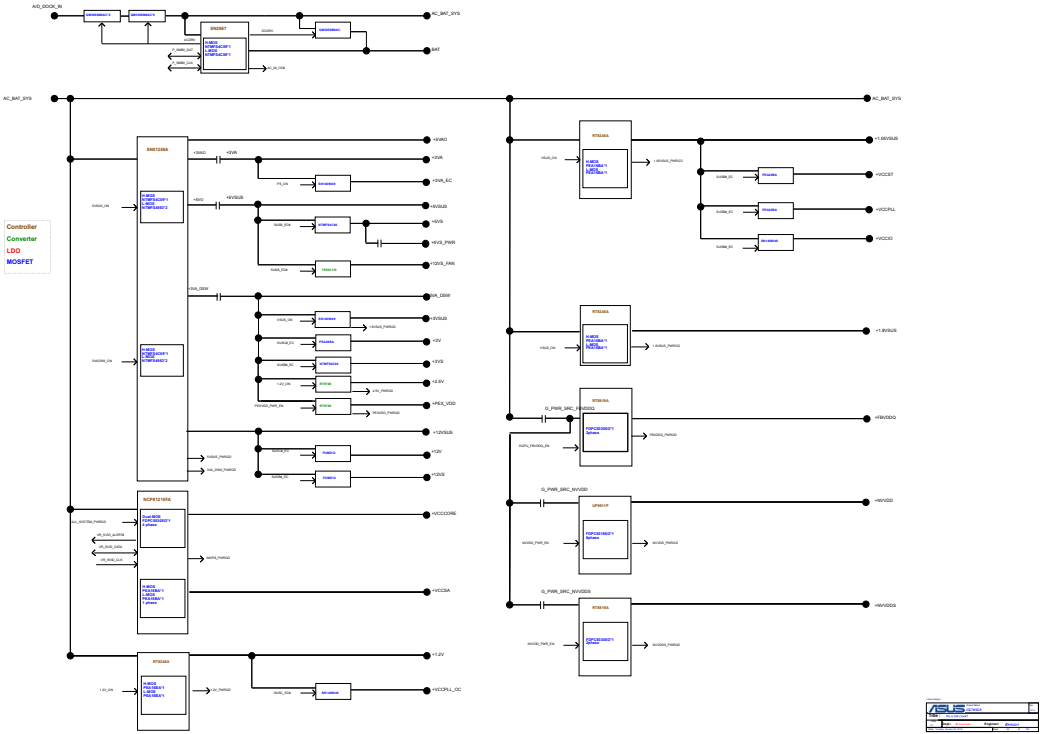
+12VS_FAN [For FAN]





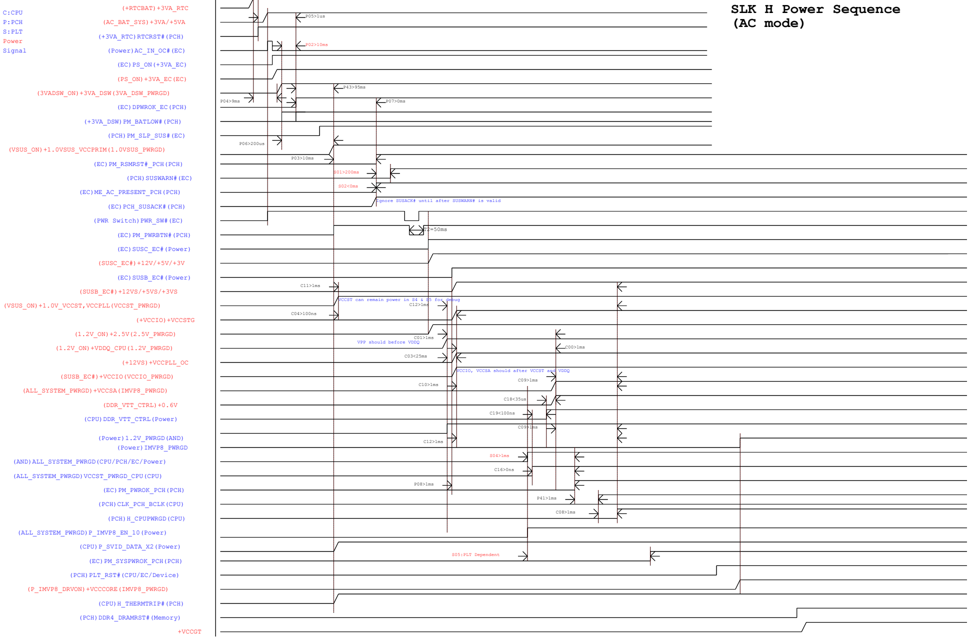





AC_BAT_SYS
AC_BAT_SYS
Controller
Converter
LDO
MOSFET
SN51208A
NCP81215RA
RT8240A
RT8240A
RT8240A
RT8819A
RT8819A
RT8240A
+5VALW
+3VALW
+1.8V_ILC
+3VSUS
+5VS
+5VS_PWR
+5VS_FAN
SW_DSW
+3VSUS
+5V
+3VS
+3.3V
+PEX_VDD
+12VSUS
+12V
+12VS
+VCCCORE
+VCCSA
+1.2V
+VCCPLL_OC
+1.8VSUS
+VCCST
+VCCPLL
+VCCIO
+1.8VSCS
+5VDUAL
+5V
+3.3V
+PEX_VDD
+12V
+12VS
+1.8VSDIO
+NVVDD
+NVVDDS

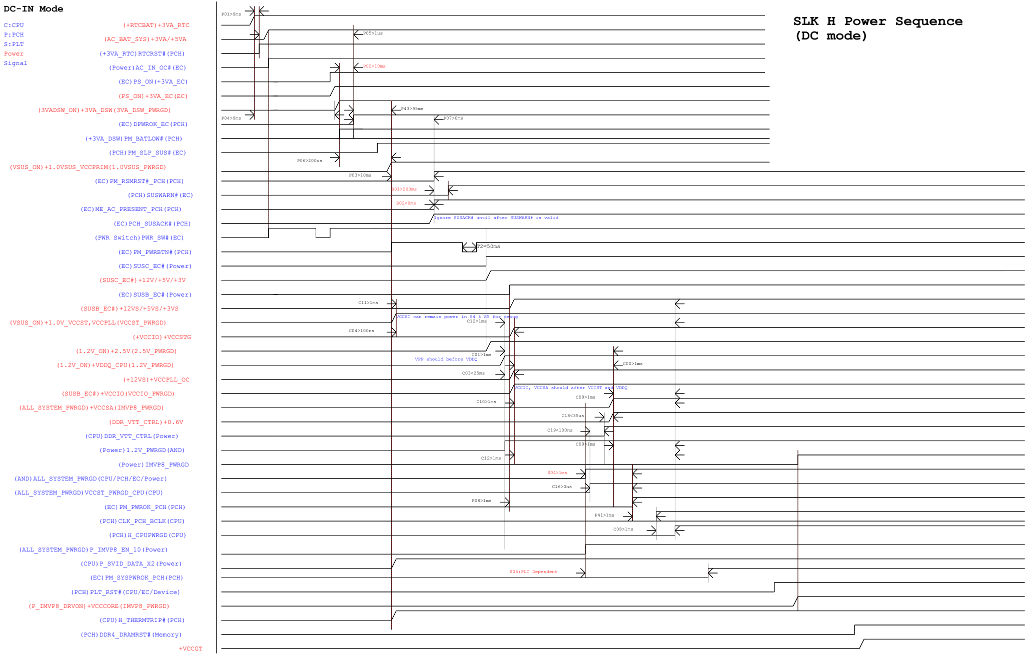
AC-IN Mode

SLK H Power Sequence (AC mode)



ASUS	Project Name: GL703GS	Rev: R1.4
Title : Power On Timing-AC mode		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Tuesday, January 30, 2018	Sheet 100 of 103	

SLK H Power Sequence (DC mode)



ASUS	Project Name GL703GS		Rev R1.4
Title : Power On Timing--DC mode			
Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, January 30, 2018		Sheet 101 of 103	

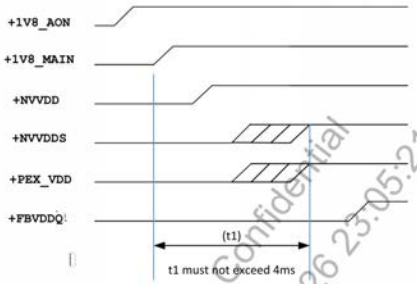


Figure 7.5 Example of Power-Up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- t1 (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_PGOOD) must NOT exceed 4ms.
- The ramp-up overshoot should not exceed the silicon reliability limit voltage.
- Power up NVVDD must be 90% before PEX_DVDD and NVVDDS can start ramp-up.
- Power up 1V8_AON must be 90% before 3V3 ramp up
- All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU CANNOT have any 3.3V leakage paths before 1V8_AON is present.
- No signal should be applied to the GPU before power rails are fully ramped.
- Refer to the JEDEC Memory Specification for memory-related power sequencing.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
- FBVDD/Q and 1V8_AON don't need power cycle for GC6 2.1

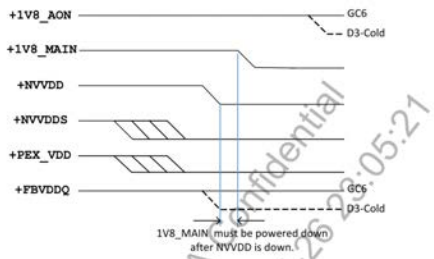
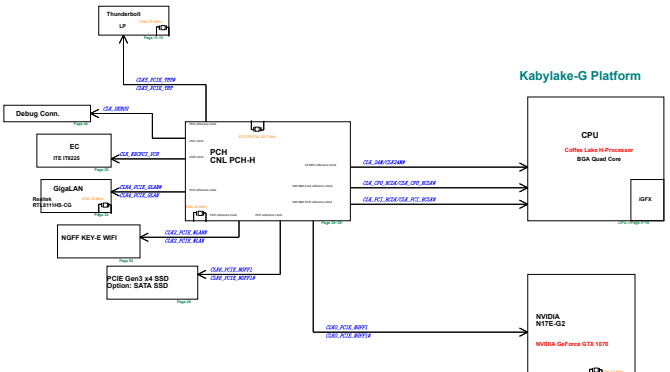


Figure 7.6 Example of Power-Down Sequencing Order

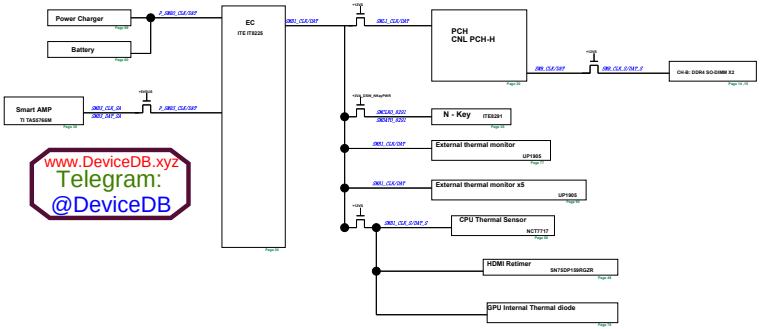
The following power-down sequence is required:

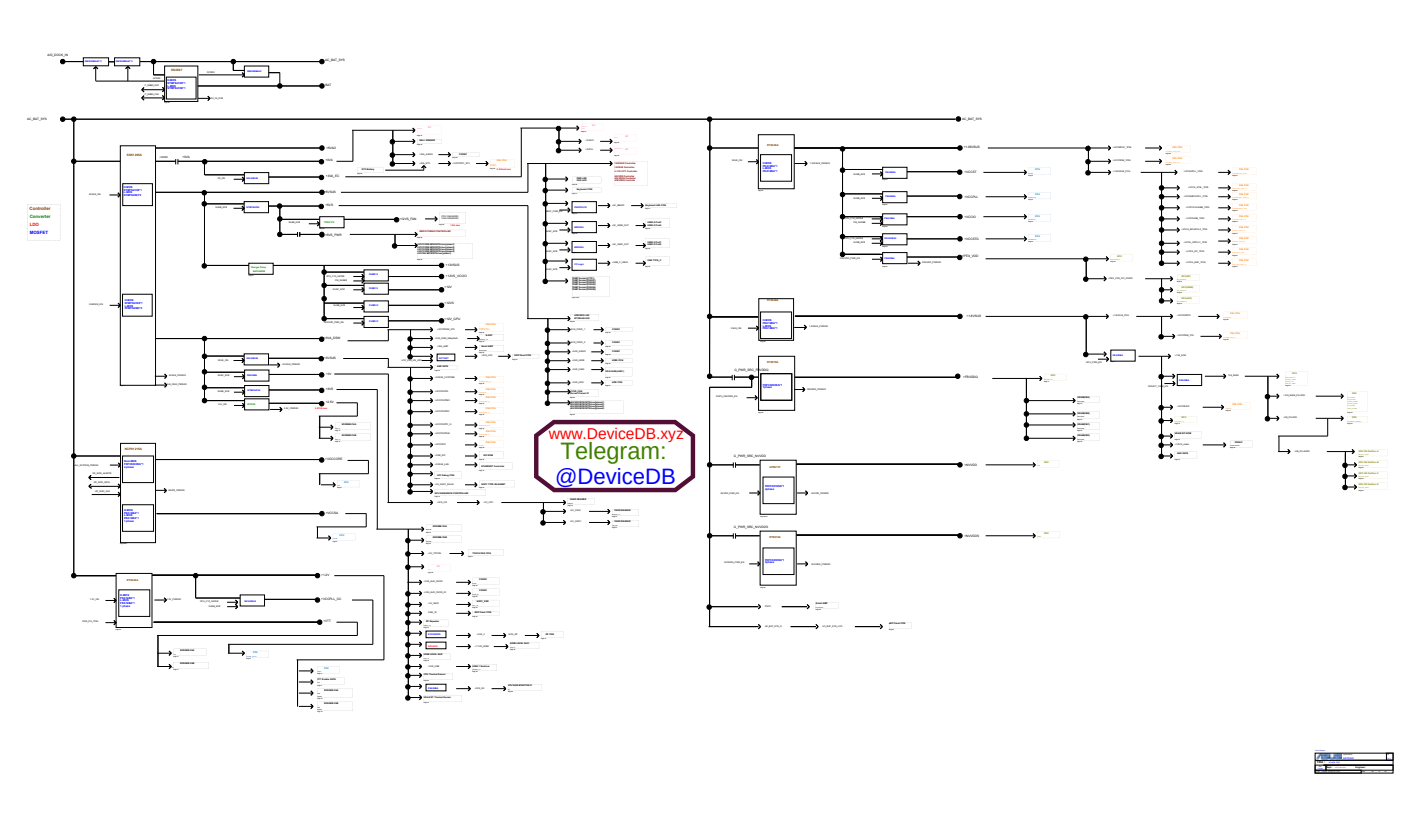
- NVVDDS/PEX_DVDD must power down before NVVDD; all other power rails can power down together with NVVDD.
- 1V8_MAIN must power down after NVVDD powers down.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power-up and power-down.
- For GDDR5X, VPP must be equal to or higher than FBVDD/Q at all times; use gate logic and discharge circuit as needed.
- All 3.3V devices that connect to the GPU must be ramped down before 1V8_AON; GPU CANNOT have any 3.3V leakage paths after 1.8V_AON and 1.8V_MAIN power-down.
- Power down of NVVDDS and PEX_DVDD must be less than 10% before NVVDD can start ramp-down.
- Power down of 3V3 must be less than 10% before 1V8_AON can start ramp-down.

CIcok Distribution



SMBUS Block Diagram




Controller
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MOSFET
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