Wistron-SKLU Schematics
Mihawk
REV : -2

DY : None Installed

Mihawk MB

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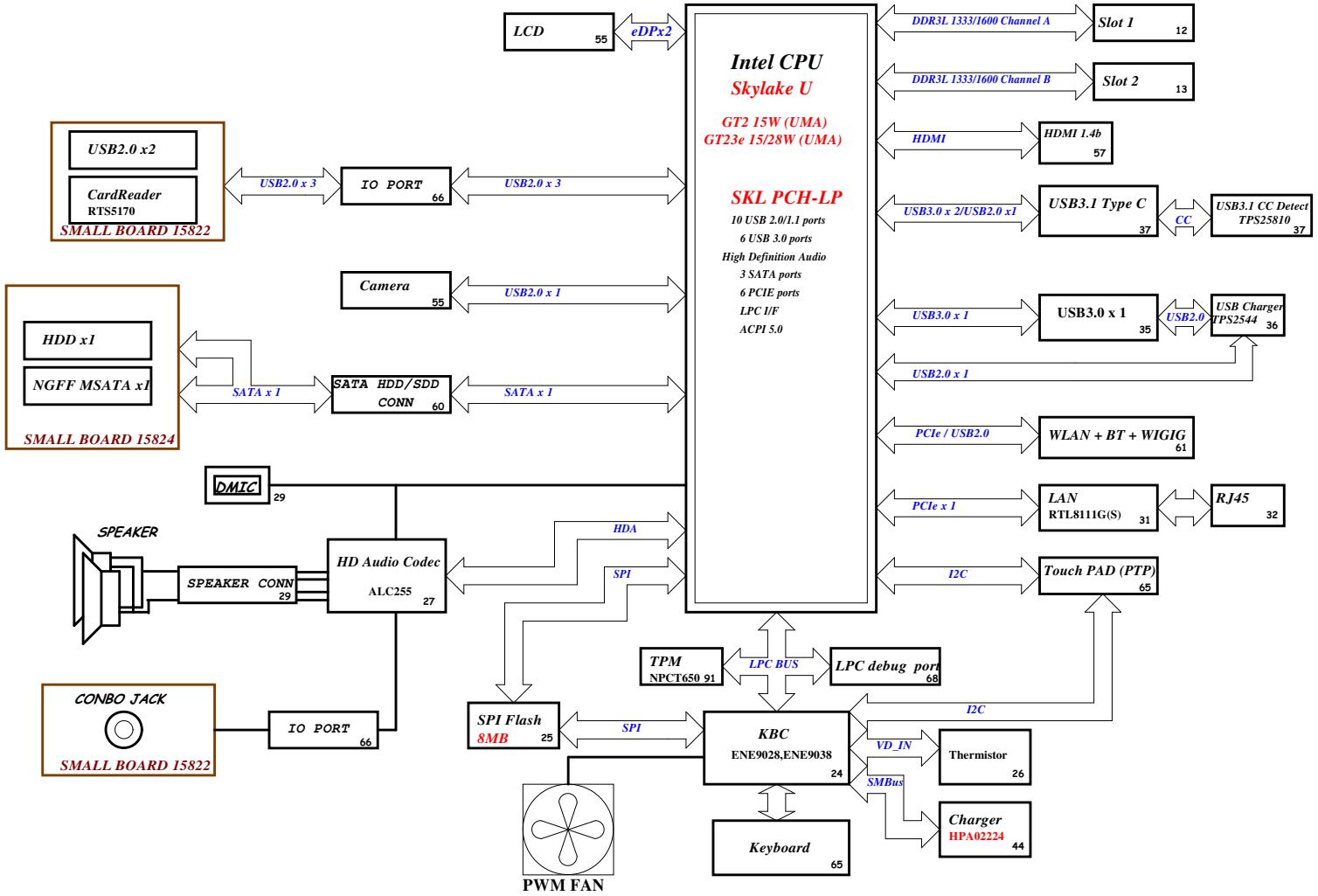
Title: *Cover Page*		
Size: A3	Document Number: Mihawk MB	Rev: -2
Date: Monday, August 10, 2015	Sheet 1 of 105	

Project code:
Mihawk SL 13 --> 4PD06J010001
PCB P/N:15208
Revision: -1



CHARGER HPA02224	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT6575D	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power ISL95857HRTZ-T-GP	46
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS RT8231AGQW-GP	51
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

CPU 1D0V_S5 RT8231AGQW-GP	52
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

CPU 1.8V_S5 RT8068AZQWID-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	1D8V_S5

Switches	40
INPUTS	OUTPUTS
1D0V_S5	1D0V_EOPIO_EDRAM
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D0V_S5	1V_VCCIO
	1V_VCCST

PCB LAYER

8-1.0-16d

L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND
L6:Signal
L7:GND
L8:Bottom

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Title: Block Diagram

Size: C | Document Number: Mihawk MB | Rev: -2

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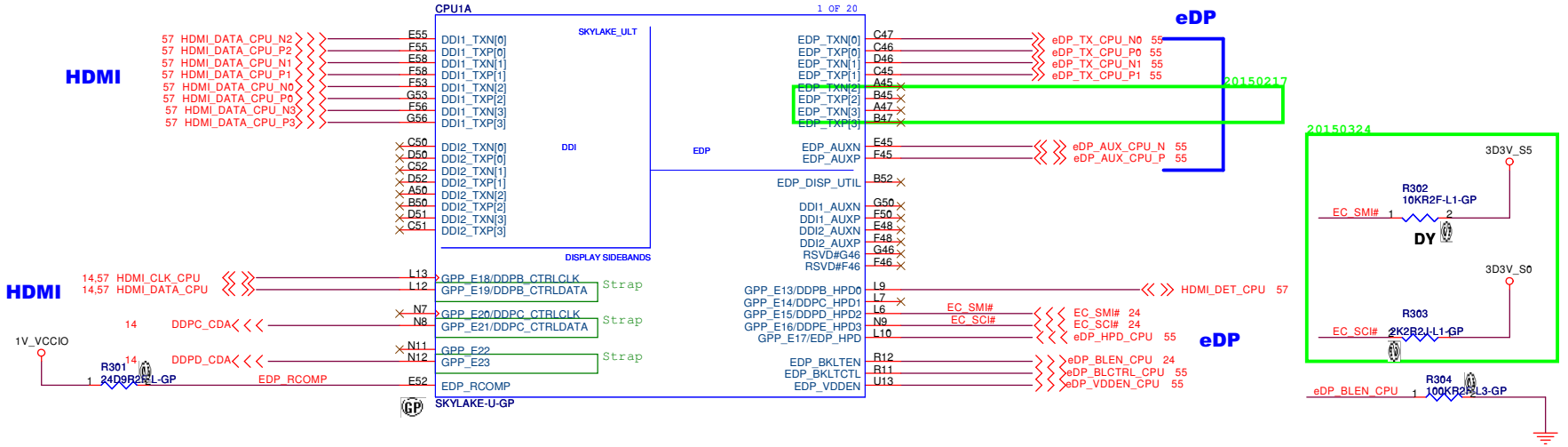
Main Func = CPU



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9Ω ±1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1%Ω resistor.

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Title: CPU_(DISPLAY)

Size	Document Number	Rev
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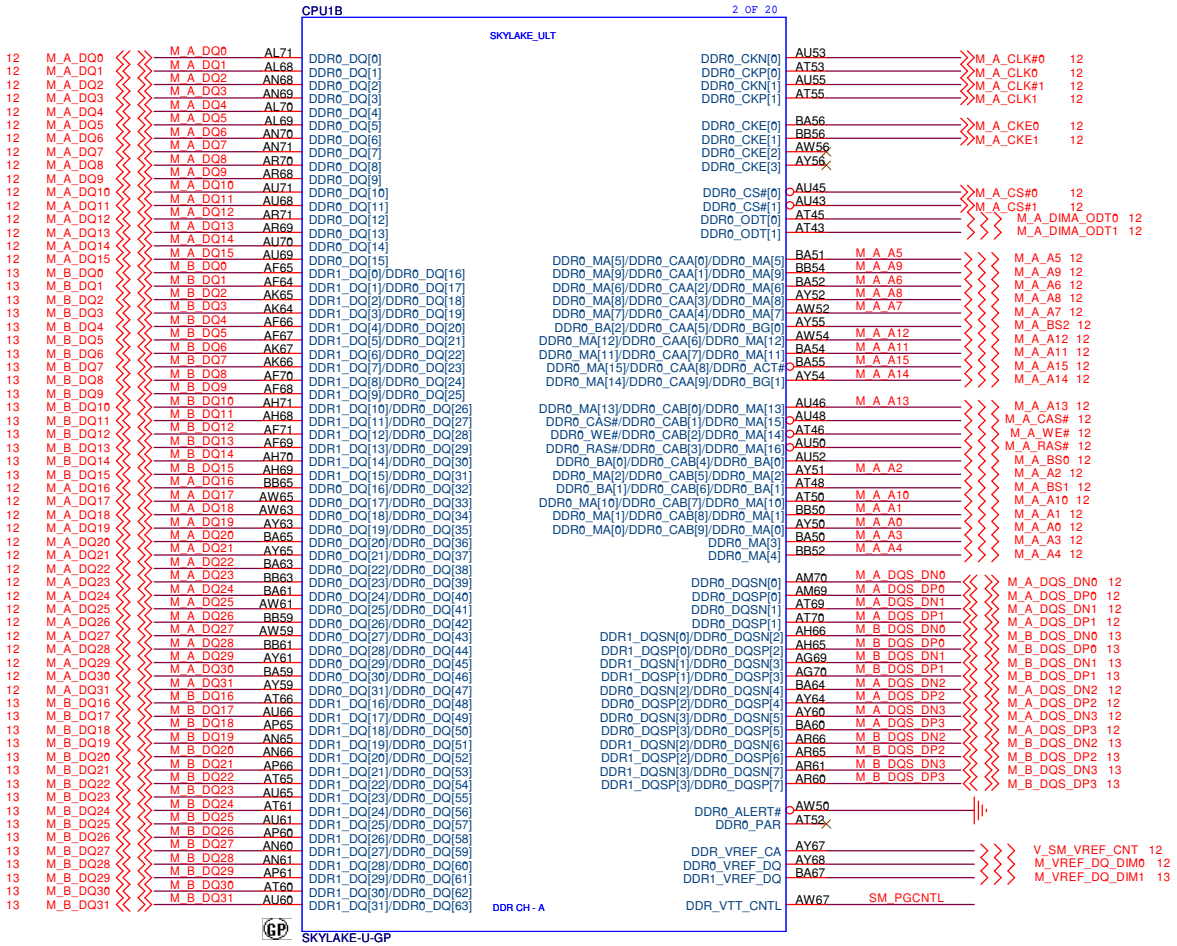
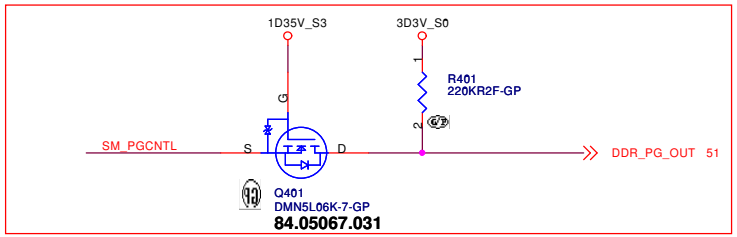
Main Func = CPU

DDR3L ball type: Interleaved Type





2nd = 084.00138.0A31

20141023 Jack

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Title	CPU_(DDR)	
Size A3	Document Number Mihawk MB	Rev -2
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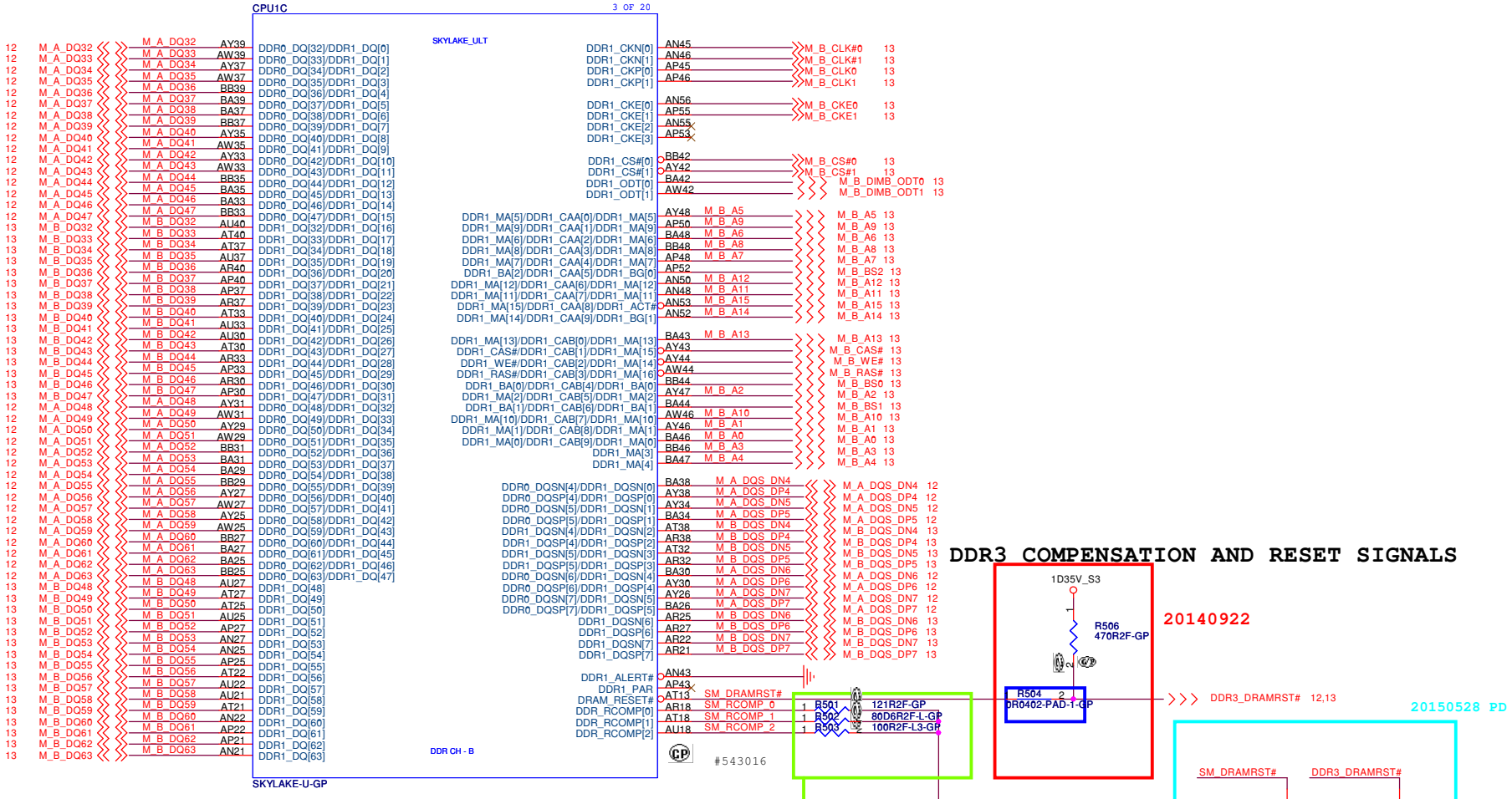
Main Func = CPU



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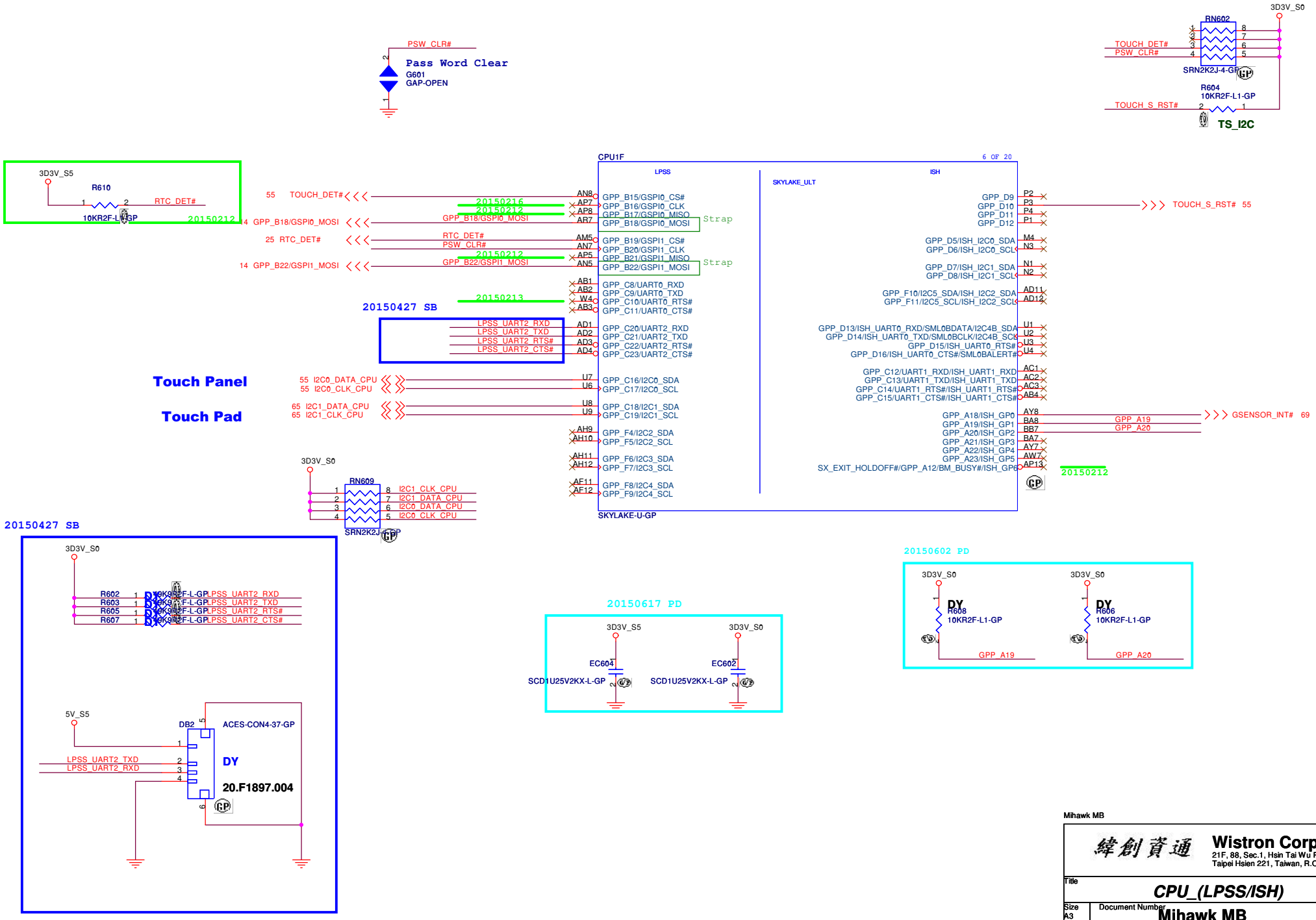
Title	CPU_(DDR)		
Size A3	Document Number Mihawk MB		Rev -2
Date: Monday, August 10, 2015		Sheet 5 of 105	

Main Func = PCH



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Title: CPU_(LPSS/ISH)		
Size: A3	Document Number: Mihawk MB	Rev: -2
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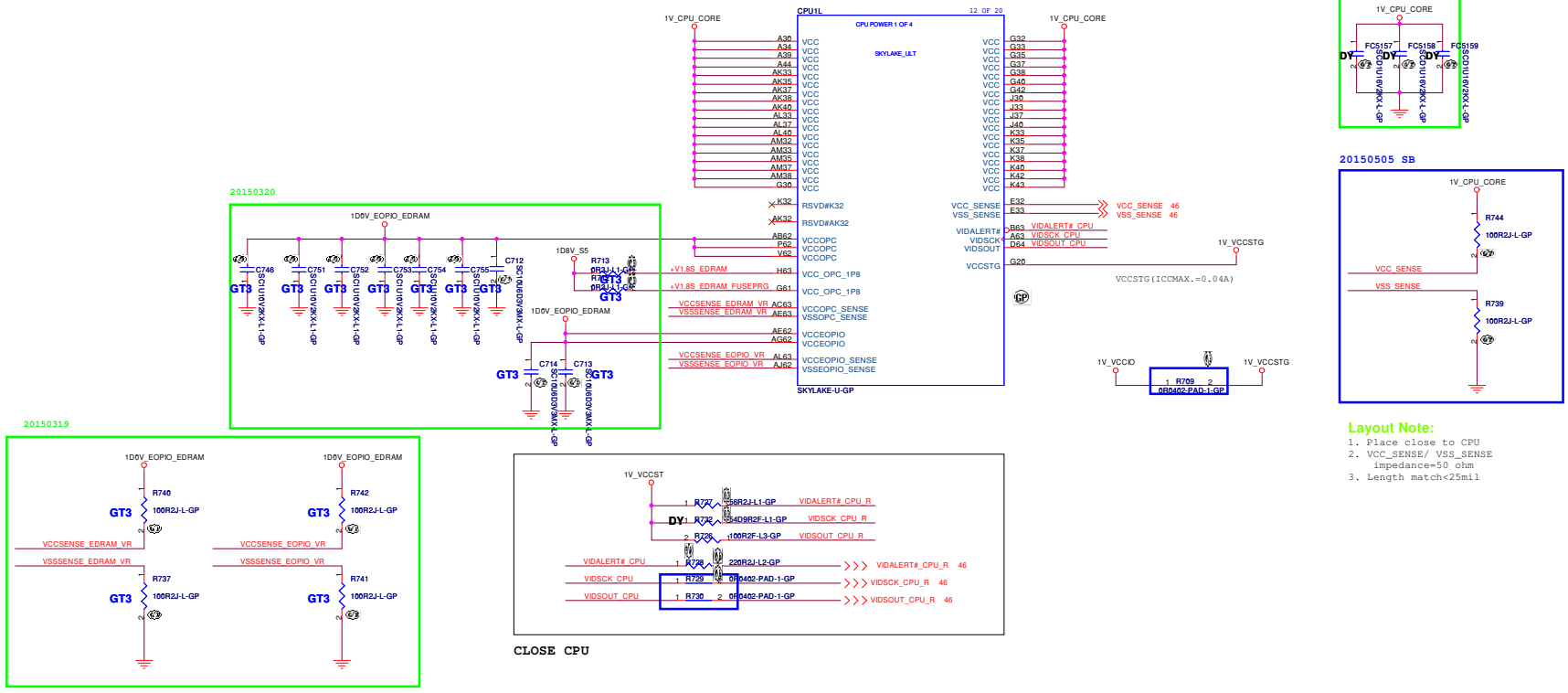
Main Func = CPU



CLOSE CPU

SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

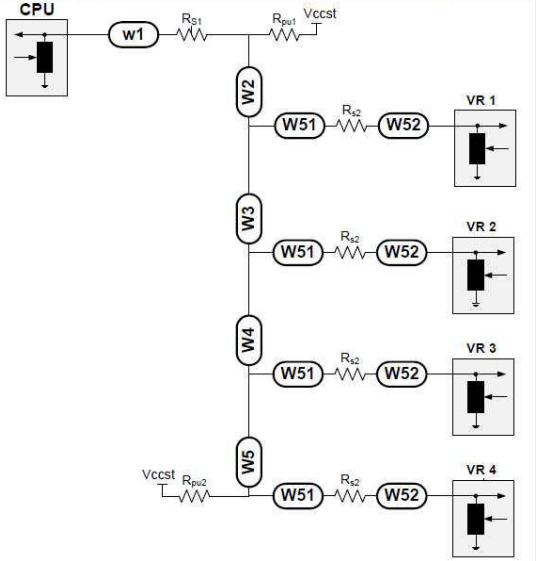


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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Title: CPU_POWER1

Size: A2 | Document Number: Mihawk MB | Rev: -2

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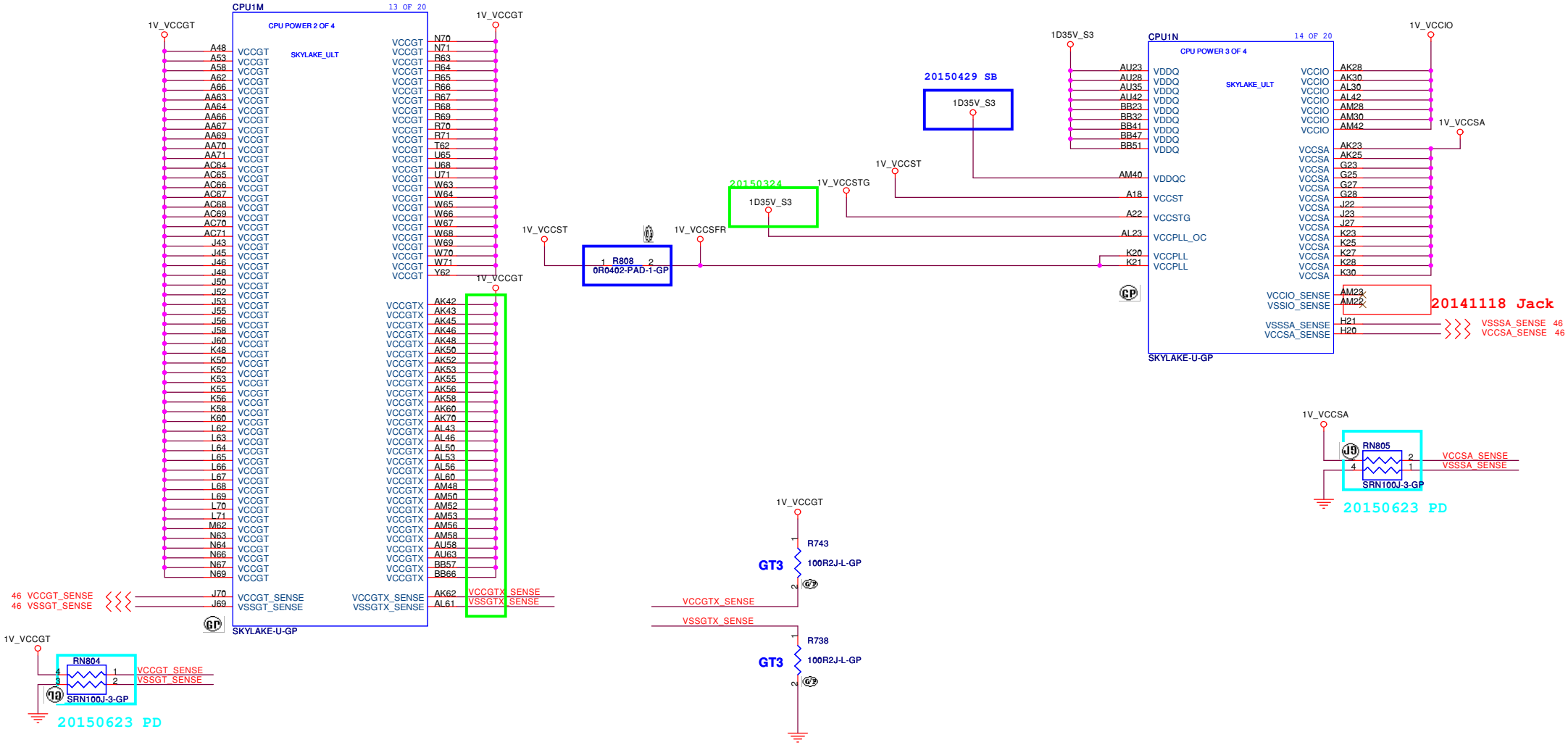
Main Func = CPU



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Title	***CPU_POWER1***	
Size: A3	Document Number: **Mihawk MB**	Rev: **-2**
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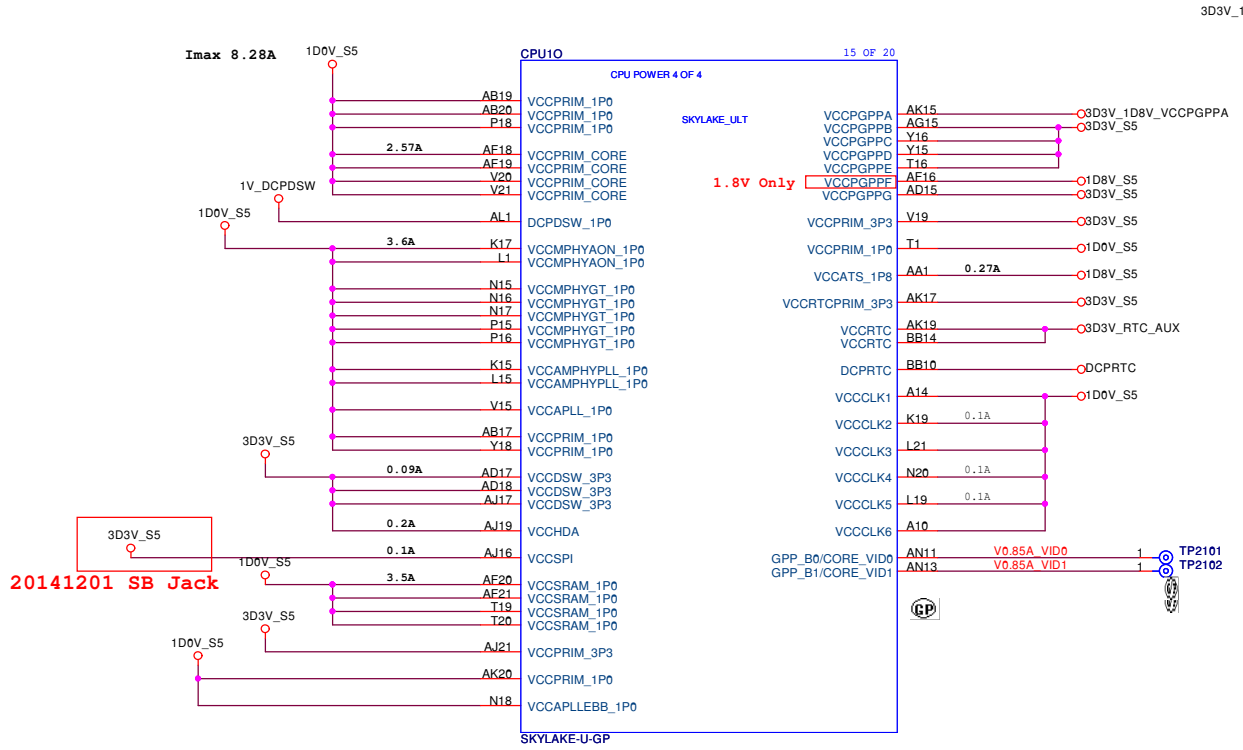
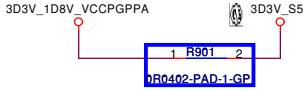
Main Func = PCH





eSPI_508740:

Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM L0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

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Title: *CPU_(POWER1)*

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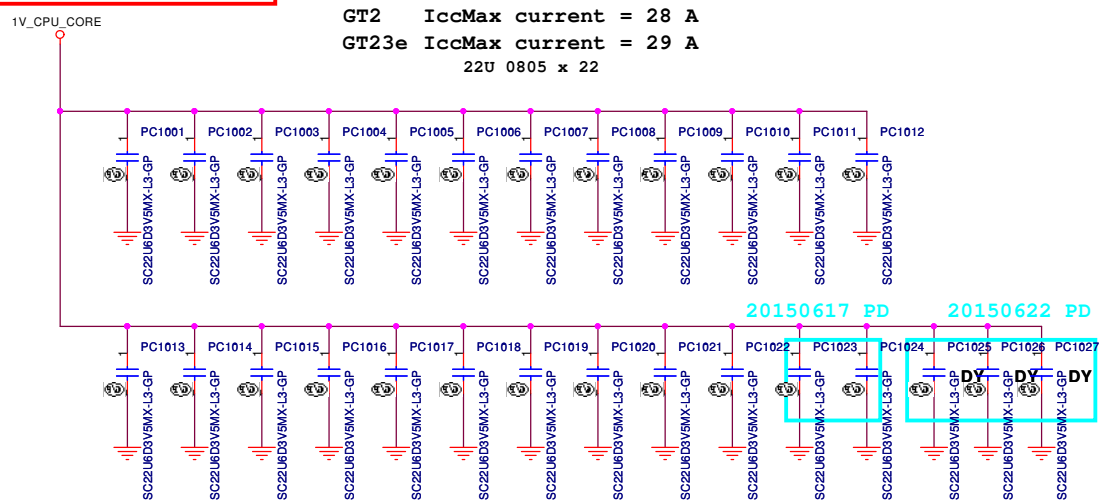
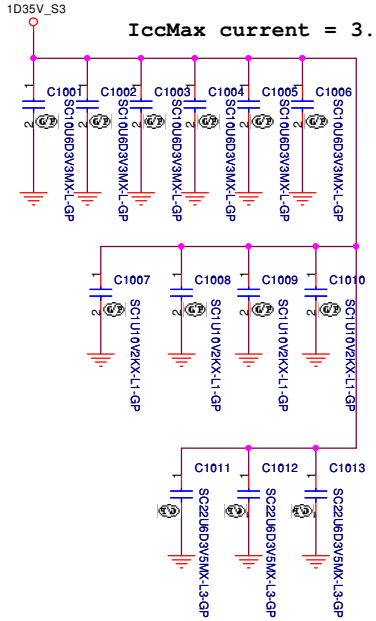
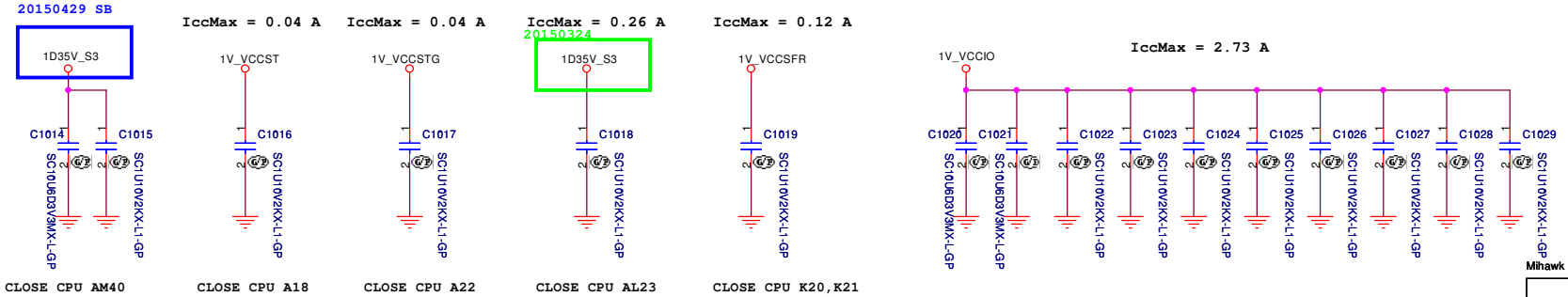
Main Func = CPU





U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	3CA (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								0r	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								0r	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

V_{DDQ}	2x 10 uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1 uF 0201 (Placeholder)		
		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible



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Title	CPU_(Power CAP1)	
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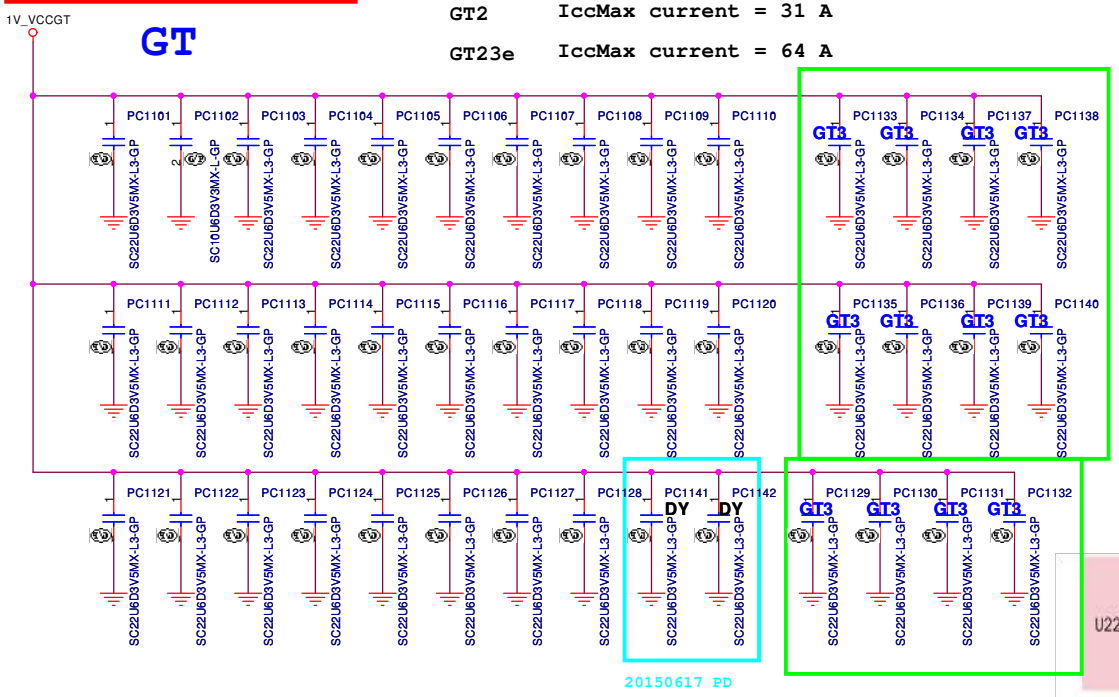
Main Func = CPU

GT

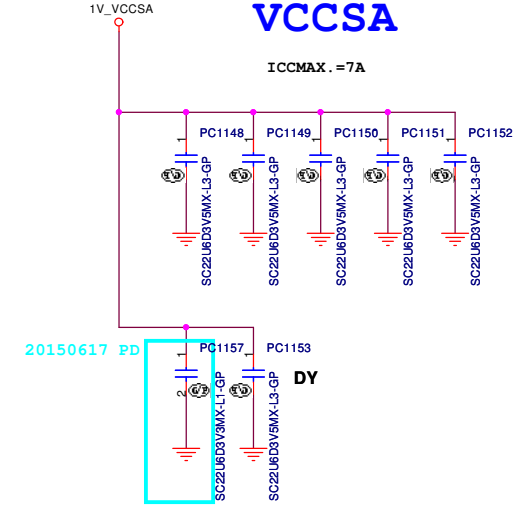
GT2 IccMax current = 31 A

GT23e IccMax current = 64 A

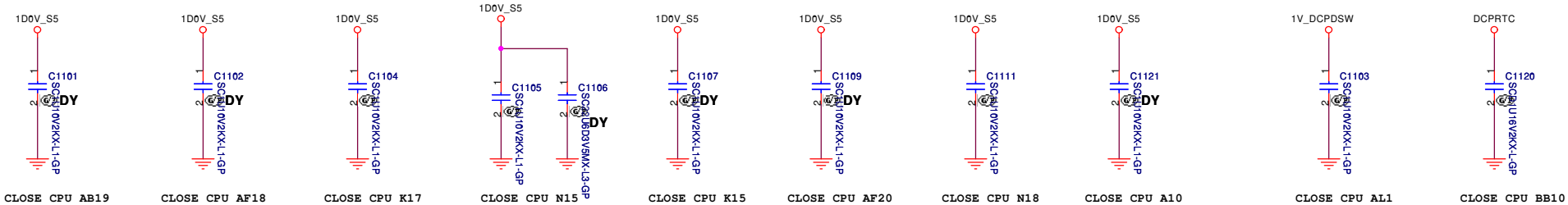


VCCSA

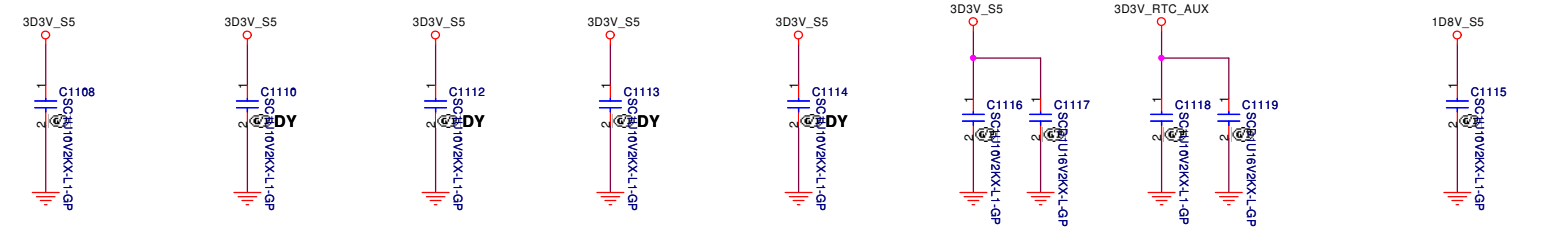
ICCMAX.=7A



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF



CLOSE CPU AB19 CLOSE CPU AF18 CLOSE CPU K17 CLOSE CPU N15 CLOSE CPU K15 CLOSE CPU AF20 CLOSE CPU N18 CLOSE CPU A10 CLOSE CPU AL1 CLOSE CPU BB10



CLOSE CPU AJ19 CLOSE CPU V19 CLOSE CPU AG15 CLOSE CPU Y16 CLOSE CPU T16 CLOSE CPU AK17 CLOSE CPU AK19 CLOSE CPU AA1

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Title	CPU_(Power CAP2)	
Size A3	Document Number Mihawk MB	Rev -2
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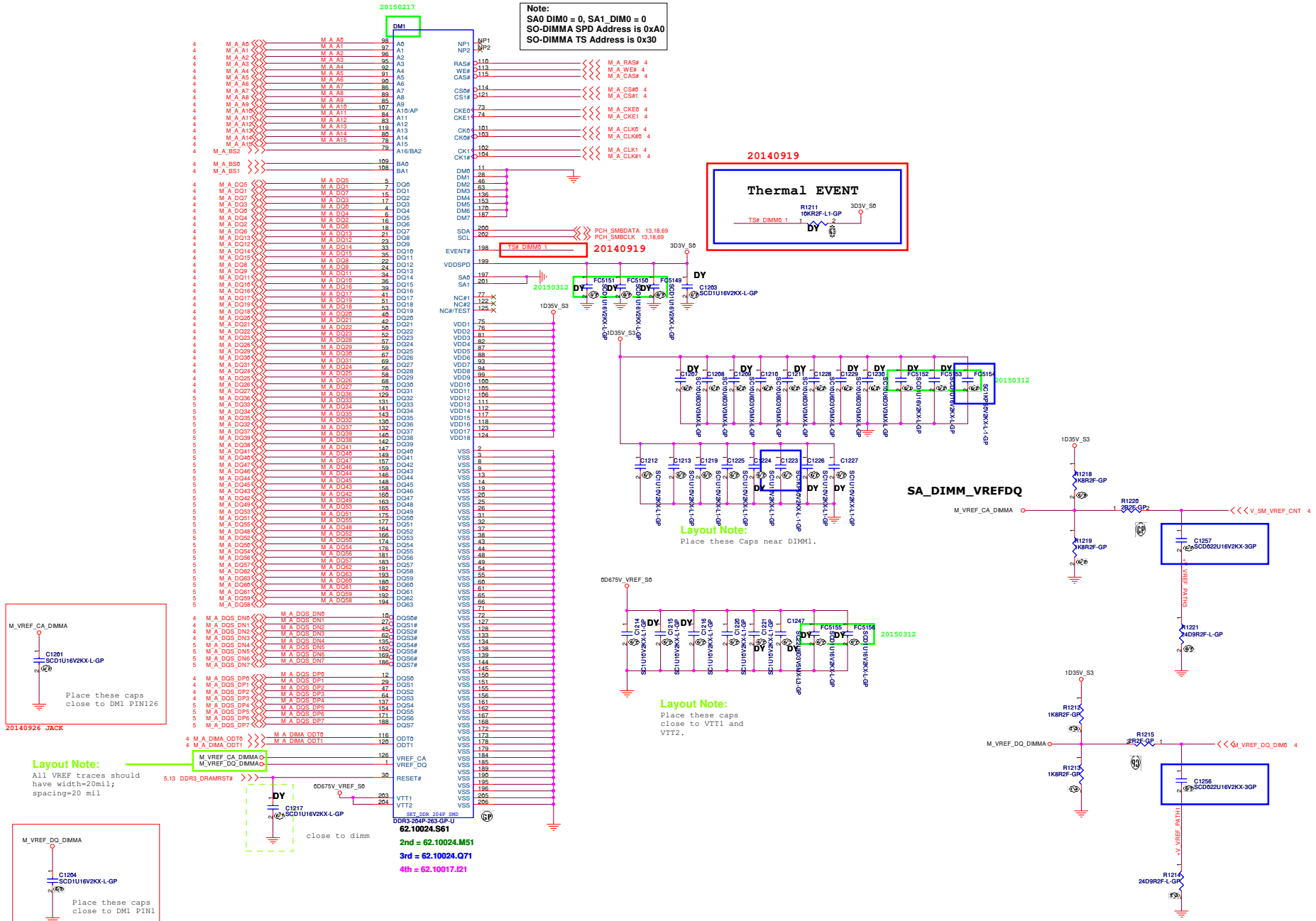
Main Func = DDR SODIMM



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Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
A2	Mihawk MB	-2

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Main Func = DDR SODIMM

20150217

DM2

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

DDR3-204P-262-GP-U

62.10024.S21

2nd = 62.10024.M31

3rd = 62.10024.Q61

4th = 62.10017.I31

20140919

20150312

20150429 SB

20140926 JACK

Layout Note:
Place these caps near DIMM2.

Layout Note:
Place these caps close to DM2 PIN126

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Layout Note:
Place these caps close to DM2 PIN1

close to dimm

Layout Note:
Place Close DIMM2

Thermal EVENT

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Title: DDR3-SODIMM2

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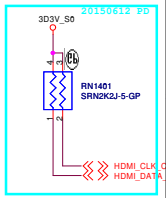
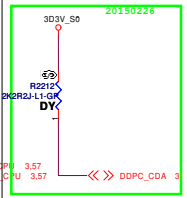
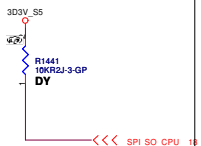
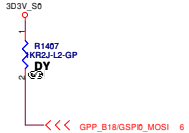
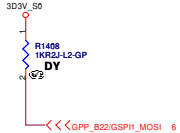
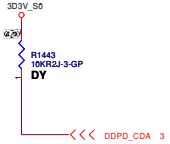
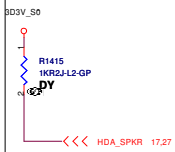
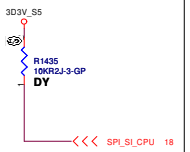
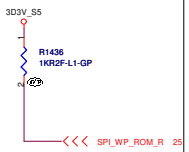
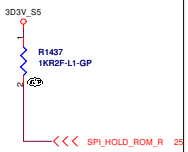
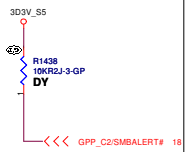
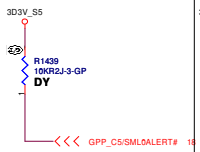
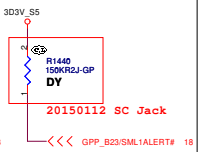
SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected		Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected		Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pul-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

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Title: (Reserved)_SODIMM _SODIMM4

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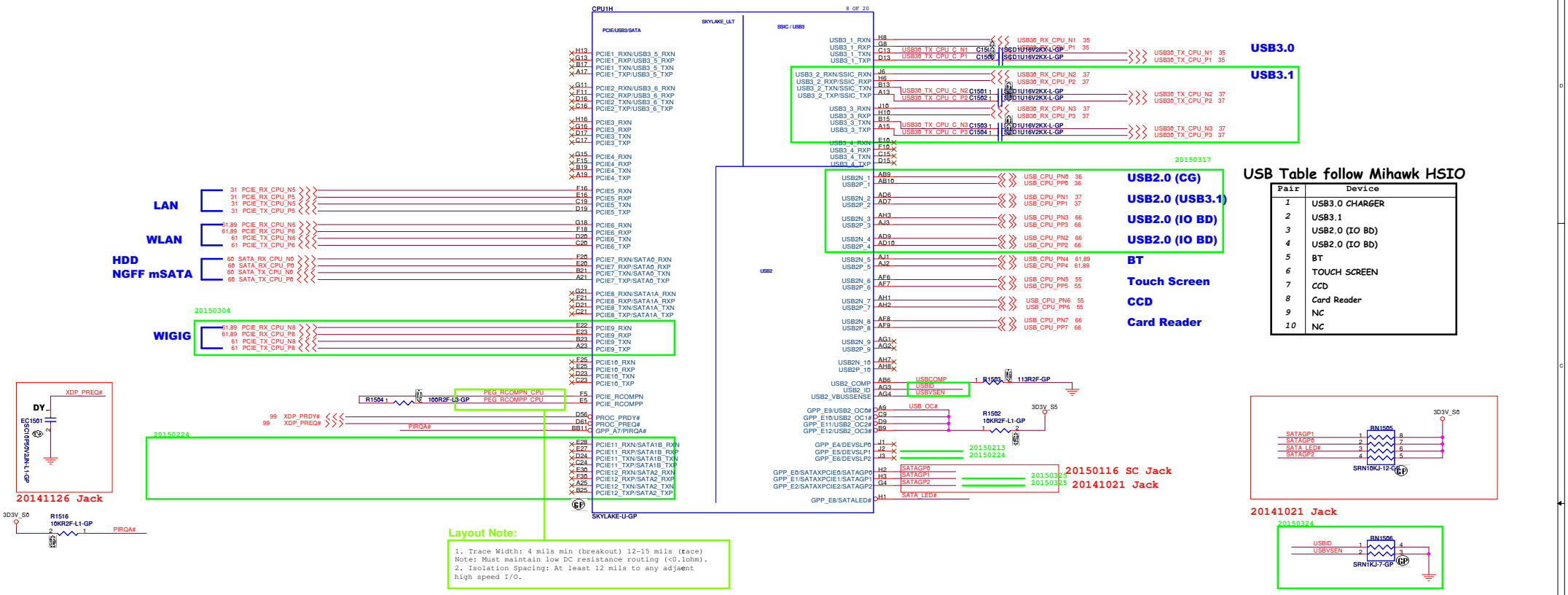
Date: Monday, August 10, 2015 | Sheet 14 of 105

Main Func = PCH



USB Table follow Mihawk HSIO

Pair	Device
1	USB3.0 CHARGER
2	USB3.1
3	USB2.0 (IO BD)
4	USB2.0 (IO BD)
5	BT
6	TOUCH SCREEN
7	CCD
8	Card Reader
9	NC
10	NC

20141021 Jack

SKL Premium U		Acer 2015	Mihawk_SL
Lane1	USB3 Port1	USB 3 (I/O)	USB 3 (I/O)
Lane2	USB3 Port2	USB 3 (I/O)	USB 3(Type C)
Lane3	USB3 Port3	USB 3 (I/O)	USB 3(Type C)
Lane4	USB3 Port4		
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU
Lane6	USB3 Port6 (Premium)	PCIe Port2	
Lane7		PCIe Port3	
Lane8		PCIe Port4	
Lane9		PCIe Port5	LAN
Lane10		PCIe Port6	WIFI
Lane11	SATA0(Base/Premium)	PCIe Port7 (Premium)	HDD
Lane12	SATA1(Base/Premium)	PCIe Port8 (Premium)	ODD
Lane13		PCIe Port9	NA / M.2 SSD (PCIeX4) * BIOS needs to set PCIE x4 Lane reversal
Lane14		PCIe Port10	
Land15	SATA1 (Premium)	PCIe Port11	
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x 1)
	USB2 Port1		USB 3 (I/O)
	USB2 Port2		USB 3 (I/O)
	USB2 Port3		USB 3 (I/O)
	USB2 Port4		USB 2 (I/O)/Sensor Hub
	USB2 Port5		BT
	USB2 Port6		TS
	USB2 Port7		CCD
	USB2 Port8		CR(USB)/FP
	USB2 Port9 (Premium)		3G
	USB2 Port10 (Premium)		

Mihawk_SL
USB 3 (I/O)
USB 3(Type C)
USB 3(Type C)
LAN
WIFI
HDD / M.2 SSD (SATA)
WIGIG (PCIe x1)
USB 3 (I/O)
USB 2(Type C)
USB 2 (I/O) for DB
USB 2 (I/O) for DB
BT
TS
CCD
CR

Mihawk MB

Wistron Corporation
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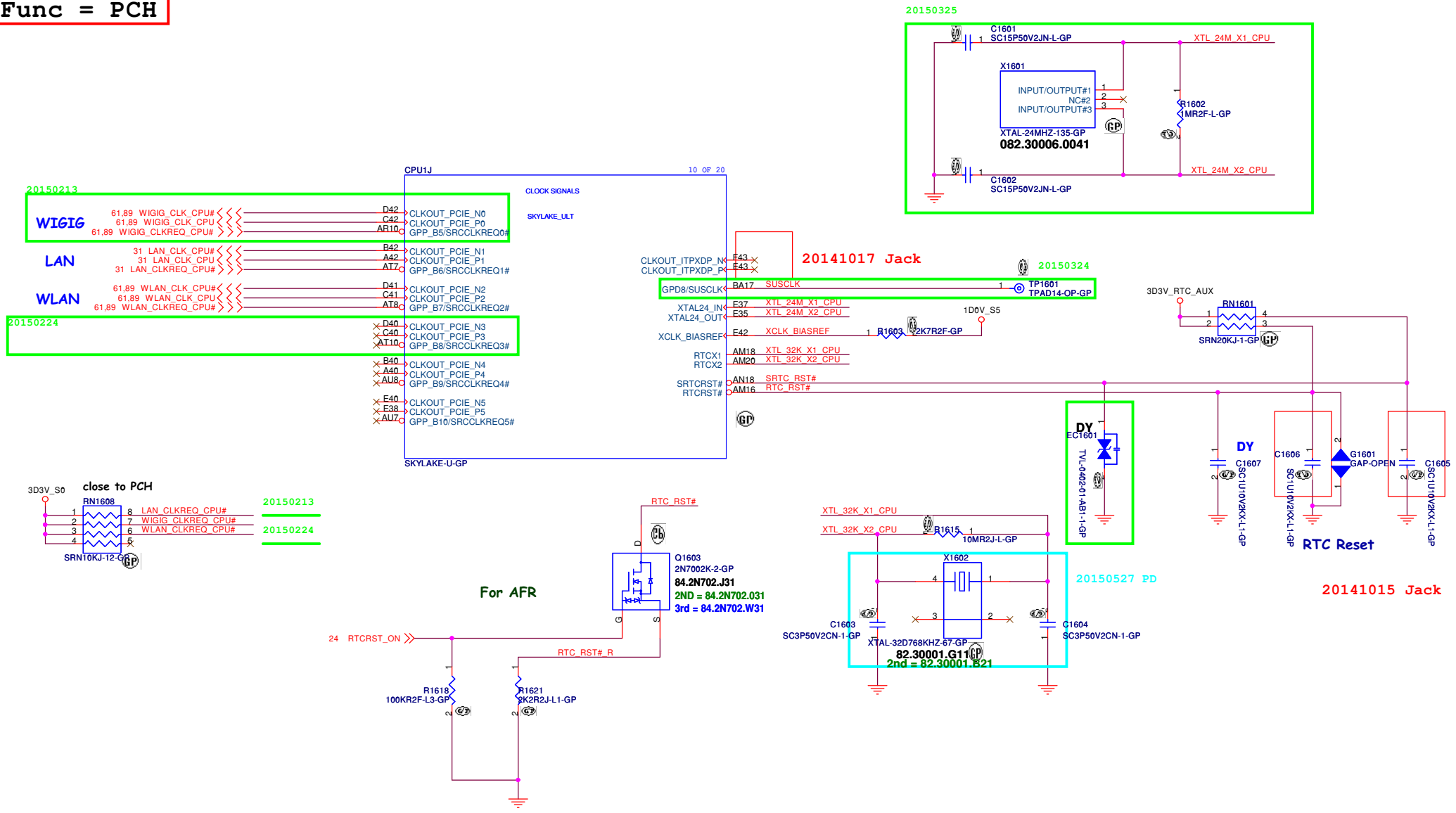
Title: CPU_(PCIE/SATA/USB)

Size: A2 | Document Number: Mihawk MB | Rev: -2

Date: Monday, August 10, 2015 | Sheet 15 of 105

Main Func = PCH



Mihawk MB

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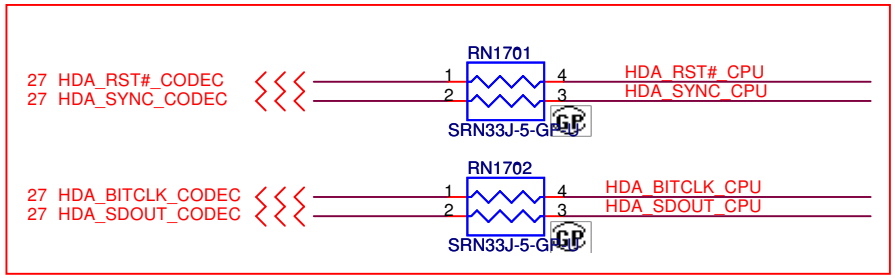
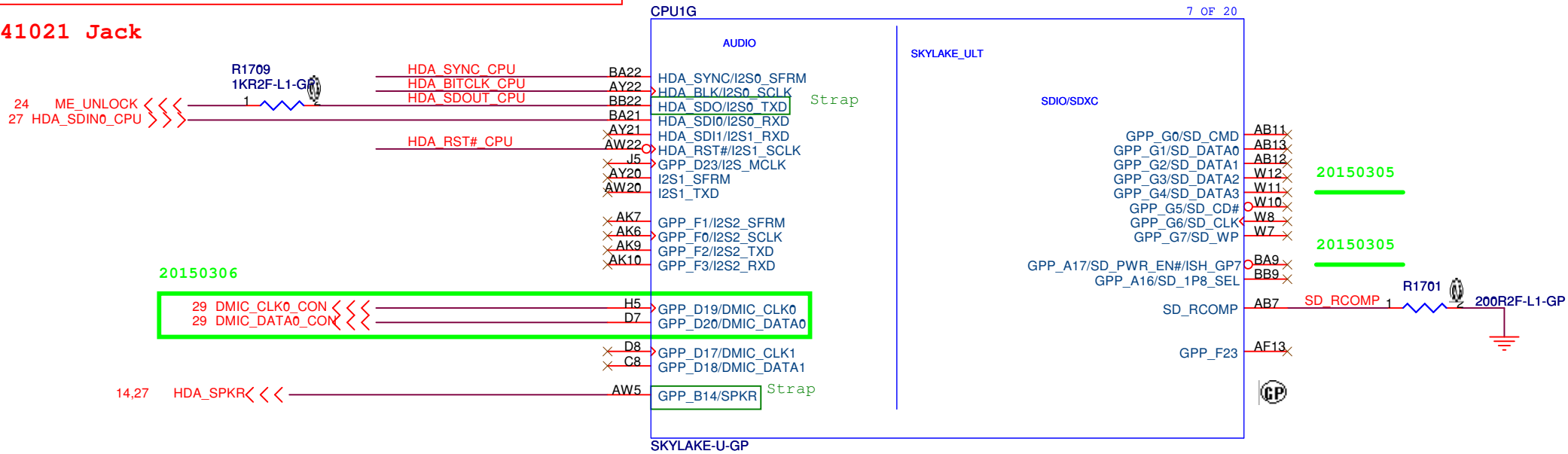
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***MCP_CLOCK***	
Size A3	Document Number **Mihawk MB**	Rev **-2**
Date: Monday, August 10, 2015	Sheet 16 of 105	

Main Func = PCH



20141021 Jack



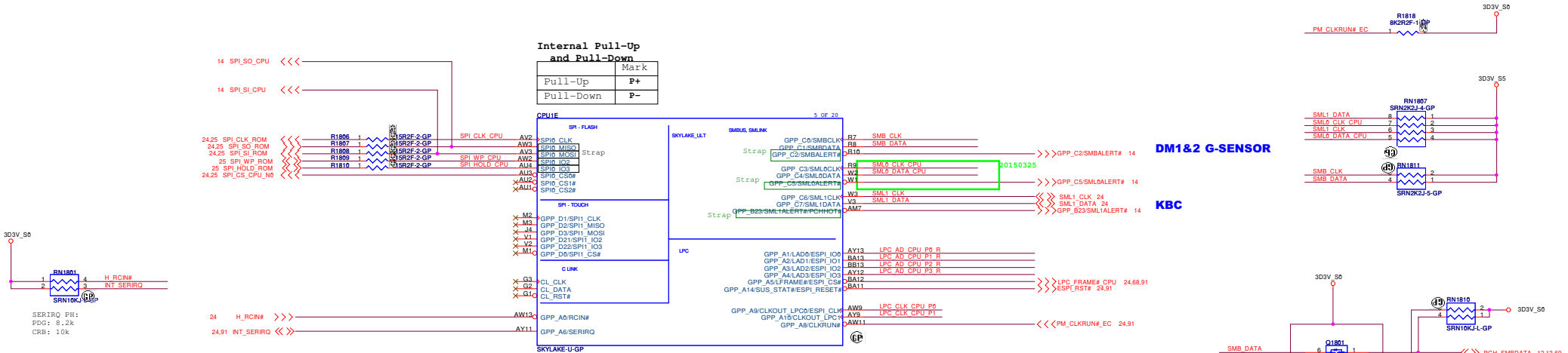
Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU_(AUDIO/SDIO/SDXC)*	
Size A4	Document Number **Mihawk MB**	Rev **-2**
Date: Monday, August 10, 2015	Sheet 17 of 105	

Main Func = PCH



Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

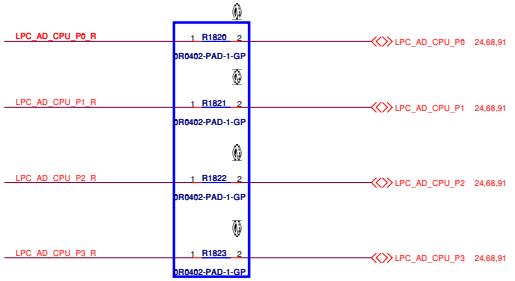
20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.



Mihawk MB

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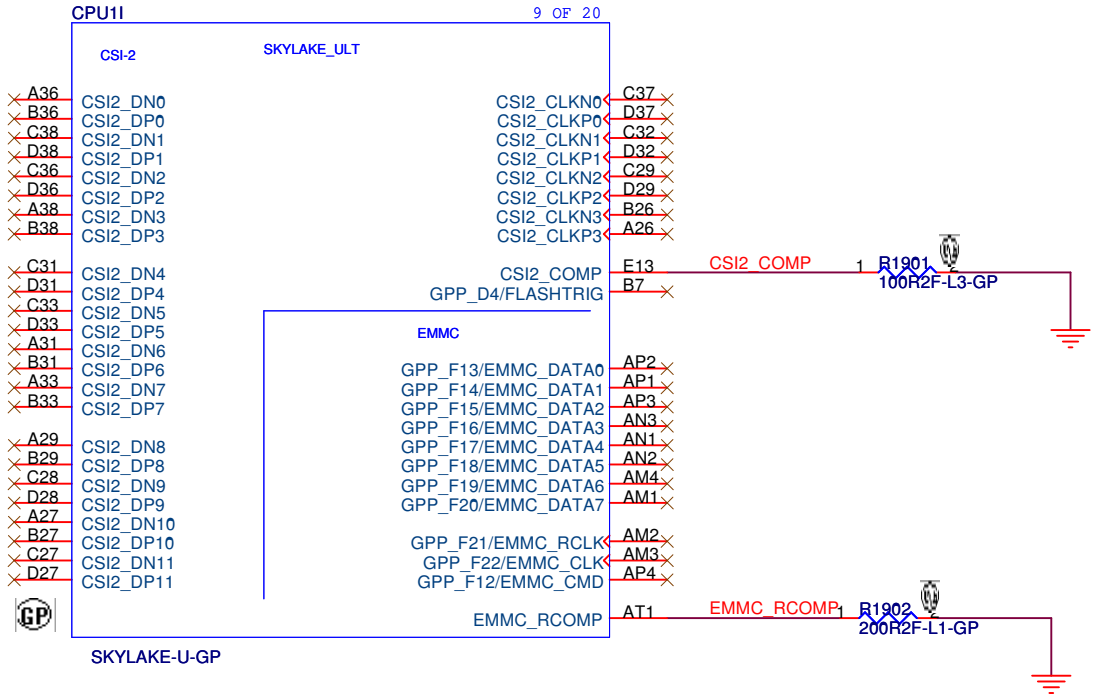
Title: LPC,SPI,SMBUS,CLINK

Size: A2 | Document Number: Mihawk MB | Rev: -2

Date: Monday, August 10, 2015 | Sheet 18 of 105

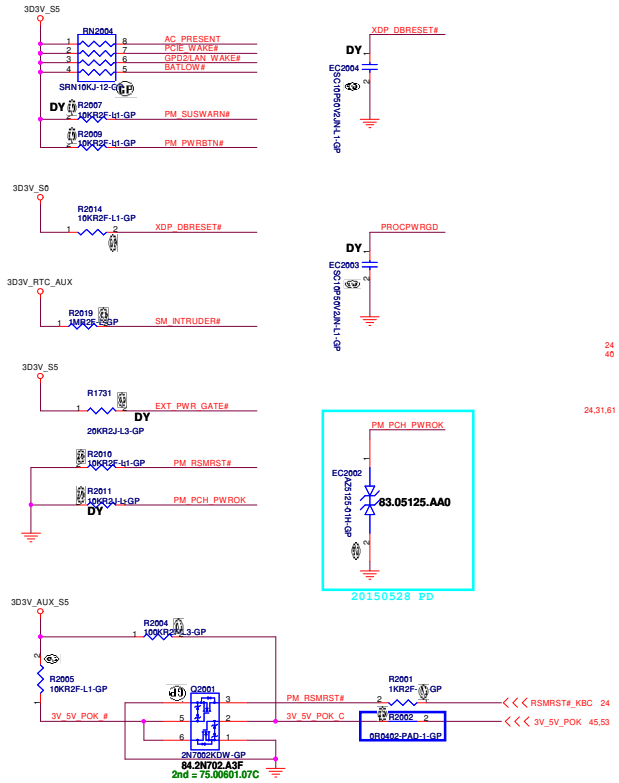
Main Func = PCH

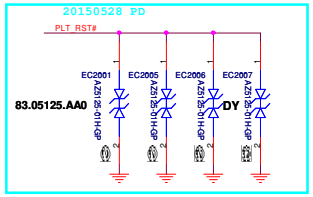


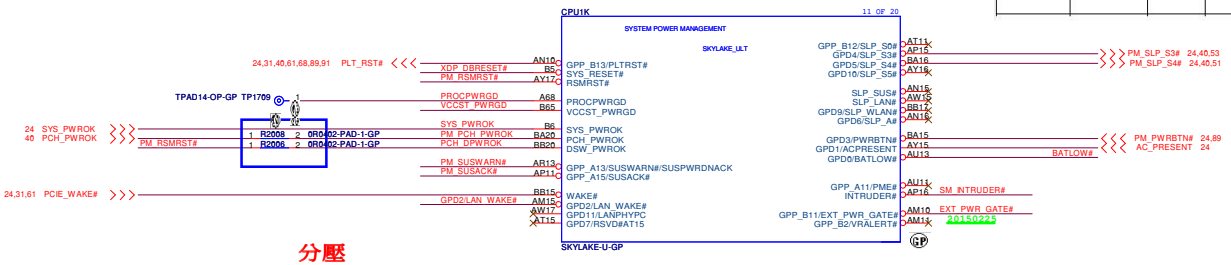
Mihawk MB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_(CS-2/EMMC)***	
Size A4	Document Number **Mihawk MB**	Rev **-2**
Date: Monday, August 10, 2015	Sheet 19 of 105	

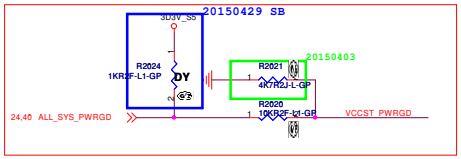
Main Func = PCH





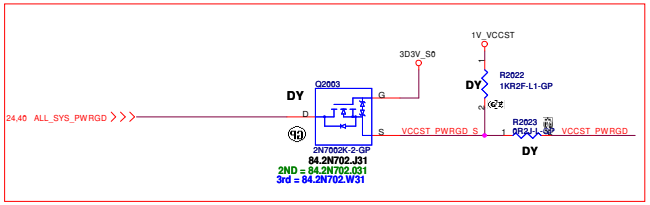


分壓



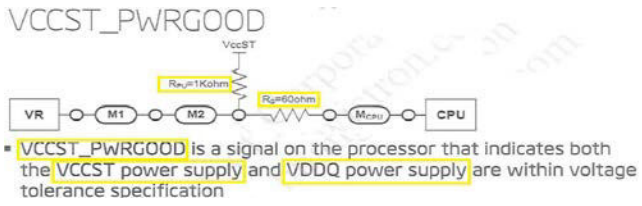
20150113 SB Jack

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST



20150113 SB Jack

VCCST_PWRGD / HWM201:



GPP_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

Mihawk MB

緯創資通 Wistron Corporation
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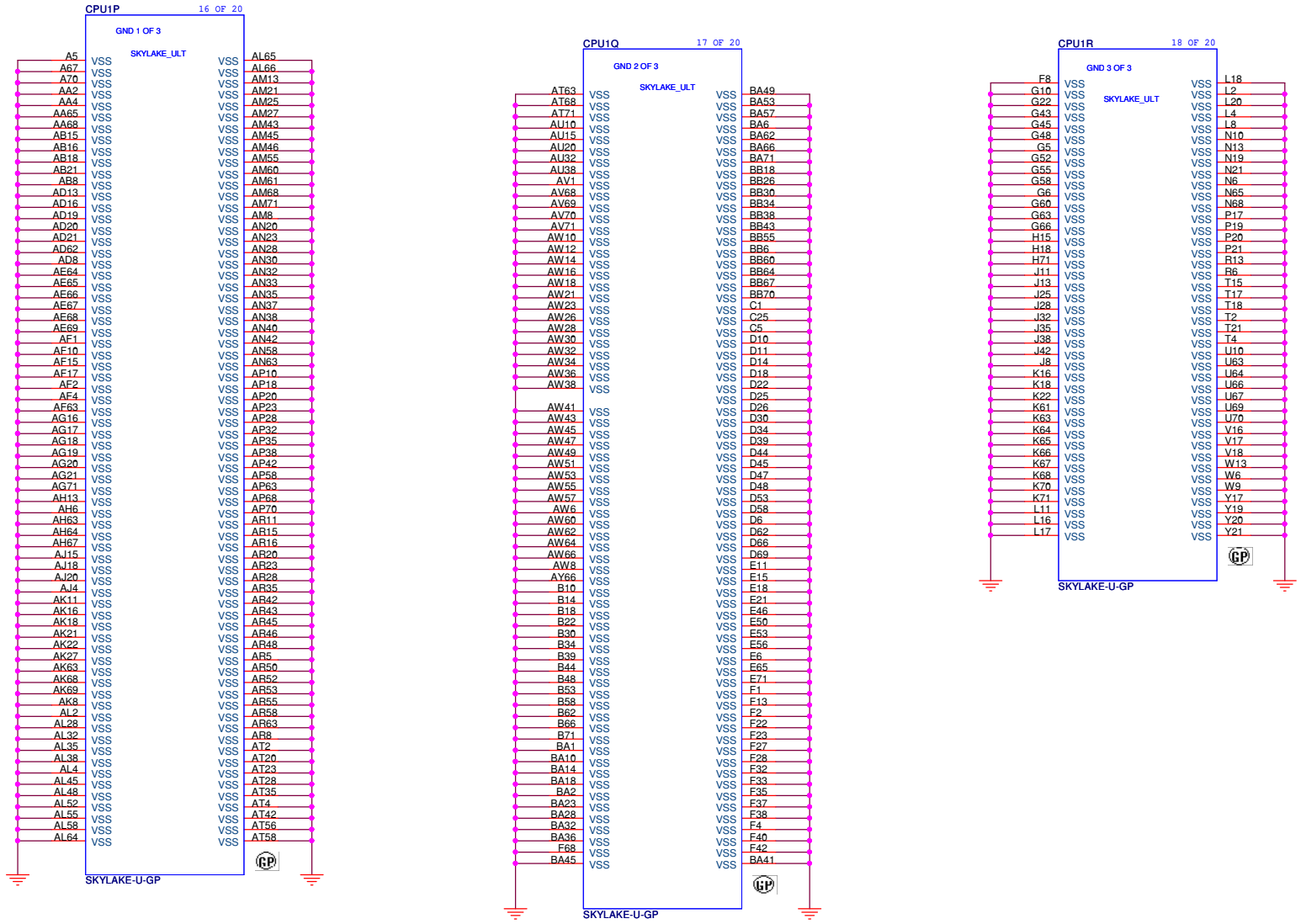
Title: CPU_(POWER MANAGEMENT)

Size: A2 | Document Number: Mihawk MB | Rev: -2

Date: Monday, August 10, 2015 | Sheet 20 of 105

Main Func = PCH



Mihawk MB

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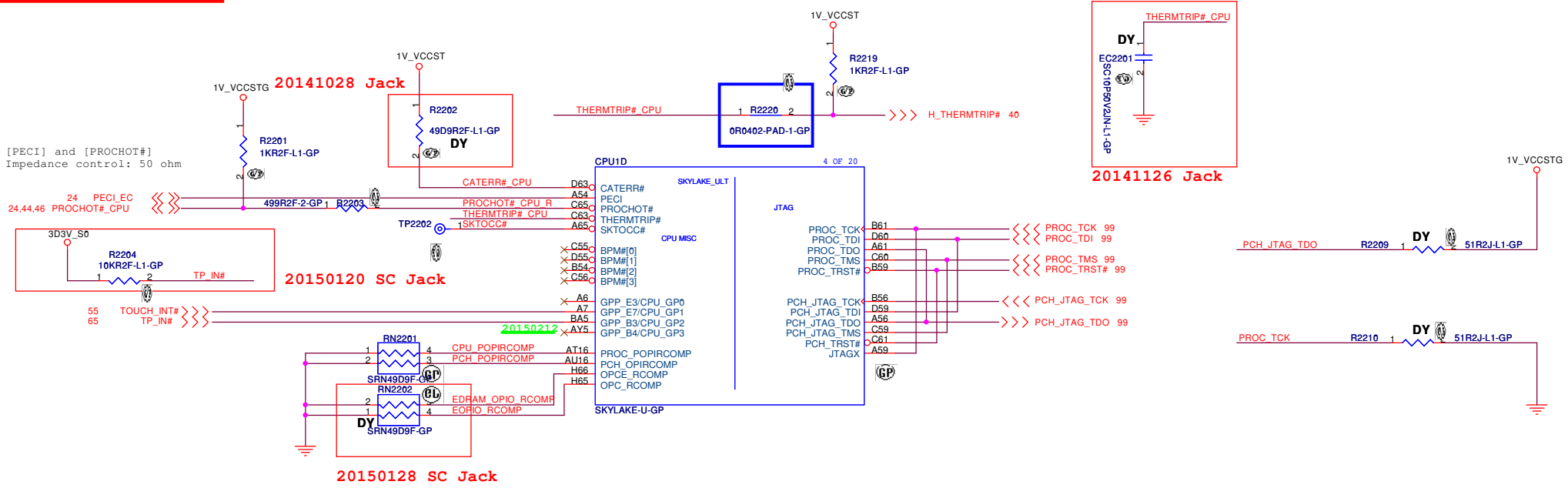
Taipei Hsien 221, Taiwan, R.O.C.

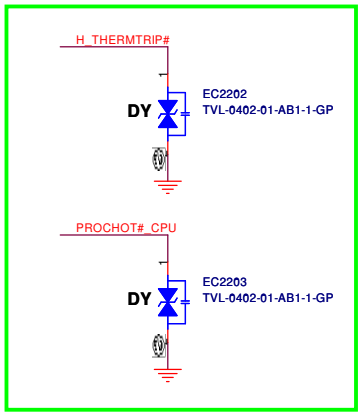
Title	CPU_(VSS)	
Size A3	Document Number Mihawk MB	Rev -2
Date: Monday, August 10, 2015	Sheet 21 of 105	

Main Func = CPU



PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

20150324



Mihawk MB

緯創資通 Wistron Corporation
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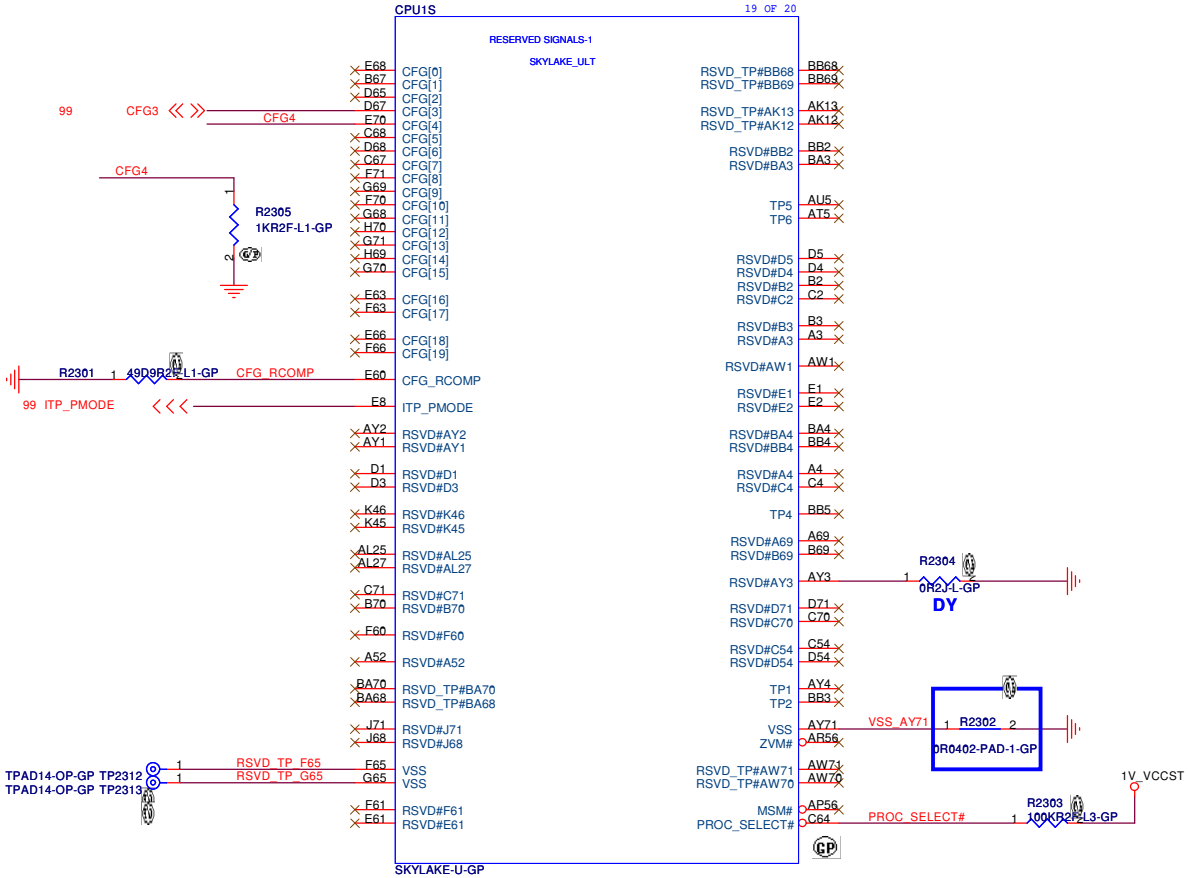
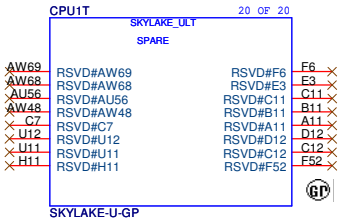
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(JTAG/CPU SIDE BAND)	
Size A3	Document Number Mihawk MB	Rev -2
Date: Monday, August 10, 2015	Sheet 22 of 105	

Main Func = CPU

CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.





PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines

Mihawk MB

緯創資通 **Wistron Corporation**
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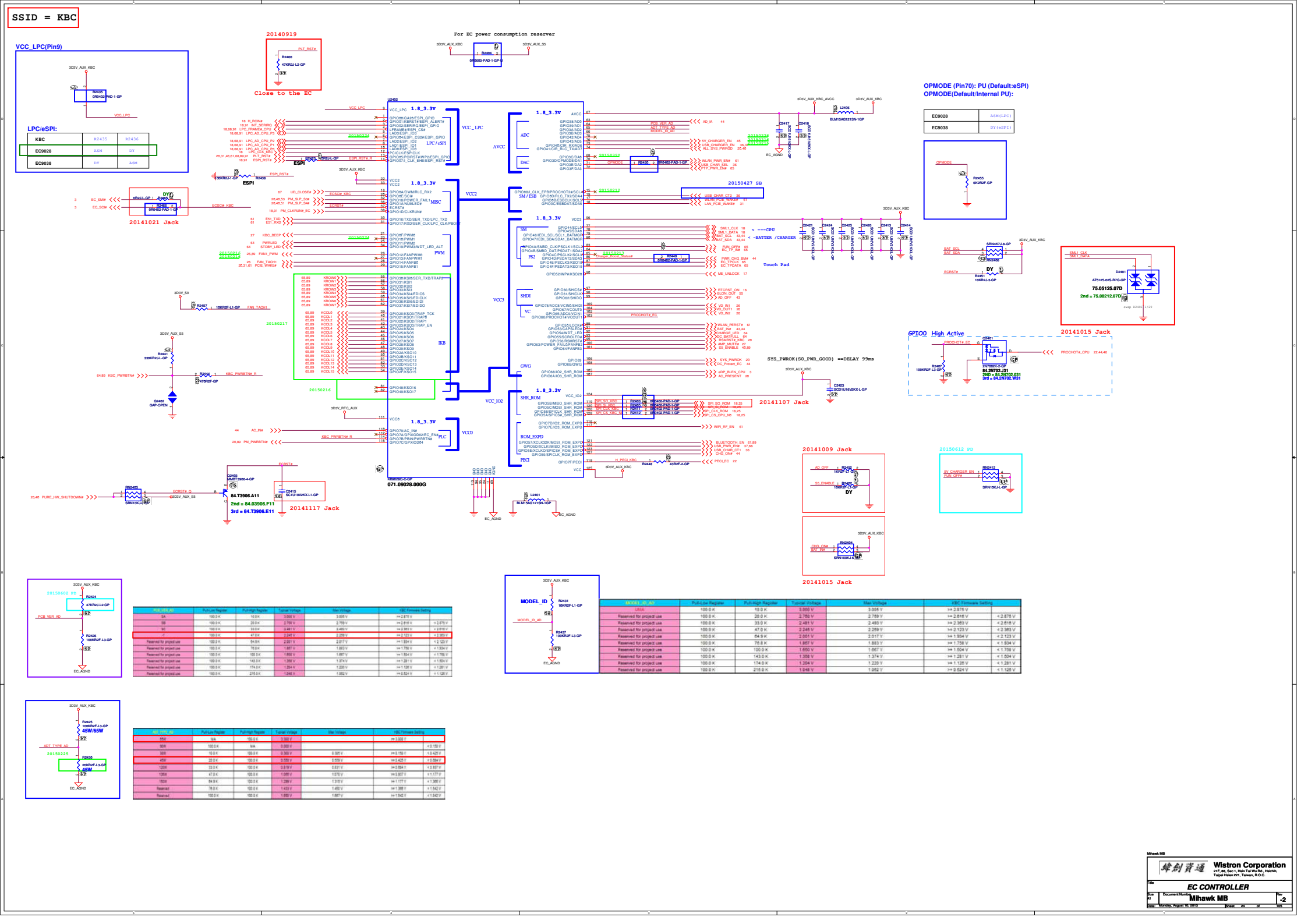
Title: **CPU_RESERVED,CFG**

Size	Document Number	Rev
A3	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 23 of 105

SSID = KBC



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.300 V	3.305 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.615 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.489 V	>= 2.363 V	< 2.615 V
-/-	100.0 K	47.0 K	2.248 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.021 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	78.8 K	1.867 V	1.883 V	>= 1.756 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.693 V	1.667 V	>= 1.504 V	< 1.756 V
Reserved for project use	100.0 K	143.0 K	1.359 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.924 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	NA	100.0 K	3.300 V		>= 2.500 V	
90W	100.0 K	NA	0.000 V			< 0.150 V
300	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.594 V
120W	33.0 K	100.0 K	0.618 V	0.631 V	>= 0.594 V	< 0.837 V
135W	47.0 K	100.0 K	1.065 V	1.076 V	>= 0.837 V	< 1.177 V
150W	64.9 K	100.0 K	1.209 V	1.319 V	>= 1.177 V	< 1.386 V
Reserved	78.8 K	100.0 K	1.403 V	1.460 V	>= 1.386 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.542 V

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
URMA	100.0 K	10.0 K	3.300 V	3.305 V	>= 2.875 V	
Reserved for project use	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.615 V	< 2.875 V
Reserved for project use	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.615 V
Reserved for project use	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	78.8 K	1.867 V	1.883 V	>= 1.756 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.756 V
Reserved for project use	100.0 K	143.0 K	1.359 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.924 V	< 1.126 V

Mihawk MB

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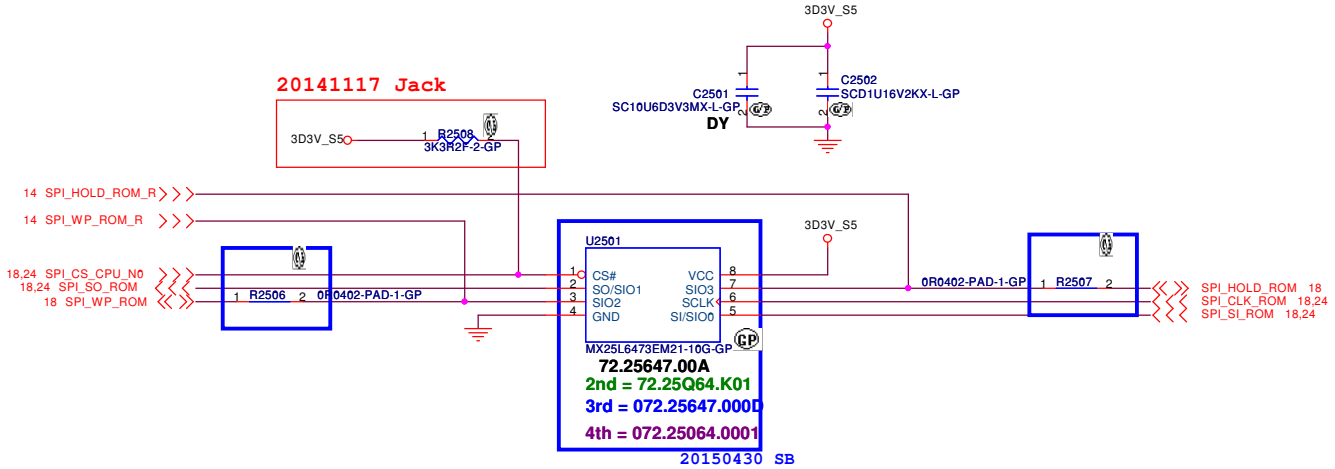
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EC CONTROLLER

Size: A1 | Document Number: Mihawk MB | Rev: -2

Date: Monday, August 10, 2015 | Sheet 24 of 105

Main Func = SPI Flash



SPI FLASH ROM (8M byte) for PCH

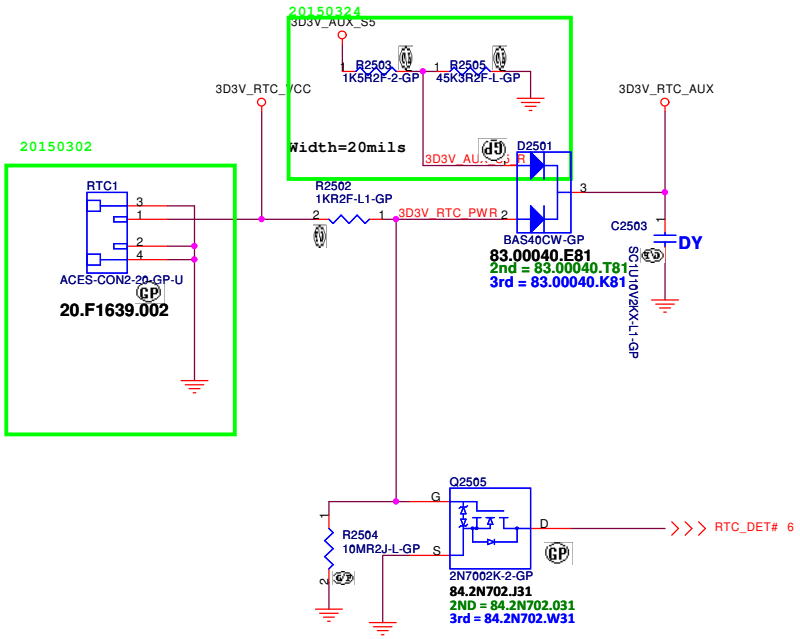
SPI ROM Equal length need to less than 500mil

20150312

SPI FLASH ROM (8M byte)

1st=72.25647.00A (MXIC MX25L6473EM2I-10G)
2nd=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
3rd=072.25647.000D(MXIC MX25L6473F)
4th=072.25064.0001(ISSI IC25LP064A-QBLE)

Main Func = RTC



Mihawk MB

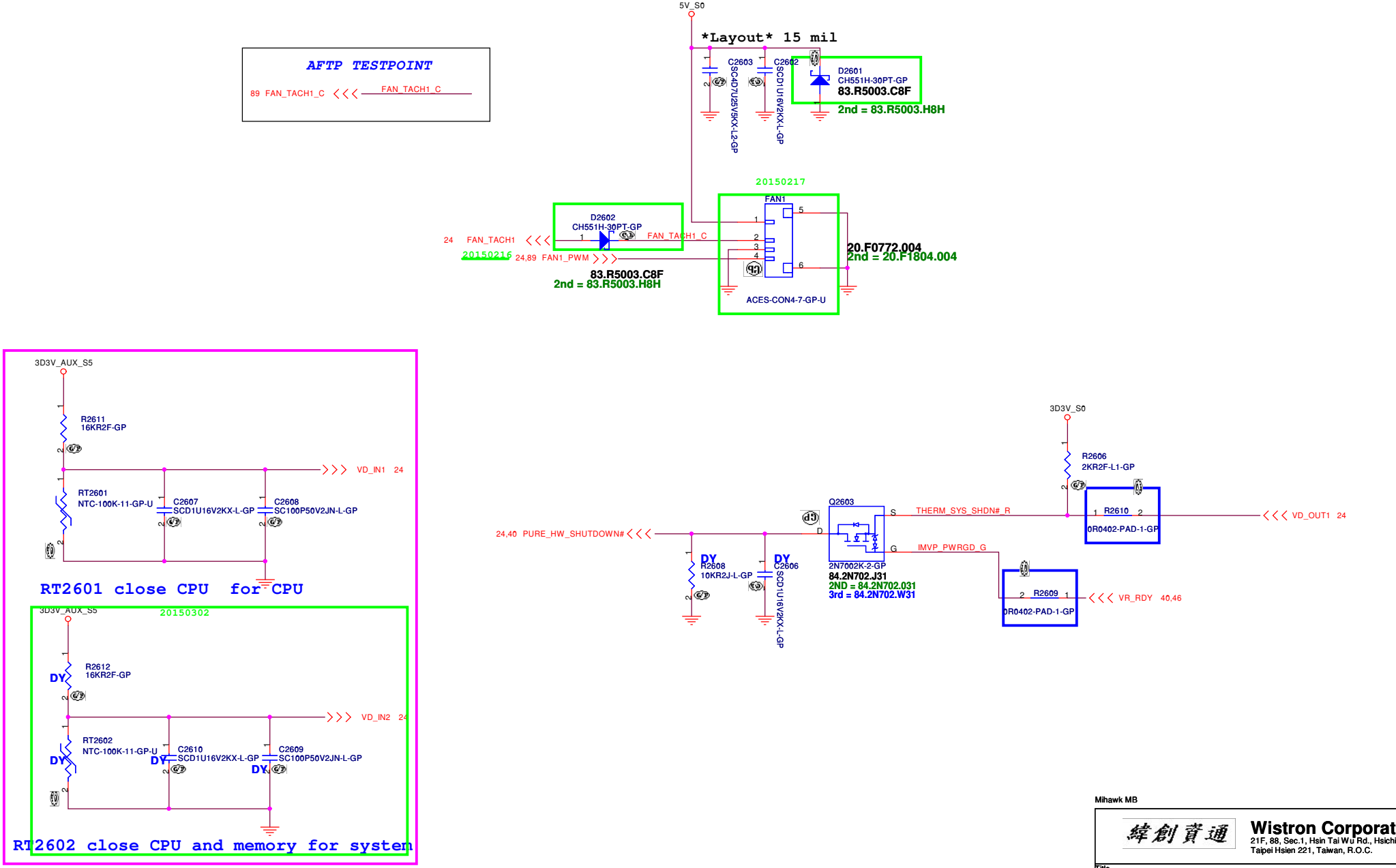
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC

Size	Document Number	Rev
A3	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 25 of 105

Main Func = Thermal Sensor



Mihawk MB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G788P81/Fan Controllor P2793

Size	Document Number	Rev
A3	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 26 of 105

SSID = 104C

20150617 PD

20141009 Jack

20141015 Jack

20141030 Jack

20150121 SC Jack

FOR EMI

AUD_AGND close to codec IC

placed nearby codec PIN12

Close to Pin46

Close to Pin41

Close pin36

Close pin40

Close to Pin1

R2708 is need to connect.To prvent the beep sound

Layout Note: Place close to Pin 26

Layout Note: Place close to Pin 13

Layout Note:

75.05125.07D

2nd = 75.08212.07D

071.00255.0003

ALC255-CG-GP-U

Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

Mihawk MB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC255

Size: A2 | Document Number: Mihawk MB | Rev: -2

Date: Monday, August 10, 2015 | Sheet 27 of 105

Mihawk MB

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio AMP_1001

Size	Document Number	Rev
A4	**Mihawk MB**	-2

Date: Monday, August 10, 2015 Sheet 28 of 105

SSID = AUDIO

Speaker

AUD_SPK1_L-_CON <<< AUD_SPK1_L-_CON 89
AUD_SPK1_L+_CON <<< AUD_SPK1_L+_CON 89
AUD_SPK1_R-_CON <<< AUD_SPK1_R-_CON 89
AUD_SPK1_R+_CON <<< AUD_SPK1_R+_CON 89

AFTP TESTPOINT

20150602 PD

27 AUD_SPK_R+ — R2914 1 2 0R0603-PAD
27 AUD_SPK_R- — R2915 1 2 0R0603-PAD
27 AUD_SPK_L- — R2916 1 2 0R0603-PAD
27 AUD_SPK_L+ — R2917 1 2 0R0603-PAD

AUD_SPK1_R+_CON
AUD_SPK1_R-_CON
AUD_SPK1_L-_CON
AUD_SPK1_L+_CON

EC2901 1 2 SC22P50V2JN-L-GP DY
EC2902 1 2 SC22P50V2JN-L-GP DY
EC2915 1 2 SC22P50V2JN-L-GP DY
EC2920 1 2 SC22P50V2JN-L-GP DY

Layout Note:
Trace width=40mil

20150224

SPK1 6 4 3 2 1 5
ACES-CON4-17-GP-U1
20.F1621.004
2nd = 20.F1937.004

20150325

AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON

ED2901 AZ5125-02S-R7G-GP 75.05125.07D
2nd = 75.08212.07D
ED2902 AZ5125-02S-R7G-GP 75.05125.07D
2nd = 75.08212.07D

DMIC

20150427 SB

3D3V_S0
C2903 SCD1U16V2KX-L-GP
DMIC1
VDD CS CLK DATA GND GND
DMIC_CLK_CON_R
DMIC_DATA_CON_R
MICROPHONE-93-GP-U
082.40006.0001
2ND = 082.40002.0031
3rd = 082.40011.0011

20150427 SB

DMIC_CLK_CON_R
DMIC_DATA_CON_R

DY R2926 33R2J-L1-GP — DMIC_DATA0_CON 17
DY R2925 33R2J-L1-GP — DMIC_CLK0_CON 17
R2909 0R2J-L-GP — DMIC_CLK_CON 27
R2911 0R2J-L-GP — DMIC_DATA_CON 27

EC2903 EC2904 SC22P50V2JN-L-GP

Mihawk MB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC
Size: A3
Document Number: Mihawk MB
Rev: -2
Date: Monday, August 10, 2015
Sheet 29 of 105

Mihawk MB

緯創資通

Wistron Corporation
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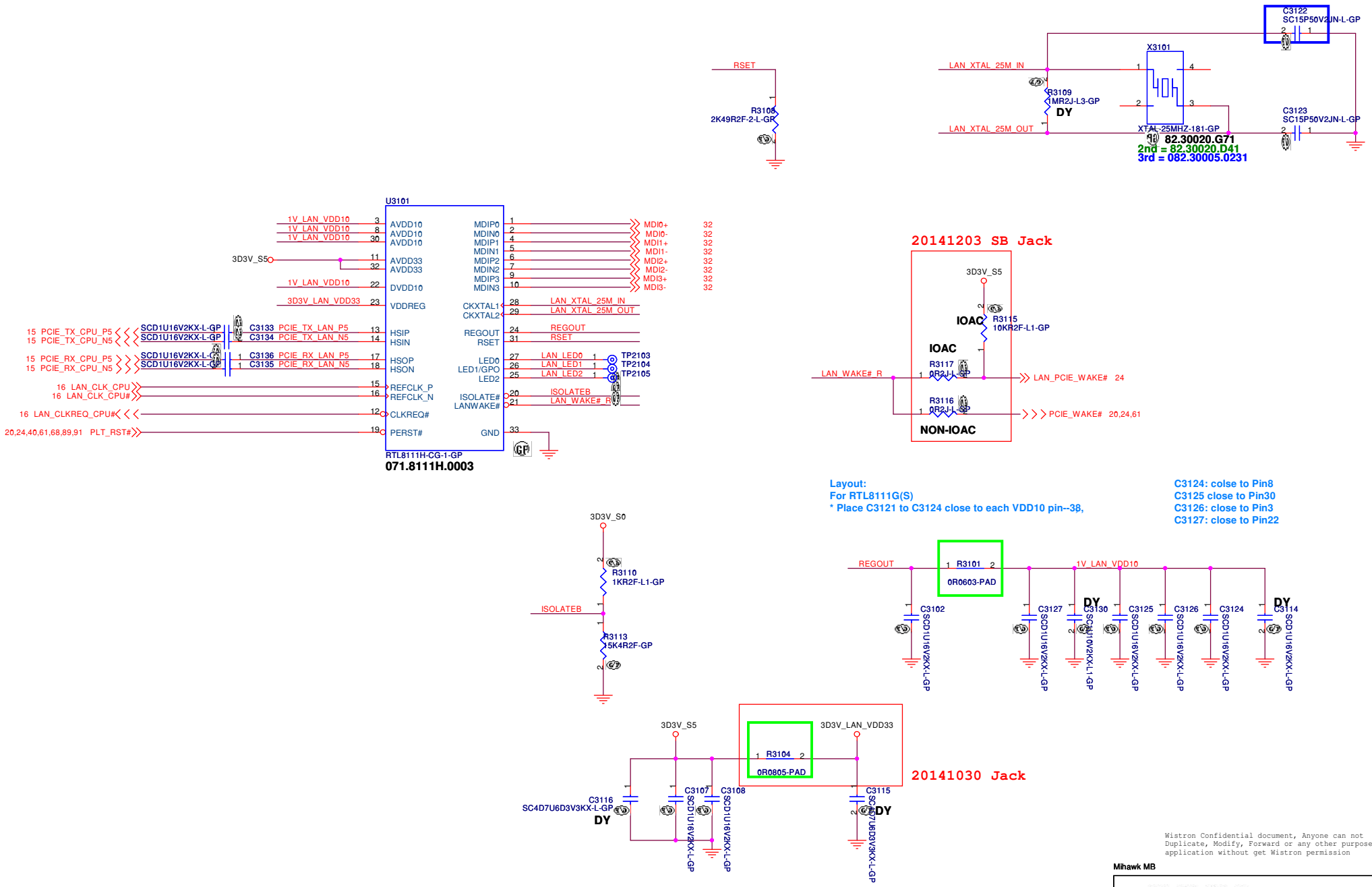
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A	**Mihawk MB**	-2

Date: Monday, August 10, 2015 Sheet 30 of 105



Mihawk MB

緯創資通 **Wistron Corporation**
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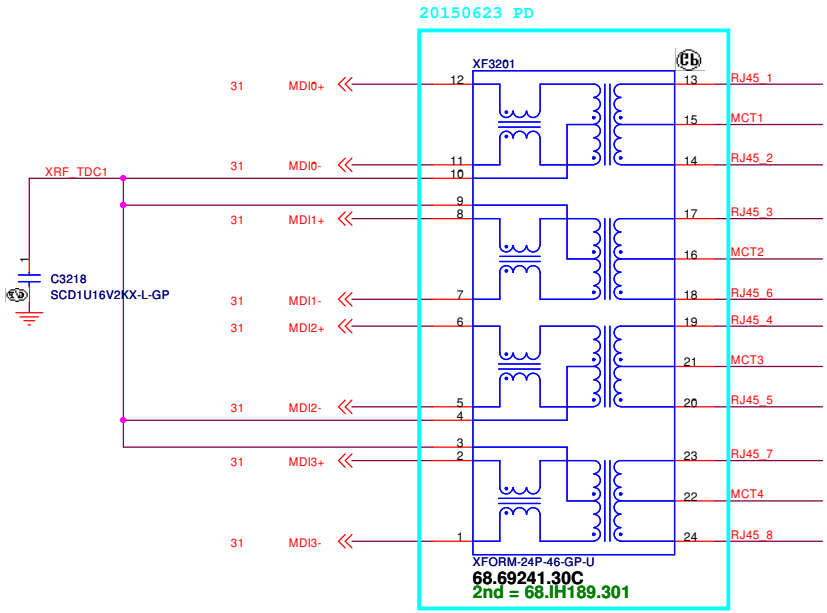
Taipei Hsien 221, Taiwan, R.O.C.

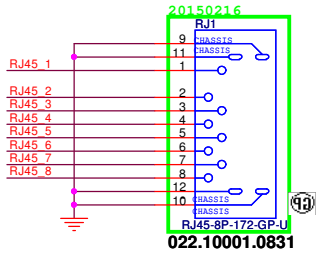
Title: **LAN(RTL8111H)**

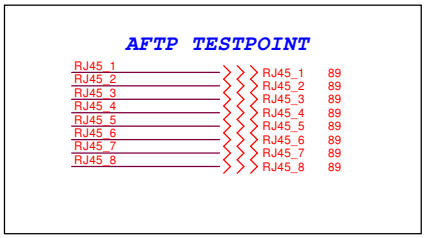
Size	Document Number	Rev
A3	Mihawk MB	-2

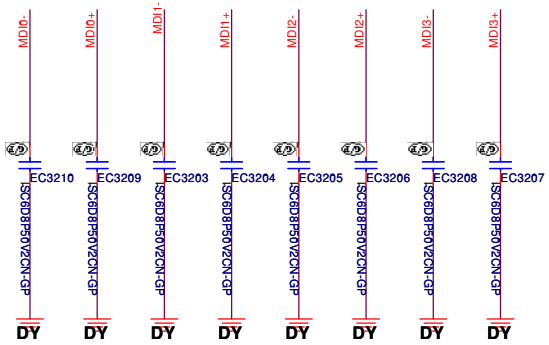
Date: Monday, August 10, 2015 Sheet 31 of 105

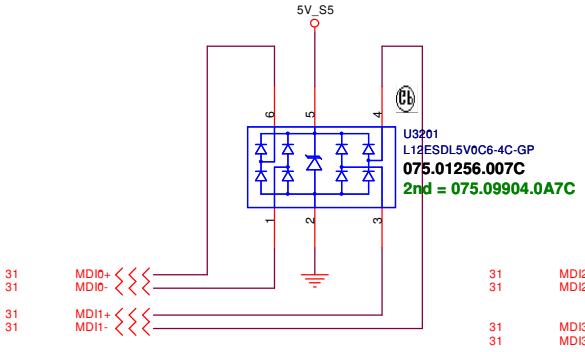
SSID = LAN

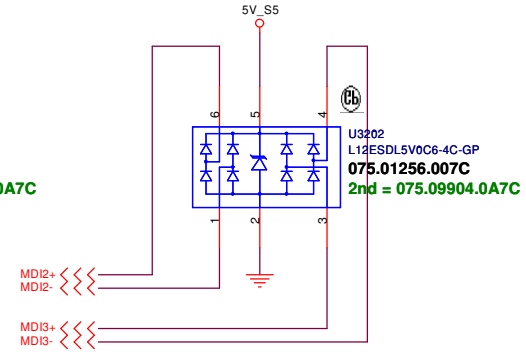


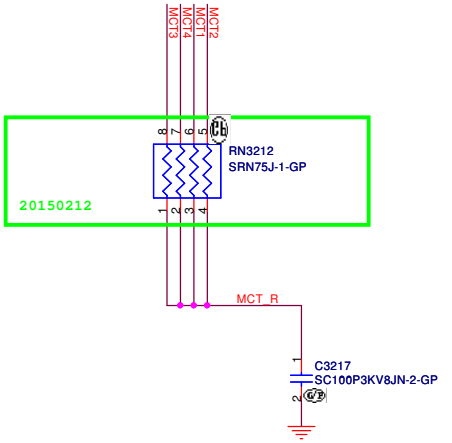












Mihawk MB

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(LAN+VGA) CONNECTOR***

Size	Document Number	Rev
A3	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 32 of 105

Mihawk MB

緯創資通 **Wistron Corporation**
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Title: **Card Reader IC+Reader Conn**

Size	Document Number	Rev
	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 33 of 105

Mihawk MB

緯創資通

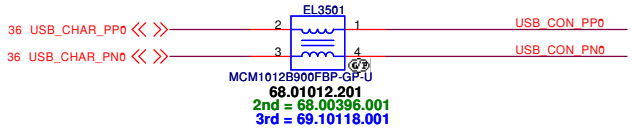
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

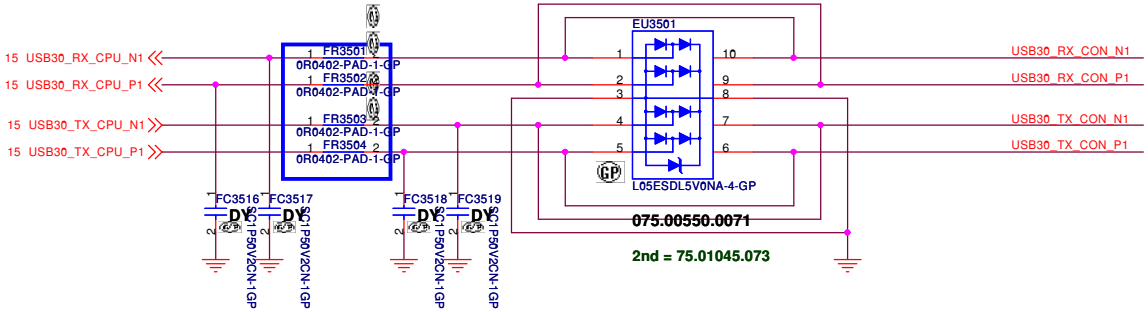
Title: ***USB2.0 CONN***

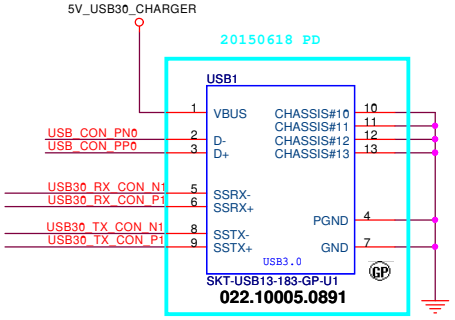
Size	Document Number	Rev
A3	**Mihawk MB**	-2

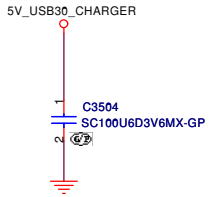
Date: Monday, August 10, 2015 Sheet 34 of 105

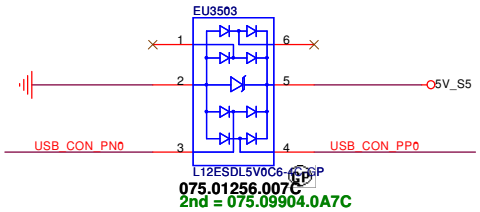
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	











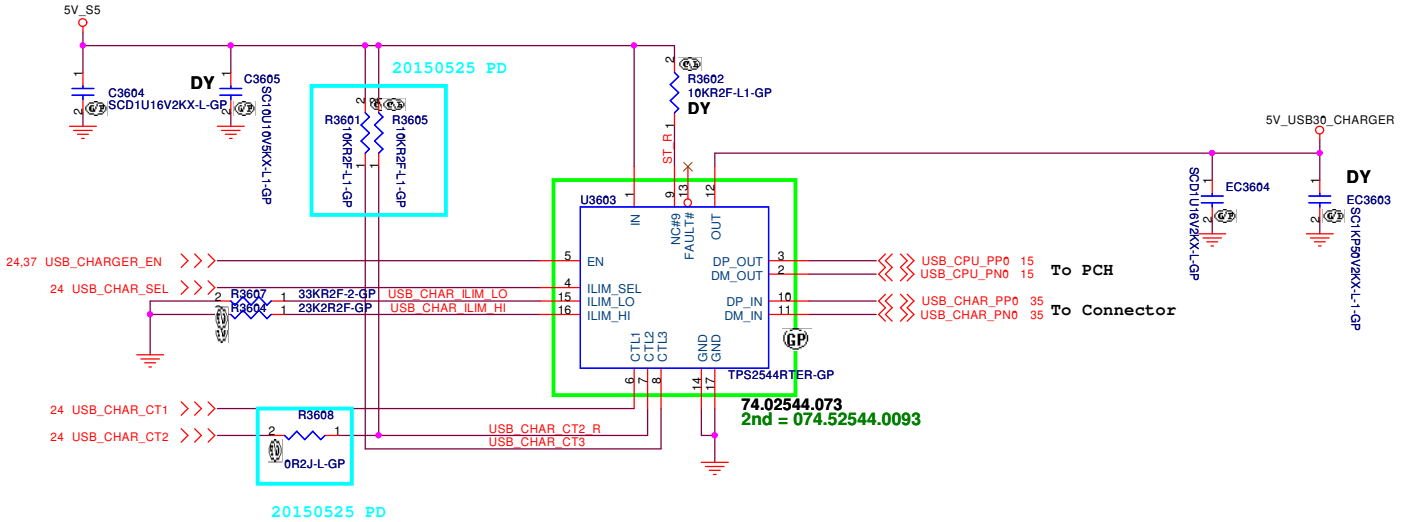
Mihawk MB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB3.0 CONN**

Size	Document Number	Rev
A3	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 35 of 105



	Device Control Pins			
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

3 Electrical Safety for USB3.0 Port

2.0 A <= Measurement value <= 2.2 A : Pass

1.9 A <= Measurement value < 2.0 A or 2.2 A < Measurement value <= 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A – 2.4 A).

Mihawk MB

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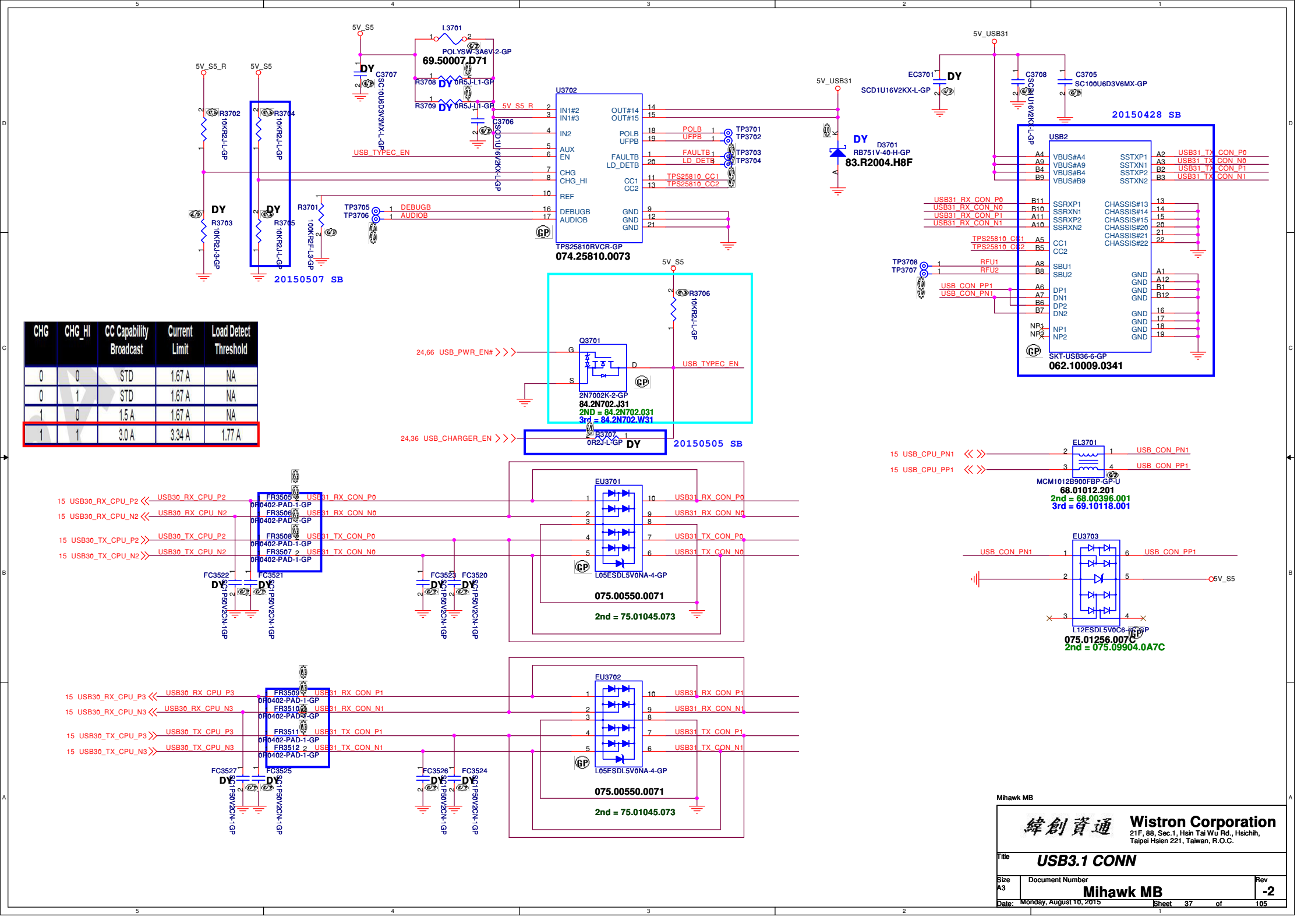
Title: USB CHARGER

Size: A3 | Document Number: Mihawk MB | Rev: -2

Date: Monday, August 10, 2015 | Sheet 36 of 105



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

Mihawk MB

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Title: **USB3.1 CONN**

Size	Document Number	Rev
A3	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 37 of 105

Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Redriver***

Size	Document Number	Rev
A3	**Mihawk MB**	**-2**

Date: Monday, August 10, 2015 Sheet 38 of 105

Mihawk MB

緯創資通
Wistron Corporation
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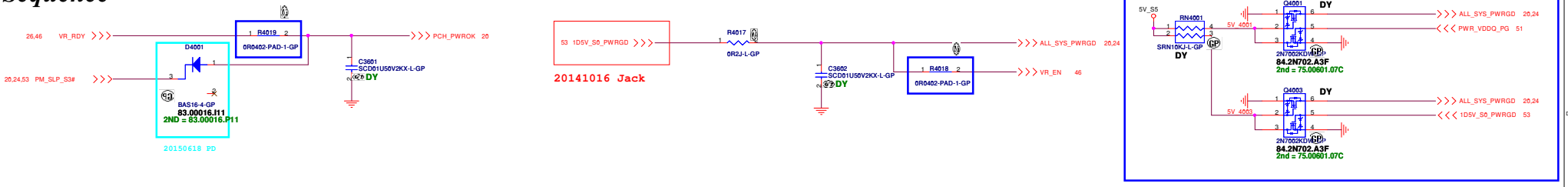
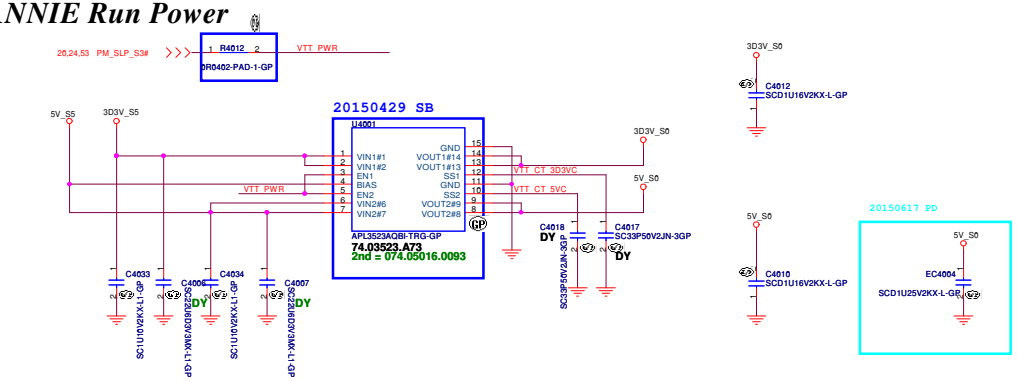
Title

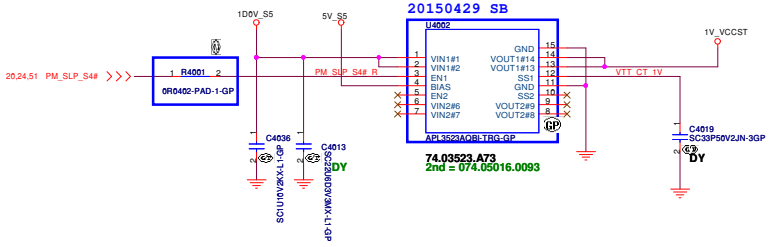
Size	Document Number	Rev
Custom	Mihawk MB	-2
Date: Monday, August 10, 2015	Sheet 39 of 105	

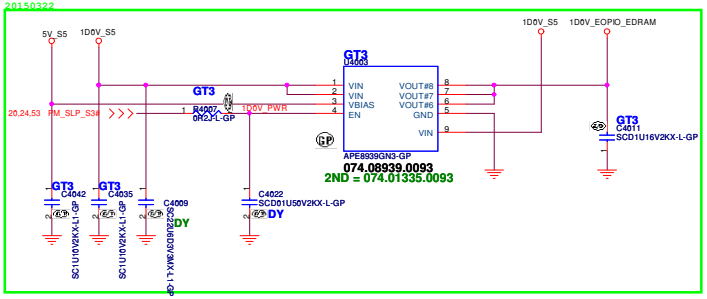
Power Sequence

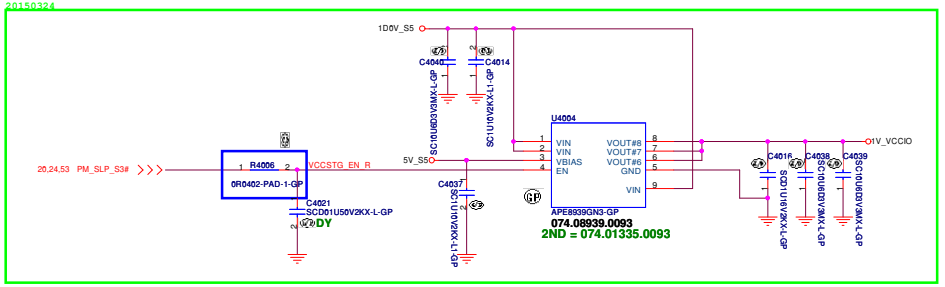


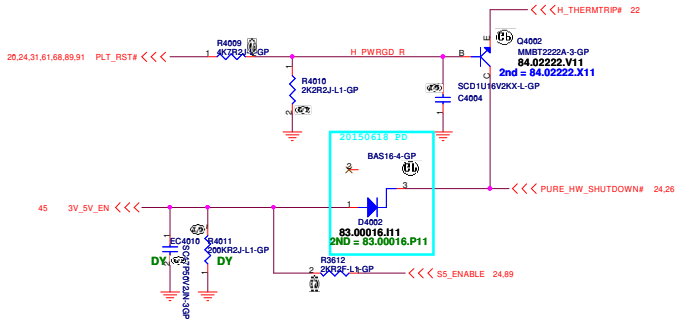
ANNIE Run Power











Mihawk MB

緯創資通 Wistron Corporation
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Title: Power Plane Enable & SEQUENCE

Size	Document Number	Rev
A2	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 40 of 105

Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DS3***	
Size A4	Document Number **Mihawk MB**	Rev **-2**
Date: Monday, August 10, 2015	Sheet 41 of 105	

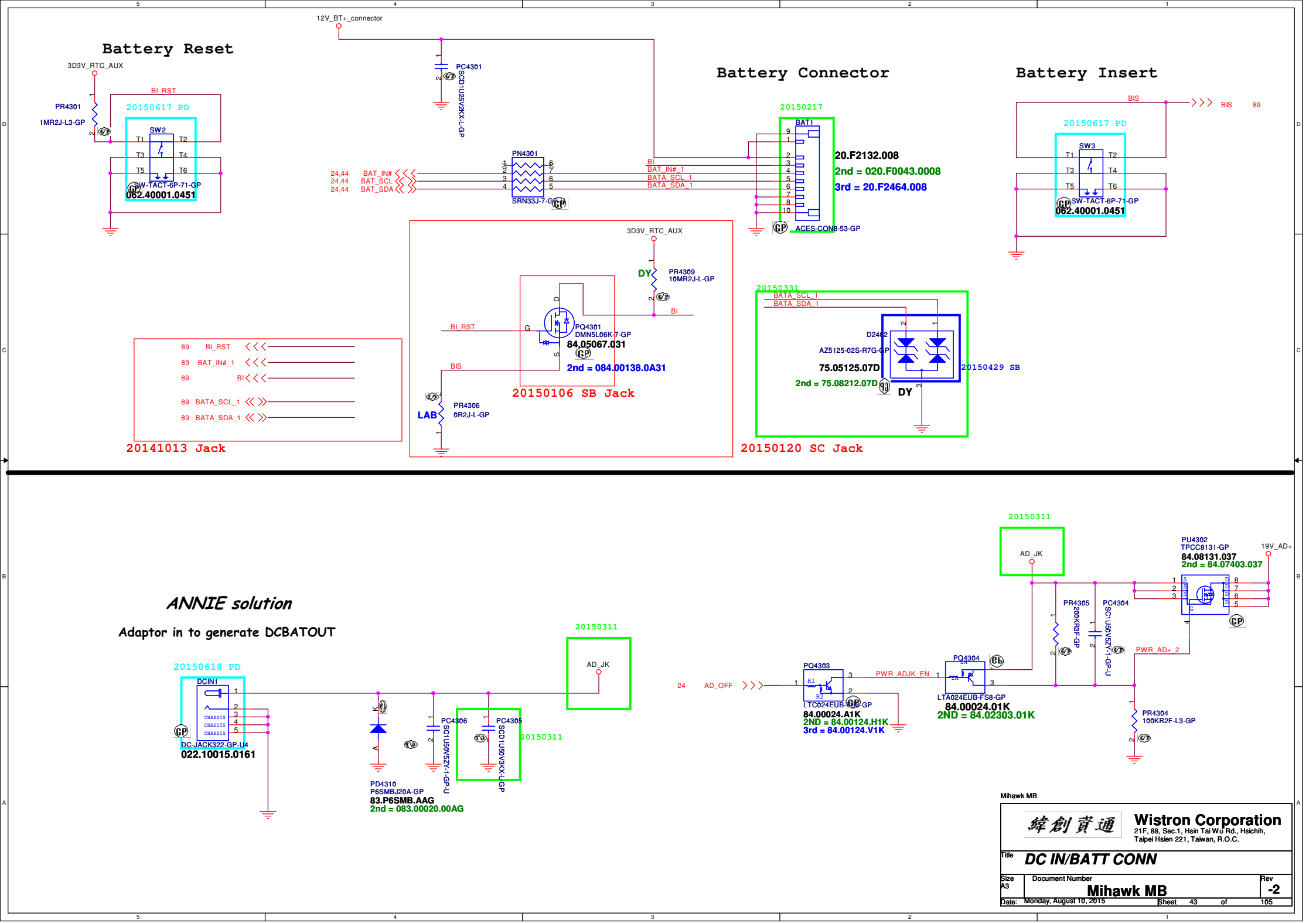
Mihawk MB

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***DCIN JACK***

Size	Document Number	Rev
A3	**Mihawk MB**	-2

Date: Monday, August 10, 2015 Sheet 42 of 105



Mihawk MB

緯創資通 **Wistron Corporation**
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Title	DC IN/BATT CONN	
Size A3	Document Number: Mihawk MB	Rev: -2
Date: Monday, August 10, 2015	Sheet 43 of 105	

SSID = Charger

The 45W adapter AC protect can change to 120% (2.8A)

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect preset (85% x 120%)	AC_protect Current	Sense resitor	Current to Voltage	PR4407	PR4401
45W	AC+Battery	High	2.37	102%	2.4174	20mOhm	0.09696	88.7	100
65W	AC+Battery	High	3.42	102%	3.4884	20mOhm	0.09696	164	100
90W	AC+Battery	High	4.74	102%	4.8348	10mOhm	0.09696	60.4	100
120W	AC+Battery	High	6.31	102%	6.4362	10mOhm	1.29724	113	100
135W	AC+Battery	High	7.1	102%	7.242	10mOhm	1.4484	130	100

	45W	65W
PR4404	20m(64.R0205.7FL)	10m(64.R0105.7FL)
PR4407	88.7K(64.88725.6DL)	16.2K(64.16225.6DL)
PR4401	100K(64.10035.L3L)	100K(64.10035.L3L)

adapter 45W and 65W
AC mode (default:120%):
set up the value by PR4401 and PR4407

20150612 PD

AC adapter detect current :
Ac input current = 20 x (Vacp - Vacn) / 10mohm

20150413 SB

Charger Current=1.4~3.6A

CYNTEC. 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A Isat : 10A

Battery I Sense

Layout Note:
1. Place PR4403, PG4409 and PG4411 near to BTY connector
2. Place PC4429, PC4430 and PC4431 near to PU4407

Battery OCP	R3	R4
6 Cell (3S2P)	7A	71.5K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP	R7	R8
6 Cell (3S2P)	14V	80.6K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

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Title: CHARGER BQ24780
Size: Custom | Document Number: Mihawk MB | Rev: -2
Date: Tuesday, August 18, 2015 | Sheet 44 of 105

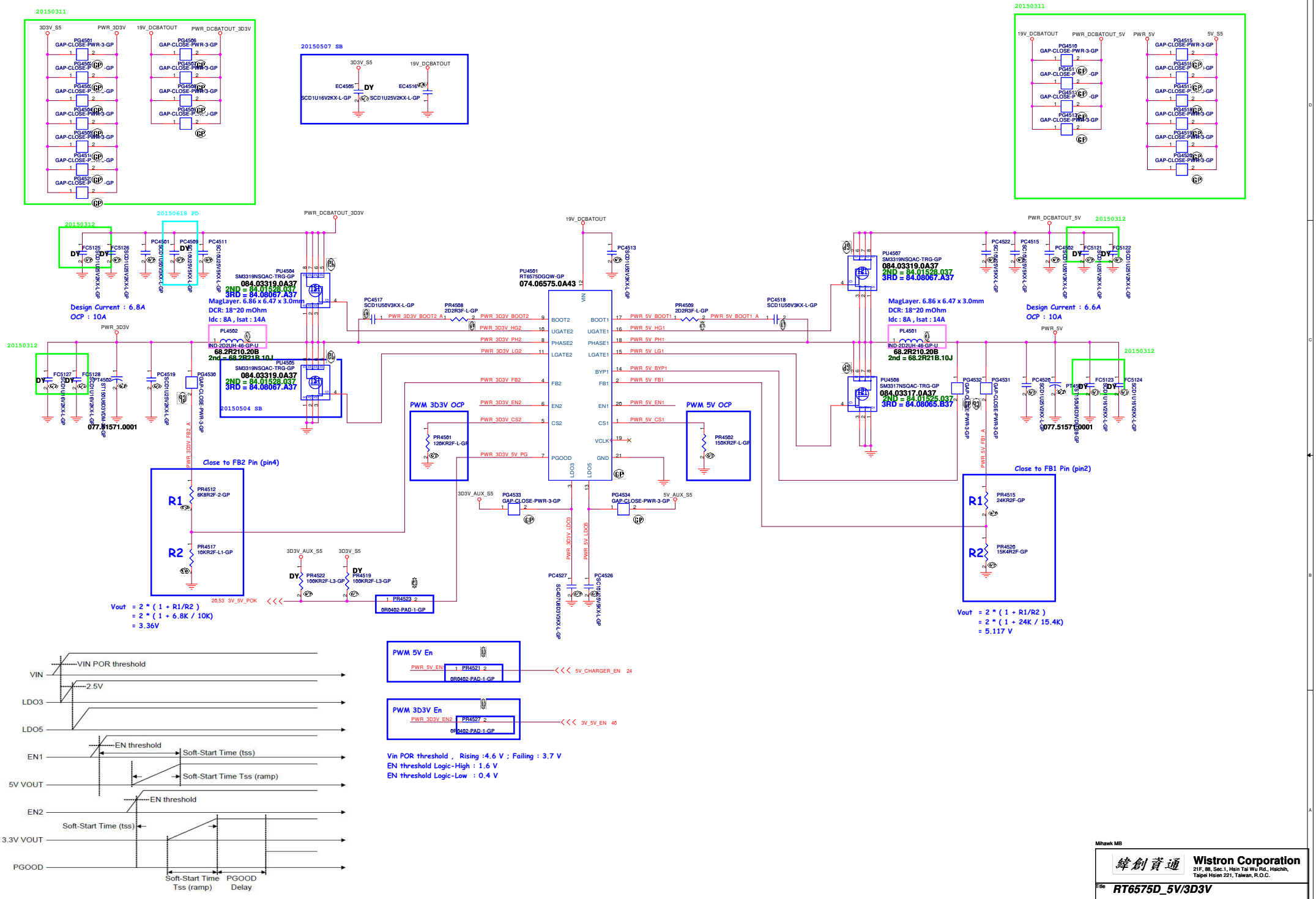

Figure 6. RT6575B Timing

Mihawk MB

Wistron Corporation
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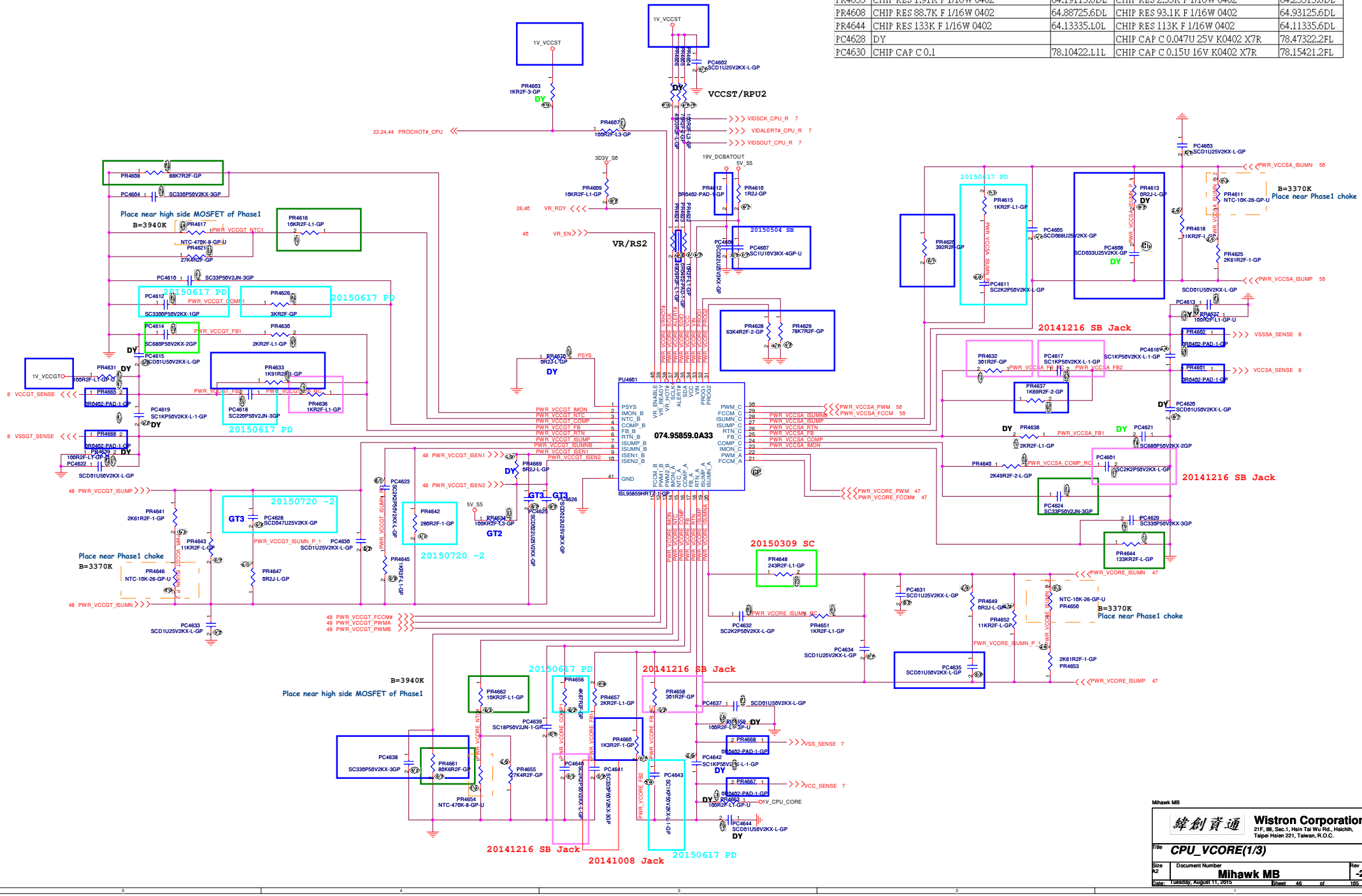
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT6575D_5V/3D3V	
Size A2	Document Number Mihawk MB	Rev -2
Date: Monday, August 10, 2015	Sheet 45 of 105	

Main Func = CPU_CORE

	U22		U23e	
PR4629	CHIP RES 78.7K F 1/16W 0402	64.78725.6DL	CHIP RES 88.7K F 1/16W 0402	64.88725.6DL
PR4634	CHIP RES 100K F 1/16W 0402 13" REEL	64.10035.L3L	DY	
PR4642	CHIP RES 280 F 1/16W 0402	64.28005.6DL	CHIP RES 357K F 1/16W 0402	64.35705.6DL
PR4633	CHIP RES 1.91K F 1/16W 0402	64.19115.6DL	CHIP RES 2.55K F 1/16W 0402	64.25515.6DL
PR4608	CHIP RES 88.7K F 1/16W 0402	64.88725.6DL	CHIP RES 93.1K F 1/16W 0402	64.93125.6DL
PR4644	CHIP RES 133K F 1/16W 0402	64.13335.L0L	CHIP RES 113K F 1/16W 0402	64.11335.6DL
PC4628	DY		CHIP CAP C 0.047U 25V K0402 X7R	78.47322.2FL
PC4630	CHIP CAP C 0.1	78.10422.L1L	CHIP CAP C 0.15U 16V K0402 X7R	78.15421.2FL



Mihawk MB

Wistron Corporation
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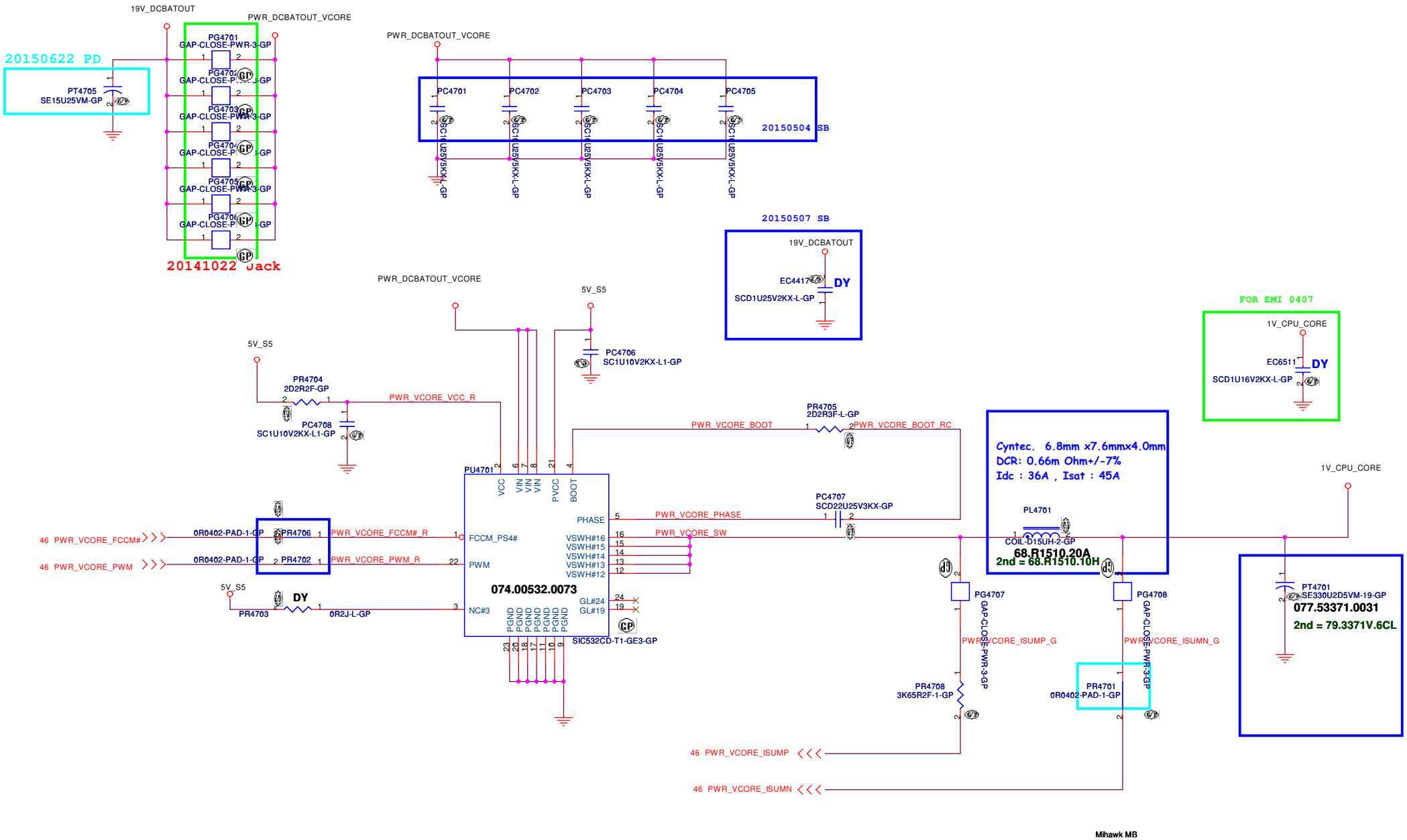
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCORE(1/3)

Size: A2 | Document Number: Mihawk MB | Rev: -2

Date: Tuesday, August 11, 2015 | Sheet 46 of 105

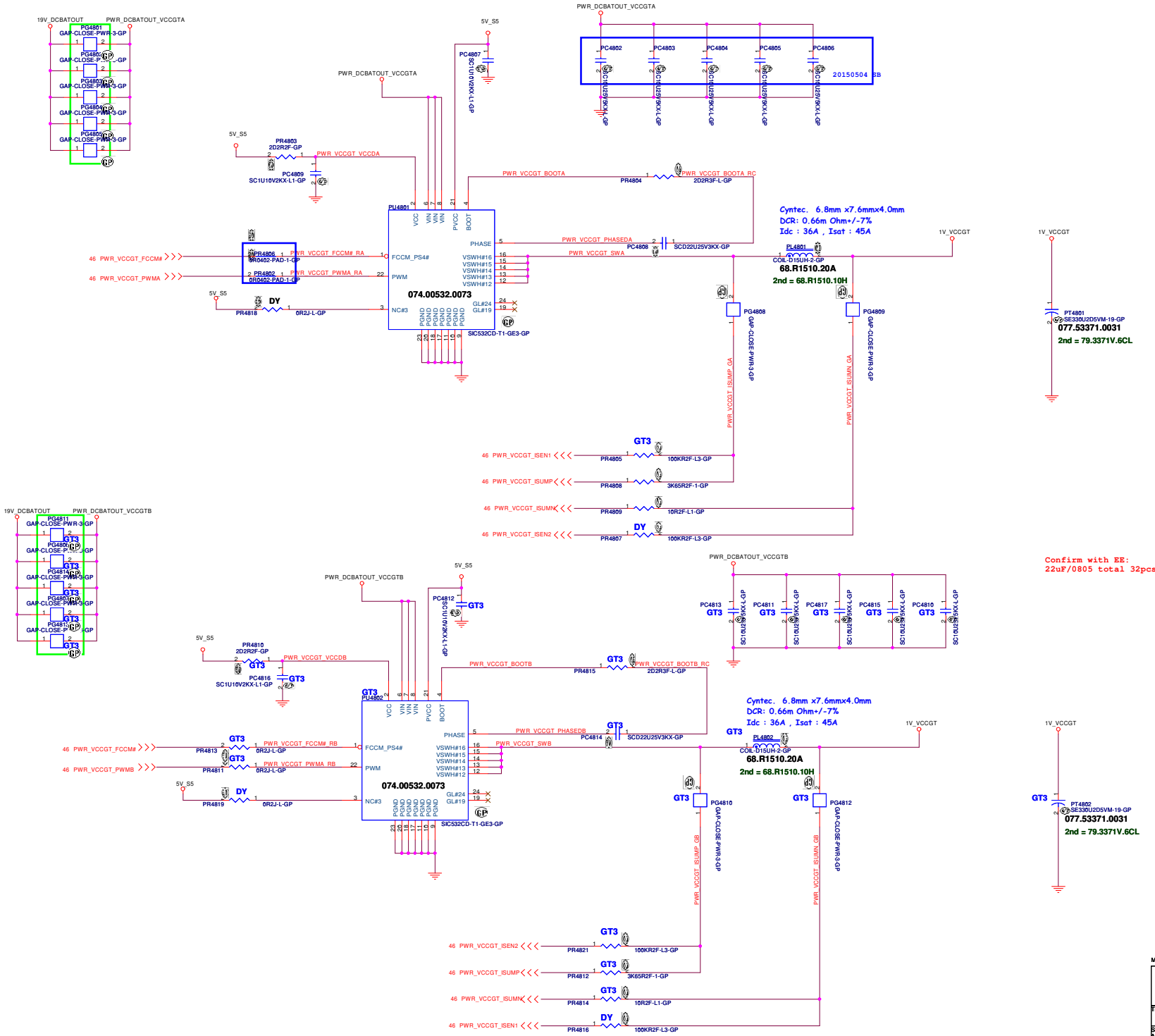
Main Func = CPU_CORE



Mihawk MB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_VCORE(2/3)		
Size: A3	Document Number: Mihawk MB	Rev: -2
Date: Monday, August 10, 2015	Sheet 47 of 105	

Main Func = CPU_CORE



Mihawk MB

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_VCCGT(3/3)*

Size	Document Number	Rev
A2	Mihawk MB	-2

Date: Monday, August 10, 2015 Sheet 48 of 105

Mihawk MB

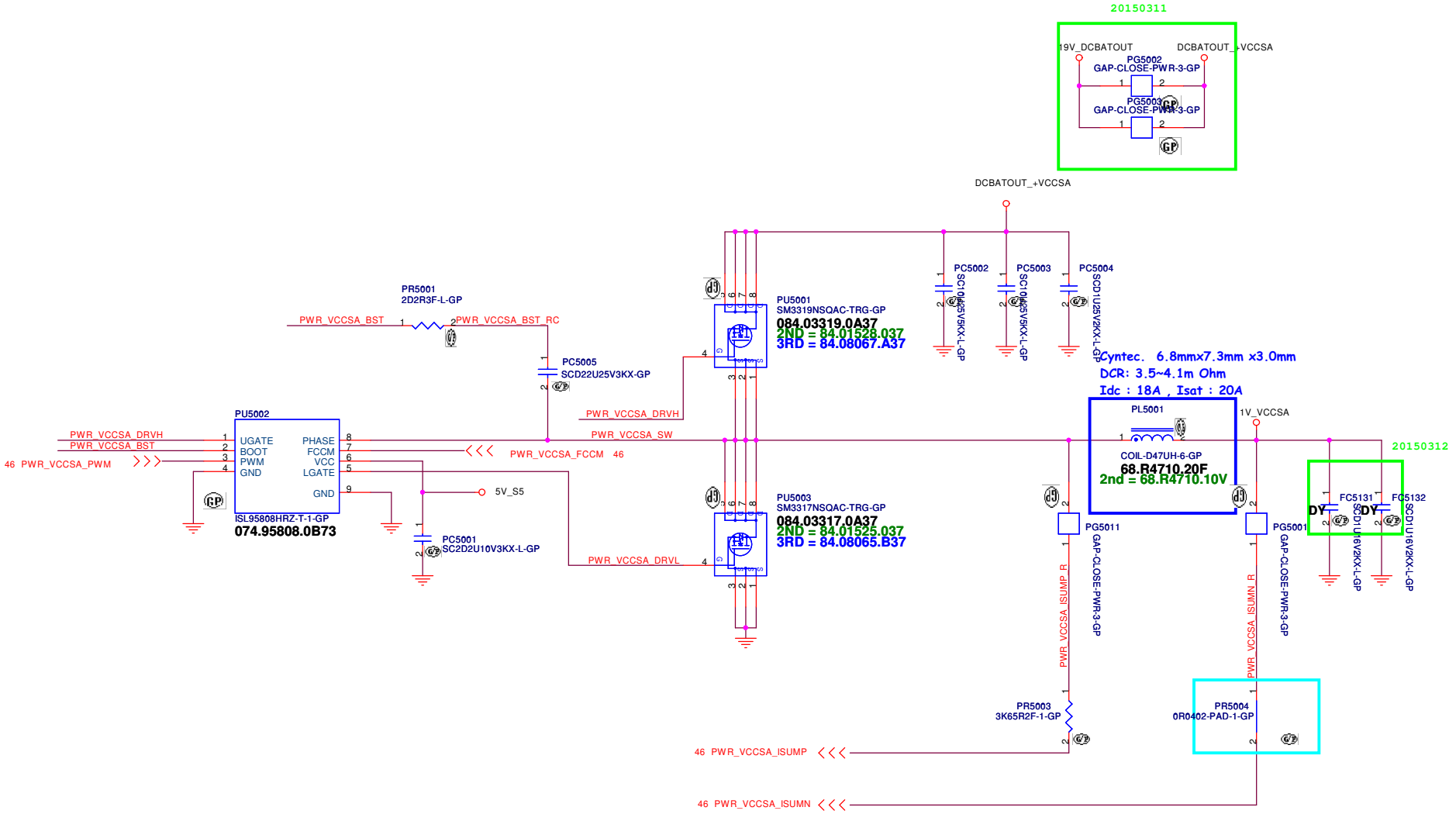
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VCCGTUS***

Size	Document Number	Rev
A2	**Mihawk MB**	-2

Date: Monday, August 10, 2015 Sheet 49 of 105

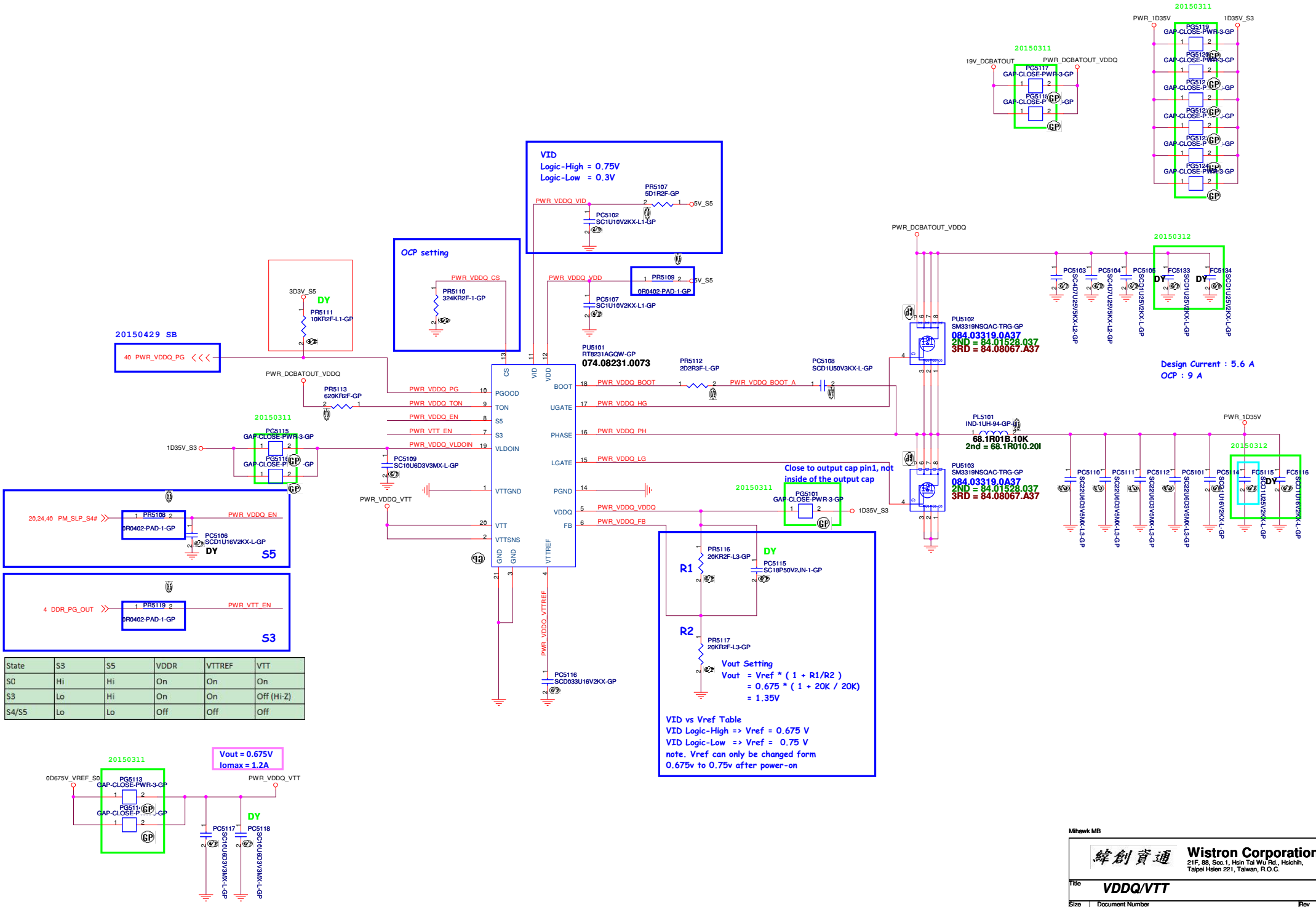
Main Func = CPU_CORE



Mihawk MB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA	
Size A3	Document Number Mihawk MB	Rev -2
Date: Tuesday, August 18, 2015	Sheet 50 of 105	



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Mihawk MB

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VDDQ/VTT

Size: Custom | Document Number: Mihawk MB | Rev: -2

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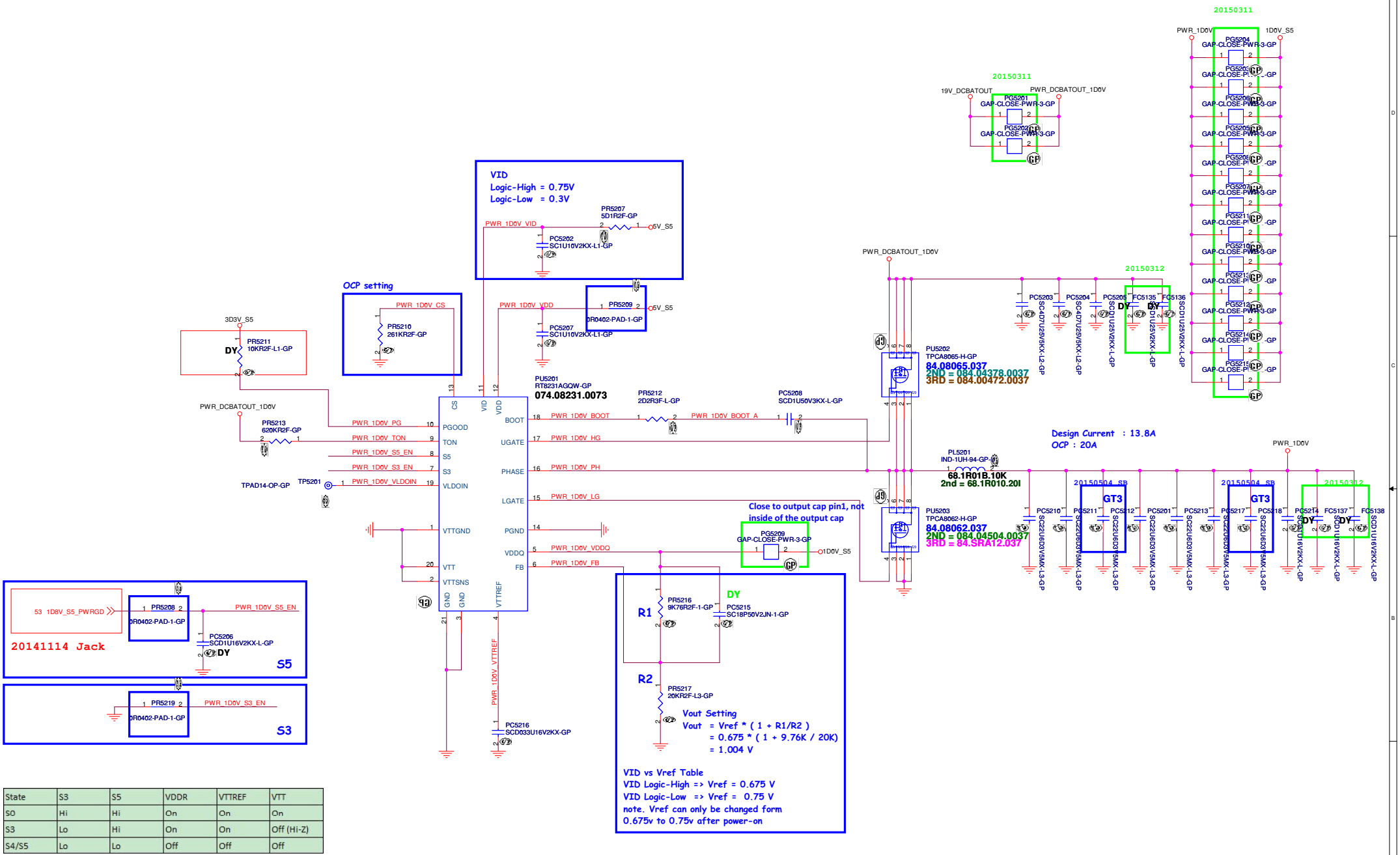

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Mihawk MB

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231_1D0V

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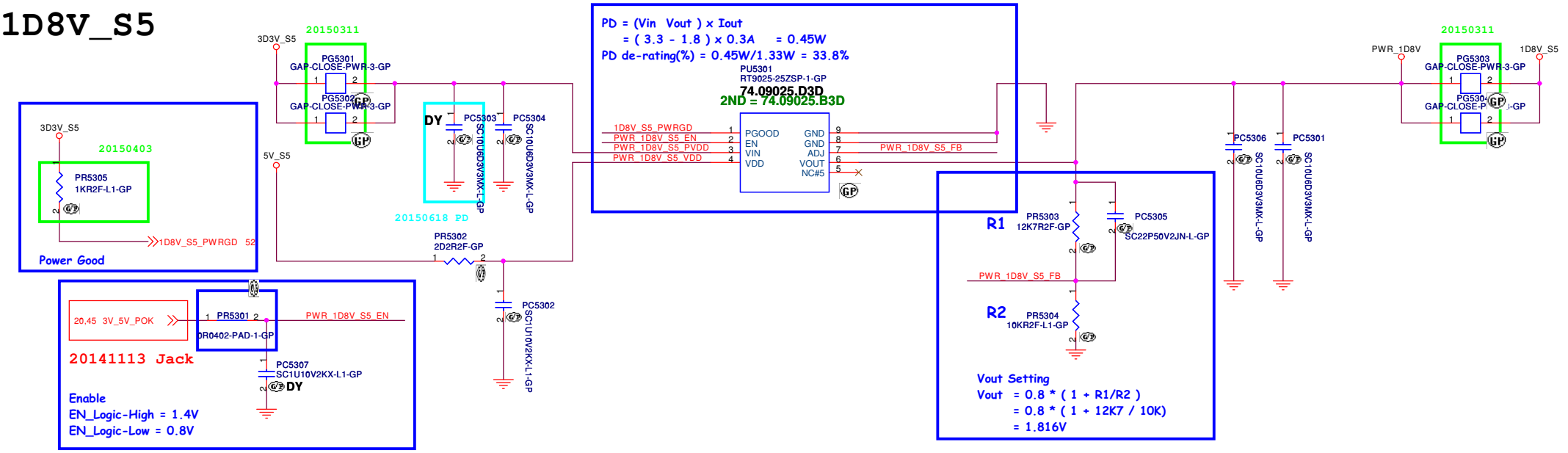
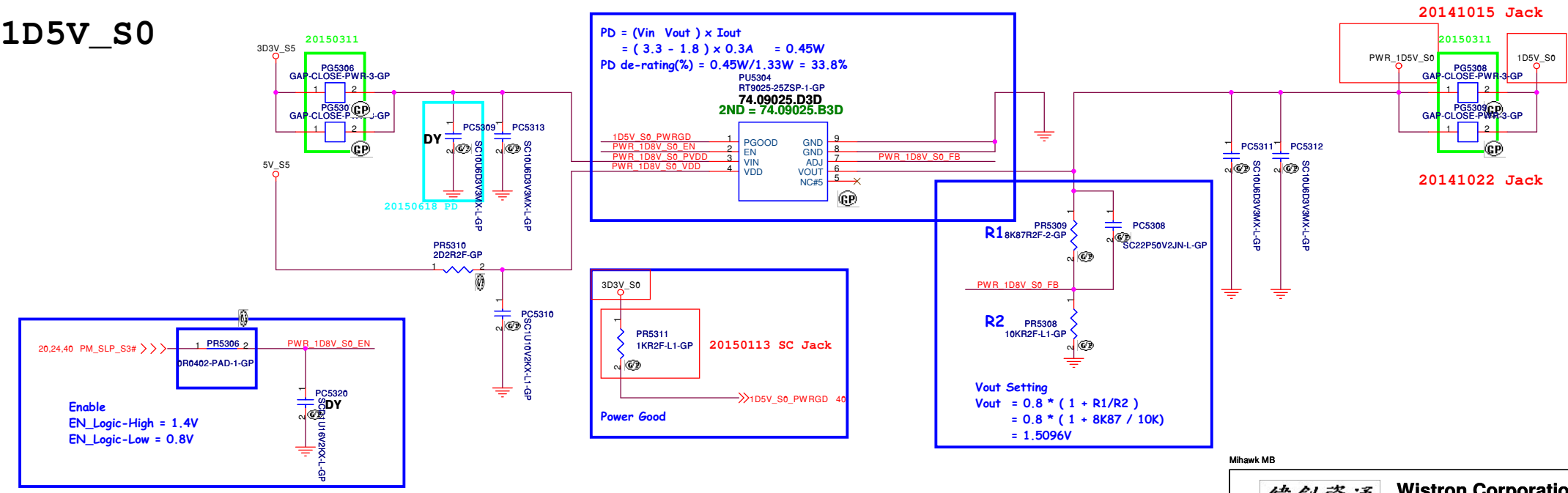
1D8V_S5



1D5V_S0



Mihawk MB

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	*RT8068_1D8V*	
Size A3	Document Number **Mihawk MB**	Rev -2
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緯創資通

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Title: ***Reserved***

Size	Document Number	Rev
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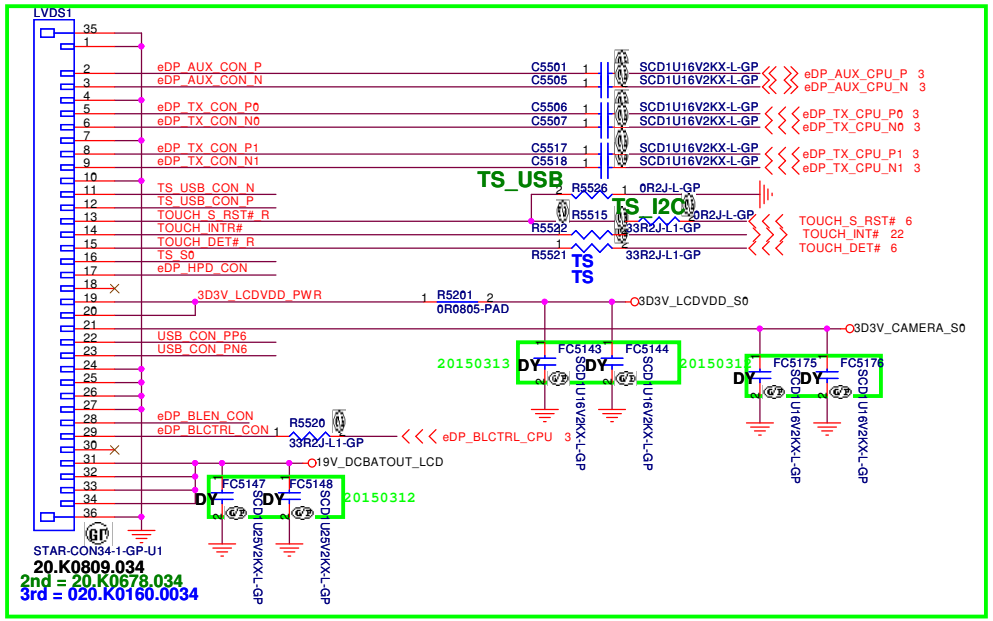
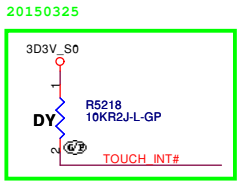
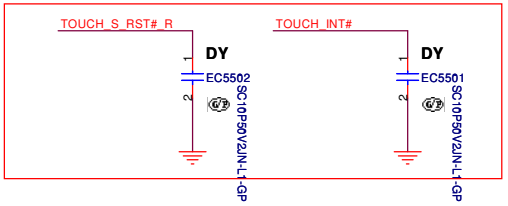
Main Func = LCD

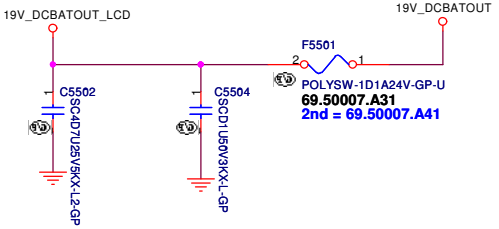


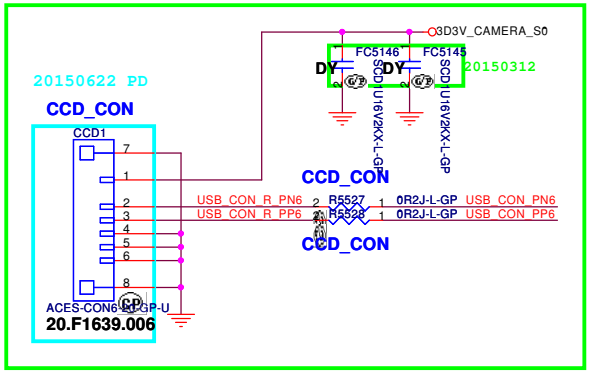


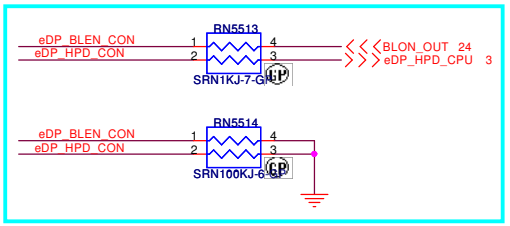


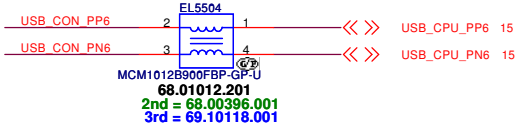
20141016 Jack

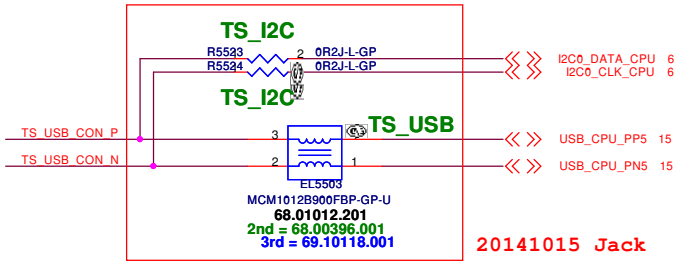
Inverter Power



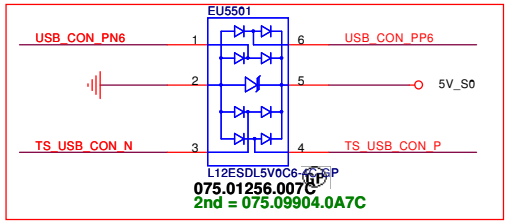




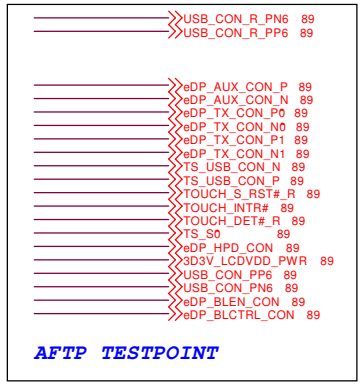




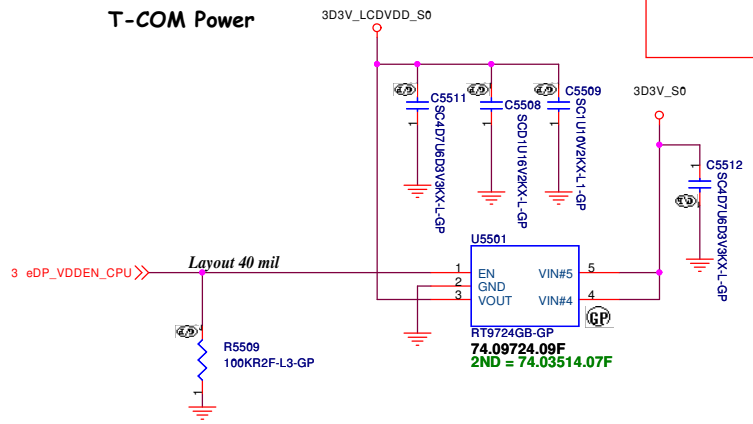
20141015 Jack



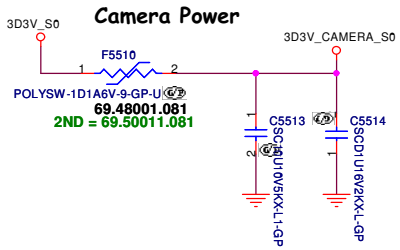
20141016 Jack



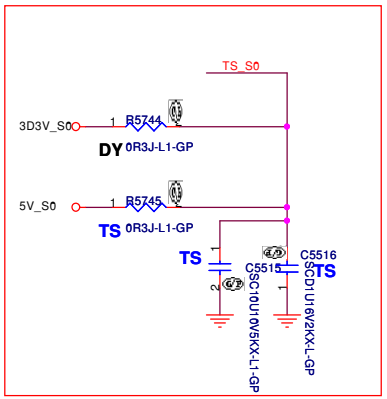
T-COM Power



Camera Power



Touch panel Power



20141015 Jack

Mihawk MB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN	
Size A3	Document Number Mihawk MB	Rev -2
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Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VGA RTD2168***	
Size: A3	Document Number: **Mihawk MB**	Rev: **-2**
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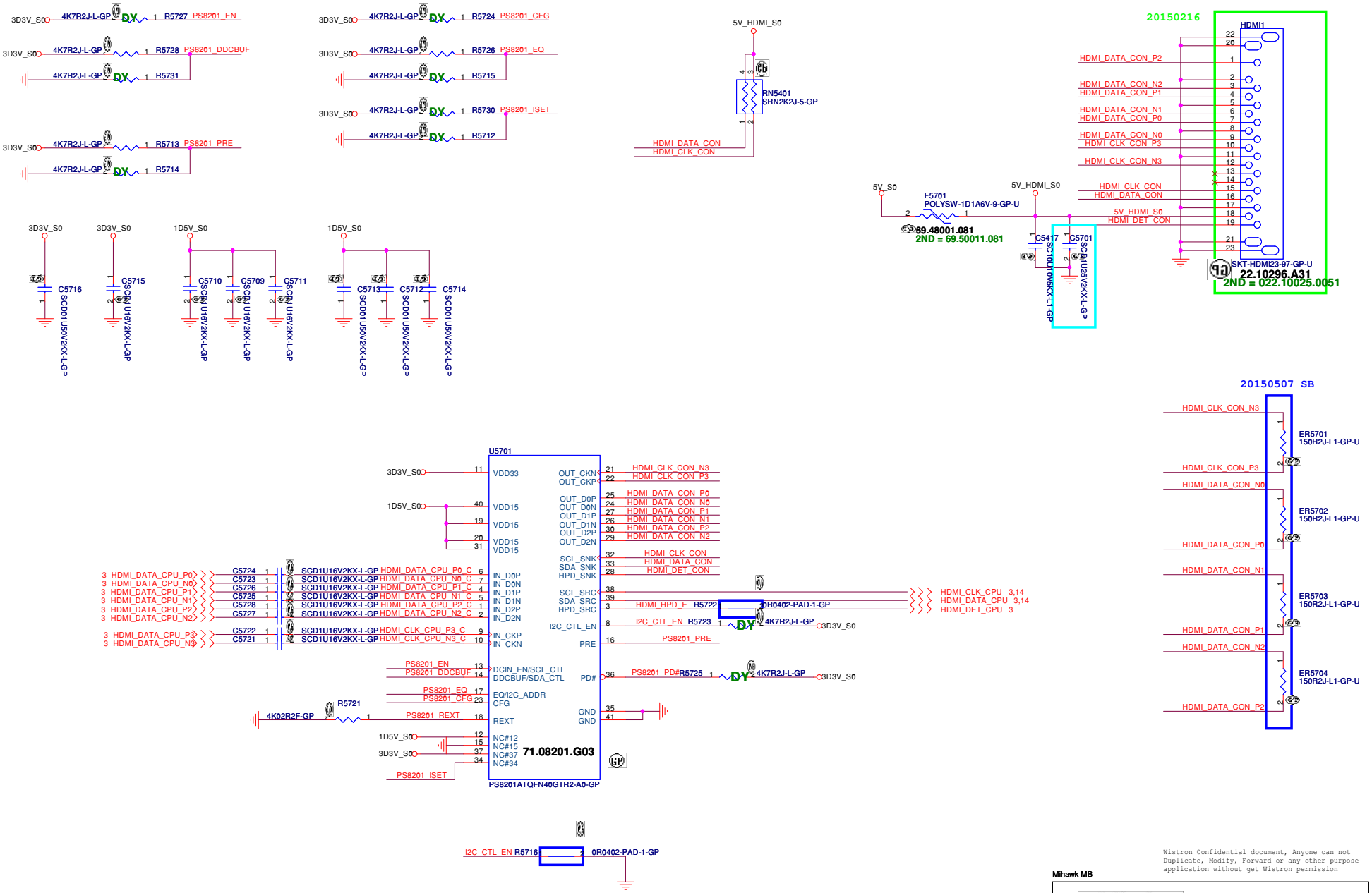
SSID = VIDEO

HDMI Level Shifter & CONNECTOR



Mihawk MB

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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Conn

Size	Document Number	Rev
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Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

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Title

DVI

Size	Document Number	Rev
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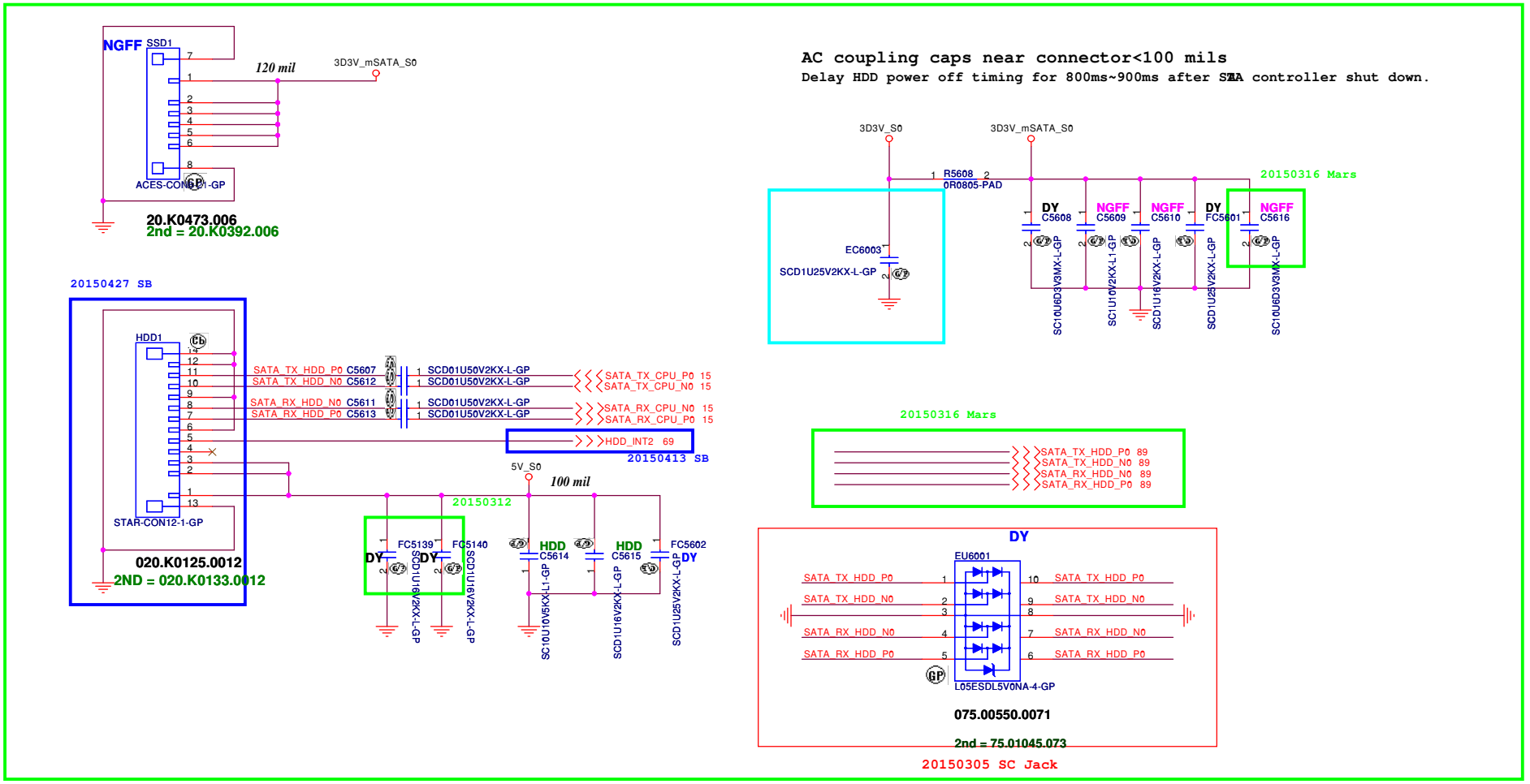
SATA HDD / SSD Connector

20150216



Mihawk MB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD / NGFF SSD***	
Size A3	Document Number **Mihawk MB**	Rev **-2**
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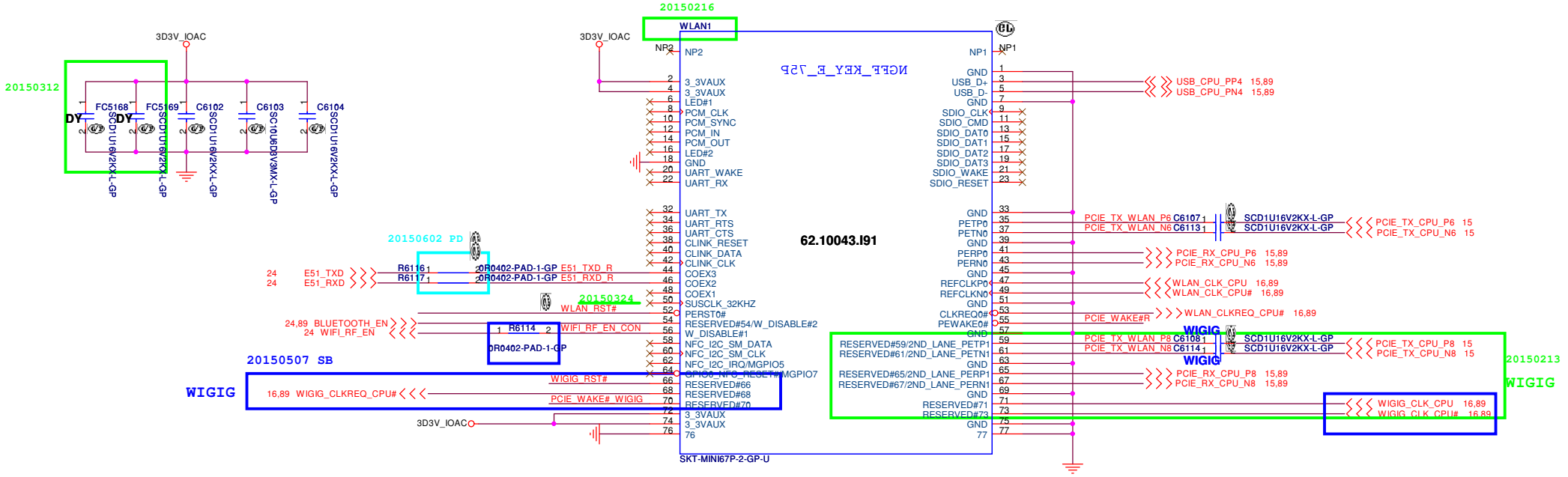
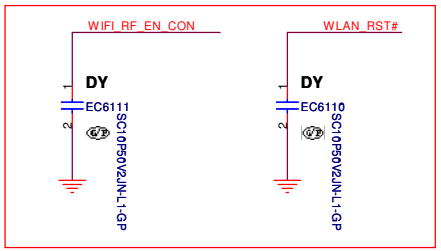
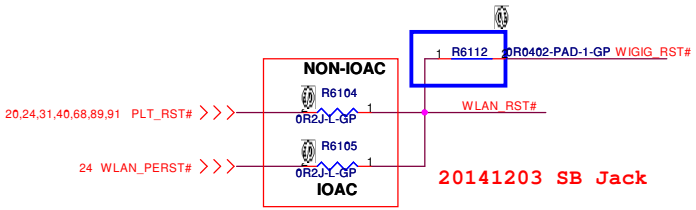
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

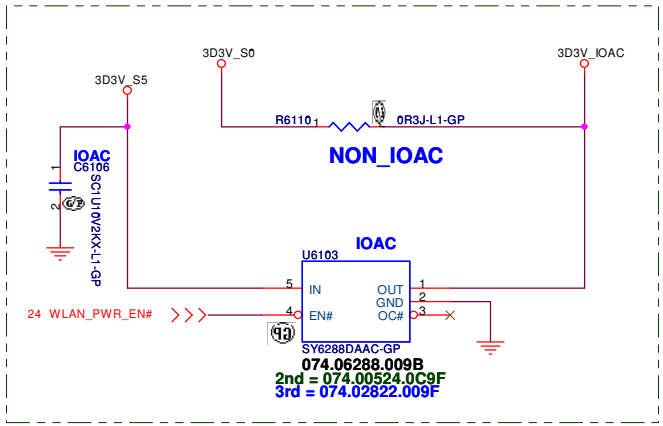


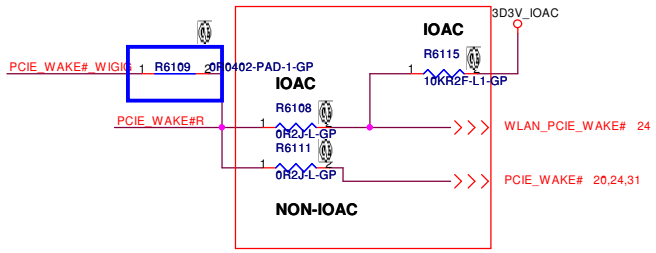


20141016 Jack



20141203 SB Jack





20141203 SB Jack

20150310

15,89 USB_CPU_PP4
15,89 USB_CPU_PN4
89 PCIE_TX_WLAN_P6
89 PCIE_TX_WLAN_N6
89 PCIE_WAKE#R
89 PCIE_TX_WLAN_P8
89 PCIE_TX_WLAN_N8
89 E51_TXD_R
89 E51_RXD_R
89 WLAN_RST#
24,89 BLUETOOTH_EN
89 WIFI_RF_EN_CON
89 PCIE_WAKE#_WIGIG
16,89 WIGIG_CLKREQ_CPU#
89 WIGIG_RST#

AFTP TEST POINT

Mihawk MB

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Mini Card-WLAN	
Size A3	Document Number Mihawk MB	Rev -2
Date: Monday, August 10, 2015	Sheet 61 of 105	

Mihawk MB

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Wireless Charging

Size	Document Number	Rev
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SSID = mSATA

Mihawk MB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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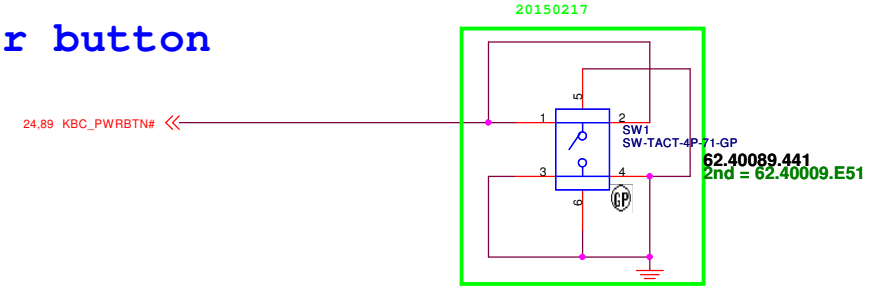
Title: *mSTAT*		
Size: A3	Document Number: **Mihawk MB**	Rev: -2
Date: Monday, August 10, 2015	Sheet 63 of 105	

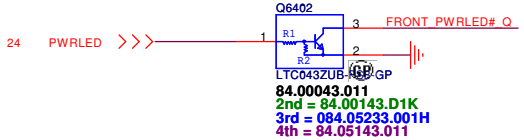
Main Func = Power BTN

Power button

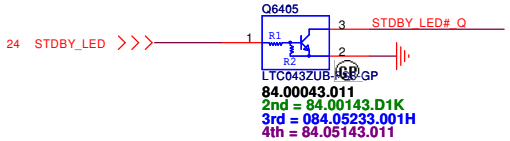


Main Func = Battery LED

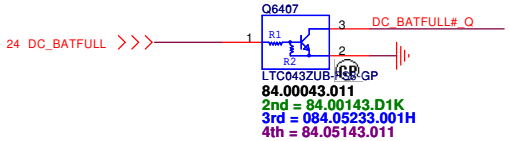
Power Button_LED



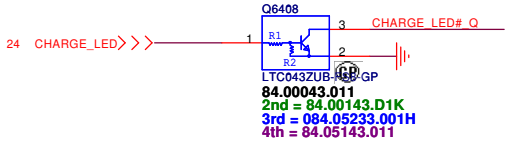
Power STDBY_LED

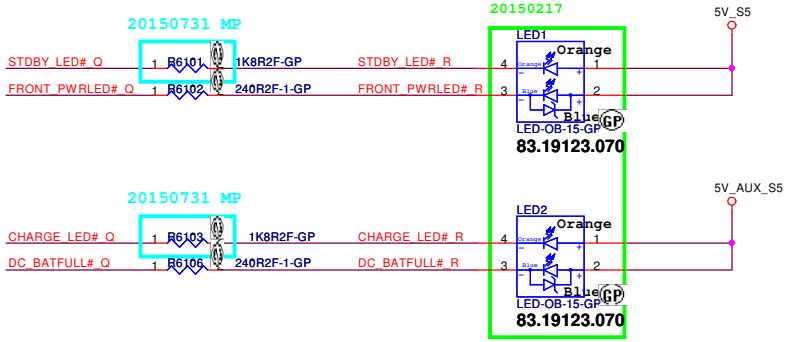


Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)





Mihawk MB

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Title: LED Bard/Power Button

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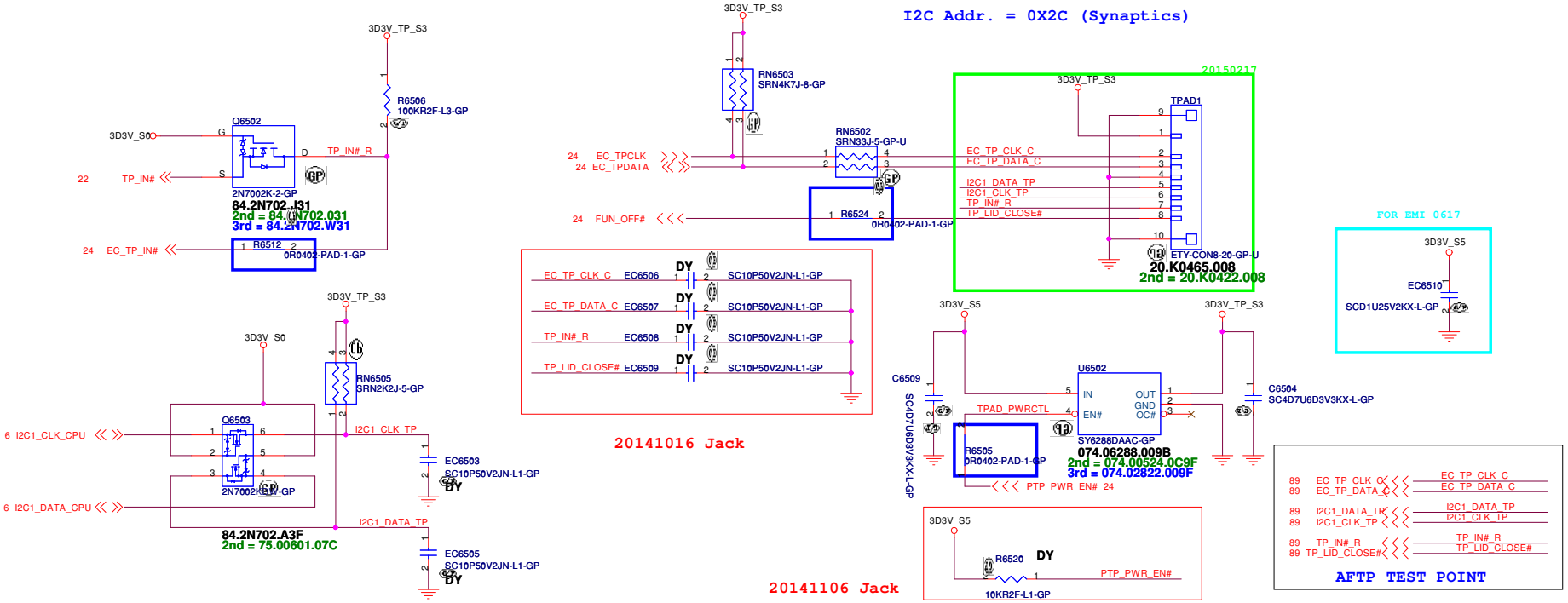
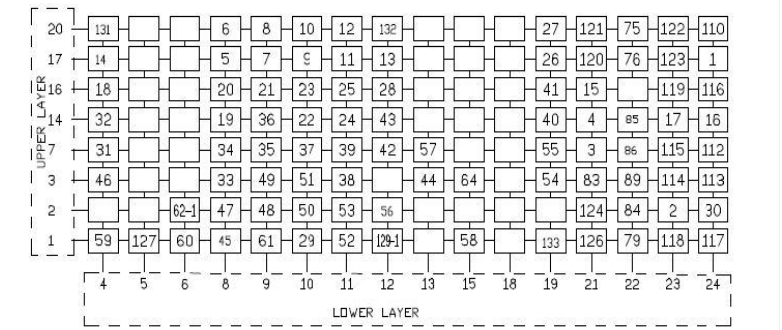
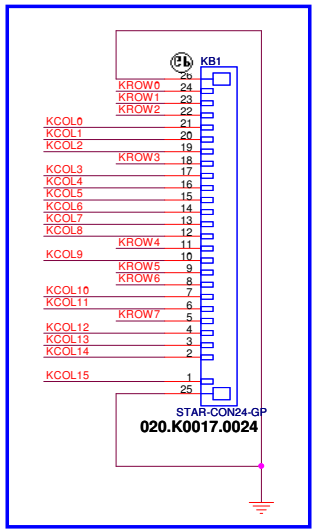
Precision Touch Pad

I2C Addr. = 0X2C (Synaptics)

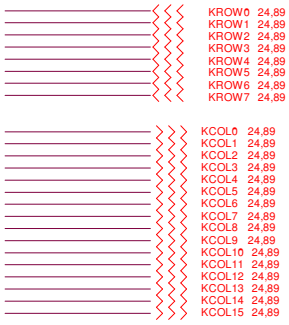


Internal KeyBoard Connector





20150429 SB



Mihawk MB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size	Document Number	Rev
Custom	Mihawk MB	-2

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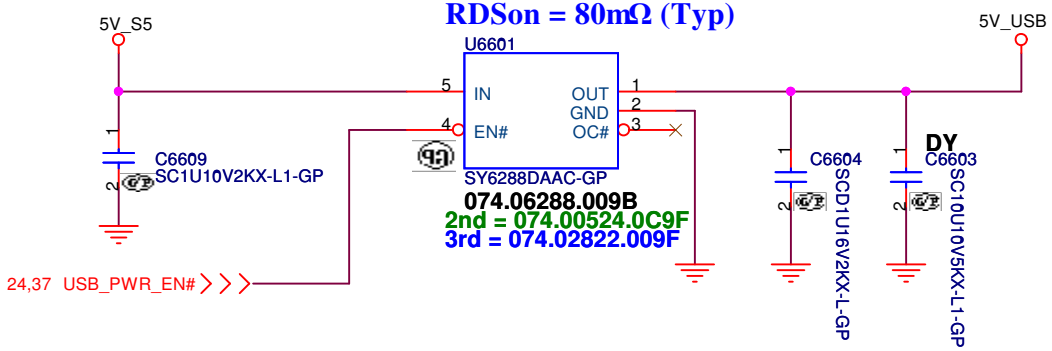
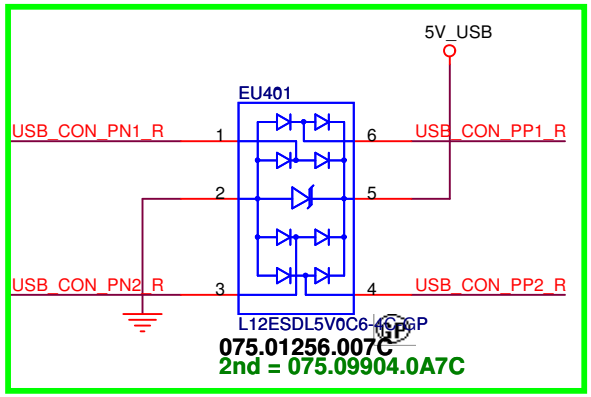
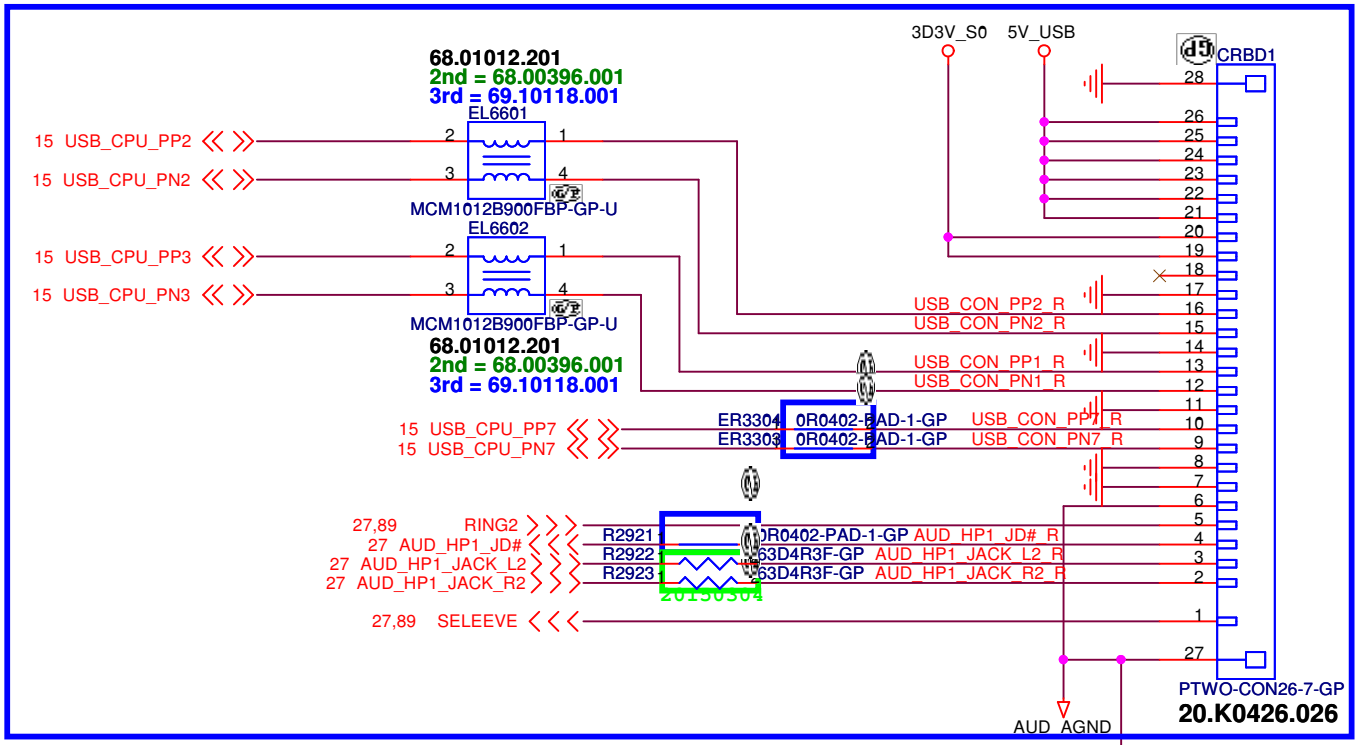
Low Active 2A
RDSon = 80mΩ (Typ)



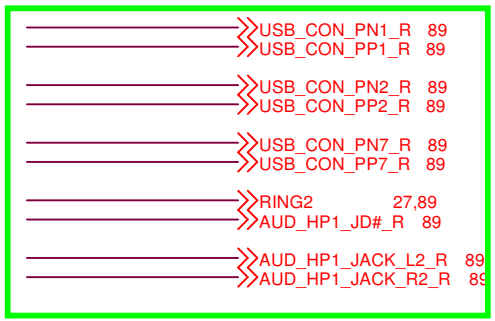
20150331



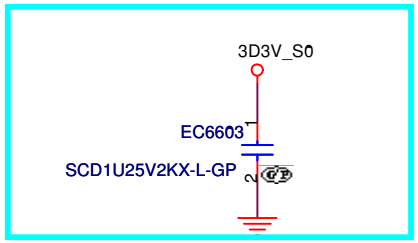
20150511 SB

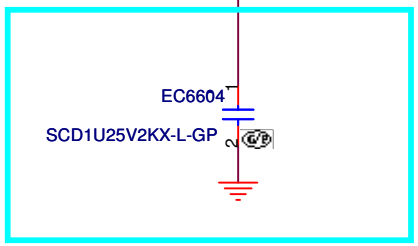


20150310



AFTP TESTPOINT





Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
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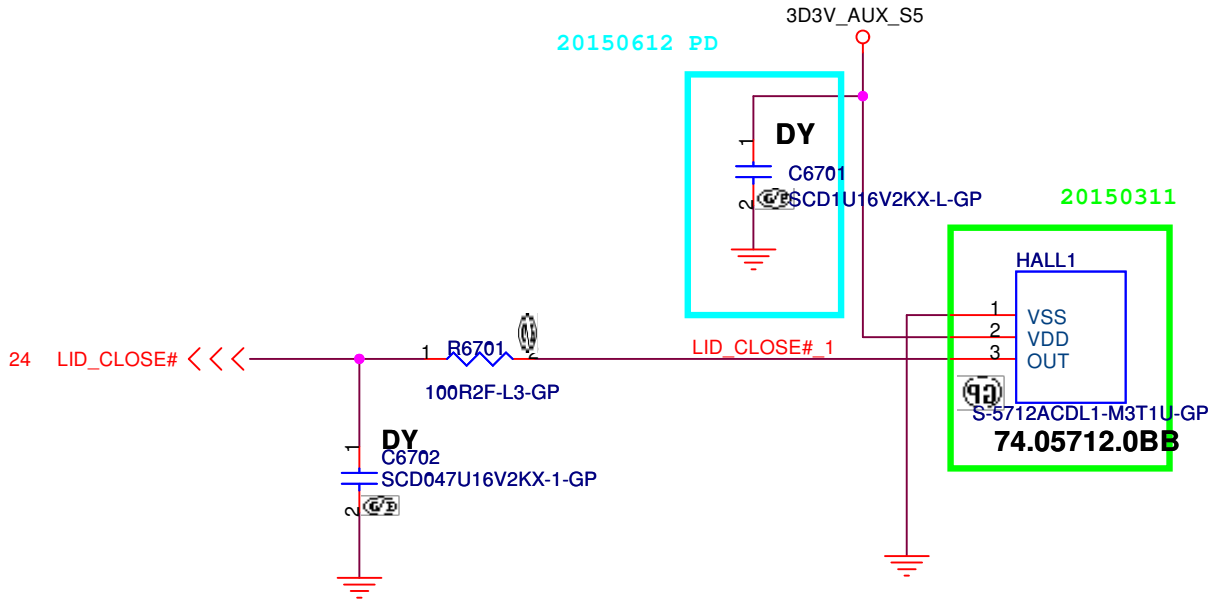

Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Security Guard connector***

Size	Document Number	Rev
A	**Mihawk MB**	-2

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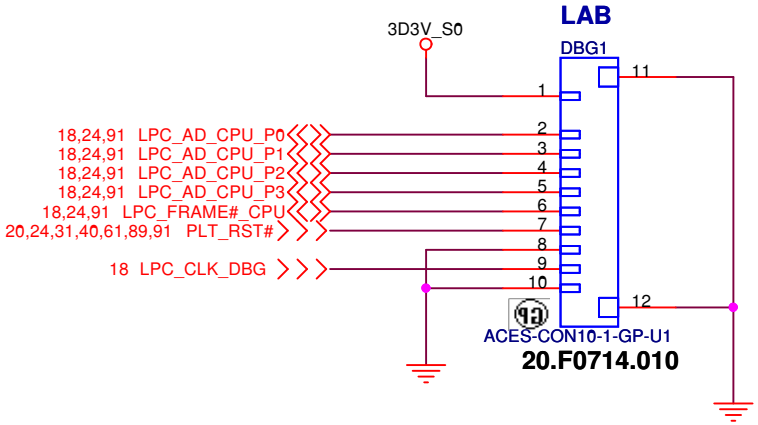

Mihawk MB

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***		
Size: A4	Document Number: **Mihawk MB**	Rev: **-2**
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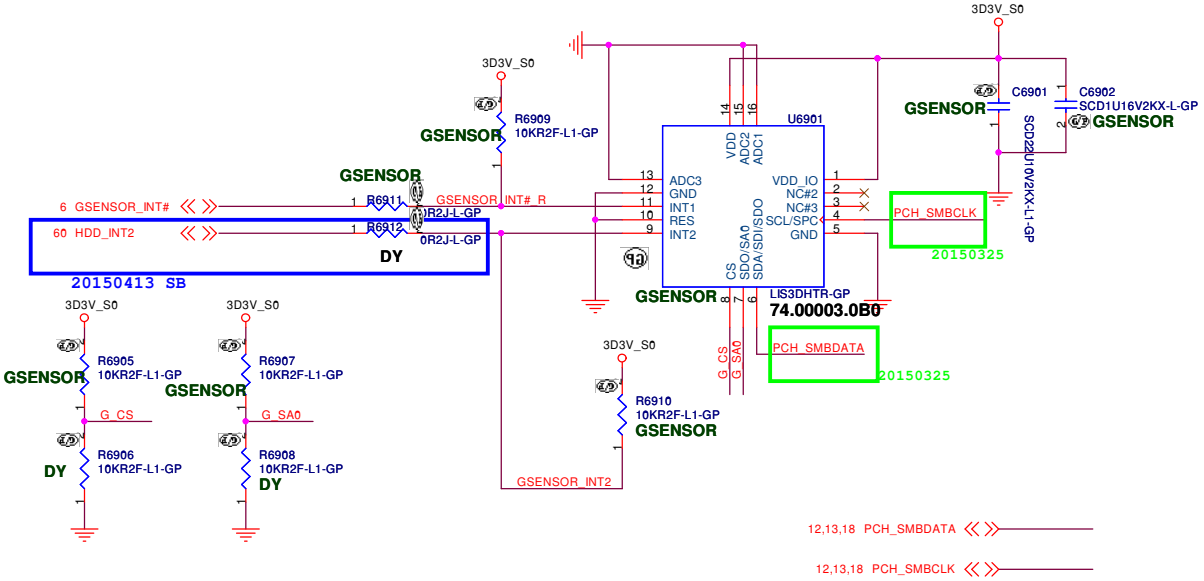
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

Mihawk MB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G-SENSOR	
Size A3	Document Number Mihawk MB	Rev -2
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Mihawk MB

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
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Mihawk MB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Thunderbolt(1/5)*		
Size: A2	Document Number: Mihawk MB	Rev: -2
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Mihawk MB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Thunderbolt(2/5)***

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A2	**Mihawk MB**	-2

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Title: ***Thunderbolt(3/5)***

Size	Document Number	Rev
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Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
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Title: ***Thunderbolt (5/5)***

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A4	**Mihawk MB**	**-2**

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Title

GPU (PEG)

Size	Document Number	Rev
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Title

GPU (DIGITALOUT)

Size	Document Number	Rev
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Title: *GPU (VRAM I/F)*

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Title

GPU (GPIO/STRAP)

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Title: ***GPU (POWER/GND)***

Size	Document Number	Rev
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Title

GPU-VRA1,2 (1/4)

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Title

GPU-VRAM3,4 (2/4)

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Title
GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
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Title
GPU-VRAM7,8 (4/4)

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Title: ***VGA_CORE***

Size	Document Number	Rev
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Title: DISCRETE VGA POWER

Size	Document Number	Rev
Custom	Mihawk MB	-2
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Title **DISCHARGE**

Size	Document Number	Rev
A4	Mihawk MB	-2

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Title
Switchable GFX LCD(2/2)

Size	Document Number	Rev
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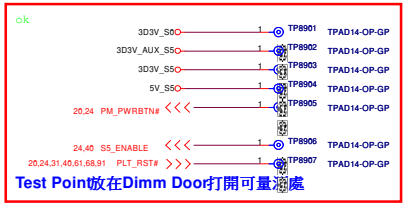
Check test point



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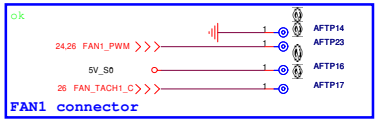

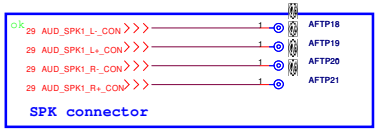

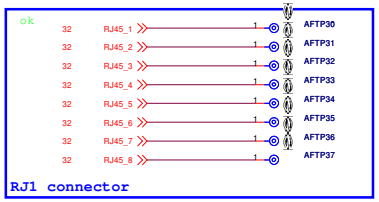

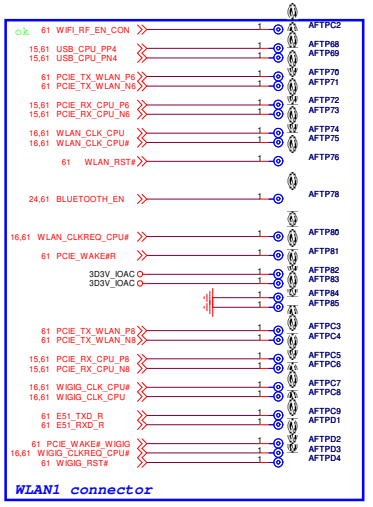

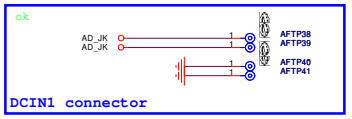

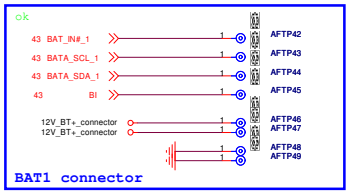

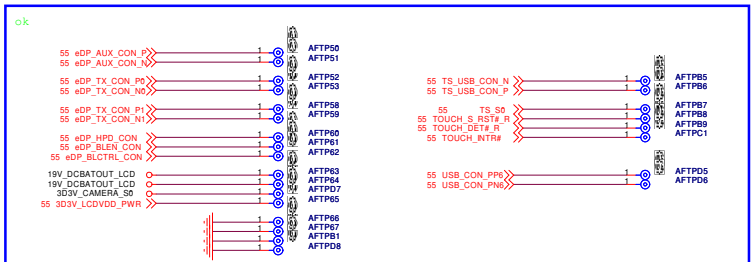

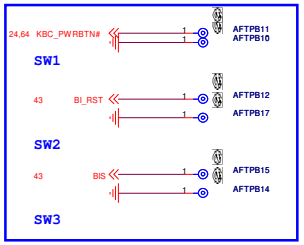

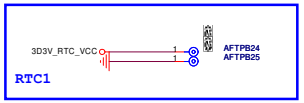

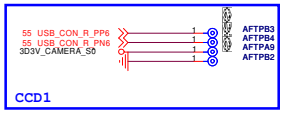

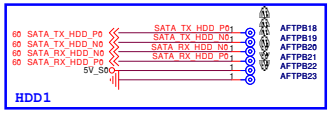

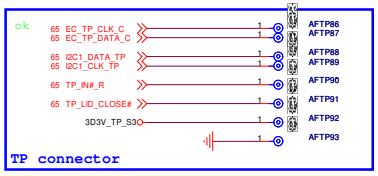

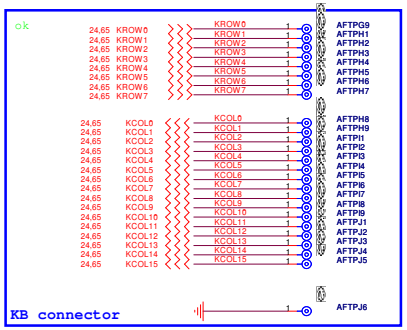

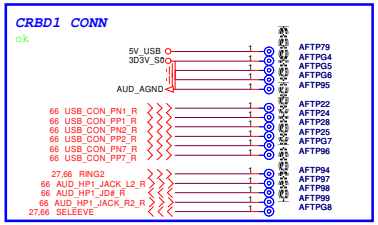

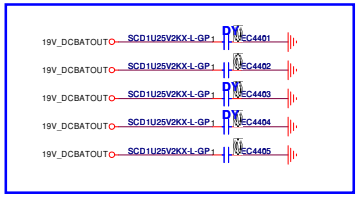

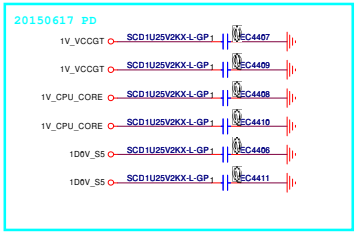

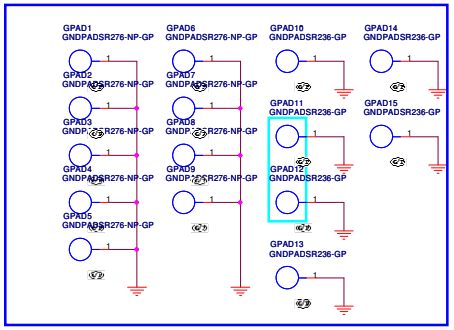

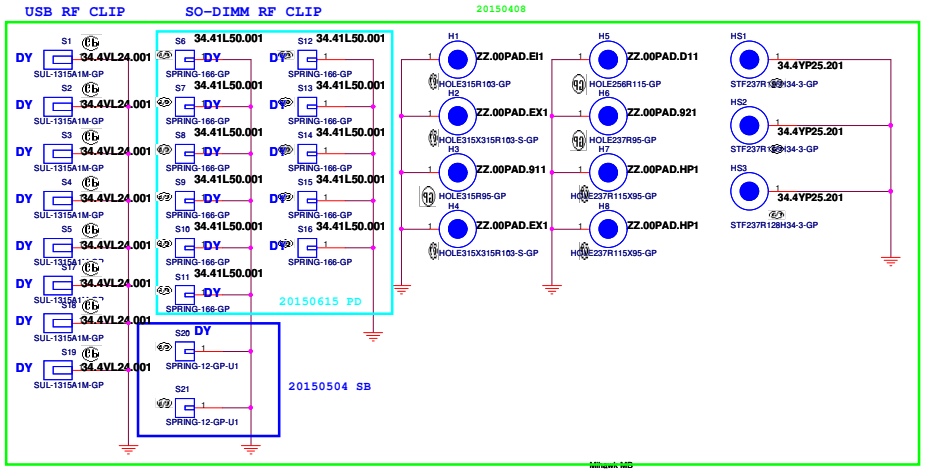

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Title: UNUSED PARTS/EMI Capacitors

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Title: NFC

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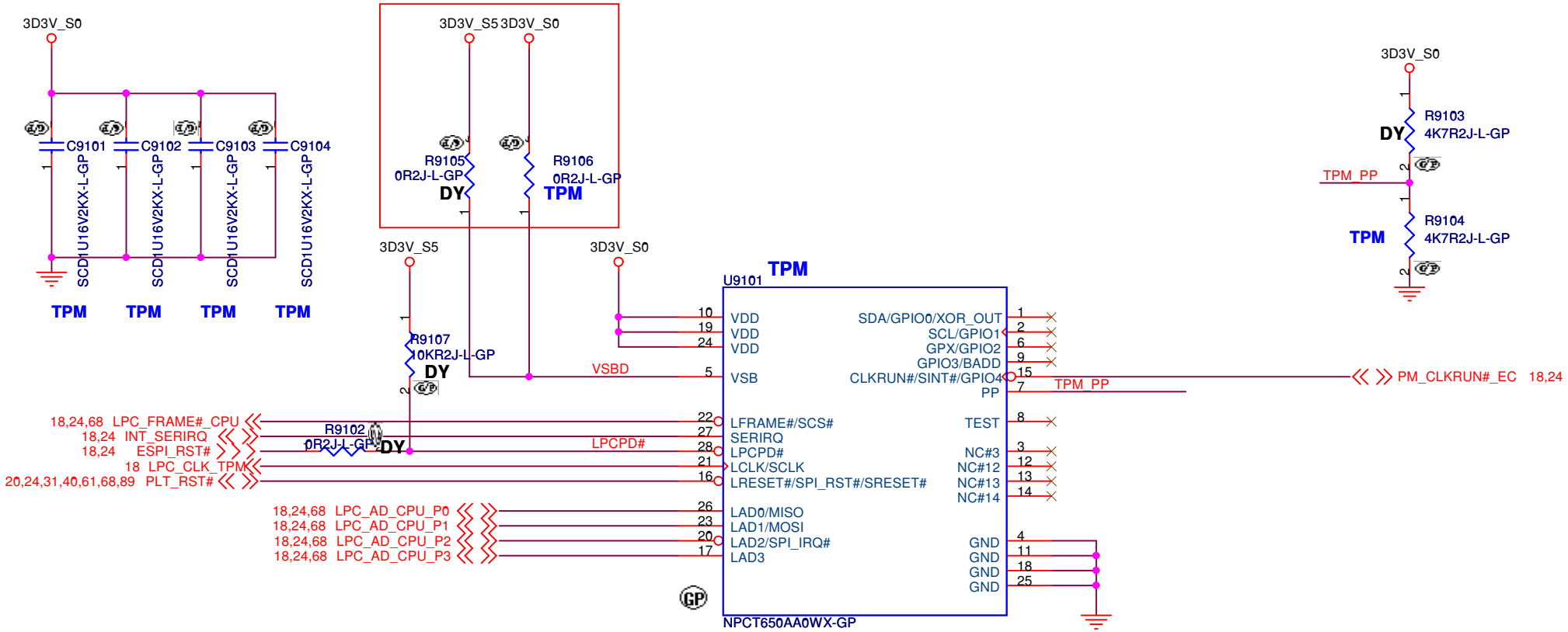

Mihawk MB

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Title: ***Finger Print***

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Title: ***Express Card***

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Smart Card socket***

Size	Document Number	Rev
A	**Mihawk MB**	**-2**

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Title: ***Switchable GFX eDP***

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A	**Mihawk MB**	-2
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Title: ***Bottom Docking***

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A	**Mihawk MB**	**-2**

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Inter LAN WG1217LM***

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Title: ***LAN Switch***

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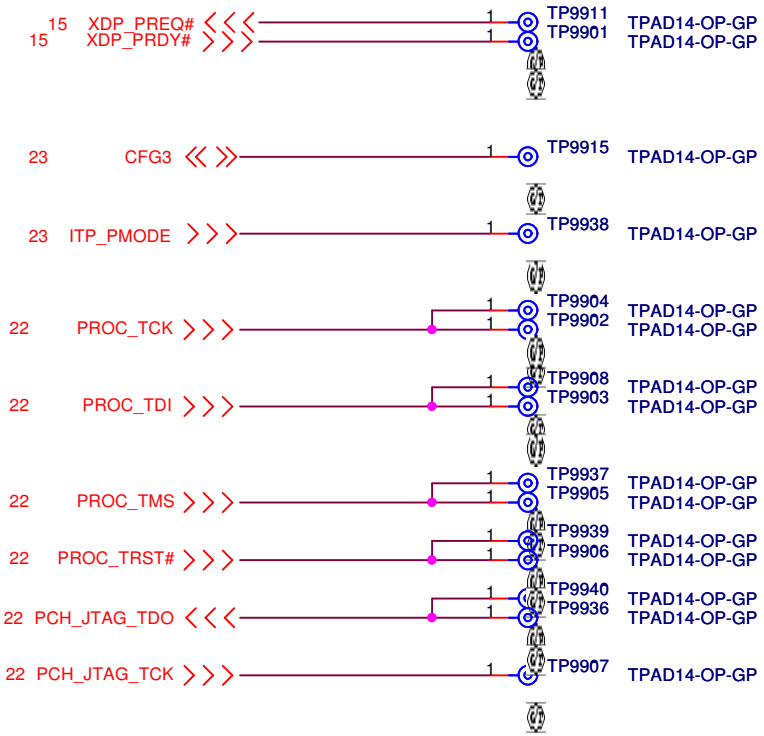
Main Func = Debug



Mihawk MB

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Title: ***CPU_XDP***

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Title: ***Change History***

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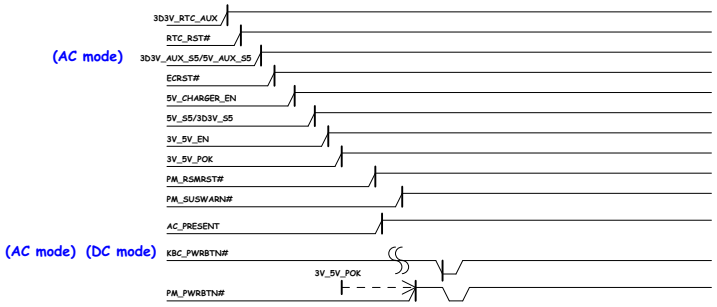
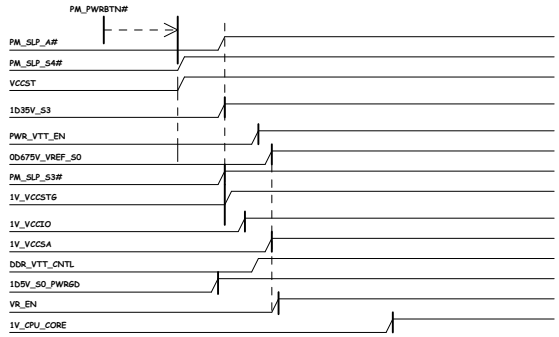
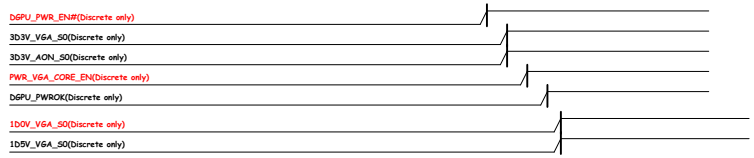
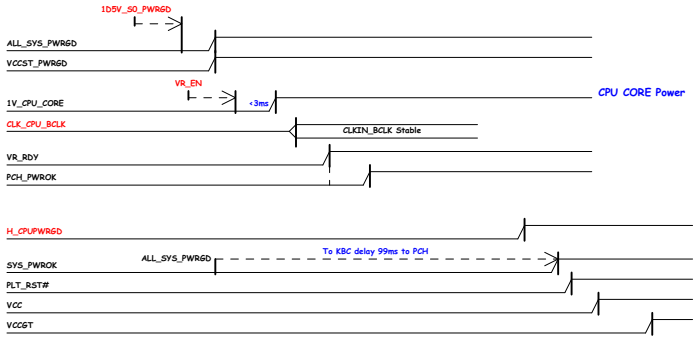
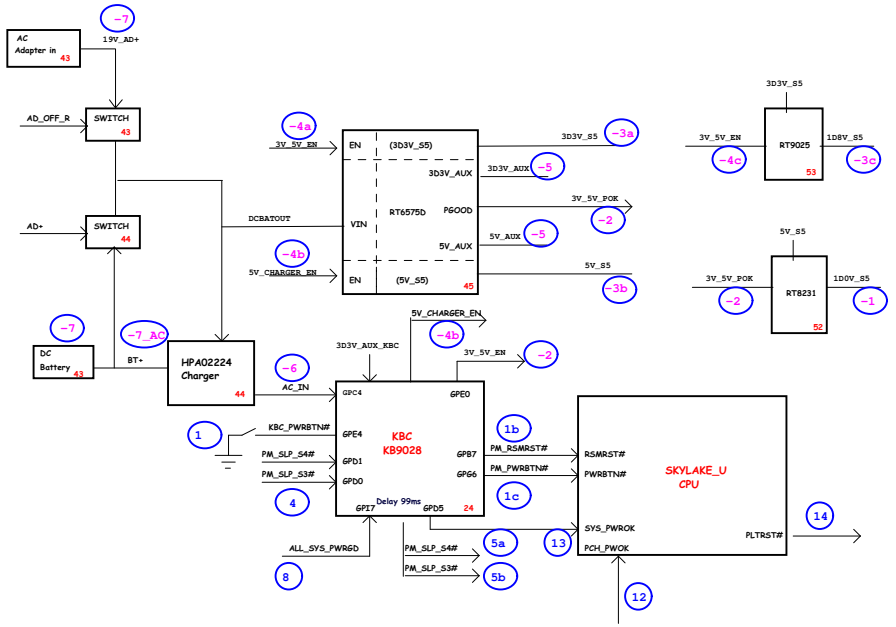
Intel-Power Up Sequence

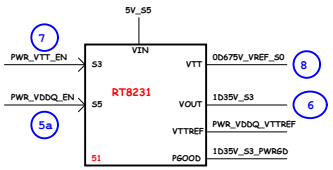


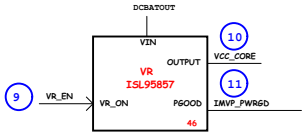


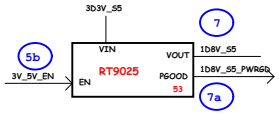


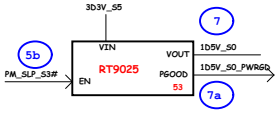


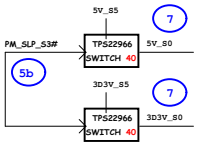


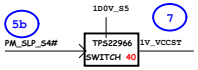


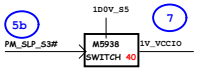












Mihawk MB

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Title: Power Sequence

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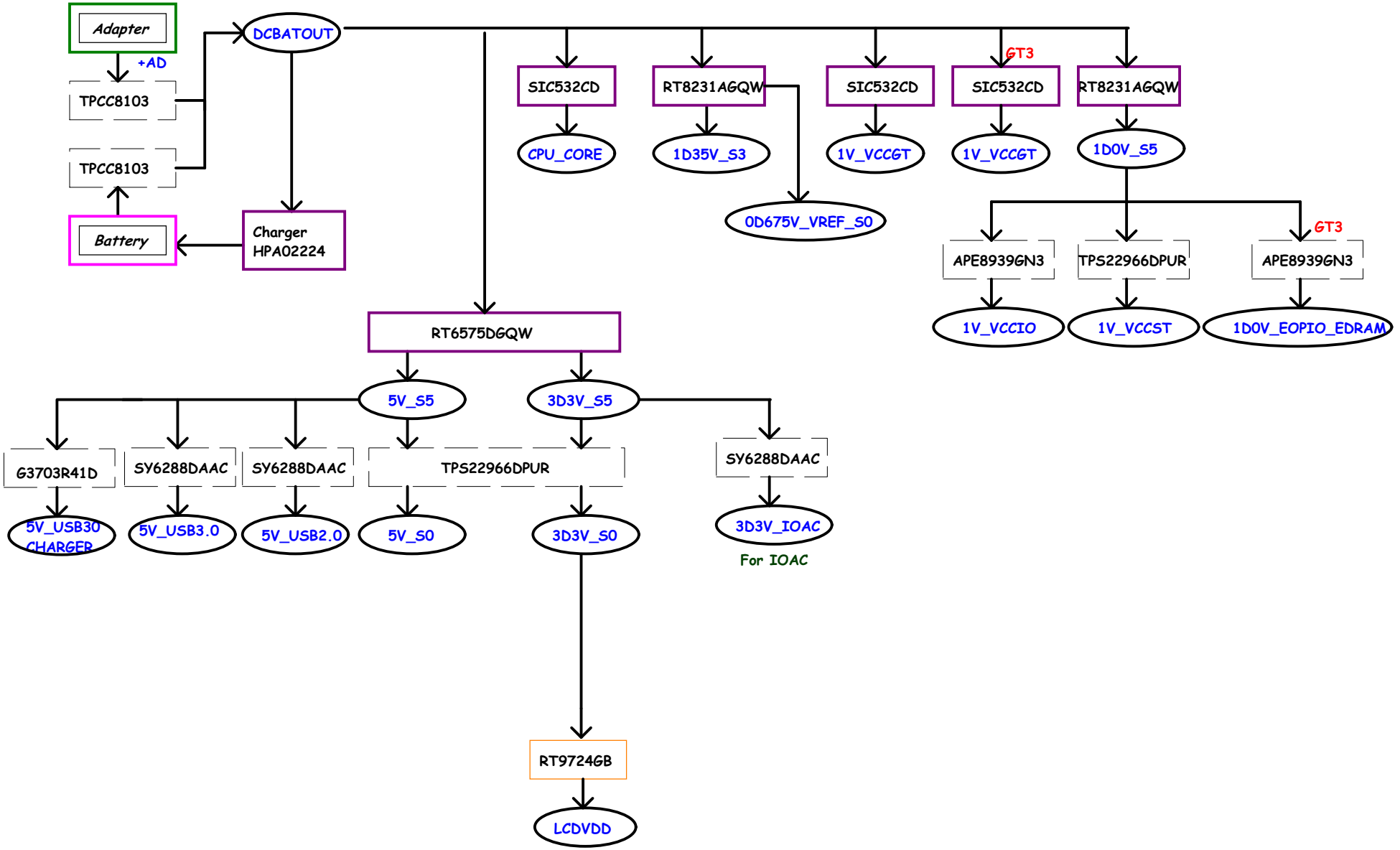

Mihawk MB

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Title: **Power Block Diagram**

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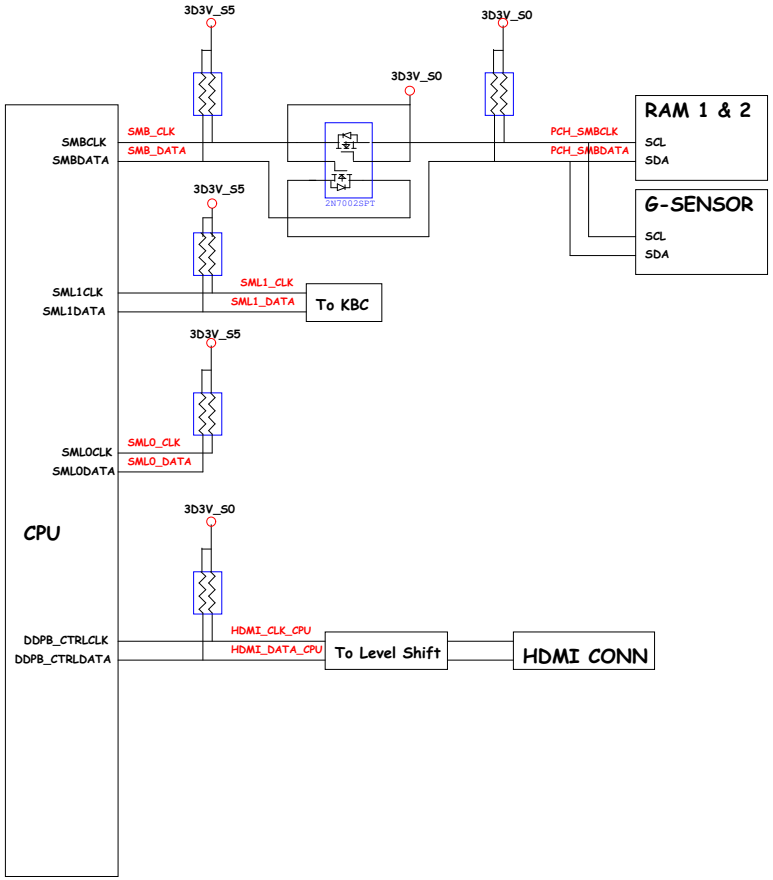
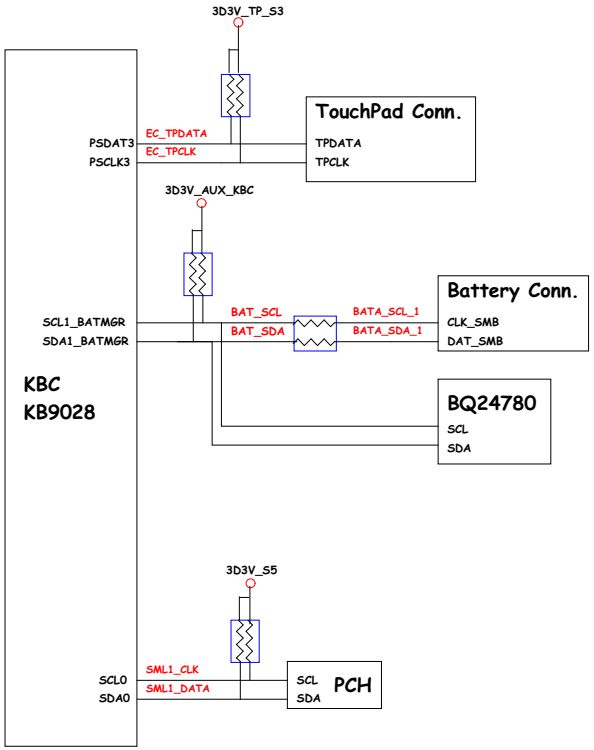
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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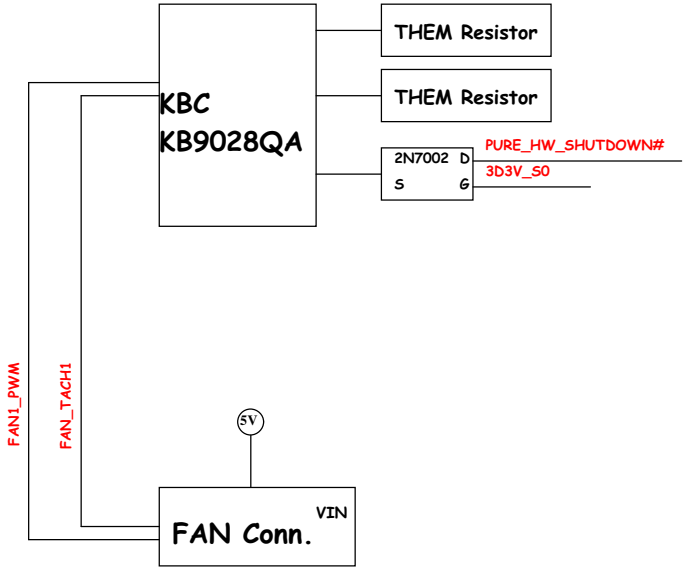
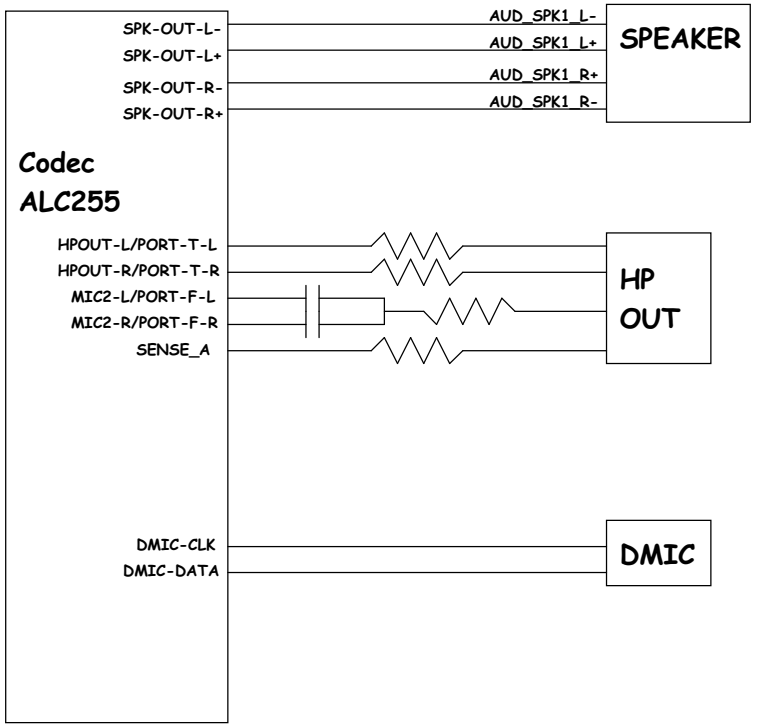
Thermal Block Diagram



Audio Block Diagram



Mihawk MB

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Title: THERMAL/AUDIO BLOCK DIAGRAM

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