Compal Confidential

Kabylake-U M/B Schematics Document

Intel ULV Processor with DDR4 SODIMMx2

Date : 2016/05/11

Version : 0.2(PV phase)

Project :*Diner_Crepe1.1(15")*

BDL50 : LA-D707P

(Modified Source:LA-D704PR20_2016-04-20)

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: Cover Page

Size	Document Number	Rev
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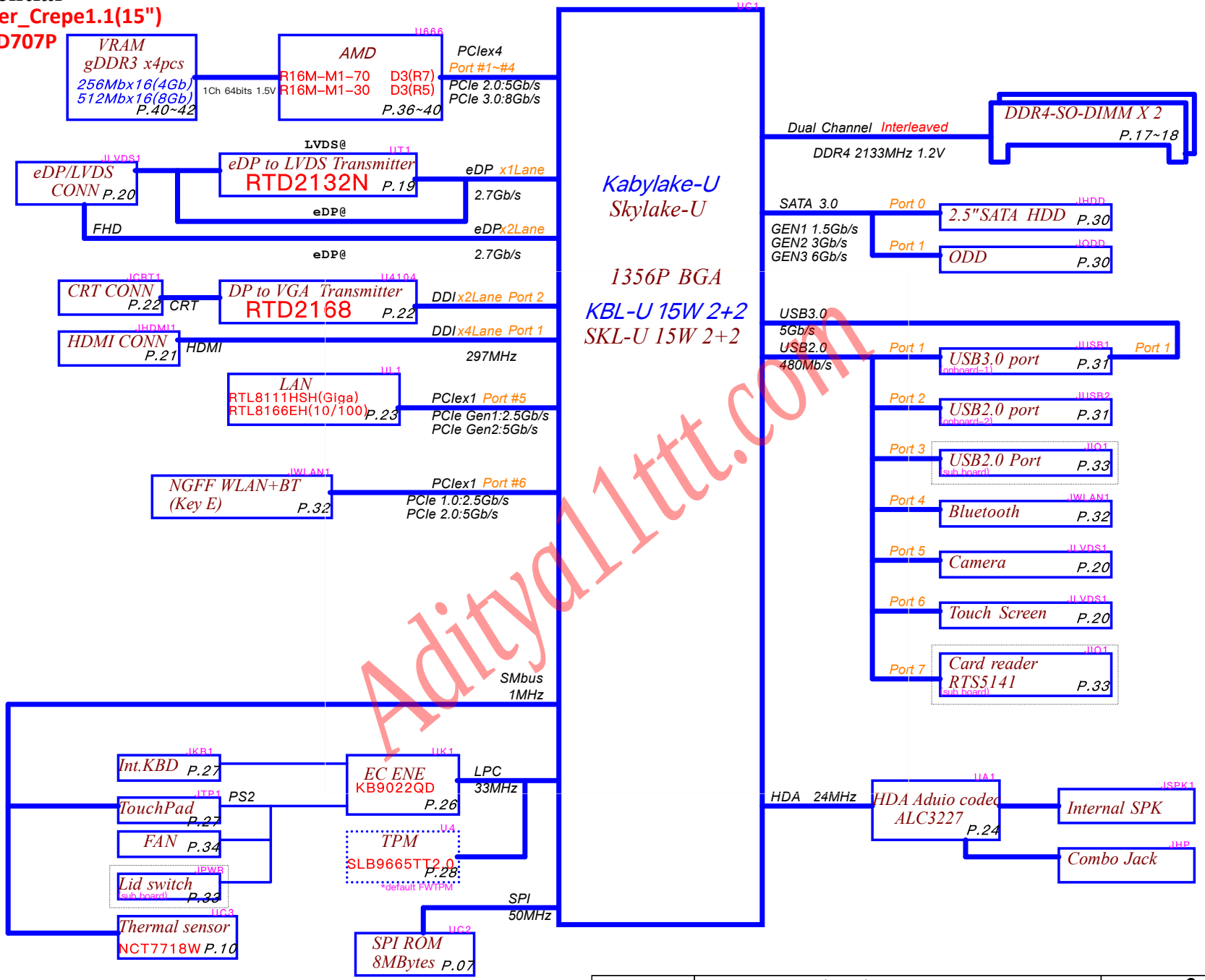
Model Name : Diner_Crepe1.1(15")

File Name : LA-D707P



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Title: Block Diagrams

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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Funct i on	Stuf f	Un-Stuf f
DGPU SKU	PX@	
UMA SKU	UMA@	
SPI_IO3(MOW36)	ES@	
Crystal (DIS)	XTALPX@	
Crystal	XTAL@	
Green CLK(UMA)	GCLK@	
Green CLK(DIS)	GCLKPX@	
TPM	TPM@	

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3VS	DIMM1	TBC	TBC	0xA2
		Touch PAD	TBC	TBC	TBC
SML0CLK SML0DATA	+3VS	ME FW	0x48/0x49	TBC	0x90/0x92
SML1CLK SML1DATA	+3VS	EC	TBC	TBC	TBC
		DGPU	TBC	TBC	TBC
		PCH	TBC	TBC	TBC

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	TBC
		Thermal Sensor	0x4C
		PCH	TBC

Power State

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

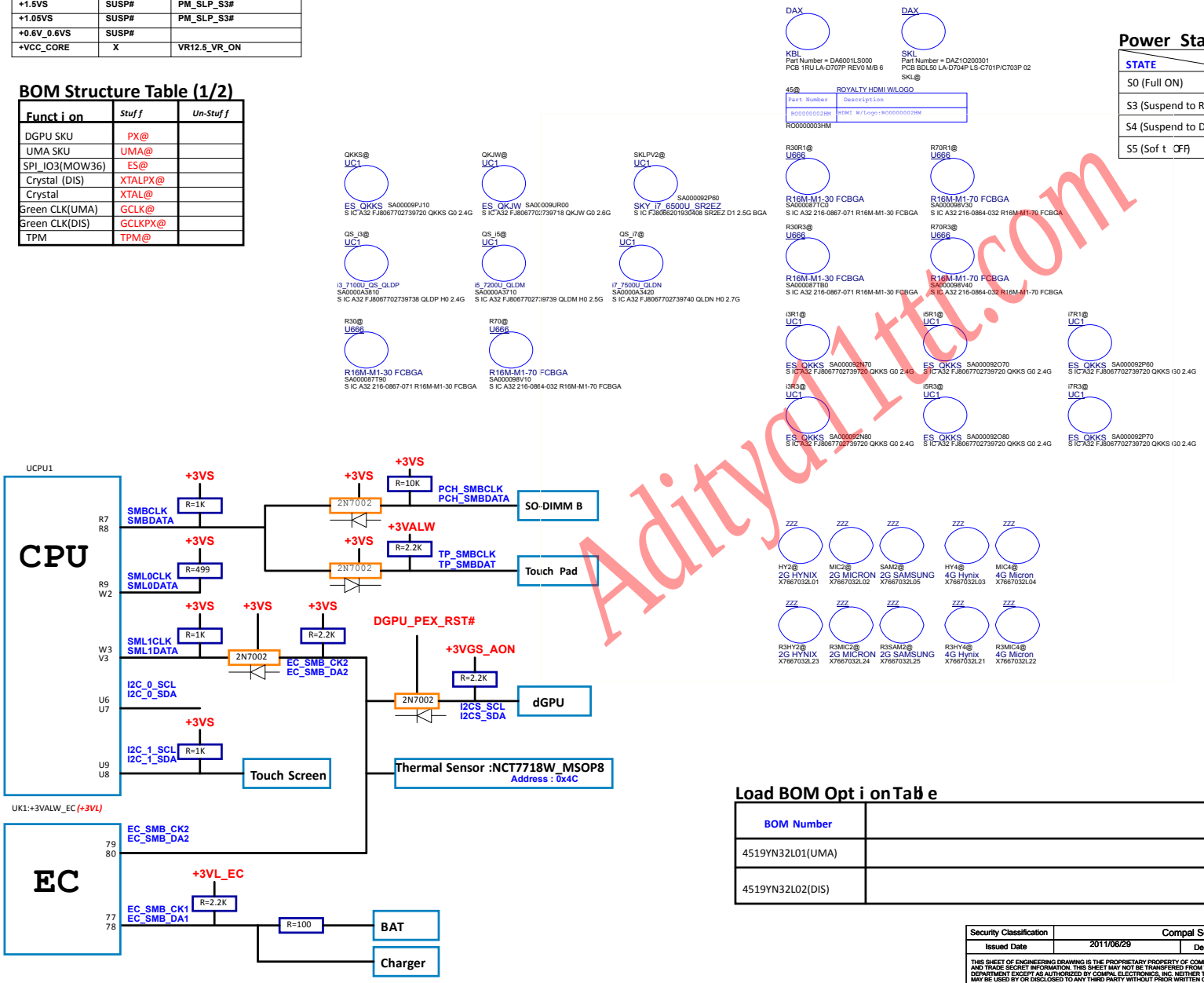
USB2.0 port	DESTINATION UMA	DESTINATION Dis
1	USB 2.0/3.0	USB 2.0/3.0
2	USB 2.0/3.0	USB 2.0/3.0
3	USB 2.0 OFF BOARD	USB 2.0 OFF BOARD
4	WLAN	WLAN
5	Camera	Camera
6	TOUCH SCREEN	TOUCH SCREEN
7	CR	CR
8		
9		
10		

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION UMA	DESTINATION Dis	CLK
1			1	USB3.0	USB3.0	X
2			2	USB3.0	USB3.0	X
3			3	USB3.0(Charger)	USB3.0(Charger)	X
4			4	USB3.0(IO Board)	USB3.0(IO Board)	X
5	1		5	X	GPU(DIS only)	CLK0
6	2		6	X	GPU(DIS only)	
7	3			X	GPU(DIS only)	
8	4			X	GPU(DIS only)	
9	5			LAN	LAN	CLK1
10	6			WLAN	WLAN	CLK2
11	7	0		2.5"HDD	2.5"HDD	X
12	8	1		ODD	ODD	X
13	9			Card reader(PCI-E)	Card reader(PCI-E)	CLK3
14	10			X	X	X
15	11	1*		X	X	X
16	12	2				X

Load BOM Opt i on Tab l e

BOM Number	Load BOM Opt i on
4519YN32L01(UMA)	
4519YN32L02(DIS)	



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.	
Title	Notes List
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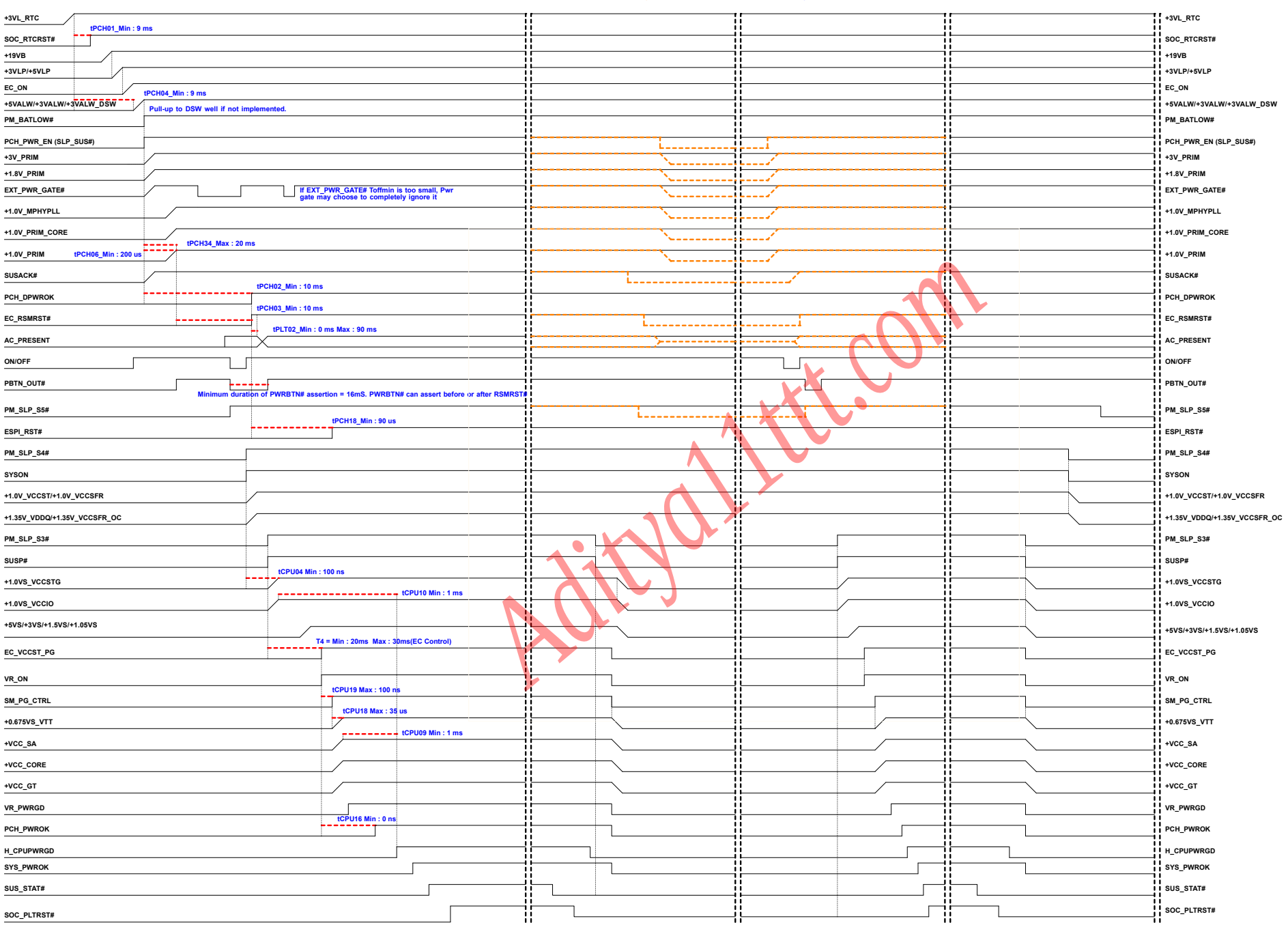
[Direct PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: HW Reserve

Size: Custom	Document Number: LA-D707P		Rev: v0.2
Date: Wednesday, May 11, 2016	Sheet: 4	of: 60	

SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

<HDMI>

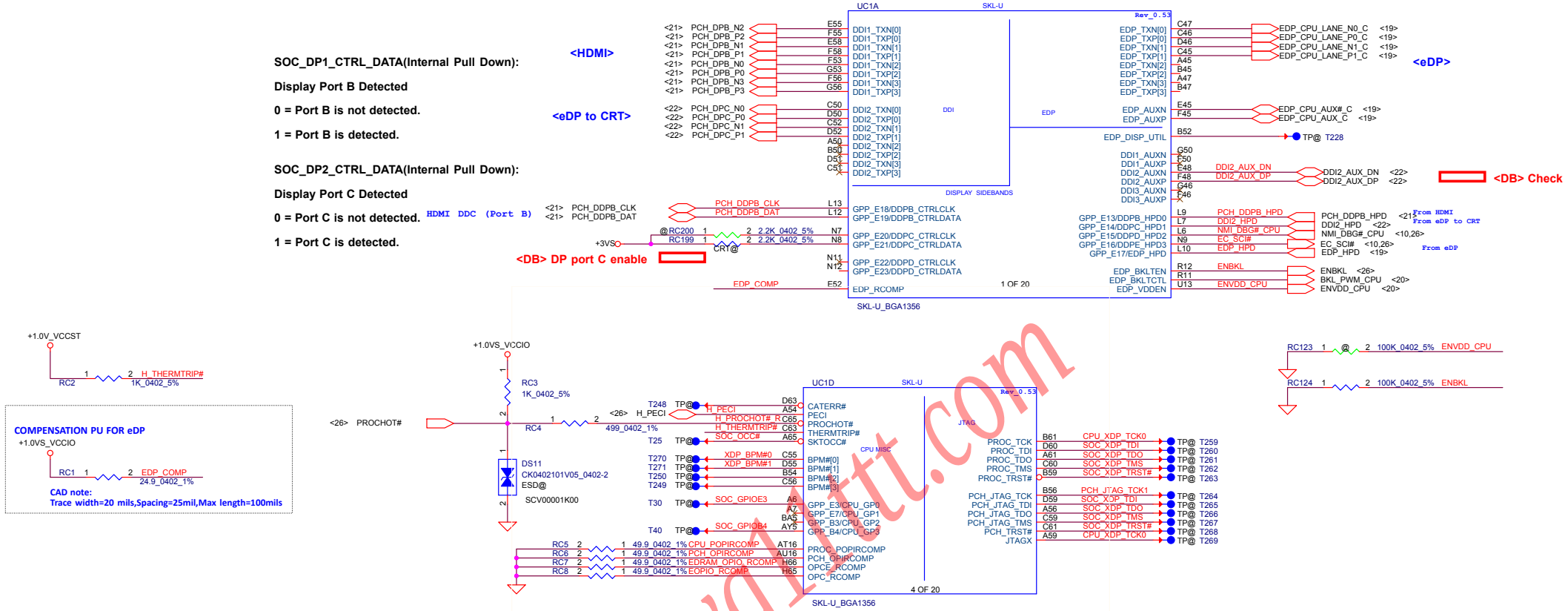
<eDP to CRT>

HDMI DDC (Port B)

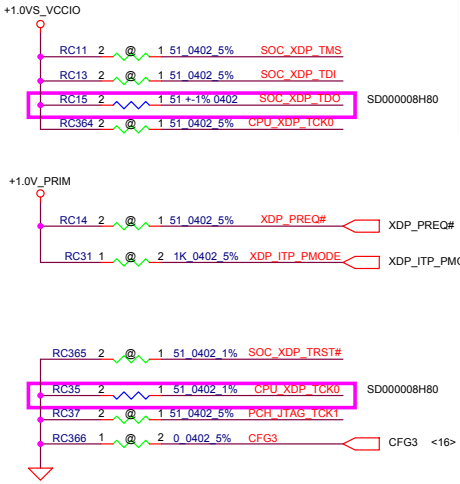
<DB> DP port C enable

<eDP>

<DB> Check



XDP CONN



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

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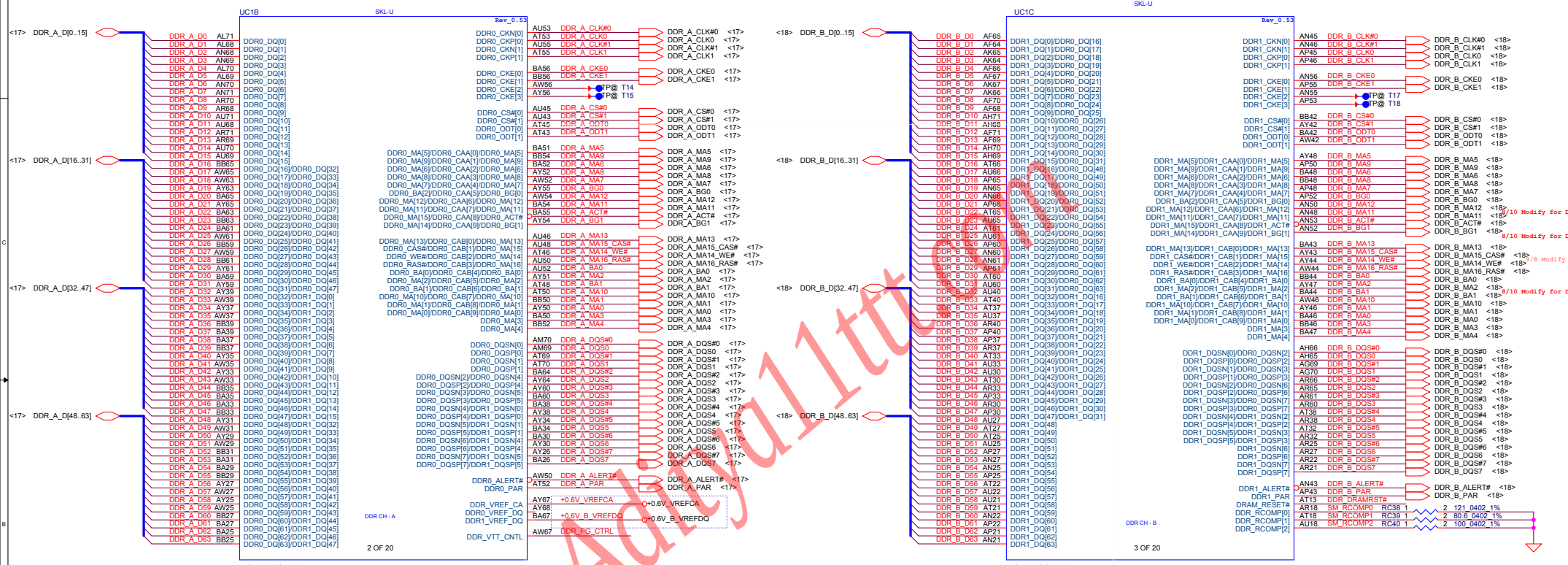
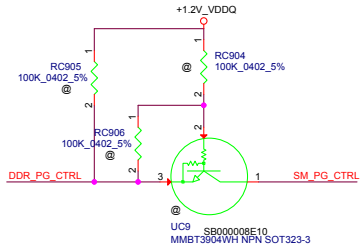
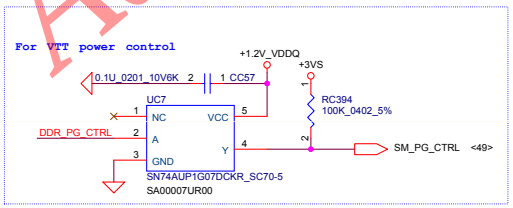
Interleaved Memory

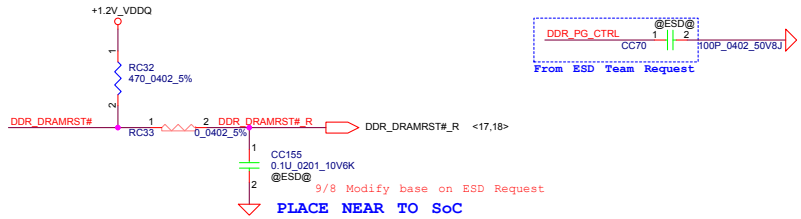
Interleaved Memory

<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)

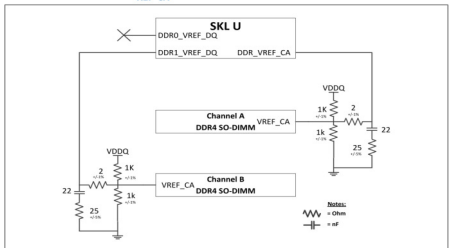








SKL U DDR4 SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	SKL-U(2/12)DDRIII		
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SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

UC1E
SKL-U
Rev_0.53
SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#
C LINK
CL_CLK
CL_DATA
CL_RST#
LPC
SMBUS, SMLINK
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#
GPP_A0/RCIN#
GPP_A6/SERIRQ
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SKL-U_BGA1356

SMB (Link to XDP, DDR, TP)
SML1 (Link to EC,DGPU, LAN, Thermal Sensor)

12/11_Delete TP
To TPM
LPC Mode

<SI>un-mount RC53
11/28 CPU side delete EC_PCIE_WAKE#
11/28_Follow Intel check list, add PU res

SPI ROM (8MByte Only)
Use socket footprint
W25Q64FVSSIQ_SO8 SA000039A30
PCB Footprint = ACES_91960-0084L_8P-T

<Cocoa 1020> add level shift

<DB> PWR Rail

11/28_Change PWR rail from +3VS to +3V_PRIM

From WW36 MOW for SKL-U ES sample

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M N25Q064A13ESE0F SO8W 8P

ENE Fixed Code Block Diagram

M:Master
S : Slave
O : Output
I : Input

Follow 543016_SKL_U_Y_PDG_0_9

Security Classification	Compal Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/31

Compal Electronics, Inc.
Title: SKL-U(3/12)SPI,ESPI,SMB,LPC
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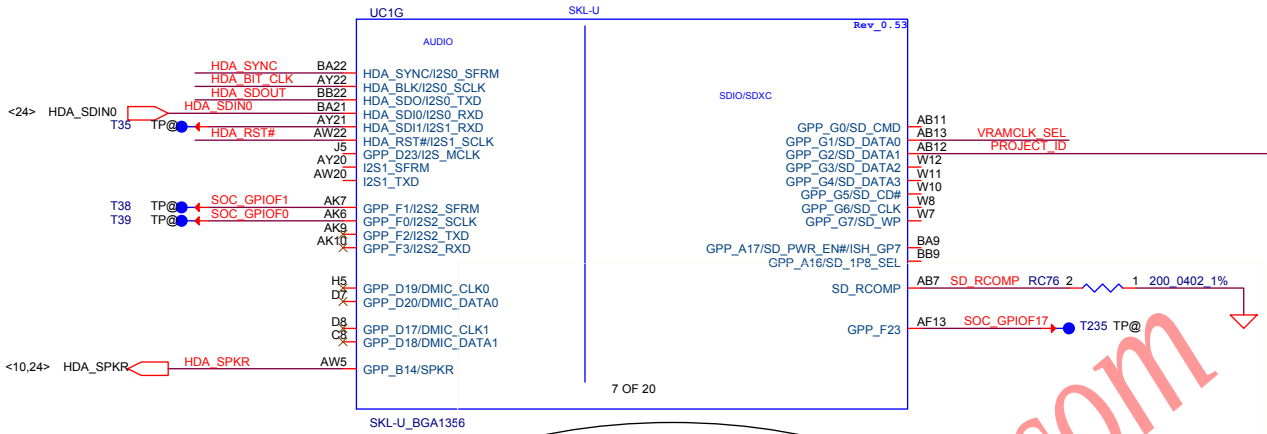
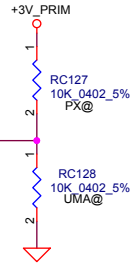
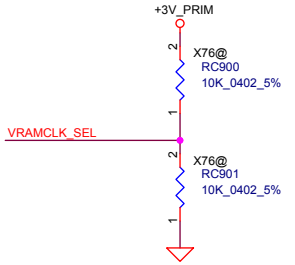


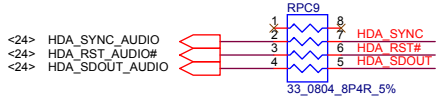


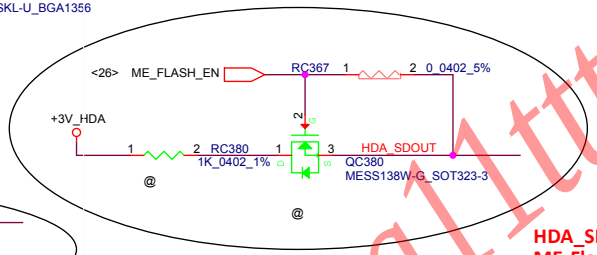
	UMA	DIS
PROJECT_ID	0	1

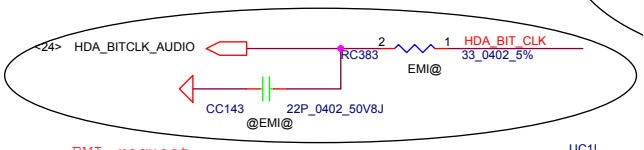
	900MHz	1000MHz
VRAM Clock	0	1



HDA for AUDIO

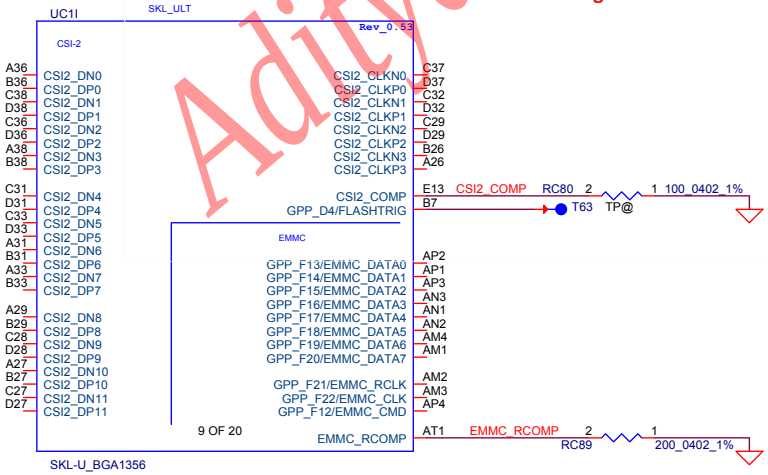






EMI request

HDA_SDOUT:
ME Flash Descriptor Security Override
Low : Disabled(Default)
High : Enabled



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

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+3VCC

RC91 1 2 20K_0402_5% PCH_SRTCRST#
CC10 1 2 1U_0402_6.3V6K
CLRP1 1 2 SHORT PADS CLR_ME
RC93 1 2 20K_0402_5% PCH_RTCRST#
CC11 1 2 1U_0402_6.3V6K
CLRP2 1 2 SHORT PADS CLR_CMOS
RC941 2 1M_0402_5% SM_INTRUDER#

PCH_RTCRST# 2 @ 1 0_0402_5% R1088
PCH_SRTCRST# 2 @ 1 0_0402_5% R1089
CLR_CMOS# <26>
Clear CMOS close to RAM door
JCMOS1 0_0603_5%

+3VS

RC165 1 2 CLKREQ_PCIE#4 10K_0402_5%
RC105 1 2 CLKREQ_PCIE#5 10K_0402_5%
From 545659_SKL_PCH_U_Y_EDS_R0_7
<Cocoa_1027>
check un-use GPIO for termination guidance

RPC10
8 1 LAN_CLKREQ#
7 2 MINI1_CLKREQ#
6 3 CR_CLKREQ#
5 4
10K_0804_8P4R_5%

+3V_PRIM
RC109 1 @ 2 VGA_CLKREQ# 10K_0402_5%
<DB> unpop, PD at GPU side

+3VALW_DSW

RPC11
8 1 PCH_PWROK
7 2 LAN_WAKE#
6 3 PCH_RSMRST#
5 4 SYS_RESET#
10K_0804_8P4R_5%

DS12
2 1 PCH_PWROK
CK0402101V05_0402-2
ESD@
SCV00001K00

CLRP3 2 1 SYS_RESET# SHORT PADS
RC100 1 @ 2 SUSCLK 1K_0402_5%
RC101 2 1 PCH_DPWROK 100K_0402_5%

+3VALW_DSW

RC103 1 2 8.2K_0402_5% PM_BATLOW#
RC104 1 2 1K_0402_5% WAKE#
RC106 1 2 10K_0402_5% AC_PRESENT_R
@ <DB> RC106 unpop , follow module design

+3V_PRIM
RC1151 @ 2 10K_0402_5% SOC_VRALERT#

+3VALW_DSW
RC111 2 @ 1 100K_0402_5% PBTN_OUT#

UC1J SKL_ULT Rev_0.53
CLOCK SIGNALS

GPU
<36> CLK_PEG_VGA# → D42 CLKOUT_PCIE_N0 / GPP_B5/SRCCLKREQ0#
<36> CLK_PEG_VGA → C42 CLKOUT_PCIE_P0
<37> VGA_CLKREQ# → AR10

LAN
<23> CLK_PCIE_LAN# → B42 CLKOUT_PCIE_N1
<23> CLK_PCIE_LAN → A42 CLKOUT_PCIE_P1 / GPP_B6/SRCCLKREQ1#
<23> LAN_CLKREQ# → AT7

WLAN
<32> CLK_PCIE_WLAN# → D41 CLKOUT_PCIE_N2
<32> CLK_PCIE_WLAN → C41 CLKOUT_PCIE_P2
<32> MINI1_CLKREQ# → AT8 / GPP_B7/SRCCLKREQ2#

CardReader
CR_CLKREQ# → D40 CLKOUT_PCIE_N3 / C40 CLKOUT_PCIE_P3 / AT10 GPP_B8/SRCCLKREQ3#

CLKREQ_PCIE#4 → B40 CLKOUT_PCIE_N4 / A40 CLKOUT_PCIE_P4 / AU8 GPP_B9/SRCCLKREQ4#

CLKREQ_PCIE#5 → E40 CLKOUT_PCIE_N5 / E38 CLKOUT_PCIE_P5 / AU7 GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N E43
CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17 → SUSCLK <32>
XTAL24_IN E37 PCH_XTAL24_IN
XTAL24_OUT E35 PCH_XTAL24_OUT
XCLK_BIASREF E42 XCLK_BIASREF RC96 1 2 2.7K_0402_1% +1.0V_CLK5_F24NS
RTCX1 AM18 PCH_RTCX1
RTCX2 AM20 PCH_RTCX2
SRTCRST# AN18 PCH_SRTCRST#
RTCRST# AM16 PCH_RTCRST#

10 OF 20
SKL-U_BGA1356

XCLK_BIASREF RC97 1 @ 2 60.4_0402_1%
<DB> stuff for cannot take 60ohm 1%
<SI> change to SJ10000Q300 , CL=9p

PCH_XTAL24_IN
PCH_XTAL24_OUT
RC92 1 2 1M_0402_5%
YC1 SJ10000IZ00 24MHZ 12PF 20PPM X3G024000DC1H
GND GND
CC12 22P_0402_50V8J
CC13 22P_0402_50V8J

PCH_RTCX2
PCH_RTCX1
RC98 1 2 10M_0402_5%
YC2 32.768KHZ 9PF 10PPM 9H03200055
SJ10000Q800
CC15 6.8P_0402_50V8J
CC16 6.8P_0402_50V8J

<Cocoa_1020>
32M use these part (SJ10000NM00, SJ10000MH00) just can meet <50k ohm spec
24M: SJ10000DI00, SJ10000CS00
<PV> change CC15,CC16 to 6.8p
<MV> change CC15,CC16 to 8.2p

PCH PLTRST Buffer <DB> Remove PLT_RST# buffer
RC99 1 2 0_0402_5%
+3VS
@CC145 1 2 0.1U_0402_16V7K
UC8
PLT_RST#_PCH → IN1
IN2 ← +3VS
O → PLT_RST# → PLT_RST# <23,26,28,32,36>
SN74AHC1G08DCKR_SC70-5

UC1K SKL-U Rev_0.53
SYSTEM POWER MANAGEMENT

PLT_RST# PCH AN10
SYS_RESET# B5
PCH_RSMRST# AY17
H_CPUPWRGD A68
EC_VCCST_PG B65
SYS_PWROK B6
PCH_PWROK BA20
PCH_DPWROK_R BB20
PCH_SUSWARN# AR13
SUSACK#_R AP11
WAKE# BB15
LAN_WAKE# AM15
AW17
AT15

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD

GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#

AT11 PM_SLP_S0#
AP15 PM_SLP_S3#
BA16 PM_SLP_S4#
AY16 PM_SLP_S5#
AN15 PM_SLP_SUS#
AW15 SLP_LAN#
BB17 SLP_WLAN#
AN16 PM_SLP_A#
BA15 PBTN_OUT#
AY15 AC_PRESENT_R
AU13 PM_BATLOW#
AU11 EC_PCIE_WAKE#
AP16 SM_INTRUDER#
AM10 EXT_PWR_GATE#
AM11 SOC_VRALERT#

PM_SLP_S3# <12,26,35>
PM_SLP_S4# <12,26,35,49>
PM_SLP_S5# <26>
PM_SLP_SUS# <13,26>
PBTN_OUT# <26>
ACIN <26,37>
EC_PCIE_WAKE# <26,32>

TP@T254
TP@T255
TP@T256
TP@T257
TP@T258
TP@T87
TP@T88
TP@T298

11 OF 20
SKL-U_BGA1356

T95 TP@
<26> PCH_RSMRST# → RC102 1 @ 2 1K_0402_5%
Only For Power Sequence Debug

<26> SYS_PWROK
<26> PCH_PWROK
<26> PCH_DPWROK

<26> PCH_SUSWARN# → RC110 1 2 0_0402_5%
<26> SUSACK#
<32> WAKE#

T94 TP@

DS13 ESD@ SCV00001K00
1 2 H_CPUPWRGD
CK0402101V05_0402-2

DS14 @ESD@ SCV00001K00
1 2 SUSACK#
CK0402101V05_0402-2

DS15 @ESD@ SCV00001K00
1 2 SYS_PWROK
CK0402101V05_0402-2

<DB> add ESD protection

DC3 SCS00003500 CH751H-40PT_SOD323-2
PCH_RSMRST# 1 2 PCH_PWROK
2 1 SPOK <48>
DC4 SCS00003500 CH751H-40PT_SOD323-2
11/28 add RSMRST protect circuit

<26> PCH_DPWROK → RC112 2 1 0_0402_5% PCH_DPWROK_R

From EC(open-drain)
+1.0V_VCCST
RC113 1K_0402_5%
<26,35> EC_VCCST_PG_R → RC1161 2 60.4_0402_1% EC_VCCST_PG

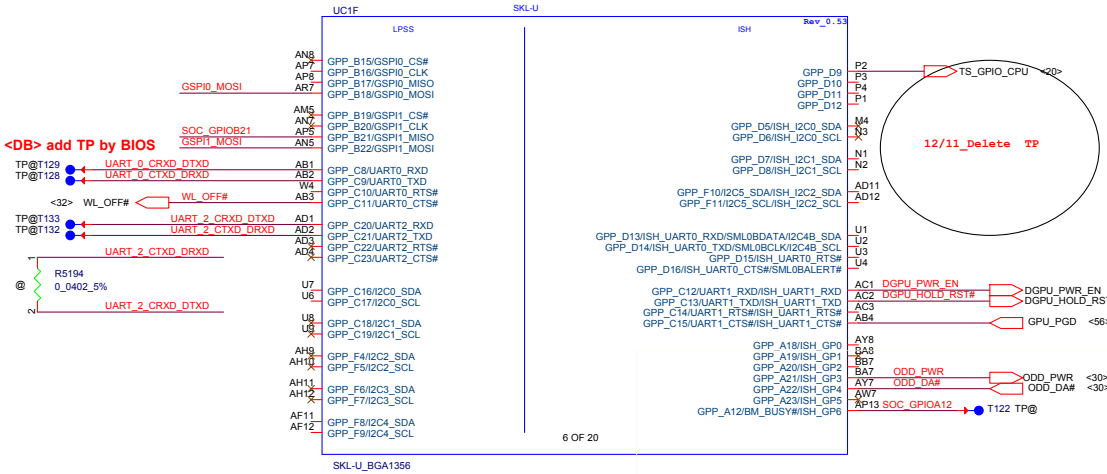
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,GPIO

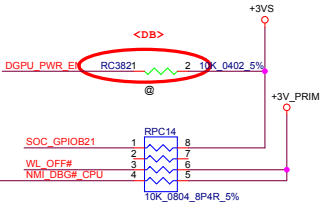
Size	Document Number	Rev
Custom	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 9 of 60

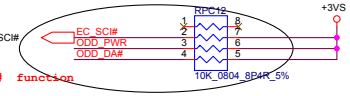


<DB> add TP by BIOS

TP@T129 UART_0_CRXD_DTXD
TP@T128 UART_0_CTXD_DRXD
<32> WL_OFF#
WL_OFF#
TP@T133 UART_2_CRXD_DTXD
TP@T132 UART_2_CTXD_DRXD
UART_2_CTXD_DRXD
R5194 0_0402_5%
UART_2_CRXD_DTXD



<Cocoa_1027>
Follow #544669 GPIO I/O setting



<Cocoa_1127> remove EC_LID_OUT# function

Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.----> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

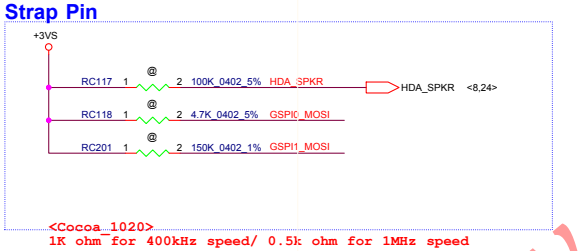
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

1 = LPC Mode

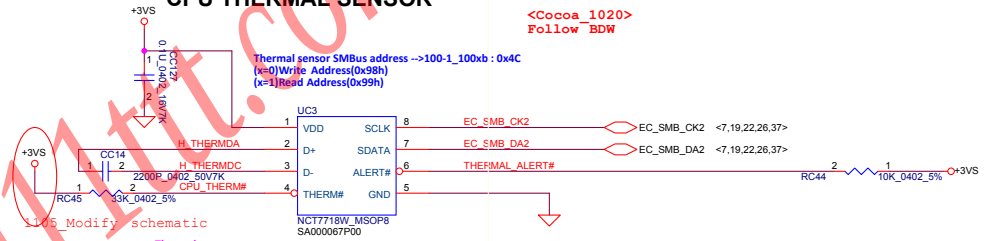
Strap Pin



<Cocoa_1020>
1K ohm for 400kHz speed/ 0.5k ohm for 1MHz speed

CPU THERMAL SENSOR

<Cocoa_1020>
Follow BDW

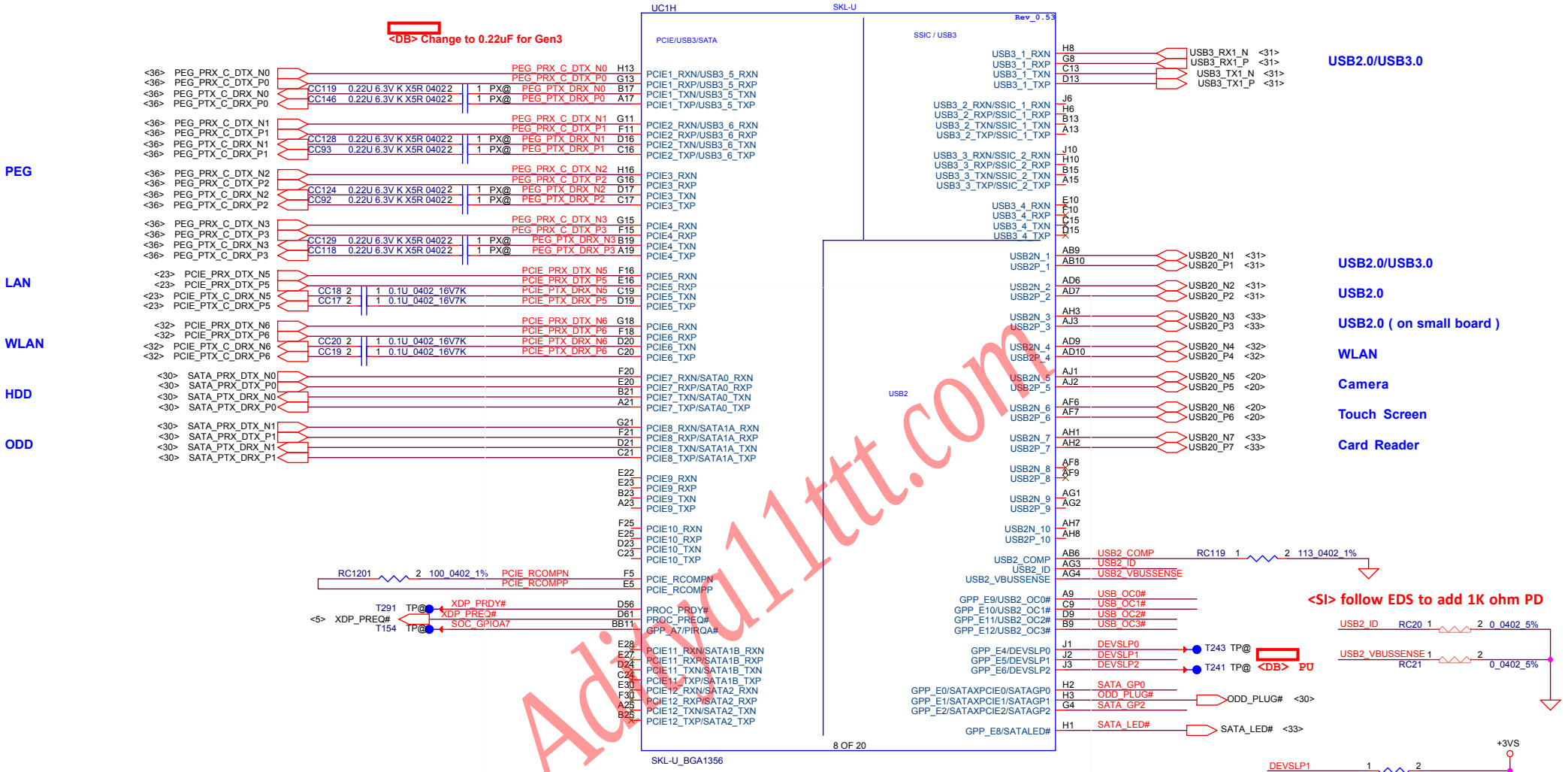


Thermal sensor:
Main:SA000067P00, S IC NCT7718W MSOP 8P THEMAL SENSOR(Nuvoton)
2nd : SA00007WP00, S IC F75397M MSOP 8P THEMAL SENSOR(Fintek)
3rd : SA007810140, S IC G781P8F MSOP 8P TEMP. SENSOR(GMT)

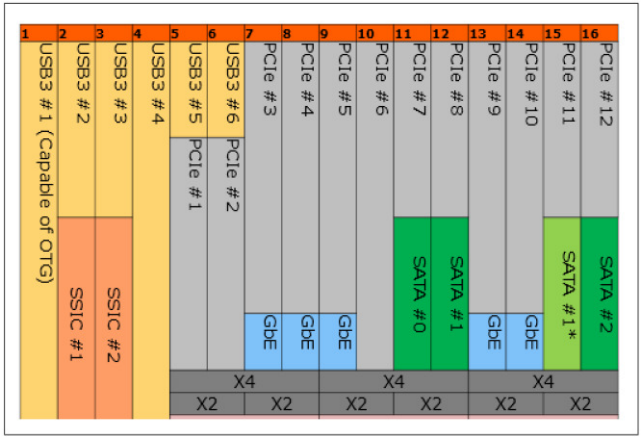
<DB>
Delete Win7 debug port

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SKL-U(6/12)GPIO			
Size: Custom	Document Number: LA-D707P		Rev: v0.2
Date: Wednesday, May 11, 2016	Sheet 10 of 60		

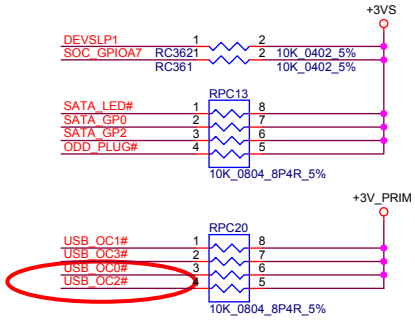


High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NGFF SSD KEY B
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	ODD_PLUG#



1128_Add pull high resistor

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 11 of 60

+1.0V_PRIM TO +1.0V_VCCSTU

1211_Delete jump RC147

1210_Delete jump RC146

I (Max) : 0.04 A(+1.0V_VCCSTU)
RON(Max) : 25 mohm
V drop : 0.001 V

I (Max) : 0.536 A(+1.8VS)
RON(Max) : 25 mohm
V drop : 0.013 V

<DB> Delete RC145

<Cocoa_1113>
Per 543977_SKL_PDDG_Rev0_91, change CC95 value from 1000pf to 10pf for meet <= 65us timing for +1.0V_VCCSTU power rail.

UC5 EM5209VF_DFN14_2X3 SA00007PM00

UC1N SKL-U CPU POWER 3 OF 4 Rev_0.53 — SKL-U_BGA1356 — 14 OF 20

<DB> change +1.35V_VDDQ

RC208 Follow 544669_SKL_U__DDR3L_RVP7_Schematic_Rev1.0

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

I (Max) : 3 A(+1.0VS_VCCIO)
RON(Max) : 6.2 mohm
V drop : 0.019 V

Imax : 2.77 A

Imax : 3 A

near pin A22

<PV> change short pad

UC6 TPS22961DNYR_WSON8

Part Number = SA00007XR00

For Verify S0IX <Cocoa_1027>
connect to EC, check /w EC

<DB> change +1.35V_VDDQ

RC208 Follow 544669_SKL_U__DDR3L_RVP7_Schematic_Rev0_53

<DB> change +1.35V_VDDQ

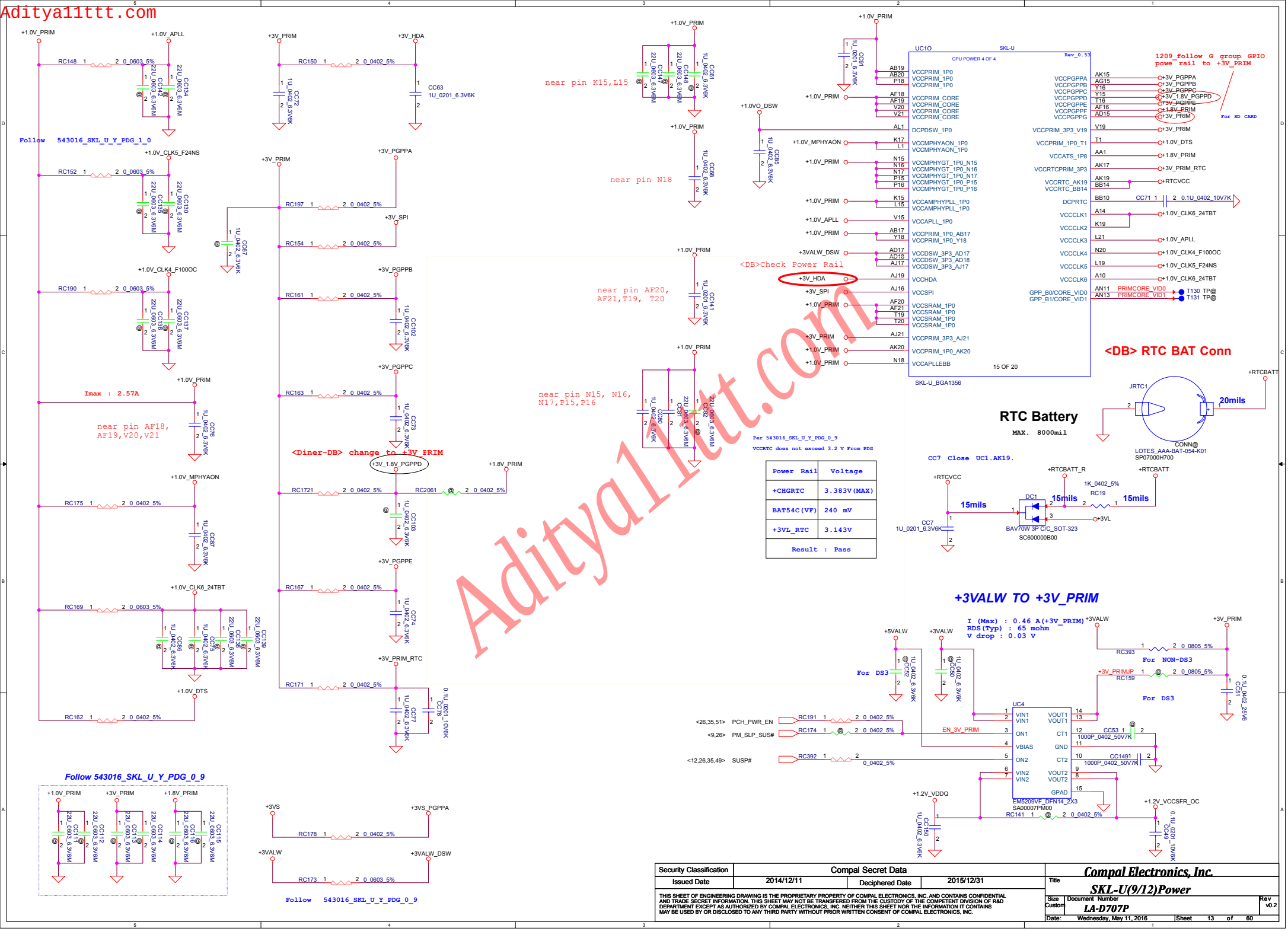
CC47 Follow 543016_SKL_U_Y_PDG_0_9

<DB> change +1.35V_VDDQ

+1.35V_VDDQ_CPU : 10UF/6.3V/0603 *6
1UF/6.3V/0402 * 4

Security Classification	Compal Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SKL-U(8/12)Power			
Size: Custom	Document Number: LA-D707P		Rev: v0.2
Date: Wednesday, May 11, 2016	Sheet 12 of 60		



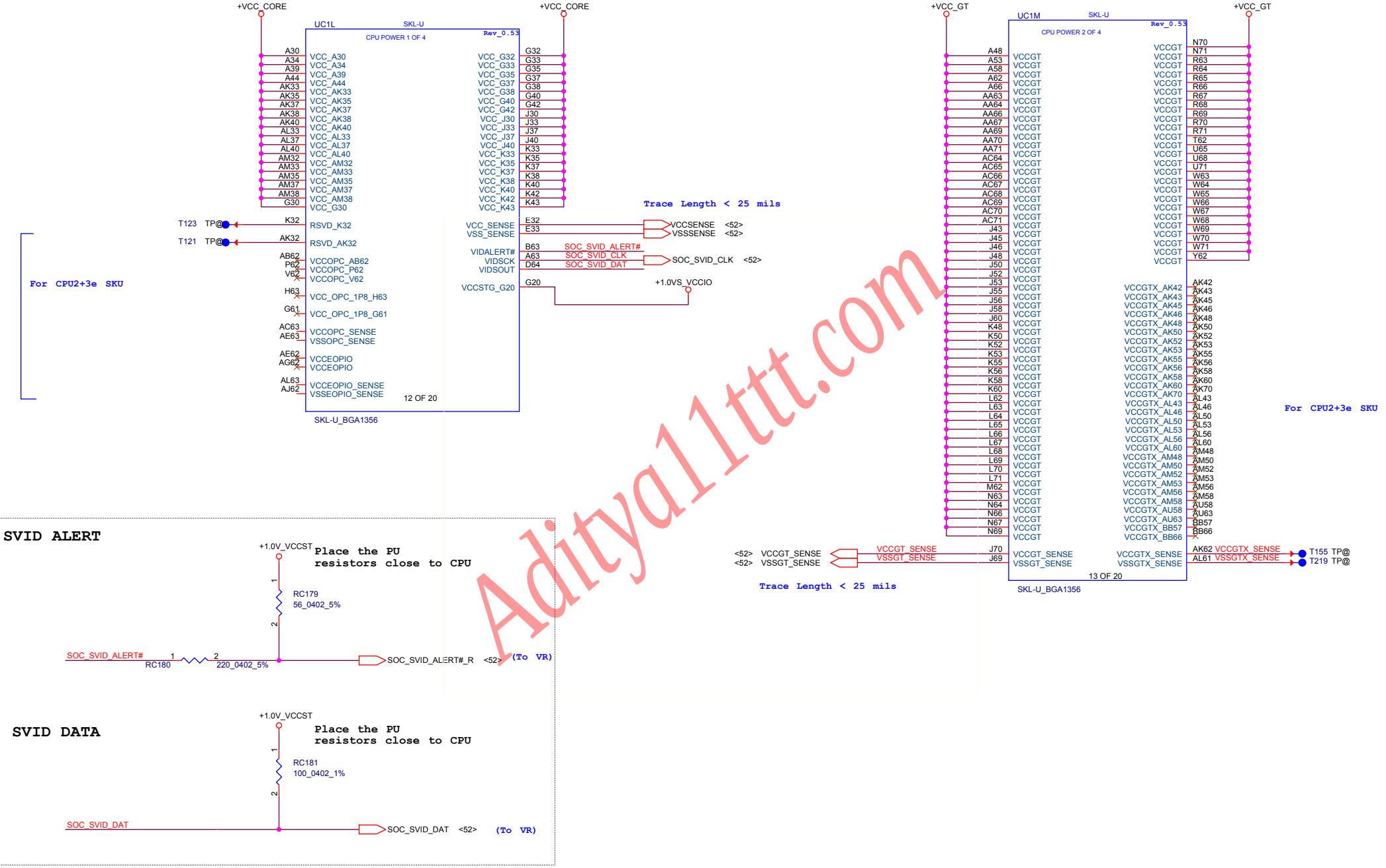
Security Classification	Compal Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(9/12)Power

Size	Document Number	Rev
Custom	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 | Sheet 13 of 60



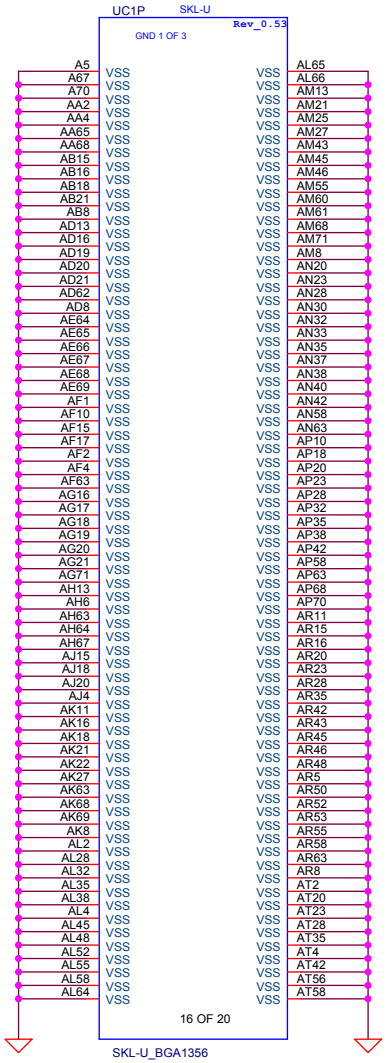
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

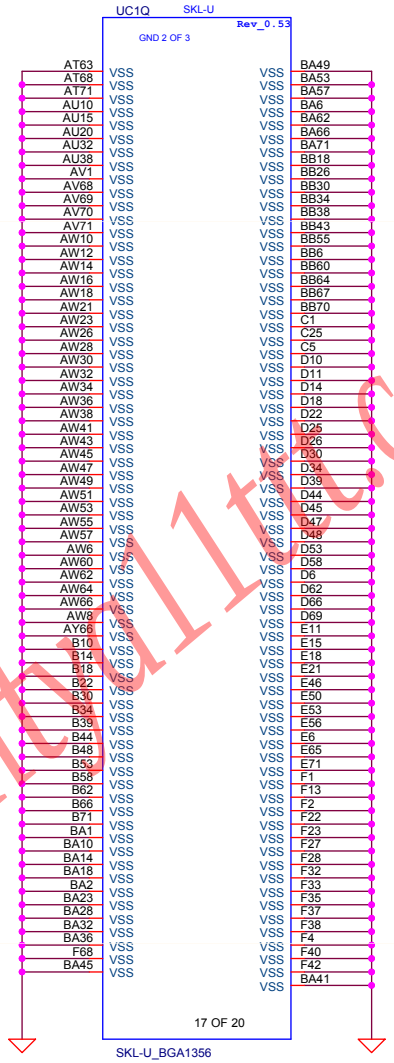
Compal Electronics, Inc.

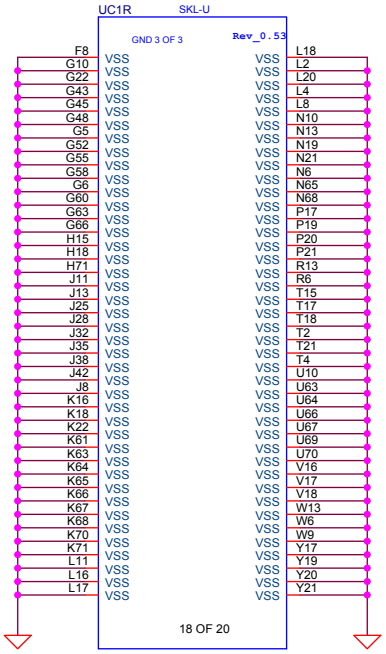
Title: SKL-U(10/12)Power,SVID

Size	Document Number	Rev
Custom	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 14 of 60







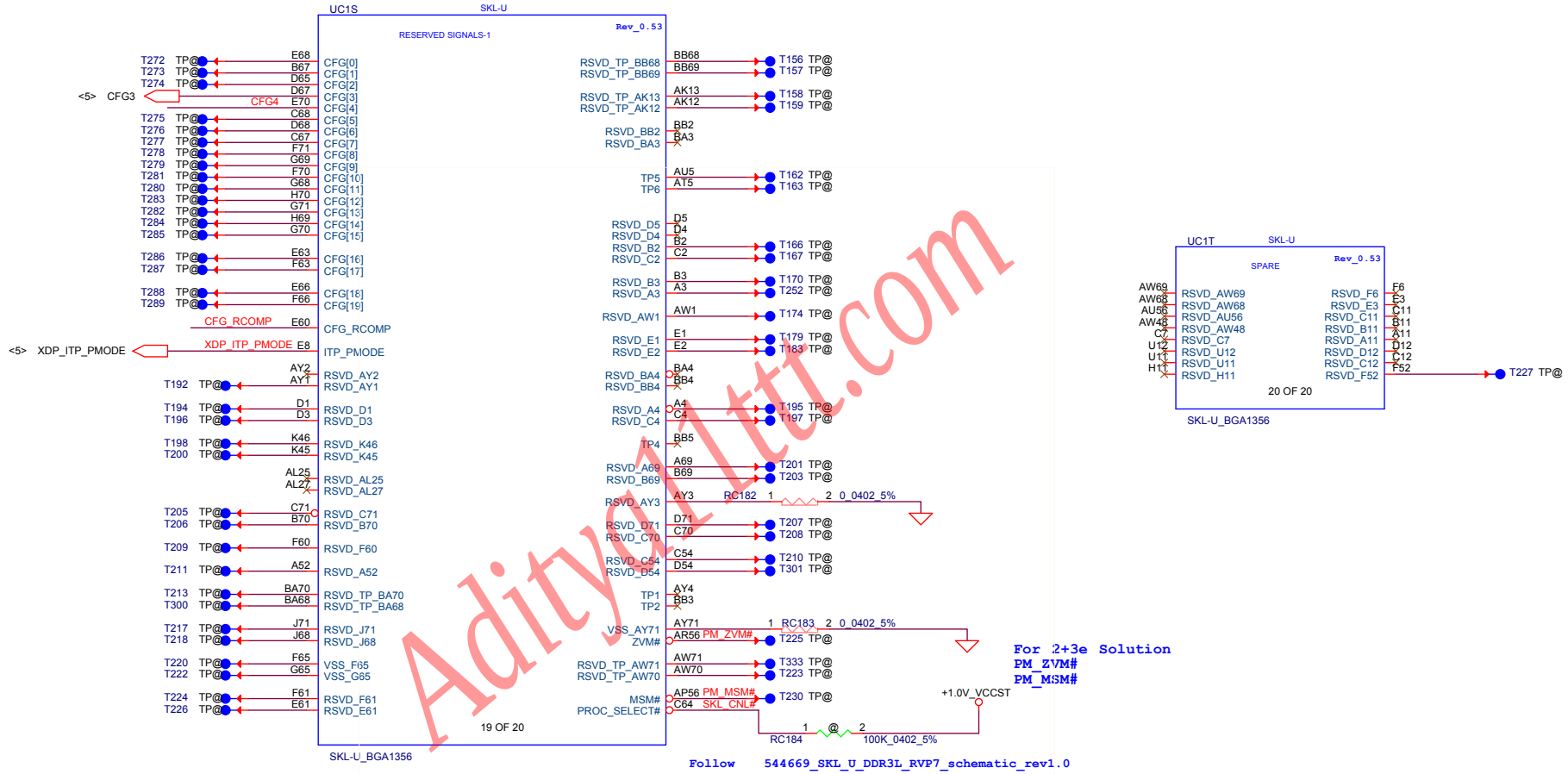
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size	Document Number	Rev
Custom	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 15 of 60



CFG_RCOMP — RC185 — 49.9_0402_1%

CFG4 — RC193 — 1K_0402_1%

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size: Custom | Document Number: LA-D707P | Rev: v0.2

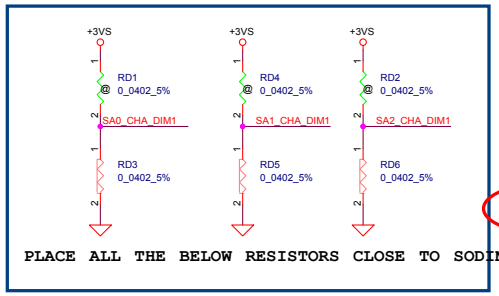
Date: Wednesday, May 11, 2016 | Sheet 16 of 60

CHANNEL-A

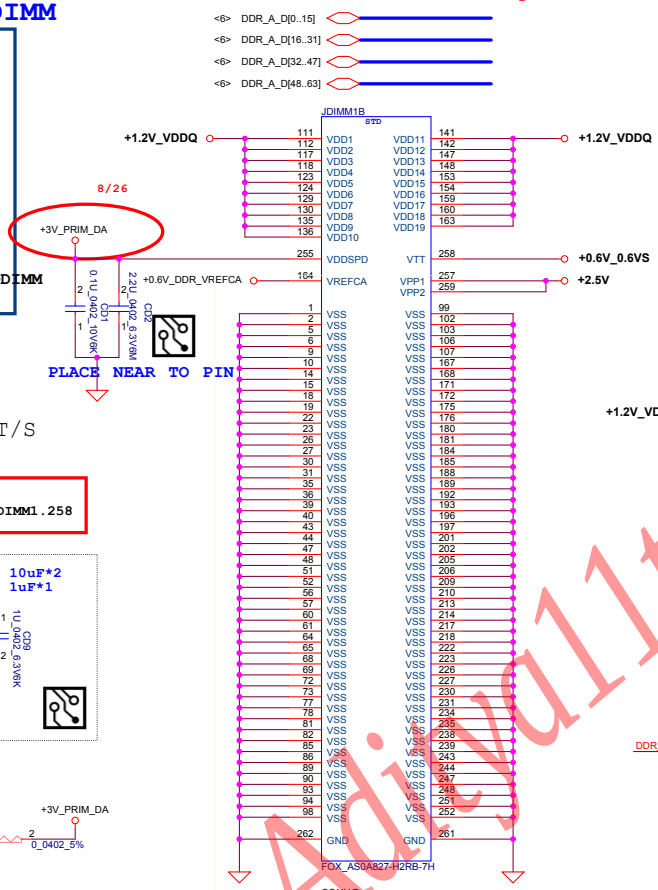
REVERSE TYPE (5.2 mm)

Interleaved Memory

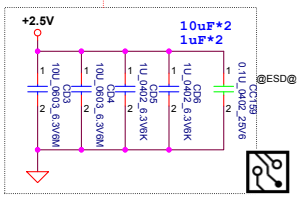
TOP: JDIMM1 CONN Non-ECC DIMM



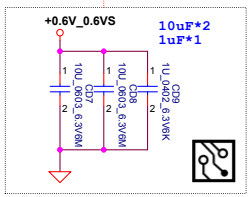
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



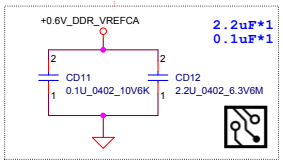
Layout Note:
Place near JDIMM1.257,259



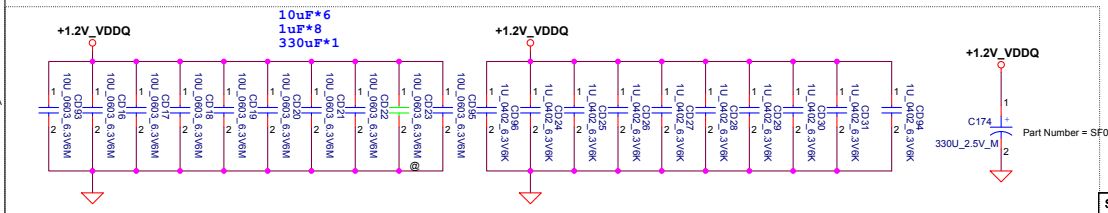
Layout Note:
Place near JDIMM1.258

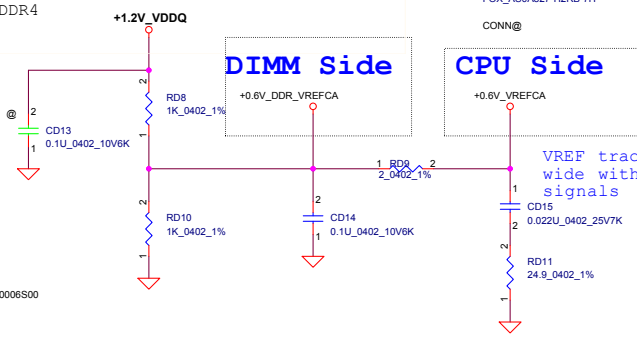


Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1





Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

Security Classification	Compal Secret Data		
Issued Date	2015/08/03	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: P18-DDRIV_CHA: DIMM0

Size | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 17 of 60

CHANNEL-B

TOP: JDIMM2 CONN Non-ECC DIMM

Interleaved Memory

STD (5.2 mm)

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.258

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

Layout Note:
Place near JDIMM2

PLACE NEAR TO PIN

PLACE NEAR TO SODIMM

For ECC DIMM

Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Security Classification	Compal Secret Data		
Issued Date	2015/08/03	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: P19-DDRIV_CHB: DIMM0

Size: | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 18 of 60

<5,6,7,9,10,11,13,17,18,20,21,22,23,24,26,28,32,33,34,35,36,37,38,52,55,56> +3VS +3VS

<CPU CTRL>

<5> EDP_HPD EDP_HPD

RT11 100K_0402_5%

RTD2132 SMBus revrse to PCH

<7,10,22,26,37> EC_SMB_CK2 RT193 1 2 0_0201_5% CIICSCL1
<7,10,22,26,37> EC_SMB_DA2 RT194 1 2 0_0201_5% CIICSDA1
<7,17,18,22> PCH_SMBCLK RT1951 @ 2 0_0201_5%
<7,17,18,22> PCH_SMBDATA RT1961 @ 2 0_0201_5%

Layout notes
CC97~CC102 must closed to connector

<CPU>

<5> EDP_CPU_AUX_C CT102 1 2 .1U_0402_16V7K EDP_CPU_AUX
<5> EDP_CPU_AUX#_C CT101 1 2 .1U_0402_16V7K EDP_CPU_AUX#
<5> EDP_CPU_LANE_P0_C CT98 1 2 .1U_0402_16V7K EDP_CPU_LANE_P0
<5> EDP_CPU_LANE_N0_C CT97 1 2 .1U_0402_16V7K EDP_CPU_LANE_N0
<5> EDP_CPU_LANE_P1_C CT103 1 2 .1U_0402_16V7K EDP_CPU_LANE_P1
<5> EDP_CPU_LANE_N1_C CT100 1 2 .1U_0402_16V7K EDP_CPU_LANE_N1
eDP@

DB phase :
add eDP Lan1 for FHD
20141117

EDP_HPD RT34 1 2 0_0201_5% EDP_HPD_PANEL EDP_HPD_PANEL <20>
Delete BKL_PWM_CPU and DP_INT_PWM
20141113

<CPU by PASS eDP>

0_0804_8P4R_5%
EDP_CPU_LANE_N0 1 8 EDP_LANE_N0
EDP_CPU_LANE_P0 2 7 EDP_LANE_P0
EDP_CPU_AUX 3 6 EDP_AUX
EDP_CPU_AUX# 4 5 EDP_AUX#
RP6 eDP@ SD309000080
2

<eDP to connector>

RP9 eDP@ SD309000080
EDP_AUX 4 5 LCD_CLK
EDP_AUX# 3 6 LCD_DATA
EDP_LANE_N0 2 7 LVDS_TXN2_LN0
EDP_LANE_P0 1 8 LVDS_TXP2_LP0
0_0804_8P4R_5%
4

LCD_CLK <20>
LCD_DATA <20>
LVDS_TXN2_LN0 <20>
LVDS_TXP2_LP0 <20>

Layout notes
RP6 RP9 RP10 must closed to connector

EDP_CPU_LANE_P1 RT16 1 2 0_0402_5% LVDS_TXP1_LP1 LVDS_TXP1_LP1 <20>
EDP_CPU_LANE_N1 RT17 1 2 0_0402_5% LVDS_TXN1_LN1 LVDS_TXN1_LN1 <20>

<RTS2132>
<EC CTRL>

<26> EC_BKOFF#

RT14 1 @ 2 0_0402_5%
CT24
+3VS 1 2 @ 0.1U_0402_16V7K
UT3
TS_BKOFF#
EC_BKOFF#
B A Y
LVDS@ TC7SH08FUF_SSOP5
RT12 100K_0402_5% LVDS@
RT15 1 2 0_0402_5%

EC_TS_BKOFF# <20>

<LVDS Panel>

PD 100K on LVDS page

DB phase :
add eDP Lan1 for FHD
20141117

Layout notes
RT16~RT19 must closed to connector

Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

Compal Electronics, Inc.

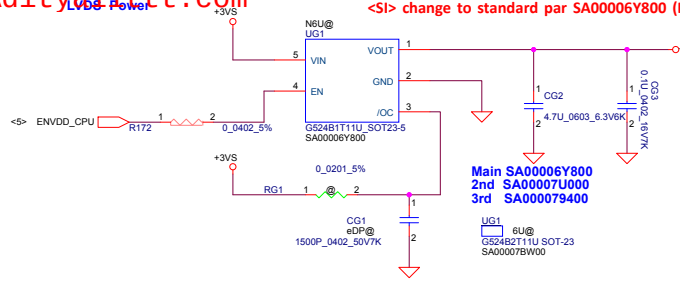
Title: LVDS Translator-RTD2132N

Size: Document Number: LA-D707P Rev: v0.2

Date: Wednesday, May 11, 2016 Sheet 19 of 60

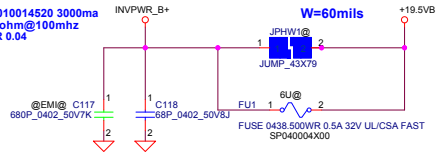
LVDS Power

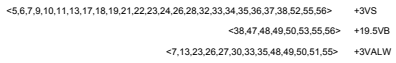
<SI> change to standard par SA00006Y800 (Different footprint)



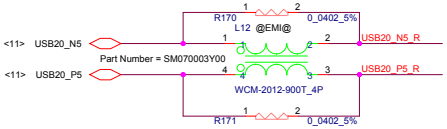
W=60mils

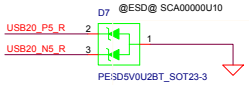
SM010014520 3000ma
220ohm@100mhz
DCR 0.04



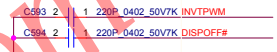


Camera

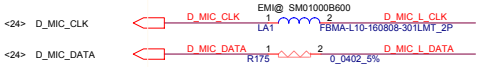


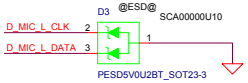


LCD/LED PANEL Conn.



<DB>LA1/LA2 closed to Aduio codec

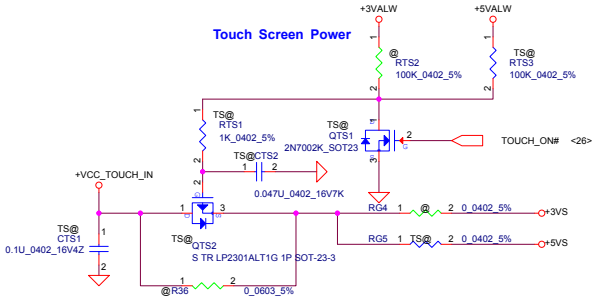


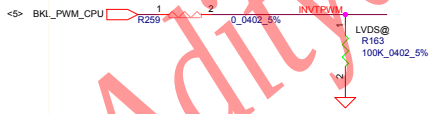


Touch Screen

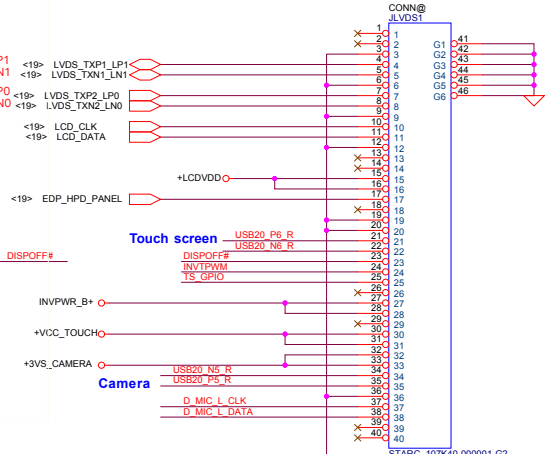
<DB> for 5V/3V TS option

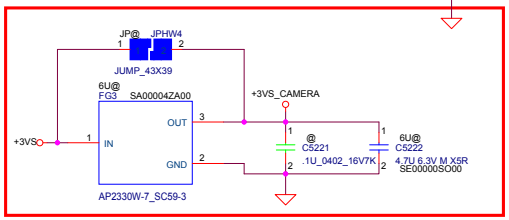
Touch Screen Power

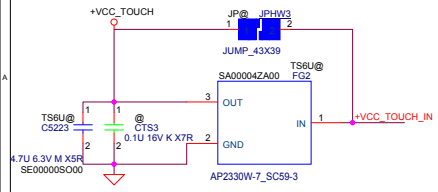


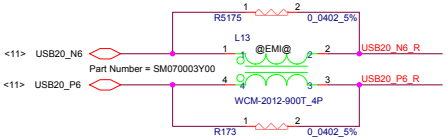


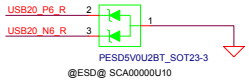
<PV> Touch GPIO control by EC











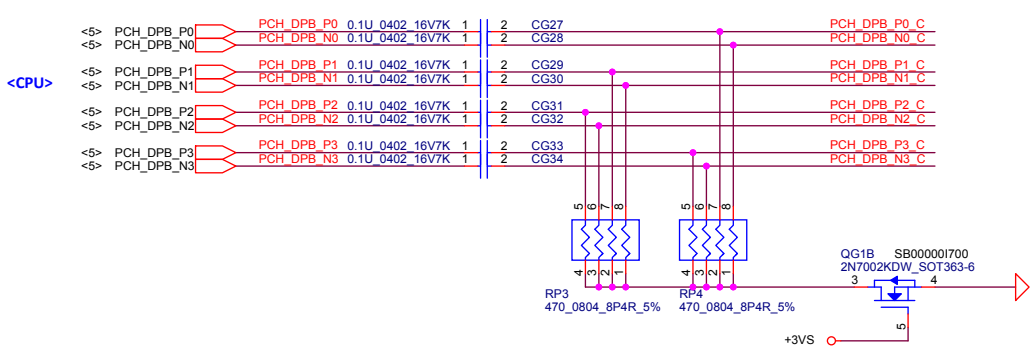
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

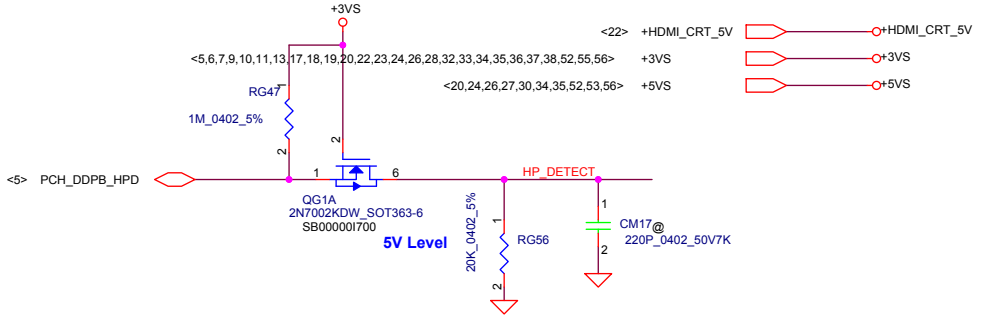
Compal Electronics, Inc.

Title: LVDS Connector

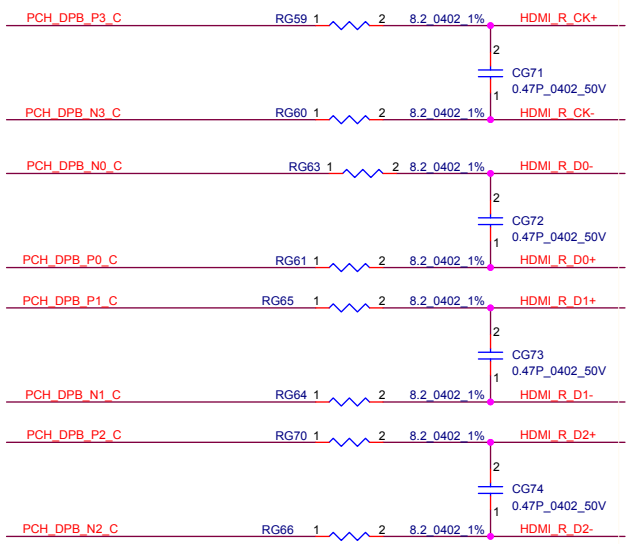
Size	Document Number	Rev
	LA-C707P	v0.2

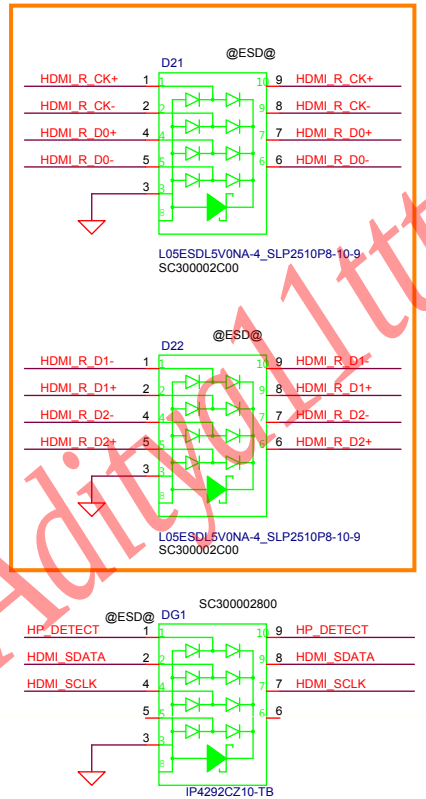
Date: Wednesday, May 11, 2016 | Sheet 20 of 60



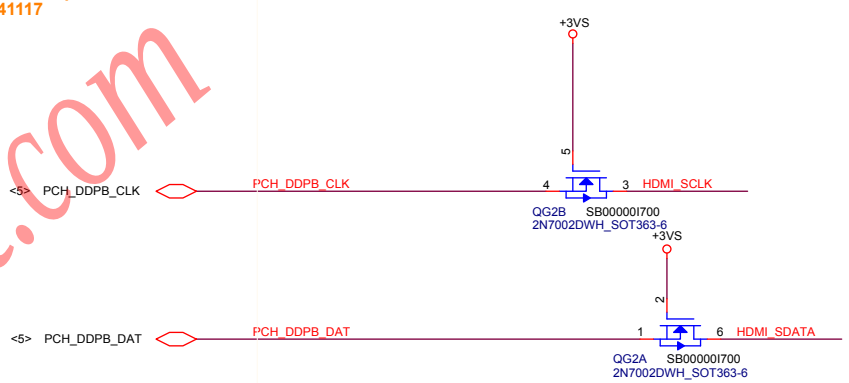


<Diner SI> change to 8.2 ohm and parallel 0.47p by EMI request
<PV> change to 10 ohm by EMI request
<DB> Delete Choke add parallel 150ohm

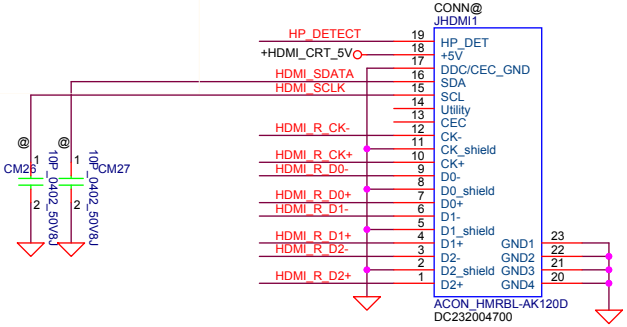




DB phase :
For ESD request
20141117



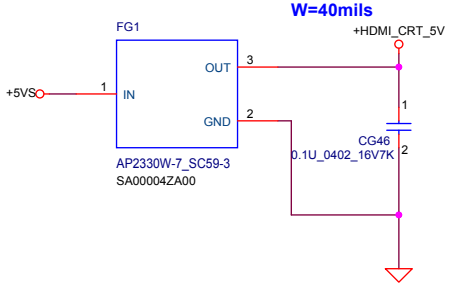
HDMI Conn.



HDMI Chock 2nd : SM070003K00

Layout notes
40 mils

W=40mils



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **HDMI Conn/Level shift**

Size	Document Number	Rev
	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 21 of 60

DP to CRT converter

<20,21,24,26,27,30,34,35,52,53,56> +5VS
<5,6,7,9,10,11,13,17,18,19,20,21,23,24,26,28,32,33,34,35,36,37,38,52,55,56> +3VS
<21> +HDMI_CRT_5V

For Power consumption Measurement

JUMP_43X39

<PV> change short pad

R34 2_0_0603_5%

<SI> change to +HDMI_CRT_5V for SVTP test fail

U4104 RTD2168-CG_QFN32

Part Number = SA000077U00

<KBL SI> Change ESD diode package
D4&D5 Only Pop for 6U SKU Indie Country

Layout notes
R61,R62,R58,R59 close to RTD2168
R55,R57,R60,R56 close to CONN

Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

Mode Configure Table(Power On Latch)

	POL1_SDA(PIN22)	
	0	1
POL2_SCL(PIN23) 0	X	EP MODE
POL2_SCL(PIN23) 1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

50 impedance

CRT Connector

W=40mils

Security Classification	Compal Secret Data
Issued Date	2014/02/18
Deciphered Date	2015/02/20

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Compal Electronics, Inc.

Title: DP to CRT RTD2168

Size: Custom | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 22 of 60

+LAN_VDD_3V3 Rising time
need>0.5mS and <100mS

8/15 Change to LDO Mode

	LDO mode	Switcing mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8,CL23	@	SMT

CL13 & CL15 close UL1 Pin22
CL14 & CL27 close UL1 Pin30

Place CL11~CL12 close UL1 Pin 3,8

LL2, CL8, CL23 for 8161
CL8 & CL18 close LL2

8151/8166 Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

0923 PV CNG from DP00 to E500

CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

CL10& CL16 close to UL1: Pin 23

EC control 08/17 Add 0ohm

SP050005L00 Footprint

Swap P/N 08/16

2016-03-03:Change Single Source
(SP050008V00) 10/100
(SP050008Y00) Giga

(SA000063500) 8166GSH 10/100
(SA000084T00) 8111HSH-CG Giga

11/18 modify vendor review results

11/15 change CONN.

11/17 reserver for ESD request

powe rail need to check

powe rail need to check

CR RTS5237S move to S/B

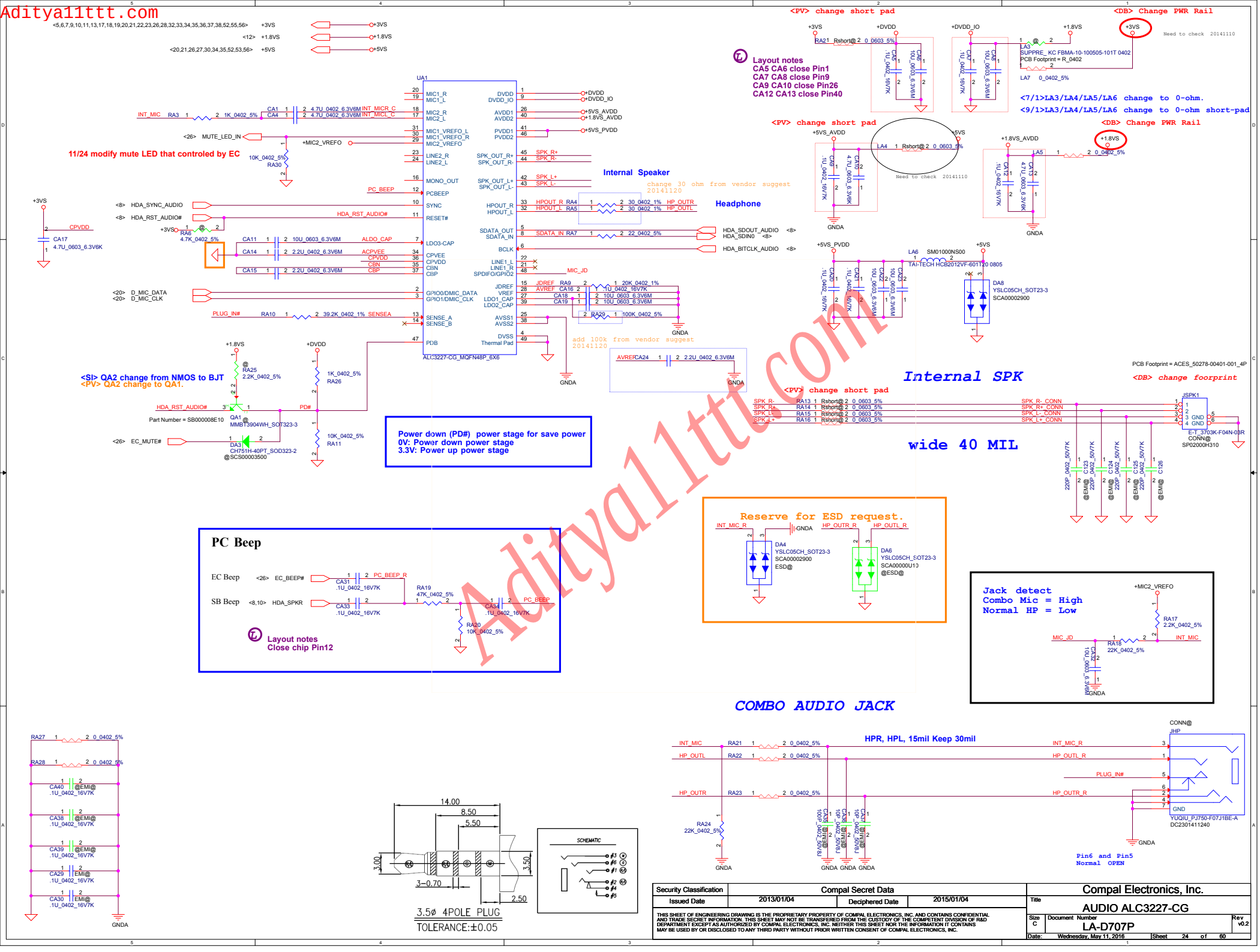
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: LAN 8151/8166_CR RTS5238

Size	Document Number	Rev
	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 | Sheet 23 of 60



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Compal Electronics, Inc.

Title: AUDIO ALC3227-CG

Size	Document Number	Rev
C	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 | Sheet 24 of 60

WIN 7 Debug Solution

Option 1 : For Closed Chassis Platforms

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 | Sheet 25 of 60

EC Board ID (UMA, Dis, phase) control table

RK4	DB	SI	PV	MV	Note
UMA	15Kohm	27Kohm	43Kohm	75Kohm	
Dis	20Kohm	33Kohm	56Kohm	100Kohm	

Current

DB_UMA_15kohm:SD034150280, S RES 1/16W 15K +-1% 0402
DB_DIS_20kohm:SD034200280, S RES 1/16W 20K +-1% 0402
SI_UMA_27kohm:SD034270280, S RES 1/16W 27K +-1% 0402
SI_DIS_33kohm:SD034330280, S RES 1/16W 33K +-1% 0402
PV_UMA_43kohm:SD034430280, S RES 1/16W 43K +-1% 0402
PV_DIS_56kohm:SD034560280, S RES 1/16W 56K +-1% 0402
MV_UMA_75kohm:SD034750280, S RES 1/16W 75K +-1% 0402
MV_DIS_100kohm:SD034100380, S RES 1/16W 100K +-1% 0402

<PV> change short pad

<SI> un-mount RC , Internal PU in 9022

Board ID control

Reserve EC_CLR_CMOS for clear CMOS
(2016-03-04 : Confirm intel platform not support EC Clear CMOS function)

<SI> EC request to add RK9

<DB> for leakage of LED light

For Solve tPCH04(Min 9ms) Sequence Timing

CC128 RC369 place near EC Side

EMI request

UK1 KB9022QD_LQFP128_14X14

20mil

2014-11-25
Reserve for co-lay Nuvoton NPCE388N

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: EC ENE-KB9022

Size: Custom | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 26 of 60

<7,13,20,23,26,30,33,35,48,49,50,51,55> +3VALW
<12,13,20,30,31,33,35,38,48,49> +5VALW

+3VALW
+5VALW

TP Button BD Connector

<26> TP_CLK
<26> TP_DATA
<7> TP_SMBCLK
<7> TP_SMBDATA

PS2+SMBus

DM5
YSLC05CH_SOT23-3
SCA00000U10
ESD@

C135 470P_0402_50V8J @
C136 470P_0402_50V8J @

<SI> add 470p for EMI issue

CONN@
JTP1
JXT_FP202DH-006M10M
SP01001YK00

Keyboard conn

<26> KSI[0..7]
KSI7 KSI6 KSI5 KSI4 KSI3 KSI2 KSI1 KSI0

<26> KSO[0..17]
KSO17 KSO16 KSO15 KSO14 KSO13 KSO12 KSO11 KSO10 KSO9 KSO8 KSO7 KSO6 KSO5 KSO4 KSO3 KSO2 KSO1 KSO0

JKB1
KSI1 1
KSI7 2
KSI6 3
KSO9 4
KSI4 5
KSI5 6
KSO0 7
KSI2 8
KSI3 9
KSO5 10
KSO1 11
KSI0 12
KSO2 13
KSO4 14
KSO7 15
KSO8 16
KSO6 17
KSO3 18
KSO12 19
KSO13 20
KSO14 21
KSO11 22
KSO10 23
KSO15 24
KSO16 25
KSO17 26
27
CAP_LOCK# 28
MUTE_LED_OUT 29
WLAN_OFF_LED# 30
WLAN_ON_LED# 31
32
G1 33
G2 34

ACES_50690-0320N-P01
CONN@ SP01001RG00

<26> CAP_LOCK#
<26> MUTE_LED_OUT
CAP_LOCK# R203 1 2 3.3K_0402_5%
R207 1 2 3.3K_0402_5%
+5VS

CAP_LOCK#
MUTE_LED_OUT
CC122 100P_0402_50V8J ESD@
CC123 100P_0402_50V8J ESD@

+5VALW
+5VALW
@EMI@ C134 470P_0402_50V8J
Amber
White
R157 3.3K_0402_5%
R158 3.3K_0402_5%
<26> WLAN_OFF_LED#
WLAN_ON_LED# <26>

2014-11-24
BOM control

KSI0 C193 ESD@ 100P_0402_50V8J

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: KB/TP

Size	Document Number	Rev
B	LA-D707P	v0.2

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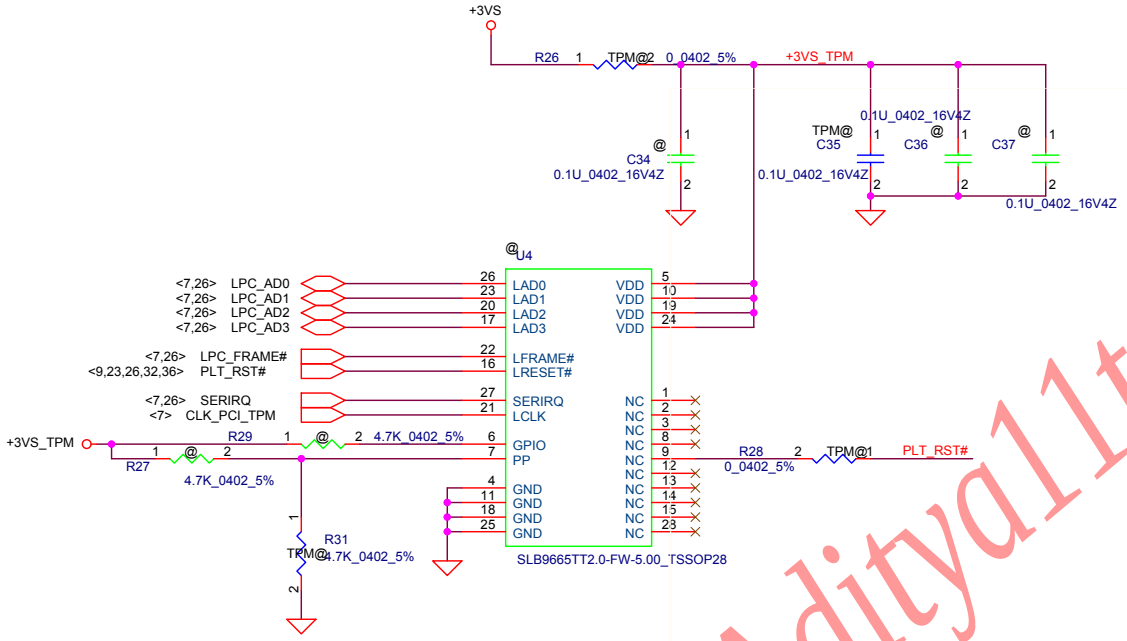
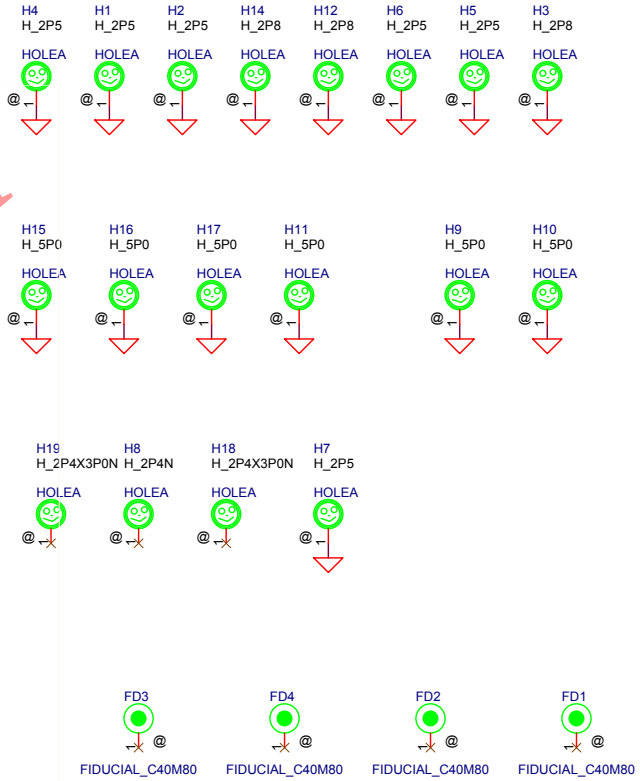
TPM2.0



SLB9665 (SA00007XU00)-->TPM2.0
SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: TPM/Screw

Size	Document Number	Rev
	LA-D707P	v0.2

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BOM control

Plat f or m	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	GCLKUMA@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	GCLKPX@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

Security Classification	Compal Secret Data		
Issued Date	2013/06/10	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title: GCLK

Size | Document Number: LA-D707P | Rev: v0.2

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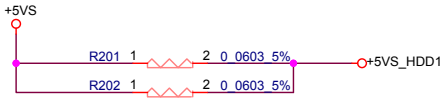
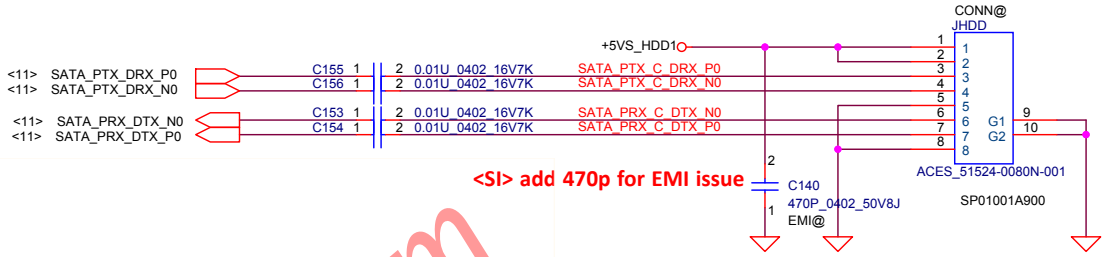
2.5" SATA HDD

<20,21,24,26,27,34,35,52,53,56> +5VS
<12,13,20,27,31,33,35,38,48,49> +5VALW
<7,13,20,23,26,27,33,35,48,49,50,51,55> +3VALW
<32> +3VS_WLAN_R

<PV> change short pad

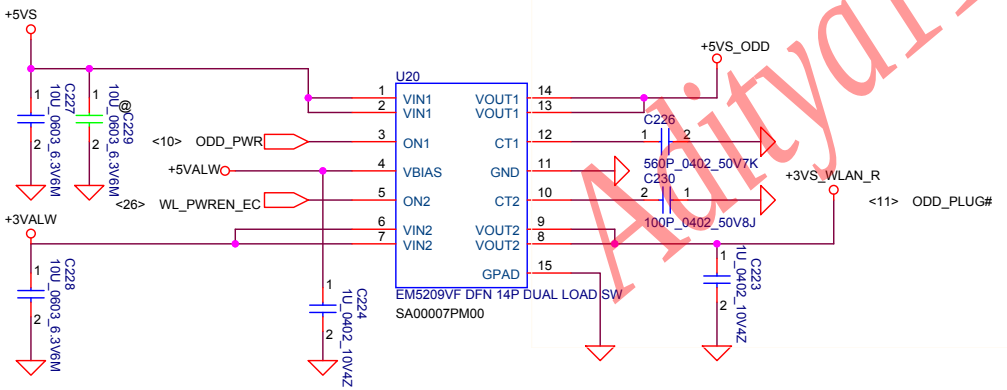


<DB> change JHDD pin define

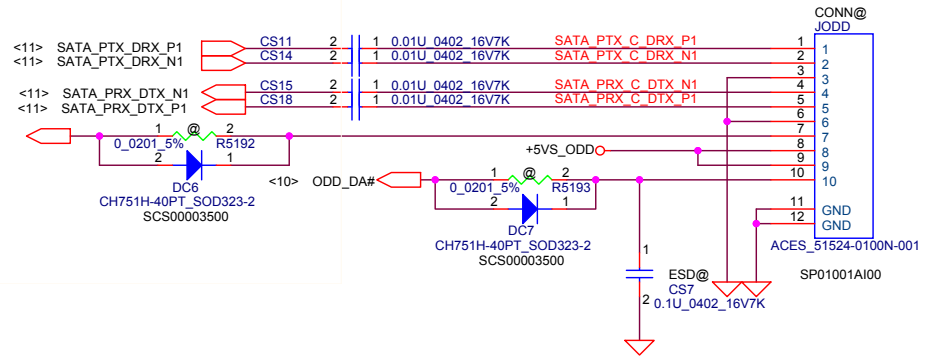


<SI> add 470p for EMI issue

2.5" SATA ODD



<11> ODD_PLUG#



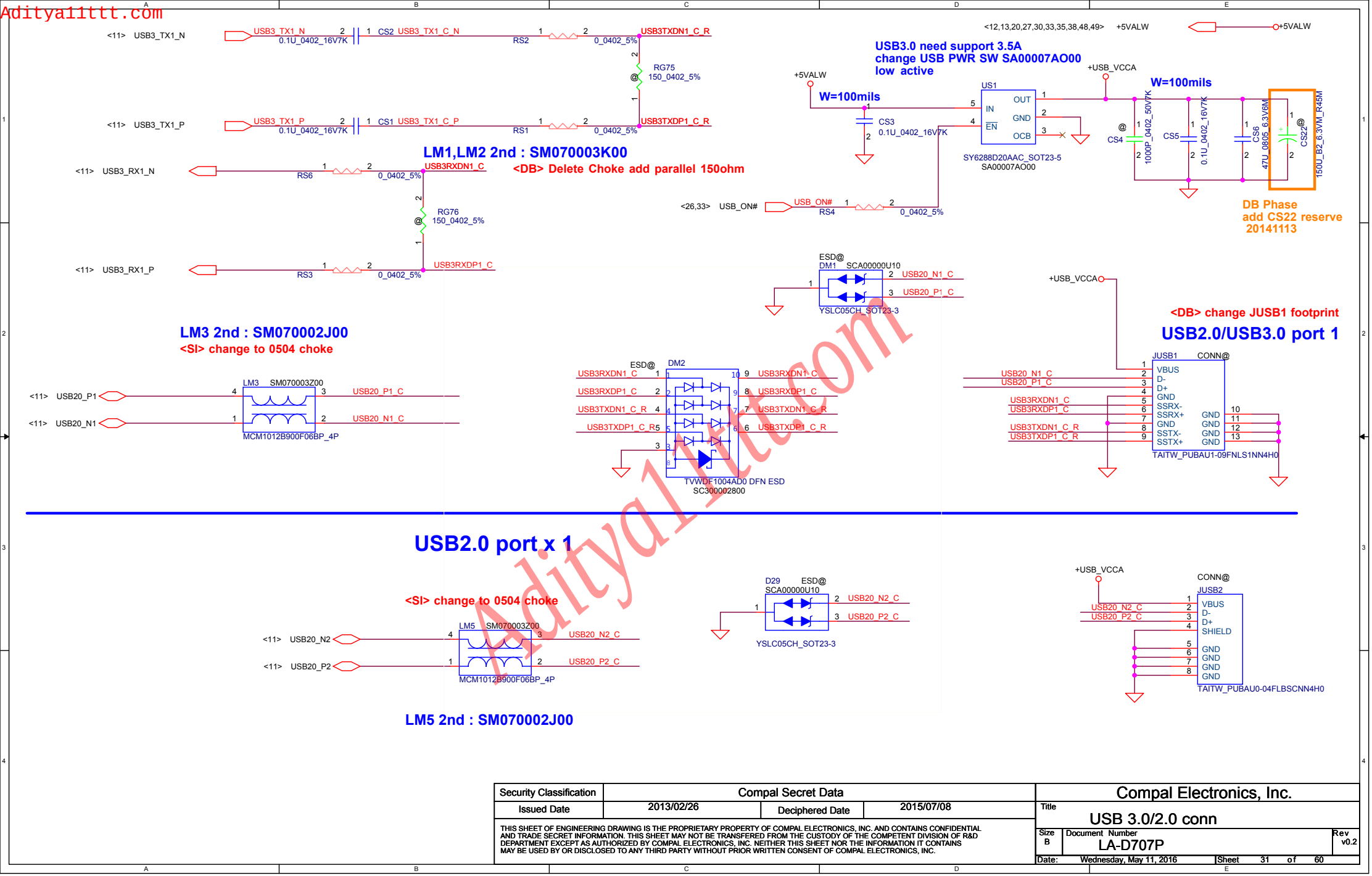
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: HDD/ODD Conn

Size	Document Number	Rev
B	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 | Sheet 30 of 60



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

Size	Document Number	Rev
B	LA-D707P	v0.2

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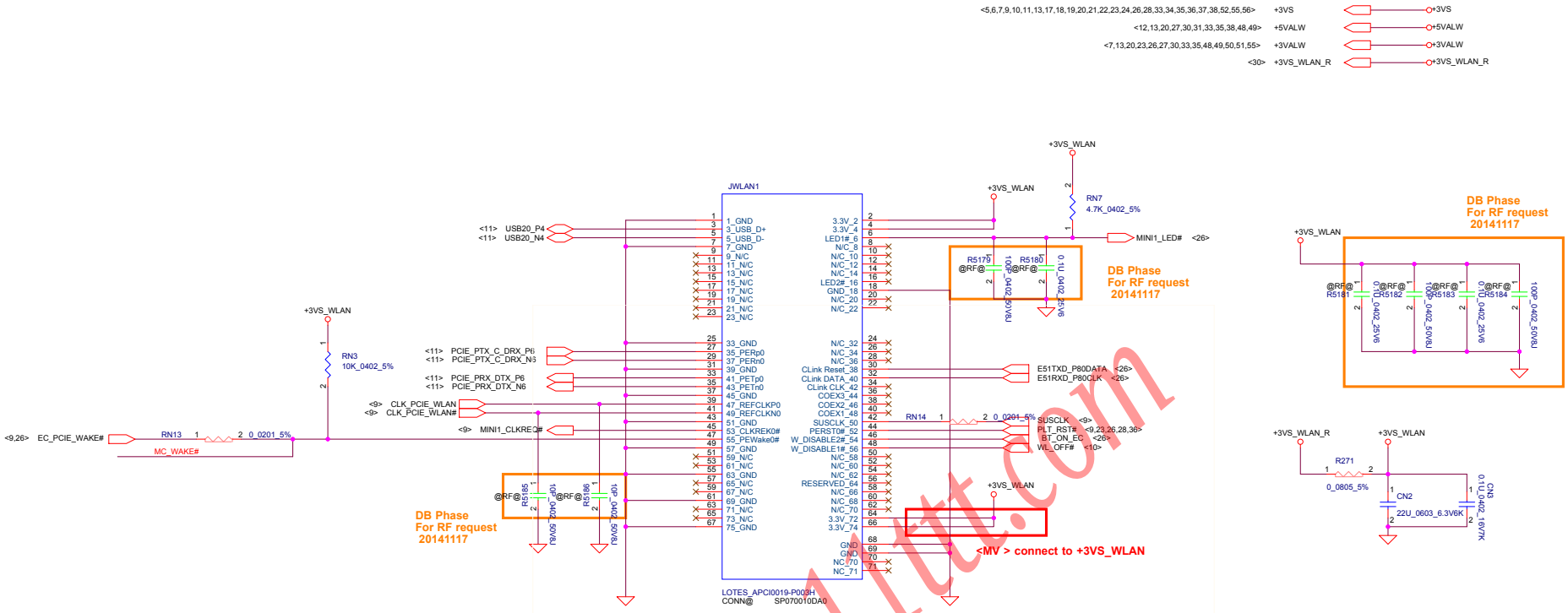
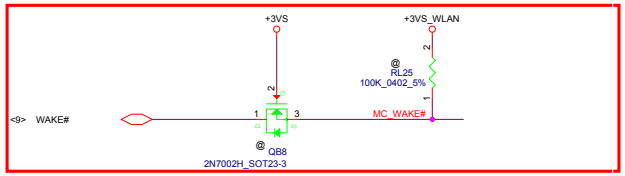


NGFF and WLAN



Unpop QB4 and RL23 for not support OBFF

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: **WLAN-BT**

Size	Document Number	Rev
	LA-D707P	v0.2

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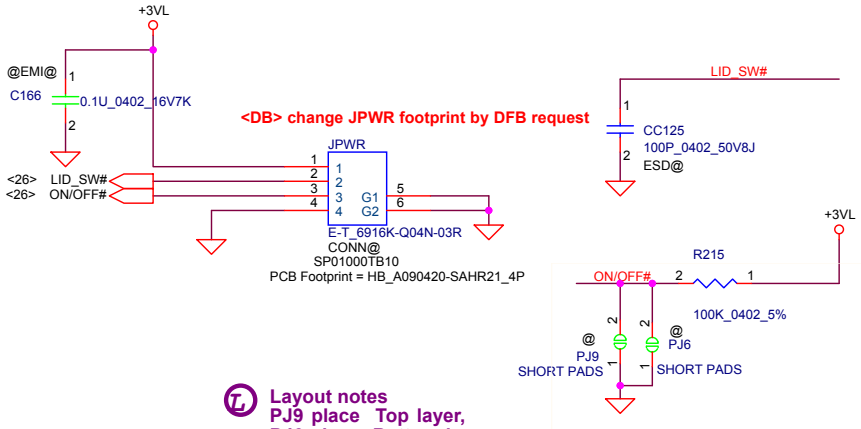
Powert Button Connector



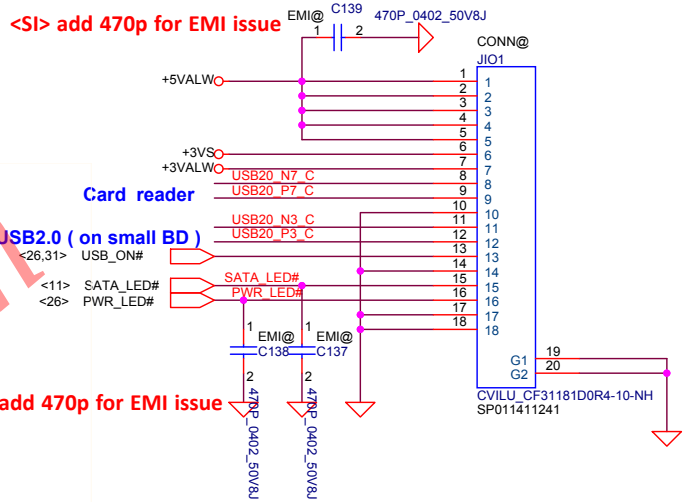
Layout notes
PJ9 place Top layer,
PJ6 place Bottom layer

<13,26,46,47,48> +3VL
<12,13,20,27,30,31,35,38,48,49> +5VALW
<5,6,7,9,10,11,13,17,18,19,20,21,22,23,24,26,28,32,34,35,36,37,38,52,55,56> +3VS
<7,13,20,23,26,27,30,35,48,49,50,51,55> +3VALW

11/26 change CONN.

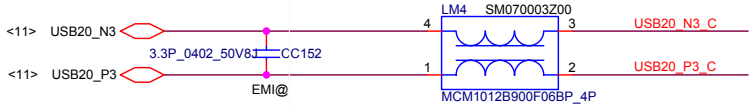
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)

<SI> add 470p for EMI issue



DB phase :
modify pin define
20141114

<SI> add 470p for EMI issue



<MV> add AC cap

<SI> change to 0504 choke

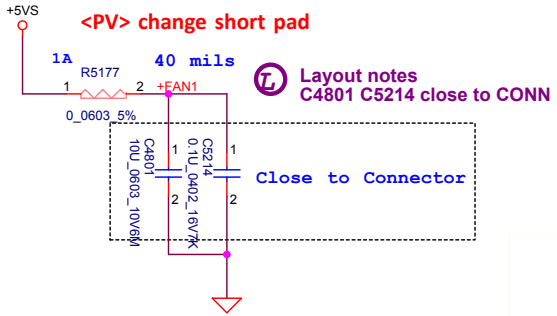
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

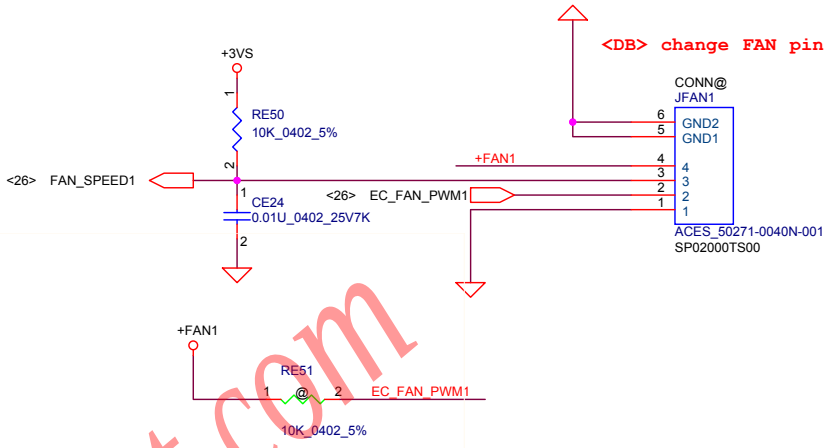
Compal Electronics, Inc.

Title	IO CON	
Size B	Document Number LA-D707P	Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 33 of 60	

<5,6,7,9,10,11,13,17,18,19,20,21,22,23,24,26,28,32,33,35,36,37,38,52,55,56> +3VS +3VS

<20,21,24,26,27,30,35,52,53,56> +5VS +5VS





Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FAN

Size	Document Number	Rev
B	LA-D707P	v0.2

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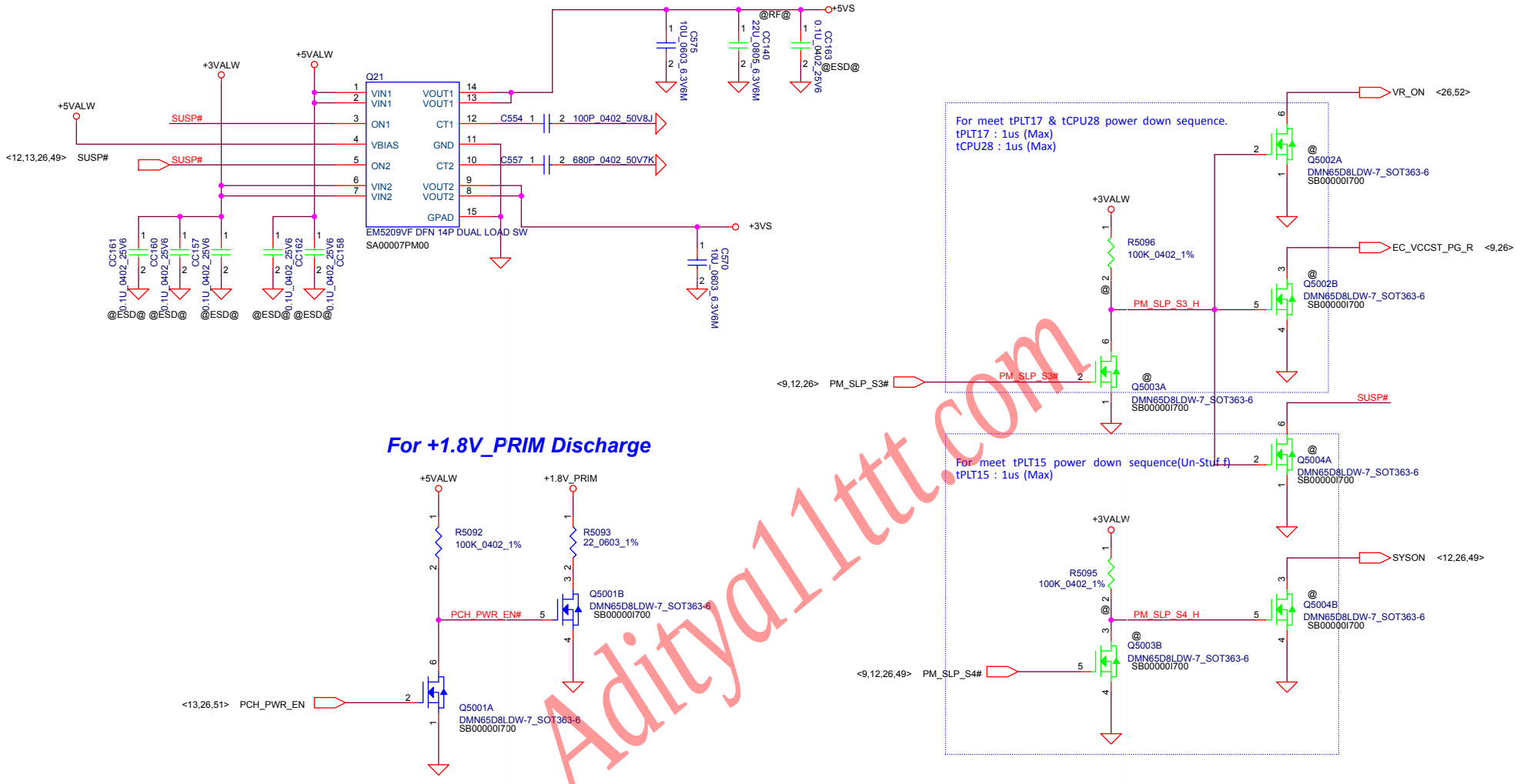

For +1.8V_PRIM Discharge

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: DC Interface

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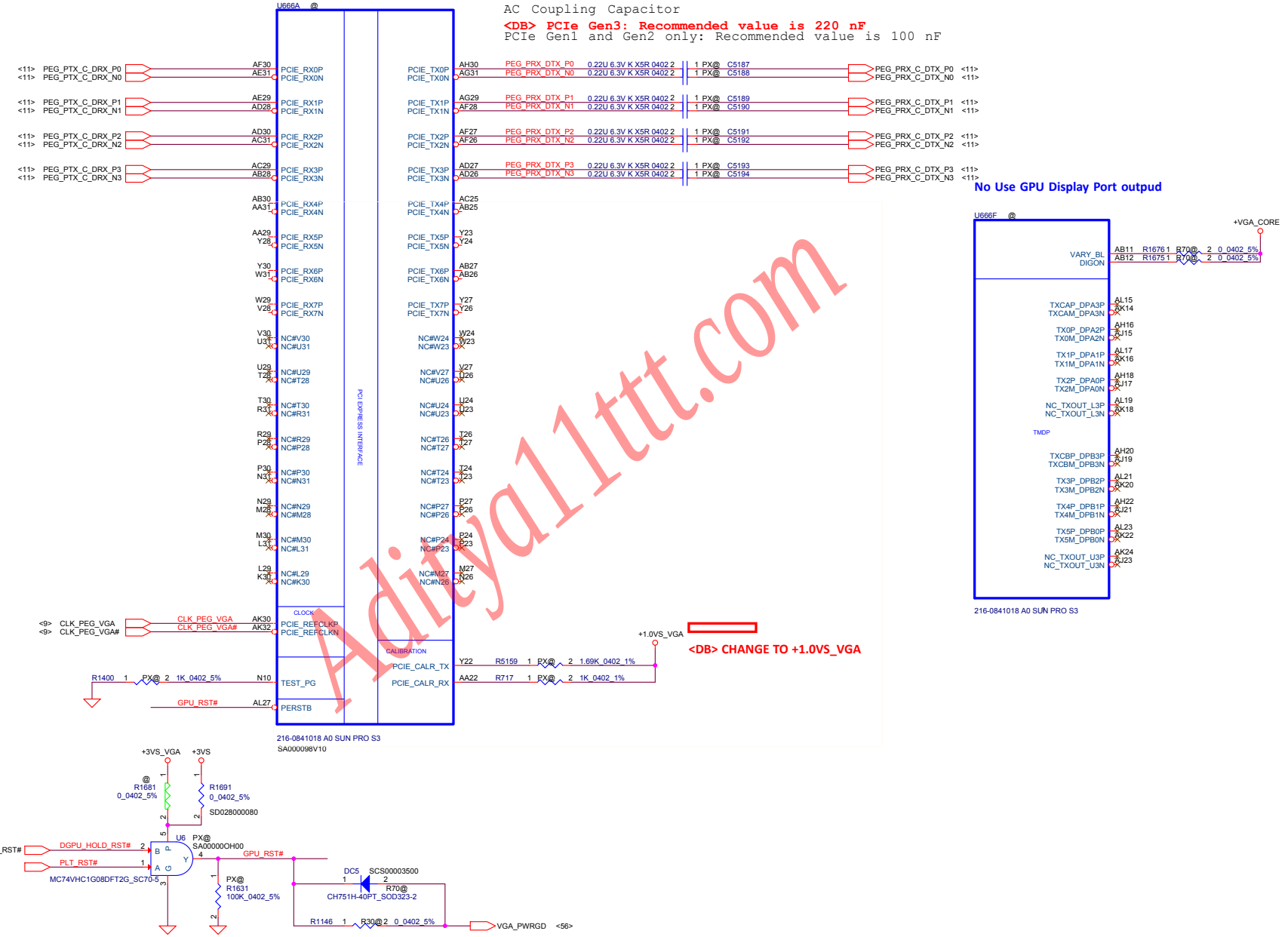
AC Coupling Capacitor

<DB> PCIe Gen3: Recommended value is 220 nF

PCIe Gen1 and Gen2 only: Recommended value is 100 nF



No Use GPU Display Port outpud

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **SUN_PCIE/DP**

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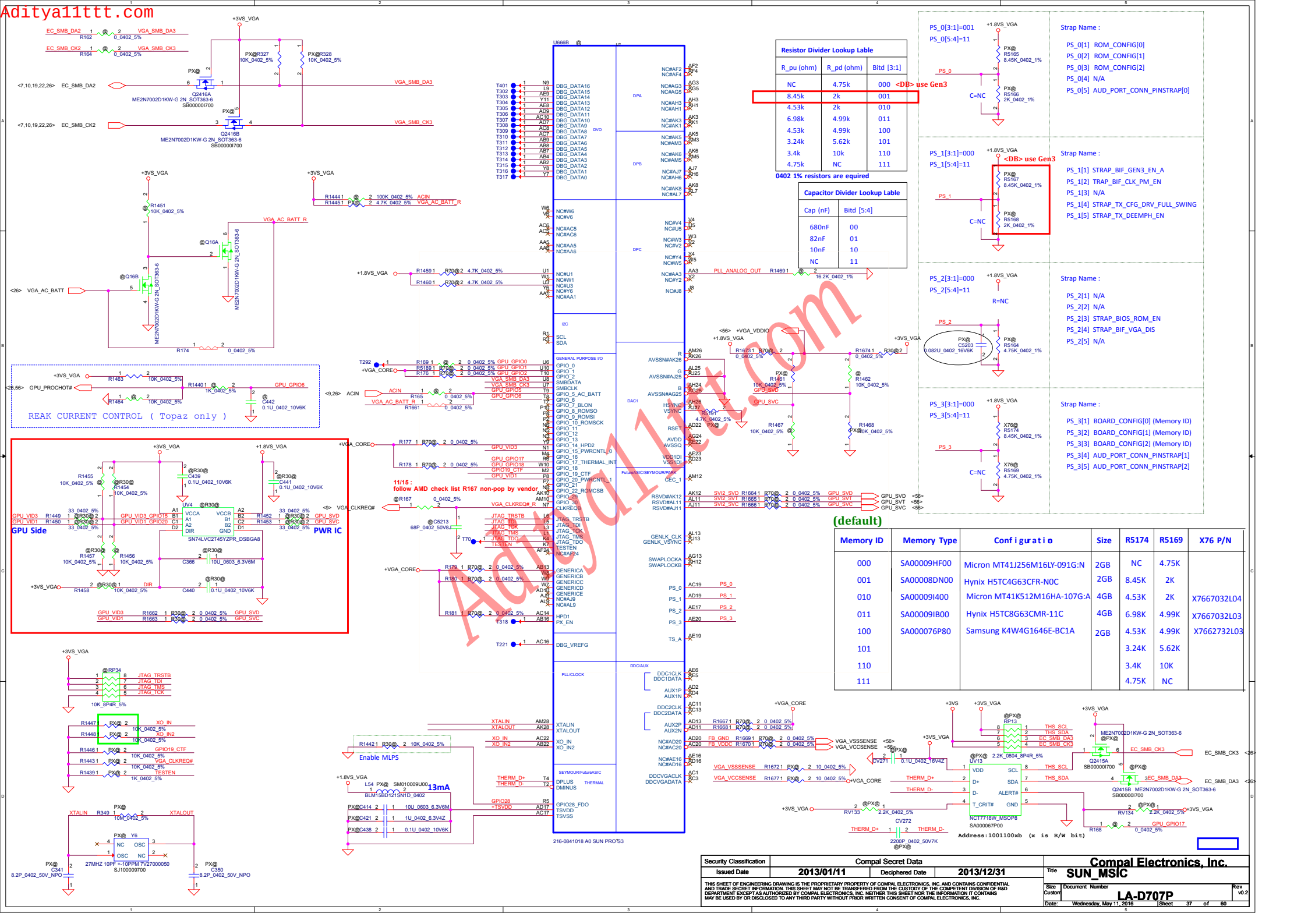
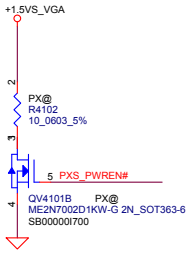


+1.5VS to +1.5VS_VGA (2.096A)

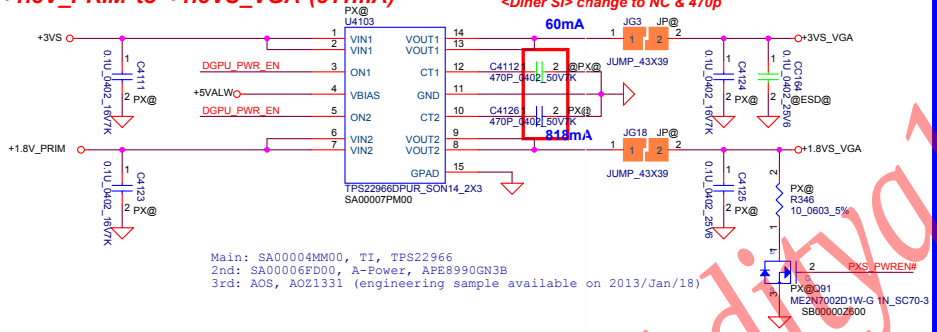
Delete +1.5VS to +1.5VS_VGA power switch



+3VS to +3VS_VGA (25mA)

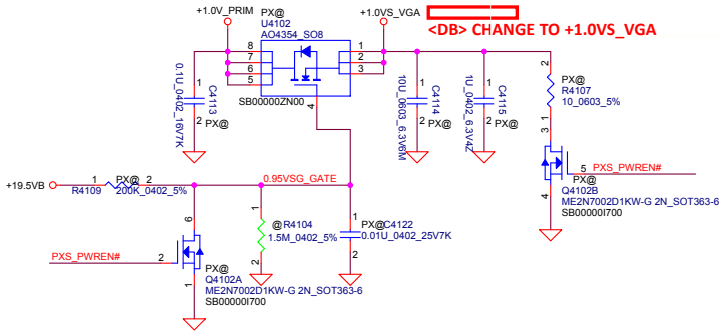
+1.8V_PRIM to +1.8VS_VGA (311mA)

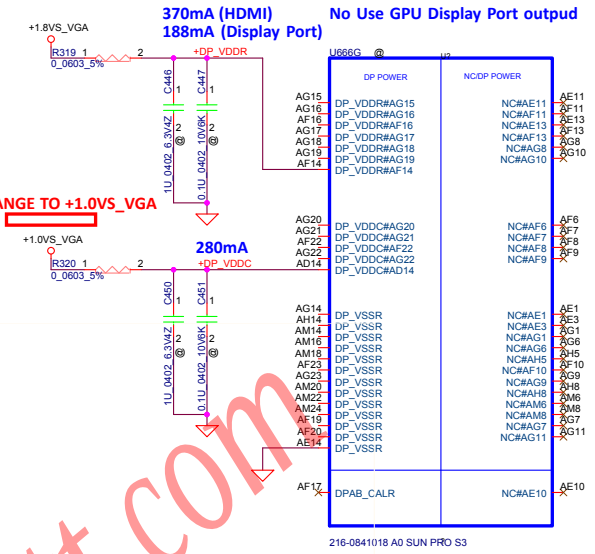
<Diner SI> change to NC & 470p

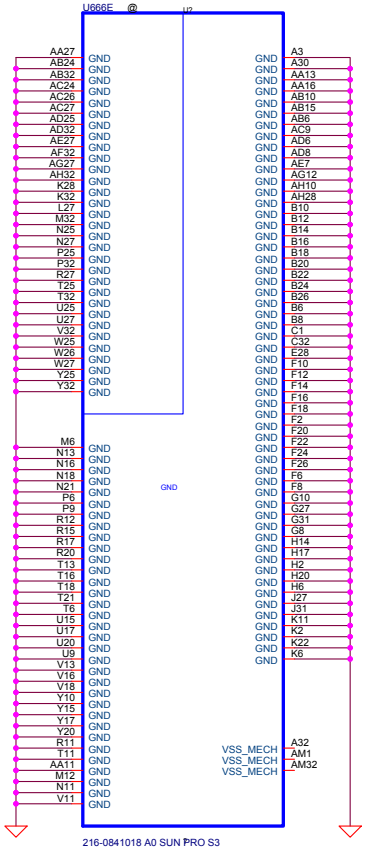


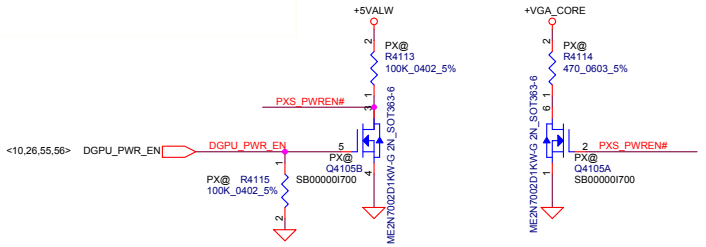
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, AO21331 (engineering sample available on 2013/Jan/18)

+1.0V_PRIM to +1.0VS_VGA (4.016A)









Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power/GND

Size: Custom | Document Number: LA-D707P | Rev: v0.2

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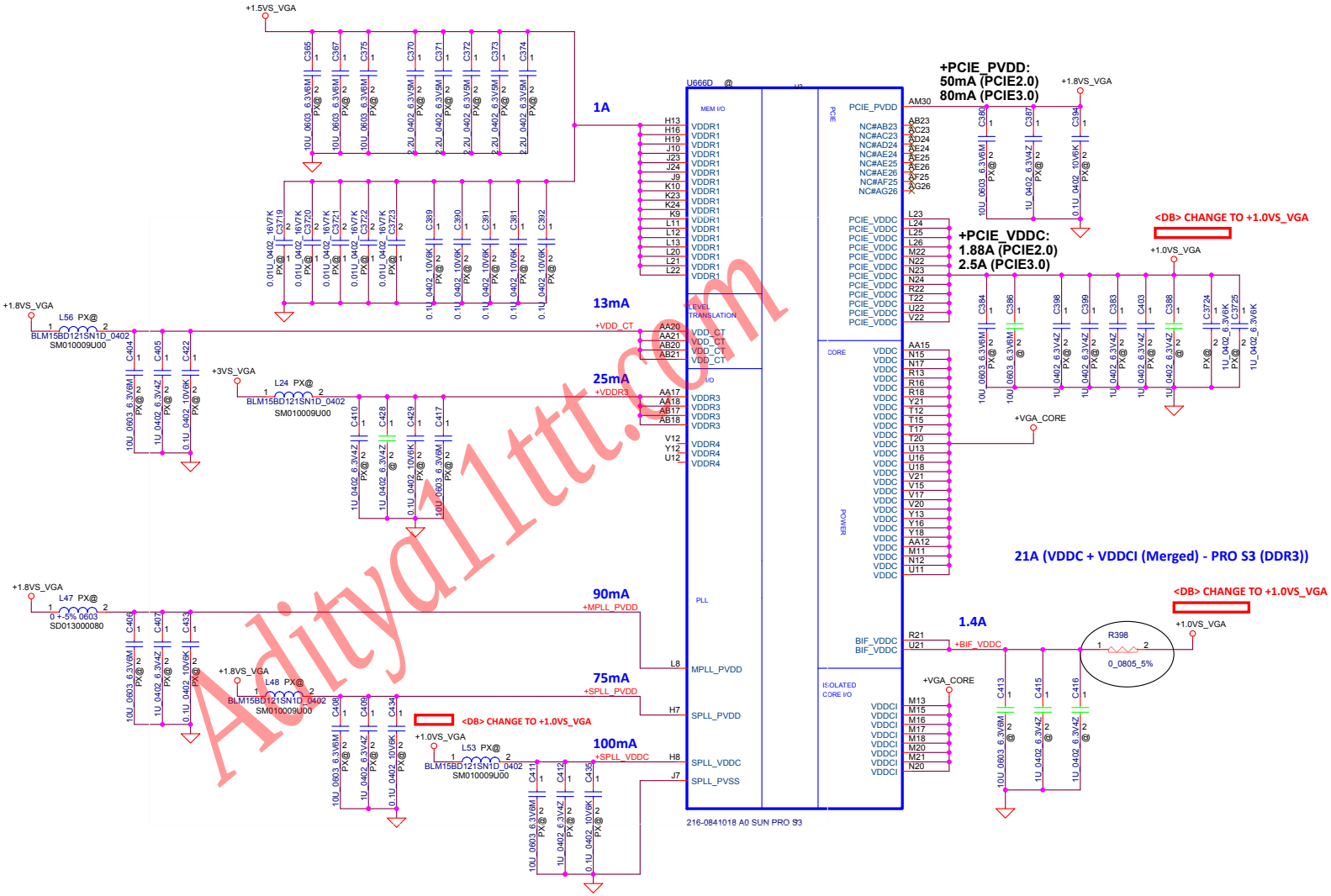
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+1.0VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power

Size: Custom | Document Number: LA-D707P | Rev: v0.2

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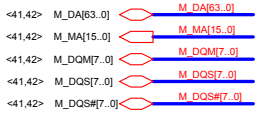
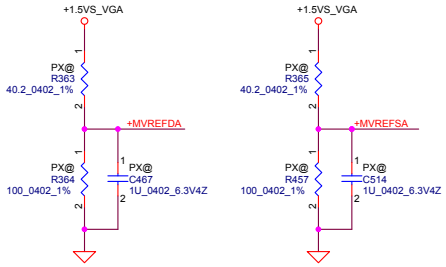
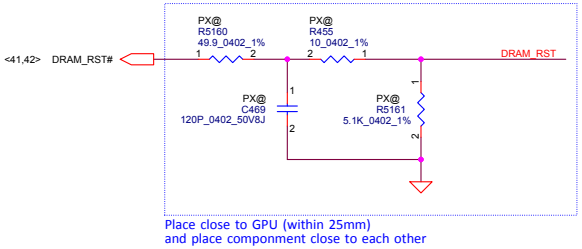
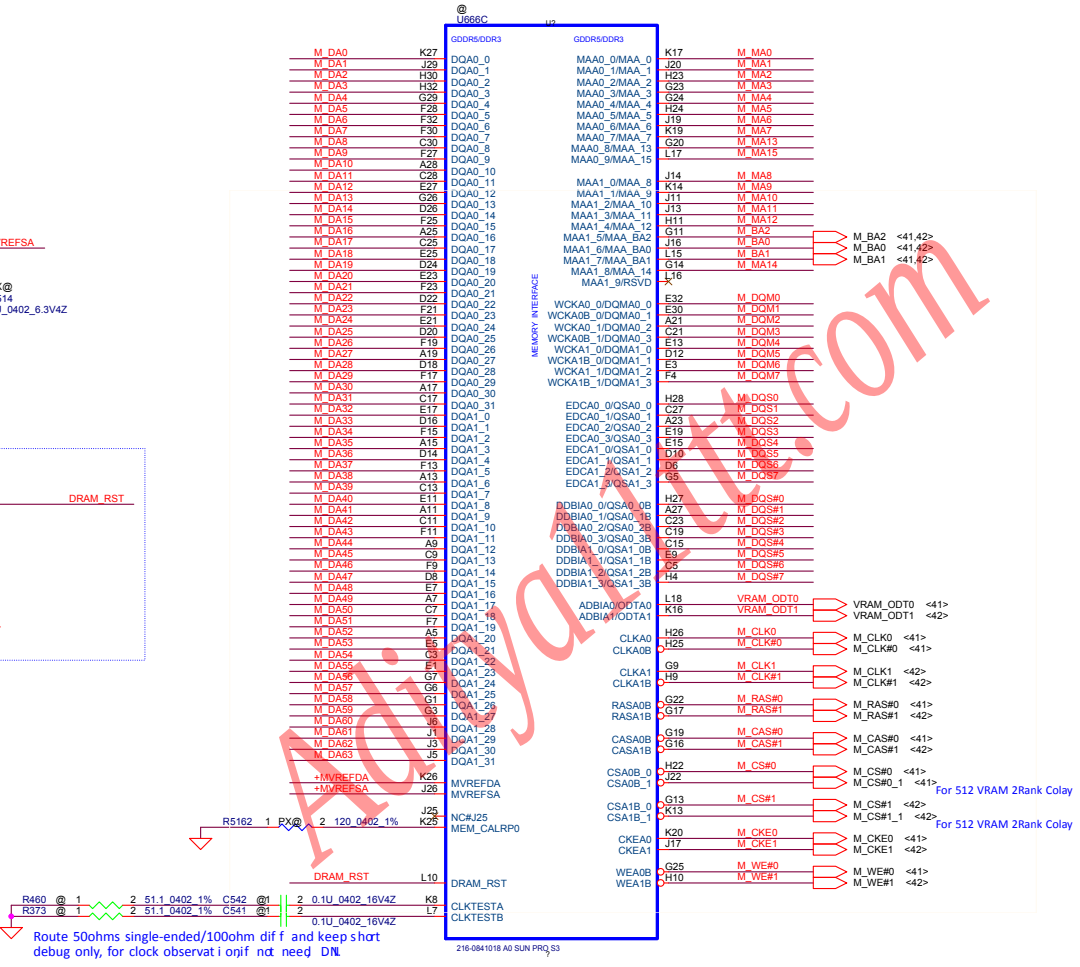








Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

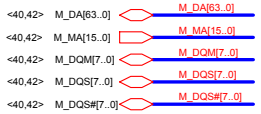
Compal Electronics, Inc.

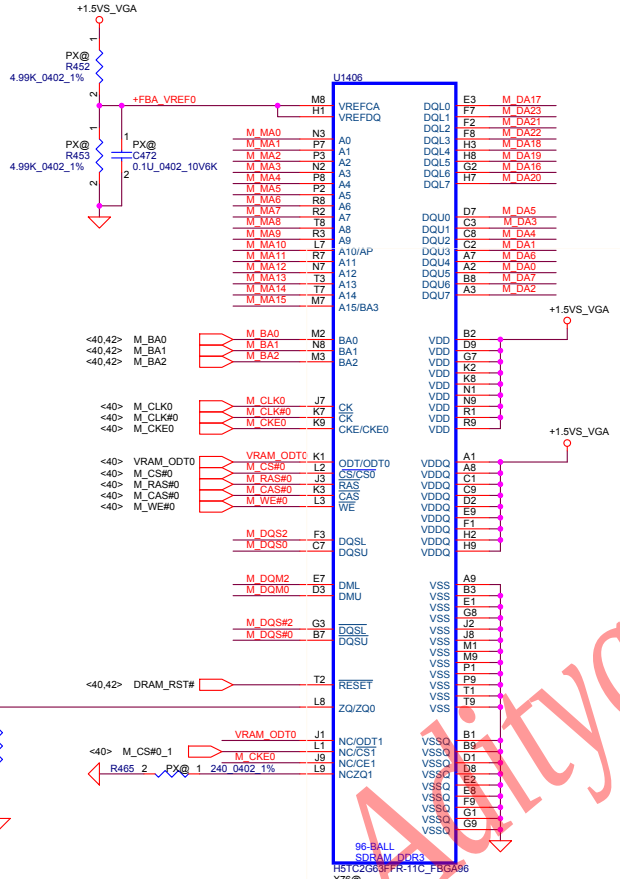
Title: SUN_MEM

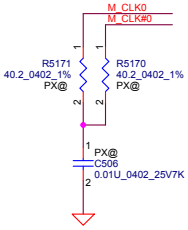
Size: Custom | Document Number: LA-D707P | Rev: v0.2

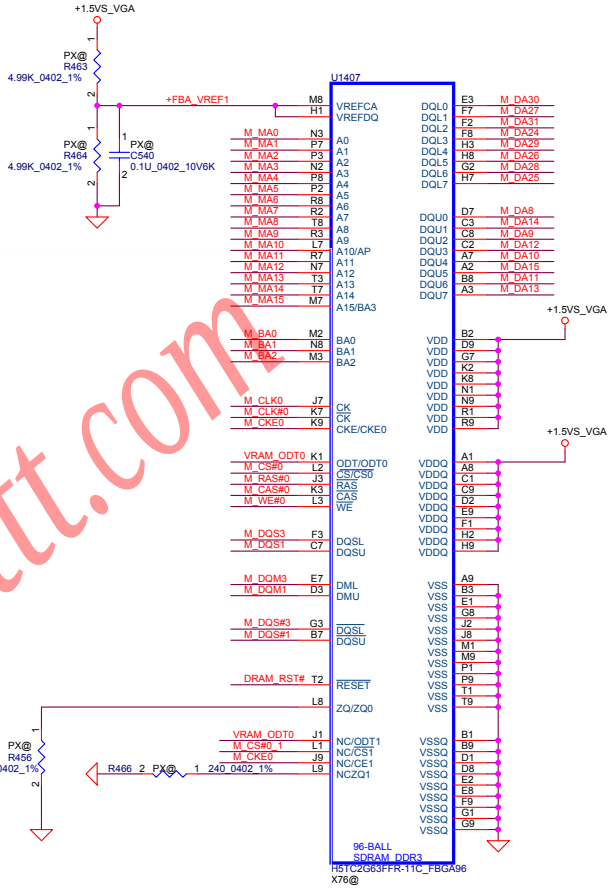
Date: Wednesday, May 11, 2016 | Sheet 40 of 60

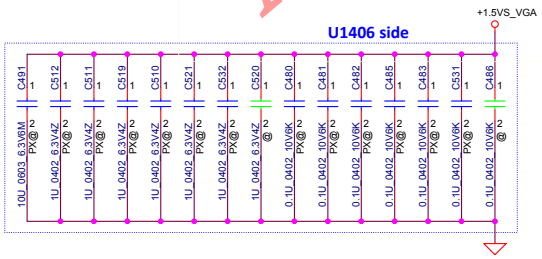
Memory Partition A - Lower 32 bits

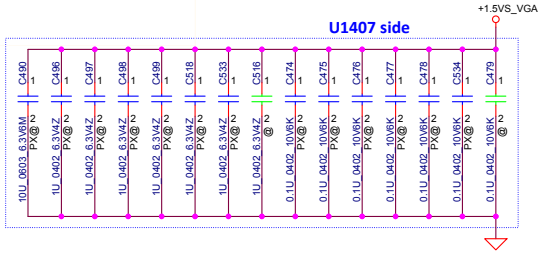












Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.			
Title: SUN_VRAM A Lower			
Size: Custom	Document Number: LA-D707P		Rev: v0.2
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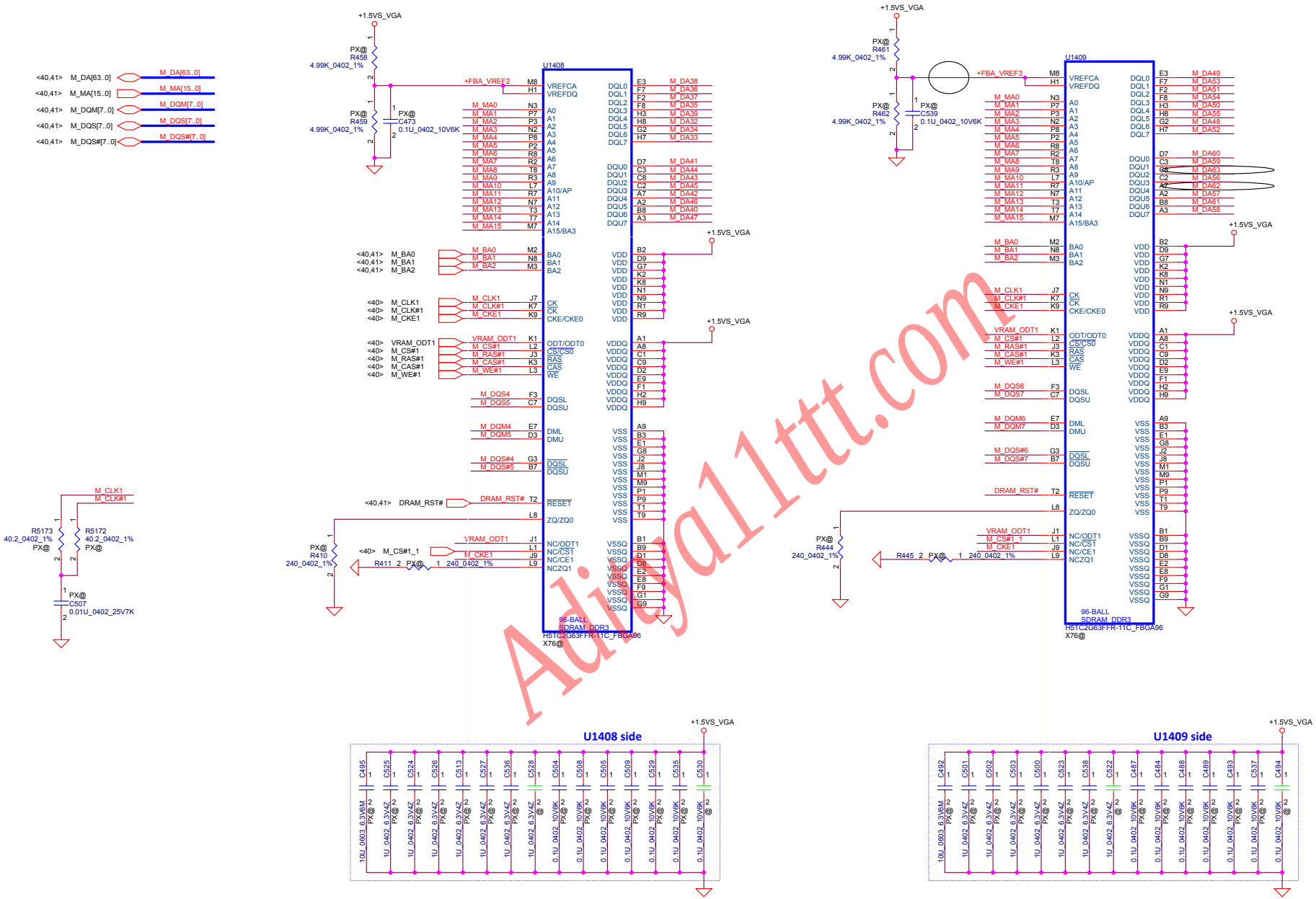
Memory Partition A - Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **SUN_VRAM A Upper**

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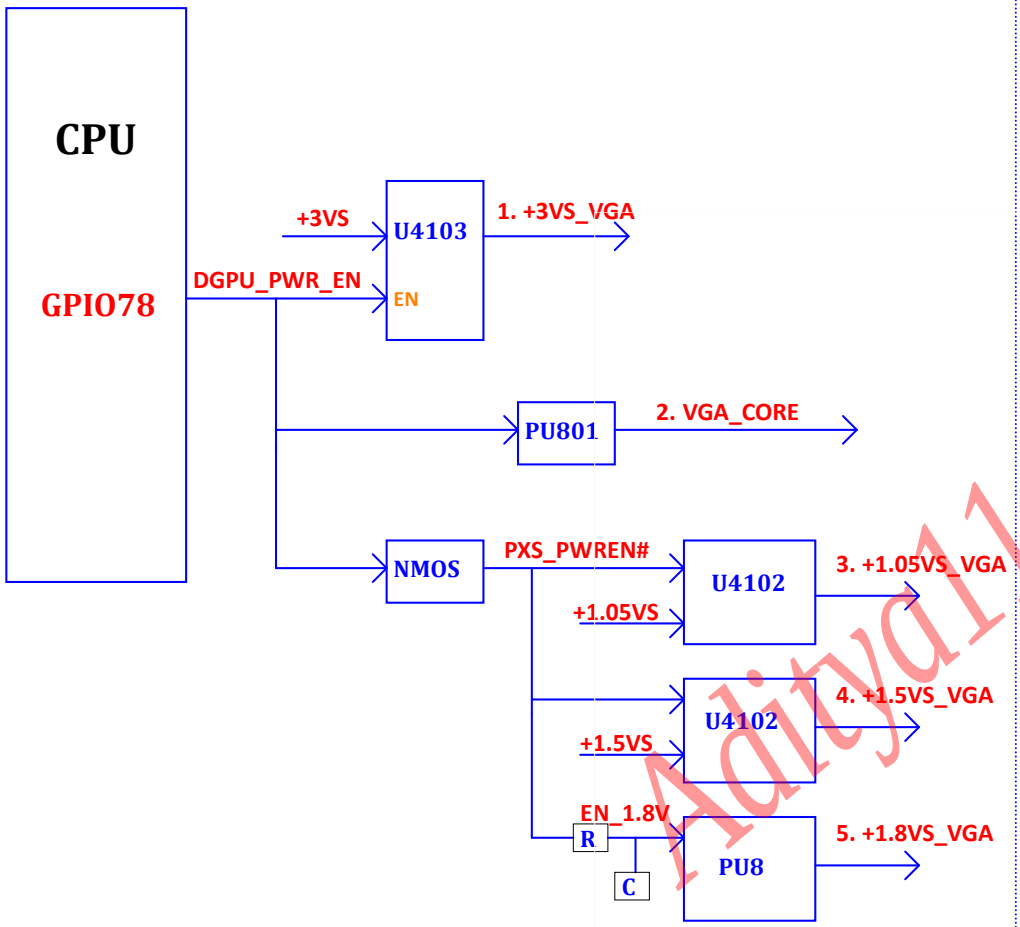

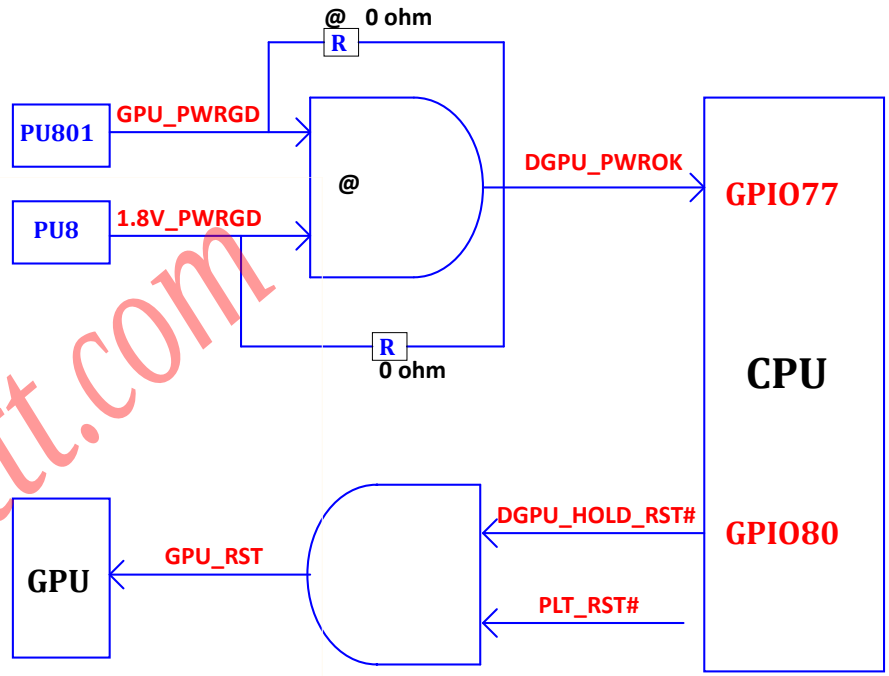

Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	Deciphered Date	Title: RSVD
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Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: **HW Reserve**

Size	Document Number	Rev
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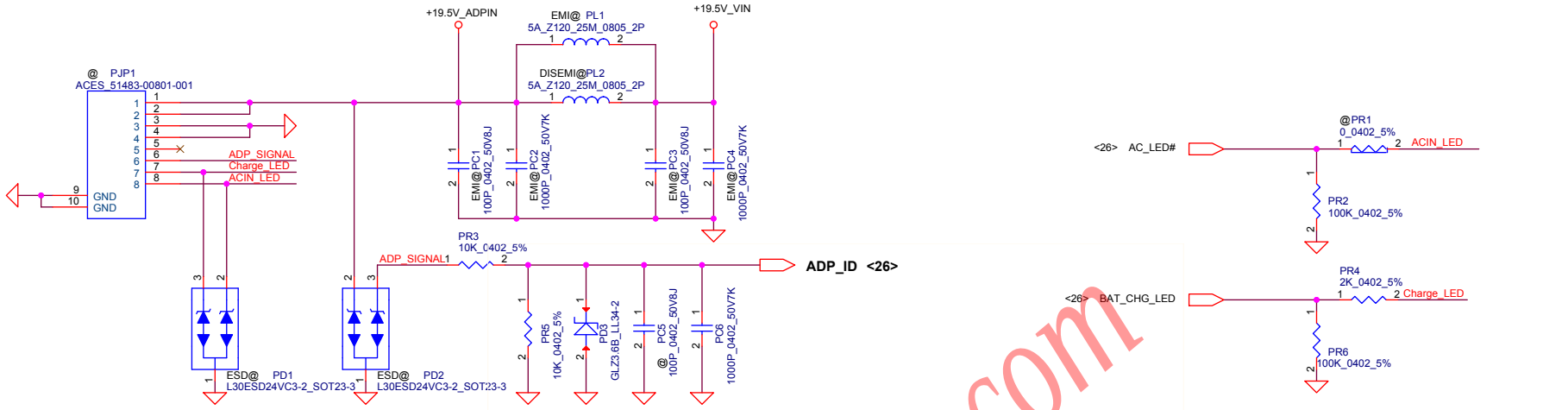
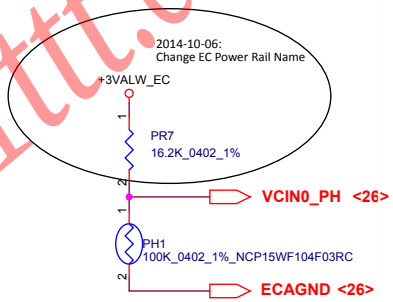
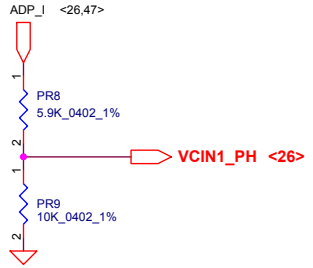






ADP_ID			
Adapter Type		Voltage Range (Dec)	Voltage Range (Hex)
None	Normal Adapter	<0.211V	< 10
	Air-Line Apdater	<0.334V	< 1A
40W	Normal Adapter	>=0.211V ;<0.349V	>= 10 < 1A
45W	Normal Adapter	>=0.349 ;<0.442	>= 1A < 20
65W	Normal Adapter	>=0.442V ;<0.549V	>=20 <2A
	Air-Line Apdater	>=0.334V ;<0.425V	>= 1A < 21
90W	Normal Adapter	>=0.549V ;<0.710V	>= 2A < 36
	Air-Line Apdater	>=0.425 ;<1.391V	>= 21 < 6A
120W	Normal Adapter	>=0.710V ;<1.391V	>= 36 < 6A
ID is shorted to VIN		>=1.391V with Normal and Air-Line	>= 6A

	Initail	Recovery
OTP	92 C	56 C

	Initail	Recovery
45W UMA	0.65V	0.45V
65W DIS	0.95V	0.67V

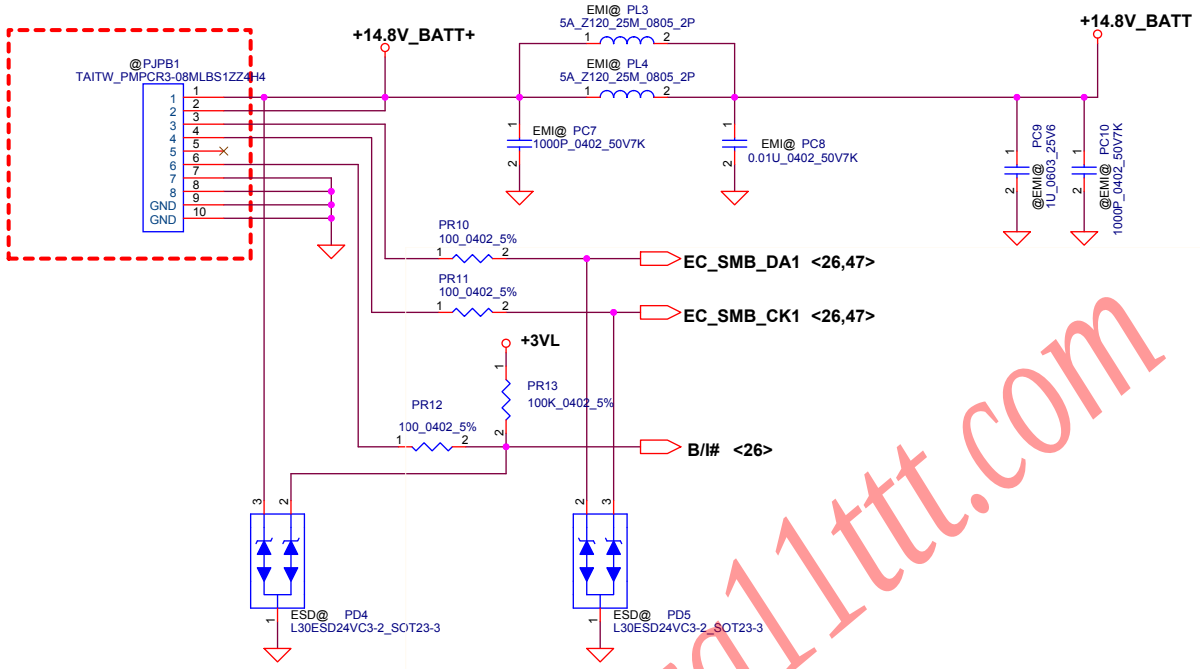
Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: *DC Conn*

Size | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 45 of 60



Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title	***BATT Conn***	
Size	Document Number: **LA-D707P**	Rev: v0.2
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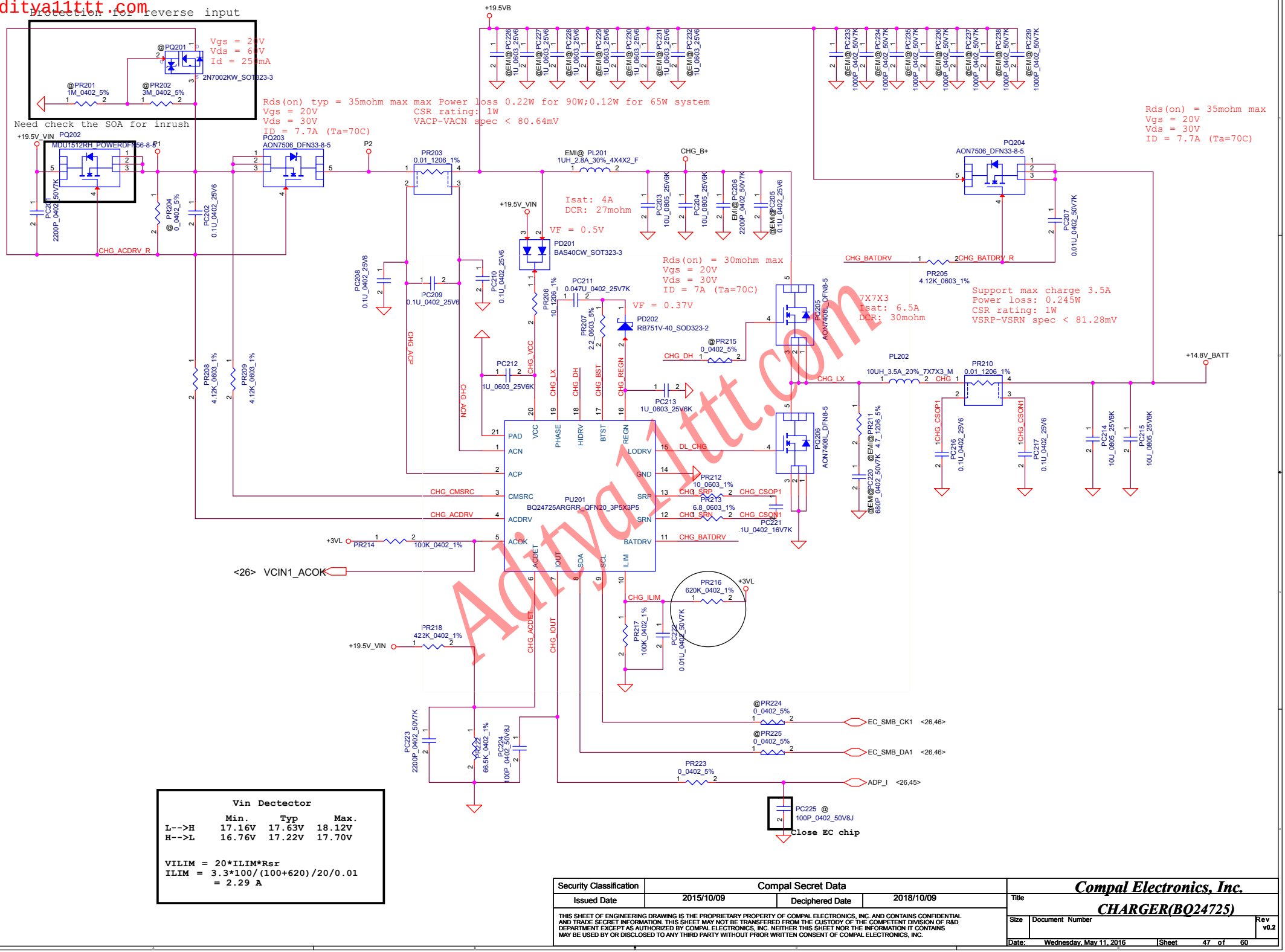

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: CHARGER(BQ24725)

Size	Document Number	Rev
		v0.2

Date: Wednesday, May 11, 2016 Sheet 47 of 60

Module model information

RT8243A_V1.mdd

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off

ENTRIPx adjustment range: 0.5V~3V,
floating or over 4.5V will shutdown channel.

Trace width need meet LDO5 demand

Vout=VFB * (1+(R1/R2))
VFB=2V
Vout=2*(1+(30K(PR39)/20K(PR43)))
Vout=5V

Vout=VFB * (1+(R1/R2))
VFB=2V
Vout=2*(1+(13.3K(PR38)/20K(PR40)))
Vout=3.3V

ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max

B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max

VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

+3.3VALWP Ipeak=4.26A ; Imax=3A
Delta I=1.92A=>1/2Delta I=0.96A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP = 5.1A

TDC:4.31A Fsw:375KHz
H-MOS PD:0.3736W Δ T:12℃
L-MOS PD:0.2713W Δ T:7.9℃
Choke PD:1.5158W Δ T:23℃
OVP margin for Vos:8% @ 330uF cap, 6% @ 220uF

5V=375KHz 3V=400KHz (Vin=12 ~ 25v)
(By Rton= 56K ohm)

+5VALWP Ipeak=9.26A ; Imax=6.5A
Delta I=3.483A=>1/2Delta I=1.742A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP =11.11A

TDC:4.9A Fsw:321KHz
H-MOS PD:0.4173W Δ T:13.3℃
L-MOS PD:0.3442W Δ T:10℃
Choke PD:1.9613W Δ T:30℃
OVP margin for Vos:9% @ 330uF cap, 8% @ 220uF

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: LA-D707P | Rev: v0.2

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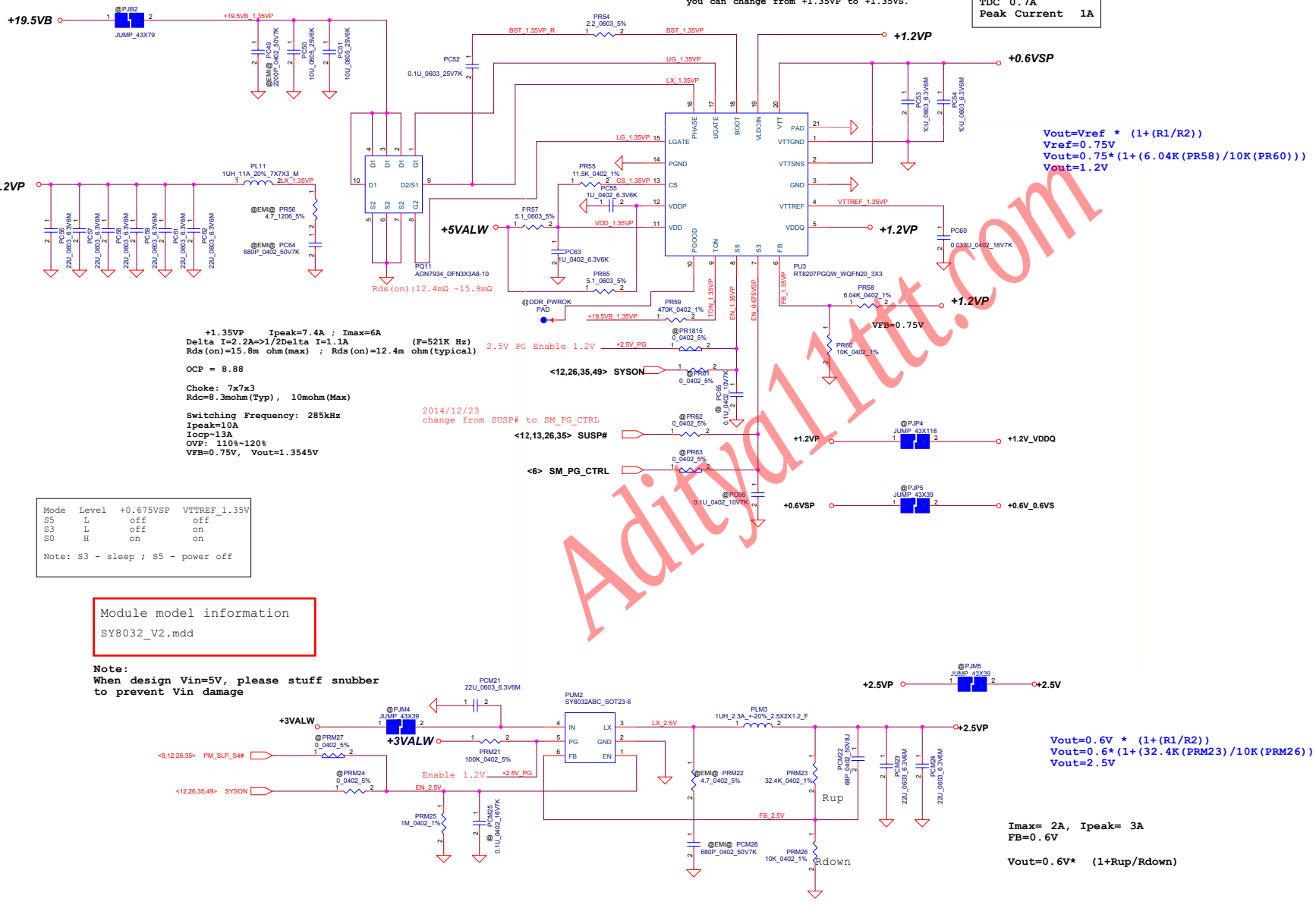
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Module model information

SY8032_V2.mdd

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5VP(RT8207P/SY8032A)

Size: Custom | Document Number | Rev: v0.2

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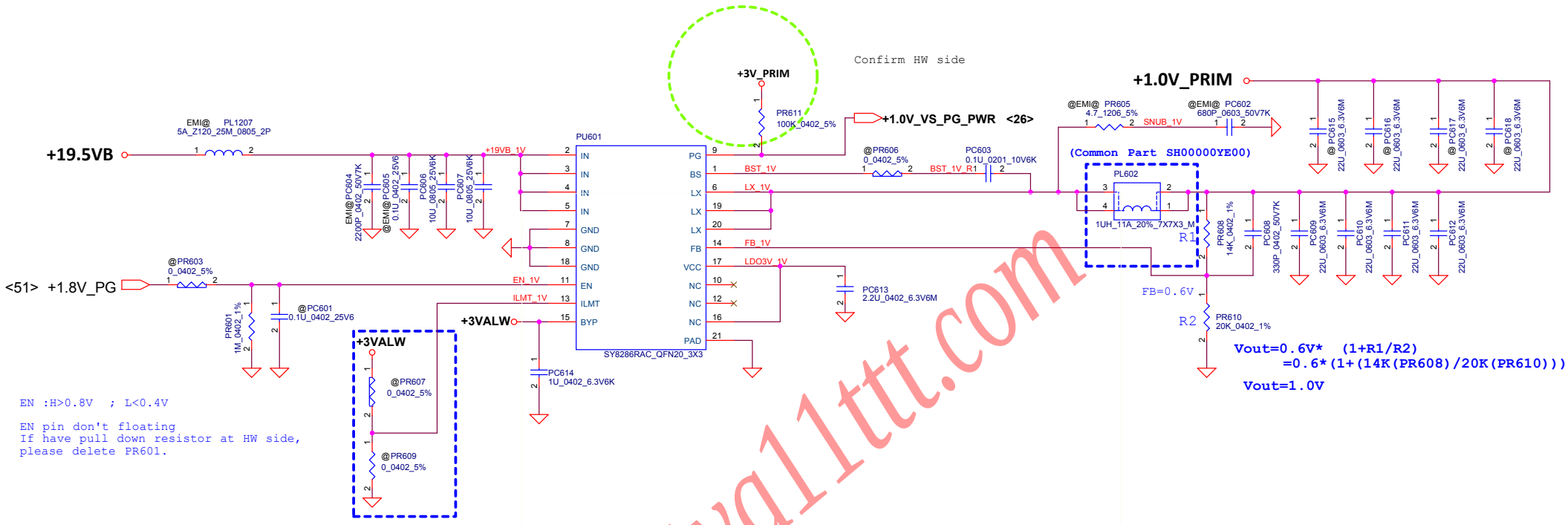

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Title: 1.0VS(SY8286)

Size: Custom | Document Number | Rev: v0.2

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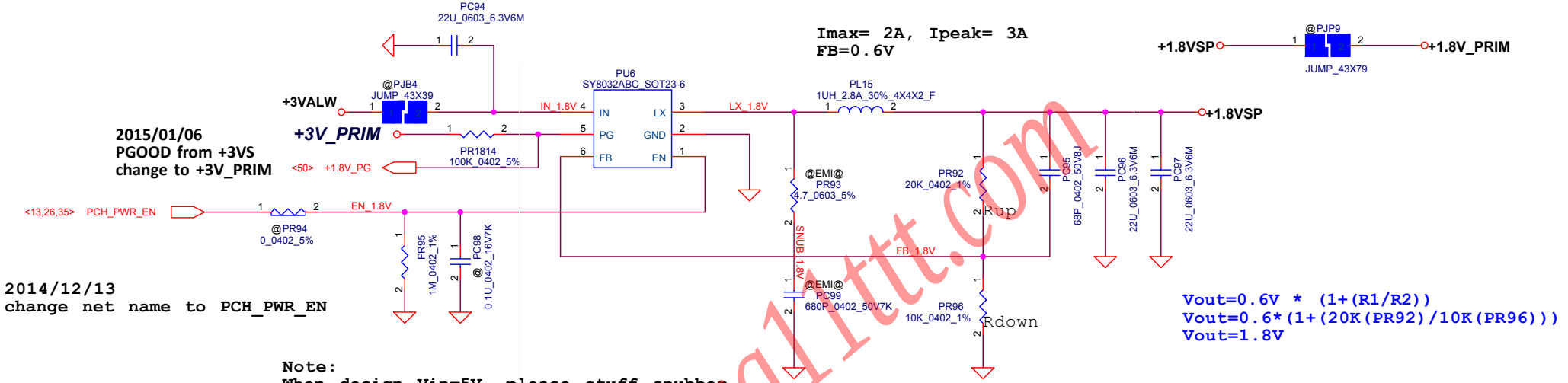

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: *1.8VS(SY8032A)*

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PR1101=2*PR1106/(10*IOUTmax*Load line)
U22 Iout@GT=31A
PR1101=25.5kohm

PR1106=Iout limit*Load line/10
U22 OCP@GT=40A
PR1106=12.4kohm

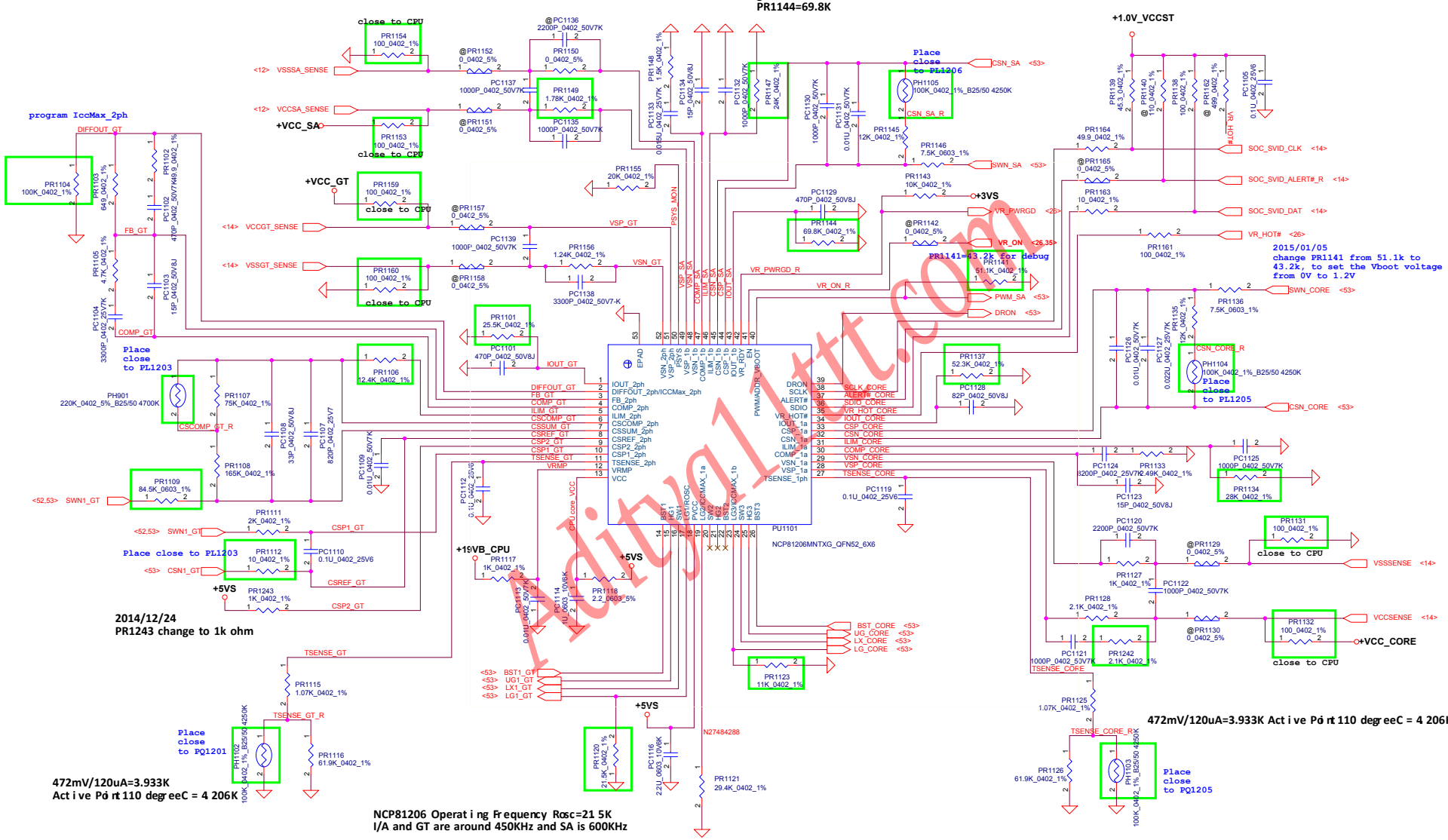
RIccMAX2ph(PR1104)= (IccMAX2Ph+32)*200kohm/ 127
U22 IccMAX@GT= 31A
PR1104= 100K

Load line=(PR1108+(PR1107+PH901/(PR1107*PH901)))*Iout tltal*DCR/PR1109
U22 Load line@GT= 3.1m
PR1109 , PR1110@GT=84.5K

RDRPSP(PR1149)= Load line*(PR1146+PH1105+PR1145)/(gm * DCR) /(PH1105+PR1145)
Load line@SA= 10.3m
gm=1mS
PR1149=1.78K

RLIMSP(PR1147)= 1.3V/(gm*(PH1105+PR1145)*IoutLIMIT*DCR/(PR1146+PH1105+PR1145))
OCP@SA= 9.6A
gm=1mS
PR1147=24K

RIOUTSP(PR1144)= 2V/(gm*(PH1105+PR1145)*ICCMAX*DCR/(PR1146+PH1105+PR1146))
IOUTSP@SA= 5A
gm=1mS
PR1144=69.8K



Title	VCC_CORE_U22(NCP81206)		
Size	Document Number		Rev v0.2
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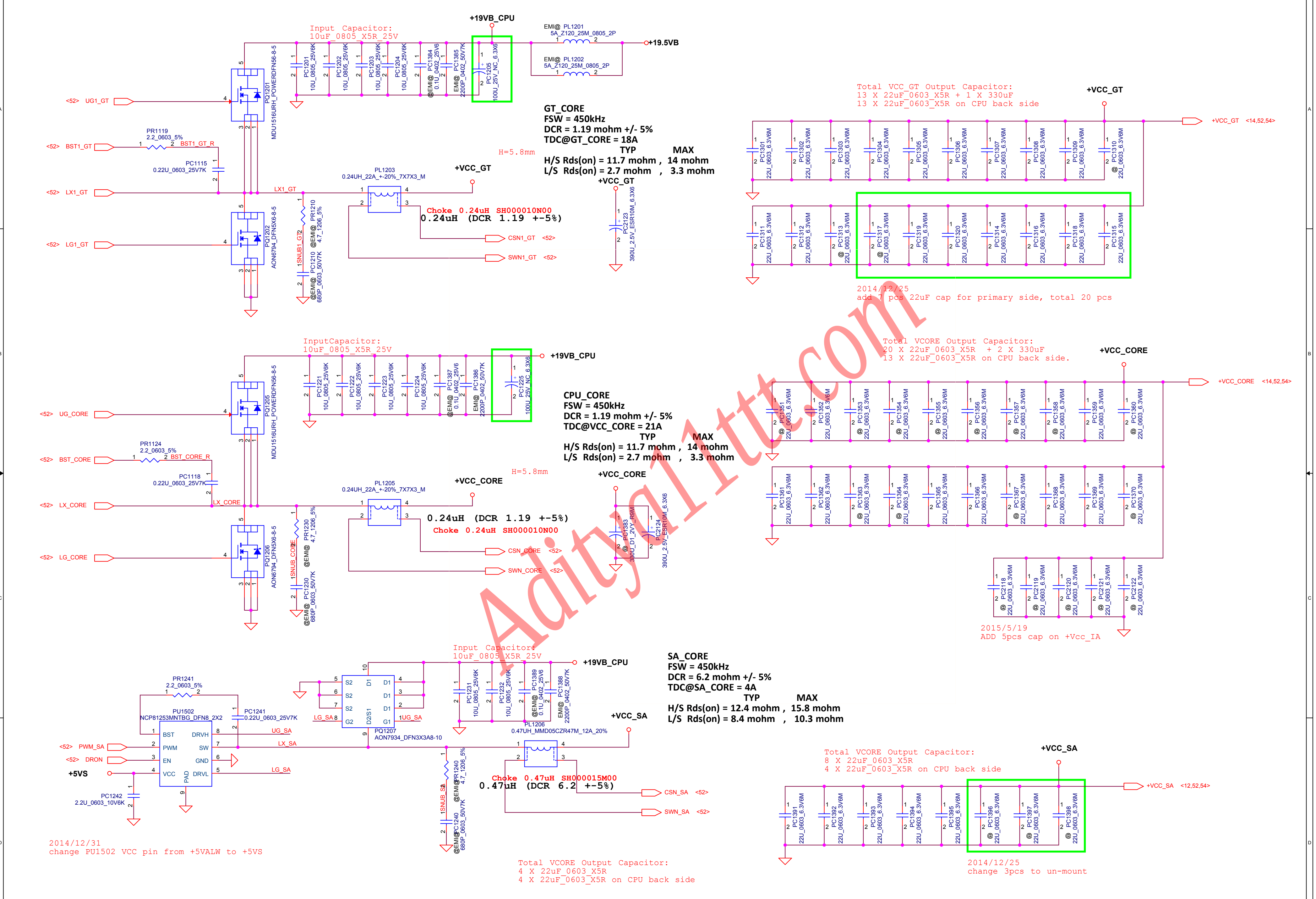

Title	VCC_CORE_PowerStage
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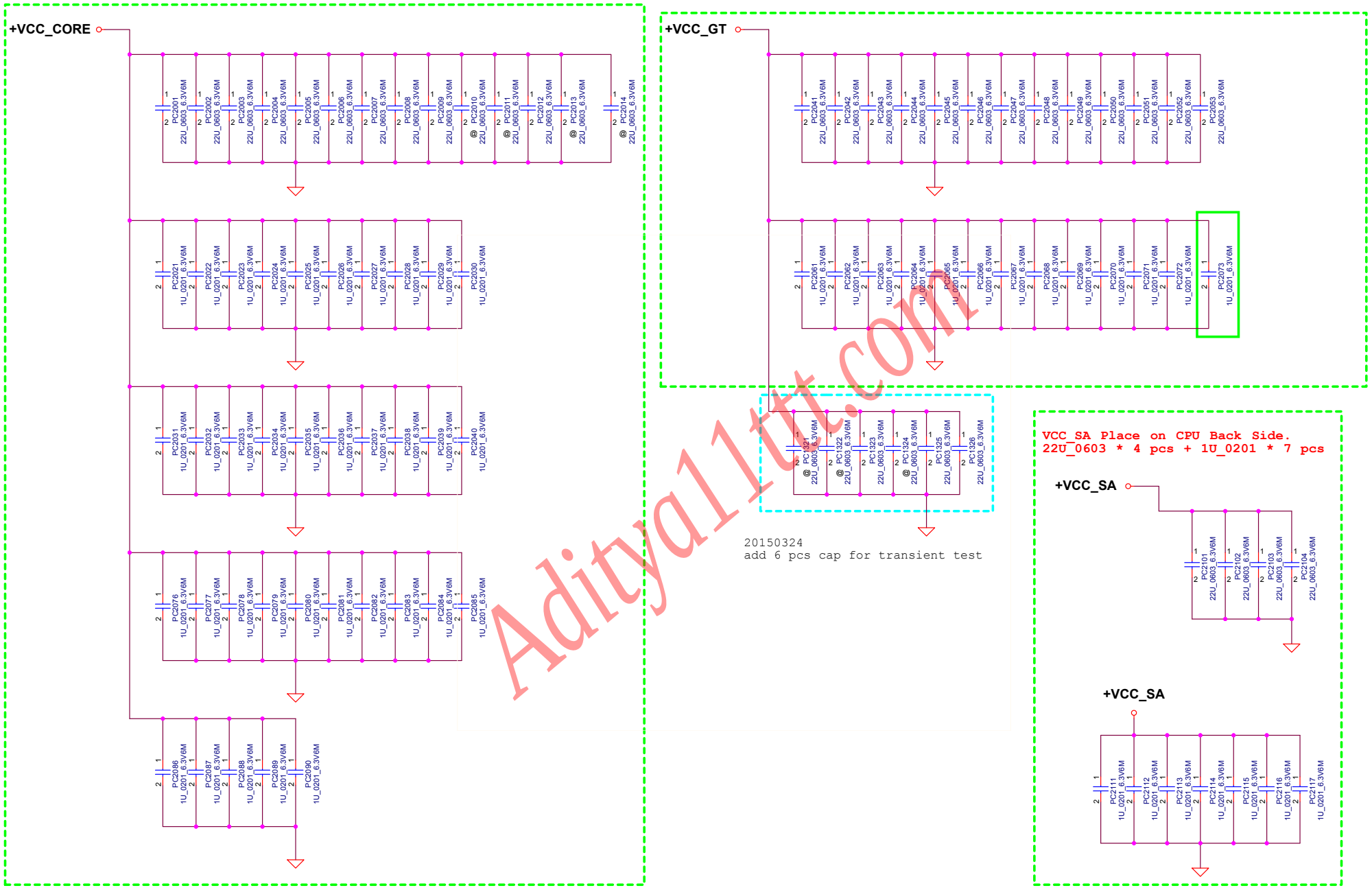
VCC_CORE Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*35 pcs

VCC_GT Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*12 pcs

2014/12/25
add 1 pcs 1uF cap for back side, total 13 pcs



Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title	*VCC_CORE_PROCESSOR DECOUPLING*	
Size	Document Number: LA-D707P	Rev: v0.2
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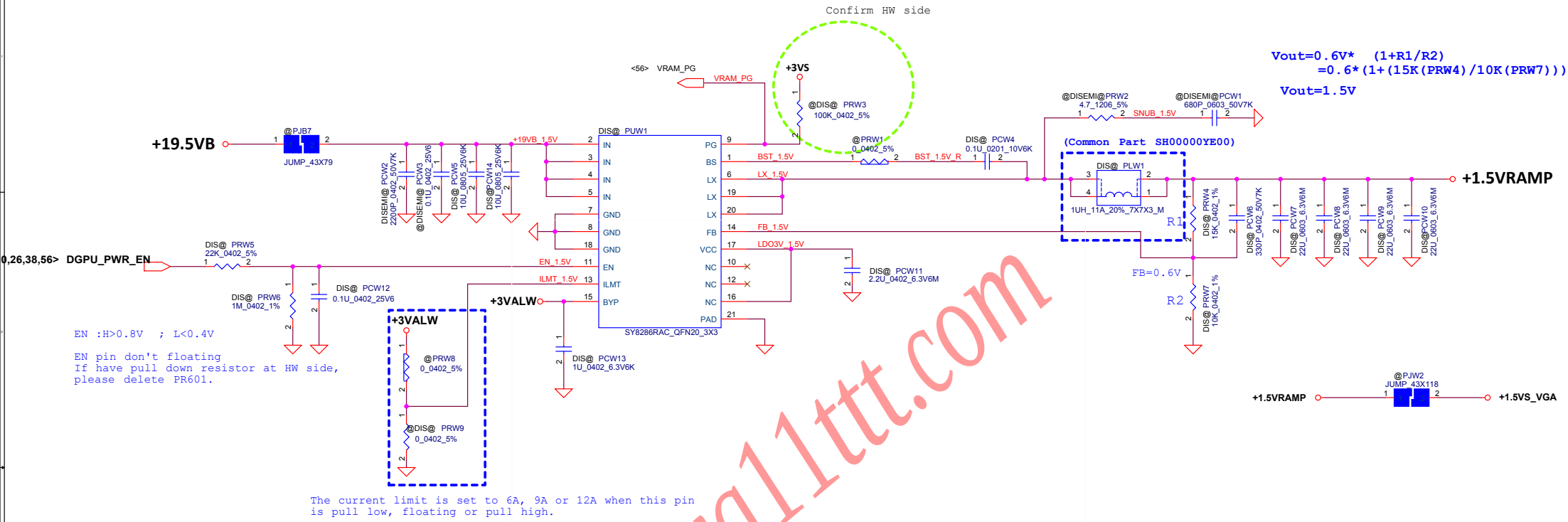

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title	*1.5VS_VGA(SY8286)*	
Size	Document Number: LA-D707P	Rev: v0.2
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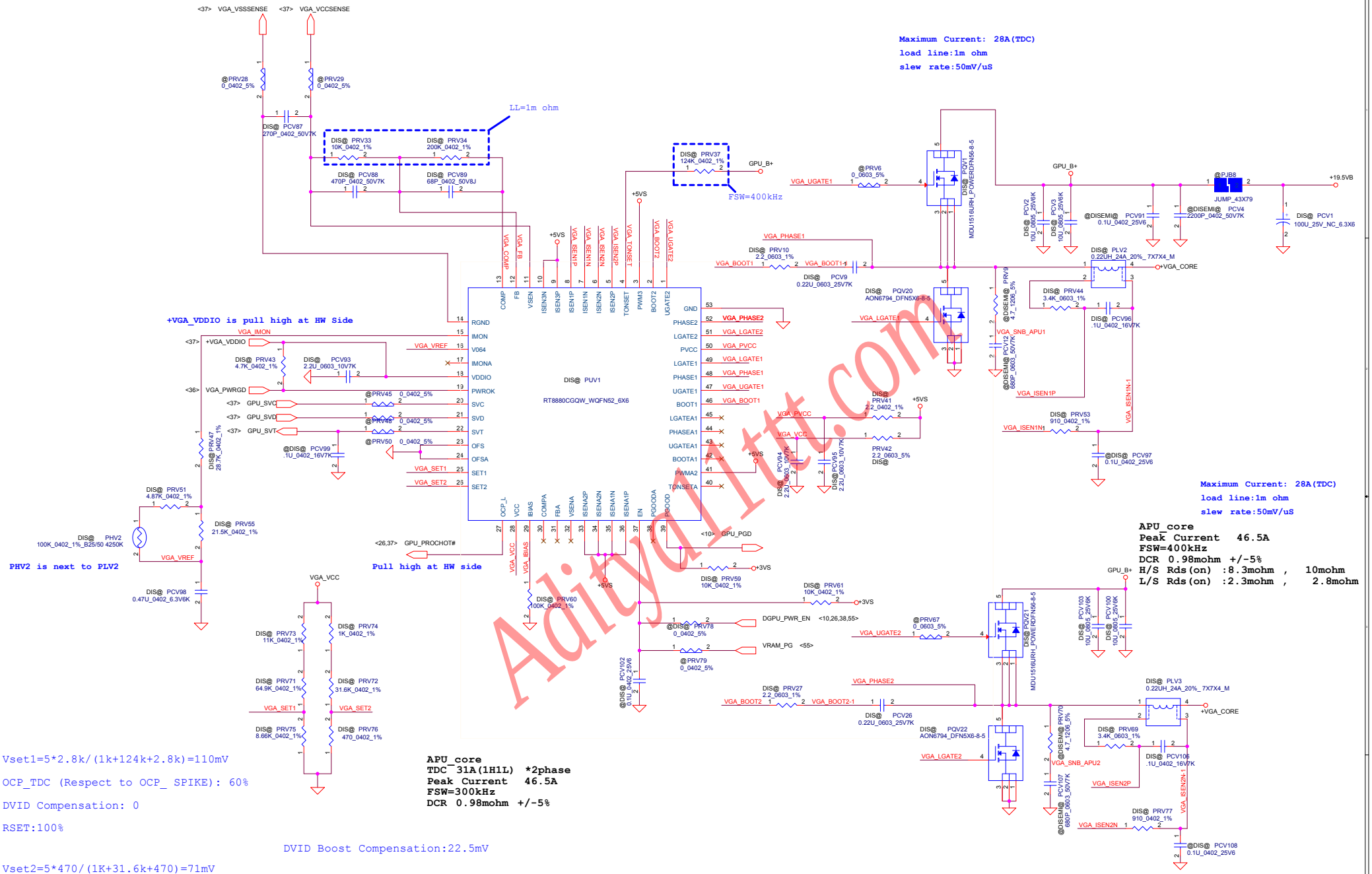

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: VGA_CORE(RT8880A)

Size	Document Number	Rev
		v0.2

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560u X 3
2.2u X 16
10u X 8
1u X 3
0.1u X 2

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title	*VGA_CORE_CHIP DECOUPLING*	
Size	Document Number: LA-D707P	Rev: v0.2
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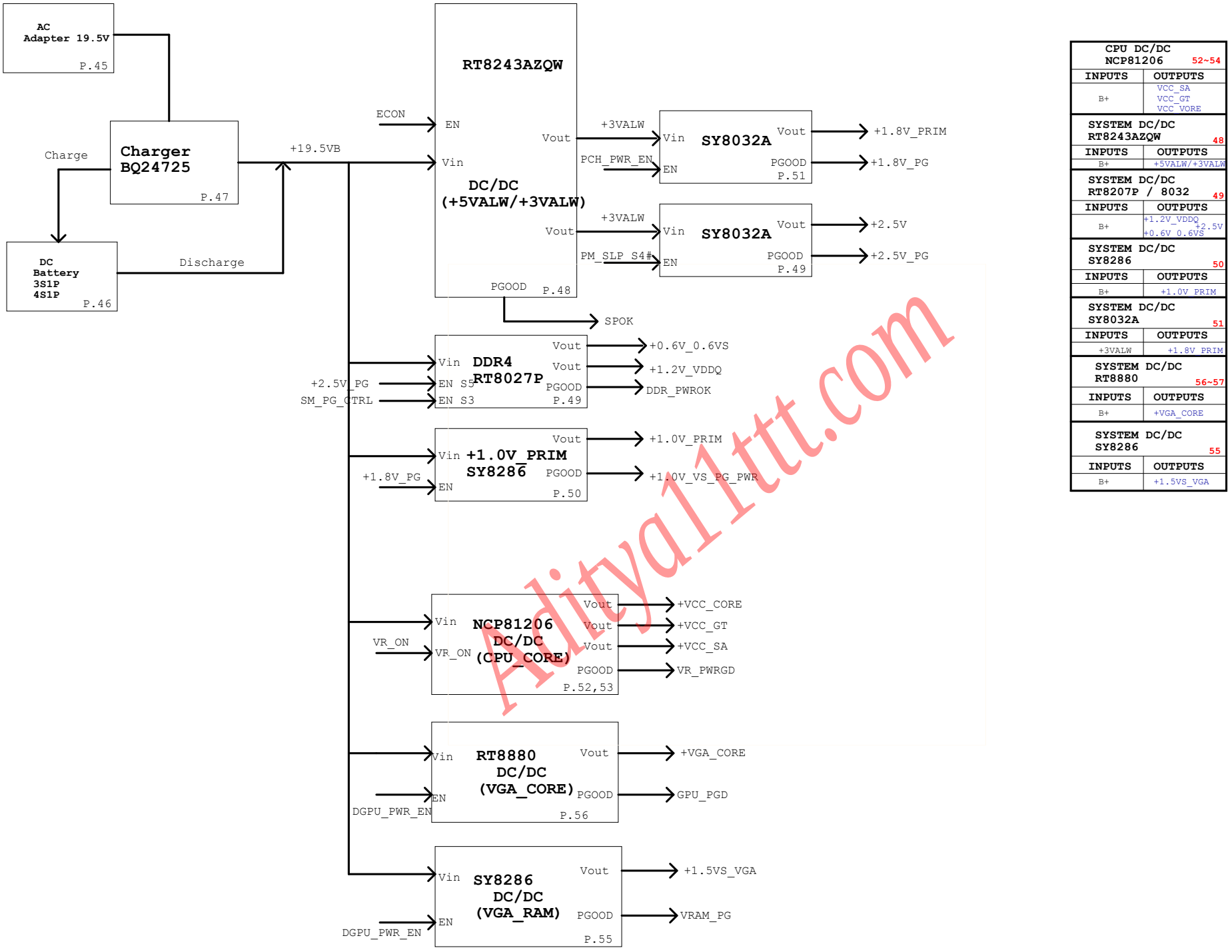

CPU DC/DC NCP81206 52~54	
INPUTS	OUTPUTS
B+	VCC_SA VCC_GT VCC_VORE

SYSTEM DC/DC RT8243AZQW 48	
INPUTS	OUTPUTS
B+	+5VALW/+3VALW

SYSTEM DC/DC RT8207P / 8032 49	
INPUTS	OUTPUTS
B+	+1.2V_VDDQ +2.5V +0.6V_0.6VS

SYSTEM DC/DC SY8286 50	
INPUTS	OUTPUTS
B+	+1.0V_PRIM

SYSTEM DC/DC SY8032A 51	
INPUTS	OUTPUTS
+3VALW	+1.8V_PRIM

SYSTEM DC/DC RT8880 56~57	
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8286 55	
INPUTS	OUTPUTS
B+	+1.5VS_VGA

SKL_SI

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52	Change Value	11/06	Power	(Set VR prochot# from 110C to 120C)	Change PR1115 and PR1125 Value 0 ohm to 1.07K ohm	
2	50	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PL602 part number from SH00000Z200 to SH00000YE00	
3	55	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PLW1 part number from SH00000Z200 to SH00000YE00	
4	48	Add Jump	11/18	Power	For easy debug	+3VL and +VL add Jump	
5	55	Add Net	11/18	EE	For VGA CORE sequence and VID error issue	Delete PG pin test point VRAM_PG Add Net VRAM_PG	
6	56	pop to unpop unpop to pop	11/18	EE	For VGA CORE sequence and VID error issue	PRV61 from unpop to pop PRV78 and PCV102 from pop to unpop	
7	56	Add Net and R	11/18	EE	For VGA CORE sequence and VID error issue	Add Net VRAM_PG Add PRV79	
8	47	Change jump to ISN choke	11/24	EMI	EMI ISN issue	Delete jump PJB9 Add ISN choke PL201	
9	48	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL7	
10	49	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL10	
11	50	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB3 Add Bead PL1207	
12	53	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB5 Add Bead PL1201 PL1202	
13	55	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1208	
14	56	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1209 and PL1210	
15	55	Change R Value Change C unpop to pop	11/24	EE	HW fi net une VRA Mpo wer sequence	Change PRW5 value from 0 ohm to 22K ohm Change PCW12 from unpop to pop (VGA sequence)	
16	53	Change Common part	11/6	Power	(Change to Common part)	Change PC1331 PC1383 PC1390 from SGA20331E10 to SGA00009S00	

SKL_PV

Item	Page	Title	Change Description	Date
1	56	Modify VGA_CORE OCP	1. Change PRW73 Value 1K ohm to 11K ohm 2. Change PRW71 Value 124K ohm to 64.9K ohm 3. Change PRW75 Value 2.8K ohm to 8.66K ohm	2015-12-12
2	47	space saving	Change PC221 0603 to 0402 size	2015-12-12
3	47,49,50,51,52,56	Change 0 ohm to short pad	Change PR63,PR94,PR215,PR603,PR1129,PR1130,PR1142,PR1151,PR1152,PR1157,PR1158,PR1165,PR1815,PRM27,PRV45,PRV48,PRV50,PRV79,PRV6,PRV67 from 0 ohm to short pad	2016-1-4
4	48,49,55,56	Delete Jump or Bead(Co-lay)	Delete Co-Lay Bead PL7,PL10,PL1208,PL1209,PL1210	2016-1-7
5	53	Delete VCC_GT,VCC_CORE Co-Lay caps	Delete Location PC1331 Footprint,PC2123 from unpop to pop Delete Location PC1390 Footprint,PC2124 from unpop to pop	2015-12-12
6	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800	2015-12-12
7	52,53,54	CPU transient request	Change PC1353,PC1363,PC1355,PC1356,PC1357,PC1354,PC1364,PC1358,PC1351,PC1370,PC1360,PC2010,PC2013,PC2011,PC1367 from pop to unpop Change PC1107 from 1000P to 820P PC1108 from 390P to 33P,PC1108 from unpop to pop PC1104 from 2200P to 3300P PR1103 from 1K to 649	2015-12-12
8	50	1V OVP issue (HW Low switch second source issue)	Delete jump PJ601 and add output MLCC PC615,PC616,PC617,PC618 PR607 from unpop to pop	2016-1-7

Title	Power_PIR(SI)		
Size C	Document Number LA-D707P		Rev v0.2
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P. I. R. List

KBL_SI

Item	Page	Title	Change Description	Date
1	50,55	Change 0 ohm to short pad	Change PR607,PRV28,PRV29 from 0 ohm to short pad PRW8 from unpop to pop , change PRW8 from 0 ohm to short pad	2016-2-19
2	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000S800 to SB00000JZ00(Change to Main source)	2016-2-19
3	54	Add IA_Core Output capacitor	Add IA_Core Output capacitor 0603 22uF(PC2014) for IccMAX=32A	2016-2-24

KBL_PV

Item	Page	Title	Change Description	Date
1	47	ADP_I resistance	Change PR223 from short pad to 0 ohm	2016-4-28
2	52	ICCmax from 29A to 32A	Change PR1121 from 20.5K to 29.4K Change PR1137 from 61.9K to 52.3K Change PR1134 from 33.2K to 28K	2016-4-28
3	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800(Change to 2nd source)	2016-4-28
4	49	Add 2nd source	Change PU3 from RT8207P (SA00007IH00) to G5616B (SA00008PH00)	2016-4-28
5	48	Add 2nd source	Change PU2 from RT8243A(SA00005VH00) to UP1590PQKF(SA00007DS00)	2016-4-28

Title	Power_PIR(PV)		
Size C	Document Number LA-D707P		Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 60 of 60		