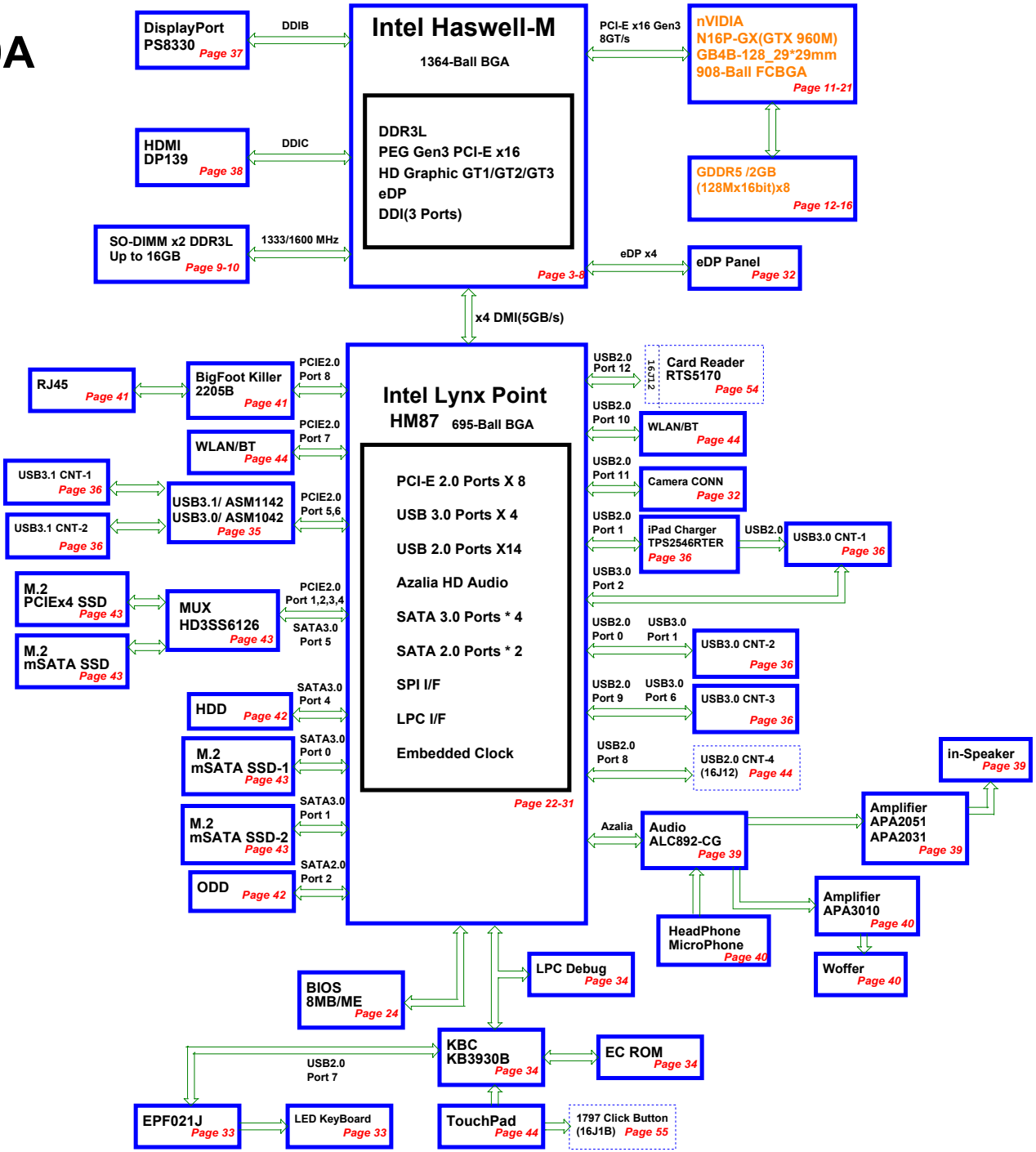
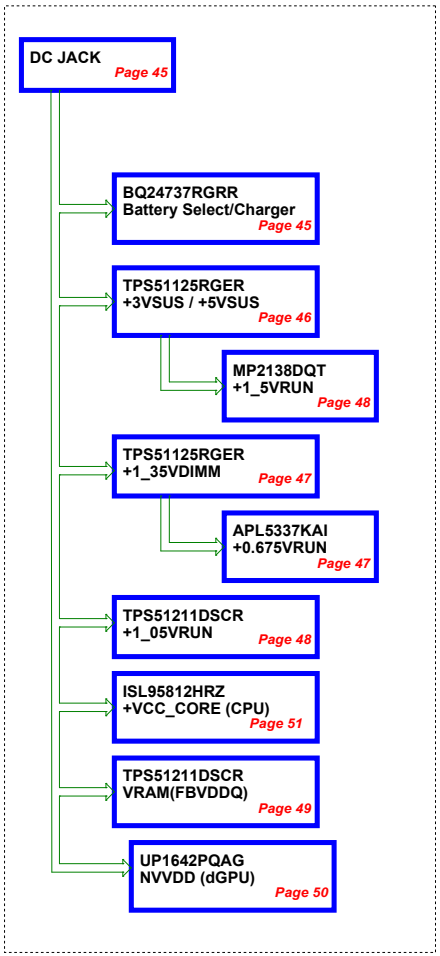
MS-16J2 /1792

Ver:0A

Shark Bay Mobile

Thursday, October 16, 2014





msi MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

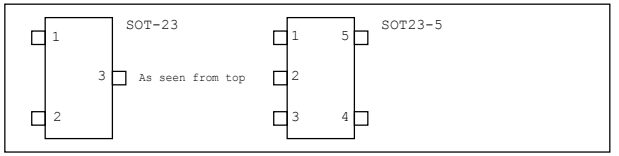
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

Net Naming Conventions

Suffix
```
#  =  Active Low Signal
```
Prefix
```
H  =  Host
M  =  DDR Memory
TP =  Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx =  Like Test Point, but using VIA.
```

PCB Footprints



BOM	607-16J21-A10	607-16J21-A20	607-16J21-A30	607-17921-A10	607-17921-A20	607-17921-A30
Graphics	N16P-GX(GTX960M)	N16P-GX(GTX960M)	N16P-GX(GTX960M)	N16P-GX(GTX960M)	N16P-GX(GTX960M)	N16P-GX(GTX960M)
MB ID	PR147 100K pull-up	PR147 100K pull-up	PR147 100K pull-up	PR147 100K pull-up	PR147 100K pull-up	PR147 100K pull-up
GDDR5	Samsung K4G20325FD-FC03 M12-2032585-S02	Hynix H5GC2H24BFR-T2C M12-5GC2H05-H23	Micron EDW2032BBBG-6A-F M12-2032B95-M30	Samsung K4G20325FD-FC03 M12-2032585-S02	Hynix H5GC2H24BFR-T2C M12-5GC2H05-H23	Micron EDW2032BBBG-6A-F M12-2032B95-M30
STRAP	R3082 4.99K 1% PD R11-4991T12-W08	R3082 10K 1% PD R11-0103T12-W08	R3082 30.1K 1% PD R11-3012T12-W08	R3082 4.99K 1% PD R11-4991T12-W08	R3082 10K 1% PD R11-0103T12-W08	R3082 30.1K 1% PD R11-3012T12-W08
SW&LED	Stuff UB1 SW1,SW2, R479,R480,R481,R482, D9,D10,D11,D12 D1 device on board A and B don't stuff			Stuff UB2 FPC17,FPCB1,SWB3,SWB4 RB479,RB480,RB481,RB482 DB9,DB10,DB11,DB12 D14		

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

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Title: Platform

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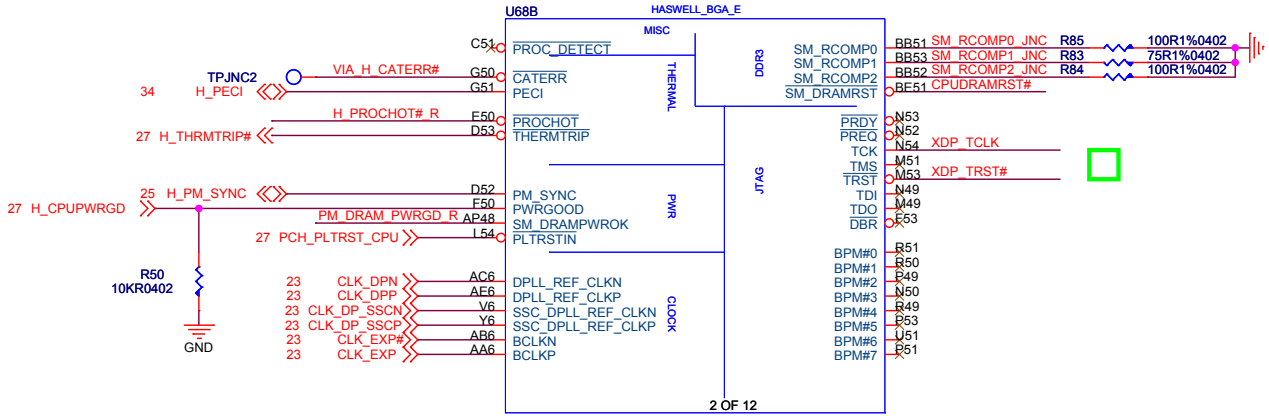
Haswell (DMI,PEG,FDI)

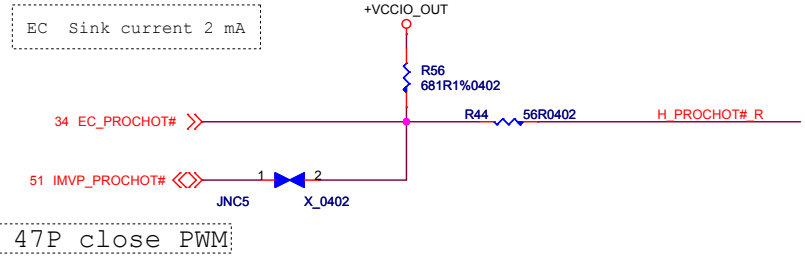
PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

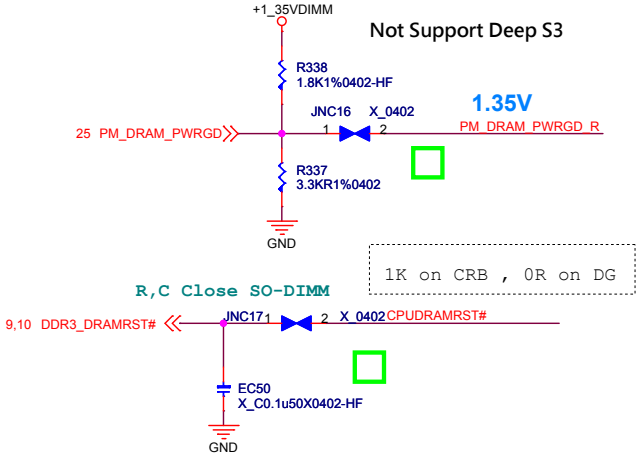
Haswell (CLK,MISC,JTAG)

i7-4710HQ,(SR1PX),2.5GHz

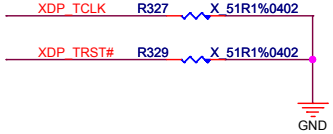
SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil







p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.



MICRO-STAR INT'L CO.,LTD.

Title	CPU-1 (Host Bus)	
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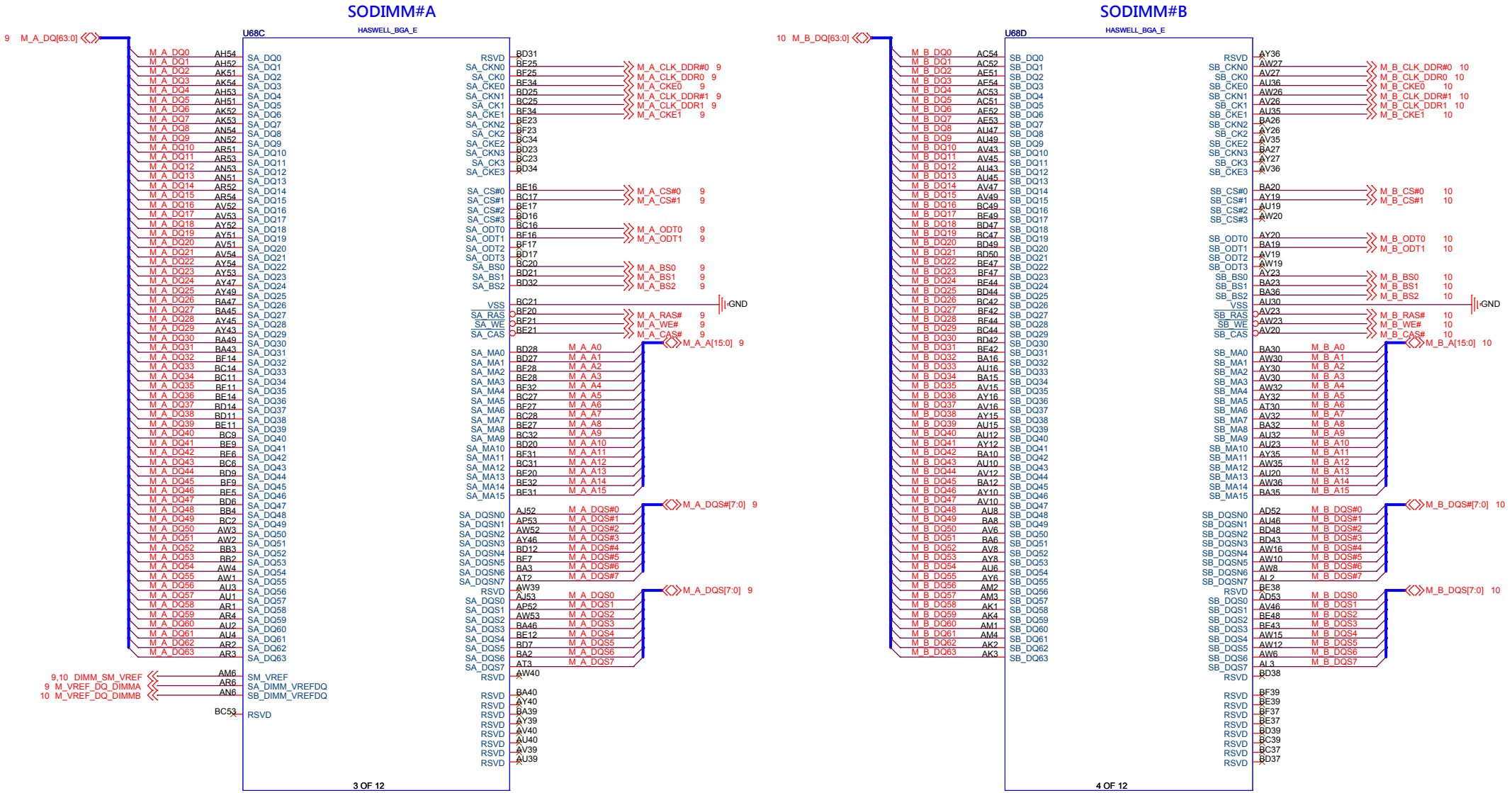
Haswell (DDR3L)



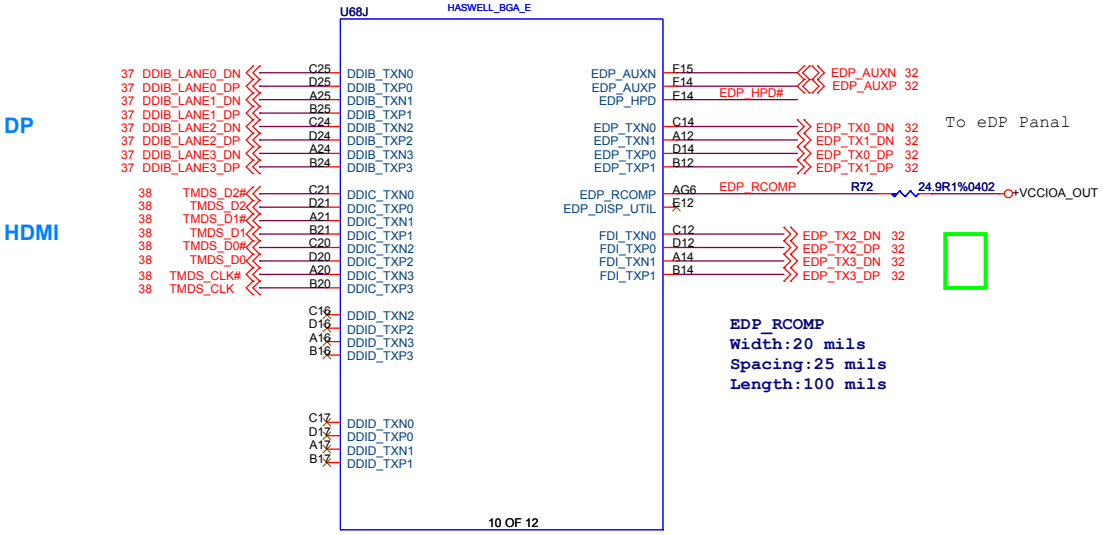
MICRO-STAR INT'L CO.,LTD.

Title: CPU-2 (DDR3L)

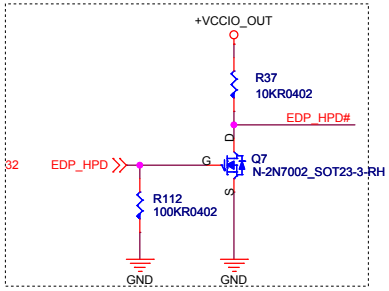
Size | Document Number: MS-16J2 | Rev: 0A

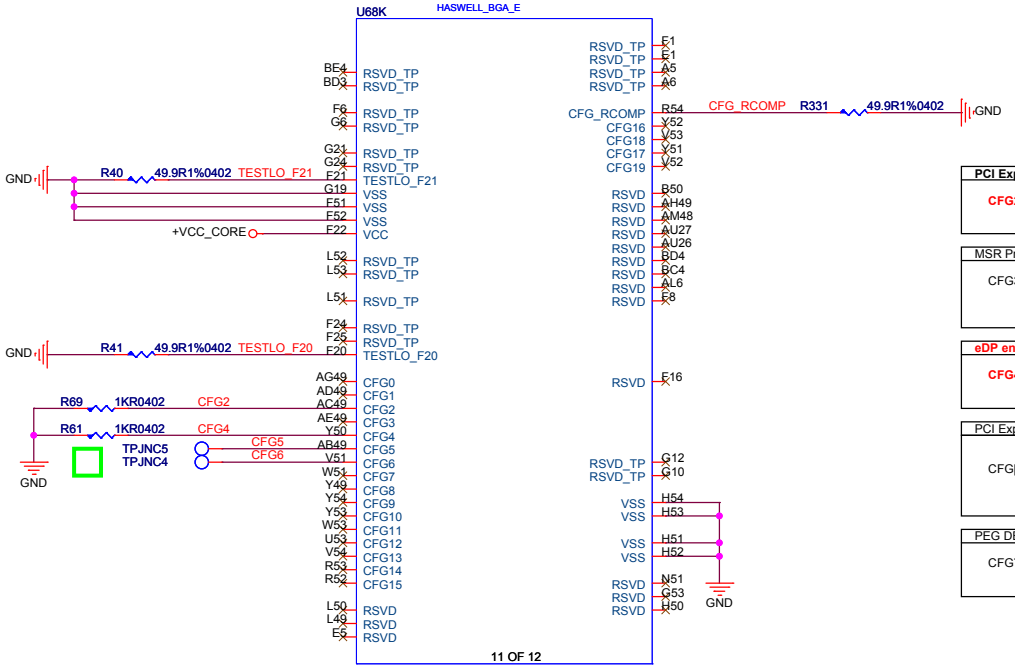
Date: Thursday, October 16, 2014 | Sheet 4 of 59

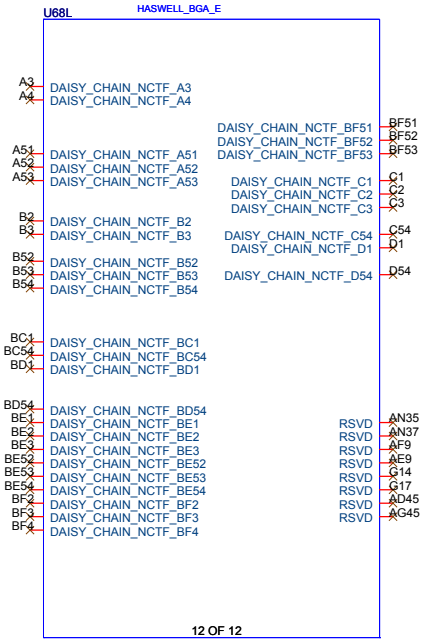
Display/Reserved



EDP_RCOMP
Width:20 mils
Spacing:25 mils
Length:100 mils







PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title: CPU-3 (Display/Reserved)

Size | Document Number: MS-16J2 | Rev: 0A

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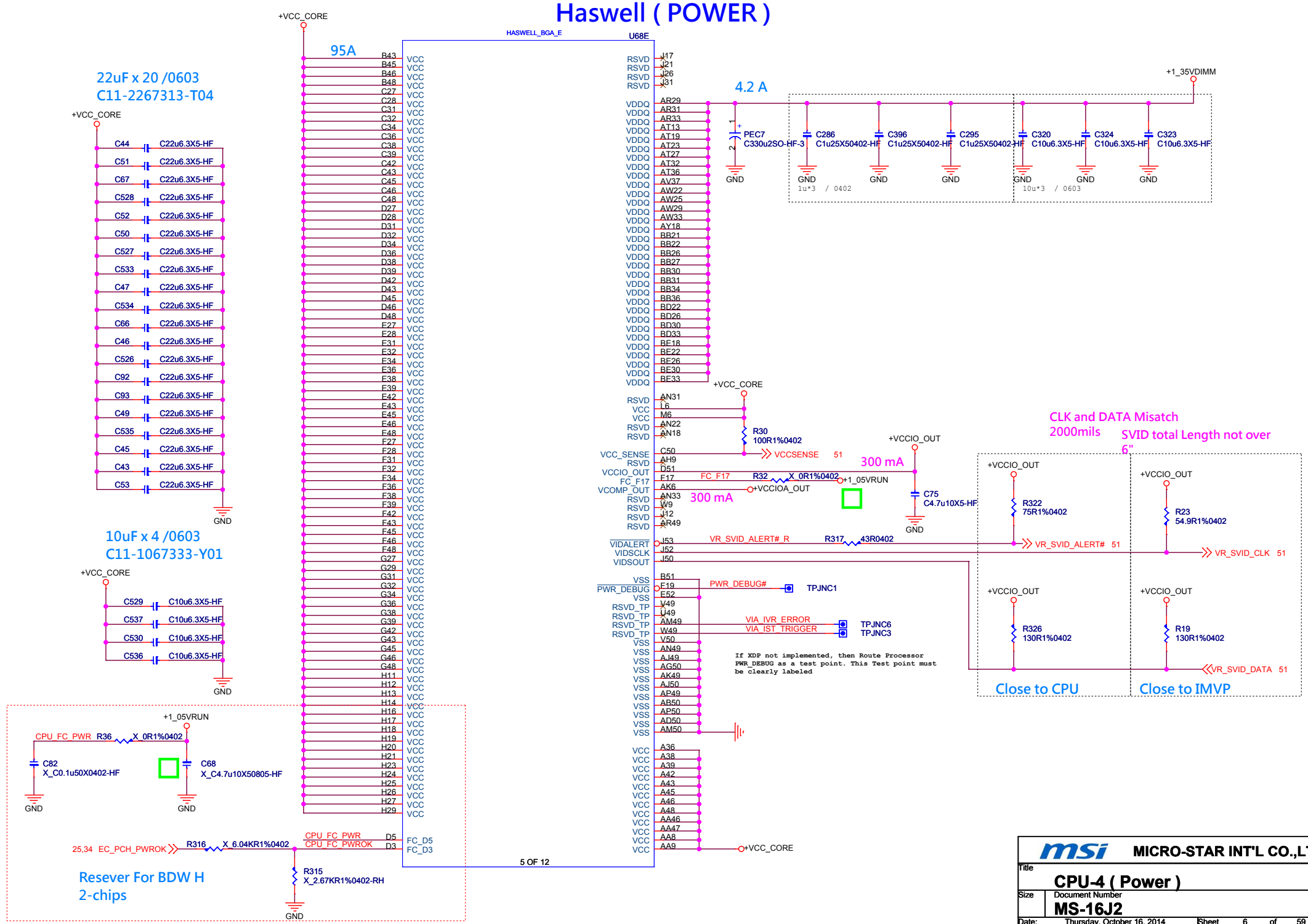
Haswell (POWER)



Title	CPU-4 (Power)
Size	Document Number: MS-16J2
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Date:	Thursday, October 16, 2014
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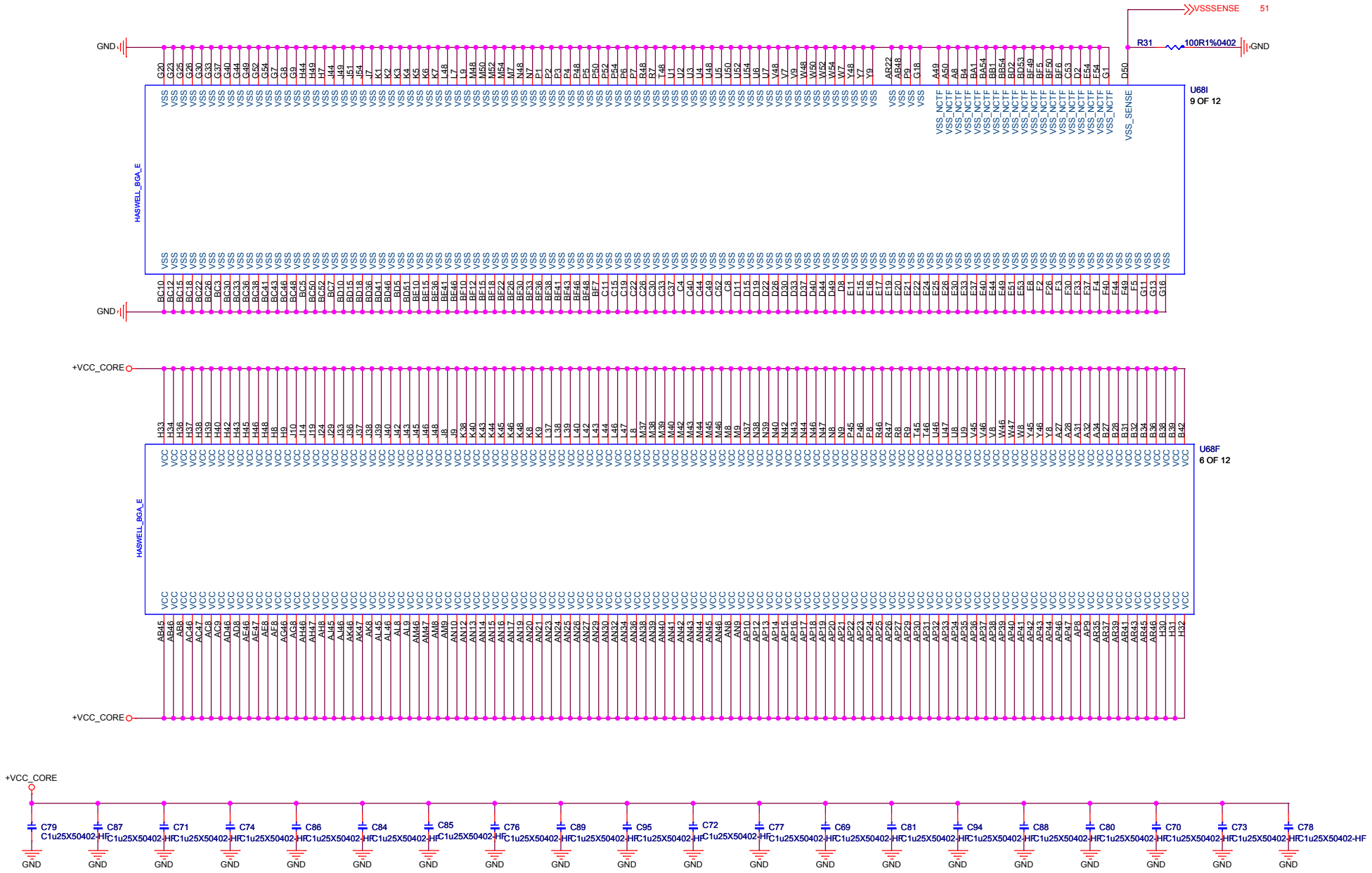
MICRO-STAR INT'L CO.,LTD.

Haswell (Power & GND)



MICRO-STAR INT'L CO.,LTD.

Title: CPU-6 (Power & GND)

Size | Document Number: MS-16J2 | Rev: 0A

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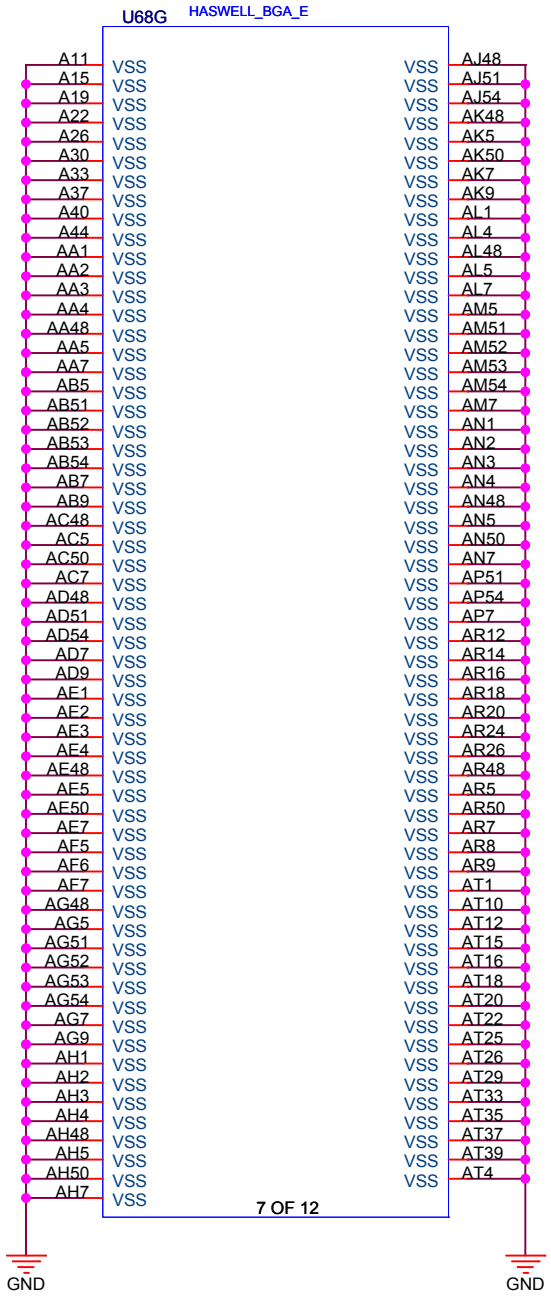
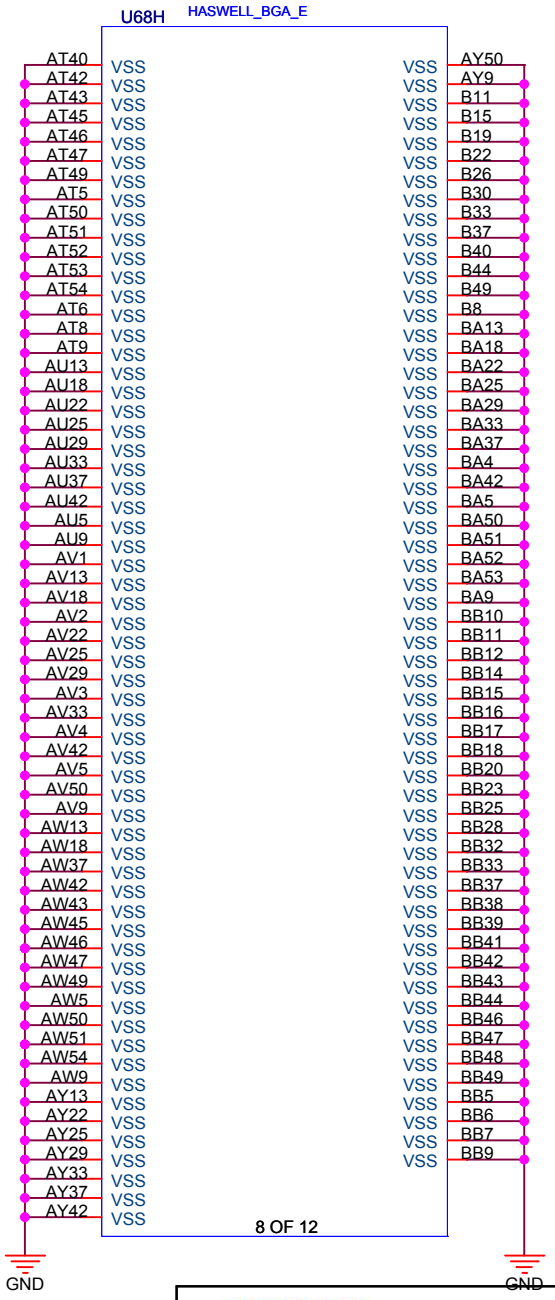
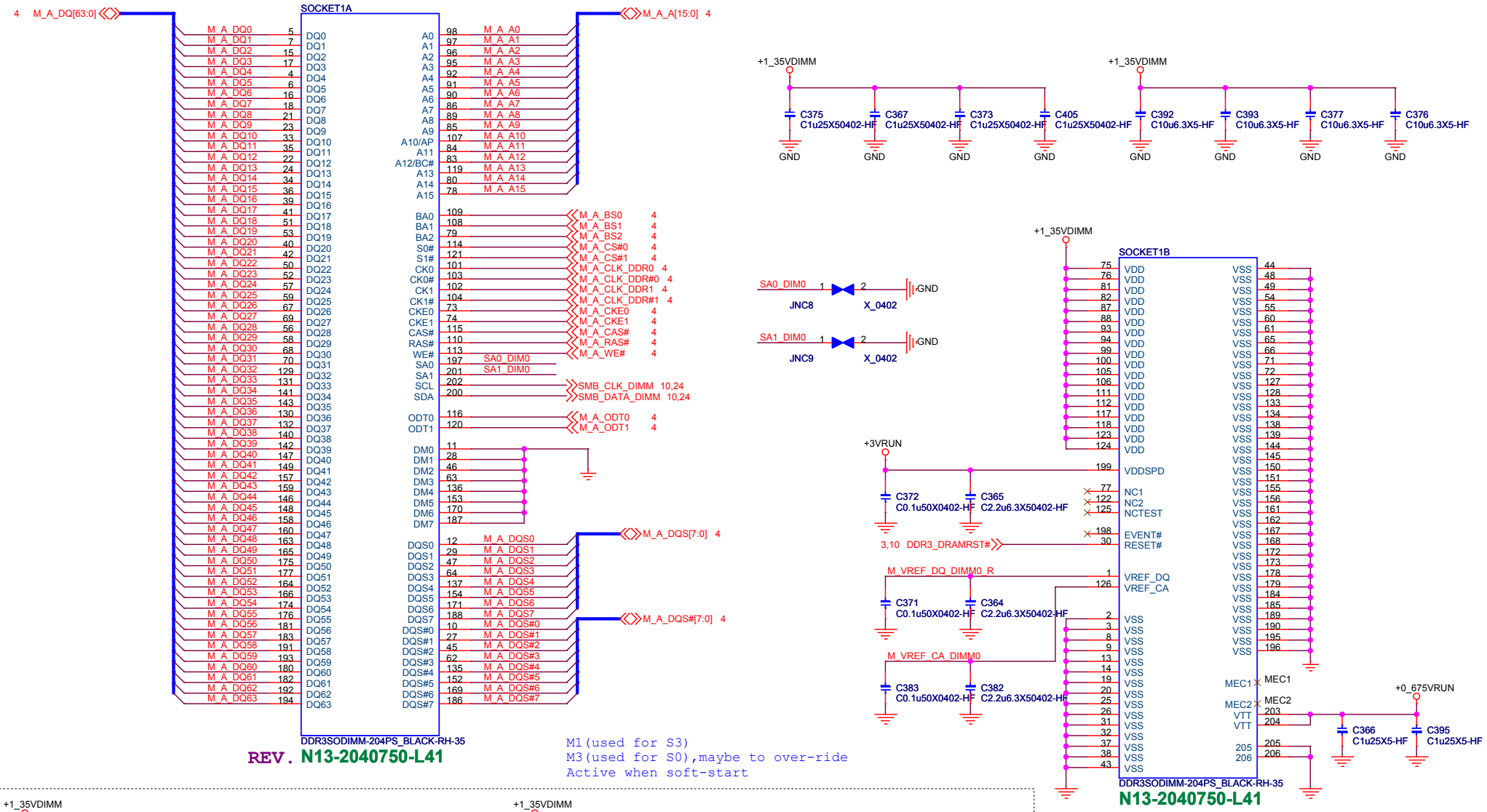
Haswell (GND)

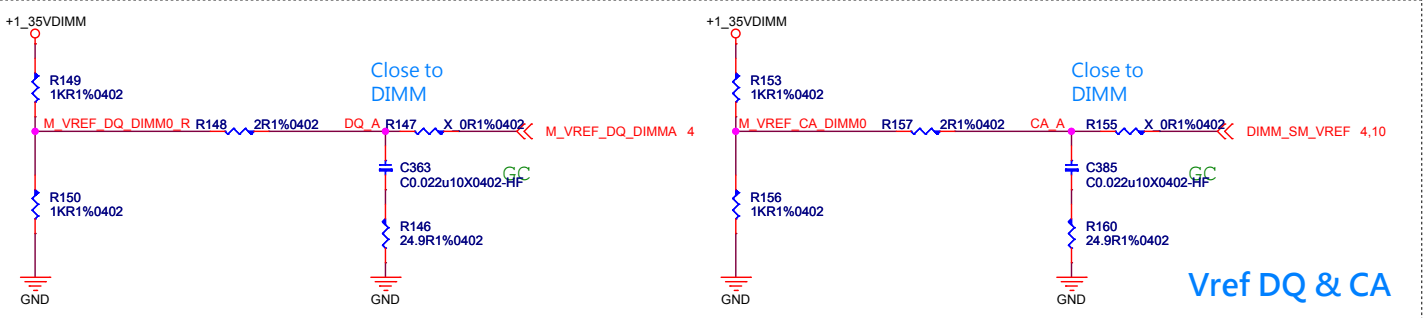




MICRO-STAR INT'L CO.,LTD.		
Title: CPU-5 (GND)		
Size	Document Number: MS-16J2	Rev: 0A
Date: Thursday, October 16, 2014	Sheet 8 of 59	

SODIMM#A





MICRO-STAR INT'L CO.,LTD.		
Title: DDR3L SODIMM 0		
Size	Document Number: MS-16J2	Rev: 0A
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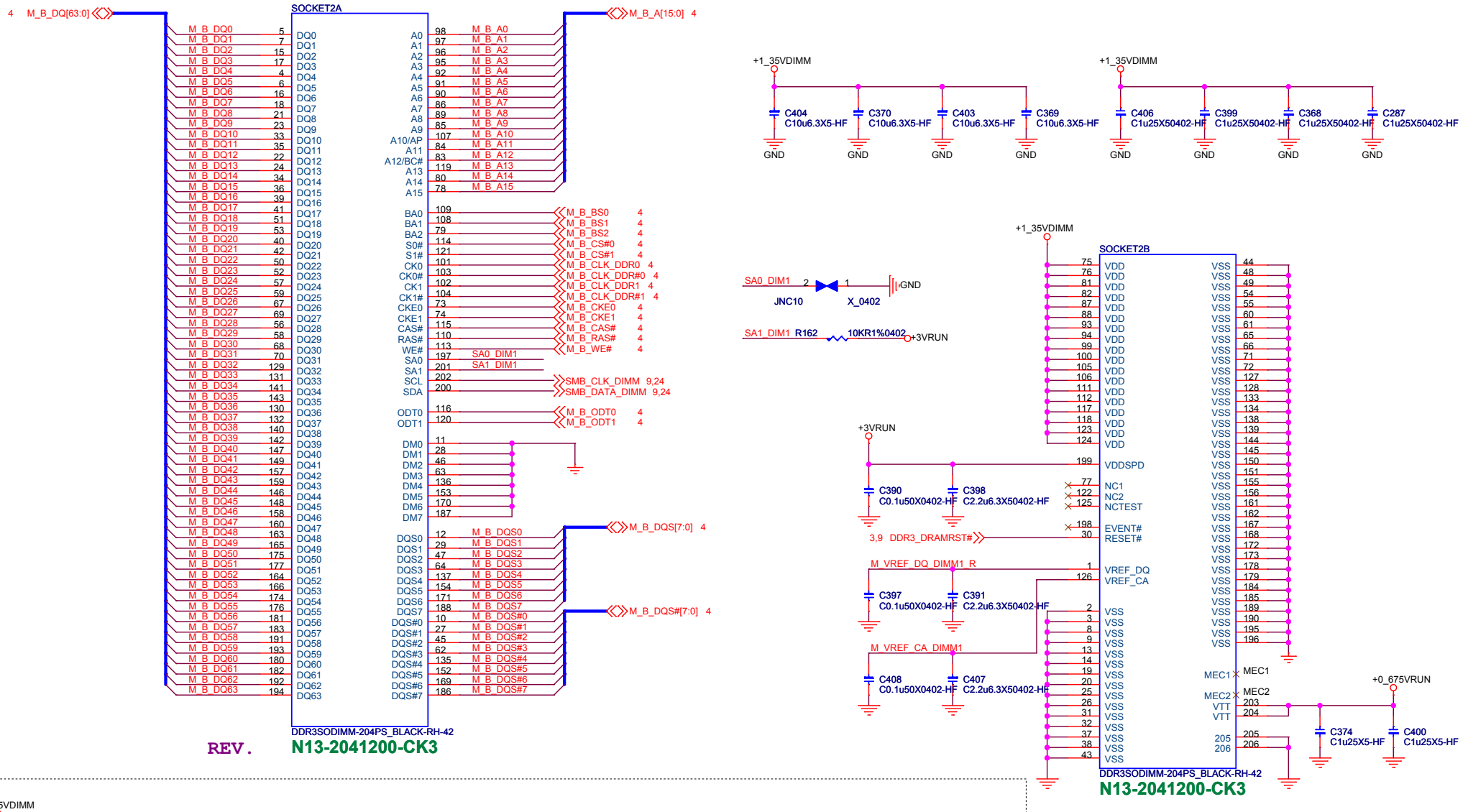
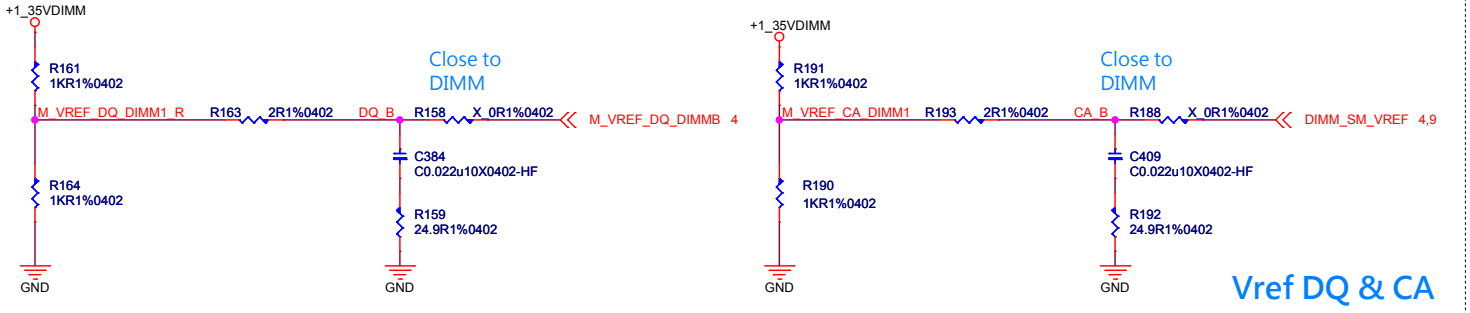
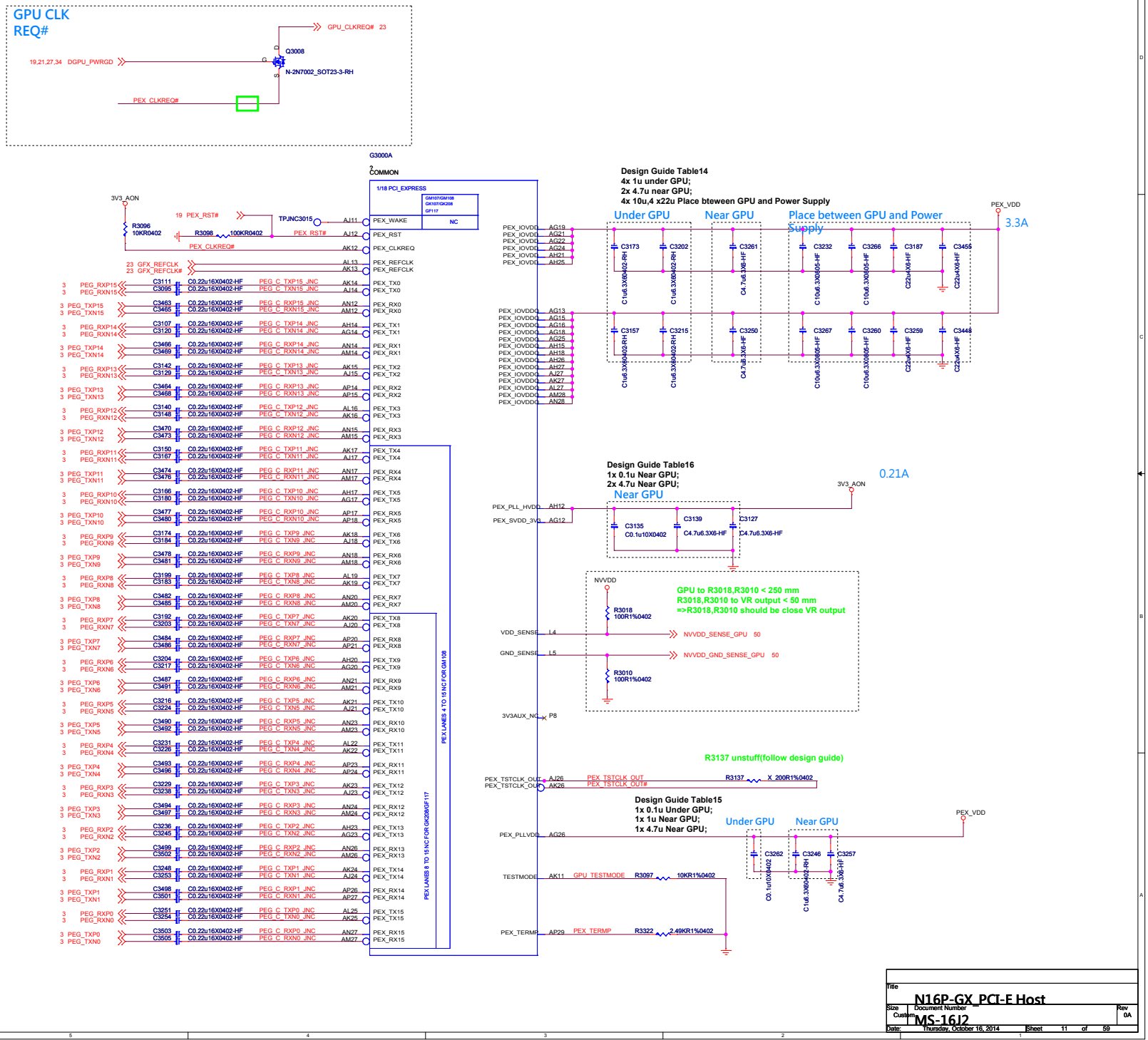
SODIMM#B





MICRO-STAR INT'L CO.,LTD.		
Title: DDR3L SODIMM 1		
Size	Document Number: MS-16J2	Rev: 0A
Date: Thursday, October 16, 2014	Sheet 10 of 59	

N16P-GX(PCI-Express Gen3 x16 Interface)



Title	N16P-GX_PCI-E Host	
Size: Custom	Document Number: MS-16J2	Rev: 0A
Date: Thursday, October 16, 2014	Sheet 11 of 59	

N16P-GX(Frame Buffer Interface)

GC6M is GC6 2.0 that it is for N15x or later GPU
So we use CRB GC6M design

G3000B
?
COMMON

2/18 FBA

FB_CLAMP E1 — R3278 10KR0402

FB_DLL_AVDD K27 — FBA_PLLAVDD

Under GPU
C3249
C0.1u10X0402

FBA_D0 L28 … FBA_D63 AG33
FBA_DBI0 P30 … FBA_DBI7 AF34
FBA_EDC0 M31 … FBA_EDC7 AF33
FBA_DQS_WP0 … FBA_DQS_WP7
FBA_DQS_RN0 … FBA_DQS_RN7

FBA_DEBUG0 NC
FBA_DEBUG1 NC
GK107/GK208 GF117 / GM107/GM108

FBA_WCKBxx ARE RESERVED,NC ON: GM108/GM107 GK208/GF117
USED ONLY ON: GK107

TPJNC3019 FB_VREF H26 FB_VREF

FBA_PLL_AVDD U27 — Under GPU — Near GPU — FBA_PLLAVDD

C3244 C0.1u10X0402
C3252 C22uA/6.4-HF

PEX_VDD
L3006 30L1.7A-50_0402-RH

FBA_CMD0 U30 … FBA_CMD31 AC32
FBA_CLK0 R30 … FBA_CLK1# AC31
FBA_WCK01 K31 … FBA_WCK67# AJ34

GDDR5 CMD Mapping Mode H Table

<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE*
13	29	RESET*

G3000C
?
COMMON

3/18 FBB

ALL PINS NC FOR GM108/ GK208/GF117

FBB_D0 G9 … FBB_D63 C26
FBB_DBI0 E11 … FBB_DBI7 A24
FBB_EDC0 D10 … FBB_EDC7 A23
FBB_DQS_WP0 … FBB_DQS_WP7
FBB_DQS_RN0 … FBB_DQS_RN7

FBB_DEBUG0 NC
FBB_DEBUG1 NC
GK107 / GM107

FBB_WCKBxx ARE RESERVED,NC ON: GM108/GM107
USED ONLY ON: GK107

FBB_PLL_AVDD H17 — FBA_PLLAVDD

Under GPU
C3185
C0.1u10X0402

FBB_CMD0 D13 … FBB_CMD31 E17
FBB_CLK0 D12 … FBB_CLK1# F20
FBB_WCK01 F8 … FBB_WCK67# C27

FBVDDQ

R3177 R3173 R3303 R3321 10KR0402

FBA CKE H — FBA_CMD30 — FBB CKE H — FBB_CMD30
FBA CKE L — FBA_CMD14 — FBB CKE L — FBB_CMD14
FBA RST H — FBA_CMD29 — FBB RST H — FBB_CMD29
FBA RST L — FBA_CMD13 — FBB RST L — FBB_CMD13

R3174 R3176 R3320 R3306 10KR0402

Title	N16P-GX_MEM IF A/B
Size	Custom
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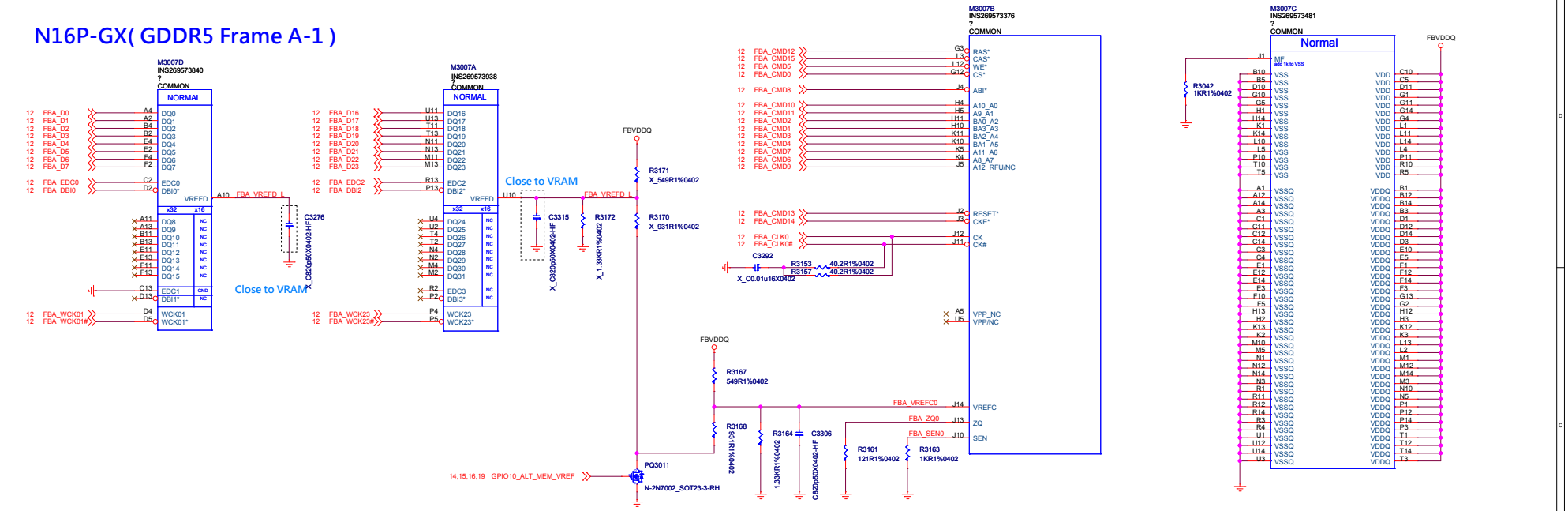
N16P-GX(GDDR5 Frame A-1)



Title	N16P-GX_GDDR5 Frame A-1		
Size	Document Number		Rev
Custom	MS-16J2		0A
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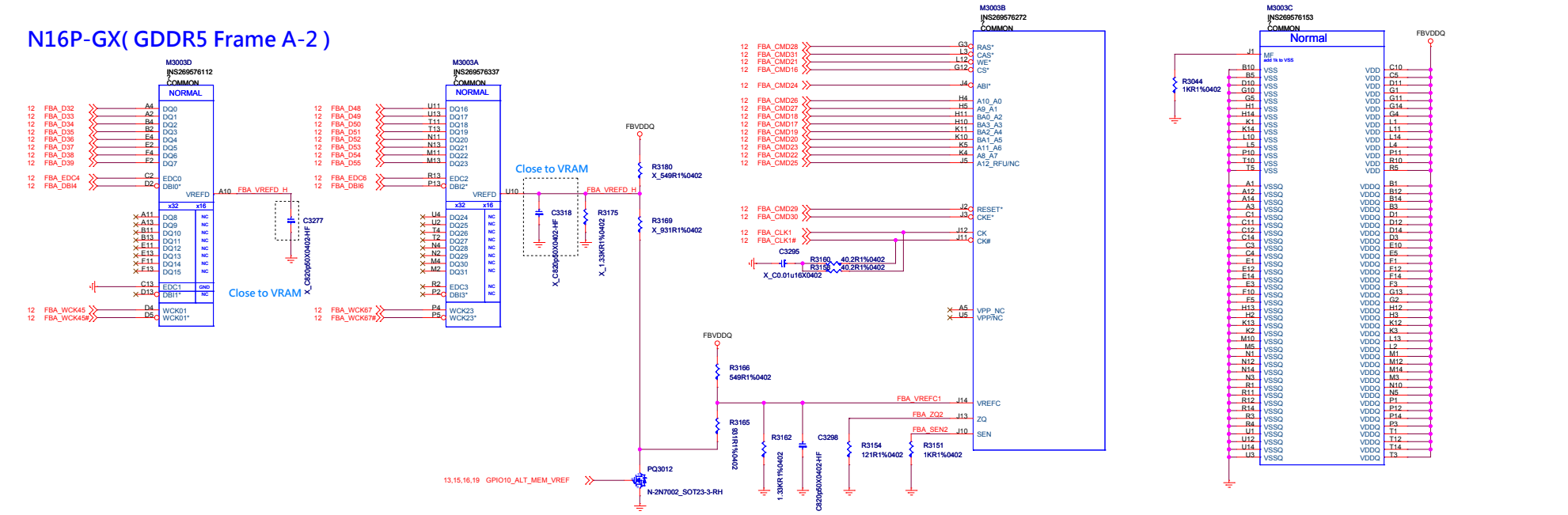
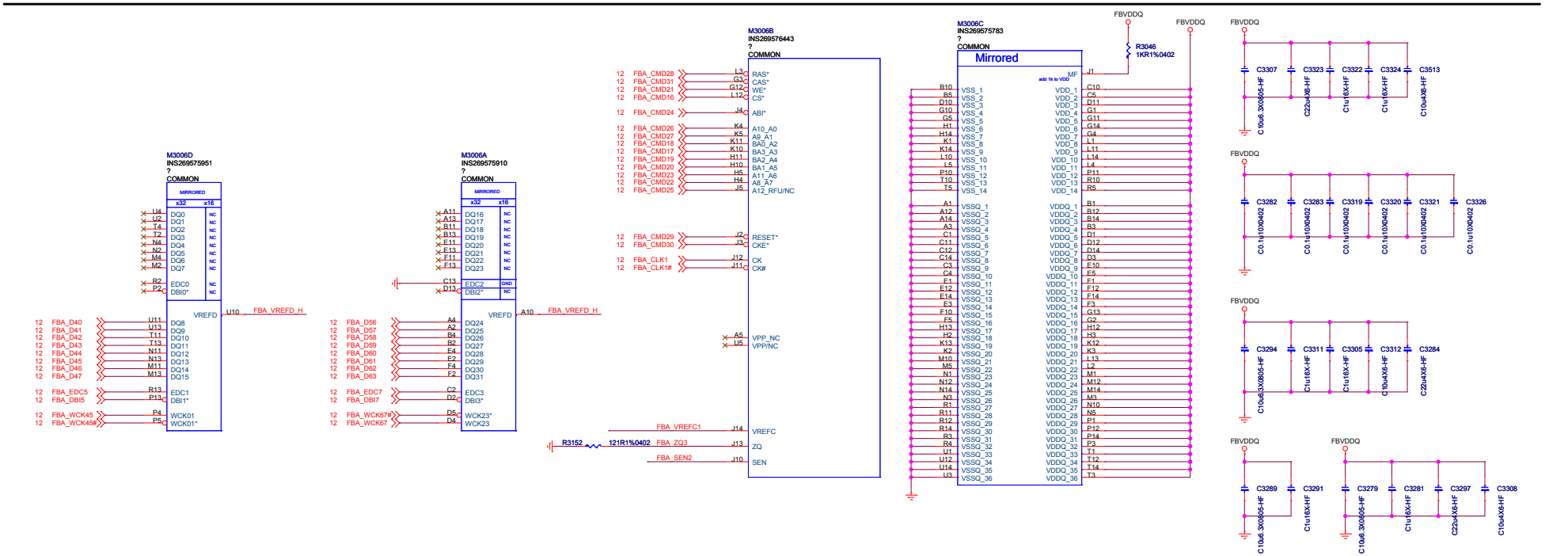
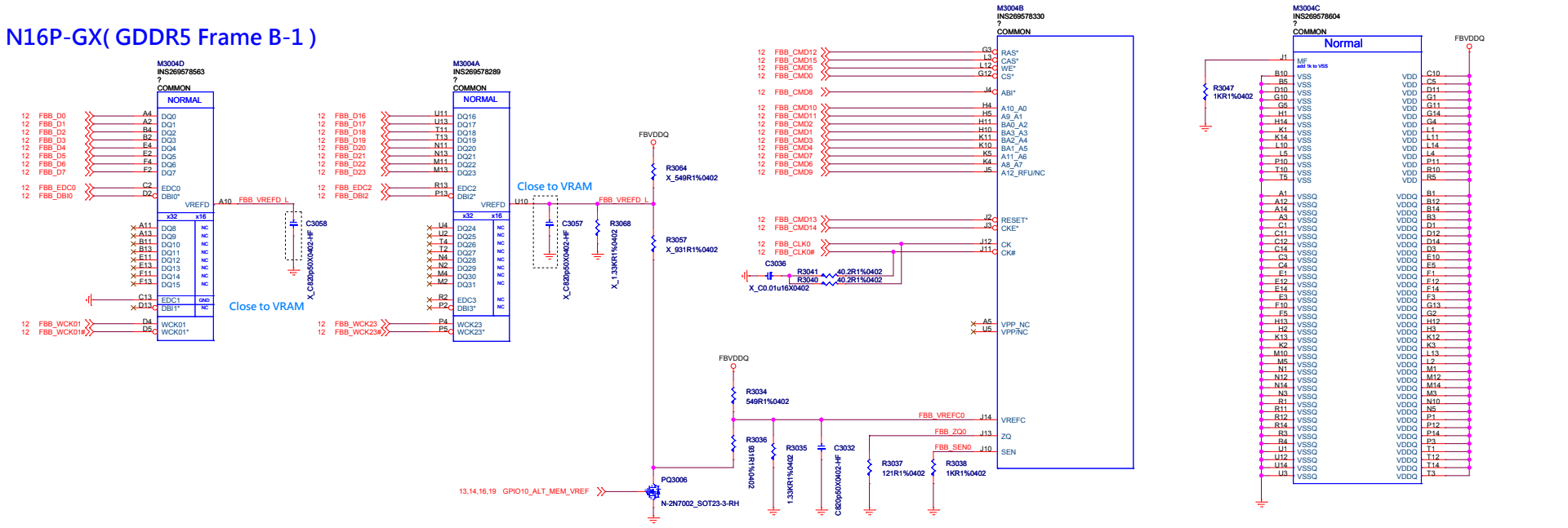
N16P-GX(GDDR5 Frame A-2)

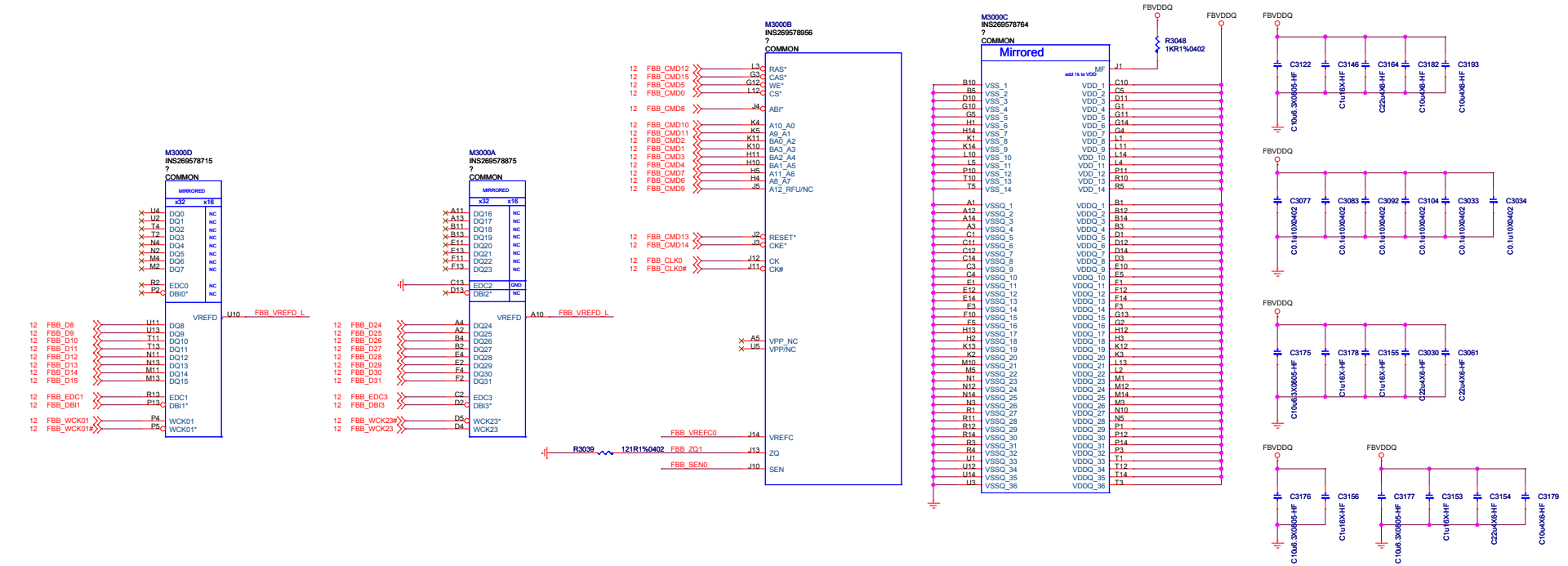




Title	N16P-GX_GDDR5 Frame A-2		
Size	Document Number		Rev
Custom	MS-16J2		0A
Date:	Thursday, October 16, 2014	Sheet	14 of 59

N16P-GX(GDDR5 Frame B-1)





Title	N16P-GX_GDDR5 Frame B-1		
Size	Document Number		Rev
Custom	MS-16J2		0A
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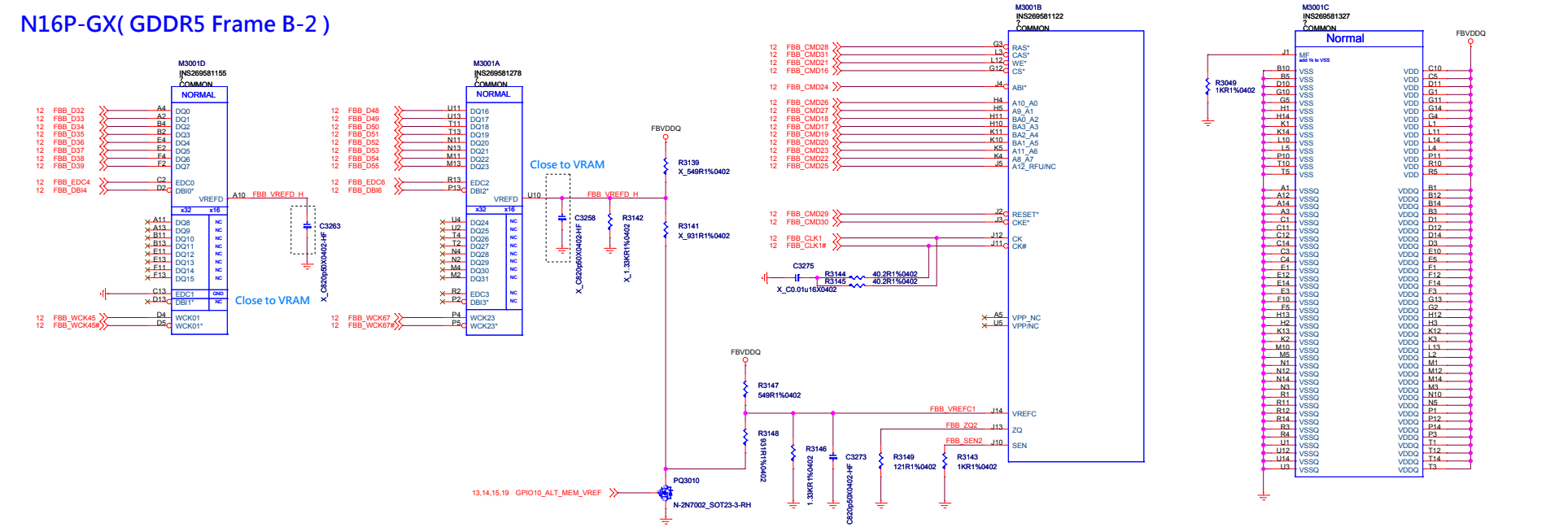
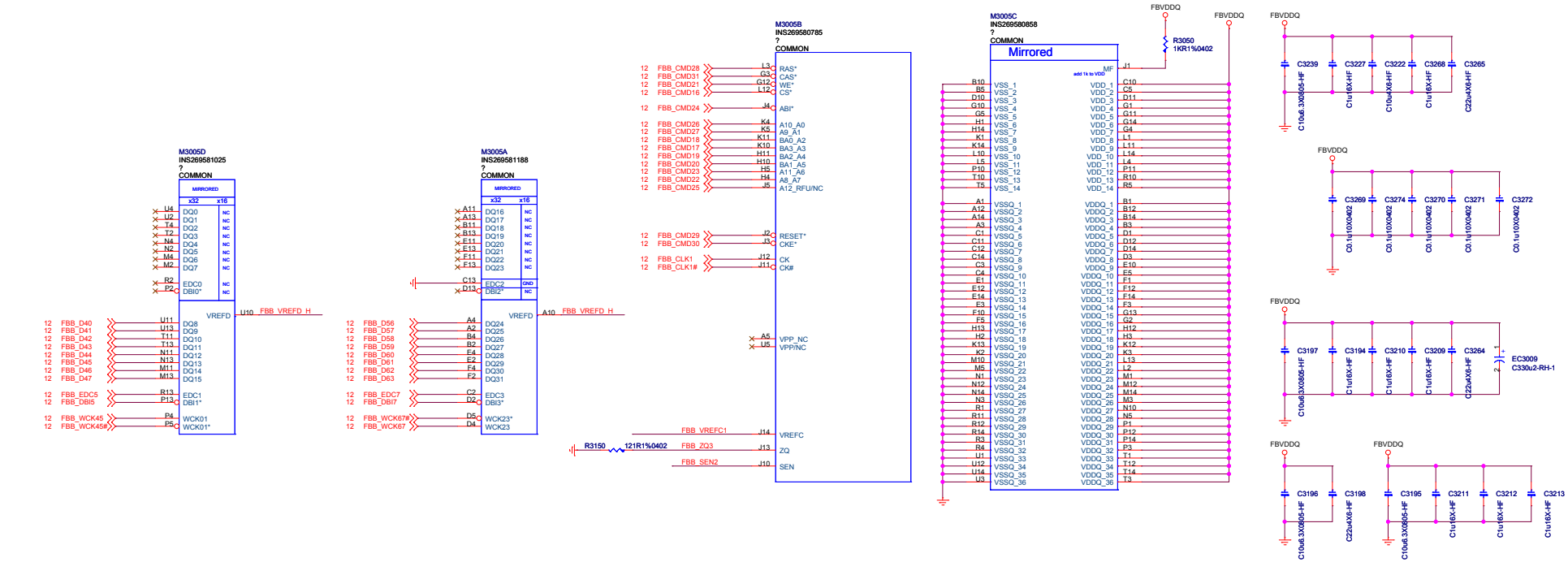
N16P-GX(GDDR5 Frame B-2)





Title	N16P-GX_GDDR5 Frame B-2
Size	Custom
Document Number	MS-16J2
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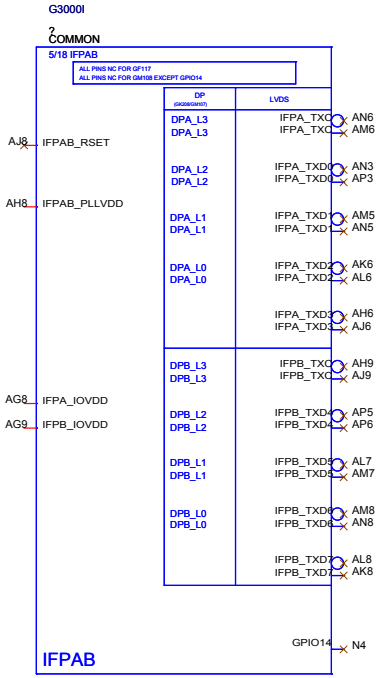
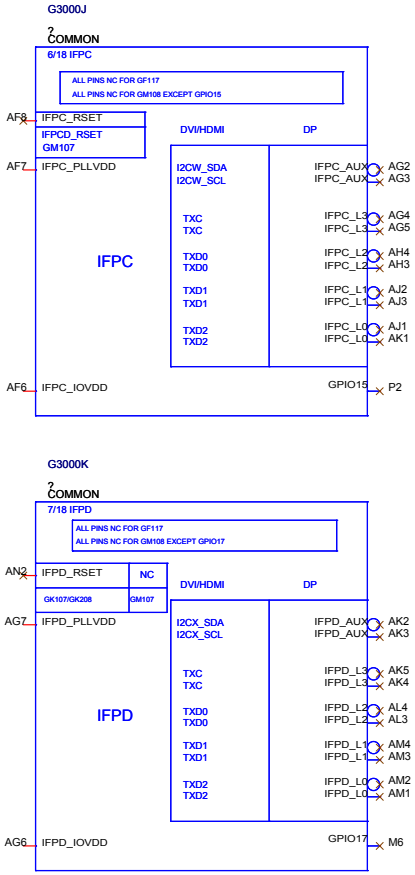
N16P-GX(Display IF)

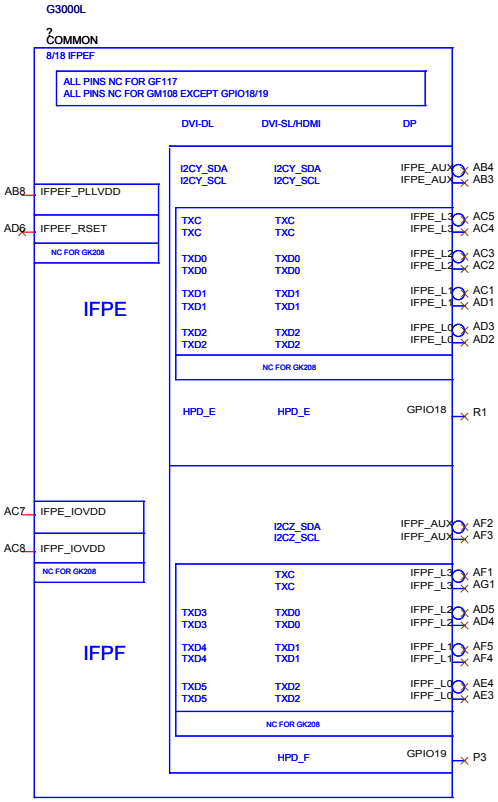
IFP A/B LVDSDual Link



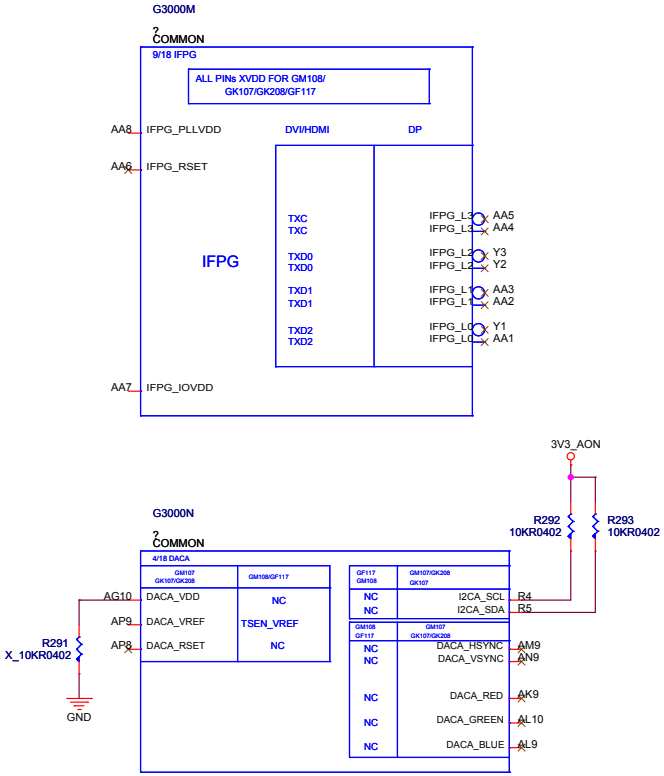
IFP C Native HDMI OR DP



IFP E/F Dual Link TMDS DVI-I



DAC A VGA



Title	N16P-GX_Display IF	
Size: Custom	Document Number: MS-16J2	Rev: 0A
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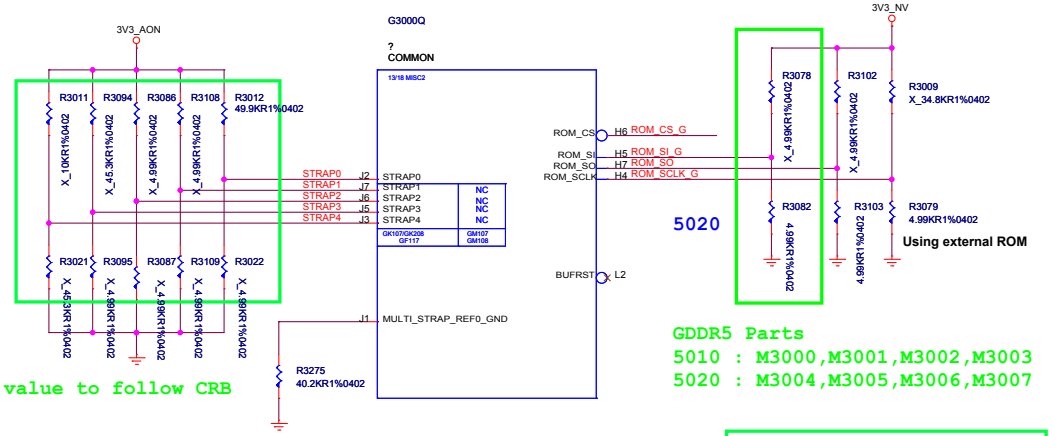
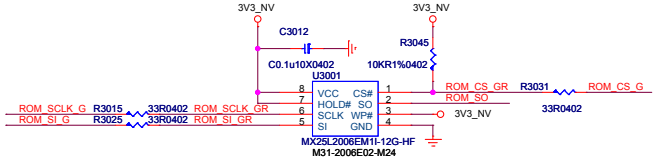
ROM, MULTI-LEVEL STRAPS



Modify R value to follow CRB

GDDR5 Parts
5010 : M3000,M3001,M3002,M3003
5020 : M3004,M3005,M3006,M3007

External EEPROM

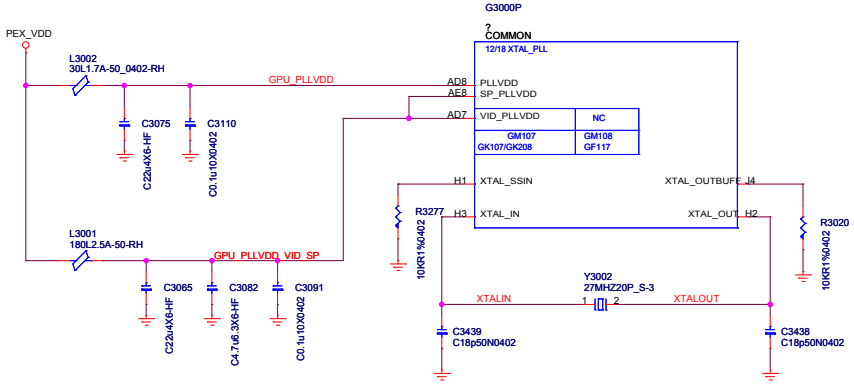


M31-2006E02-M24

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

Samsung GDDR5 : M12-2032565-S02
Hynix GDDR5 : M12-5GQ2H85-H23
Micron GDDR5 : M12-2032B95-M30

ROM_SI	RAM_CFG[3:0]	0x0 4.99K PD Samsung 128x16bit 0x1 10K PD Hynix 128x16bit 0x5 30.1K PD Micron 128x16bit
ROM_SO	DEVID_SEL PCIE_CFG SMB_ALT_ADDR VGADEVICE	5K PD
ROM_SCLK	SOR_EXposed[3:0]	5K PD
STRAP0		50K PU 3V3_AON
STRAP1		Reserved
STRAP2		Reserved
STRAP3		Reserved
STRAP4		Reserved

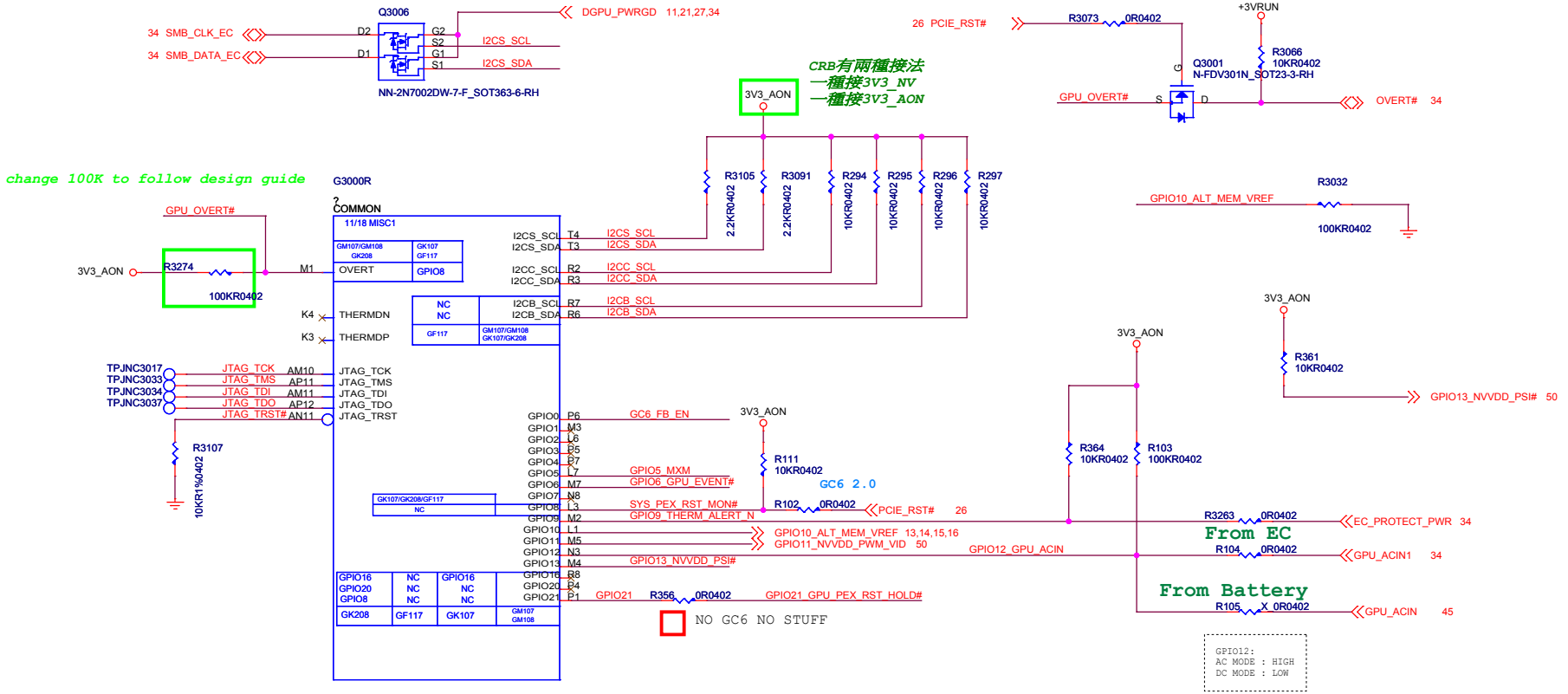


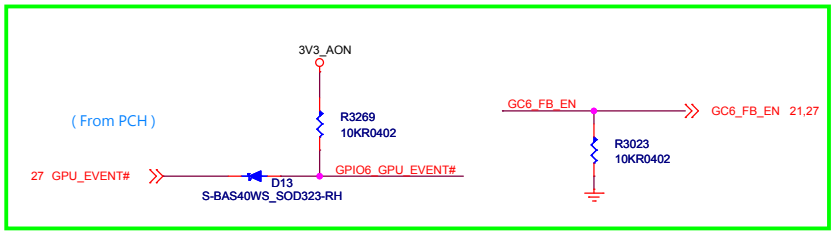
DEFAULT SETTING

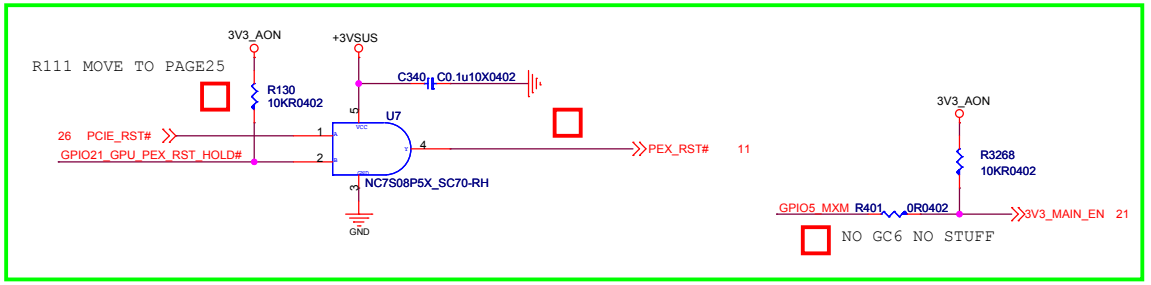
BOT 記得轉階層

ROM_S1 Samsung	V_TOP1		V_BOT1
128Mx16bit	5010		5020
R11-4991T12-W08	M12-2032585-S02		M12-2032585-S02
X_4.99KR1%0402	X_K4G20325FD-FC03		X_K4G20325FD-FC03
ROM_H1 Hynix	V_TOP2		V_BOT2
128Mx16bit	5010		5020
R11-0103T12-W08	M12-5GC2H05-H23		M12-5GC2H05-H23
X_10KR1%0402	X_H5GC2H24BFR-T2C-HF		X_H5GC2H24BFR-T2C-HF
ROM_M1 Micron	V_TOP3		V_BOT3
128Mx16bit	5010		5020
R11-3012T12-W08	M12-2032B95-M30		M12-2032B95-M30
X_30.1KR1%0402	X_EDW2032BBBG-6A-F		X_EDW2032BBBG-6A-F

Title	N16P-GX_ROM & HW Straps		
Size Custom	Document Number MS-16J2		Rev 0A
Date: Thursday, October 16, 2014	Sheet 18 of 59		

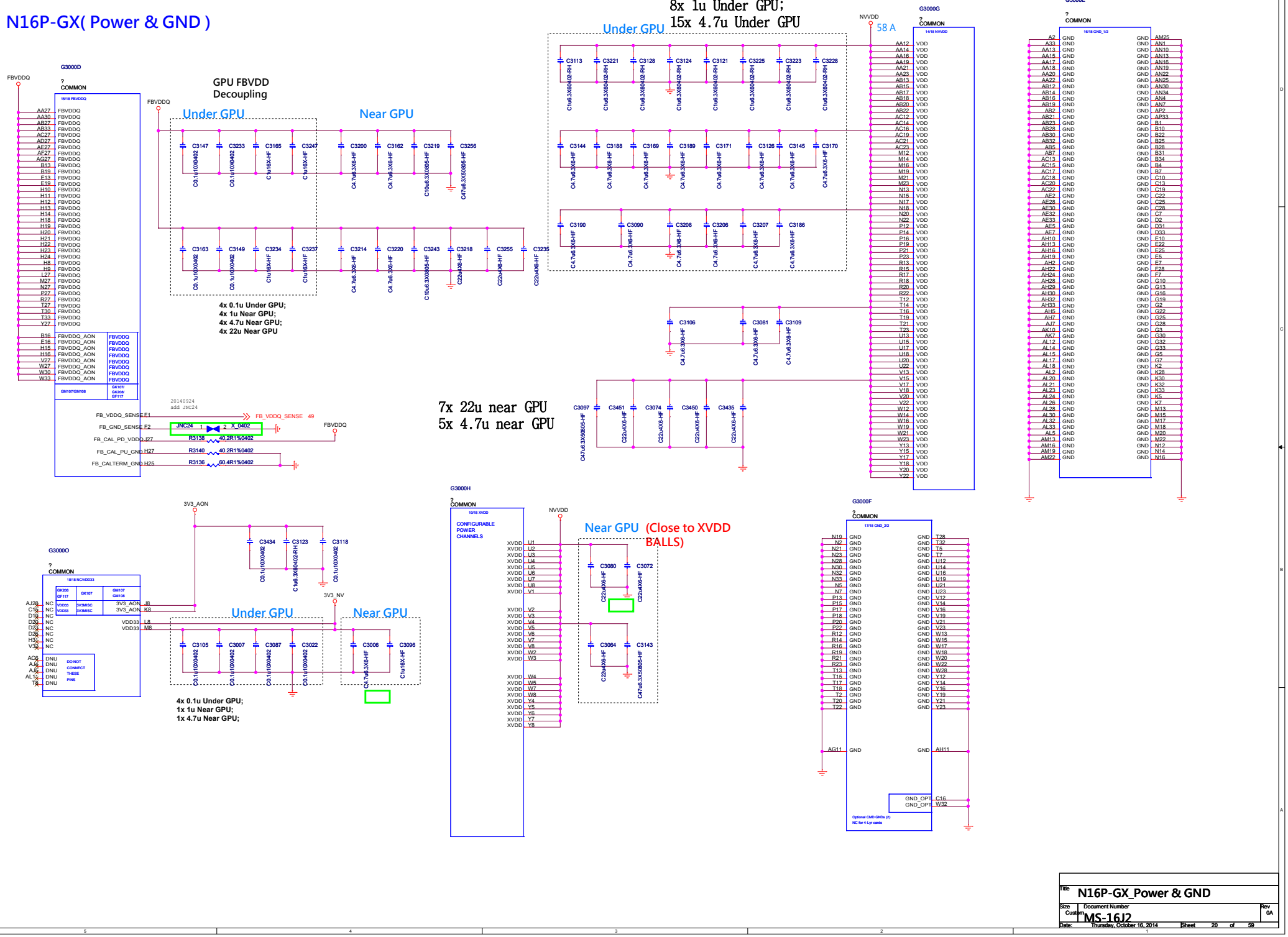






Title	N16P-GX_Thermal & GPIO	
Size: Custom	Document Number: MS-16J2	Rev: 0A
Date: Thursday, October 16, 2014	Sheet 19 of 59	

N16P-GX(Power & GND)



Title	N16P-GX_Power & GND
Size	Custom
Document Number	MS-16J2
Rev	0A
Date:	Thursday, October 16, 2014
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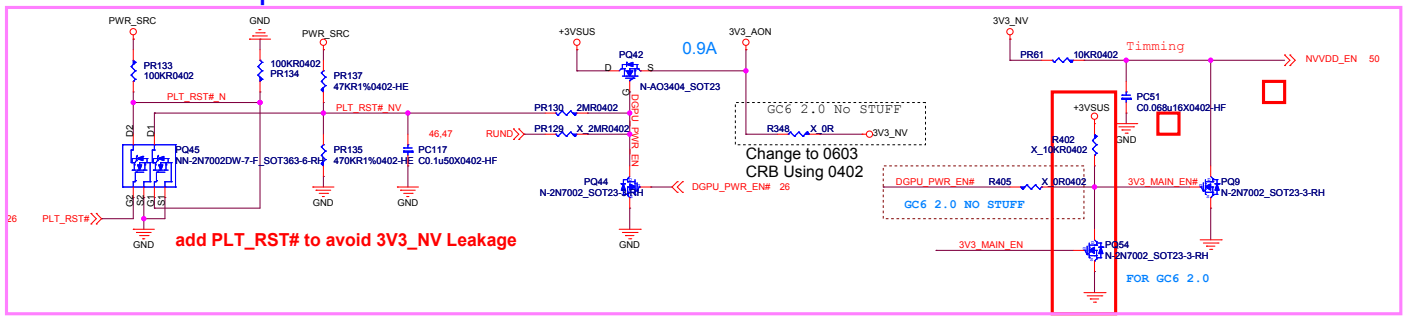
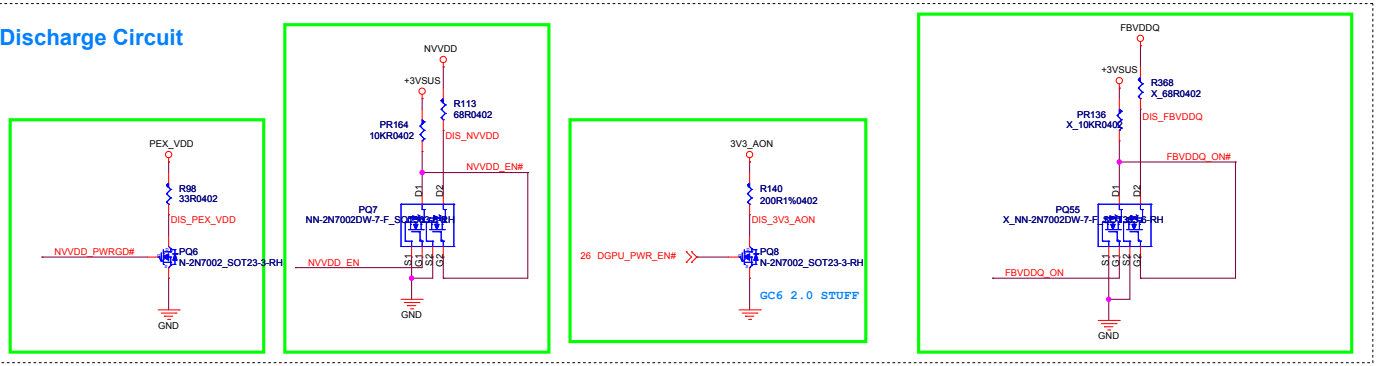
N16P-GX(Power Control)

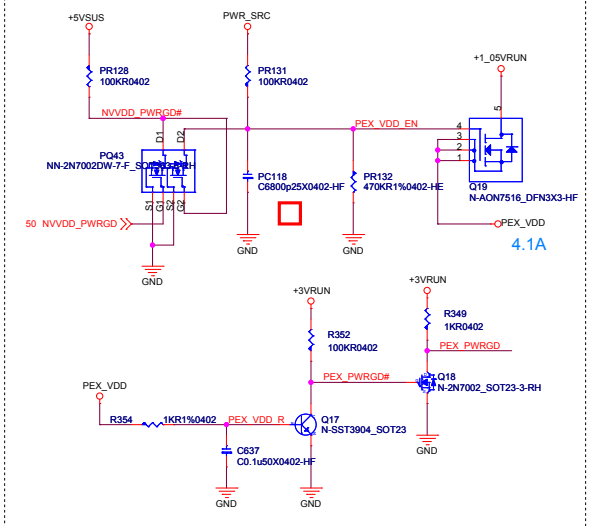
nVIDIA Power Sequence Control 3V3_AON -> 3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD

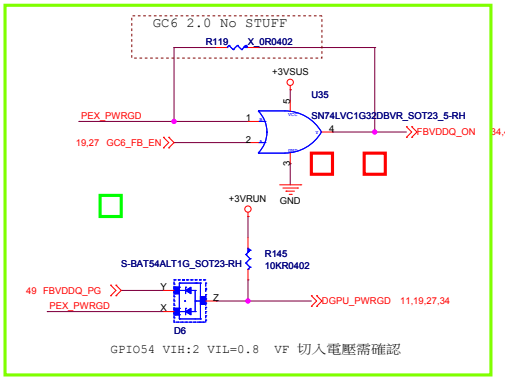


Discharge Circuit

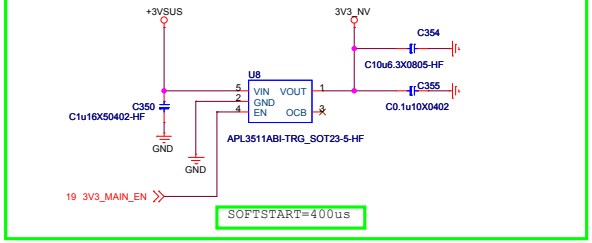


PEX_VDD





GC6 2.0 STUFF



Title	N16P-GX_Power Control		
Size Custom	Document Number MS-16J2		Rev 0A
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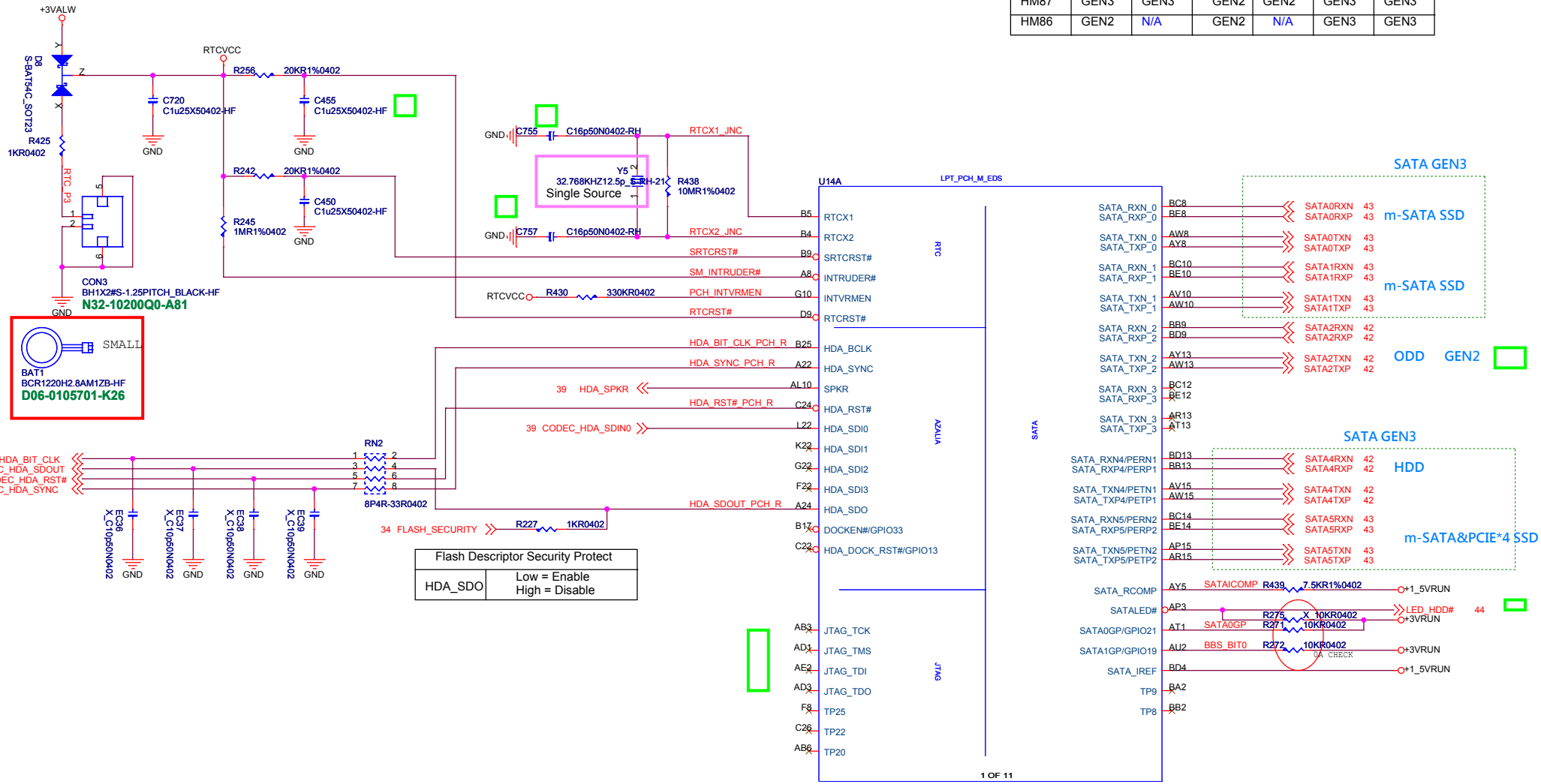
Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

Title: PCH-1 (HDA/JTAG/SATA)

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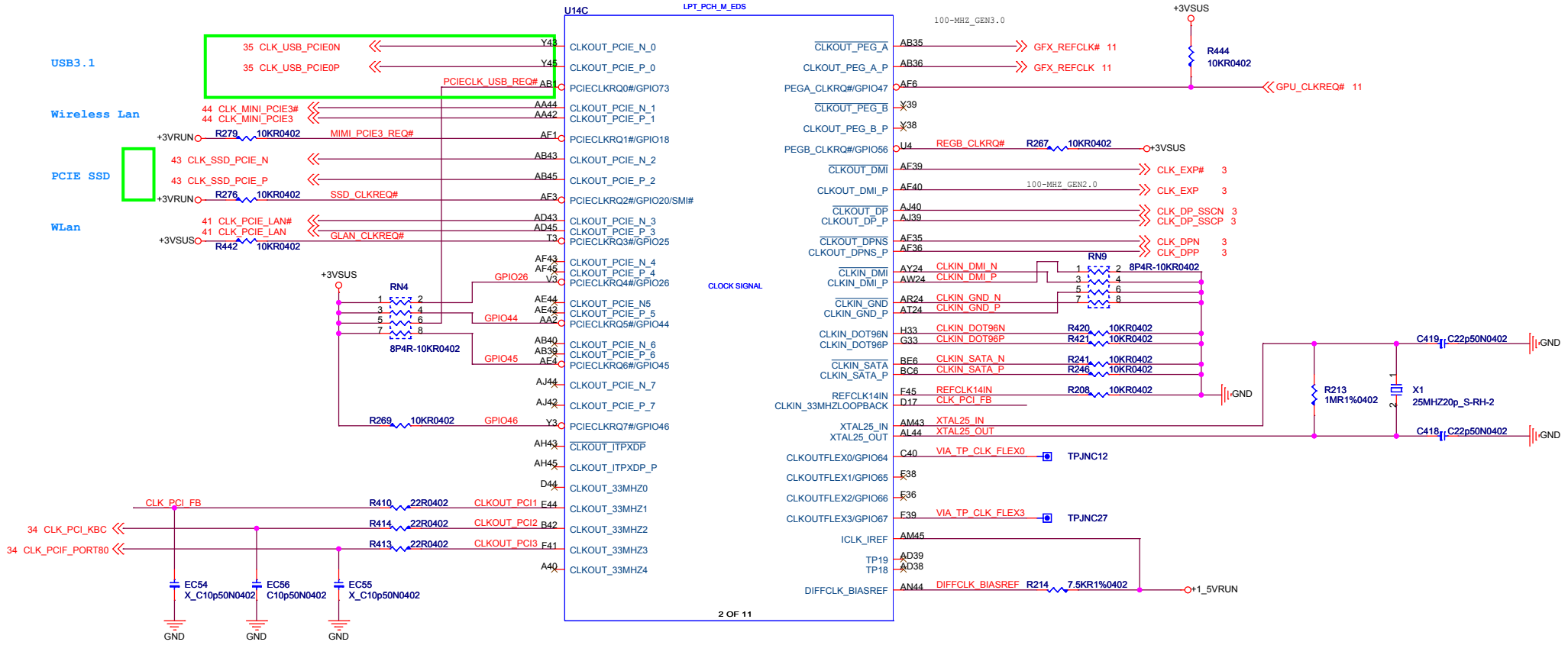
Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-2 (CLK)		
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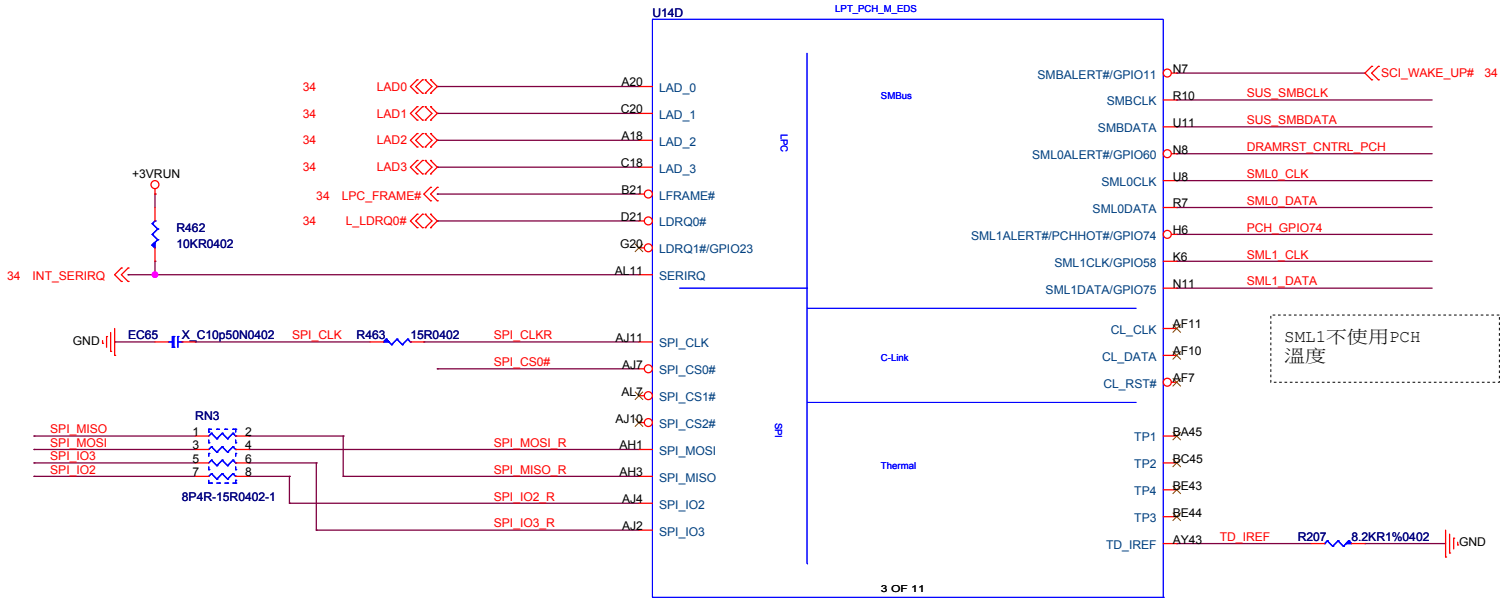
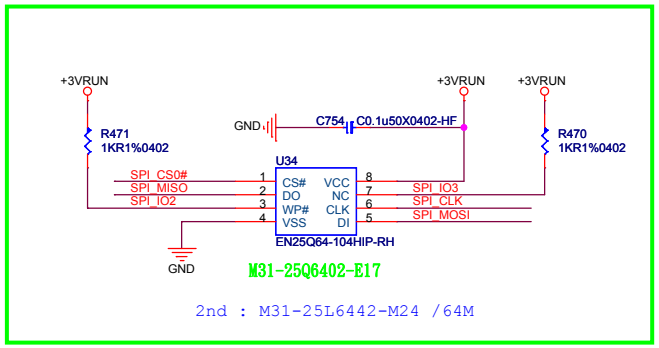
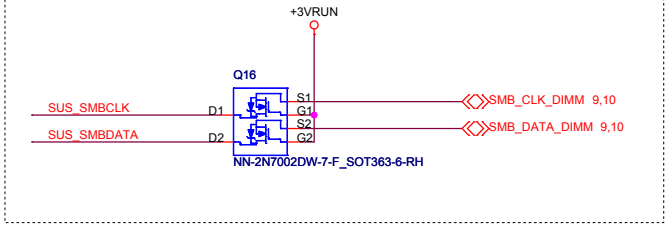
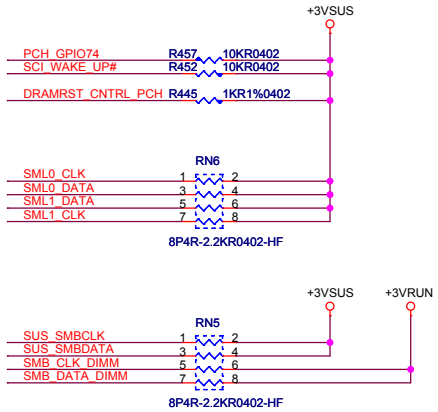
Lynx Point (LPC,SMBUS)









MICRO-STAR INT'L CO.,LTD.

Title: PCH-3 (LPC,SMBUS)

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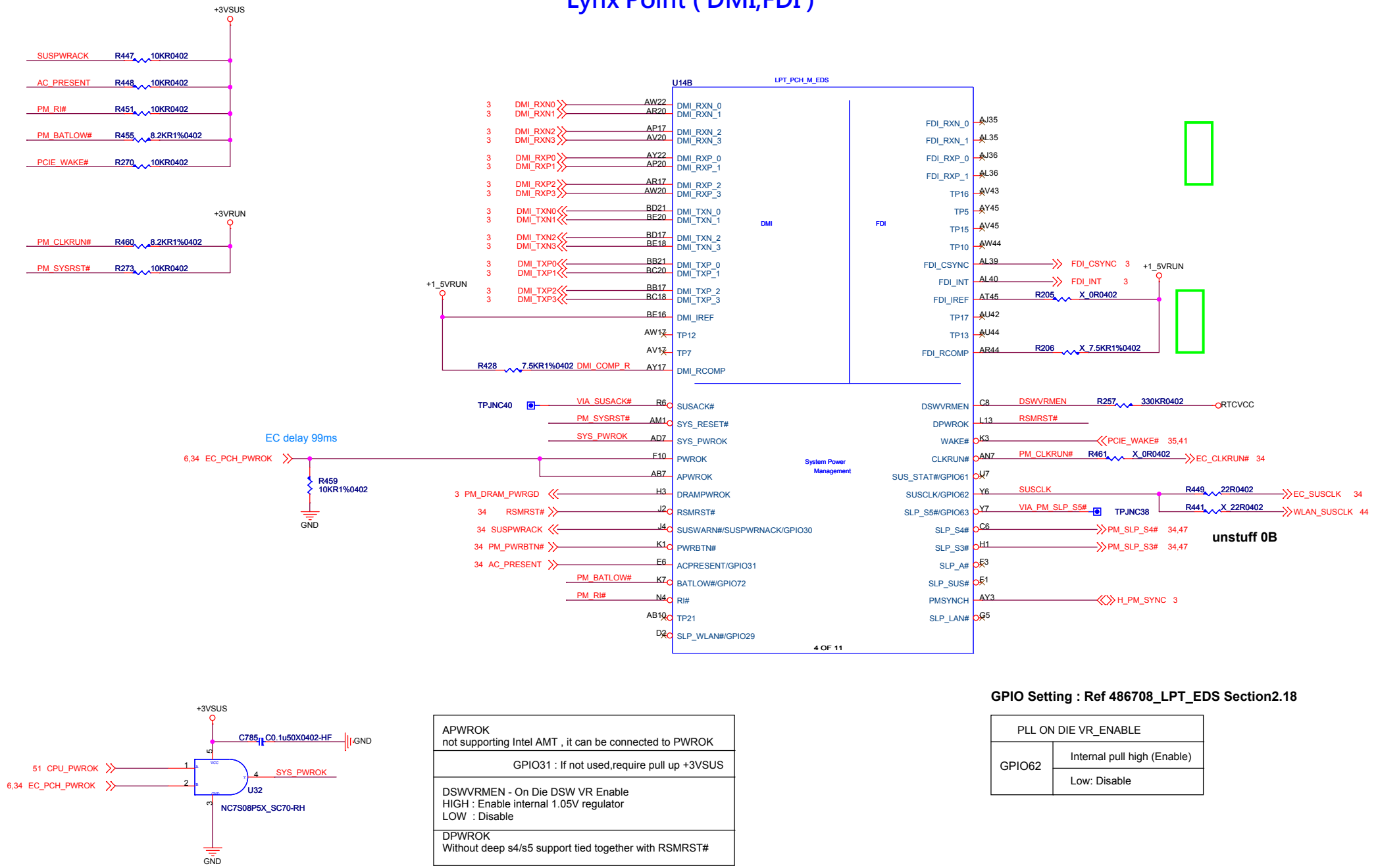
Lynx Point (DMI,FDI)



APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

MICRO-STAR INT'L CO.,LTD.

Title: PCH-4 (DMI,FDI)

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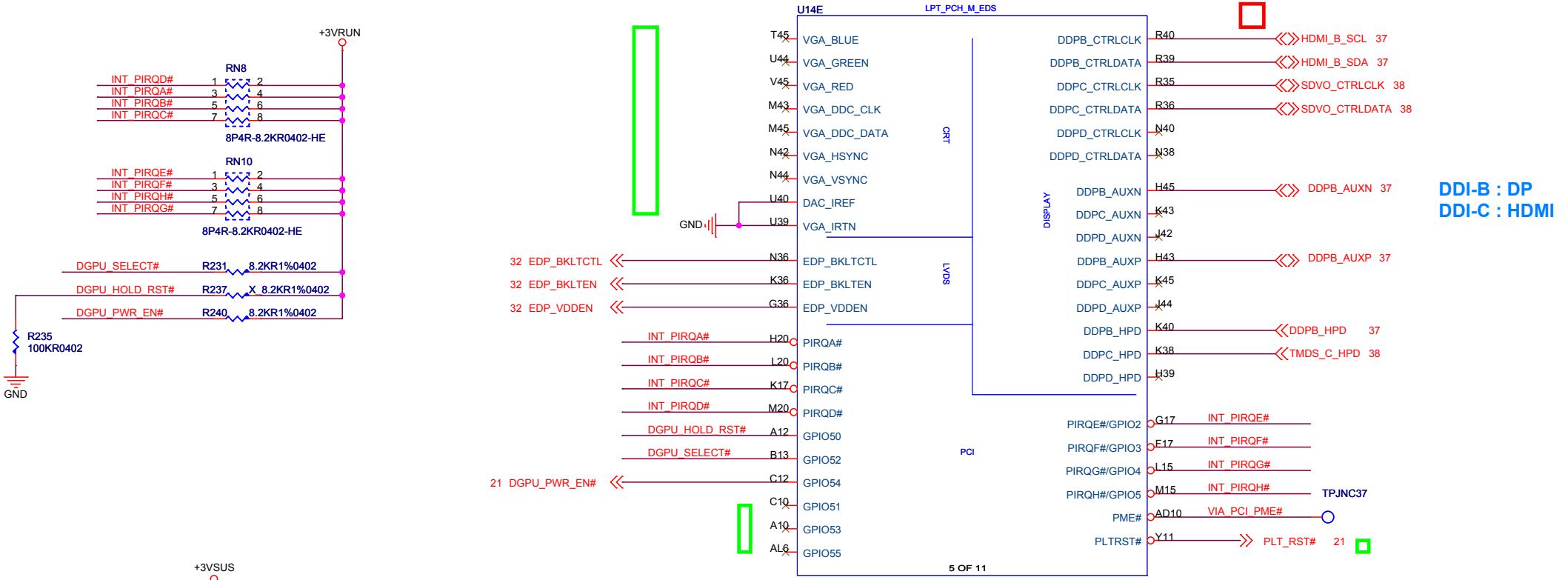
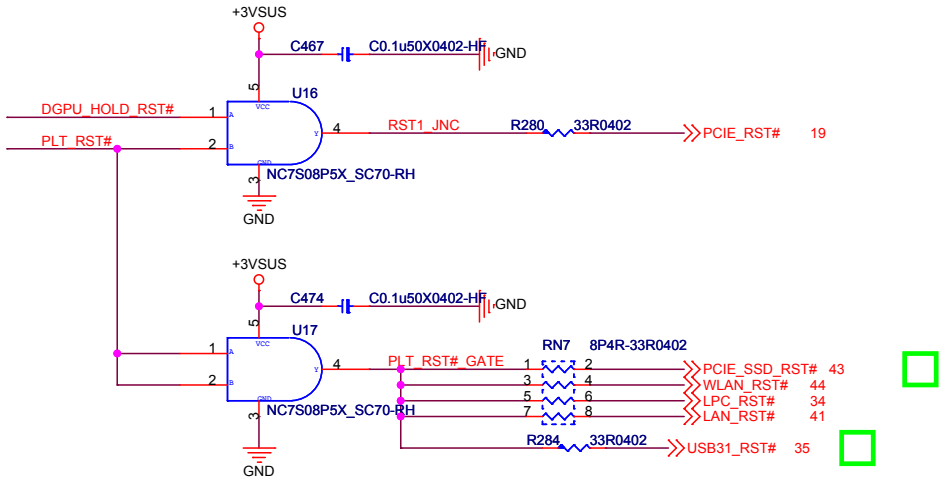
Lynx Point (PCI,DDI)

CTRLDATA This signal needs to be pulled up
through a 2.2 kOhms ±5% pull-up to 3.3 V to" enable Port" .





Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

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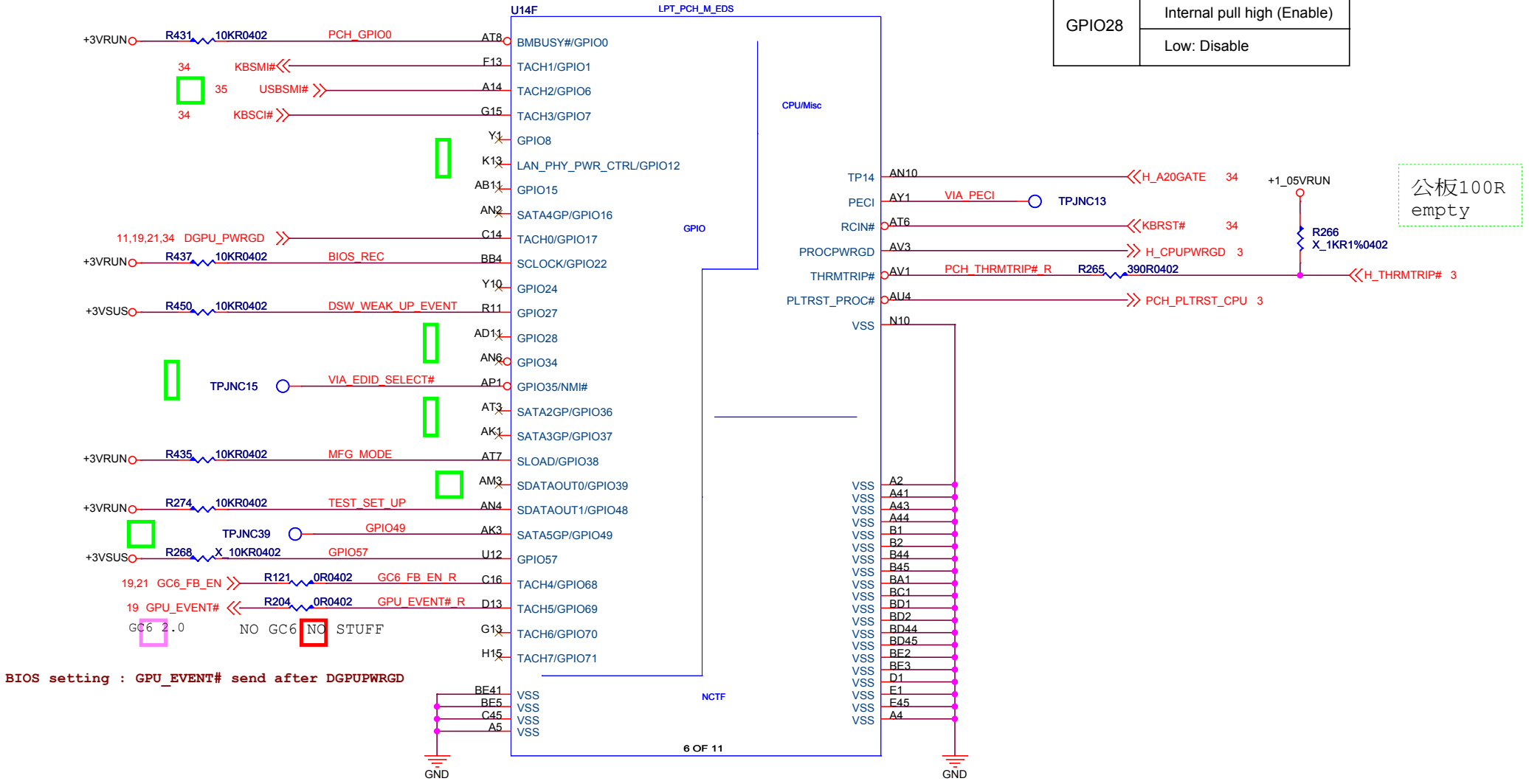
Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



BIOS setting : GPU_EVENT# send after DGPUPWRGD

MSI	MICRO-STAR INT'L CO.,LTD.
Title	PCH-6 (GPIO,MISC)
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Lynx Point (PCIE,USB)

Table 5-1. PCI Express* Ports 1 thru 4 - Supported Configurations

Port 1	Port 2	Port 3	Port 4
x4			
x2		x2	
x2		x1	x1
x1	x1	x1	x1

Table 5-2. PCI Express* Ports 5 thru 8 - Supported Configurations

Port 5	Port 6	Port 7	Port 8
x4			
x2		x2	
x2		x1	x1
x1	x1	x1	x1

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16J11
1	2	USB 3.0 Port 2	16J11 DEBUG PORT
2			
3			
4			
5			
6			
7		EPF021	3 色KBC
8		USB 2.0	16J12
9	6	USB 3.0 Port 6	16J11 CHARGER DEBUG PORT
10		WLAN	
11		WebCam	
12		CARDREADER	16J12
13			

HM86 沒USB3.0 PORT 5,6

MICRO-STAR INT'L CO.,LTD.

Title: PCH-7 (PCIE,USB)

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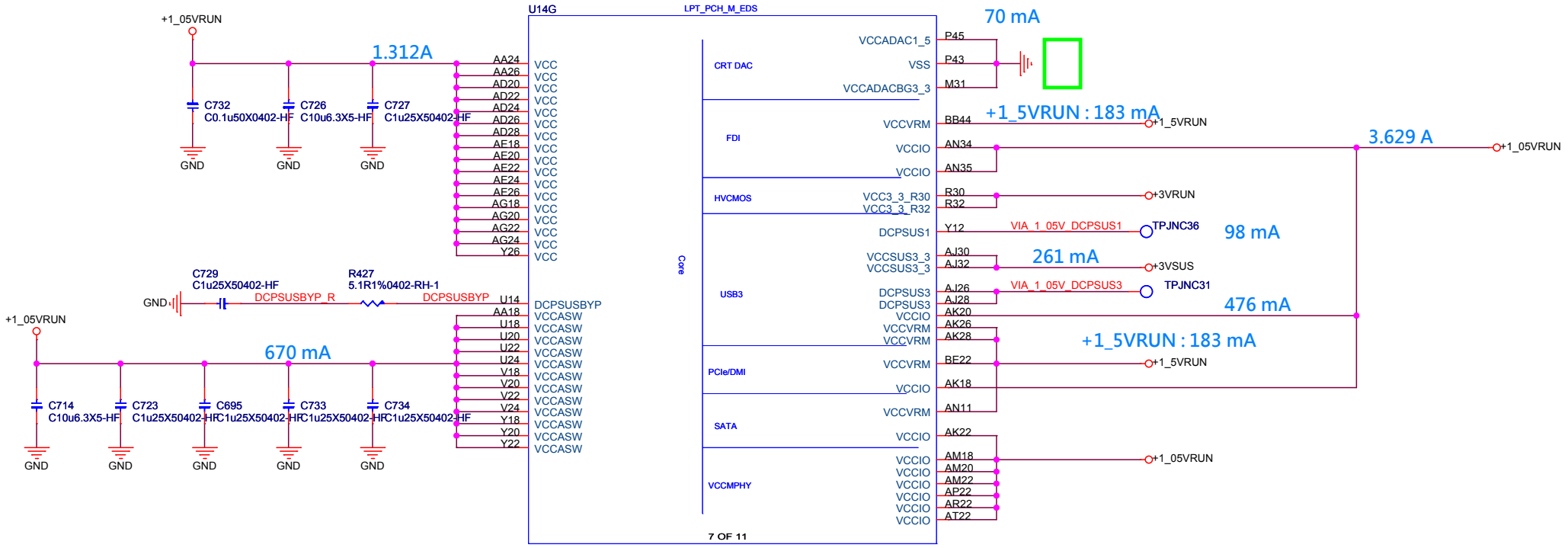
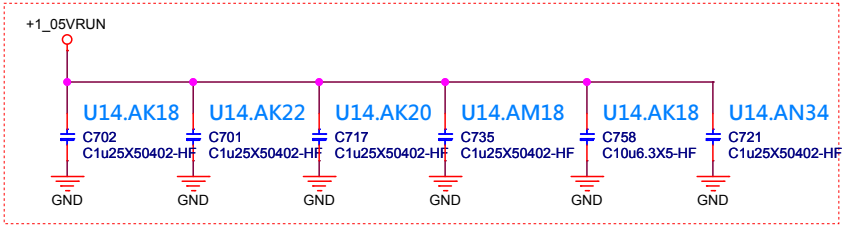
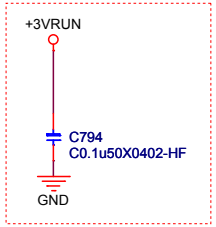
Lynx Point (Power)







MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

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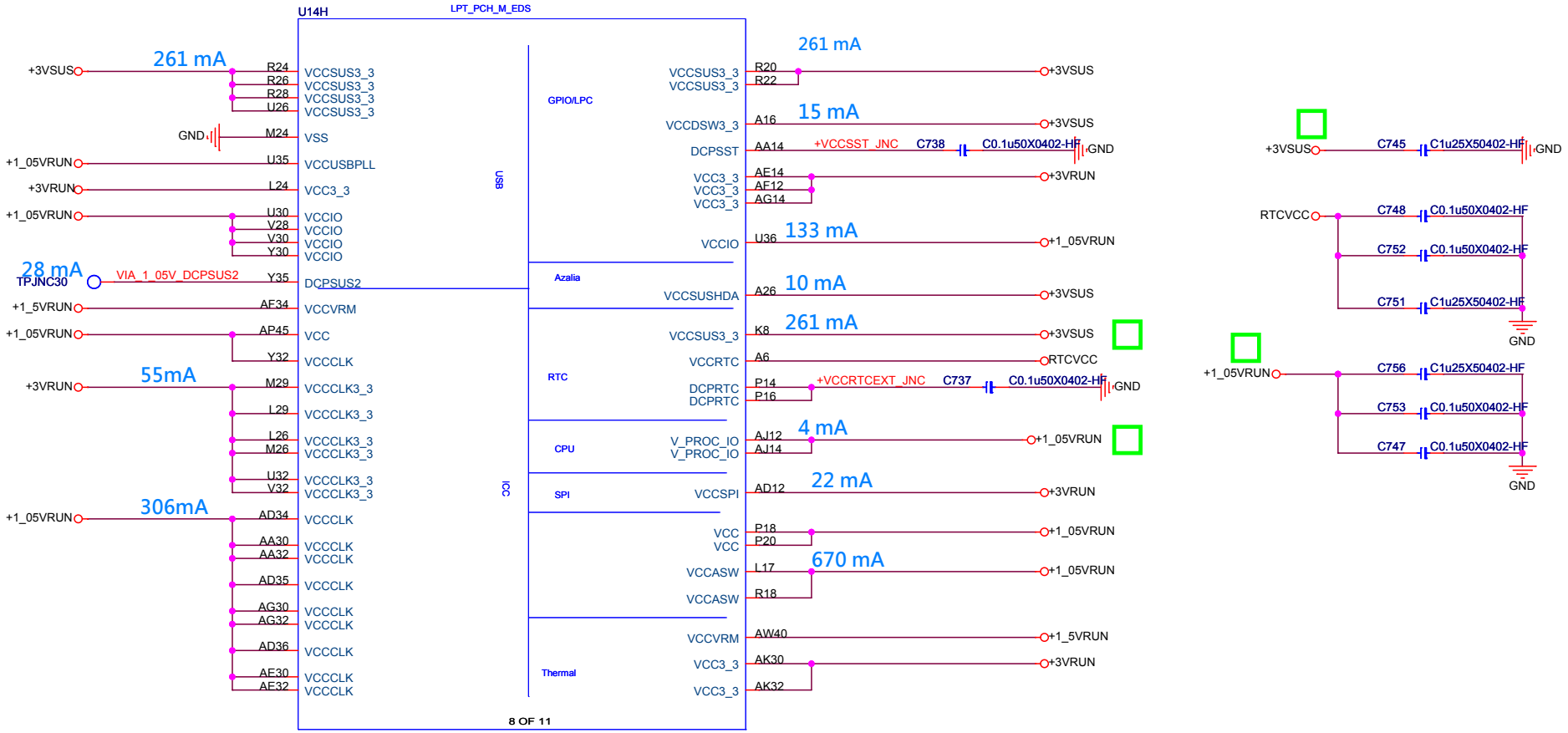
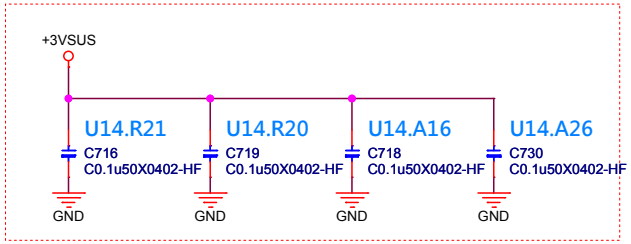
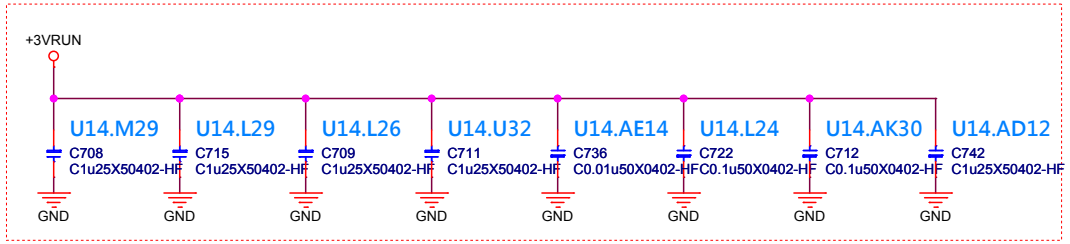
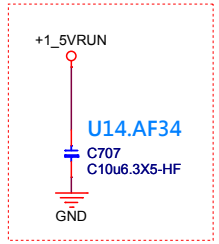
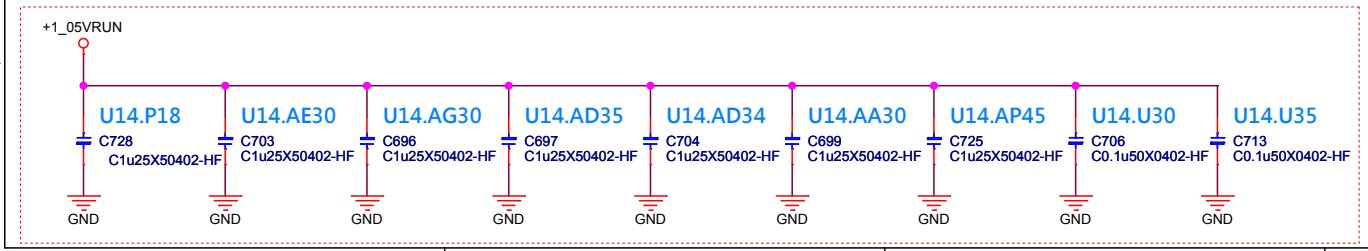
Lynx Point (Power)











MICRO-STAR INT'L CO.,LTD.

Title: PCH-9 (Power)

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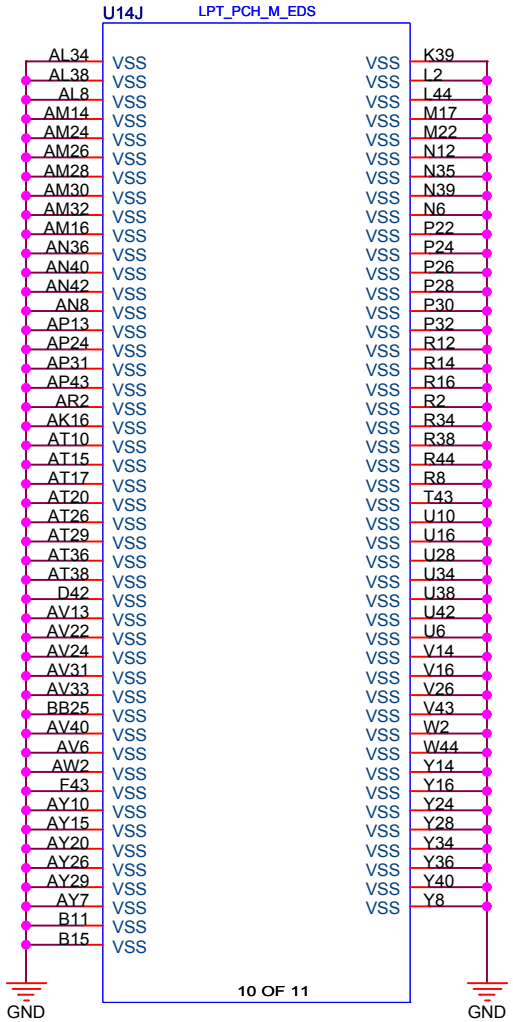
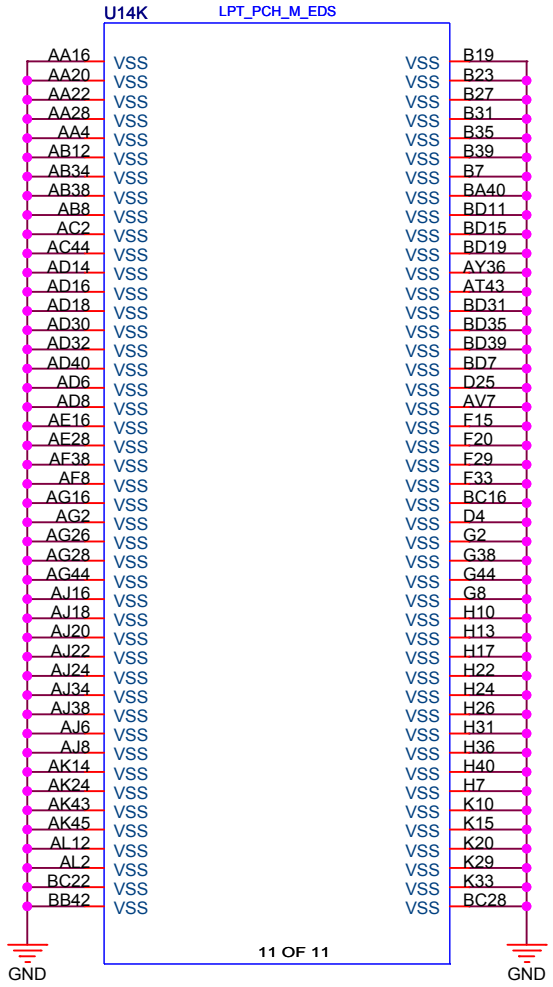
Lynx Point (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: PCH-10 (GND)		
Size	Document Number: MS-16J2	Rev: 0A
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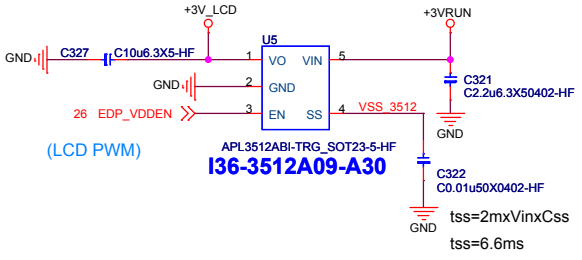
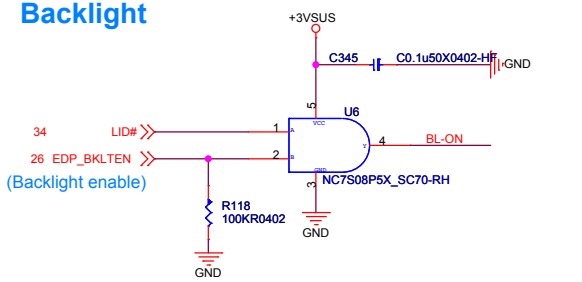
eDP

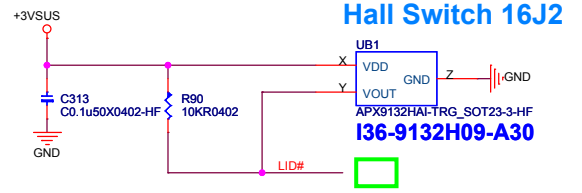
Pannel Device Logic Power



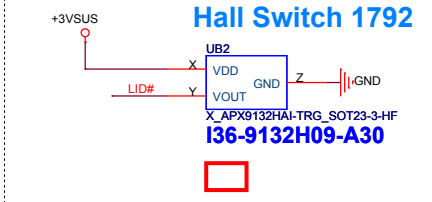
Backlight



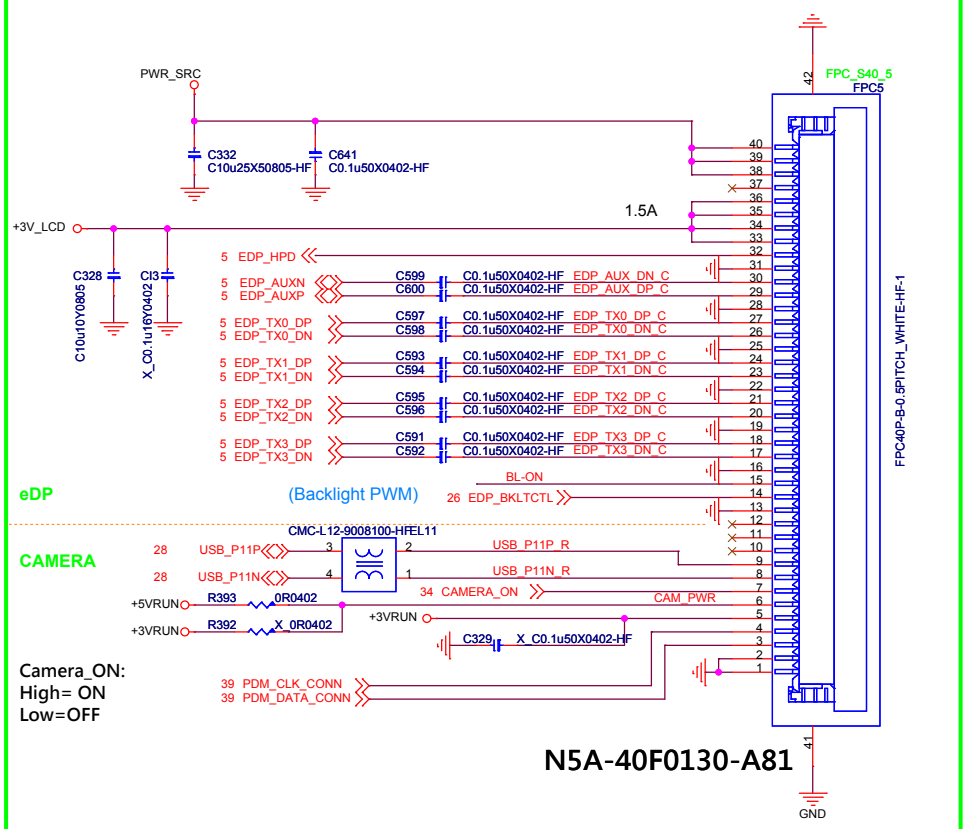
Hall Switch 16J2

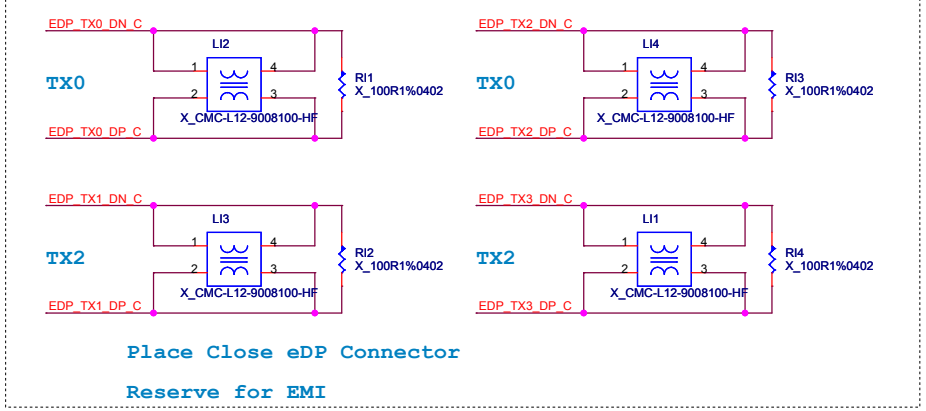


Hall Switch 1792



eDP CONN CAMERA





LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

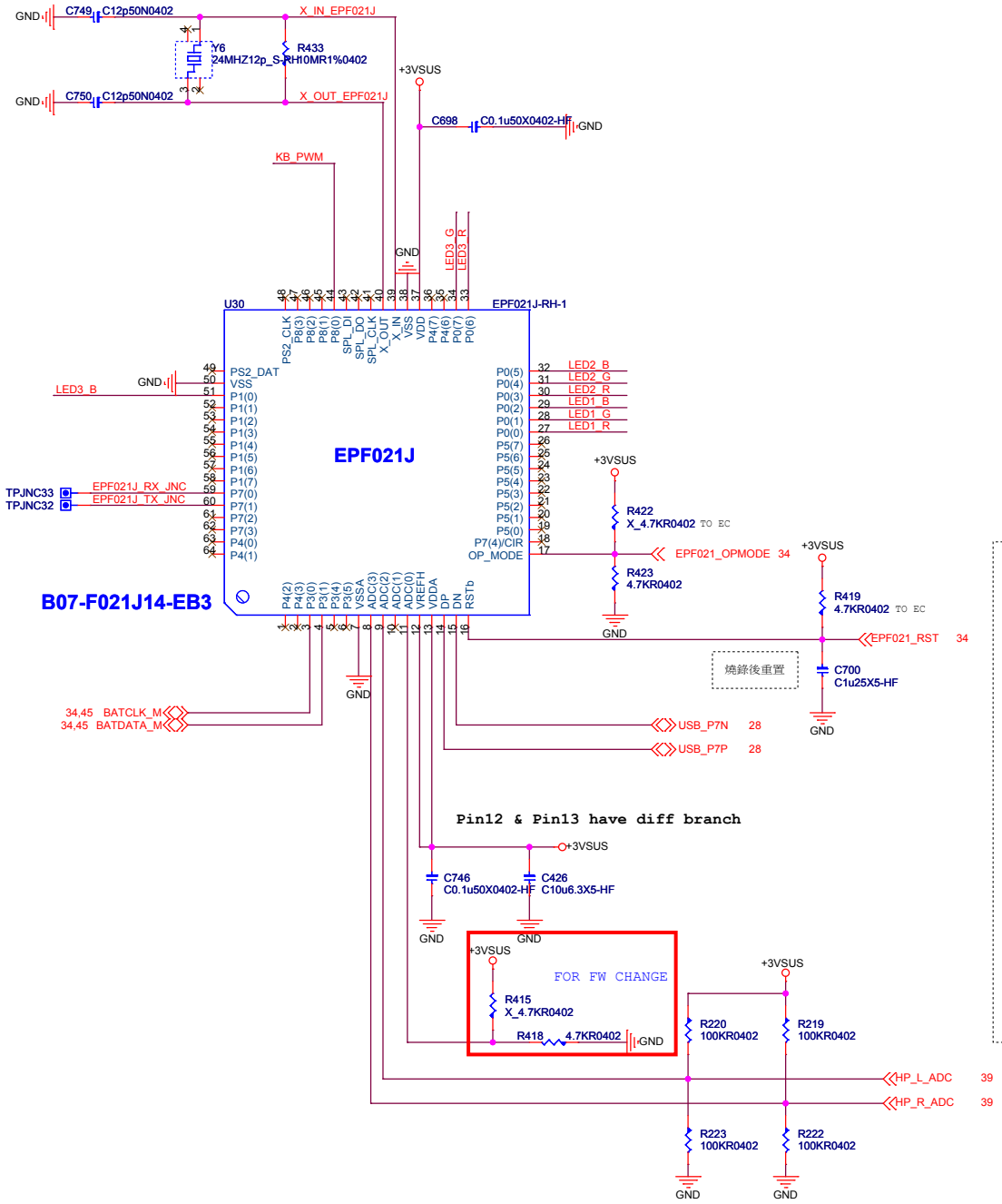
MICRO-STAR INT'L CO.,LTD.

Title: eDP /Camera

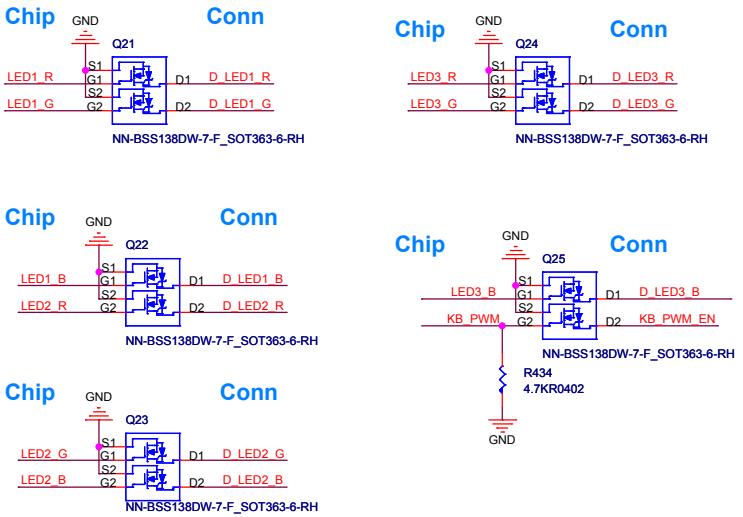
Size | Document Number: MS-16J2 | Rev: 0A

Date: Thursday, October 16, 2014 | Sheet 32 of 59

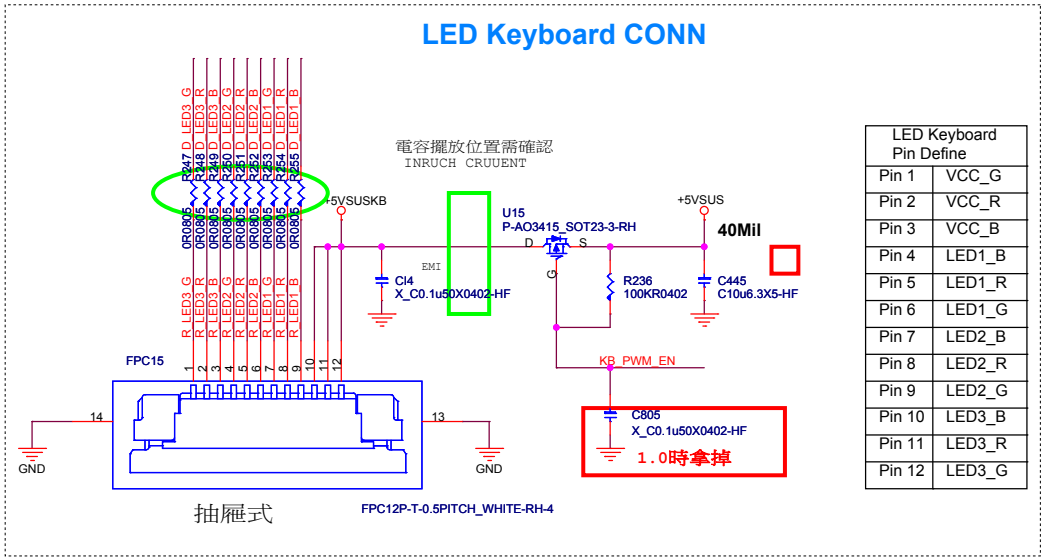
LED 8051 Controller



EPF021J Sink current not enough, only using BSS138 (0.22A)



LED Keyboard CONN



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED_8051

Size | Document Number: MS-16J2 | Rev: 0A

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KBC(KB3930QFB1)

Hardware Reset

ED before RC

RC and R Close SW

SW6 SW-TACTB1-4PS-RH-14

R436 47KR1%0402-HF

ED6 ESD-SFI0402-050E101NP-L

RB744

C0.1u50X0402-HF

RST_SW#

SW Debug (LPC)

CON6 BH1X14HS-1.25PITCH_WHITE-RH

直立式

N32-1140060-H06

MVT 移除SW5

SW5 X_SW-TACTB1S-HF

0B改包裝

R58 10KR0402

C163 C0.1u50X0402-HF

PWR_SW#

U1

LPC I/F

SERIRQ
LFARAME#
PCICLK
CLKRUN#/GPIO1D
LAD0
LAD1
LAD2
LAD3

POWER/GROUND

VCC
AVCC
AGND
GND

C430 C0.1u50X0402-HF
C710 C0.1u50X0402-HF
L9 80L700mA-150-RH
C724 C0.1u50X0402-HF
C411 C10u6.3X5-HF
C705 C0.1u50X0402-HF
C743 C0.1u50X0402-HF
C694 C0.1u50X0402-HF
EC_AVCC

FAN&PWM

PWM0/GPIO0F
PWM1/GPIO10
GPIO11/PWM2
GPIO19/PWM3
FANPWM0/GPIO12
FANPWM1/GPIO13
FANFB0/GPIO14
FANFB1/GPIO15

SMBUS

SDA0/GPIO45
SCL0/GPIO44
SDA1/GPIO47
SCL1/GPIO46

BATDATA_M 33,45
BATCLK_M 33,45
SMB_DATA_EC 19
SMB_CLK_EC 19

AD/DA

DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
AD4/GPI42
AD5/GPI43

EPF021_RST 33
EPF021_OPMODE 33
DGPU_ON# 44
CTL1_EC 36
FBVDDQ_ON 21,49
MB_ID
ADP_ICC 45
SUSPWRACK 25
AC_OK# 45
BAT_IN# 45

SDI

GPXIOA00/SDICS#
GPXIOA01/SDICLK
GPXIOA02/SDIMOSI

AC_PRESENT 25
SUS_ON 46
RSMRST# 25

IKB

KSO0/GPIO20/TP_TEST
KSO1/GPIO21/TP_PLL
KSO2/GPIO22/TP_ANA_TEST
KSO3/GPIO23/TP_ISP
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F/E51_RXD(ISP)
KSO16/GPIO48
KSO17/GPIO49

KSI0/GPIO30/E51TXD(ISP)
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34/EDI_CS
KSI5/GPIO35/EDI_CLK
KSI6/GPIO3/EDI_DIN
KSI7/GPIO37/EDI_DO

KBOUT0 39
KBOUT1 40
KBOUT2 41
KBOUT3 42
KBOUT4 43
KBOUT5 44
KBOUT6 45
KBOUT7 46
KBOUT8 47
KBOUT9 48
KBOUT10 49
KBOUT11 50
KBOUT12 51
KBOUT13 52
KBOUT14 53
KBOUT15 54
KBOUT16 81
KBOUT17 82

KBIN0 55
KBIN1 56
KBIN2 57
KBIN3 58
KBIN4 59
KBIN5 60
KBIN6 61
KBIN7 62

GPXIOA03 100
GPXIOA04 101
GPXIOA05 102
GPXIOA06 103
GPXIOA07 104
GPXIOA08 105
GPXIOA09 106
GPXIOA10 107
GPXIOA11 108
GPXIOD0 109
GPXIOD1 110
GPXIOD2 112
GPXIOD3 114
GPXIOD4 115
GPXIOD5 116
GPXIOD6 117
GPXIOD7/PECI 118

DIMM_ON 47
RUN_ON 46,48
EC_PCH_PWROK 6,25
COOLER_LED# 44
WLAN_PWRON 44
LED_CHARGE# 44
LED_BATLOW# 44
SUSPWROK 46
PM_SLP_S4# 25,47
PM_SLP_S3# 25,47
EC_ALLSYSPG
PWR_SW# 44
SCI_WAKE_UP# 24
LID# 32
H_PECI 3
R211 43R0402

EC_PROTECT_PWR=>OD pin

TPJNC23 EC_PROTECT_PWR 19
Pin 105-108 8mA-16mA Sink
OVERT# 19
TPJNC24

ESB

GPIO0B/ESB_CLK
GPIO0C/ESB_DAT_O/ESB_DAT_I

EC_MUTE# 39
BAT_BM# 45

CIR

GPIO40/CIR_RX/AD6
GPIO41/CIR_RLC_TX/AD7
GPIO0A/RLC_RX2
GPIO0D/RLC_TX2

EAPD 39
FB_CLAMP_REQ# 16
FB_CLAMP 19
TPJNC26
TPJNC28

GPIO04
GPIO07/I_clk_8051
GPIO08/I_clk_peri
GPIO18
GPIO50
E51CS#/GPIO52
E51TMR0/GPIO54/WDT_LED#
E51INT1/GPIO56
GPIO57/XCLK32K
GPIO59/TEST_CLKSPICLKI

KBLED_BACKLIGHT_SW# 44
GPU_ACIN1 19
DGPU_PWRGD 11,19,21,27
KBSMI# 27
COOLER_BOOST_SW# 44
BATT_OFF 45
LED_WLAN# 44
PM_PWRBTN# 25
BT_PWR_ON 44
CAMERA_ON 32

Pin 92 16mA-20mA Sink

SPI FLASH

MISO
MOSI
SPICLK/GPIO58
SPICS#

EC_RD# 119
EC_WR# 120
EC_SPI_CLK 126
EC_CS# 128

PS2 I/F

PSCLK2/GPIO4E
PSDAT2/GPIO4F
PSCLK1/GPIO4C
PSDAT1/GPIO4D
PSCLK0/GPIO4A/P80CLK
PSDAT0/GPIO4B/P80DAT

TP_CLK 44
TP_DATA 44
CTL2_EC 36
CTL3_EC 36
EC_PROCHOT# 3
USB_ENABLE 36,44

GPIO1A/NUMLED#
E51TMR1/GPIO53/CAPSLED#
E51INT0/GPIO55/SCROLED#

LED_NUM# 44
LED_CAP# 44
SCROLED# JNC
TPJNC25

Pin 39,91 16mA-20mA Sink

UART

E51TXD/GPIO16
E51RXD/GPIO17

E51_JNC 30
E51RXD_JNC 31
TPJNC34
TPJNC35

LED

XCLK

XCLKI
XCLKO

EC_XOUT 122 123
JNC21 X_0402
EC_SUSCLK 25
ER10 X_22R0402
SUSCLK_RC
R404 680KR0402-HF
C688 X_C22p50N0402

V18R

V18R 124
C425 C4.7u10X5-HF

KB3930QFB1-B1-HF

B02-0393024-E18

Keyboard conn

CON5 FPC28P-T-1PITCH_WHITE-RH-1

抽屜式

8p4C-100p50N0402-HF
CNI4 CNI3 CNI2 CNI1

KBOUT17 C15 C100p50N0402
KBOUT16 C16 C100p50N0402

+3VRUN R263 X_10KR0402 KBLED_BACKLIGHT_SW# C477 C0.1u50X0402-HF
+3VRUN R358 10KR0402 COOLER_BOOST_SW# C690 C0.1u50X0402-HF

ROM

AVL : M31-2551232-GA0

R407 2.2KR1%0402
WP#_EC_ROM
C681 C0.1u50X0402-HF
R403 10KR0402
U28 MX25L512EMI-10G-HF
SPI_HOLD#
EC_SPICLK
EC_WR#
EC_CS#
EC_RD#

M31-2551222-M24

EC_SPI_CLK ER9 22R0402 EC_SPICLK EC53 C22p50N0402

ALLSYSPG

R216 10KR0402

48 +1_5VRUN_PWRGD JNC13 X_0402
48 +1_05VRUN_PWRGD JNC12 X_0402
47 +1_35VDIMM_PWRGD JNC11 X_0402
EC_ALLSYSPG 37,51

PU/PD

BATCLK_M R417 2.2KR1%0402
BATDATA_M R416 2.2KR1%0402
SMB_CLK_EC R224 2.2KR1%0402
SMB_DATA_EC R221 2.2KR1%0402

KBRST#, H_A20GATE

KBRST# R215 X_100KR0402
RSMRST# R264 10KR0402

MB_ID

GTX 960M
PR147 100KR0402
MB_ID
R429 X_10KR1%0402

Title	KBC(KB3930QFB1)
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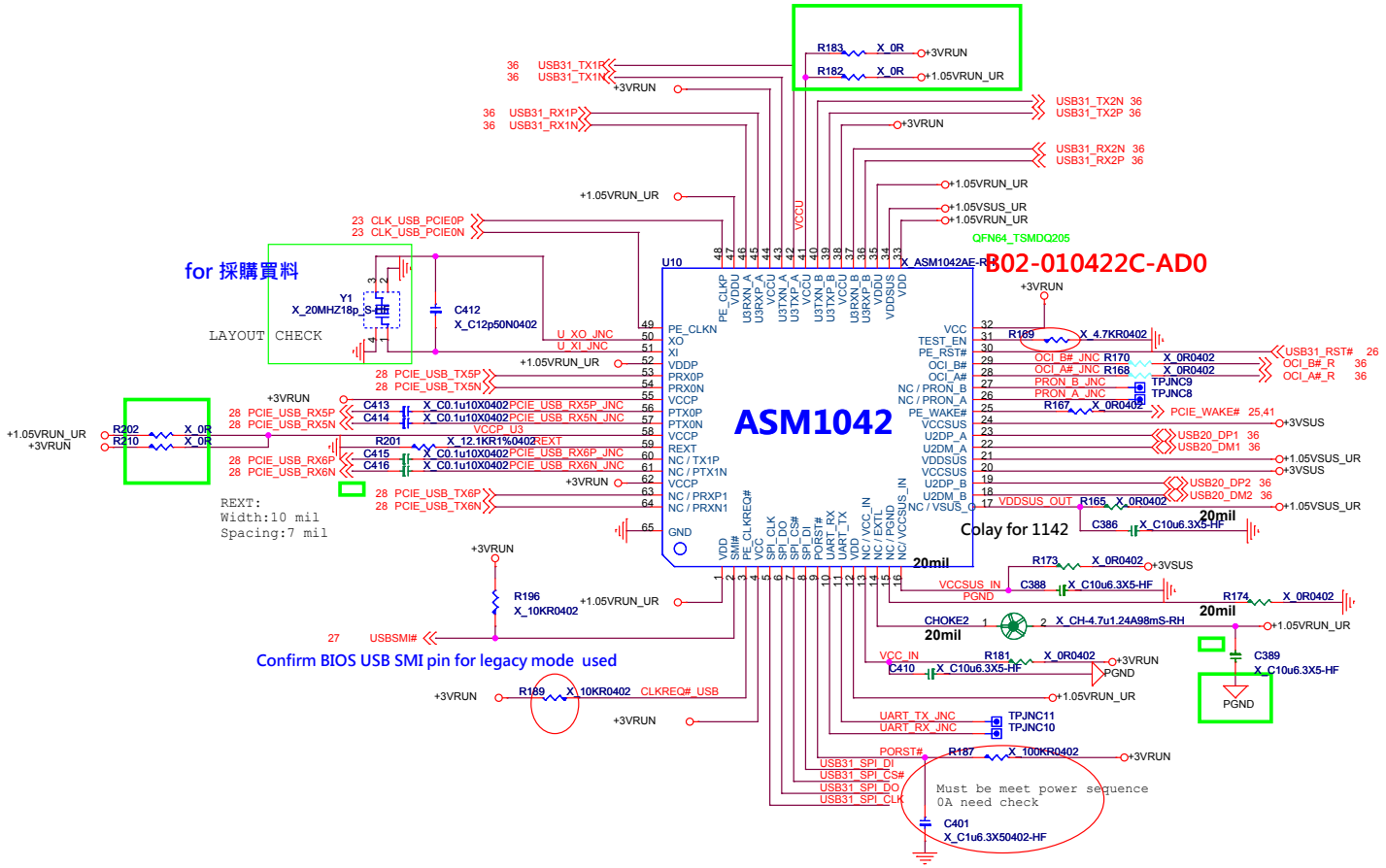
MICRO-STAR INT'L CO.,LTD.

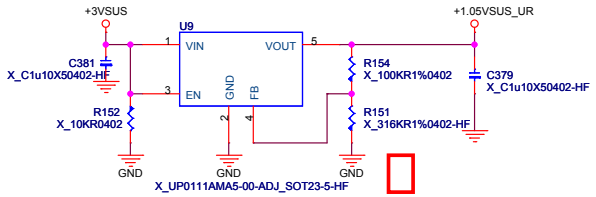
PCIE to USB 3.1

USB 3.0/ USB.3.1

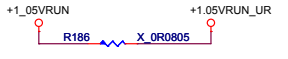
BOM DEFAULT 1042 (USB3.0) CHECK FUNCTION
VDD= 1.05V



ASM1042 stuff



ASM1142 含內轉1.05V時不上件



HW strap

PE_PWRDET fuction

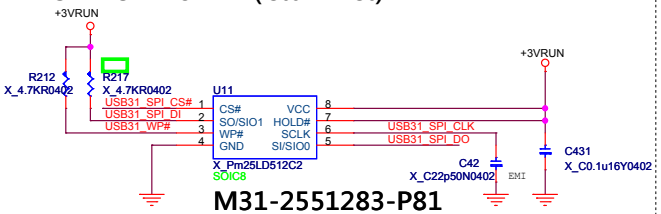
PU for D3cold (detect AUXpower)

Internal PU

UART_TX_JNC
UART_RX_JNC

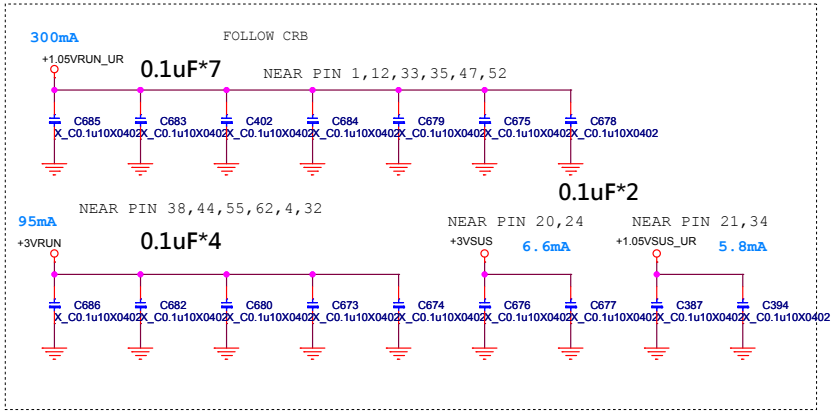
CSEL1(RX):CSEL0(TX) Clock select
11:External 20MHz Crystal
01:48MHz Clock Input
X0:Reserve for Test Mode

SPI ROM For FW (stuff first)



M31-2551283-P81

需使用與EC ROM不同的料號上件



msi MICRO-STAR INT'L CO.,LTD.		
Title: USB 3.0 / USB 3.1		
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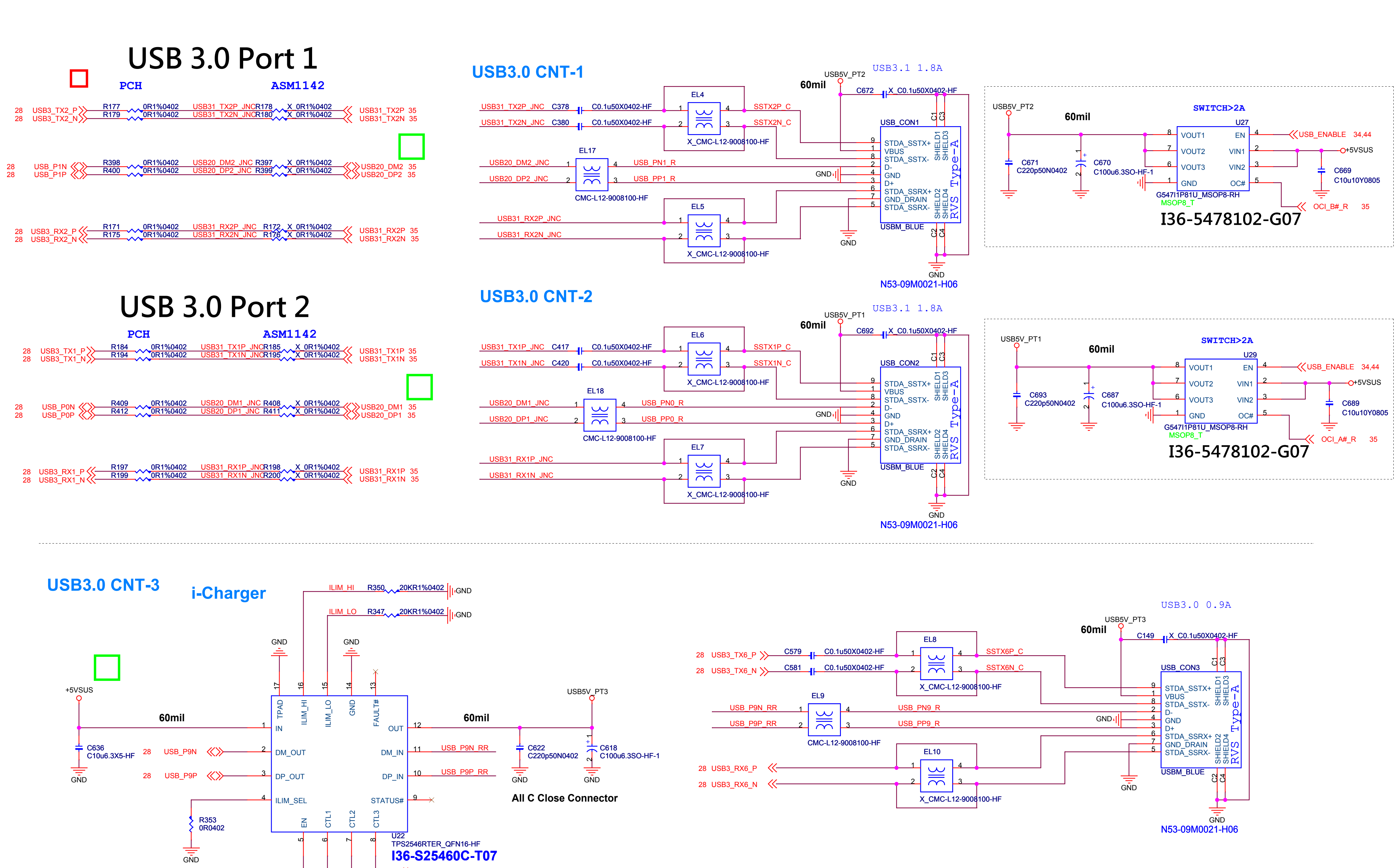

msi MICRO-STAR INT'L CO.,LTD.

Title	USB 3.0 /iCharger
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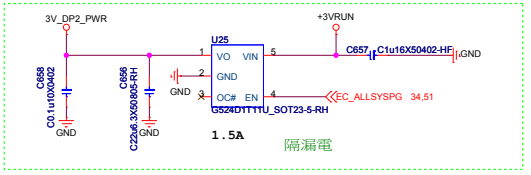
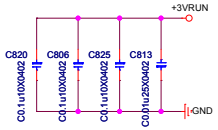
Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.

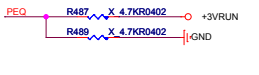




3 Level Input:
L: LOW
H: HIGH
M: VDD33/2, connect both pull-up and pull-down resistors

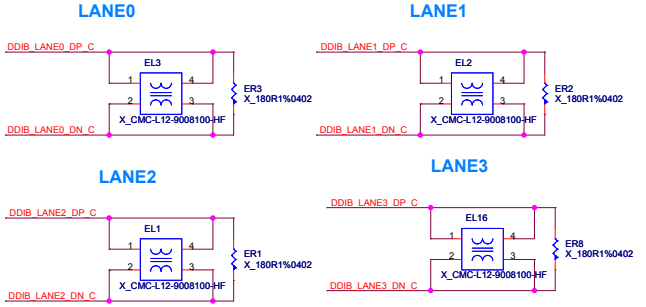
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable



Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

EMI Close Connector



MICRO-STAR INT'L CO.,LTD.

Title	DP PS8330	
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HDMI Level Shifter

HP_DET
PLUGGED 5V
UNPLUGGED 0V

HPD_SNK Internal PD 130kohm ESD 10KV

V1.0 reserved for AOC TV issue.

R115 2.2KR1%0402

U23 SN75DP139RSBR-RH

R359 10KR0402
QB1 N-2N7002_SOT23-3-RH
R367 X_0R0402
R360 X_4.7KR0402
R369 0R0402
R384 X_4.7KR0402
R379 X_0R0402
R366 4.7KR0402
R363 4.7KR0402
R380 4.7KR0402
R381 4.02KR1%0402
R385 X_100KR0402
X_0402
JNC18
R382 2.2KR1%0402
R383 2.2KR1%0402

C647 C0.1u50X0402-HF
C648 C0.1u50X0402-HF
C649 C0.1u50X0402-HF
C650 C0.1u50X0402-HF
C651 C0.1u50X0402-HF
C652 C0.1u50X0402-HF
C654 C0.1u50X0402-HF
C655 C0.1u50X0402-HF

DDC I2C buffer offset select
H:Offset 1
L:Offset 2
Hi-Z:Offset 3

Output Enable and power saving function for High Speed Differential level shifter path.
H: Power Saving OUT_Dx outputs = high impedance
L: Normal Mode OUT_Dx outputs = active

TMDS outputs rise and fall time select
H:Edge Rate:Slowest SRC =High adds ~60ps
L:Edge Rate: Slow SRC =Low adds ~30ps
Hi-Z:Edge Rate VCC/2

HPD_SOURCE Logic and Level Select
H:HPD Inversion HPD_SOURCE VOH =0.9V
L:HPD non-inversion HPD_SOURCE VOH =3.2V

Enables or Disables the DDC I2C buffer
H:DDC Buffer enabled
L:DDC Buffer disabled

HDMI Connector

HDMI1 HDMI19PM_BLACK-HF-7

D2 S-BAT54ALT1G_SOT23-RH
D3 X_BAV99LT1_SOT23
PF1 F-0805L075WR-HF
R120 2.2KR1%0402
R100 2.2KR1%0402
R101 X_100KR0402
C229 C0.22u25X-HF
C639 C0.1u50X0402-HF

W>20mils

C349 C0.1u50X0402-HF
C344 C0.01u50X0402-HF
C351 C1u25X50402-HF
C343 C1u25X50402-HF

Place Under DUT

C346 C0.1u50X0402-HF
C352 C0.01u50X0402-HF
C348 C1u25X50402-HF
C347 C1u25X50402-HF

EMI Close Connector

TX0: EL13, ER5 X_180R1%0402, X_CMC-L12-9008100-HF
TX2: EL15, ER7 X_180R1%0402, X_CMC-L12-9008100-HF
TX1: EL14, ER6 X_180R1%0402, X_CMC-L12-9008100-HF
CLK: EL12, ER4 X_180R1%0402, X_CMC-L12-9008100-HF

MICRO-STAR INT'L CO.,LTD.

Title	HDMI DP139	
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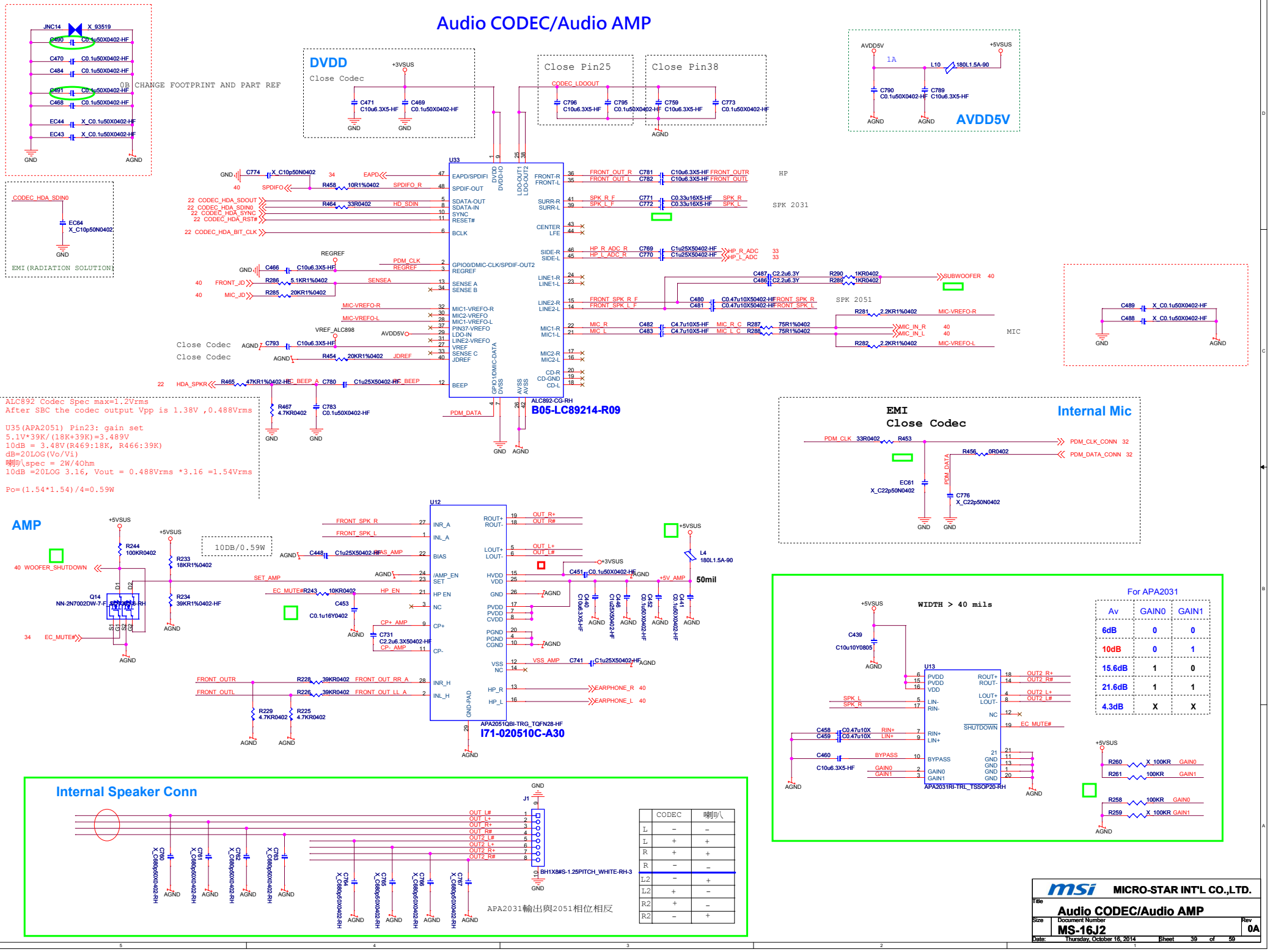
Audio CODEC/Audio AMP



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

	CODEC	喇叭
L	–	–
L	+	+
R	+	+
R	–	–
L2	–	+
L2	+	–
R2	+	–
R2	–	+

MICRO-STAR INT'L CO.,LTD.

Title: Audio CODEC/Audio AMP

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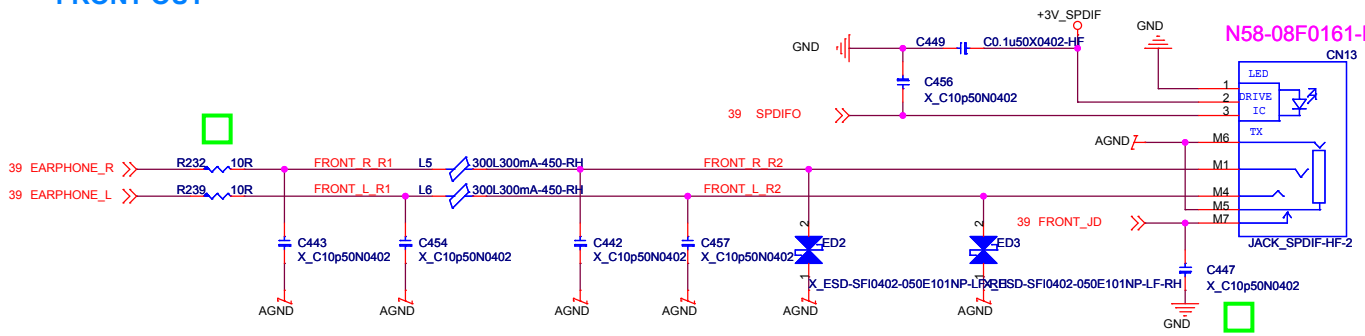
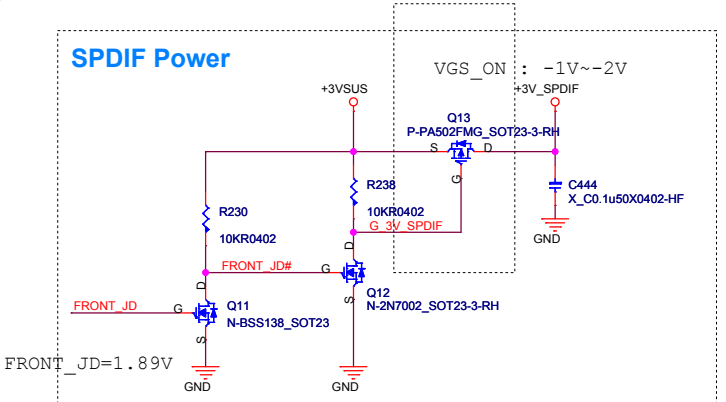
Audio CONN /Woffer

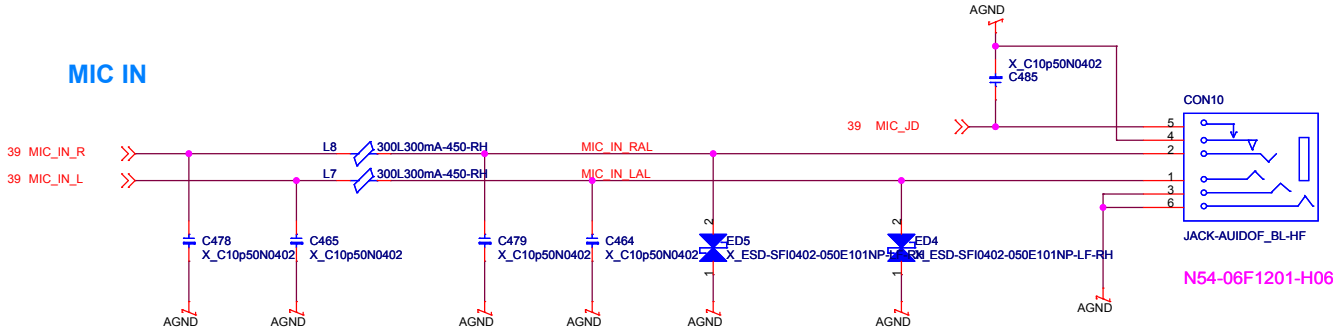
FRONT OUT



SPDIF Power



MIC IN

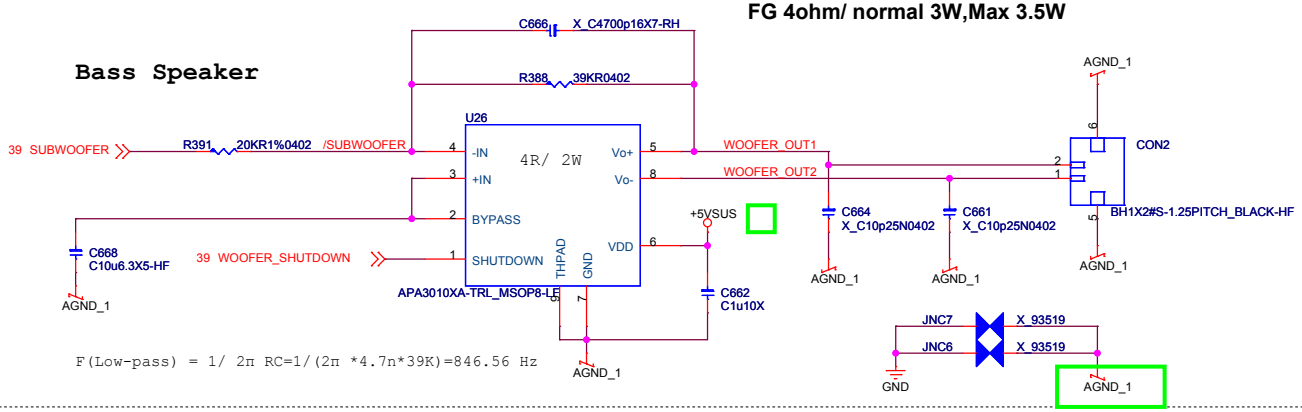


ALC892 SPC MAX 為 1.2Vrms
gain= -2*(R370/R371)= -2*(40K/20K) = -4

Vout= 0.58Vrms *4 = 2.32Vrms , Po=(2.32*2.32)/3.8=1.42W

Woofer SPEC
YG 3.8ohm / normal 3W,Max 3.5W
FG 4ohm/ normal 3W,Max 3.5W

Bass Speaker



F(Low-pass) = 1/ 2π RC=1/(2π *4.7n*39K)=846.56 Hz

MSI MICRO-STAR INT'L CO.,LTD.		
Title: Audio / Woffer		
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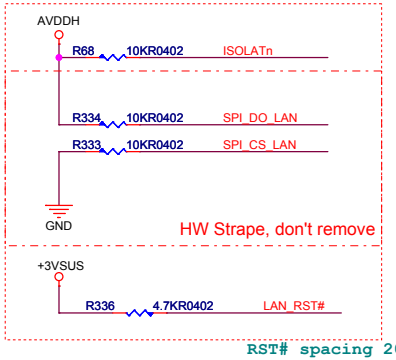
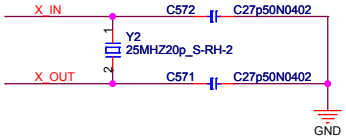
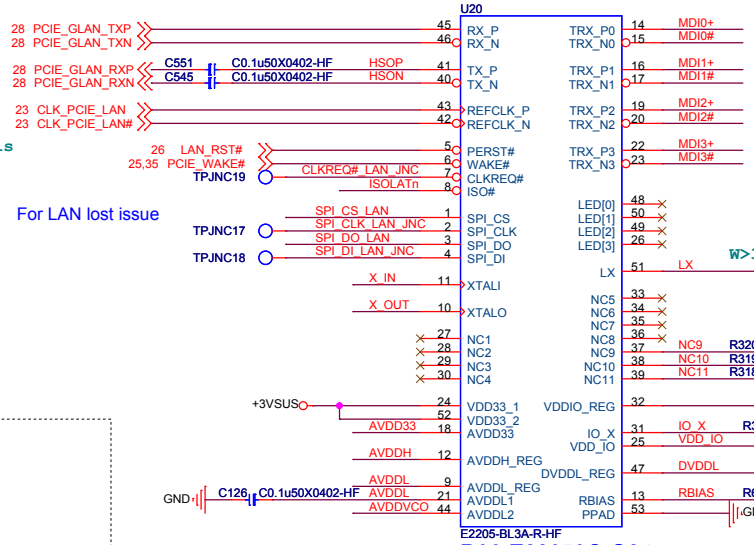
GIGA LAN(BigFoot BFN2205B)



RST# spacing 20mils

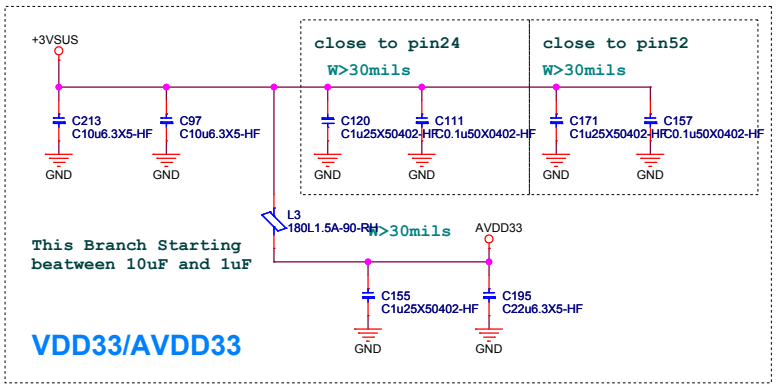


For LAN lost issue

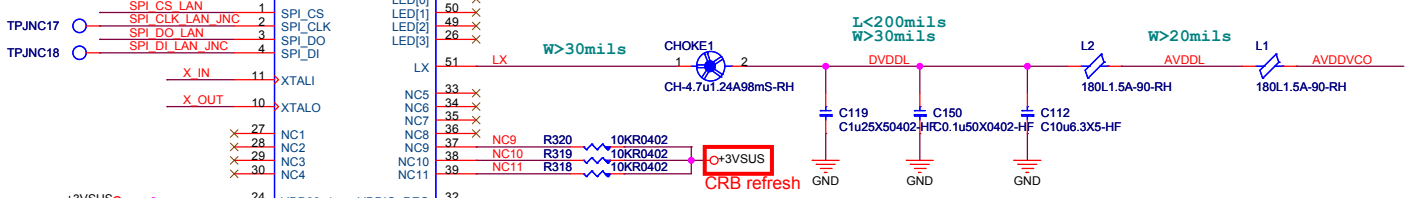


B06-E22050C-Q24

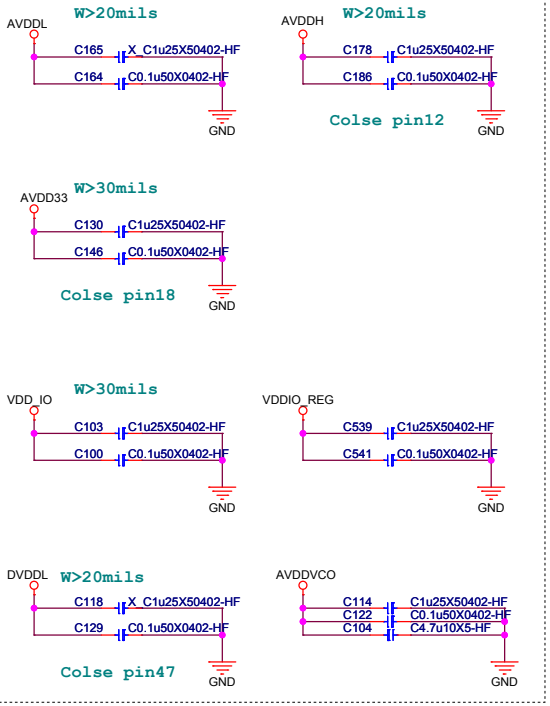
MAC 燒 CHIP 內
,有次數限制

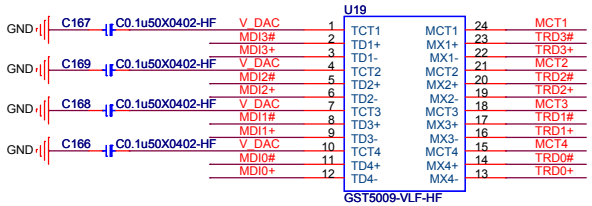


VDD33/AVDD33

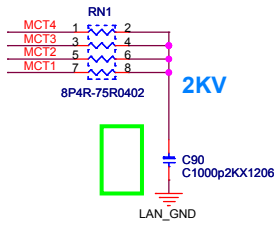


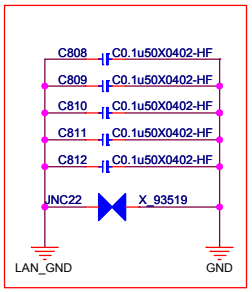
Power CAP

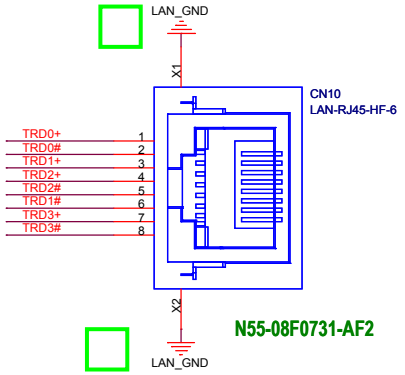




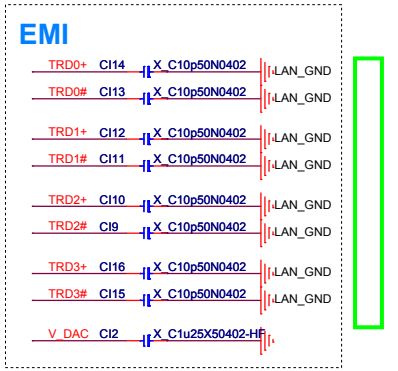
L05-0200150-B09







N55-08F0731-AF2



MICRO-STAR INT'L CO.,LTD.

Title: GIGA LAN(BigFoot BFN2205B)

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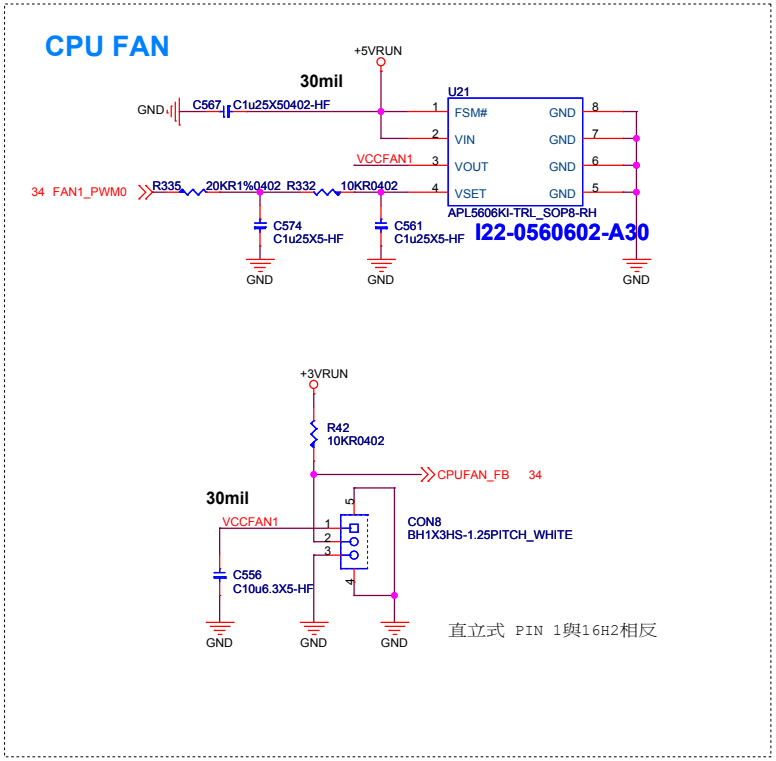
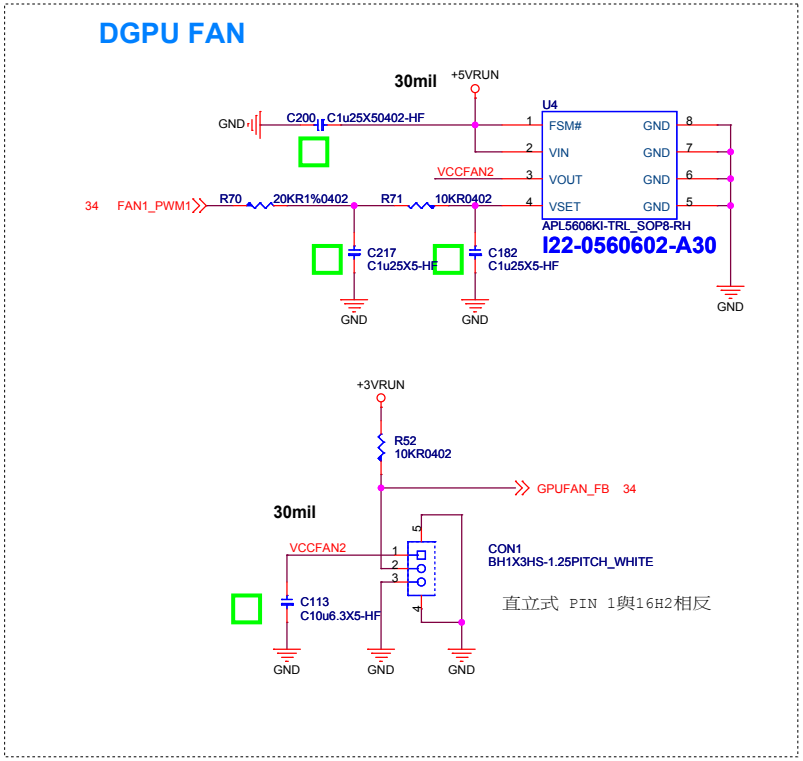
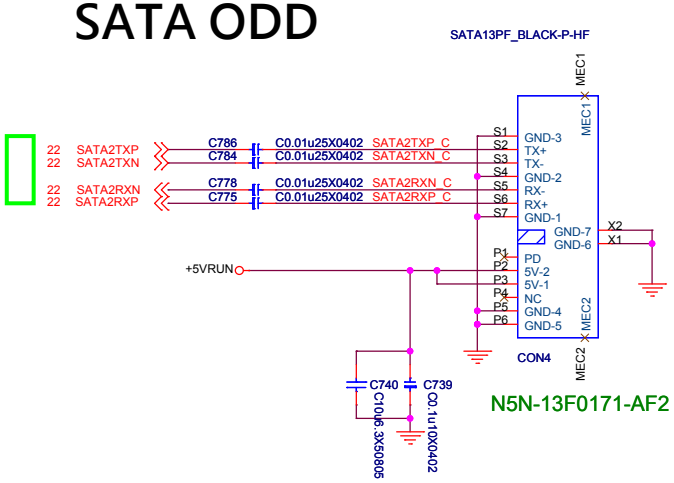
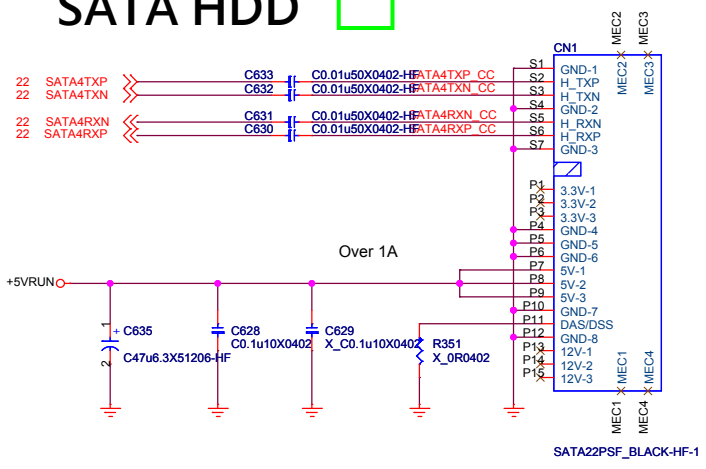
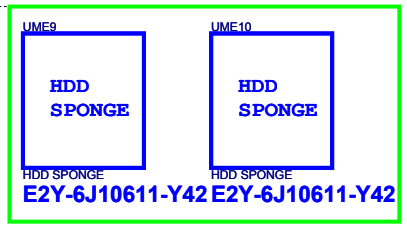


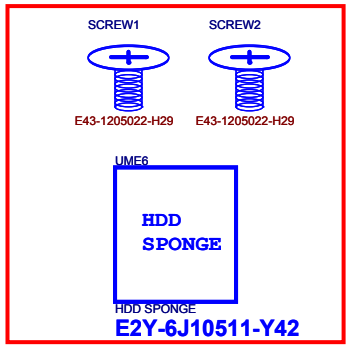


20141016 ME add









Title	ODD/HDD/FAN		
Size A3	Document Number MS-16J2		Rev 0A
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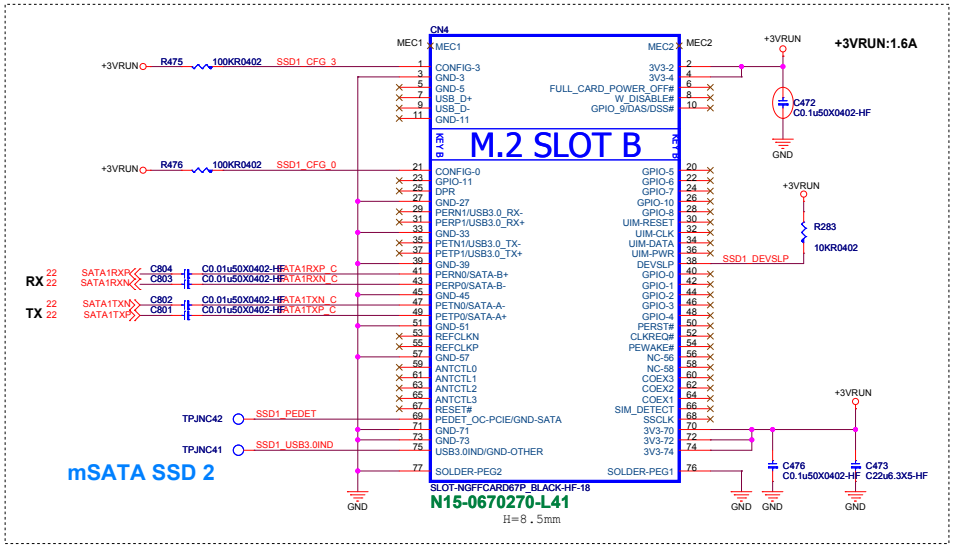
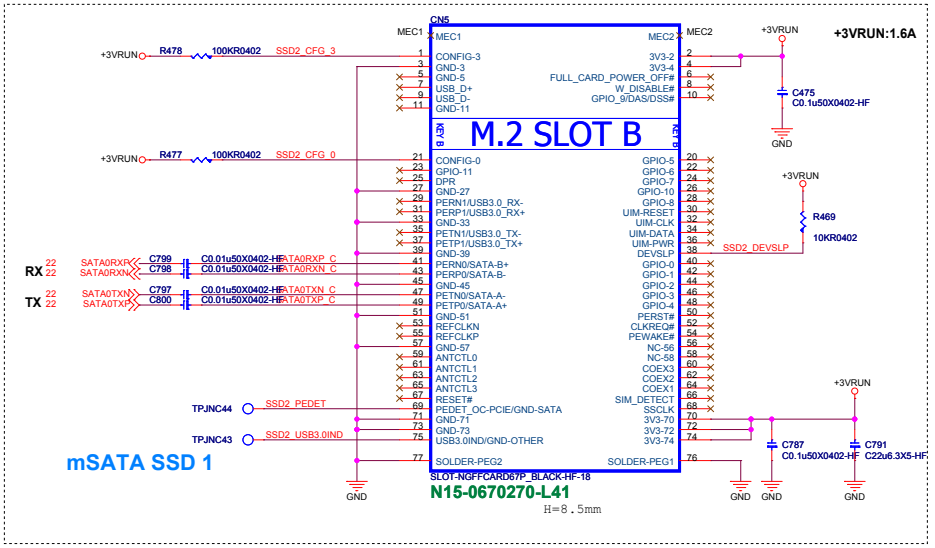
SSD

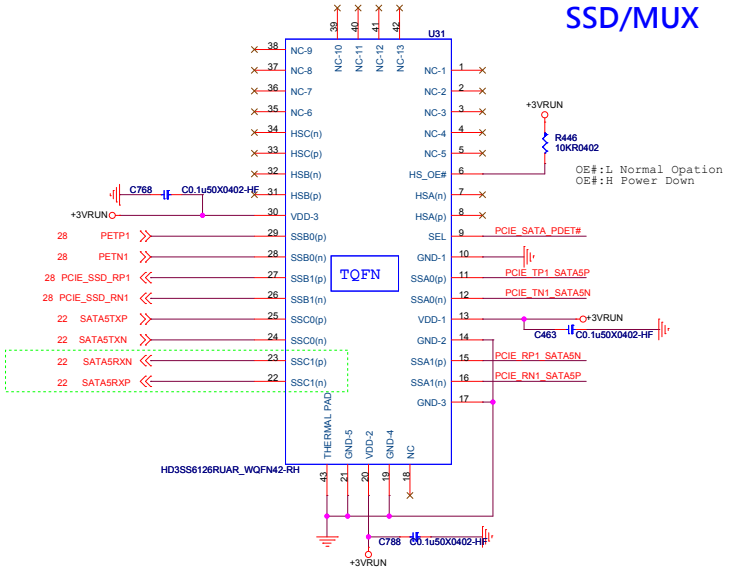
SATA SIGNAL



SATA SIGNAL



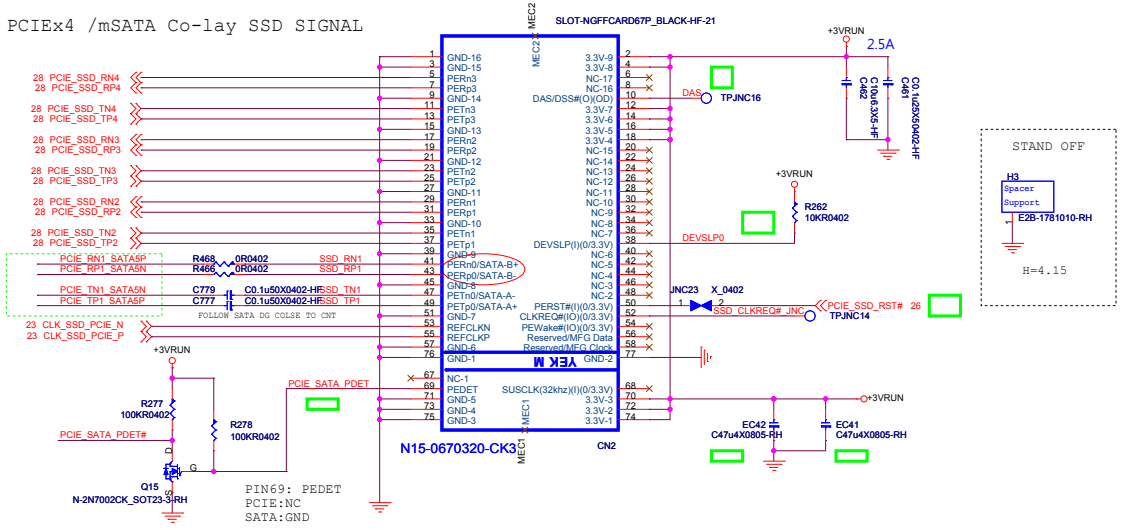
SSD/MUX



TRUTH TABLE USB 3.0 SuperSpeed USB

SEL	USB 3.0 Port Selection		
	SSA0/1	SSB0/1	SSC0/1
0	To/From SSB0/1	To/From SSA0/1	Off
1	To/From SSC0/1	Off	To/From SSA0/1

PCIEx4 /mSATA Co-lay SSD SIGNAL



中間 H=3.2mm

msi MICRO-STAR INT'L CO.,LTD.

Title: SSD/MUX

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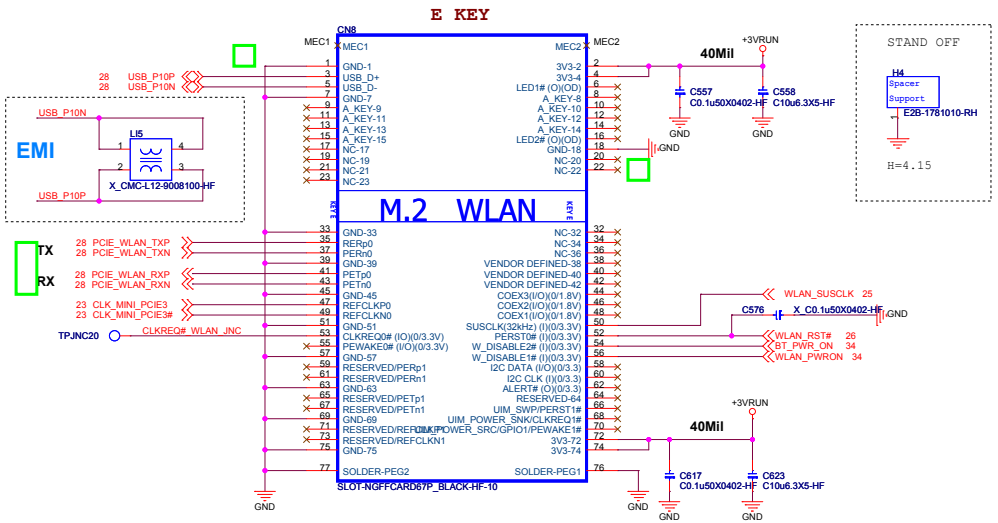
WLAN

WLAN/LED

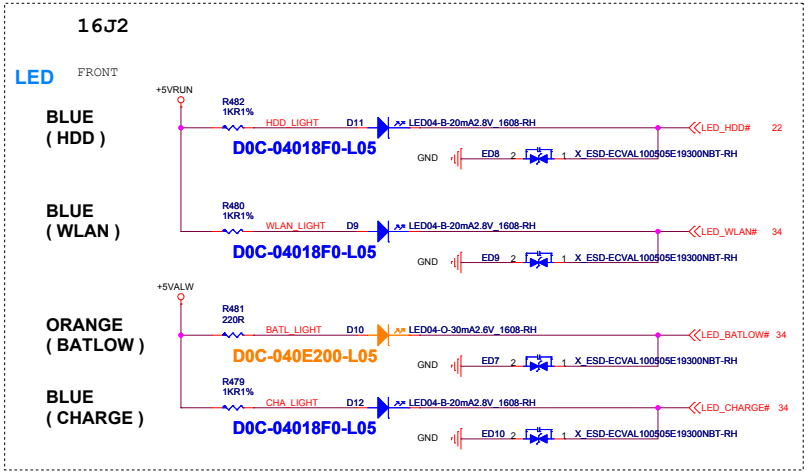


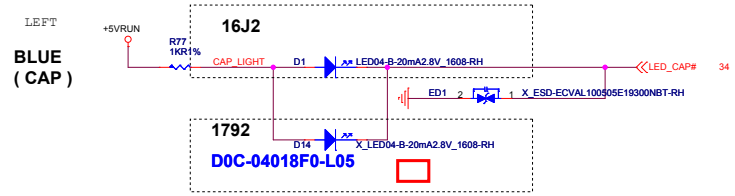
Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

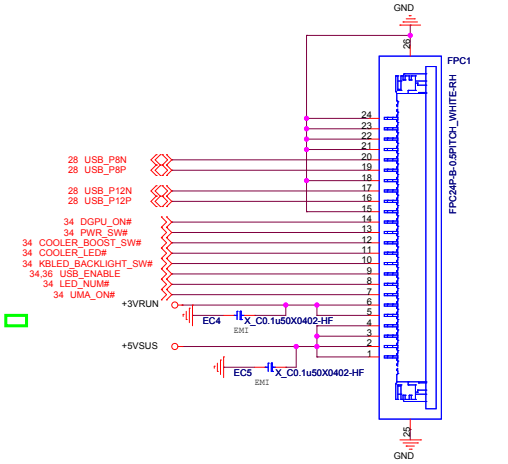
1792不上件

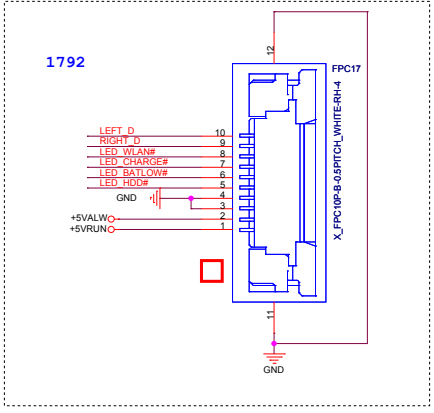
16J2

LED FRONT

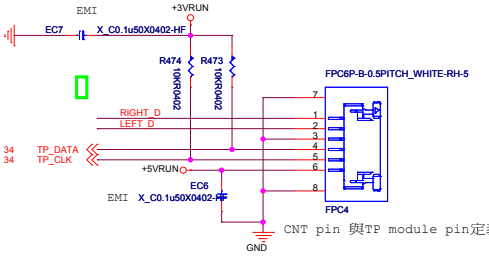


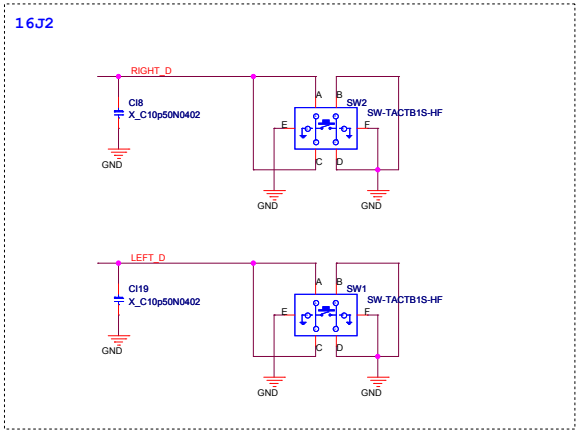






Touch Pad





msi	MICRO-STAR INT'L CO.,LTD.		
Title	WLAN /LED/TP		
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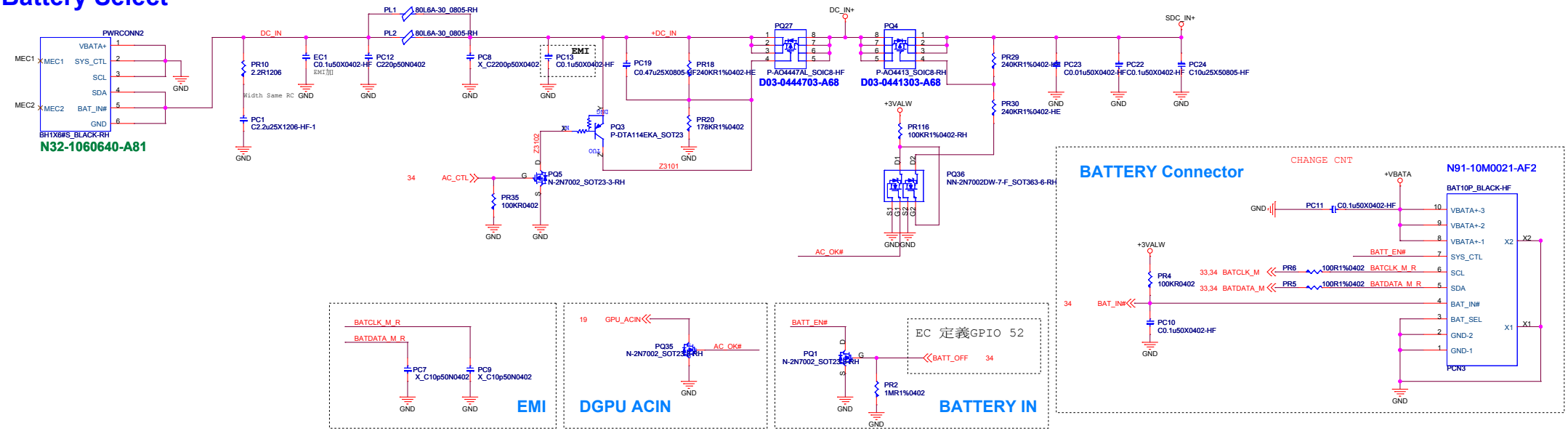
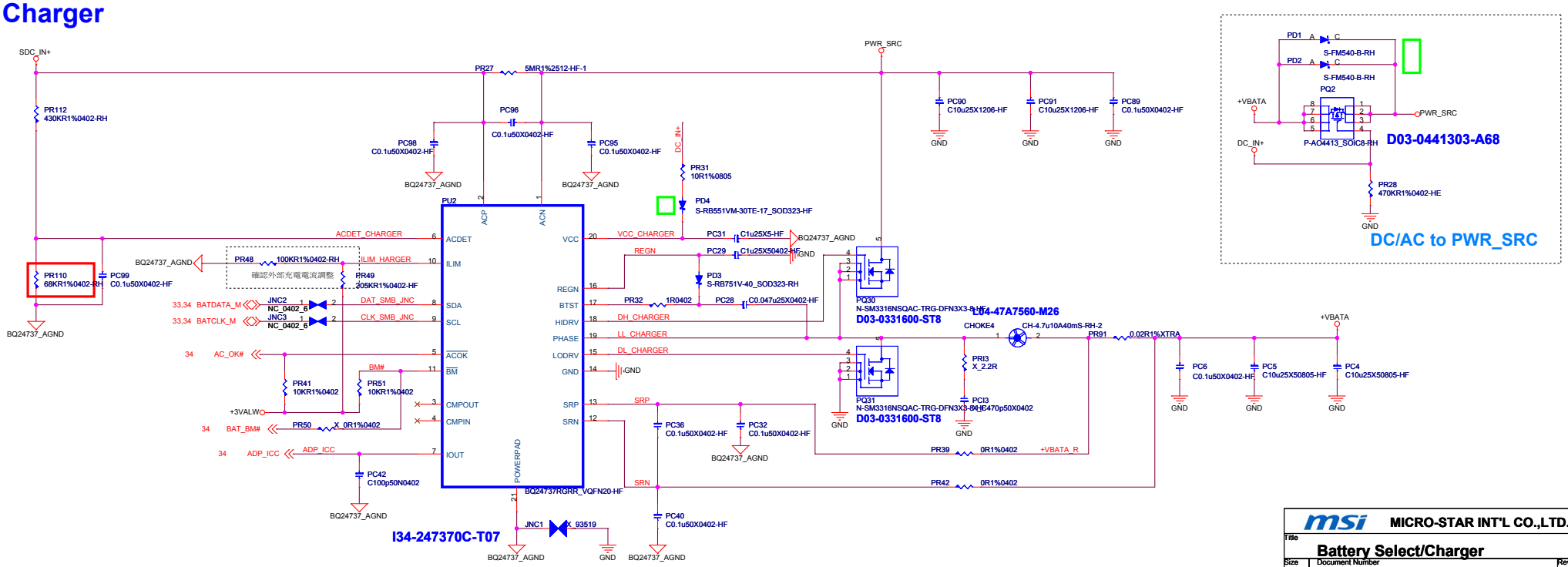
Battery Select/Charger

Battery Select



Battery Charger



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Battery Select/Charger		
Size	Document Number MS-16J2	Rev	0B
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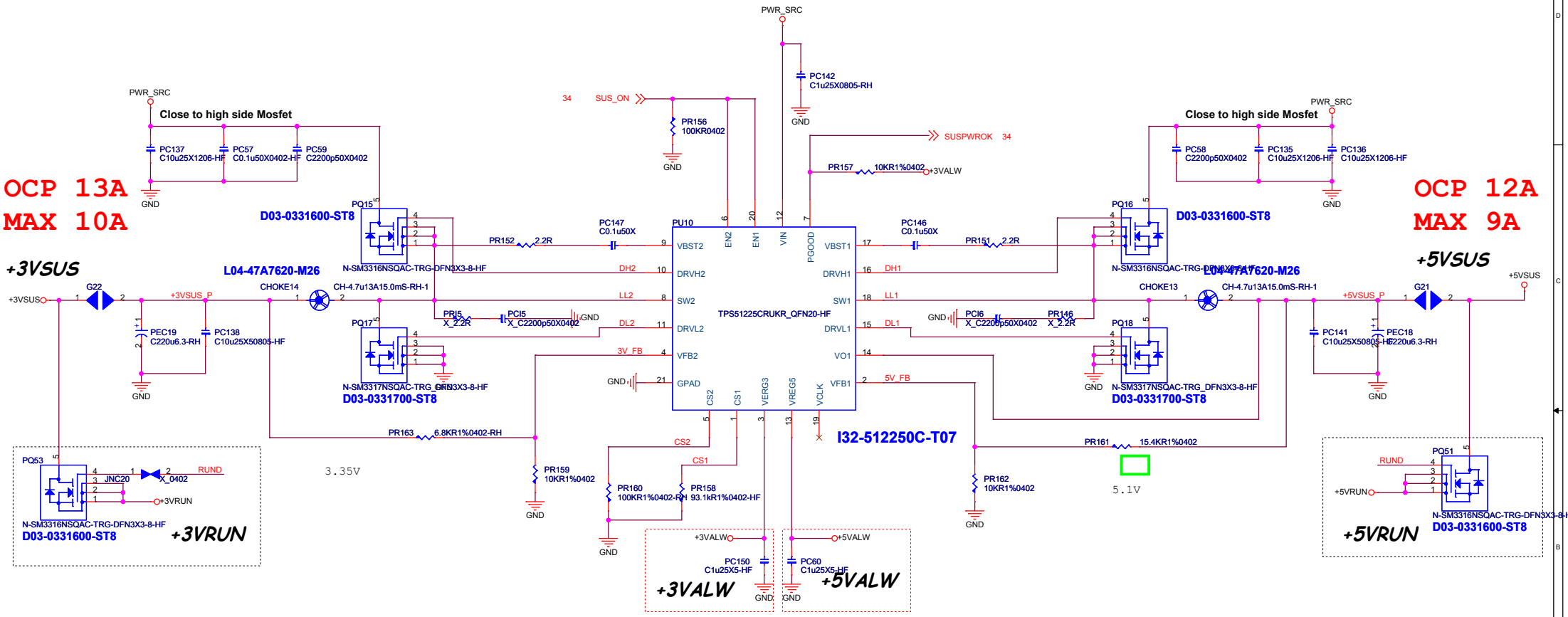
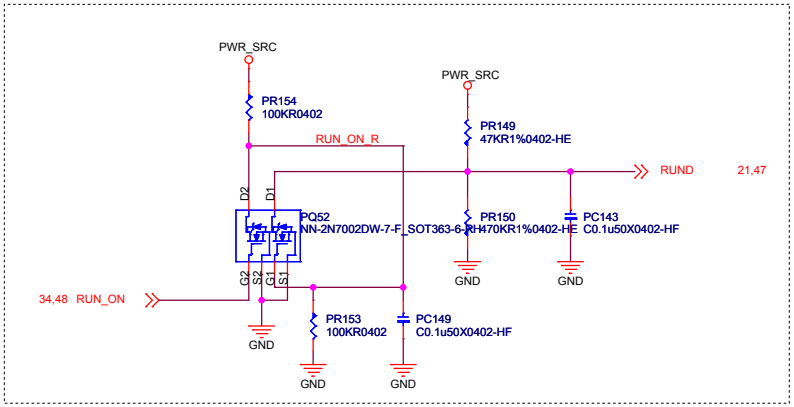
System Power





MICRO-STAR INT'L CO.,LTD.		
Title: System Power		
Size	Document Number: MS-16J2	Rev: 0B
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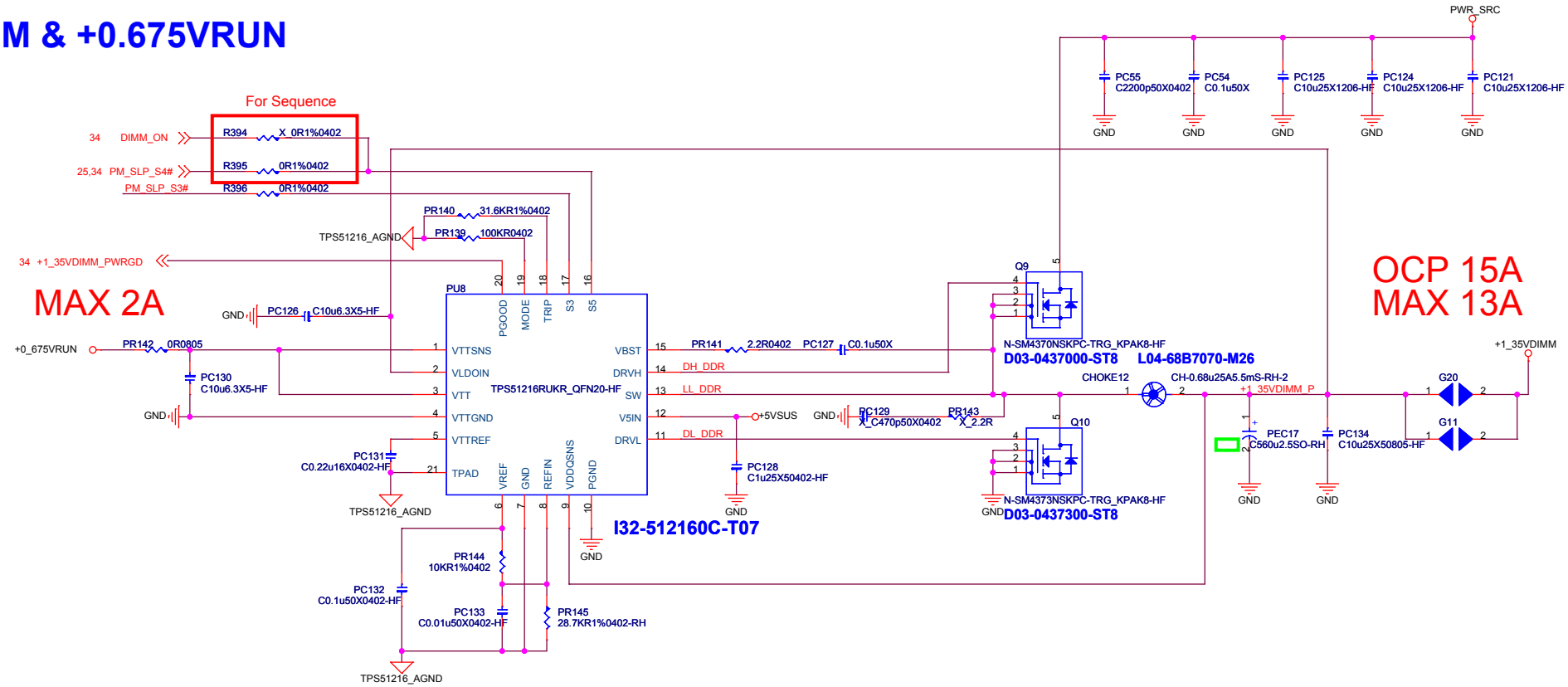
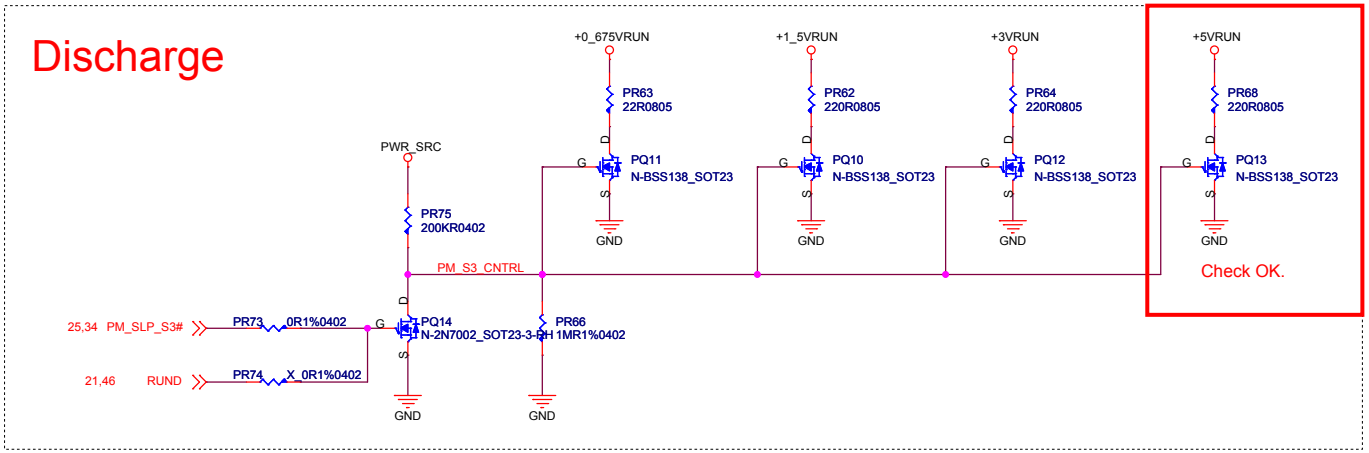
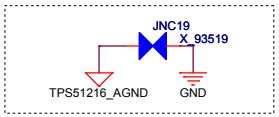
+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN







MICRO-STAR INT'L CO.,LTD.		
Title: +1.35VDIMM/+0.675VRUN		
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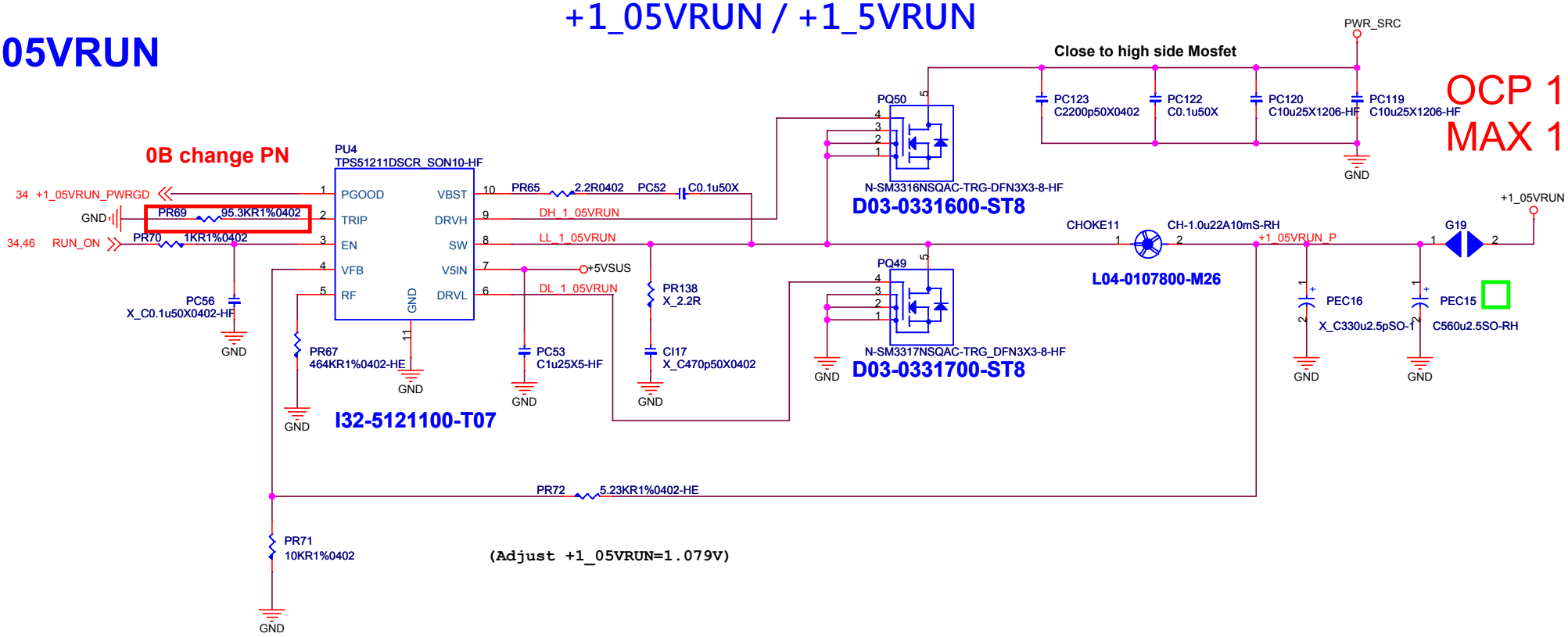
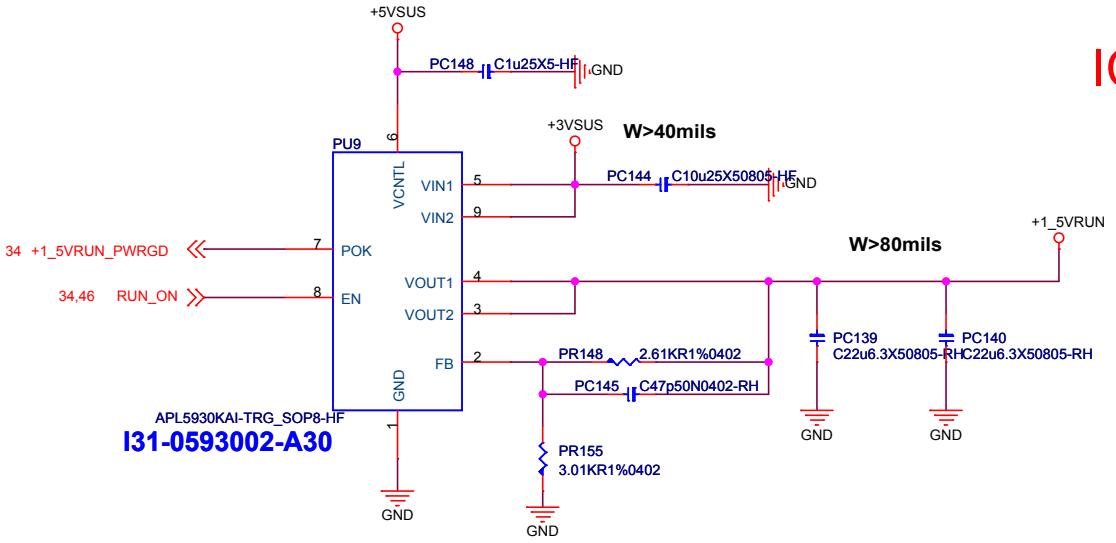
+1_05VRUN / +1_5VRUN

+1.05VRUN



+1.5VRUN



MICRO-STAR INT'L CO.,LTD.		
Title: +1_05VRUN / +1_5VRUN		
Size	Document Number: MS-16J2	Rev: 0B
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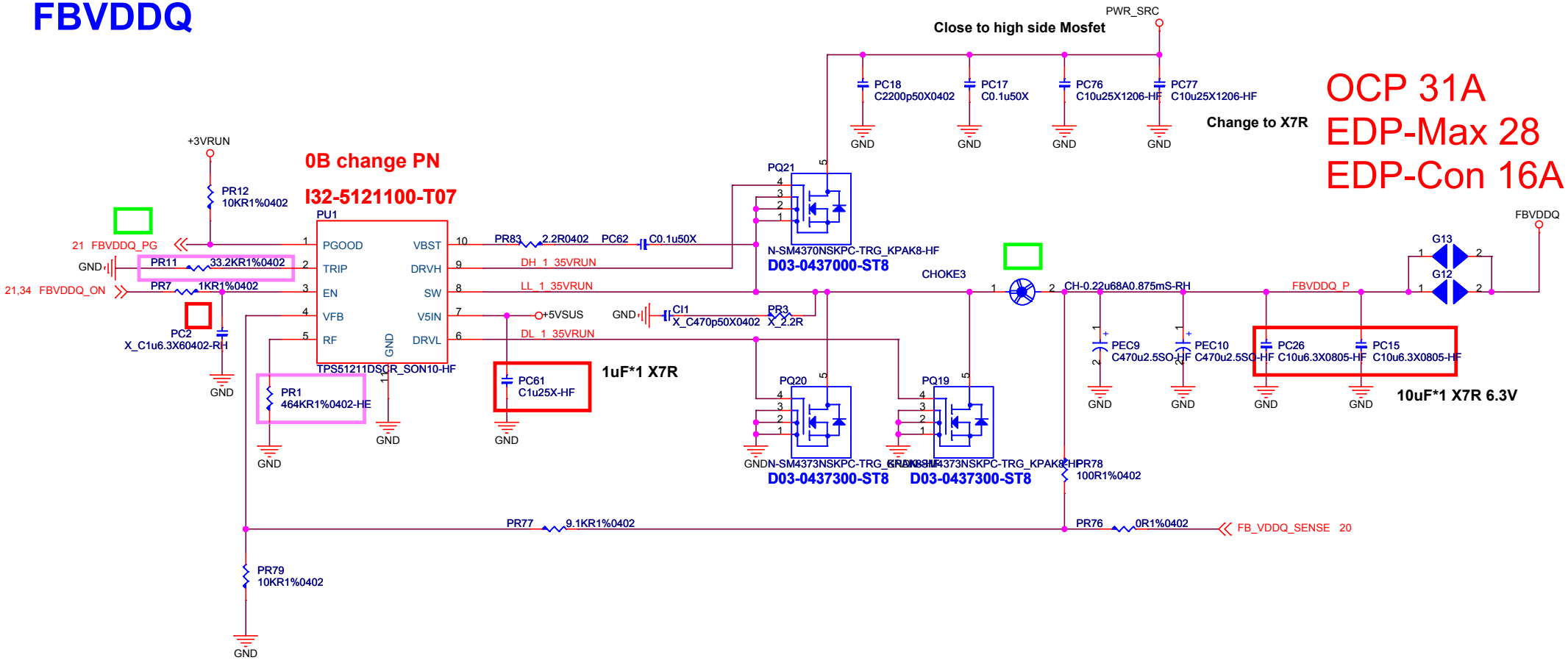
DGPU POWER FBVDDQ

FBVDDQ



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU POWER FBVDDQ		
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DGPU POWER / UP1642PQAG

EDP-Peak 85A

EDP-MAX 50A

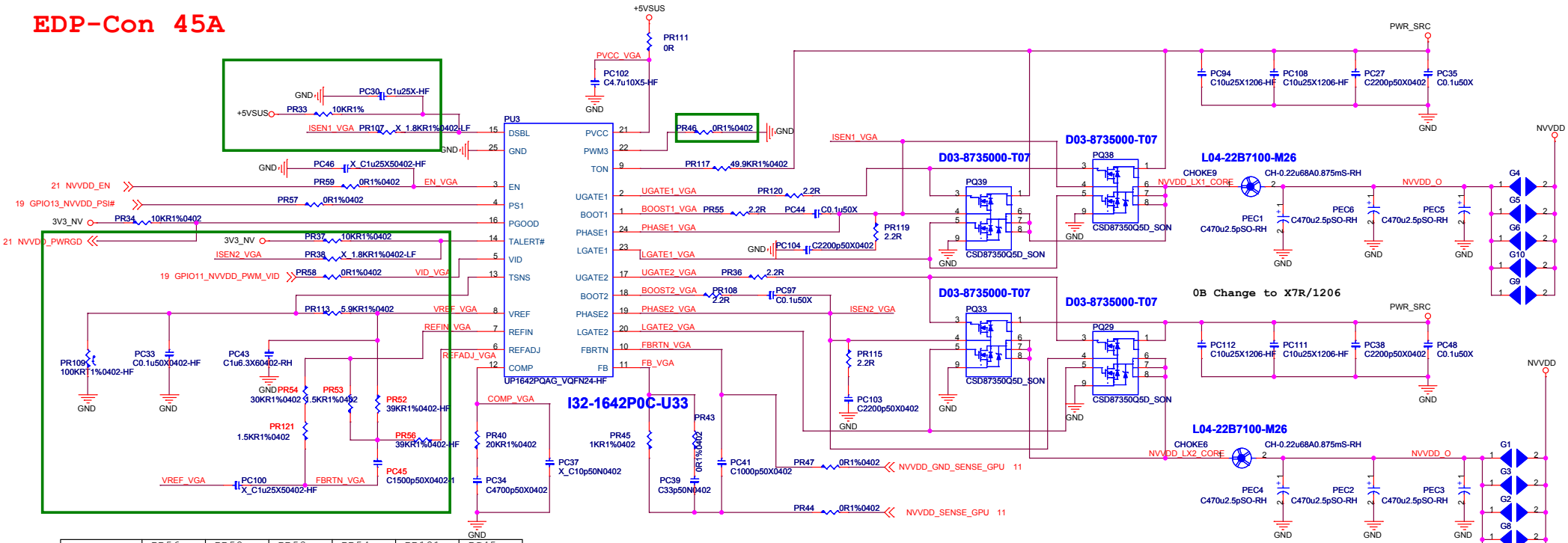
EDP-Con 45A

DGPU POWER NVVDD

CONFIG A

VBoot:0.875V

Vmin:0.6V / Vmax:1.2V



	PR56	PR52	PR53	PR54	PR121	PC45
CONFIG	R1	R2	R3	R4	R5	C
N16E-GT N16P-GX-B	39K	39K	1.5K	30K	1.5K	1.5nF

MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER NVVDD

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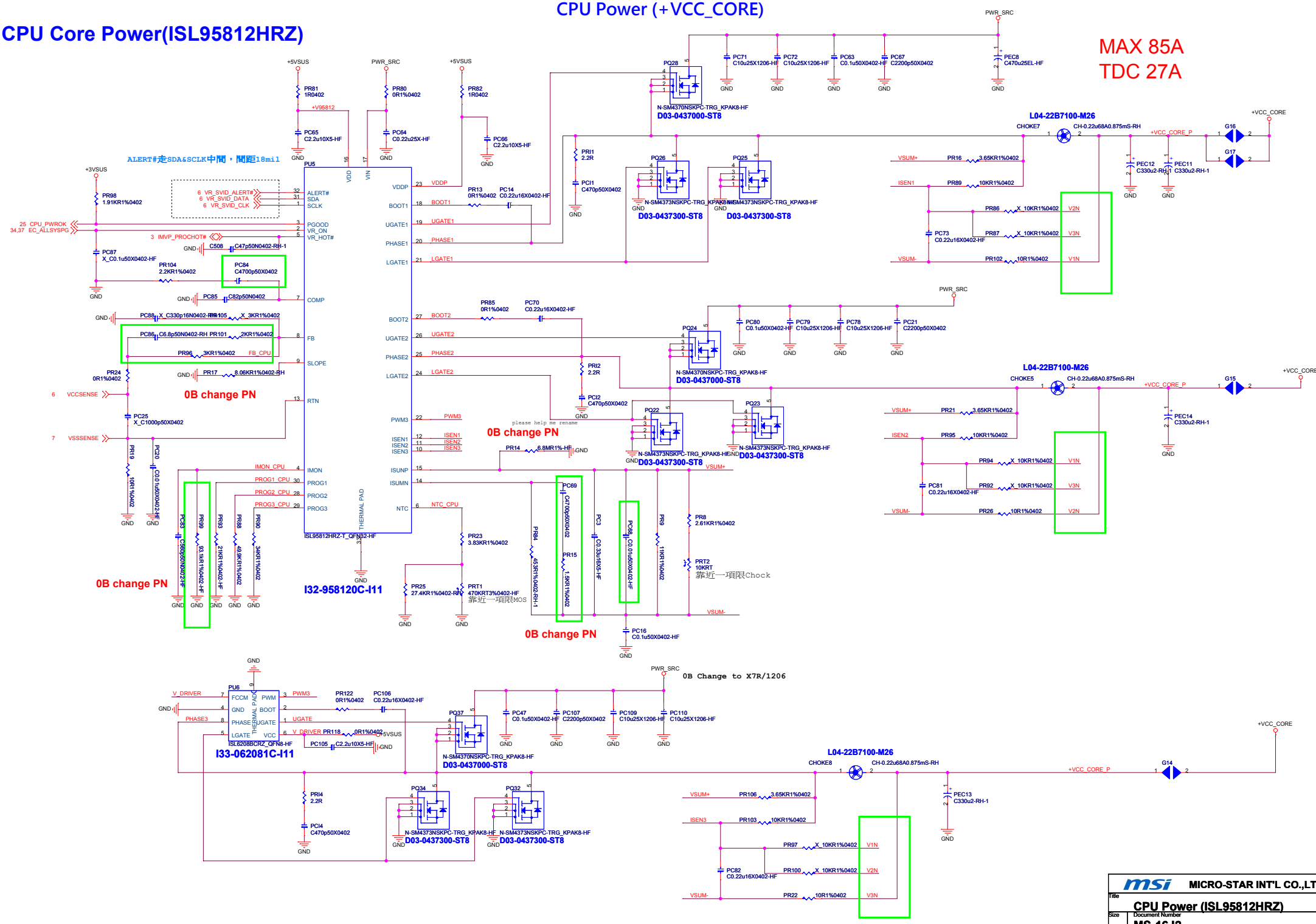
CPU Core Power(ISL95812HRZ)

CPU Power (+VCC_CORE)

MAX 85A
TDC 27A



MICRO-STAR INT'L CO.,LTD.			
Title: CPU Power (ISL95812HRZ)			
Size	Document Number: MS-16J2		Rev: 0B
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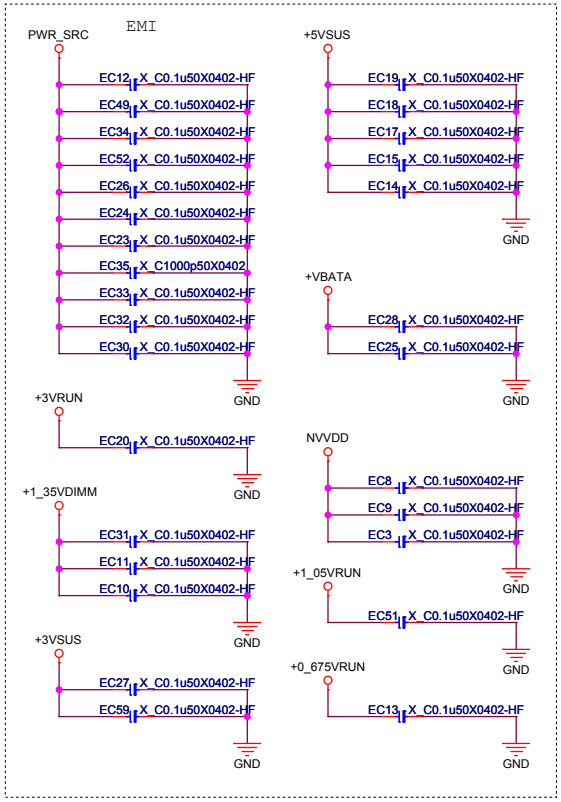

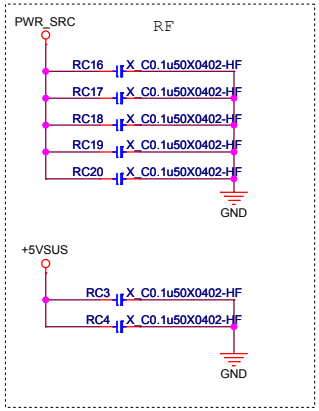

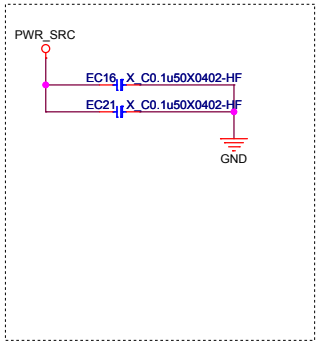

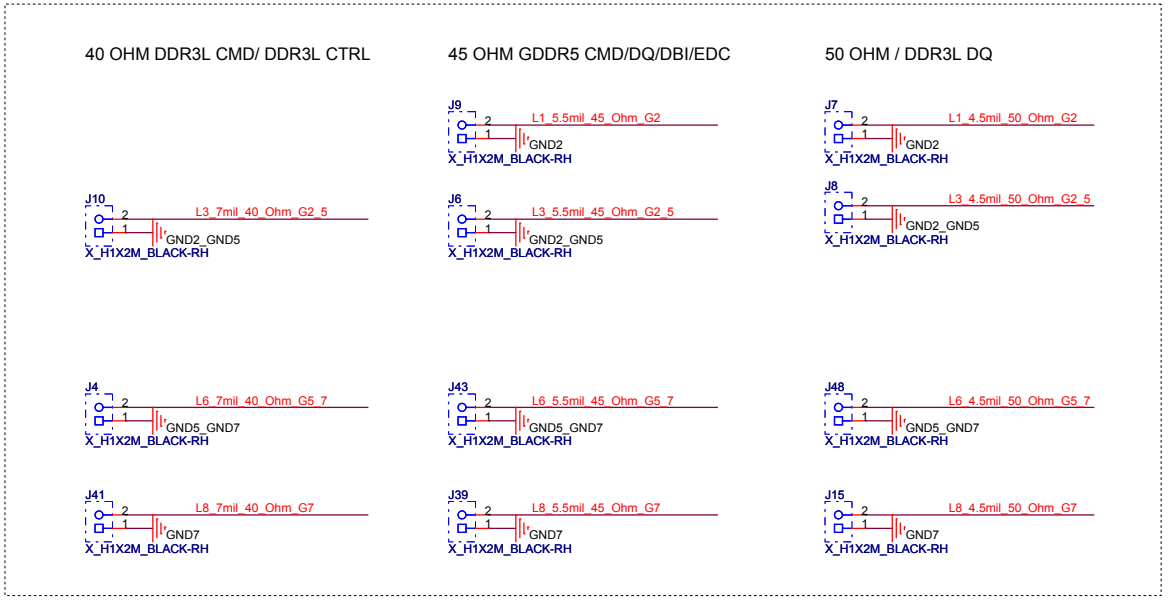

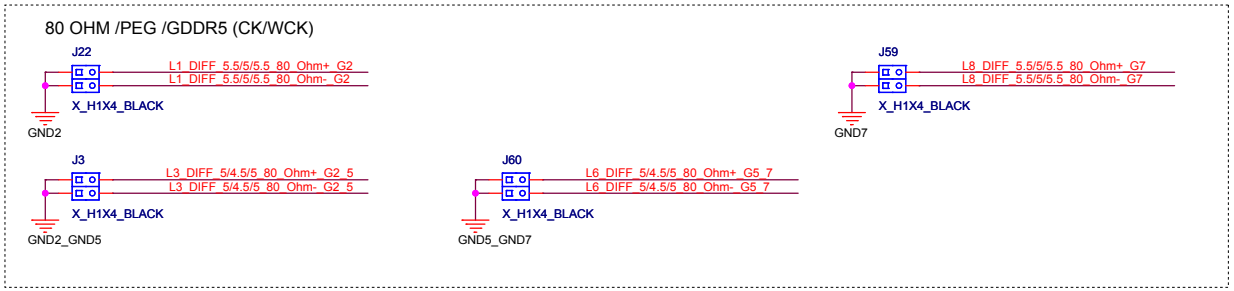

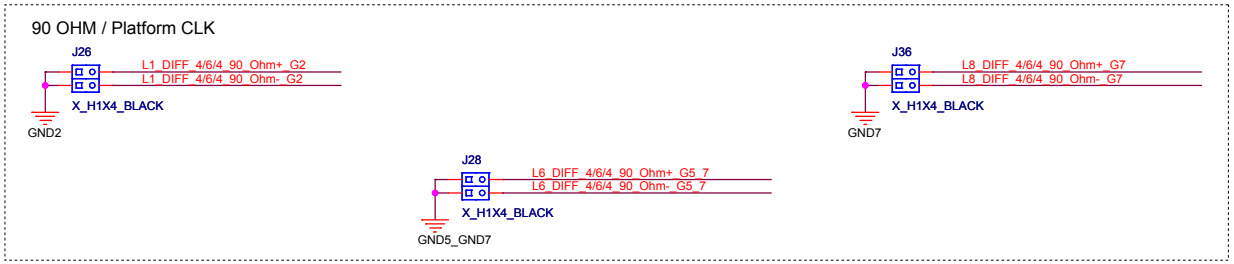

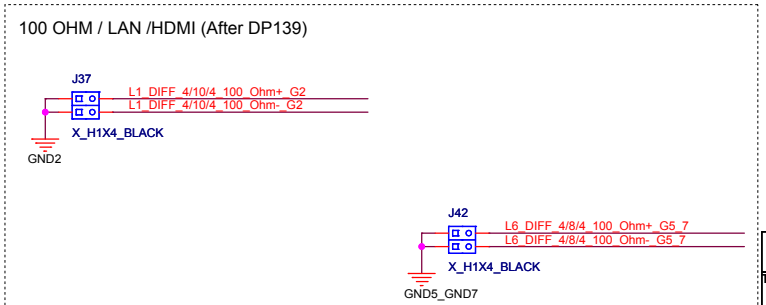

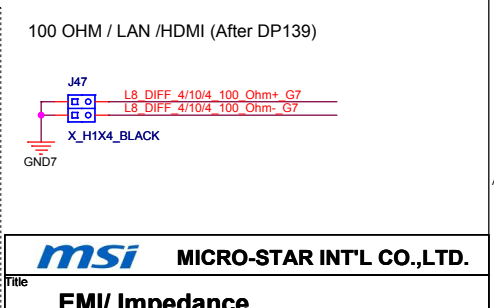

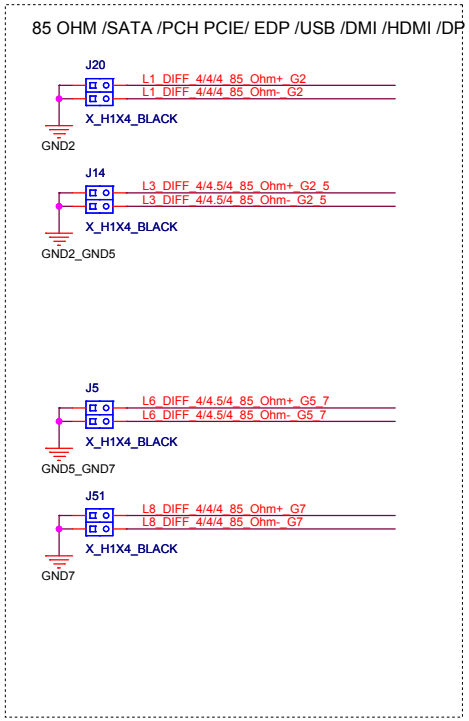

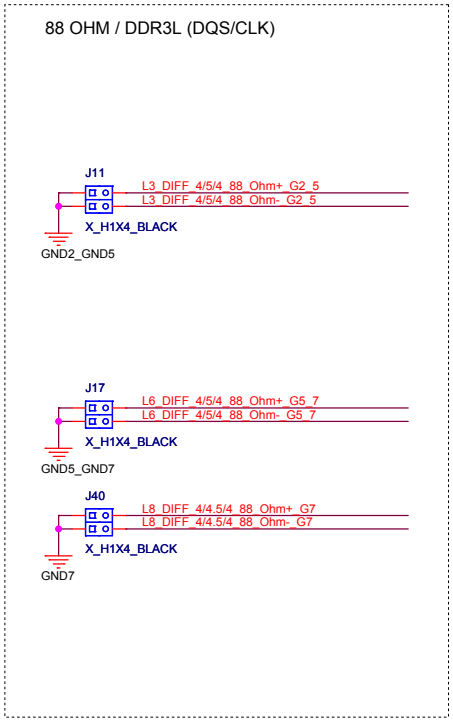

MICRO-STAR INT'L CO.,LTD.

Title: EMI/ Impedance

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CPU/GPU Holes

MCPU4 H_R276D169_PB
MCPU2 H_R276D169_PB
MCPU3 H_R276D169_PB
MCPU1 H_R276D169_PB
MGPU2 H_R276D169_PB
MGPU4 H_R276D169_PB
MGPU1 H_R276D169_PB
MGPU3 H_R276D169_PB

GND
X_CPU_HOLE

OD 2.3

MH6 H_R197D118_PT X_ME_ SCREW HOLE
MH3 H_R197D118_PT X_ME_ SCREW HOLE
修改內徑3mm
MH7 H_R197D91 X_ME_ SCREW HOLE
MH5 H_R197D91 X_ME_ SCREW HOLE
MH4 H_R197D91 X_ME_ SCREW HOLE

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8
FM9 FM10 FM11 FM12 FM13 FM14 FM15 FM16
FM17 FM18 FM19 FM20 FM21 FM22 FM23 FM24
X_FM

7/31 改料號

UME3 CPU BKT
CPU BKT
E2M-7810111-A89

UME4 GPU BKT
GPU BKT
307-6H20211-C22

8/5 改料號

UME5 CPU MYLAR
CPU MYLAR
E2P-6J11211-Y42

UME7 LED SPONGE
LED SPONGE
E2Y-6J10611-Y42

UME8 LED SPONGE
LED SPONGE
E2Y-6J10611-Y42

UME1 HDMI Lable
HDMI ROYALTY
Y01-RHDMI03-000

UME2 BIOS Lable
BIOS_LABEL
G51-LA01678-A09
For MP

PCB1
P30-16J210A-H73
P30-16J210A-H73
Hannstar: P30-16J210A-H73
TRIPOD: P30-16J210A-T53

UME11 HIDE_GAP_MYLAR
HIDE_GAP_MYLAR
E2P-6J11411-G40
20141016 ME add

版邊 內3 / 外8

MH1 H_R197D118_PT X_ME_ SCREW HOLE
HOLES_8X8_D3MM_VIA8
MH8 X_8x8

HOLE3 NPTH_80 X_NPTH_80
HOLE4 NPTH_80 X_NPTH_80
HOLE2 H_NR118D118_1 X_H_NR118D118_1
HOLE1 H_NR118D118_1 X_H_NR118D118_1
HOLE12 npth_98 X_npth_98
HOLE13 npth_98 X_npth_98
HOLE14 npth_98 X_npth_98
HOLE15 npth_98 X_npth_98

MH9 X_H_R197D118_PT_V3 H_R197D118_PT_V3
GND
MH2 X_H_R197D118_PT_V3 H_R197D118_PT_V3
LAN_GND

HOLE5 X_NPTH_80 NPTH_80
HOLE6 X_NPTH_80 NPTH_80
HOLE7 X_NPTH_80 NPTH_80
HOLE8 X_NPTH_80 NPTH_80
HOLE9 X_NPTH_80 NPTH_80
HOLE10 X_NPTH_80 NPTH_80
HOLE11 X_NPTH_80 NPTH_80

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Title: Screw/ME
Size:
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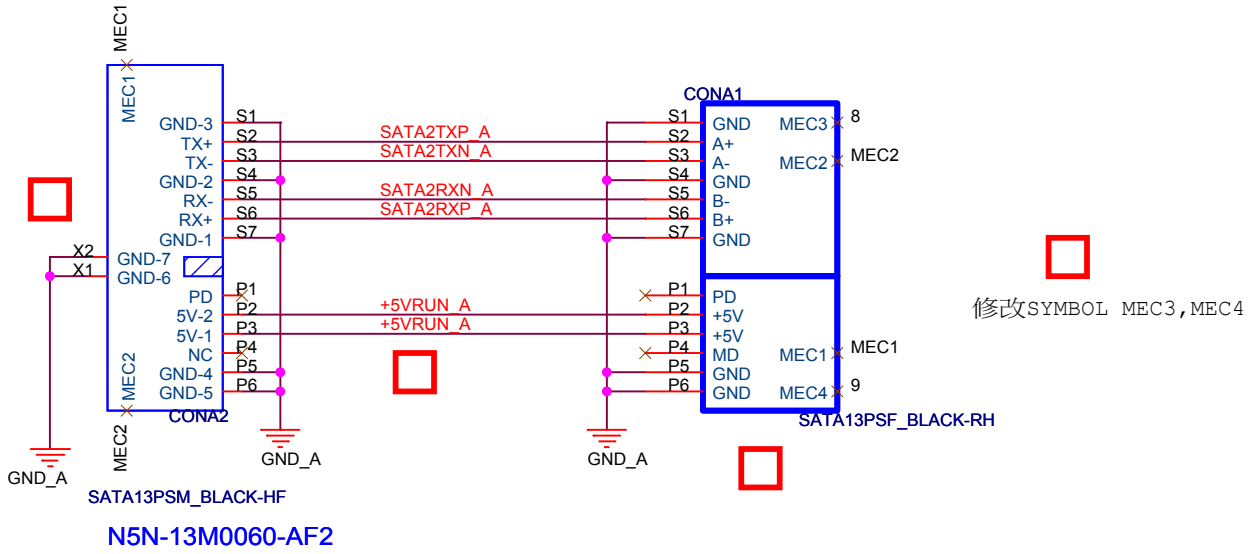

N5N-13M0060-AF2

PCBA1

P30-16J2A0A-H73

P30-16J2A0A-H73

HB2
X_NPTH_80
NPTH_80

HB1
X_NPTH_80
NPTH_80

MB1
X_H_R197D91
H_R197D91

MB2
X_H_R197D91
H_R197D91

GND_A GND_A

SCREWA2 SCREWA1

E43-1205003-H29 **E43-1205003-H29**

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Title: **[A] 1792 ODD**

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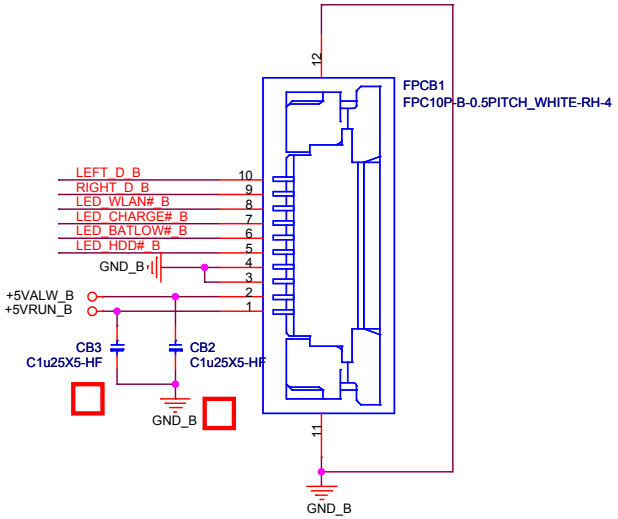
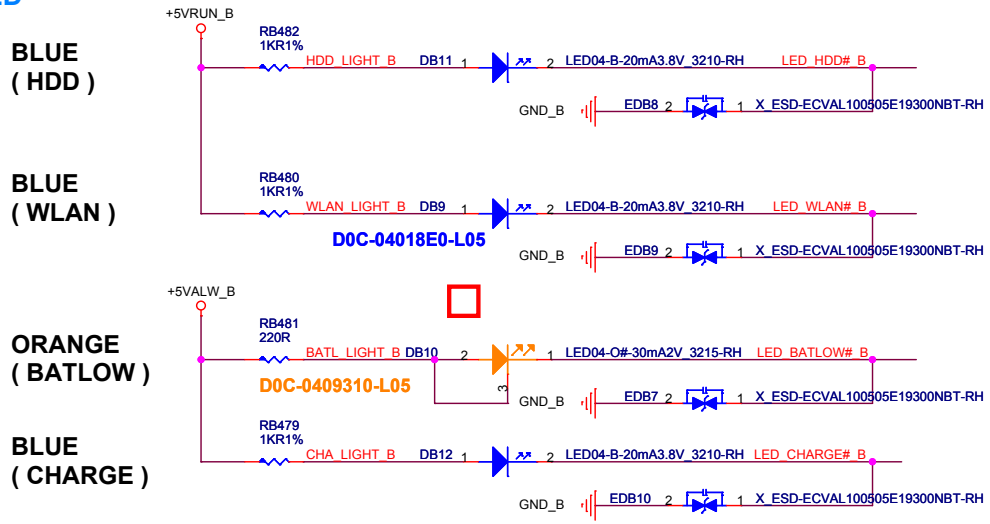
1792

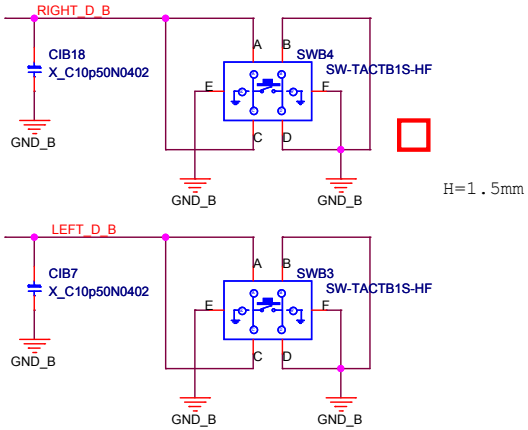


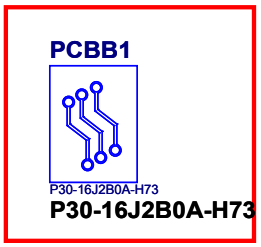
LED

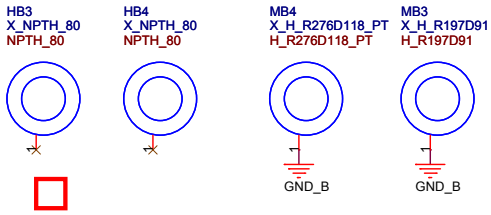
FRONT



1792







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Title: [B] 1792 LED/ TP

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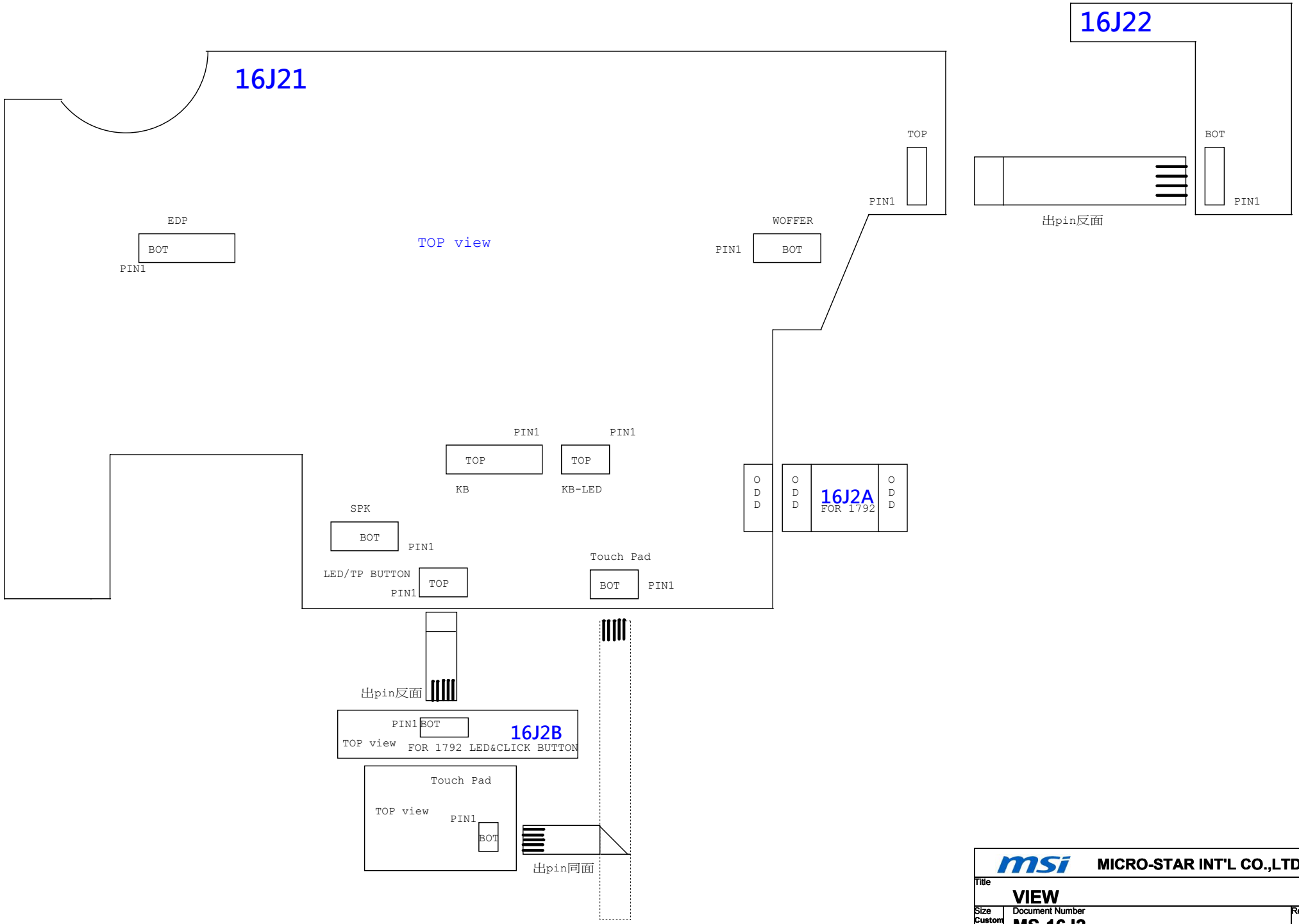

msi MICRO-STAR INT'L CO.,LTD.		
Title: VIEW		
Size: Custom	Document Number: MS-16J2	Rev: 0A
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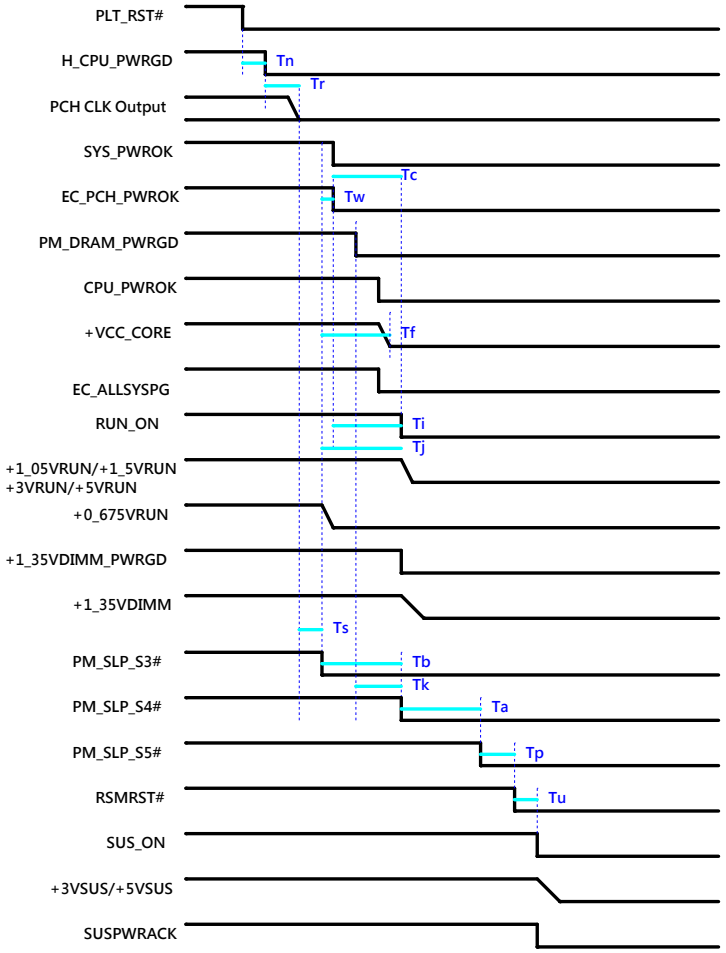
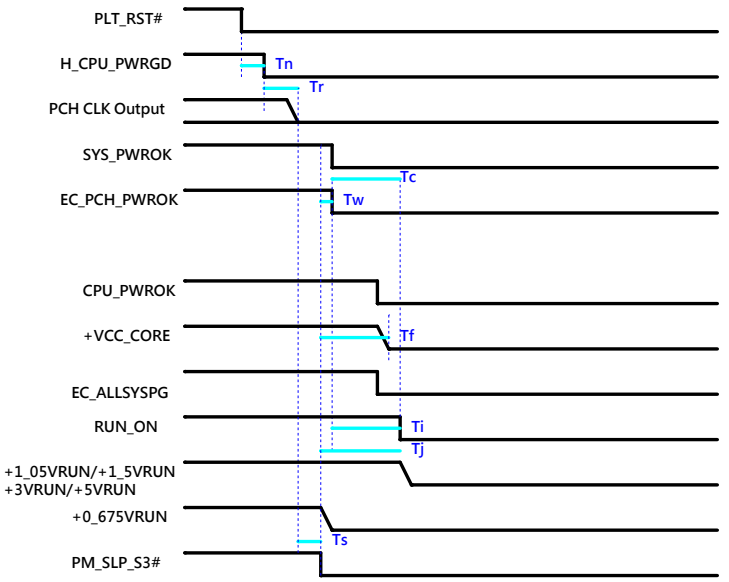
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3



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Title: Power down Sequence

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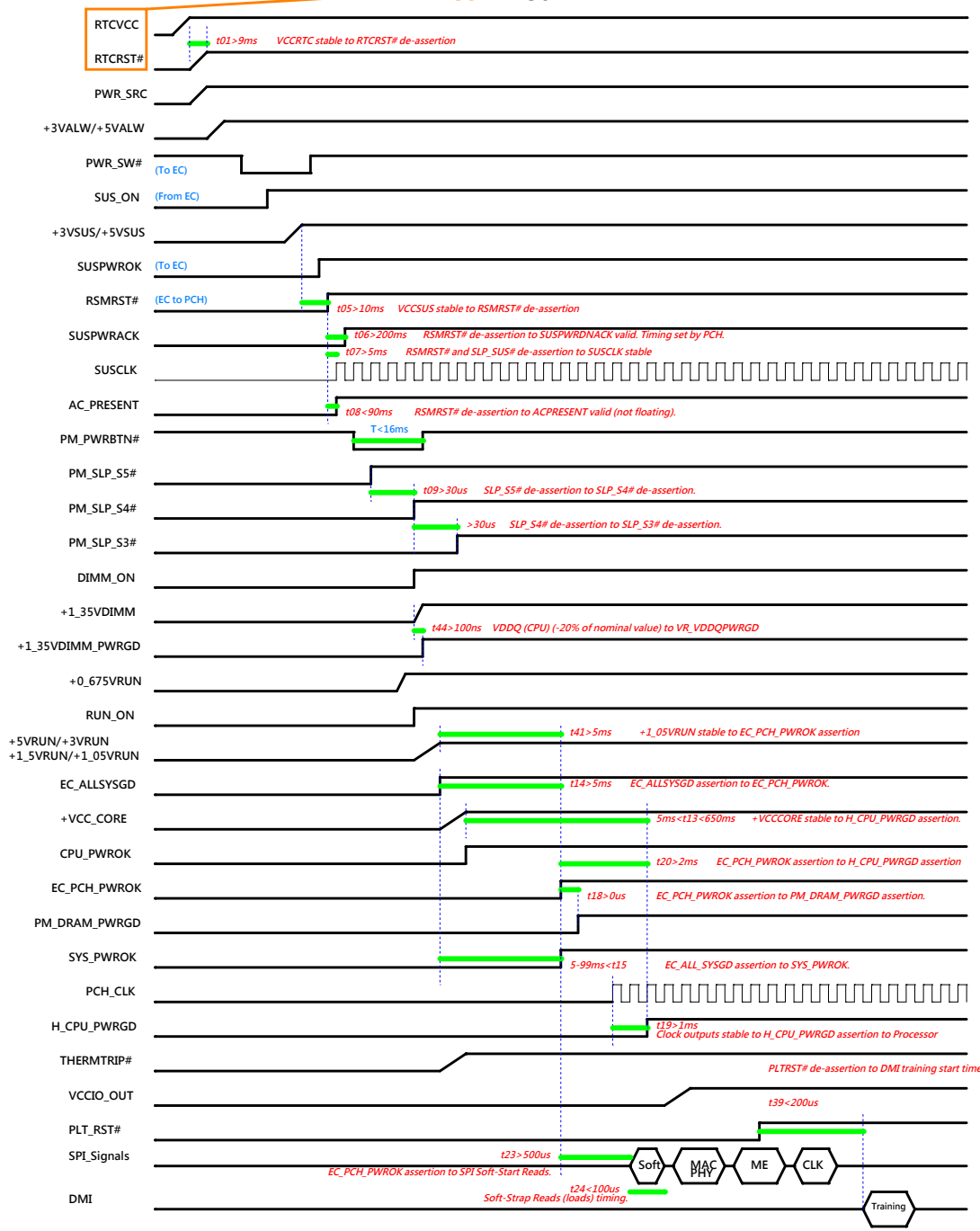
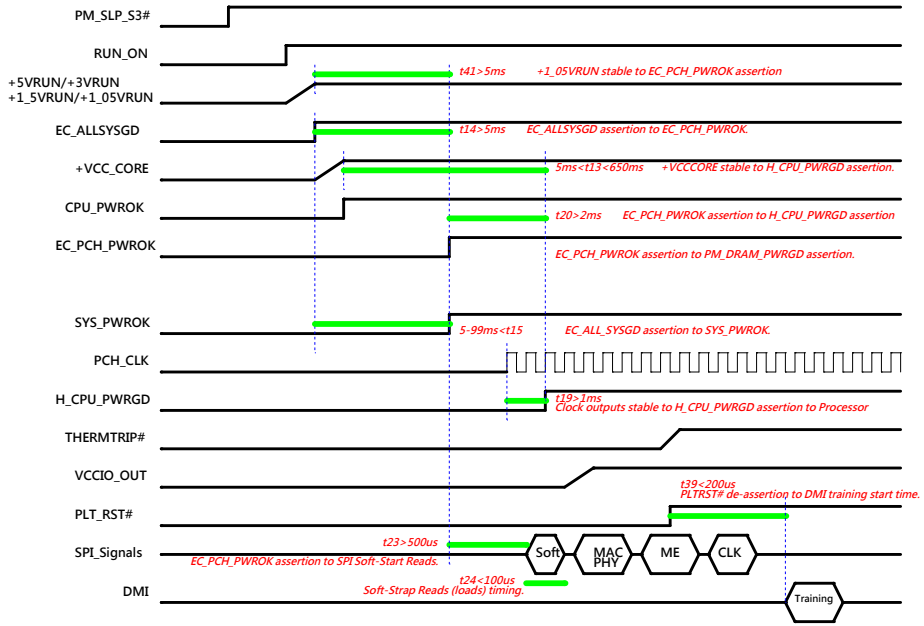
Power on Sequence

G3 -> S0



S3-> S0



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Title: Power on Sequence

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History

0A

Page	Description
21	change U8 from I36-3512A09-A30 to I36-0351109-A30 to reduce softstart time to 400uS
19	modify GPU GPIO setting to follow design guide
18	modify STRAP pin power from 3V3_NV to 3V3_AON (refer to CRB)
11	G3000 update to formal P/N OB3-AE6B101
18	modify GPU strap pin R value to follow CRB
11	delete R3085 and R3092 for useless (delete signals GFX_REFCLK1 and GFX_REFCLK1#)
13	R3170,R3171,R3172,C3315,C3276 change to unstuff to follow CRB and design guide
14	R3169,R3175,R3180,C3277,C3318 change to unstuff to follow CRB and design guide
15	R3057,R3064,R3068,C3057,C3058 change to unstuff to follow CRB and design guide
16	R3139,R3141,R3142,C3258,C3263 change to unstuff to follow CRB and design guide
13~16	delete net from VPP01_JNC to VPP16_JNC for useless
50	delete net ISEN3_VGA and PR114 for useless
34	add net EC_PROTECT_PWR
19	GPU I2CS interface connect with 3V3_AON
49~50	change PWR_SRC_FBVDDQ,PWR_SRC_NVVDD to PWR_SRC
52	delete EC2,EC21,EC22,EC29 for useless
19	add R3263
52	fix impedance
20	add JNC24
19	R3274 change from 10K to 100K to follow design guide
21	delete PQ46 and R373 for useless
21	delete PQ47,PQ48(D03-0700299-F09) and add PQ55(D03-7002D10-D07)
21	change PQ7 from D03-0700299-F09 to D03-7002D10-D07
21	change PC118 footprint from C0603 to C0402
39	J1 change to connect with GND
24	change U34 from socket to BIOS ROM
11~21	change Cap from 0805 to 0603 (C3065,C3075,C3187,C3259,C3448,C3455,C3064, C3074,C3218,C3435,C3450,C3451)
11~21	change Cap from X5R to X6S (C3113,C3121,C3123,C3124,C3128,C3221,C3223, C3225,C3228)
11~21	change Cap from X5R to X6S (C3310,C3314,C3308,C3312,C3513,C3179,C3182, C3193,C3222)
21	change C354 from C11-1063034-W08 to C11-1062314-M09
53	MH7 change to connect with GND
59	use MS-16J2_0A_0928B2.upd to update material
53	add UME7 and UME8 for LED sponge
58	update schematics description
50	change PWR_SRC_NVVDD to PWR_SRC
53	UME2 BIOS LABEL change to stuff
	modufy schematics by NVIDIA request
53	remove Q3003,R3099 and connect PEX_CLKREQ# to Q3008
18	C3438,C3439 change to 18pF
20	C3237 change to 1uF
17,19	add R292,R293,R294,R295,R296,R297
44	SW1 and SW2 change to N71-0101630-D02 to fix ME problem
44,55	modify SW1,SW2,SWB3,SWB4
19	change C3090,C3109,C3170,C3206,C3208 to 4.7uF to follow NVIDIA suggestion
52	delete useless impedance line
39	reserve C488,C489 to connect GND with AGND
52	reserve EC16,EC21 to connect PWR_SRC with GND
34	SW5 change to unstuff
2	Add compare list for BOM
39	delete JNC15 and R203, add C490 and C491 by vendor suggestion
32	modify eDP pin define
13~16	change C3514,C3293,C3278,C3288,C3307,C3294,C3289, C3122,C3175,C3176,C3177,C3239,C3197,C3195 from C11-4767314-T34 to C11-1062314-M09
2	update compare list for BOM
ALL	update 5010/5020
33	C805 unstuff
2	update compare list for BOM (Add Micron in AVL)
42	ME add HDD sponge UME9,UME10
53	ME add HIDE_GAP_MYLAR UME11

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Title: History

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