Tesla Schematics
Skylake-U

BOM1

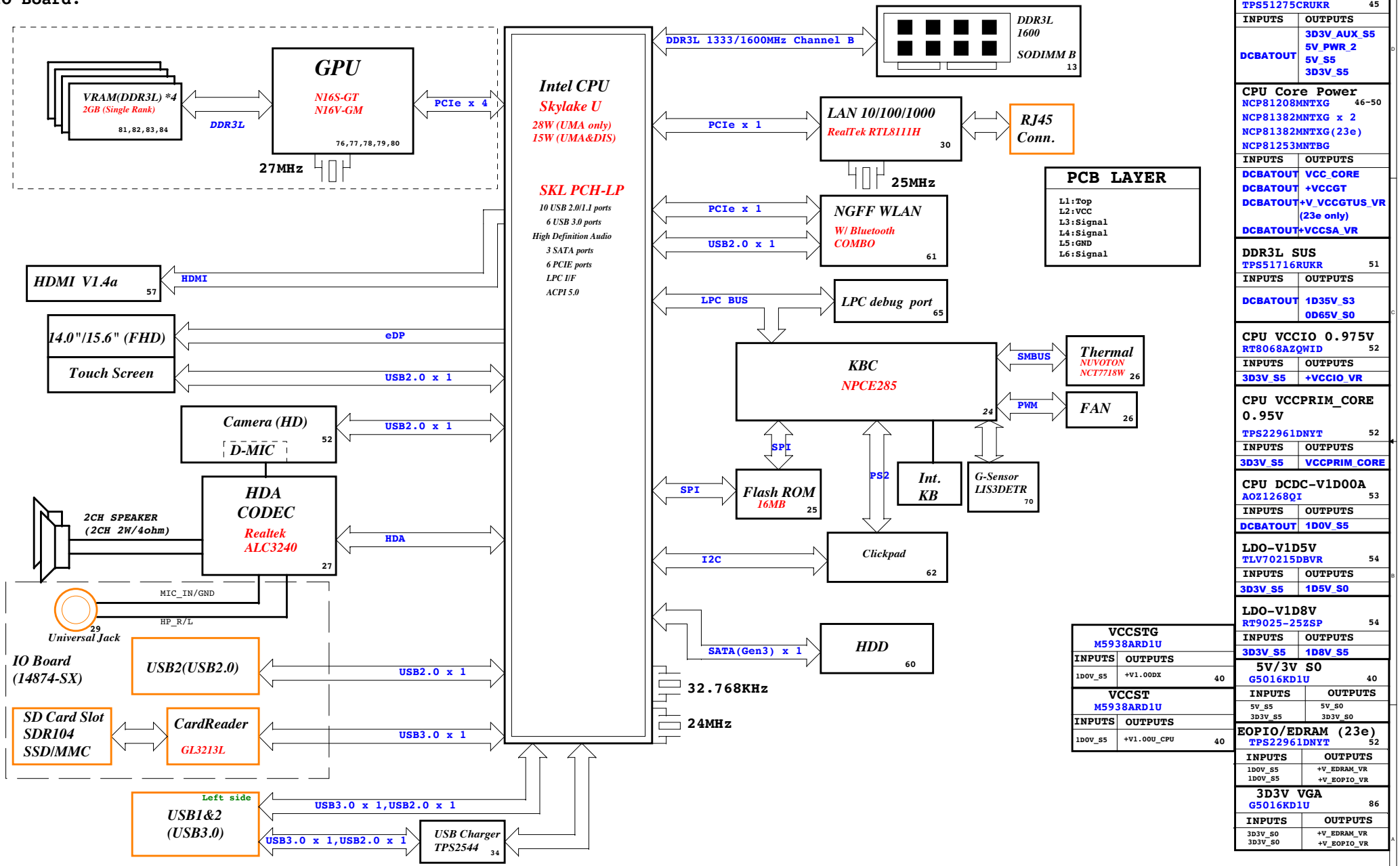
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***		
Size: A3	Document Number: **Tesla SKL-U**	Rev: **-1**
Date: Tuesday, July 21, 2015	Sheet 1 of 102	

Project code:
PCB P/N: 14292-1
Revision: -1

IO Board:

Tesla SKL-U Block Diagram



CHARGER BQ24780RUYR 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51275CRUKR 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5

CPU Core Power NCP81208MNTXG 46-50
NCP81382MNTXG x 2
NCP81382MNTXG(23e)
NCP81253MNTBG

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+V_VCCGTUS_VR (23e only)
DCBATOUT	+VCCSA_VR

DDR3L SUS TPS51716RUKR 51

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU VCCIO 0.975V RT8068AZQWID 52

INPUTS	OUTPUTS
3D3V_S5	+VCCIO_VR

CPU VCCPRIM_CORE 0.95V TPS22961DNYT 52

INPUTS	OUTPUTS
3D3V_S5	VCCPRIM_CORE

CPU DCDC-V1D00A AOZ1268QI 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D5V TLV70215DBVR 54

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

LDO-V1D8V RT9025-25ZSP 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 G5016KD1U 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e) TPS22961DNYT 52

INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA G5016KD1U 86

INPUTS	OUTPUTS
3D3V_S0 3D3V_S0	+V_EDRAM_VR +V_EOPIO_VR

VCCSTG M5938ARD1U

INPUTS	OUTPUTS
1D0V_S5	+V1.00DX 40

VCCST M5938ARD1U

INPUTS	OUTPUTS
1D0V_S5	+V1.00U_CPU 40

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

BOM1

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Title: Block Diagram
Size: C | Document Number: Tesla SKL-U | Rev: -1
Date: Tuesday, July 21, 2015 | Sheet 2 of 102

Main Func = CPU

(Blanking)

BOM1

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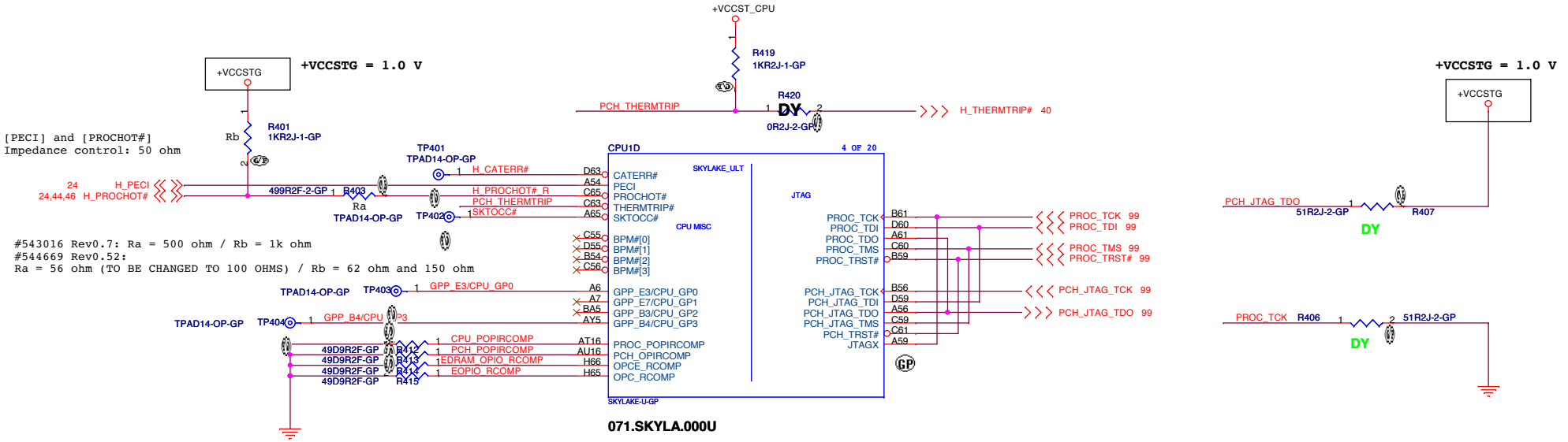
Title: Reserved

Size: A3 | Document Number: Tesla SKL-U | Rev: -1

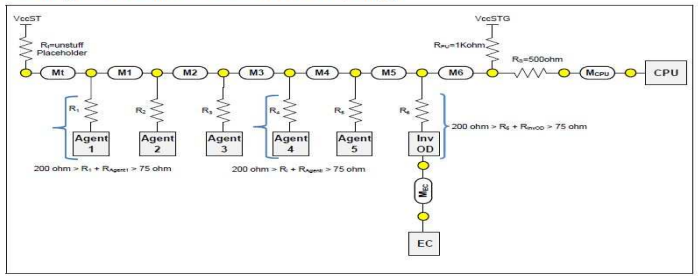
Date: Tuesday, July 21, 2015 | Sheet 3 of 102

Main Func = CPU



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

BOM1

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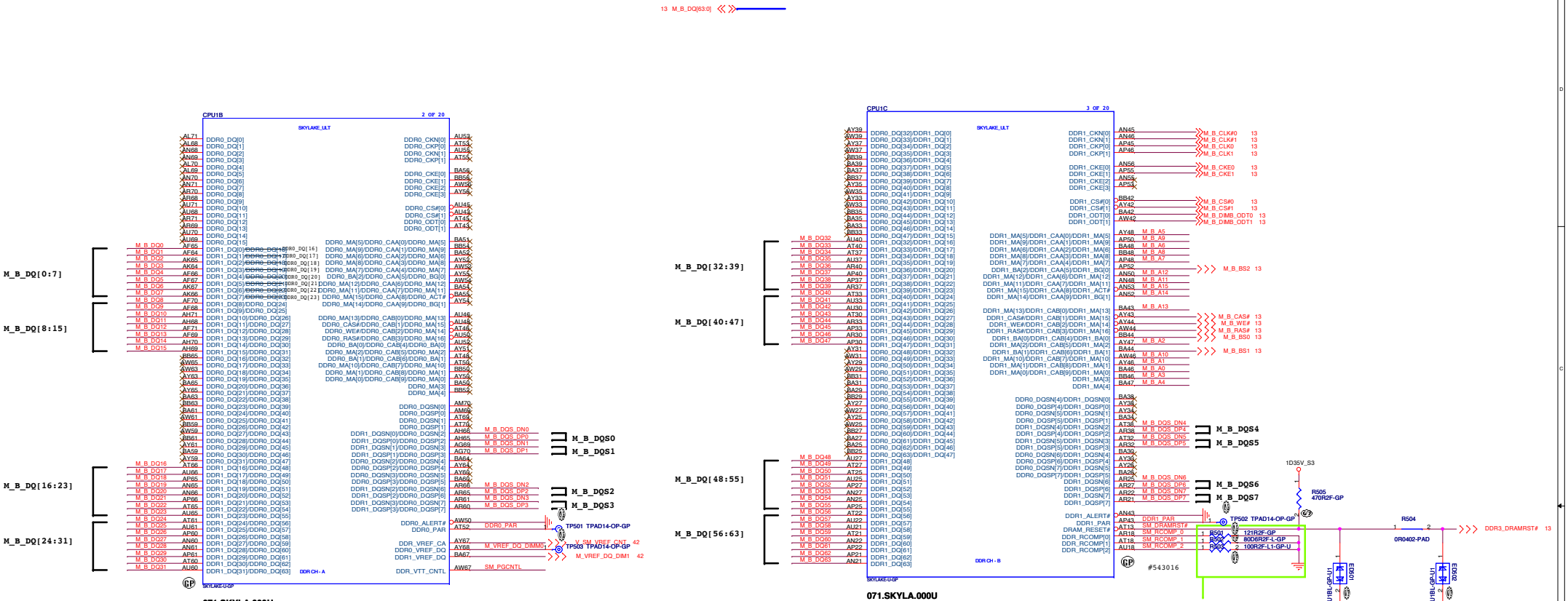
Title: CPU (JTAG/CPU SIDE BAND)

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 4 of 102

Main Func = CPU

DDR3L ball type: Interleaved Type



071.SKYLA.000U

071.SKYLA.000U

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

Layout Note:

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

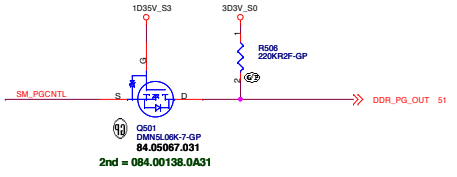
PDG: DDR/ODT

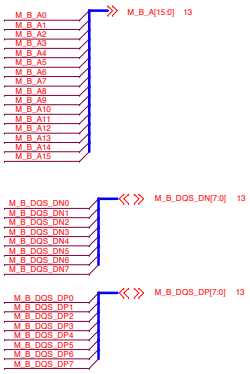
4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT . Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z).
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.





BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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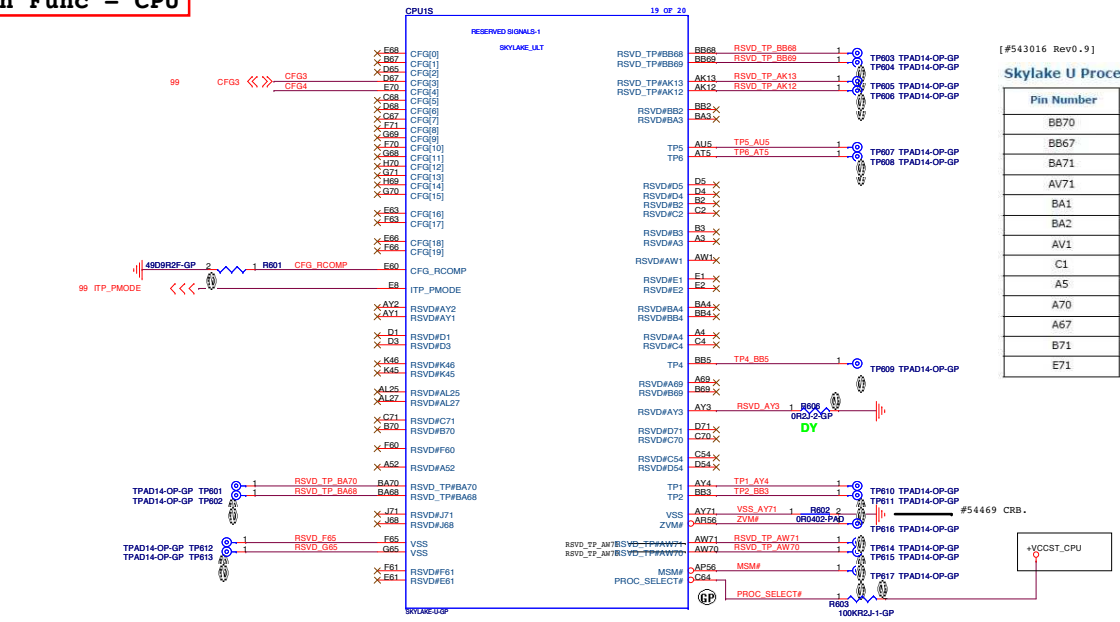
Title: CPU (DDR)

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 5 of 102

Main Func = CPU

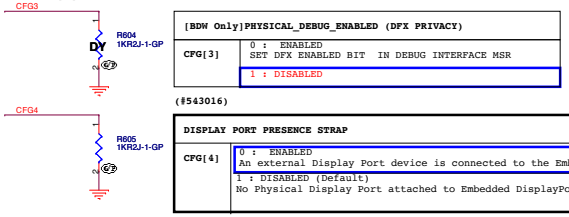


[#543016 Rev0.9]

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

PCH strap pin: **071.SKYLA.000U**



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

BOM1

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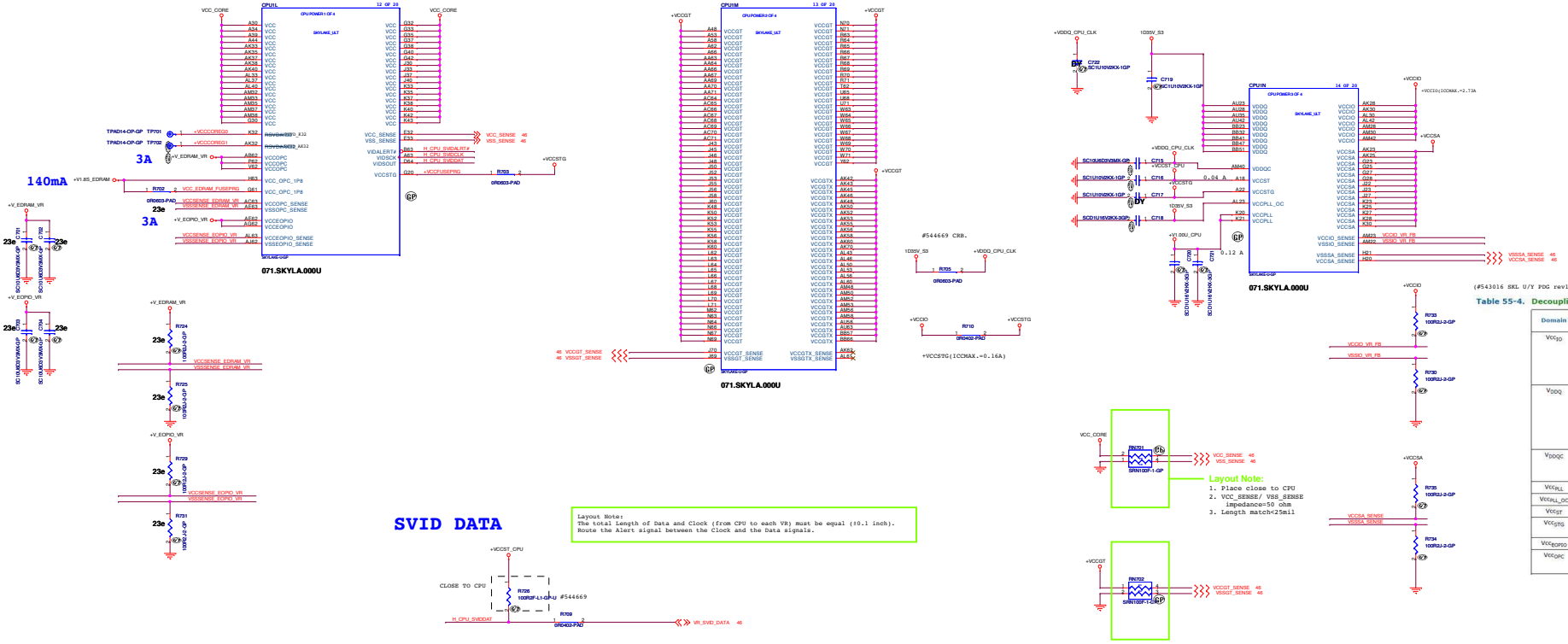
Title: CPU (RESERVED)

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 6 of 102

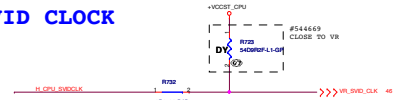
Main Func = CPU

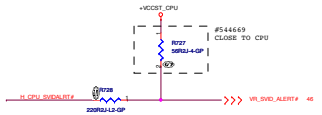


SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID CLOCK



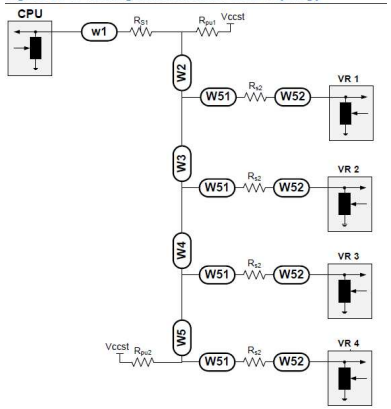


SVID_543016:

Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU0} [Ω]	R_{PU1} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{BT} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology



(#543016 SKL U/Y PDG rev1.0)

Table 55-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
V_{CCIO}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 1uF 0402	Place as close to the package as possible
V_{DDQ}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 10uF 0402	Place as close to the package as possible
		3 x 22uF 0603	Place as close to the package as possible
V_{DDQC}	1x 1uF 0201 (Placeholder)		Place on secondary side, underneath the package
		1 x 10uF 0402	Place as close to the package as possible
V_{CCPLL}		1x 1uF 0402	Place as close to the package as possible
V_{CCPLL_OC}		1x 1uF 0201	Place as close to the package as possible
V_{CCST}		1x 1uF 0402	Place as close to the package as possible
V_{CCSTG}	1x 1uF 0402 (Placeholder)		Place on secondary side, underneath the package Placeholder only
$V_{CCEOPIO}$	2x 10uF 0402		Place on secondary side, underneath the package
$V_{CCEOPIC}$	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

BOM!

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21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
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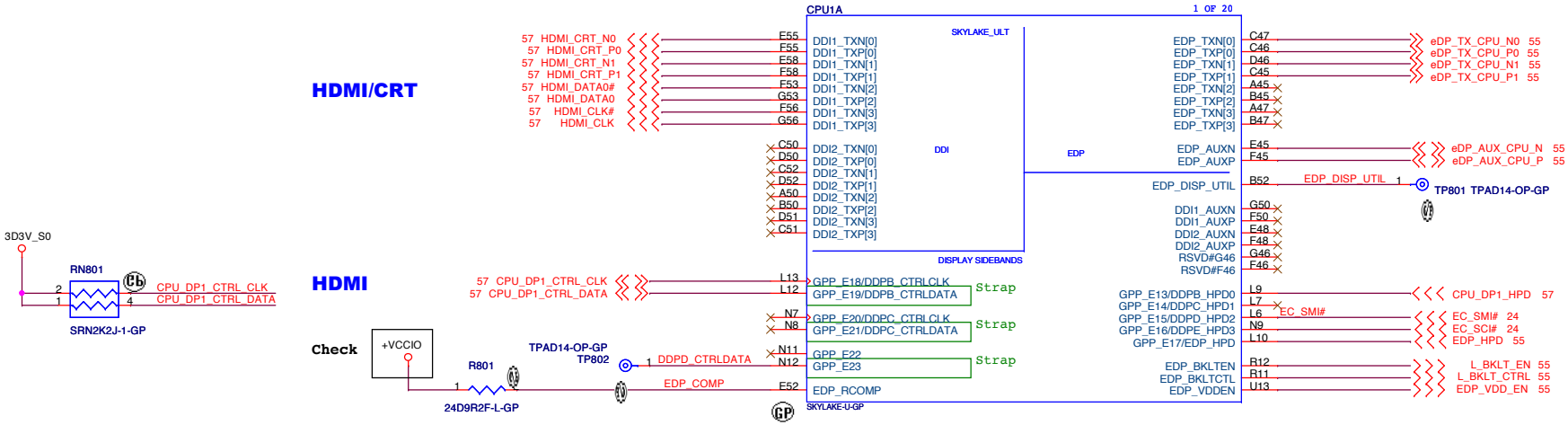
Title: CPU(VCC_CORE)

Size: A3 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 7 of 102

Main Func = CPU



071.SKYLA.000U

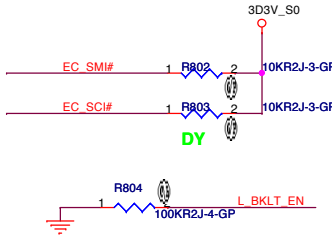
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

BOM1

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Title: CPU_(DISPLAY)

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 8 of 102

Main Func = CPU

(Blanking)

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)CPU

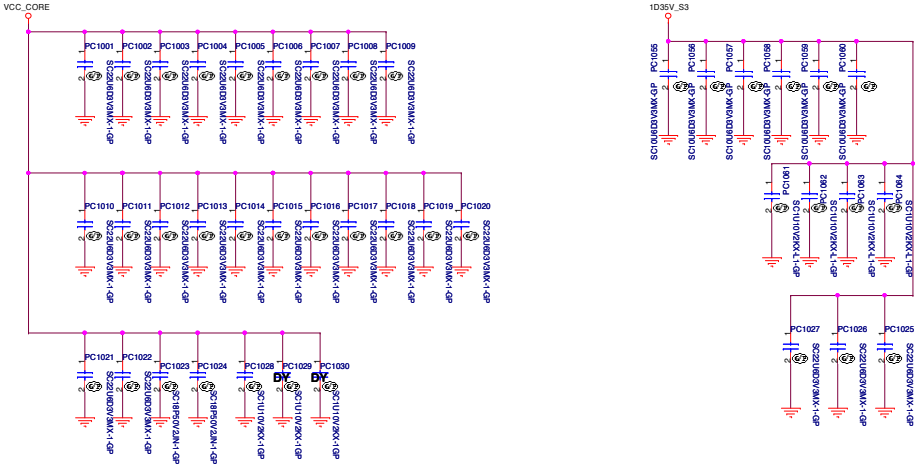
Size: A3 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 9 of 102

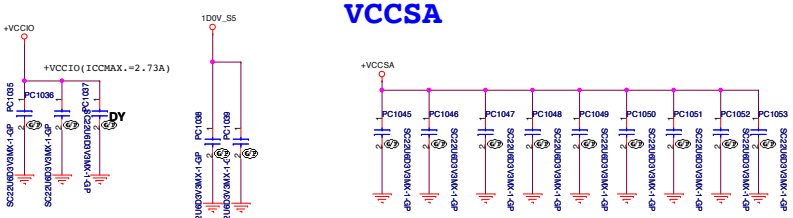
Main Func = CPU

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

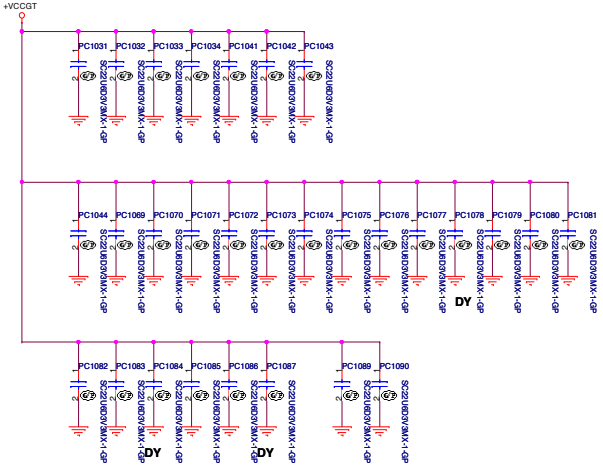


VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A



(#543016 PDG)

Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CPU (Power CAP1)

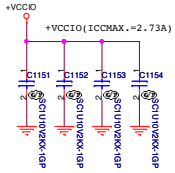
Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 10 of 102

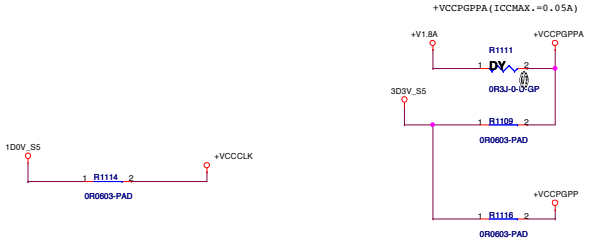
Main Func = CPU

UNSLICED GT

VCCIO



PCH DERIVED RAILS



GTUS

20141114 Alden

+V_VCCGTUS_VR can merge to +VCCGT

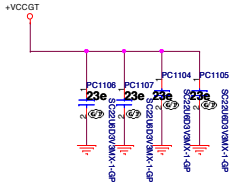
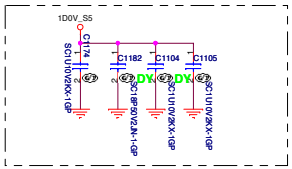
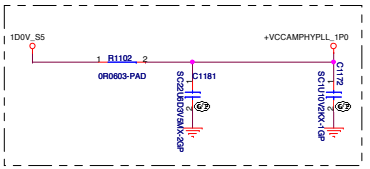
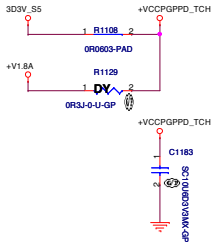


Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		
		(6.3V)[4]	
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible







BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP2)

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 11 of 102

Main Func = DDR SODIMM

(Blanking)

BOM1

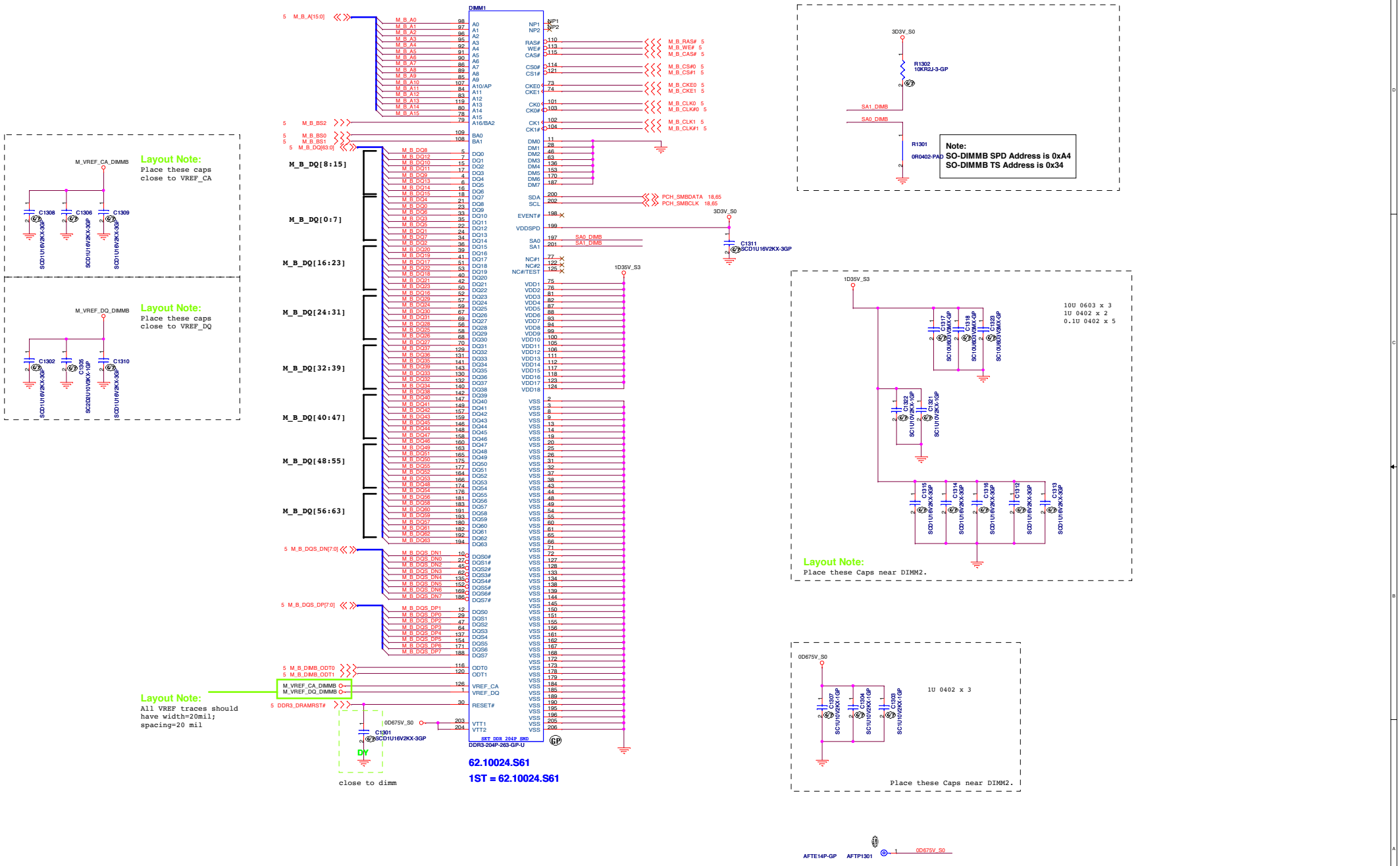
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 12 of 102

Main Func = DDR SODIMM



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 13 of 102

(Blanking)

BOM1

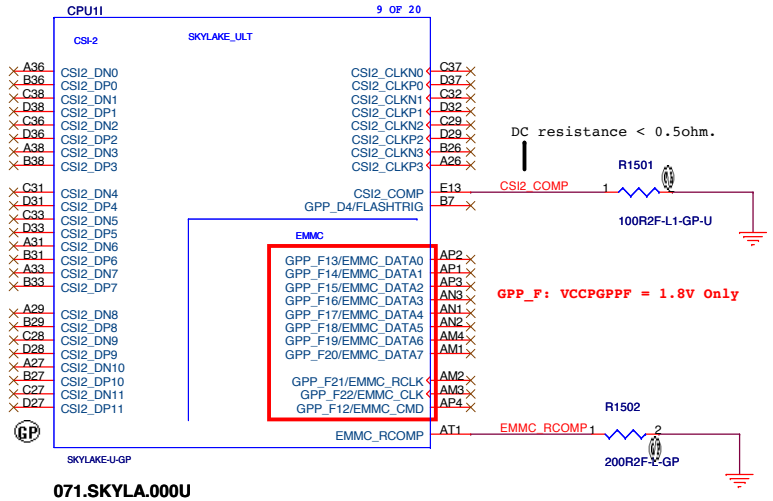
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)SODIMM3_SODIMM4*

Size	Document Number	Rev
A4	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 14 of 102

Main Func = PCH



071.SKYLA.000U

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

BOM1

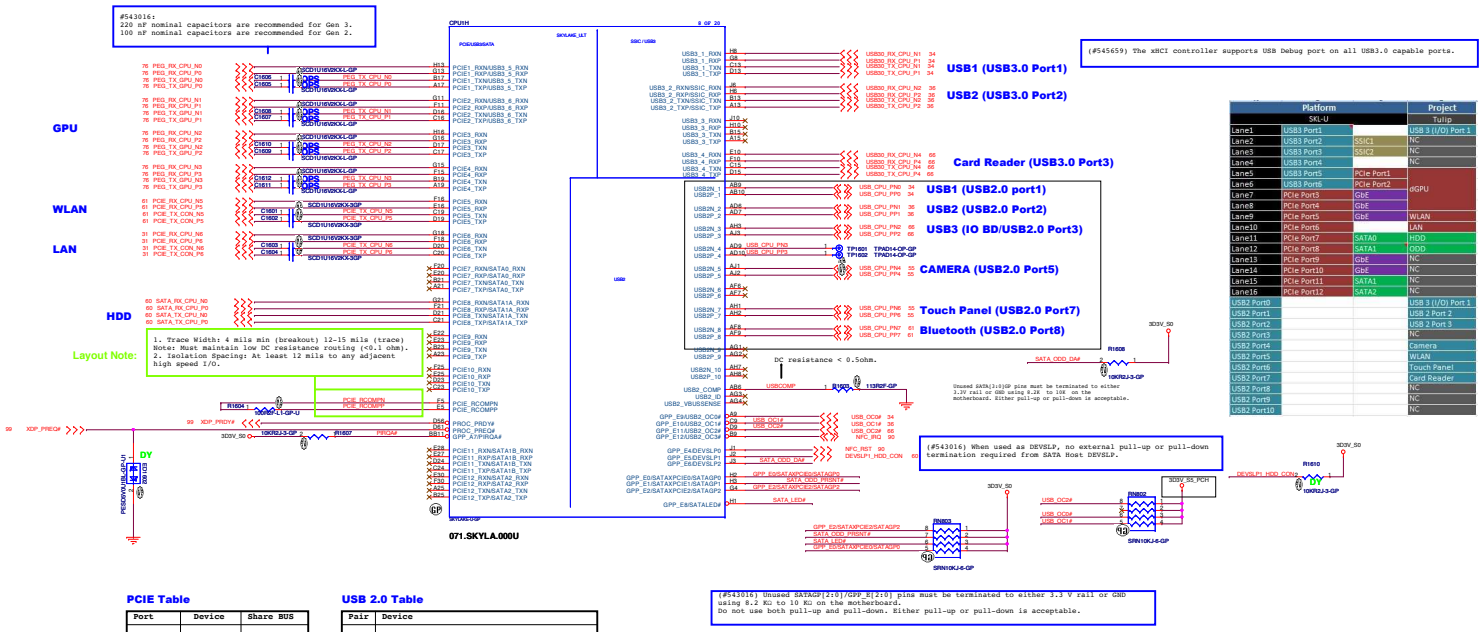
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CS-2/EMMC)

Size: A3 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 15 of 102

Main Func = PCH



Platform SKL-U	Project Tulip
Lane1 USB3 Port1	USB 3 (I/O) Port 1
Lane2 USB3 Port2 SSIC1	NC
Lane3 USB3 Port3 SSIC2	NC
Lane4 USB3 Port4	NC
Lane5 USB3 Port5 PCIe Port1	dGPU
Lane6 USB3 Port6 PCIe Port2	
Lane7 PCIe Port3 GbE	
Lane8 PCIe Port4 GbE	
Lane9 PCIe Port5 GbE	WLAN
Lane10 PCIe Port6	LAN
Lane11 PCIe Port7 SATA0	HDD
Lane12 PCIe Port8 SATA1	ODD
Lane13 PCIe Port9 GbE	NC
Lane14 PCIe Port10 GbE	NC
Lane15 PCIe Port11 SATA1	NC
Lane16 PCIe Port12 SATA2	NC
USB2 Port0	USB 3 (I/O) Port 1
USB2 Port1	USB 2 Port 2
USB2 Port2	USB 2 Port 3
USB2 Port3	NC
USB2 Port4	Camera
USB2 Port5	WLAN
USB2 Port6	Touch Panel
USB2 Port7	Card Reader
USB2 Port8	NC
USB2 Port9	NC
USB2 Port10	NC

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(LO-L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	N/A	SATA1
6(LO-L1)	N/A	

USB 2.0 Table

Pair	Device
0	USB3.0 port1 (Debug Port)
1	USB2.0 Port2
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	Card Reader
6	Touch Panel
7	Bluetooth

(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

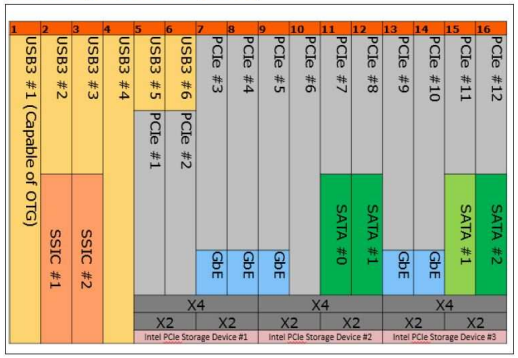


Table 24-2. PCI Express* Port Feature Details

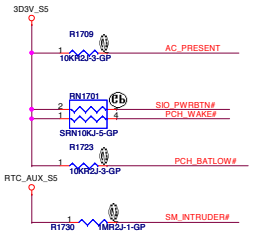
SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

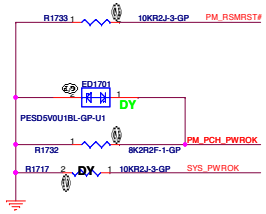
Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

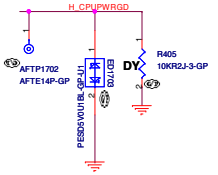
BOM:
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (PCIE/SATA/USB)
Size: A3 | Document Number: Tesla SKL-U | Rev: -1
Date: Tuesday, July 21, 2015 | Sheet 16 of 102

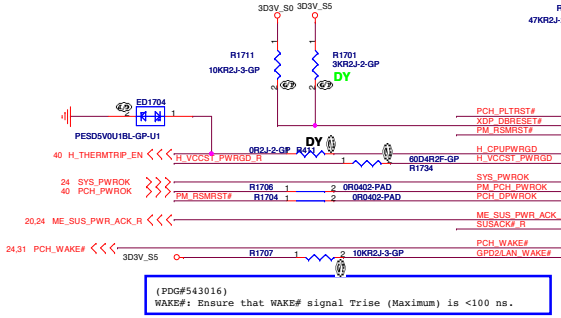
Main Func = PCH



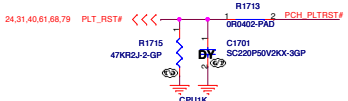


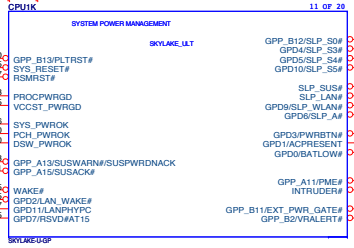
#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.





(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.





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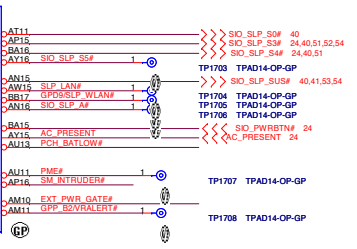
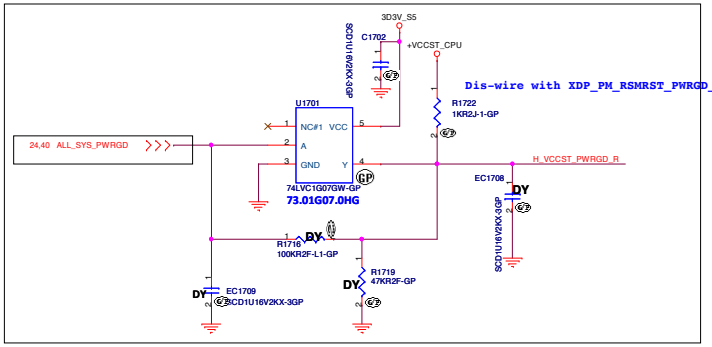


SIO_SLP_S3# AFTP1701 TPAD14-OP-GP

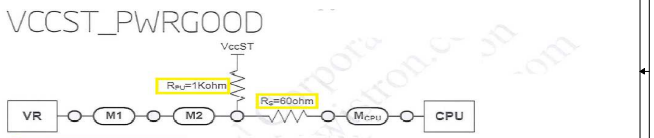
[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

3D3V_S5 R1731 20KR2J-L2-GP EXT_PWR_GATE#

BATLOW#:
Pull-up required even if not implemented.

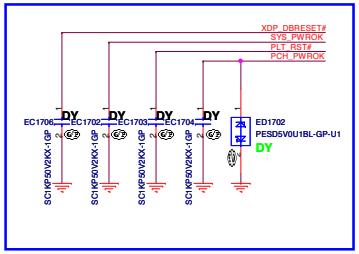


VCCST_PWRGD / HWM201:

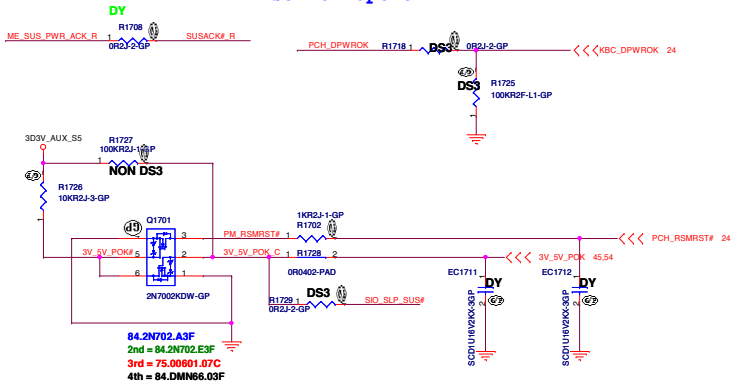


- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST



DS3 BOM Option



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Monday, July 27, 2015 Sheet 17 of 102

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PLACE WITHIN 1.1 INCH OF PCH

(#543016)Optional, can be left as OPEN/No-Connect.

add Circuit for NFC

RCIN#:
Frequency to Avoid: 33 MHz

SERIRQ PH:
PDG: 8.2k
CRB: 10k

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071.SKYLA.000U

82.30001.G11

GPU

WLAN

LAN

Layout: Place at the open door area.

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CL/CLK)

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

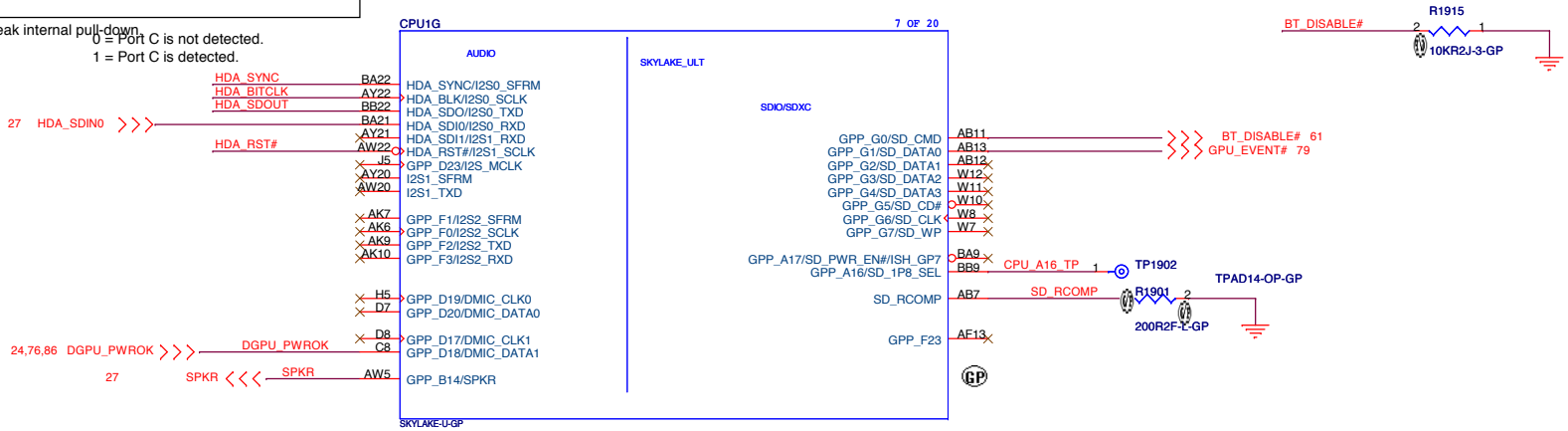
Date: Tuesday, July 21, 2015 | Sheet 18 of 102

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	* 0 = Port C is not detected. 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

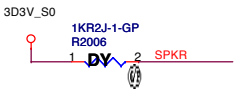
Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

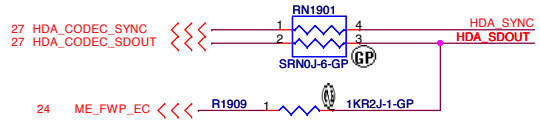
The internal pull-down is disabled after PLTRST# deasserts

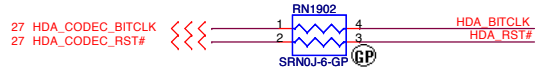
PCH strap pin:

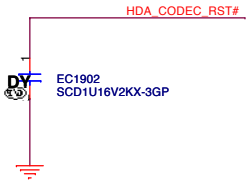
NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts









BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (AUDIO/SDIO/SDXC)

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 19 of 102

Main Func = PCH

PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

TPM/TCM Strap pin	TPM_DETECT_1	TPM_DETECT_2
TPM	0	0
TCM	0	1
Non-TPM&Non-TCM	1	0

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

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BOM1

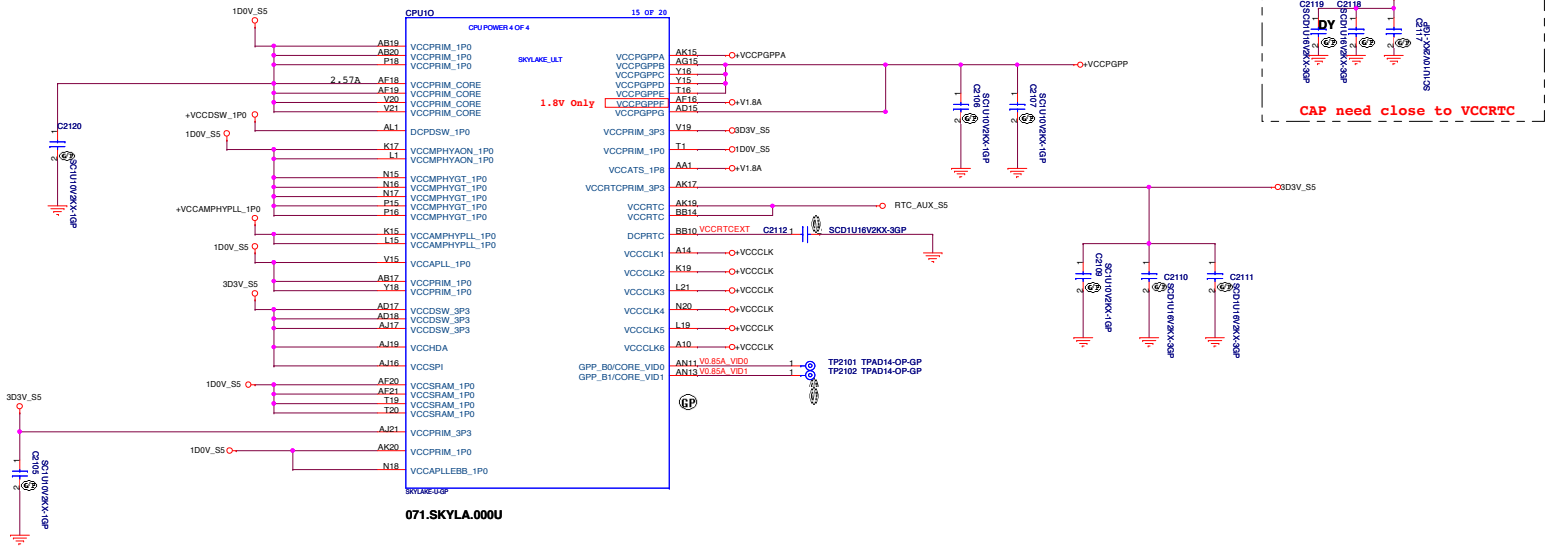
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

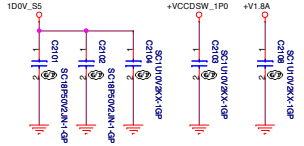
Title: CPU (LPSS/ISH)

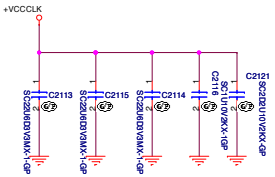
Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 20 of 102

Main Func = PCH







BOM1

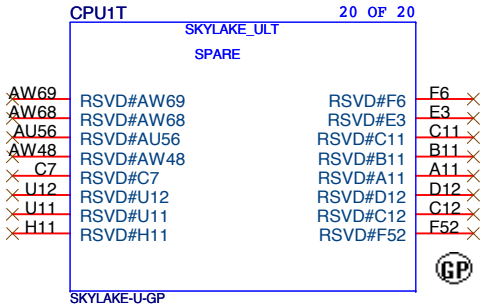
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 21 of 102

Main Func = PCH



071.SKYLA.000U

BOM1

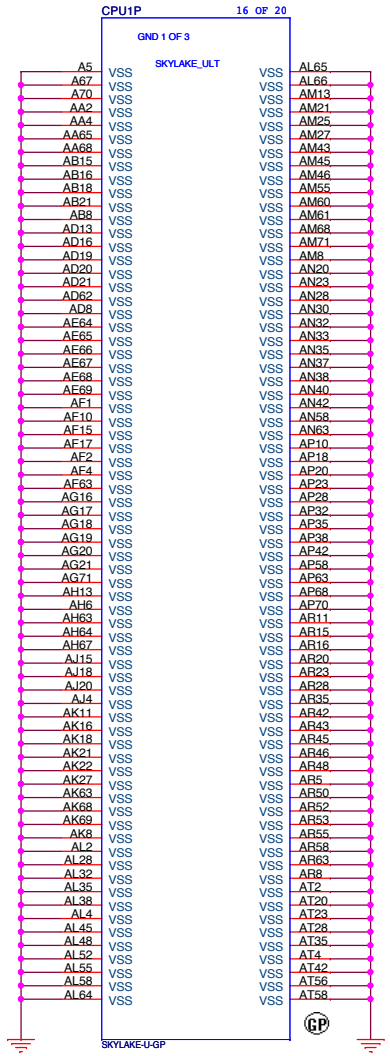
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (RSVD)***

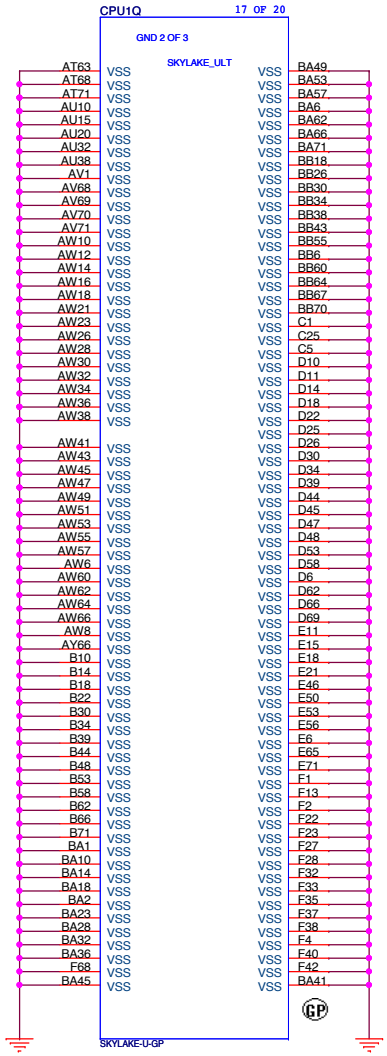
Size	Document Number	Rev
A4	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 22 of 102

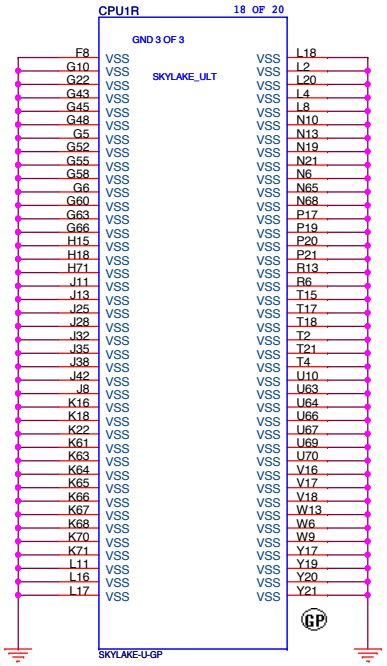
Main Func = PCH



071.SKYLA.000U



071.SKYLA.000U



071.SKYLA.000U

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(VSS)***

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 23 of 102

SSID = KBC

Model_ID_BOM Ctrl

MODEL ID

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LT41 Intel skylake	100.0K	10.0K 64.10025.6DL	3.0V
LT51 Intel skylake	100.0K	20.0K 64.20025.L0L	2.75V
LC41 Intel skylake	100.0K	33.0K 64.33025.L0L	2.48V
LC51 Intel skylake	100.0K	47.0K 64.47025.6DL	2.24V
LC51P Intel skylake	100.0K	64.9K 64.64925.6DL	2.0V
M51	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
SE	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

SPEC: ADT PWR Detection Function V1 3

DELTA Model:ADP65FD BB-PD03 ADP

PIN 3 PIN 1 PIN 2

TABLE

	SIGNAL
PIN 1	287~ohm(1% TOLERANCE)
PIN 3	------
PIN 2	

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.109V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.234V < ID <= 0.663V	45W

SA

Prevent BIOS data loss solution

84.T3906.A11
2nd = 84.T3906.E11

NPCE285G

Thermal VD

BATTERY / CHARGER ---->

PCH / GPU N15S / Gsensor /NCT7718

TP---->

06/24 NOVO Button---->

06/16 MAX R1717 DY

Reserved AOAC

KBC PWR supply at PSL mode.

NOTE: Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils.. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE: Locate resistors R2415 and R2417 close to the U2401.

<---06/26 L741 USB_CHAR_SEL

<---06/26 AD_OFF

<---06/26 AOU_IFLG#

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

6/18 U2403 Change Part Number to 71.00285.0A0G (285P)

071.00285.0A0G

2013/9/12
GPIO83/SOUT_CR & GPIO87/SIN_CR Need reserved TP for Debug

R2472 close to Pin103

NOTE: Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE: PWM Signal : 1. If unused, select alternative GPIO function and enable internal pull-down. 2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

075.00054.0B7D

06/24 add D2401, 將Novo button 與 Power button 接一起,因KBC PSL 只有4Pin ,所以要讓: Pin給AOU_tFLG#

Nuvoton KBC PSL Power Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

84.02130.031
2nd = 084.03413.0031
84.2N702.J31

EC GPIO PH

EC GPIO PL

06/24 R2464 KBC_NOVO_BTN#_Change Net Name to KBC_NOVO_BTN#_EC
06/25 KBC_NOVO_BTN#_EC 接3D3V_AUX_S5, 要改成 3D3V_AUX_KBC

06/05 Delete R2460(DG)

EC_GPIO47 High Active

2nd = 84.2N702.J31

(Debug Card Side)

(Main Board Side)

3.3V_S5

3.3V

KBC

GND

TX

RX

(RX) (reserved)

(RX)

(TX)

(TX) (reserved)

LF15V Note:
(1) R21= DY R2458(ES1_TXD)
(2) R13= DY R2451(ES1_RXD)

Nuvoton KBC PSL Logic

Table 11. PSL Operation States

Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

Micrel P/N:74.02782.072

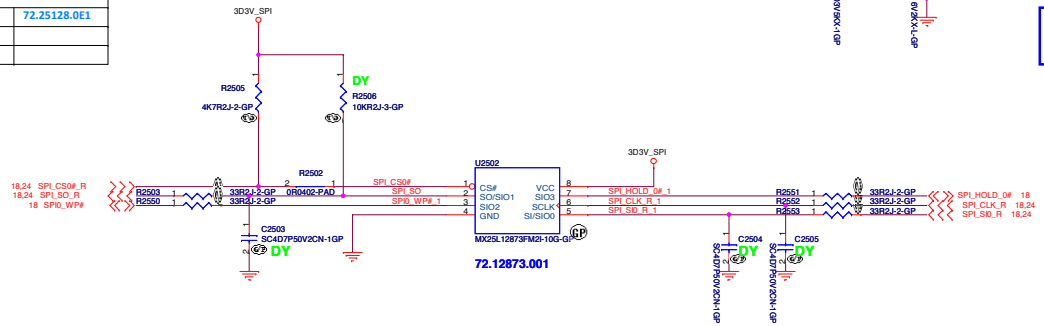
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

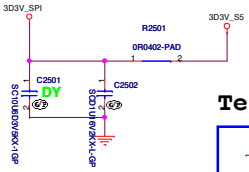
Title: NPCE285
Size: A3 | Document Number: Tesla SKL-U | Rev: -1
Date: Tuesday, July 21, 2015 | Sheet 24 of 102

SSID = Flash.ROM

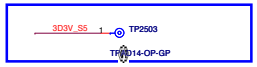
SPI ROM Equal length need to less than 500mil

U2502			
Main	Winbond		72.25128.0E1
SC			
SD			



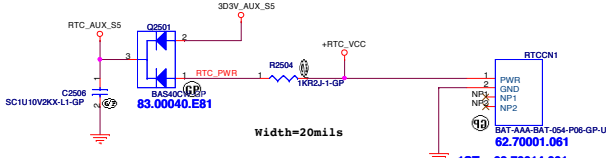


Test point

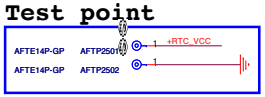


SSID = RBATT

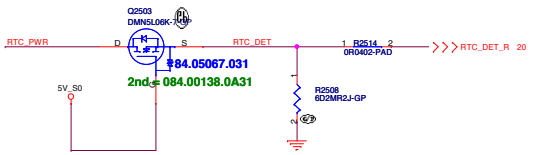
SSID = RBATT



Test point



High Detect
Need to Check whether to PD in PCH Side



BOM1

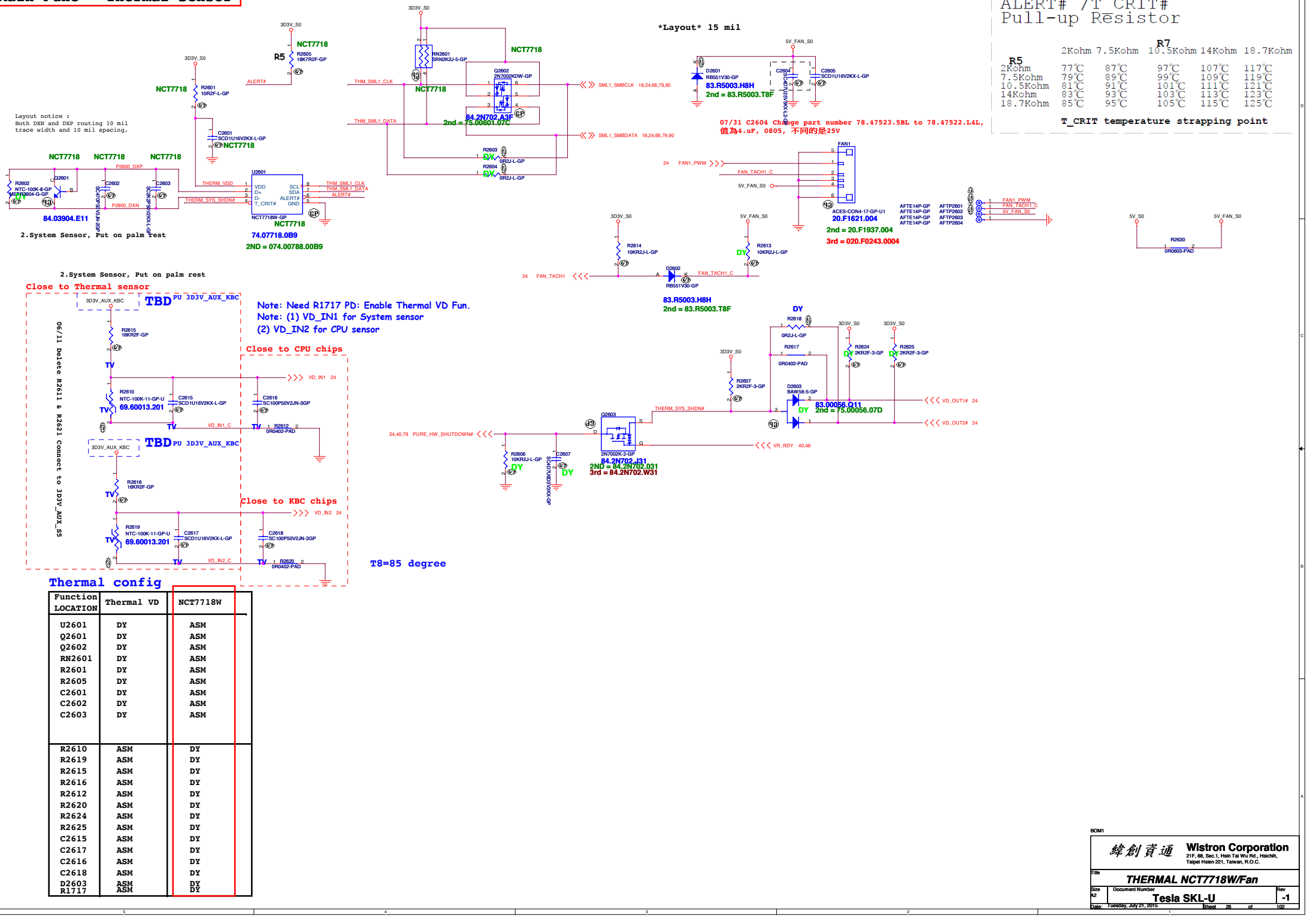
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Flash(KBC+PCH)/RTC*

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 25 of 102

Main Func = Thermal Sensor



ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

Thermal config

Function LOCATION	Thermal VD	NCT7718W
U2601	DY	ASM
Q2601	DY	ASM
Q2602	DY	ASM
RN2601	DY	ASM
R2601	DY	ASM
R2605	DY	ASM
C2601	DY	ASM
C2602	DY	ASM
C2603	DY	ASM
R2610	ASM	DY
R2619	ASM	DY
R2615	ASM	DY
R2616	ASM	DY
R2612	ASM	DY
R2620	ASM	DY
R2624	ASM	DY
R2625	ASM	DY
C2615	ASM	DY
C2617	ASM	DY
C2616	ASM	DY
C2618	ASM	DY
D2603	ASM	DY
R1717	ASM	DY

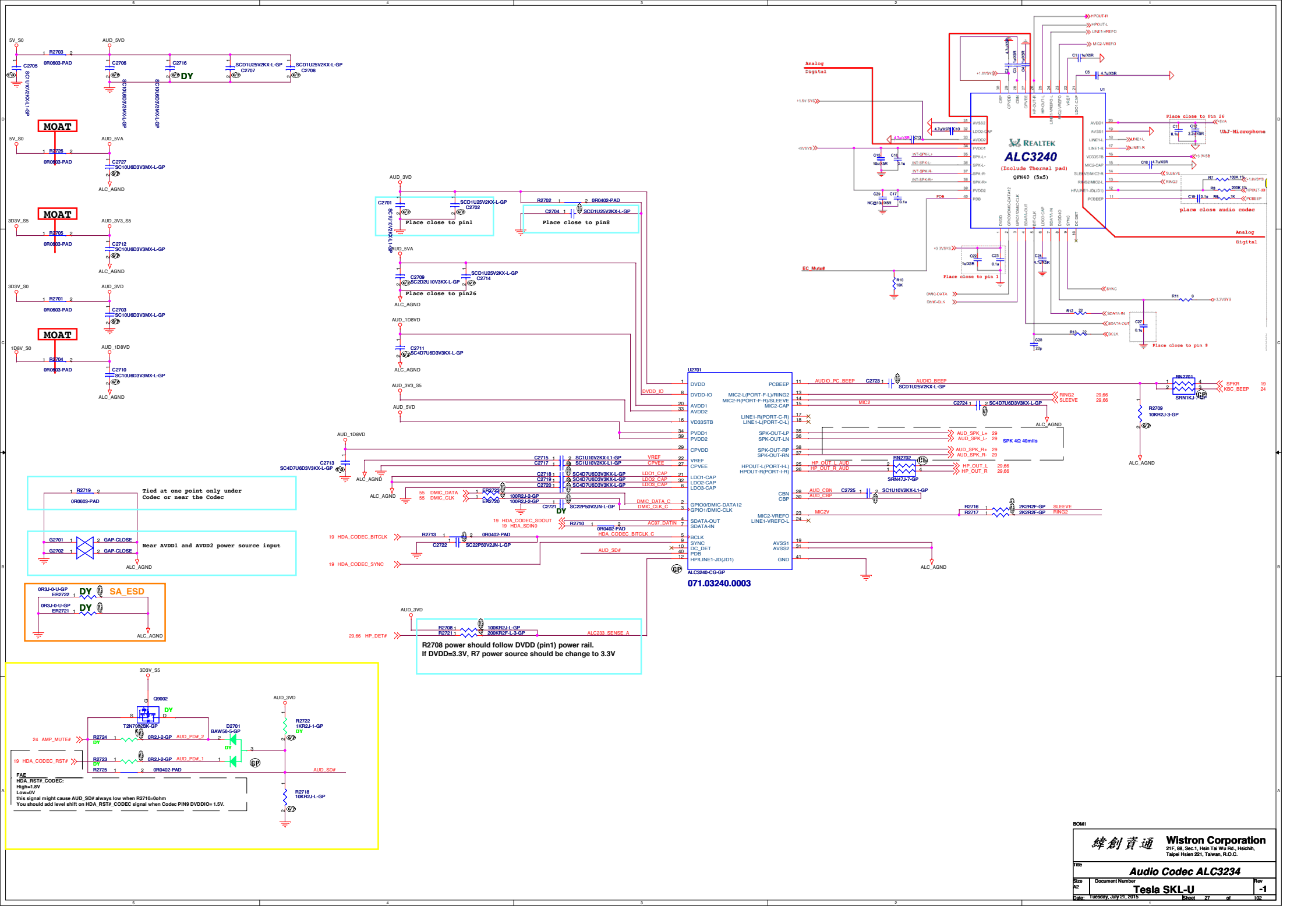
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 26 of 102


MOAT
MOAT
MOAT
MOAT
ALC3240
(Include Thermal pad)
QFN40 (5x5)
REALTEK
071.03240.0003
ALC3240-CG-GP
Wistron Corporation
Audio Codec ALC3234
Tesla SKL-U
Tied at one point only under Codec or near the Codec
Near AVDD1 and AVDD2 power source input
SA_ESD
R2708 power should follow DVDD (pin1) power rail.
If DVDD=3.3V, R7 power source should be change to 3.3V
FAE
HDA_RST#_CODEC:
High=1.8V
Low=0V
this signal might cause AUD_SD# always low when R2710=0ohm
You should add level shift on HDA_RST#_CODEC signal when Codec PIN9 DVDDIO= 1.5V.

BOM#

緯創資通 **Wistron Corporation**
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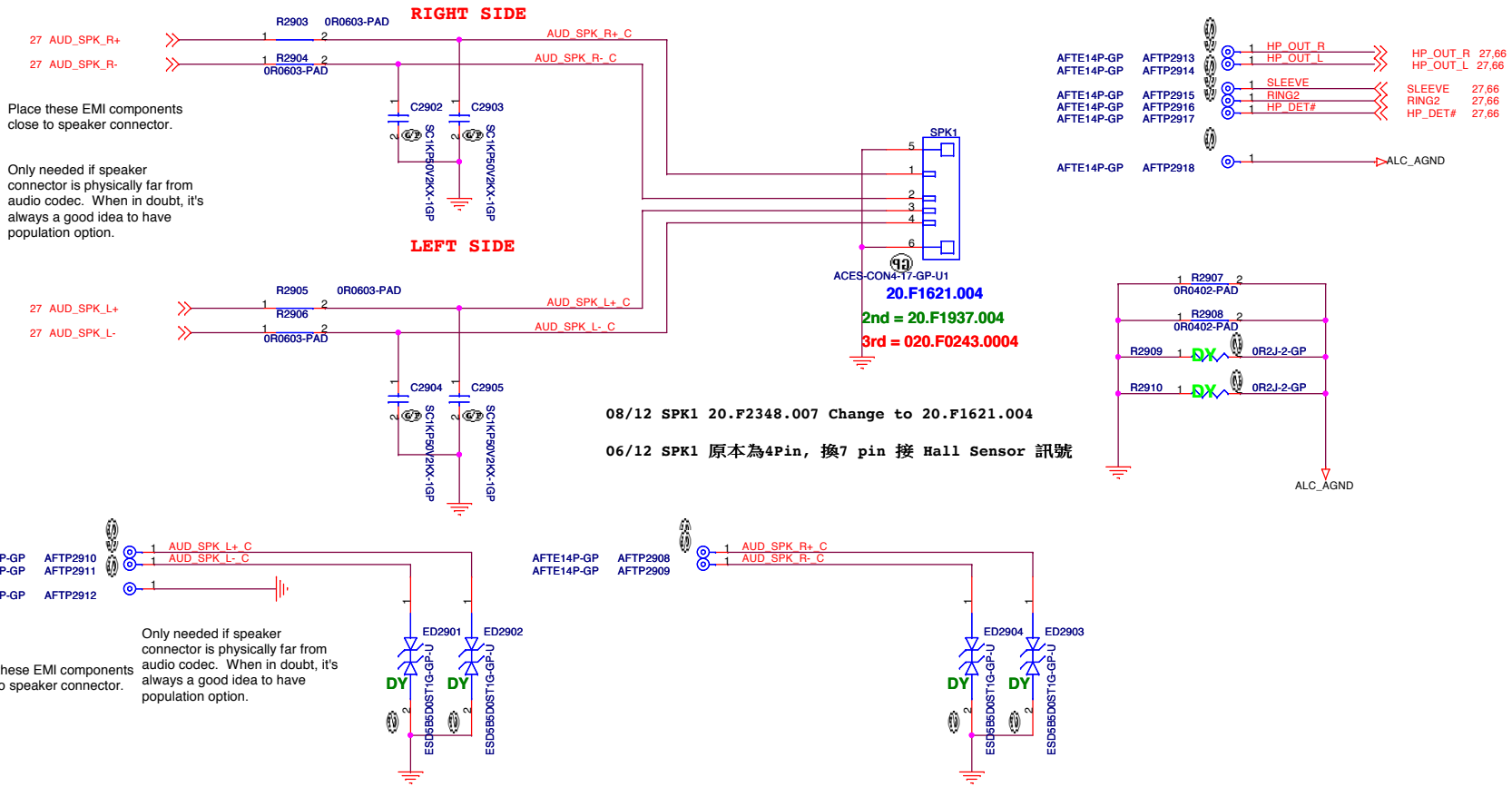
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 28 of 102

INTERNAL STEREO SPEAKERS



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Audio IO**		
Size: A3	Document Number: **Tesla SKL-U**	Rev: **-1**
Date: Tuesday, July 21, 2015	Sheet 29 of 102	

Main Func = Audio

(Blanking)

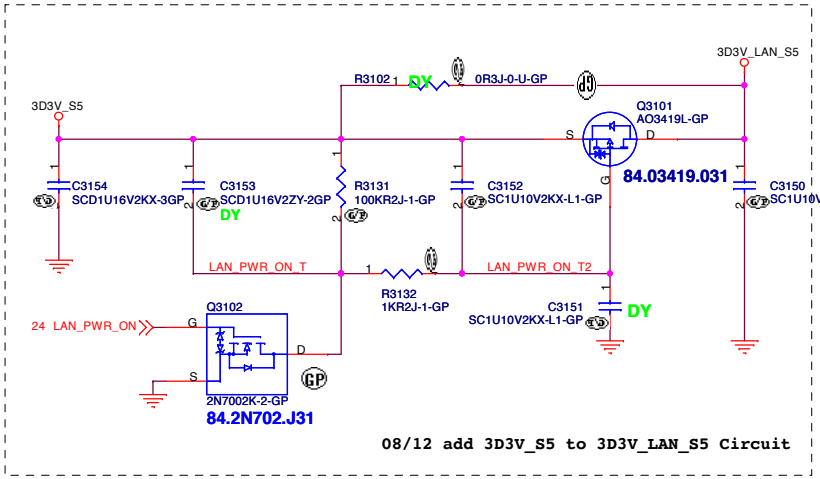
BOM1

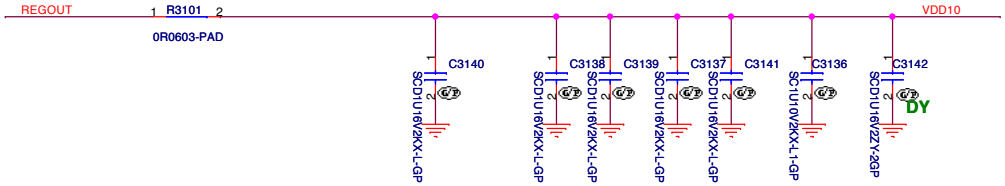
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	Tesla SKL-U	-1

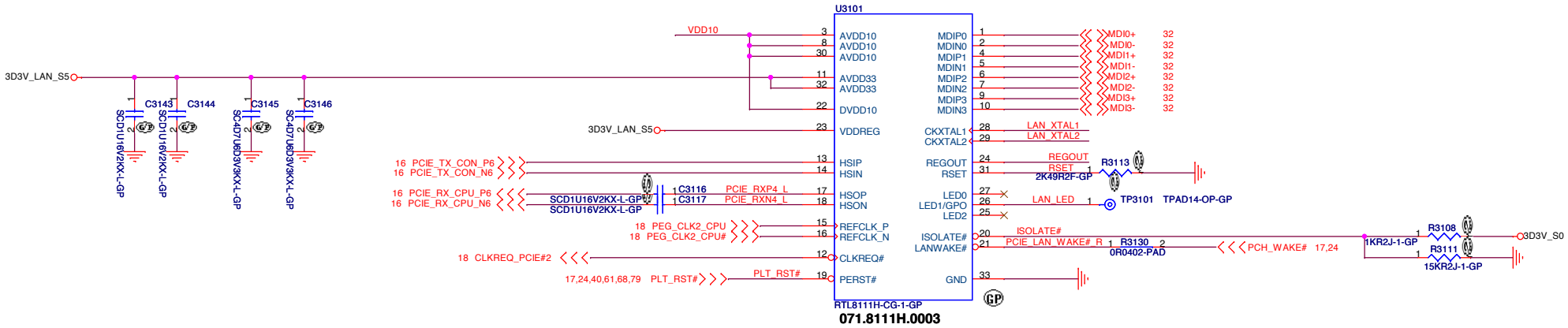
Date: Tuesday, July 21, 2015 Sheet 30 of 102



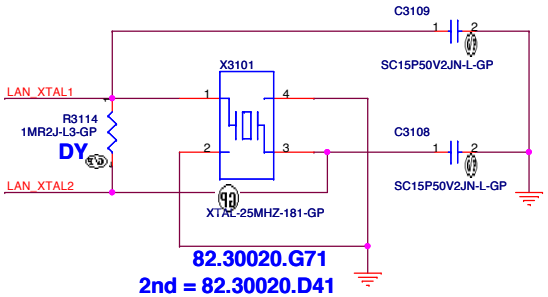


For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C3138 to C3141 close to each VDD10 pin-- 3, 8, 22, 30

For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C20 and C21 close to each VDD10 pin-- 22 (Reserved)



25MHz XTAL



Crystal 27MHz			
MAIN	HASONIC	82.30020.G71	78.15034.L1L
2ND	HARMONY	82.30020.D41	78.18034.1FL

Change LAN PN to SC50H01259

LAN and Transformer Config:

LAN/Transformer	
RTL8111GUL 1000M 20200540	
1000M Transformer 068.IH219.3001	Main source
1000M Transformer 68.89246.301	2nd source

BOM1

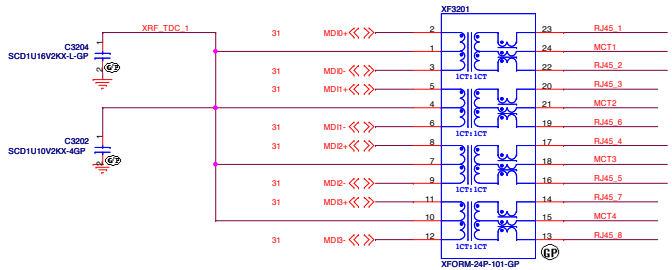
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN_RTL8111

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Wednesday, August 19, 2015 Sheet 31 of 102

10/100M/1000M Lan Transformer



068.IH219.3001

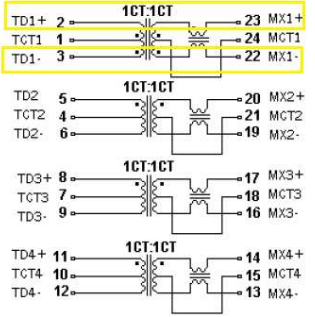
2nd = 68.89240.30D

1000M Lan Transformer pin define

Part Number	Insertion Loss (dB Max) 1-100MHz	Return lo (dB MIN @1 1-30	40	50	60
IH-106-A	-1.0	-18	-14.4	-13.1	

SCHEMATICS :

Pin Define

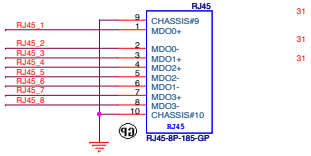


LAN and Transformer Config:

LAN/Transformer	
RTL8111GUL 1000M 20200540	
1000M Transformer 068.IH219.3001	Main source
1000M Transformer 68.89246.301	2nd source

1000M Transformer PN:
068.01010.3001 (AZ chip

LAN Connector



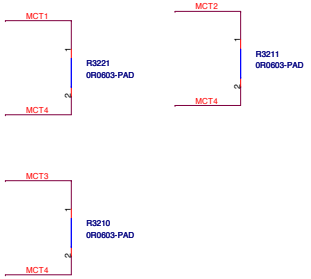
022.10001.00A1

2nd = 022.10001.0E71

08/13 RJ45 22.10019.141 Change to 022.10001.00A1

10/100/1000 LAN surge circuit

For test stuff



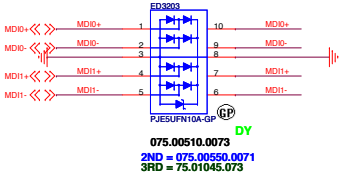
069.A0002.0001

1ST = 069.A0002.0001

2ND = 069.A0007.0001

3rd = 069.A0007.0011

10/6 Change ED3202 1st & 3rd source

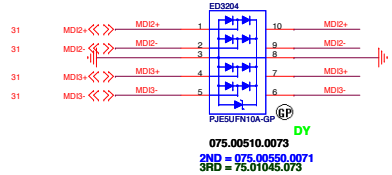


075.00510.0073

DY

2ND = 075.00550.0071

3RD = 75.01045.073



075.00510.0073

DY

2ND = 075.00550.0071

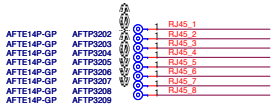
3RD = 75.01045.073

8/25 將ED3203,ED3204 屬性ESD STUFF OPTION 改成DY, 上件會無法Wake on Lan

10/13 ED3203,ED3204 改成跟ED3501一樣, 增加三個Source

10/23 將3rd Source拿掉 75.09904.07C, 因為已有案子50米網線測不過(Part number跟ED3501一樣,BOM別帶錯)

10/23 ED3203, ED3204 ESD STUFF OPTION改 DY,不上件



06/13 Delete LAN_AGND

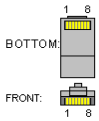
AZ&NON AZ

Function LOCATION	AZ	NON AZ
ED3102	DY	ASM
R3114	DY	ASM
ED3103	ASM	DY
ED3104	ASM	DY
ED3105	ASM	DY
ED3106	ASM	DY
ED3107	ASM	DY
ED3108	ASM	DY
R3112	ASM	DY
R3115	ASM	DY
R3116	ASM	DY
R3117	ASM	DY
R3118	ASM	DY
R3119	ASM	DY
R3120	ASM	DY

RJ45 Pin define

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BI_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BI_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BI_DB+
4	Not connected or BiDirectional	n/c	n/c	BI_DC+
5	Not connected or BiDirectional	n/c	n/c	BI_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BI_DB-
7	Not connected or BiDirectional	n/c	n/c	BI_DD+
8	Not connected or BiDirectional	n/c	n/c	BI_DD-

The connector is 8 pin RJ45 (8P8C) male



The associated connector is 8 pin RJ45 (8P8C) female

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45&Transformer

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Wednesday, August 19, 2015 | Sheet 32 of 102

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

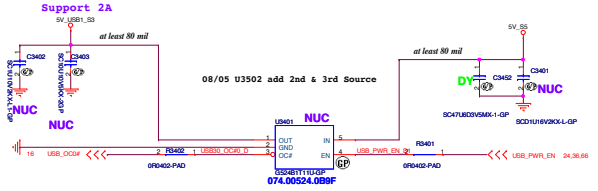
Size	Document Number	Rev
A2	**Tesla SKL-U**	-1

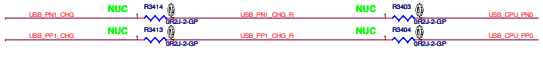
Date: Tuesday, July 21, 2015 Sheet 33 of 102

UC, UC_ST, DY_UC_TI不上件

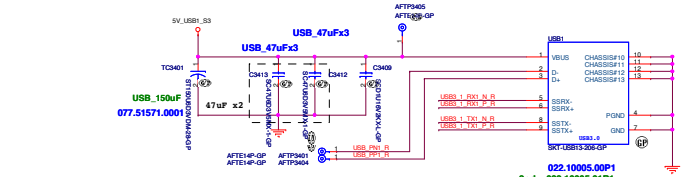
USB3.0 Port1

Support 2A



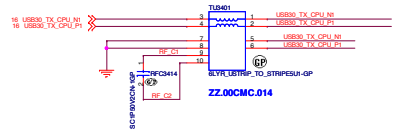


06/12 NUC 有USB Charger 時,不上件

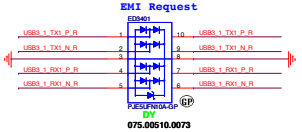


10/23 USB1 改接GND(原本USB3_AGND)

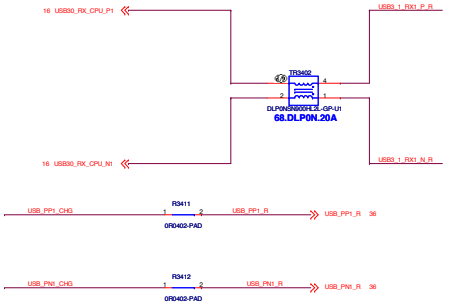
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



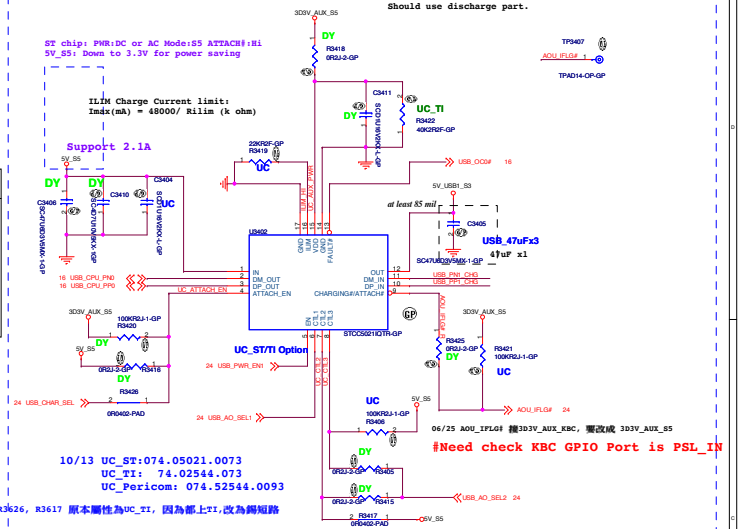
EMI Request



EMI Request



USB charger



STCC5021 Truth Table

Table 5. Truth table control pins CTLx

Host state	CTL1	CTL2	CTL3	Mode description
S0, S1	1	1	1	CDP BC1.2 with charging detection.
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto-mode for full-speed or high-speed USB devices or after a USB device detached
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection

Table 6. Attach detector truth table

ATTACH_EN	EN	Attach detector
0	x	OFF
1	1	OFF
1	0	ON

Table 3 can be used as an *aid* to program the TPS2544 per system states however not restricted to below settings only.

Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2544 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., HsiChih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Charger
Size: Custom | Document Number: Tesla SKL-U | Rev: -1
Date: Tuesday, July 21, 2015 | Sheet 34 of 102

BOM1

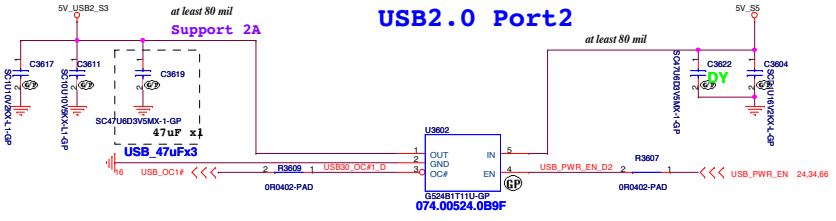
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	**Tesla SKL-U**	-1

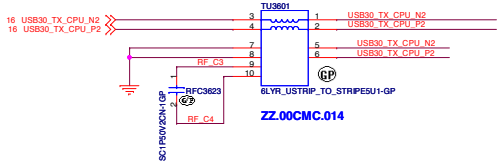
Date: Tuesday, July 21, 2015 Sheet 35 of 102

USB2.0 Port2

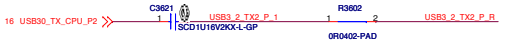


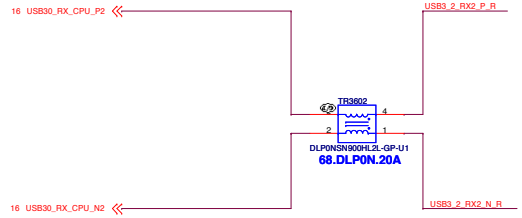
074.00524.0B9F

2ND = 74.06288.07F

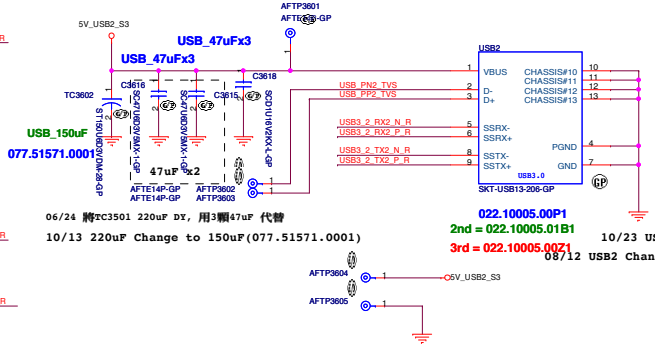


ZZ.00CMC.014





WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR



06/24 將TC3501 220uF DY, 用3顆47uF 代替

10/13 220uF Change to 150uF(077.51571.0001)

022.10005.00P1

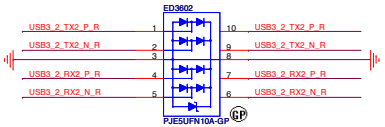
2nd = 022.10005.01B1

3rd = 022.10005.0071

10/23 USB2 改接GND(原本USB3_AGND)

08/12 USB2 Change to 022.10005.00P1

EMI Request



075.00510.0073

2ND = 075.00550.0071

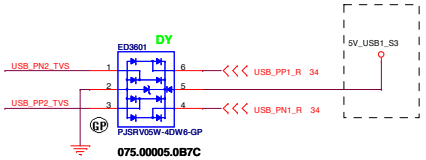
3RD = 75.01045.073

DY

08/18 ED3501 USB_PP2 Change to USB_PP2_TVS
USB_PN2 Change to USB_PN2_TVS
USB_PP1_CHG Change to USB_PP1_R
USB_PN1_CHG Change to USB_PN1_R

08/19 ED3501 USB_PN1_R 與 USB_PP1_R SWAP
USB_PP2_TVS 與 USB_PN2_TVS SWAP

06/25 ED3501 VDD change Net Name to 5V_USB1_S3



075.00005.0B7C

2ND = 075.01256.007C

3RD = 075.09904.0A7C

6/17 ED3501 Change Part Number to 75.09904.07C
與 ED3602 合併,共用一顆ESD

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 36 of 102

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 37 of 102

Main Func = USB3.0 Port1

(Blanking)

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 38 of 102

Main Func = USB3.0 Port1

(Blanking)

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

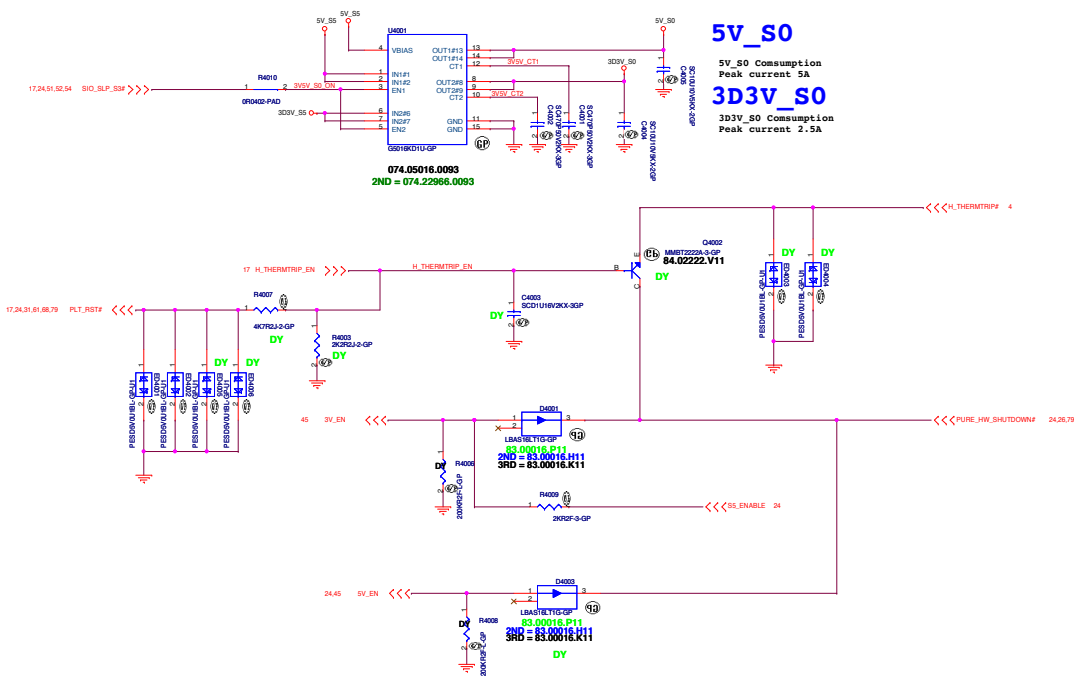
Title: *Reserved*

Size	Document Number	Rev
A4	Tesla SKL-U	-1

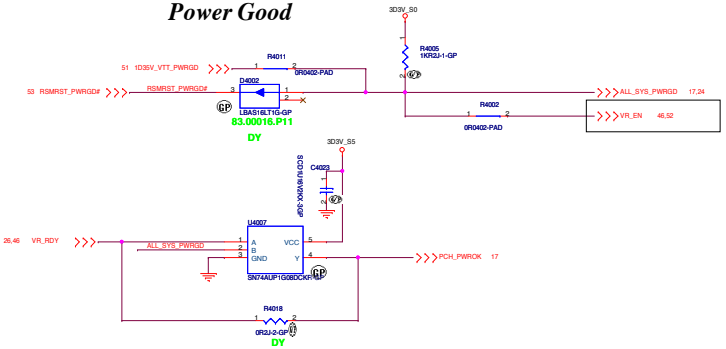
Date: Tuesday, July 21, 2015 Sheet 39 of 102

Main Func = Power Plane & Sequence

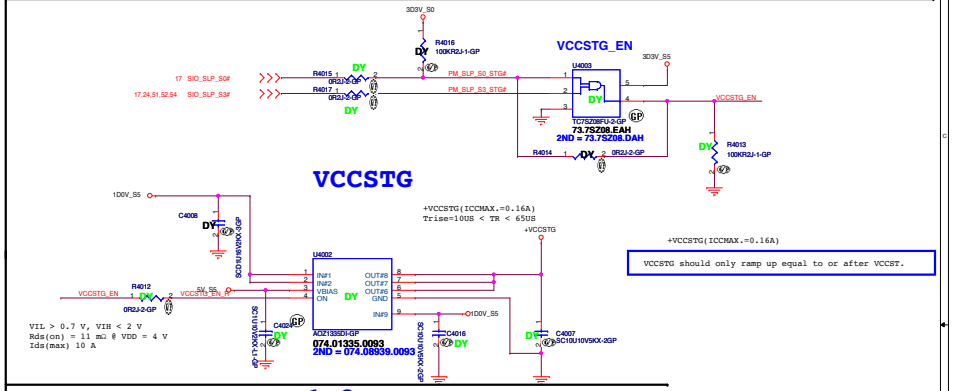
ROSA Run Power



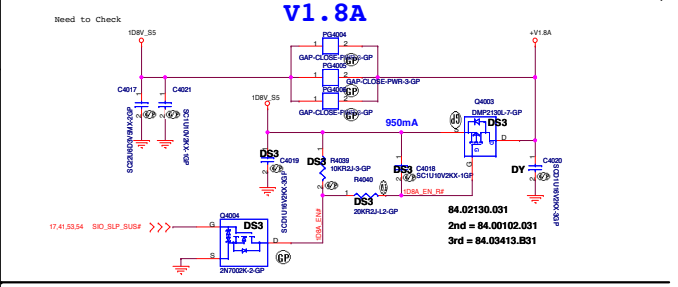
Power Good



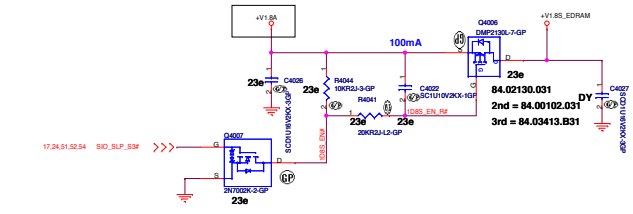
VCCSTG



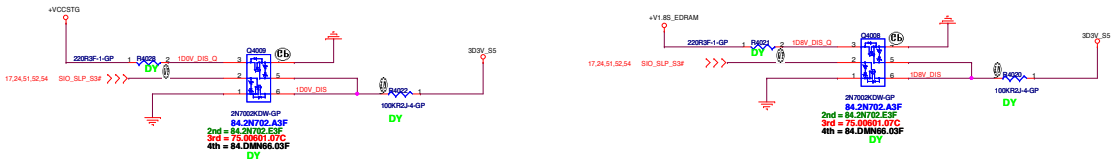
V1.8A



V1.8S



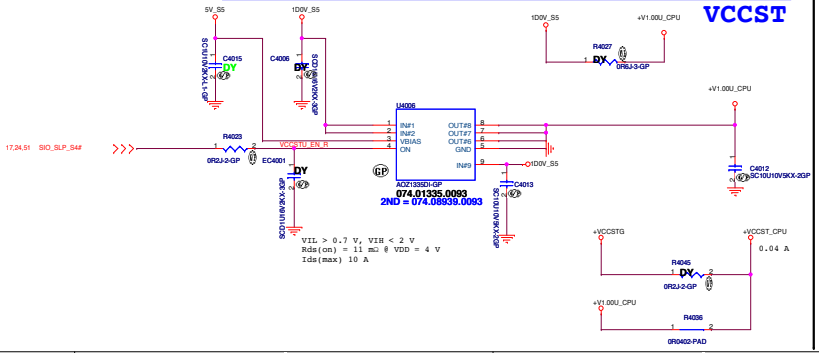
Discharge circuit



MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST



BOM1

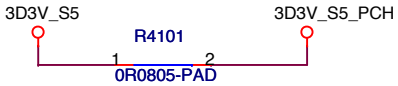
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

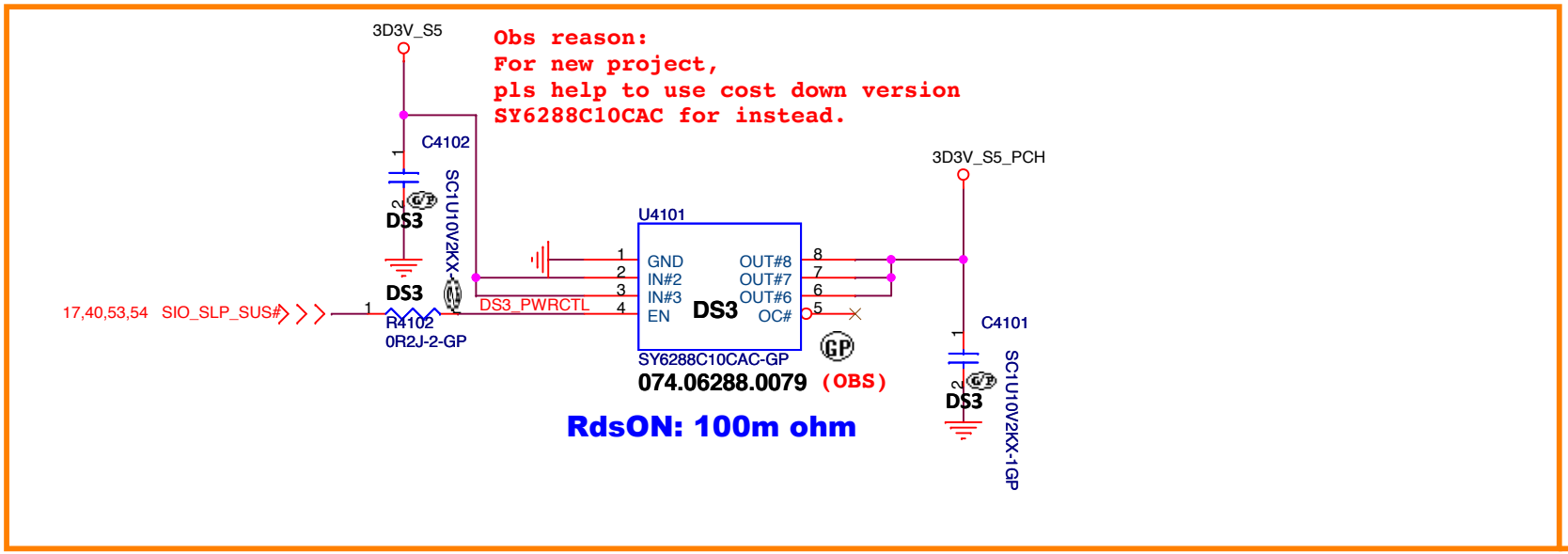
Title: Power Plane EN Sequence

Size: Custom | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 40 of 102

Main Func = Power Plane & Sequence





DS3

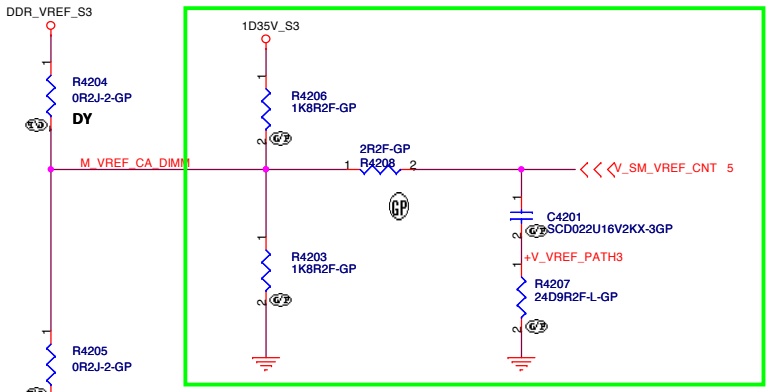
BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Connected_Standby(1/2)+DS3*		
Size: A4	Document Number: Tesla SKL-U	Rev: -1
Date: Tuesday, July 21, 2015	Sheet 41 of 102	

Main Func = DIMM1
Main Func = DIMM2

VREF CIRCUITRY

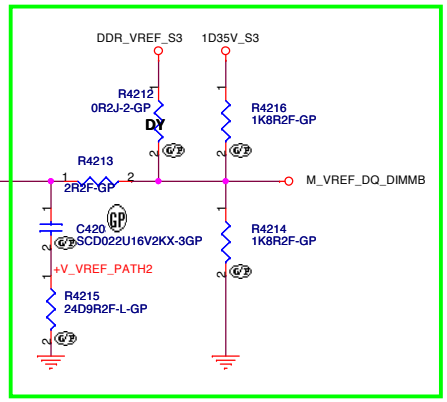
Layout Note:
Place Close DIMMs



SA_DIMM_VREFDQ

DIMM1 M_VREF_CA_DIMMB

Layout Note:
Place Close DIMM1

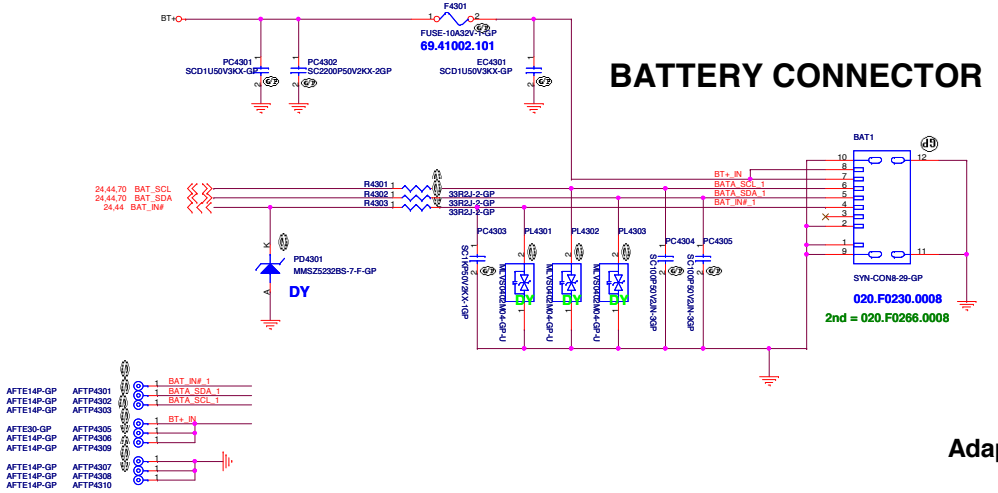


BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Connected_Standby(2/2)	
Size A3	Document Number Tesla SKL-U	Rev -1
Date: Tuesday, July 21, 2015	Sheet 42 of 102	

BATTERY CONNECTOR



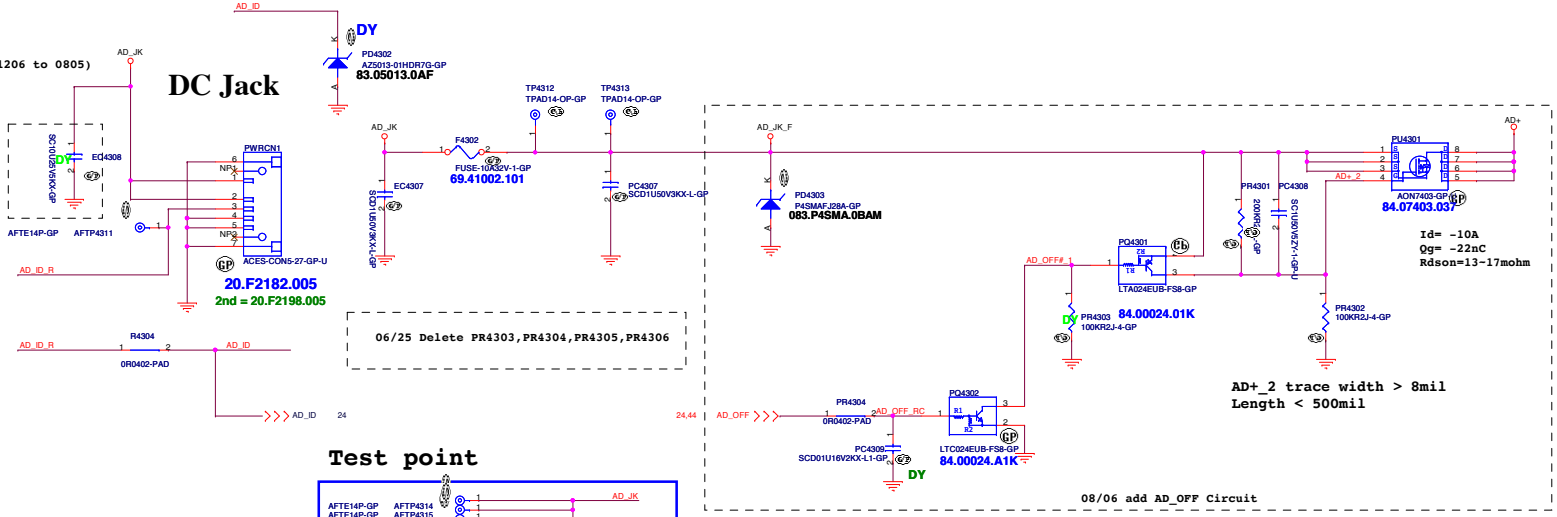
Connector Pin Alignment(Vendor：Suyin,Aces)

Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

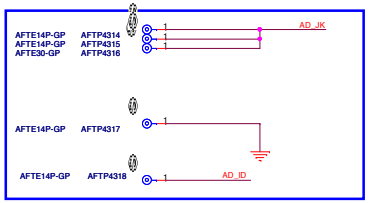
It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

Adaptor in to generate DCBATOUT

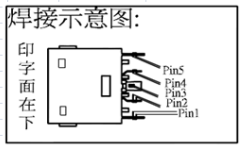
08/01 EC4308 Change part number 78.10622.L5L to 78.10622.51L(1206 to 0805)



Test point



MB_Side		Cable
		Max_Current
Pin 1	AD_JK_F	UL10064AWG28# (3A)
Pin 2	AD_JK_F	UL10064AWG28# (3A)
Pin 3	AD_ID	UL10064AWG28# (3A)
Pin 4	GND	UL10064AWG26# (3.8A)
Pin 5	GND	UL10064AWG26# (3.8A)



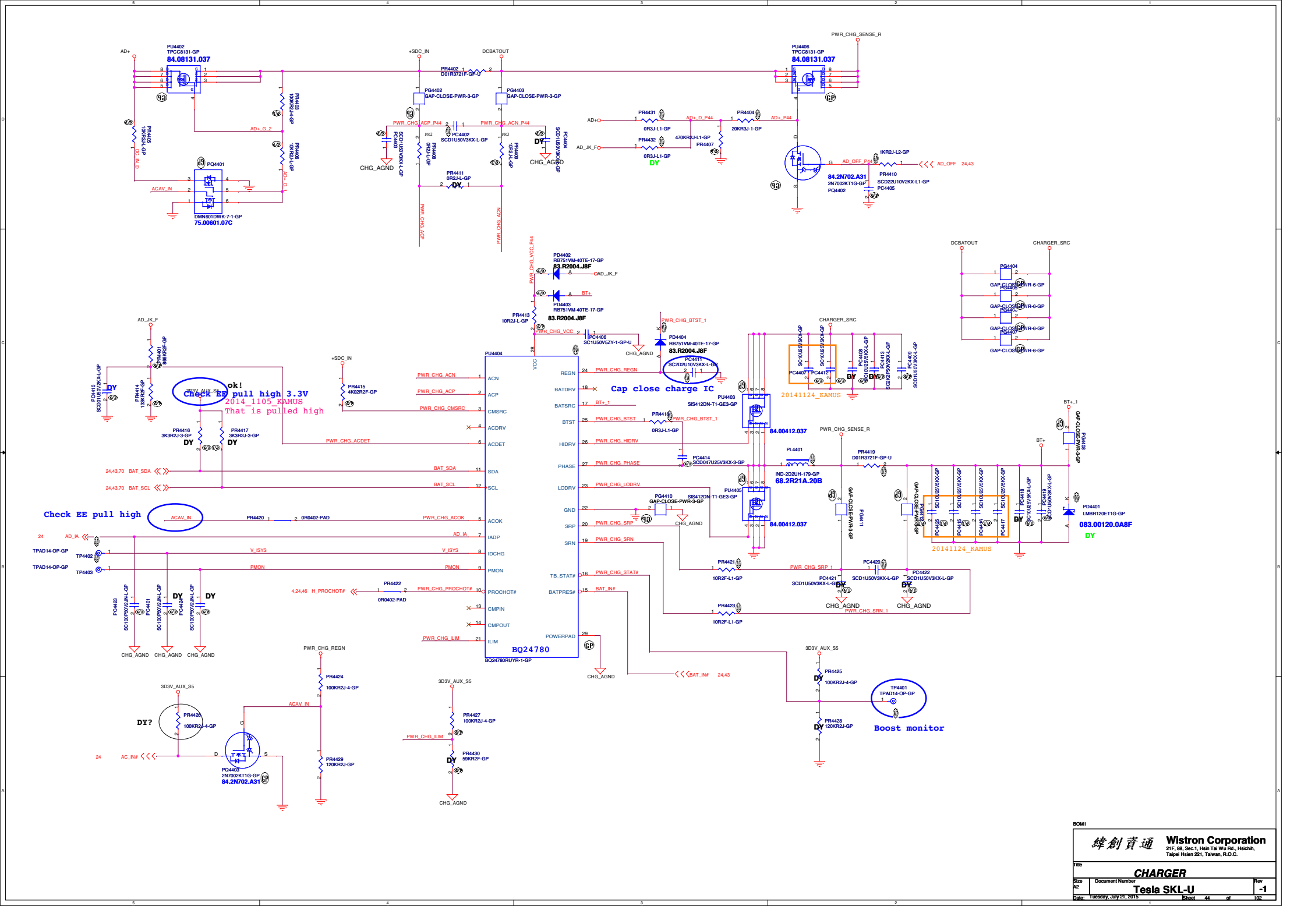
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN & BATT Com

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 43 of 102

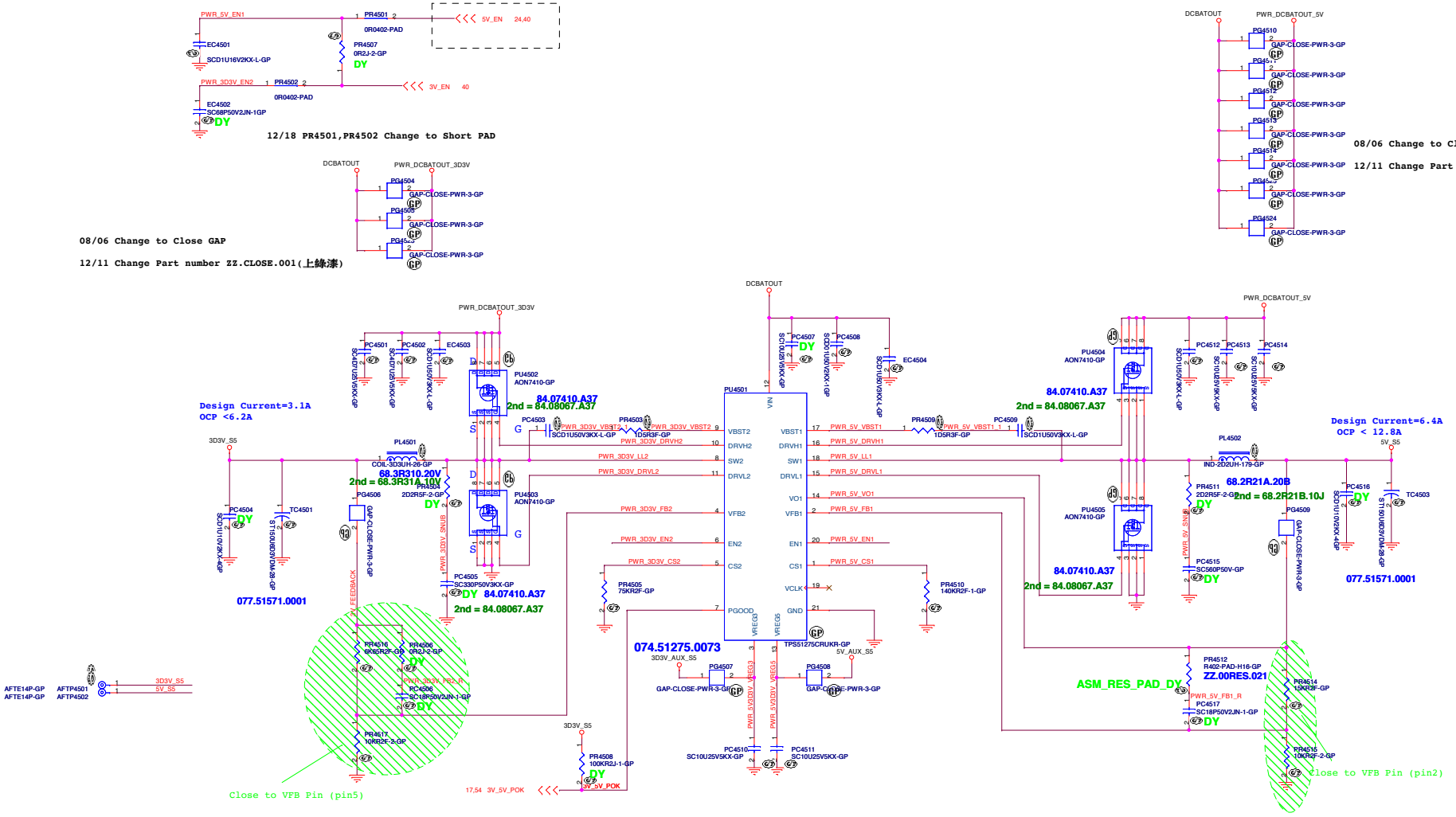

Check EE pull high 3.3v
2014_1105_KAMUS
That is pulled high
ok!
Check EE pull high
Cap close charge IC
Boost monitor
BQ24780
BQ24780RUYR-1-GP
CHARGER
Wistron Corporation
Tesla SKL-U
-1
Tuesday, July 21, 2015

08/20 add 5V_EN

12/18 PR4501,PR4502 Change to Short PAD

08/06 Change to Close GAP

12/11 Change Part number ZZ.CLOSE.001(上綠潔)



06/16 PU4501 Change Part Number from TPS51275 to RT6575B (074.06575.0043).
06/17 PU4501 Change Part Number from RT6575B to TPS51275 (074.51275.0073)

BOM1

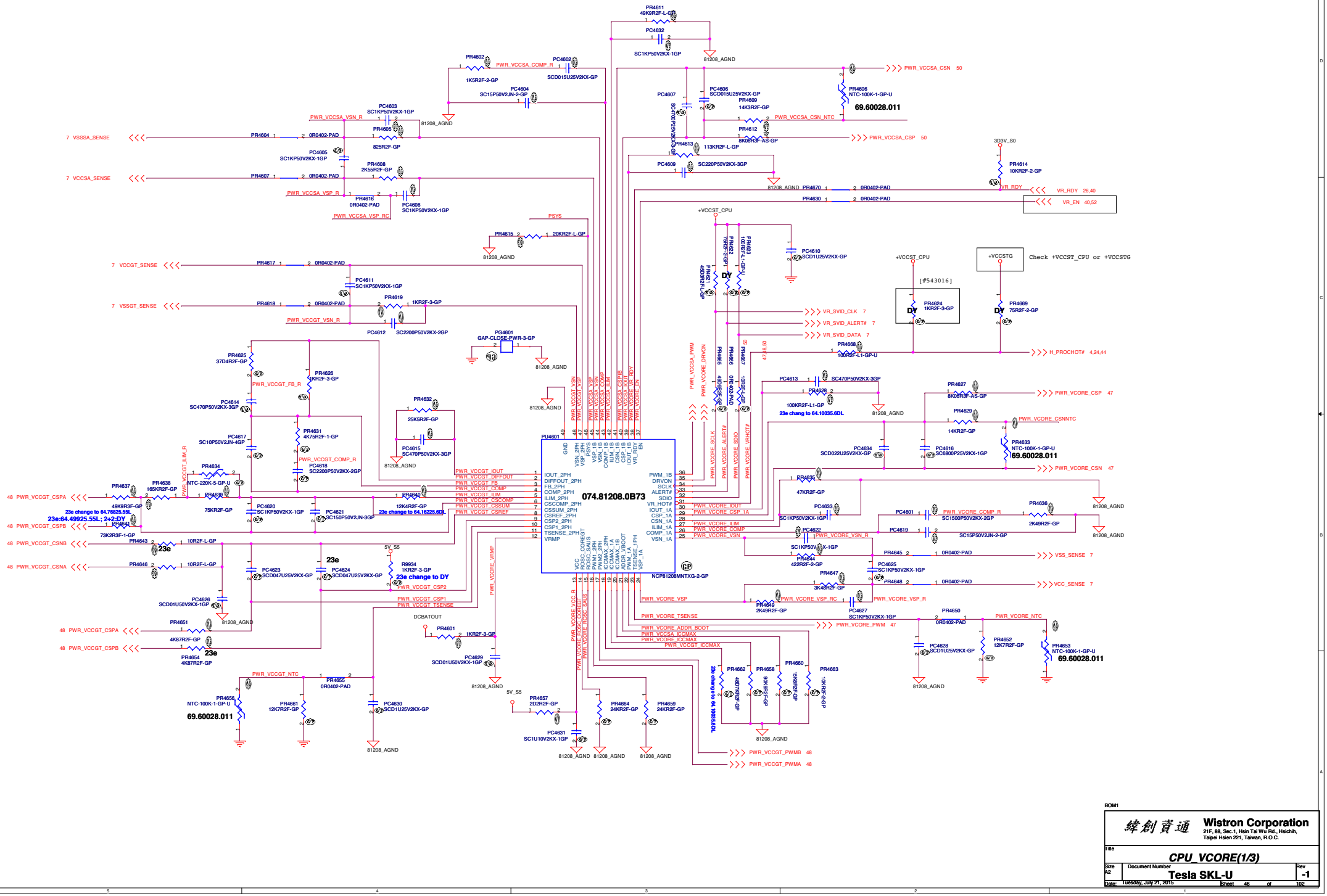
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SYN256 5V/3D3V

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 45 of 102

Main Func = CPU_CORE



BOM1

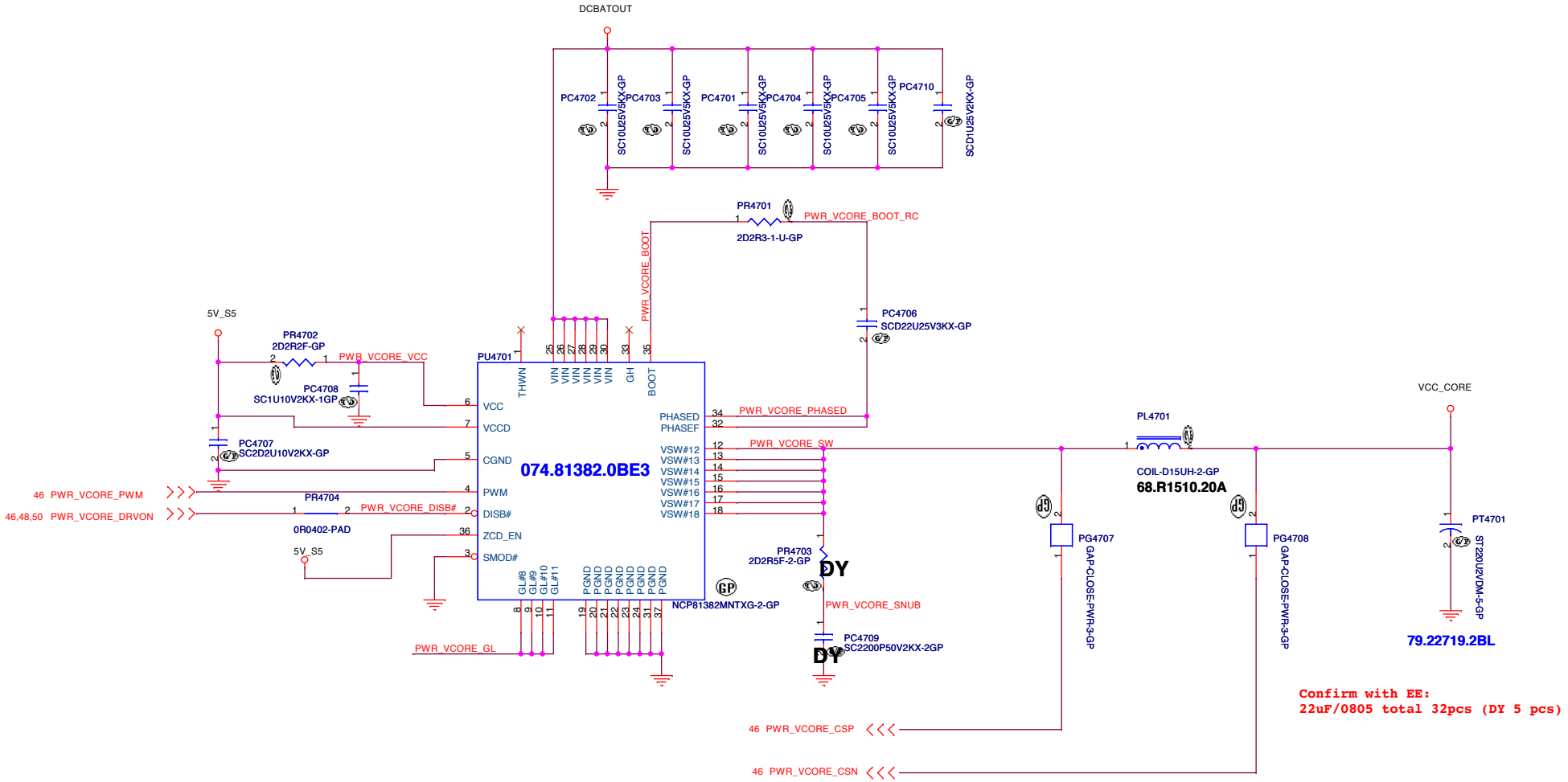
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCORE(1/3)

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 46 of 102

Main Func = CPU_CORE



BOM1

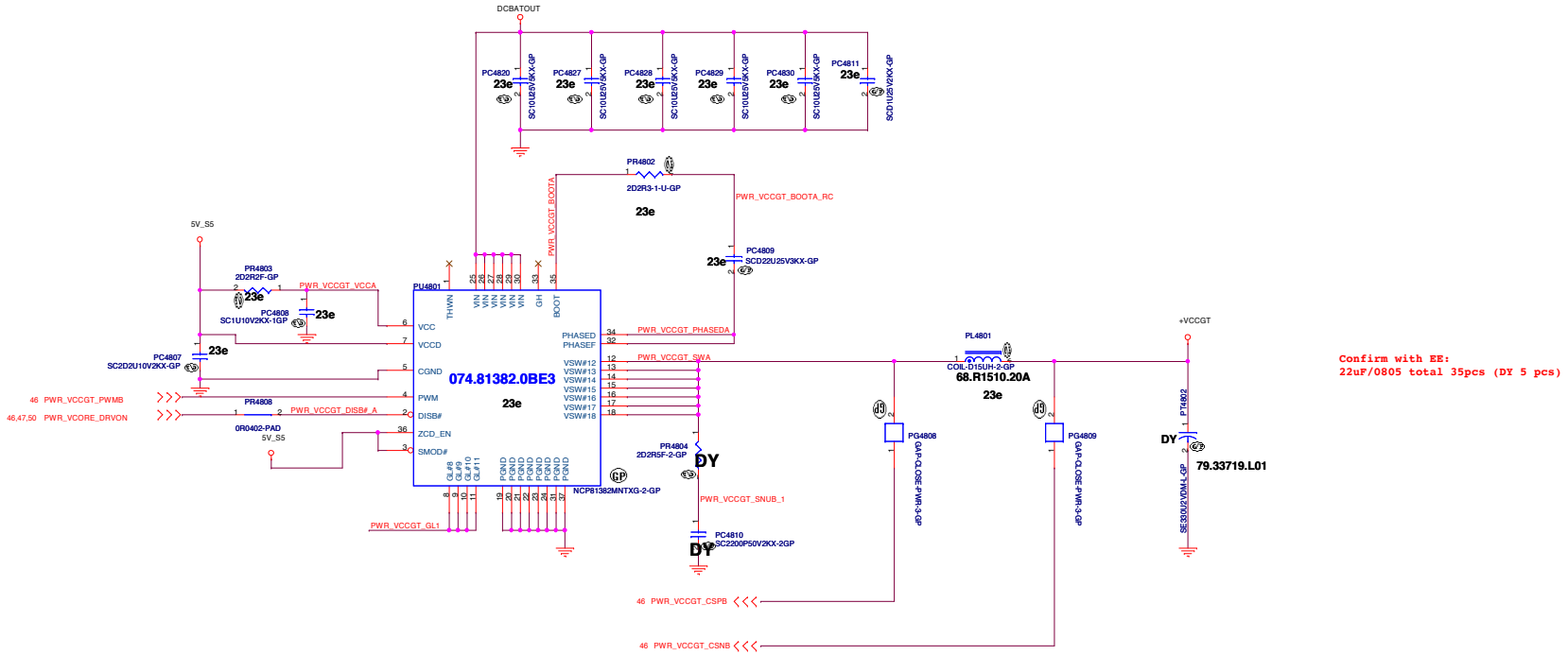
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_VCORE(2/3)***

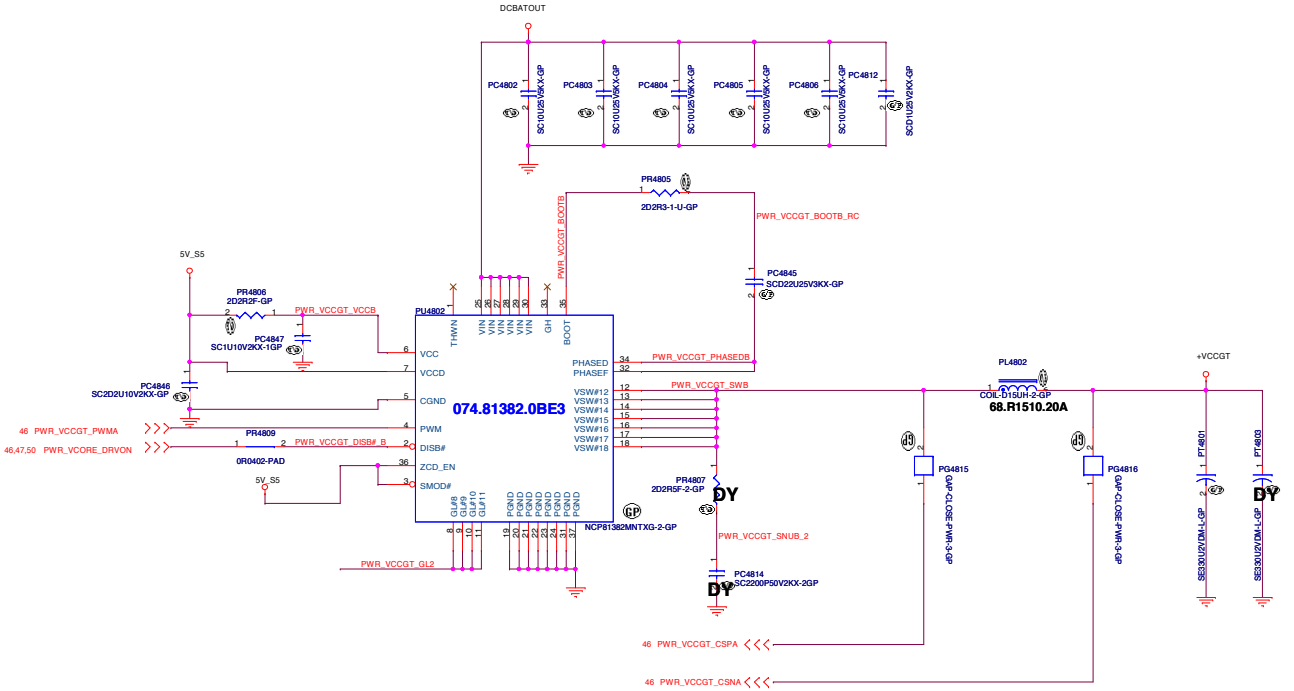
Size	Document Number	Rev
A3	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 47 of 102

Main Func = CPU_CORE



Confirm with EE:
22uF/0805 total 35pcs (DY 5 pcs)



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCCGT3/3)

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 48 of 102

BOM1

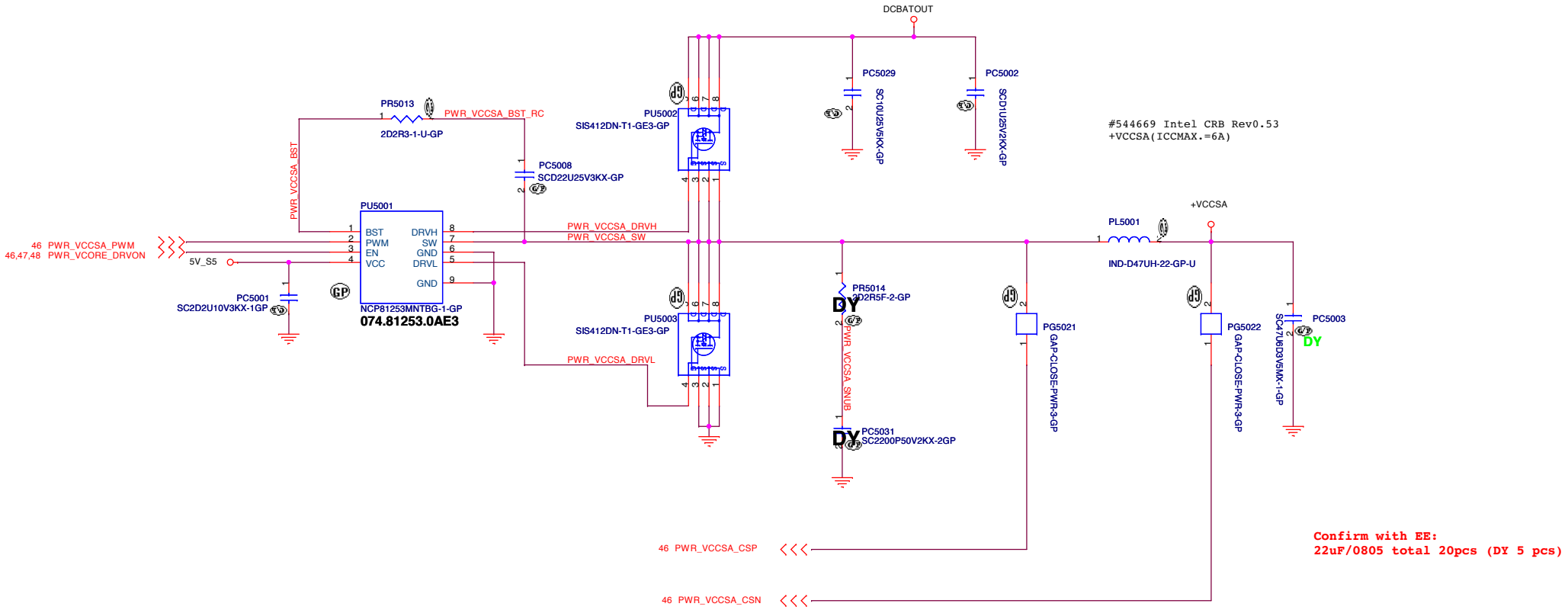
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU VCCGTUS***

Size	Document Number	Rev
A2	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 49 of 102

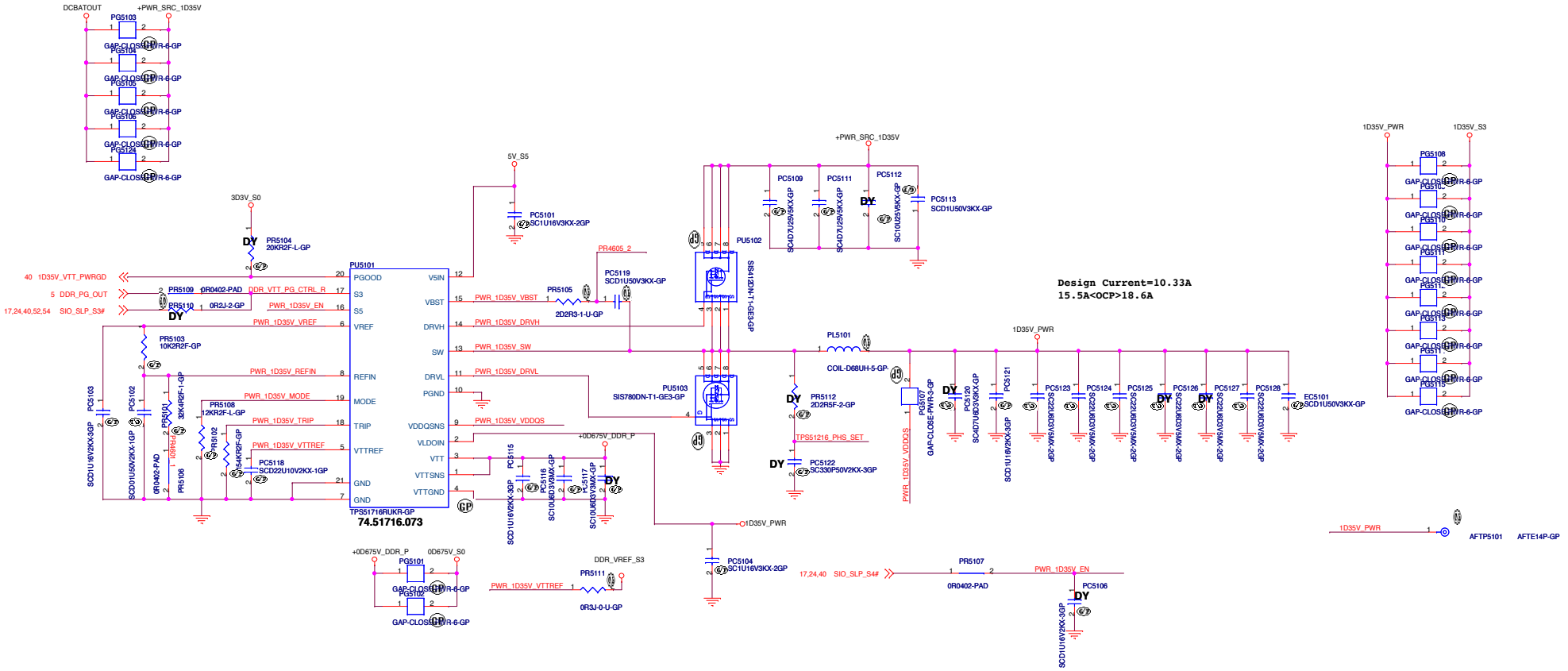
Main Func = CPU_CORE



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_VCCSA		
Size: A3	Document Number: Tesla SKL-U	Rev: -1
Date: Tuesday, July 21, 2015	Sheet 50 of 102	

Main Func = VDDQ



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 0.68UH PCMC063T-R68 5~5.5mohm Isat =25Arms 68.R6810.20B
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

BOM1

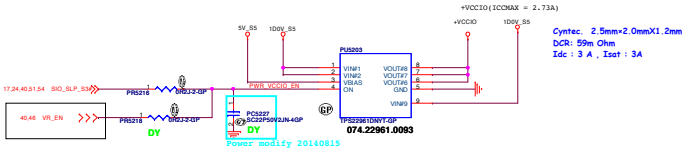
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MEM&MEMVTT

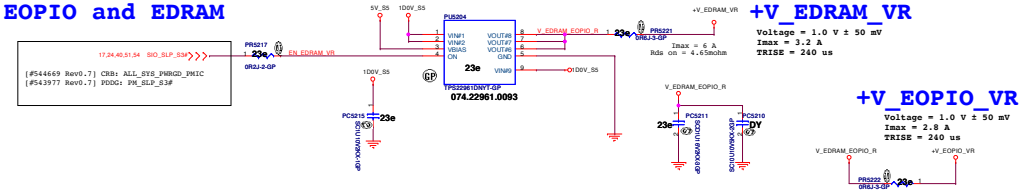
Size: C | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 51 of 102

VCCIO



EOPIO and EDRAM



BOM#

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

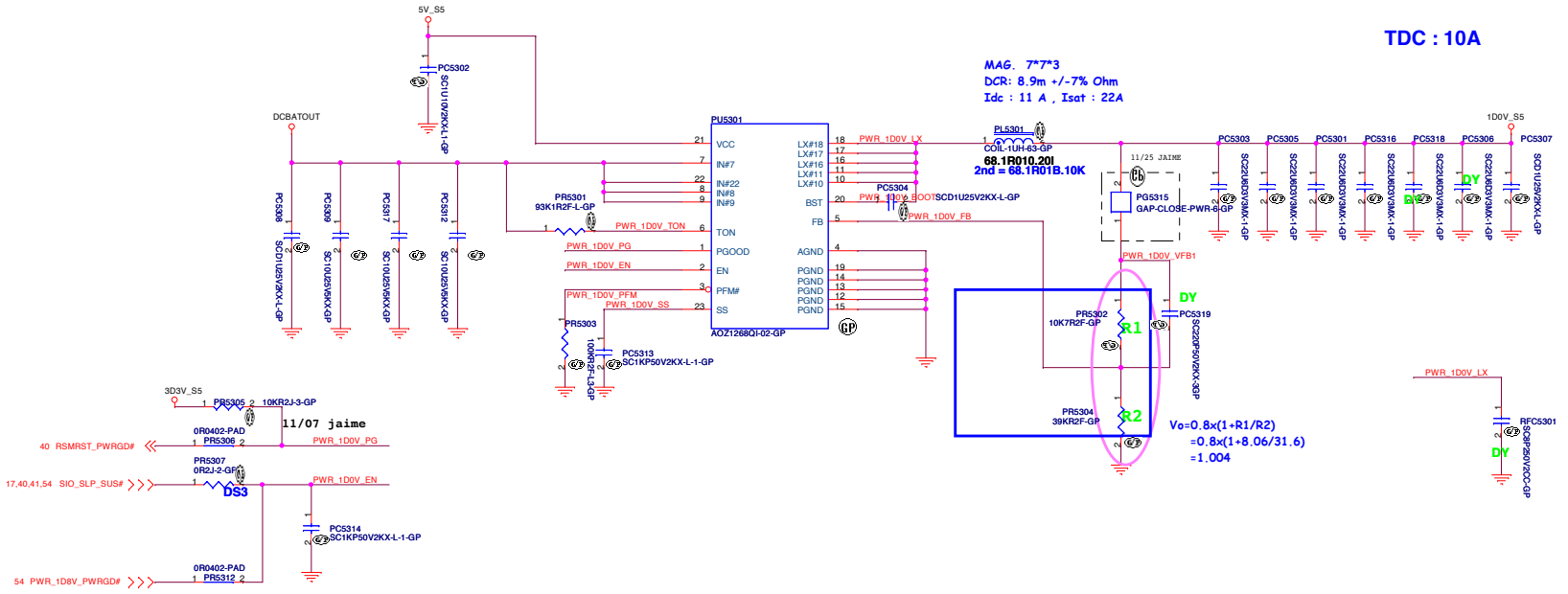
Title: *DCDC-0D975V_VCCIO*

Size	Document Number	Rev
Custom	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 52 of 102

Main Func = 1D0V

AOZ1268 for 1D0V

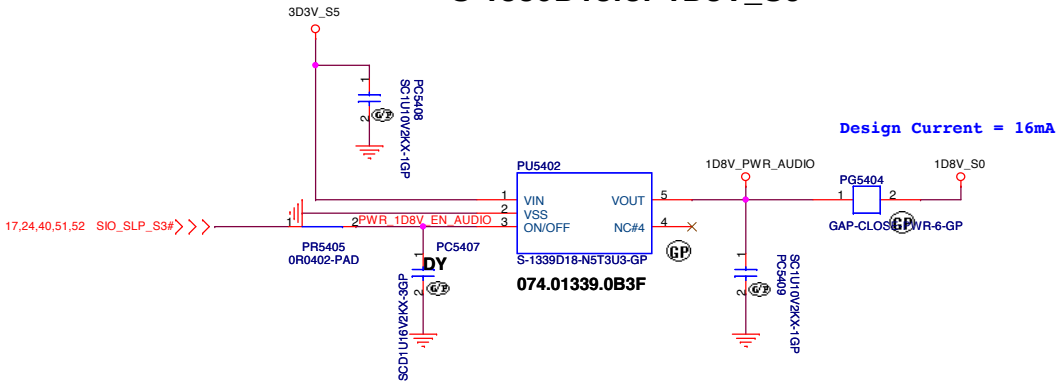


BOM1

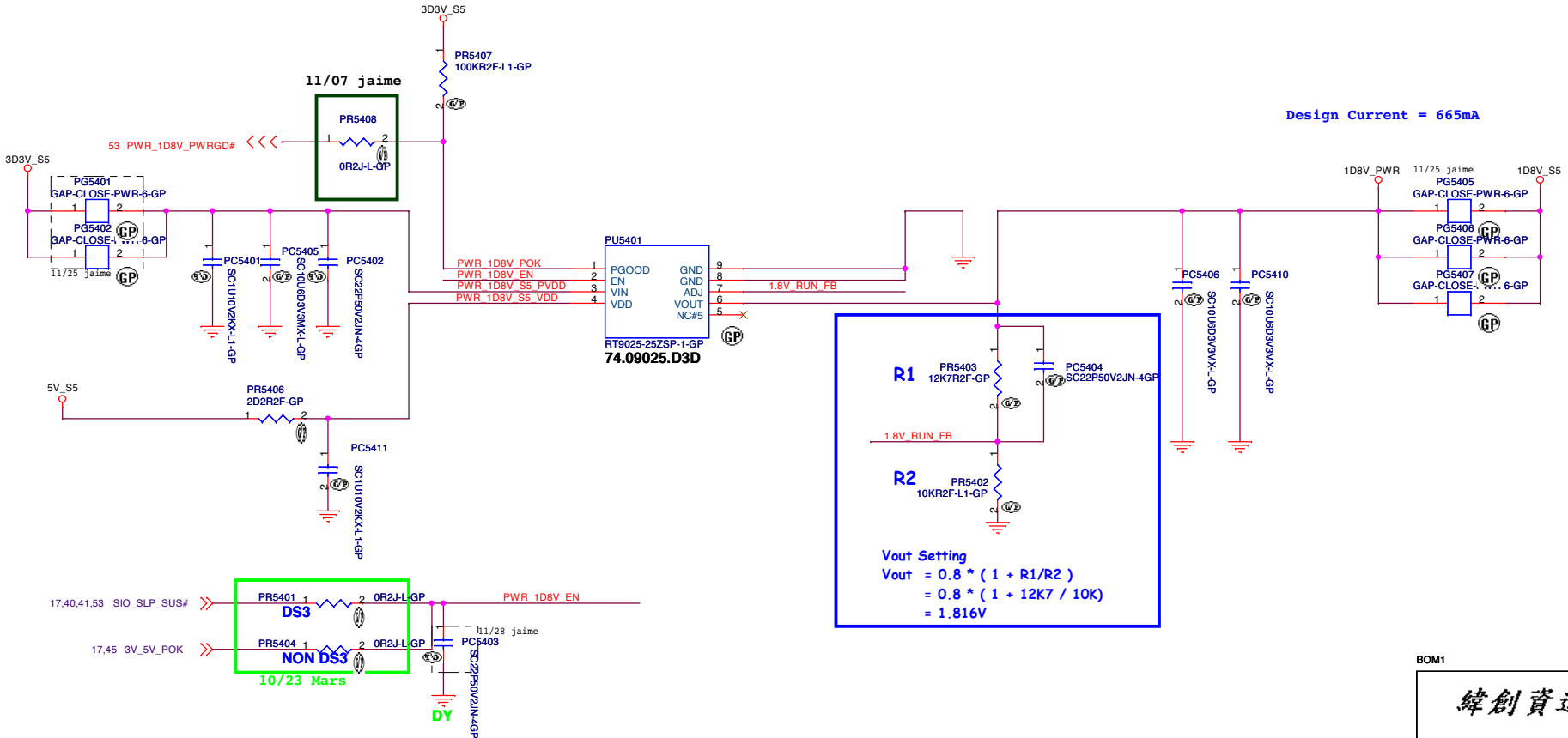
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCDC-V1D00A		
Size: Custom	Document Number: Tesla SKL-U	Rev: -1
Date: Tuesday, July 21, 2015	Sheet 53 of 102	

Main Func = 1D5V

S-1339D18for 1D8V_S0



1D8V_S5



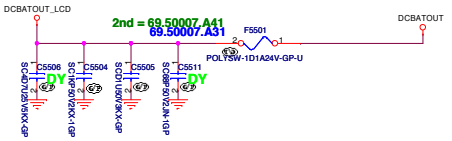
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LDO-V1D8V	
Size A3	Document Number Tesla SKL-U	Rev -1
Date: Tuesday, July 21, 2015	Sheet 54 of 102	

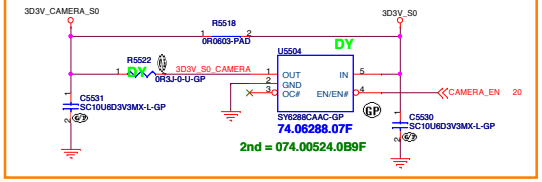
SSID = VIDEO

INVERTER POWER

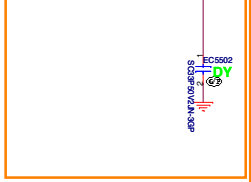


CAMERA POWER

Layout 40 mil



Close to eDP connector

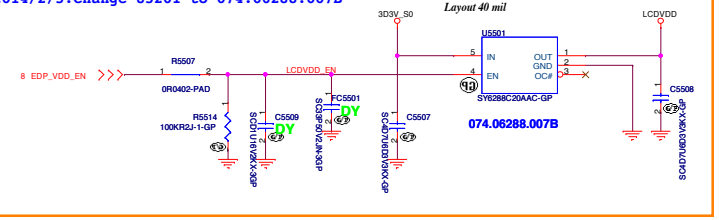


SSID = VIDEO

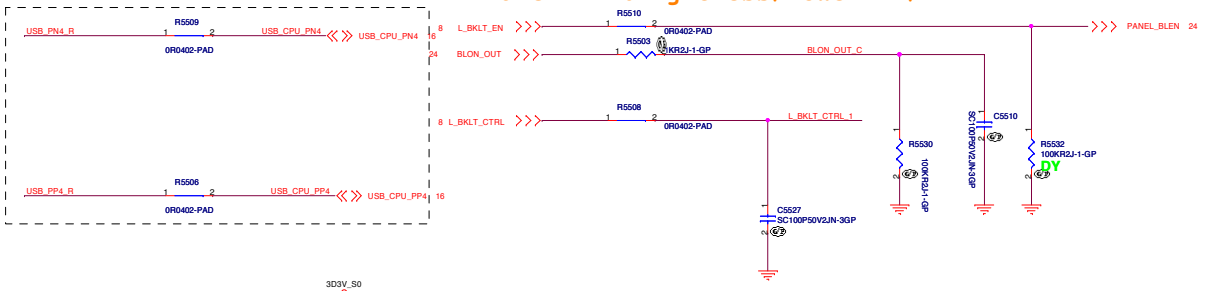
LCD POWER (Do Not use SW 74.09724.09F)

2014/2/5:Change U5201 to 074.06288.007B

Layout 40 mil



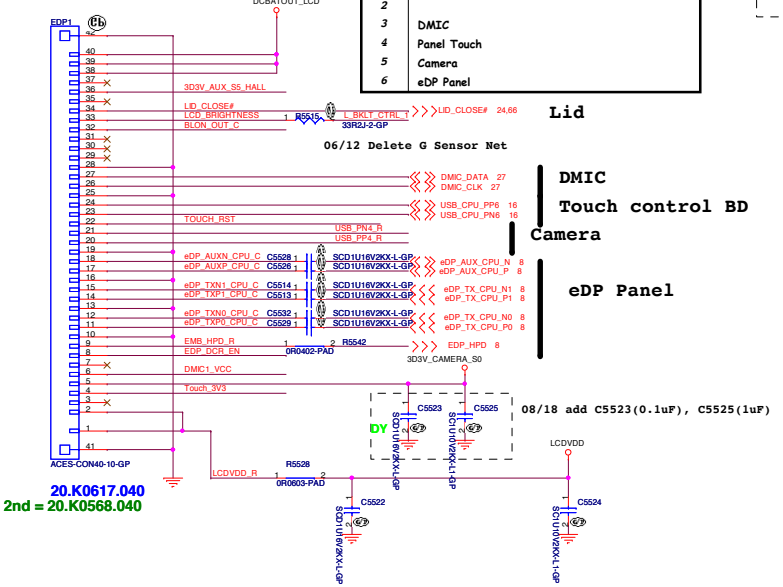
Panel BL brightness/Power En/BL En



eDP connector

eDP Device

Item	Device
1	Lid
2	
3	DMIC
4	Panel Touch
5	Camera
6	eDP Panel



Lid

06/12 Delete G Sensor Net

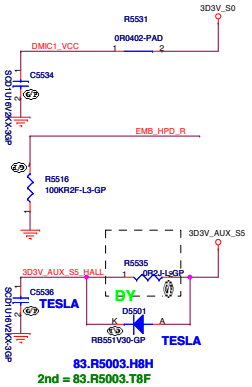
DMIC

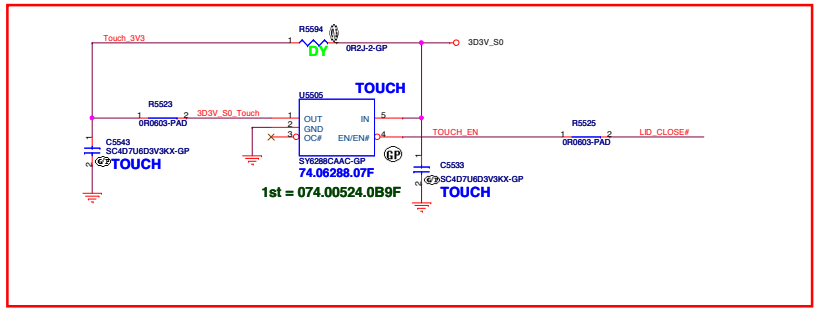
Touch control BD

Camera

eDP Panel

08/18 add C5523(0.1uF), C5525(1uF)



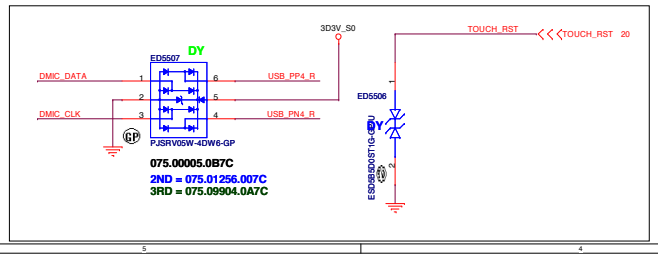


ESD Request

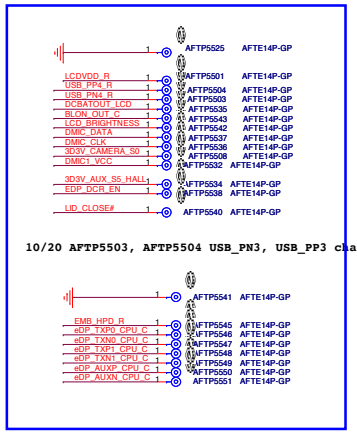
10/16 add ED5507

10/17 change ED5507 從6pin 改為10 pin(EMI要求)

10/20 change ED5507 從10pin 改為6 pin(EMI要求)



Test point



BOM1

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 55 of 102

BOM1

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Title: ***Reserved***

Size	Document Number	Rev
A3	**Tesla SKL-U**	-1

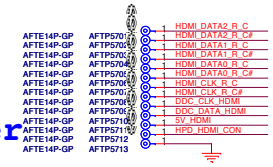
Date: Tuesday, July 21, 2015 Sheet 56 of 102

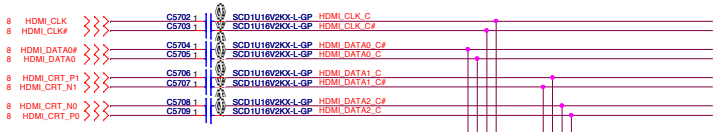
SSID = VIDEO

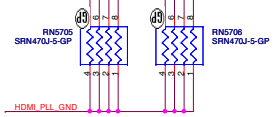
HDMI CONNECTOR

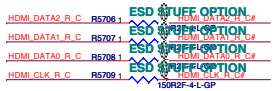
HDMI Passive Level Shifter

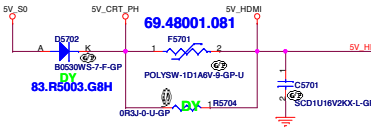
Close to HDMI Connector

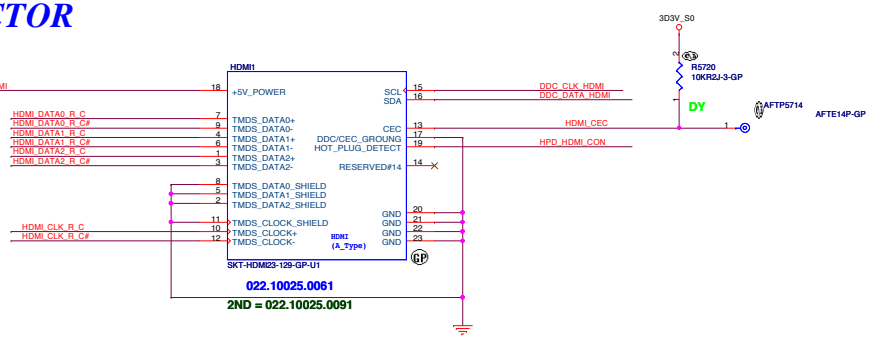






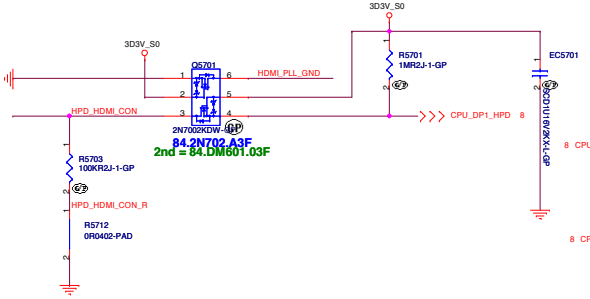


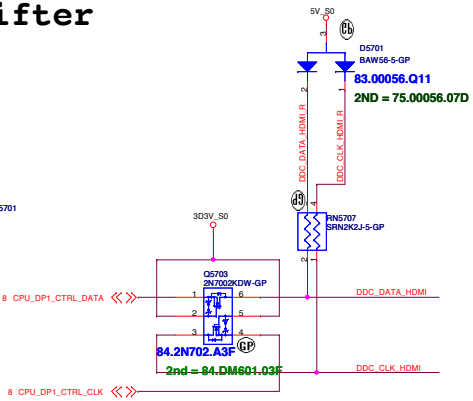


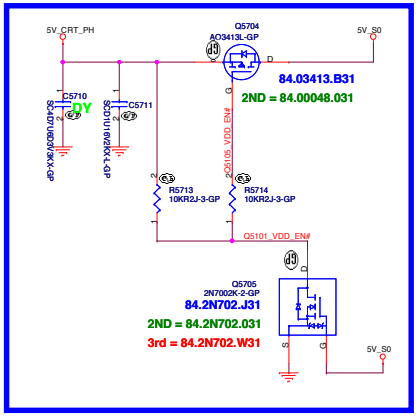


08/12 HDMI1 22.10296.B41 Change to 022.10025.0061

HDMI DDC Passive Level Shifter



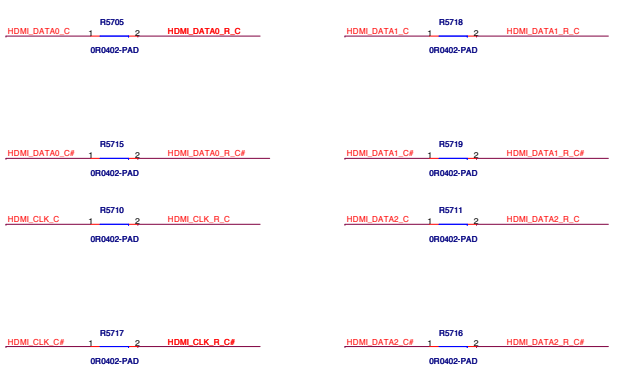


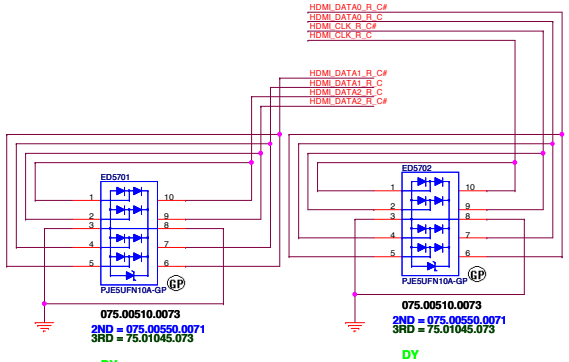


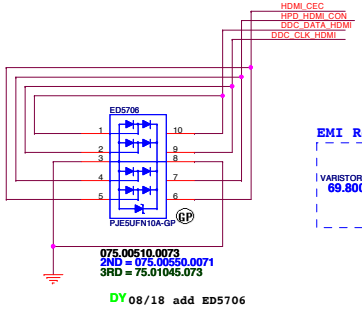
07/02 Change Part Number 84.07002.I31(禁用) to 84.2N702.J31

HDMI A type pin define (Total: 19pin)

Pin	Pin定義
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2–
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1–
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock–
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

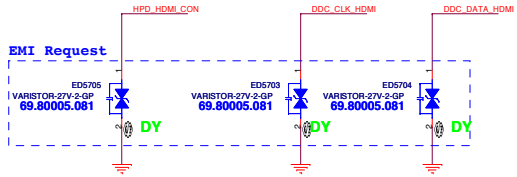






08/18 add ED5706

08/19 HPD_HDMI_CON & DDC_CLK_HDMI SWAP



10/15 ED5701,ED5702,ED5706 Change Part number to 75.00524.073

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 57 of 102

(Blanking)

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 58 of 102

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BOM1

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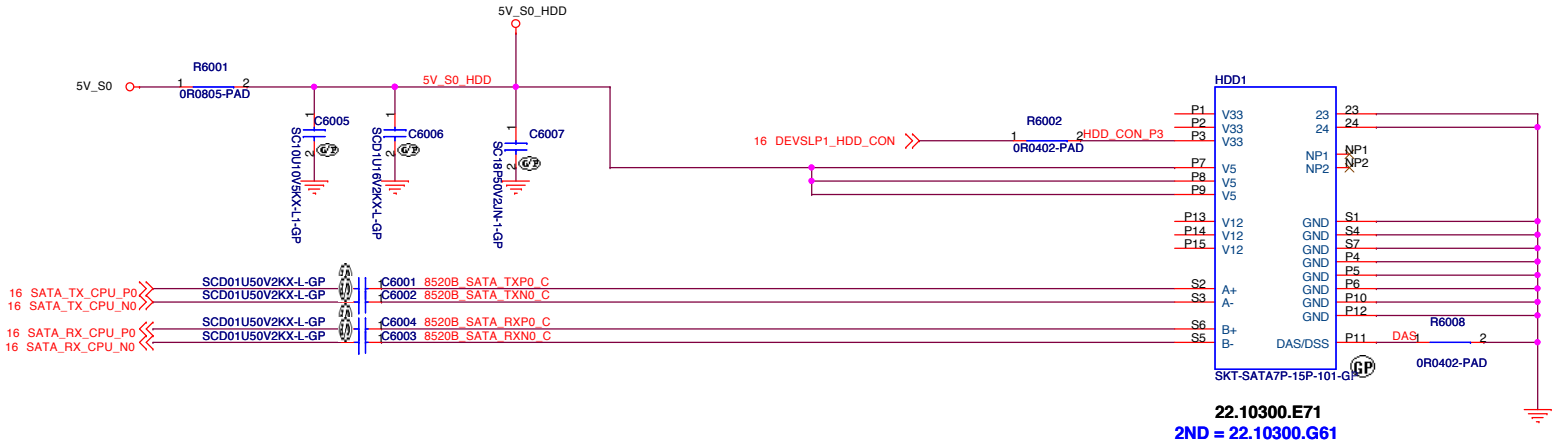
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A3	Tesla SKL-U	-1

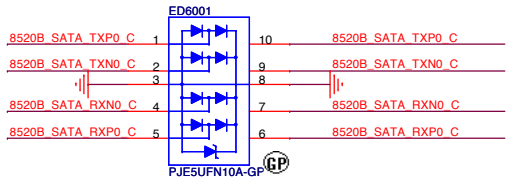
Date: Tuesday, July 21, 2015 Sheet 59 of 102

SSID = SATA



22.10300.E71

2ND = 22.10300.G61



075.00510.0073

1ST = 075.00550.0071

3RD = 75.01045.073

BOM1

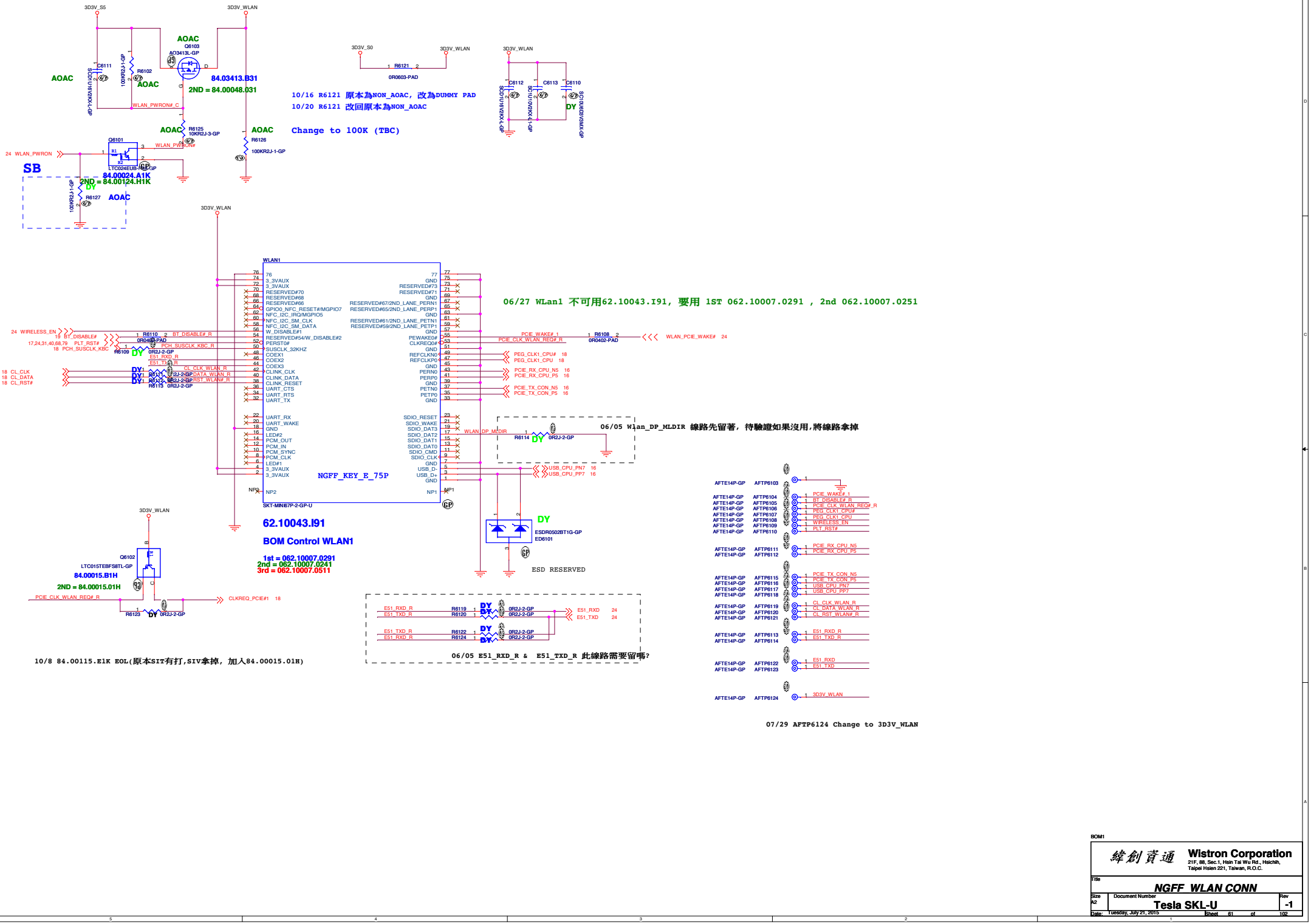
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SATA IF_HDD/ODD***

Size: A3 | Document Number: **Tesla SKL-U** | Rev: **-1**

Date: Wednesday, July 22, 2015 | Sheet 60 of 102


3D3V_S5
3D3V_WLAN
AOAC
Q6103
AO3413L-GP
84.03413.B31
2ND = 84.00048.031
C6111
R6102
100KR2J-1-GP
WLAN_PWRON#_C
R6125
10KR2J-3-GP
R6126
100KR2J-1-GP
Q6101
LTC024EUB-GP
WLAN_PWRON#
24 WLAN_PWRON
SB
84.00024.A1K
2ND = 84.00124.H1K
R6127
DY
3D3V_S0
R6121
0R0603-PAD
10/16 R6121 原本為NON_AOAC, 改為DUMMY PAD
10/20 R6121 改回原本為NON_AOAC
Change to 100K (TBC)
C6112
C6113
C6110
SC10U10V2KX-1-GP
SC10U6D3V0MX-GP
WLAN1
NGFF_KEY_E_75P
SKT-MINI67P-2-GP-U
24 WIRELESS_EN
19 BT_DISABLE#
17,24,31,40,68,79 PLT_RST#
18 PCH_SUSCLK_KBC
R6110
R6109
0R0402-PAD
0R2J-2-GP
18 CL_CLK
18 CL_DATA
18 CL_RST#
E51_RXD_R
E51_TXD_R
CL_CLK_WLAN_R
CL_DATA_WLAN_R
CL_RST_WLAN#_R
R6111
R6112
R6113
PCIE_WAKE#_1
PCIE_CLK_WLAN_REQ#_R
R6108
0R0402-PAD
WLAN_PCIE_WAKE# 24
PEG_CLK1_CPU# 18
PEG_CLK1_CPU 18
PCIE_RX_CPU_N5 16
PCIE_RX_CPU_P5 16
PCIE_TX_CON_N5 16
PCIE_TX_CON_P5 16
USB_CPU_PN7 16
USB_CPU_PP7 16
WLAN_DP_MLDIR
R6114
06/27 WLan1 不可用62.10043.I91, 要用 1ST 062.10007.0291 , 2nd 062.10007.0251
06/05 Wlan_DP_MLDIR 線路先留著, 待驗證如果沒用,將線路拿掉
62.10043.I91
BOM Control WLAN1
1st = 062.10007.0291
2nd = 062.10007.0241
3rd = 062.10007.0511
Q6102
LTC015TEBFS8TL-GP
84.00015.B1H
2ND = 84.00015.01H
PCIE_CLK_WLAN_REQ#_R
CLKREQ_PCIE#1 18
R6123
ESDR0502BT1G-GP
ED6101
ESD RESERVED
R6119
R6120
R6122
R6124
E51_RXD 24
E51_TXD 24
06/05 E51_RXD_R & E51_TXD_R 此線路需要留嗎?
10/8 84.00115.E1K EOL(原本SIT有打,SIV拿掉, 加入84.00015.01H)
AFTE14P-GP
AFTP6103
AFTP6104
AFTP6105
AFTP6106
AFTP6107
AFTP6108
AFTP6109
AFTP6110
AFTP6111
AFTP6112
AFTP6115
AFTP6116
AFTP6117
AFTP6118
AFTP6119
AFTP6120
AFTP6121
AFTP6113
AFTP6114
AFTP6122
AFTP6123
AFTP6124
PCIE_WAKE#_1
BT_DISABLE#_R
PCIE_CLK_WLAN_REQ#_R
PEG_CLK1_CPU#
PEG_CLK1_CPU
WIRELESS_EN
PLT_RST#
PCIE_RX_CPU_N5
PCIE_RX_CPU_P5
PCIE_TX_CON_N5
PCIE_TX_CON_P5
USB_CPU_PN7
USB_CPU_PP7
CL_CLK_WLAN_R
CL_DATA_WLAN_R
CL_RST_WLAN#_R
E51_RXD_R
E51_TXD_R
E51_RXD
E51_TXD
3D3V_WLAN
07/29 AFTP6124 Change to 3D3V_WLAN
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NGFF WLAN CONN
Size
A2
Document Number
Tesla SKL-U
Rev
-1
Date: Tuesday, July 21, 2015
Sheet 61 of 102

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 62 of 102

(Blanking)

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	**Tesla SKL-U**	-1

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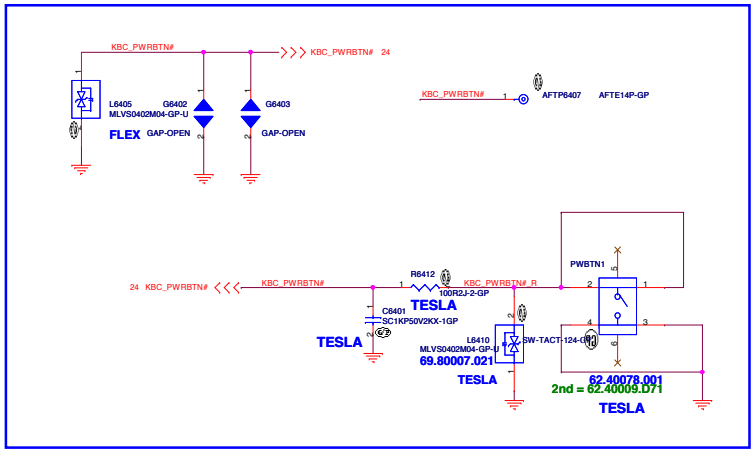
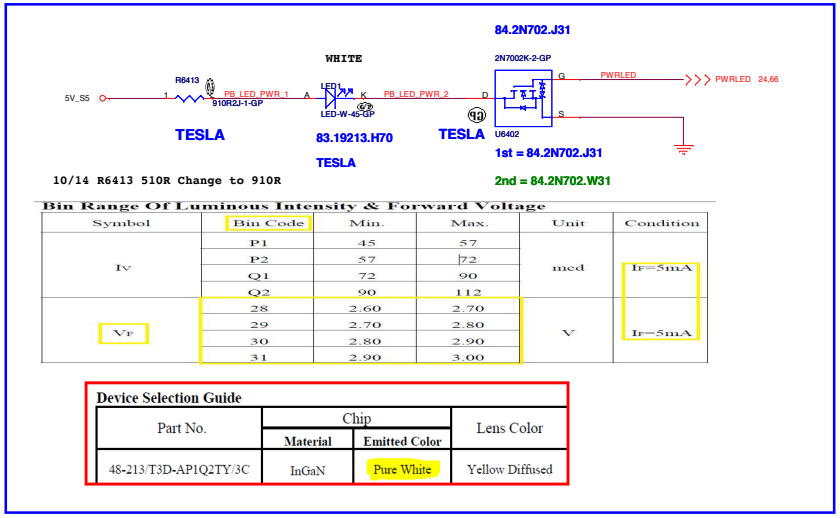
Power Button



POWER BTN LED



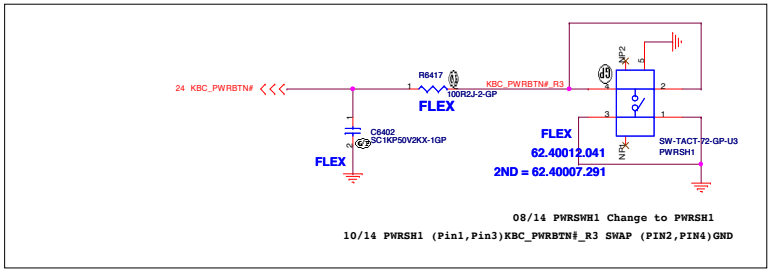
Bin Range Of Luminous Intensity & Forward Voltage

Symbol	Bin Code	Min.	Max.	Unit	Condition
Iv	P1	45	57	mcd	IF=5mA
	P2	57	72		
	Q1	72	90		
	Q2	90	112		
VF	28	2.60	2.70	V	IF=5mA
	29	2.70	2.80		
	30	2.80	2.90		
	31	2.90	3.00		

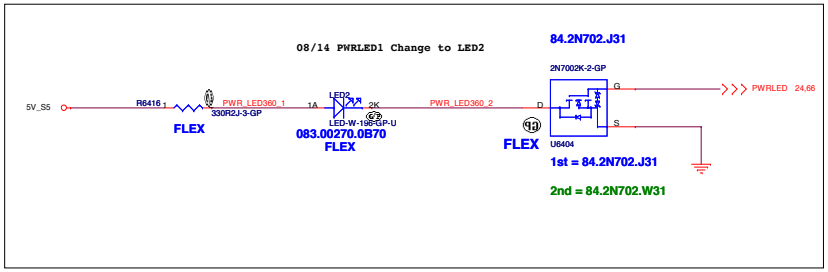
Device Selection Guide

Part No.	Chip		Lens Color
	Material	Emitted Color	
48-213/T3D-AP1Q2TY/3C	InGaN	Pure White	Yellow Diffused

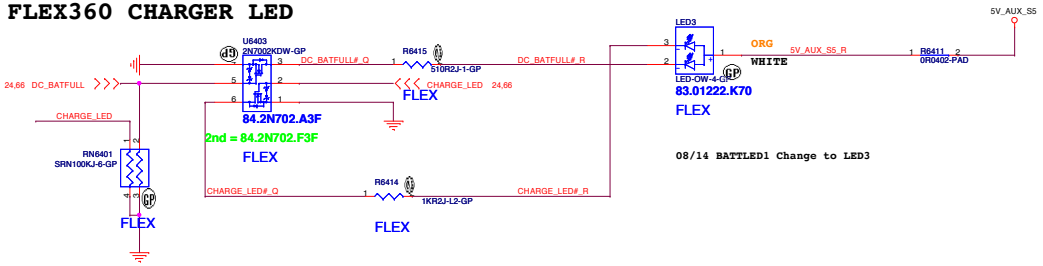
FLEX360 Power Button



FLEX360 POWER BTN LED



FLEX360 CHARGER LED

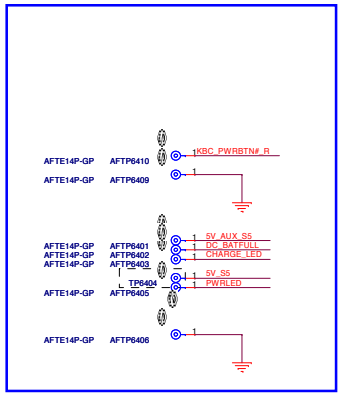


Electro-Optical Characteristics (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	VF (2 Different Bin Code type: S2S / T3)	1.7	-----	2.3	V	IF=5mA
		2.7	-----	3.3		

Chip Materials	Emitted Color
AlGaInP	Brilliant Orange
InGaN	Pure White

Test point



BOM1

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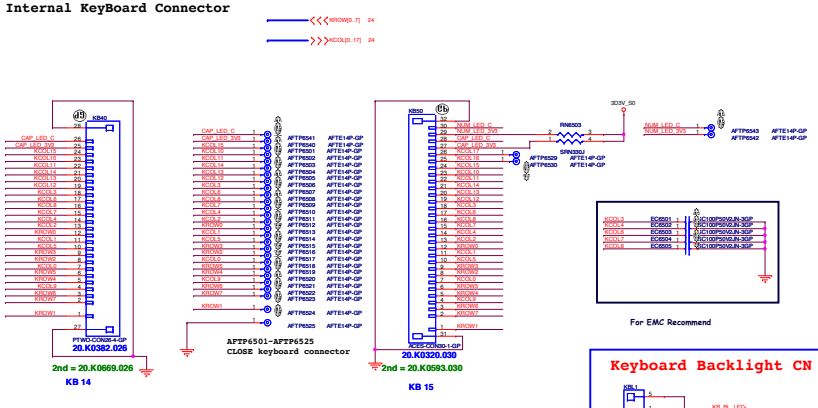
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

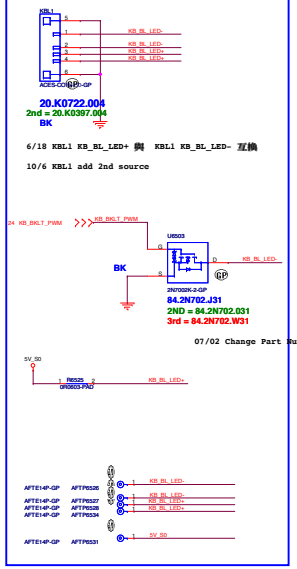
Size: A2 | Document Number: Tesla SKL-U | Rev: -1

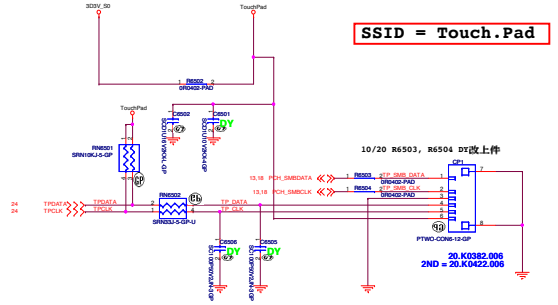
Date: Tuesday, July 21, 2015 | Sheet 64 of 102

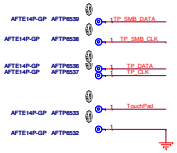
Internal KeyBoard Connector



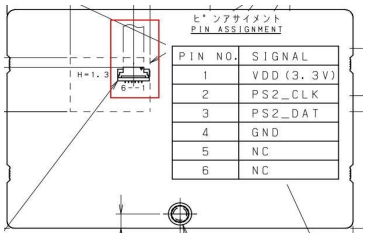
Keyboard Backlight CN







Ref. SPEC:KGDFF0106A11BO 31A
SA469D-22H1_v1.0
VCC=3.3V



U6203 Keyboard Backlight U6203&BLKB1:

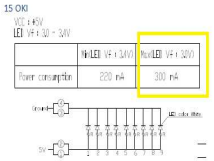
目前spec所看到
14和15的keyboard spec最大為300 mA

84.07002.I31

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_{amb} = 25 °C		-	-	60	V
V_{GS}	gate-source voltage	T_{amb} = 25 °C		-	-	±20	V
I_D	drain current	T_{amb} = 25 °C; V_{GS} = 10 V	[1]	-	-	350	mA
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 10 V; I_D = 500 mA		-	1	1.6	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



BOM#

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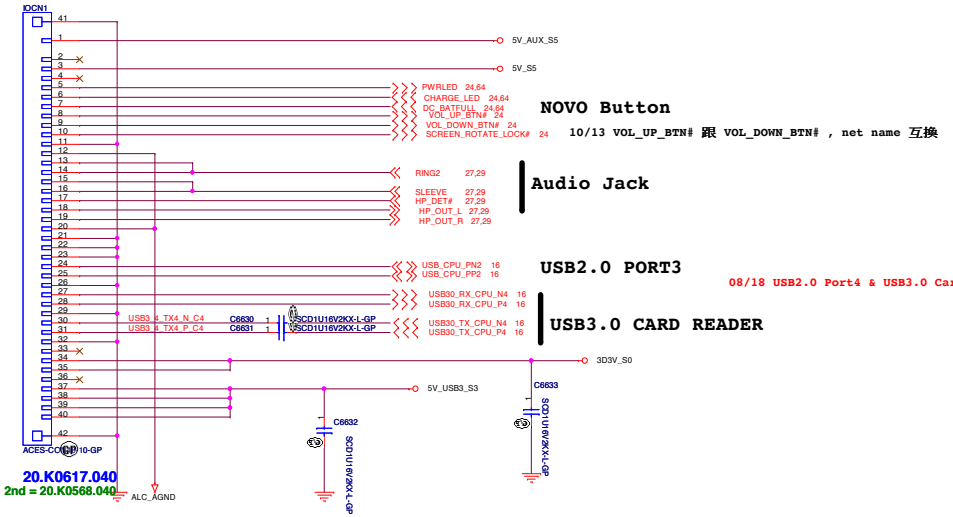
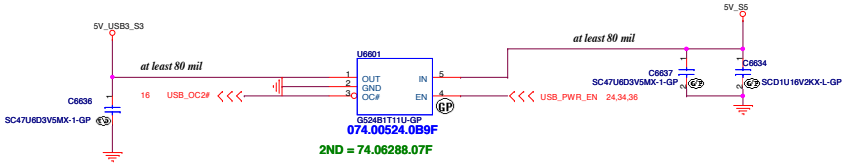
Title: Key Board&Touch Pad			
Size: A3	Document Number: Tesla SKL-U		Rev: -1
Date: Wednesday, July 02, 2015	Sheet: 65	of: 102	

IO BD Device

Item	Device
1	NOVO Button
2	Audio Jack
3	USB Card Reader
4	USB2.0 Port4

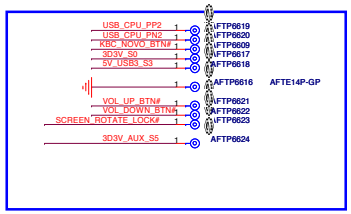


USB 2.0 Power SW

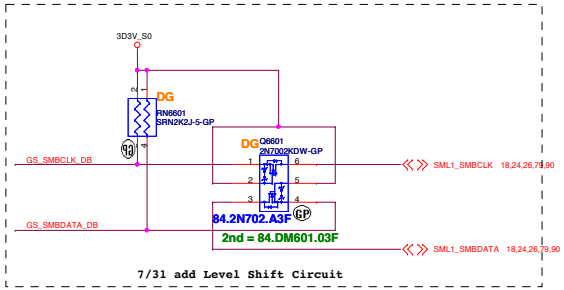


U6301 place near to IOCN1

Test point

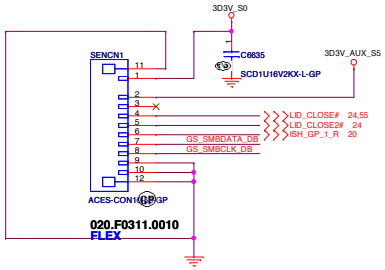


10/13 VOL_UP_BTN# 跟 VOL_DOWN_BTN# , net name 互換



7/31 add Level Shift Circuit

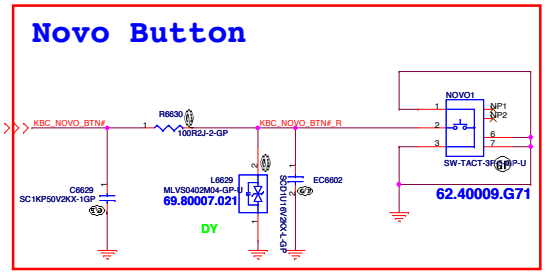
Flex360 SENSOR BD



Hall sensor

06/12 Delete Hall Sensor CONN, 換7 pin 與SPK 訊號接同一CONN, SPK1

Novo Button



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 66 of 102

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

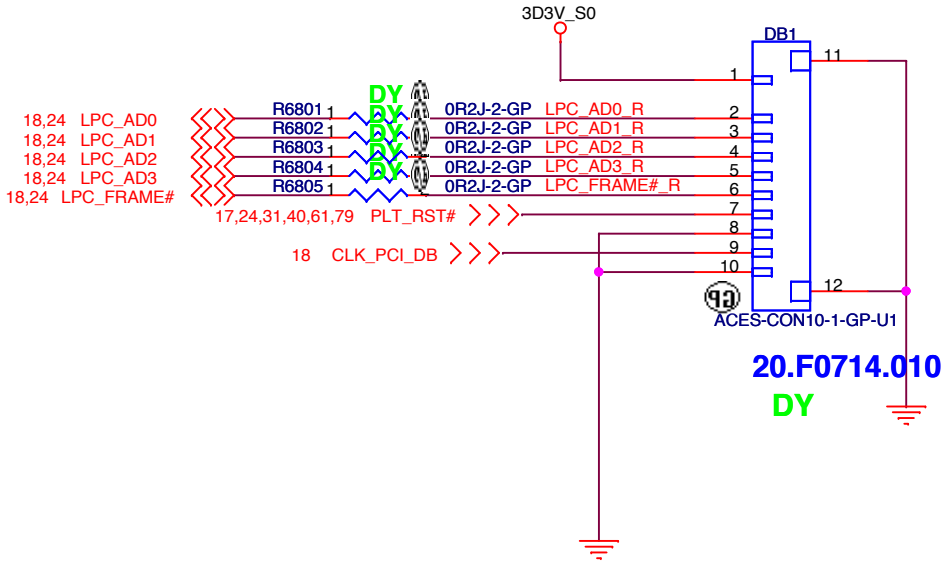
Title: ***RESERVED***

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 67 of 102

Main Func = Debug

Debug Connector



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Debug connector*		
Size: A4	Document Number: Tesla SKL-U	Rev: -1
Date: Tuesday, July 21, 2015	Sheet 68 of 102	

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BOM1

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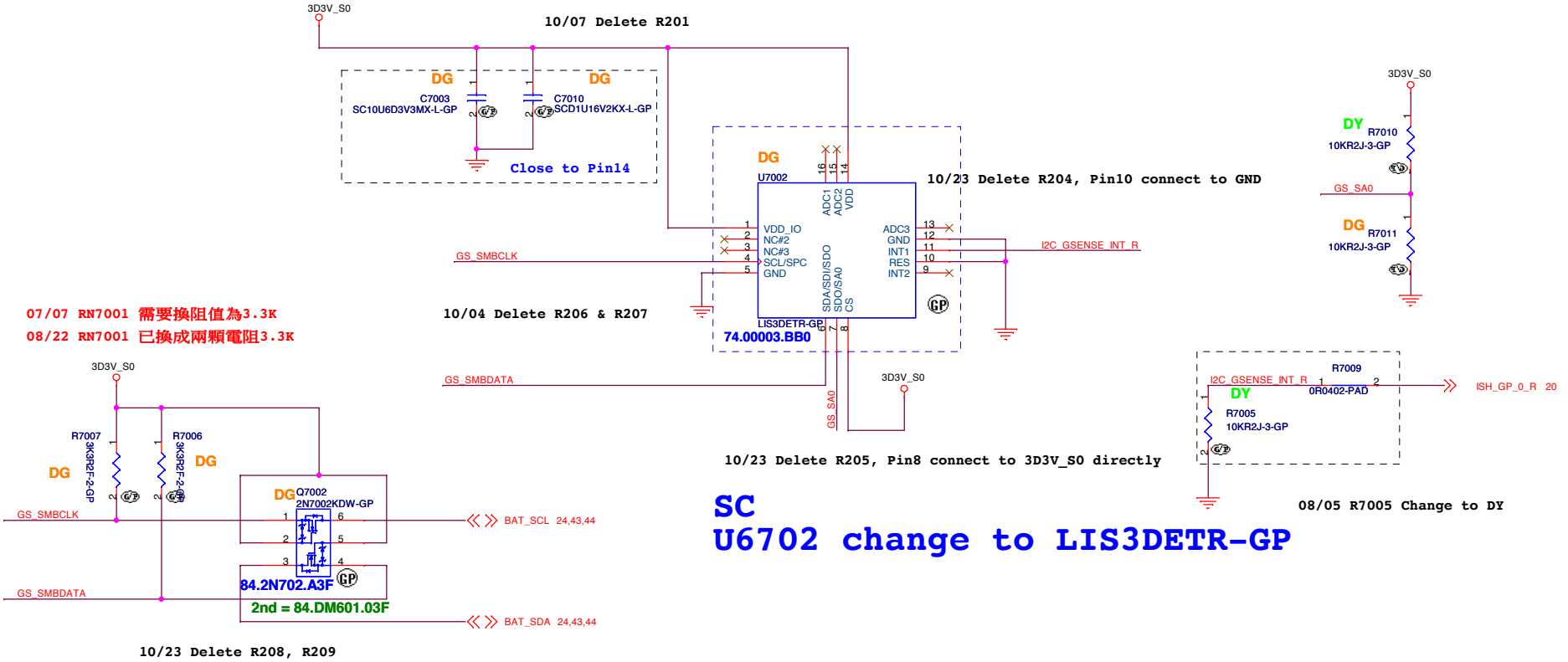
Title: ***Reserved***

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 69 of 102

SC Digital_G-sensor

The Slave ADdress (SAD) associated to the LIS3DH is 001100xb. SDO/SA0 pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b) else if SA0 pad is connected to ground, LSb value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I2C lines.



SC U6702 change to LIS3DETR-GP

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: G Sensor		
Size: A3	Document Number: Tesla SKL-U	Rev: -1
Date: Tuesday, July 21, 2015	Sheet 70 of 102	

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Title: ***Reserved***

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 71 of 102

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Size	Document Number	Rev
A3	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 72 of 102

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Title: ***Reserved***

Size	Document Number	Rev
A3	**Tesla SKL-U**	**-1**

Date: Tuesday, July 21, 2015 Sheet 73 of 102

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A3	Document Number: **Tesla SKL-U**	Rev: **-1**
Date: Tuesday, July 21, 2015	Sheet 74 of 102	

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BOM1

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Title: ***Reserved***

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 75 of 102

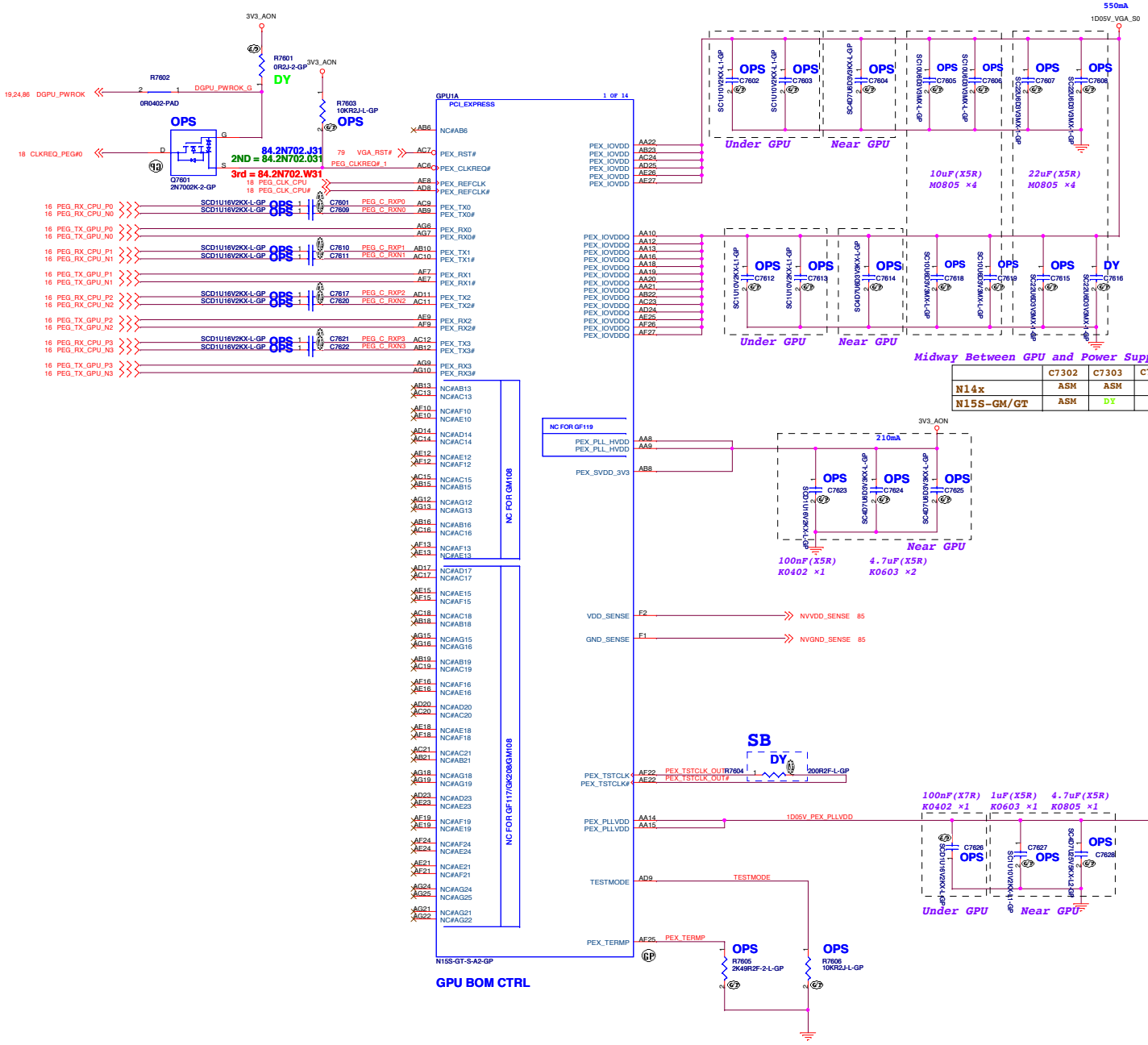

Table 3. PEX_IOVDD/Q Decoupling

Capacitor Type			Typical N14x Population	N15V-GM Population	N15S-GV Population	N15S-GM/-GT Population	Location
1u0uF	X6S	0402	4	4	4	1	Under GPU
4.7uF	X6S	0603	2	2	2	1	Under GPU
10uF	X5R	0805	4	4	4	1	Near GPU
22uF	X5R	0805	4	4	4	1	Near GPU

	C7302	C7303	C7304	C7305	C7306	C7307	C7308	C7312	C7313	C7314	C7318	C7319	C7315	C7316
N14x	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM
N15S-GM/GT	ASM	DY	ASM	ASM	DY	ASM	DY	DY	DY	DY	DY	DY	DY	DY

BOM1

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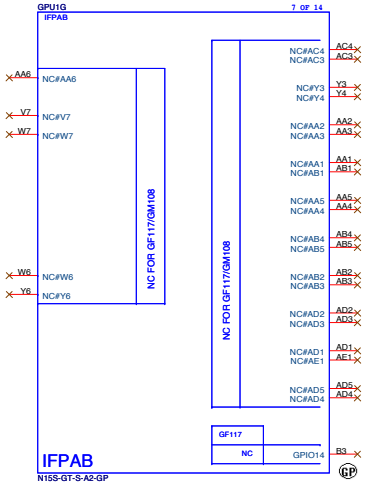
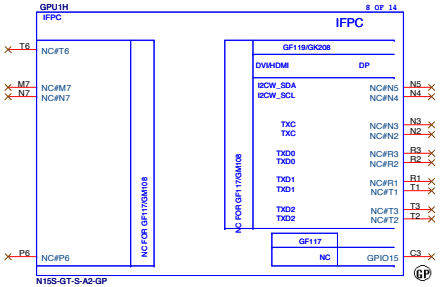
Title: GPU(1/5) PEG

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

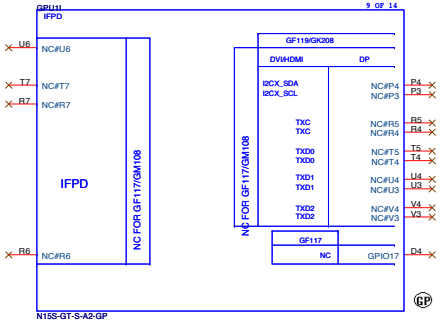
Date: Tuesday, July 21, 2015 | Sheet 76 of 102



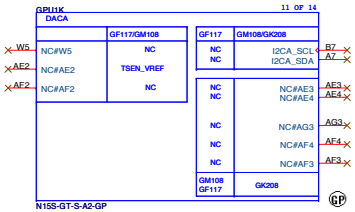
GPU BOM CTRL



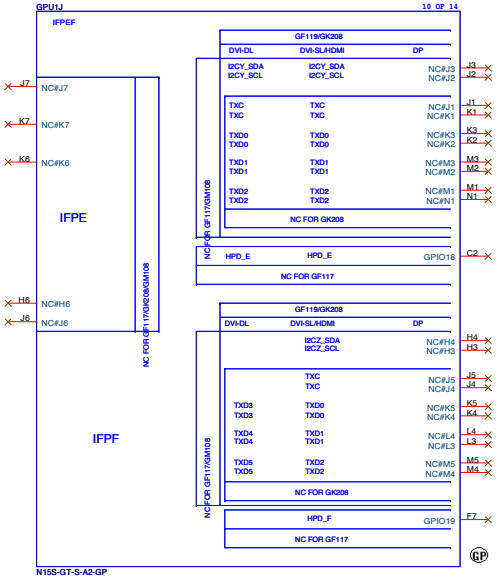
GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL

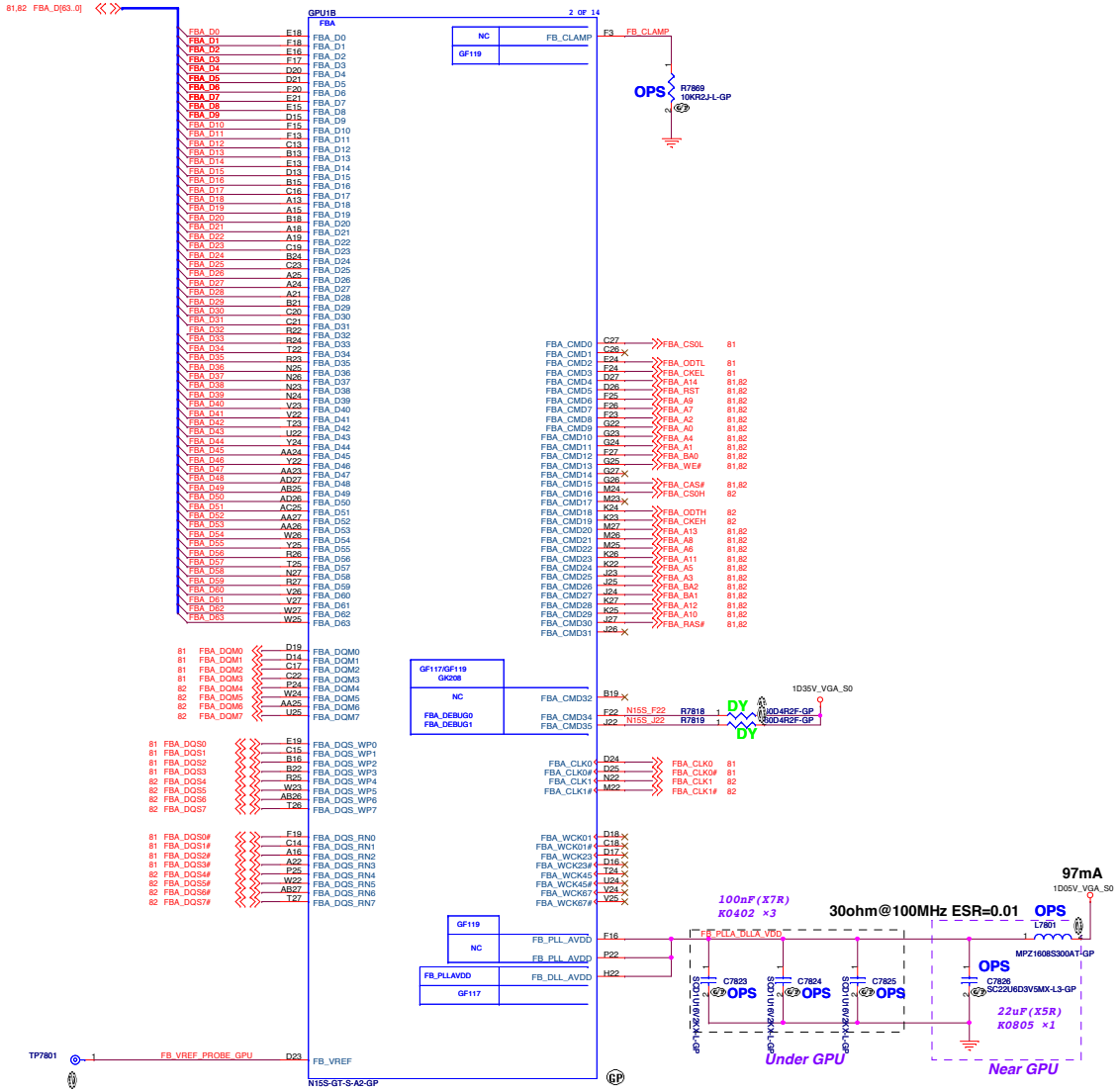
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (2/5) DIGITALOUT***

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 77 of 102



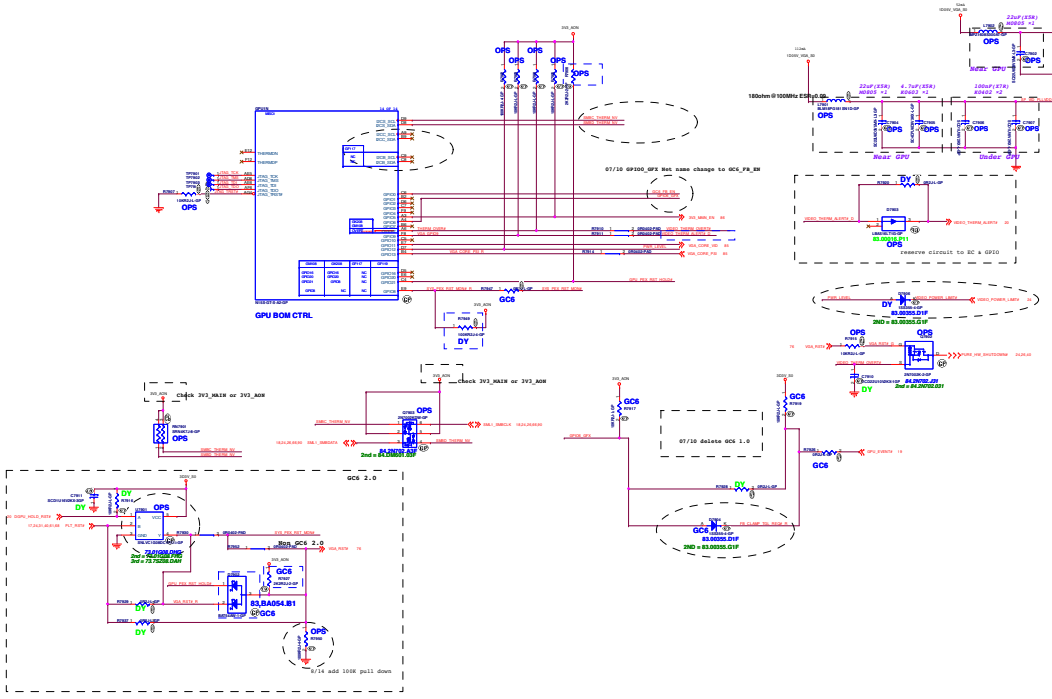
BOM1

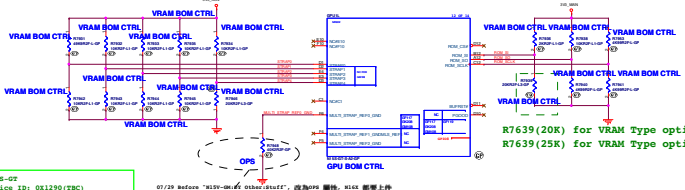
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (3/5) VRAM I/F

Size: Custom | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 78 of 102





R7639(20K) for VRAM Type option (Default: Hynix)
R7639(25K) for VRAM Type option (Micron)

N15S-GT
Device ID: 0X1290(TBC)

07/29 Before "N15V-GM-K Other stuff", 改為OPS 屬性, N16S 都要上件
NOTE: "N15V-GM" with Binary mode support, left Multi_Strap_Ref0_GND pin "NC";
All other N16x GPUs, connect Multi_Strap_Ref0_GND pin to GND per 40.2K resister

NVIDIA TABLE		N15S-GT Hynix 256Mx16 H5TC4G63AFR-11C Device ID 0X1140(TBC)	N15S-GT Micron 256Mx16 MT41J256M16HA-093:E Device ID 0X1140(TBC)
ROM_SI(Depend on VRAM type)	R7636	DY	DY
	R7639	20Kohm	25Kohm
ROM_SO	R7637	DY	DY
	R7640	4.99Kohm	4.99Kohm
ROM_CLK	R7638	DY	DY
	R7641	4.99Kohm	4.99Kohm
STRAP0	R7631	50Kohm	50Kohm
	R7642	DY	DY
STRAP1	R7632	DY	DY
	R7643	DY	DY
STRAP2	R7633	DY	DY
	R7644	DY	DY
STRAP3	R7635	DY	DY
	R7645	DY	DY
STRAP4	R7634	DY	DY
	R7646	DY	DY

NVVDD Boot Voltage 0.9V

SKU4, SKU5 ----->
4GB (VRAM*8)
SKU2, SKU3 ----->
2GB(VRAM*4)(VRAM1,2,5,6 ASM)

1D35V Compatible VRAM P/N List

Vendor	Vendor P/N	Lenovo P/N	1 chip VRAM Size
Hynix	H5TC4G63AFR-11C	1100897	512MB
Micron	MT41J256M16HA-093G:E	1101018	512MB

GPU Config:

GPU	SKU1 UMA	SKU2	SKU3	SKU4	SKU5
N15S-GT 071.0N15S.0C0U	NA	STUFF	STUFF	STUFF	STUFF

GPIO Description (DG-06803-001_v04_p.180_Tale 12-1)

Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage.
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	10K pull-up to 3V3_AON unless actively driven.
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON

GPU (Dual Rank) VRAM Config:

Table 4. N15V-GM DDR3L Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3L	Hynix	0x4	1.35 V/ 1.35 V	H5TC4G63AFR-11C	900	N/A	Production ready
	Micron	0xD	1.35 V/ 1.35 V	MT41K256M16HA-107G:E	900	N/A	Production ready

N15S-GT(GB2-64/GT840M)-->SB SKU2,3,4,5

Table 20. N15S-GT/GM DDR3L Dual-Rank Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256M-16 DDR3L	Hynix	0x3	1.35 V/ 1.35 V	H5TC4G63AFR-11C	900	N/A	Preliminary
	Micron	0x4	1.35 V/ 1.35 V	MT41J256M16HA-093G:E	900	1322	Preliminary
	Samsung	0x5	1.35V/ 1.35V	K4W4G1646D-HC1A	900	N/A	Preliminary

Note: For N15S-GT/-GM, the maximum allowable memory case temperature is 85 °C.

Table 1. N15E-GX /-GT GC6 pin assignment

GPIO	GC6 1.0 Control Signal	GC6 2.0 Control Signal
GPIO1	FB_CLAMP_MON	GC6_FB_EN
GPIO2	FBCLAMP_TGL_REQ#	GPU_EVENT#
GPIO4	Reserve	PWR_EN
GPIO23	Reserve	GPU_PEX_RST_HOLD#
CEC	NC	SYS_PEX_RST_MON#

GC6 1.0/2.0 GPU Support List

GPU	GC6 feature
N15V-GM-S(GF117)	No
N15V-GM-B(GF117)	No
N15S-GV(GK208)	GC6 1.0 only
N15S-GM(GM108)	GC6 2.0 only
N15S-GT(GM108)	GC6 2.0 only
N15S-GS(GM107)	GC6 2.0 only
N15P-GT(GM107)	GC6 2.0 only
N15P-GX(GM107)	GC6 2.0 only
N15E-GX(GK104)	GC6 1.0 only
N15E-GT(GK104)	GC6 1.0 only

Wistron Corporation
GPU (4/5) GPIOSTRAP
Tesla SKU-U

10/16 GPU PN change to 071.GM108.000U

VGA_CORE

4.7uF(X5R) K0603 ×10

Under GPU

Change to 78.47520.5BL for layout space SC

4.7uF(X5R) K0805 ×5

Near GPU

10/17 Delete C7712

1uF(X5R) K0402 ×4

8/15 Change 1uF 0603 to 0402 size

Under GPU

22uF(X5R) M0805 ×1

47uF(X5R) M0805 ×1

Near GPU

GPU1E 5 OF 14

N15S-GT-S-A2-GP

GPU BOM CTRL

GPU1F 6 OF 14

N15S-GT-S-A2-GP

GPU BOM CTRL

85mA

3V3_MAIN

0.1uF(X7R) K0402 ×2

1uF(X5R) K0603 ×1

4.7uF(X5R) K0603 ×1

Under GPU

Near GPU

1uF(X5R) K0603 ×1

4.7uF(X5R) K0603 ×1

3V3_AON

0.1uF(X7R) K0402 ×1

Under GPU

Near GPU

TP8004

GPU_NC_F11

GPU1C 3 OF 14

N15S-GT-S-A2-GP

GPU BOM CTRL

1D35V_VGA_S0

0.1uF(X7R) K0402 ×2

1uF(X7R) K0603 ×2

4.7uF(X5R) K0603 ×2

Under GPU

22uF(X5R) M0805 ×1

10uF(X5R) M0805 ×1

Near GPU

GPU1D 4 OF 14

N15S-GT-S-A2-GP

GPU BOM CTRL

1D35V_VGA_S0

FB_CAL_VDDQ

FB_CAL_GND

FB_CAL_TERM

FB_CAL_PD_VDDQ

FB_CAL_PU_GND

FB_CAL_TERM_GND

R8001 40D2R2F-GP

R8002 51D1R2F-GP

R8003 40D2R2F-GP

BOM1

緯創資通 Wistron Corporation

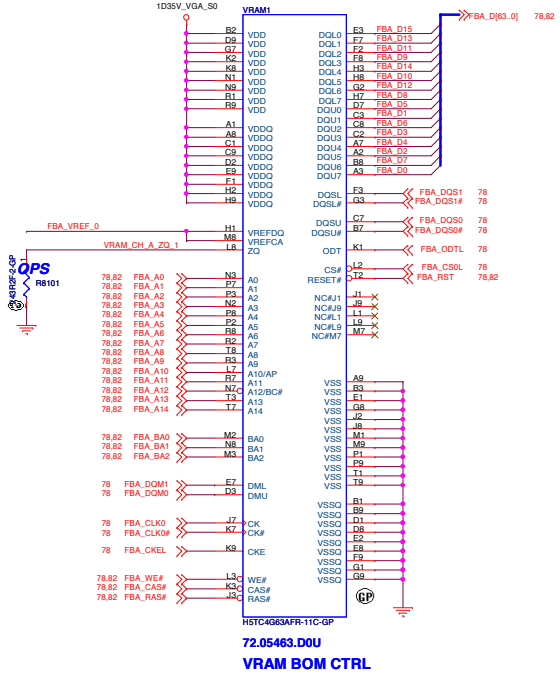
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

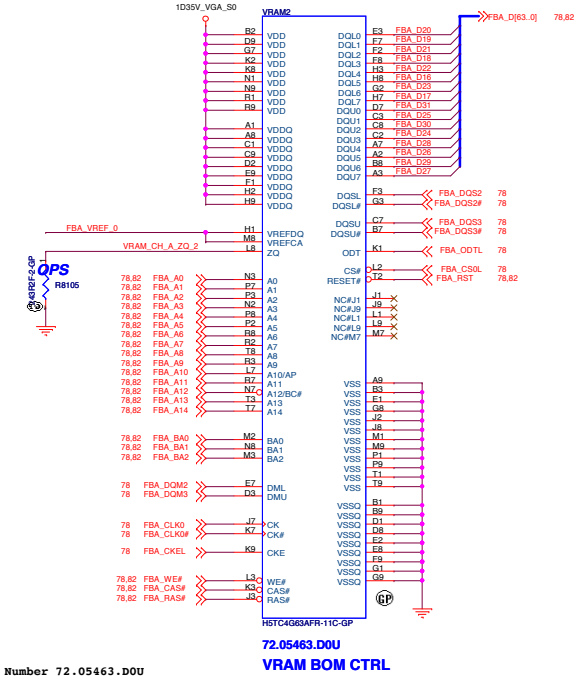
Title: GPU (5/5) PWR/GND

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

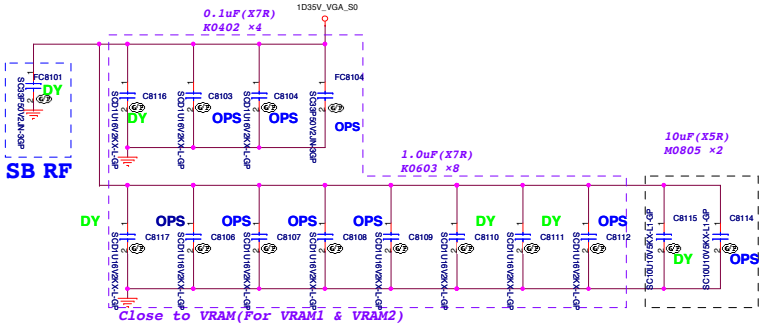
Date: Tuesday, July 21, 2015 | Sheet 80 of 102

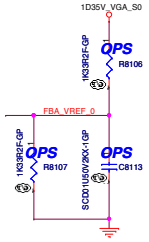
Data Bits 31:0 RANK 0





10/23 VRAM1-VRAM8 改Part Number 72.05463.D0U





08/18 C7801, C7804, C7805,C7810, C7811 Change to DY

08/18 C7814 Change to VRAM_8PCS

BOM1

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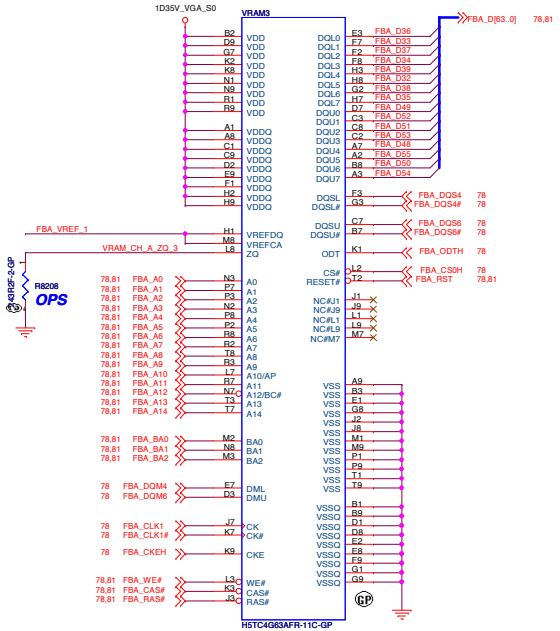
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM1,2 (1/4)

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 81 of 102

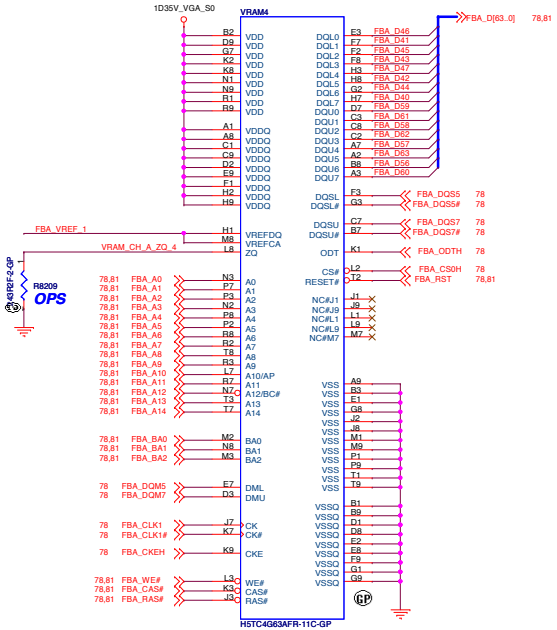
Data Bits 31:0 RANK 1



72.05463.D0U

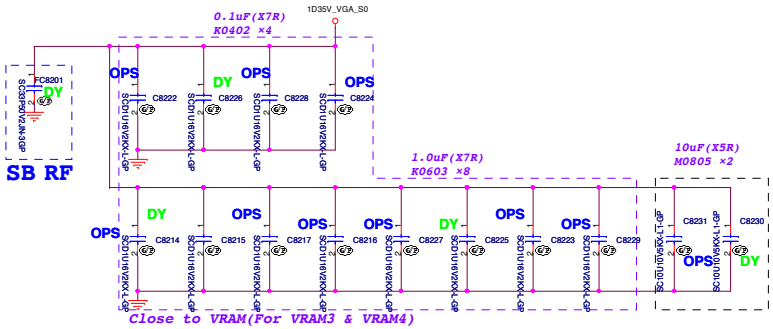
VRAM BOM CTRL

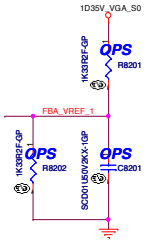
10/23 VRAM1~VRAM8 改Part Number 72.05463.D0U



72.05463.D0U

VRAM BOM CTRL





08/18 C7915, C7921, C7926 Change to DY

08/18 C7914, C7917, C7918, C7919 ,C7920, C7925 Change to VRAM_8PCS

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM3,4 (2/4)***

Size	Document Number	Rev
A2	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 82 of 102

Data Bits 63:32 RANK 0

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM5.6 (3/4)***

Size	Document Number	Rev
A2	**Tesla SKL-U**	-1

Date: Tuesday, July 21, 2015 Sheet 83 of 102

BOM1

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Title: ***VRAM7,8 (4/4)***

Size	Document Number	Rev
A2	**Tesla SKL-U**	-1

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	Main source	2nd source
PU8202 PU8204	084.06970.0037	84.03660.037
PU8203 PU8205	084.06970.0037	84.03660.037

06/30 Change PU8202~PU8205 Main Source & 2nd Source

12/17 Change back

12/17 Change back

12/17 Change back

12/17 Change back

SB

SB

07/09 3V3_AON Change to 3V3_MAIN

08/07 N16S-GT & N16V-GM 都為Config B 0.9V

Design Current
= 33.5 A
OCP< 67A

Cyntec. 0.36uH 10*10*4
DCR=1.05mohm
Idc=30A, Isat=60A

68.R3610.20X
2ND = 068.R3610.1001

OPS Change to 084.06970.0037

2nd = 84.03660.037

74.08812.073

GPU BOM CTRL

R1 R2 R3 R4 R5

Nvidia GPU Vreg Strap Table & P/N:

Nvidia GPU Vreg Strap	Table & P/N	
GPU	N15V-GM	N15S-GT
Vreg Mode	Config D	Config B
R1(PR8222	64.27025.6DL	64.20025.L0L
R2(PR8206	64.75015.6DL	64.20025.L0L
R3(PR8208	63.R0034.1DL	64.20015.6DL
R4(PR8209	64.62015.6DL	64.18025.6DL
R5(PR8204	64.17415.6DL	63.R0034.1DL
C(PC8223)	78.56222.2FL	78.27224.2FL

GM108 SKU	
Item	N16S-GT-B/S
Device ID	0x1347
Package	GB4B-128/GB2B-64
Internal P/N	GM108-755/655,28nm
ROM_SI	Refer to GM108 RAM Straps
ROM_SO	0x0000, 4.99Kohm pull down
ROM_SCLK	0x0 for Optimus, 4.99Kohm pull down
Strap0	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)
Strap1	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
Strap2	
Strap3	
Strap4	
Open_VRG SKU	B
NVVDD Boot Voltage	0.9V

GK208s SKU	
Item	N16V-GM-S
Device ID	0X1299
Package	GB2-64
Internal P/N	GK208-620,28nm
ROM_SI	Refer to GK208s RAM Straps
ROM_SO	0x8, 5K pull up for Optimus/0x9 ,10K Pull Up for Discrete SKU
ROM_SCLK	0x1000,0x8, 4.99Kohm pull up
Strap0	User Strap, 0xF, 45kohm pull up
Strap1	3OIO_PAD_Config, 0x7, 45kohm pull down
Strap2	Device_ID, 0x1001_ 10Kohm pull UP
Strap3	0x0 for Optimus, 5kohm pull low
Strap4	0x0111, 45kohm pull down (PCIE_SPEED_CHANGE=)1
Open_VRG SKU	Config B[PSI not supported]
NVVDD Boot Voltage	0.9V

07/09 3V3_AON Change to 3V3_MAIN

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU CORE

Size: Custom | Document Number: Tesla SKL-U | Rev: -1

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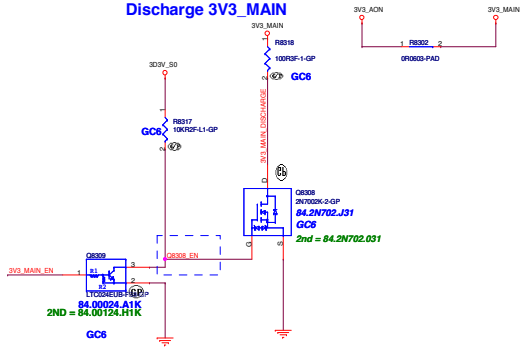
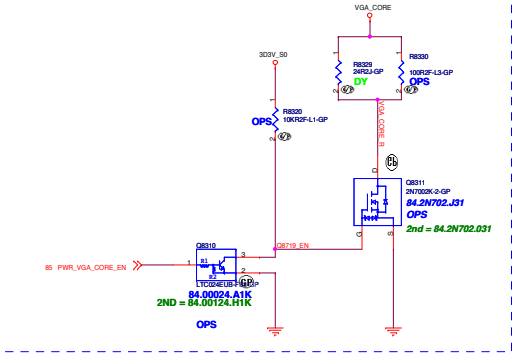
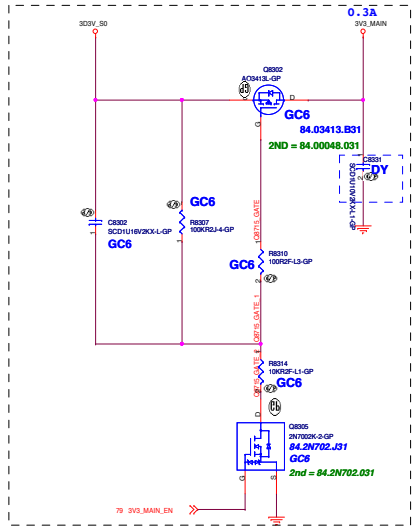
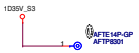
Discharge 3V3_MAIN

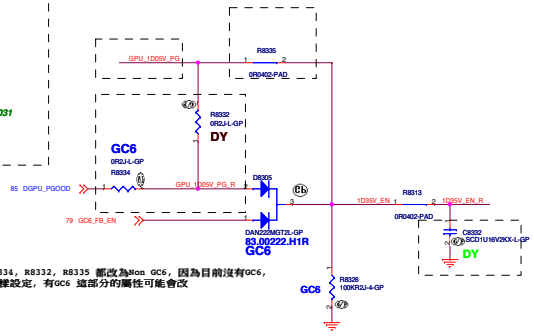


Discharge VGA_CORE

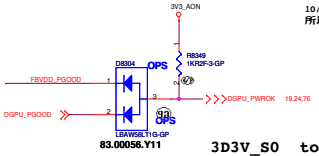






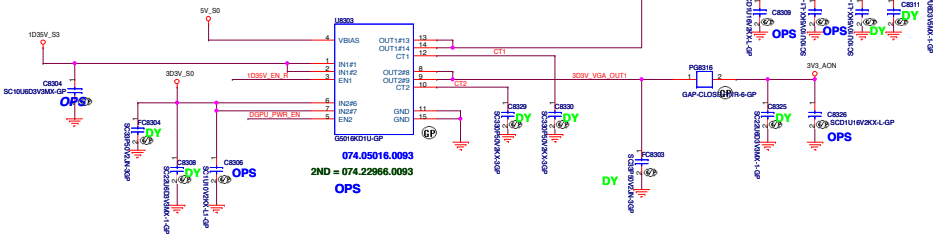


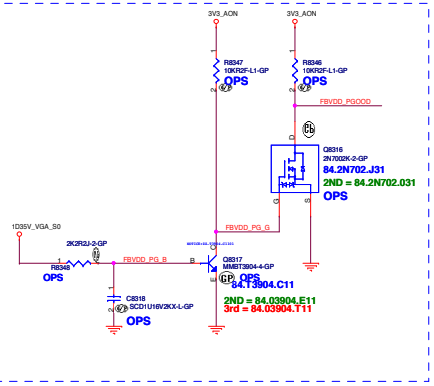
10/21 R8334, R8332, R8335 都改為Non GC6，因為目前沒有GC6，所以先這樣設定，有GC6 這部分的屬性可能會改

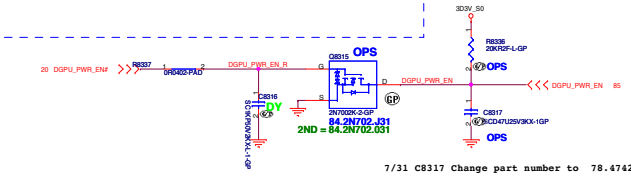


10/14 R8332 原本屬性為Non GC6，改為DY，因為Sequence有問題，
多一組線路用1D05V_VGA_S0來控制1D35V_EN
(如果要上GC6的元件，上件部分要重新做，多一組線路是FOR Non GC6的)

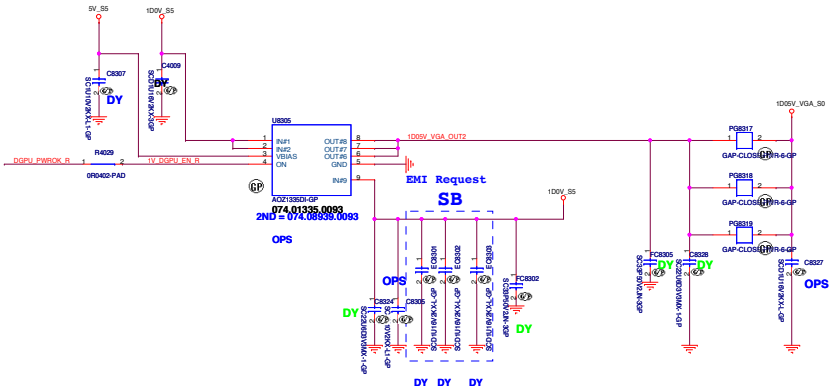
3D3V_S0 to 3V3_AON
1D05V_VTT to 1D05V_VGA_S0

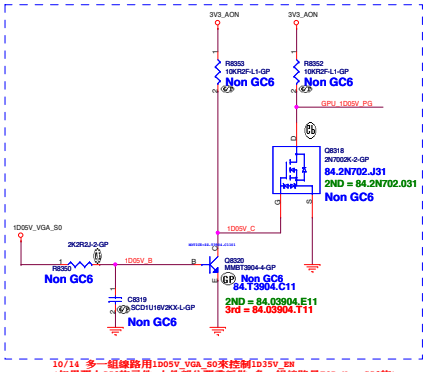






7/31 C8317 Change part number to 78.47422.5BL(0402 to 0603)





10/14 多一組線路用1D05V_VGA_S0來控制1D35V_EN
(如果要上GC6的元件，上件部分要重新做，多一組線路是FOR Non GC6的)
10/21 R8350, C8319, Q8320, Q8318, R8353, R8352 Change to DY
(原本為Non GC6)

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Discrete Power

Size: Custom | Document Number: Tesla SKL-U | Rev: -1

Date: Tuesday, July 21, 2015 | Sheet 86 of 102

(Blanking)

BOM1

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Title: *Reserved*

Size	Document Number	Rev
A3	Tesla SKL-U	-1

Date: Tuesday, July 21, 2015 Sheet 87 of 102

(Blanking)

BOM1

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Title: ***Reserved***

Size	Document Number	Rev
A3	**Tesla SKL-U**	-1

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Structure boss

H6 HOLET315B315X315R237-S-1-GP — ZZ.SCREW.H21 (GP)

H8 HOLET315B315X315R237-S-1-GP — ZZ.SCREW.H21 (GP)

H9 HOLET237B315X315R91-S-GP-U2 — ZZ.00PAD.591 (CL)

H12 HOLE237X189R103-S-GP — ZZ.SCREW.I21 (GP)

H13 HOLE237R158-GP — ZZ.0HOLE.011 (GP)

H18 HOLE237R158-GP — ZZ.0HOLE.011 (GP)

Stand off

H14 STF236R128H88-GP — 34.4LY03.001 — 1st = 34.4LY03.201

07/29 H3 Change to OPS

CPU

H1 STF237R128H42-GP	H2 STF237R128H42-GP	H4 STF237R128H42-GP
34.4GD01.101	34.4GD01.101	34.4GD01.101
1ST = 34.4WZ01.001	1ST = 34.4WZ01.001	1ST = 34.4WZ01.001
2nd = 34.4WZ01.101	2nd = 34.4WZ01.101	2nd = 34.4WZ01.101

GPU

H3 STF237R128H42-GP	H5 STF237R128H42-GP
OPS	OPS
34.4GD01.101	34.4GD01.101
1st = 34.4WZ01.001	1st = 34.4WZ01.001
2nd = 34.4WZ01.101	2nd = 34.4WZ01.101

CL02 CL03 CL04 CL05 CL06 CL07 CL08 CL09 CL10 CL11 CL12 CL13 SPRING-166-GP — 34.41L50.001

Clip change to 434.03N0G.0001

DCBATOUT: EC8601 EC8602 EC8603 EC8607 (SCD1U50V3KX-GP / SCD1U50V2ZX-1GP-U)

DCBATOUT: EC8604 EC8605 EC8606 EC8609 EC8610 EC8611 (SCD1U50V2ZX-1GP-U)

VCC_CORE: RFC8911 RFC8912 RFC8913 RFC8914 RFC8915 (SC8F250V2CC-GP)

1D35V_S3: RFC8920 RFC8916 RFC8917 RFC8918 RFC8919 RFC8921 RFC8922 (SC8F250V2CC-GP)

3D3V_S5: EC8612 EC8613 EC8614 (SCD1U25V3KX-GP); EC8615 EC8907 (SC8F250V2AN-1-GP); EC8908 (SCD1U10V2KX-1GP)

5V_S5: EC8614 EC8615 EC8907 EC8908

3D3V_S0: EC8616 EC8617 (SCD1U25V3KX-GP)

VGA_CORE: EC8901 EC8902 EC8903 EC8904 (SC8F250V2JN-1-GP)

+VCCGT: EC8905 EC8906 (SC8F250V2JN-1-GP)

5V_S0: EC8909 EC8910 (SC8F250V2JN-1-GP)

1D0V_S5: RFC8927 RFC8923 RFC8924 RFC8925 RFC8926 (SC8F250V2CC-GP)

+VCCSA: RFC8928 (SC8F250V2CC-GP)

1D35V_VGA_S0: RFC8935 RFC8931 RFC8933 RFC8932 RFC8934 RFC8929 RFC8930 (SC8F250V2CC-GP)

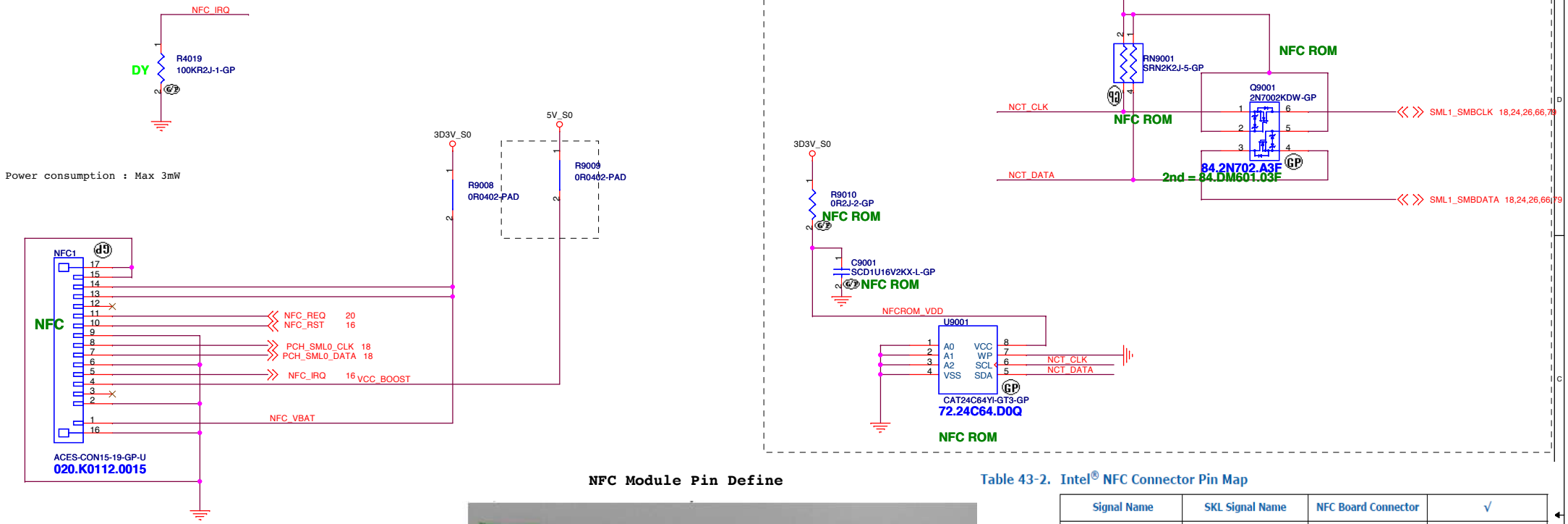
BOM1

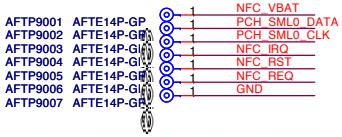
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size: A2 | Document Number: Tesla SKL-U | Rev: -1

Date: Thursday, August 13, 2015 | Sheet 89 of 102





NFC Module Pin Define

Pin#	Pin Name	Type	Refer	Description
1	VBAT	power	3.3V	Power supply voltage
2	GND	Power	GND	Ground
3	SWP	IO	-	SIM Card data
4	VCC_BOOST	Power	5V	Booster supply
5	IRQ	O	PVDD	Interrupt
6	PMUVCC	Power	connect to outside SE power or GND (no SE)	UICC power input from external PMU
7	I2C_SDA	I/O	PVDD	I2C Serial Data Line
8	I2C_SCL	I/O	PVDD	I2C Serial Clock Line
9	GND	Power	GND	Ground
10	VEN	I	GPIO Control (Normal 3.3V)	Enable/ disable LDO regulator / Reset
11	DWL_REQ	I	GPIO Control (Normal 0V)	Firmware download control pin
12	SIMVCC	Power	1.8V or N.C	Power output to supply the UICC
13	VBAT	Power	3.3V	Power supply voltage
14	PVDD	Power	3.3V	Pad supply voltage
15	GND	Power	GND	Ground

Suggestion Host Pin define (Use Sinbon FFC A9152420)

Pin#	Pin Name
15	VBAT
14	GND
13	SWP
12	VCC_BOOST
11	IRQ
10	PMUVCC
9	I2C_SDA
8	I2C_SCL
7	GND
6	VEN
5	DWL_REQ
4	SIMVCC
3	VBAT
2	PVDD
1	GND

Table 43-2. Intel® NFC Connector Pin Map

Signal Name	SKL Signal Name	NFC Board Connector	√
GND		Pin 1	
NFC_VDD_IO		Pin 2	+V3.3A
NFC_MOD_VDD		Pin 3	+V3.3A
NFC_SWP_PWR_RSVD		Pin 4	
NFC_DFU	GPP_B15/GSPIO0_CS#	Pin 5	NFC Device FW update
NFC_RESET	**SKL U:** GPP_E4/DEVSLP0 **SKL Y:** GPP_E6/DEVSLP2	Pin 6	NFC Reset
GND		Pin 7	
NFC_SM_CK	SML0_CLK	Pin 8	SMLINK CLK
NFC_SM_DATA	SML0_DATA	Pin 9	SMLINK DATA
SWP_PWR		Pin 10	Route to test point
NFC_IRQ	GPP_E12/USB2_OC3#	Pin 11	NFC IRQ
VCC_ANTENNA_BOOST		Pin 12	Antenna Booster: +5VA
Reserved		Pin 13	
GND		Pin 14	
NFC_MOD_VDD		Pin 15	

Note: Refer to Figure 43-9 for details on NFC module to board connector.

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SSID = Finger Print

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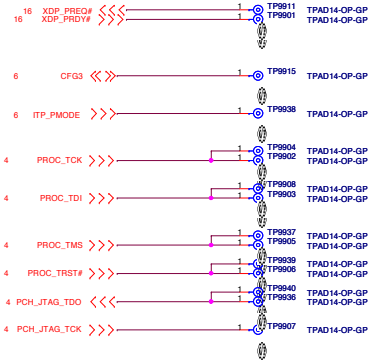

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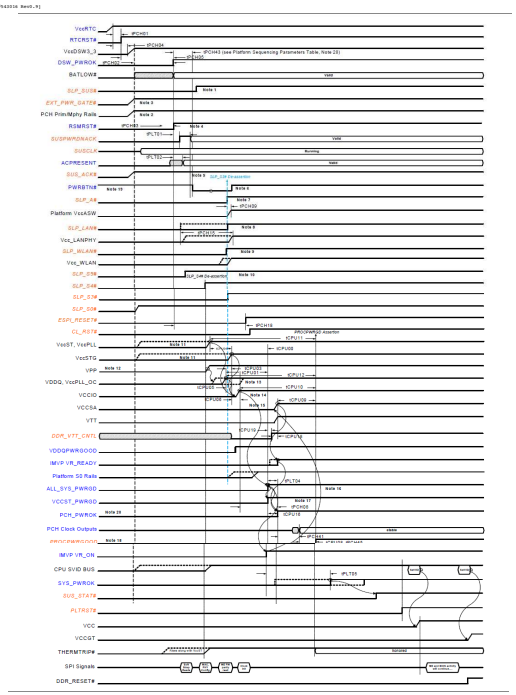
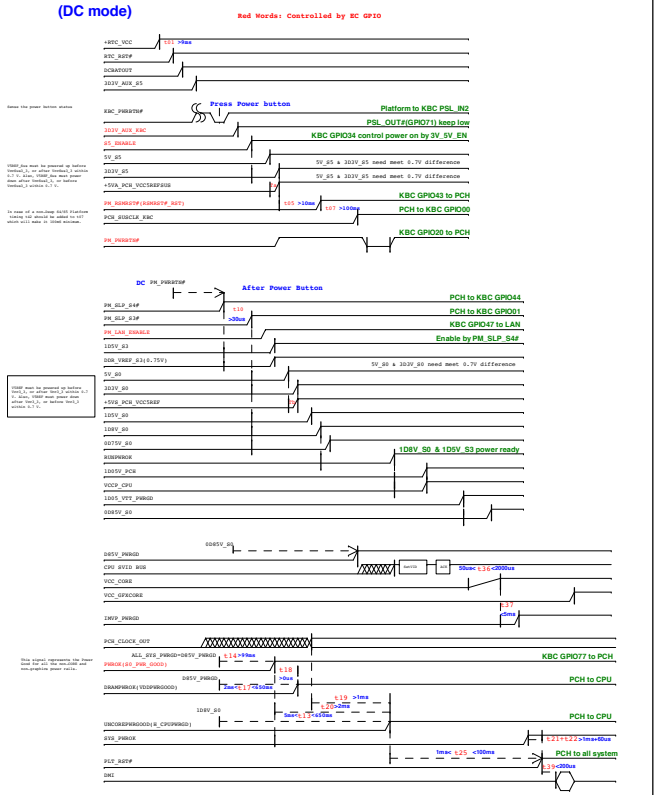
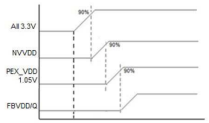
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



(DC mode)



[dGPU] N16x Power-Up/Down Sequence



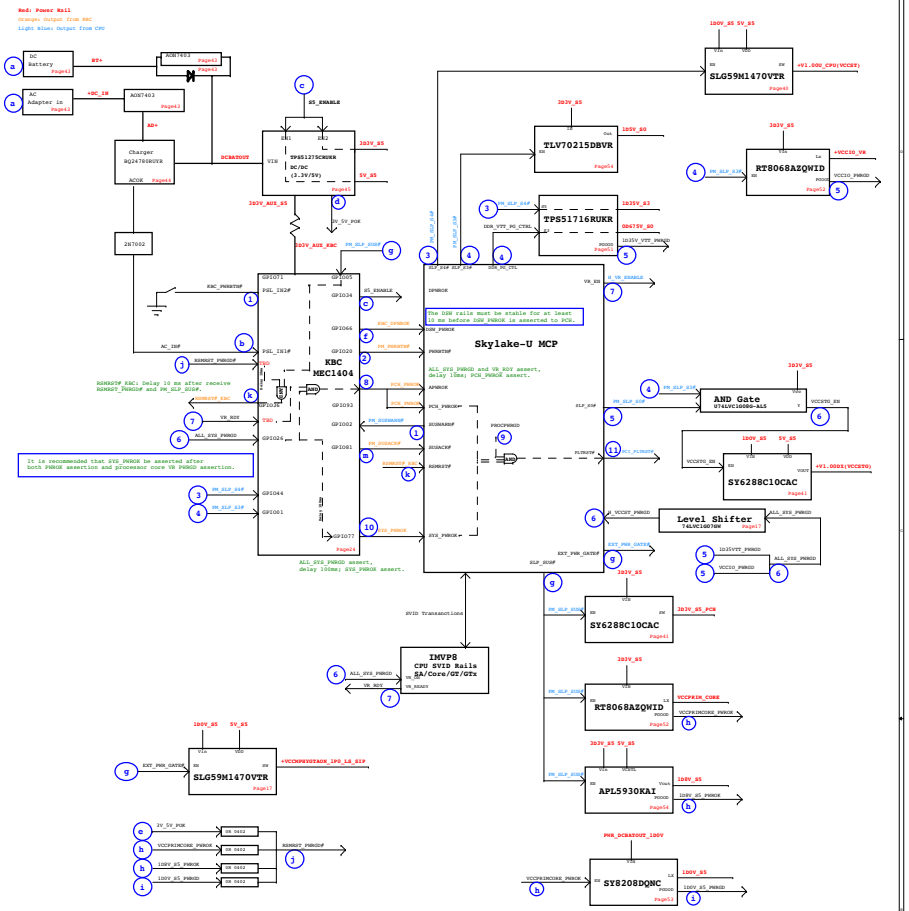
Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

> Note:
> - The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
> - The ramp up overshoot should not exceed the silicon reliability limit voltage.
> - The previous power rail must ramp up to 90% before the next power rail can start ramping up.
> - No signal should be applied to the GPU before the power rails are fully ramped
> - Refer to the JEDEC Memory Specification for memory related power sequencing.
> - The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

Skylake POWER UP SEQUENCE DIAGRAM



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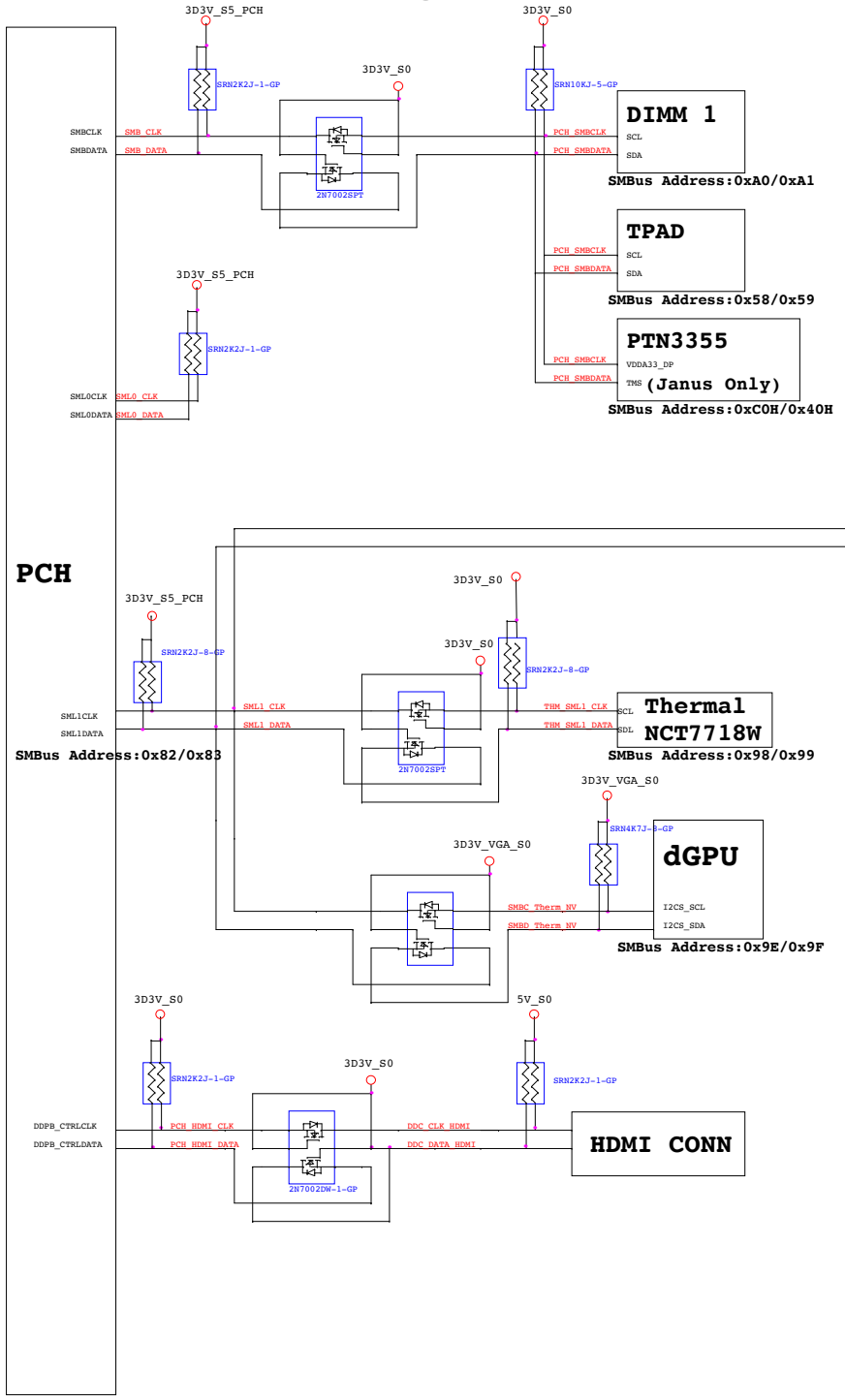
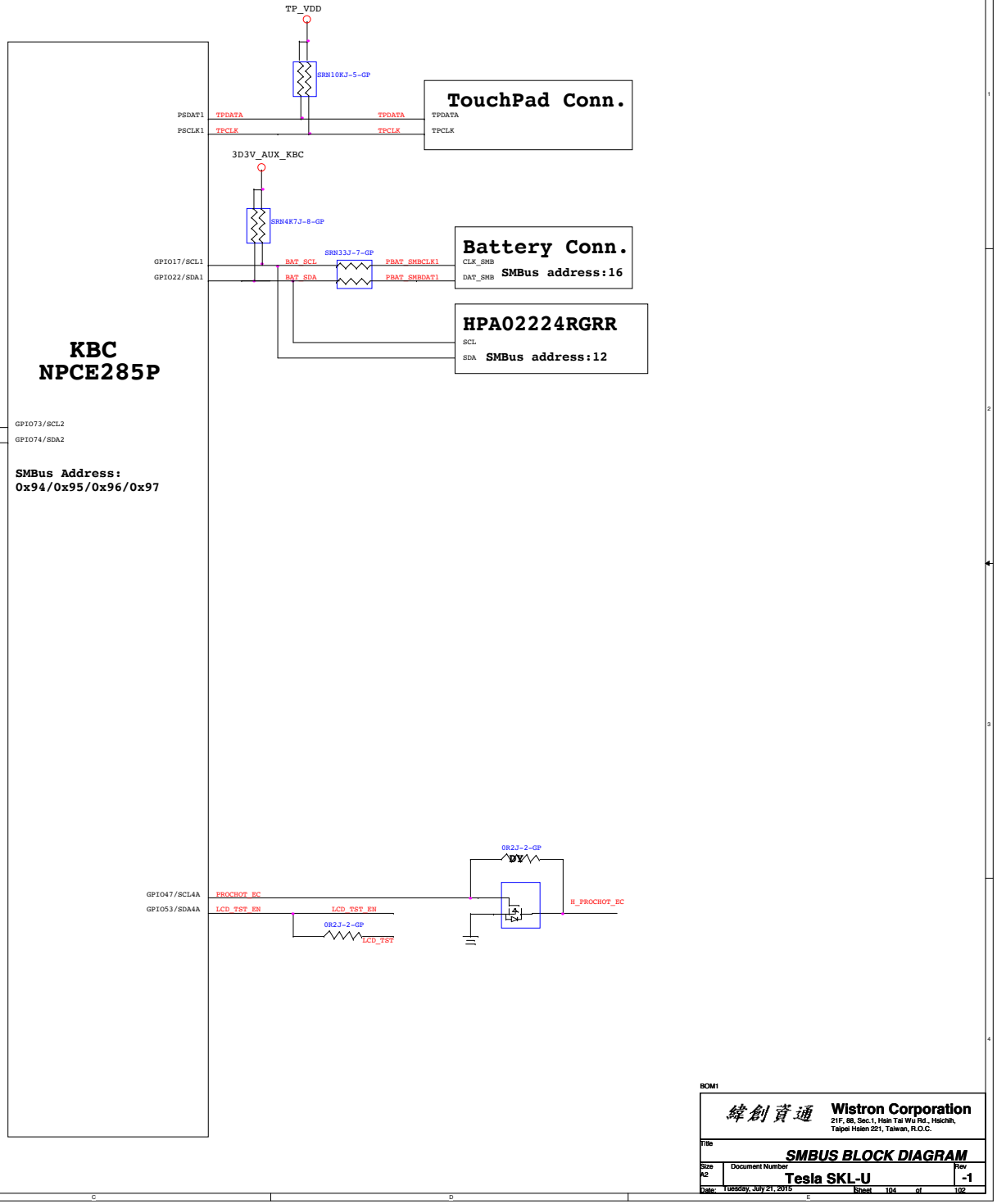
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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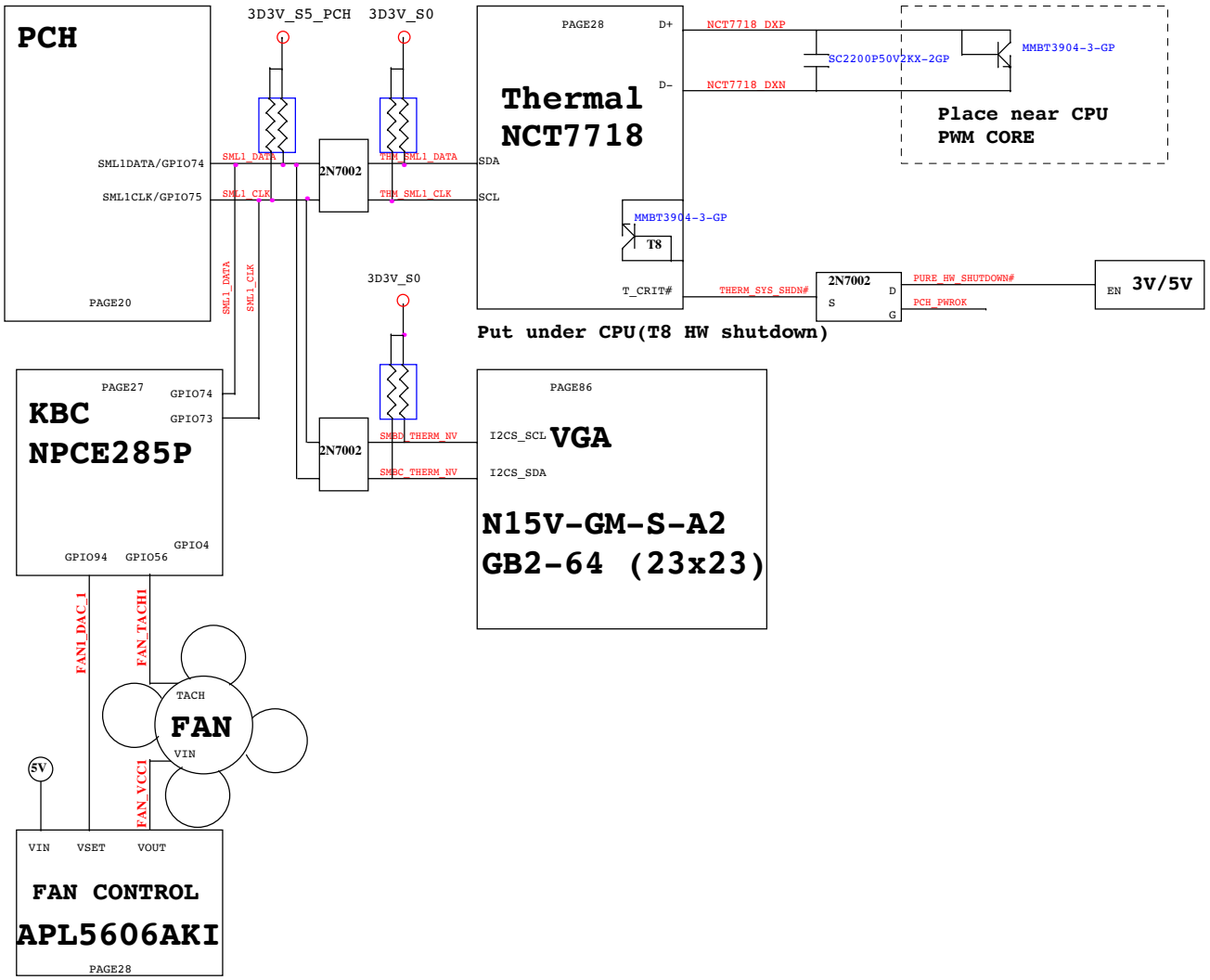
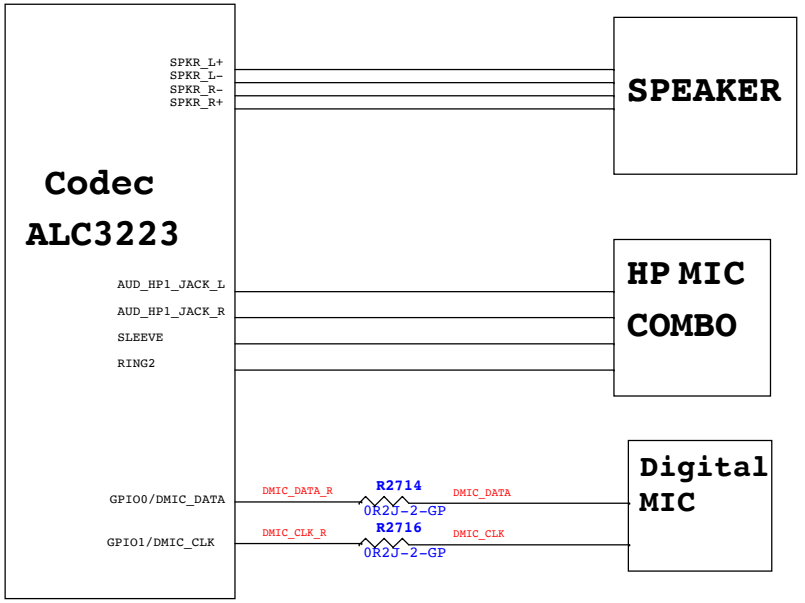
Thermal Block Diagram



Audio Block Diagram



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Title	THERMAL/AUDIO BLOCK DIAGRAM	
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