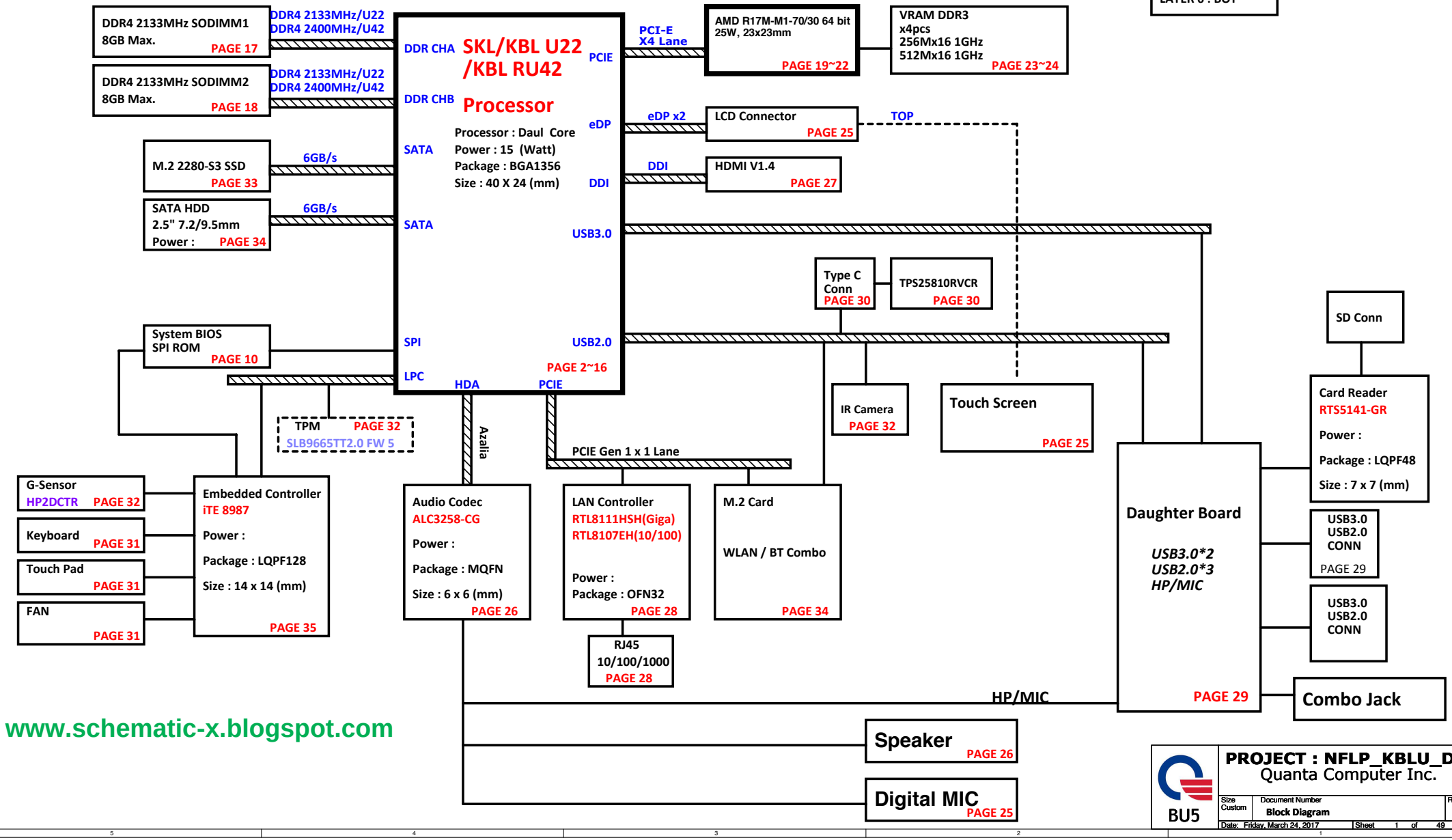
NFL_1SPD DIS (14/15")
Intel SKL/KBL ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT



BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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+3V 4,10,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41,48
+1.0V 4,6,35,40
+VCCSTPLL 4,5,6,9,40,41

HDMI

U1A — SKL_ULT ? — Need apply PN

Justsurport FHD 1920x1080

27 IN_D2# → IN_D2# → E55 DDI1_TXN[0]
27 IN_D2 → IN_D2 → F55 DDI1_TXP[0]
27 IN_D1# → IN_D1# → E58 DDI1_TXN[1]
27 IN_D1 → IN_D1 → F58 DDI1_TXP[1]
27 IN_D0# → IN_D0# → F53 DDI1_TXN[2]
27 IN_D0 → IN_D0 → G53 DDI1_TXP[2]
27 IN_CLK# → IN_CLK# → F56 DDI1_TXN[3]
27 IN_CLK → IN_CLK → G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI — EDP — DISPLAY SIDEBANDS

27 SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
27 SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

TP2 1 DDPC_CTRLDATA → N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA

TP3 1 DDPD_CTRLDATA → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO — R3 24.9_1%_4 — EDP_RCOMP → E52 EDP_RCOMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 25
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 25
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 25
EDP_TXP[1] C45 INT_EDP_TXP1 → INT_EDP_TXP1 25
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN 25
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP 25

EDP_DISP_UTIL B52 EDP_DISP_UTIL → TP1

DDI1_AUXN G50
DDI1_AUXP C50
DDI2_AUXN F48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E13/DDPB_HPD0 L9 HDMI_HPD_CON → HDMI_HPD_CON 27
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L5
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 ULT_EDP_HPD → ULT_EDP_HPD 25

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON 25
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM 25
EDP_VDDEN U13 PCH_DISP_ON → PCH_DISP_ON 25

*SKL_ULT
REV = 1
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?

Reserve EDP_HPD opposites circuit!

+3V — R1 *10K/F_4 — ULT_EDP_HPD — R2 100K_4

U1D — SKL_ULT ? — Need apply PN

35,41 H_PROCHOT# → R4 499/F_4 → CATERR# D63
35 EC_PECI → EC_PECI A54 PECI
PROCHOT# C65 PROCHOT#
35 PM_THRMTRIP# → PM_THRMTRIP# C63 THERMTRIP#
A65 SKTOCC#

CPU MISC

TP127 1 XDP_BPM0 → C55 BPM#[0]
TP128 1 XDP_BPM1 → D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

TP5 1 CPU_GP2 → A6 GPP_E3/CPU_GP0
TP6 1 CPU_GP3 → A7 GPP_E7/CPU_GP1
BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3

R8 49.9/F_4 PROC_POPIRCOMP → AT16 PROC_POPIRCOMP
R11 49.9/F_4 PCH_OPI_RCOMP → AU16 PCH_OPIRCOMP
R12 49.9/F_4 EDRAM_OPIO_RCOMP → H66 OPCE_RCOMP
R14 49.9/F_4 EOPIO_RCOMP → H65 OPC_RCOMP

JTAG

PROC_TCK B61 XDP_TCK0
PROC_TDI D60 XDP_TDI_CPU 1 → TP999
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU 1 → TP998
PROC_TRST# B59 PROC_TRST#

PCH_JTAG_TCK B56 JTAG_TCK_PCH
PCH_JTAG_TDI D59 JTAG_TDI_PCH
PCH_JTAG_TDO A56 JTAG_TDO_PCH
PCH_JTAG_TMS C59 JTAG_TMS_PCH
PCH_TRST# C61 XDP_TRST#_CPU
JTAGX A59 JTAGX_PCH

XDP_TRST#_CPU R863 0_4 PROC_TRST#

*SKL_ULT
REV = 1
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?

+VCCSTPLL — R6 *49.9/F_4 — CATERR#

+1.0V — R9 *0_4/S — R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset

Close to EC

+VCCSTPLL — PM_THRMTRIP# — R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/15 (eDP/DDI)	1A
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SkyLake ULT Processor (DDR4)

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.2VSUS 6,17,18,38,40

Need apply PN

U1B — SKL_ULT

M_A_DQ0	AL71	DDR0_DQ[0]	DDR0_CKN[0]	AU53	M_A_CLKN0 17
M_A_DQ1	AL68	DDR0_DQ[1]	DDR0_CKP[0]	AT53	M_A_CLKP0 17
M_A_DQ2	AN68	DDR0_DQ[2]	DDR0_CKN[1]	AU55	M_A_CLKN1 17
M_A_DQ3	AN69	DDR0_DQ[3]	DDR0_CKP[1]	AT55	M_A_CLKP1 17
M_A_DQ4	AL70	DDR0_DQ[4]	DDR0_CKE[0]	BA56	M_A_CKE0 17
M_A_DQ5	AL69	DDR0_DQ[5]	DDR0_CKE[1]	BB56	M_A_CKE1 17
M_A_DQ6	AN70	DDR0_DQ[6]	DDR0_CKE[2]	AW56	
M_A_DQ7	AN71	DDR0_DQ[7]	DDR0_CKE[3]	AY56	
M_A_DQ8	AR70	DDR0_DQ[8]	DDR0_CS#[0]	AU45	M_A_CS#0 17
M_A_DQ9	AR68	DDR0_DQ[9]	DDR0_CS#[1]	AU43	M_A_CS#1 17
M_A_DQ10	AU71	DDR0_DQ[10]	DDR0_ODT[0]	AT45	M_A_DIM0_ODT0 17
M_A_DQ11	AU68	DDR0_DQ[11]	DDR0_ODT[1]	AT43	M_A_DIM0_ODT1 17
M_A_DQ12	AT71	DDR0_DQ[12]			
M_A_DQ13	AR69	DDR0_DQ[13]	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BA51	M_A_A5
M_A_DQ14	AU70	DDR0_DQ[14]	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BB54	M_A_A9
M_A_DQ15	AU69	DDR0_DQ[15]	DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	BA52	M_A_A6
M_B_DQ0	AF64	DDR1_DQ[0]/DDR0_DQ[16]	DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AY52	M_A_A8
M_B_DQ1	AF64	DDR1_DQ[1]/DDR0_DQ[17]	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AW52	M_A_A7
M_B_DQ2	AK65	DDR1_DQ[2]/DDR0_DQ[18]	DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AV55	M_A_BG#0
M_B_DQ3	AK64	DDR1_DQ[3]/DDR0_DQ[19]	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	AW54	M_A_A12
M_B_DQ4	AF66	DDR1_DQ[4]/DDR0_DQ[20]	DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA54	M_A_A11
M_B_DQ5	AF67	DDR1_DQ[5]/DDR0_DQ[21]	DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	BA55	
M_B_DQ6	AK67	DDR1_DQ[6]/DDR0_DQ[22]	DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]	AY54	
M_B_DQ7	AK66	DDR1_DQ[7]/DDR0_DQ[23]			
M_B_DQ8	AF70	DDR1_DQ[8]/DDR0_DQ[24]	DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	BA46	M_A_A13
M_B_DQ9	AF68	DDR1_DQ[9]/DDR0_DQ[25]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AU48	M_A_CAS#
M_B_DQ10	AH71	DDR1_DQ[10]/DDR0_DQ[26]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AT46	M_A_WE#
M_B_DQ11	AH68	DDR1_DQ[11]/DDR0_DQ[27]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU50	M_A_RAS#
M_B_DQ12	AF71	DDR1_DQ[12]/DDR0_DQ[28]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AU52	M_A_BS#0
M_B_DQ13	AF69	DDR1_DQ[13]/DDR0_DQ[29]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AY51	M_A_A2
M_B_DQ14	AH70	DDR1_DQ[14]/DDR0_DQ[30]	DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT48	M_A_BS#1
M_B_DQ15	AH69	DDR1_DQ[15]/DDR0_DQ[31]	DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	AT50	M_A_A10
M_A_DQ16	BB65	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	BB50	M_A_A1
M_A_DQ17	AW65	DDR0_DQ[17]/DDR0_DQ[33]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AY50	M_A_A0
M_A_DQ18	AW63	DDR0_DQ[18]/DDR0_DQ[34]	DDR0_MA[3]	BA50	M_A_A3
M_A_DQ19	AY63	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_MA[4]	BB52	M_A_A4
M_A_DQ20	BA65	DDR0_DQ[20]/DDR0_DQ[36]			
M_A_DQ21	AY65	DDR0_DQ[21]/DDR0_DQ[37]	DDR0_DQSN[0]	AM70	M_A_DQSN0
M_A_DQ22	BA63	DDR0_DQ[22]/DDR0_DQ[38]	DDR0_DQSP[0]	AM69	M_A_DQSP0
M_A_DQ23	BB63	DDR0_DQ[23]/DDR0_DQ[39]	DDR0_DQSN[1]	AT69	M_A_DQSN1
M_A_DQ24	BA61	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_DQSP[1]	AT70	M_A_DQSP1
M_A_DQ25	AW61	DDR0_DQ[25]/DDR0_DQ[41]	DDR1_DQSN[0]/DDR0_DQSN[2]	AH66	M_B_DQSN0
M_A_DQ26	BB59	DDR0_DQ[26]/DDR0_DQ[42]	DDR1_DQSP[0]/DDR0_DQSP[2]	AH65	M_B_DQSP0
M_A_DQ27	AW59	DDR0_DQ[27]/DDR0_DQ[43]	DDR1_DQSN[1]/DDR0_DQSN[3]	AG69	M_B_DQSN1
M_A_DQ28	BB61	DDR0_DQ[28]/DDR0_DQ[44]	DDR1_DQSP[1]/DDR0_DQSP[3]	AG70	M_B_DQSP1
M_A_DQ29	AY61	DDR0_DQ[29]/DDR0_DQ[45]	DDR0_DQSN[2]/DDR0_DQSN[4]	BA64	M_A_DQSN2
M_A_DQ30	BA59	DDR0_DQ[30]/DDR0_DQ[46]	DDR0_DQSP[2]/DDR0_DQSP[4]	AY64	M_A_DQSP2
M_A_DQ31	AY59	DDR0_DQ[31]/DDR0_DQ[47]	DDR0_DQSN[3]/DDR0_DQSN[5]	AY60	M_A_DQSN3
M_B_DQ16	AT66	DDR1_DQ[16]/DDR0_DQ[48]	DDR0_DQSP[3]/DDR0_DQSP[5]	BA60	M_A_DQSP3
M_B_DQ17	AU66	DDR1_DQ[17]/DDR0_DQ[49]	DDR1_DQSN[2]/DDR0_DQSN[6]	AR66	M_B_DQSN2
M_B_DQ18	AP65	DDR1_DQ[18]/DDR0_DQ[50]	DDR1_DQSP[2]/DDR0_DQSP[6]	AR65	M_B_DQSP2
M_B_DQ19	AN65	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_DQSN[3]/DDR0_DQSN[7]	AR61	M_B_DQSN3
M_B_DQ20	AN66	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_DQSP[3]/DDR0_DQSP[7]	AR60	M_B_DQSP3
M_B_DQ21	AP66	DDR1_DQ[21]/DDR0_DQ[53]			
M_B_DQ22	AT65	DDR1_DQ[22]/DDR0_DQ[54]	DDR0_ALERT#	AW50	M_A_ALERT#
M_B_DQ23	AU65	DDR1_DQ[23]/DDR0_DQ[55]	DDR0_PAR	AT52	M_A_PARITY
M_B_DQ24	AT61	DDR1_DQ[24]/DDR0_DQ[56]			
M_B_DQ25	AU61	DDR1_DQ[25]/DDR0_DQ[57]	DDR_VREF_CA	AY67	SM_VREF
M_B_DQ26	AP60	DDR1_DQ[26]/DDR0_DQ[58]	DDR0_VREF_DQ	BA67	SMDDR_VREF_DQ1_M3
M_B_DQ27	AN60	DDR1_DQ[27]/DDR0_DQ[59]	DDR1_VREF_DQ		
M_B_DQ28	AN61	DDR1_DQ[28]/DDR0_DQ[60]			
M_B_DQ29	AP61	DDR1_DQ[29]/DDR0_DQ[61]	DDR_VTT_CNTL	AW67	DDR_VTT_CNTL
M_B_DQ30	AT60	DDR1_DQ[30]/DDR0_DQ[62]			
M_B_DQ31	AU60	DDR1_DQ[31]/DDR0_DQ[63]			

NIL-DDR CH - A

M_A_ALERT# 17
M_A_PARITY 17
SM_VREF 17
TP7
SMDDR_VREF_DQ1_M3 18
DDR_VTT_CNTL 18

20mils width

*SKL_ULT
REV = 1
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U1C — SKL_ULT

Need apply PN

M_A_DQ32	AY39	DDR0_DQ[32]/DDR1_DQ[0]	DDR1_CKN[0]	AN45	M_B_CLKN0 18
M_A_DQ33	AW39	DDR0_DQ[33]/DDR1_DQ[1]	DDR1_CKN[1]	AN46	M_B_CLKN1 18
M_A_DQ34	AY37	DDR0_DQ[34]/DDR1_DQ[2]	DDR1_CKP[0]	AP45	M_B_CLKP0 18
M_A_DQ35	AW37	DDR0_DQ[35]/DDR1_DQ[3]	DDR1_CKP[1]	AP46	M_B_CLKP1 18
M_A_DQ36	BB39	DDR0_DQ[36]/DDR1_DQ[4]	DDR1_CKE[0]	AN56	M_B_CKE0 18
M_A_DQ37	BA39	DDR0_DQ[37]/DDR1_DQ[5]	DDR1_CKE[1]	AP55	M_B_CKE1 18
M_A_DQ38	BA37	DDR0_DQ[38]/DDR1_DQ[6]	DDR1_CKE[2]	AN55	
M_A_DQ39	BB37	DDR0_DQ[39]/DDR1_DQ[7]	DDR1_CKE[3]	AP53	
M_A_DQ40	AY35	DDR0_DQ[40]/DDR1_DQ[8]	DDR1_CS#[0]	BB42	M_B_CS#0 18
M_A_DQ41	AW35	DDR0_DQ[41]/DDR1_DQ[9]	DDR1_CS#[1]	AY42	M_B_CS#1 18
M_A_DQ42	AY33	DDR0_DQ[42]/DDR1_DQ[10]	DDR1_ODT[0]	BA42	M_B_DIM0_ODT0 18
M_A_DQ43	AW33	DDR0_DQ[43]/DDR1_DQ[11]	DDR1_ODT[1]	AW42	M_B_DIM0_ODT1 18
M_A_DQ44	BB35	DDR0_DQ[44]/DDR1_DQ[12]			
M_A_DQ45	BA35	DDR0_DQ[45]/DDR1_DQ[13]	DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	AY48	M_B_A5
M_A_DQ46	BA33	DDR0_DQ[46]/DDR1_DQ[14]	DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	AP50	M_B_A9
M_A_DQ47	BB33	DDR0_DQ[47]/DDR1_DQ[15]	DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	BA48	M_B_A8
M_B_DQ32	AU40	DDR1_DQ[32]/DDR1_DQ[16]	DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	BB48	M_B_A6
M_B_DQ33	AT40	DDR1_DQ[33]/DDR1_DQ[17]	DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	AP48	M_B_A7
M_B_DQ34	AT37	DDR1_DQ[34]/DDR1_DQ[18]	DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]	AP52	M_B_A8
M_B_DQ35	AU37	DDR1_DQ[35]/DDR1_DQ[19]	DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	AN50	M_B_BG#0
M_B_DQ36	AR40	DDR1_DQ[36]/DDR1_DQ[20]	DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	AN48	M_B_A12
M_B_DQ37	AP40	DDR1_DQ[37]/DDR1_DQ[21]	DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	AN53	M_B_A11
M_B_DQ38	AP37	DDR1_DQ[38]/DDR1_DQ[22]	DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]	AN52	M_B_ACT#
M_B_DQ39	AR37	DDR1_DQ[39]/DDR1_DQ[23]			M_B_BG#1
M_B_DQ40	AT33	DDR1_DQ[40]/DDR1_DQ[24]	DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	BA43	M_B_A13
M_B_DQ41	AU33	DDR1_DQ[41]/DDR1_DQ[25]	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AY43	M_B_CAS#
M_B_DQ42	AU30	DDR1_DQ[42]/DDR1_DQ[26]	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AY44	M_B_WE#
M_B_DQ43	AT30	DDR1_DQ[43]/DDR1_DQ[27]	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	AW44	M_B_RAS#
M_B_DQ44	AR33	DDR1_DQ[44]/DDR1_DQ[28]	DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	BB44	M_B_BS#0
M_B_DQ45	AP33	DDR1_DQ[45]/DDR1_DQ[29]	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	AY47	M_B_A2
M_B_DQ46	AR30	DDR1_DQ[46]/DDR1_DQ[30]	DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	BA44	M_B_BS#1
M_B_DQ47	AP30	DDR1_DQ[47]/DDR1_DQ[31]	DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	AW46	M_B_A10
M_A_DQ48	AY31	DDR0_DQ[48]/DDR1_DQ[32]	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	AY46	M_B_A1
M_A_DQ49	AW31	DDR0_DQ[49]/DDR1_DQ[33]	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	BA46	M_B_A0
M_A_DQ50	AY29	DDR0_DQ[50]/DDR1_DQ[34]	DDR1_MA[3]	BB46	M_B_A3
M_A_DQ51	AW29	DDR0_DQ[51]/DDR1_DQ[35]	DDR1_MA[4]	BA47	M_B_A4
M_A_DQ52	BB31	DDR0_DQ[52]/DDR1_DQ[36]			
M_A_DQ53	BA31	DDR0_DQ[53]/DDR1_DQ[37]	DDR0_DQSN[4]/DDR1_DQSN[0]	BA38	M_A_DQSN4
M_A_DQ54	BA29	DDR0_DQ[54]/DDR1_DQ[38]	DDR0_DQSP[4]/DDR1_DQSP[0]	AY38	M_A_DQSP4
M_A_DQ55	BB29	DDR0_DQ[55]/DDR1_DQ[39]	DDR0_DQSN[5]/DDR1_DQSN[1]	AY34	M_A_DQSN5
M_A_DQ56	AY27	DDR0_DQ[56]/DDR1_DQ[40]	DDR0_DQSP[5]/DDR1_DQSP[1]	BA34	M_A_DQSP5
M_A_DQ57	AW27	DDR0_DQ[57]/DDR1_DQ[41]	DDR0_DQSN[6]/DDR1_DQSN[2]	AT38	M_B_DQSN4
M_A_DQ58	AY25	DDR0_DQ[58]/DDR1_DQ[42]	DDR0_DQSP[6]/DDR1_DQSP[2]	AR38	M_B_DQSP4
M_A_DQ59	AW25	DDR0_DQ[59]/DDR1_DQ[43]	DDR0_DQSN[7]/DDR1_DQSN[3]	AT32	M_B_DQSN5
M_A_DQ60	BB27	DDR0_DQ[60]/DDR1_DQ[44]	DDR0_DQSP[7]/DDR1_DQSP[3]	AR32	M_B_DQSP5
M_A_DQ61	BA27	DDR0_DQ[61]/DDR1_DQ[45]		BA30	M_A_DQSN6
M_A_DQ62	BA25	DDR0_DQ[62]/DDR1_DQ[46]		AY30	M_A_DQSP6
M_A_DQ63	BB25	DDR0_DQ[63]/DDR1_DQ[47]		AY26	M_A_DQSN7
M_B_DQ48	AU27	DDR1_DQ[48]		BA26	M_A_DQSP7
M_B_DQ49	AT27	DDR1_DQ[49]		AR25	M_B_DQSN6
M_B_DQ50	AT25	DDR1_DQ[50]		AR27	M_B_DQSP6
M_B_DQ51	AU25	DDR1_DQ[51]		AR22	M_B_DQSN7
M_B_DQ52	AP27	DDR1_DQ[52]		AR21	M_B_DQSP7
M_B_DQ53	AN27	DDR1_DQ[53]			
M_B_DQ54	AN25	DDR1_DQ[54]		AN43	M_B_ALERT#
M_B_DQ55	AP25	DDR1_DQ[55]		AP43	M_B_PARITY
M_B_DQ56	AT22	DDR1_DQ[56]		AT13	SM_DRAMRST#
M_B_DQ57	AU22	DDR1_DQ[57]		AR18	SM_RCOMP_0
M_B_DQ58	AU21	DDR1_DQ[58]		AT18	SM_RCOMP_1
M_B_DQ59	AT21	DDR1_DQ[59]		AU18	SM_RCOMP_2
M_B_DQ60	AN22	DDR1_DQ[60]			
M_B_DQ61	AP22	DDR1_DQ[61]			
M_B_DQ62	AP21	DDR1_DQ[62]			
M_B_DQ63	AN21	DDR1_DQ[63]			

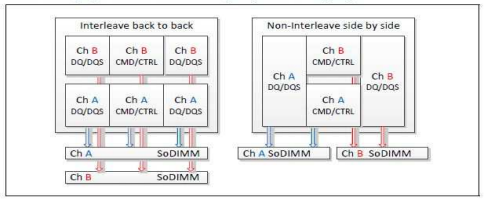
DDR1_ALERT# 18
DDR1_PAR 18
DRAM_RESET# 18
DDR_RCOMP[0]
DDR_RCOMP[1]
DDR_RCOMP[2]

NIL-DDR CH - B

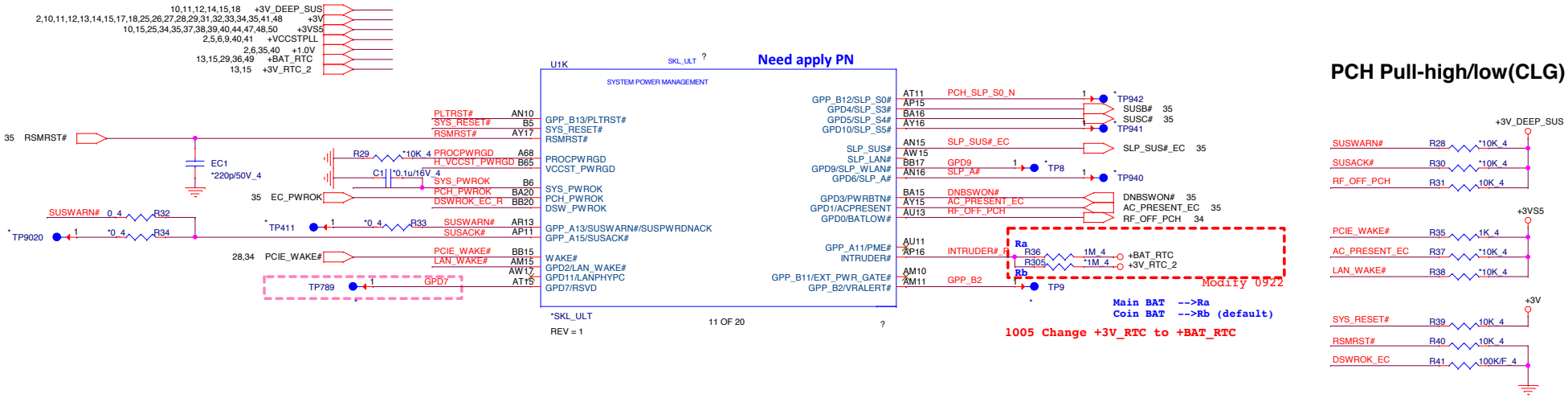
+1.2VSUS
R24 470/F_4
R25 121/F_4
R26 80.6/F_4
R27 100/F_4
DDR3_DRAMRST# 17,18

*SKL_ULT
REV = 1
3 OF 20

Interleave (IL) and Non-Interleave (NIL) Modes Mapping

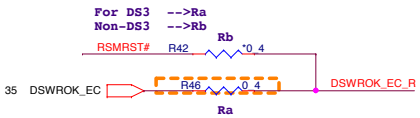


PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size: Custom | Document Number: 03 -- SKYLAKE 2/15(DDR4 I/F) | Rev: 1A
Date: Friday, March 24, 2017 | Sheet 3 of 49



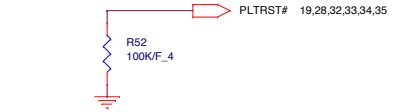
PCH Pull-high/low(CLG)

For DS3 Sequence

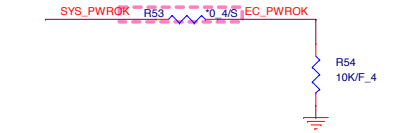


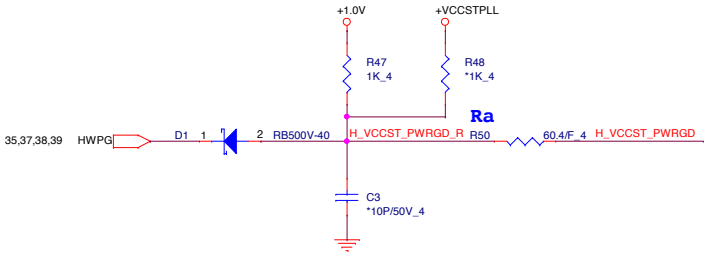
PLTRST#(CLG)

Check Rise/Fall time less than 100ns

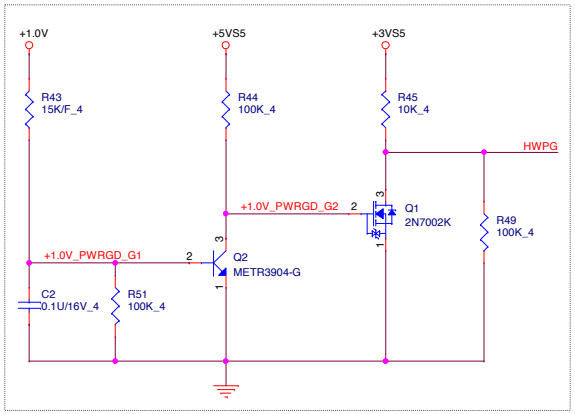


System PWR_OK(CLG)

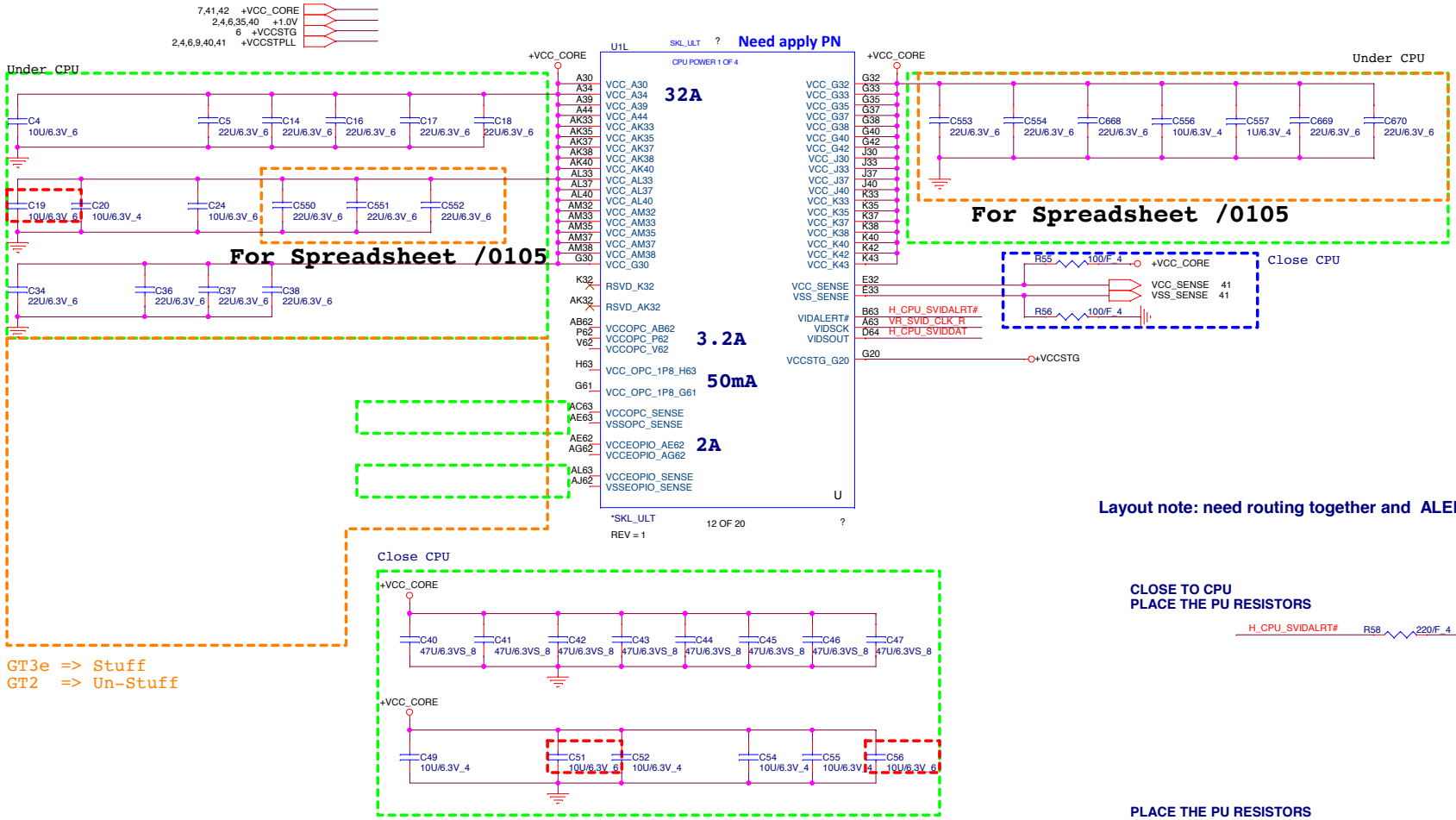


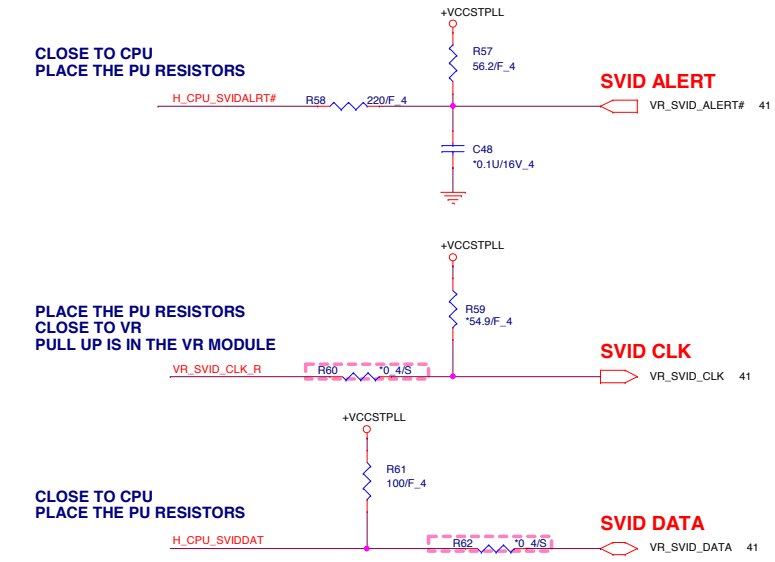


Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size: Custom	Document Number: 04 -- SKYLAKE 3/15(PowerManger)	Rev: 1A
Date: Friday, March 24, 2017	Sheet 4 of 49	





Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYLAKE 4/15 (POWER-1)	1A

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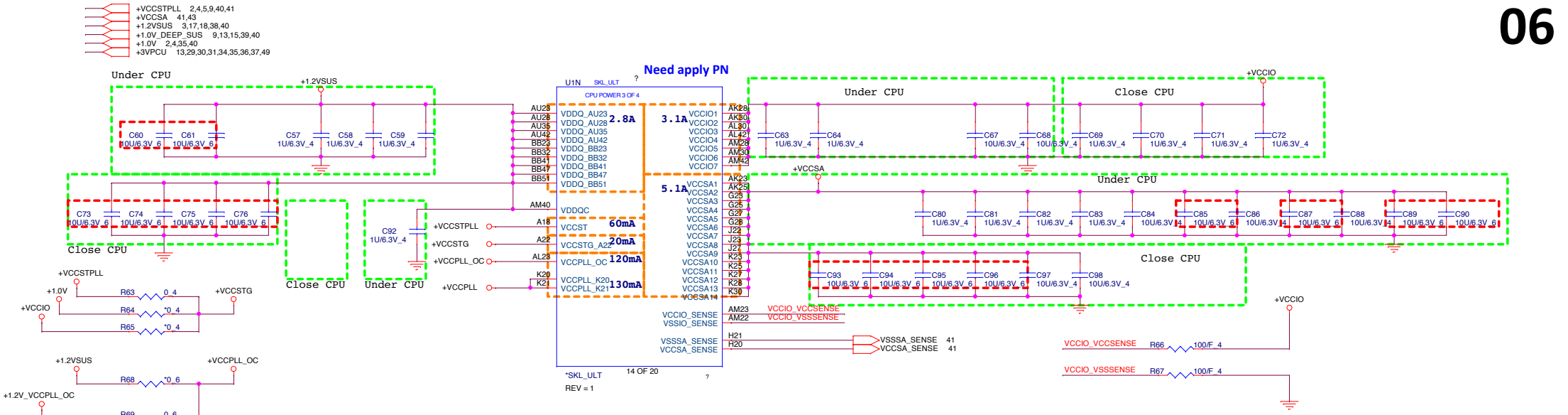
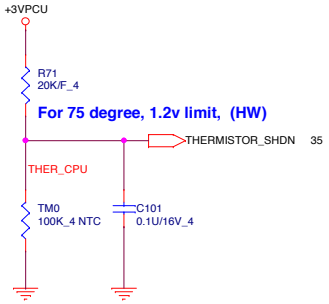
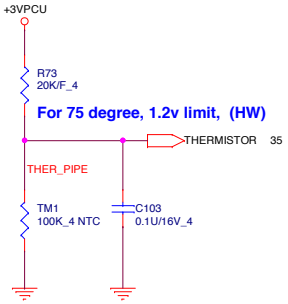


IO Thrm Protect

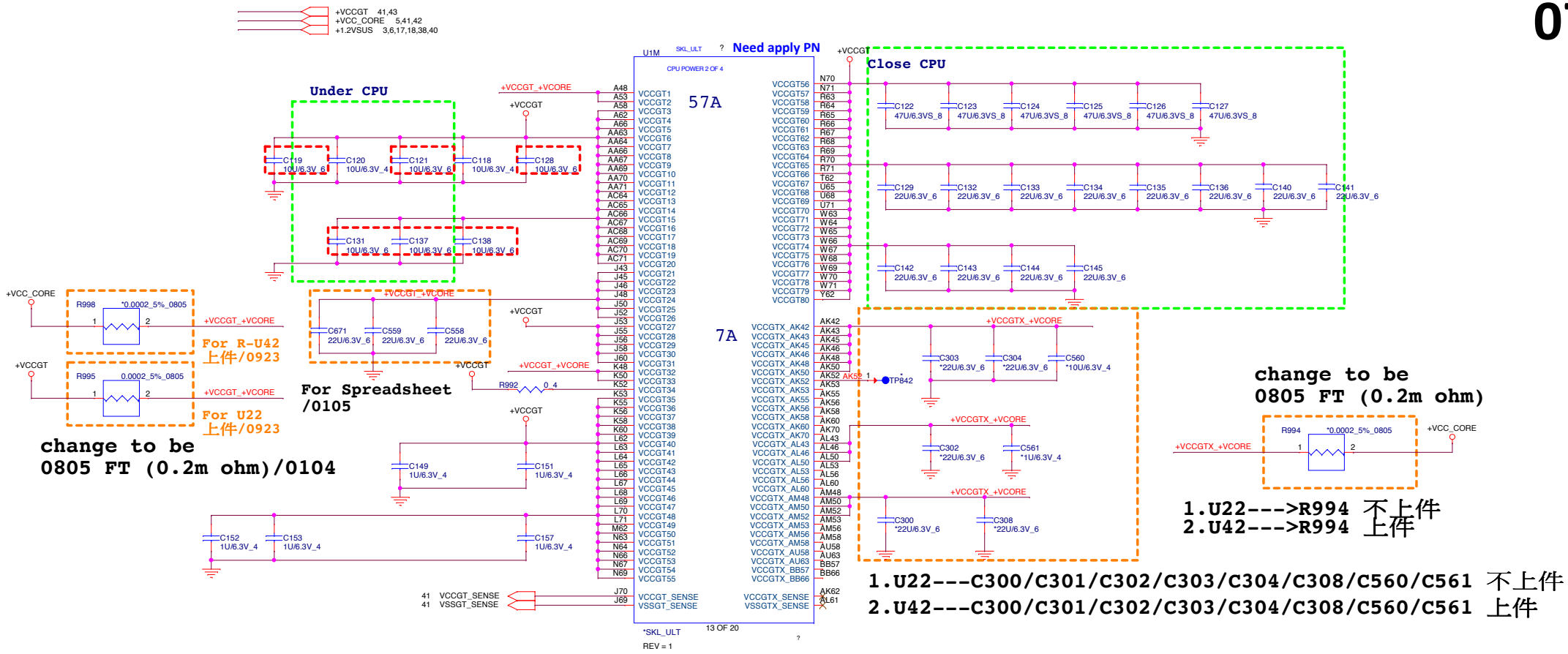
For CPU USE



For PIPE USE



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



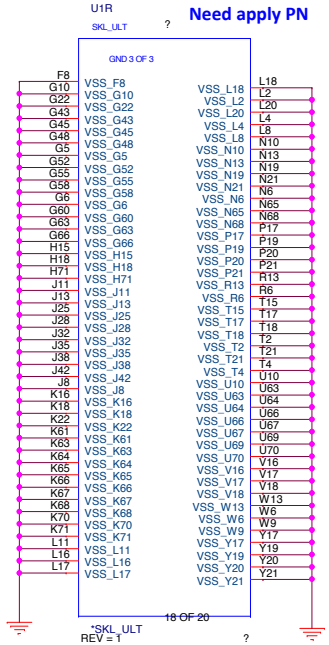
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

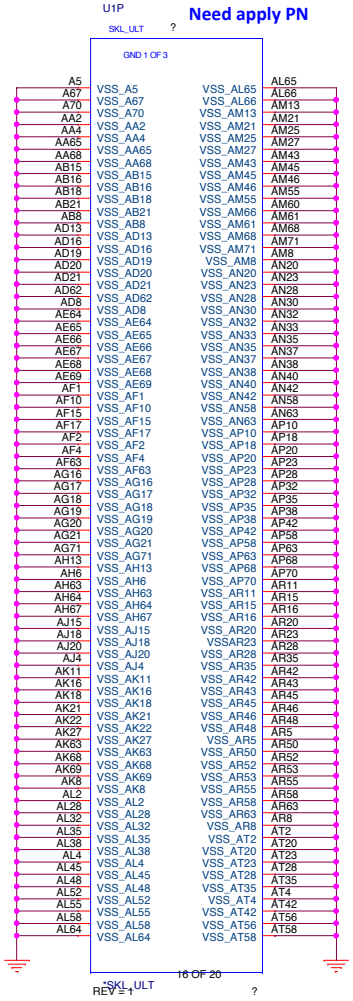
BU5

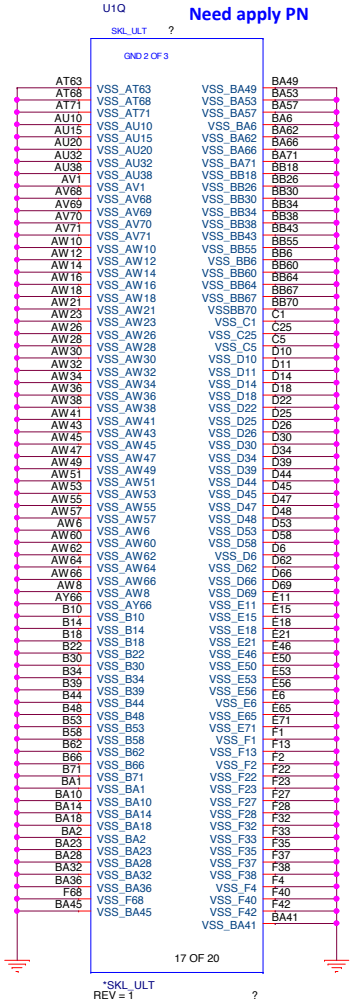
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 -- SKYLAKE 6/15 (POWER-3)	1A

Date: Friday, March 24, 2017 Sheet 7 of 49







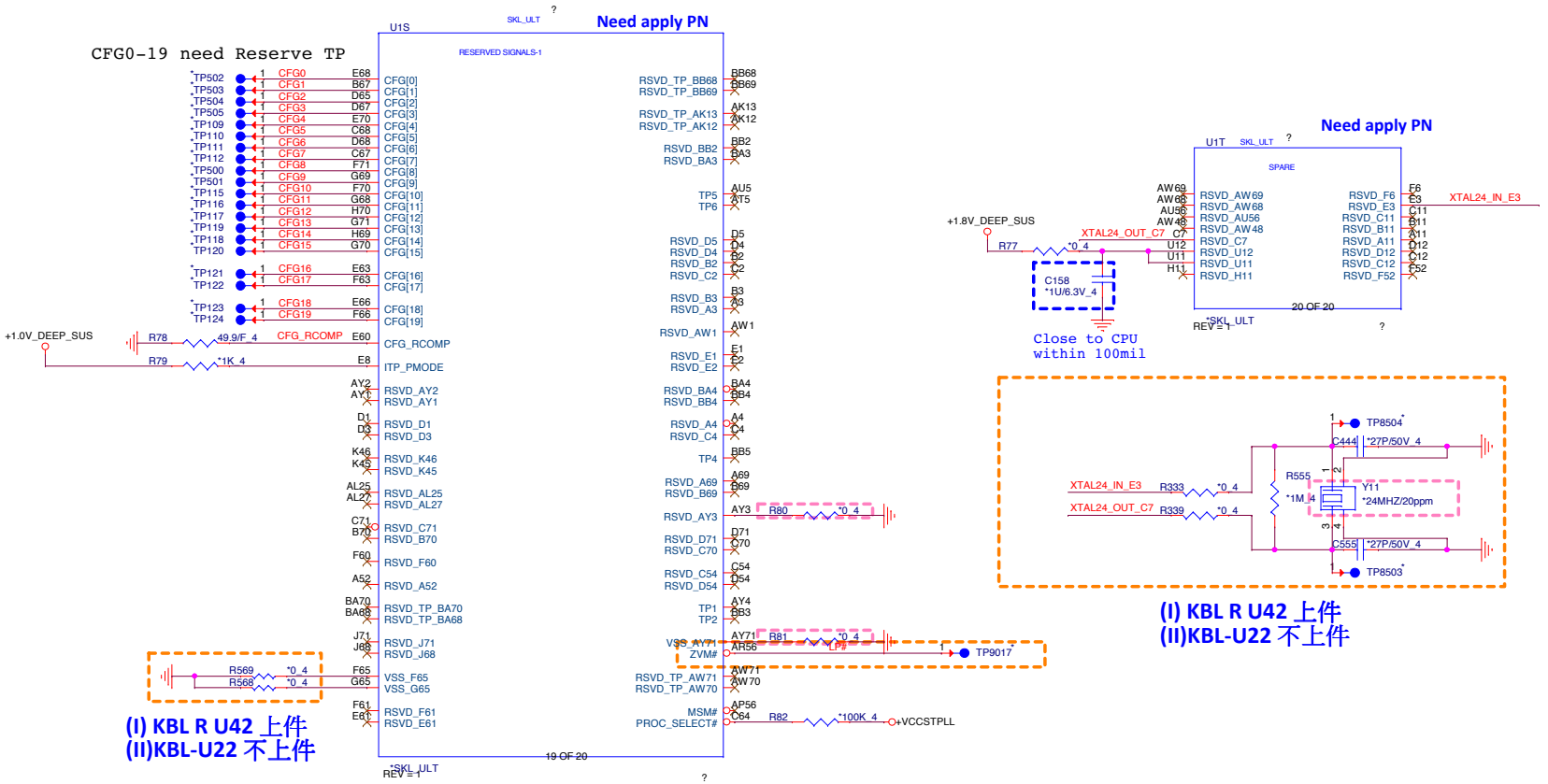
BU5

PROJECT : NFLP_KBLU_DR

Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE 7/15 (GND)	1A

Date: Friday, March 24, 2017 | Sheet 8 of 49



Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- SKYLAKE 8/15 (RSV)	1A

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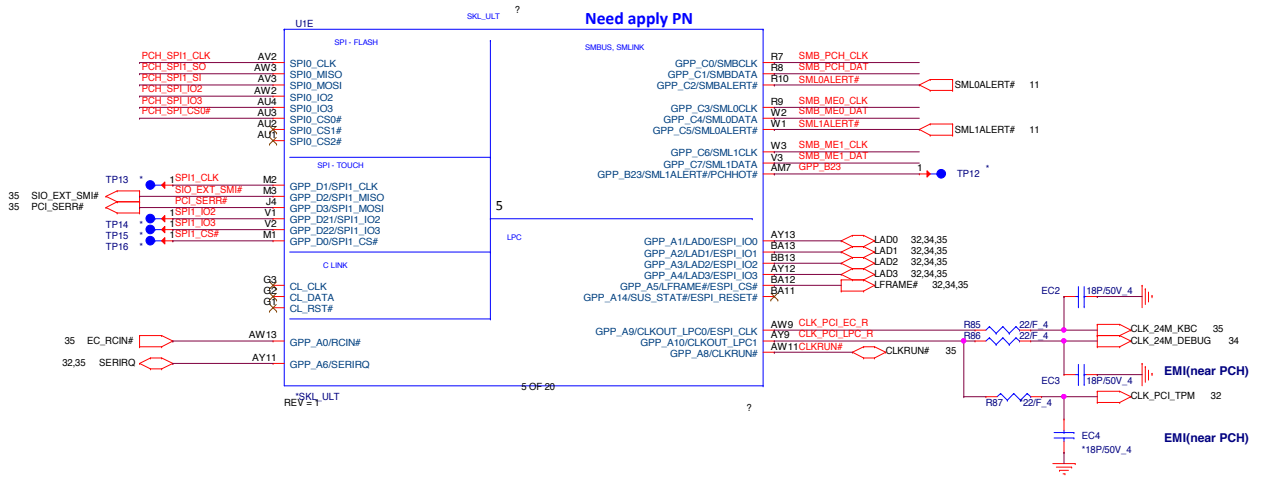
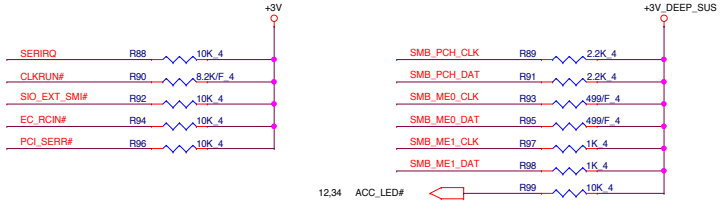
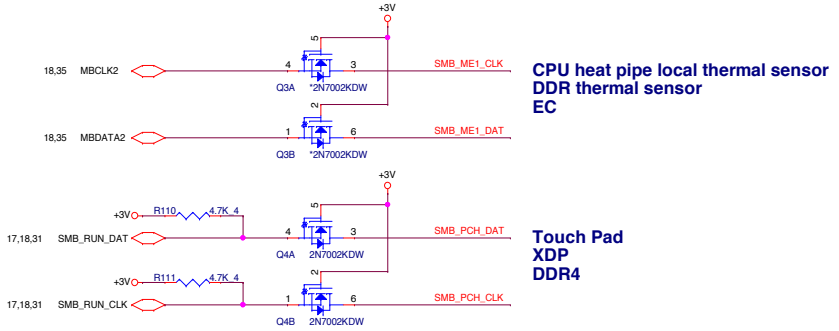
+3V_DEEP_SUS 4,11,12,14,15,18
+3V 2,4,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41,48
+5V 25,26,27,31,32,34,48,50
+1.0V 2,4,6,35,40
+3VS5 4,15,25,34,35,37,38,39,40,44,47,48,50



GPIO Pull UP



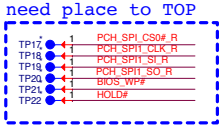
SMBus/Pull-up(CLG)



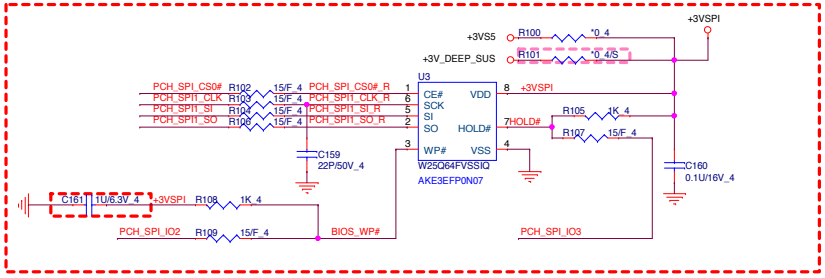
PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

need place to TOP



PCH SPI ROM(CLG)



1005 Change P/N to DFHS08FS023(Socket)

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYLAKE 09/15(SPI/LPC/SM)	1A
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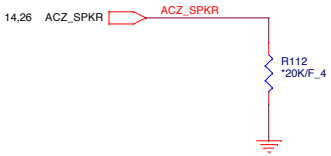
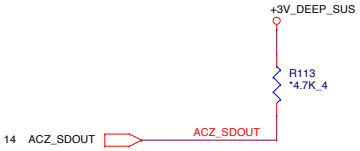
Functional Strap Definitions

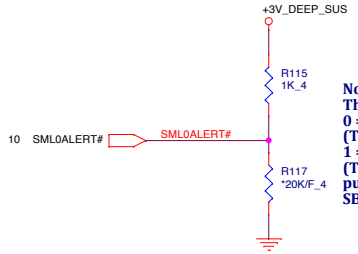
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



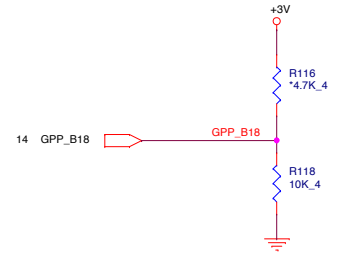
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



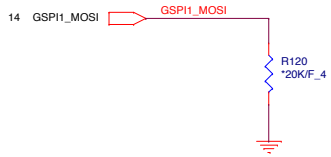
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

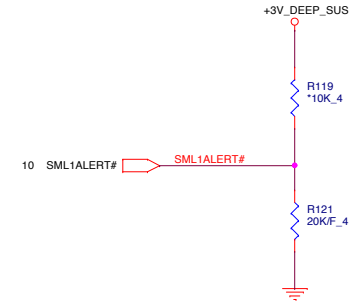


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE 10/15(HDA)	1A

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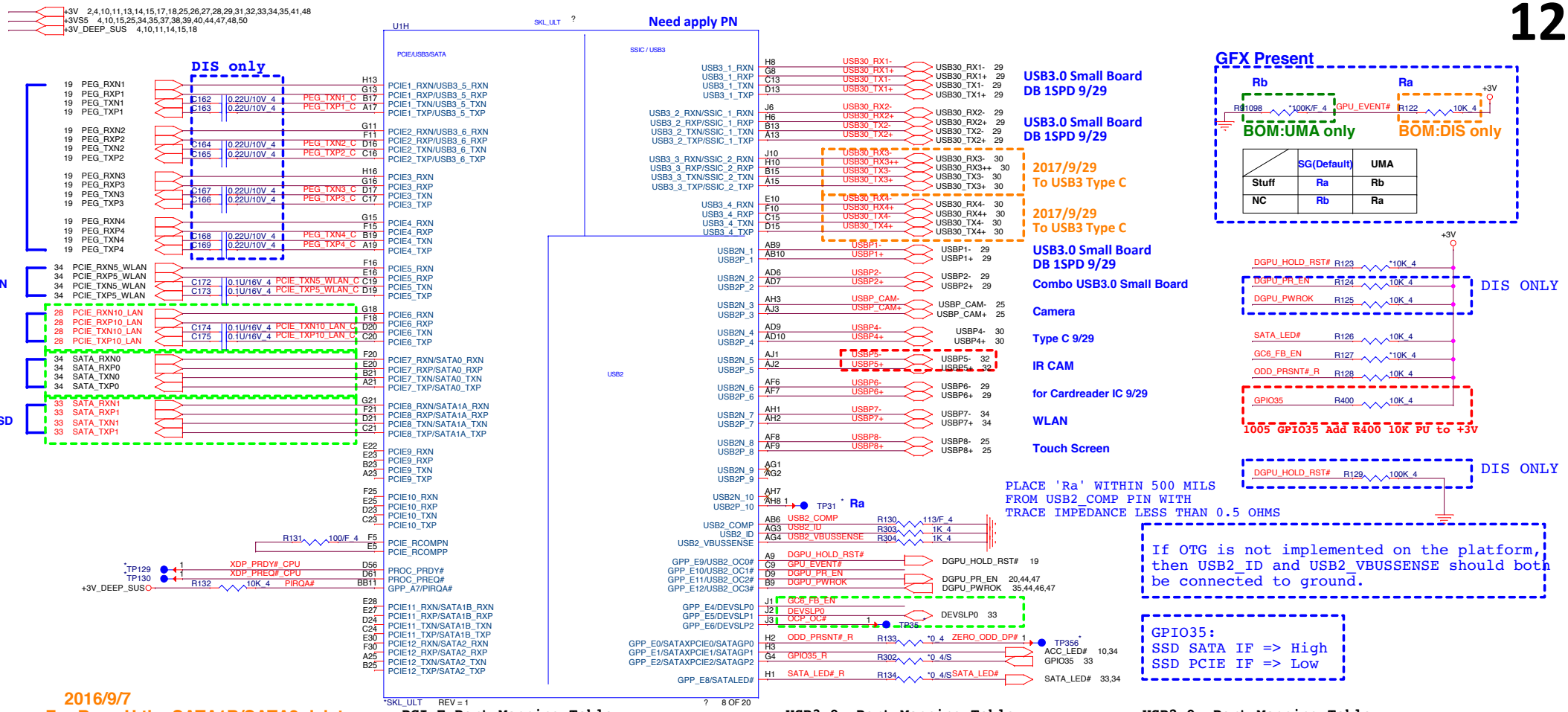


USB3.0 Small Board
DB 1SPD 9/29

USB3.0 Small Board
DB 1SPD 9/29

2017/9/29
To USB3 Type C

2017/9/29
To USB3 Type C

USB3.0 Small Board
DB 1SPD 9/29

Combo USB3.0 Small Board

Camera

Type C 9/29

IR CAM

for Cardreader IC 9/29

WLAN

Touch Screen

PLACE 'Ra' WITHIN 500 MILS
FROM USB2_COMP PIN WITH
TRACE IMPEDANCE LESS THAN 0.5 OHMS

If OTG is not implemented on the platform, then USB2_ID and USB2_VBUSSENSE should both be connected to ground.

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

GFX Present

	SG(Default)	UMA
Stuff	Ra	Rb
NC	Rb	Ra

2016/9/7
For Base-U the SATA1B/SATA2 delete

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	Un-used
Port3	dGPU	Port2	Un-used
Port4	dGPU	Port3	WLAN
Port5	WLAN	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	SATA SSD		
Port9	Un-used		
Port10	Un-used		
Port11	Un-used		
Port12	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	NC
PORT-4	NC

1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 Small Board
PORT-2	USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	Cardreader IC
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE 10/15(HDA)	1A

Date: Friday, March 24, 2017 Sheet 12 of 49

+3V_RTC_2 4,15
+BAT_RTC 4,15,29,36,49
+1.8V_DEEP_SUS 9,15,39,47
+3V 2,4,10,11,12,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41,48

VGA
Cardreader
SSD
WLAN
LAN

19 CLK_VGA_N
19 CLK_VGA_P
20 PCIE_CLKREQ_VGA#
34 CLK_PCIE_WLANN
34 CLK_PCIE_WLANP
34 PCIE_CLKREQ_WLAN#
28 CLK_PCIE_LANN
28 CLK_PCIE_LANP
28 PCIE_CLKREQ_LAN#

CLK_VGA_N
CLK_VGA_P
PCIE_CLKREQ_VGA#
PCIE_CLKREQ_CR#
PCIE_CLKREQ_SSD#
CLK_PCIE_WLANN
CLK_PCIE_WLANP
PCIE_CLKREQ_WLAN#
CLK_PCIE_LANN
CLK_PCIE_LANP
PCIE_CLKREQ_LAN#
PCIE_CLKREQ5#

U1J SKL_ULT ? Need apply PN
CLOCK SIGNALS

D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5
E39 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#

F43 CLKOUT_ITPXDP_N
E43 CLKOUT_ITPXDP_P
BA17 GPD8/SUSCLK
E37 XTAL24_IN
E35 XTAL24_OUT
E42 XCLK_BIASREF
AM18 RTCX1
AM20 RTCX2
AN18 SRTCRST#
AM16 RTCRST#

TBT
TP38
10 OF 20
*SKL_ULT REV = 1

+1.0V_DEEP_SUS
R135 2.7K/F_4
XCLK_BIASREF
R137 *60.4/F_4

CLK_REQ/Strap Pin(CLG)
+3V
PCIE_CLKREQ_VGA# R136 10K_4
PCIE_CLKREQ_WLAN# R138 10K_4
PCIE_CLKREQ_LAN# R139 10K_4
PCIE_CLKREQ_CR# R140 10K_4
PCIE_CLKREQ_SSD# R141 10K_4
PCIE_CLKREQ5# R142 10K_4

U1I SKL_ULT ? Need apply PN
CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C36 CSI2_DN1
D36 CSI2_DP1
C35 CSI2_DN2
D35 CSI2_DP2
A35 CSI2_DN3
B35 CSI2_DP3
C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A33 CSI2_DN6
B33 CSI2_DP6
A31 CSI2_DN7
B31 CSI2_DP7
A29 CSI2_DN8
B29 CSI2_DP8
C29 CSI2_DN9
D29 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

C37 CSI2_CLKN0
C37 CSI2_CLKP0
C32 CSI2_CLKN1
C32 CSI2_CLKP1
C29 CSI2_CLKN2
C29 CSI2_CLKP2
C26 CSI2_CLKN3
C26 CSI2_CLKP3
E13 CSI2_COMP
B7 GPP_D4/FLASHTRIG

EMMC
AP2 GPP_F13/EMMC_DATA0
AP1 GPP_F14/EMMC_DATA1
AP3 GPP_F15/EMMC_DATA2
AN3 GPP_F16/EMMC_DATA3
AN1 GPP_F17/EMMC_DATA4
AN2 GPP_F18/EMMC_DATA5
AM4 GPP_F19/EMMC_DATA6
AM1 GPP_F20/EMMC_DATA7
AM2 GPP_F21/EMMC_RCLK
AM3 GPP_F22/EMMC_CLK
AP4 GPP_F12/EMMC_CMD
AT1 EMMC_RCOMP

R143 100/F_4
1005 Delete TP
EMMC_RCOMP R144 200/F_4

9 OF 20
*SKL_ULT REV = 1

RTC Clock 32.768KHz

C177 15P/50V_4
C179 15P/50V_4
Y1 32.768KHZ/20ppm
R147 10M_4
RTC_X1
RTC_X2

RTC Circuitry(RTC)

+3V_RTC_2
+BAT_RTC
30mils
Main BAT -->Ra
Coin BAT -->Rb (default)
Rb
Ra
R306 *0_4
R307 0_4
R145 *0_6
R146 20K/F_4
RTC_RST#
C178 1U/6.3V_4
RTC Power trace width 20mils.
+3V_RTC_0
+3VPCUO
+3V_RTC_1
R150 1K_4
D2 BAT54CW-7-F
C181 1U/6.3V_4
R149 20K/F_4
SRTC_RST#
C182 1U/6.3V_4
R9042 *0_6
R9041 0_6
RTC_RST# R152 *0_6 SRTC_RST#
CN101 *BAT_CONN DFHS02FS027 BAT-23_2-4_2
CN11 *88266-020L

R151 10K_4
EC_RTC_RST 35
Q5A 2N7002KDW
R942 *0_4
EC_SRTC_RST 35
Q5B 2N7002KDW
R153 10K_4

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

change 40.2ohm enhance RF immunity 1/23
XTAL24_IN R666 40.2/F_4
XTAL24_OUT R667 40.2/F_4
R148 1M_4
Y2 24MHZ/20ppm
C176 27P/50V_4
C180 27P/50V_4
TP51
TP52

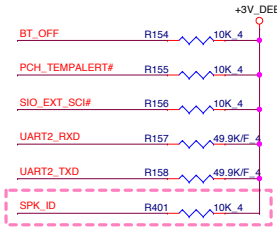
BU5

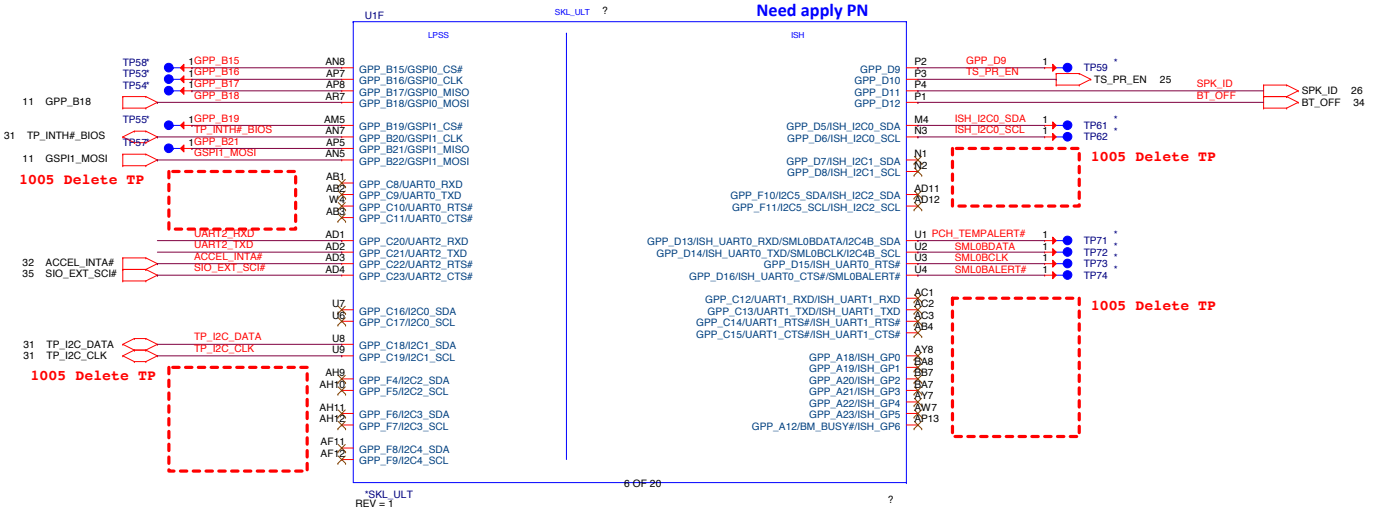
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYLAKE 12/15 (CLK/EMMC)	1A
Date: Saturday, March 25, 2017	Sheet 13 of 49	

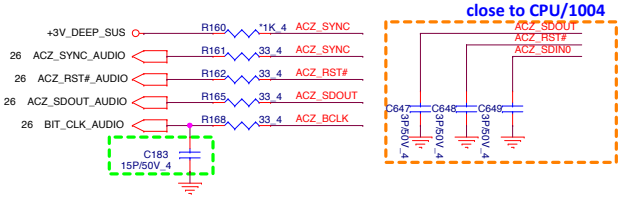
Skylake (GPIO)

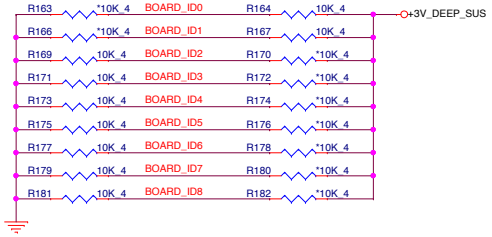
+3V 2,4,10,11,12,13,15,17,18,25,26,27,28,29,31,32,33,34,35,41,48
+3V_DEEP_SUS 4,10,11,12,15,18

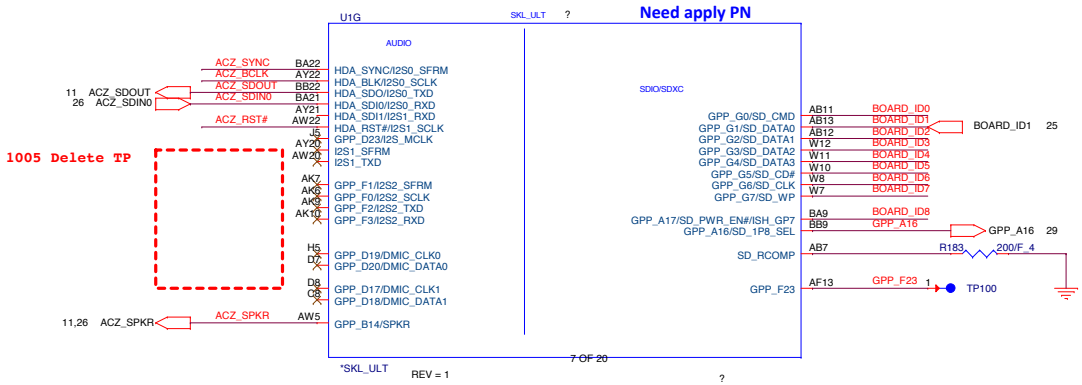




HDA Bus(CLG)







Skylake U	BOARD_ID[8:6]	BOARD_ID[5]	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7 ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 000)	GPU 0 : AMD 1 : Intel	0 4 VRAMs 1 8 VRAMs	0 VGA CAM 1 IR CAM	01 14" (14" cable is 00) 01 15" 1SPD 10 17" 11 2SPD	0 : UMA 1 : DIS

ID1(R167)always 上件

4,10,11,12,14,18 +3V_DEEP_SUS
9,13,39,40 +1.0V_DEEP_SUS
9,39,47 +1.8V_DEEP_SUS
4,13,29,36,49 +BAT_RTC
4,10,25,34,35,37,38,39,40,44,47,48,50 +3VSS

U1O SKL_ULT — CPU POWER 4 OF 4 — 15 OF 20 — *SKL_ULT REV = 1

Need apply PN

PCH Internal VRM

Ca and Cb close to CPU less then 100 mils

Ca

Cb

close to CPU/1004

close to CPU/1004

for DS3

Main BAT -->Ra
Coin BAT -->Rb (default)

20mils

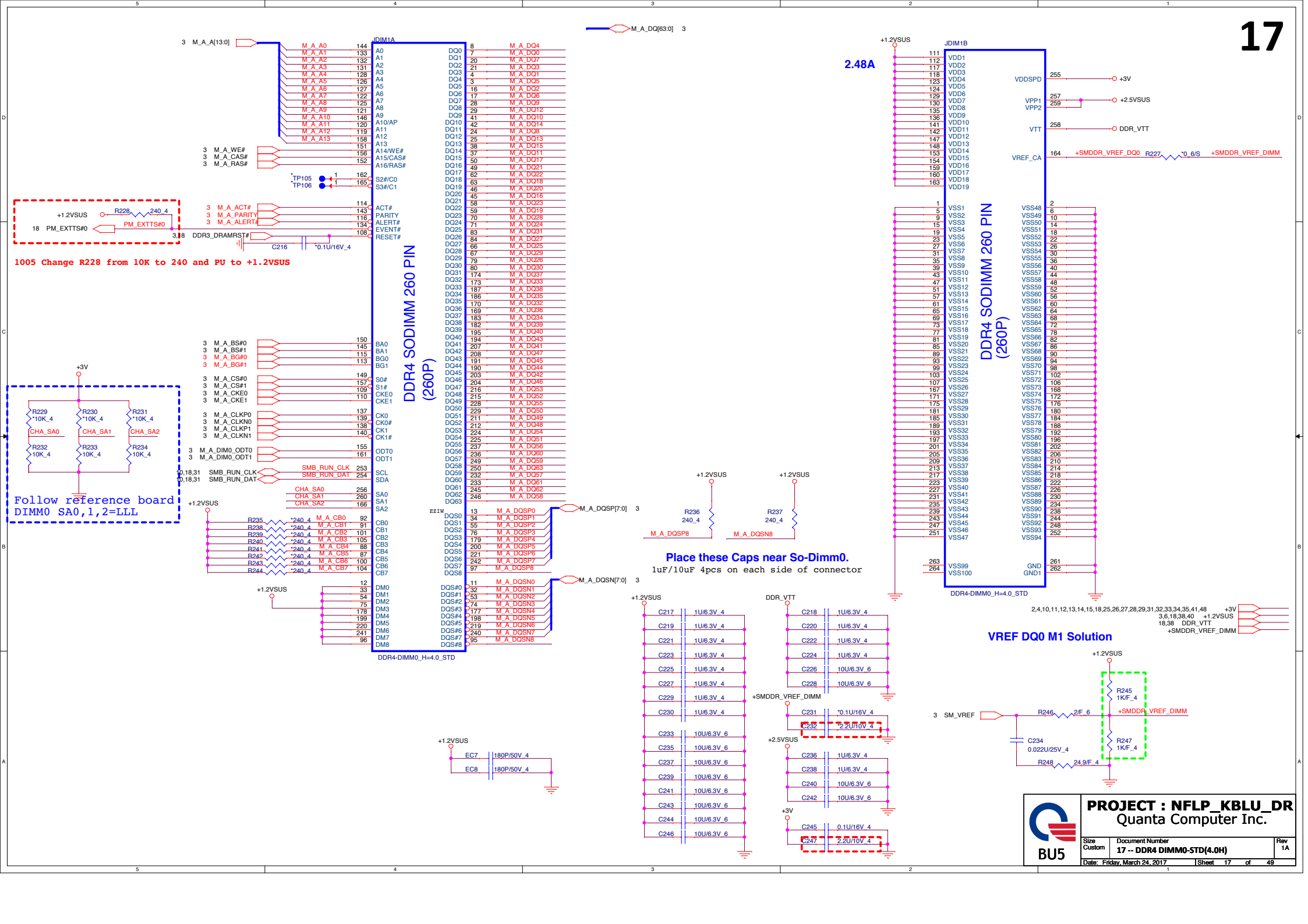
1005 Change +3V_RTC to +BAT_RTC

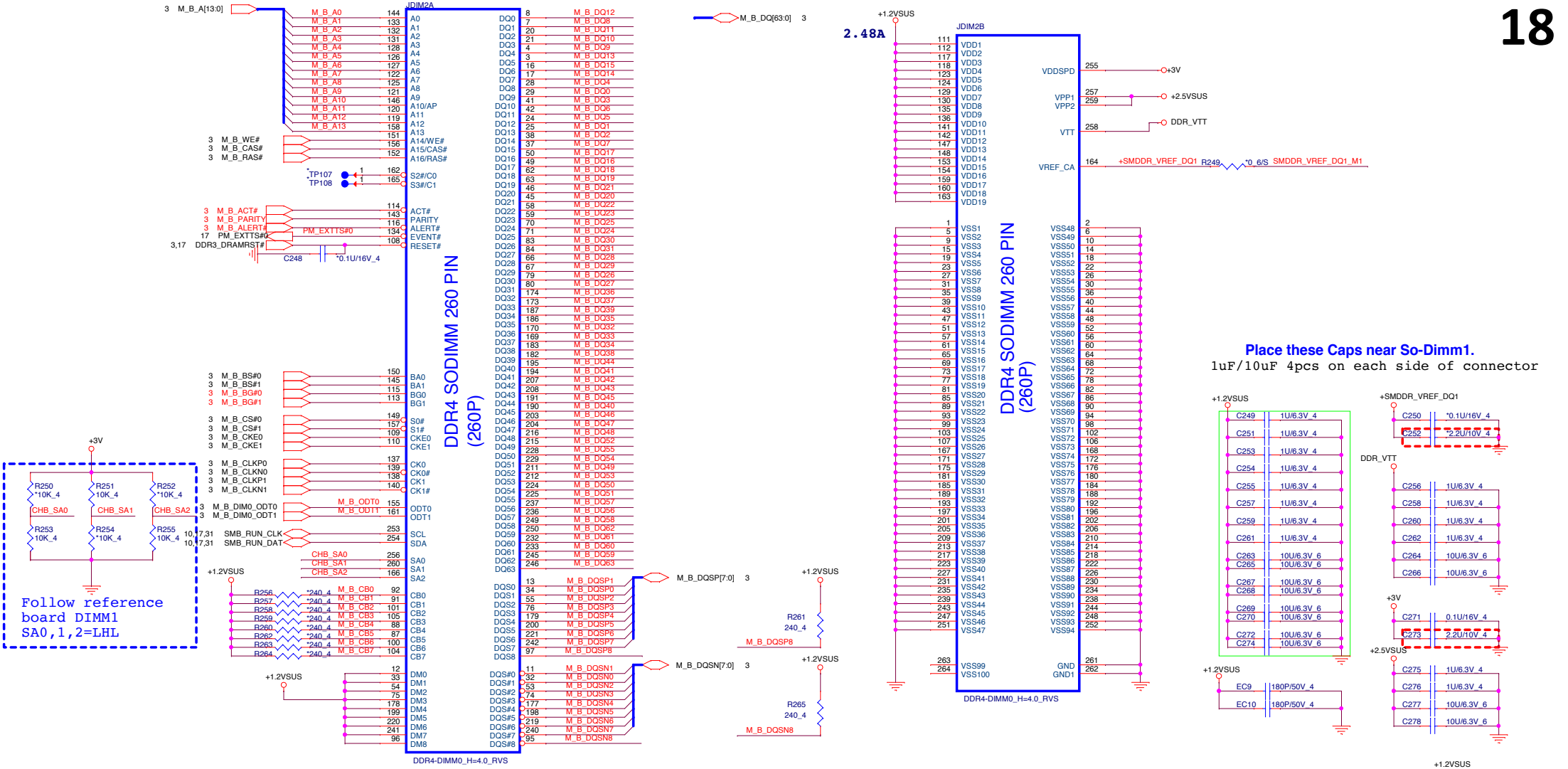
2.899A
2.57A
1.714A
0.03A
0.09A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

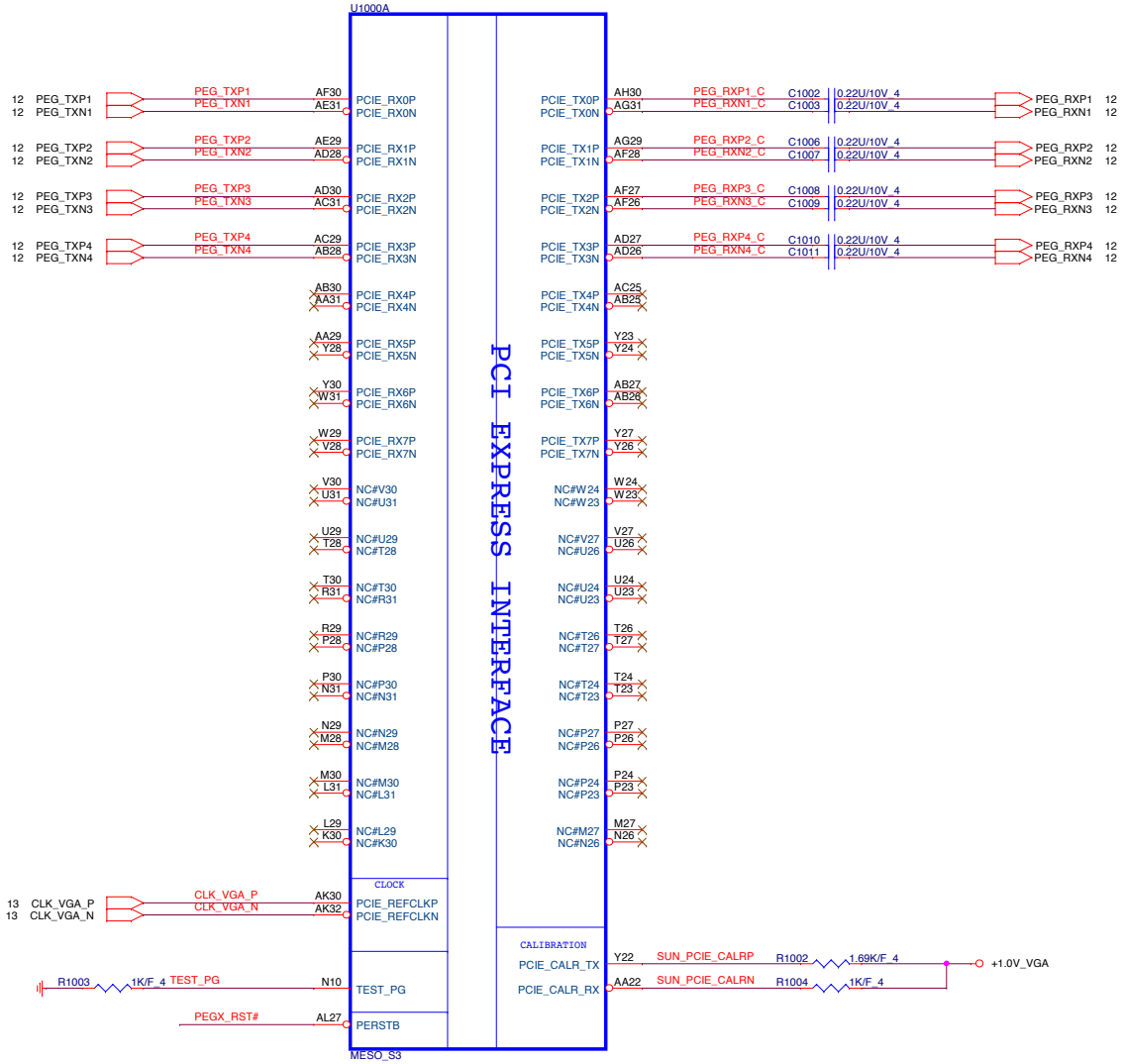
Size	Document Number	Rev
	16 -- SKYLAKE 15/15 XDP&APS *	1A
Date: Friday, March 24, 2017	Sheet 16 of 49	

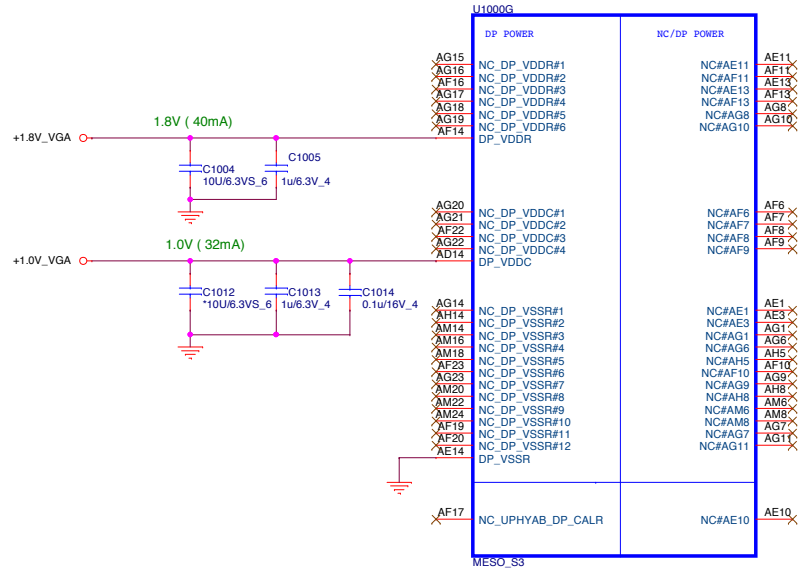

JDIM1A
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
M_A_DQ[63:0]
M_A_A[13:0]
2.48A
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
Date: Friday, March 24, 2017
Sheet 17 of 49

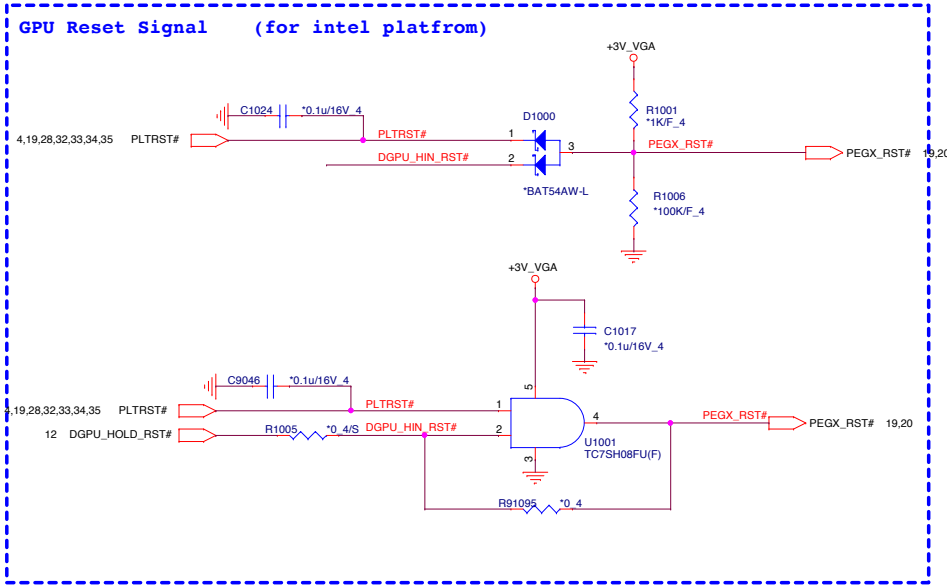


PROJECT :	NFLP_KBLU_DR
Quanta Computer Inc.	
Size: Custom	Document Number: 18 -- DDR4 DIMM1-RVS(4.0H)
Rev:	1A
Date: Friday, March 24, 2017	Sheet 18 of 49

BU5



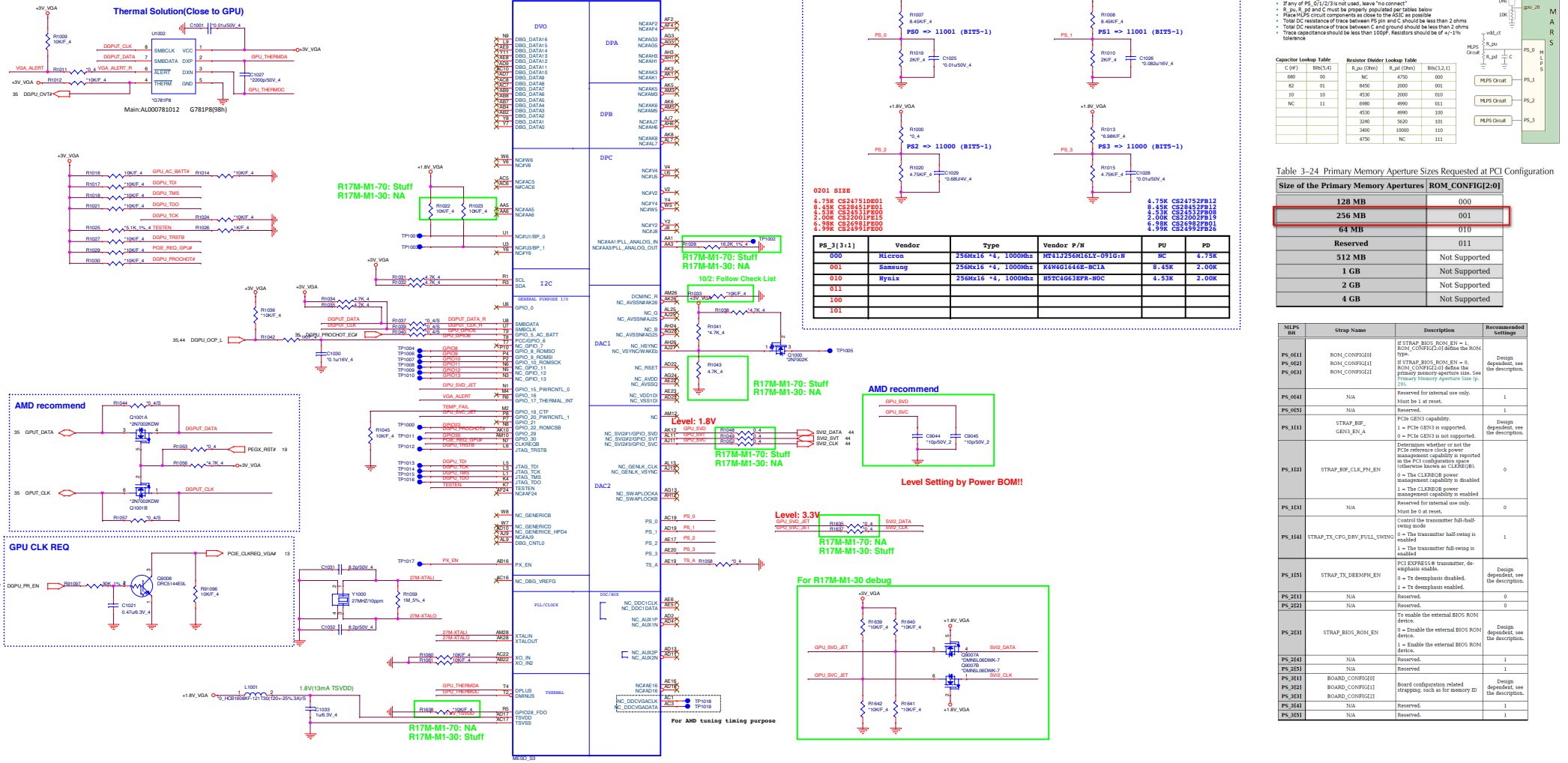




NB5

PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
	R17M_M2-50_S3_PCIE	1A
Date: Friday, March 24, 2017	Sheet 19 of 48	



PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Micron	256Mx16 *4, 1000Mhz	MT41J256M16LY-091G:N	NC	4.75K
001	Samsung	256Mx16 *4, 1000Mhz	K4W4G1646E-BC1A	8.45K	2.00K
010	Hynix	256Mx16 *4, 1000Mhz	H5TC4G63EFR-NOC	4.53K	2.00K
011					
100					
101					

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

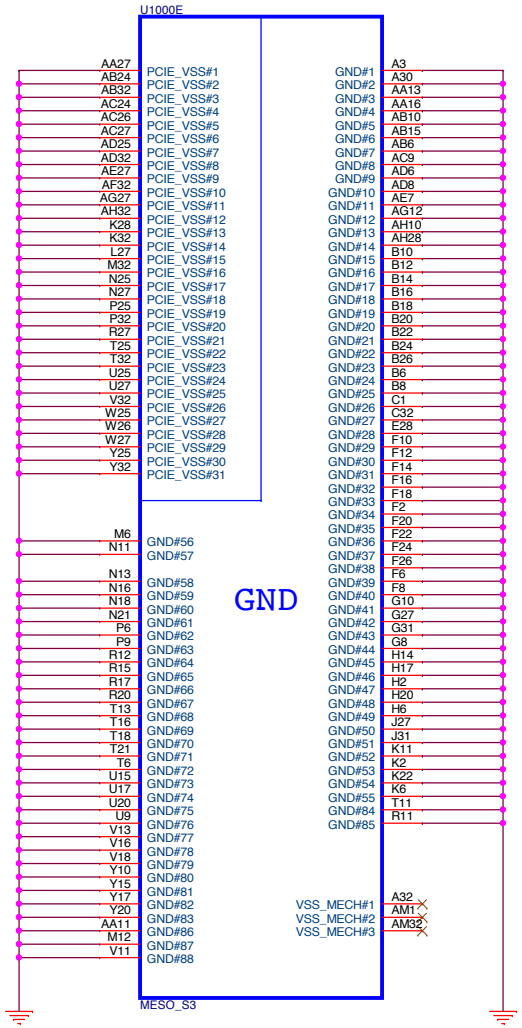
Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Table 3–24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CPG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

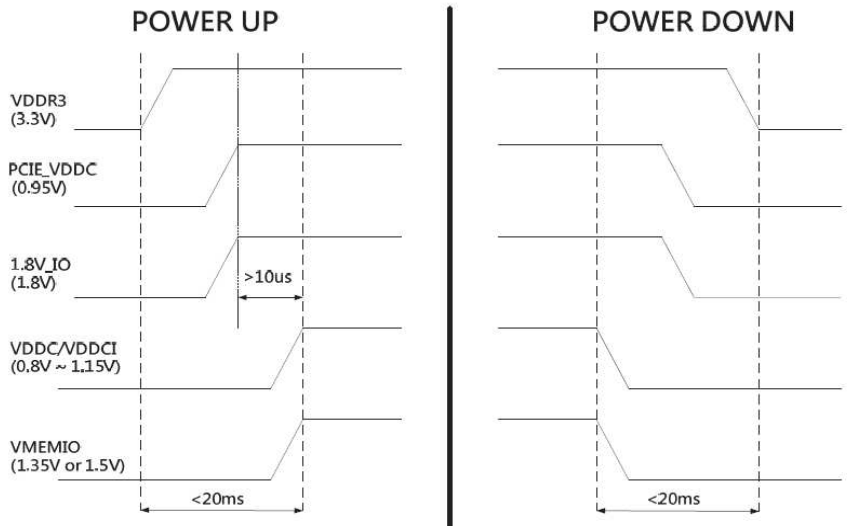
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2

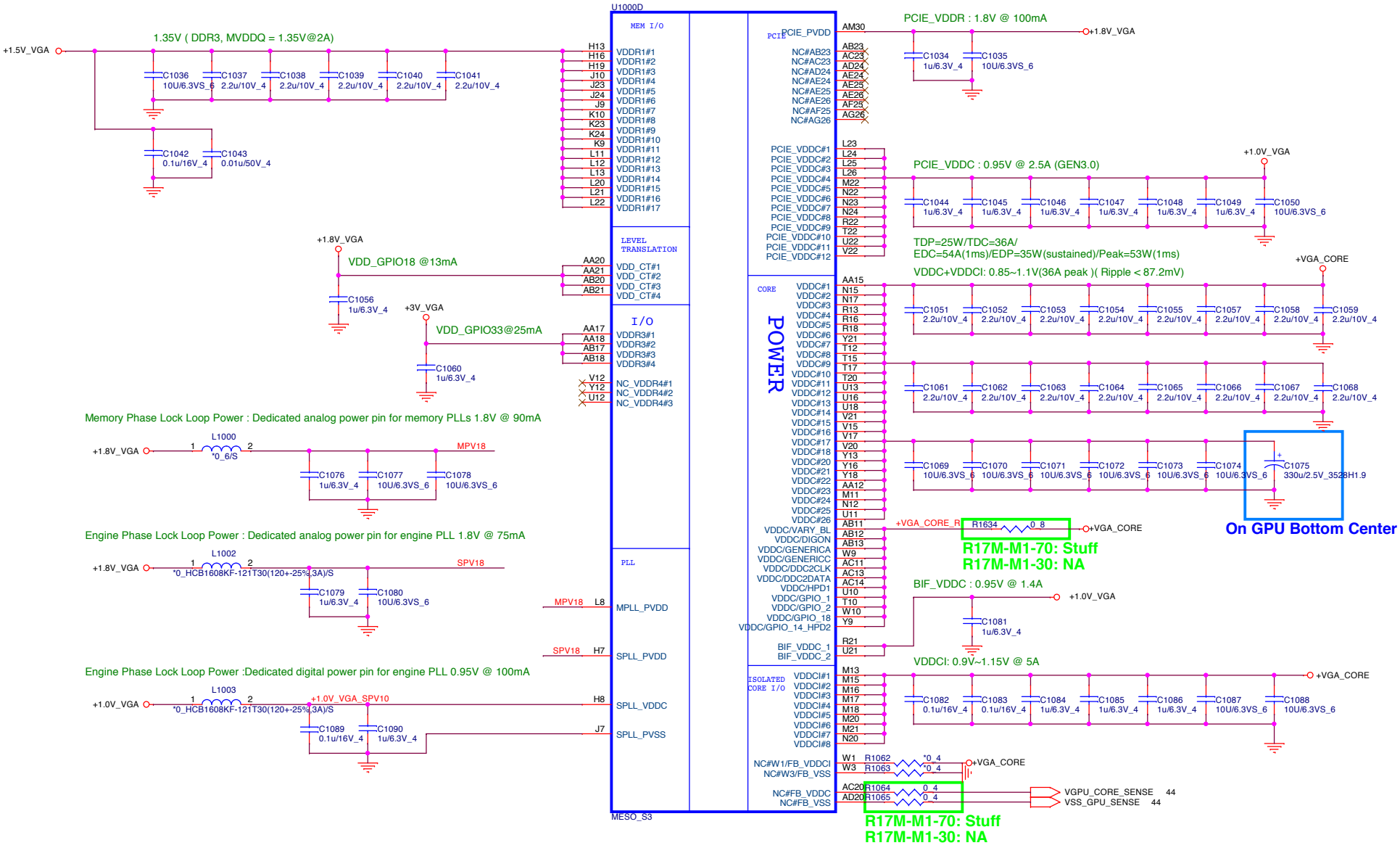
POWER UP / POWER DOWN SEQUENCE



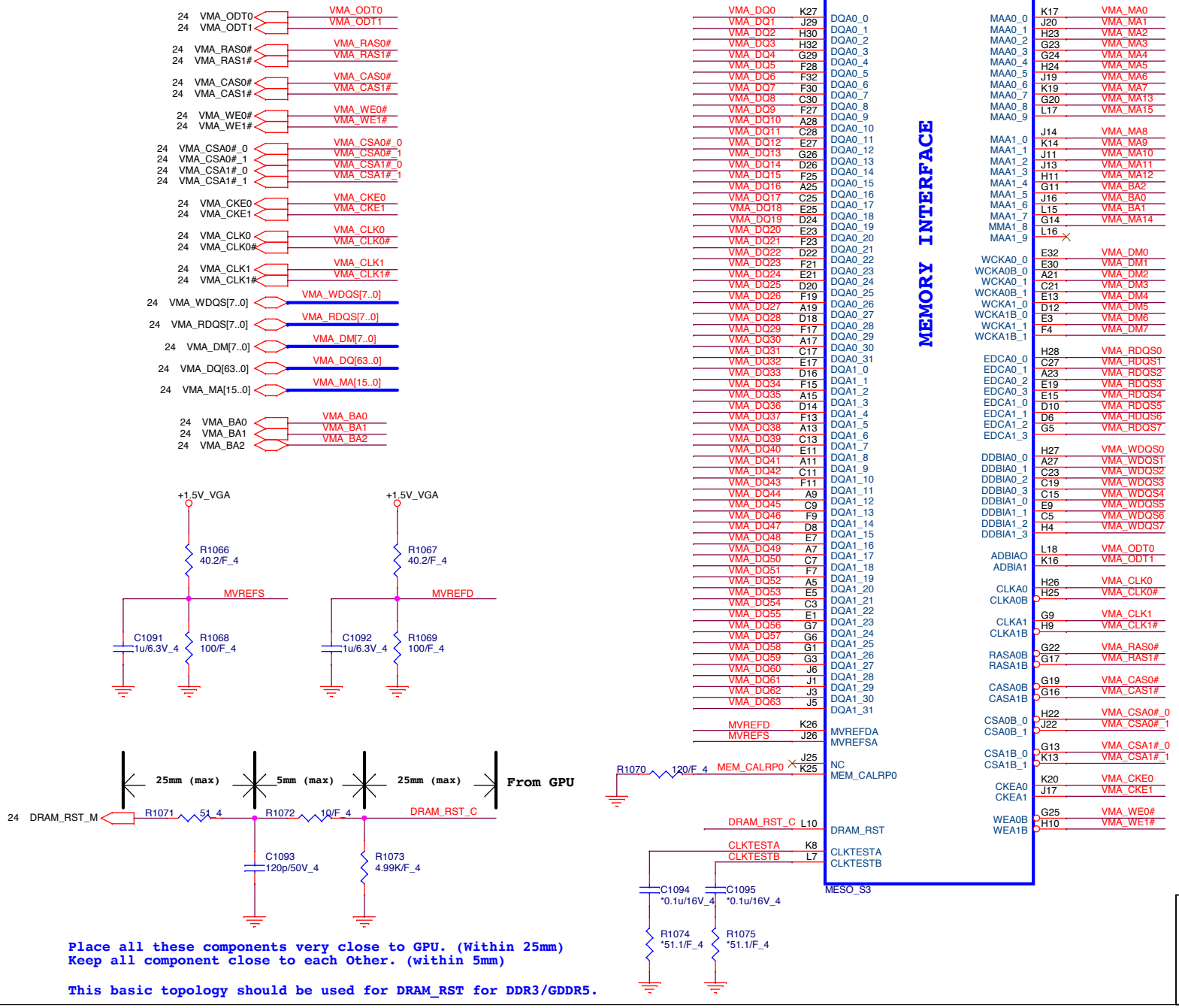
NB5

PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
	R17M_M2-50_DIS/GND	1A
Date: Friday, March 24, 2017	Sheet 21 of 48	



NB5	PROJECT : G54A Quanta Computer Inc.	
Size	Document Number R17M_M2-50_S3_POWER	Rev 1A
Date: Friday, March 24, 2017	Sheet 22 of 48	



Place all these components very close to GPU. (Within 25mm)
Keep all component close to each Other. (within 5mm)

This basic topology should be used for DRAM_RST for DDR3/GDDR5.

NB5

PROJECT : G54A
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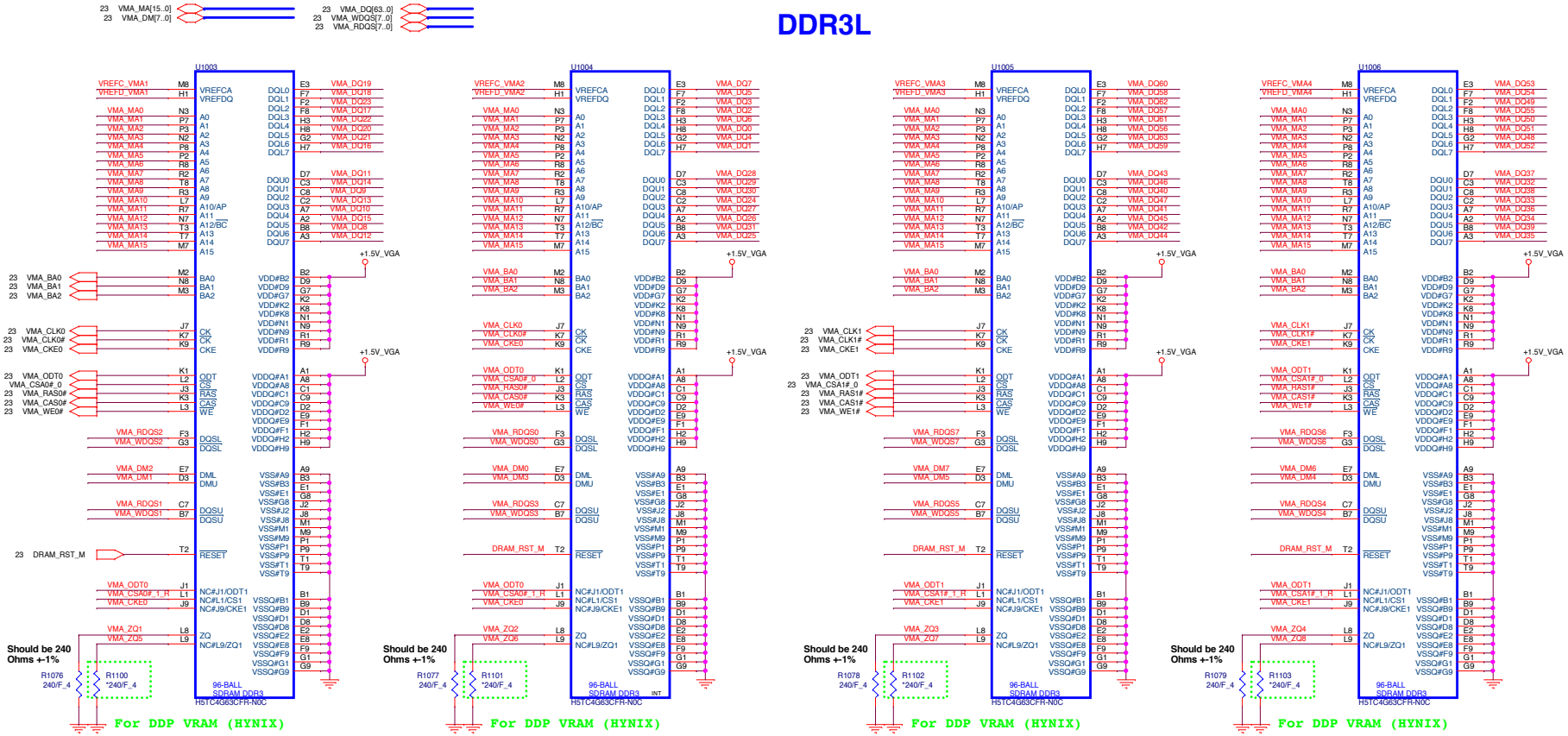
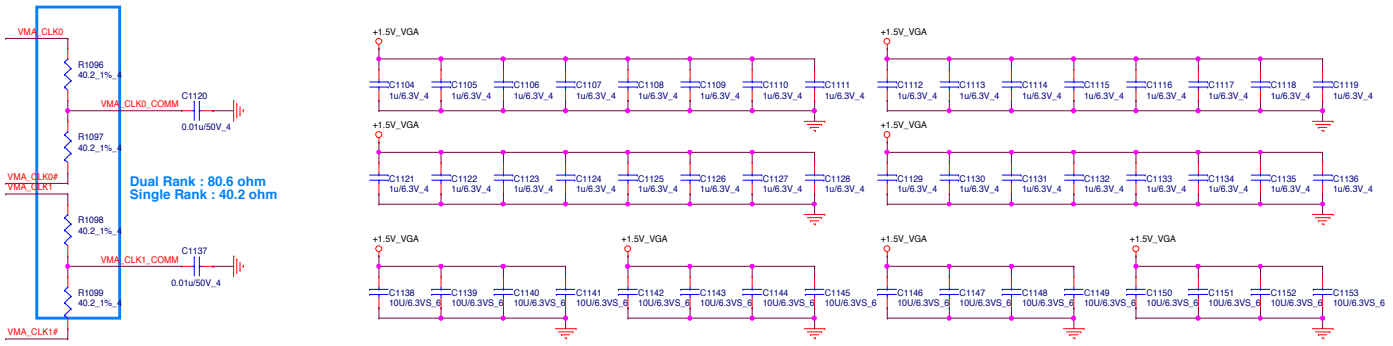
Size	Document Number	Rev
	R17M_M2-50_S3_MEM	1A
Date: Friday, March 24, 2017	Sheet 23 of 48	

DDR3L





	QBCON PN	TOP BSQ
Micron 4G (SDP)	AKD5QGSTL09	AKD5QGSTL05
Hynix 4G (DDP)	AKD5QFDTW01	AKD5QFDTW00
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

NB5

PROJECT : G54A
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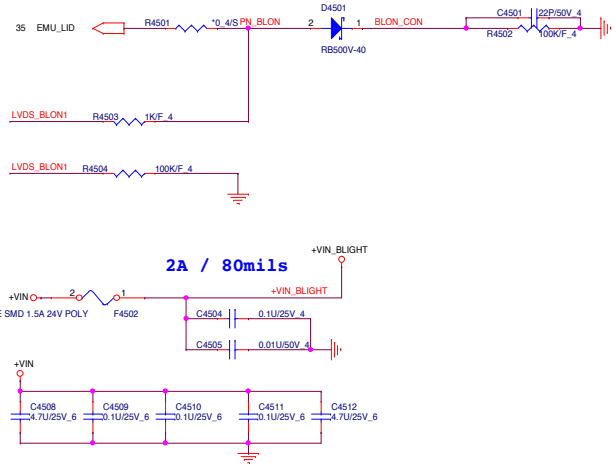
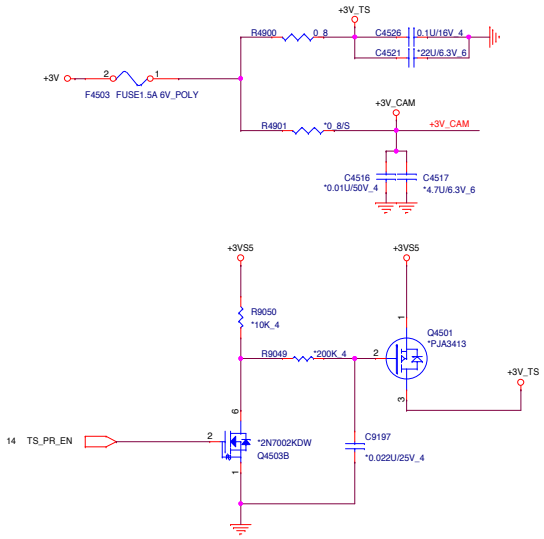
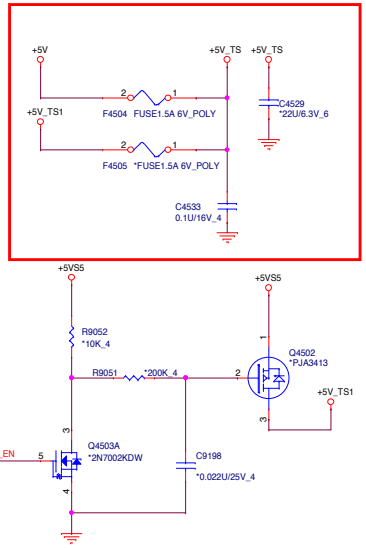
Size	Document Number	Rev
C	R17M_M2-50_VRAM(DDR3L)	1A

Date: Friday, March 24, 2017 | Sheet 24 of 48

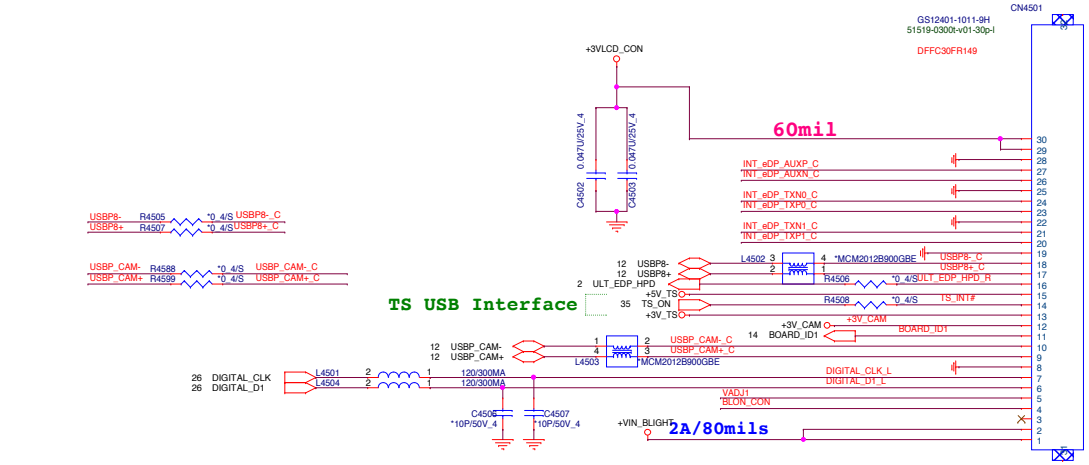
LID Switch

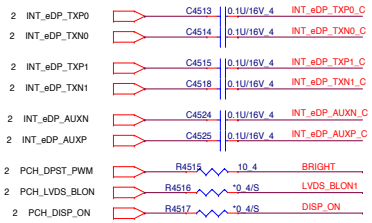


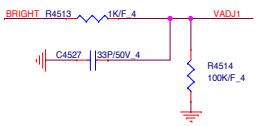


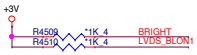


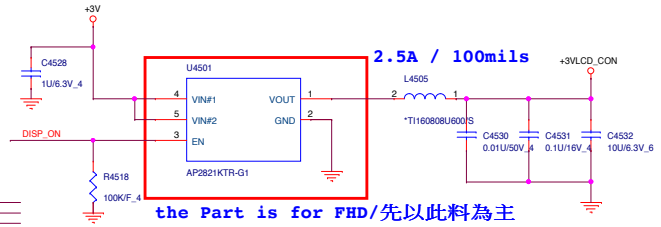
eDP Conn.











2,4,10,11,12,13,14,15,17,18,26,27,28,29,31,32,33,34,35,41,48 +3V
6,13,29,30,31,34,35,36,37,49 +3VPCU
26,27,31,32,34,48,50 +5V
31,36,37,38,39,42,43,44,45,46,50 +VIN

the Part is for FHD/先以此料為主

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 -- eDP CONN/LID/CAM/D-MIC/TS	1A
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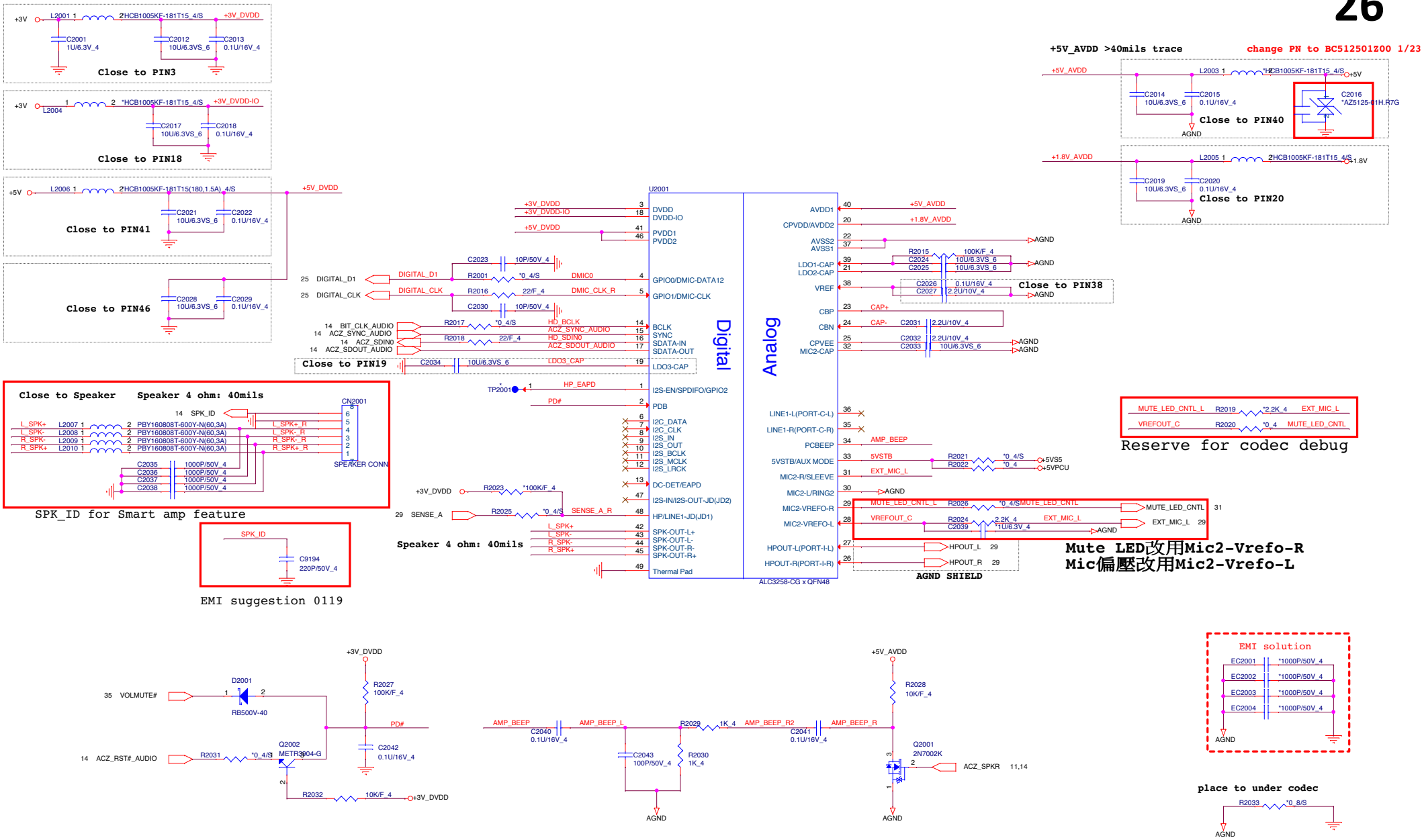
+5V_AVDD >40mils trace
change PN to BC512501200 1/23
Close to PIN3
Close to PIN18
Close to PIN41
Close to PIN46
Close to PIN40
Close to PIN20
Close to PIN38
Close to PIN19
Close to Speaker
Speaker 4 ohm: 40mils
SPK_ID for Smart amp feature
EMI suggestion 0119
Reserve for codec debug
Mute LED改用Mic2-Vrefo-R
Mic偏壓改用Mic2-Vrefo-L
AGND SHIELD
Speaker 4 ohm: 40mils
EMI solution
place to under codec
U2001
Digital
Analog
ALC3258-CG x QFN48
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Document Number
28 -- Codec ALC3258-CG
Date: Friday, March 24, 2017
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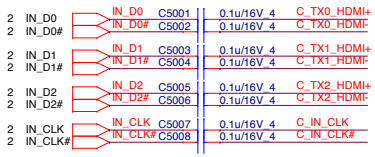
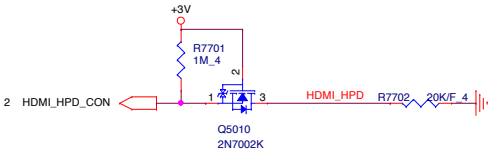
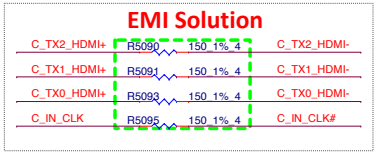
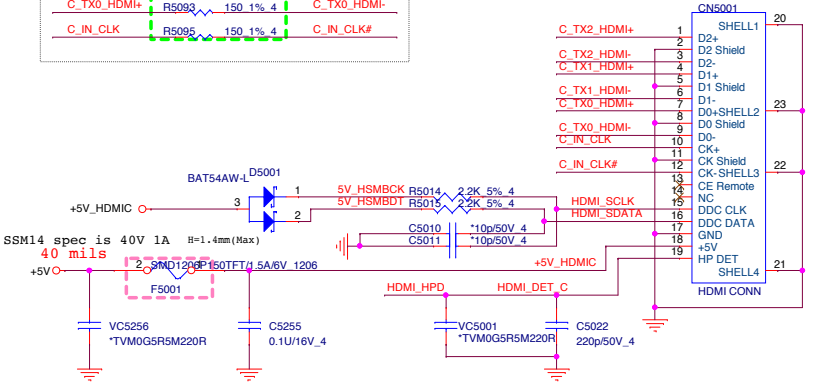
HDMI CONN

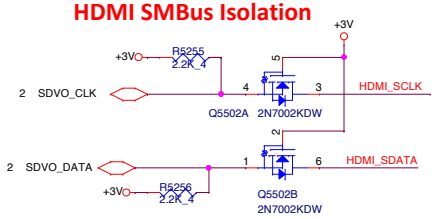




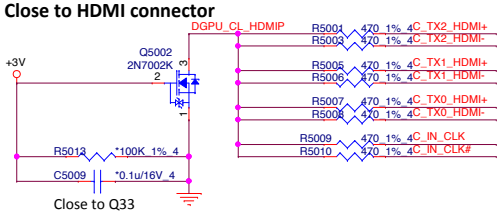




HDMI SMBus Isolation



Close to HDMI connector



Head Phone out

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Size: Custom	Document Number: 29 – HDMI/AMP HPA022642RTJR	Rev: 1A
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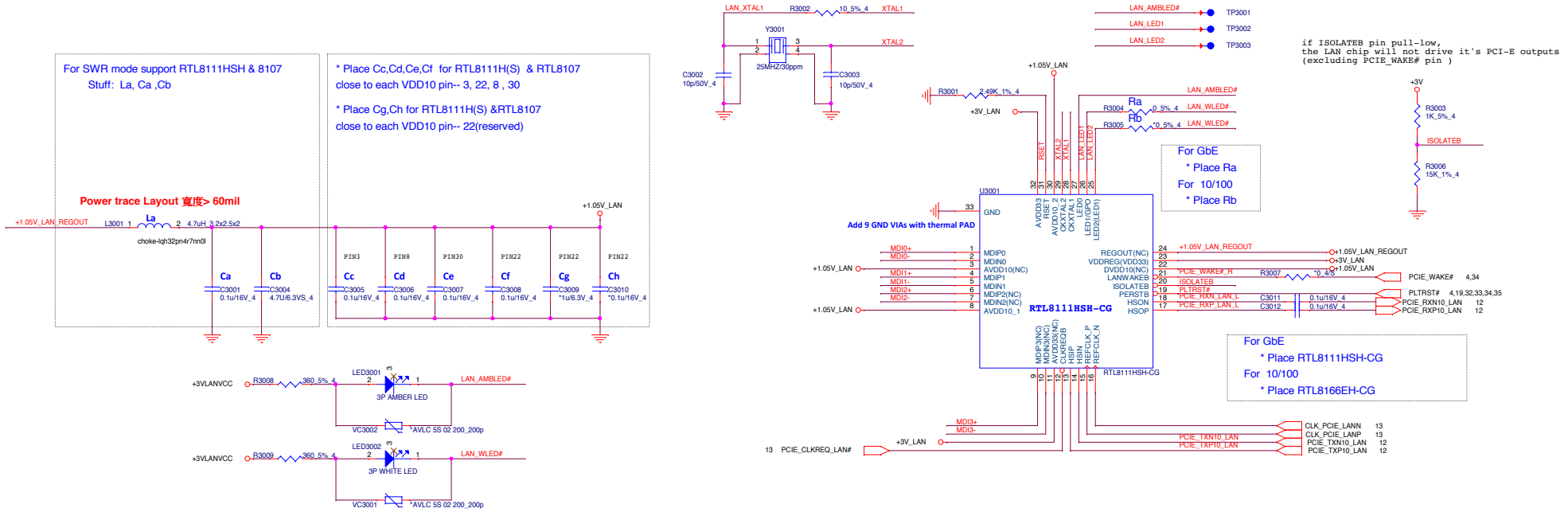
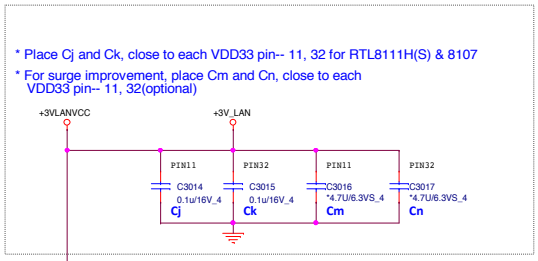
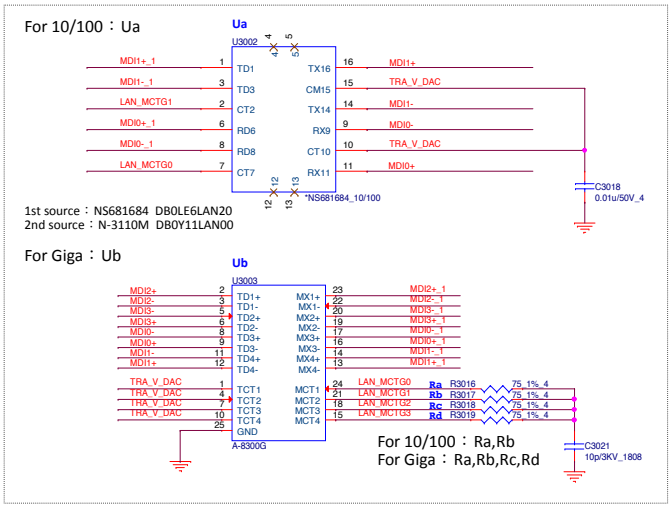
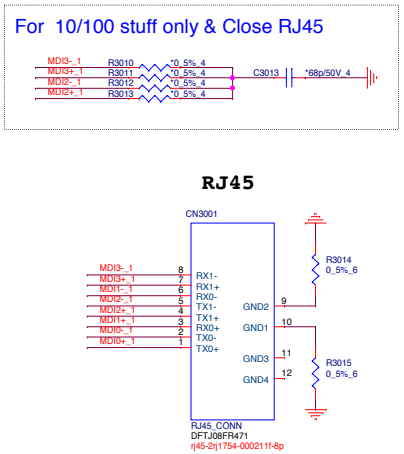
LAN RTL8107EH/RTL8111HSH







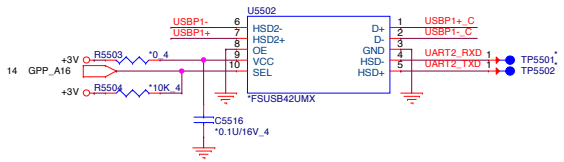
For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00



12,29 USBP1-
12,29 USBP1+
USBP1- R5502 *0_4/S USBP1-_C
USBP1+ R5501 *0_4/S USBP1+_C

+3VPCU R9045 360_5%_4 LED7011 3P WHITE LED DEEP_PWRLED#
VC9002 *AVLC 5S 02 200_200p

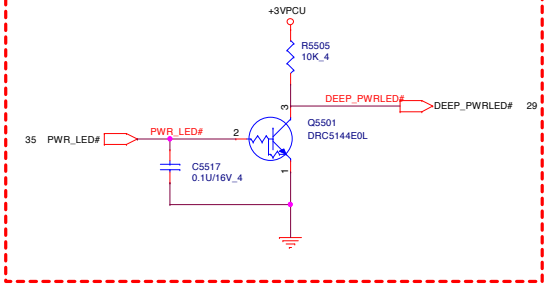
UART for Win7 WHQL DEBUG



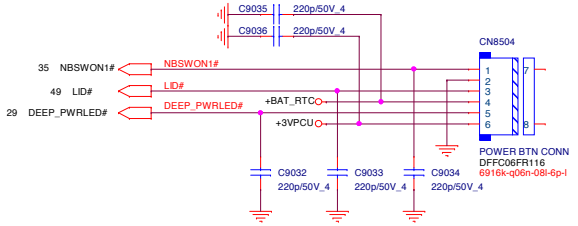
Place Back to Back La

Daughter Board

1123 Add PWR LED MOS Circuit



Power Board

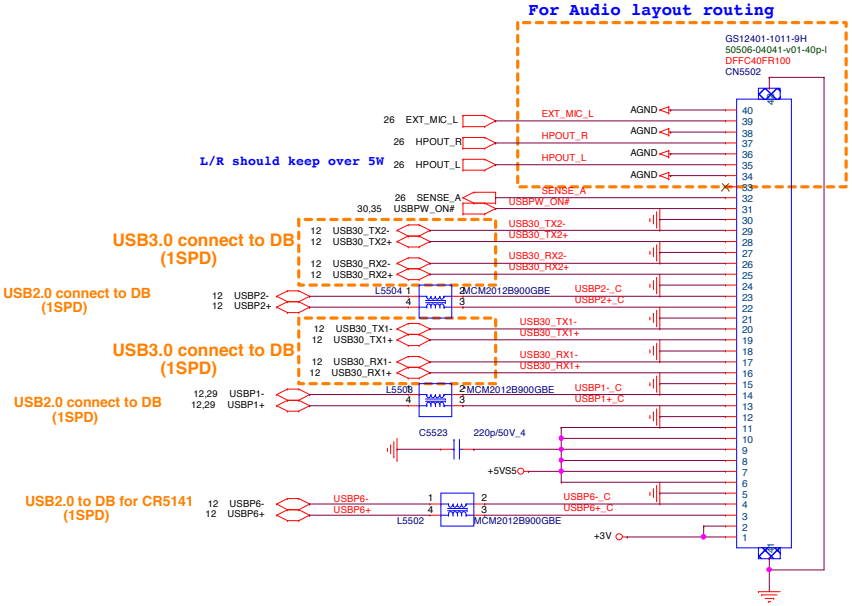


USB3.0

reserve for re-driver un-stuff 01/18

Daughter Board

For Audio layout routing



Layout Notes:
Stubs Trace less than 150mil

USB3.0

reserve for re-driver un-stuff 01/18

Layout Notes:
Stubs Trace less than 150mil

BU5

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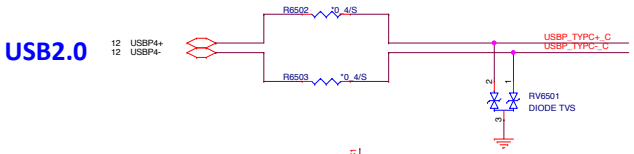
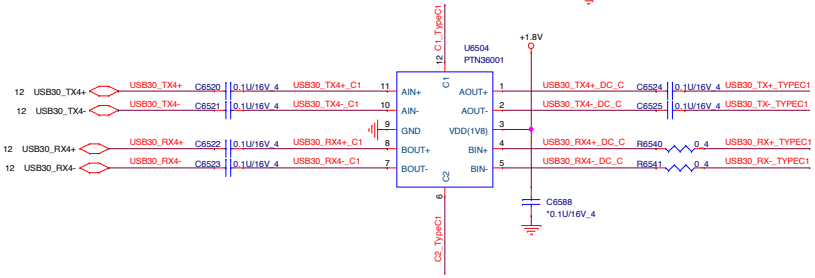
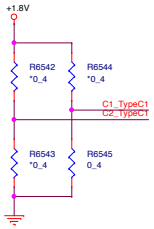
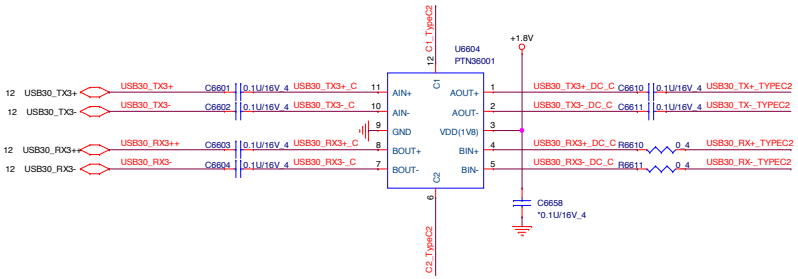
USB TYPE-C - TPS25810

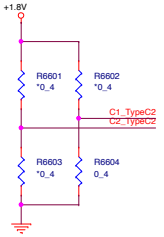
USB2.0



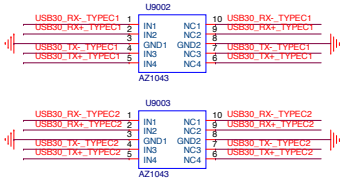


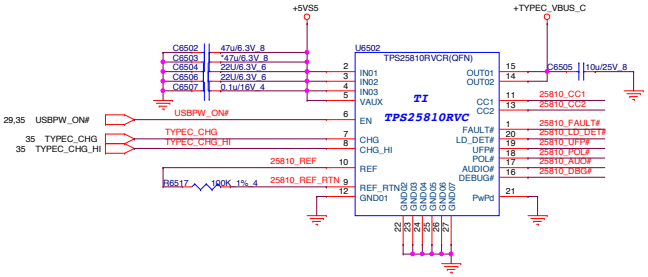


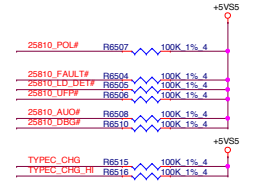




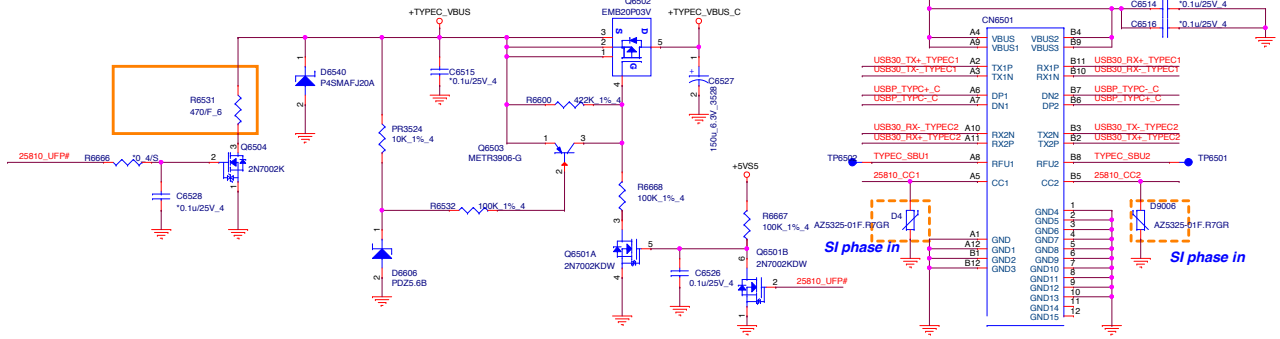
TYPE C USB3.0 ESD

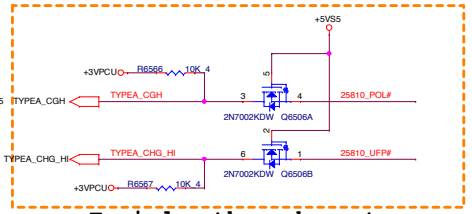






CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A





To judge the usb port for factory

TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

BU5

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Quanta Computer Inc.

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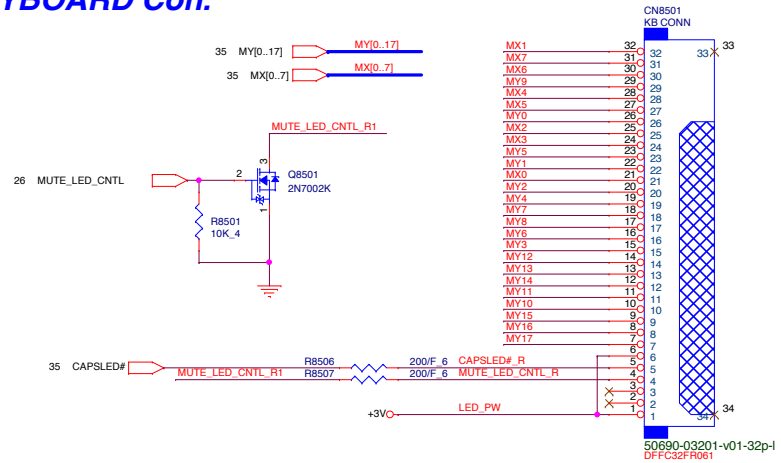
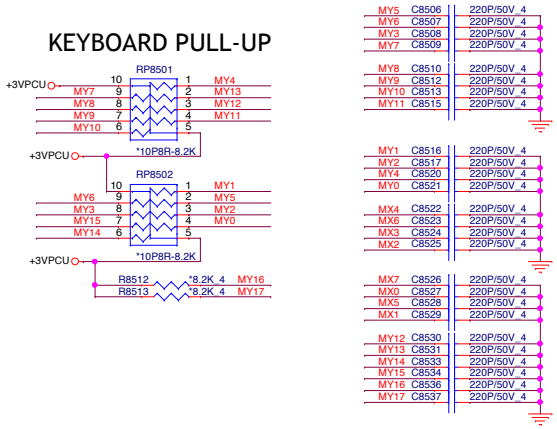
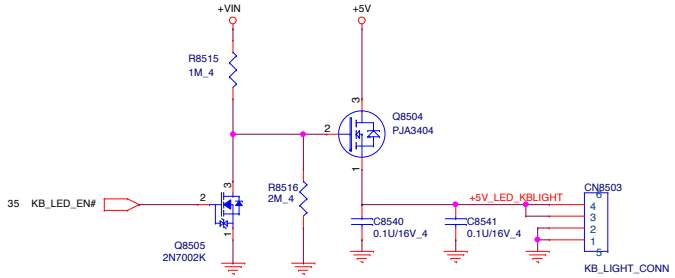
KEYBOARD Con.



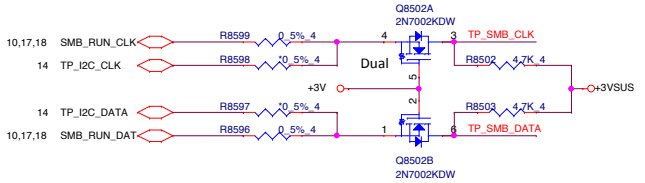
KEYBOARD PULL-UP

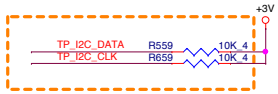


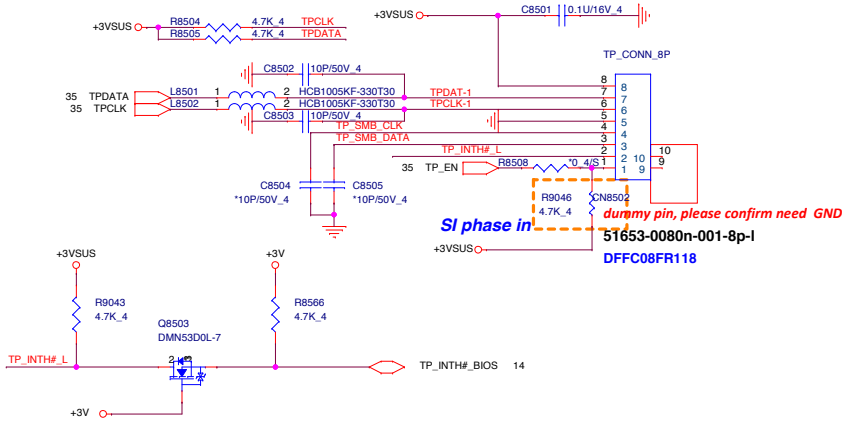
KB LIGHT CONN



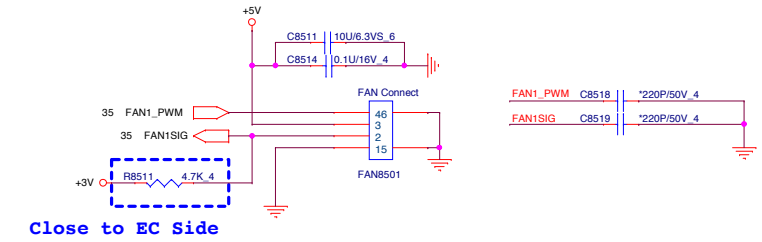
Touch Pad Connector







FAN



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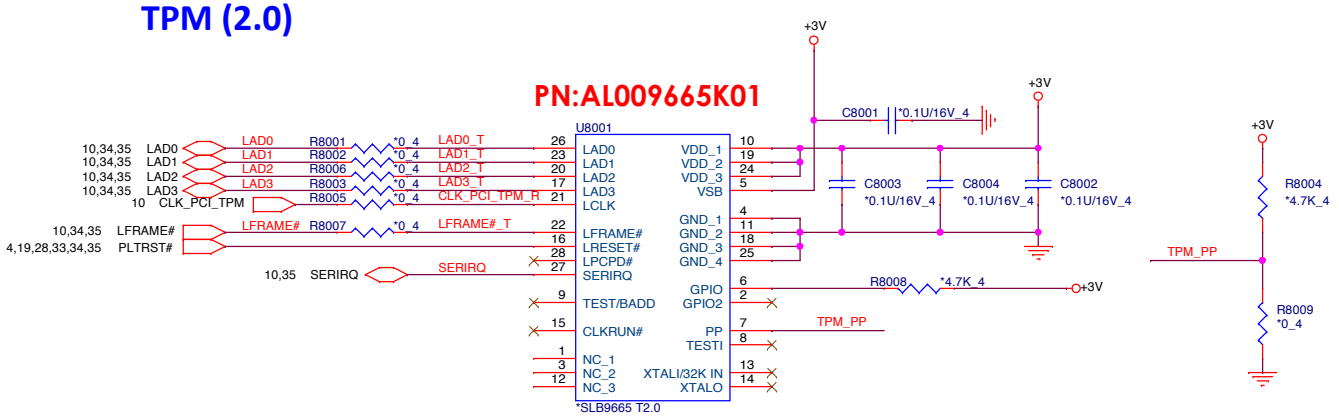
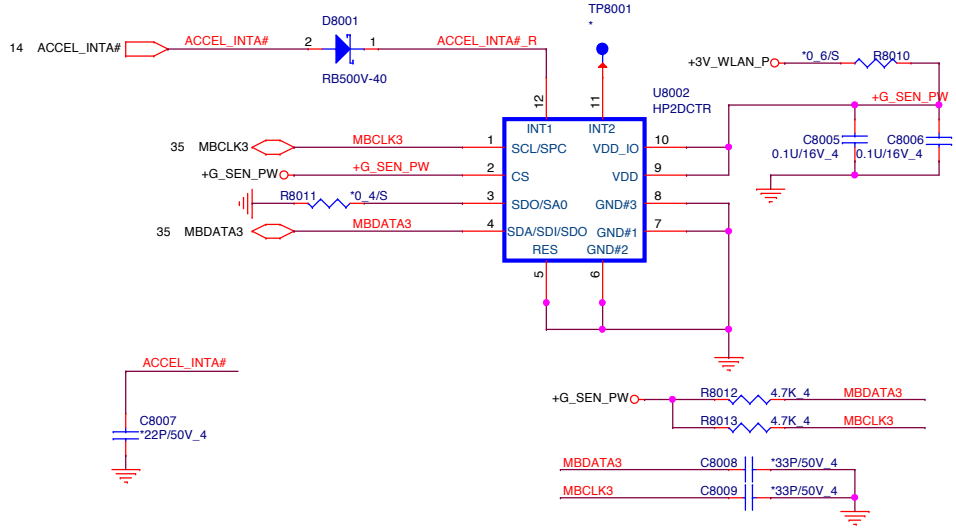
TPM (2.0)

PN:AL009665K01

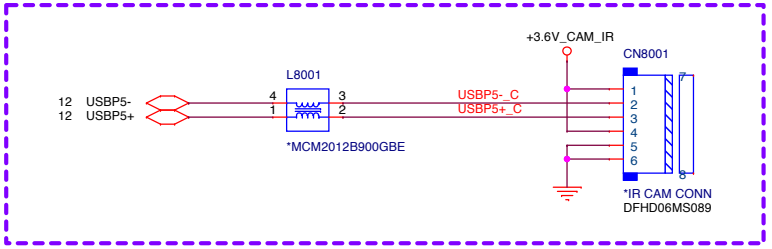


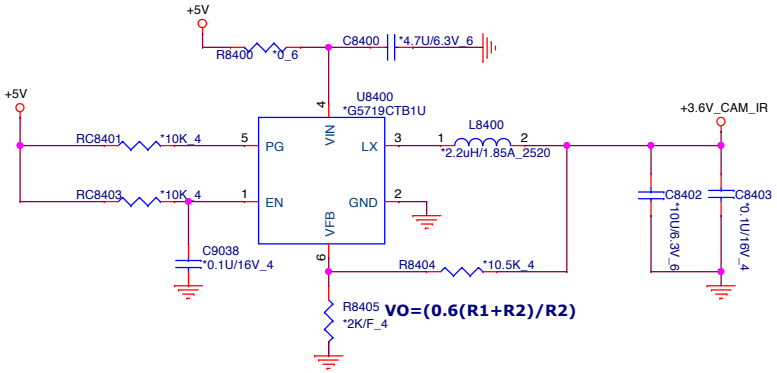
Accelerometer Sensor



IR CAM

current:4A





BU5

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Quanta Computer Inc.

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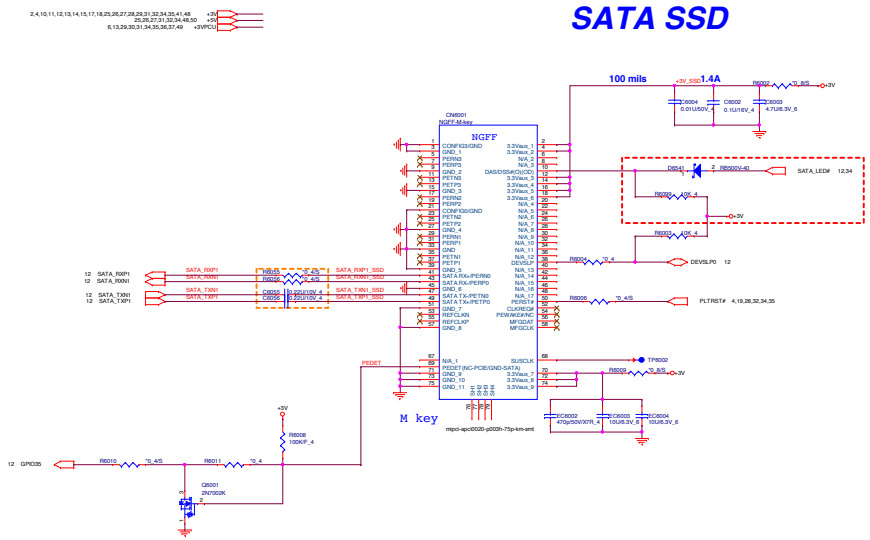
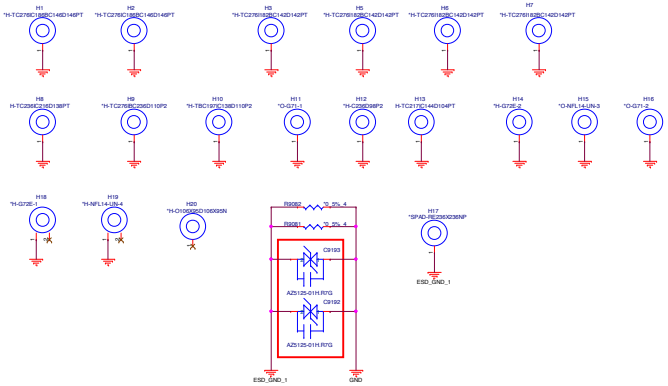
SATA SSD



SATA ODD

Screw Hole



eMMC

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Quanta Computer Inc.	
Size: Custom	Document Number: 35 – SSD_ODD_EMMC_ASM1154
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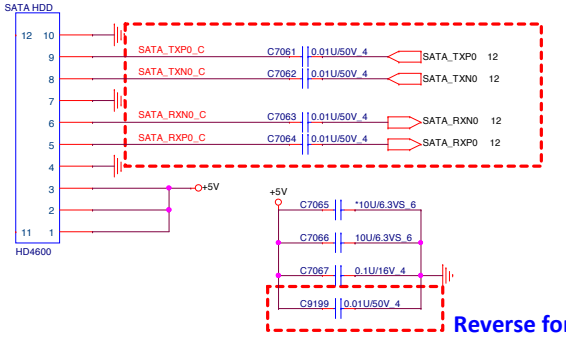
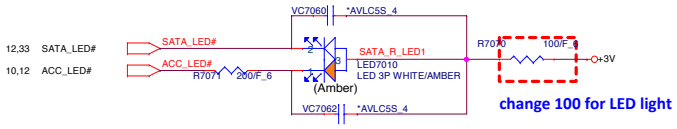
HDD

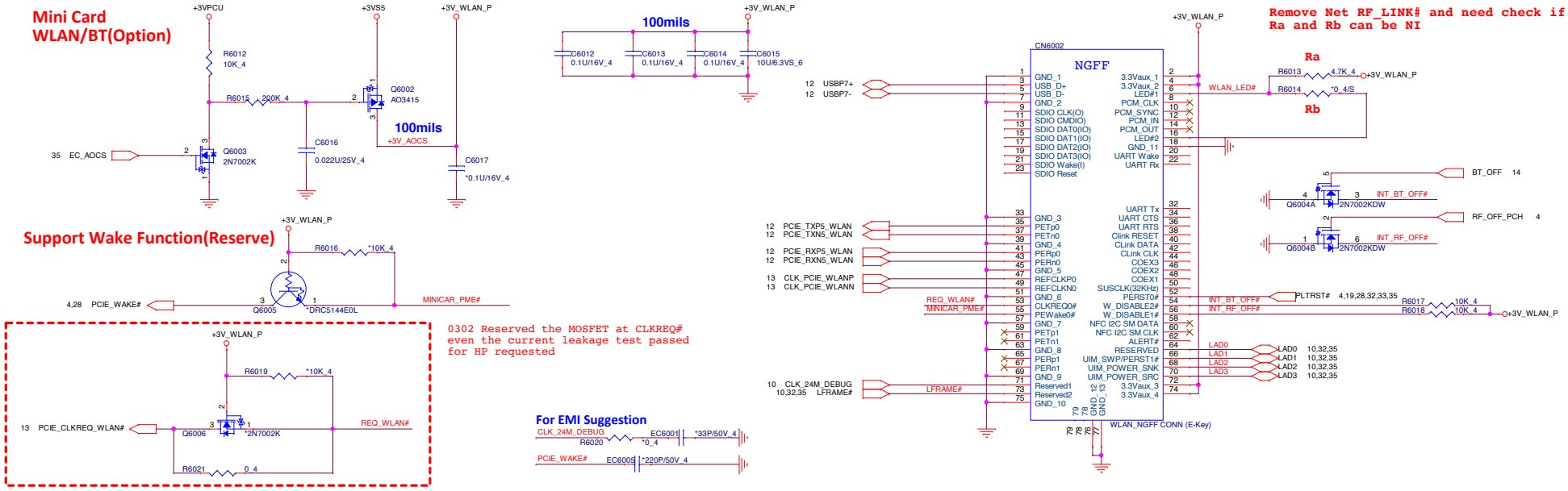
SATA HDD

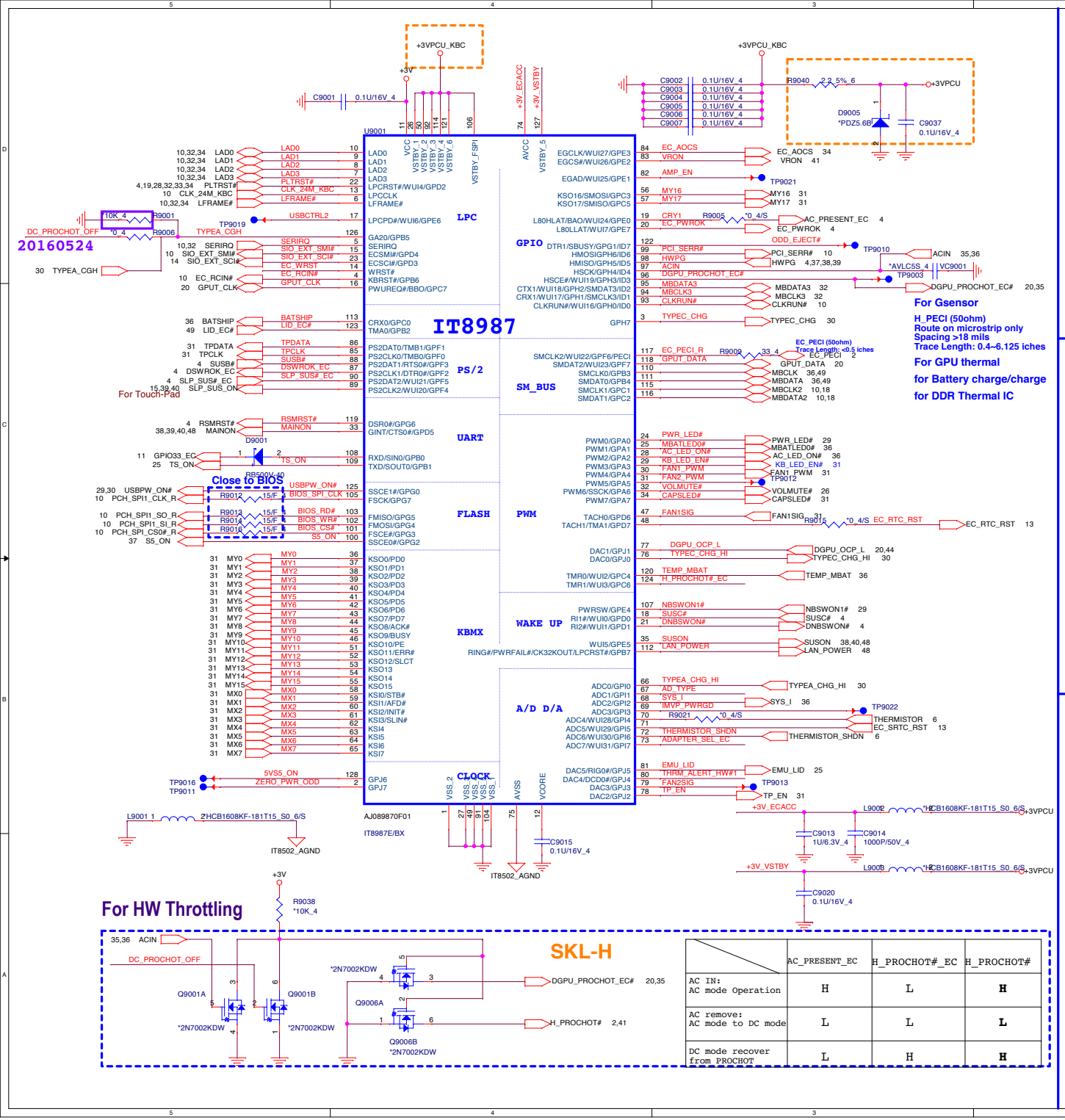


SATA LED



WLAN





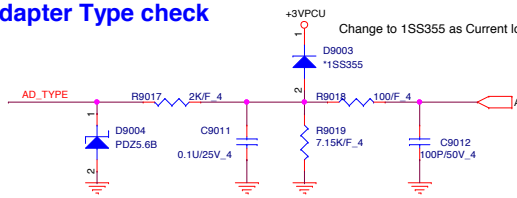
	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

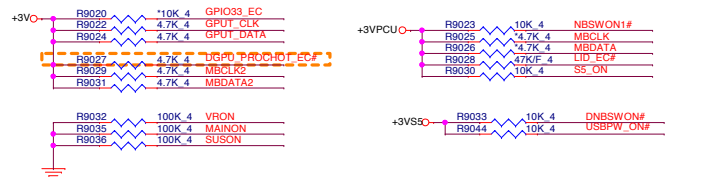
Adapter select for EC

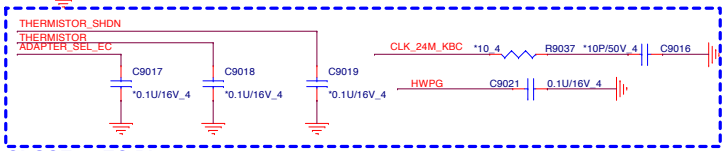
Ra / Rb

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W				
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	3V	
120W	10K(CS31002FB26)		2.25V	
90W	10K(CS31002FB26)		1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB0)	0.75V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

Adapter Type check







CLOSE to EC Pin

2,4,10,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,41,48 +3V
4,10,15,25,34,37,38,39,40,44,47,48,50 +3VS5
6,13,29,30,31,34,36,37,49 +3VPCU

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+3VPCU 6,13,29,30,31,34,35,36,37,49
+5VPCU 26,37,47,48
+BAT_RTC 4,13,15,29,49
+VIN 25,31,37,38,39,42,43,44,45,46,50
+3VPCU 6,13,29,30,31,34,35,36,37,49

ADP=65W

3S1P 41Whr

CN1 51483-00801-V01_Header

N-channel MOS

PQ1 AP0203GMT-HF
PQ2 AON7408
PQ3 AON6414AL

Place this ZVS close to DC_IN conn

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this R&C close to EC

PU9 BQ24738HRGRR

+BAT_RTC SET
BAT= 1S---10-ohm
BAT >2S---100ohm

ACDET

VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

Vacdet=2.4V

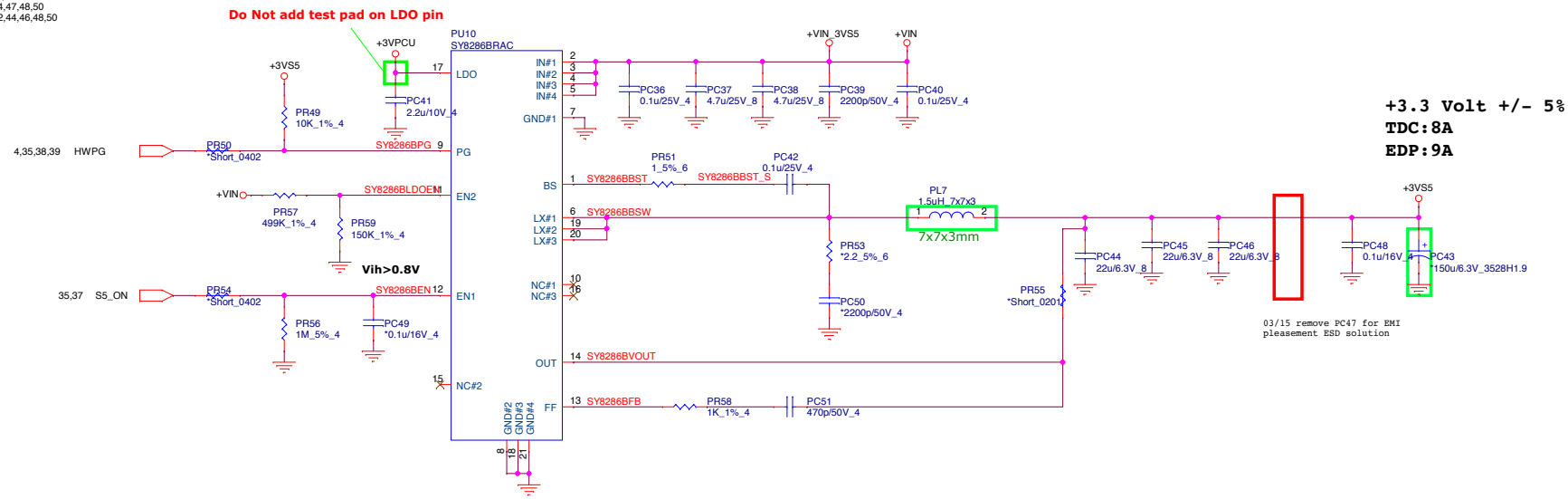
Ra

MIN. BATV=7.2V

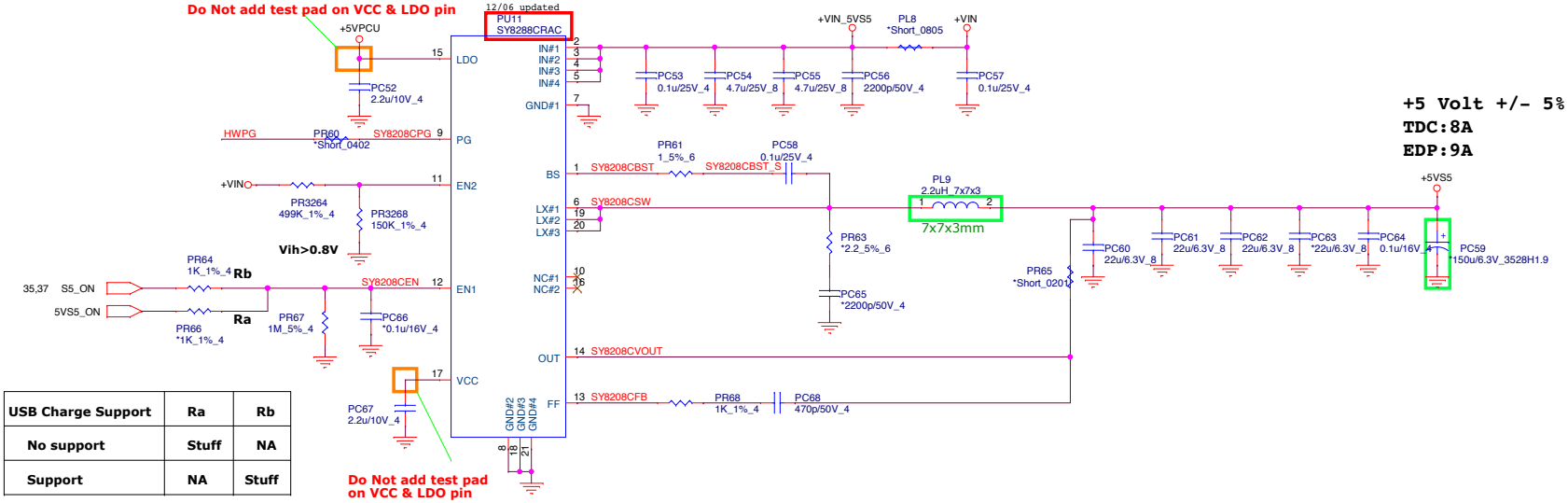
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.		
	Size: Custom	Document Number: Charger (BQ24738H)	Rev: 1A
	Date: Friday, March 24, 2017	Sheet 36 of 51	

DC/DC +3VS5/+5VS5

+VIN 25,31,36,38,39,42,43,44,45,46,50
+3VS5 4,10,15,25,34,35,38,39,40,44,47,48,50
+5VS5 4,25,26,29,30,38,39,40,41,42,44,46,48,50
+3VPCU 6,13,29,30,31,34,35,36,49
+5VPCU 26,36,47,48



+3.3 Volt +/- 5%
TDC:8A
EDP:9A



+5 Volt +/- 5%
TDC:8A
EDP:9A

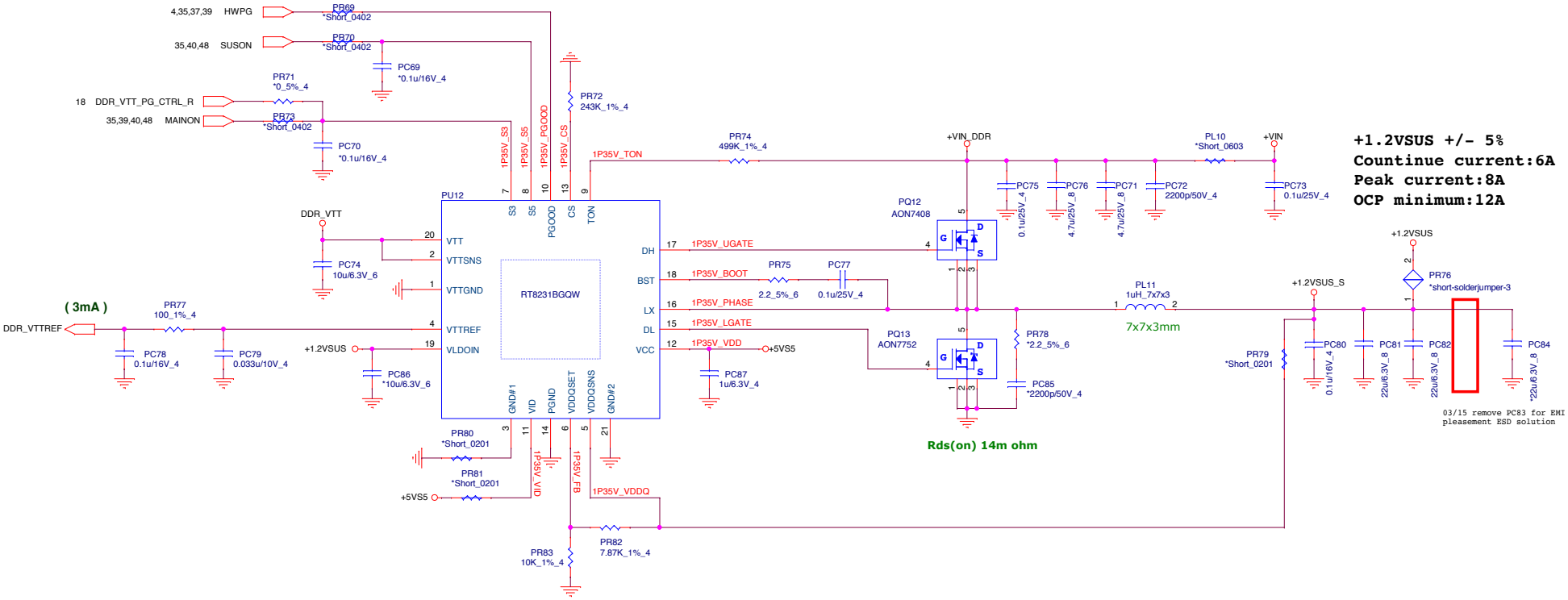
USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

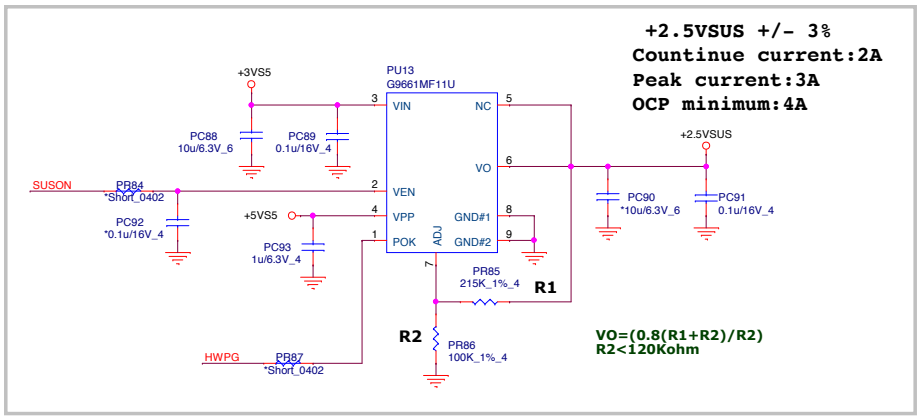
BU5

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Friday, March 24, 2017	Sheet 37 of 51	

+VIN 25,31,36,37,39,42,43,44,45,46,50
+5VS5 4,25,26,29,30,37,39,40,41,42,44,46,48,50
+1.2VSUS 3,6,17,18,40
DDR_VTT 17,18

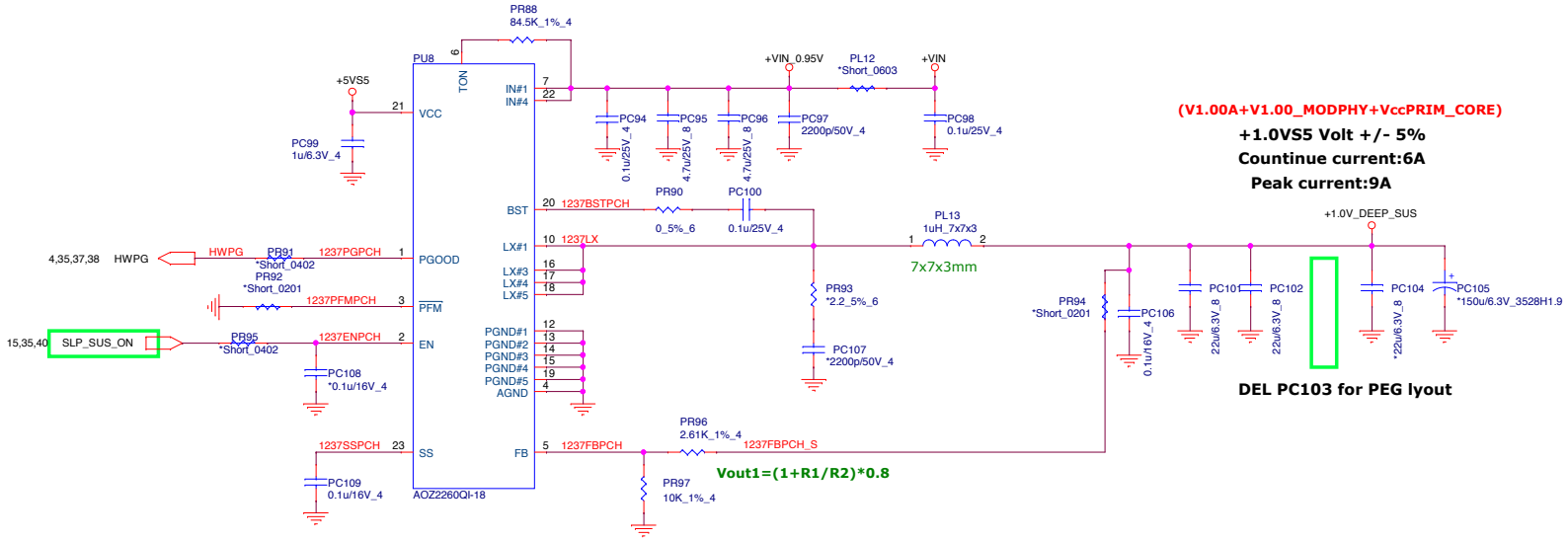


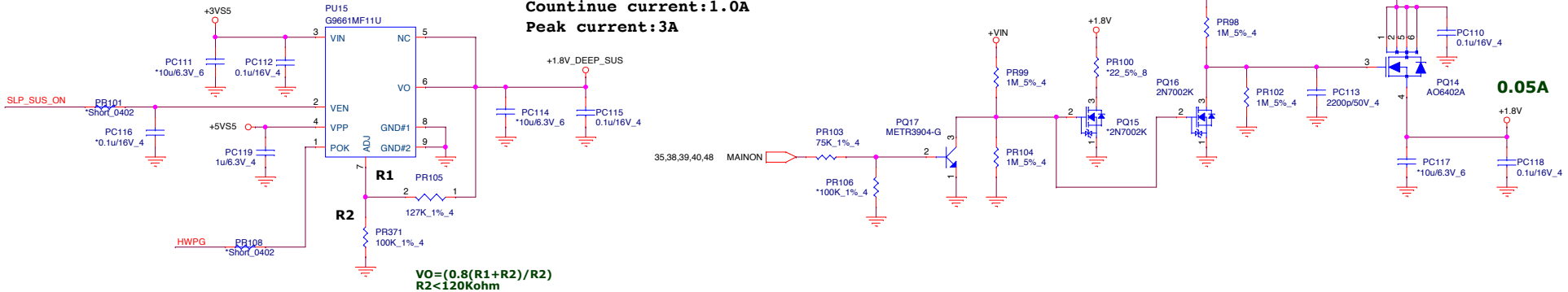
20151015 updated



BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size	Document Number DDR4 (G5619RZ1U)	Rev 1A
Date: Friday, March 24, 2017	Sheet 38 of 51	

+VIN 25,31,36,37,38,42,43,44,45,46,50
+3VS5 4,10,15,25,34,35,37,38,40,44,47,48,50
+5VS5 4,25,26,29,30,37,38,40,41,42,44,46,48,50
+1.0V_DEEP_SUS 9,13,15,40
+1.8V_DEEP_SUS 9,15,47
MAINON 35,38,39,40,48
+1.5V





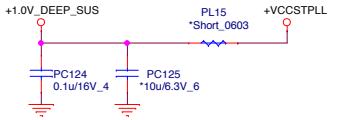
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size: Custom	Document Number: +1.0V/+1.8V_DEEP_SUS	Rev: 1A
Date: Tuesday, March 28, 2017	Sheet 39 of 51	

+1.0V 2,4,6,35
+3VS5 4,10,15,25,34,35,37,38,39,44,47,48,50
+5VS5 4,25,26,29,30,37,38,39,41,42,44,46,48,50
+VCCIO 2,6
+1.2VSUS 3,6,17,18,38
+VCCSTPLL 2,4,5,6,9,41
+1.0V_DEEP_SUS 9,13,15,39
+1.2V_VCCPLL_OC 6
MAINON 35,38,39,48

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

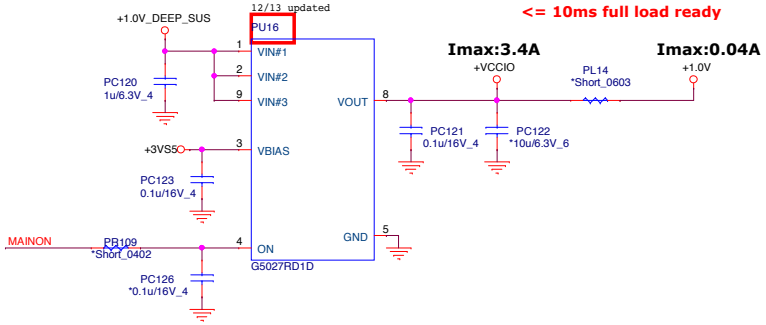
Imax:0.24A

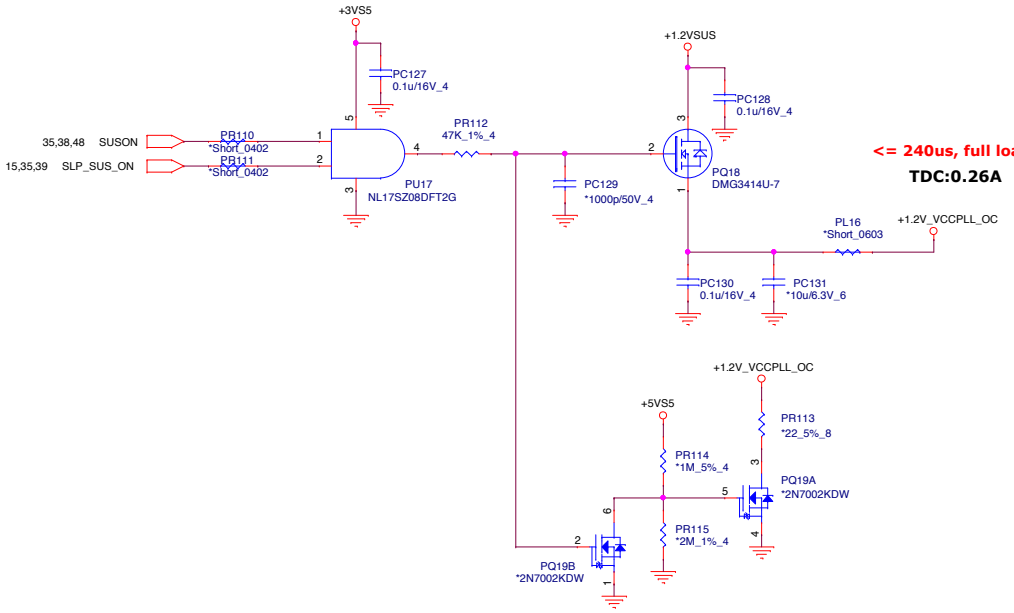


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**





<= 240us, full load ready
TDC:0.26A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A

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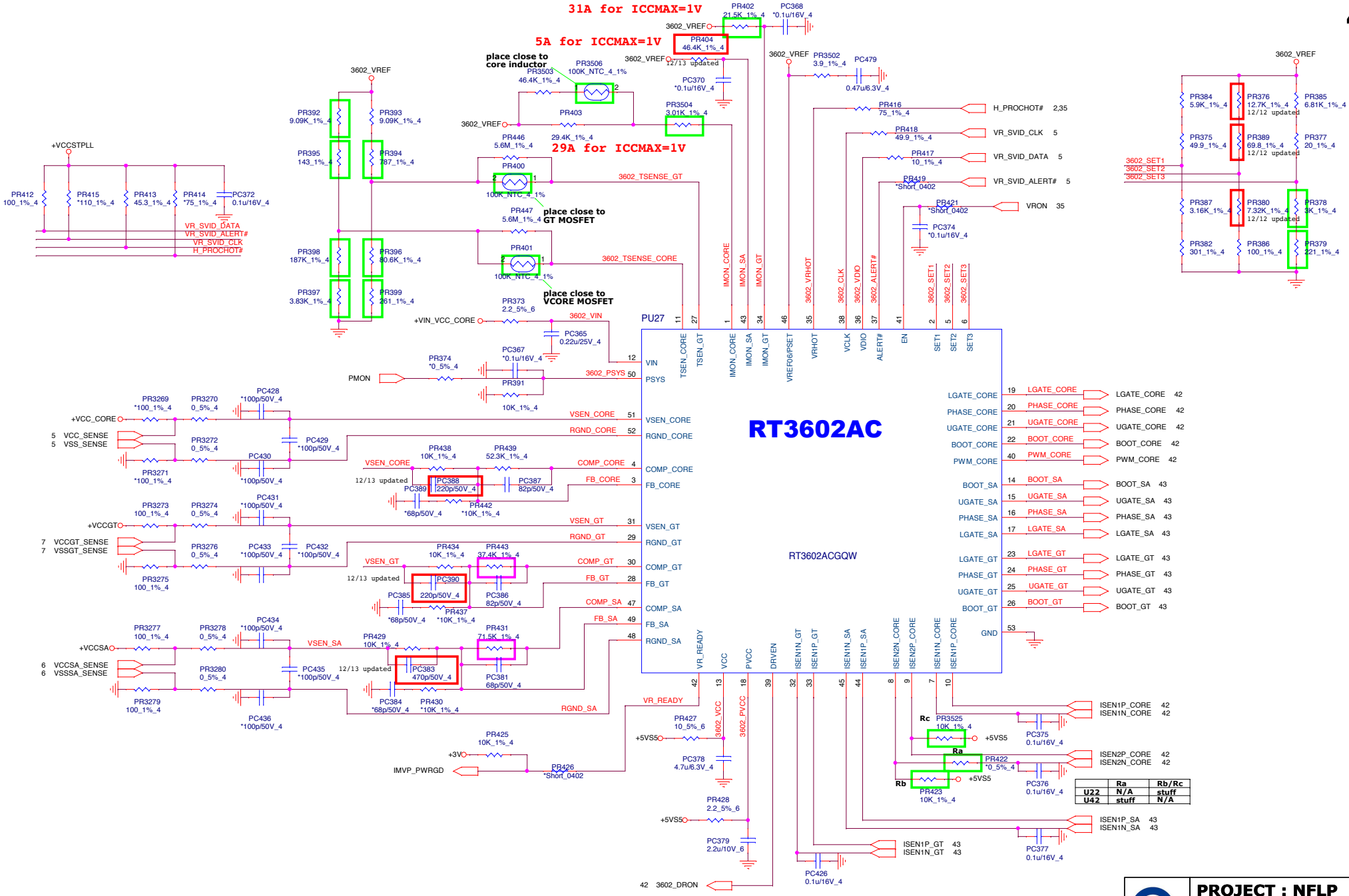

Size	Document Number	Rev
Custom	CPU VR IC (RT3602AC)	2A

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

BU5

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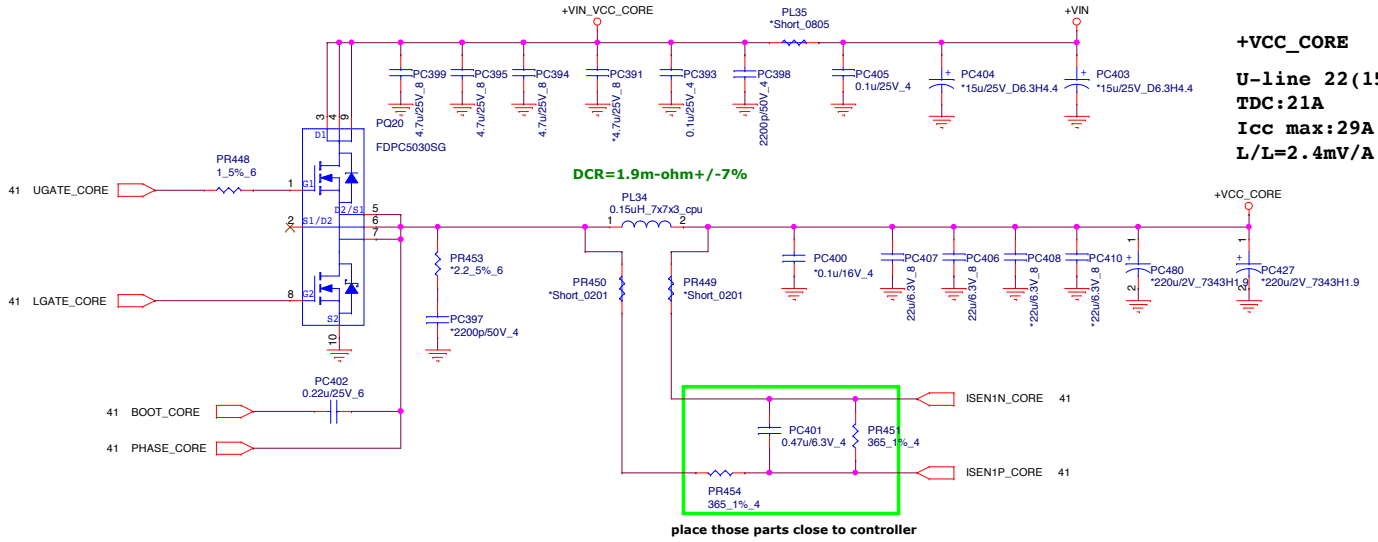
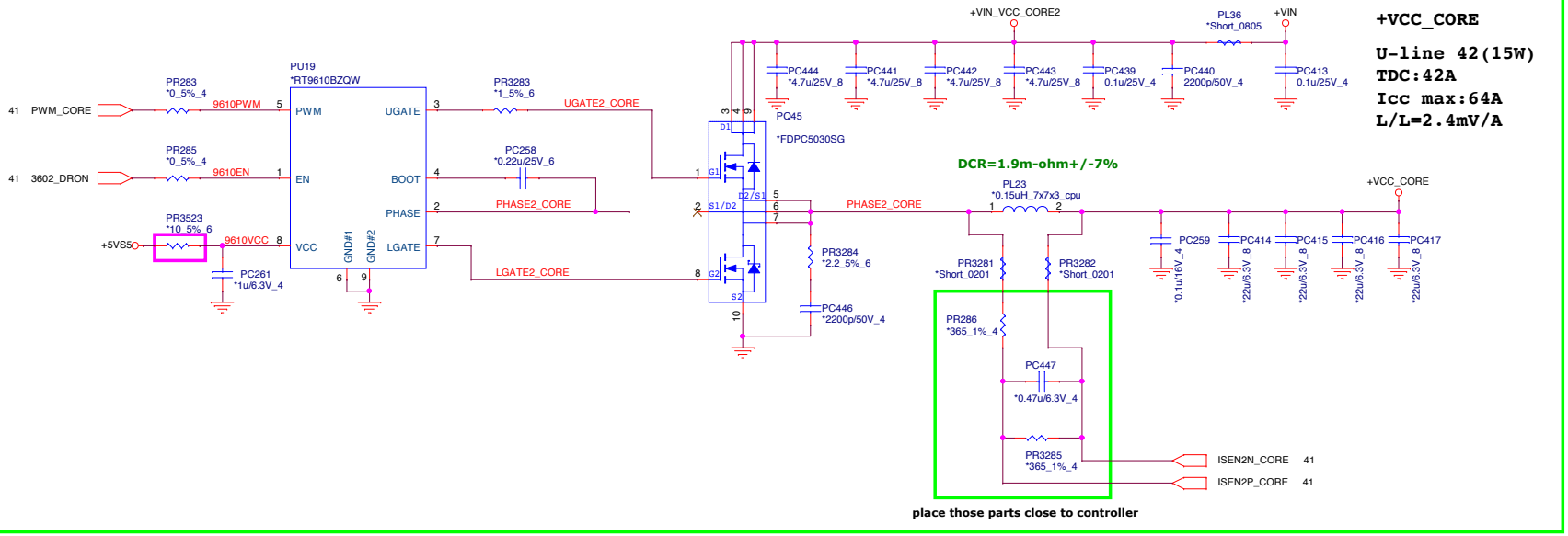
+VIN 25,31,36,37,38,39,43,44,45,46,50
+5VS5 4,25,26,29,30,37,38,39,40,41,44,46,48,50



For U42 --> Add These Components

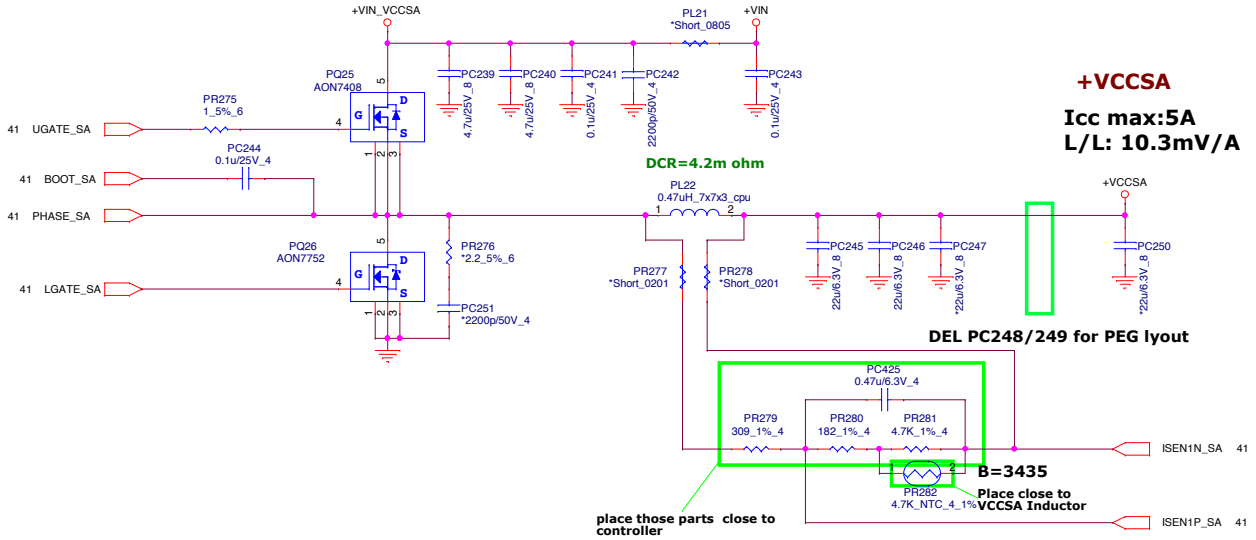


BU5

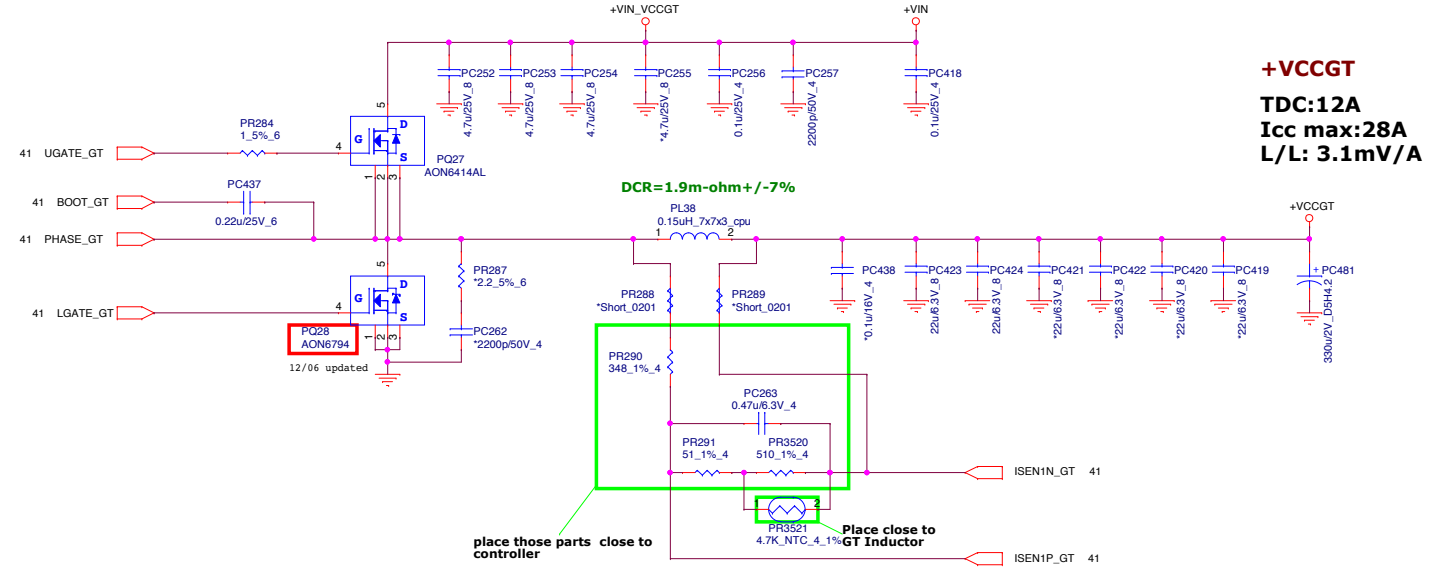
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A
Date: Friday, March 24, 2017	Sheet 42 of 51	

+VIN 25,31,36,37,38,39,42,44,45,46,50
+5VS5 4,25,26,29,30,37,38,39,40,41,42,44,46,48,50
+VCCSA 6,41
+VCCGT 7,41



+VCCSA
Icc max:5A
L/L: 10.3mV/A



+VCCGT
TDC:12A
Icc max:28A
L/L: 3.1mV/A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A
Date: Friday, March 24, 2017	Sheet 43 of 51	

R17M-M1-70

+1.8V_VGA

PR3528 10K_1%_4
PR3529 *10K_1%_4
PC483 0.1u/16V_4
3662SVC
3662SVD
PR3531 *10K_1%_4
PR3532 10K_1%_4

VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

8899VCC
PR3526 4.7_5%_4
+5VS5
PC482 2.2u/10V_4
8899PVCC
PR3527 *Short_0402
+5VS5
PC484 2.2u/10V_4
+VIN_GPU
PC485 0.1u/25V_4
PR3530 4.7_5%_4
PR3533 1_5%_6

PU28
RT3662EBGQW

NC 22
VCC 14
PVCC 27
VIN 1
SET1 11
TSEN 10
EN 32
VDDIO 19
PWROK 15
SVC 16
SVD 17
SVT 18
PGOOD 20
VRHOT_L 9
IMON 12
VREF_PINSET 13
GND 33

UGATE1 24 3662UGATE1 → 3662UGATE1_G 45
BOOT1 23 3662BOOT1
PHASE1 25 3662LX1 → 3662LX1 45
LGATE1 26 3662LGATE1 → 3662LGATE1 45
ISEN1P 7 3662ISEN1P_1
ISEN1N 8 3662ISEN1N_1
UGATE2 30 3662UGATE2 → 3662UGATE2_G 45
BOOT2 31 3662BOOT2
PHASE2 29 3662LX2 → 3662LX2 45
LGATE2 28 3662LGATE2 → 3662LGATE2 45
ISEN2P 5 3662ISEN2P_1
ISEN2N 6 3662ISEN2N_1
COMP 3 3662COMPA
FB 4 3662FBA
VSEN 21
RGND 2

VREF_PINSET
PR3534 10K_1%_4
PR3535 48.7K_1%_4
3662SET1
PR3543 10K_1%_4
PR3536 2.94K_1%_4

VREF_PINSET
PR3537 60.4K_1%_4
PR3538 6.04K_1%_4
PR3539 60.4K_1%_4
3662TSEN
PR3540 10K_1%_4
PR3541 23.7K_1%_4
PR3542 100K_NTC_4_1%

PD1002
RB500V-40
Put close to VGACORE HOT SPOT
12,20,47 DGPU_PR_EN
46 3662EN
PR3545 10K_1%_4
PC488 0.47u/6.3V_4
Vih=2V

3V_VGA
1.8V_VGA
PR3548 *2.2_5%_6
PR3549 2.2_5%_6
R17M-M1-30
R17M-M1-70
PC490 1u/6.3V_4

PR3351 *Short_0201
DGPU_PWROK
PR3553 *Short_0201
20 SVI2_CLK
PR3554 *Short_0201
20 SVI2_DATA
PR3556 *Short_0201
20 SVI2_SVT

12,35,46,47 DGPU_PWROK
DGPU_PWROK
PR3560 *Short_0201
+3VS5
PR3559 10K_1%_4

+3VS5
PR3561 *10K_1%_4
20,35 DGPU_OCP_L
PR3564 *Short_0402

Put close to VGACORE hot sport PHASE 1
R1
PR3565 6.98K_1%_4
PC496 *100p/50V_4
R2
PR3569 14K_1%_4
R3
PR3570 11K_1%_4
PR3568 100K_NTC_4_1%
PR3571 3.9_1%_4
PC498 0.47u/6.3V_4

PR3544 3.3K_1%_4
PC487 0.47u/6.3V_4
PR3546 357_1%_4
PC489 0.1u/16V_4
PR3547 0_5%_4
3662ISEN1P 45
3662ISEN1N 45

PC486 0.1u/25V_4
PC491 0.1u/25V_4

PR3552 3.3K_1%_4
PC492 0.47u/6.3V_4
PR3555 357_1%_4
PC493 0.1u/16V_4
PR3557 0_5%_4
3662ISEN2P 45
3662ISEN2N 45
Unstuff
1 Phase setting

PR3558 *10K_1%_2 +5VS5 stuff 1 Phase setting

PC494 68p/50V_4
12/16 updated
PC495 270p/50V_4
PR3562 56.2K_1%_4
PR3563 10K_1%_4
R4
+VGA_CORE
PR3566 10_1%_4
PR3567 0_5%_4
VGPU_CORE_SENSE_SRC
PC497 *82p/50V_4
VSS_GPU_SENSE_SRC
VGPU_CORE_SENSE 22
VSS_GPU_SENSE 22
PR3572 10_1%_4

	1 Phase setting	
R1		
R2		
R3		

	1 Phase setting	
R4		

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC ENE KB9027B	1A

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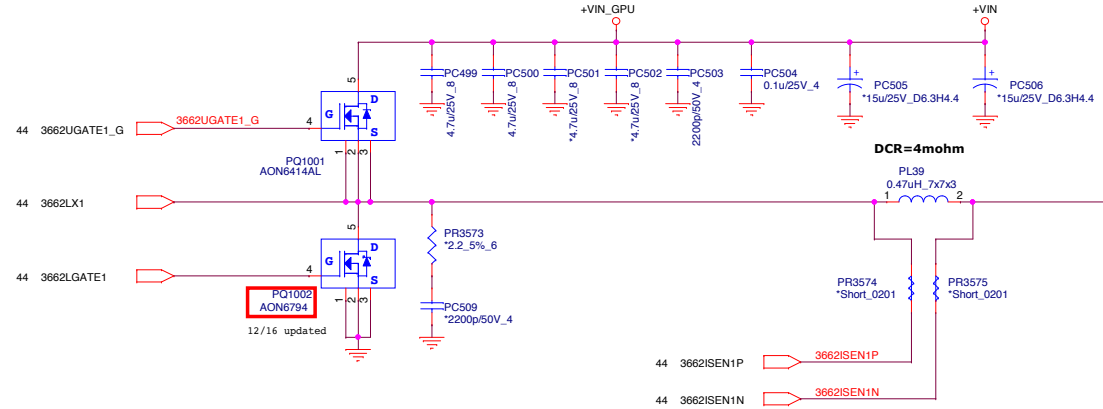
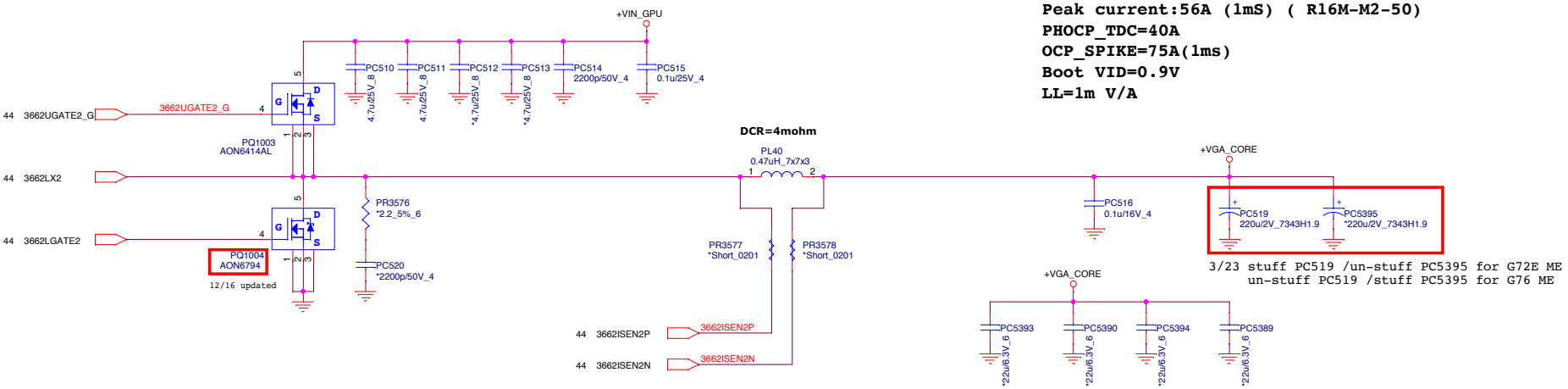


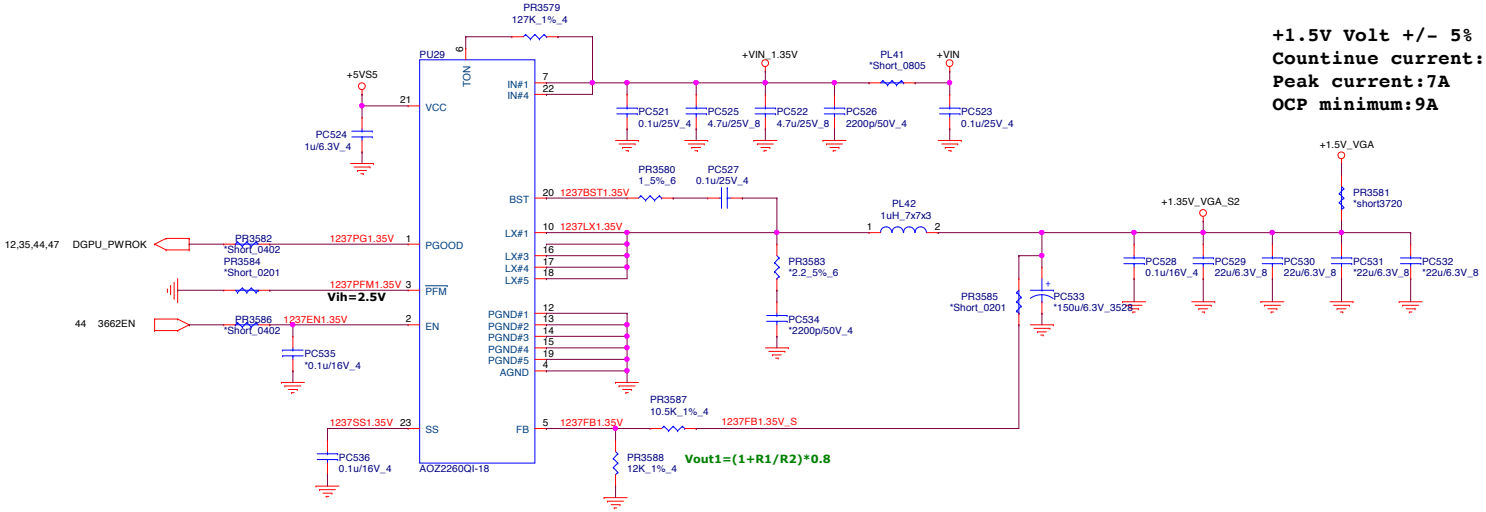
VGACORE (R17M-M1-30_ 25W/38W(1ms))
Countinue current:28A
Peak current=38A (1ms)
PHOCP_TDC=40A (soft-start only)
OCP_SPIKE=55A(1ms)
Boot VID=0.9V
LL=1m V/A



VGACORE (R16M-M2-50_ 37W/56W(1ms))
Countinue current:40A (R16M-M2-50)
Peak current:56A (1mS) (R16M-M2-50)
PHOCP_TDC=40A
OCP_SPIKE=75A(1ms)
Boot VID=0.9V
LL=1m V/A

3/23 stuff PC519 /un-stuff PC5395 for G72E ME
un-stuff PC519 /stuff PC5395 for G76 ME

NB5	**PROJECT : 0P1B** Quanta Computer Inc.	
Size: Custom	Document Number: EC ENE KB9027B	Rev: 1A
Date: Friday, March 24, 2017	Sheet 45of 15	



+1.5V Volt +/- 5%
Countinue current:6A
Peak current:7A
OCP minimum:9A

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

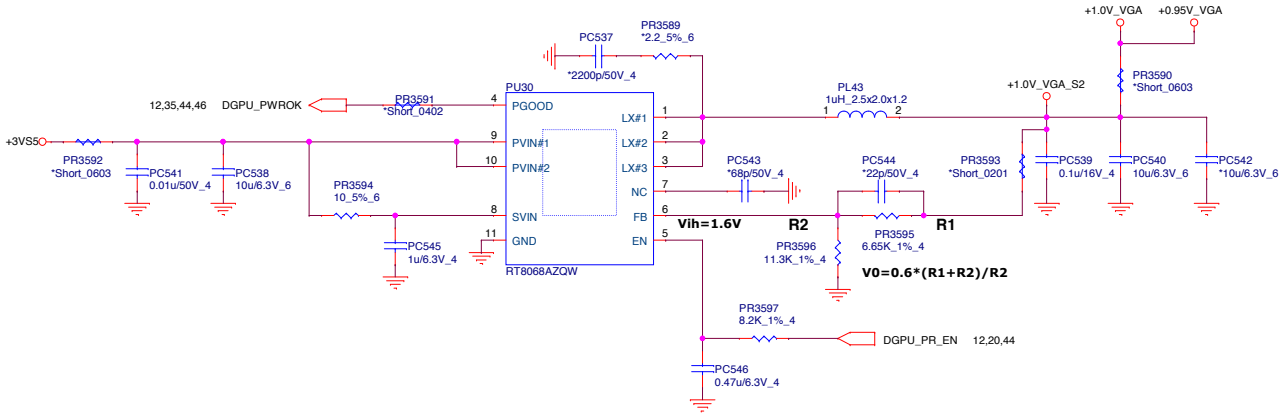
NB5

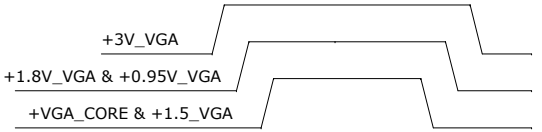
PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC ENE KB9027B	1A

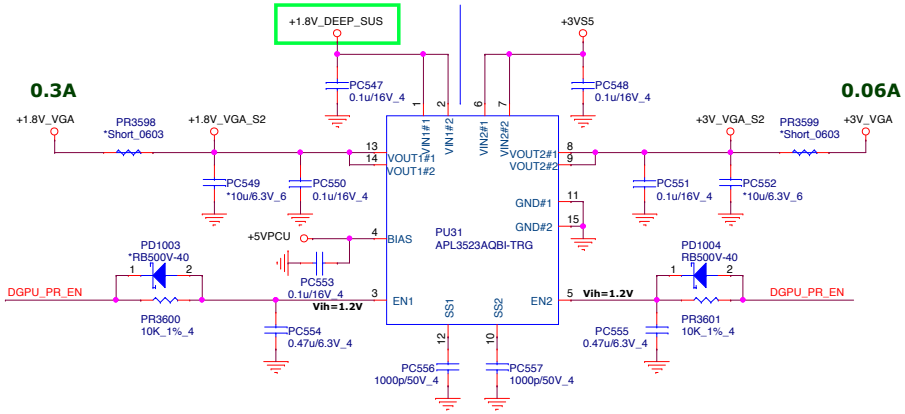
Date: Friday, March 24, 2017 | Sheet 46of 15

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



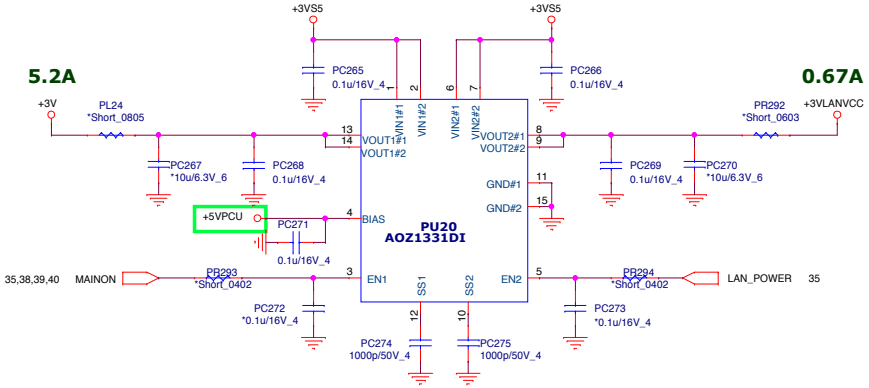


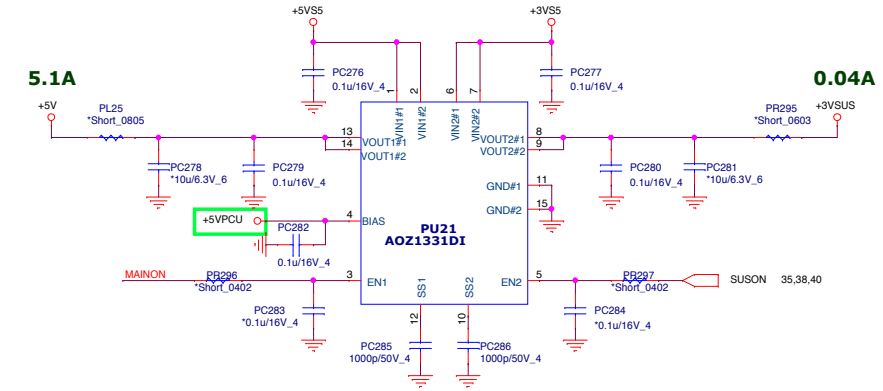
PUT COLSE TO +1.8V power.



NB5	**PROJECT : 0P1B** Quanta Computer Inc.	
Size: Custom	Document Number: **EC ENE KB9027B**	Rev: 1A
Date: Friday, March 24, 2017	Sheet: 47of 15	

+3V 2,4,10,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41
+5V 25,26,27,31,32,34,50
+VIN 25,31,36,37,38,39,42,43,44,45,46,50
+3VS5 4,10,15,25,34,35,37,38,39,40,44,47,50
+5VS5 4,25,26,29,30,37,38,39,40,41,42,44,46,50
+3VSUS 31
+5VPCU 26,36,37,47
+3VLANVCC 28



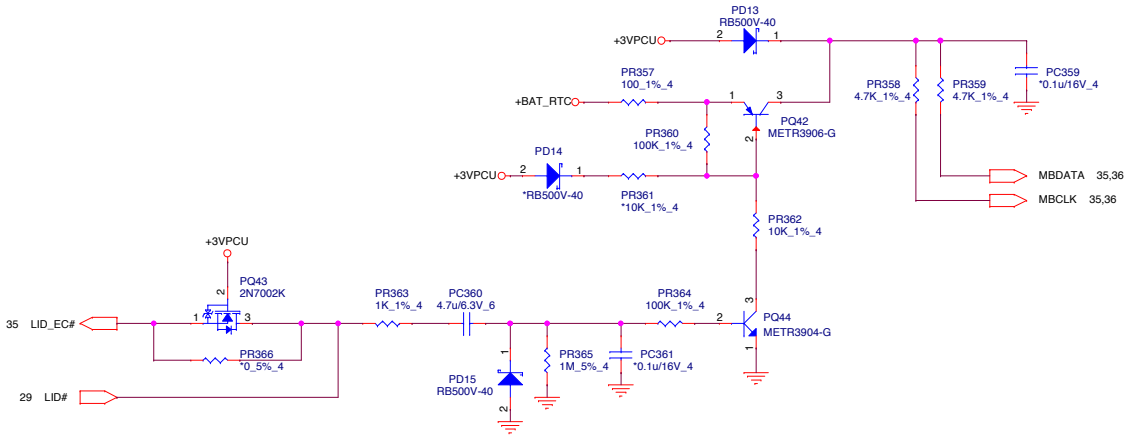


BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A
Date: Friday, March 24, 2017	Sheet 48 of 51	

+3VPCU 6,13,29,30,31,34,35,36,37
+BAT_RTC 4,13,15,29,36

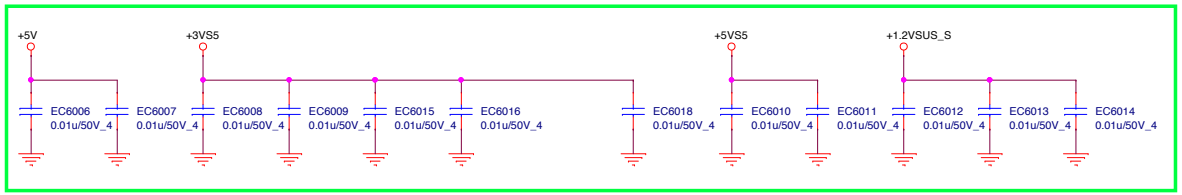


BU5

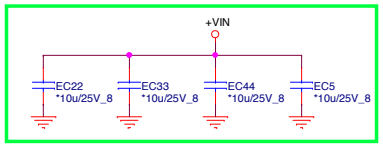
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LID SW for storage mode	1A
Date: Friday, March 24, 2017	Sheet 49 of 51	

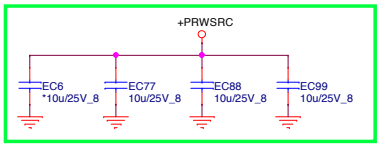
EMI request for ESD 03/21 updated



EMI request for ISN



EMI request for ISN



BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI solution	1A

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