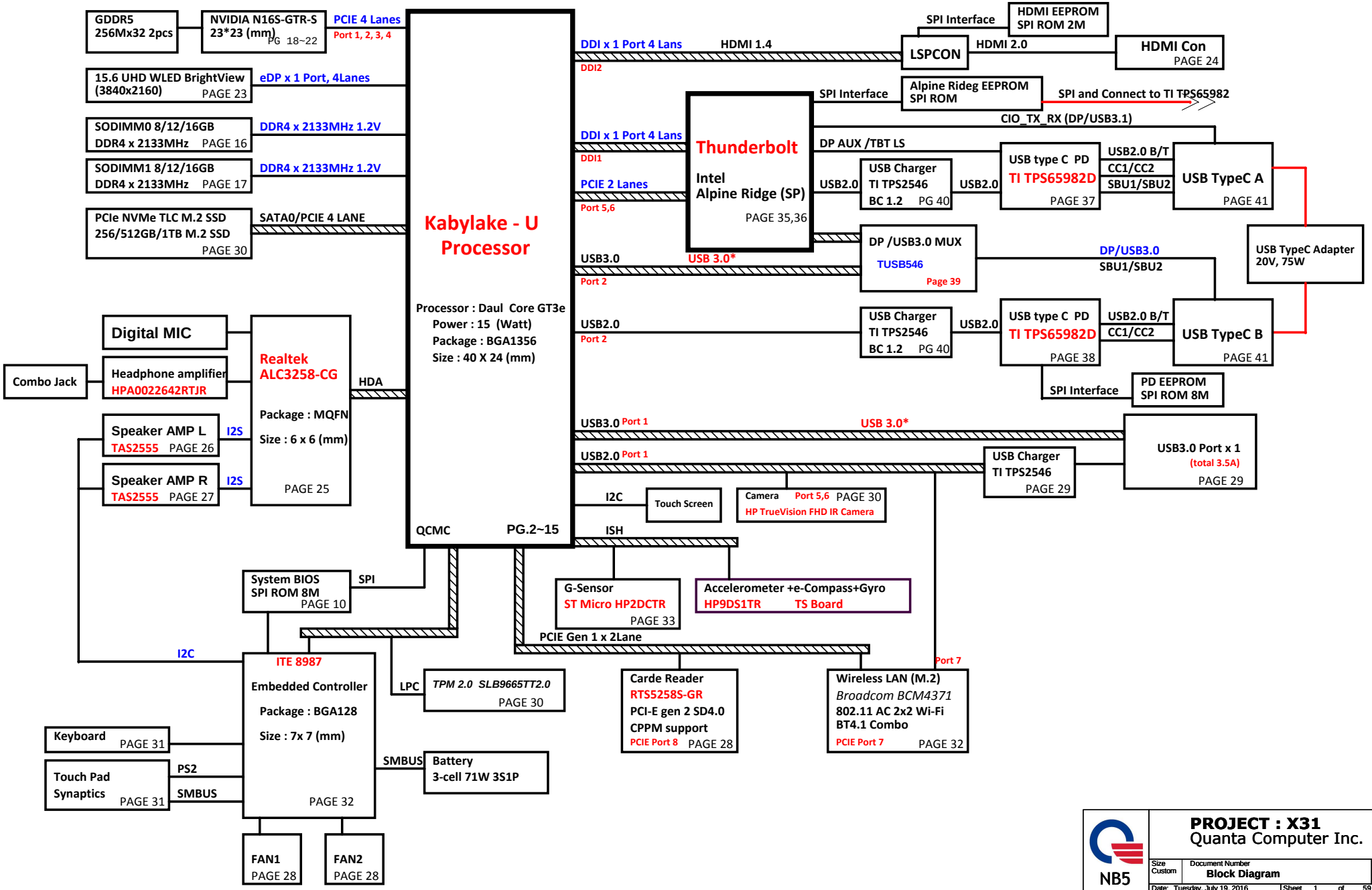
# Monster Intel KABY LAKE ULT Platform Block Diagram

01

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|---|---|---|
| Custom | Block Diagram | |

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I'm from VIETNAM sualaptop365

+3V
INT_DP_SCL R131 2.2K_2
INT_DP_SDA R133 2.2K_2
SDVO_CLK R121 2.2K_2
SDVO_DATA R123 2.2K_2

Kris Modify 20160520

U16A SKL_ULT ? Need apply PN

35 DDI1_TX0_DN E55
35 DDI1_TX0_DP F55
35 DDI1_TX1_DN E58
35 DDI1_TX1_DP F58
35 DDI1_TX2_DN F53
35 DDI1_TX2_DP G53
35 DDI1_TX3_DN F56
35 DDI1_TX3_DP G56

24 IN_D0# C50
24 IN_D0 D50
24 IN_D1# C52
24 IN_D1 D52
24 IN_D2# A50
24 IN_D2 B50
24 IN_CLK# D51
24 IN_CLK C51

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]
DDI
DISPLAY SIDEBANDS

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 23
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 23
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 23
EDP_TXP[1] C45 INT_EDP_TXP1 → INT_EDP_TXP1 23
EDP_TXN[2] A45 INT_EDP_TXN2 → INT_EDP_TXN2 23
EDP_TXP[2] B45 INT_EDP_TXP2 → INT_EDP_TXP2 23
EDP_TXN[3] A47 INT_EDP_TXN3 → INT_EDP_TXN3 23
EDP_TXP[3] B47 INT_EDP_TXP3 → INT_EDP_TXP3 23
EDP

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN 23
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP 23
EDP_DISP_UTIL B52

DDI1_AUXN G50 → DDI1_AUX_DN 35
DDI1_AUXP F50 → DDI1_AUX_DP 35
DDI2_AUXN E48 → DDI2_AUX_DN 24
DDI2_AUXP F48 → DDI2_AUX_DP 24
DDI3_AUXN G46
DDI3_AUXP E46

SDVO_CLK L13
SDVO_DATA L12
INT_DP_SCL N7
INT_DP_SDA N8
N11
DDPD_CTRLDATA N12
+VCCIO R310 24.9/F_2 EDP_RCOMP E52

GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA
EDP_RCOMP

GPP_E13/DDPB_HPD0 L9 → DDI1_HPD0 35
GPP_E14/DDPC_HPD1 L7 → DDI2_HPD0 24
GPP_E15/DDPD_HPD2 L6 → GPU_EVENT# 21
GPP_E16/DDPE_HPD3 N9 → DGPU_PWROK 20,34,56
GPP_E17/EDP_HPD L10 ULT_EDP_HPD → ULT_EDP_HPD 23

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON 23
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM 23
EDP_VDDEN U13 PCH_DISP_ON → PCH_DISP_ON 23

*SKL_ULT
REV = 1
1 OF 20
?

DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.
DDPD_CTRLDATA R129 10K_2

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!
+3V
R144 *10K_2
ULT_EDP_HPD
R147 100K_2

0718 R107 unstuff
DDI2_HPD0 R107 *100K/F_2

Jun Modify 20160414

+3V 4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55
+1.0V 4,6,34,49
+VCCIO 6,49
+VCCSTPLL 5,6,9,49,50

+VCCSTPLL
R316 *49.9/F_2 CATERR# D63
EC_PECI A54
PROCHOT# C65
PM_THRMTRIP# C63
A65
34,45,50 H_PROCHOT# R299 499/F_4
34 EC_PECI
34 PM_THRMTRIP#

U16D SKL_ULT ? Need apply PN

CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
CPU MISC
C55 BPM#[0]
D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

19,57 DGPU_PWR_EN A6
19,21 GC6_FB_EN A7
BA5
AY5
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

R162 49.9/F_2 PROC_POPIRCOMP AT16
R161 49.9/F_2 PCH_OPI_RCOMP AU16
R344 49.9/F_2 EDRAM_OPIO_RCOMP H66
R345 49.9/F_2 EOPIO_RCOMP H65
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG
PROC_TCK B61 XDP_TCK0
PROC_TDI D60 XDP_TDI_CPU
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU
PROC_TRST# B59 XDP_TRST#
B56 JTAG_TCK_PCH
PCH_JTAG_TCK D59 JTAG_TDI_PCH R314 0_2 XDP_TDI_CPU
PCH_JTAG_TDI A56 JTAG_TDO_PCH R308 0_2 XDP_TDO_CPU
PCH_JTAG_TDO C59 JTAG_TMS_PCH R307 0_2 XDP_TMS_CPU
PCH_JTAG_TMS C61 XDP_TRST#_CPU R287 0_2 XDP_TRST#
PCH_TRST# A59 JTAGX_PCH R286 0_2 XDP_TCK0
JTAGX

*SKL_ULT
REV = 1
4 OF 20

+1.0V
R284 1K_2 H_PROCHOT#

Close to EC
+VCCSTPLL
PM_THRMTRIP# R285 1K_2

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

+1.0V
JTAG_TMS_PCH R288 51_2
JTAG_TDI_PCH R290 51_2
JTAG_TDO_PCH R289 51_2
JTAG_TCK_PCH R309 51_2
XDP_TCK0 R317 51_2
XDP_TRST#_CPU R318 51_2
Close to Chipset

For GPU
+3V
R342 10K_2
DGPU_PWR_EN
R354 *10K_2
+3V
R888 10K/F_4
DGPU_PWROK

0512 SI Add R888 10K pu +3V

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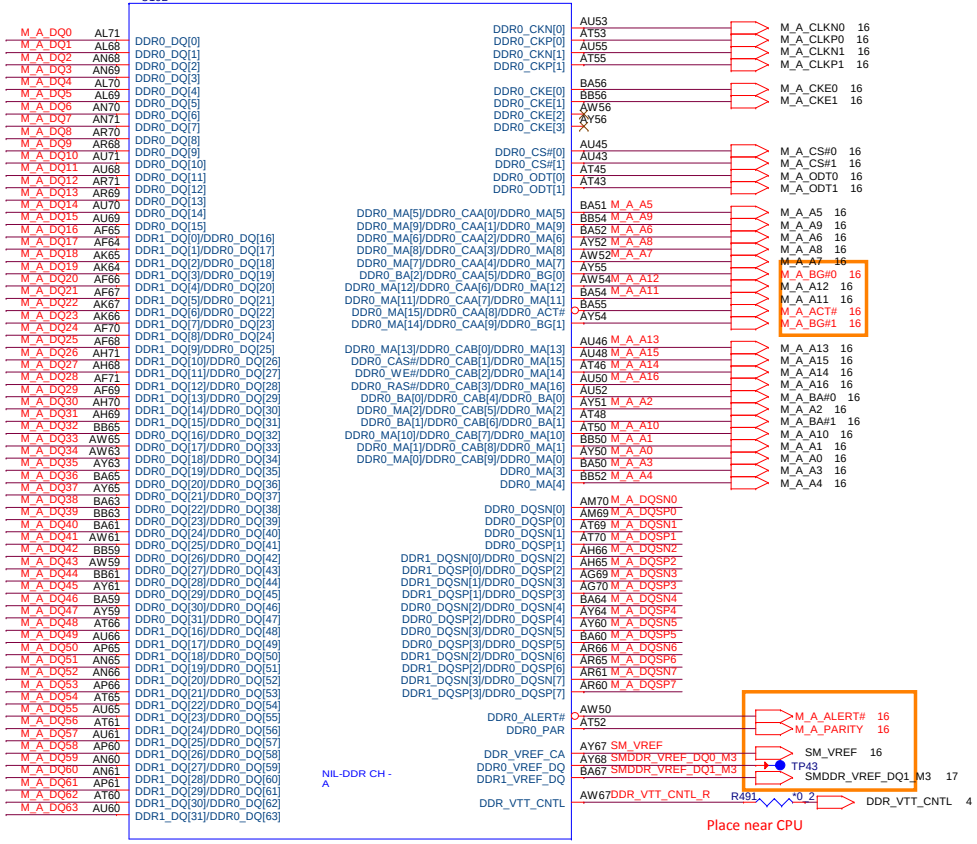
# KABYLAKE ULT Processor DDR4

16 M_A_DQSN[7:0]
16 M_A_DQSP[7:0]
17 M_B_DQSN[7:0]
17 M_B_DQSP[7:0]
16 M_A_DQ[63:0]
17 M_B_DQ[63:0]
+1.2VSUS 6,16,17,24,47,49,57,59

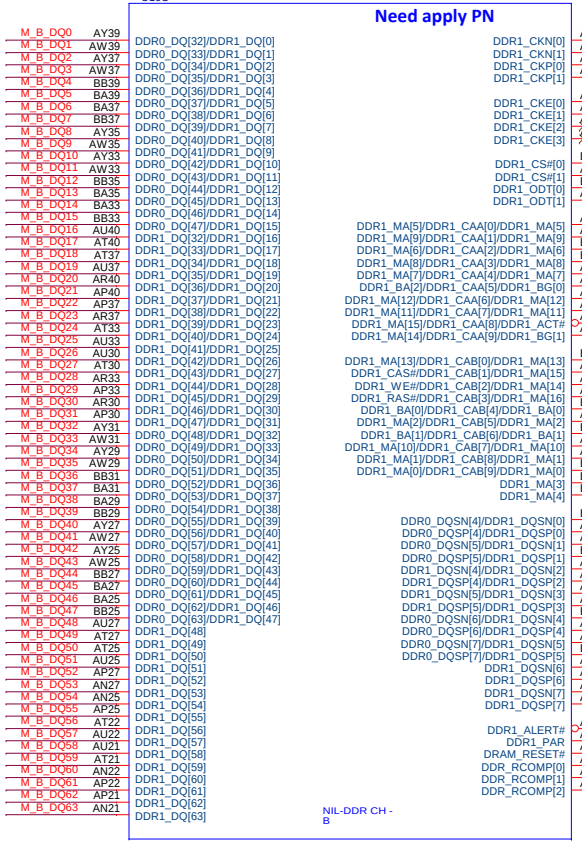
Need apply PN

U16B SKL_ULT

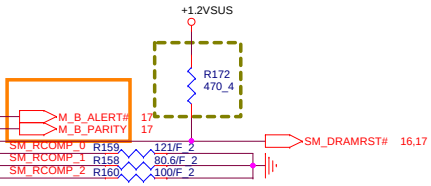



U16C SKL_ULT

Need apply PN




0419 change 470ohm 0402 stuff




DDR Rcomp need follow Intel Spec
12-15 min trance length

Table 4-34. KBL U DDR4/-RS SODIMM T3/8L Inline NIL Signal Routing Guidelines (Sh 2 of 3)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | | R (Ω±1%) C(uF) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Breakout | Total | |
| RCOMP[0] | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25 | | 500 | | 500 | 121 |
| RCOMP[1] | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25 | | 500 | | 500 | 80.6 |
| RCOMP[2] | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25 | | 500 | | 500 | 100 |

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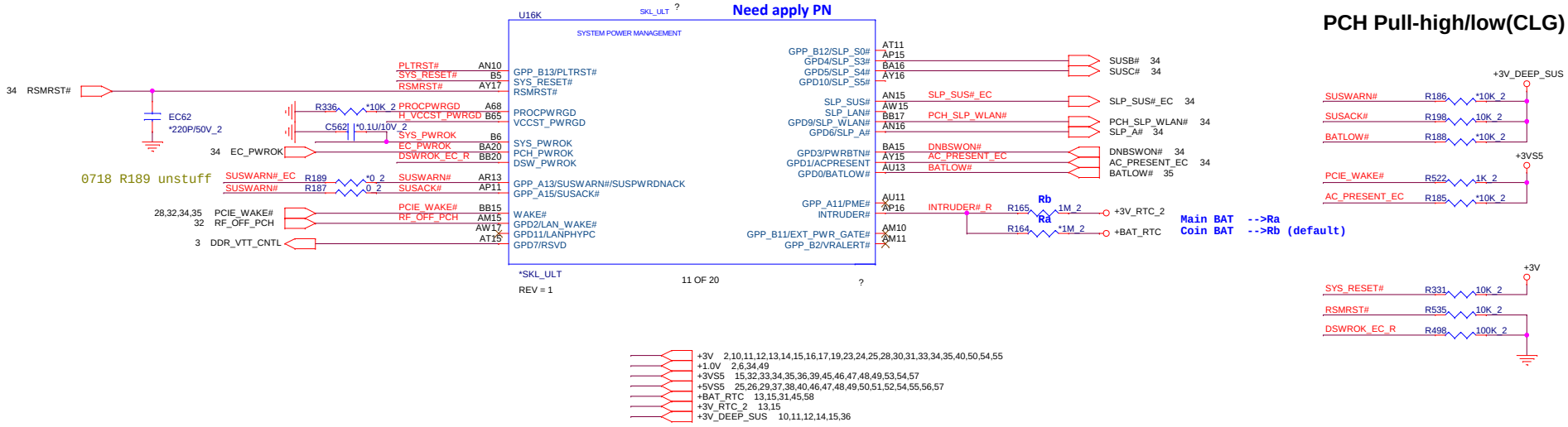
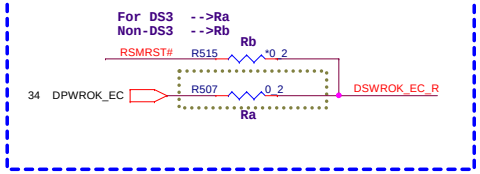
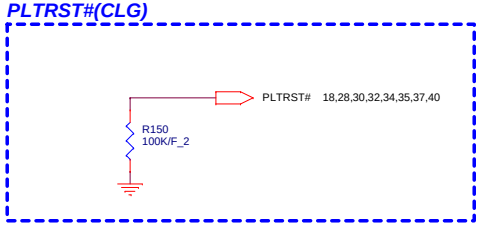
## PCH Pull-high/low(CLG)




## For DS3 Sequence

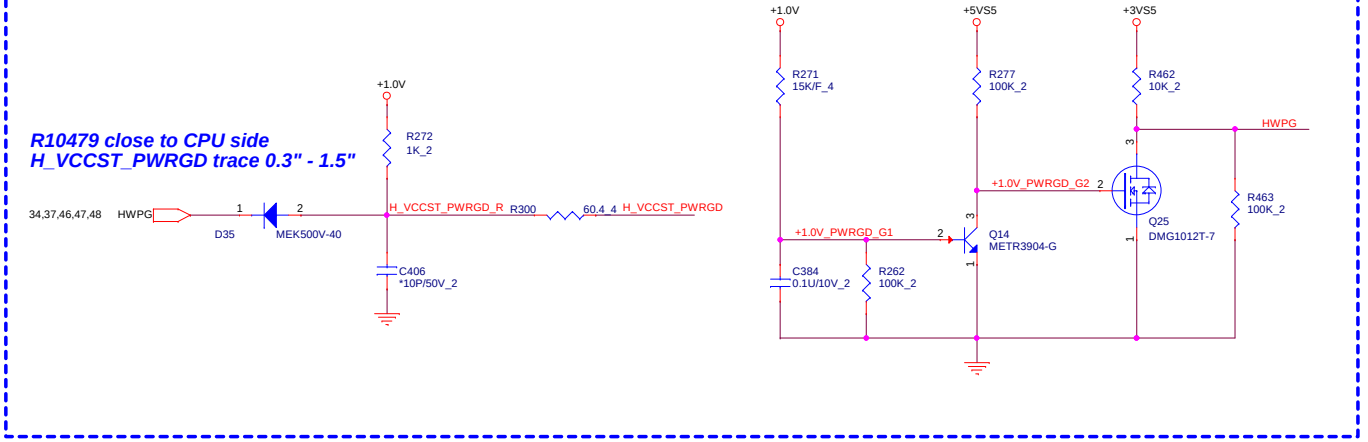



## PLTRST#(CLG)




## System PWR_OK(CLG)


## HW Power Good Circuit

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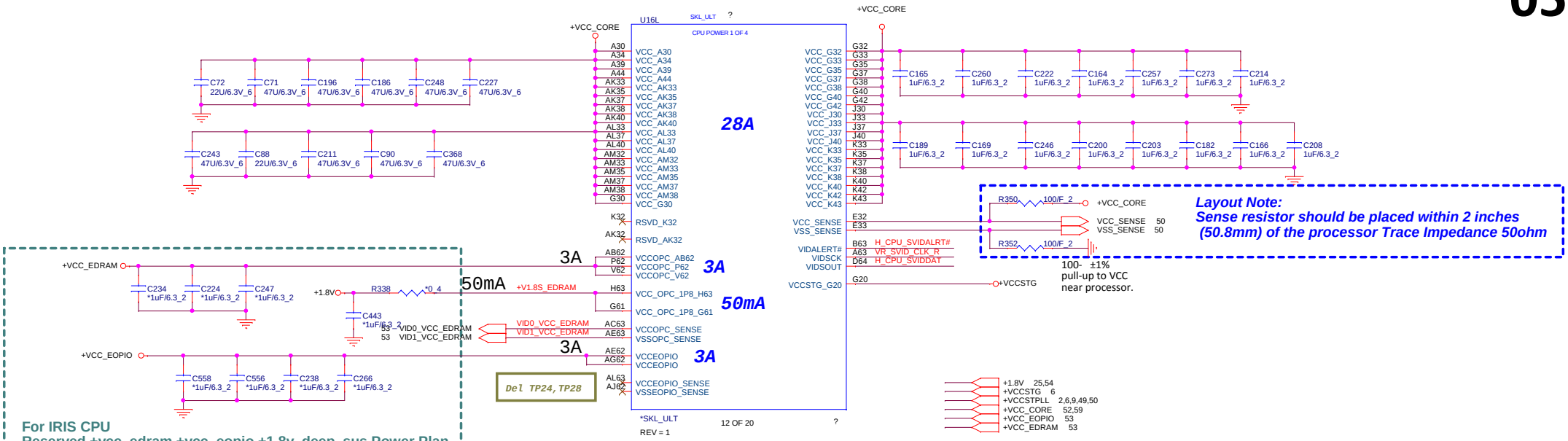
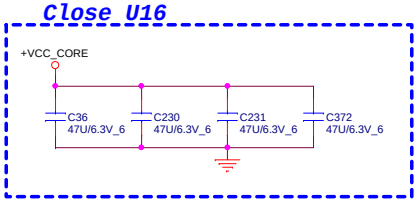


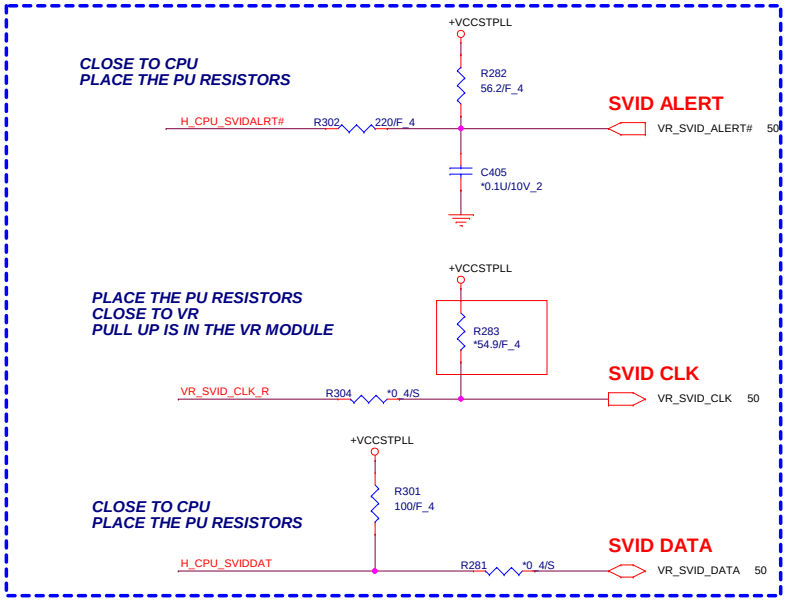

**Layout Note:**
**Sense resistor should be placed within 2 inches (50.8mm) of the processor Trace Impedance 50ohm**

For IRIS CPU
Reserved +vcc_edram,+vcc_eopio,+1.8v_deep_sus Power Plan

**Close U16**




**Layout note: need routing together and ALERT need between CLK and DATA.**




| Power Rail | Description | Control |
|---|---|---|
| $V_{CC}$ | Processor IA Cores Power Rail | SVID |
| $V_{CC_{GT}}$ | Processor Graphics Power Rails | SVID |
| $V_{CC_{GTX}}$ | Processor Graphics Extended Power Rail<br>Available only for GT3/GT4 processor SKUs | SVID |
| $V_{CC_{SA}}$ | System Agent Power Rail | SVID/Fixed (SKU dependent) |
| $V_{CC_{IO}}$ | IO Power Rail | Fixed |
| $V_{CC_{ST}}$ | Sustain Power Rail | Fixed |
| $V_{CC_{PLL}}$ | Processor PLLs power rail | Fixed |
| $V_{DDQ}$ | Integrated Memory Controller Power Rail | Fixed (Memory technology dependent) |
| $V_{CC_{OPC}}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $V_{CC_{OPC\_1P8}}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $V_{CC_{EOPIO}}$ | Processor EOPIO power rail (available only in SKU's with OPC) | Fixed |

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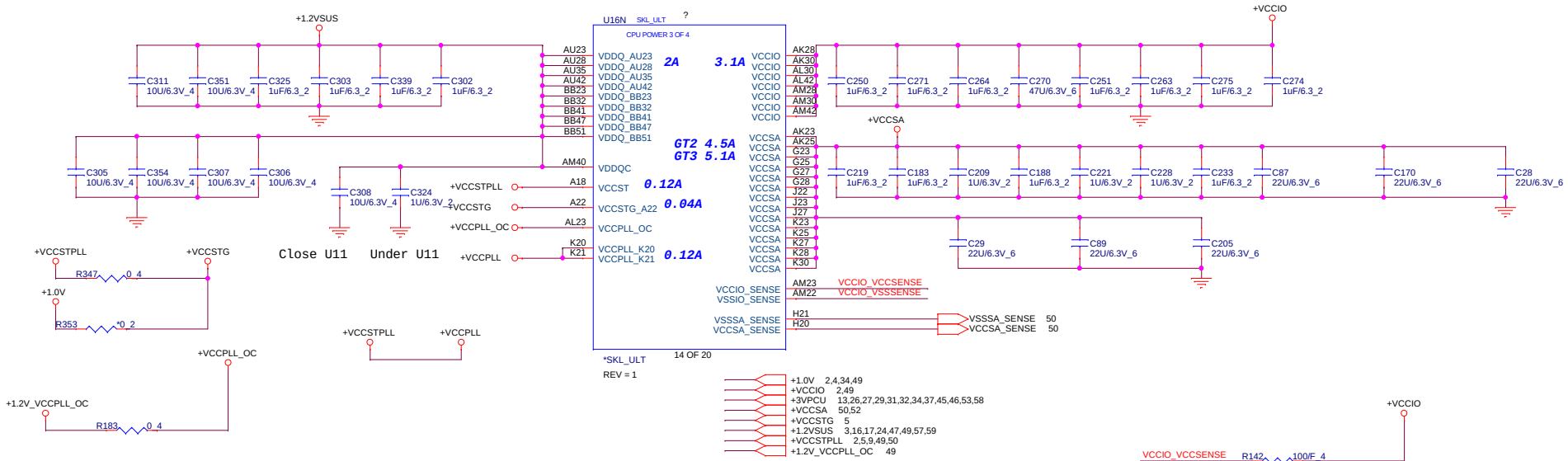
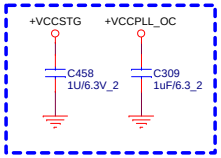
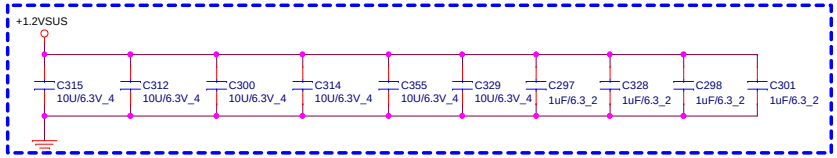


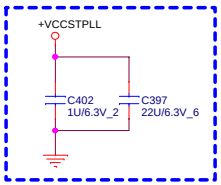

***Under U11***



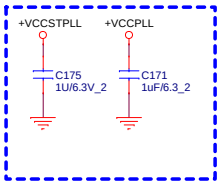

***Close to CPU***




***Close A18 Ball***

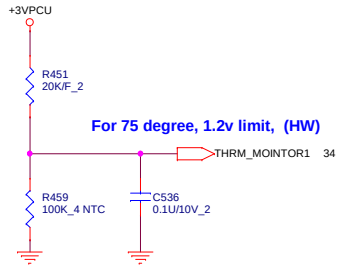



***Close U11***

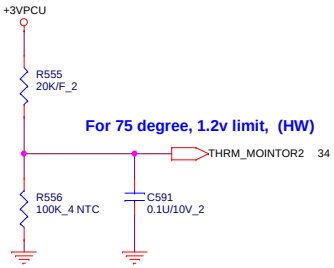



## CHOCK Ther Protect

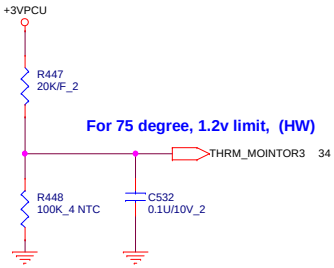
***For 65 degree, 1.8v limit, (SW)***




## DDR Ther Protect




## SSD Ther Protect




| Power Rail | Description | Control |
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| $Vcc_{OPC}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $Vcc_{OPC\_1P8}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $Vcc_{EOPIO}$ | Processor EOPIO power rail (available only in SKU's with OPC) | Fixed |

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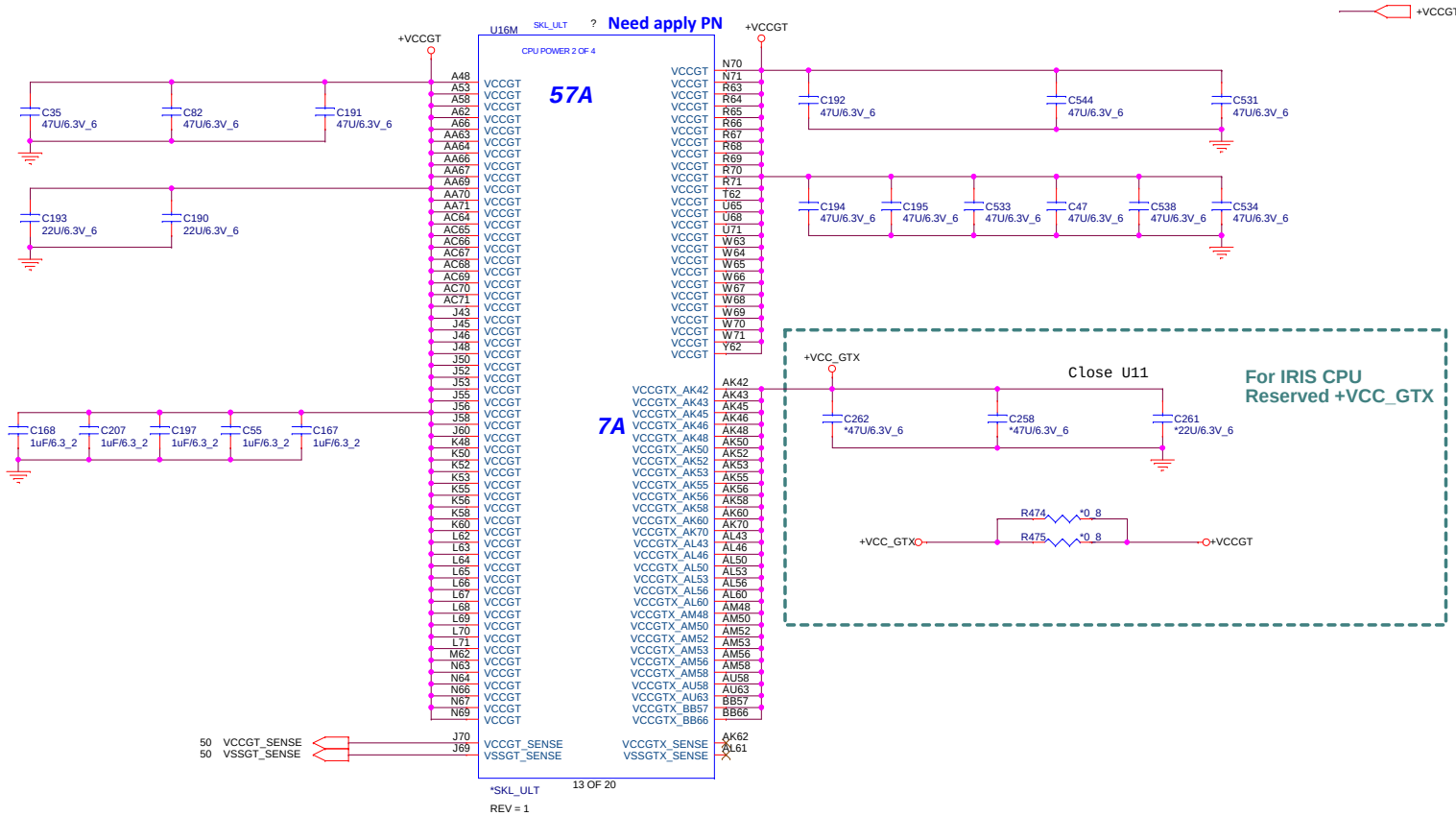


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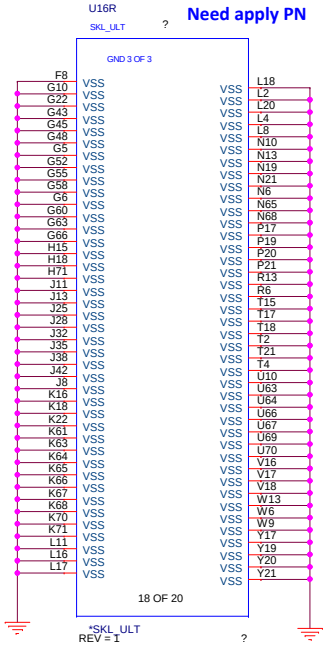


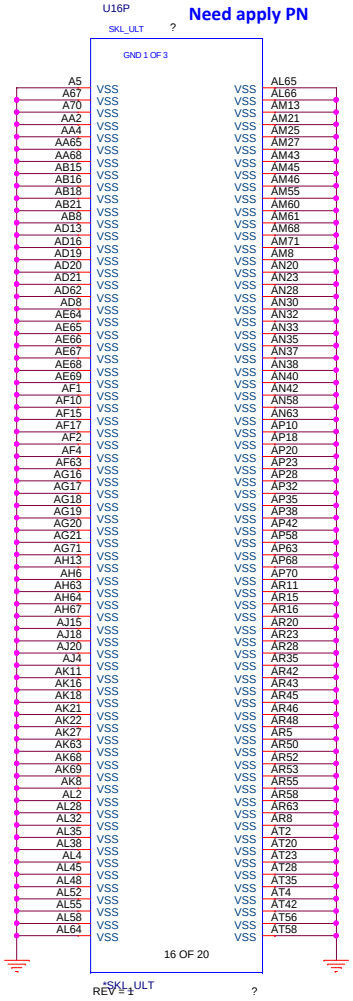


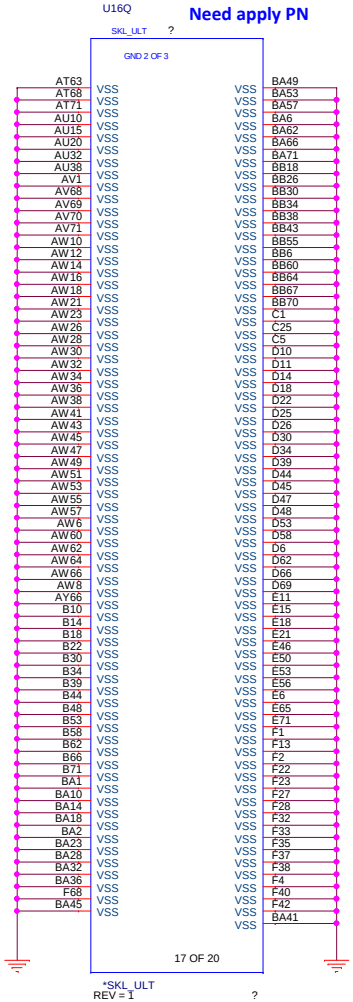


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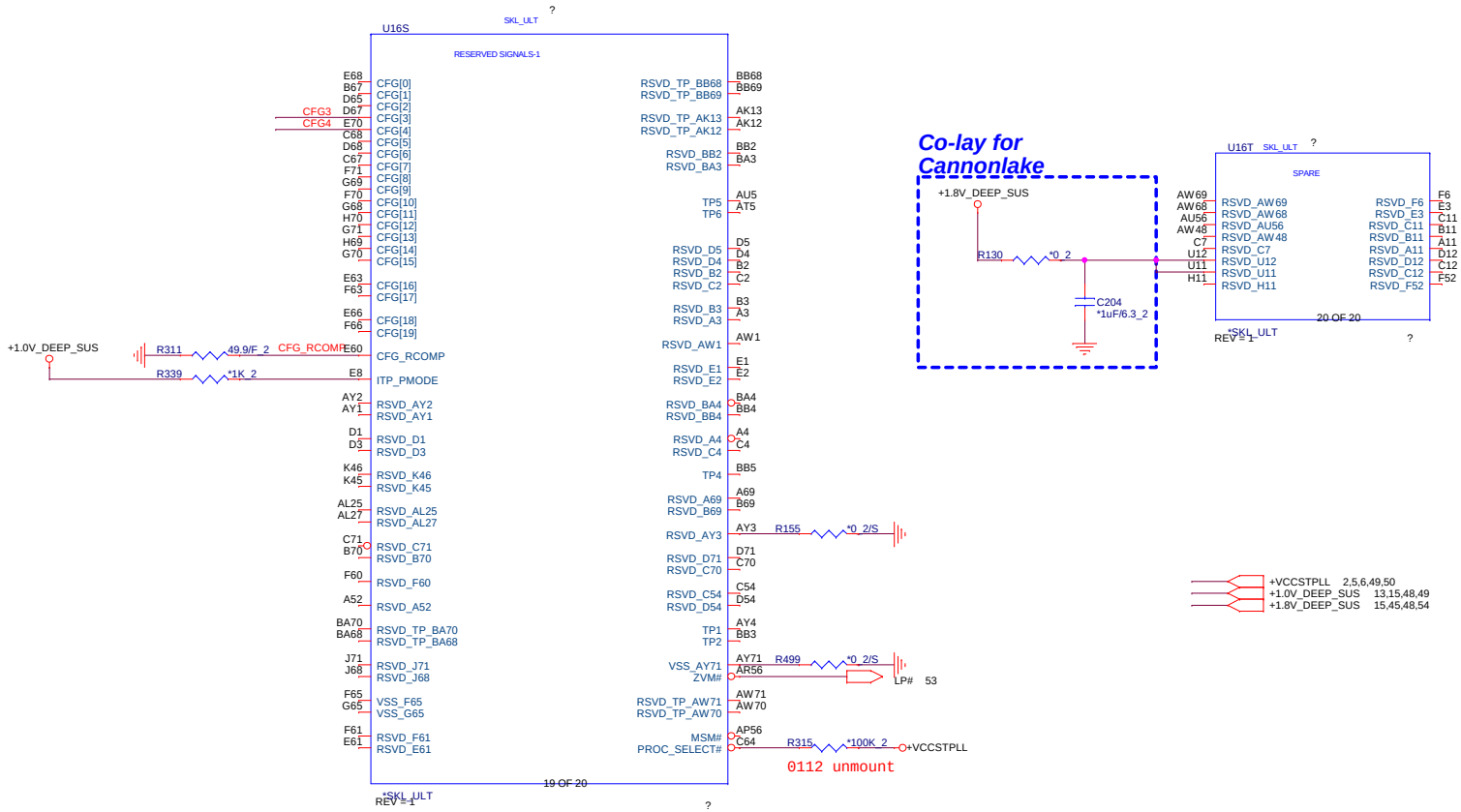


## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 | Circuit |
|---|---|---|---|
| CFG3<br>(Physcial Debug Enable)<br>DFX Privacy | Disable: | Enable: Set DFX Enable in DFX interface MSR | CFG3 R346 *1K_2 |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP | CFG4 R324 1K_2 |
| | | | |

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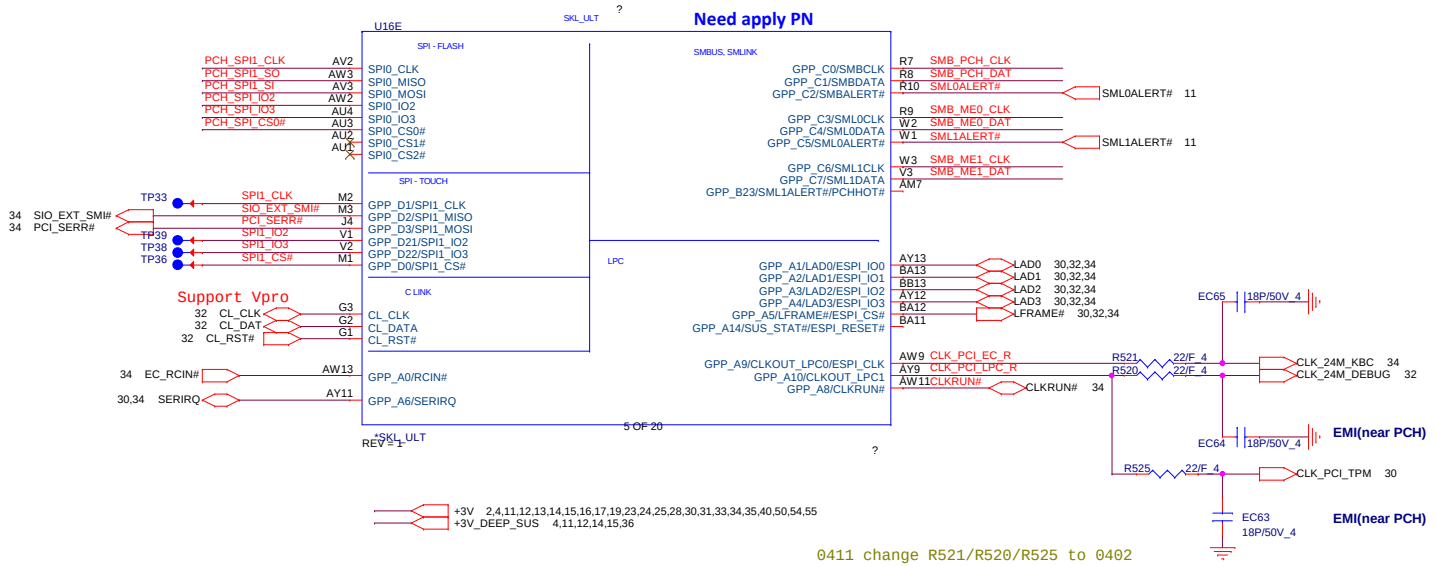
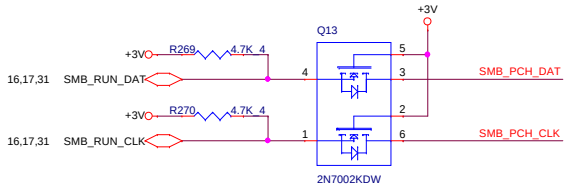



## GPIO Pull UP

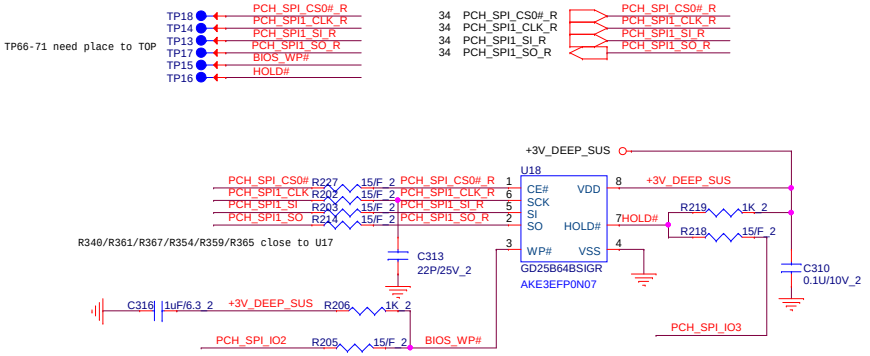

## SMBus/Pull-up(CLG)

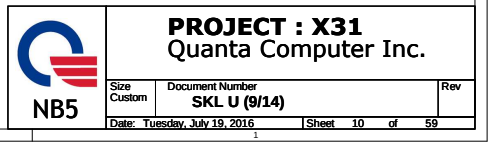



*Touch Pad*
*XDP*
*LPDDR3 thermal sensor*

## PCH SPI ROM(CLG)

| Vender | Size | P/N |
|---|---|---|
| EON | 8MB | AKE3EZN0Q01 (EN25QH64-104HIP) |
| Winbond | 8MB | AKE3EFP0N07 (W25Q64FVSSIQ) |
| GigaDevice | 8MB | AKE3EGN0Q01 (GD25B64BSIGR) |
| Socket | | DFHS08FS023 |



# Functional Strap Definitions

*DESIGN NOTE:*
*WEAK PULL UP RESISTOR PRESENT ON THIS NET*

14,25 ACZ_SPKR — ACZ_SPKR — R524 *20K/F_2

*TOP SWAP OVERRIDE*
*HIGH - TOP SWAP ENABLE*
*LOW-DISABLED*
*HIGH: LPC SELECTED FOR SYSTEM FLASH*
*WEAK INTERNAL PD*

+3V_DEEP_SUS — R506 *4.7K_2 — ACZ_SDOUT — 14 ACZ_SDOUT

*No Boot:*
*The signal has a weak internal pull-down.*
*0 = Enable security measures defined in the Flash Descriptor.*
*1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.*
*This function is useful when running ITP/XDP.*

34 GPIO33_EC — R514 1K_2 — ACZ_SDOUT

+3V_DEEP_SUS — R486 1K_2 — SML0ALERT# — R488 *20K/F_2 — 10 SML0ALERT#

*No Boot:*
*The signal has a weak internal pull-down.*
*0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).*
*1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.*

+3V — R156 *4.7K_2 — GPP_B18 — R157 10K_2 — 14 GPP_B18

*No Boot:*
*The signal has a weak internal pull-down.*
*0 = Disable No Reboot mode.*
*1 = Enable No Reboot mode*
*(PCH will disable the TCO Timer system reboot feature).*
*This function is useful when running ITP/XDP.*

+3V 2,4,10,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55
+3V_DEEP_SUS 4,10,12,14,15,36

14 GSPI1_MOSI — GSPI1_MOSI — R484 *20K/F_2

*No Boot:*
*The signal has a weak internal pull-down.*
*This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.*

| Bit 10 | Boot BIOS Destination |
|---|---|
| 0 | SPI |
| 1 | LPC |

+3V_DEEP_SUS — R431 *10K_2 — SML1ALERT# — R430 20K/F_2 — 10 SML1ALERT#

*No Boot:*
*The signal has a weak internal pull-down.*
*0 = LPC Is selected for EC.*
*1 = eSPI Is selected for EC.*

NB5

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL U (10/14) | |

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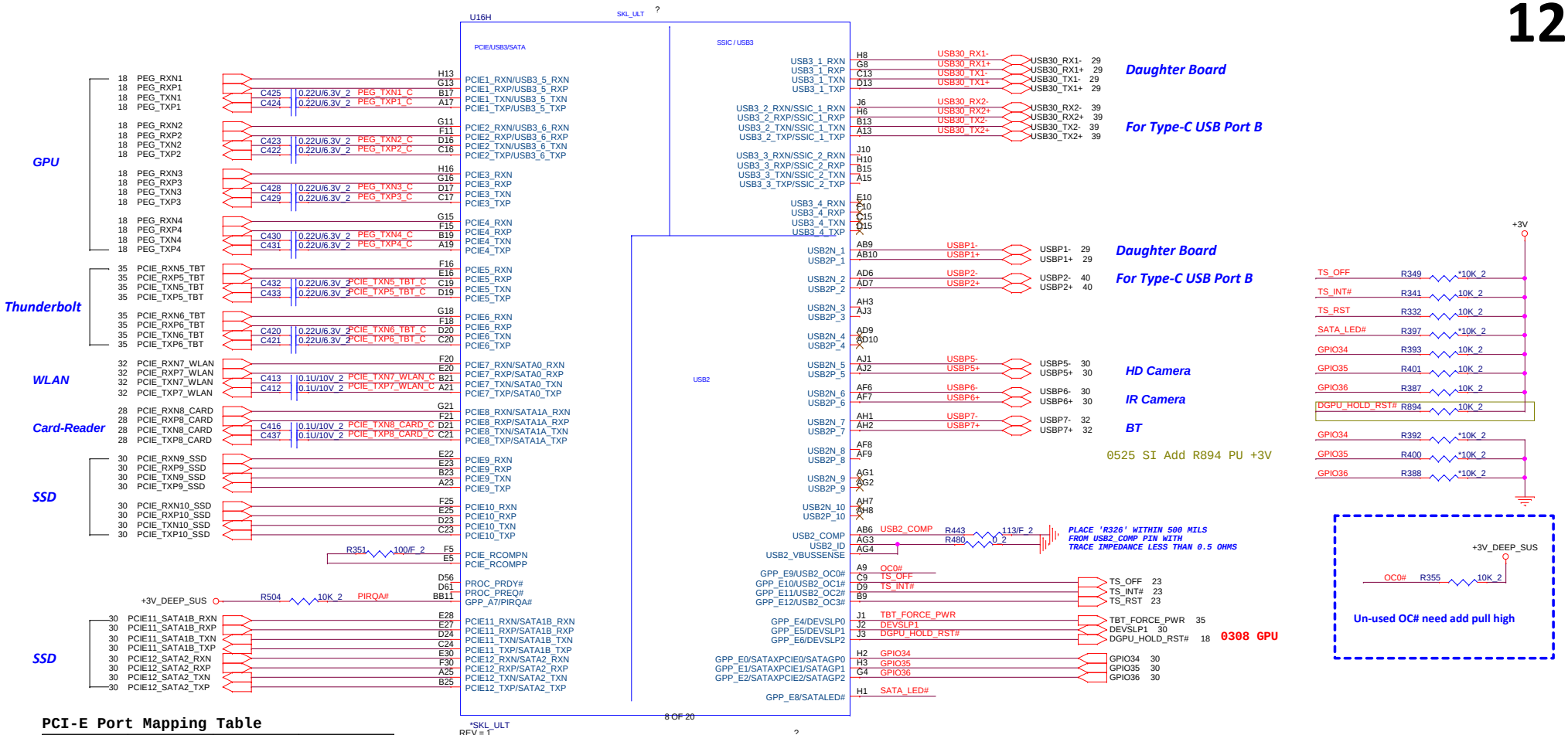



## PCI-E Port Mapping Table

| PCI-E Port | Function | CLK RQ Port | Function |
|---|---|---|---|
| Port1 | GPU | Port0 | Un-used |
| Port2 | GPU | Port1 | Un-used |
| Port3 | GPU | Port2 | WLAN |
| Port4 | GPU | Port3 | Un-used |
| Port5 | Thunderbolt | Port4 | Thunderbolt |
| Port6 | Thunderbolt | Port5 | SSD HDD |
| Port7 | WLAN | | |
| Port8 | CR | | |
| Port9 | SSD HDD | | |
| Port10 | SSD HDD | | |
| Port11 | SSD HDD | | |
| Port12 | SSD HDD | | |

## USB3.0 Port Mapping Table

| USB3.0 | Function |
|---|---|
| PORT-1 | USB3.0 MB-1 |
| PORT-2 | Type-C USB Port B |
| PORT-3 | Type-C USB Port B |
| PORT-4 | NC |

## USB2.0 Port Mapping Table

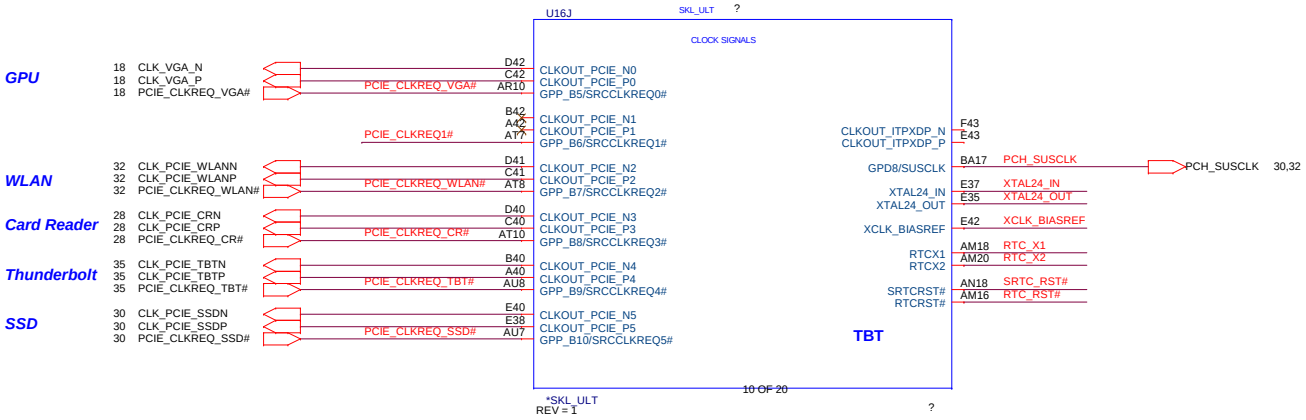
| USB2.0 | Function |
|---|---|
| PORT-1 | USB3.0 MB-1 |
| PORT-2 | Type-C USB Port B |
| PORT-3 | NC |
| PORT-4 | NC |
| PORT-5 | HD Camera |
| PORT-6 | IR Camera |
| PORT-7 | WLAN |
| PORT-8 | NC |
| PORT-9 | NC |
| PORT-10 | NC |

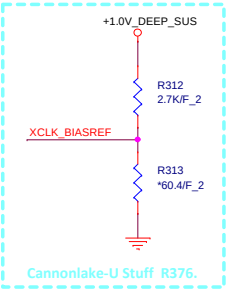
**PROJECT : X31**
Quanta Computer Inc.

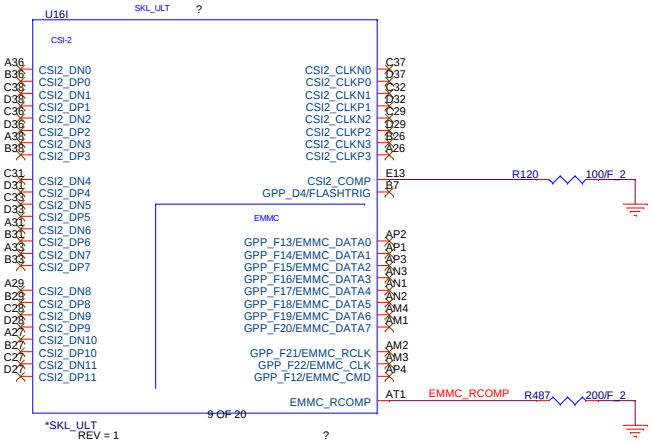
NB5

Size: Custom | Document Number: SKL U (11/14) | Rev

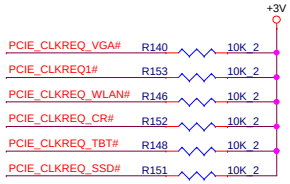
Date: Tuesday, July 19, 2016 | Sheet 12 of 59



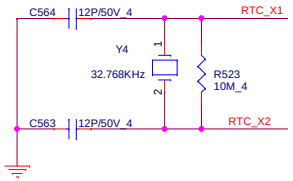




## CLK_REQ/Strap Pin(CLG)



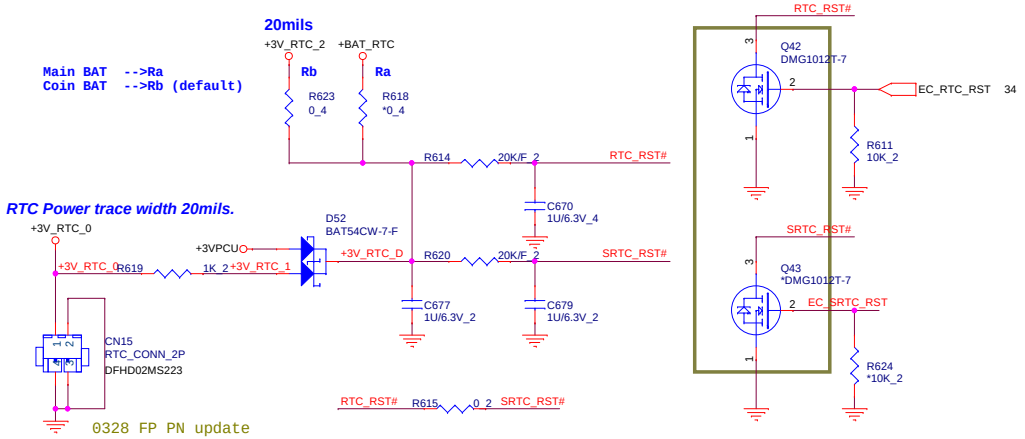

+3V 2,4,10,11,12,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55
+3VPCU 6,26,27,29,31,32,34,37,45,46,53,58
+BAT_RTC 4,15,31,45,58
+3V_RTC_2 4,15
+1.0V_DEEP_SUS 9,15,48,49

## RTC Clock 32.768KHz



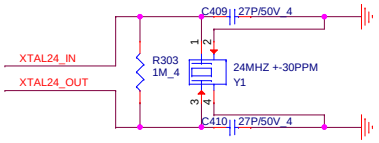

0523 SI Change to 12PF

## RTC Circuitry(RTC)




0328 FP PN update

## External Crystal

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Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL U (12/14) | |
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NB5

# Skylake (GPIO)



+3V 2,4,10,11,12,13,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55
+3V_DEEP_SUS 4,10,11,12,15,36

+3V_DEEP_SUS

BT_OFF R413 10K_2
PCH_TEMPALERT# R416 10K_2
SIO_EXT_SCI# R479 10K_2
UART2_RXD R472 49.9K/F_4
UART2_TXD R473 49.9K/F_4
SPK_ID_CODEC R483 10K_2

DB2 Change Footprint

11 GPP_B18 — GPP_B18
11 GSPI1_MOSI — GSPI1_MOSI
35 TBT_HTPLG
34 SIO_EXT_SCI#
UART2_RXD
UART2_TXD
TBT_HTPLG
SIO_EXT_SCI#

Touch Screen
23 I2C0_SDA
23 I2C0_SCL

27 SPK_ID_CODEC

U16F SKL_ULT ? Need apply PN

LPSS

AN8 GPP_B15/GSPI0_CS#
AP7 GPP_B16/GSPI0_CLK
AP8 GPP_B17/GSPI0_MISO
AR7 GPP_B18/GSPI0_MOSI
AM5 GPP_B19/GSPI1_CS#
AN7 GPP_B20/GSPI1_CLK
AP5 GPP_B21/GSPI1_MISO
AN5 GPP_B22/GSPI1_MOSI
AB1 GPP_C8/UART0_RXD
AB2 GPP_C9/UART0_TXD
W4 GPP_C10/UART0_RTS#
AB3 GPP_C11/UART0_CTS#
AD1 GPP_C20/UART2_RXD
AD2 GPP_C21/UART2_TXD
AD3 GPP_C22/UART2_RTS#
AD4 GPP_C23/UART2_CTS#
U7 GPP_C16/I2C0_SDA
U6 GPP_C17/I2C0_SCL
U8 GPP_C18/I2C1_SDA
U9 GPP_C19/I2C1_SCL
AH9 GPP_F4/I2C2_SDA
AH10 GPP_F5/I2C2_SCL
AH11 GPP_F6/I2C3_SDA
AH12 GPP_F7/I2C3_SCL
AF11 GPP_F8/I2C4_SDA
AF12 GPP_F9/I2C4_SCL

*SKL_ULT
REV = 1

6 OF 20

ISH

P2 GPP_D9
P3 GPP_D10
P4 GPP_D11
P1 GPP_D12 — BT_OFF — BT_OFF 32
M4 GPP_D5/ISH_I2C0_SDA — ISH_I2C0_SDA — ISH_I2C0_SDA 33
N3 GPP_D6/ISH_I2C0_SCL — ISH_I2C0_SCL — ISH_I2C0_SCL 33
N1 GPP_D7/ISH_I2C1_SDA — ISH_I2C1_SDA
N2 GPP_D8/ISH_I2C1_SCL — ISH_I2C1_SCL
AD11 GPP_F10/I2C5_SDA/ISH_I2C2_SDA — ISH_I2C2_SDA — TP4
AD12 GPP_F11/I2C5_SCL/ISH_I2C2_SCL — ISH_I2C2_SCL — TP5
U1 GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA — PCH_TEMPALERT#
U2 GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
Y3 GPP_D15/ISH_UART0_RTS#
U4 GPP_D16/ISH_UART0_CTS#/SML0BALERT#
AC1 GPP_C12/UART1_RXD/ISH_UART1_RXD
AC2 GPP_C13/UART1_TXD/ISH_UART1_TXD
AC3 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AB4 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AY8 GPP_A18/ISH_GP0 — ISH_AE_INT_K
BA8 GPP_A19/ISH_GP1 — ISH_GYRO_DRDY_K — R213 *0_2 — ISH_GYRO_DRDY 33
BB7 GPP_A20/ISH_GP2 — ISH_GYRO_INT_K — R210 *0_2 — ISH_GYRO_INT 33
BA7 GPP_A21/ISH_GP3 — ISH_GP3
AY7 GPP_A22/ISH_GP4 — ISH_ACC_INT_K
AW7 GPP_A23/ISH_GP5 — DISABLE KB — DISABLE KB 34
AP13 GPP_A12/BM_BUSY#/ISH_GP6 — EMU_LID_D

?

+3V
EMU_LID_D R225 *10K_2
ISH_GYRO_DRDY R223 *10K_2
ISH_GYRO_INT R220 *10K_2
ISH_AE_INT R212 *10K_2
ISH_ACC_INT R221 *10K_2
DISABLE KB R229 *10K_2
R224 *10K_2
R222 *10K_2
R228 *10K_2

ISH_I2C0_SDA R217 10K_2
ISH_I2C0_SCL R208 10K_2
ISH_I2C2_SDA R137 10K_2
ISH_I2C2_SCL R139 10K_2
ISH_I2C1_SDA R215 10K_2
ISH_I2C1_SCL R216 10K_2
I2C0_SDA R132 10K_2
I2C0_SCL R135 10K_2

ISH_AE_INT_K R207 0_2 — ISH_AE_INT 33
ISH_GP3 R204 *0_2

ISH_GYRO_INT_K R209 0_2
ISH_ACC_INT_K R211 *0_2 — ISH_ACC_INT 33

EMU_LID_D R226 *10K_2 — +3V_DEEP_SUS
D49 RB500V-40 — EMU_LID 23,34

R465 10K_2 BOARD_ID0 — R464 *10K_2
R482 *10K_2 BOARD_ID1 — R481 10K_2
R471 10K_2 BOARD_ID2 — R470 *10K_2
R460 10K_2 BOARD_ID3 — R461 *10K_2
R441 *10K_2 BOARD_ID4 — R444 10K_2
R456 10K_2 BOARD_ID5 — R457 *10K_2
R449 10K_2 BOARD_ID6 — R450 *10K_2
R454 10K_2 BOARD_ID7 — R453 *10K_2
R490 *10K_2 BOARD_ID8 — R513 10K_2
+3V_DEEP_SUS

## HDA Bus(CLG)

+3V_DEEP_SUS R510 *1K_2 ACZ_SYNC
25 ACZ_SYNC_AUDIO R518 33_2 ACZ_SYNC
25 ACZ_RST#_AUDIO R508 33_2 ACZ_RST#
25 ACZ_SDOUT_AUDIO R519 33_2 ACZ_SDOUT
25 BIT_CLK_AUDIO R509 33_2 ACZ_BCLK
C561 *10P/50V_2

## Sensors Debug CONN

CN1
1 ISH_I2C0_SCL
2 ISH_I2C0_SDA
3 ISH_I2C1_SCL
4 ISH_I2C1_SDA
5
6 ISH_GYRO_DRDY
7 ISH_GYRO_INT
8 ISH_AE_INT
9 ISH_ACC_INT
10
11 EMU_LID_D
12 DISABLE KB
13 TP22
14 TP19
15 TP21
16 TP20
17 +3V
18
*ACES_88511-180N

| KBL-U | BOARD_ID8 | BOARD_ID7 | BOARD_ID6 | Board ID [5:4] | BOARD_ID[3:0] | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Model | ID8 | ID7 | ID6 | ID5 ID4 | ID3 | ID2 | ID1 | ID0 | |
| X32 | 0 VPRO<br>1 Non VPRO | 0 2+2 CPU<br>1 2+3E CPU | 0 ESH<br>1 ISH | 0 DIS<br>(Default = 01) | 0 | 0 | 0 | 0 | Hynix 8Gb |
| | | | | | 0 | 0 | 0 | 1 | Samsung 8Gb |
| | | | | | 0 | 0 | 1 | 0 | Micron 8Gb |
| | | | | | 0 | 0 | 1 | 1 | Hynix 16G |
| | | | | | 0 | 1 | 0 | 0 | Samsung 16G |
| | | | | | 0 | 1 | 0 | 1 | Micron 16G |
| | | | | | 0 | 1 | 1 | 0 | |
| | | | | | 0 | 1 | 1 | 1 | |
| | | | | | 1 | 0 | 0 | 0 | |
| | | | | | 1 | 0 | 0 | 1 | |
| | | | | | 1 | 0 | 1 | 0 | |
| | | | | | 1 | 0 | 1 | 1 | |
| | | | | | | | | | |

U16G SKL_ULT ? Need apply PN

AUDIO

11 ACZ_SDOUT
25 ACZ_SDIN0
ACZ_SYNC BA22
ACZ_BCLK AY22
ACZ_SDOUT BB22
ACZ_SDIN0 BA21
AY21
ACZ_RST# AW22
J5
AY20
AW20
AK7
AK6
AK9
AK10
H5
D7
D8
C8
11,25 ACZ_SPKR AW5

HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
GPP_B14/SPKR

SDIO/SDXC

AB11 GPP_G0/SD_CMD — BOARD_ID0
AB13 GPP_G1/SD_DATA0 — BOARD_ID1
AB12 GPP_G2/SD_DATA1 — BOARD_ID2
W12 GPP_G3/SD_DATA2 — BOARD_ID3
W11 GPP_G4/SD_DATA3 — BOARD_ID4
W10 GPP_G5/SD_CD# — BOARD_ID5
W8 GPP_G6/SD_CLK — BOARD_ID6
W7 GPP_G7/SD_WP — BOARD_ID7
BA9 GPP_A17/SD_PWR_EN#/ISH_GP7 — BOARD_ID8
BB9 GPP_A16/SD_1P8_SEL
AB7 SD_RCOMP — R136 200/F_2
AF13 GPP_F23

*SKL_ULT
REV = 1

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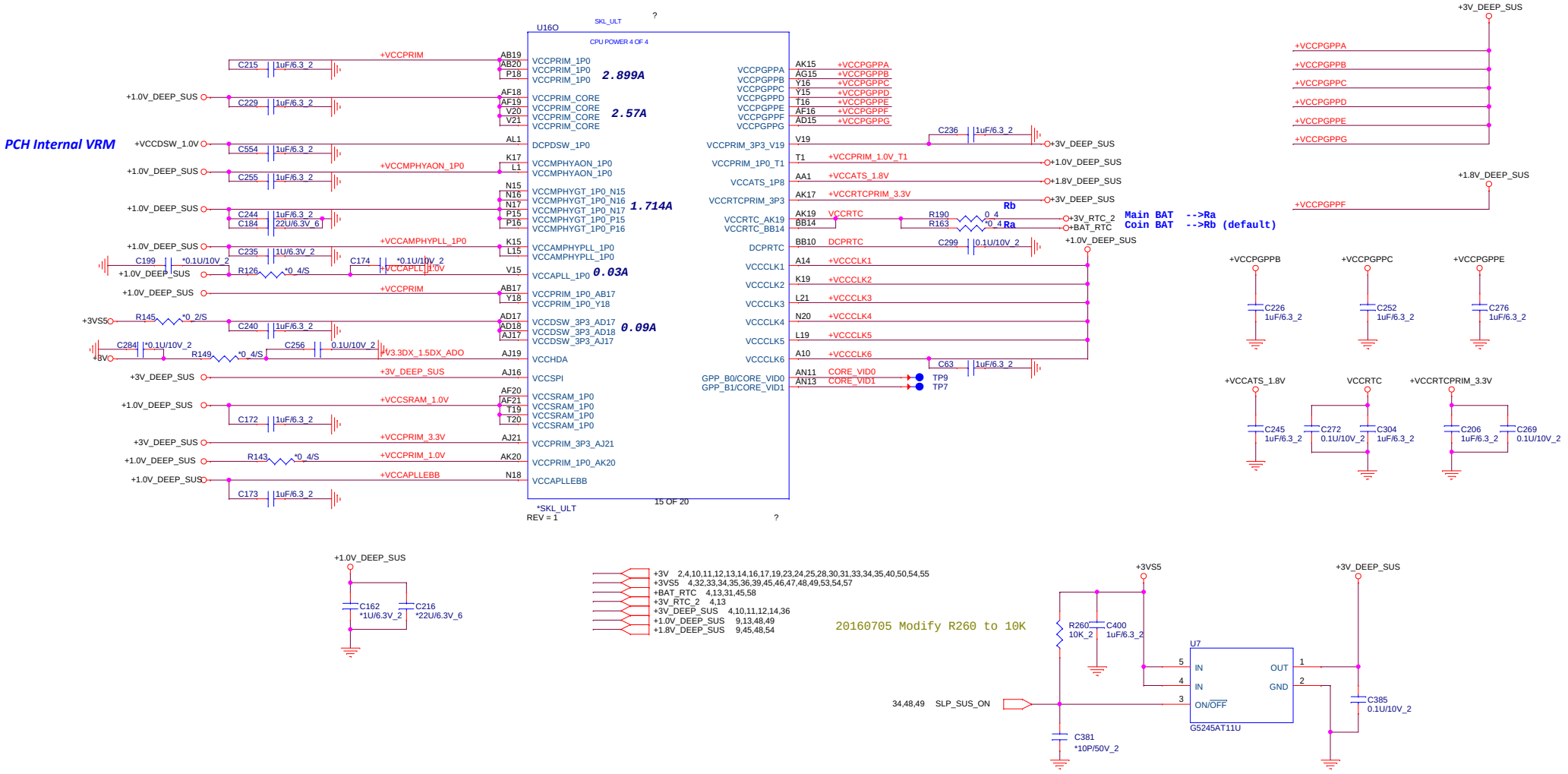
?

NB5

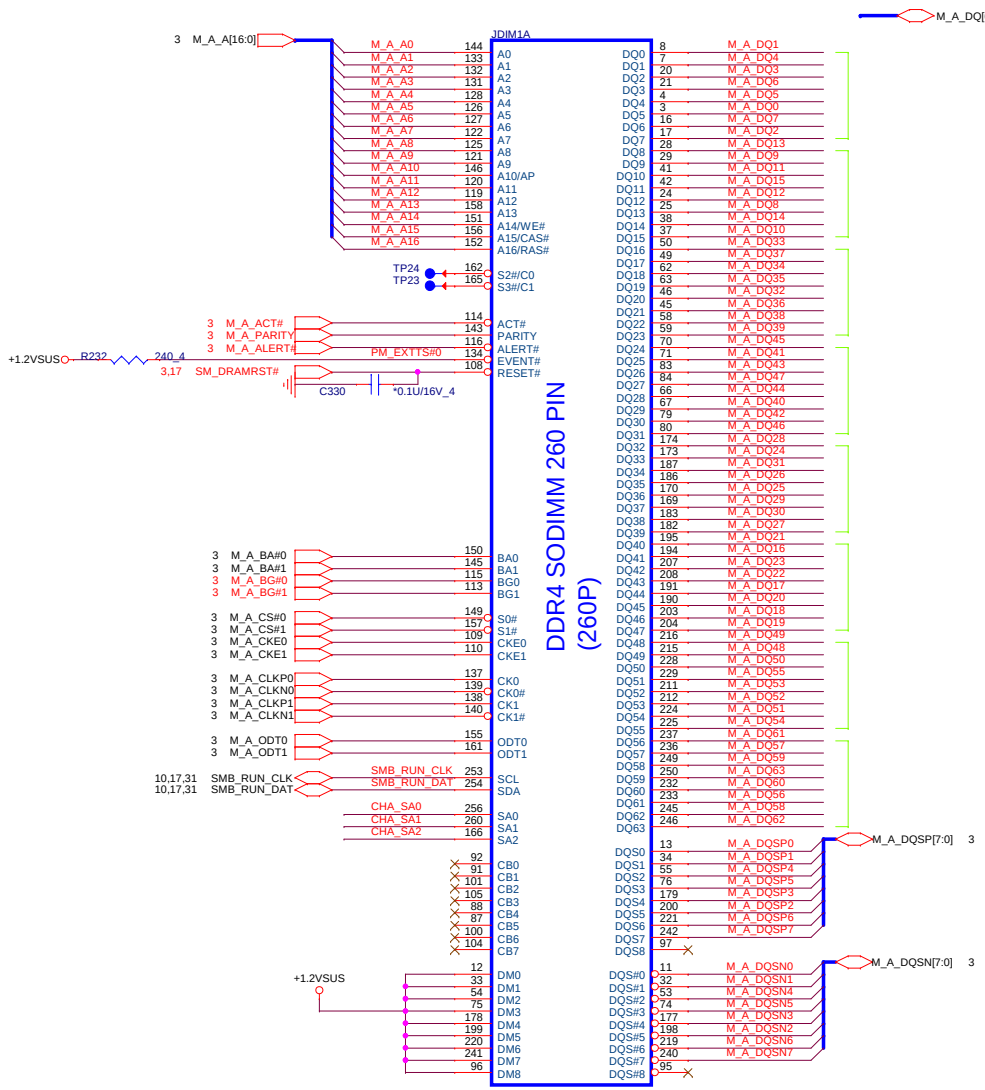
**PROJECT : X31**
Quanta Computer Inc.

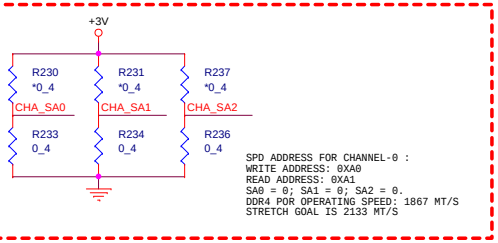
| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL U (13/14) | |
| Date: Tuesday, July 19, 2016 | Sheet 14 of 59 | |

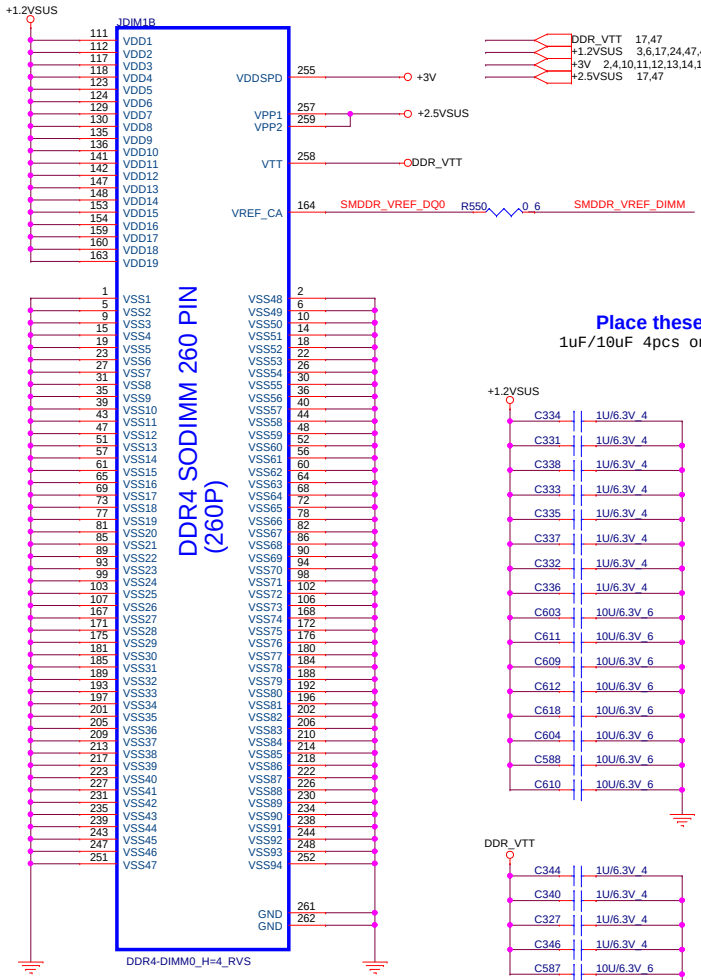



| | | | |
|---|---|---|---|
| PROJECT : X31 Quanta Computer Inc. | | | |
| NB5 | Size: Custom | Document Number: SKL U (14/14) | Rev: |
| | Date: Tuesday, July 19, 2016 | Sheet 15 of 59 | |

2.48A

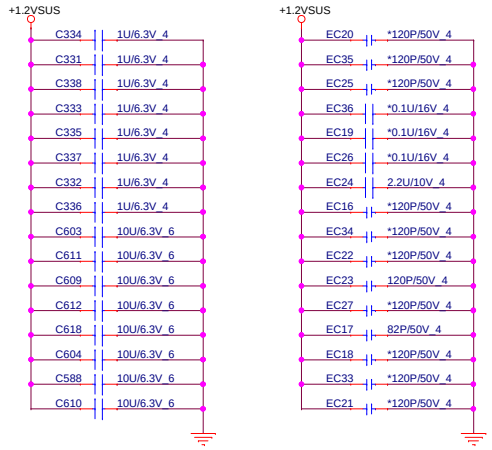


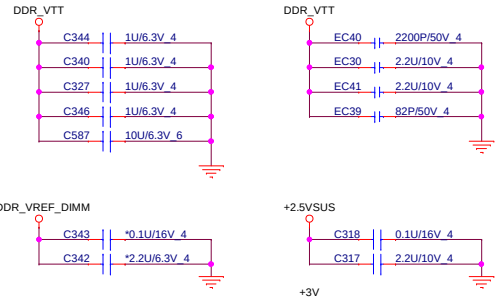



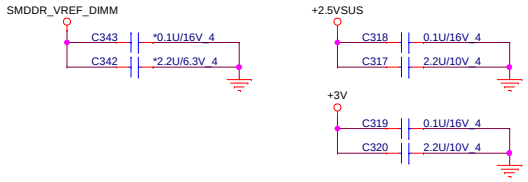




Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector

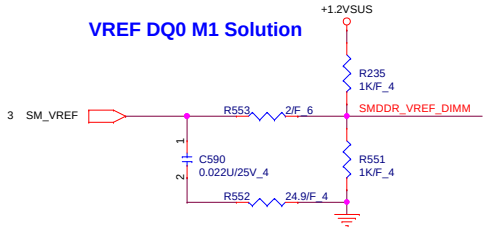
For EMI RESERVE




VREF DQ0 M1 Solution




PROJECT : Damon
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR4 DIMM0-RVS(4.0H) | 1A |
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BU5/HW

2.48A

JDIM2A

DDR4 SODIMM 260 PIN (260P)

JDIM2B

DDR4 SODIMM 260 PIN (260P)

DDR4-DIMM0_H=4_RVS

Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector

For RF RESERVE For RF RESERVE

VREF DQ1 M1 Solution

SPD ADDRESS FOR CHANNEL-1 :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

PROJECT : Damon
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR3 DIMM1-RVS(4.0H) | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 17 of 59 | |

BU5/HW

**PEX_IOVDD + PEX_IOVDDQ = 1.042A**

**PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA**

**PEX_PLLVDD = 130mA**

**NVDD = 32.22 ~ 26.66 A**

**VDD33 = 56mA**

0602 Change 4.7uf to 47uf

1230 Change C338 size to 0603

1230 Change C395, C370, C386, C349, C403 size to 0402

0611
Change R196, R155 to short pad

0611
Change R433 to short pad

CX300T30001 Change to 0ohm

**Power up sequence**

ALL 3.3V
+3VGFX & +3V3_AON

NVDD
+VGACORE

PEX_VDD
+1.05V_GFX

FBVDDQ
+1.35V_GFX

t>0

t>=0

t>=0

**Power down sequence**

First Rail to Power Down

Last Rail to Power Down

$t_{POWER\_OFF}$ < 10 ms

**PROJECT : X1BD**
Quanta Computer Inc.

NB5

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|---|---|---|
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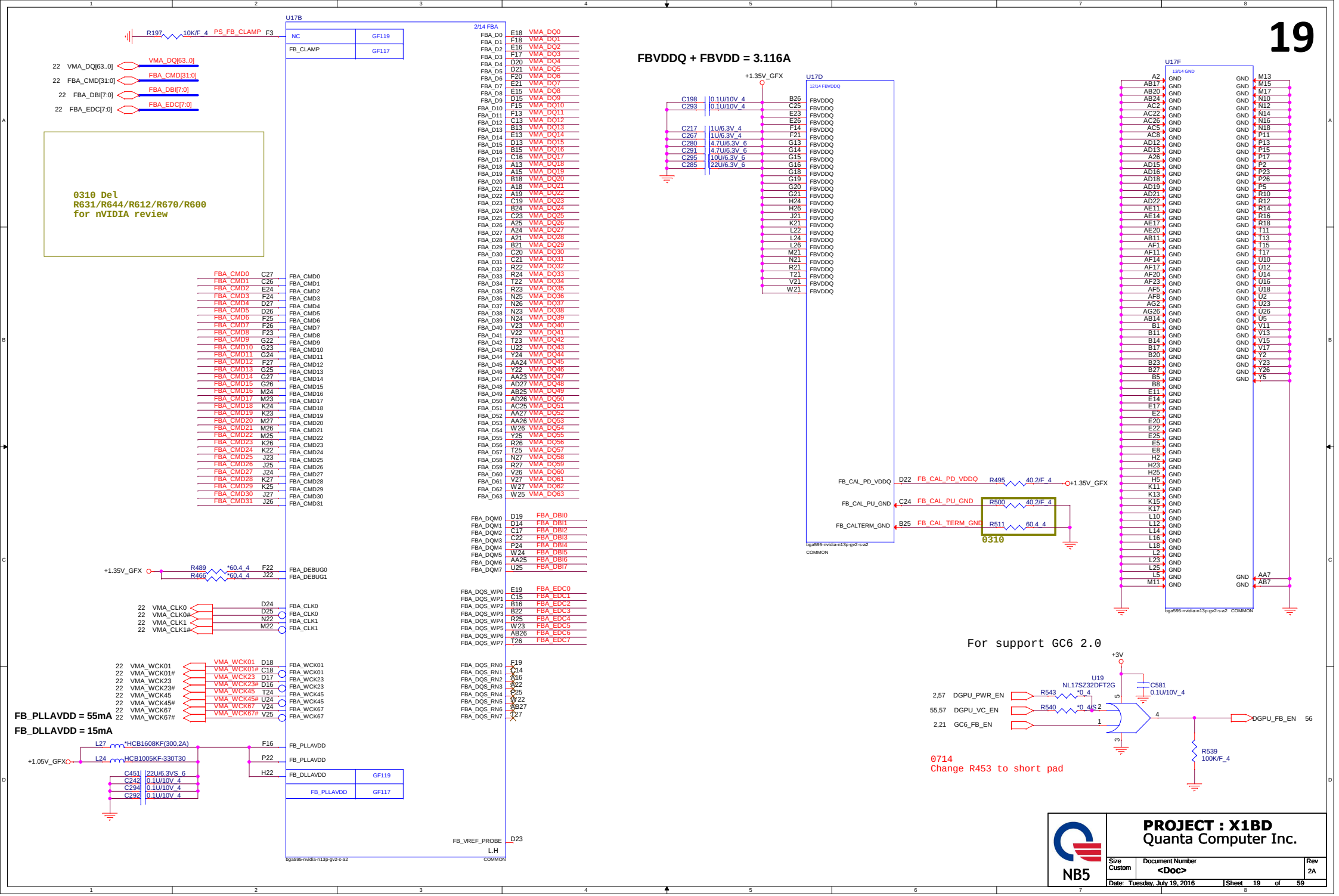
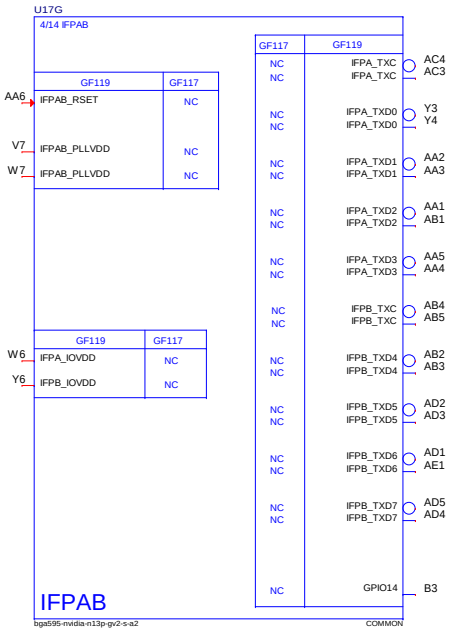
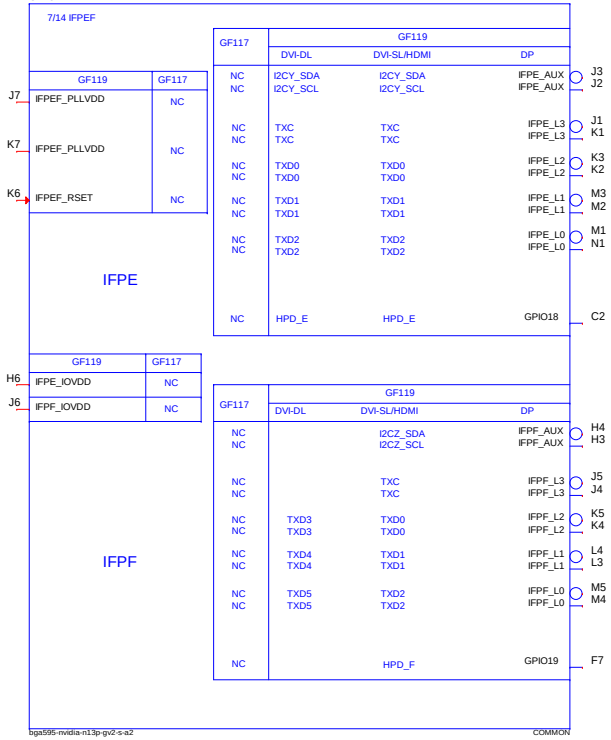
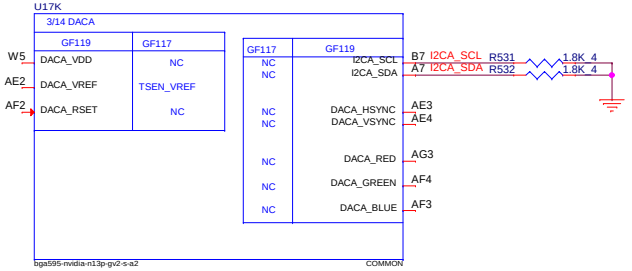
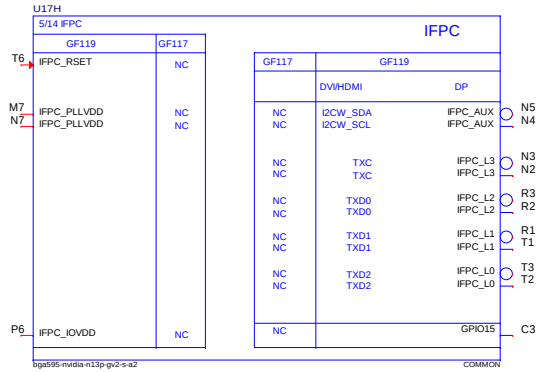
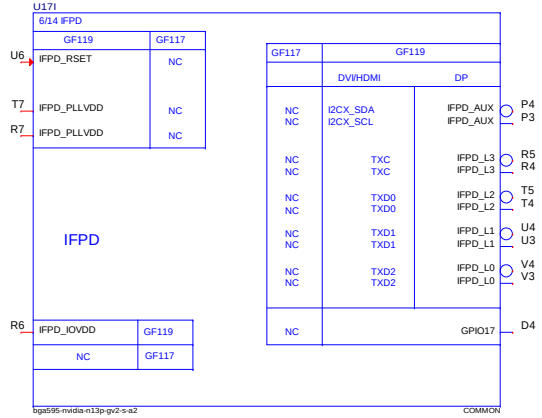




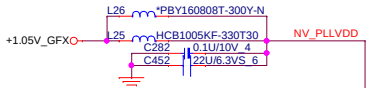



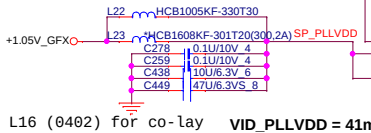

**PLLVDD = 38mA**




Add L27 (0402) for co-lay

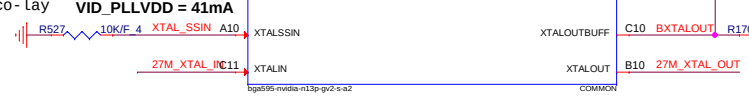
0507 L16 stuff, L15 unstuff

**SP_PLLVDD = 17mA**

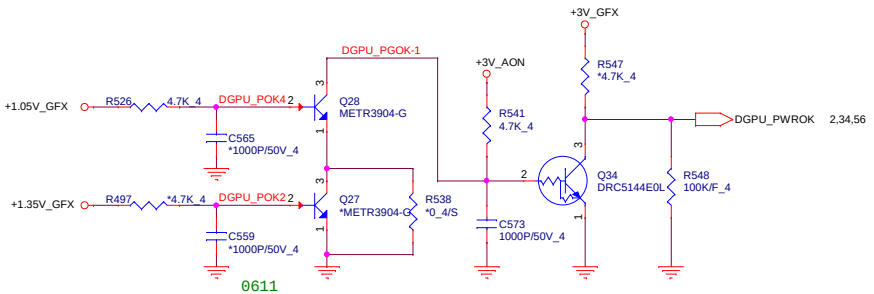



Add L16 (0402) for co-lay

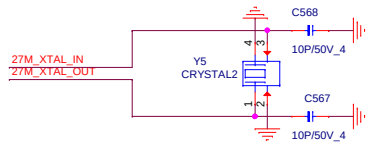
**VID_PLLVDD = 41mA**




0310 Reserve 10K for BXTALOUT




0611
Change R450 to short pad







| | | |
|---|---|---|
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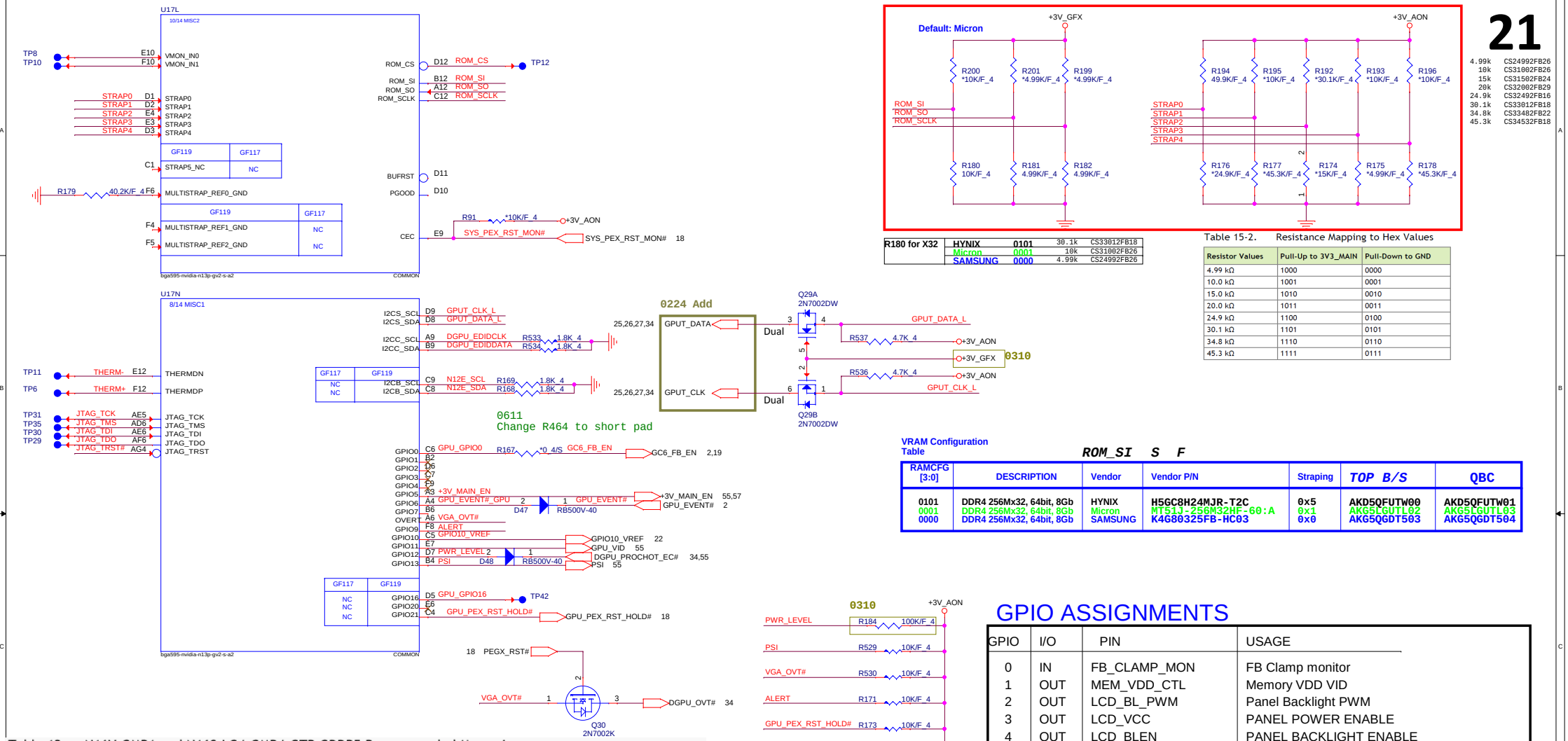


| R180 for X32 | | | | |
|---|---|---|---|---|
| | HYNIX | 0101 | 30.1k | CS33012FB18 |
| | Micron | 0001 | 10k | CS31002FB26 |
| | SAMSUNG | 0000 | 4.99k | CS24992FB26 |

Table 15-2. Resistance Mapping to Hex Values

| Resistor Values | Pull-Up to 3V3_MAIN | Pull-Down to GND |
|---|---|---|
| 4.99 kΩ | 1000 | 0000 |
| 10.0 kΩ | 1001 | 0001 |
| 15.0 kΩ | 1010 | 0010 |
| 20.0 kΩ | 1011 | 0011 |
| 24.9 kΩ | 1100 | 0100 |
| 30.1 kΩ | 1101 | 0101 |
| 34.8 kΩ | 1110 | 0110 |
| 45.3 kΩ | 1111 | 0111 |

**VRAM Configuration Table**

*ROM_SI S F*

| RAMCFG [3:0] | DESCRIPTION | Vendor | Vendor P/N | Straping | *TOP B/S* | QBC |
|---|---|---|---|---|---|---|
| 0101 | DDR4 256Mx32, 64bit, 8Gb | HYNIX | H5GC8H24MJR-T2C | 0x5 | AKD5QFUTW00 | AKD5QFUTW01 |
| 0001 | DDR4 256Mx32, 64bit, 8Gb | Micron | MT51J-256M32HF-60:A | 0x1 | AKG5LGUTL02 | AKG5LGUTL03 |
| 0000 | DDR4 256Mx32, 64bit, 8Gb | SAMSUNG | K4G80325FB-HC03 | 0x0 | AKG5QGDT503 | AKG5QGDT504 |

Table 12. N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories

| Memory Type | FBVDD/ FBVDDQ | Memory Density | Vendor | Manufacturer Part Number | Die Revision | Strap | Memory Speed CK Grade(MHz) | Memory Date Code Minimum | Status |
|---|---|---|---|---|---|---|---|---|---|
| GDDR5 | 1.35V/ 1.35V | 256Mx16 | Samsung | K4G41325FE-HC28 | E-die | 0x7 | 2500 | N/A | Post production ready |
| | | | Samsung | K4G41325FC-HC03 | C-die | 0x3 | 2500 | N/A | Production ready |
| | | | Hynix | H5GC4H24AJR-T2C | A-die | 0x6 | 2500 | N/A | Production ready |
| | | | Micron | EDW4032BABG-60-F | A-die | 0x4 | 2500 | N/A | Production ready |
| | | 128Mx32 | Samsung | K4G41325FE-HC28 | E-die | 0x7 | 2500 | N/A | Post production ready |
| | | | Samsung | K4G41325FC-HC03 | C-die | 0x3 | 2500 | N/A | Production ready |
| | | | Hynix | H5GC4H24AJR-T2C | A-die | 0x6 | 2500 | N/A | Production ready |
| | | | Micron | EDW4032BABG-60-F | A-die | 0x4 | 2500 | N/A | Production ready |
| | | 256Mx32 | Samsung | K4G80325FB-HC03 | B-die | 0x0 | 2500 | N/A | Production ready |
| | | | Micron | MT51J256M32HF-60:A | A-die | 0x1 | 2500 | N/A | Production ready |
| | | 512Mx16 | Samsung | K4G80325FB-HC03 | B-die | 0x0 | 2500 | N/A | Production ready |
| | | | Micron | MT51J256M32HF-60:A | A-die | 0x1 | 2500 | N/A | Production ready |

## GPIO ASSIGNMENTS

| GPIO | I/O | PIN | USAGE |
|---|---|---|---|
| 0 | IN | FB_CLAMP_MON | FB Clamp monitor |
| 1 | OUT | MEM_VDD_CTL | Memory VDD VID |
| 2 | OUT | LCD_BL_PWM | Panel Backlight PWM |
| 3 | OUT | LCD_VCC | PANEL POWER ENABLE |
| 4 | OUT | LCD_BLEN | PANEL BACKLIGHT ENABLE |
| 5 | OUT | Reserved | -- |
| 6 | OUT | FB_CLAMP_TGL_REQ | Active low FB Clamp toggle request |
| 7 | OUT | 3D VISION | 3D VISION LEFT/RIGHT signal |
| 8 | I/O | OVERT | ACTIVE LOW THERMAL OVER TEMP |
| 9 | I/O | ALERT | ACTIVE LOW THERMAL ALERT |
| 10 | OUT | MEM VREF_CTL | MEMMORY VREF CONTROL |
| 11 | OUT | PWR_VID | GPU CORE_VDD PWM Control signal |
| 12 | IN | PWR_LEVEL | AC Power detect or power supply overdraw input |
| 13 | OUT | PSI | Phase Shedding |



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# CHANNEL A: 2G GDDR5

19 VMA_DQ[63..0] — VMA_DQ[31:0]
19 FBA_CMD[31:0] — FBA_CMD[31:0]
19 FBA_DBI[7:0] — FBA_DBI[7:0]
19 FBA_EDC[7:0] — FBA_EDC[7:0]

## MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7

VRAM2 — +1.35V_GFX

VMA_DQ31 M2 … VMA_DQ00 A4 | DQ31 | DQ7 … DQ0 | DQ24 | VDDQ-B1 … VDDQ-T14

FBA_CMD9 J5 … FBA_CMD10 H4 | RFU/A12/NC | A7/A8 | A0/A10 | A6/A11 | A1/A9 | A5/BA1 | A3/BA3 | A4/BA2 | A2/BA0 | A3/BA3 | A5/BA1 | A2 /BA0 | A4/BA2 | A1/A9 | A6/A11 | A0/A10 | A7/A8 | VDD-C5 … VDD-R10

19 VMA_WCK01 — VMA_WCK01 D4 — VMA_WCK01# D5 — WCK01 | WCK23 | WCK01# | WCK23#
19 VMA_WCK23 — VMA_WCK23 P4 — VMA_WCK23# P5

FBA_EDC3 R2 … FBA_EDC0 C2 | EDC3 | EDC0 | EDC2 | EDC1 | EDC1 | EDC2 | EDC3 | EDC0 | VSSQ-A1 … VSSQ-T14

FBA_DBI3 P2 … FBA_DBI0 D2 | DBI3# | DBI0# | DBI2 #| DBI1# | DBI1# | DBI2# | DBI0# | DBI3# |

FBA_CMD12 G3 — FBA_CMD15 L3 — RAS# | CAS# | CAS# | RAS#

19 VMA_CLK0# — VMA_CLK0# J11
19 VMA_CLK0 — VMA_CLK0 J12
FBA_CMD14 J3 — CKE# | CK# | CK

FBA_CMD0 G12 — FBA_CMD5 L12 — CS# | WE# | WE# | CS#

0310 R671/R672 to 121ohm
R546 121/F_4 — R545 1K/F_4 — SEN_R J10 — ZQ | SEN

FBA_CMD13 J2 — R477 1K/F_4 — J1 — RESET# | MF

A5 U5 — Vpp,NC | Vpp,NC1

VREFD_VMA1 A10 U10 — VREFD1 | VREFD2
VREFD_VMA1 0.4MM=16mils

VREFC_VMA1 J14 — VREFC
VREFC_VMA1 0.4MM=16mils

FBA_CMD8 J4 — ABI# | GDDR5

VSS-B5 … VSS-T10 | VRAM2

VREF_VMA1_MOS
+1.35V_GFX — R501 549/F_4 — R493 931/F_4 — VREFC_VMA1 — C560 820P/50V_4
+1.35V_GFX — R505 *549/F_4 — R496 *931/F_4 — VREFD_VMA1 — C566 *820P/50V_4
R494 1.33K/F_4 — R517 *1.33K/F_4
VMA_CLK0# — R544 80.6/F_4 — VMA_CLK0
VREF_VMA1_MOS
Q26 2N7002K — GPIO10_VREF — GPIO10_VREF 21

+1.35V_GFX — Close DRAM
C583 10U/6.3VS_6 — C549 10U/6.3VS_6
C550 1U/6.3V_4 — C551 1U/6.3V_4 — C582 1U/6.3V_4 — C469 1U/6.3V_4
C555 0.1U/16V_4 — C572 0.1U/16V_4 — C471 0.1U/16V_4 — C580 0.1U/16V_4 — C584 0.1U/16V_4 — C569 0.1U/16V_4 — C466 0.1U/16V_4 — C470 0.1U/16V_4 — C585 0.1U/16V_4 — C468 0.1U/16V_4
Under DRAM

## MF=0 Non-mirrored

QD56~63
QD48~55
QD40~47
QD32~39

VRAM1 — +1.35V_GFX

VMA_DQ63 M2 … VMA_DQ32 A4 | DQ31 | DQ7 … DQ0 | DQ24 | VDDQ-B1 … VDDQ-T14

FBA_CMD25 J5 … FBA_CMD26 H4 | RFU/A12/NC | A7/A8 | A0/A10 | A6/A11 | A1/A9 | A5/BA1 | A3/BA3 | A4/BA2 | A2/BA0 | A3/BA3 | A5/BA1 | A2 /BA0 | A4/BA2 | A1/A9 | A6/A11 | A0/A10 | A7/A8 | VDD-C5 … VDD-R10

19 VMA_WCK45 — VMA_WCK45# D4
19 VMA_WCK67 — VMA_WCK67# P4
WCK01 | WCK23 | WCK01# | WCK23# | WCK01#

FBA_EDC7 R2 … FBA_EDC4 C2 | EDC3 | EDC0 | EDC2 | EDC1 | EDC1 | EDC2 | EDC3 | EDC0 | VSSQ-A1 … VSSQ-T14

FBA_DBI7 P2 … FBA_DBI4 D2 | DBI3# | DBI0# | DBI2 #| DBI1# | DBI1# | DBI2# | DBI0# | DBI3# |

FBA_CMD28 G3 — FBA_CMD31 L3 — RAS# | CAS# | CAS# | RAS#

19 VMA_CLK1# — VMA_CLK1# J11
19 VMA_CLK1 — VMA_CLK1 J12
FBA_CMD30 J3 — CKE# | CK# | CK

FBA_CMD16 G12 — FBA_CMD21 L12 — CS# | WE# | WE# | CS#

0310 R671/R672 to 121ohm
R367 121/F_4 — R368 1K/F_4 — SEN_B J10 — ZQ | SEN

FBA_CMD29 J2 — R468 1K/F_4 — J1 — RESET# | MF

A5 U5 — Vpp,NC | Vpp,NC1

VREFD_VMA2 A10 U10 — VREFD1 | VREFD2
VREFD_VMA2 0.4MM=16mils

VREFC_VMA2 J14 — VREFC
VREFC_VMA2 0.4MM=16mils

FBA_CMD24 J4 — ABI# | GDDR5

VSS-B5 … VSS-T10 | VRAM1

VREF_VMA2_MOS
+1.35V_GFX — R407 549/F_4 — R410 931/F_4 — VREFC_VMA2 — C516 820P/50V_4
+1.35V_GFX — R406 *549/F_4 — R409 *931/F_4 — VREFD_VMA2 — C511 *820P/50V_4
R394 1.33K/F_4 — R398 *1.33K/F_4
VMA_CLK1 — R370 80.6/F_4 — VMA_CLK1#
VREF_VMA2_MOS
Q21 2N7002K — GPIO10_VREF

+1.35V_GFX — Close DRAM
C530 10U/6.3VS_6 — C546 10U/6.3VS_6
C578 1U/6.3V_4 — C467 1U/6.3V_4 — C545 1U/6.3V_4 — C527 1U/6.3V_4
C552 0.1U/16V_4 — C535 0.1U/16V_4 — C472 0.1U/16V_4 — C577 0.1U/16V_4 — C571 0.1U/16V_4 — C541 0.1U/16V_4 — C579 0.1U/16V_4 — C465 0.1U/16V_4 — C576 0.1U/16V_4 — C570 0.1U/16V_4
Under DRAM

+1.35V_GFX — C575 0.1U/16V_4 — C547 10U/6.3V_6 — C548 10U/6.3V_6 — C574 10U/6.3V_6

+1.35V_GFX — FBA_CMD14 R476 10K_4 — FBA_CMD30 R469 10K_4
CKE* is strap pin to set ODT value of memory chip

FBA_CMD13 R478 10K_4 — FBA_CMD29 R467 10K_4
RST PD place @ the end of daisy-chain.

**GDDR5 Mode H Mapping**

| < 0-31 > | < 32-63 > | Memory |
|---|---|---|
| CMD0 | CMD16 | CS* |
| CMD1 | CMD17 | A3_BA3 |
| CMD2 | CMD18 | A2_BA0 |
| CMD3 | CMD19 | A4_BA2 |
| CMD4 | CMD20 | A5_BA1 |
| CMD5 | CMD21 | WE* |
| CMD6 | CMD22 | A7_A8 |
| CMD7 | CMD23 | A0_A11 |
| CMD8 | CMD24 | ABI* |
| CMD9 | CMD25 | A12_RFU |
| CMD10 | CMD26 | A0_A10 |
| CMD11 | CMD27 | A1_A9 |
| CMD12 | CMD28 | RAS* |
| CMD13 | CMD29 | RST* |
| CMD14 | CMD30 | CKE* |
| CMD15 | CMD31 | CAS* |

GDDR5 CMD Mapping Table
<0..31> <32..63> MEMORY

| | | |
|---|---|---|
| 12 | 28 | RAS* |
| 15 | 31 | CAS* |
| 5 | 21 | WE* |
| 0 | 16 | CS* |
| 8 | 24 | ABI* |
| 10 | 26 | A0_A10 |
| 11 | 27 | A1_A9 |
| 2 | 18 | A2_BA0 |
| 1 | 17 | A3_BA3 |
| 3 | 19 | A4_BA2 |
| 4 | 20 | A5_BA1 |
| 7 | 23 | A6_A11 |
| 6 | 22 | A7_A8 |
| 9 | 25 | A12_RFU |
| 13 | 29 | RESET* |
| 14 | 30 | CKE* |

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|---|---|---|
| | N15P-GX/GT GDDR5 VRAM 1/2 | 1A |

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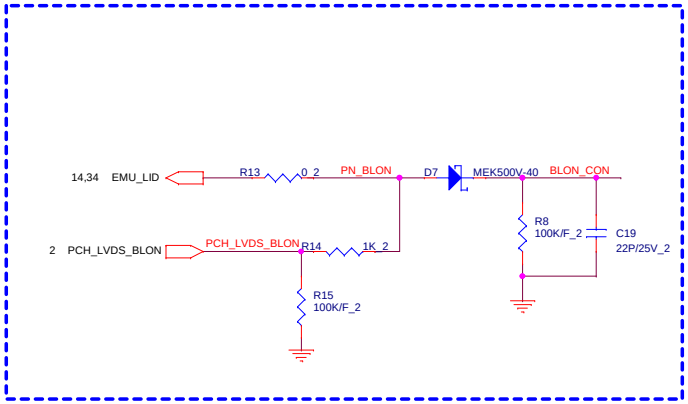
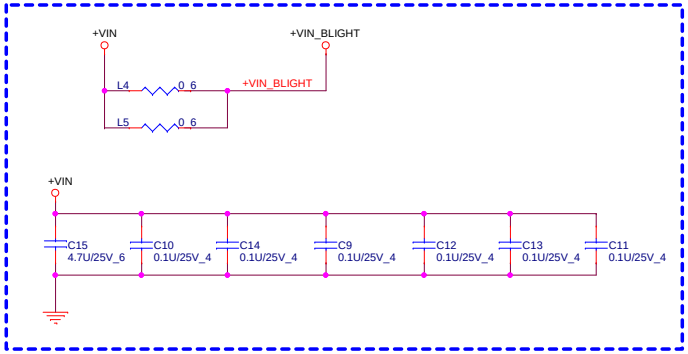
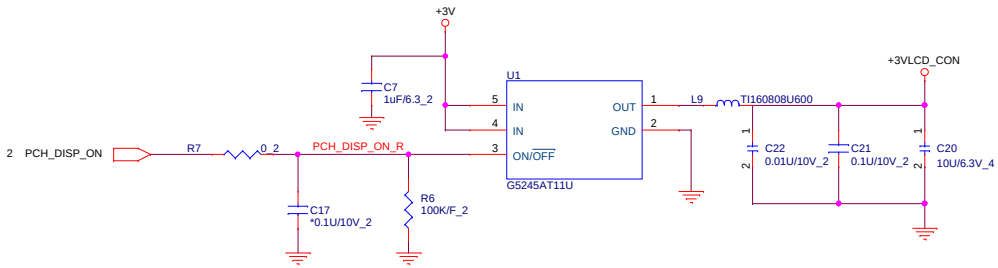
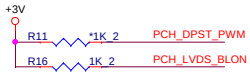
## LID Switch

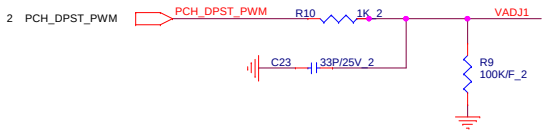


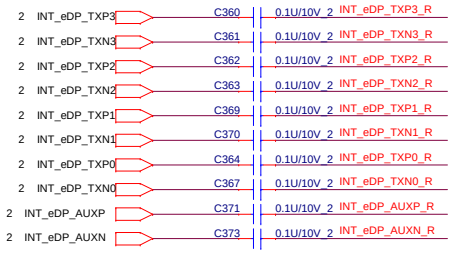

## Panel Vin Cap



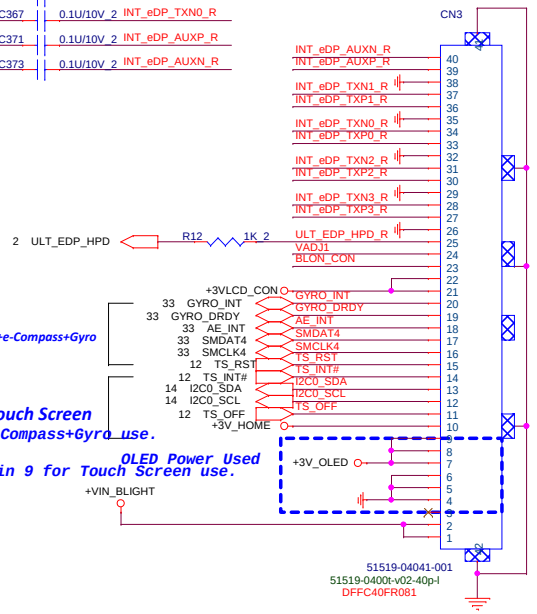




## eDP Conn.




*Accelerometer +e-Compass+Gyro*

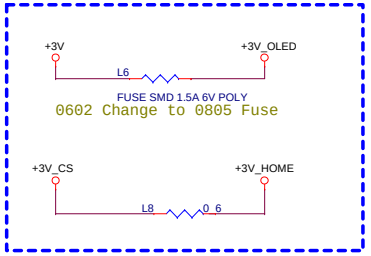
*Touch Screen*

***+3V_HOME Power for Accelerometer +e-Compass+Gyro use.***

***OLED Power Used***

***No support OLED SKU Pin 9 for Touch Screen use.***

## OLED Power Used




+3V 2,4,10,11,12,13,14,15,16,17,19,24,25,28,30,31,33,34,35,40,50,54,55
+VIN 26,31,45,46,47,48,50,51,52,53,55,56,59
+3V_CS 33

| | | |
|---|---|---|
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0525 SI Change U12 P/N AL000175T02

0512 SI Change
R112/R115/R116/R117/R118/R119 to 10ohm

4K_175@PS175HDMBGA64GTR2-B1

Need Check Connection Jun 20160414

Jun Modify 20160414

0323 modify

*Clamp-Diode

NM3 type
footprint check OK

Need to close to REXT pin

Add ground shielding between REXT and XTLO/XTLI

GPIO2: Firmware Initial Address, internal pull-up ~80K
0: Start from Bank 7 1: Start from Bank 3 (default)

I2C_ADDR/GPIO5: Control I2C slave address selection, internal pull-down ~80K
0: 0x10h - 0x2Fh (default) 1: 0x90h - 0x9Fh, 0xD0h - 0xDFh

CEC_EN/GPIO4: For debug purpose

0523 change Q7 to BAM37EN0000

| | | |
|---|---|---|
| PROJECT : Pegasus | | |
| Quanta Computer Inc. | | |
| NB5 | Size: Custom | Document Number: HDMI |
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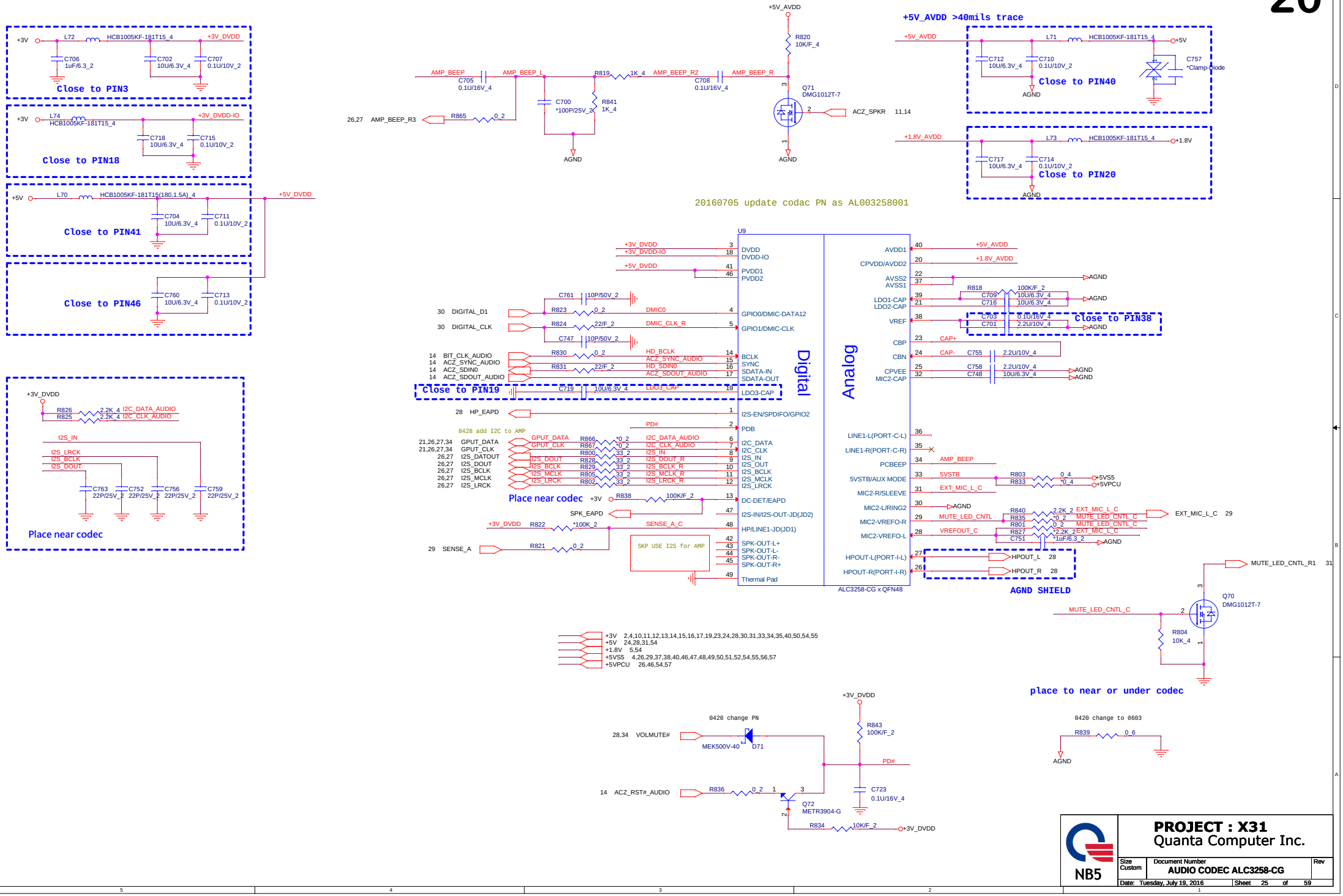


| | | |
|---|---|---|
| NB5 | PROJECT : X31<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: AUDIO CODEC ALC3258-CG | Rev |
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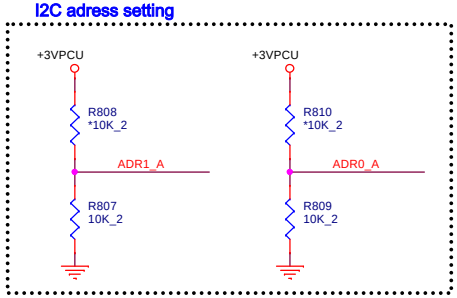
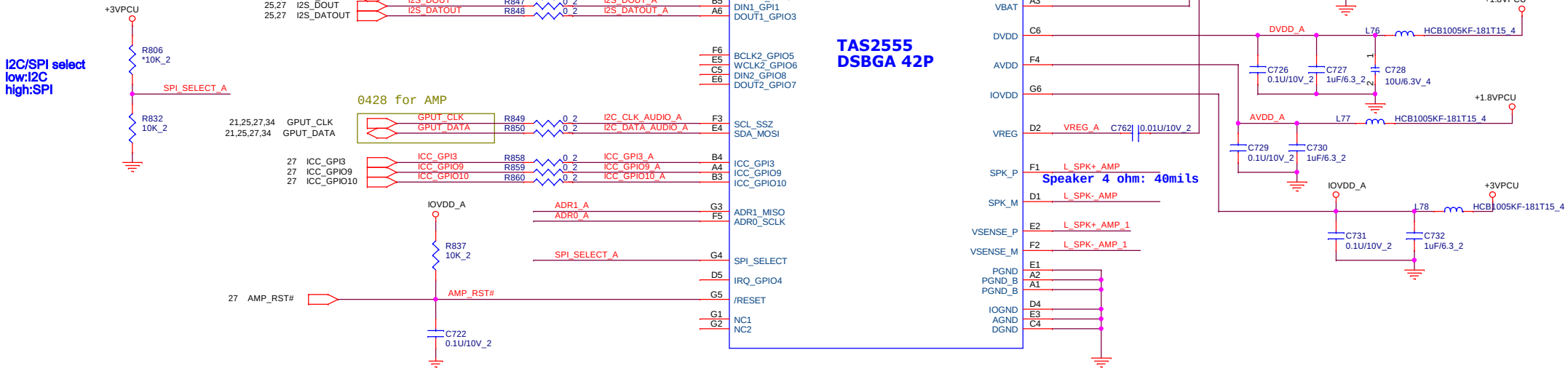
## I2C adress setting



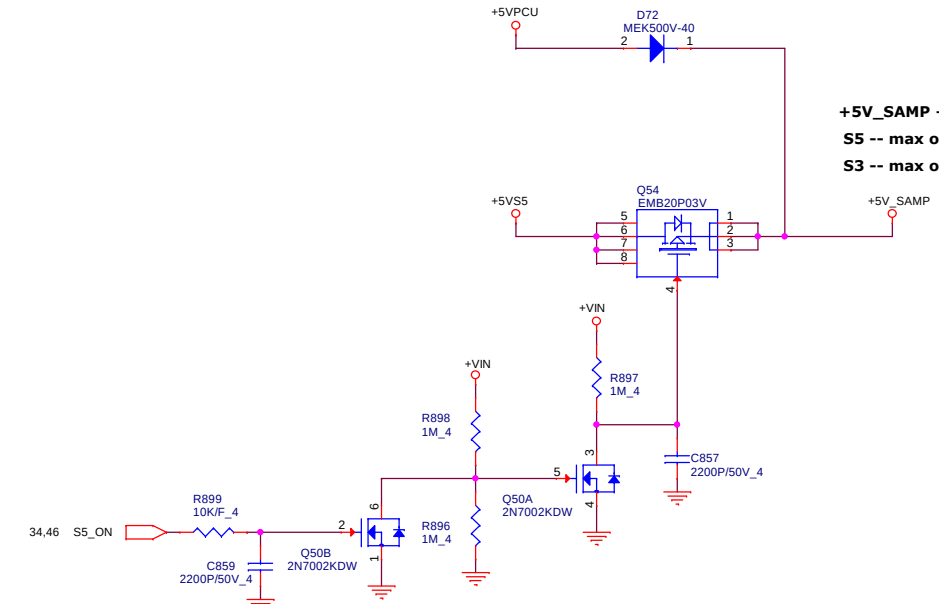

| ADR0/ADR1 | |
|---|---|
| 00 : 0x4C | 10 :0X4E |
| 01 :0X4D | 11 :0X4F |

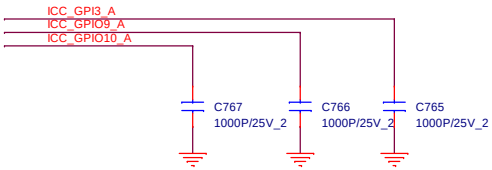
20160705 update AMP PN as AL002555T02

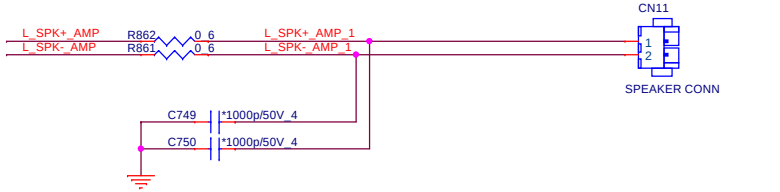









+5V_SAMP 27
+5VPCU 25,46,54,57
+5VS5 4,25,29,37,38,40,46,47,48,49,50,51,52,54,55,56,57
+VIN 23,31,45,46,47,48,50,51,52,53,55,56,59
+3VPCU 6,13,27,29,31,32,34,37,45,46,53,58
+5V 24,25,28,31,54
+1.8VPCU 27,46

NB5

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| A3 | AUDIO AMP TAS2555 | 1A |

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| ADR0/ADR1 | |
|---|---|
| 00 : 0x4C | 10 :0X4E |
| 01 :0X4D | 11 :0X4F |

I2C adress setting

+3VPCU
R815 *10K_2
ADR1_B
R814 10K_2

+3VPCU
R817 10K_2
ADR0_B
R816 *10K_2

20160705 update AMP PN as AL002555T02

U25

TAS2555
DSBGA 42P

25,26 AMP_BEEP_R3
C862 0.1U/10V_2 IN_MR
C3 IN_P
D3 IN_M

25,26 I2S_MCLK
25,26 I2S_BCLK
25,26 I2S_LRCK
25,26 I2S_DOUT
25,26 I2S_DATOUT
I2S_MCLK R851 0_2 I2S_MCLK_B D6 MCLK_GPI2
I2S_BCLK R852 0_2 I2S_BCLK_B B6 BCLK1_GPIO1
I2S_LRCK R854 0_2 I2S_LRCK_B A5 WCLK1_GPIO2
I2S_DOUT R853 0_2 I2S_DOUT_B B5 DIN1_GPI1
R855 0_2 I2S_DATOUT_B A6 DOUT1_GPIO3

+3VPCU
R813 *10K_2
SPI_SELECT_B
R811 10K_2
I2C/SPI select
low:I2C
high:SPI

F6 BCLK2_GPIO5
E5 WCLK2_GPIO6
C5 DIN2_GPIO8
E6 DOUT2_GPIO7

0428 for AMP

21,25,26,34 GPUT_CLK
21,25,26,34 GPUT_DATA
GPUT_CLK R856 0_2 I2C_CLK_AUDIO_B F3 SCL_SSZ
GPUT_DATA R857 0_2 I2C_DATA_AUDIO_B E4 SDA_MOSI

26 ICC_GPIO10
26 ICC_GPIO9
26 ICC_GPI3
ICC_GPIO10 B4 ICC_GPI3
ICC_GPIO9 A4 ICC_GPIO9
ICC_GPI3 B3 ICC_GPIO10

IOVDD_B
R812 10K_2
ADR1_B G3 ADR1_MISO
ADR0_B F5 ADR0_SCLK
SPI_SELECT_B G4 SPI_SELECT
D5 IRQ_GPIO4
26 AMP_RST#
AMP_RST# G5 /RESET
C745 0.1U/10V_2
G1 NC1
G2 NC2

SW B1 SW_B
SW B2
need change PN
L79 2.2uH/3A_4020
VBOOST C1
VBOOST C2
VBOOST_B
VBAT A3
DVDD C6
AVDD F4
IOVDD G6
VREG D2
VREG_B C742 0.01U/10V_2
SPK_P F1 R_SPK+_AMP
Speaker 4 ohm: 40mils
SPK_M D1 R_SPK-_AMP
VSENSE_P E2 R_SPK+_AMP_1
VSENSE_M F2 R_SPK-_AMP_1
PGND E1
PGND_B A2
PGND_B A1
IOGND D4
AGND E3
DGND C4

+5V_SAMP
C734 0.1U/10V_2
C735 1uF/6.3_2
C746 10U/6.3V_4
TP71
C736 0.1U/16V_2
C764 22U/16V_8
+1.8VPCU
DVDD_B
L81 HCB1005KF-181T15_4
C737 0.1U/10V_2
C739 1uF/6.3_2
C738 10U/6.3V_4
+1.8VPCU
AVDD_B
L80 HCB1005KF-181T15_4
C740 0.1U/10V_2
C741 1uF/6.3_2
IOVDD_B
+3VPCU
L82 HCB1005KF-181T15_4
C744 1uF/6.3_2
0503 Del C743

ICC_GPI3
ICC_GPIO9
ICC_GPIO10
C770 1000P/25V_2
C769 1000P/25V_2
C768 1000P/25V_2
0420 change C768/C769/C770

SPK-AMP-R
Wire Black
Wire Red

R_SPK-_AMP R864 0_6 R_SPK-_AMP_1
R_SPK+_AMP R863 0_6 R_SPK+_AMP_1
CN13
1
2
3 6
4 5
SPEAKER CONN
14 SPK_ID_CODEC
C720 *1000p/50V_4
C721 *1000p/50V_4

+3VPCU 6,13,26,29,31,32,34,37,45,46,53,58
+5V 24,25,28,31,54
+1.8VPCU 26,46
+5V_SAMP 26

I'm from VIETNAM sualaptop365

PROJECT : X31
Quanta Computer Inc.
NB5
Size A3
Document Number AUDIO AMP TAS2555
Rev 1A
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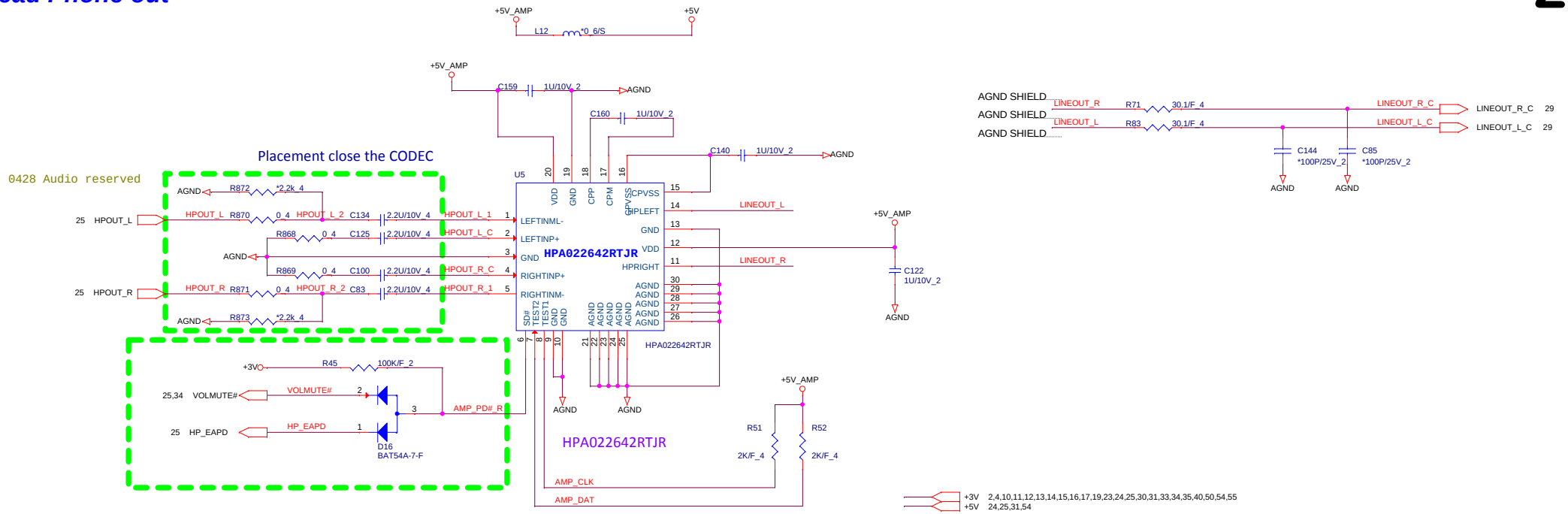
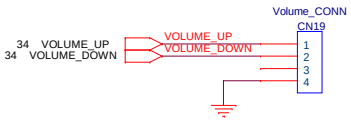
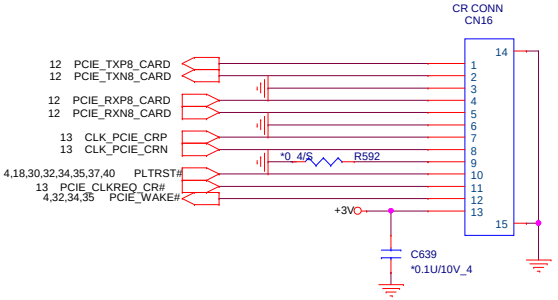
## Head Phone out




## Volume up/down Button

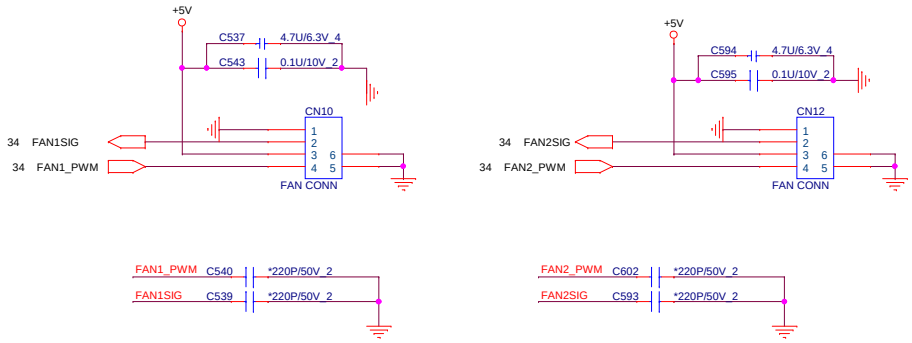



## Card Reader CONN



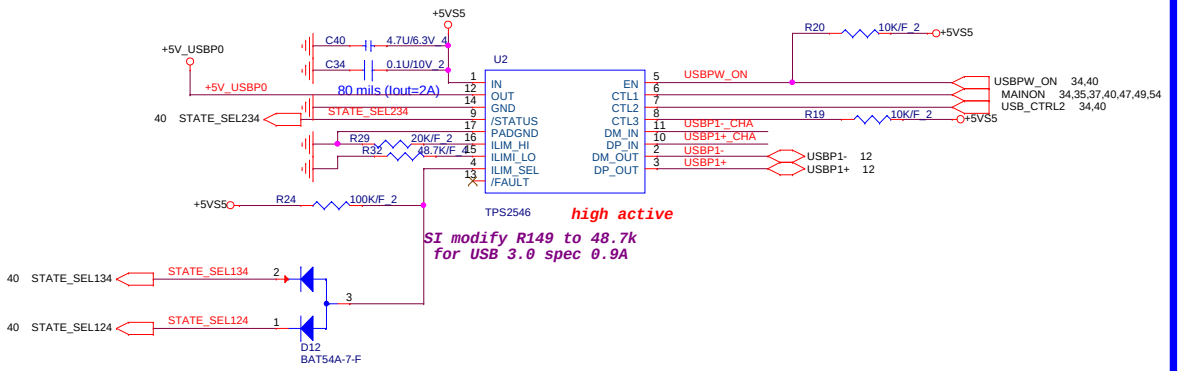

## FAN

0426 Update CN10/CN12 PN and FP




| | |
|---|---|
| PROJECT : X31 | Quanta Computer Inc. |
| Size: Custom | Document Number: AUDIO AMP/FAN/Volume Button |
| Rev | |
| NB5 | Date: Tuesday, July 19, 2016 Sheet 28 of 59 |

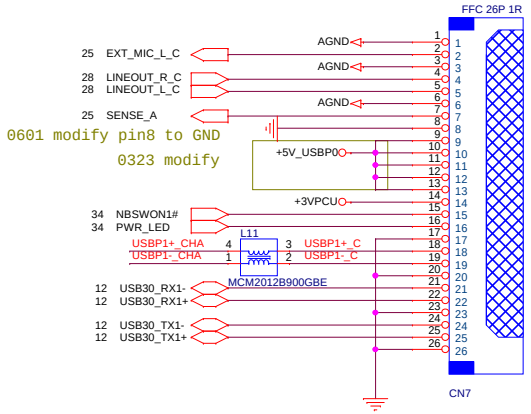
## For Daughter USB3.0 CN




## UART for DEBUG

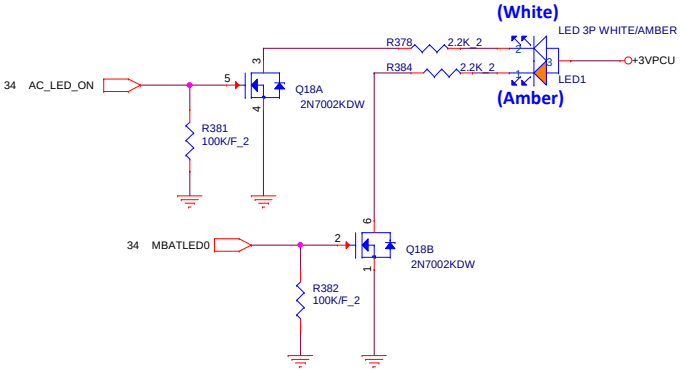
UART for Win7 DEBUG

## Audio Combo Jack + USB3.0 Daughter Board+PW BTM




0304 modify USB3.0 connection for daughter board

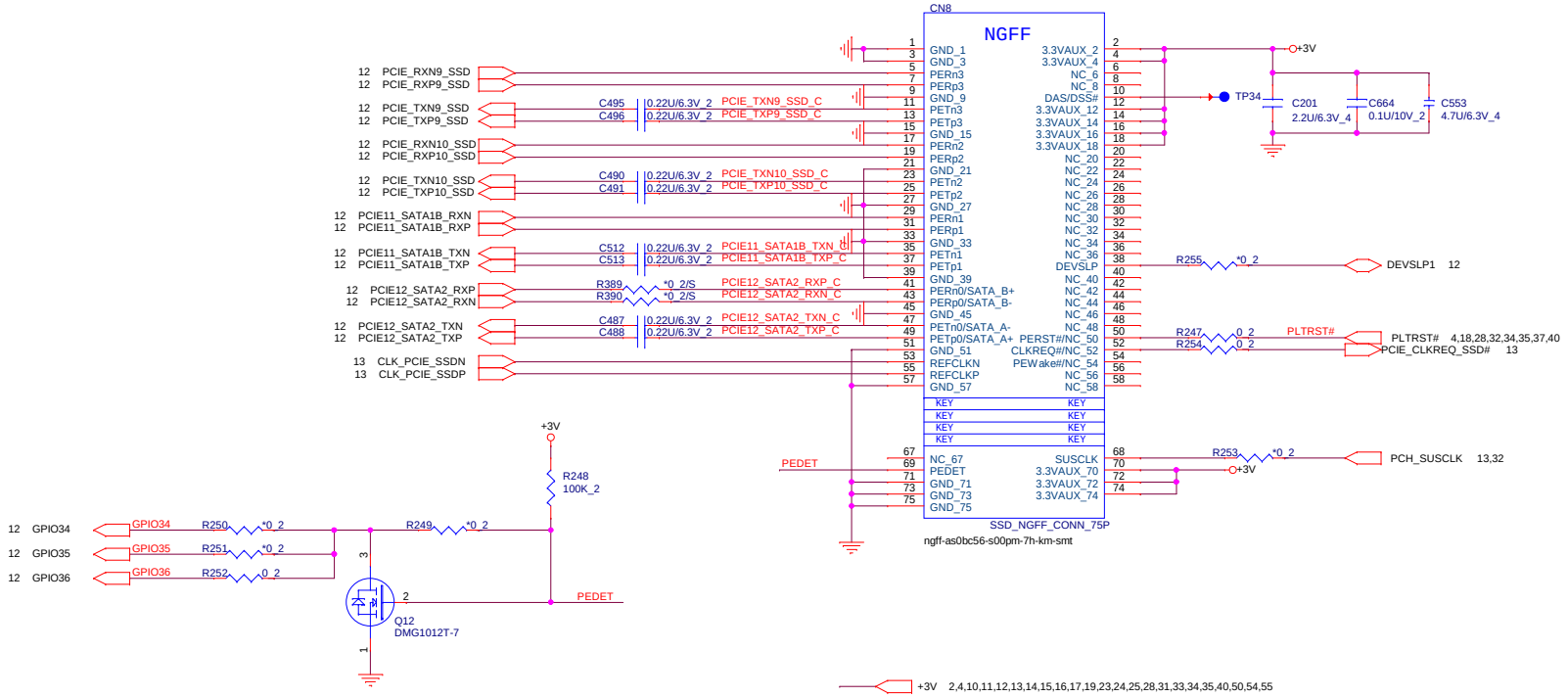
## AC_IN / BATTERY LOW LED



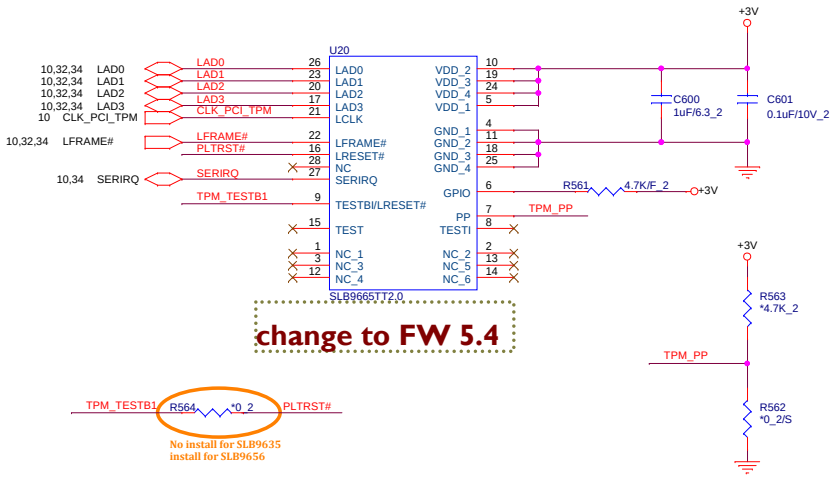

| | | |
|---|---|---|
| NB5 | PROJECT : X31<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: USB20/30 | Rev |
| Date: Tuesday, July 19, 2016 | Sheet 29 of 59 | |

## SSD CONN

CONN: M KEY
MODULE: N/A



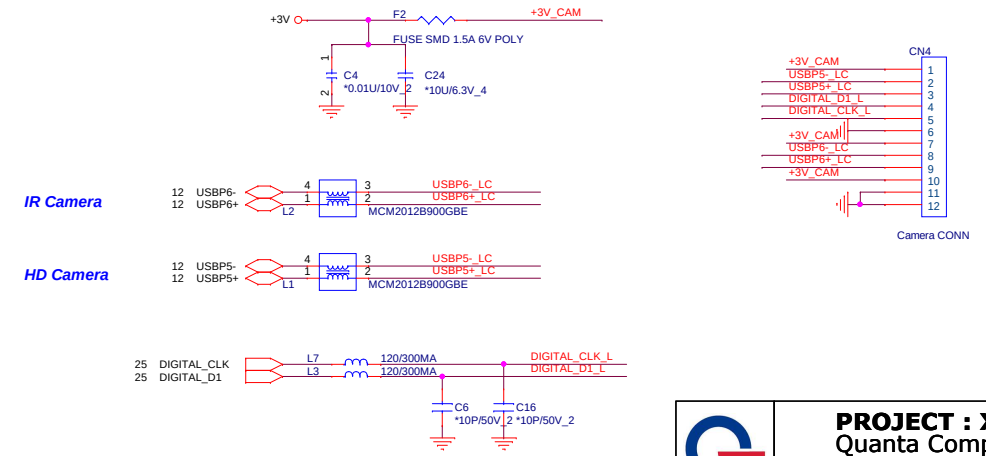

## TPM (2.0)




## CAMERA CONN

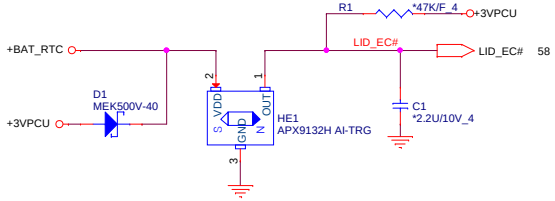
0602 SI Change poly fuse to 0805

*Camera 3V, 620mA*

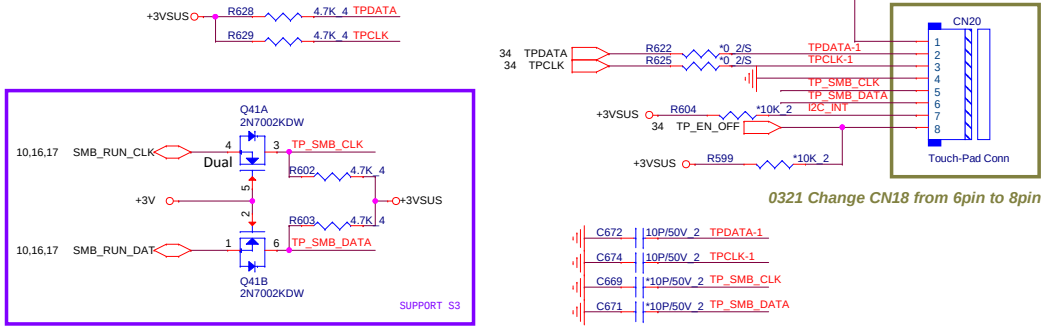



| | | | |
|---|---|---|---|
| NB5 | PROJECT : X31<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: NGFF HDD/TPM/CR | Rev |
| | Date: Tuesday, July 19, 2016 | Sheet 30 of 59 | |

## LID switch



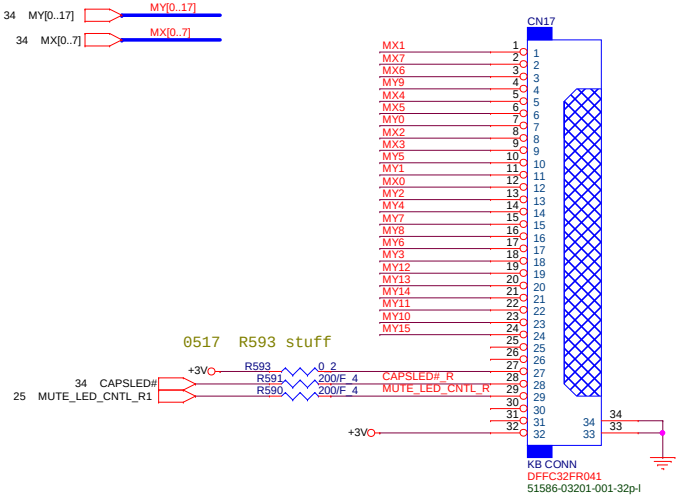

## Touch Pad Connector




*0321 Change CN18 from 6pin to 8pin*

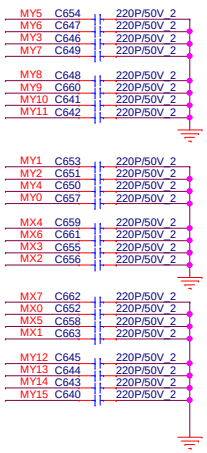
+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,33,34,35,40,50,54,55
+5V 24,25,28,54
+VIN 23,26,45,46,47,48,50,51,52,53,55,56,59
+3VSUS 32,54
+3VPCU 6,13,26,27,29,32,34,37,45,46,53,58
+BAT_RTC 4,13,15,45,58

## KEYBOARD Con.

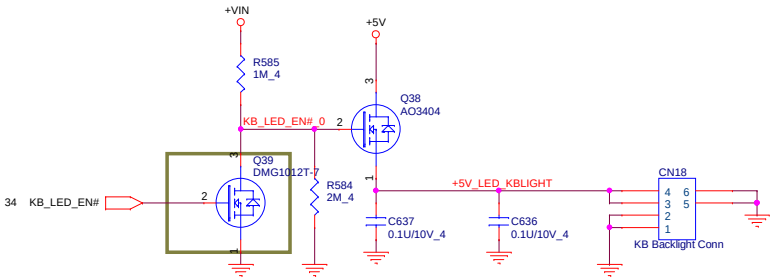



20160705 Del Q40,R589,MUTE_LED_EC

## KEYBOARD PULL-UP




## KB backlight




*0201 Change Footprint*

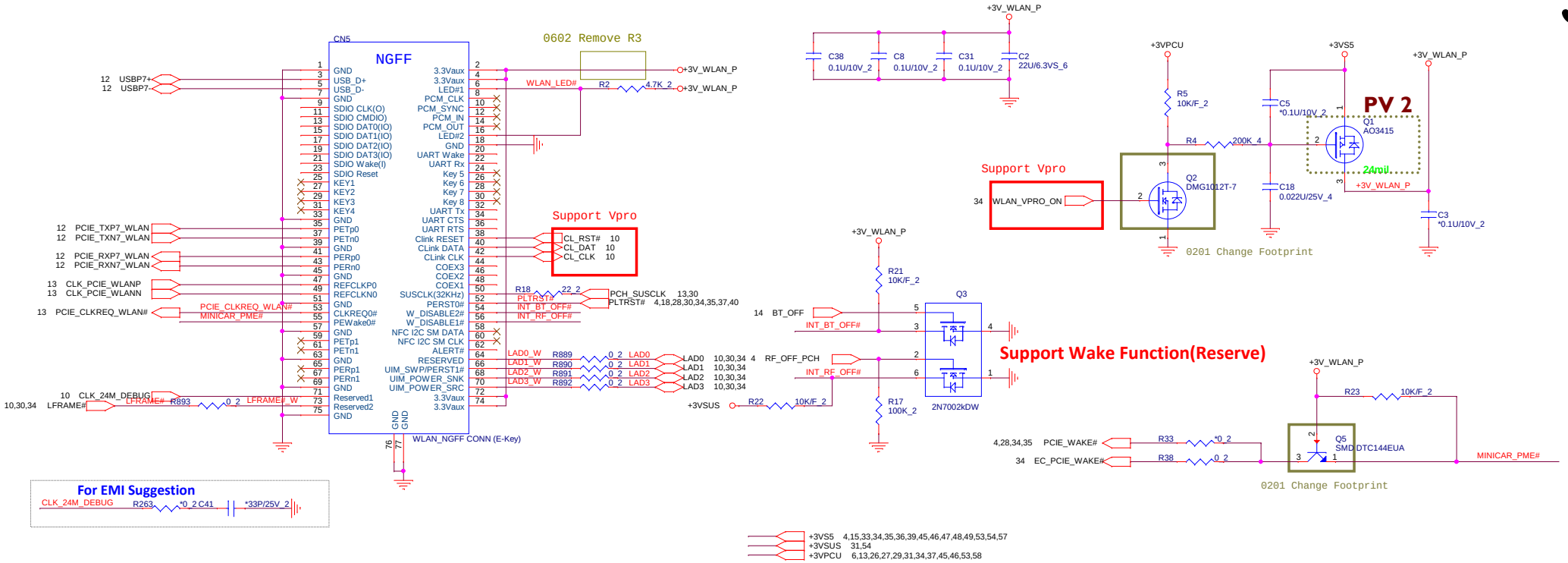
**PROJECT : X31**
Quanta Computer Inc.

NB5

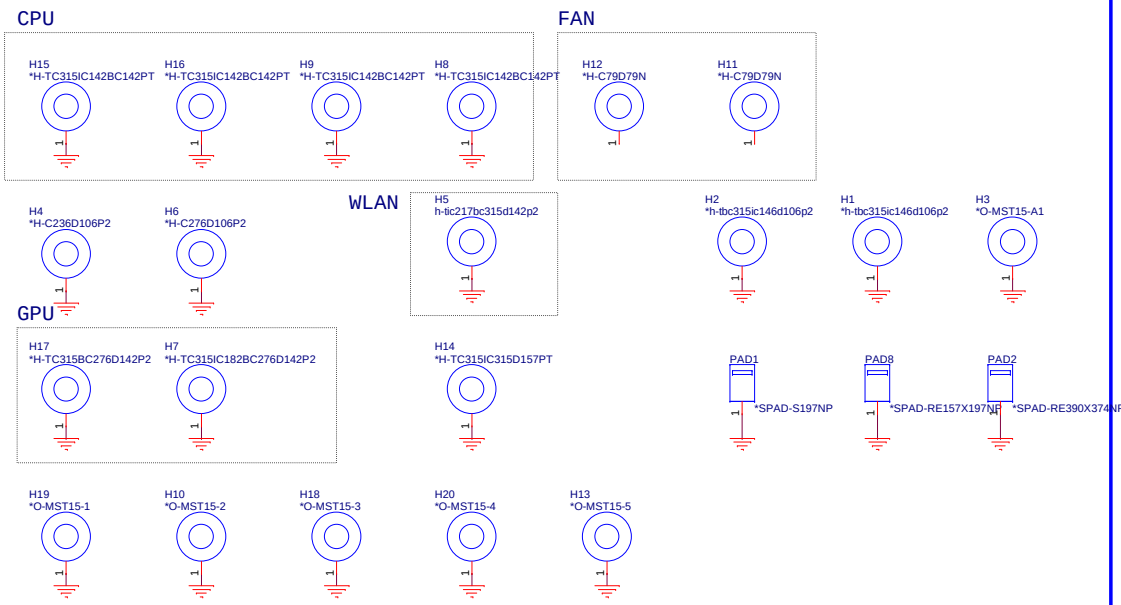
| Size | Document Number | Rev |
|---|---|---|
| Custom | KB/PB/TP | |
| Date: Tuesday, July 19, 2016 | Sheet 31 of 59 | |

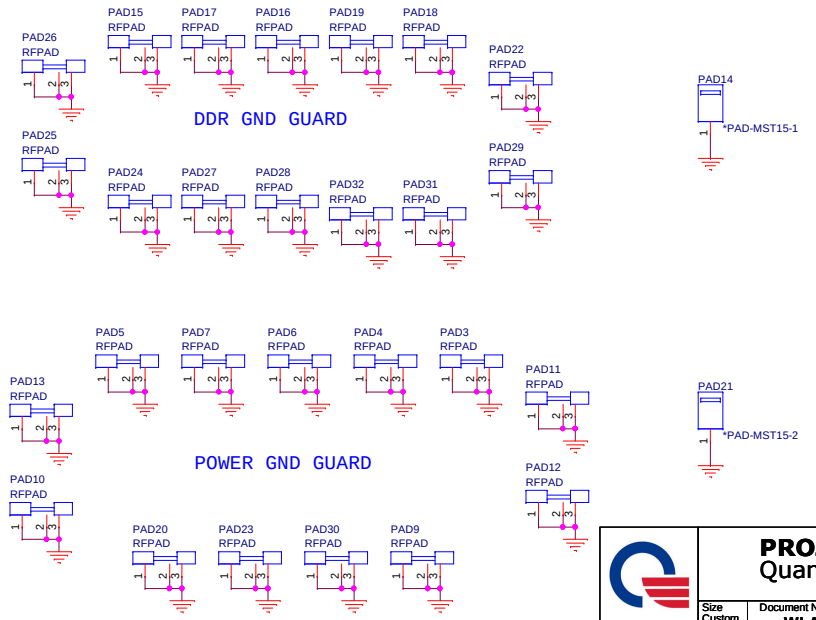
# WLAN/BT






# Hole



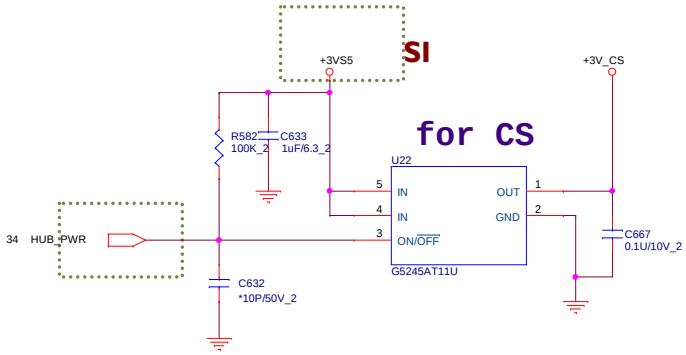



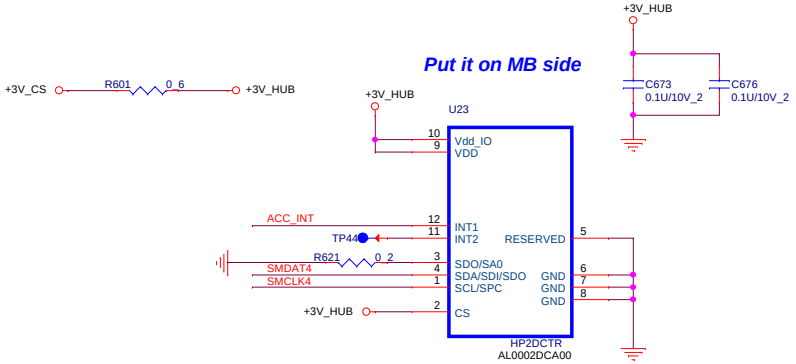

**PROJECT : X31**
Quanta Computer Inc.

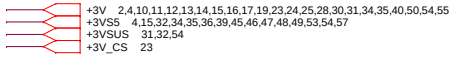
NB5

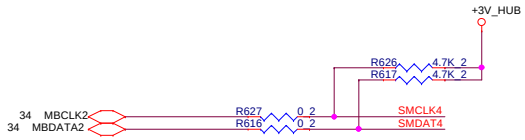
| Size | Document Number | Rev |
|---|---|---|
| Custom | WLAN/HOLE | |
| Date: Tuesday, July 19, 2016 | Sheet 32 of 59 | |

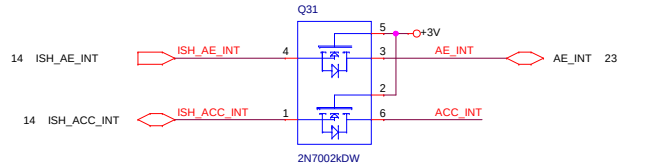
# Accelerometer Sensor

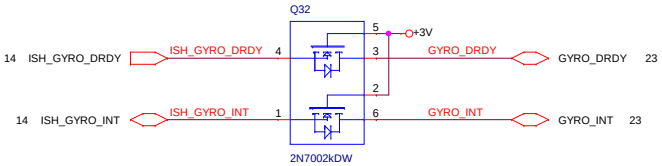


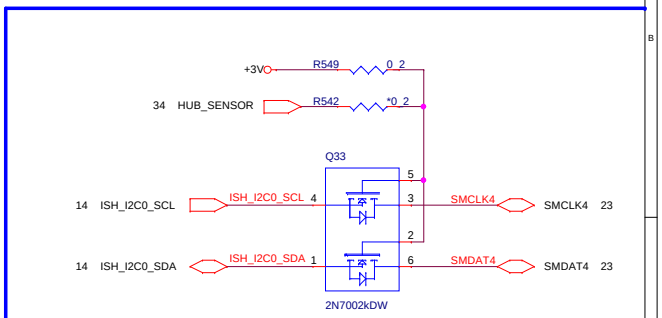




NB5

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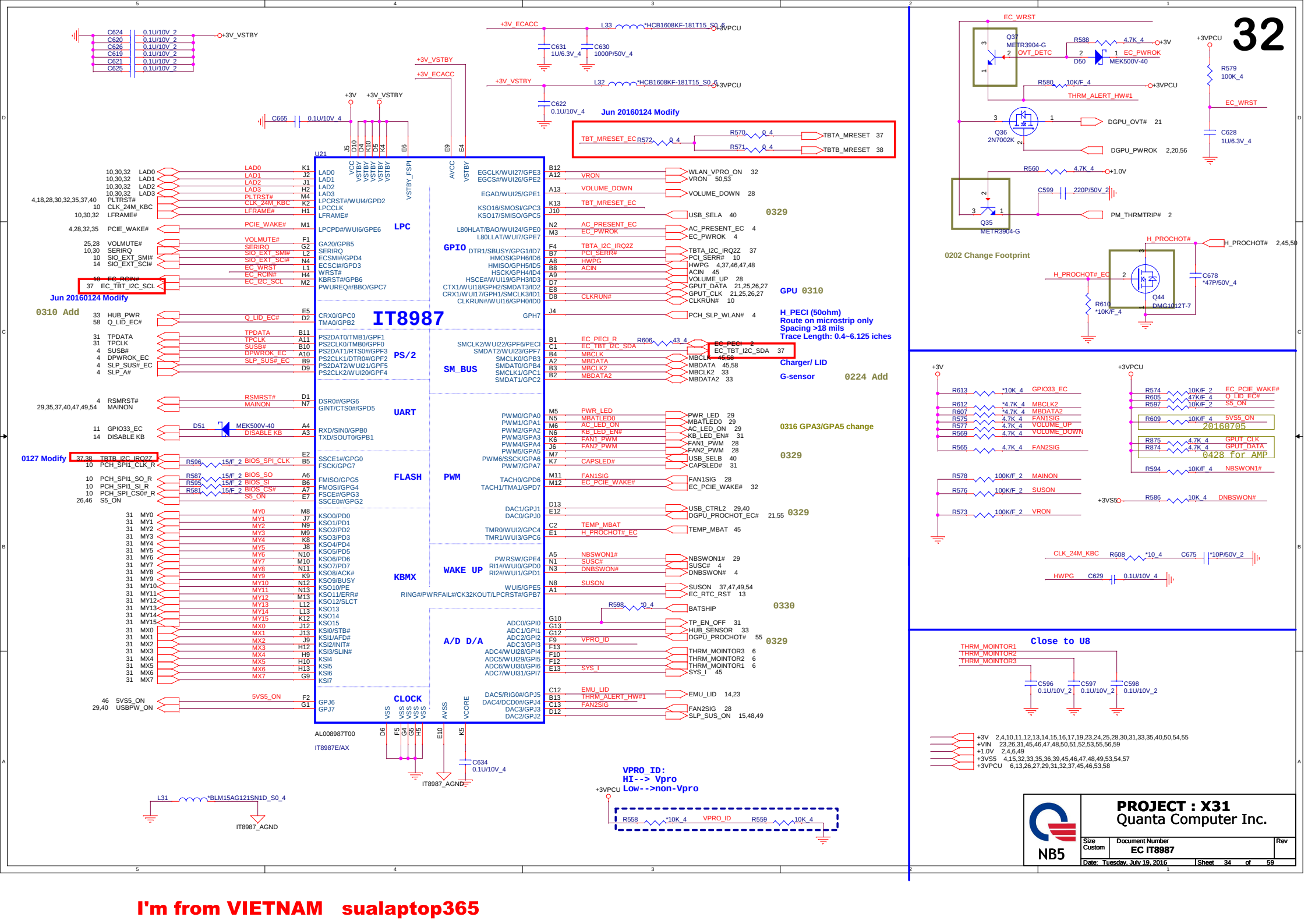
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SENSOR HUB | |
| Date: Tuesday, July 19, 2016 | Sheet 33 of 59 | |


32
IT8987
LPC
GPIO
SM_BUS
PS/2
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
Jun 20160124 Modify
0310 Add
0127 Modify
0329
0330
0224 Add
0316 GPA3/GPA5 change
0202 Change Footprint
GPU 0310
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
Charger/ LID
G-sensor
Close to U8
VPRO_ID:
HI--> Vpro
Low-->non-Vpro
PROJECT : X31
Quanta Computer Inc.
NB5
EC IT8987
Date: Tuesday, July 19, 2016
Sheet 34 of 59
I'm from VIETNAM sualaptop365

25MHz, 30ppm, 20pF AR Crystal

C464 6.8P/50V_4
Y2 25MHZ +-10PPM
TBT_XTAL_25_IN
TBT_XTAL_25_OUT
C482 6.8P/50V_4

Jun 20160124 Modify

VCC3V3_FLASH R423 0_4

8Mbit Flash (Mutual for AR and ACE)

R417 3.32K/F_4 R422 3.32K/F_4 R420 3.32K/F_4
C522 0.1U/10V_2
R418 3.32K/F_4
U14 W25Q80DVSSIG
TBT_EE_CS_N TBT_EE_DO TBT_EE_WP_N
TBT_HOLD_N TBT_EE_CLK TBT_EE_DI
AKE3GGN0N00
IC FLASH (8P)W25Q80DVSSIG (SOIC)
Silk: "NVM"

SPI/EE: AR to/from NVM & ACE

AR_DDC_CLK R111 2.2K_2 VCC3P3_S0
AR_DDC_DAT R89 2.2K_2
TBT_HDMI_DDC_DATA R363 2.2K_2
TBT_HDMI_DDC_CLK R365 2.2K_2

TBT_CIO_PLUG_EVENT R114 10K/F_2 +VCC3P3_SX
TBT_I2C_SDA R333 2.2K_2
TBT_I2C_SCL R343 2.2K_2
TBTA_I2C_INT R68 10K/F_2

Jun Modify 20160414

TBTA_ACE_GPIO0 R43 100K/F_2
TBT_SNK1_DDC_CLK R108 100K/F_2
AR_DDC_EN R84 100K/F_2
TBT_FORCE_PWR R63 100K/F_2
TBT_TMU_CLK_OUT R358 100K/F_2
DDI1_HPD0 R113 100K/F_2
TBTA_LSTX R258 1M/F_2
TBTA_HPD R82 100K/F_2
TBTA_LSRX R259 1M/F_2

Jun Modify 20160601

TBT_SRC_CFG1 = 0 , AUX CONNECTS TO AR
TBT_SRC_CFG1 = 1 , ddc CONNECTS TO AR

TBT_GPIO7 R374 *10K/F_2 +3VS5

NOTE:
ASSEMBLE R548, R549 if DPSRC
NOT IN USE

TBT_GPIO7 R366 1M/F_2
TypeC2_DDI2_HPD R798 1M/F_2

IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

| GPIO | TERMINATION | Power Rail |
|---|---|---|
| GPIO_0 | 10K PU | VCC3V3_LC |
| GPIO_1 | 10K PU | VCC3V3_LC |
| GPIO_2 | 100K PD | |
| GPIO_3 | 100k PD | |
| GPIO_4 | 10K PU | VCC3V3_LC |
| GPIO_5 | 10K PU | VCC3V3_LC |
| GPIO_6 | 100K PD | |
| GPIO_7 | 100K PD | |
| GPIO_8 | 100K PD | |
| POC_GPIO_0 | 10K PU | VCC3V3_TBT_SX |
| POC_GPIO_1 | 10K PU | VCC3V3_TBT_SX |
| POC_GPIO_2 | 100K PD | |
| POC_GPIO_3 | 100K PD | |
| POC_GPIO_4 | 10K PU | VCC3V3_TBT_SX |
| POC_GPIO_5 | 10K PU | VCC3V3_TBT_SX |
| POC_GPIO_6 | 100K PD | |

**NOTE:**
**SNK0_DDC_data/clk ?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.**
**SNK1_DDC_data ?connect to 100k PD. If SRC0 support HDMI, connect as SNK0_CFG1 to GPU and/or appropriate AUX/DDC demux control**
**SNK1_DDC_clk ?connect to 100k PD.**

CPU PCIE TX
12 PCIE_TXP5_TBT
12 PCIE_TXN5_TBT
12 PCIE_TXP6_TBT
12 PCIE_TXN6_TBT
13 CLK_PCIE_TBTP
13 CLK_PCIE_TBTN
13 PCIE_CLKREQ_TBT#

CPU DDI1
2 DDI1_TX0_DP
2 DDI1_TX0_DN
2 DDI1_TX1_DP
2 DDI1_TX1_DN
2 DDI1_TX2_DP
2 DDI1_TX2_DN
2 DDI1_TX3_DP
2 DDI1_TX3_DN
2 DDI1_AUX_DP
2 DDI1_AUX_DN
2 DDI1_HPD0

PCIe GEN3
PCIE_RX0_P PCIE_RX0_N
PCIE_RX1_P PCIE_RX1_N
PCIE_RX2_P PCIE_RX2_N
PCIE_RX3_P PCIE_RX3_N
PCIE_REFCLK_100_IN_P PCIE_REFCLK_100_IN_N PCIE_CLKREQ_N
PCIE_TX0_P PCIE_TX0_N
PCIE_TX1_P PCIE_TX1_N
PCIE_TX2_P PCIE_TX2_N
PCIE_TX3_P PCIE_TX3_N
PERST_N
PCIE_RBIAS R85 3.01K/F_4

CPU PCIE RX
PCIE_RXP5_TBT_C C457 0.22U/6.3V_2 PCIE_RXP5_TBT 12
PCIE_RXN5_TBT_C C460 0.22U/6.3V_2 PCIE_RXN5_TBT 12
PCIE_RXP6_TBT_C C435 0.22U/6.3V_2 PCIE_RXP6_TBT 12
PCIE_RXN6_TBT_C C441 0.22U/6.3V_2 PCIE_RXN6_TBT 12

PLTRST# 4,18,28,30,32,34,37,40

SINK PORT 0
DPSNK0_ML0_P DPSNK0_ML0_N
DPSNK0_ML1_P DPSNK0_ML1_N
DPSNK0_ML2_P DPSNK0_ML2_N
DPSNK0_ML3_P DPSNK0_ML3_N
DPSNK0_AUX_P DPSNK0_AUX_N
DPSNK0_HPD
DPSNK0_DDC_CLK DPSNK0_DDC_DATA

SOURCE PORT 0
DPSRC_ML0_P DPSRC_ML0_N
DPSRC_ML1_P DPSRC_ML1_N
DPSRC_ML2_P DPSRC_ML2_N
DPSRC_ML3_P DPSRC_ML3_N
DPSRC_AUX_P DPSRC_AUX_N
DPSRC_HPD
DPSRC_RBIAS R76 14K_4

Jun Modify 20160414

SINK PORT 1
DPSNK1_ML0_P DPSNK1_ML0_N
DPSNK1_ML1_P DPSNK1_ML1_N
DPSNK1_ML2_P DPSNK1_ML2_N
DPSNK1_ML3_P DPSNK1_ML3_N
DPSNK1_AUX_P DPSNK1_AUX_N
DPSNK1_HPD
DPSNK1_DDC_CLK DPSNK1_DDC_DATA
DPSNK_RBIAS R106 14K_4

Jun Modify 20160414

LC GPIO
GPIO_0 TBT_I2C_SDA 37
GPIO_1 TBT_I2C_SCL 37
GPIO_2 TBT_TMU_CLK_OUT
GPIO_3 PCIE_WAKE# 4,28,32,34
GPIO_4 TBT_CIO_PLUG_EVENT
GPIO_5 TBT_HDMI_DDC_DATA
GPIO_6 TBT_HDMI_DDC_CLK
GPIO_7 TBT_GPIO7
GPIO_8

POC GPIO
POC_GPIO_0 TBTB_I2C_INT
POC_GPIO_1 TBTA_ACE_GPIO0
POC_GPIO_2
POC_GPIO_3 R326 0_2 TBT_FORCE_PWR 12
POC_GPIO_4 R297 0_2 BATLOW# 4
POC_GPIO_5 TBTB_ACE_GPIO0 MAINON 29,34,37,40,47,49,54
POC_GPIO_6

0329
TBTA_I2C_INT 37
TP51
TBTA_ACE_GPIO0 37
TP50

Jun Modify 20160414

Misc
TEST_EN E1 TBT_TEST_EN R296 100/F_2
TEST_PWR_GOOD AB5 TBT_TEST_PWG R391 100/F_2
RESET_N F4 TBT_RESET_N 37

20160705 for leakage
+3V
R900 10K/F_2
D73 MEK500V-40 TBT_HTPLG 14

TBT_CIO_PLUG_EVENT_N:
Connect to PCH (Make sure PCH supports SCI)

20160705 for leakage
BATLOW# R901 10K/F_2 +VCC3P3_SX

MISC
TDI TMS TCK TDO
TBT_TDI V4
TBT_TMS V4
TBT_TCK T4
TBT_TDO W4
+/-0.5%
R50 4.75K/F_4 TBT_RBIAS TBT_RSENSE
RBIAS RSENSE
XTAL_25_IN D22 TBT_XTAL_25_IN
XTAL_25_OUT D23 TBT_XTAL_25_OUT
EE_DI AB3 TBT_EE_DI 37
EE_DO AC4 TBT_EE_DO 37
EE_CS_N AC3 TBT_EE_CS_N 37
EE_CLK AB4 TBT_EE_CLK 37

TBT PORT A
41 TBTA_CA2HD_1_P
41 TBTA_CA2HD_1_N
41 TBTA_HD2CA_1_P
41 TBTA_HD2CA_1_N
41 TBTA_HD2CA_0_P
41 TBTA_HD2CA_0_N
41 TBTA_CA2HD_0_P
41 TBTA_CA2HD_0_N
37 TBTA_DPSRC_AUX_P
37 TBTA_DPSRC_AUX_N
40 TBTA_USB2_D_P
40 TBTA_USB2_D_N
37 TBTA_LSTX
37 TBTA_LSRX
37 TBTA_HPD

Port A
PA_RX1_P PA_RX1_N
PA_TX1_P PA_TX1_N
PA_TX0_P PA_TX0_N
PA_RX0_P PA_RX0_N
C380 0.22U/6.3V_2 TBTA_TX1_P
C379 0.22U/6.3V_2 TBTA_TX1_N
C377 0.22U/6.3V_2 TBTA_TX0_P
C378 0.22U/6.3V_2 TBTA_TX0_N
C509 0.1uF/10V_2 TBTA_AUX_P
C510 0.1uF/10V_2 TBTA_AUX_N
PA_DPSRC_AUX_P PA_DPSRC_AUX_N
PA_USB2_D_P PA_USB2_D_N
PA_LSTX PA_LSRX PA_DPSRC_HPD
PA_USB2_RBIAS R64 499/F_4 PA_USB2_RBIAS

TBT PORTS
PORT B
PB_RX1_P PB_RX1_N
PB_TX1_P PB_TX1_N
PB_TX0_P PB_TX0_N
PB_RX0_P PB_RX0_N
PB_DPSRC_AUX_P PB_DPSRC_AUX_N
PB_USB2_D_P PB_USB2_D_N
PB_LSTX PB_LSRX PB_DPSRC_HPD
PB_USB2_RBIAS R44 499/F_4

POC
POC

DEBUG
THERMDA THERMDA
PCIE_ATEST
TEST_EDM
FUSE_VQPS_64 FUSE_VQPS_128
MONDC_CIO_0 MONDC_CIO_1
MONDC_SVR
ATEST_P ATEST_N
USB2_ATEST
MONDC_DPSNK_0
MONDC_DPSNK_1
MONDC_DPSRC
U10A AR_4C

DEBUG PINs:

| PIN | TERMINATION |
|---|---|
| MONDC_SVR | GND |
| MONDC_DPSNK_0 | GND |
| MONDC_DPSNK_1 | GND |
| MONDC_DPSRC | GND |
| MONDC_CIO_0 | GND |
| MONDC_CIO_1 | GND |
| TEST_EDM | GND |
| FUSE_VQPS_64 | GND |
| FUSE_VQPS_128 | GND |
| ATEST_P/N | FLOATING |
| USB2_ATEST | FLOATING |
| PCIE_ATEST | FLOATING |

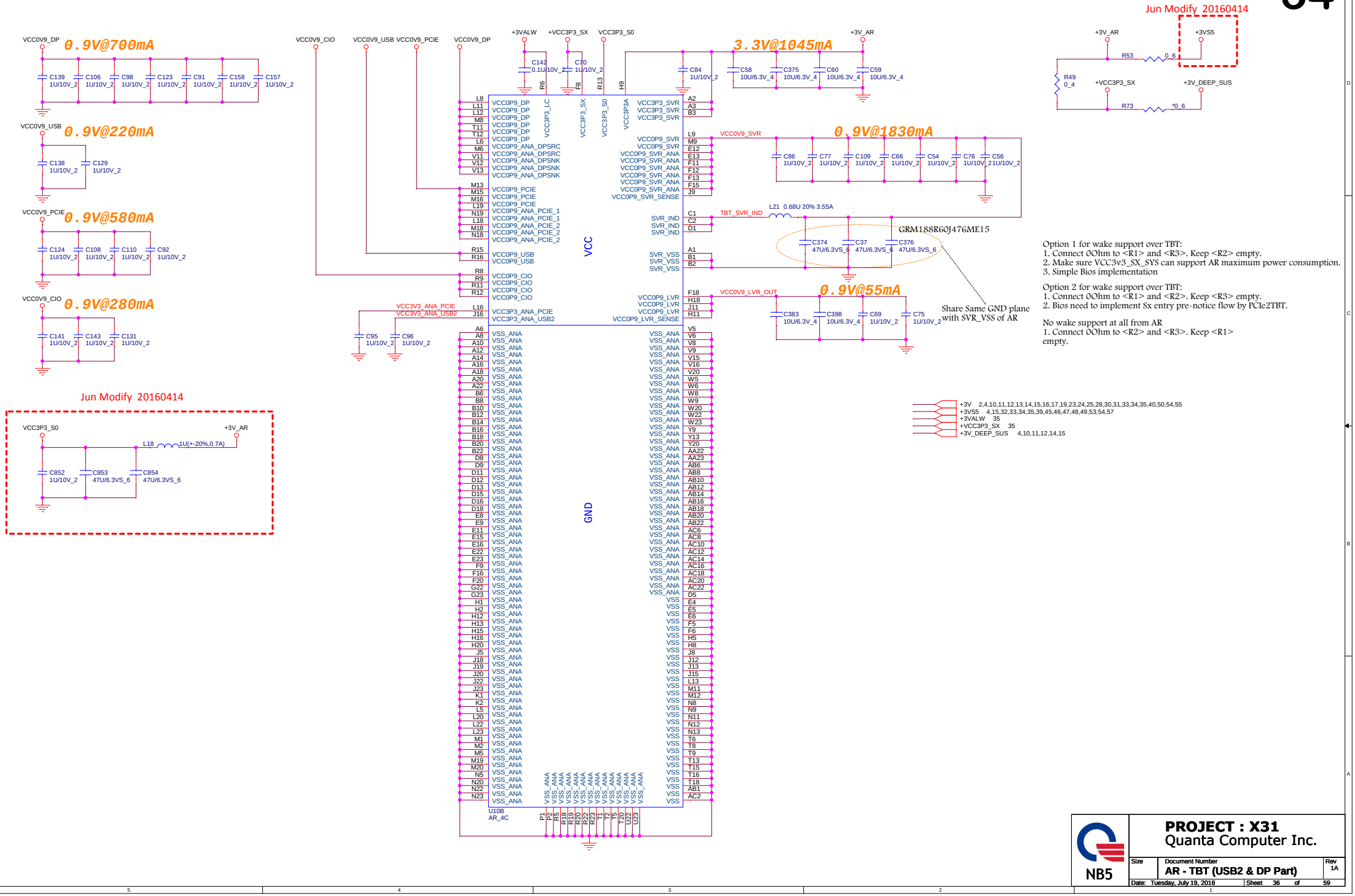
+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,40,50,54,55
+3VS5 4,15,32,33,34,36,39,45,46,47,48,49,53,54,57
+3VALW 36
+VCC3P3_SX 36
VCC3V3_FLASH 37

JTAG
+3VALW
TBT_TDI R110 10K/F_2
TBT_TMS R102 10K/F_2
TBT_TCK R97 10K/F_2
TBT_TDO R109 10K/F_2

NB5

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | AR - TBT (USB2 & DP Part) | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 35 of 59 | |



# Port A Controller - ACE

TPS65982 (ACE) -
USB3.1 PD

0318 Del R414 R413

PP_EXT circuit

W = 200 mils

W = 120 mils

Supporting up to 60W to VBUS
ACE configuration:
* SENSEP & SENSEN should be connected to 10mOhm resistor
* PP_HV should be tied to GND.

0330 Del R409

0330

I2C_ADDR
'0' - Sets ACE as Primary
'1' - Sets ACE as Secondary

I2C1
Connect to AR and PD2

I2C2
Directly to EC

FOR EMI

0512 SI SWAP TBTA_SENN/P

20160705 Modify PD PN to AJ659820T02

Primary

Type-C USB1 Top

Type-C USB1 Bot

Tie RPD_Gn to C_CCn pins to support no-power or dead-battery modes

Jun Modify 20160414

Dual Power Role:
BUSPOWERZ < 0.8v --> Receiving VBUS Power through the PP_EXT path (Host Charging mode from USBC)
BUSPOWERZ > 2.4v --> Disabling system power from VBUS (Host providing power to the USBC)

0525 SI R427 change to 15K 0.1% 0402

0201 Change Footprint

To Policy Manager or PCH

To Policy Manager

NOTE:
GPIO MAPPING SUBJECT TO CHANGES BASED ON VENDOR REQURIEMETNS. PLEASE REFER TO DATASHEET FOR MORE DETAILS.

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | AR - TBT (USB2 & DP Part) | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 37 of 59 | |

NB5

# Port B Controller - ACE

TPS65982 (ACE) - USB3.1
PD

PP_EXT
circuit

Supporting up to 60W to VBUS
ACE configuration:
* SENSEP & SENSEN should be
connected to 10mOhm resistor
* PP_HV should be tied to GND.

W = 120 mils

W = 200 mils

20160705 Modify PD PN to AJ659820T02

I2C_ADDR
'0' - Sets ACE as Primary
'1' - Sets ACE as
Secondary

I2C2
Directly to EC

Secondary

Type-C USB1 Top

Type-C USB1 Bot

Tie RPD_Gn to C_CCn pins
to support no-power or
dead-battery modes

4/11 ADD pull high & pull down for TI request

4/11change to 1M

0525 SI R761 change to 15K 0.1% 0402

Dual Power Role:
BUSPOWERZ < 0.8v --> Receiving VBUS
Power through the PP_EXT path (Host
Charging mode from USBC)
BUSPOWERZ > 2.4v --> Disabling system
power from VBUS (Host providing power
to the USBC)

8Mbit Flash (Only for ACE)

Winbond : AKE3GF00N00

SPI/EE: AR to/from NVM
& ACE

Silk: "NVM"

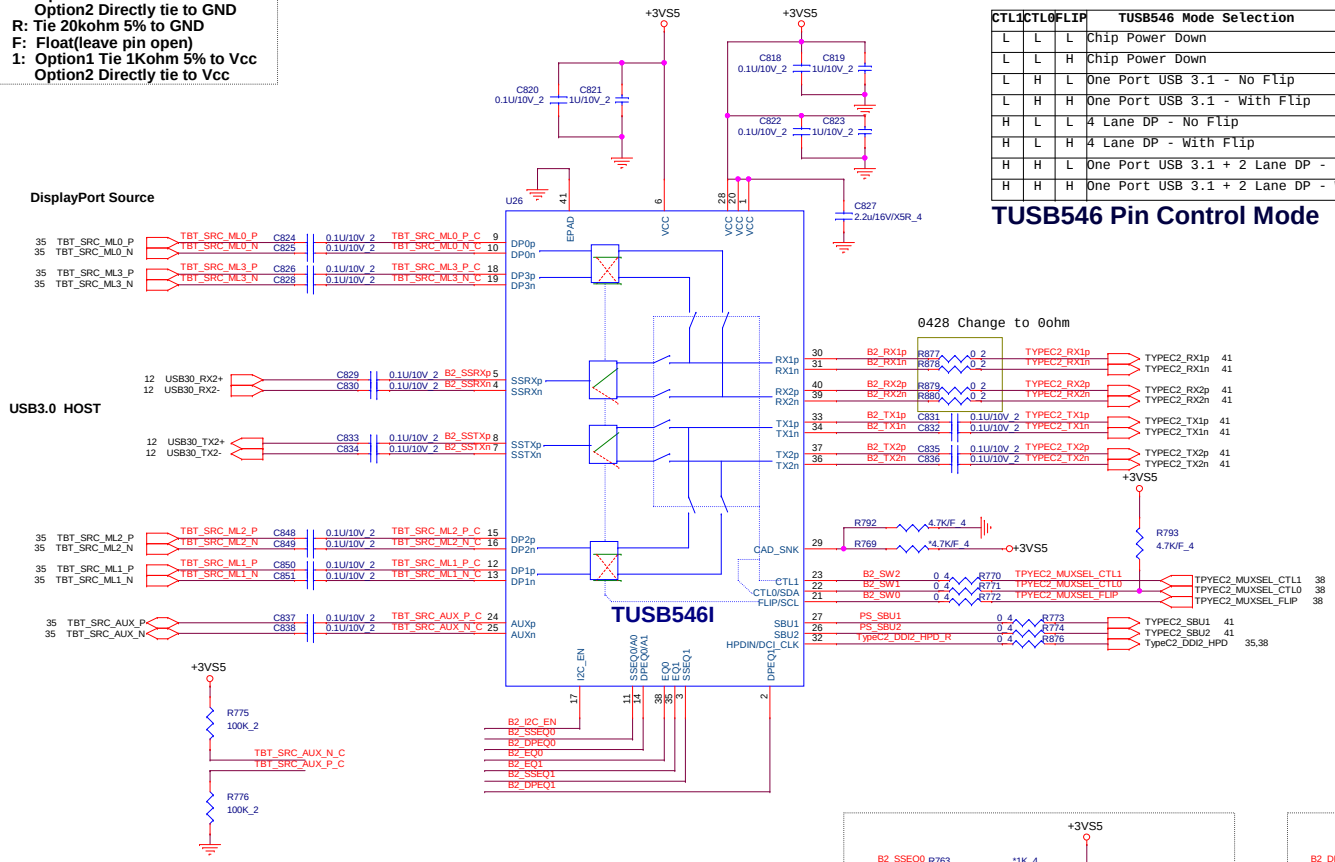
NOTE:
GPIO MAPPING SUBJECT TO
CHANGES BASED ON VENDOR
REQURIEMETNS. PLEASE REFER TO
DATASHEET FOR MORE DETAILS.

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | AR - TBT (USB2 & DP Part) | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 38 of 59 | |

NB5

**4 Level Input:**
- **L: Option1 Tie 1Kohm 5% to GND**
  **Option2 Directly tie to GND**
- **R: Tie 20kohm 5% to GND**
- **F: Float(leave pin open)**
- **1: Option1 Tie 1Kohm 5% to Vcc**
  **Option2 Directly tie to Vcc**




| CTL1 | CTL0 | FLIP | TUSB546 Mode Selection |
|---|---|---|---|
| L | L | L | Chip Power Down |
| L | L | H | Chip Power Down |
| L | H | L | One Port USB 3.1 - No Flip |
| L | H | H | One Port USB 3.1 - With Flip |
| H | L | L | 4 Lane DP - No Flip |
| H | L | H | 4 Lane DP - With Flip |
| H | H | L | One Port USB 3.1 + 2 Lane DP - No Flip |
| H | H | H | One Port USB 3.1 + 2 Lane DP - With Flip |

## TUSB546 Pin Control Mode

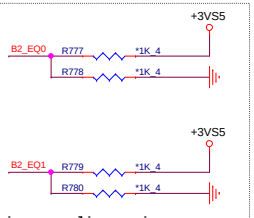
| CTL1 | FLIP | AUX Select |
|---|---|---|
| H | L | AUXP->SBU1,AUXN->SBU2 |
| H | H | AUXP->SBU2,AUXN->SBU1 |
| L>2ms | X | One Port USB 3.1 - No Flip |

## AUX Pin Control Mode

**Table 8-7 TUSB546 Receiver Equalization GPIO Control**

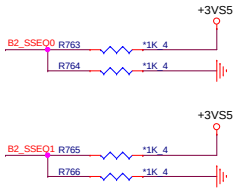
| USB3.1 Downstream Facing Ports | | | USB 3.1 Upstream Facing Port | | | All DisplayPort Lanes | | |
|---|---|---|---|---|---|---|---|---|
| EQ1 pin Level | EQ0 pin Level | EQ GAIN @2.5GHz (dB) | SSEQ1 pin Level | SSEQ0 pin Level | EQ GAIN @2.5GHz (dB) | DPEQ1 pin Level | DPEQ0 pin Level | EQ GAIN @2.5GHz (dB) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | R | 1 | 0 | R | 1 | 0 | R | 1 |
| 0 | F | 2 | 0 | F | 2 | 0 | F | 2 |
| 0 | 1 | 3 | 0 | 1 | 3 | 0 | 1 | 3 |
| R | 0 | 4 | R | 0 | 4 | R | 0 | 4 |
| R | R | 5 | R | R | 5 | R | R | 5 |
| R | F | 6 | R | F | 6 | R | F | 6 |
| R | 1 | 7 | R | 1 | 7 | R | 1 | 7 |
| F | 0 | 8 | F | 0 | 8 | F | 0 | 8 |
| F | R | 9 | F | R | 9 | F | R | 9 |
| F | F | 10 | F | F | 10 | F | F | 10 |
| F | 1 | 11 | F | 1 | 11 | F | 1 | 11 |
| 1 | 0 | 12 | 1 | 0 | 12 | 1 | 0 | 12 |
| 1 | R | 13 | 1 | R | 13 | 1 | R | 13 |
| 1 | F | 14 | 1 | F | 14 | 1 | F | 14 |
| 1 | 1 | 15 | 1 | 1 | 15 | 1 | 1 | 15 |



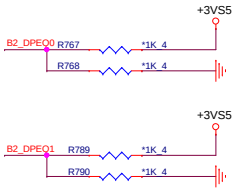



**EQ0,EQ1 : USB receiver equalizer gain for downstream facing RX1 & RX2**
**F,F(Default)**


**I2C Programming or pin strap programming select.**
**I2C is only disable when this pin is '0'**
**0 : Pin Strap(I2C disable)(Default)**
**R : TI test mode(I2C enable at 3.3V)**
**F : I2C enabled at 1.8V**
**1 : I2C enabled at 3.3V**




**SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N**
**F,F(Default)**
**When I2C_EN is not '0' SSEQ0 sets I2C adress**



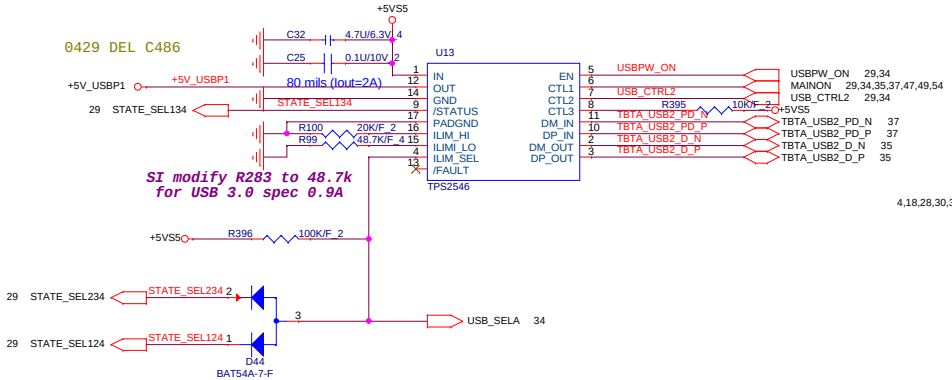

**DPEQ0,DPEQ1 : DP Receiver equalization gain**
**F,F(Default)**
**When I2C_EN is not '0' DPEQ0 sets I2C adress**

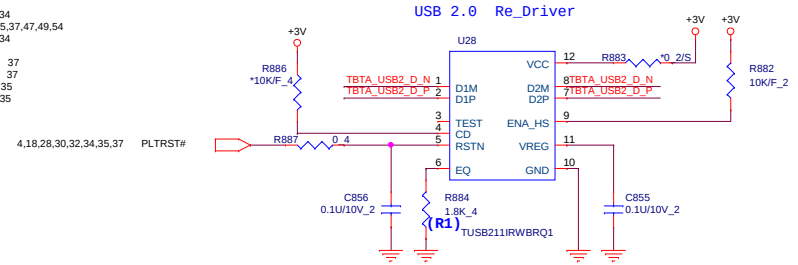
**PROJECT :Hydra**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | TUSB546 | A |
| Date: Tuesday, July 19, 2016 | Sheet 39of 59 | |

# PortA Support BC1.2



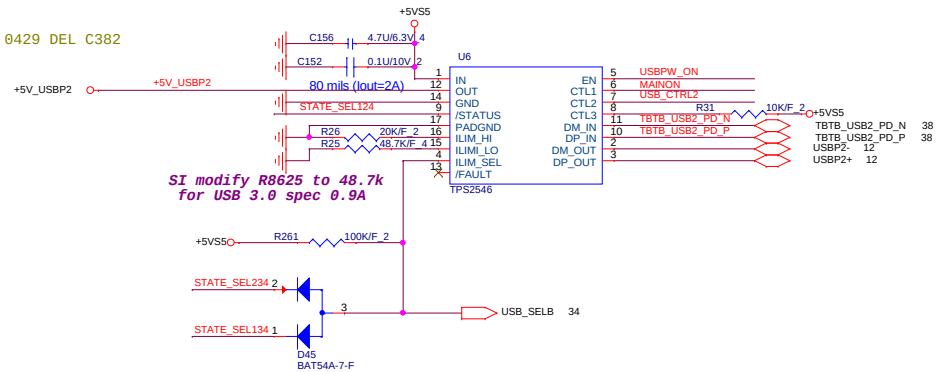



| EQ gain R1 setting | |
|---|---|
| L0 | 100 5% |
| L1 | 1.8K 5% |
| L2 | 3.9K 1% |
| L3 | 9.1K 5% |

+5VS5 4,25,26,29,37,38,46,47,48,49,50,51,52,54,55,56,57
+5V_USBP1 37
+5V_USBP2 38
TBTB_VBUS_L 37,38,41

# PortB Support BC1.2




NB5

**PROJECT : X31**
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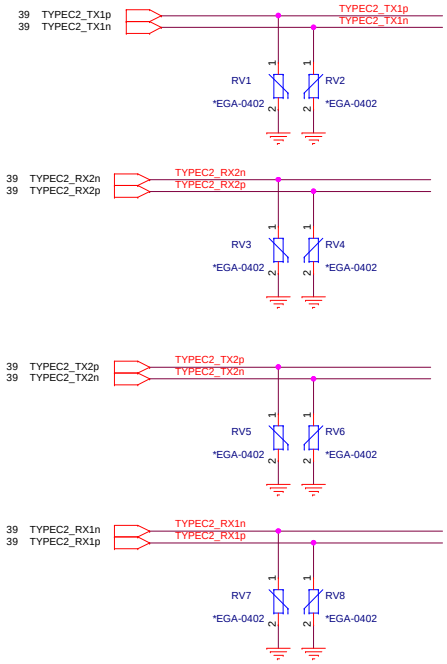
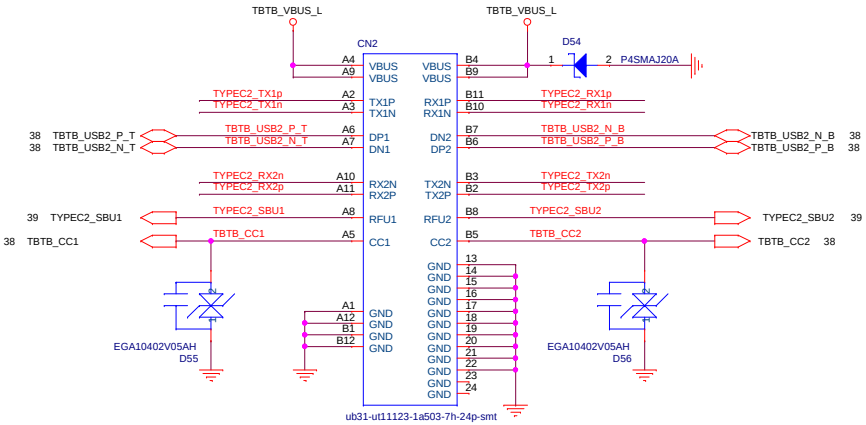
| Size | Document Number | Rev |
|---|---|---|
| | AR - TBT (USB2 & DP Part) | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 40 of 59 | |

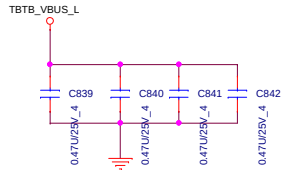
## Type C2_HSIO_ ESD

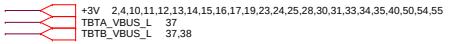



## USB Type-C Port B

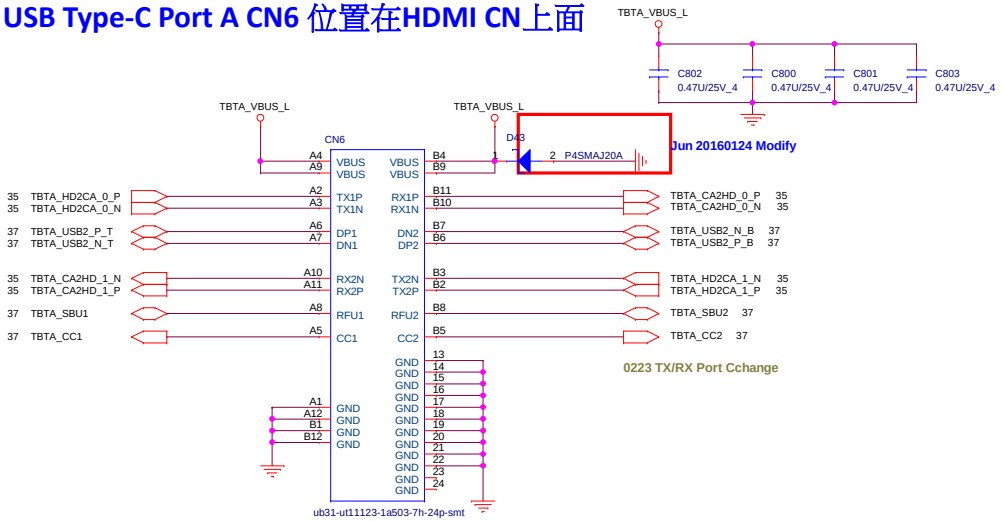



0603 update FP as ub31-ut11123-1a503-7h-24p-smt




## USB Type-C Port A CN6 位置在HDMI CN上面

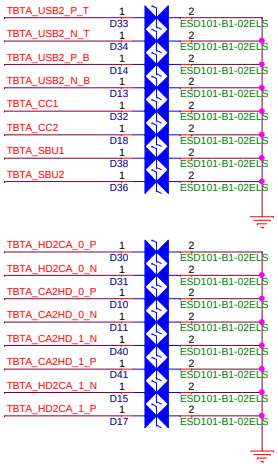



0223 TX/RX Port Cchange

0603 update FP as ub31-ut11123-1a503-7h-24p-smt

0604 update PN as BC0101B1Z01

0503 update FP as d-0_62x0_32-0_32h

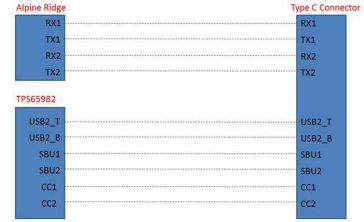


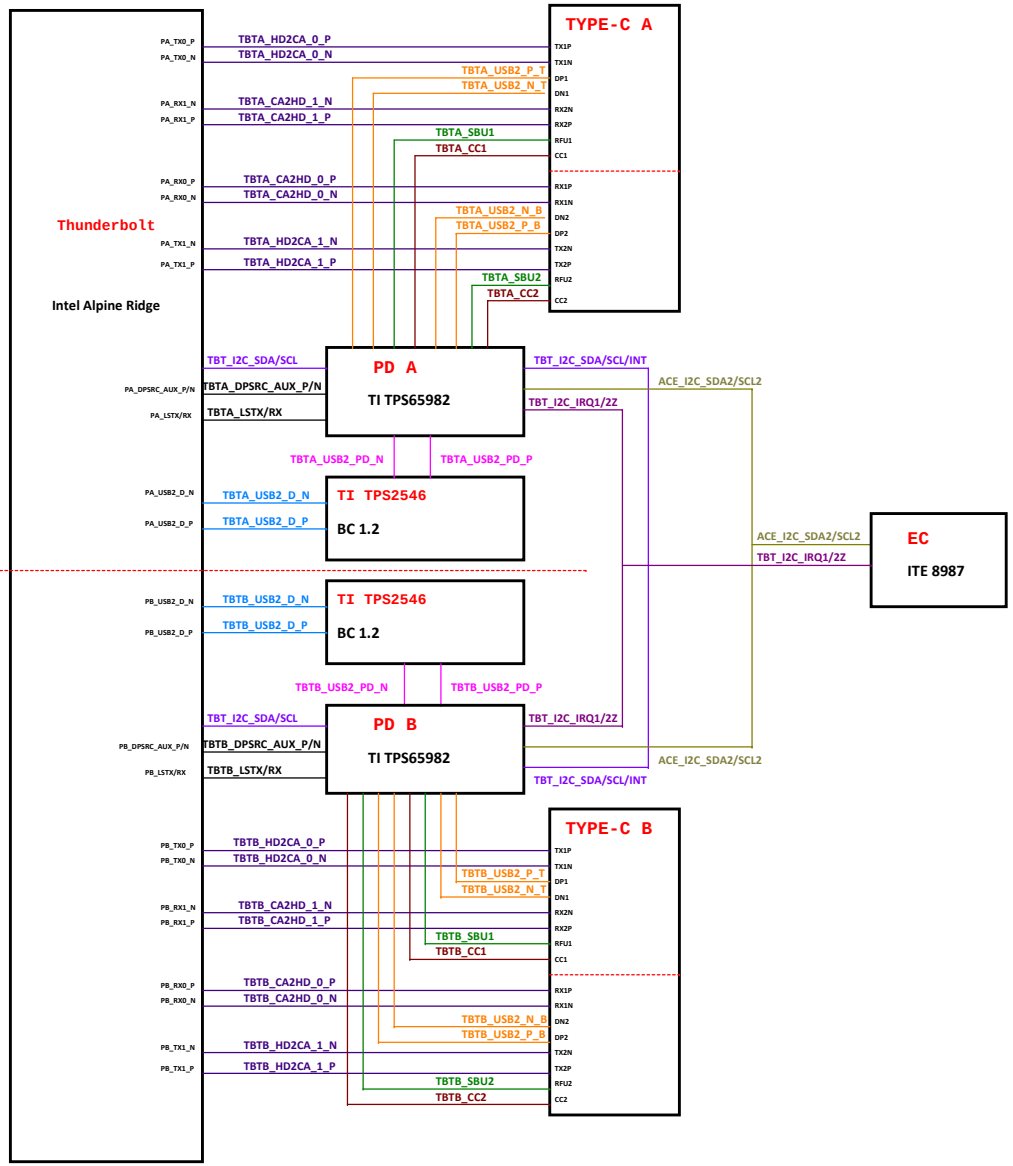

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | AR - TBT (USB2 & DP Part) | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 41 of 59 | |

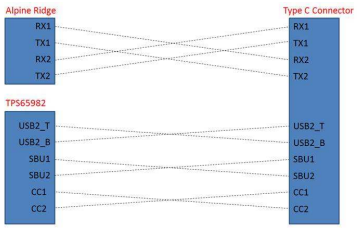
NB5

## Keep the same Typc-C CN as the same as Intel AR CRB Board

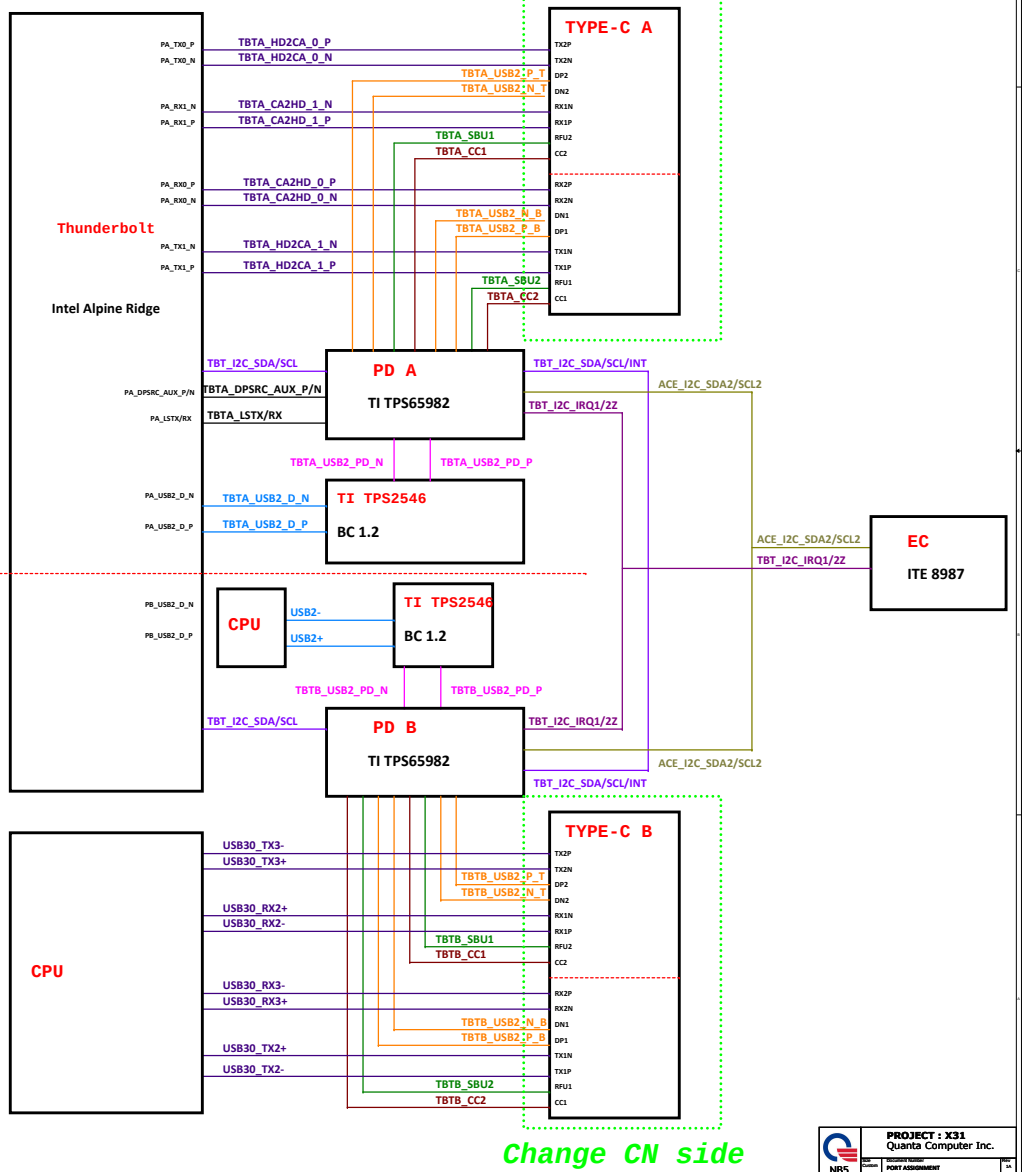



## Change CIO connection in Type-C Connector side




Change CN side




Change CN side

PROJECT : X31
Quanta Computer Inc.
PONT ASSIGNMENT

## Dead Battery Block

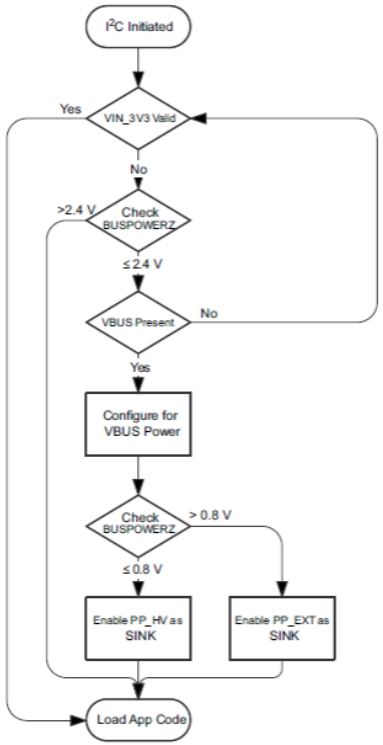



Figure 65. Dead-Battery Condition Flow Diagram

## USB Type-C Connector – Pinout and Alignment

Receptacle (Front View)

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1− | VBUS | CC1 | D+ | D− | SBU1 | VBUS | RX2− | RX2+ | GND |
| GND | RX1+ | RX1− | VBUS | SBU2 | D− | D+ | CC2 | VBUS | TX2− | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |

USB3.0 USB2.0 USB3.0

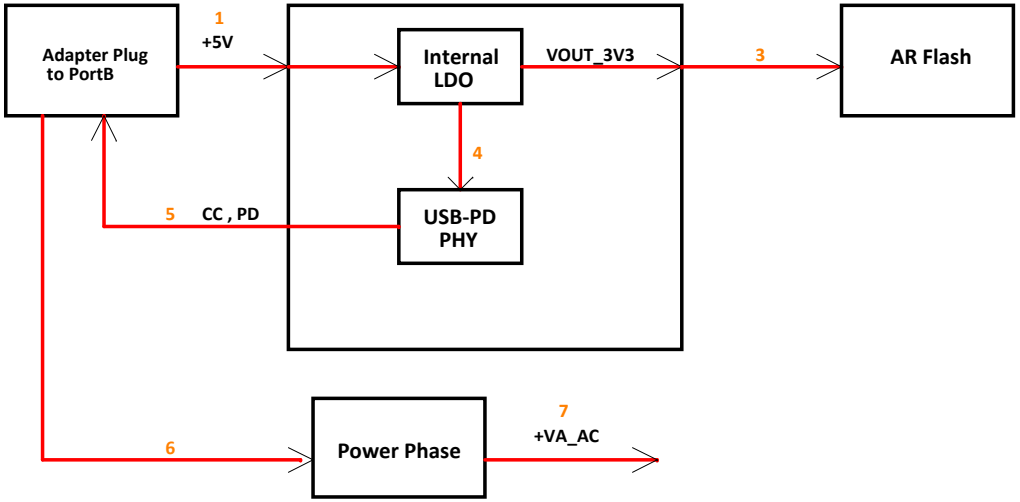
Normal Plug

Reverse Plug

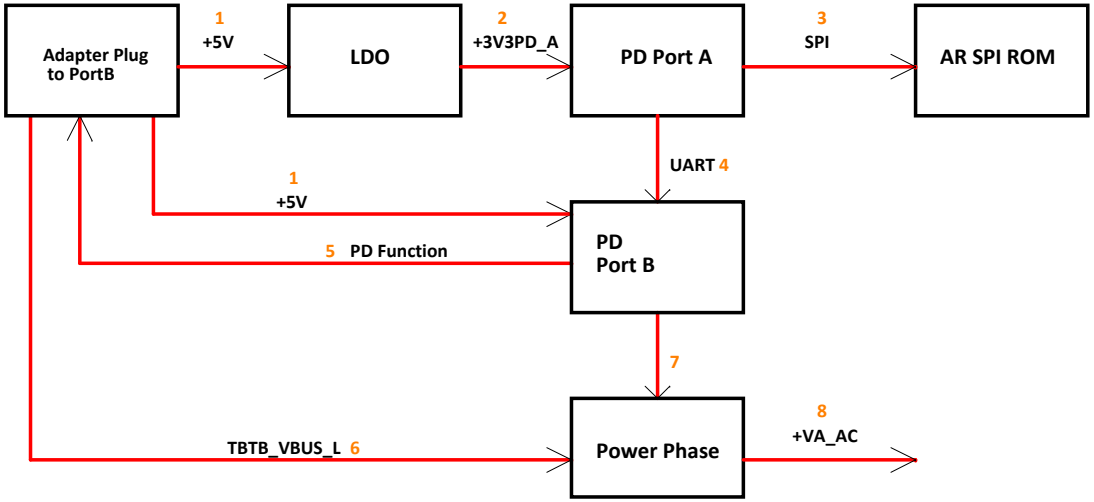
| A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | RX2+ | RX2− | VBUS | SBU1 | D− | D+ | CC | VBUS | TX1− | TX1+ | GND |
| GND | TX2+ | TX2− | VBUS | VCONN | | | SBU2 | VBUS | RX1− | RX1+ | GND |
| B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | B11 | B12 |

## PortA Dead Battery

TI PD TPS65982 Port A

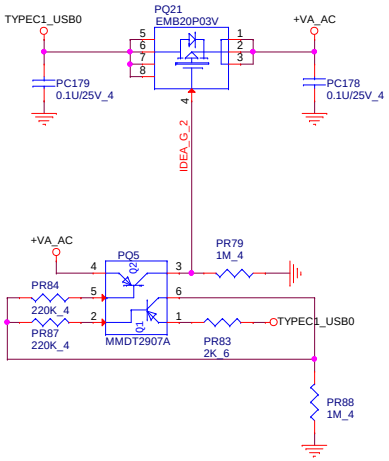


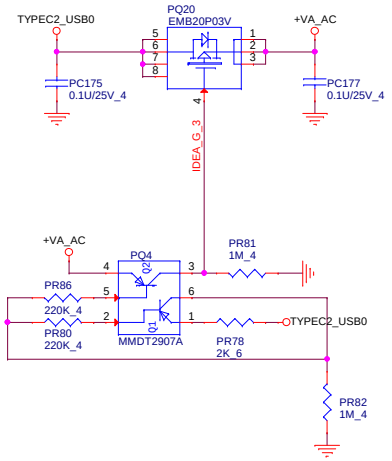

## PortB Dead Battery




| | | |
|---|---|---|
| NB5 | PROJECT : X31<br>Quanta Computer Inc. | |
| | Size: Custom<br>Document Number: Load switch IC | Rev |
| | Date: Tuesday, July 19, 2016 | Sheet 43 of 59 |

+VA_AC 45,59
TYPEC1_USB0 37
TYPEC2_USB0 38

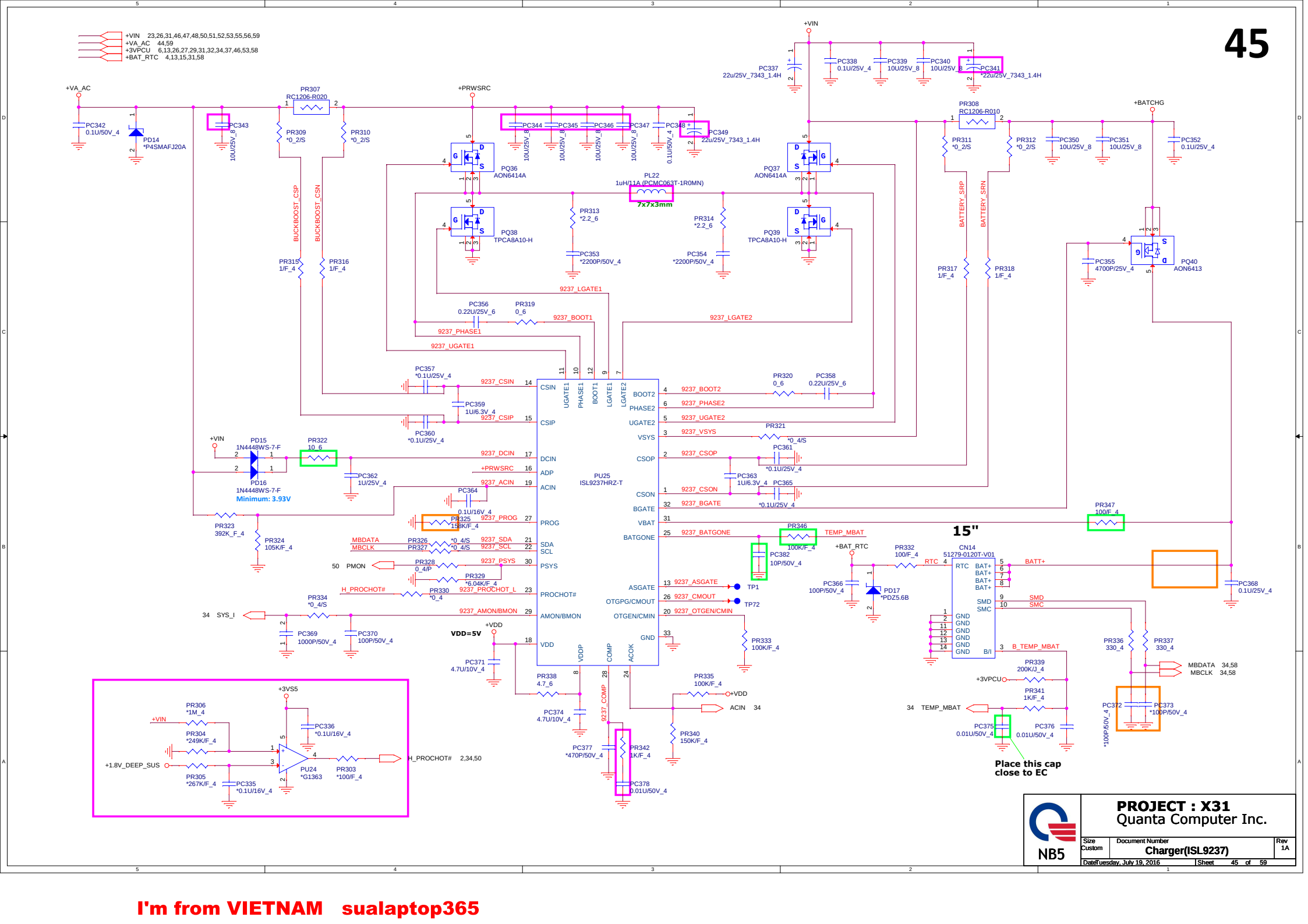



NB5

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | TYPE C S/W | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 44 of 59 | |


45
+VIN 23,26,31,46,47,48,50,51,52,53,55,56,59
+VA_AC 44,59
+3VPCU 6,13,26,27,29,31,32,34,37,46,53,58
+BAT_RTC 4,13,15,31,58
PU25 ISL9237HRZ-T
PQ36 AON6414A
PQ37 AON6414A
PQ38 TPCA8A10-H
PQ39 TPCA8A10-H
PQ40 AON6413
PL22 1uH/11A (PCMC063T-1R0MN)
7x7x3mm
9237_LGATE1
9237_BOOT1
9237_PHASE1
9237_UGATE1
9237_LGATE2
9237_BOOT2
9237_PHASE2
9237_UGATE2
9237_VSYS
9237_CSOP
9237_CSON
9237_BGATE
9237_BATGONE
9237_CSIN
9237_CSIP
9237_DCIN
9237_ACIN
9237_PROG
9237_SDA
9237_SCL
9237_PSYS
9237_PROCHOT_L
9237_AMON/BMON
9237_ASGATE
9237_CMOUT
9237_OTGEN/CMIN
9237_COMP
BUCKBOOST_CSP
BUCKBOOST_CSN
BATTERY_SRP
BATTERY_SRN
MBDATA
MBCLK
SYS_I
PMON
H_PROCHOT#
ACIN
TEMP_MBAT
B_TEMP_MBAT
VDD=5V
Minimum: 3.93V
15"
Place this cap close to EC
PROJECT : X31
Quanta Computer Inc.
NB5
Charger(ISL9237)
Tuesday, July 19, 2016
Sheet 45 of 59
I'm from VIETNAM sualaptop365

# DC/DC +3VS5/+5VS5



+VIN 23,26,31,45,47,48,50,51,52,53,55,56,59
+3VS5 4,15,32,33,34,35,36,39,45,47,48,49,53,54,57
+5VS5 4,25,26,29,37,38,40,47,48,49,50,51,52,54,55,56,57
+3VPCU 6,13,26,27,29,31,32,34,37,45,53,58
+5VPCU 25,26,54,57

Do Not add test pad on VCC & LDO pin

PU15 SY8286BRAC

+3.3 Volt +/- 5%
TDC:6A
EDP:8A

Ven_th>0.8V

7x7x3mm

PU26 G9090-180T11U

PU18 SY8286CRAC

+5 Volt +/- 5%
TDC:6A
EDP:8A

Reserve for USB Charge

| USB Charge Support | Ra | Rb |
|---|---|---|
| No support | Stuff | NA |
| Support | NA | Stuff |

Do Not add test pad on VCC & LDO pin

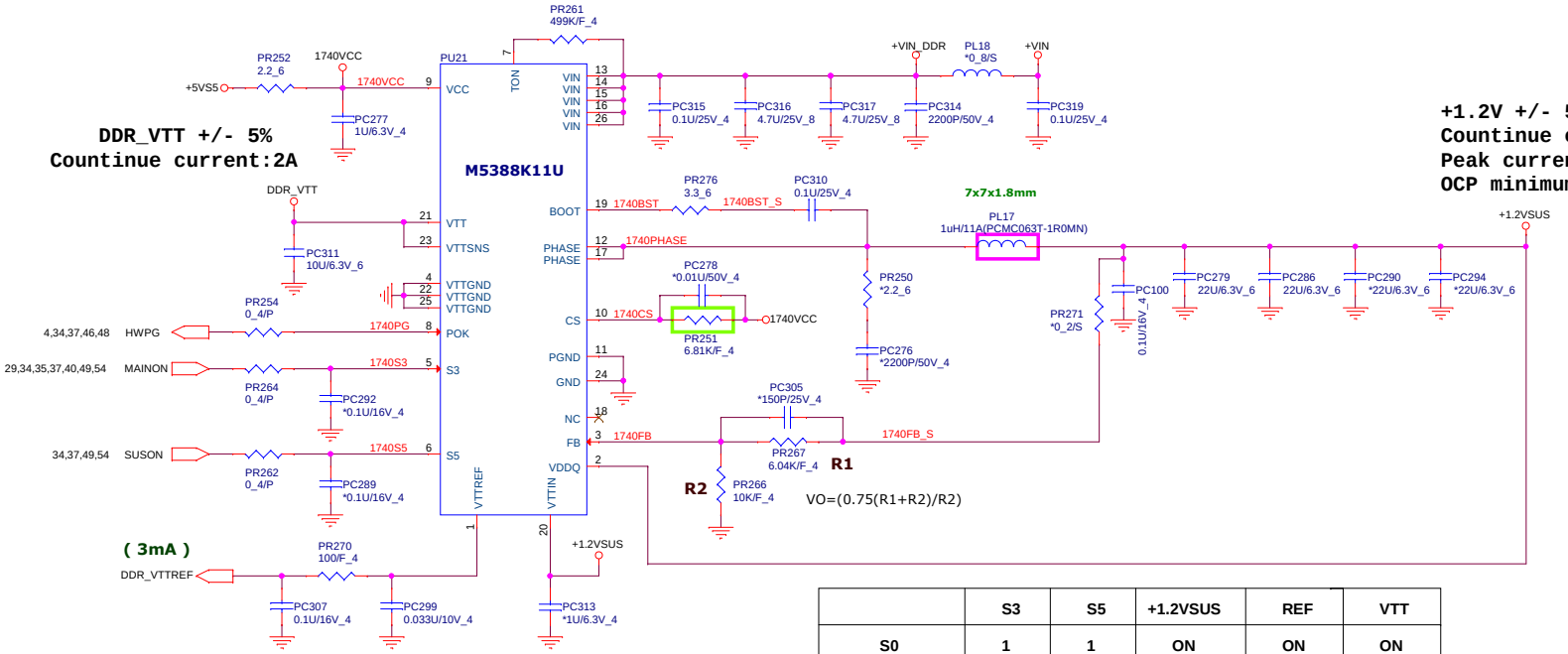
NB5

PROJECT : X31
Quanta Computer Inc.

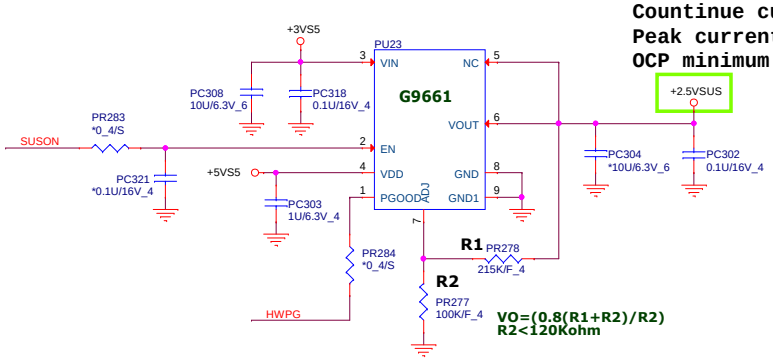
Size Custom | Document Number 3/5VPCU(RT8243A) | Rev 1A

Date Tuesday, July 19, 2016 | Sheet 46 of 59

+VIN 23,26,31,45,46,48,50,51,52,53,55,56,59
+3VS5 4,15,32,33,34,35,36,39,45,46,48,49,53,54,57
+5VS5 4,25,26,29,37,38,40,46,48,49,50,51,52,54,55,56,57
+1.2VSUS 3,6,16,17,24,49,57,59
DDR_VTT 16,17
+2.5VSUS 16,17



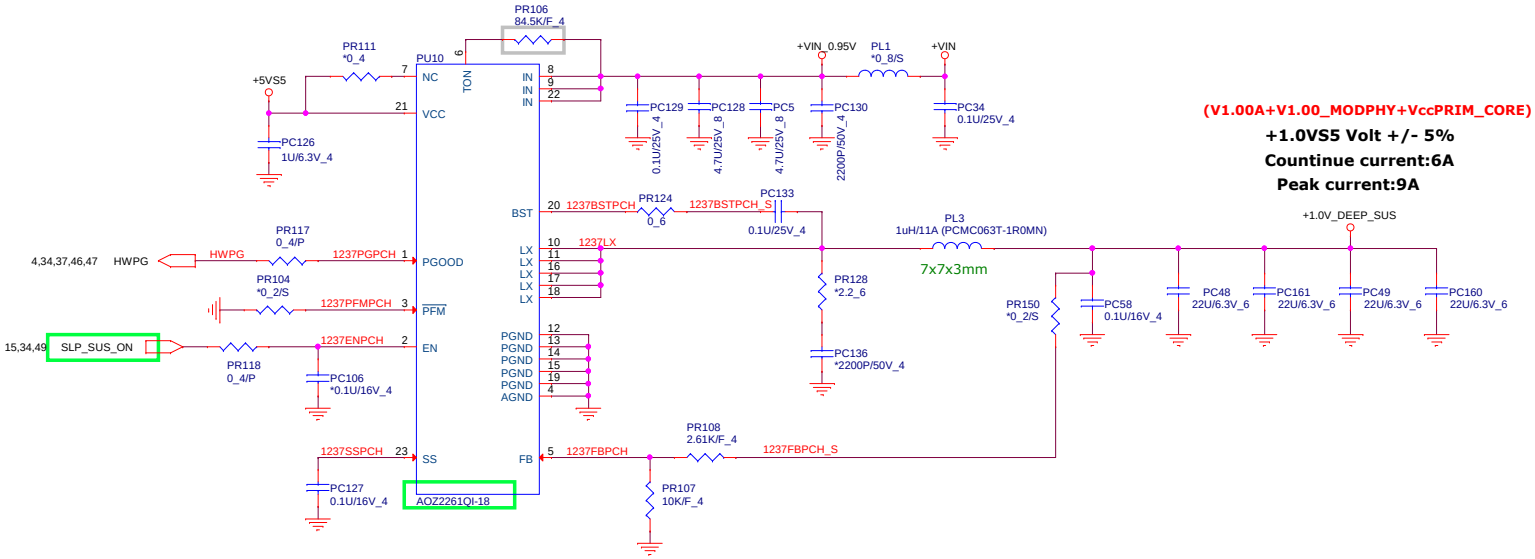

| | S3 | S5 | +1.2VSUS | REF | VTT |
|---|---|---|---|---|---|
| S0 | 1 | 1 | ON | ON | ON |
| S3 (mainon off) | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |



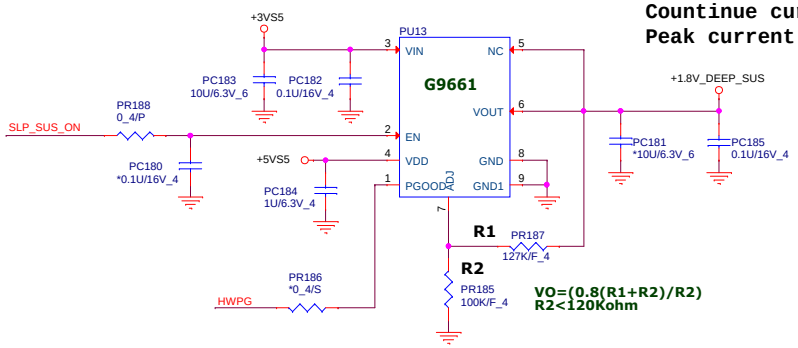

+2.5VSUS +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum:3A

| | | |
|---|---|---|
| PROJECT : X31 | | |
| Quanta Computer Inc. | | |
| NB5 | Size | Document Number: DDR3 (RT8231B)/2.5VSUS Rev: 1A |
| Tuesday, June 28, 2016 | Date: | Sheet 47 of 59 |

+VIN 23,26,31,45,46,47,50,51,52,53,55,56,59
+3VS5 4,15,32,33,34,35,36,39,45,46,47,49,53,54,57
+5VS5 4,25,26,29,37,38,40,46,47,49,50,51,52,54,55,56,57
+1.0V_DEEP_SUS 9,13,15,49
+1.8V_DEEP_SUS 9,15,45,54




**+1.8V_DEEP_SUS +/- 5%**
**Countinue current:1.0A**
**Peak current:3A**

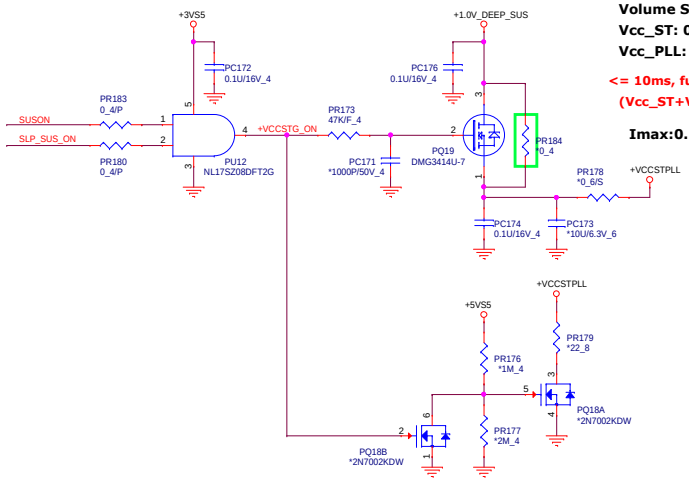



NB5

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | +1.1VS5 (RT8228)/2.5V | 1A |
| Date: Tuesday, July 19, 2016 | Sheet 48 of 59 | |

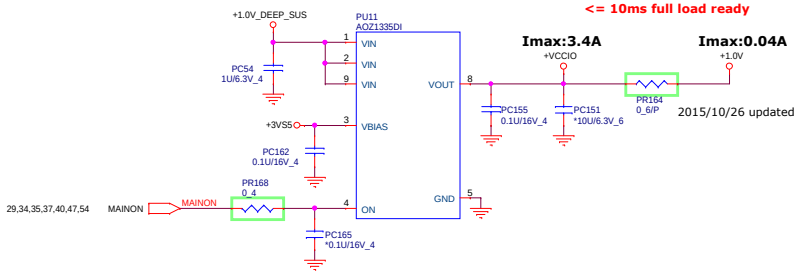
+1.0V 2,4,6,34
+3VS5 4,15,32,33,34,35,36,39,45,46,47,48,53,54,57
+5VS5 4,25,26,29,37,38,40,46,47,48,50,51,52,54,55,56,57
+VCCIO 2,6
+1.2VSUS 3,6,16,17,24,47,57,59
+VCCSTPLL 2,5,6,9,50
+1.0V_DEEP_SUS 9,13,15,48
+1.2V_VCCPLL_OC 6




**Volume Segment**
**Vcc_ST: 0.12A**
**Vcc_PLL: 0.12A**

**<= 10ms, full load ready**
**(Vcc_ST+Vcc_PLL)**

**Imax:0.24A**

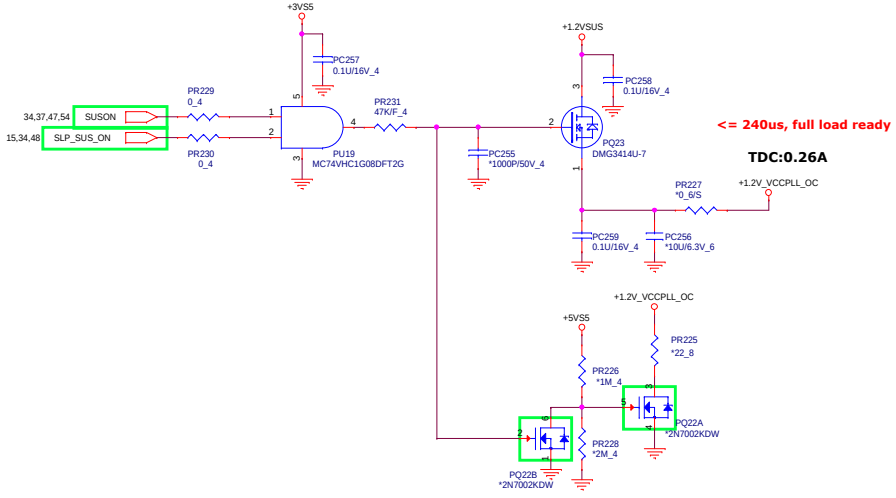



**Volume Segment**
**Vcc_STG: 0.04A**
**Vcc_IO: 3.4A**

**<= 10ms full load ready**

**Imax:3.4A** **Imax:0.04A**

2015/10/26 updated




**<= 240us, full load ready**

**TDC:0.26A**



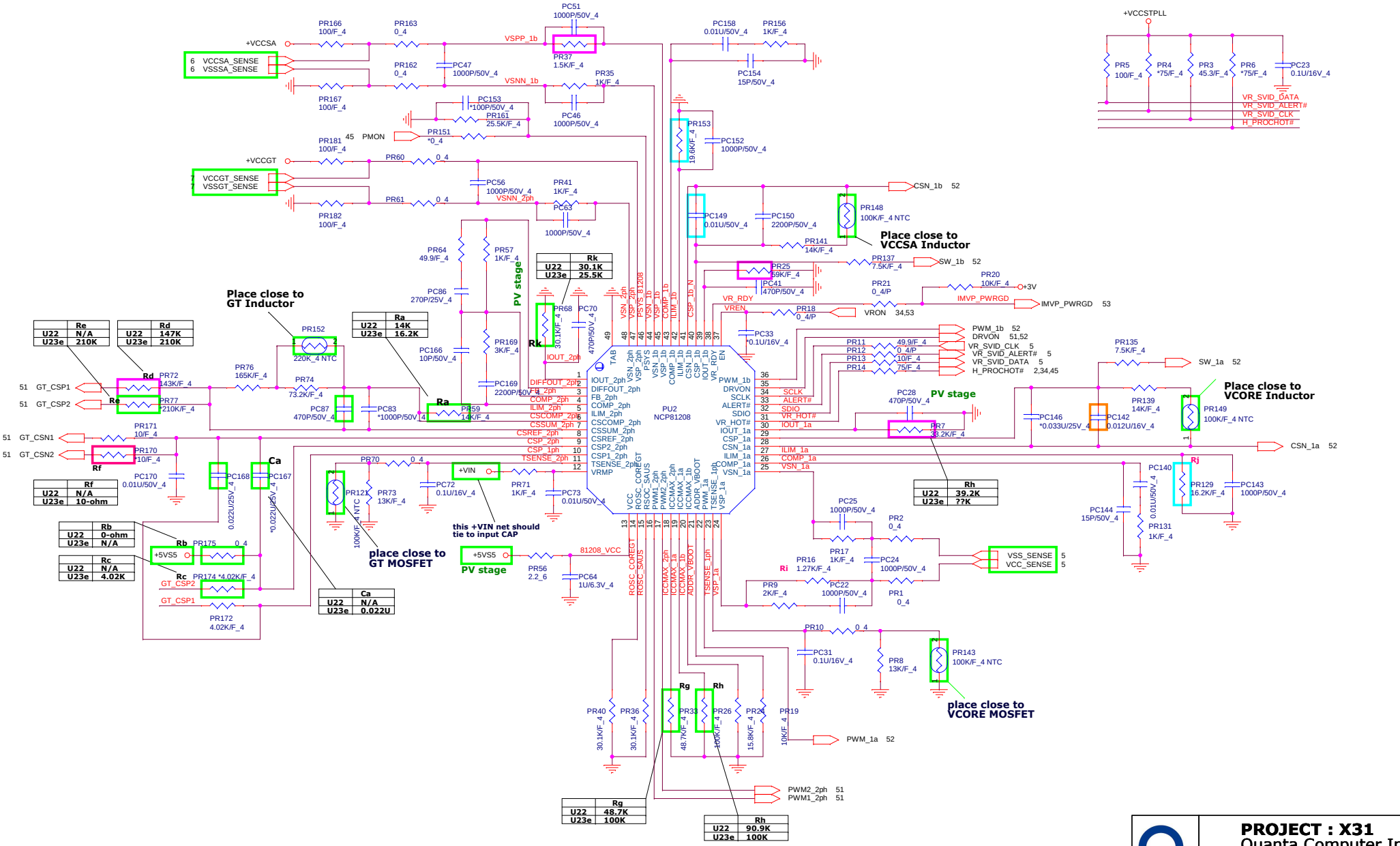
**PROJECT : X31**
Quanta Computer Inc.

NB5

| Size | Document Number | Rev |
|---|---|---|
| C | +1.0V/+VCCSTPLL | 1A |

Date: Tuesday, July 19, 2016 Sheet 49 of 59

+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,54,55
+5V 24,25,28,31,54
+VIN 23,26,31,45,46,47,48,51,52,53,55,56,59
+5VPCU 25,26,46,54,57
+VCCSA 6,52
+VCCGT 7,51
+VCCSTPLL 2,5,6,9,49

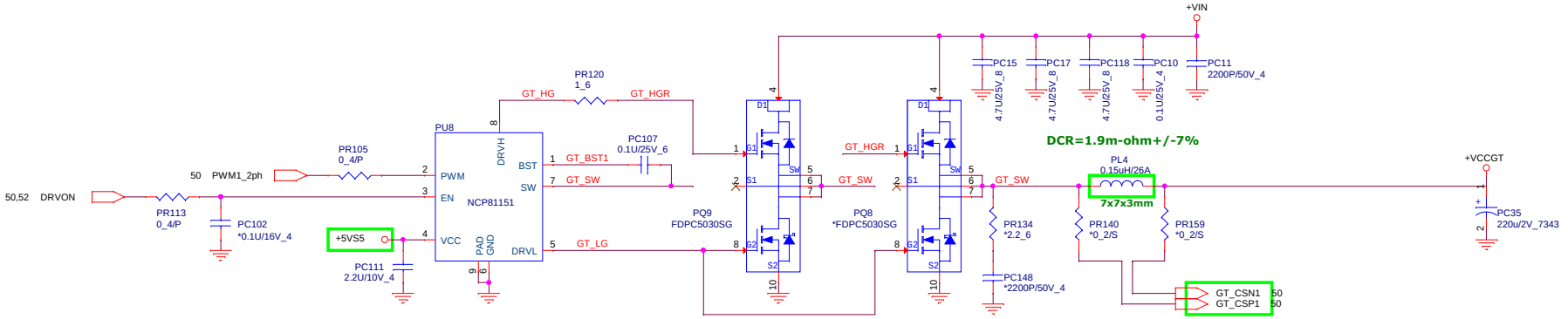


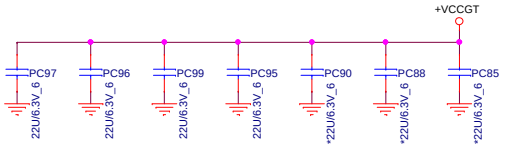

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CPU VR IC (NCP81206) | 2A |
| Date: Tuesday, July 19, 2016 | Sheet 50 of 59 | |

NB5

+VIN 23,26,31,45,46,47,48,50,52,53,55,56,59
+5VS5 4,25,26,29,37,38,40,46,47,48,49,50,52,54,55,56,57
+VCCGT 7,50




**H/W side output CAP list**

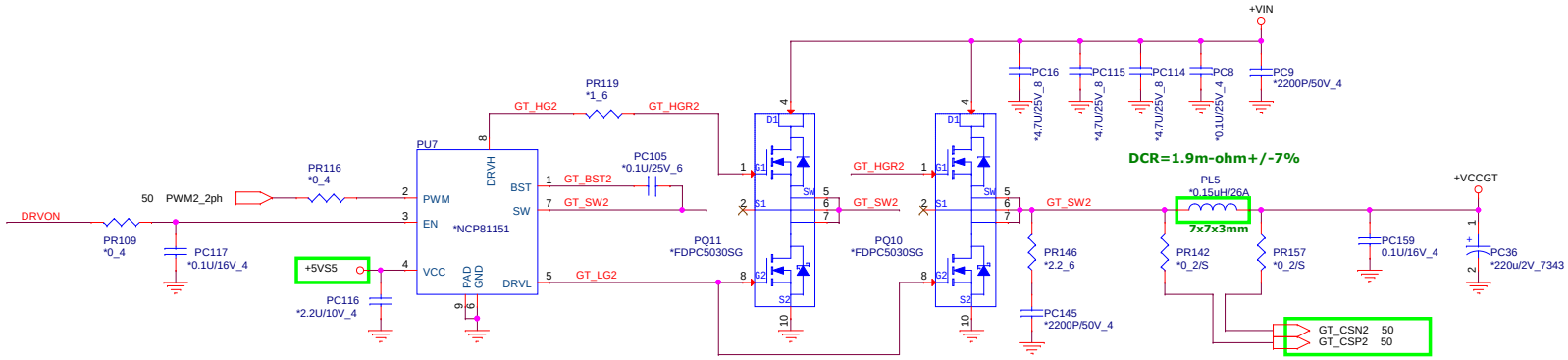
- 47U/6.3V_0805 X 6
- 22U/6.3V_0603 X 12 (GTX+5)
- 10U/6.3V_0402 X 10
- 1U/6.3V_0402 X 12

**+VCC_GT**

**U-line 22 (15W)**
**TDC:18A(22)**
**Icc max:31A(22)**
**L/L=3.1mV/A**

**U-line 23e(28W)**
**TDC:35A(23e)**
**Icc max =64A(GT+GTx)**
**L/L=2mV/A**

**For U23e --> Add These Components**

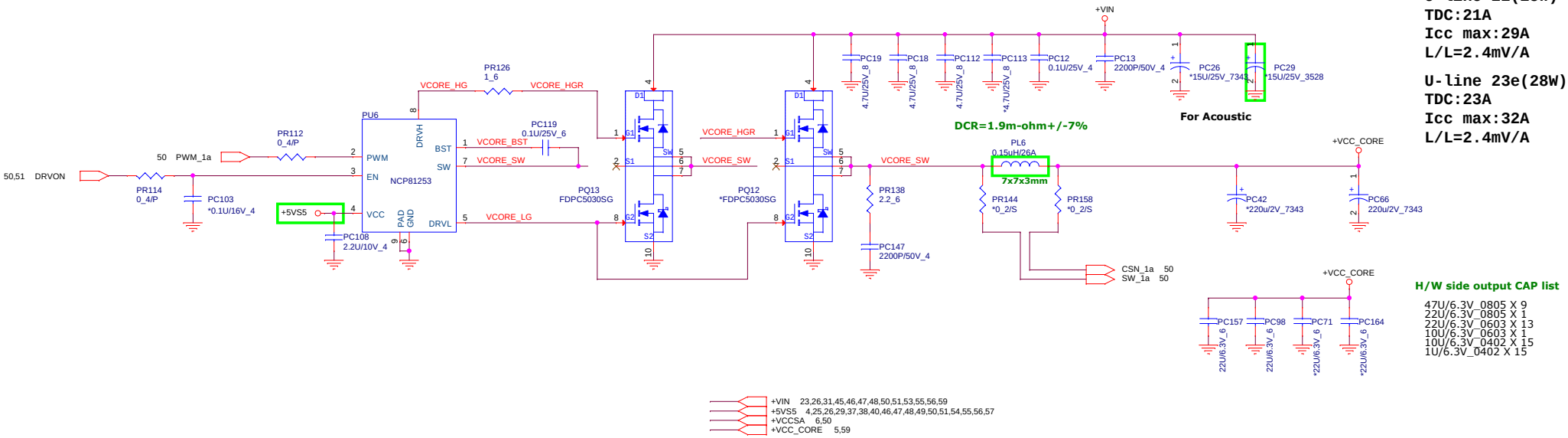



NB5

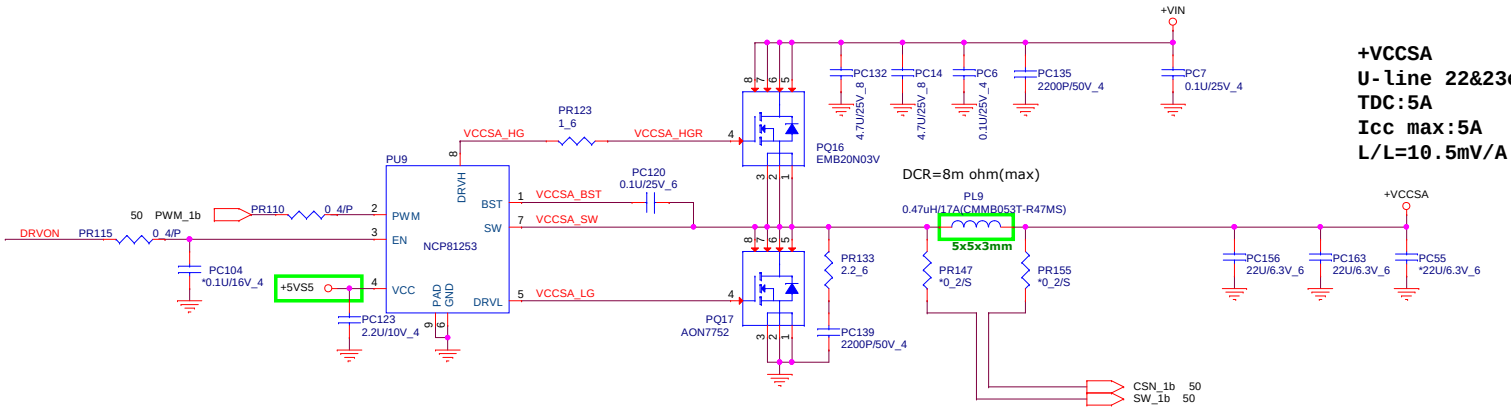
**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | +VCCSA (NCP81253) | 2A |
| Date: Tuesday, July 19, 2016 | Sheet 51 of 59 | |

# CPU CORE




# VCCSA

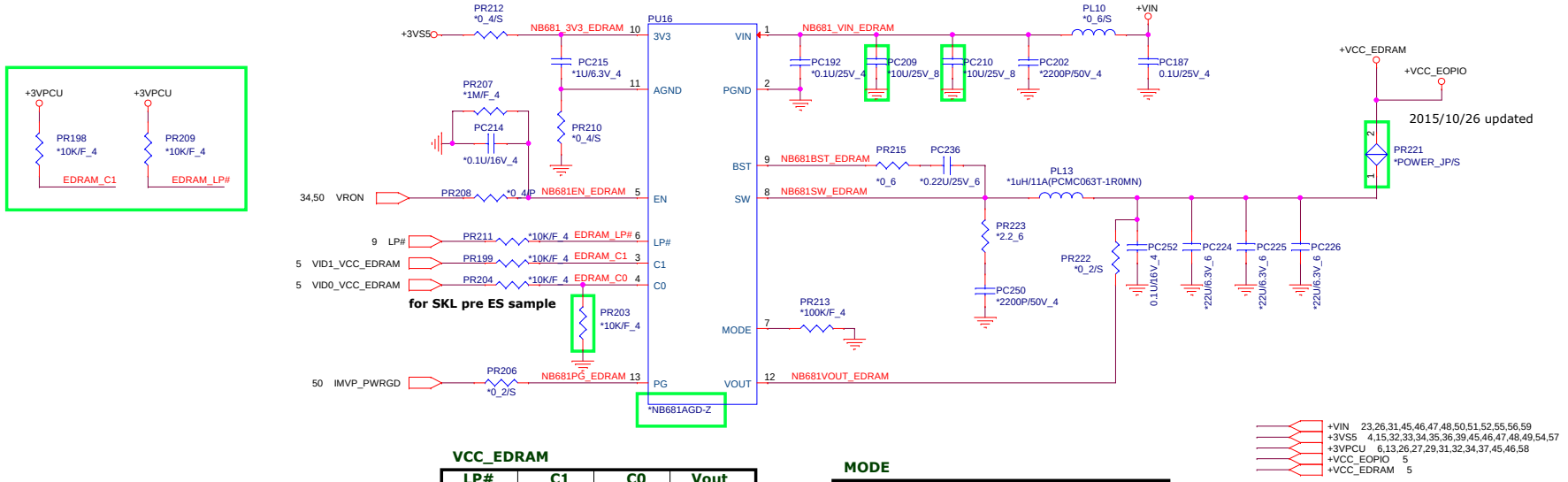



NB5

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | +VCORE/VCCSA (NCP81253) | |
| Date: Tuesday, July 19, 2016 | Sheet 52 of 59 | |

**+VCC_EDRAM +/- 5%**
**Countinue current:4.5A**
**Peak current:6A**




+VIN 23,26,31,45,46,47,48,50,51,52,55,56,59
+3VS5 4,15,32,33,34,35,36,39,45,46,47,48,49,54,57
+3VPCU 6,13,26,27,29,31,32,34,37,45,46,58
+VCC_EOPIO 5
+VCC_EDRAM 5

**VCC_EDRAM**

| LP# | C1 | C0 | Vout |
|---|---|---|---|
| 0 | X | X | 0 |
| 1 | 0 | 0 | 0.8 |
| 1 | 0 | 1 | 0.95 |
| 1 | 1 | 0 | 1.0 |
| 1 | 1 | 1 | 1.05 |

**MODE**

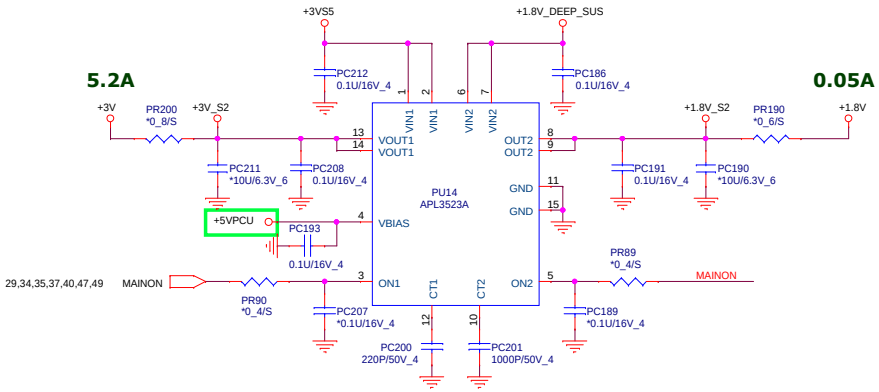
| | VR rail | Resistor |
|---|---|---|
| M1 | VCCIO | 0 |
| M2 | PRIMCORE | Float |
| M3 | EDRAM/EOPIO | 100K |
| M4 | other | 150K |

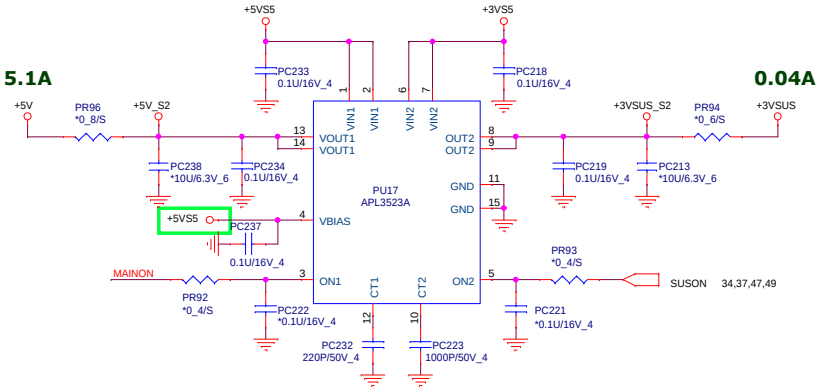
**PROJECT : X31**
Quanta Computer Inc.

NB5

| Size | Document Number | Rev |
|---|---|---|
| Custom | +VCC_EDRAM (NB681)_23E | |
| Date: Tuesday, July 19, 2016 | Sheet 53 of 59 | |

+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,55
+5V 24,25,28,31
+1.8V 5,25
+3VS5 4,15,32,33,34,35,36,39,45,46,47,48,49,53,57
+5VS5 4,25,26,29,37,38,40,46,47,48,49,50,51,52,55,56,57
+3VSUS 31,32
+5VPCU 25,26,46,57






NB5

**PROJECT : X31**
Quanta Computer Inc.

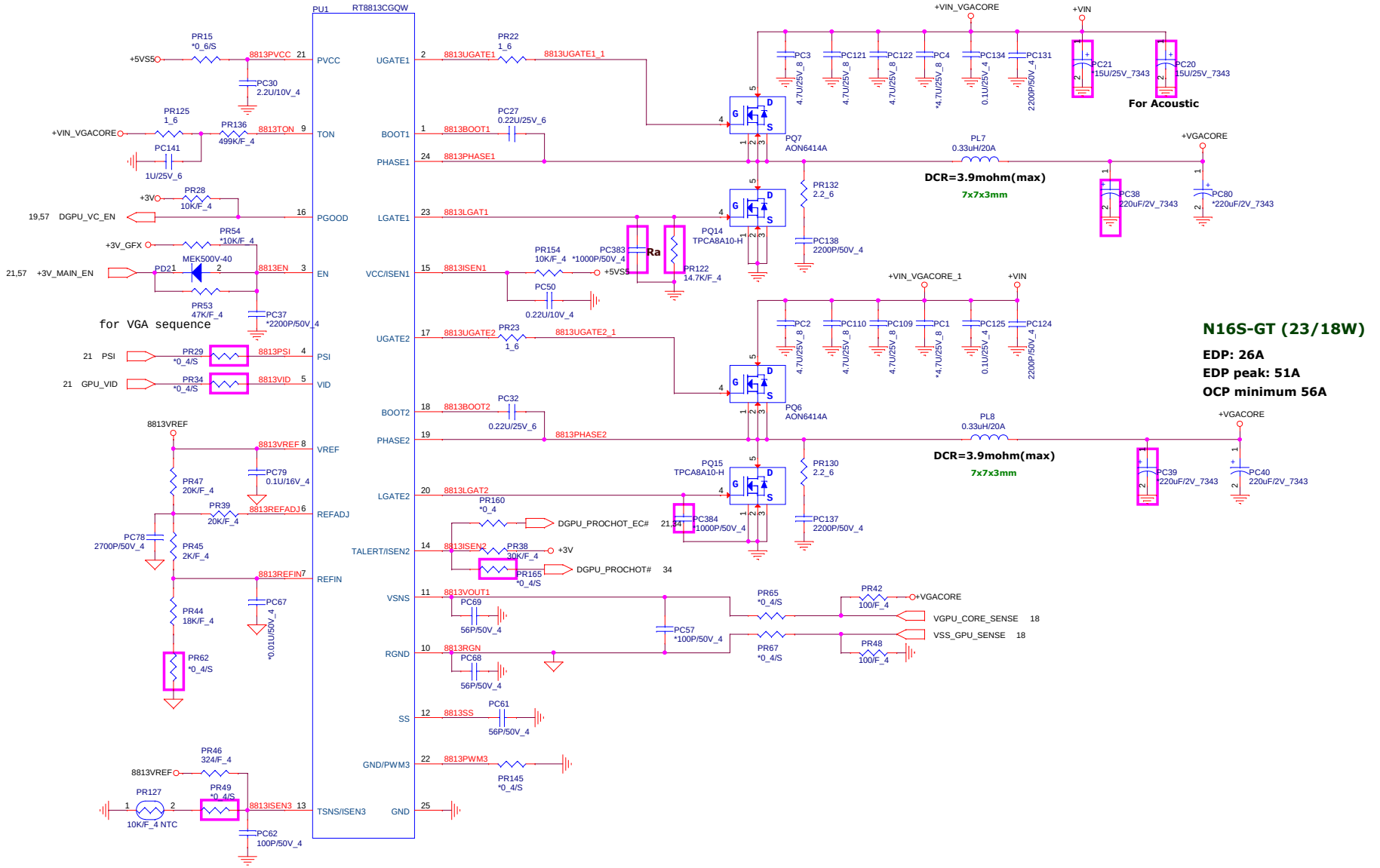
| Size | Document Number | Rev |
|---|---|---|
| Custom | Dis-charge IC (SLG55448) | 1A |

Date: Tuesday, July 19, 2016 Sheet 54 of 59

# VGA Core

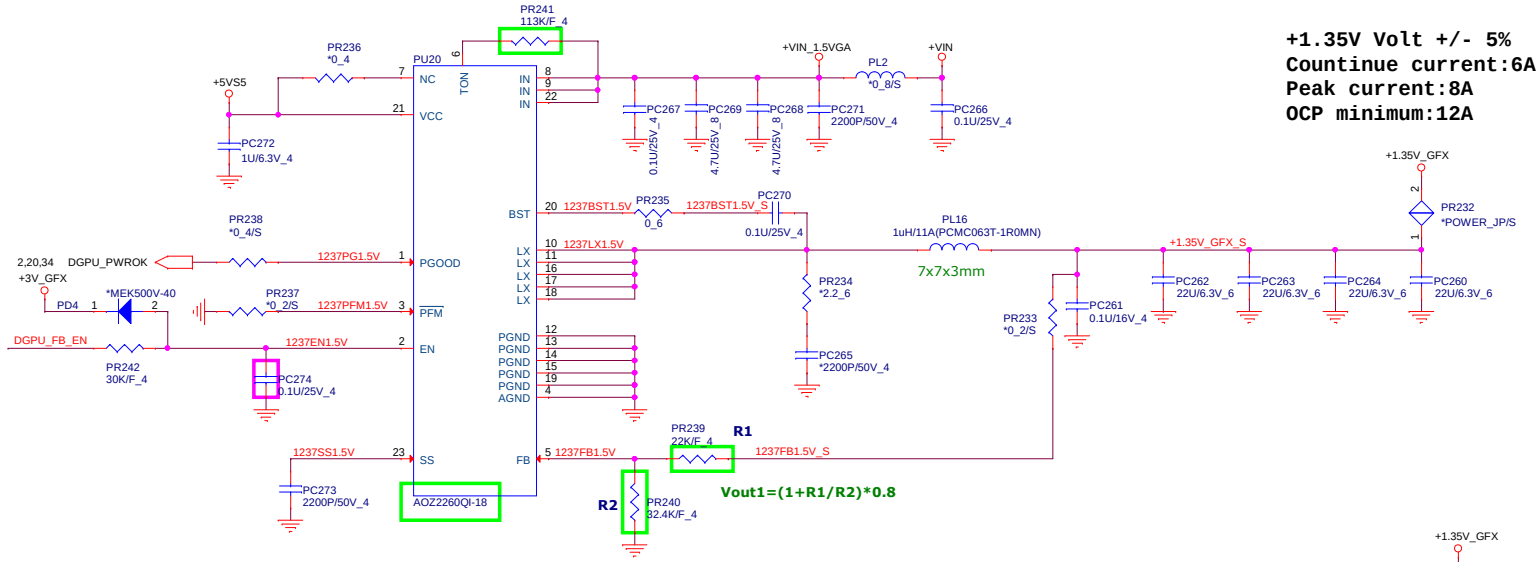


+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54
+VIN 23,26,31,45,46,47,48,50,51,52,53,56,59
+5VS5 4,25,26,29,37,38,40,46,47,48,49,50,51,52,54,56,57
+3V_GFX 18,20,21,56,57
+VGACORE 18




| | | |
|---|---|---|
| NB5 | PROJECT : X1Q<br>Quanta Computer Inc. | |
| Size Custom | Document Number +VGACORE (RT8813A) | Rev 2A |
| Date: Tuesday, July 19, 2016 | Sheet 55 of 59 | |

+VIN 23,26,31,45,46,47,48,50,51,52,53,55,59
+5VS5 4,25,26,29,37,38,40,46,47,48,49,50,51,52,54,55,57
+1.35V_GFX 19,20,22



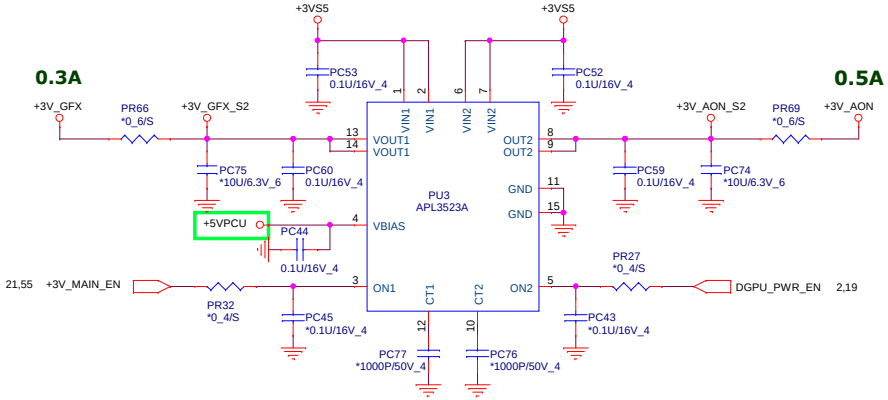

**PROJECT : X1Q**
Quanta Computer Inc.

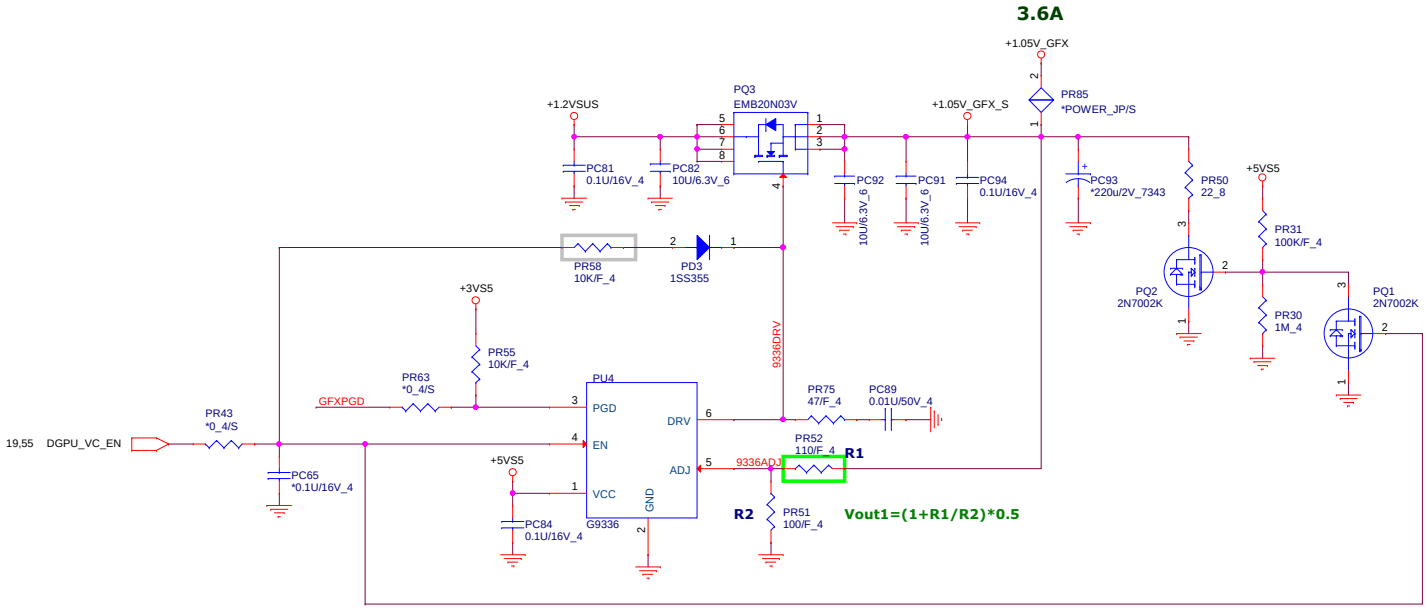
| Size | Document Number | Rev |
|---|---|---|
| Custom | +1.35V_VGA(AOZ1237) | 1A |

NB5

Date: Tuesday, July 19, 2016 Sheet 56 of 59

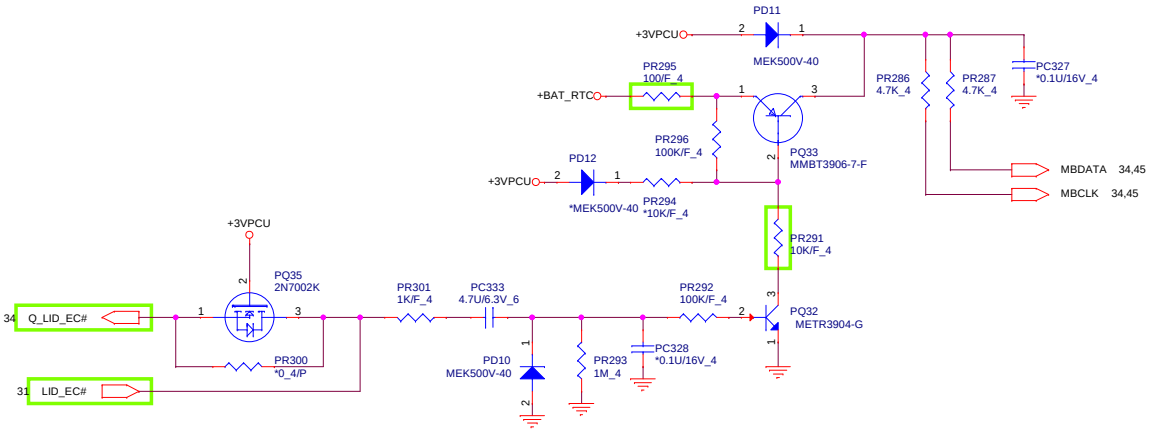
+VIN 23,26,31,45,46,47,48,50,51,52,53,55,56,59
+3VS5 4,15,32,33,34,35,36,39,45,46,47,48,49,53,54
+5VS5 4,25,26,29,37,38,40,46,47,48,49,50,51,52,54,55,56
+3V_GFX 18,20,21,55,56
+3V_AON 18,20,21
+1.2VSUS 3,6,16,17,24,47,49,59
+1.05V_GFX 18,19,20




| | | |
|---|---|---|
| NB5 | PROJECT : X1Q<br>Quanta Computer Inc. | |
| Size Custom | Document Number 1.05V_VGA/3V_VGA | Rev 1A |
| Date Tuesday, July 19, 2016 | Sheet 57 of 59 | |

+3VPCU 6,13,26,27,29,31,32,34,37,45,46,53
+BAT_RTC 4,13,15,31,45




| | | |
|---|---|---|
| NB5 | **PROJECT : X31**<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: EMI solution | Rev: 1A |
| Date: Tuesday, July 19, 2016 | Sheet 58 of 59 | |

+VIN 23,26,31,45,46,47,48,50,51,52,53,55,56
+PRWSRC 45
+VA_AC 44,45

0329

**Reserve for RF**

+VCC_CORE

EC11 *2.2U/10V_4
EC10 *2.2U/10V_4
EC7 *2.2U/10V_4
EC14 *2.2U/10V_4
EC15 *2.2U/10V_4

**Reserve for RF**

+1.2VSUS

EC31 *2.2U/10V_4
EC32 *2.2U/10V_4
EC38 *2.2U/10V_4
EC37 *2.2U/10V_4
EC48 *2.2U/10V_4
EC45 *2.2U/10V_4
EC44 *2.2U/10V_4
EC28 *2.2U/10V_4
EC47 *2.2U/10V_4
EC49 *2.2U/10V_4

**EMI request for ISN**

+VIN

EC72 *10U/25V_8
EC76 *10U/25V_8
EC73 *10U/25V_8
EC71 *10U/25V_8

**EMI request for ISN**

+PRWSRC

EC69 *10U/25V_8

**Reserve for RF**

+VIN

EC3 *2.2U/25V_4
EC5 *2.2U/25V_4
EC8 *2.2U/25V_4
EC6 *2.2U/25V_4
EC2 *2.2U/25V_4
EC1 *2.2U/25V_4
EC4 *2.2U/25V_4

**Reserve for RF**

+VA_AC

EC50 *2.2U/25V_4
EC75 *2.2U/25V_4
EC74 *2.2U/25V_4
EC66 *2.2U/25V_4
EC51 *2.2U/25V_4

NB5

**PROJECT : X31**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | EMI solution | 1A |

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