TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory, CPU-PEG/Display	3,4
CPU-Control/MISC/CFG/Audio	5
CPU-Power,CPU-GND	6,7
DDR4 1/2,DDR4-POWER/GND-1/2	8,9,10,11
PCH-USB/PCIE/DMI/SATA	12
PCH-Audio/Display/Clock	13
PCH-GPIO/USBOC#/SATASTRAP	14
PCH-LPC/SPI/SMBUS/MISC	15
PCH-Power,PCH-GND,PCH-Strap	16,17,18
PCIE SLOT-CPU(X16)	19
PCIE SLOT-PCH(X1)	20
SIO-NCT5563D-M/FAN CONTROLLOR	21,22
AUDIO - ALC892/887,AUDIO - depop circuit	23,24
LAN - RTL8111H	25
DVI/HDMI/VGA	26,27,28
USB2.0/USB3.0/SATA connector	29,30,31
CUT_VBAT circuit/BIOS ROM	32,33
ACPI CONTROLLER	34
PWM-RT3606BC/VCORE 3PHASE/VGT 2PHASE	35,36,37
DDR-RT8231/DDR-MP2147-VPP25	38,39
CPU PWR_ST/PLL	40
PCH Core power	41
VCCSA - POWER/VCCIO - POWER	42,43
ATX F_Panel/TPM/MSI_LED	44
DEBUG LED/EMI CAP/Manial Part	45,46,47
Power Map/Power Sequence/GPIO MAP	48,49,50
Revision History	51

MS-7996

ATX:235*180

Ver: 10

Intel -SkyLake-S plamform

CPU:

LGA1151
*CPU POWER PAK *3 Phase*
*GT POWER PAK *2 Phase*

Onboard Chip:

HD Audio Codec: ALC892
SIO: NCT5563D
Flash ROM: SPI 64 MB
DP to VGA: ITE6515

Main Memory:

*DDR4 * 2 (Dual Channel)*

ACPI:

5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7133+PN MOS
3VDSW:GS7133

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 2*

System Chipset:

SPT-H :B150
SPT-H :H150

PWM:

VCORE - RT3606
DDR - RT8231
PCH(1.0V) - UP1540
VCCSA - RT8125C
VCCIO - NB681(Converter)
VPP25 - MP2147

LDO:

VCCSTPLL - GS7133

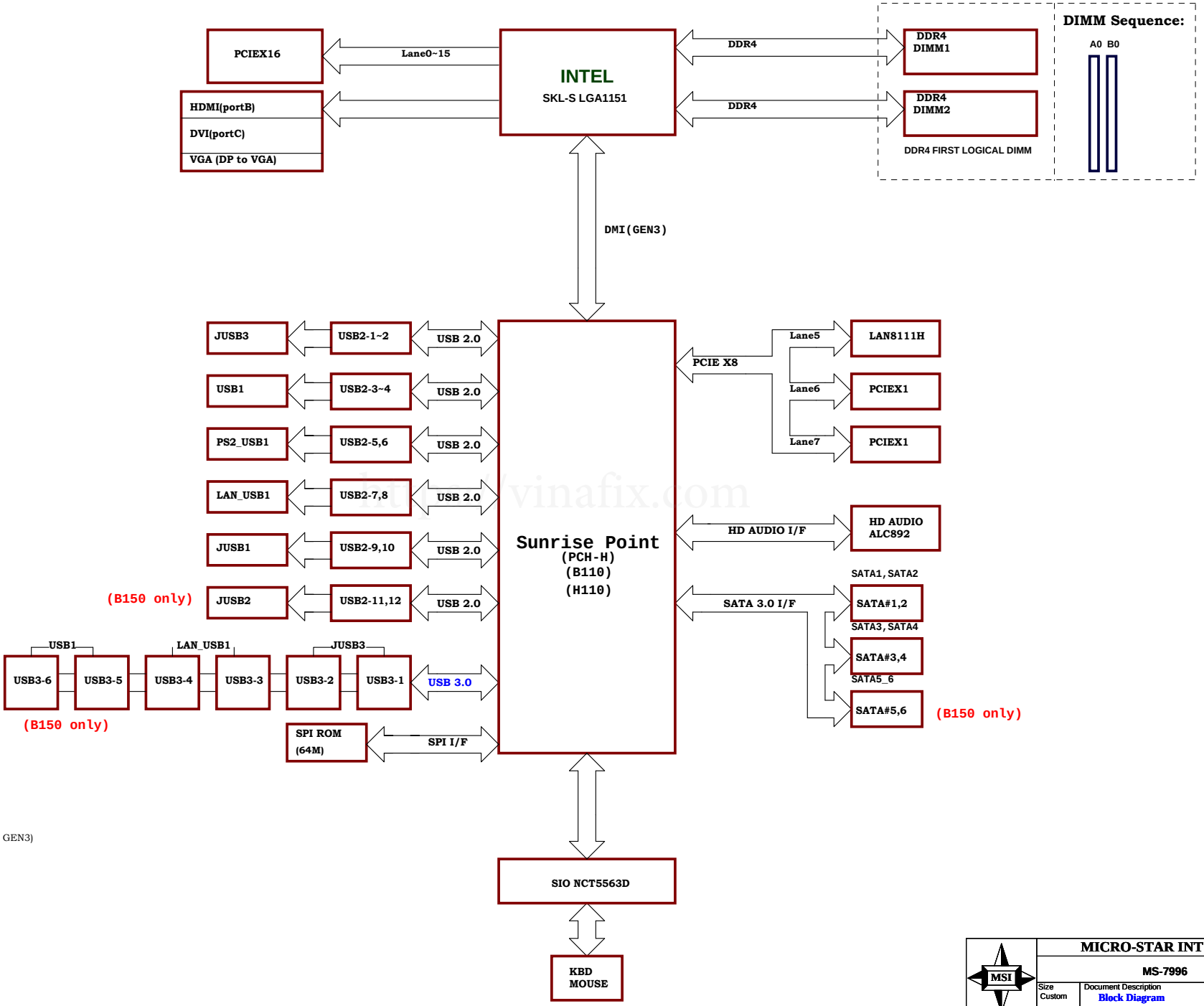
MICRO-STAR INT'L CO.,LTD

MS-7996

Size	Document Description	Rev
Custom	Cover Sheet	10

Date: Friday, August 07, 2015 Sheet 1 of 51

MS-7996 Block Diagram



Slot Sequence:

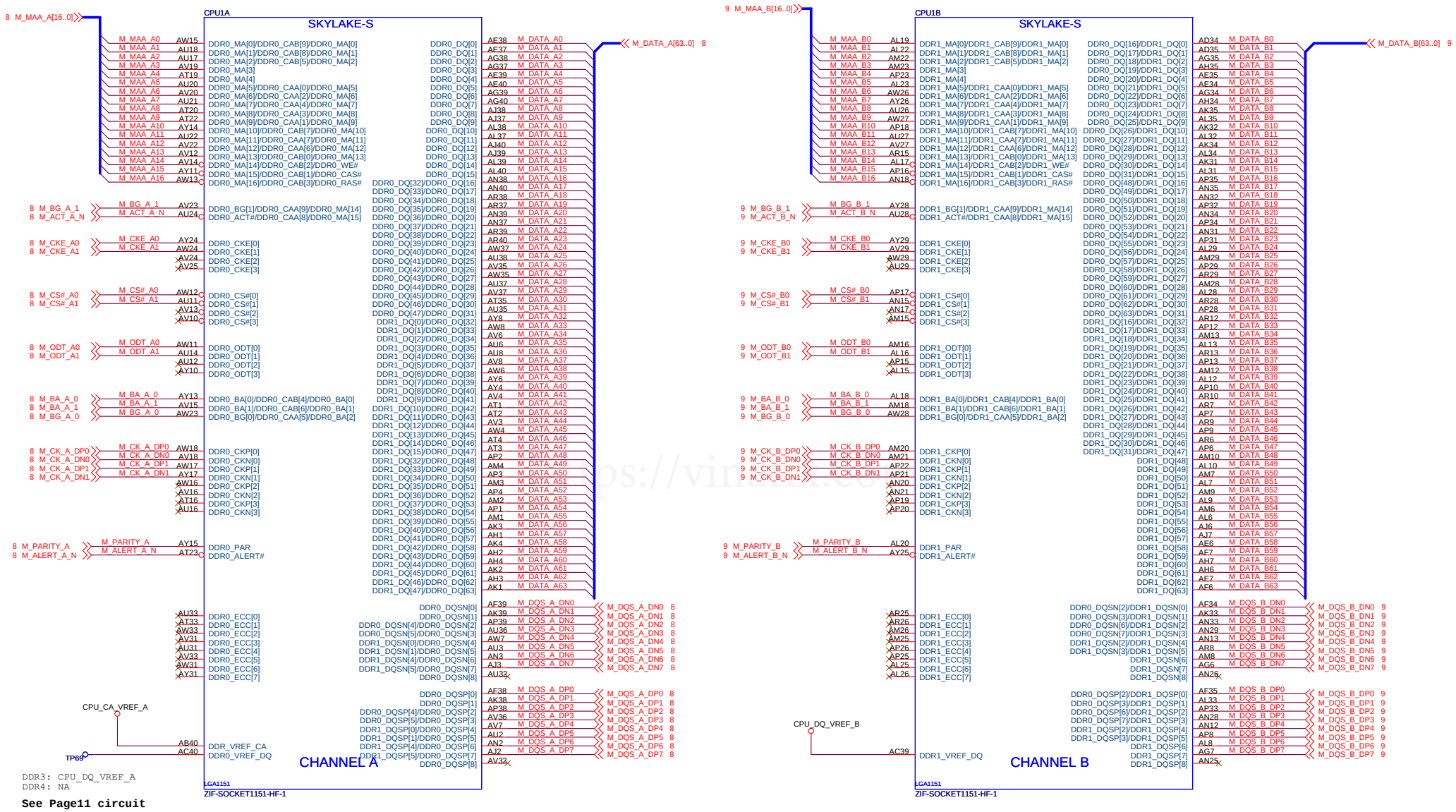
PCIE X16	(By CPU GEN3)
PCIE X1	(By PCH GEN3)
PCIE X1	(By PCH GEN3)

MICRO-STAR INT'L CO.,LTD

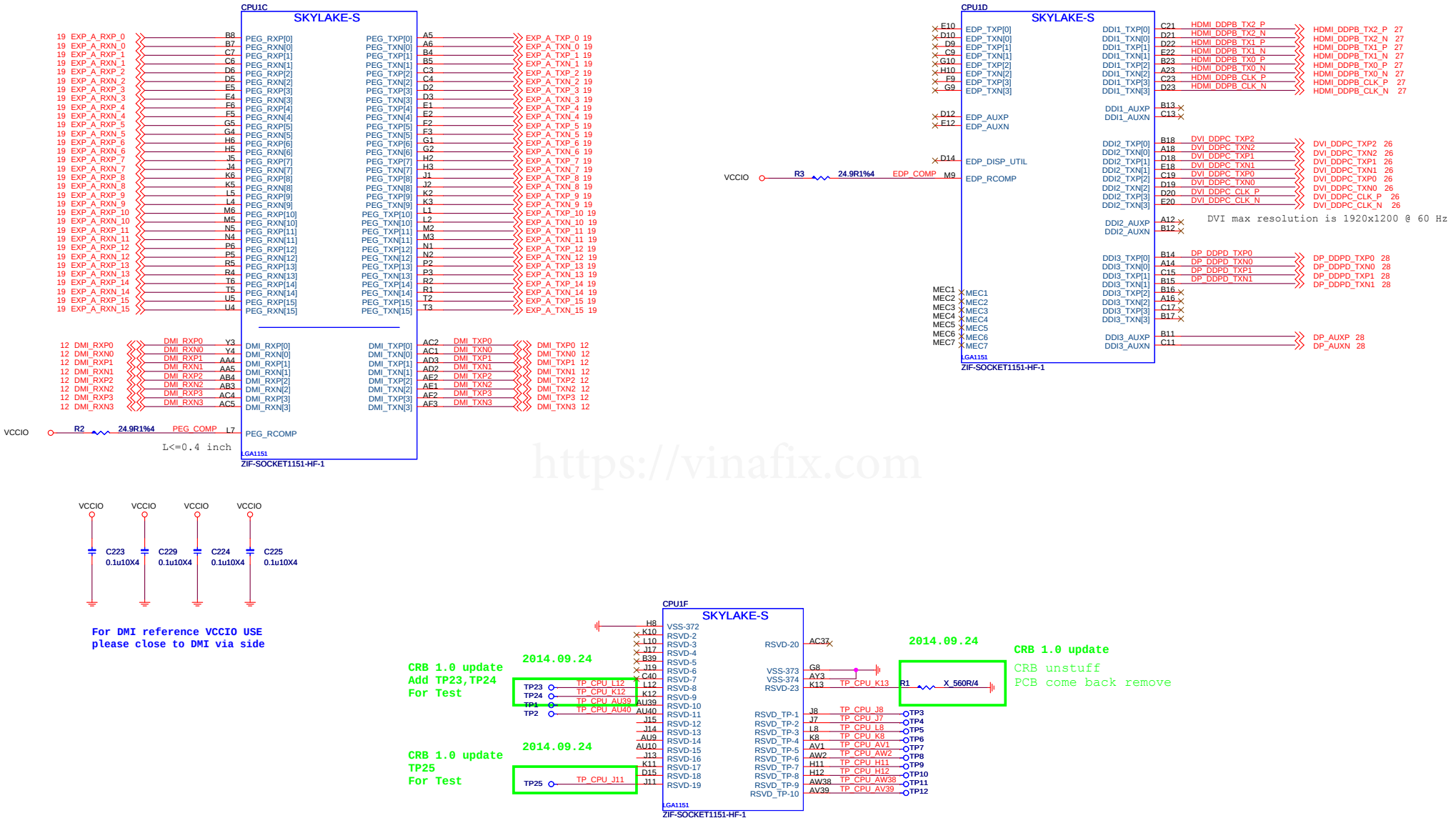
MS-7996

Size: Custom | Document Description: Block Diagram | Rev: 10

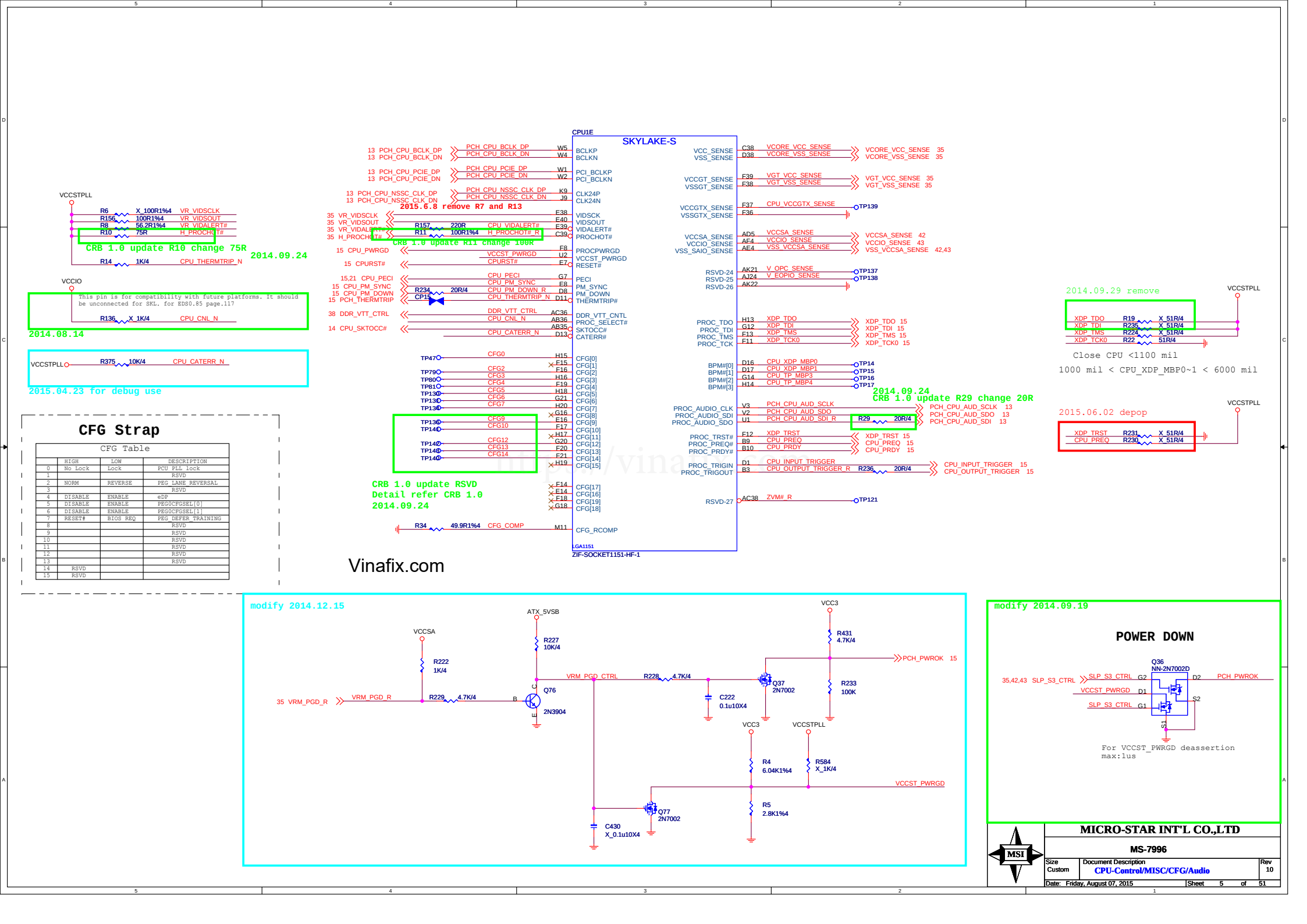
Date: Friday, August 07, 2015 | Sheet 2 of 51



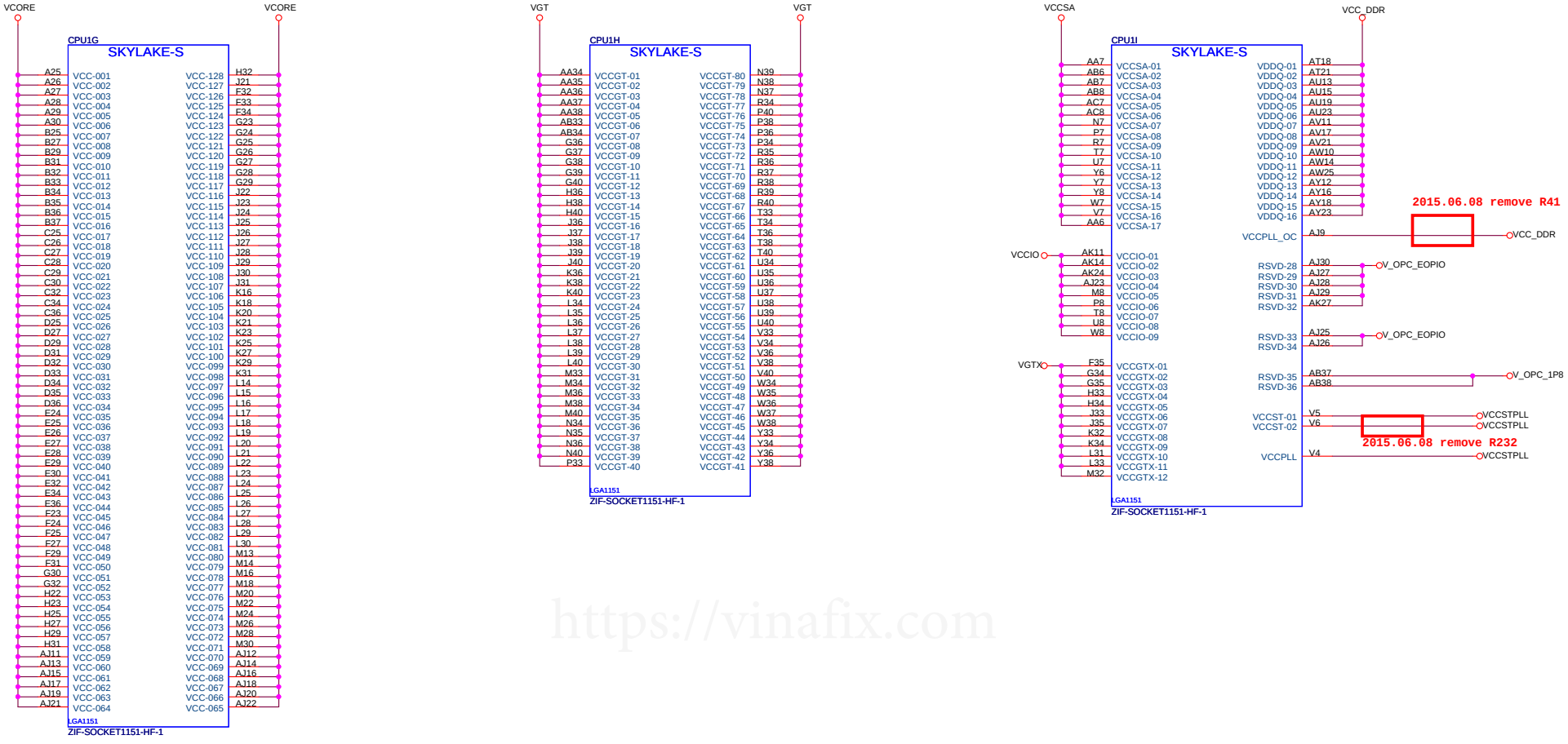
MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: CPU-Memory
Rev: 10	
Date: Friday, August 07, 2015	Sheet 3 of 51



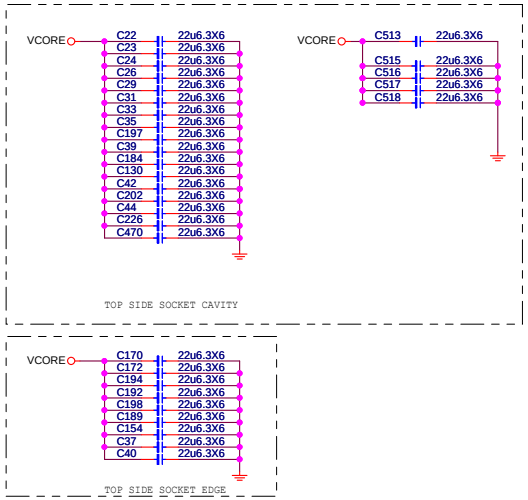
MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: CPU-PEG/Display
Rev: 10	
Date: Friday, August 07, 2015	Sheet 4 of 51

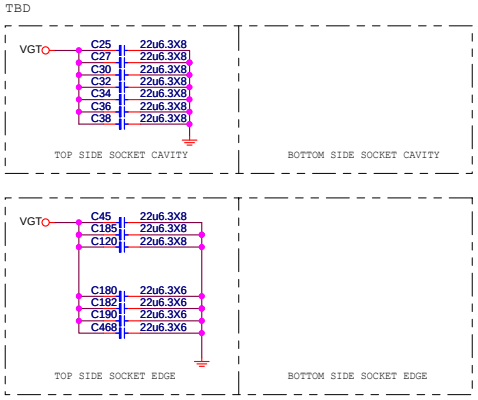


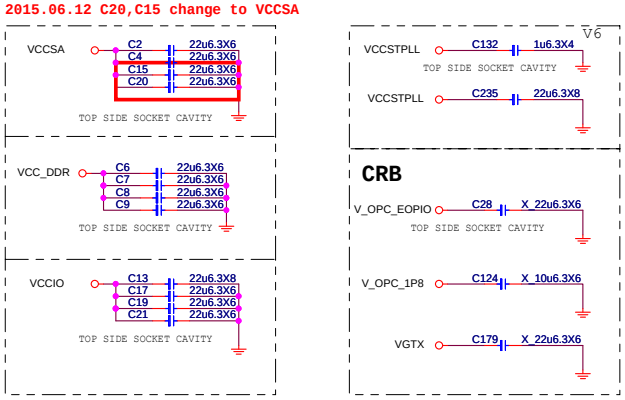
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU_PLL_lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS_REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



CAP





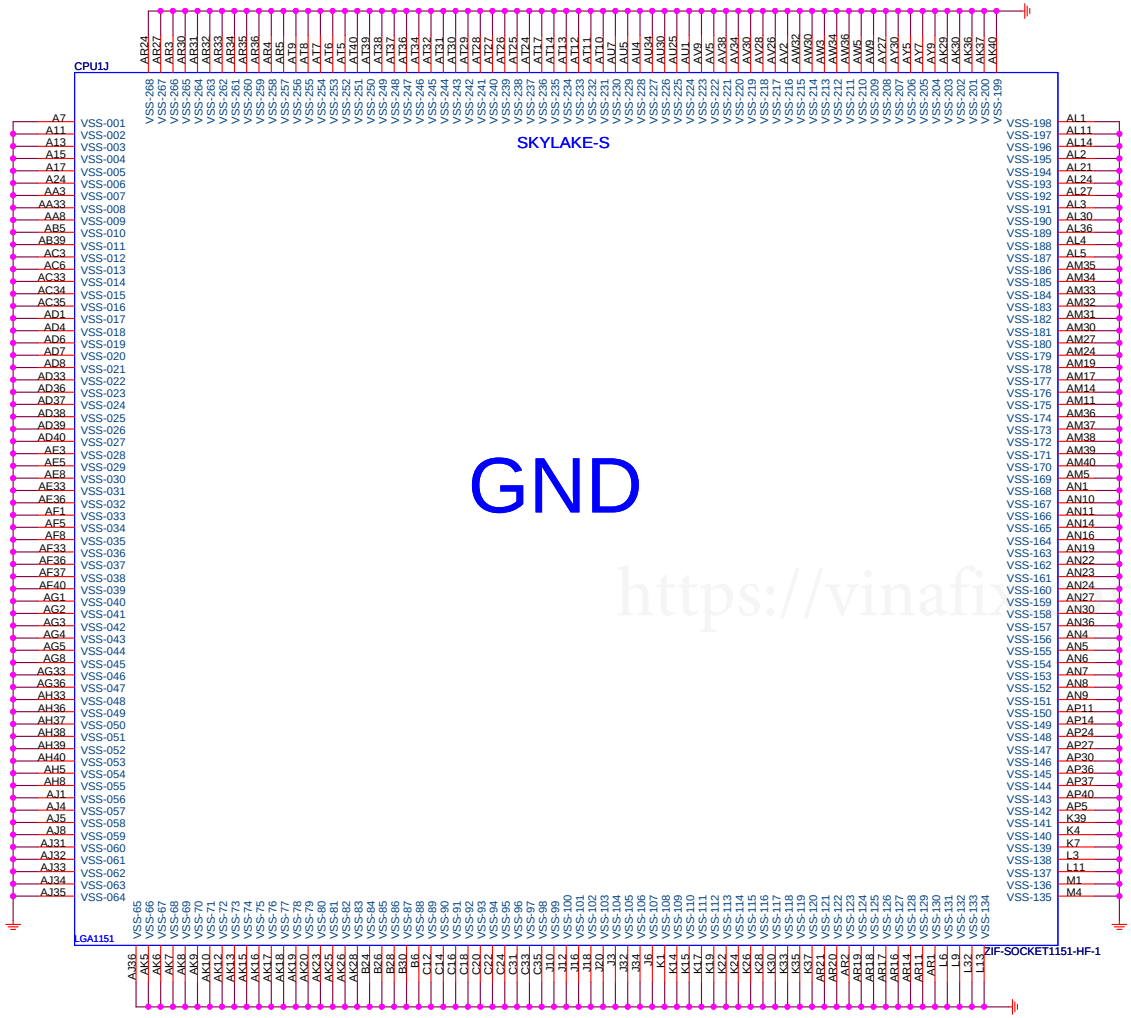


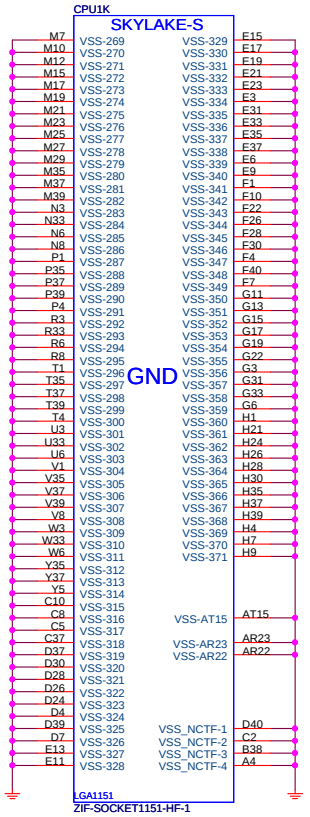
MICRO-STAR INT'L CO.,LTD

MS-7996

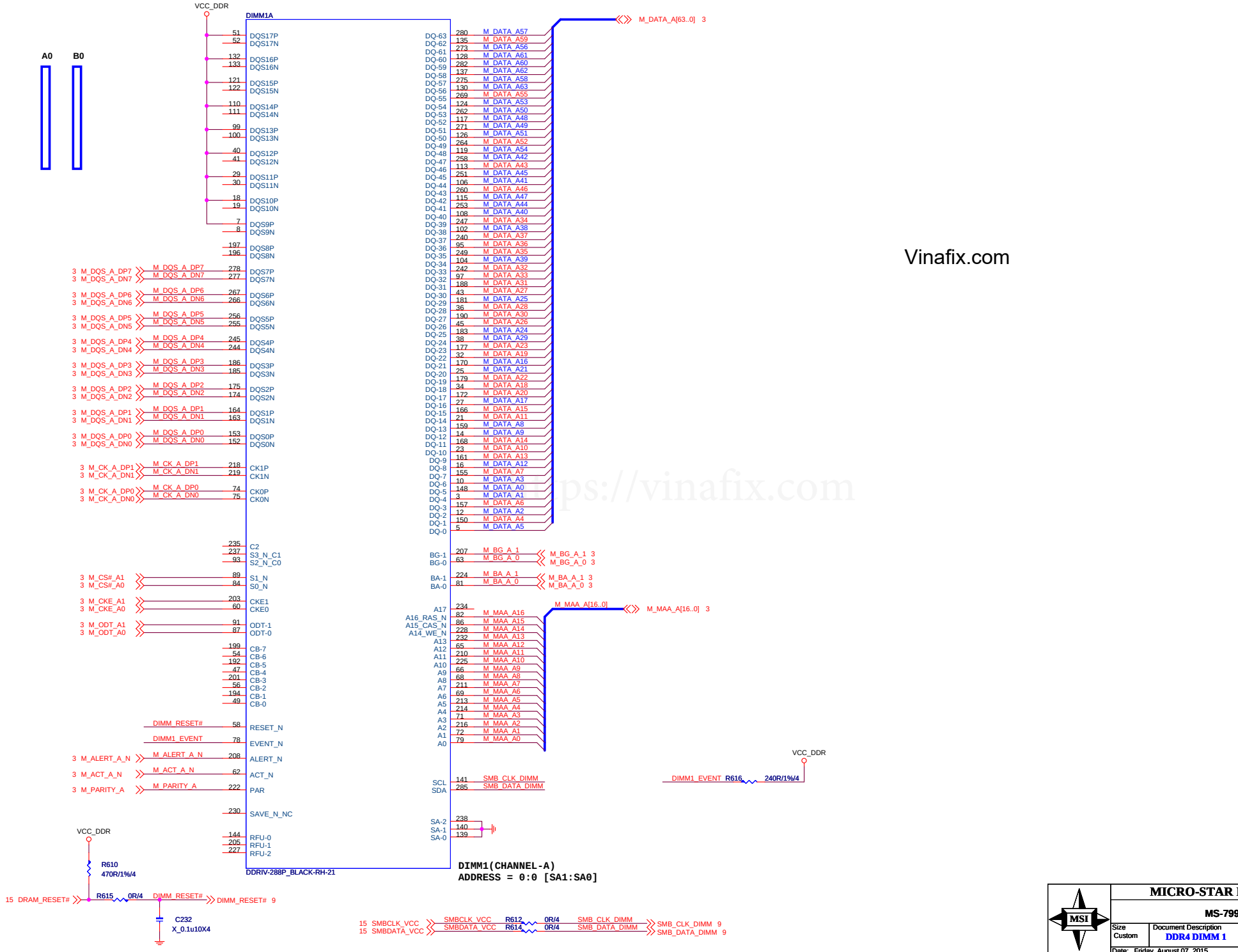
Size	Document Description	Rev
Custom	CPU-Power	10

Date: Friday, August 07, 2015 Sheet 6 of 51

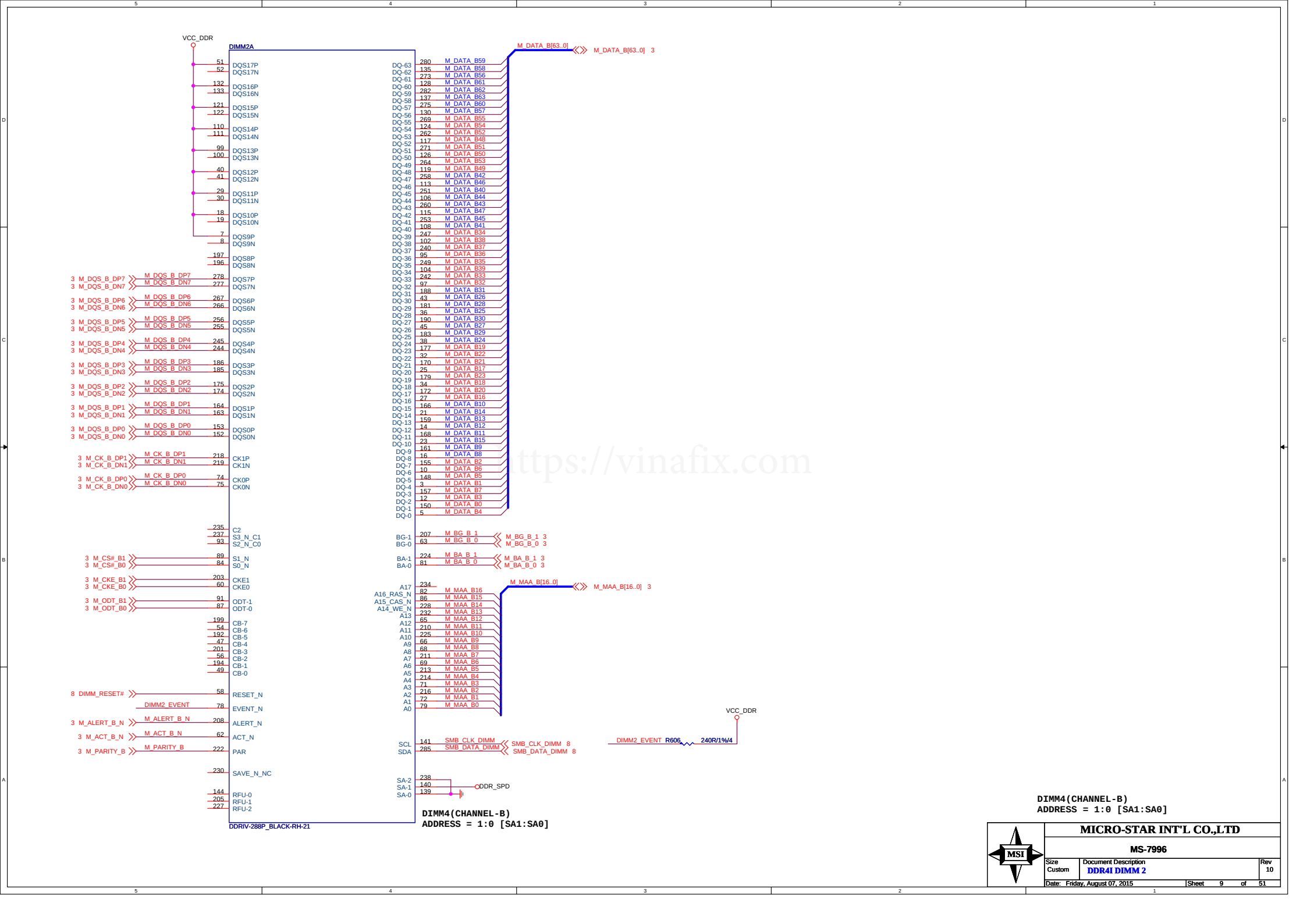


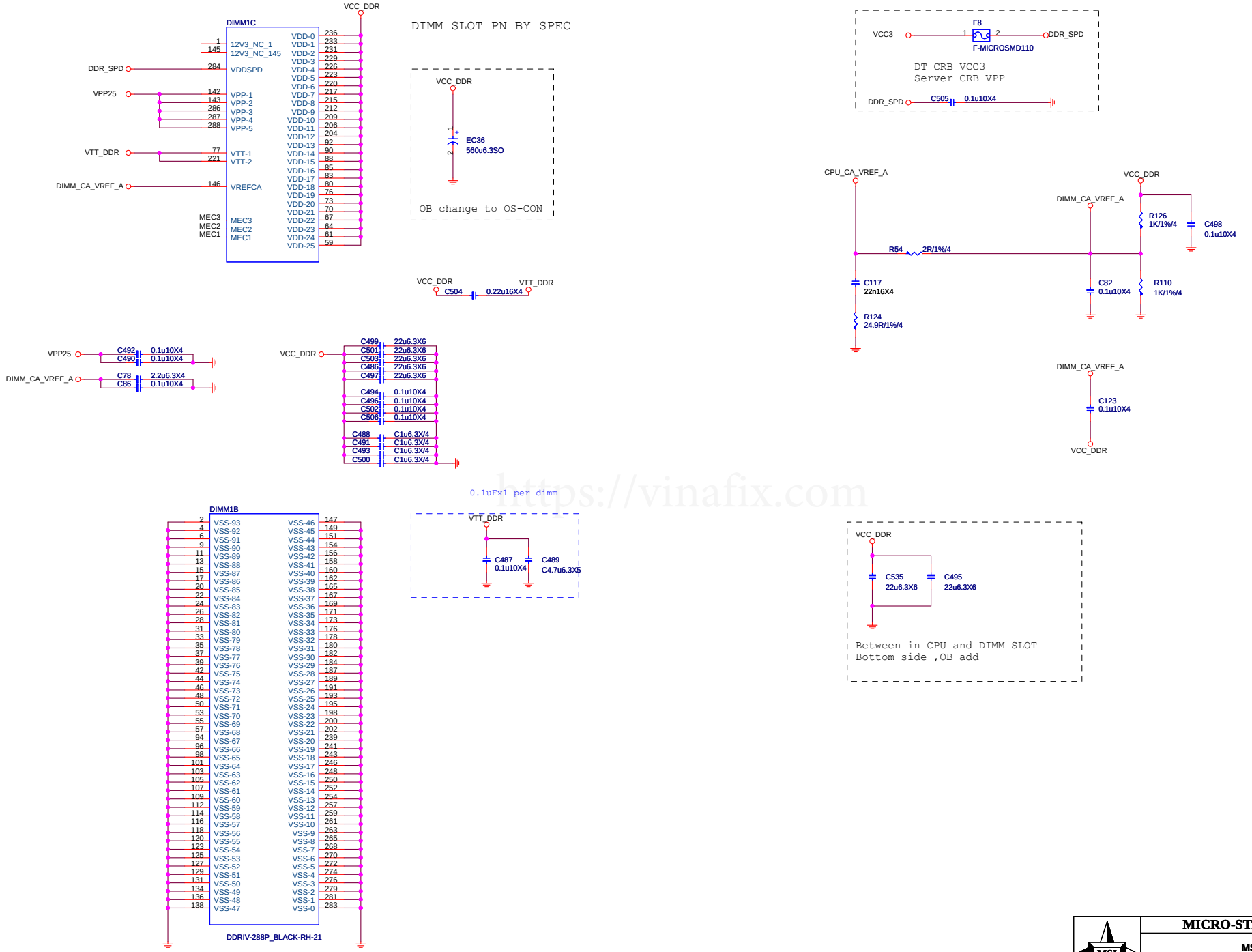


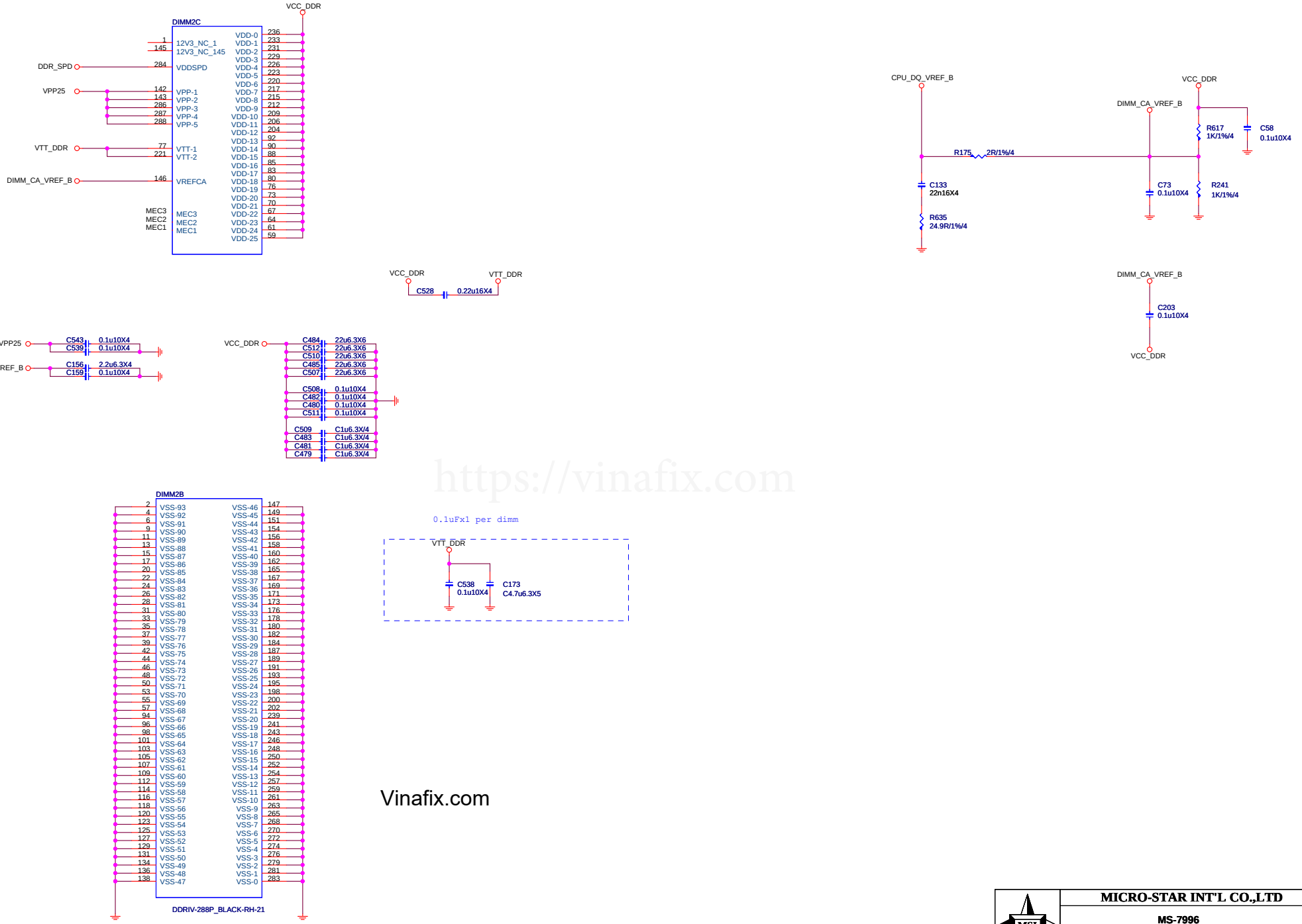
MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: CPU-GND	Rev: 10
Date: Friday, August 07, 2015	Sheet 7 of 51	



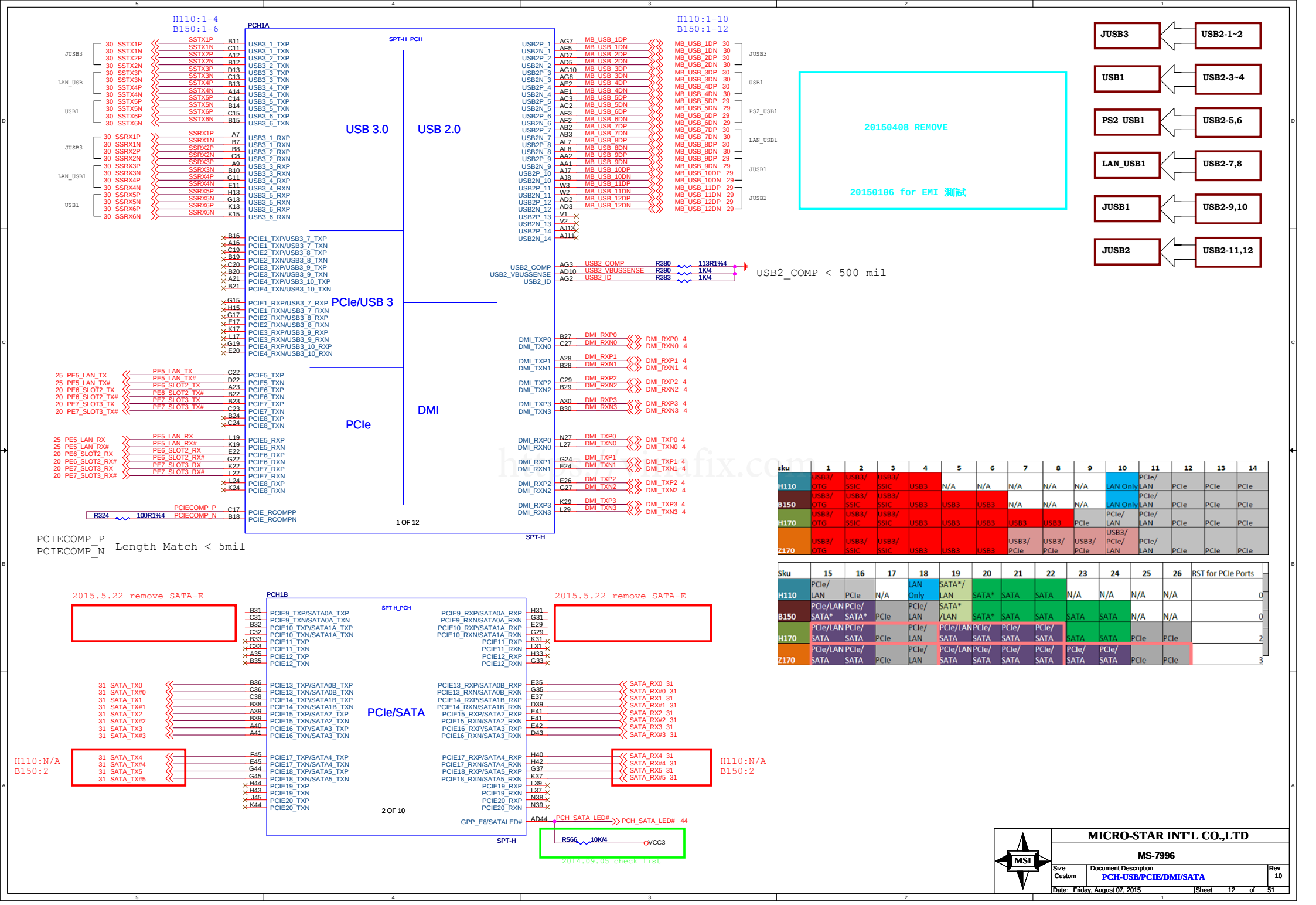
MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: DDR4 DIMM 1	Rev: 10
Date: Friday, August 07, 2015	Sheet 8 of 51	


VCC_DDR
DIMM2A
DDRIV-288P_BLACK-RH-21
M_DATA_B[63..0]
M_DATA_B[63..0] 3
M_MAA_B[16..0]
M_MAA_B[16..0] 3
DIMM4(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
DDR_SPD
DIMM2_EVENT
R606
240R/1%/4
MICRO-STAR INT'L CO.,LTD
MS-7996
DDR4I DIMM 2
Date: Friday, August 07, 2015
Sheet 9 of 51





MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: DDR4-POWER/GND-2	Rev: 10
Date: Friday, August 07, 2015	Sheet 11 of 51	



sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe

Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: PCH-USB/PCIE/DMI/SATA
Rev: 10	
Date: Friday, August 07, 2015	Sheet 12 of 51

2015.7.28 R510 33R→30R

GPP_I[3:0] with SMI/NMI

EMI

AZ_BITCLK

CA23 X_10p50N4

23 AZ_BITCLK — AZ_BITCLK — R449 33R/4 — R510 30R1%4 — AZ_BITCLK_LR — AZ_RST#_R
23 AZ_RST#
23 AZ_SDIN0

18 AZ_SDOUT_R — AZ_SDOUT_R — R489 33R/4 — AZ_SDOUT_R
23 AZ_SDOUT — AZ_SDOUT — R490 33R/4 — AZ_SYNC_R
23 AZ_SYNC — AZ_SYNC

5 PCH_CPU_AUD_SDO — R412 33R/4 — PCH_CPU_AUD_SDO_R
5 PCH_CPU_AUD_SDI — PCH_CPU_AUD_SDI
5 PCH_CPU_AUD_SCLK — R419 33R/4 — PCH_CPU_AUD_SCLK_R

PCH1D

SPT-H_PCH

BA9 HDA_BCLK
BD8 HDA_RST#
BE7 HDA_SDI0
BC8 HDA_SDI1
BB7 HDA_SDO
BD9 HDA_SYNC
AM1 DISPA_SDO
AN2 DISPA_SDI
AM2 DISPA_BCLK

AUDIO

AL42 GPP_D8/SSP0_SCLK
AN42 GPP_D7/SSP0_RXD
AM43 GPP_D6/SSP0_TXD
AJ33 GPP_D5/SSP0_SFRM

AH44 GPP_D20/DMIC_DATA0
AJ35 GPP_D19/DMIC_CLK0
AJ38 GPP_D18/DMIC_DATA1
AJ42 GPP_D17/DMIC_CLK1

4 OF 10

Port B
GPP_I5/DDPB_CTRLCLK — BA5 — HDMI_DDPB_CTRLCLK — HDMI_DDPB_CTRLCLK 27
GPP_I6/DDPB_CTRLDATA — BC4 — HDMI_DDPB_CTRLDATA — HDMI_DDPB_CTRLDATA 27
GPP_I0/DDPB_HPD0 — AW4 — HDMI_DDPB_HPD — HDMI_DDPB_HPD 27

Port C
GPP_I7/DDPC_CTRLCLK — BB3 — DVI_DDPC_CTRLCLK — DVI_DDPC_CTRLCLK 26
GPP_I8/DDPC_CTRLDATA — BD6 — DVI_DDPC_CTRLDATA — DVI_DDPC_CTRLDATA 26
GPP_I1/DDPC_HPD1 — AY2 — DVI_DDPC_HPD — DVI_DDPC_HPD 26

Port D
GPP_I9/DDPD_CTRLCLK — BE5 — DP_DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA — BE6 — DP_DDPD_CTRLDATA
GPP_I2/DDPD_HPD2 — AV4 — DP_HPD — DP_HPD 28

GPP_I3/DDPE_HPD3 — BA4 — DDPE_HPD3 — R428 10K/4

By Server CRB

eDP
GPP_F21/EDP_BKLTCTL — W36
GPP_F20/EDP_BKLTEN — W35
GPP_F19/EDP_VDDEN — W42
GPP_I4/EDP_HPD — BD7 — EDP_HPD — R476 100K

SPT-H

VCC3

For HDMI
HDMI_DDPB_CTRLCLK — R414 2.2K/4
HDMI_DDPB_CTRLDATA — R422 2.2K/4

For DVI
DVI_DDPC_CTRLCLK — R410 X_2.2K/4
DVI_DDPC_CTRLDATA — R415 X_2.2K/4

DP_DDPD_CTRLCLK — R523 2.2K/4
DP_DDPD_CTRLDATA — R492 2.2K/4

DDI interfaace Disable
no connect

Port B HDMI

Port C DVI,HDMI2.0 OR Others

Port D DisplayPort

2015.6.1 updata circuit

24M CLOCK BUFFER

CLK_BUFFER — R1092 0R/6 — TPM_CLK

3VSB

21 CLK_SIO_24M — R541 X_10K/4 — R539 X_0R/4 — CLK_BUFFER — CLK_BUFFER_OUT0

U19
1 CLK_IN
2 OE
3 CLK0
4 GND
8 CLK3
7 CLK2
6 VDD
5 CLK1

X_5V30014PGGI8_TSSOP8-HF

3VSB

TPM_CLK — TPM_CLK 44

PCH1C

SPT-H_PCH

21 CLK_SIO_PCI — R499 22R/4 — CLK_PCH_LPC0 — BC17 GPP_A9/CLKOUT_LPC0/ESPI_CLK
CLK_BUFFER — R620 22R/4 — CLK_PCH_LPC1 — AV19 GPP_A10/CLKOUT_LPC1
TP18 — CLKOUT_48M — AR17 GPP_A16/CLKOUT_48

PCH_CLK5_1P0 — R339 2.7K1%4 — XCLK_BIASREF — E1 XCLK_BIASREF

XCLK_BIASREF < 500 mil

CLKOUT_CPUBCLK_P — G2 — PCH_CPU_BCLK_DP — PCH_CPU_BCLK_DP 5
CLKOUT_CPUBCLK_N — H2 — PCH_CPU_BCLK_DN — PCH_CPU_BCLK_DN 5 — 100M

CLKOUT_CPUNSSC_P — G1 — PCH_CPU_NSSC_CLK_DP — PCH_CPU_NSSC_CLK_DP 5
CLKOUT_CPUNSSC_N — F1 — PCH_CPU_NSSC_CLK_DN — PCH_CPU_NSSC_CLK_DN 5 — 24M

CLKOUT_CPUPCIBCLK_P — J2 — PCH_CPU_PCIE_DP — PCH_CPU_PCIE_DP 5
CLKOUT_CPUPCIBCLK_N — J1 — PCH_CPU_PCIE_DN — PCH_CPU_PCIE_DN 5 — 100M

CLKOUT_ITPXDP_P — L2
CLKOUT_ITPXDP_N — L1

3VSB

R527 10K/4 CLKREQ#0
R529 10K/4 CLKREQ#1
R531 10K/4 CLKREQ#2
R528 10K/4 CLKREQ#3
R501 10K/4 CLKREQ#4
R546 10K/4 CLKREQ#5
R479 10K/4 CLKREQ#6
R405 10K/4 CLKREQ#7
R465 10K/4 CLKREQ#8
R466 10K/4 CLKREQ#9
R481 10K/4 CLKREQ#10
R468 10K/4 CLKREQ#11
R478 10K/4 CLKREQ#12
R477 10K/4 CLKREQ#13
R469 10K/4 CLKREQ#14
R467 10K/4 CLKREQ#15

Conntact to SLOT Pin B12
for support L1 PM Substates
ME also can disable this funtion.

LAN — 25 CLKREQ#4

CLKREQ#0 — BC24 GPP_B5/SRCCLKREQ0#
CLKREQ#1 — AW24 GPP_B6/SRCCLKREQ1#
CLKREQ#2 — AT24 GPP_B7/SRCCLKREQ2#
CLKREQ#3 — BD25 GPP_B8/SRCCLKREQ3#
CLKREQ#4 — BB24 GPP_B9/SRCCLKREQ4#
CLKREQ#5 — BE25 GPP_B10/SRCCLKREQ5#
CLKREQ#6 — AT33 GPP_H0/SRCCLKREQ6#
CLKREQ#7 — AR31 GPP_H1/SRCCLKREQ7#
CLKREQ#8 — BD32 GPP_H2/SRCCLKREQ8#
CLKREQ#9 — BC32 GPP_H3/SRCCLKREQ9#
CLKREQ#10 — BB31 GPP_H4/SRCCLKREQ10#
CLKREQ#11 — BC33 GPP_H5/SRCCLKREQ11#
CLKREQ#12 — BA33 GPP_H6/SRCCLKREQ12#
CLKREQ#13 — AW33 GPP_H7/SRCCLKREQ13#
CLKREQ#14 — BB33 GPP_H8/SRCCLKREQ14#
CLKREQ#15 — BD33 GPP_H9/SRCCLKREQ15#

Clock

CLKOUT_SRC_P0 — N8 — CK_SLOT2_DP — CK_SLOT2_DP 20
CLKOUT_SRC_N0 — N7 — CK_SLOT2_DN — CK_SLOT2_DN 20
CLKOUT_SRC_P1 — L5
CLKOUT_SRC_N1 — L7
CLKOUT_SRC_P2 — F2
CLKOUT_SRC_N2 — D3
CLKOUT_SRC_P3 — G4 — CK_SLOT1_DP — CK_SLOT1_DP 19
CLKOUT_SRC_N3 — E5 — CK_SLOT1_DN — CK_SLOT1_DN 19
CLKOUT_SRC_P4 — E6 — CK_PE_LAN — CK_PE_LAN 25
CLKOUT_SRC_N4 — D5 — CK_PE_LAN# — CK_PE_LAN# 25
CLKOUT_SRC_P5 — D7
CLKOUT_SRC_N5 — D8
CLKOUT_SRC_P6 — R7
CLKOUT_SRC_N6 — R8
CLKOUT_SRC_P7 — U7
CLKOUT_SRC_N7 — U5
CLKOUT_SRC_P8 — W11
CLKOUT_SRC_N8 — W10
CLKOUT_SRC_P9 — N2
CLKOUT_SRC_N9 — N3
CLKOUT_SRC_P10 — P2
CLKOUT_SRC_N10 — P3
CLKOUT_SRC_P11 — R4 — CK_SLOT3_DP — CK_SLOT3_DP 20
CLKOUT_SRC_N11 — R3 — CK_SLOT3_DN — CK_SLOT3_DN 20
CLKOUT_SRC_P12 — U3
CLKOUT_SRC_N12 — U2
CLKOUT_SRC_P13 — Y5
CLKOUT_SRC_N13 — W7
CLKOUT_SRC_P14 — R2
CLKOUT_SRC_N14 — P1
CLKOUT_SRC_P15 — R11
CLKOUT_SRC_N15 — R13

XTAL_24M_PCH_IN — A6 XTAL24_IN
XTAL_24M_PCH_OUT — A5 XTAL24_OUT

3 OF 10

SPT-H

XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
R327 1M1%6

Y1
24MHZ20p_S-HF

2015.5.22 Y1 change to using SMD type

C332 27p50N4
C326 27p50N4

MICRO-STAR INT'L CO.,LTD

MS-7996

Size: Custom
Document Description: PCH-Audio/Display/Clock
Rev: 10
Date: Friday, August 07, 2015
Sheet 13 of 51

W/ SMI/NMI Funtion

GPP_B[23,20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]

3VSB PWR_GPP_A CP13 BC42 C380 X_0.1u10X4

2014.10.16 PCH cOM BACK test

VCC3 CRB R400 X_8.2K1%4 GPP_E3 R545 8.2K1%4 GPP_B4

GPP_B11 default GPO to LOW

If the interface is not used: the signals can be used as GPIO. If GPIO functionality is also not used, the signals can be left as no-connect.

ISH For U,Y only use

UART/GPIO no use can no connect

3VSB R384 X_10K/4 GPP_H16 R459 10K/4 R379 10K/4 GPP_H17 R455 X_10K/4 R454 10K/4 GPP_H18 R461 X_10K/4

PCH GPIO For BIOS DETCET MSI ID USED

SML For sever only use

PCH1F SPT-H_PCH

GPIO A: BA31 VCCPGPPA; BC19 GPP_A17/ISH_GP7; BB22 GPP_A18/ISH_GP0; BD21 GPP_A19/ISH_GP1; BD22 GPP_A20/ISH_GP2; BE21 GPP_A21/ISH_GP3; BD18 GPP_A22/ISH_GP4; BC22 GPP_A23/ISH_GP5

GROUP BCH PWR: BC42 VCCPGPPBCH_BC42; BD40 VCCPGPPBCH_BD40

GPIO B: BC23 GPP_B3/CPU_GP2; BD24 GPP_B4/CPU_GP3; AN24 GPP_B11; AR24 GPP_B15/GSPI0_CS#; AW27 GPP_B16/GSPI0_CLK; BD27 GPP_B17/GSPI0_MISO; BD28 GPP_B18/GSPI0_MOSI; BC27 GPP_B19/GSPI1_CS#; AV29 GPP_B20/GSPI1_CLK; AR29 GPP_B21/GSPI1_MISO; AT29 GPP_B22/GSPI1_MOSI

GPIO C: BA41 GPP_C8/UART0_RXD; AV44 GPP_C9/UART0_TXD; AV43 GPP_C10/UART0_RTS#; AU44 GPP_C11/UART0_CTS#; AU43 GPP_C12/UART1_RXD/ISH_UART1_RXD; AT43 GPP_C13/UART1_TXD/ISH_UART1_TXD; AT44 GPP_C14/UART1_RTS#/ISH_UART1_RTS#; AU41 GPP_C15/UART1_CTS#/ISH_UART1_CTS#; AT42 GPP_C16/I2C0_SDA; AR38 GPP_C17/I2C0_SCL; AR44 GPP_C18/I2C1_SDA; AR41 GPP_C19/I2C1_SCL; AR45 GPP_C20/UART2_RXD; AR39 GPP_C21/UART2_TXD; AN44 GPP_C22/UART2_RTS#; AN43 GPP_C23/UART2_CTS#

GPIO H: BD34 GPP_H10/SML2CLK; AW35 GPP_H11/SML2DATA; BD35 GPP_H12/SML2ALERT#; BC35 GPP_H13/SML3CLK; BA35 GPP_H14/SML3DATA; BB36 GPP_H15/SML3ALERT#; BD39 GPP_H16/SML4CLK; BE34 GPP_H17/SML4DATA; BC36 GPP_H18/SML4ALERT#; BB38 GPP_H19/ISH_I2C0_SDA; BC38 GPP_H20/ISH_I2C0_SCL; BE39 GPP_H21/ISH_I2C1_SDA; BD38 GPP_H22/ISH_I2C1_SCL; BD36 GPP_H23

GROUP CD PWR: BC44 VCCPGPPCD_BC44; BA45 VCCPGPPCD_BA45; BC45 VCCPGPPCD_BC45; BB45 VCCPGPPCD_BB45 → PWR_GPP_D

GPIO D: AM44 GPP_D4/ISH_I2C2_SDA/I2C3_SDA; AL44 GPP_D9 → TP60; AL36 GPP_D10 → TP77; AL35 GPP_D11 → TP28; AJ39 GPP_D12 → TP29; AK45 GPP_D13/ISH_UART0_RXD; AK44 GPP_D14/ISH_UART0_TXD; AL43 GPP_D15/ISH_UART0_RTS#; AJ43 GPP_D16/ISH_UART0_CTS#; AJ44 GPP_D23/ISH_I2C2_SCL/I2C3_SCL

GROUP EF PWR: AJ41 VCCPGPPEF_AJ41; AL41 VCCPGPPEF_AL41 → 3VSB

GPIO E: AF41 GPP_E3; AE44 GPP_E7 → TP40

GPIO F: AB33 GPP_F10 → TP43; AB35 PCH_RSVD; AA45 SV_ADVANCE; AA44 GFX_CRB_DETECT; Y44 CPU_SKTOCC#_R R373 X_0R/4 → CPU_SKTOCC# 5; W39 GPP_F22 → GPP_F22 21; V44 GPP_F23 → TP49

2014.08.14

GPIO G: AD41 VCCPGPPG → 3VSB; U43 GPP_G0/FAN_TACH_0; U42 GPP_G1/FAN_TACH_1; U41 GPP_G2/FAN_TACH_2; M44 GPP_G3/FAN_TACH_3; U36 GPP_G4/FAN_TACH_4; P44 GPP_G5/FAN_TACH_5; T45 GPP_G6/FAN_TACH_6; T44 GPP_G7/FAN_TACH_7; R44 GPP_G8/FAN_PWM_0; R43 USB_MODE → USB_MODE 34; U39 GPP_G9/FAN_PWM_1; N42 GPP_G10/FAN_PWM_2; R39 GPP_G11/FAN_PWM_3; R36 GPP_G12/GSXDOUT; R42 GPP_G13/GSXSLOAD; R41 GPP_G14/GSXDIN; P43 GPP_G15/GSXSRESET#; N44 GPP_G16/GSXCLK; R35 GPP_G17/ADR_COMPLETE; U35 GPP_G20 → TEST_SETUP_MENU; L44 GPP_G21 → GPP_G21; L43 GPP_G22 → GPP_G22; GPP_G23 → GPP_G23

Remove

2014.08.14

GPIO DSW: BA24 VCCDSW_3P3_BA24 → 3VDSW; BD14 GPD7/RSVD → GPD7 → TP87

6 OF 10

SPT-H

Vinafix.com

3VSB PWR_GPP_D CP16

3VSB AJ41 C367 X_0.1u10X4; 3VSB AD41 C356 X_0.1u10X4

2015.04.23 USB mode change Pull down

USB_MODE R361 X_10K/4 R360 10K/4 → 3VSB

GPP_F22 R392 10K/4 → VCC3

TEST_SETUP_MENU R346 10K/4 → VCC3; R355 X_10K/4 → 3VSB

PCH_RSVD R406 10K/4 → VCC3; R417 X_10K/4 → 3VSB

GFX_CRB_DETECT R387 X_10K/4 → VCC3; R378 10K/4; R376 X_10K/4 → 3VSB

SV_ADVANCE R398 20K/4 → VCC3; R386 X_10K/4 → 3VSB

For BIOS BOM USE

3VSB R362 10K/4 GPP_G21 R365 X_10K/4; R344 10K/4 GPP_G22 R345 X_10K/4; R333 X_10K/4 GPP_G23 R338 10K/4

For BIOS BOM USE

	GPP_G21	GPP_G22	GPP_G23
B150 DVI	0	0	0
B150 HDMI	0	0	1
H110 DVI	0	1	0
H110 HDMI	0	1	1
H110 DVI only	1	0	0
B150M -IE35	1	0	1

When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

PCH1E SPT-H_PCH

USB OC#: C359 X_0.1u10X4 OC#0; C357 X_0.1u10X4 OC#1; C350 X_0.1u10X4 OC#2; C355 X_0.1u10X4 OC#3; C352 X_0.1u10X4 OC#4; C439 X_0.1u10X4 OC#5

3VSB R370 10K/4 OC#6 R369 10K/4 OC#7

R391 10K/4 OC#2 R634 10K/4 OC#5

2015.05.22 add R634
2015.06.08 add R391

29 OC#0 OC#0 AD43; 29 OC#1 OC#1 AD42; OC#2 AD39; 29 OC#3 OC#3 AC44; 29 OC#4 OC#4 Y43; OC#5 Y41; OC#6 W44; OC#7 W43

GPP_E9/USB2_OC0#; GPP_E10/USB2_OC1#; GPP_E11/USB2_OC2#; GPP_E12/USB2_OC3#; GPP_F15/USB2_OC4#; GPP_F16/USB2_OC5#; GPP_F17/USB2_OC6#; GPP_F18/USB2_OC7#

SATA DEVSLP: GPP_E4/DEVSLP0 AG42 GPP_E4 → TP19; GPP_E5/DEVSLP1 AG43 GPP_E5 → TP21; GPP_E6/DEVSLP2 AE45; GPP_F5/DEVSLP3 AB41; GPP_F6/DEVSLP4 AB42; GPP_F7/DEVSLP5 AB43; GPP_F8/DEVSLP6 AB36; GPP_F9/DEVSLP7 AB39

RSVD For B150 SATA/PCIE use

2015.5.22 remove SATA-E
2015.6.16 R607,R608 change to 1K, and DEPOP

GPP_E0 R607 X_1K/4; GPP_E1 R608 X_1K/4 → 3VSB

Low: PCIE
High: SATA

CLINK: Remove; AV2 CL_CLK; AV3 CL_DATA; AW2 CL_RST#

2014.08.14

SATA Strap: GPP_E0/SATAXPCIE0/SATAGP0; GPP_E1/SATAXPCIE1/SATAGP1; GPP_E2/SATAXPCIE2/SATAGP2; GPP_F0/SATAXPCIE3/SATAGP3; GPP_F1/SATAXPCIE4/SATAGP4; GPP_F2/SATAXPCIE5/SATAGP5; GPP_F3/SATAXPCIE6/SATAGP6; GPP_F4/SATAXPCIE7/SATAGP7

5 OF 10

SPT-H

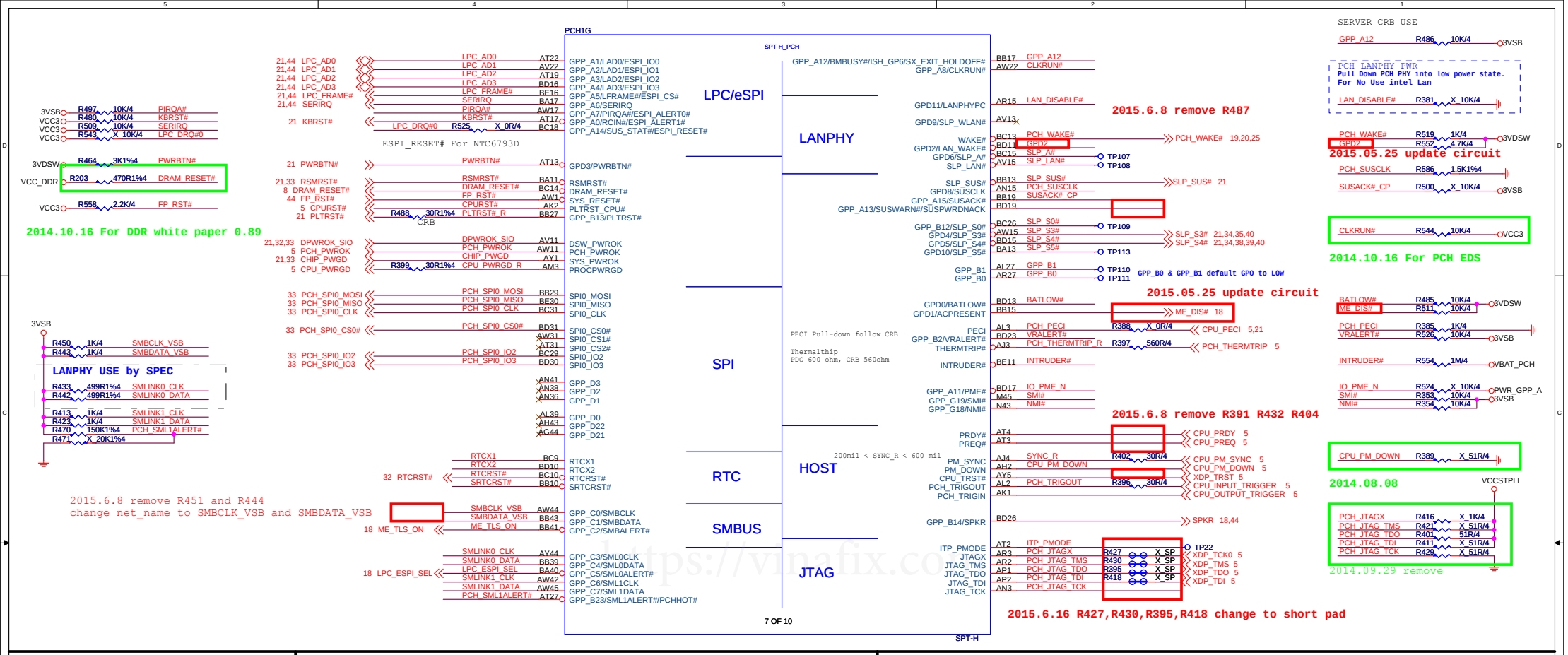
If an AMT capable Intel WLAN device is not implemented then this signal can be left as NO CONNECT (NC).

MICRO-STAR INT'L CO.,LTD

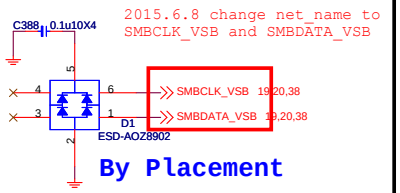
MS-7996

Size: Custom | Document Description: PCH-GPIO/USBOC#/SATASTRAP | Rev: 10

Date: Friday, August 07, 2015 | Sheet 14 of 51



SMBUS ESD

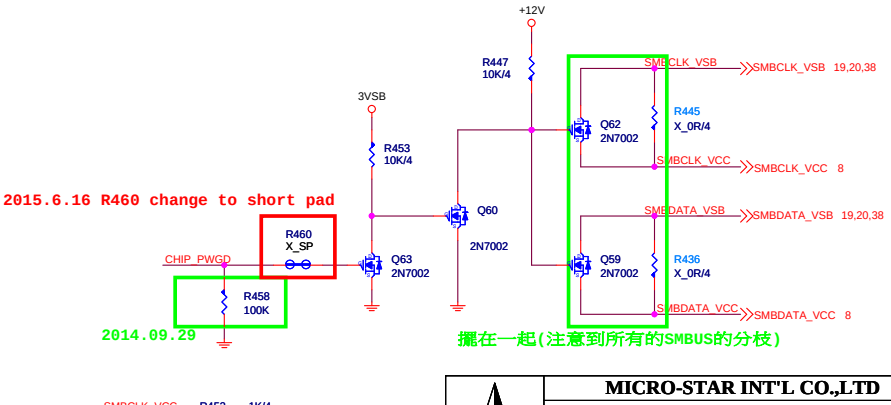


PCH Thermal Monitor

當溫度高於設定之後，此信號會被拉LOW。
PS:只能在S0下使用，S5 不會有功能

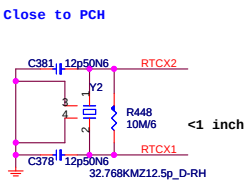
SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC

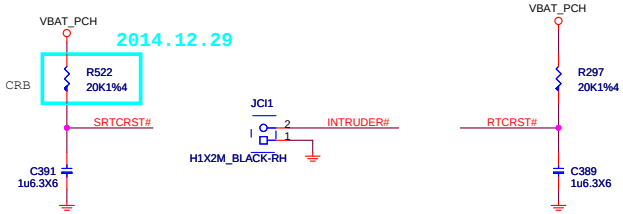
基本上PCIE的SLOT要接
3VSB的CPU的PWM IC/DDR
要接VCC3的其他的請注意
要怎麼接



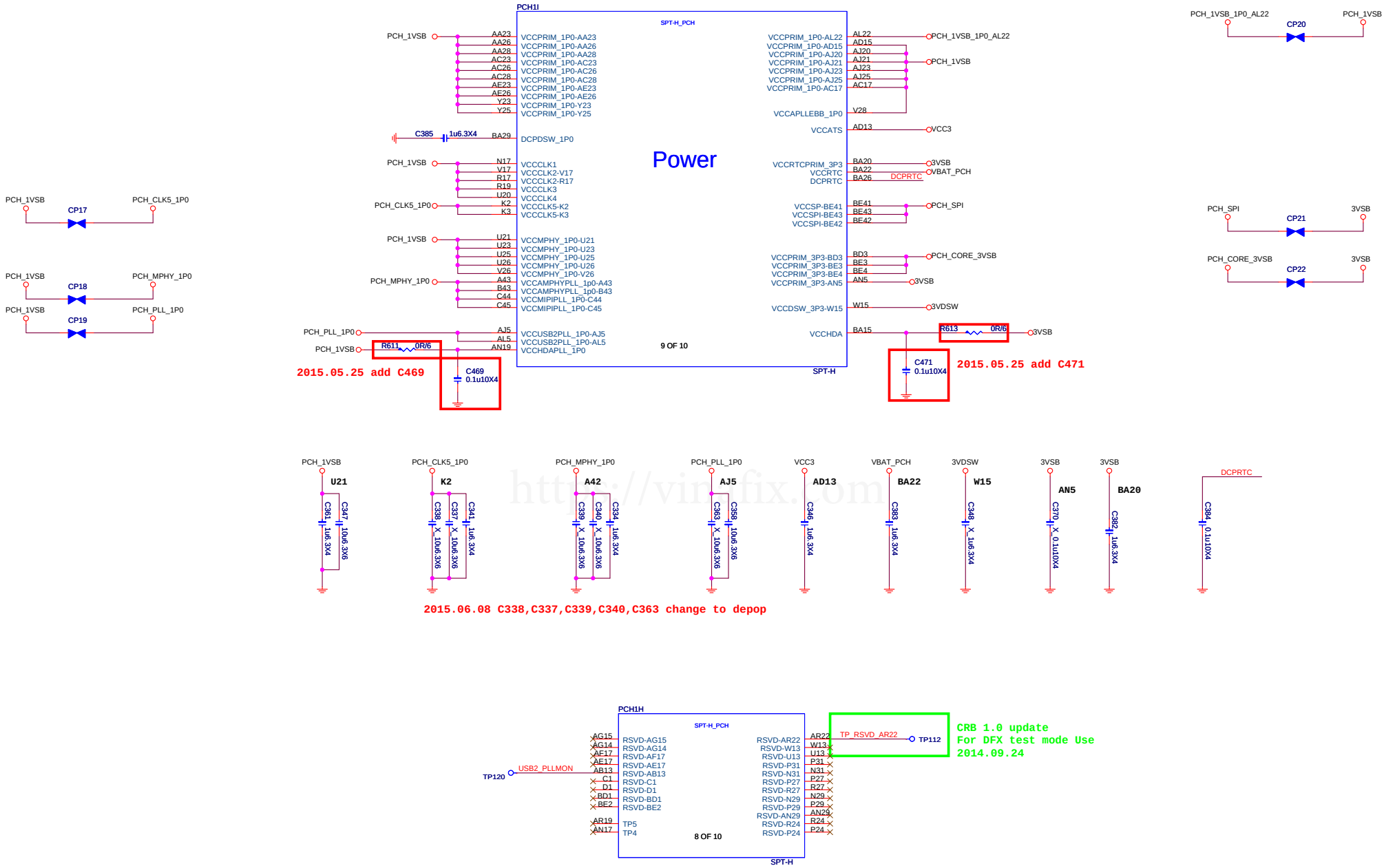
RTC Block

Close to PCH

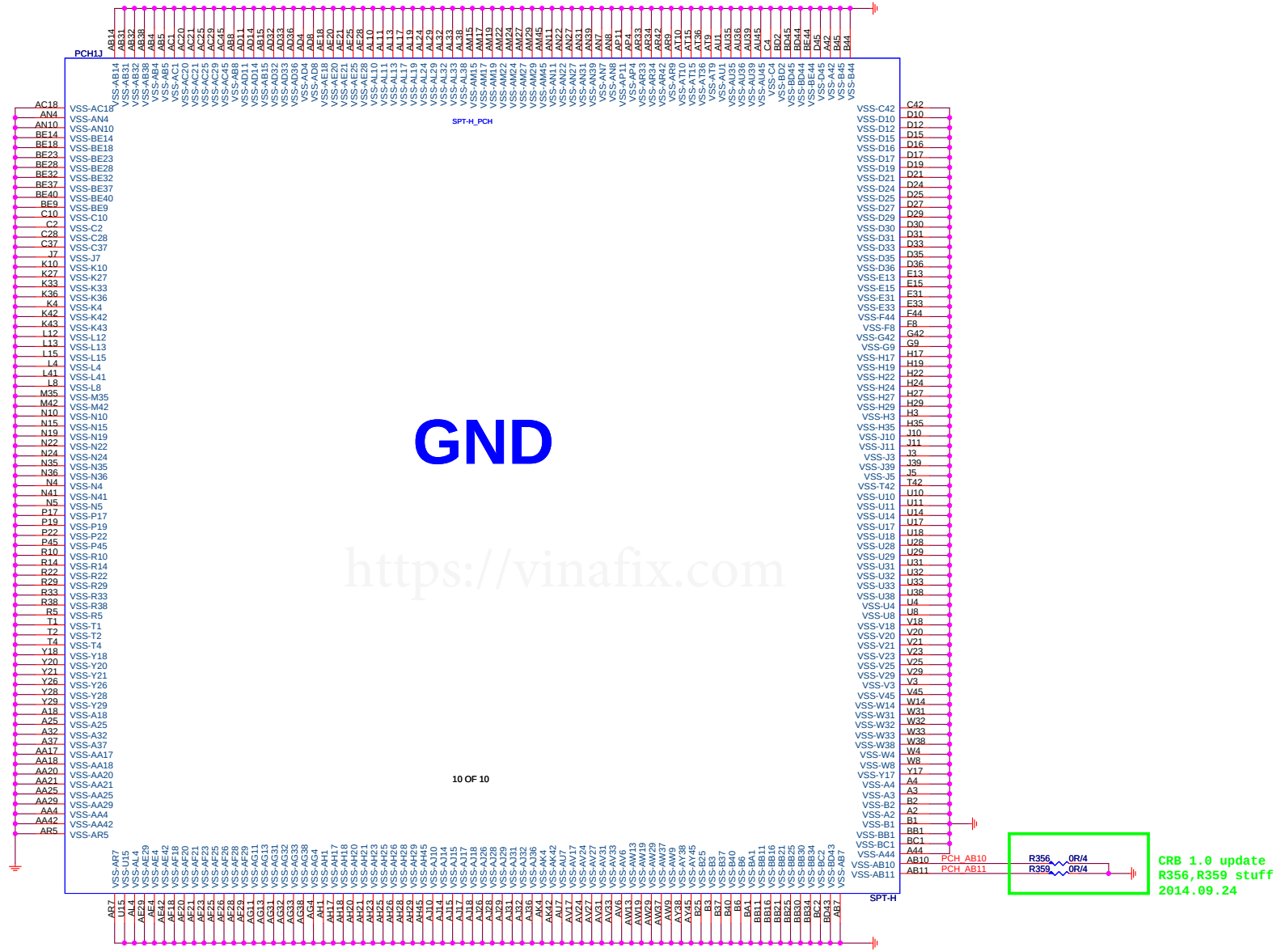




MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC
Rev: 10	
Date: Friday, August 07, 2015	Sheet 15 of 51

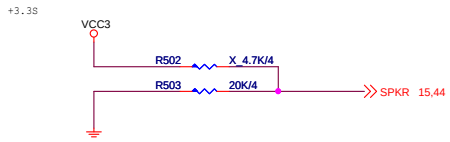


MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: PCH-Power	Rev: 10
Date: Friday, August 07, 2015	Sheet 16 of 51	



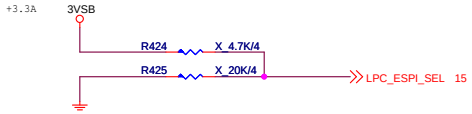
MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: PCH-GND
Rev: 10	
Date: Friday, August 07, 2015	Sheet 17 of 51

TOP Swap



Internal pull-down 20K is disabled after PLTRST#

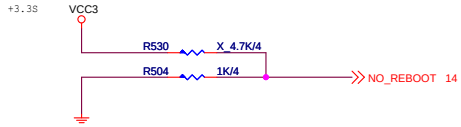
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

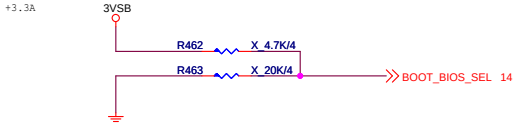
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

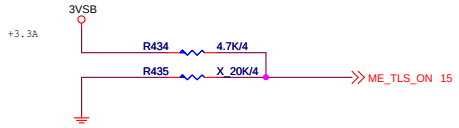
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

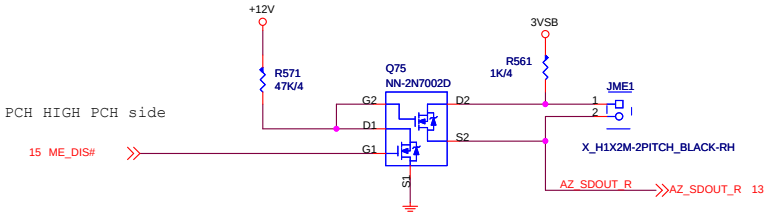
AMT and SBA with confidentiality



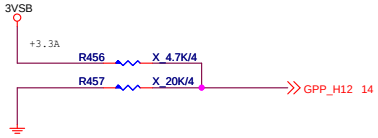
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE

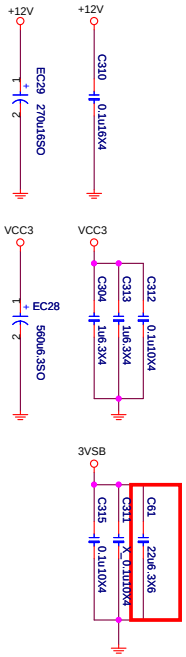


0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: PCH-Strap	Rev: 10
Date: Friday, August 07, 2015	Sheet 18 of 51	

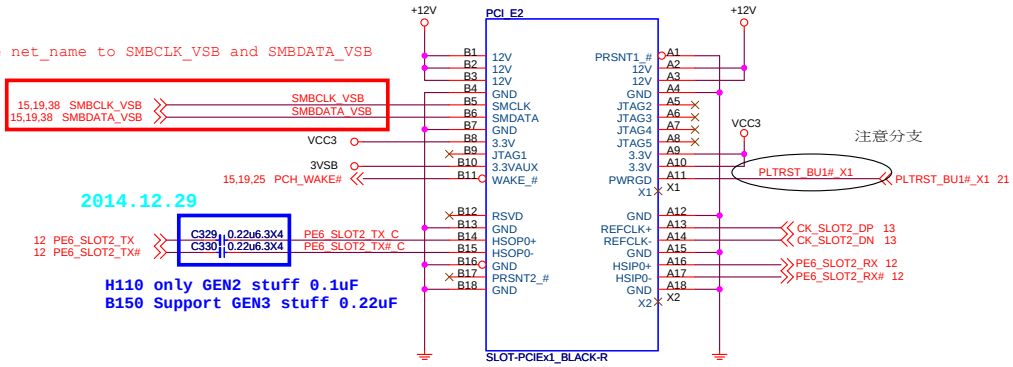
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB



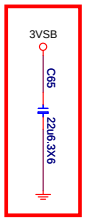
2015.6.16 add C61

MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: PCIE SLOT-CPU(X16)
Rev: 10	
Date: Friday, August 07, 2015	Sheet 19 of 51

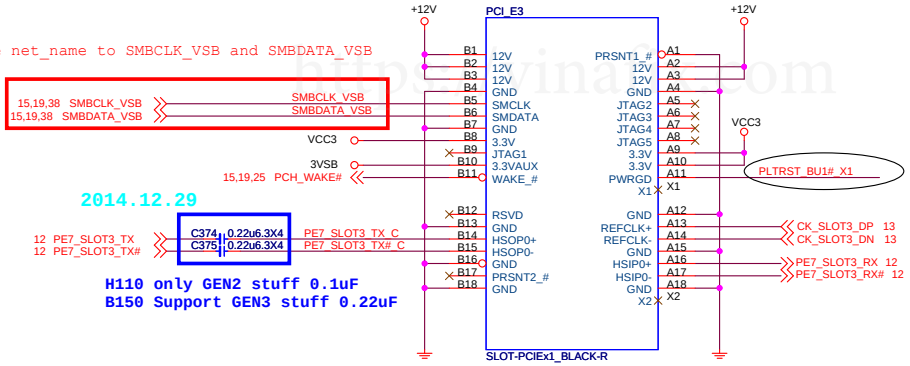
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB



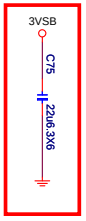
2015.6.16 add C65



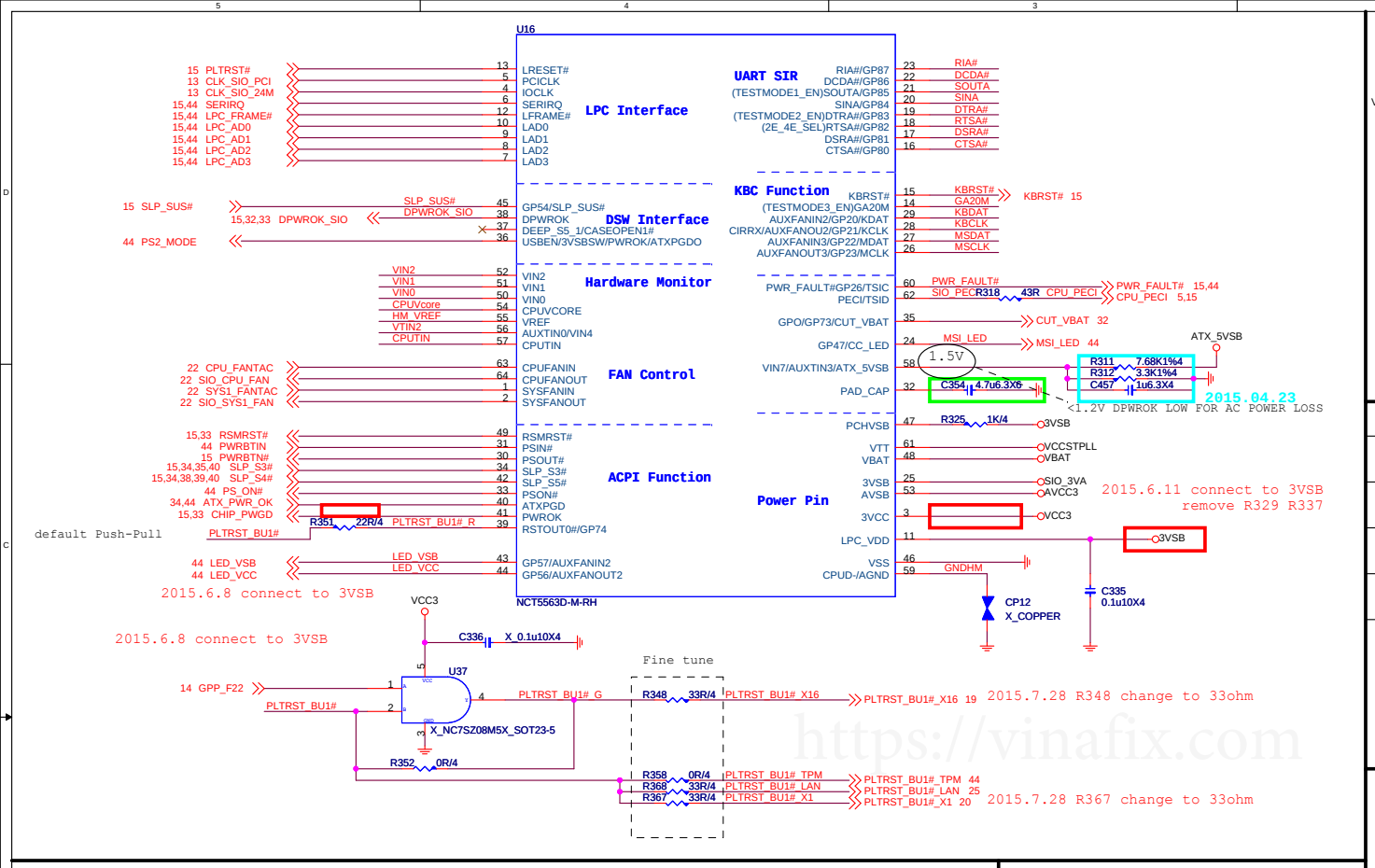
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB

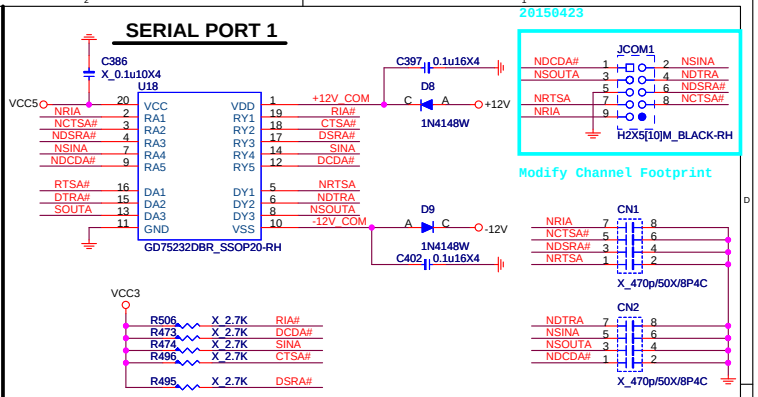


2015.6.16 add C75



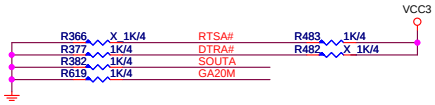
MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: PCIE SLOT-PCH(X1)	Rev: 10
Date: Friday, August 07, 2015	Sheet 20 of 51	

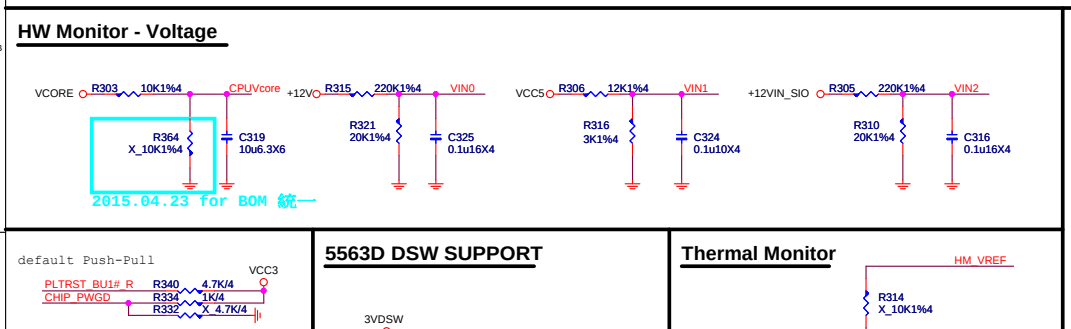




POWER ON STRAPPING PIN FOR NCT5563D

PIN	5563D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	24M_48M_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE

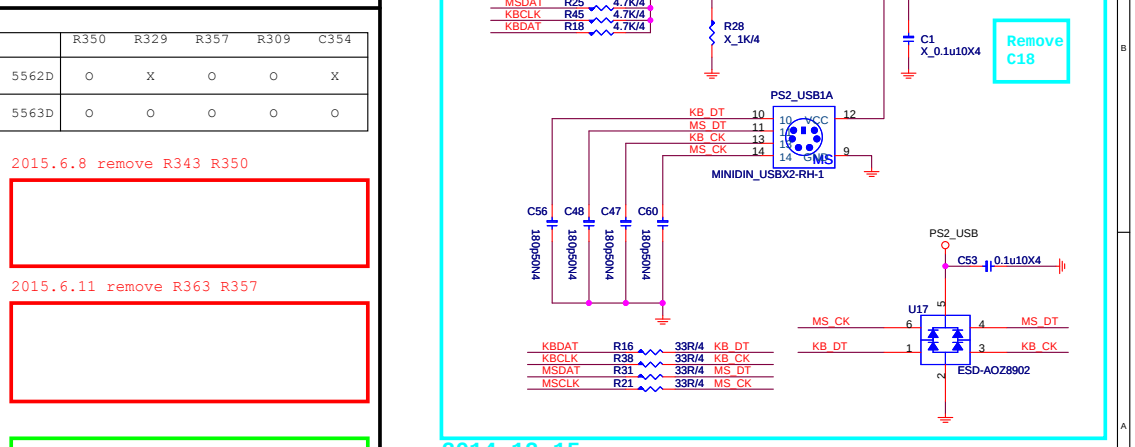


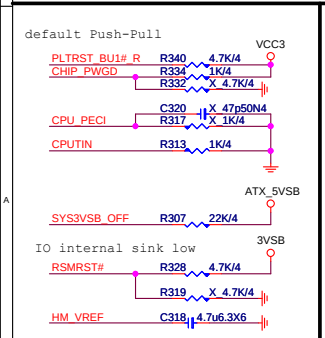


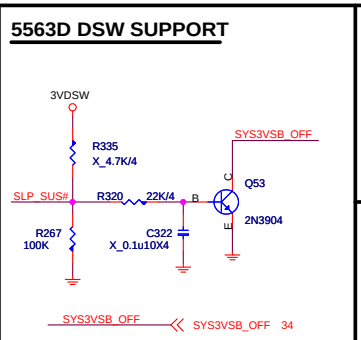
	R350	R329	R357	R309	C354
5562D	O	X	O	O	X
5563D	O	O	O	O	O

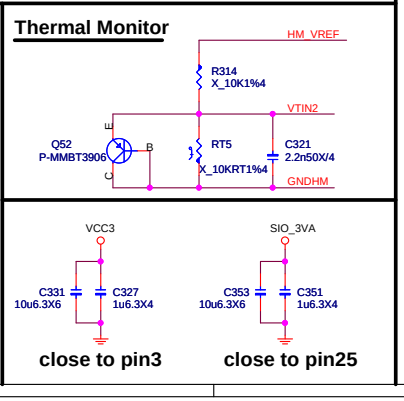
2015.6.8 remove R343 R350

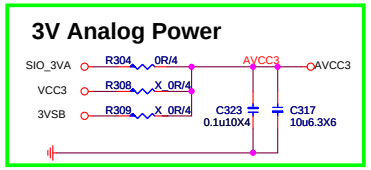
2015.6.11 remove R363 R357

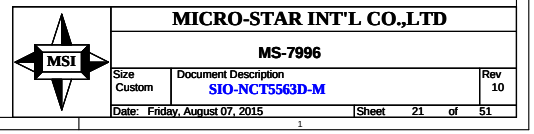




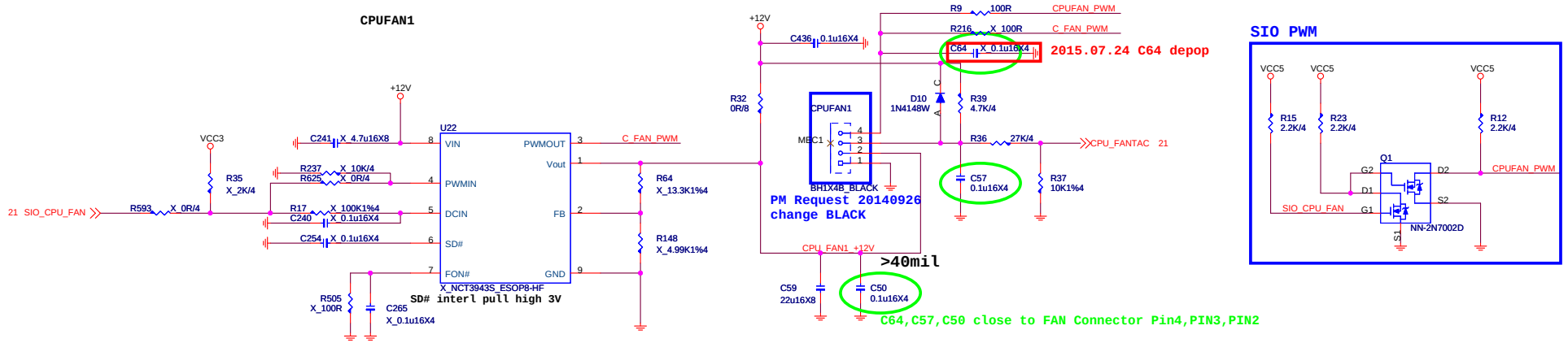








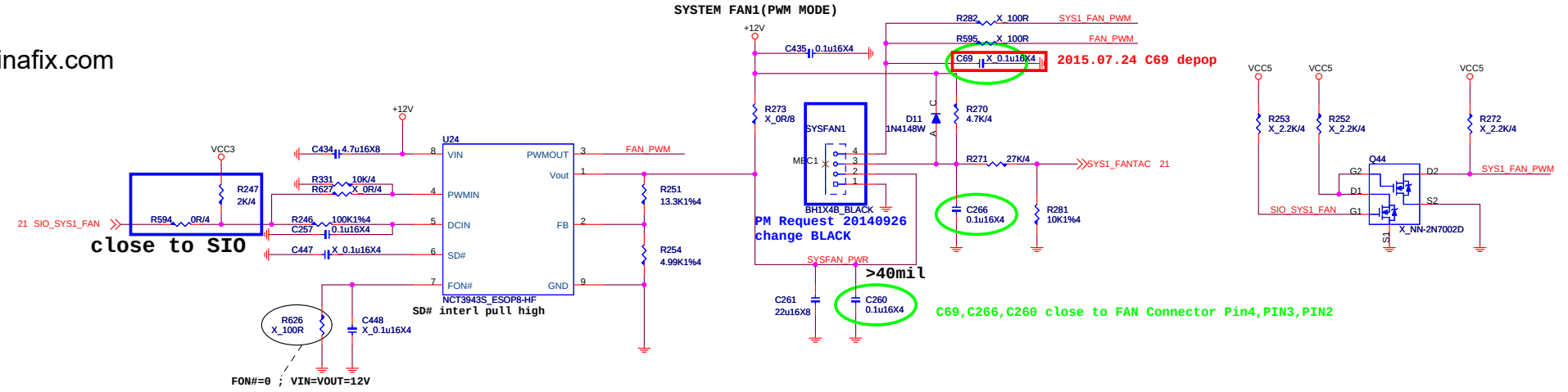
Type G : 4 PIN CPU FAN FROM SIO



CPUFAN_PWR_OFF
GPIO Control
Deafult GPI
If USE CUT POWER
1.OPEN DRAIN LOW:SD# LOW Active，CPUFAN(PIN2)= 0V
2.OPEN DRAIN : SD# Internal Pull high，CPUFAN(PIN2)=12V

Type H : 4 PIN SYS FAN FROM SIO

Vinafix.com



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7996	
Size: Custom	Document Description: FAN CONTROLLOR	Rev: 10
Date: Friday, August 07, 2015	Sheet 22 of 51	

Type B:
ALC892/887

2014.09.15

CA4 closed PIN25
CA3 closed PIN38
CA38 closed PIN38

11mA
3VSB
Closed Codec

CA28 10u6.3X6
CA18 0.1u10X4
CA30 0.1u10X4
CA14 22u6.3X8
CA31 10u6.3X6

SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass

2015.05.22 change to OSC

UA1

24 EAPD
13 AZ_SDOUT
13 AZ_SDIN0
13 AZ_SYNC
13 AZ_RST#
13 AZ_BITCLK
AZ_SDIN0

RA21 33R/4
2015.6.8 remove RA22

EAPD
SDIN0
EPAD/SPDIF-IN
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
Sense A
Sense B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
Sense C
JDREF
BEEP
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2
GPIO1/DMIC-DATA
DVSS
AVSS1
AVSS2

FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L

A_LOUT_R ECA3 100u10EL5 LOUT_R
A_LOUT_L ECA4 100u10EL5 LOUT_L
A_LINE_IN_R CA8 4.7u6.3X8 LINE_IN_R
A_LINE_IN_L CA9 4.7u6.3X8 LINE_IN_L
A_LINE2_R ECA1 100u10EL5 LINE2_R
A_LINE2_L ECA2 100u10EL5 LINE2_L
A_MIC1_R CA10 4.7u6.3X8 MIC1_R
A_MIC1_L CA11 4.7u6.3X8 MIC1_L
A_MIC2_R CA12 4.7u6.3X8 MIC2_R
A_MIC2_L CA13 4.7u6.3X8 MIC2_L

ALC887-VD2-CG-HF

CA22 X_10p50N4
CA24 10u6.3X6
REGREF
SENSE_A
SENSE_B
MIC1_V_R
MIC2_VREFO
MIC1_V_L
LINE2_VREFO
VREF_AUDIO
JDREF
45.8mA
LDOVDD
CA16 X_0.1u10X4
CA17 10u6.3X6
RA23 20K1%4
Closed Codec

CA29.CA30 close to Pin27

LIN_OUT
LOUT_R
LOUT_L
RA9 75R
RA12 75R
LOUT_RA
LOUT_LA
FRONT_JD
AUDIO1B
JACK-AUDIOX3F_PK/GR/BU-RH-13
DA1 ESD-SFI0402
DA2 ESD-SFI0402

LIN_IN
LINE_IN_R
LINE_IN_L
RA5 1K/4
RA7 1K/4
LINE_IN_RA
LINE_IN_LA
LINE1_JD
AUDIO1A
JACK-AUDIOX3F_PK/GR/BU-RH-13
CA3 100p50N4
CA4 100p50N4

2.2k for better recording quality

MIC1_V_L RA6 2.2K/4 MIC1_LA
MIC1_V_R RA2 2.2K/4 MIC1_RA
MIC1_R
MIC1_L
RA8 1K/4
RA3 1K/4
MIC1_RA
MIC1_LA
MIC1_JD
MIC1
AUDIO1C
JACK-AUDIOX3F_PK/GR/BU-RH-13
CA1 100p50N4
CA2 100p50N4

for rear I/O 6port:
887VD/892:1k

for rear I/O 3port:
887VD/892:75R

D LIN_IN
E LIN_OUT
F MIC1
N54-13F0271-K06

24 LOUT_LA
24 LOUT_RA
LOUT_LA
LOUT_RA
RA4 22K/4
RA1 22K/4

EMI
CA6 X_0.1u10X4
CA5 X_1000p50N4

CPA1 X_COPPER
CPA2 X_COPPER

MIC2_R RA28 75R F_MIC2_R
MIC2_L RA24 75R F_MIC2_L
LINE2_L RA34 75R F_LINE2_L
LINE2_R RA32 75R F_LINE2_R

DA8
LINE2_VREFO
S-BAT54A_SOT23
MIC2_VREFO
S-BAT54A_SOT23
DA4
R579 4.7K/4
R580 4.7K/4
R581 4.7K/4
R582 4.7K/4

F_MIC2_L
F_MIC2_R
F_LINE2_R
SENSE_B
F_LINE2_L
RA26 47R

DA5 ESD-SFI0402
DA6 ESD-SFI0402
DA7 ESD-SFI0402
DA9 ESD-SFI0402

JAUD1
MIC
GND
MICPWR
PRESENCE#
FLINE OUTR
LINE NEXT R
HPON
FLINE OUTL
LINE NEXT L
H2X5[8]M_BLACK-RH
MIC2_JD
LINE2_JD

CA35 1000p16X4
N31-2051411-H06
RA27 39.2K1%4
RA25 20K1%4

Close to Front panel
For HDA/AC97 front cable.

Closed Codec

SENSE_A
RA17 5.1K1%4 FRONT_JD
RA18 10K1%4 LINE1_JD
RA16 20K1%4 MIC1_JD

0R for cost down
ATX_5VSB
LA1 0R/8
LDOVDD
DA3 X_TVS
CA32 0.1u10X4
CA33 10u6.3X6

CA23,CA24 close to LA1

24 F_LINE2_L
24 F_LINE2_R
F_LINE2_L
F_LINE2_R
RA33 22K/4
RA31 22K/4

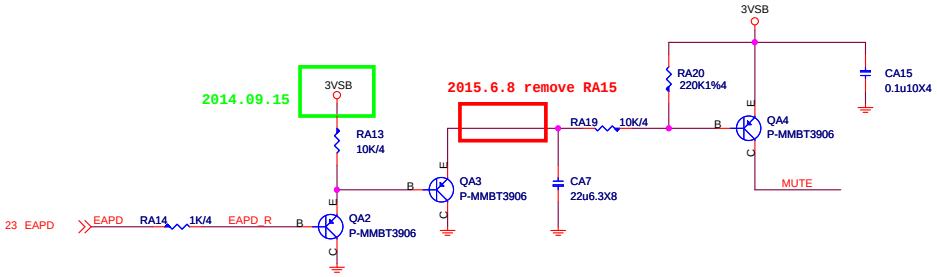
Varister --> cap for cost down

D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: AUDIO - ALC892/887	Rev: 10
Date: Friday, August 07, 2015	Sheet 23 of 51	

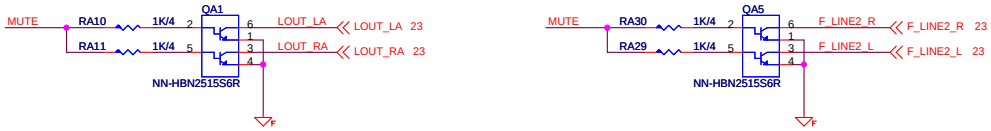
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



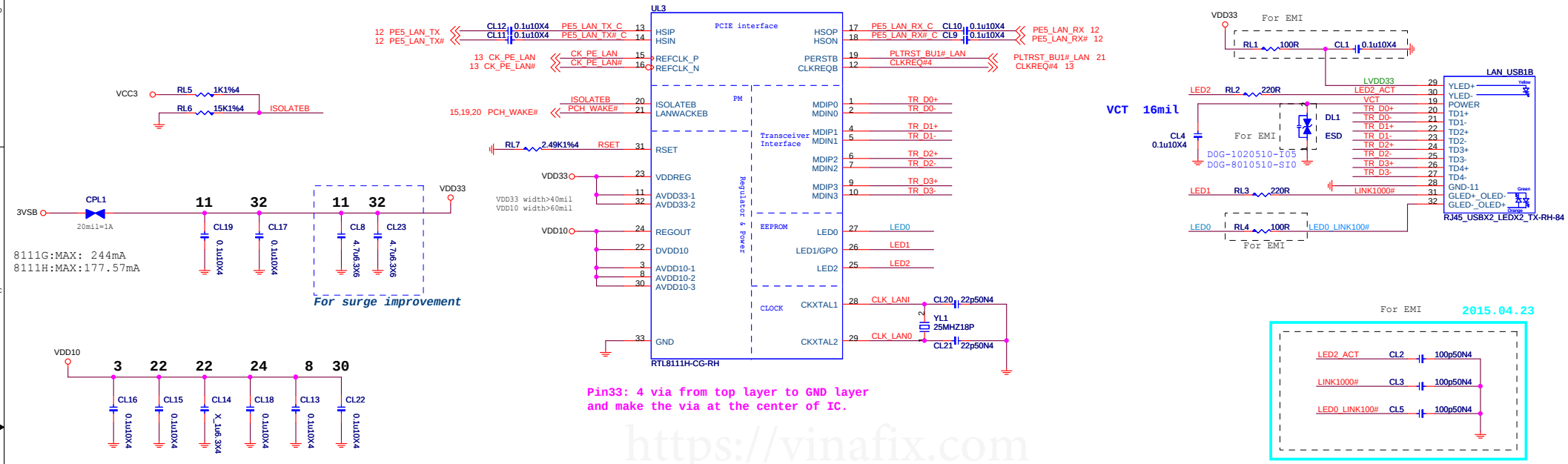
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: AUDIO - depop circuit	Rev: 10
Date: Friday, August 07, 2015	Sheet 24 of 51	

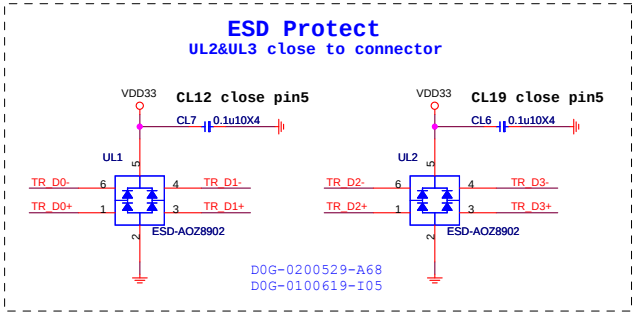
RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

LAN Connector



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-STAR INT'L CO.,LTD

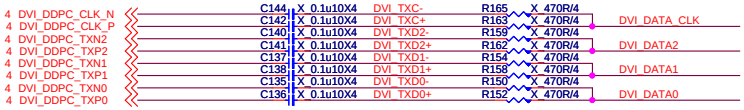
MS-7996

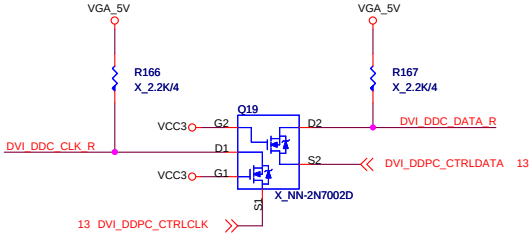
Size: Custom | Document Description: LAN - RTL8111H | Rev: 10

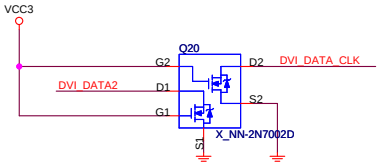
Date: Friday, August 07, 2015 | Sheet 25 of 51

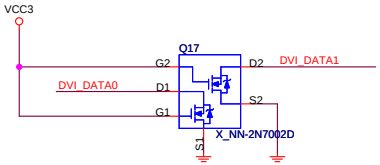
DVI level shifter

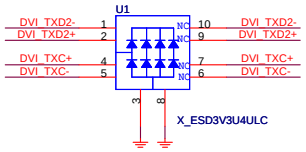
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

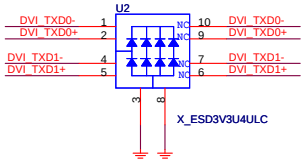


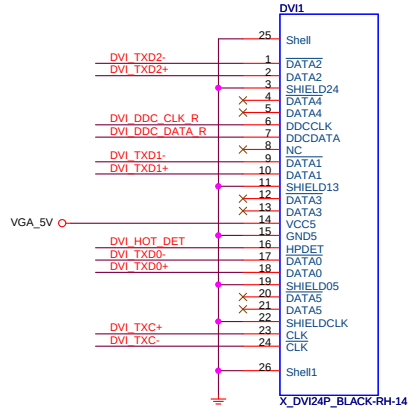


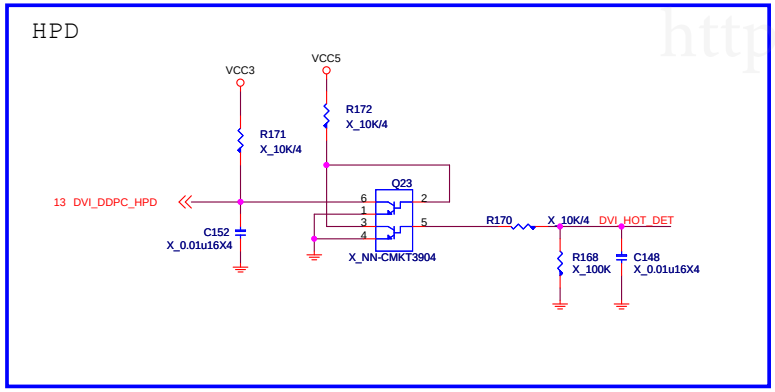


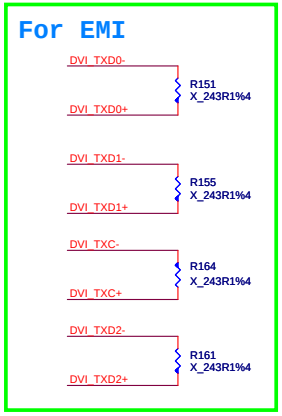


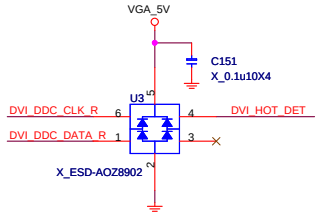


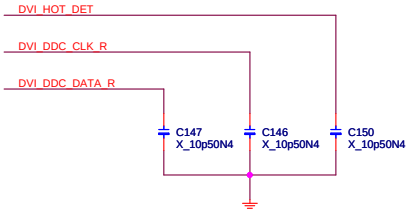






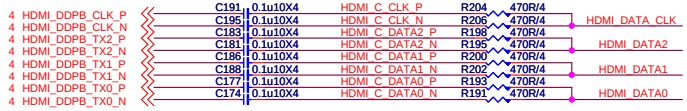


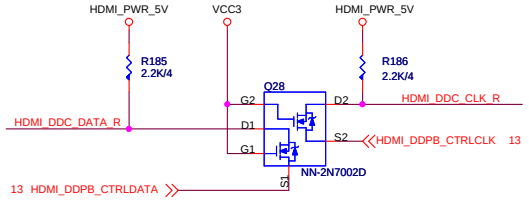


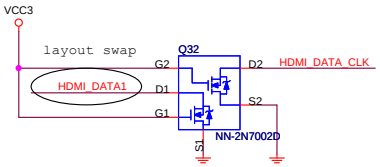


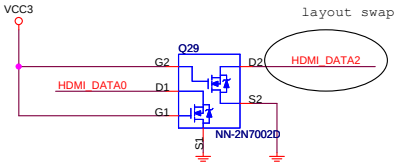
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7996	
Size: Custom	Document Description: DVI	Rev: 10
Date: Friday, August 07, 2015	Sheet 26 of 51	

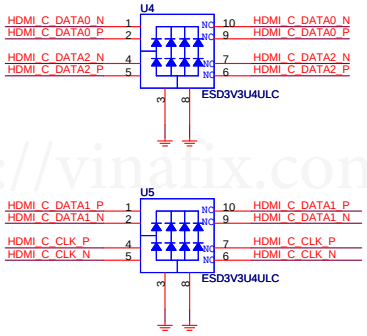
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

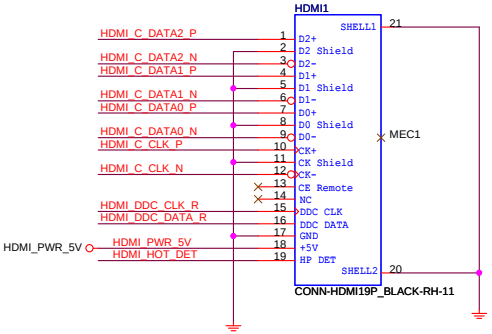


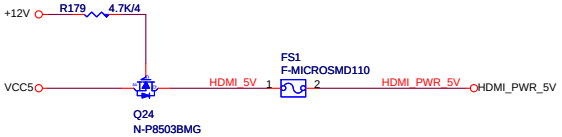


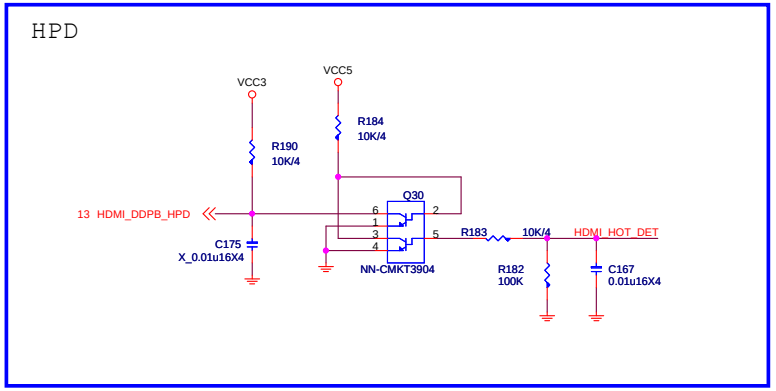


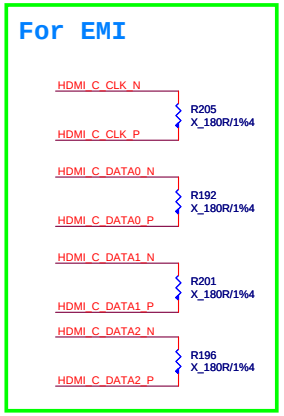


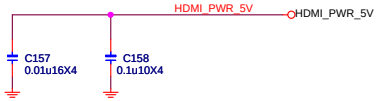


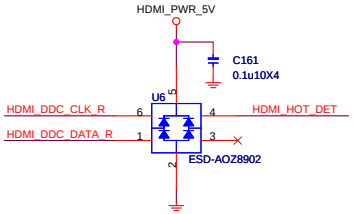












MICRO-STAR INT'L CO.,LTD

MS-7996

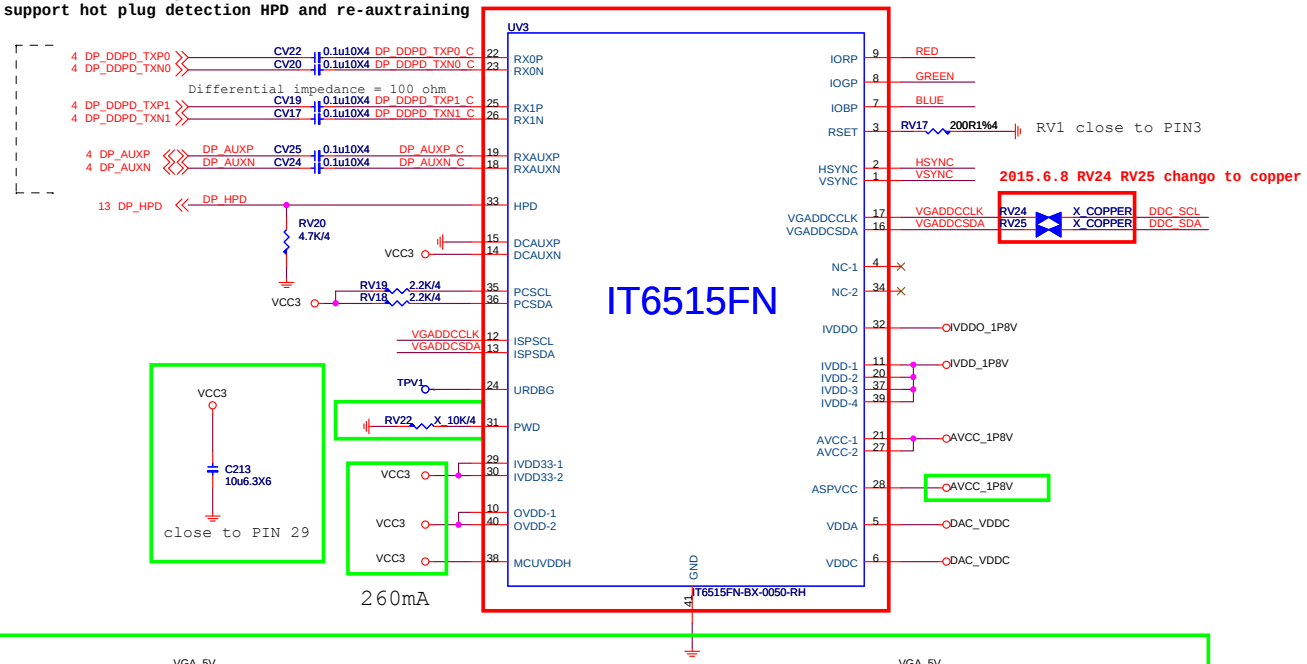
Size	Document Description	Rev
Custom	HDMI Connector	10

Date: Friday, August 07, 2015 | Sheet 27 of 51

Note:

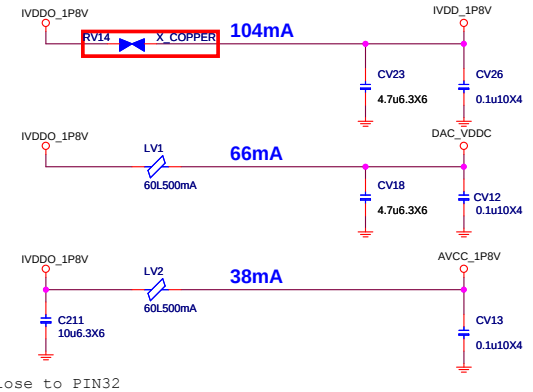
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

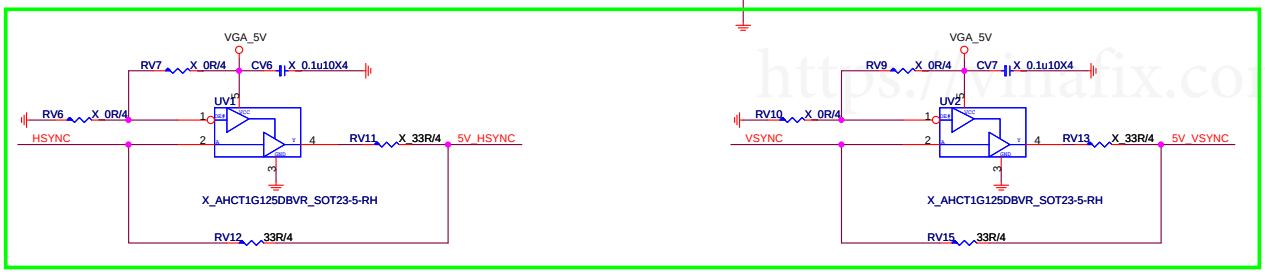
2015.05.22 UV3 change to B0B-6515F1C-I15

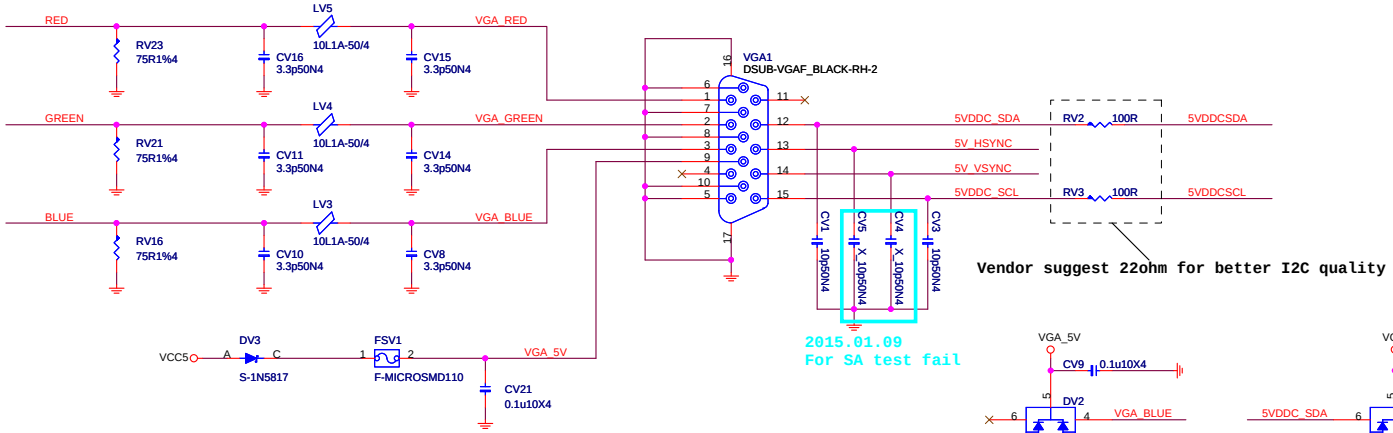


Remove

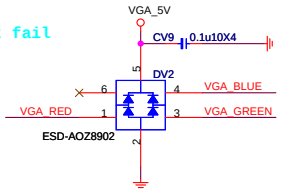
2015.6.8 RV14 chango to copper

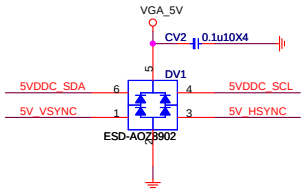


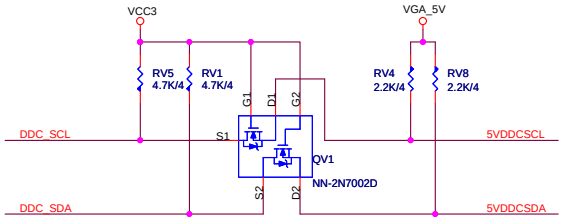




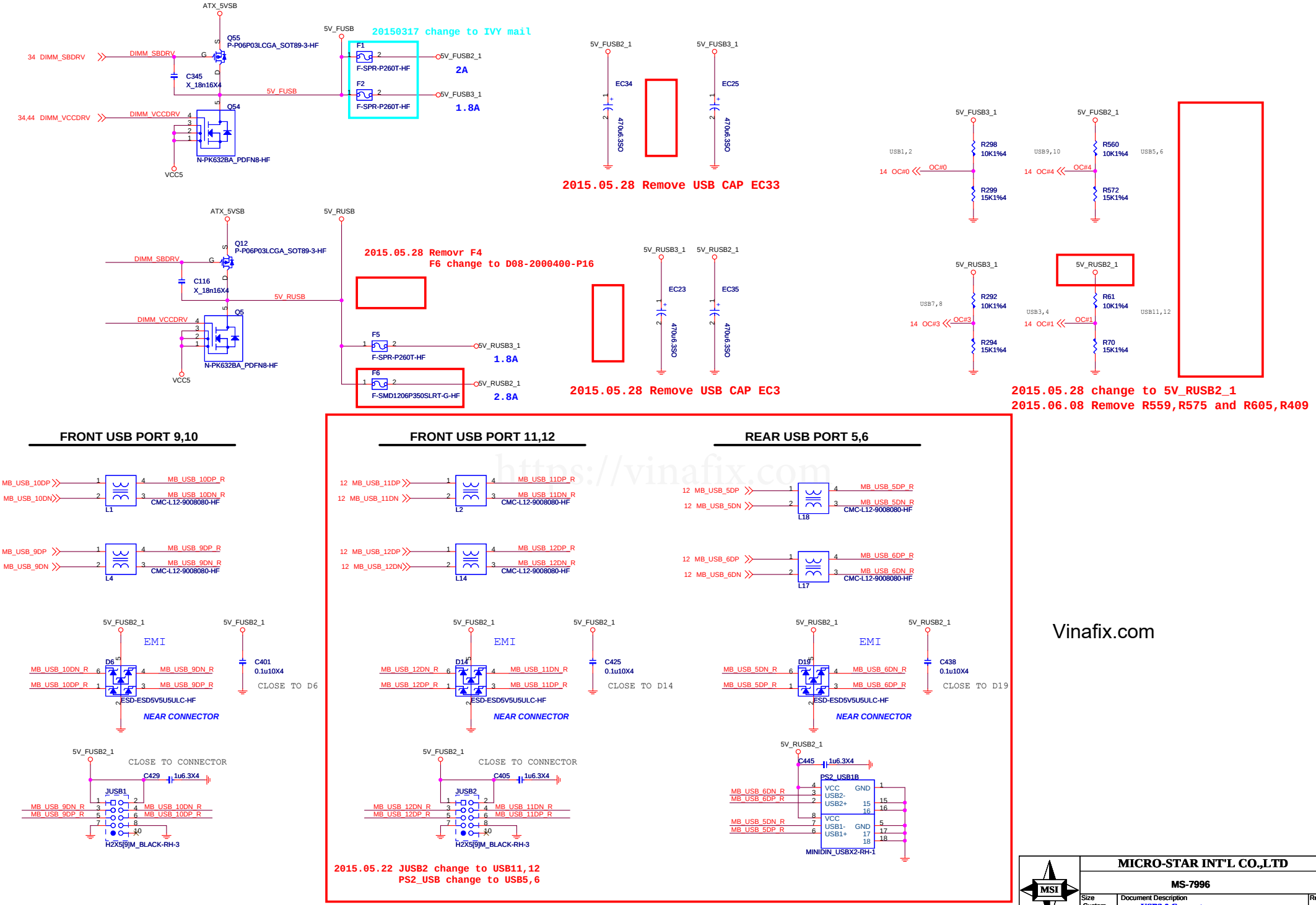
2015.01.09
For SA test fail

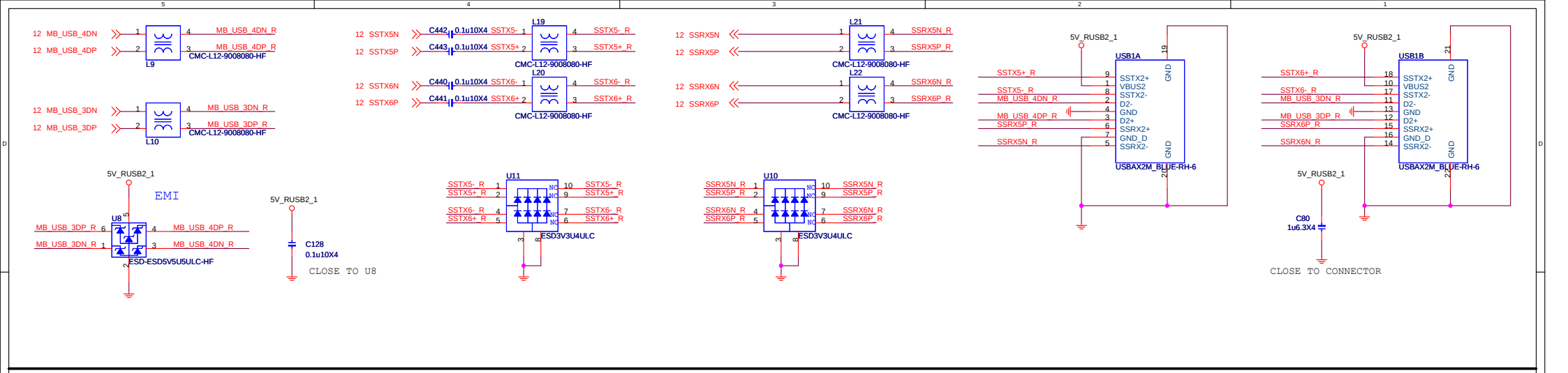


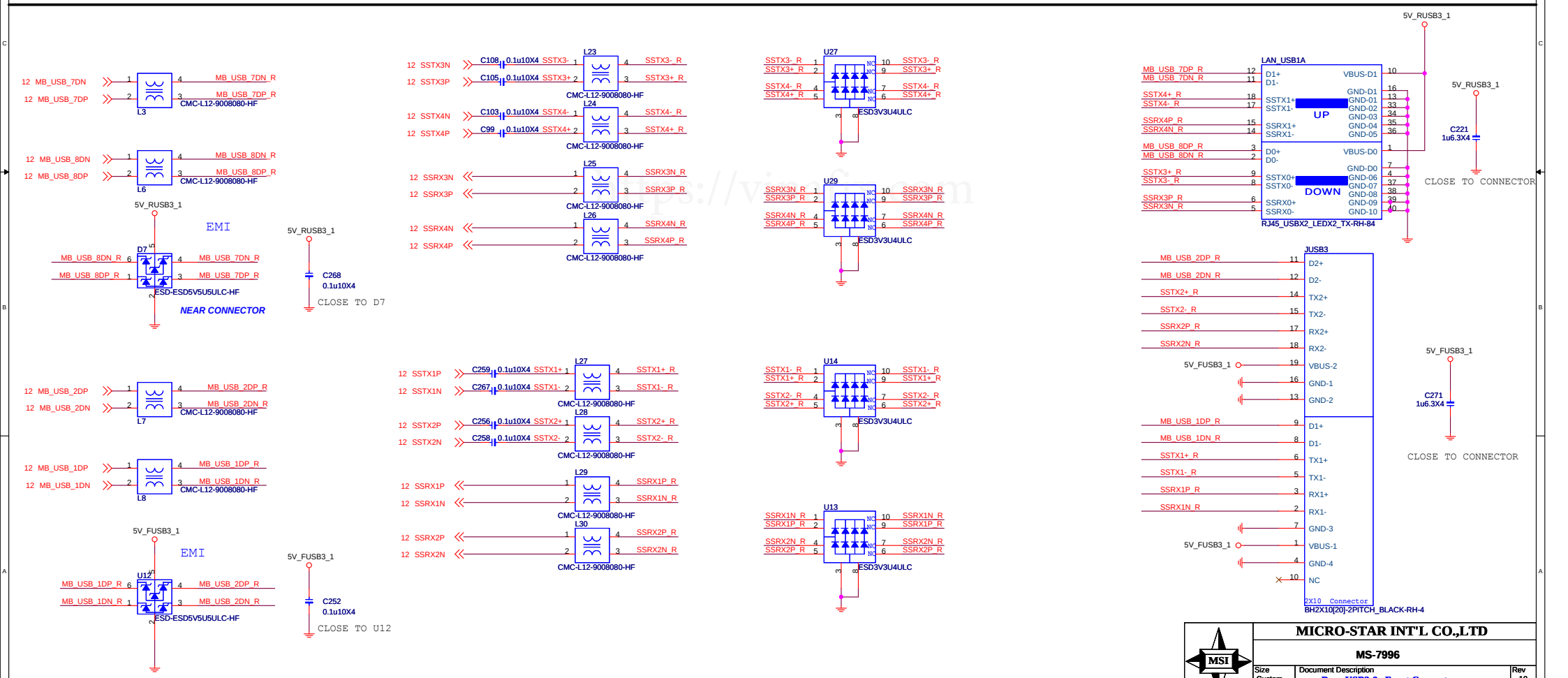




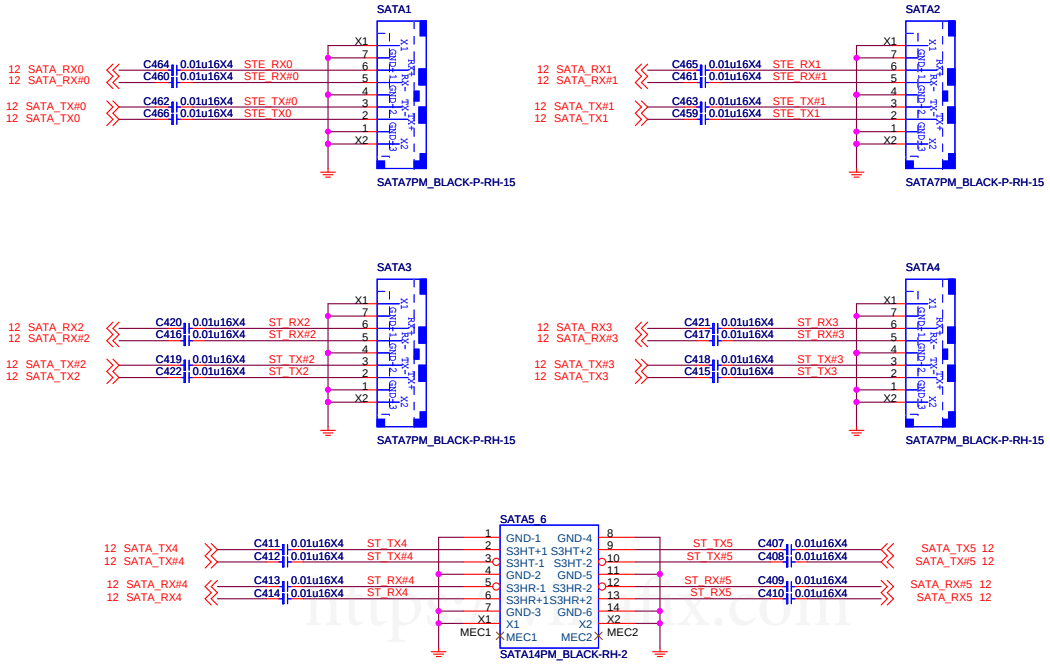
MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: VGA - ITE6515
Rev: 10	
Date: Friday, August 07, 2015	Sheet 28 of 51


ATX_5VSB
5V_FUSB
20150317 change to IVY mail
34 DIMM_SBDRV
DIMM_SBDRV
Q55
P-P06P03LCGA_SOT89-3-HF
C345
X_18n16X4
F1
F-SPR-P260T-HF
F2
F-SPR-P260T-HF
5V_FUSB2_1
2A
5V_FUSB3_1
1.8A
34,44 DIMM_VCCDRV
DIMM_VCCDRV
Q54
N-PK632BA_PDFN8-HF
VCC5
5V_FUSB2_1
5V_FUSB3_1
EC34
EC25
470u6.3SO
2015.05.28 Remove USB CAP EC33
5V_FUSB3_1
5V_FUSB2_1
USB1,2
USB9,10
USB5,6
14 OC#0
OC#0
R298
10K1%4
R299
15K1%4
14 OC#4
OC#4
R560
10K1%4
R572
15K1%4
ATX_5VSB
5V_RUSB
DIMM_SBDRV
Q12
P-P06P03LCGA_SOT89-3-HF
C116
X_18n16X4
5V_RUSB
DIMM_VCCDRV
Q5
N-PK632BA_PDFN8-HF
VCC5
2015.05.28 Removr F4
F6 change to D08-2000400-P16
F5
F-SPR-P260T-HF
5V_RUSB3_1
1.8A
F6
F-SMD1206P350SLRT-G-HF
5V_RUSB2_1
2.8A
5V_RUSB3_1
5V_RUSB2_1
EC23
EC35
470u6.3SO
2015.05.28 Remove USB CAP EC3
5V_RUSB3_1
5V_RUSB2_1
USB7,8
USB3,4
USB11,12
14 OC#3
OC#3
R292
10K1%4
R294
15K1%4
14 OC#1
OC#1
R61
10K1%4
R70
15K1%4
2015.05.28 change to 5V_RUSB2_1
2015.06.08 Remove R559,R575 and R605,R409
FRONT USB PORT 9,10
12 MB_USB_10DP
12 MB_USB_10DN
MB_USB_10DP_R
MB_USB_10DN_R
CMC-L12-9008080-HF
L1
12 MB_USB_9DP
12 MB_USB_9DN
MB_USB_9DP_R
MB_USB_9DN_R
L4
5V_FUSB2_1
EMI
D6
MB_USB_10DN_R
MB_USB_10DP_R
MB_USB_9DN_R
MB_USB_9DP_R
ESD-ESD5V5U5ULC-HF
NEAR CONNECTOR
C401
0.1u10X4
CLOSE TO D6
CLOSE TO CONNECTOR
C429
1u6.3X4
JUSB1
H2X5[9]M_BLACK-RH-3
FRONT USB PORT 11,12
12 MB_USB_11DP
12 MB_USB_11DN
MB_USB_11DP_R
MB_USB_11DN_R
L2
12 MB_USB_12DP
12 MB_USB_12DN
MB_USB_12DP_R
MB_USB_12DN_R
L14
D14
C425
CLOSE TO D14
C405
JUSB2
2015.05.22 JUSB2 change to USB11,12
PS2_USB change to USB5,6
REAR USB PORT 5,6
12 MB_USB_5DP
12 MB_USB_5DN
MB_USB_5DP_R
MB_USB_5DN_R
L18
12 MB_USB_6DP
12 MB_USB_6DN
MB_USB_6DP_R
MB_USB_6DN_R
L17
5V_RUSB2_1
D19
C438
CLOSE TO D19
C445
PS2_USB1B
MINIDIN_USBX2-RH-1
https://vinafix.com
Vinafix.com
MICRO-STAR INT'L CO.,LTD
MS-7996
Size
Custom
Document Description
USB2.0 Connector
Rev
10
Date: Friday, August 07, 2015
Sheet 29 of 51





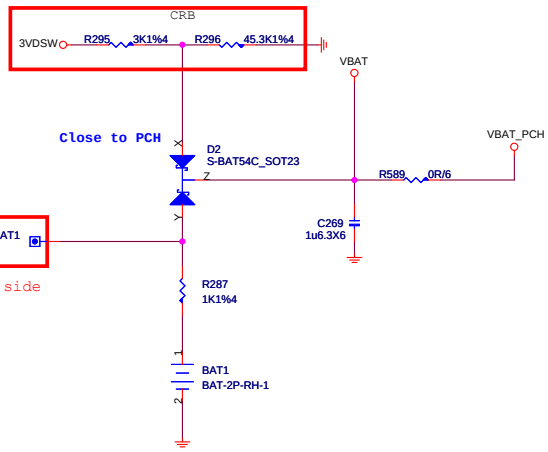
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7996	
Size: Custom	Document Description: Rear USB3 & Front Connector	Rev: 10
Date: Friday, August 07, 2015	Sheet 30 of 51	

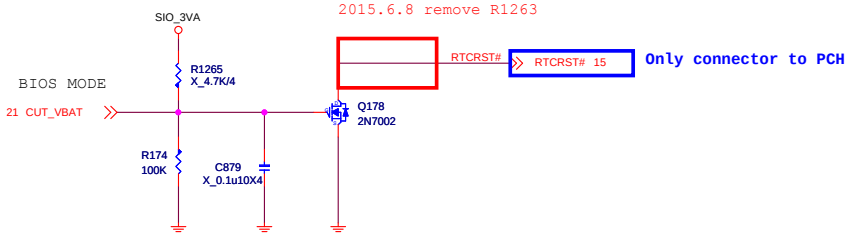


MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: SATA connector	Rev: 10
Date: Friday, August 07, 2015	Sheet 31 of 51	

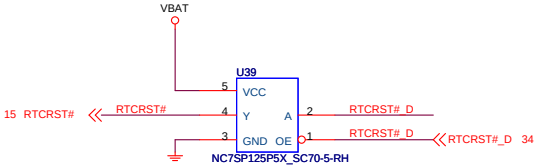
CUT_VBAT

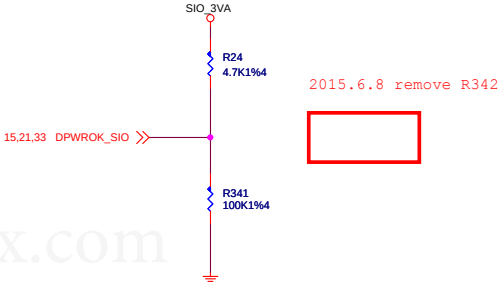
2015.7.20 R295,R296 change to POP

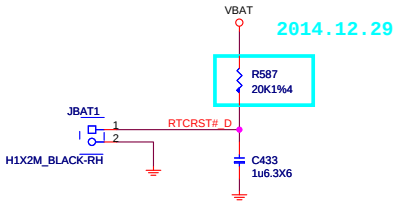


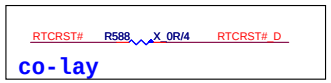


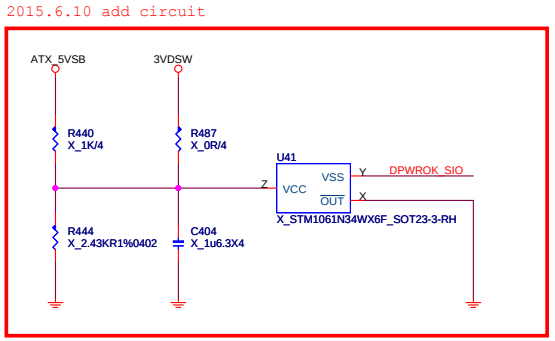
tri-state		
INPUT		outout pin4
PIN1	PIN2	
L	H	H
L	L	L
H	X	Z









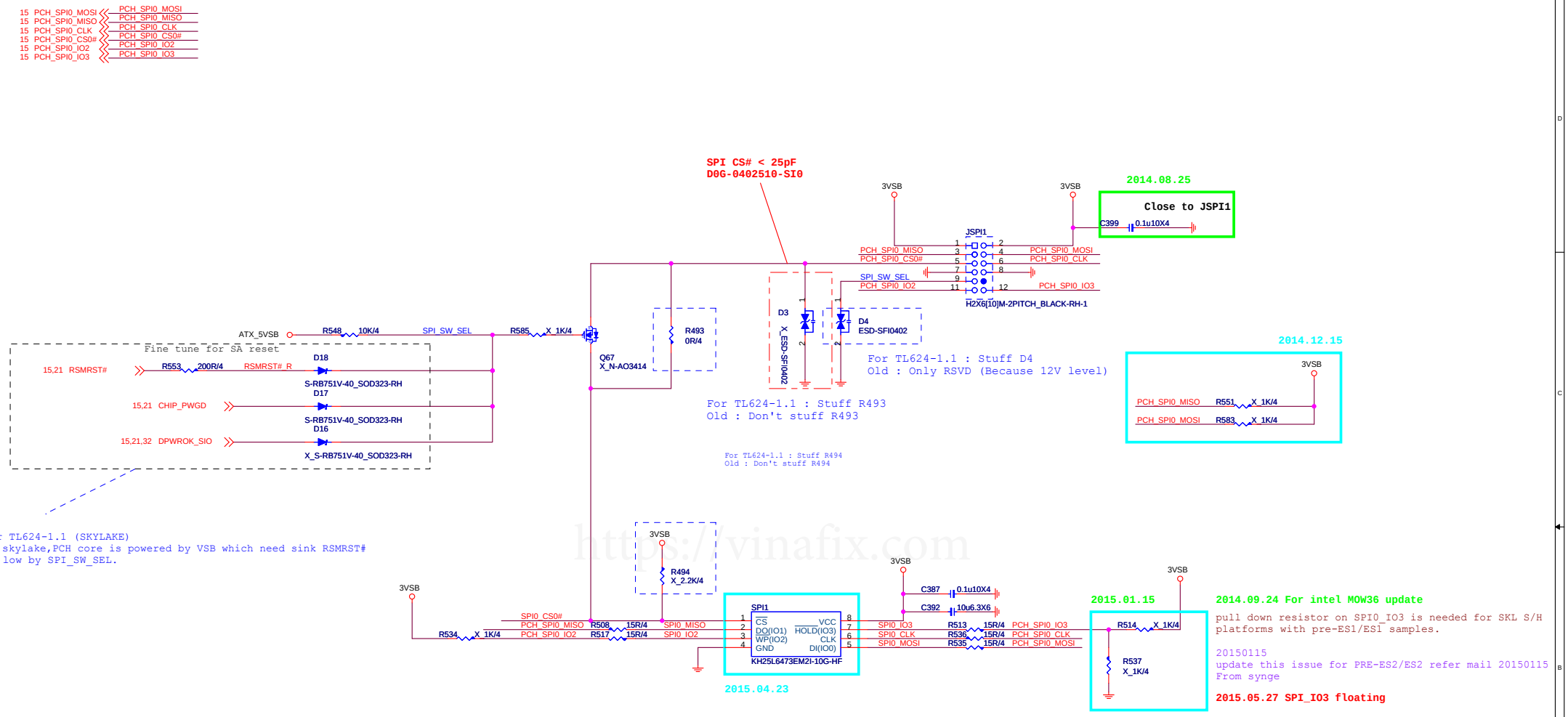


MICRO-STAR INT'L CO.,LTD

MS-7996

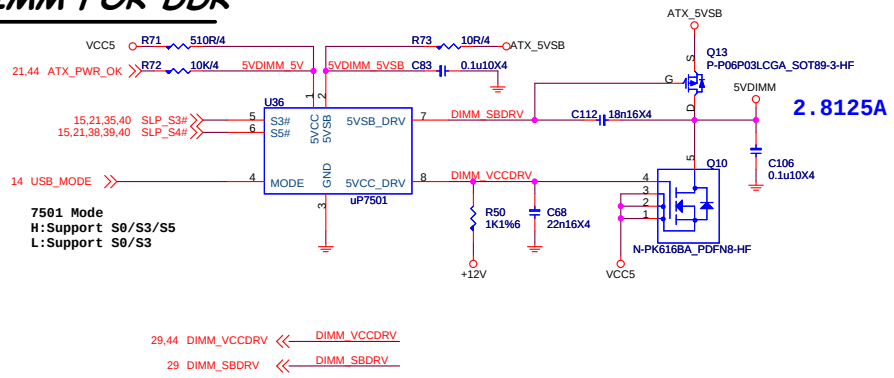
Size: Custom | Document Description: CUT_VABT circuit teknisi indonesia | Rev: 10

Date: Friday, August 07, 2015 | Sheet 32 of 51

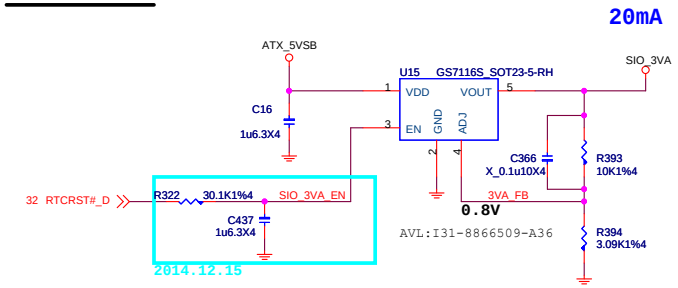


MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: BIOS ROM
Rev: 10	
Date: Friday, August 07, 2015	Sheet 33 of 51

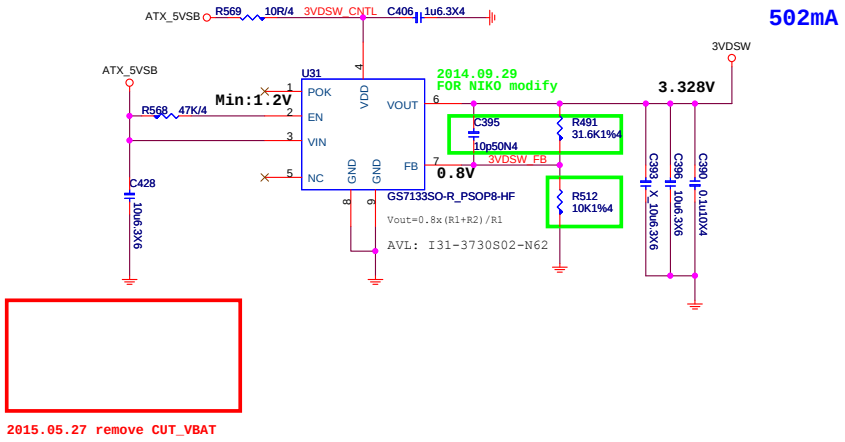
5VDIMM FOR DDR



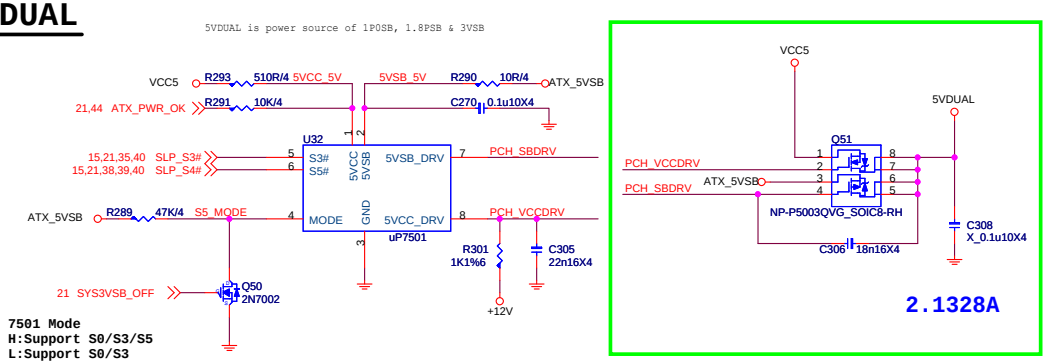
SIO_3VA

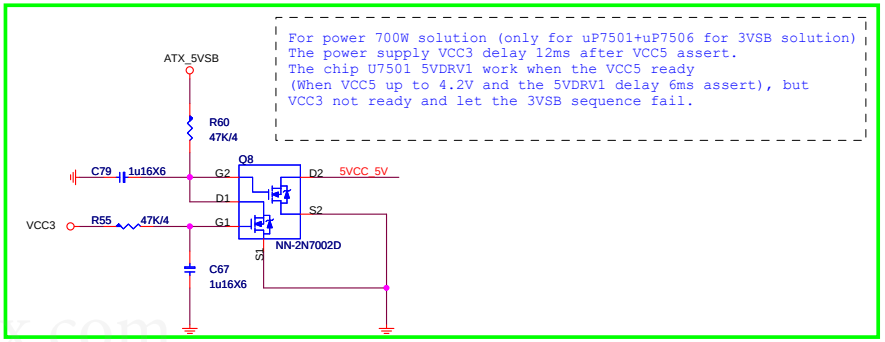


3VDSW

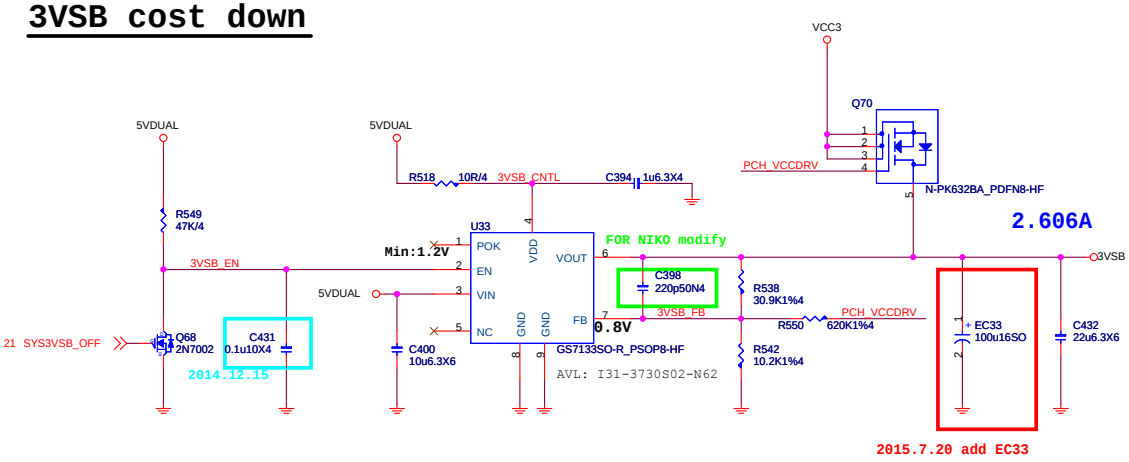


5VDUAL

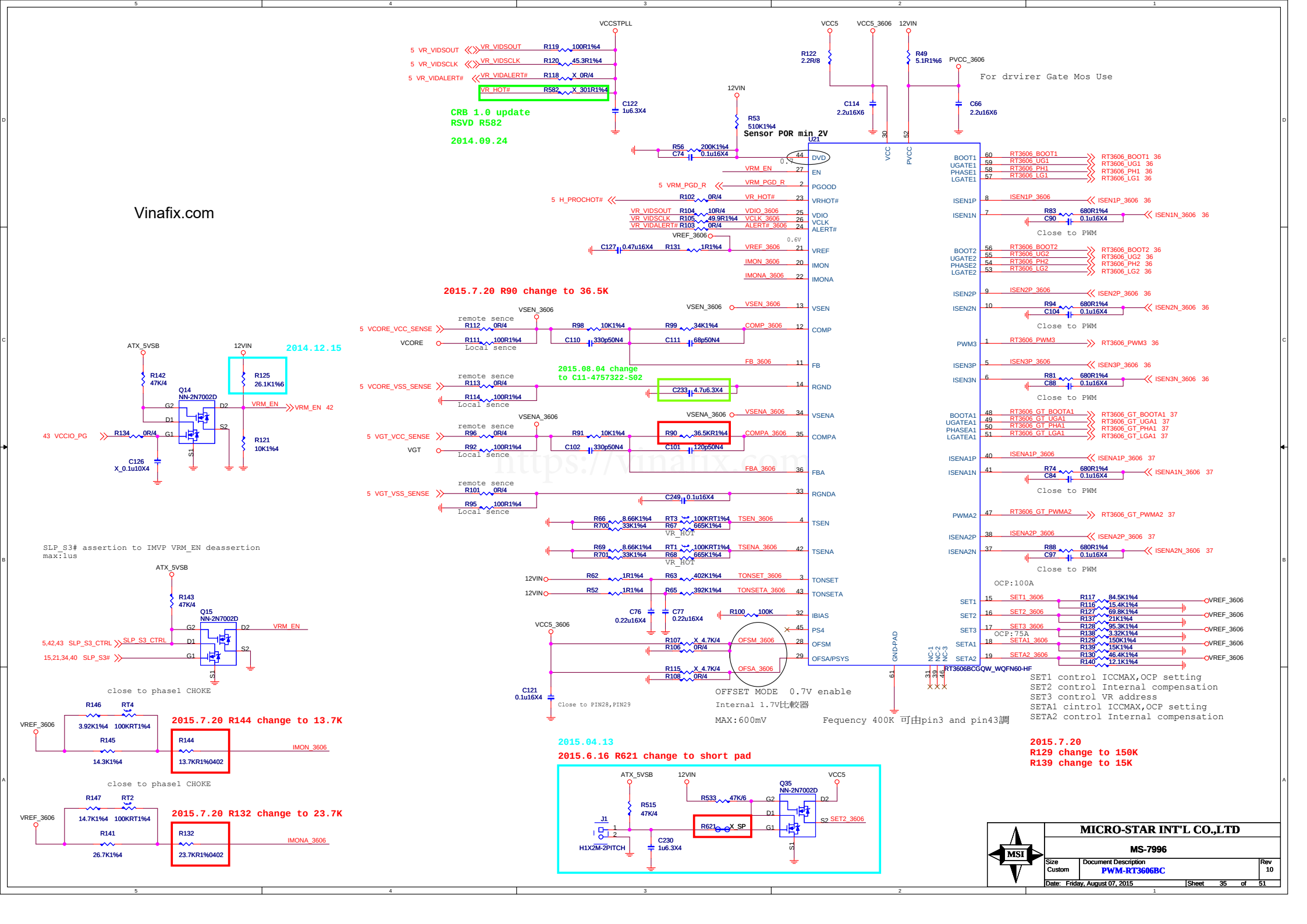


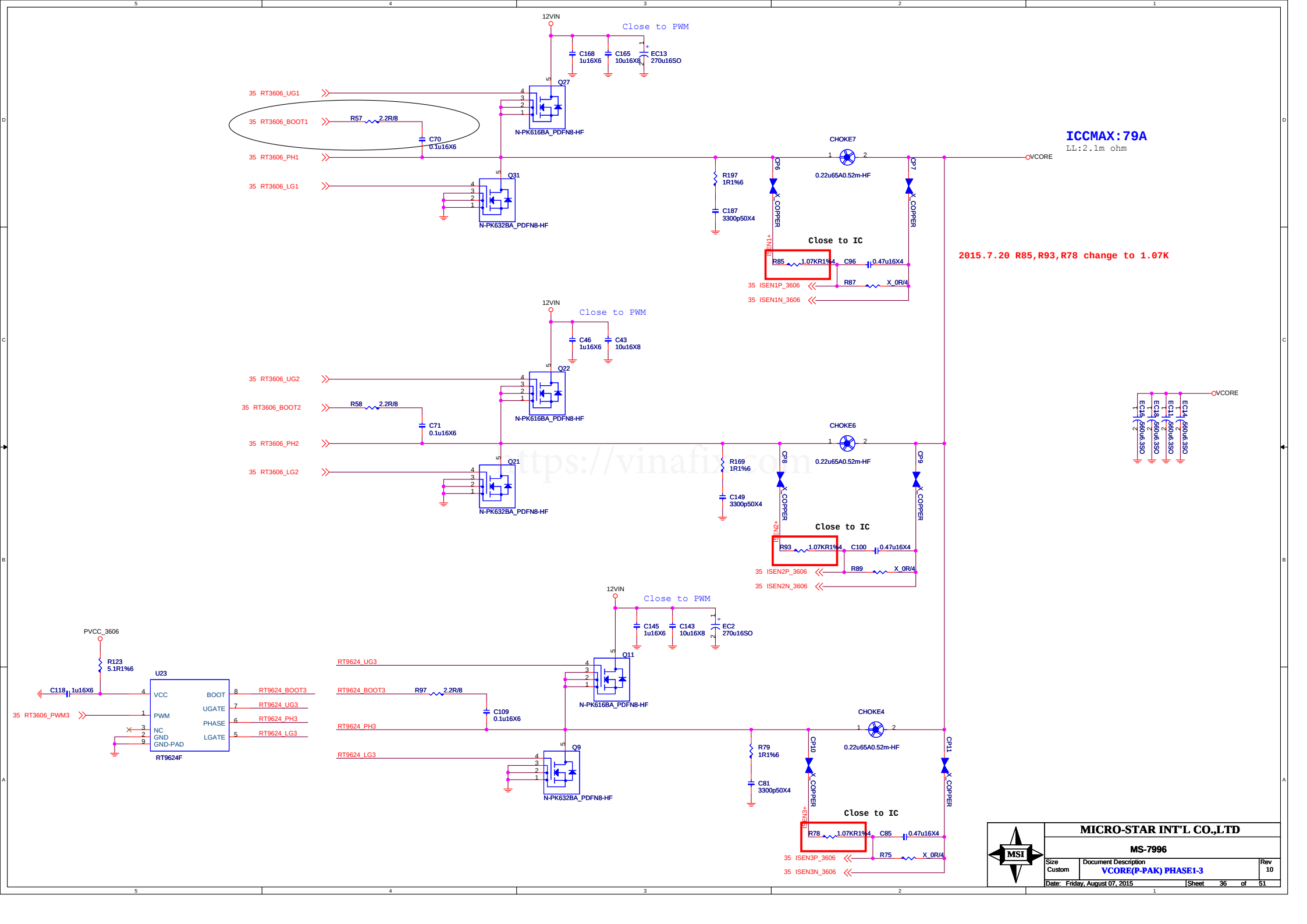


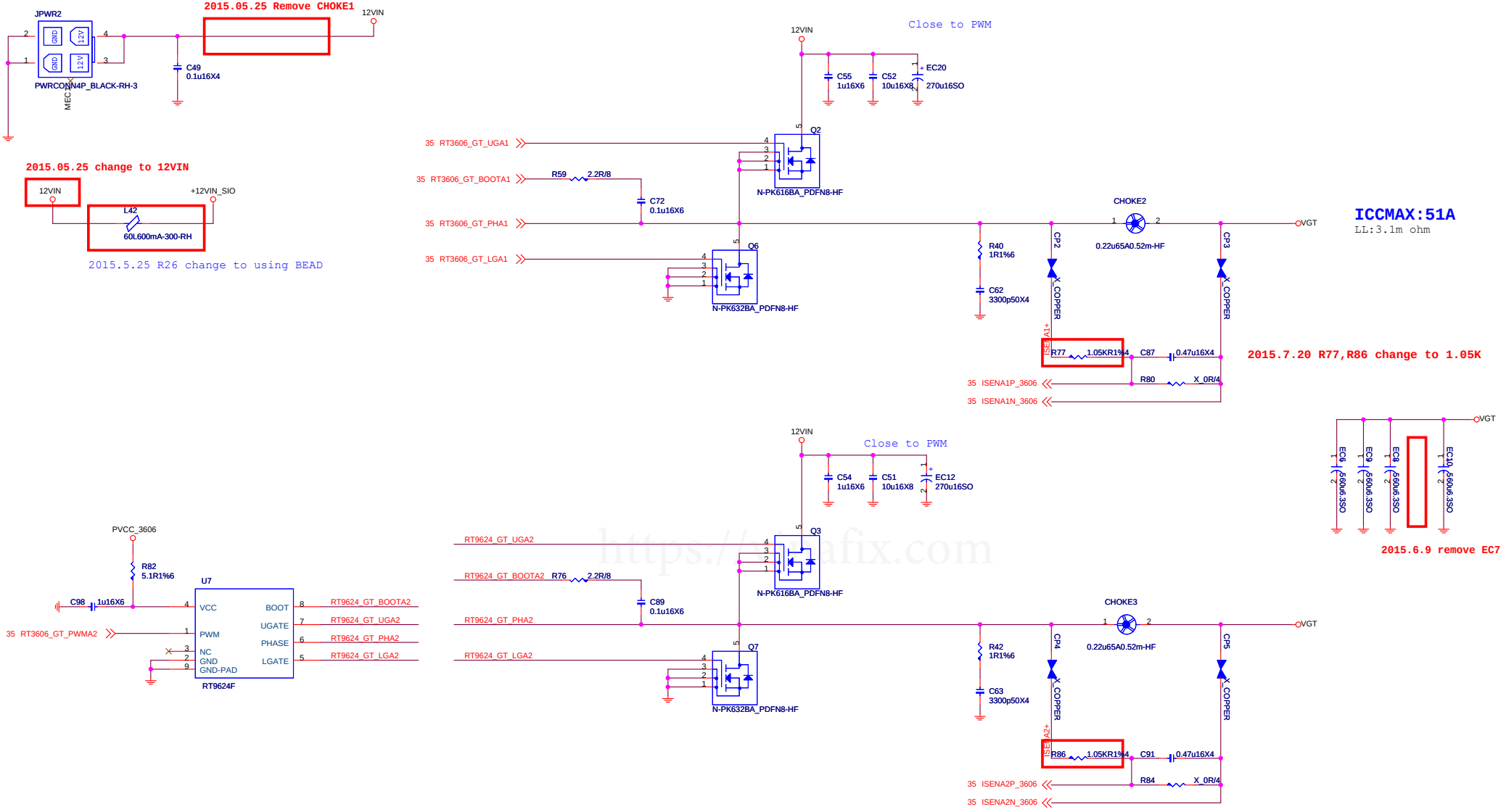
3VSB cost down



MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: ACPI CONTROLLER	Rev: 10
Date: Friday, August 07, 2015	Sheet 34 of 51	


Vinafix.com
CRB 1.0 update
RSVD R582
2014.09.24
Sensor POR min_2V
For drvirer Gate Mos Use
2015.7.20 R90 change to 36.5K
2014.12.15
2015.08.04 change to C11-4757322-S02
SLP_S3# assertion to IMVP VRM_EN deassertion max:1us
close to phase1 CHOKE
2015.7.20 R144 change to 13.7K
2015.7.20 R132 change to 23.7K
OFFSET MODE 0.7V enable
Internal 1.7V比較器
MAX:600mV
Fequency 400K 可由pin3 and pin43調
OCP:100A
OCP:75A
SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
SET3 control VR address
SETA1 cintrol ICCMAX,OCP setting
SETA2 control Internal compensation
2015.04.13
2015.6.16 R621 change to short pad
2015.7.20
R129 change to 150K
R139 change to 15K
MICRO-STAR INT'L CO.,LTD
MS-7996
PWM-RT3606BC
Date: Friday, August 07, 2015
Sheet 35 of 51


12VIN
Close to PWM
C168 1u16X6
C165 10u16X8
EC13 270u16SO
Q27
N-PK616BA_PDFN8-HF
35 RT3606_UG1
35 RT3606_BOOT1
R57 2.2R/8
C70 0.1u16X6
35 RT3606_PH1
35 RT3606_LG1
Q31
N-PK632BA_PDFN8-HF
CHOKE7
0.22u65A0.52m-HF
R197 1R1%6
C187 3300p50X4
CP6
CP7
X_COPPER
VCORE
Close to IC
R85 1.07KR1%4
C96 0.47u16X4
R87 X_0R/4
35 ISEN1P_3606
35 ISEN1N_3606
ISEN1+
ICCMAX:79A
LL:2.1m ohm
2015.7.20 R85,R93,R78 change to 1.07K
12VIN
Close to PWM
C46 1u16X6
C43 10u16X8
Q22
N-PK616BA_PDFN8-HF
35 RT3606_UG2
35 RT3606_BOOT2
R58 2.2R/8
C71 0.1u16X6
35 RT3606_PH2
35 RT3606_LG2
Q21
N-PK632BA_PDFN8-HF
CHOKE6
0.22u65A0.52m-HF
R169 1R1%6
C149 3300p50X4
CP8
CP9
X_COPPER
Close to IC
R93 1.07KR1%4
C100 0.47u16X4
R89 X_0R/4
35 ISEN2P_3606
35 ISEN2N_3606
ISEN2+
EC16 560u6.3SO
EC15 560u6.3SO
EC12 560u6.3SO
EC14 560u6.3SO
VCORE
12VIN
Close to PWM
C145 1u16X6
C143 10u16X8
EC2 270u16SO
Q11
N-PK616BA_PDFN8-HF
RT9624_UG3
RT9624_BOOT3
R97 2.2R/8
C109 0.1u16X6
RT9624_PH3
RT9624_LG3
Q9
N-PK632BA_PDFN8-HF
PVCC_3606
R123 5.1R1%6
C118 1u16X6
U23
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
35 RT3606_PWM3
RT9624_BOOT3
RT9624_UG3
RT9624_PH3
RT9624_LG3
RT9624F
CHOKE4
0.22u65A0.52m-HF
R79 1R1%6
C81 3300p50X4
CP10
CP11
X_COPPER
Close to IC
R78 1.07KR1%4
C85 0.47u16X4
R75 X_0R/4
35 ISEN3P_3606
35 ISEN3N_3606
ISEN3+
MICRO-STAR INT'L CO.,LTD
MS-7996
Size Custom
Document Description
VCORE(P-PAK) PHASE1-3
Rev 10
Date: Friday, August 07, 2015
Sheet 36 of 51



MICRO-STAR INT'L CO.,LTD

MS-7996

Size	Document Description	Rev
Custom	VGT(P-PAK) PHASE1-2	10

Date: Friday, August 07, 2015 | Sheet 37 of 51

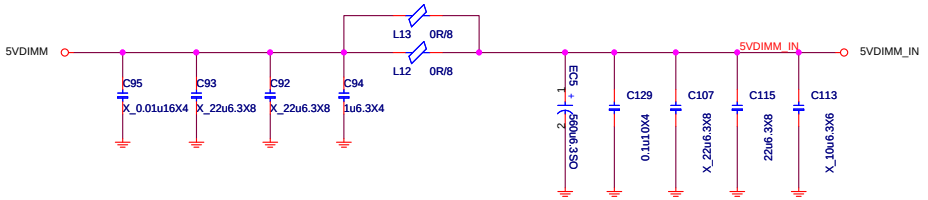
DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU
4.8A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

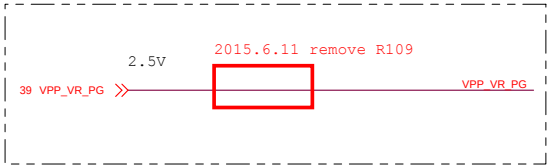
OCP =7.925A*1.5=11.8875A
Current limit= 95.3K(R1054)*5uA/10/4mohm)=11.91A

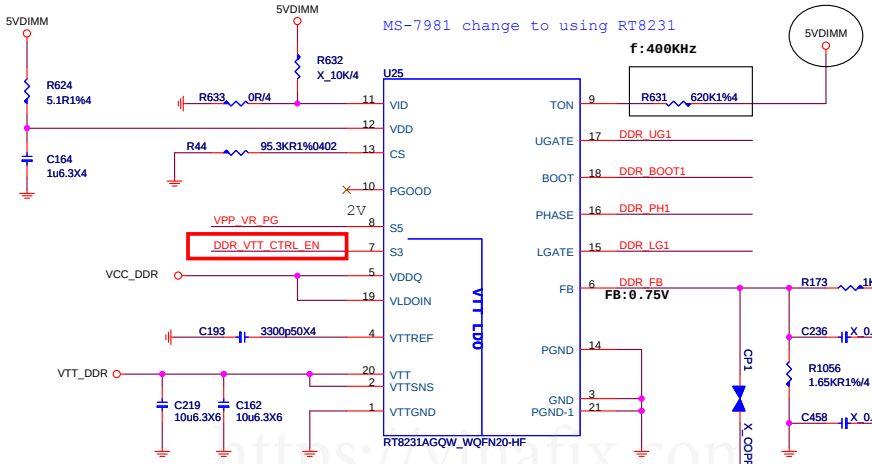
2015.05.22 change to DDR4

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 9.357 * 0.44
= 4.154A



VID	Reference Voltage (V)
H	0.675
L	0.75

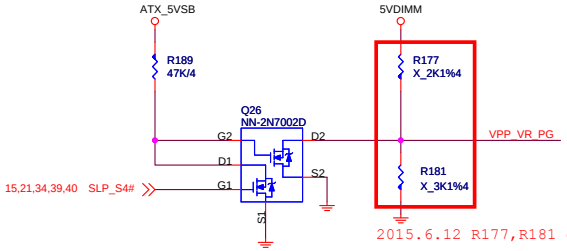




5VDIMM By layout modify

MAX:7.925A

1.2V



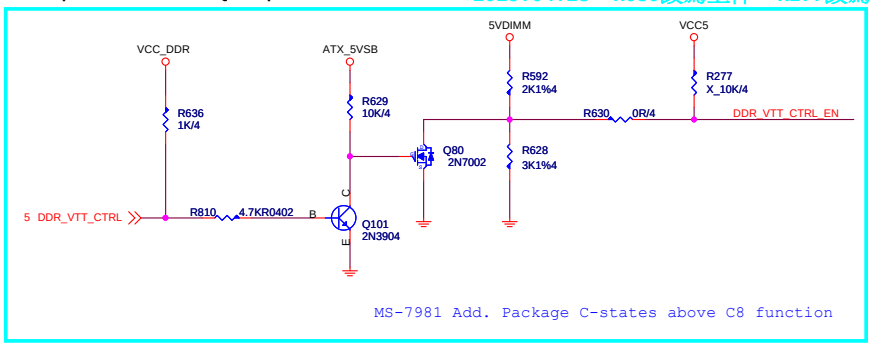
2015.6.12 R177,R181 depop

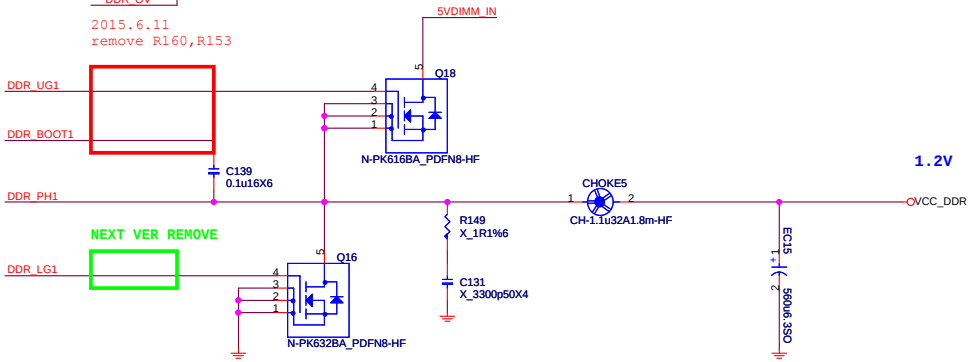
2015.6.11 remove circuit

SLP_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down

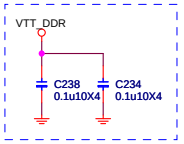
2015.04.23 R630改為上件，R277改為不上件





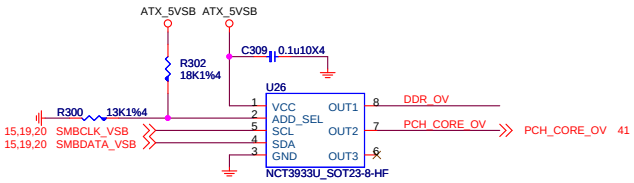
2015.6.11
remove R160,R153

0.1uFx1 per dimm



UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



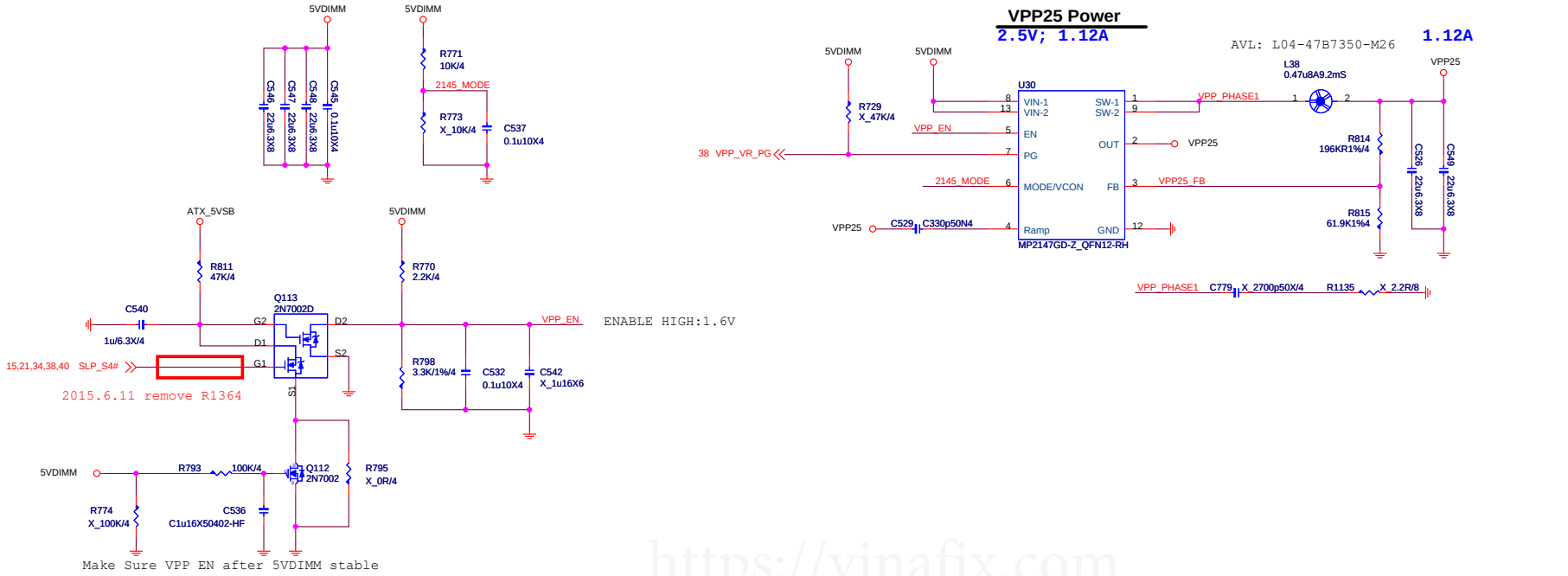
MICRO-STAR INT'L CO.,LTD

MS-7996

Size: Custom | Document Description: DDR-RT8231 | Rev: 10

Date: Friday, August 07, 2015 | Sheet 38 of 51

2DIMM :1.12A FOR DDR VPP2.5V

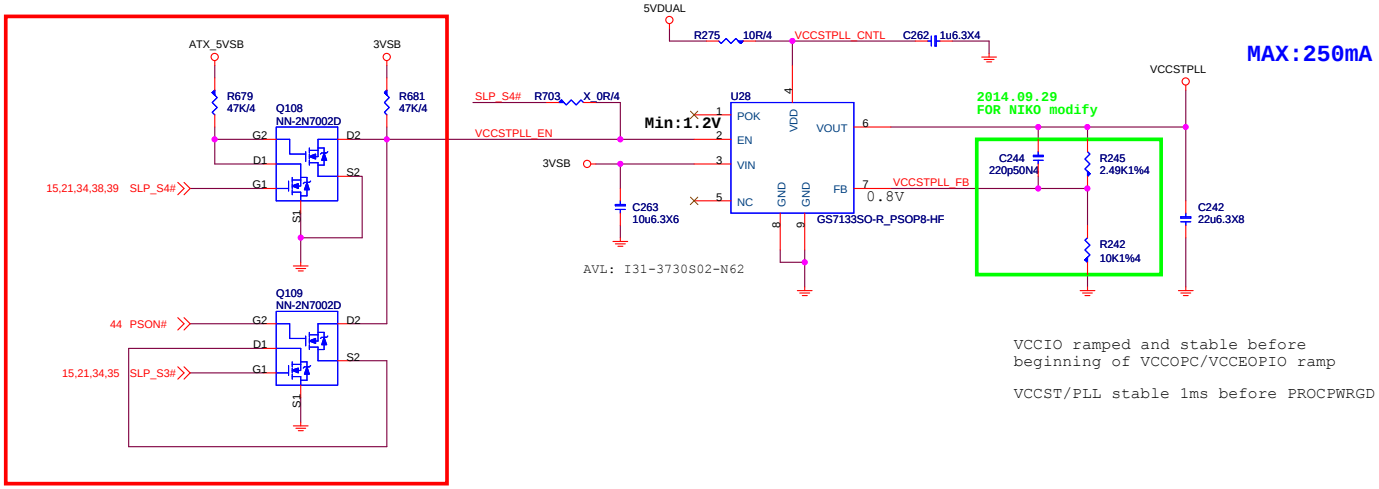


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7996	
Size: Custom	Document Description: DDR-MP2147-VPP25	Rev: 10
Date: Friday, August 07, 2015	Sheet 39 of 51	

VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge



VCCIO ramped and stable before
beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

2015.05.25 add circuit

MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: CPU PWR_ST/PLL	Rev: 10
Date: Friday, August 07, 2015	Sheet 40 of 51	

PCH_1VSB

1.0V; 7.858A

OCP = 11.787A

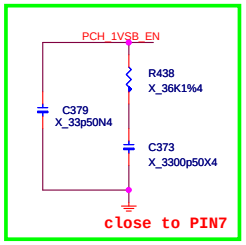
Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 7.858 * 5mohm / 10uA
= 5.8935K

Rocs:5.9K,OCP:
D03-4C05N03-O05 : 11.8A
D03-632BA0C-N03 : 12.82A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

2015.04.23 change to UP1540

2014.08.22 close to U34



2015.01.22
for up1540:stuff R438->36K,
C379->NC,C373->3.3nF
for RT8125:R438.C379.C373->NC

2015.01.22
for up1540:R403->2.2R,C362->1uF
for RT8125:R403->10R,C362->1uF

2015.6.11
remove R372,R371

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

MAX:10.664A

2014.12.25
for up1540:C364&R407 ->NC

2015.08.06
R407 -> 806R

2015.05.25
for up1540:C365 is OCP set min:5Kohm
stuff 5.9K OCP SET:11.787A
RT8125C stuff C1000P C11-1022032-W08

2014.12.25
for up1540:R623 ->NC

2014.12.25
for up1540:R374->NC

to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

2014.12.25
for up1540:stuff R622->0R

2014.12.25
for up1540:R420 ->NC
RT8125C:R420 ->NC

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

PLACE UNDER THE PCH

Vinafix.com

MICRO-STAR INT'L CO.,LTD	
MS-7996	
Size: Custom	Document Description: PCH Core power
Rev: 10	
Date: Friday, August 07, 2015	Sheet 41 of 51

SA Power:1.05V,11.1A

*OCP =11.1A*1.4=15.54A*
*Rocs(R15)=OCP*Rdson(Low side)3.4mohm]/10uA*
=15.54(3.4)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

2015.01.22
for up1540:R96->2.2R,C84->1uF
for RT8125:R96->10R,C84->1uF

12VIN R210 10R/8 C207 1u16X6

EN:VIH2.4V
EN pin Maximum:6.5V

POR:4.2V

2015.6.8 remove R211

MAX:11.1A

U35
VCCSA_EN → EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT → SA_BOOT1 → C208 0.1u16X4
PHASE → SA_PH1
UGATE → SA_UG1
LGATE/OCSET → SA_LG1
FB → SA_FB → R217 1K1%4 → R218 10R1%4 → R221 0R/4 → VCCSA_SENSE 5
VCCSA
C212 X_0.1u10X4
R215 3.16K1%4
R225 0R/4 → VSS_VCCSA_SENSE 5,43
R226 10R1%4

FB:0.8V
Vout=0.8*(1+R19/R20)

2015.08.06
R407 -> 806R

2014.10.16
up1540 no stuff
SA_REFOUT → R219 768R1%4 → SA_REFIN
C216 1000p16X4
C215 1000p16X4

up1540 stuff R
RT8125C stuff C1000P C11-1022032-W08

F:300K 不可調

2014.09.11 By layout

12VIN
R214 26.1K1%4
VCCSA_EN
R243 10K1%4
C243 X_0.1u16X4
Q42 2N7002
ATX_5VSB
R248 47K/4
C239 X_0.1u10X4
Q43 2N7002
35 VRM_EN

2015.6.8 remove R244

2014.12.25
for up1540:R214&R243 ->NC

2014.08.14

VCCSA_EN
R223 X_36K1%4
C214 X_33p50N4
C218 X_0.01u16X4
RSVD for up1540

close to U35

2015.01.22
for up1540:stuff R223->36K,
C214->NC,C218->10nF
for RT8125:R223.C214.C218->NC

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.2825
= 3.13575A

12VIN
C196 1u16X6
C201 10u16X8
EC1 270u16SO

2015.6.8 remove R207

SA_UG1 → Q33 N-PK616BA_PDFN8-HF

SA_PH1
CHOKE8 CH-1.1u25A1.07m-HF → VCCSA
R212 X_2.2R/8
C210 X_3300p50X4
snubber
C205 1u6.3X4
C200 22u6.3X8
EC21 560u6.3SO
EC22 560u6.3SO

1.05V,18A

VCCSA_EN
5,35,43 SLP_S3_CTRL → SLP_S3_CTRL → Q41 2N7002

SLP_S3# assertion to VR disabled
max:1us

NEXT VER REMOVE

SA_LG1 → Q34 N-PK632BA_PDFN8-HF
R213 5.36K1%4

OCPSET:min 5Kohm

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

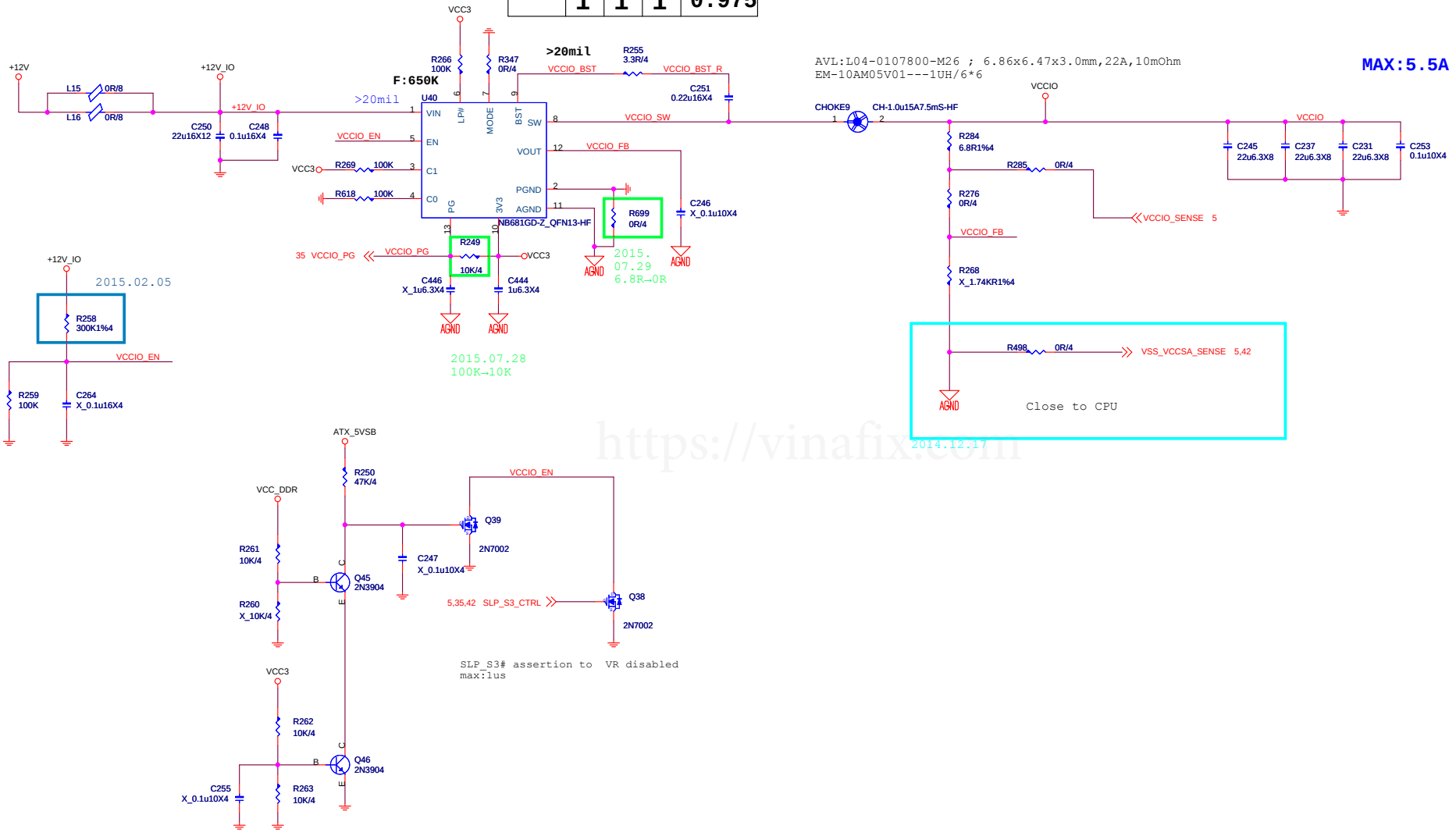
MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: VCCSA - POWER RT8125C	Rev: 10
Date: Friday, August 07, 2015	Sheet 42 of 51	

VCCIO

0.95V; 5.5A

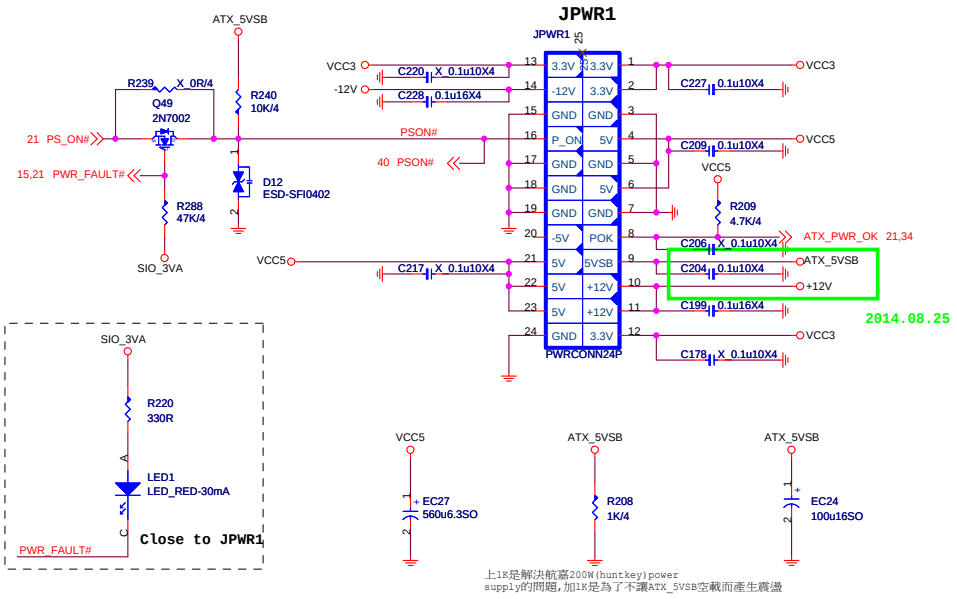
IMAX 6A
ILIMIT=8.5~9A

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

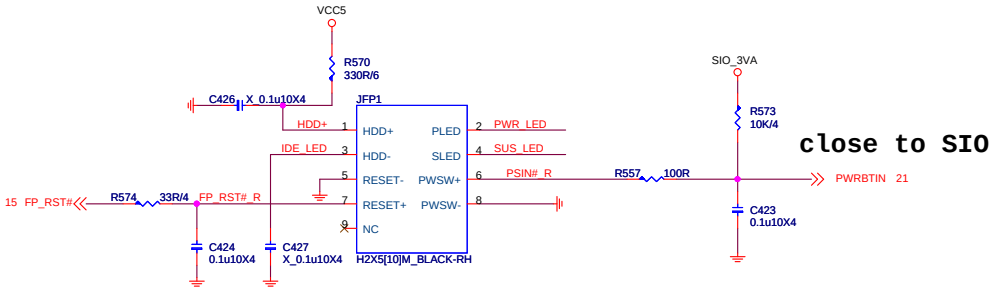


MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size: Custom	Document Description: VCCIO - POWER NB671	Rev: 10
Date: Friday, August 07, 2015	Sheet 43 of 51	

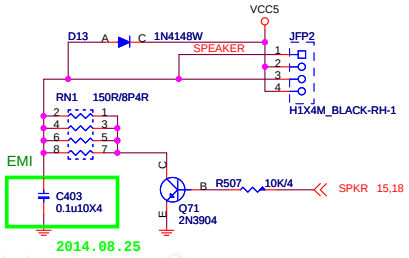
ATX POWER CONNECTOR



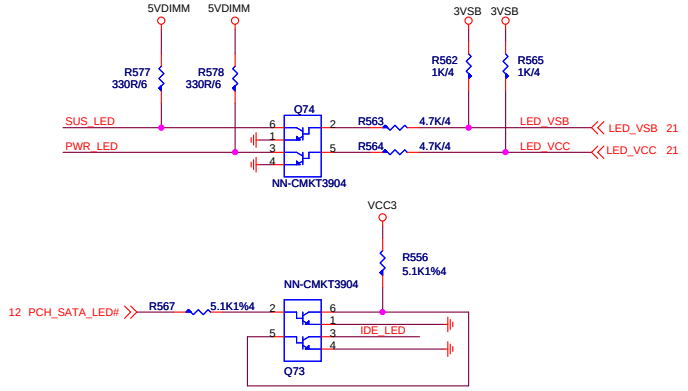
FRONT PANNEL



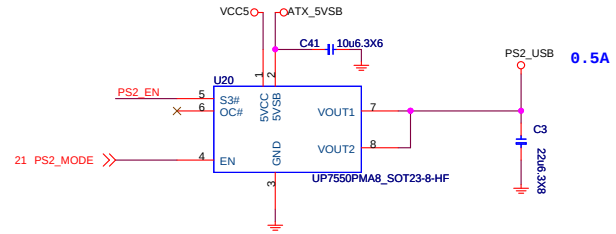
Speaker Pin Header



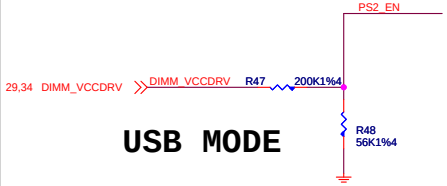
LED (for NV5533)



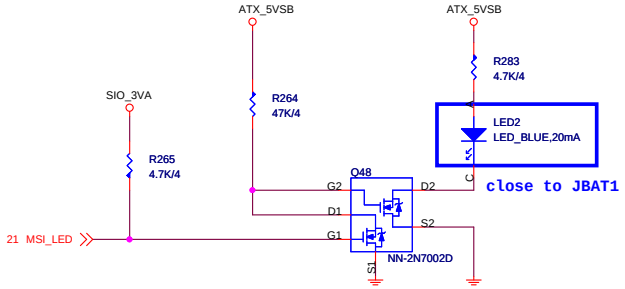
PS2 POWER



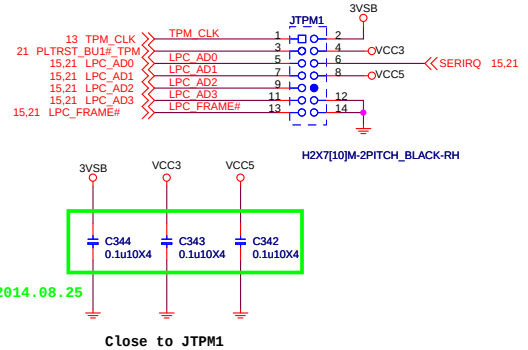
USB MODE



MSI LED



TPM



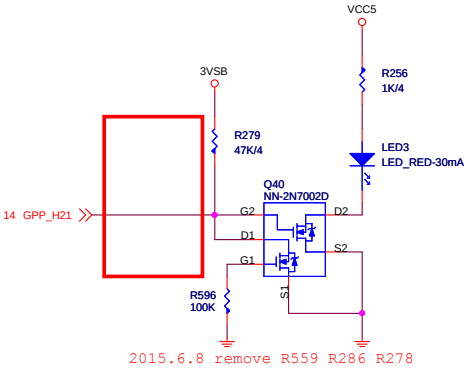
MICRO-STAR INT'L CO.,LTD

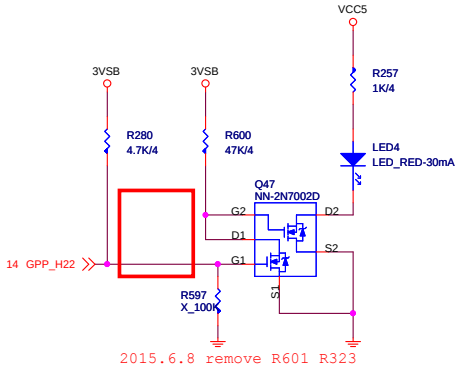
MS-7996

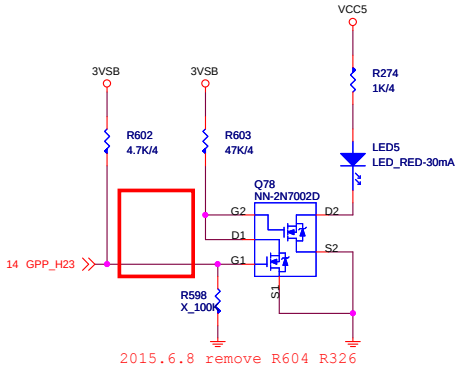
Size	Document Description	Rev
Custom	ATX F_Panel/TPM/MSI_LED	10

Date: Friday, August 07, 2015 Sheet 44 of 51

DEBUG LED







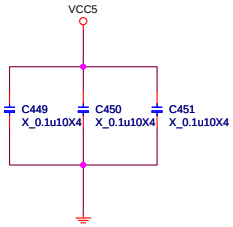
GPIO / LED	GPP_H21	GPP_H21	GPP_H21
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

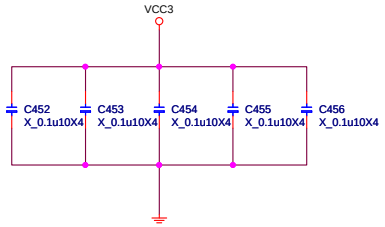
關機斷電狀態下，3個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

MSI	MICRO-STAR INT'L CO.,LTD
	MS-7996
Size: Custom	Document Description: ATX F_Panel/TPM/MSI_LED — Rev: 10
Date: Friday, August 07, 2015	Sheet 45 of 51

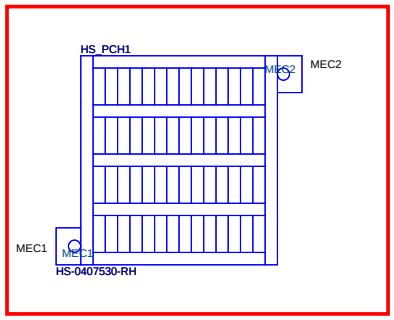
EMI CAP

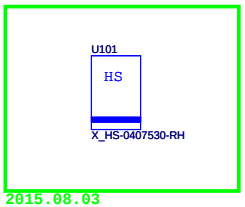




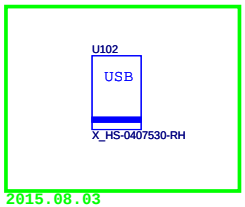
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7996	
Size: Custom	Document Description: EMI	Rev: 10
Date: Friday, August 07, 2015	Sheet 46 of 51	

2015.06.01 change to using E31-0407530-K08

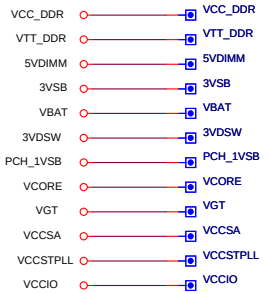




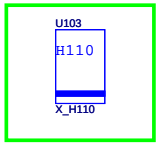
2015.08.03
colay Heatsink for H110



2015.08.03
USB2.0 Connector colay for H110

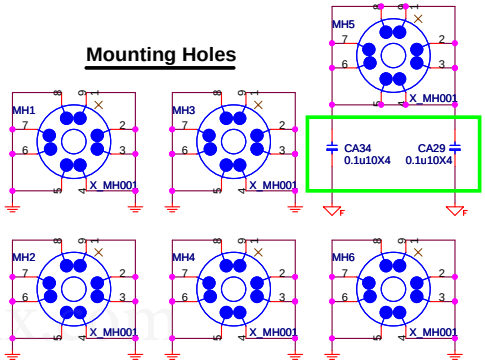


2015.08.03
PCH H110 colay

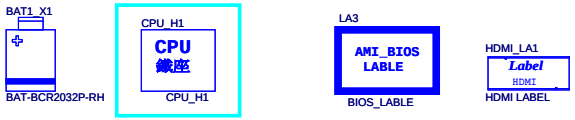


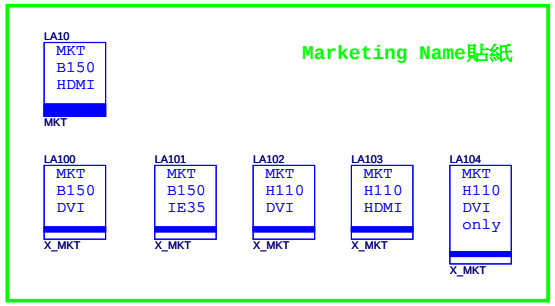
Vinafix.com

Mounting Holes

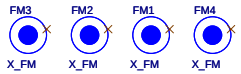


20150423 PM Request cost down

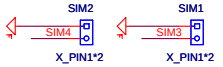




Optical Fiducial Marks-120



Simulation



2015/08/04 PK0-0799611-E48,競華,23,寶安恩斯邁廠(MSIS)
2015/08/04 PK0-0799611-E48,競華,27,寶安恩斯邁廠(MSIS)
2015/08/04 PK0-0799611-G37,精成,23,寶安恩斯邁廠(MSIS)
2015/08/04 PK0-0799611-G37,精成,28,寶安恩斯邁廠(MSIS)

MICRO-STAR INT'L CO.,LTD

MS-7996

Size	Document Description	Rev
Custom	Manual Parts	10

Date: Friday, August 07, 2015 Sheet 47 of 51