Compal Confidential

ZAUSA Schematics Document

AMD "Kabini" Platform

AMD 25W APU With Jaguar Core and Integrated Yangtze FCH + ATI Sun Pro S3

LA-A331P REV: 0.1

2013-02-04

Security Classification	Compal Secret Data		
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Title: COVER PAGE		
Size: Custom	Document Number: LA-A331P	Rev: 0.1
Date: Monday, February 04, 2013	Sheet 1 of 40	

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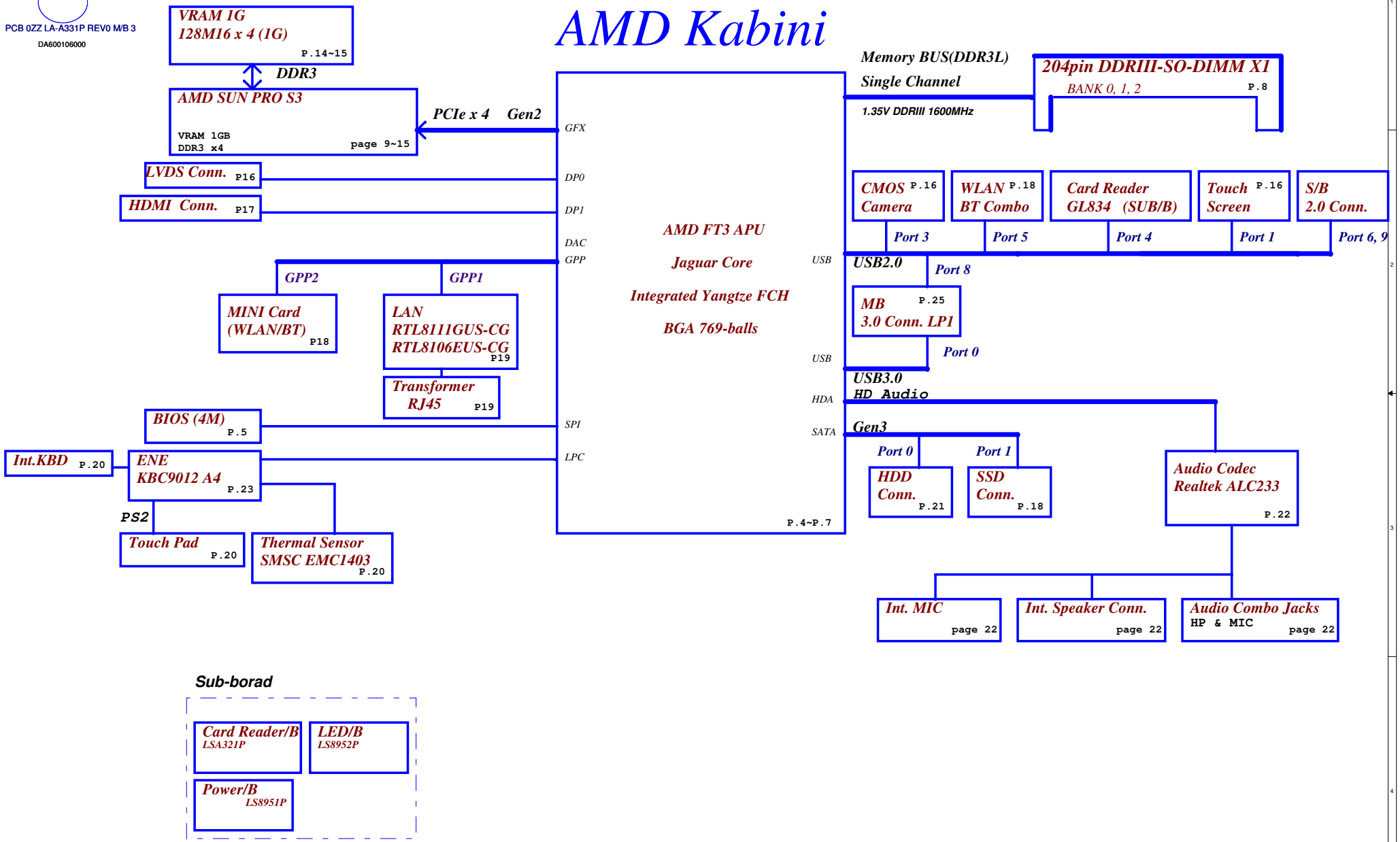
Model Name : ZAUSA

ZZZ1
PCB 0ZZ LA-A331P REV0 M/B 3
DA600106000



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Title: BLOCK DIAGRAMS

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+RTC_APU	RTC power	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+0.95VALW	0.95V always on power rail	ON	ON	ON
+1.35V	1.35V power rail for APU and DDR	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	PX	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	PX	OFF	OFF
+3VS_VGA	3.3V switched power rail for VGA	PX	OFF	OFF
+1.8VS_VGA	1.8V switched power rail for VGA	PX	OFF	OFF
+1.5VS_VGA	1.5V switched power rail for VGA	PX	OFF	OFF
+0.95VS_VGA	0.95V switched power rail for VGA	PX	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	EVT
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

USB OC MAPPING

OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

4319OS38L01: EMIP@/ESDP@/SWR@/8106@/TS@/UMA@/43L01@
4319OS38L02: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L02@
4319OS38L03: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L03@
4319OS38L04: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L04@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1 +3VALW	KB9012	X	V	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0 +3VS	APU	X	X	X	V	V	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2 +3VS	KB9012	V	X	X	X	X	V	X	V	X

APU PCIE PORT LIST

Port	Device
0	
1	LAN
2	WLAN
3	

BOM Structure Table

BOM Structure	BTO Item
43L01@	X4-5110 BGA APU
43L02@	X2-3450 BGA APU
43L03@	E1-2210 BGA APU
43L04@	X4-4110 BGA APU
ME@	ME part
SWR@	LAN Switching mode
LDO@	LAN LDO mode
GAS@	Gastube
PX@	Common VGA circuit
TS@	Touch Screen
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component
X76@	VRAM
VRAM1@	Samsung 128Mbx16 K4W2G1646E-BC1A
VRAM2@	Hynix 128Mbx16 H5TC2G63FFR-11C
VRAM3@	Micron 126Mbx16 MT41J128M16JT-093G:K
8111@	Realtek RTL8111GUS-CG (Giga LAN)
8106@	Realtek RTL8106EUS-CG (10/100M)
@	Unpop

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
VGA Internal Thermal	1000 001X b	82H

APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H

USB Port Table

USB 2.0	USB 3.0		Port	3 External USB Port
			0	RIGHT USB
			1	Touch Screen
			2	
			3	Camera
			4	CardReader
			5	WLAN/BT Combo
			6	LEFT USB2.0
			7	
	XHCI	0	8	LEFT USB3.0
		1	9	LEFT USB2.0

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Title: NOTES LIST

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HDMI & LVDS should be reverse in KABINI:
APU TX0 to Connector TX2 ; APU TX1 to Connector TX1
APU TX2 to Connector TX0 ; APU TX3 to Connector CLK

UAPU1A
MEMORY
FT3 REV 0.51
2M201079J4461 2G_BGA769P
43L01@

UAPU1C
DISPLAY/SVID/JTAG/TEST
FT3 REV 0.51
2M201079J4461 2G_BGA769P
43L01@

UAPU1
2MA5B078J2361 1.65G BGA 769P
43L02@

UAPU1
2M101082J2361 1G BGA 769P
43L03@

UAPU1
2M151278J4461 1.5G BGA 769P
43L04@

HDMI

LVDS

PU +3VS

PU +1.8VS

PU +1.8VS + PD

PD

HDT+

JHDT2 @
SAMTE_ASP-136446-07-B

MEMORY VREF

RP11, RP6 will @ when MP

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Compal Electronics, Inc.

Title: FT3 DDR3/DISP/MISC//HDT+

Size	Document Number	Rev
Custom	LA-A331P	0.1

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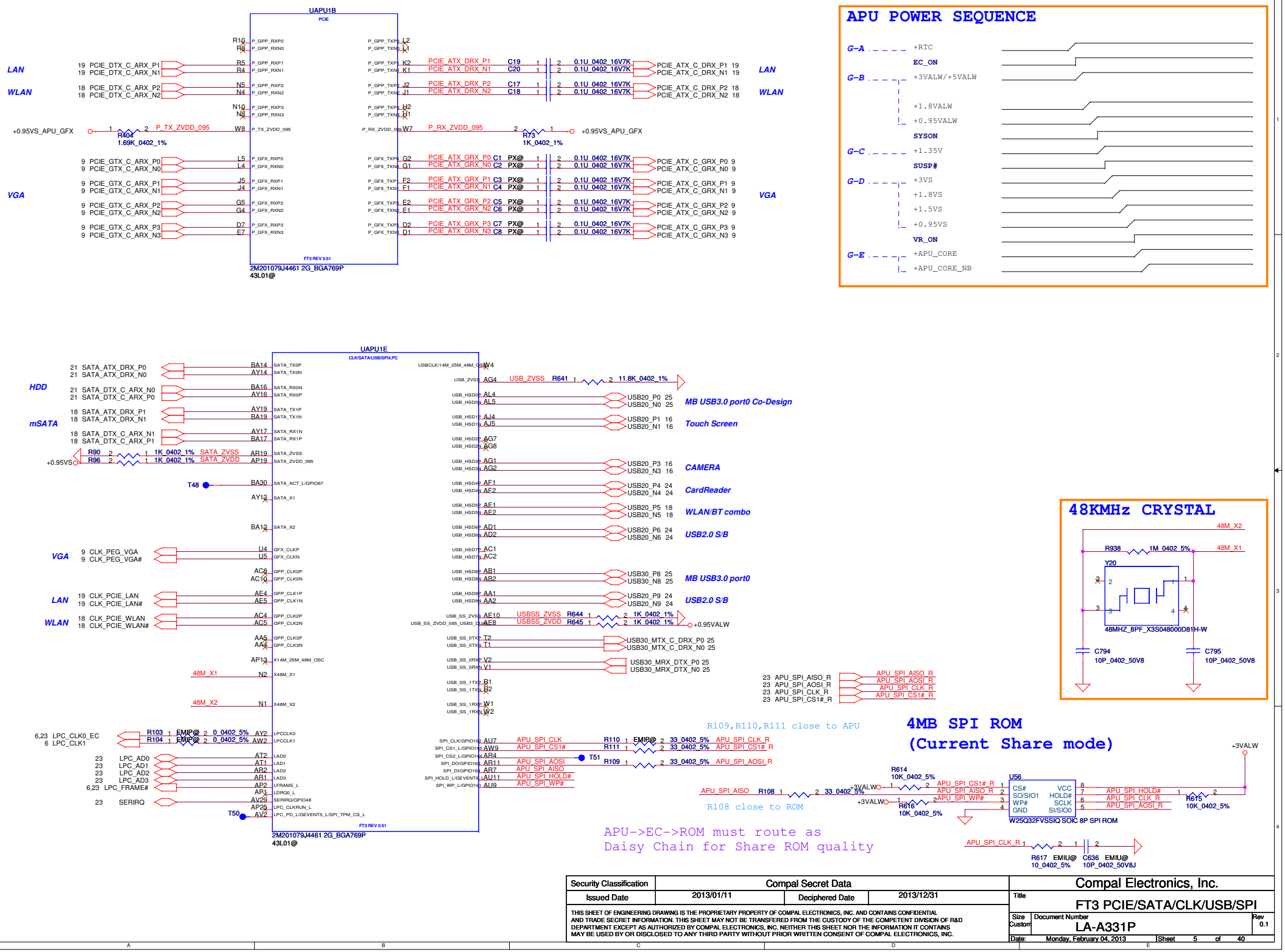

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Compal Electronics, Inc.

Title: FT3 PCIE/SATA/CLK/USB/SPI

Size	Document Number	Rev
Custom	LA-A331P	0.1

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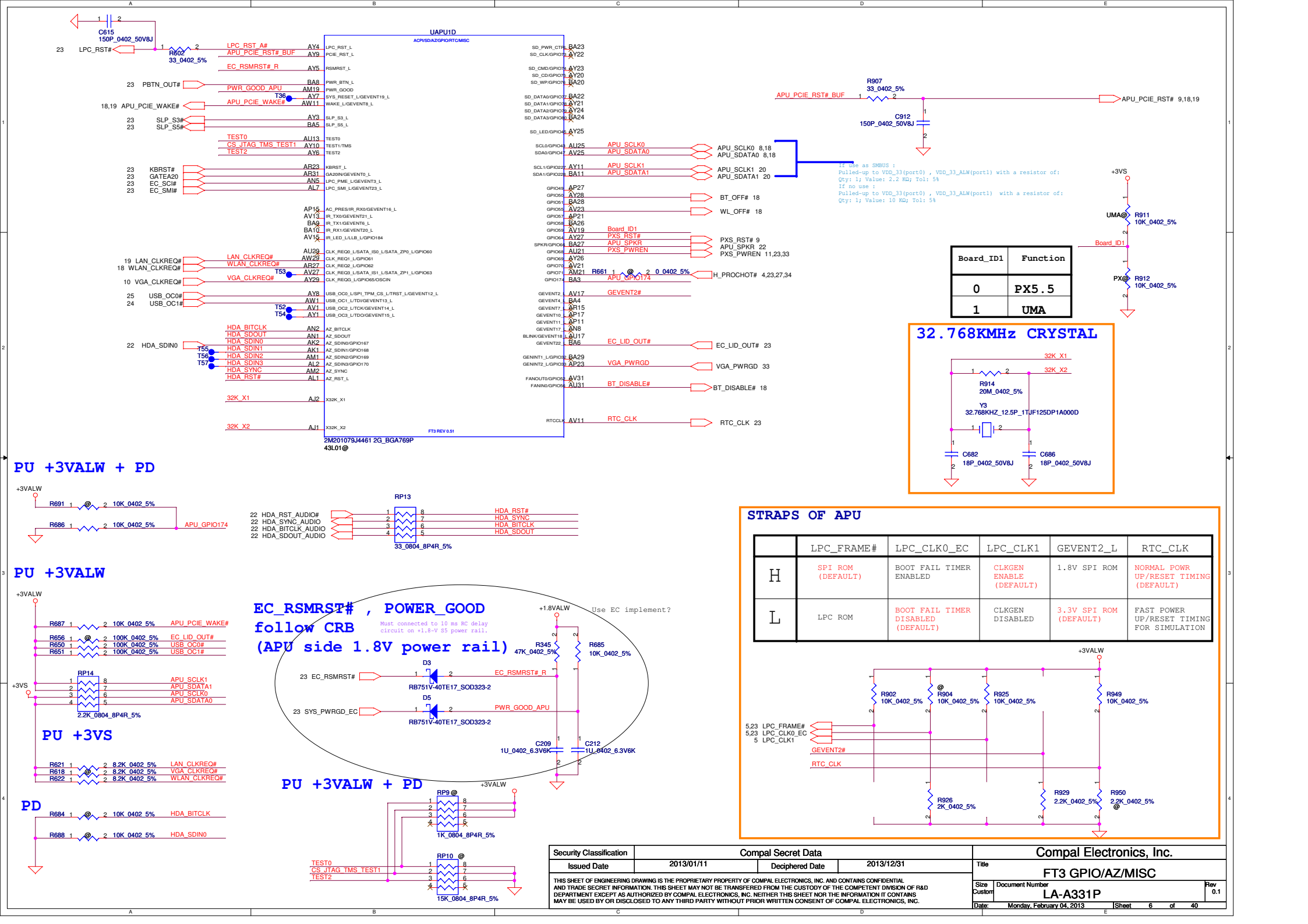

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Compal Electronics, Inc.

Title: FT3 GPIO/AZ/MISC

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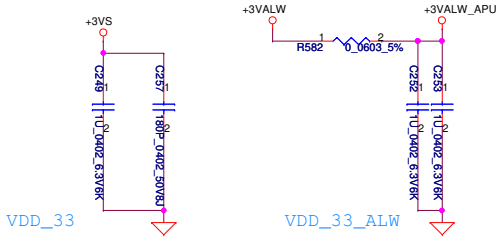
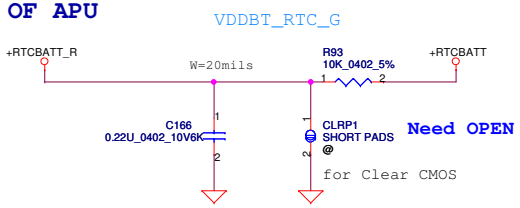
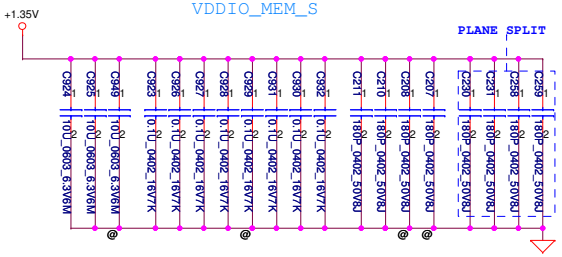
+3VALW/+3VS OF APU

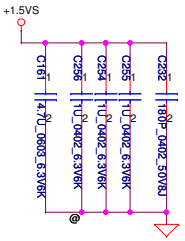


RTC OF APU

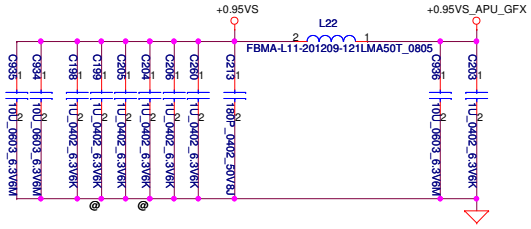


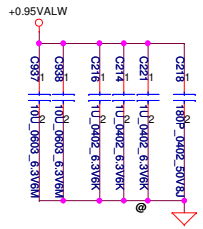
+1.35V OF APU

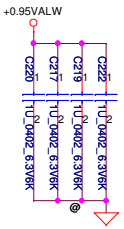




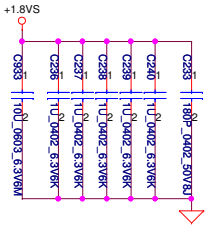
+0.95VALW/+0.95VS OF APU

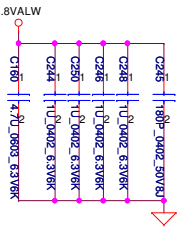


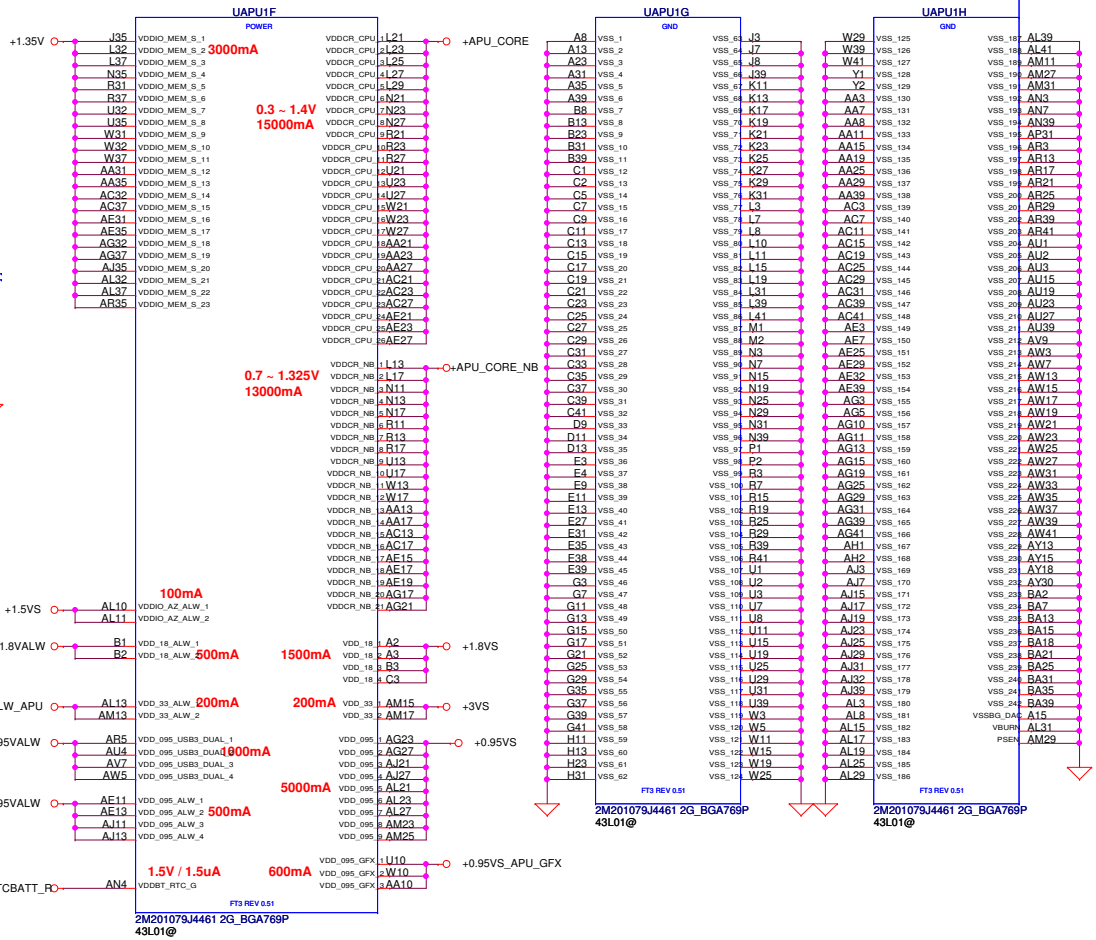




+1.8VALW/+1.8VS OF APU







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Title: FT3 PWR/GND

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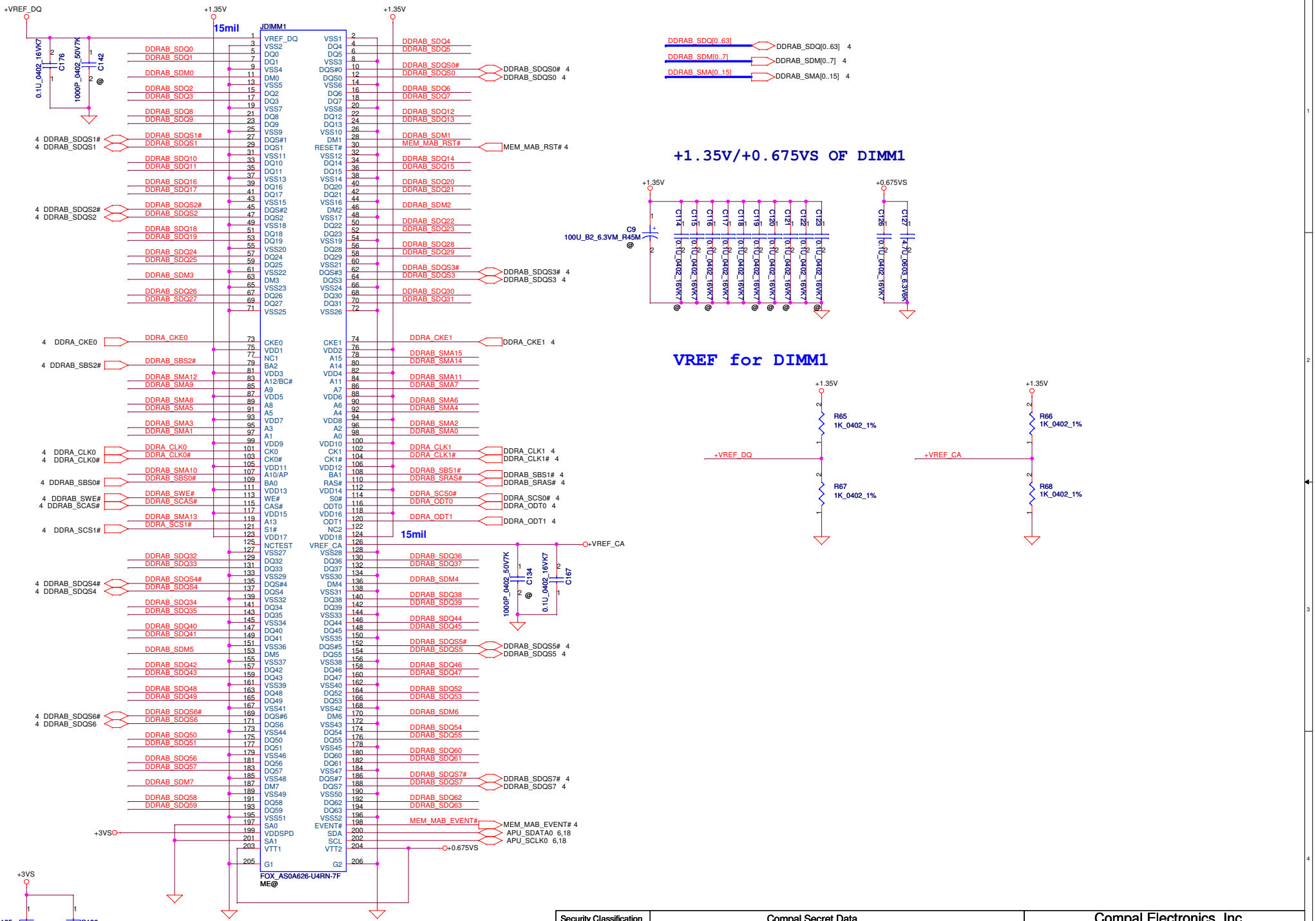

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Title: DDR3 SODIMM-I Socket

Size	Document Number	Rev
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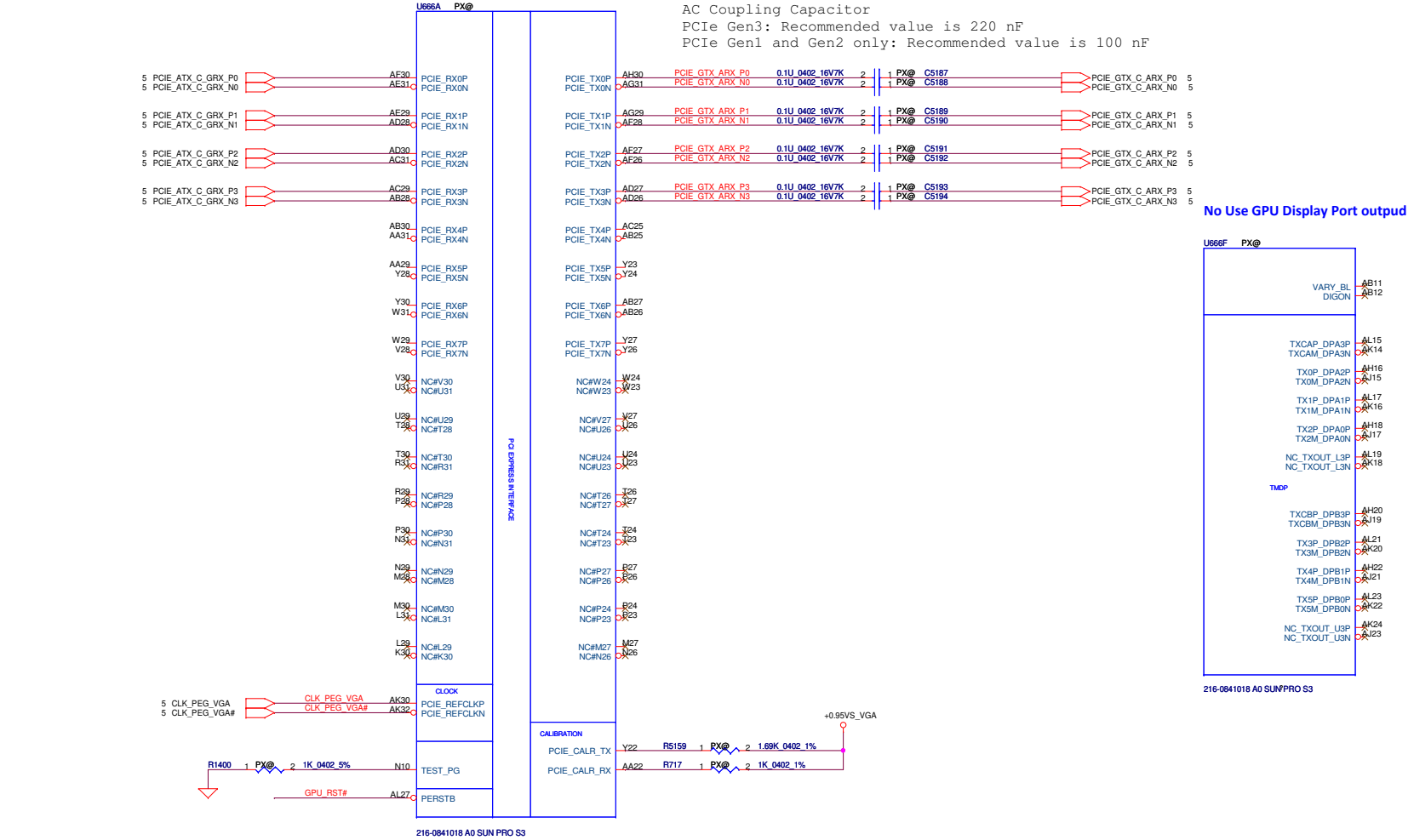

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Title: **SUN_PCIE/DP**

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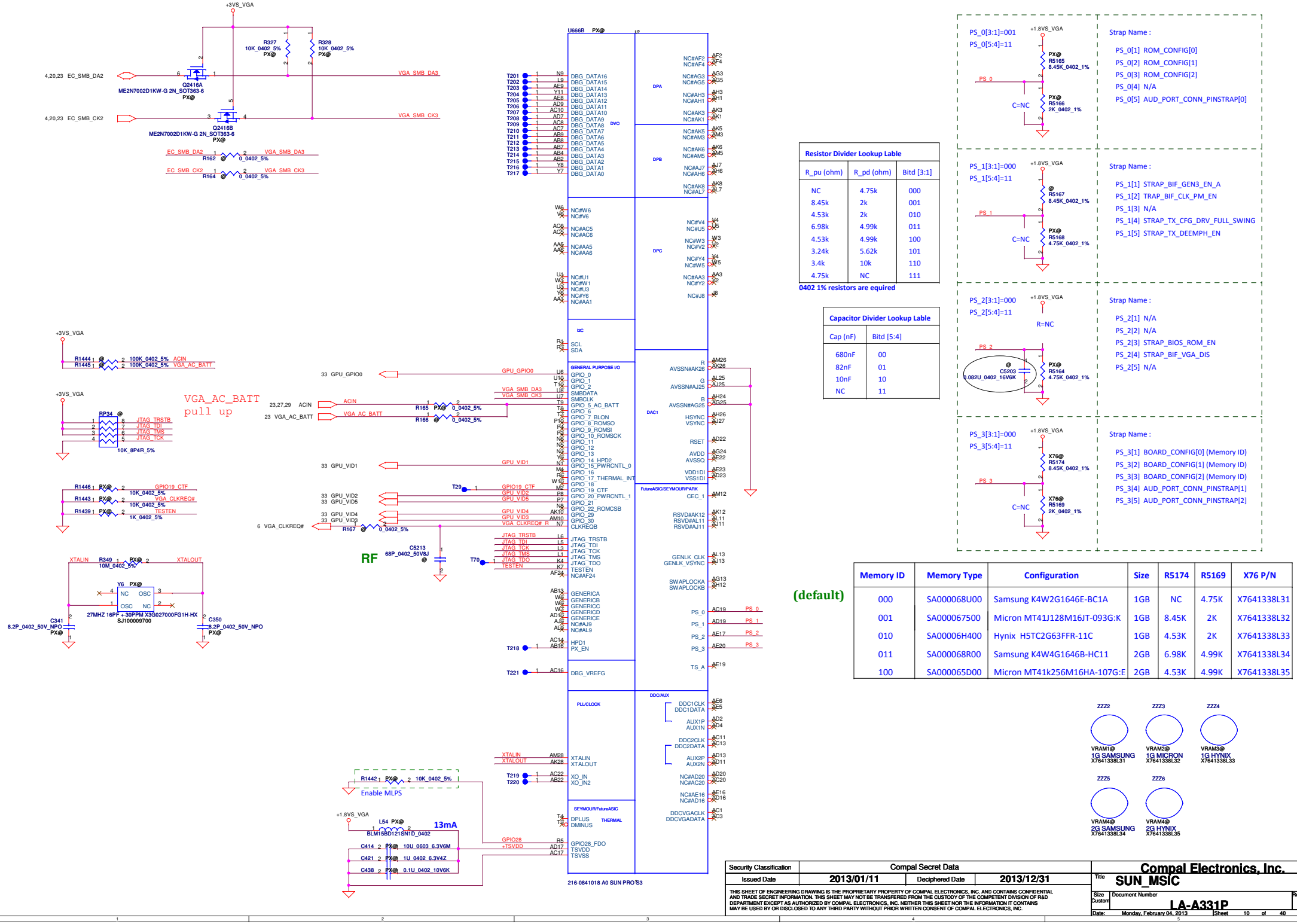

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

(default)

Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB	NC	4.75K	X7641338L31
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB	8.45K	2K	X7641338L32
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7641338L33
011	SA000068R00	Samsung K4W4G1646B-HC11	2GB	6.98K	4.99K	X7641338L34
100	SA000065D00	Micron MT41k256M16HA-107G:E	2GB	4.53K	4.99K	X7641338L35

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Title: SUN_MSIC

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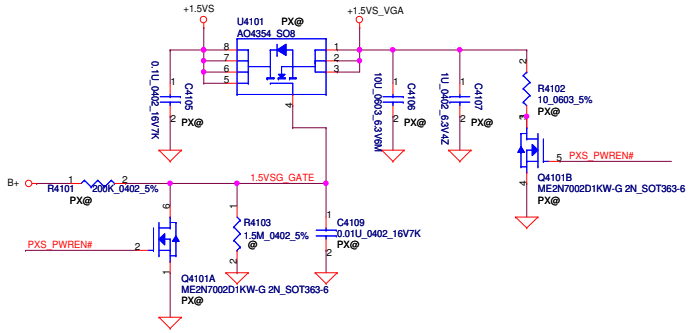
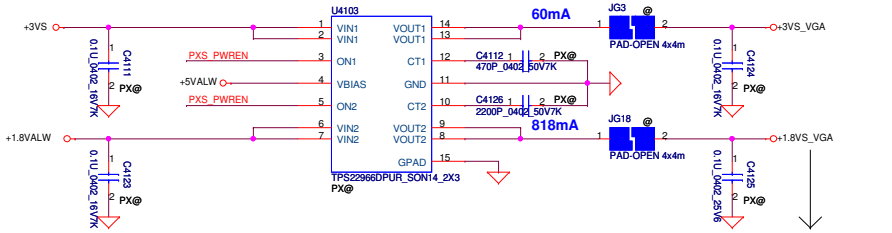
+1.5VS to +1.5VS_VGA (2.096A)



+3VS to +3VS_VGA (25mA)

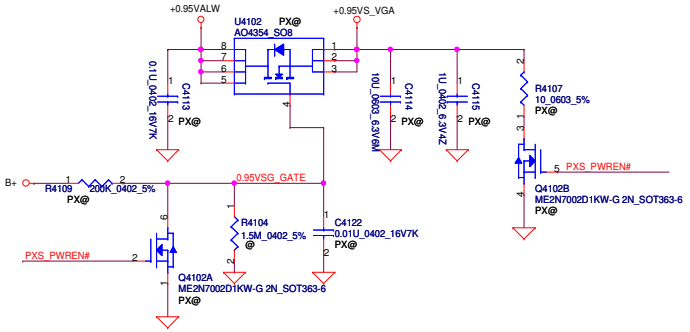
+1.8VALW to +1.8VS_VGA (311mA)

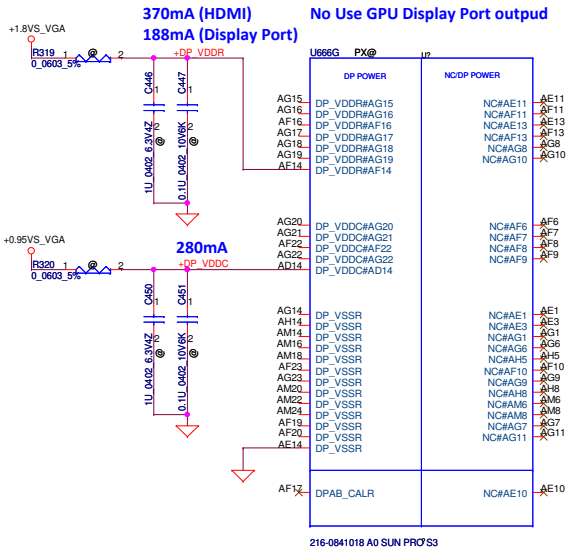


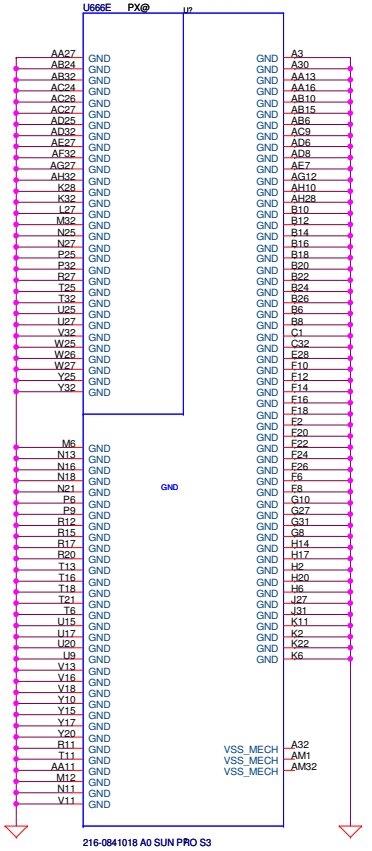
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, AOZ1331 (engineering sample available on 2013/Jan/18)

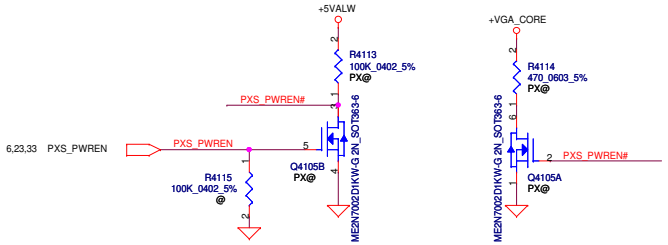
+1.8VS_VGA 必須比 +VGA_CORE晚起來

+0.95VALW to +0.95VSG (4.016A)









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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: SUN_Power/GND

Size: Custom | Document Number: LA-A331P | Rev: 0.1

Date: Monday, February 04, 2013 | Sheet 11 of 40

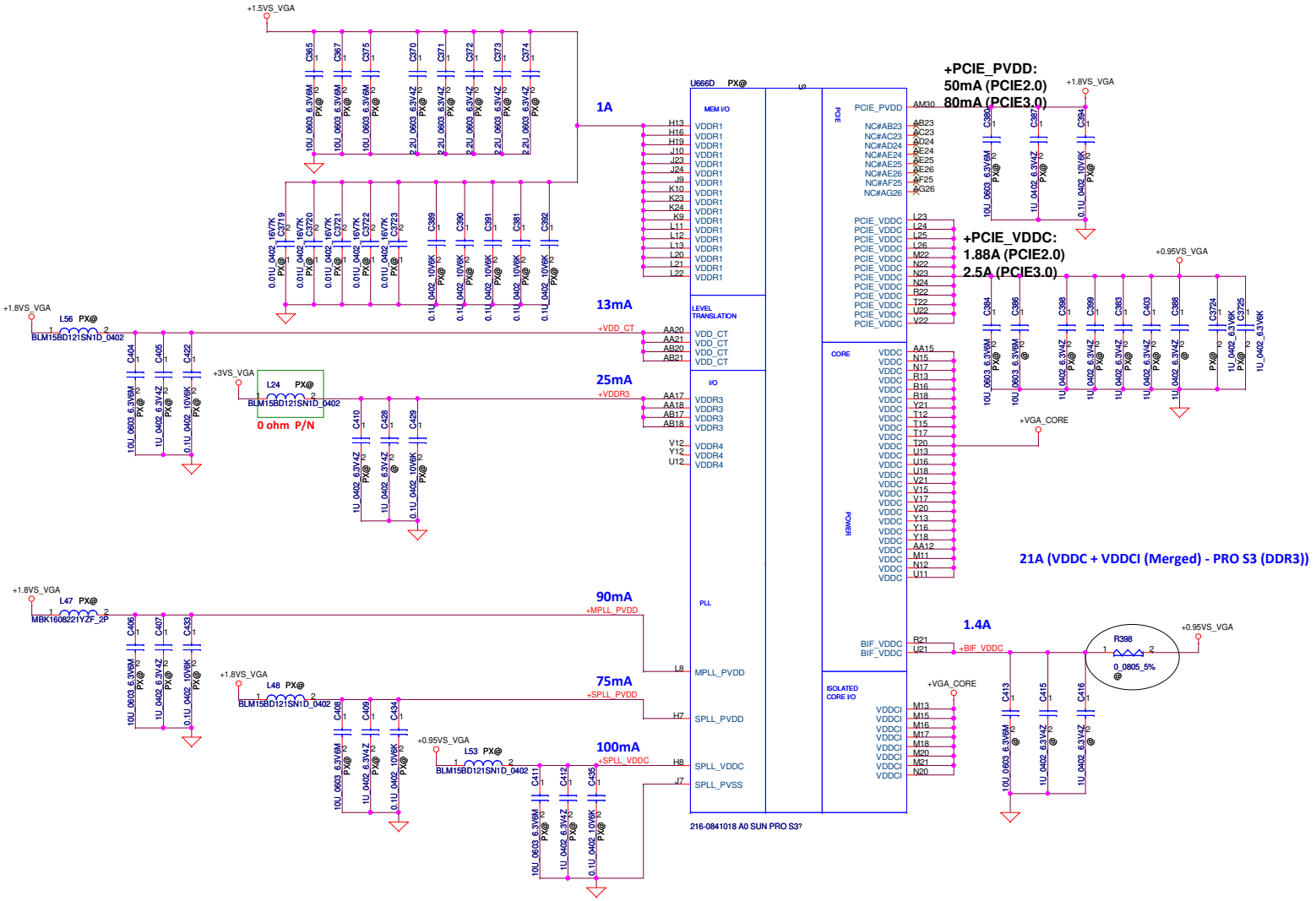
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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Compal Electronics, Inc.

Title: SUN_Power

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Date: Monday, February 04, 2013 | Sheet 12 of 40

14,15 M_DA[63..0] M_DA[63..0]
14,15 M_MA[15..0] M_MA[15..0]
14,15 M_DQM[7..0] M_DQM[7..0]
14,15 M_DQS[7..0] M_DQS[7..0]
14,15 M_DQS#[7..0] M_DQS#[7..0]

+1.5VS_VGA
PX@ R363 40.2_0402_1%
+MVREFDA
PX@ R364 100_0402_1%
PX@ C467 1U_0402_6.3V4Z

+1.5VS_VGA
PX@ R365 40.2_0402_1%
+MVREFSA
PX@ R457 100_0402_1%
PX@ C514 1U_0402_6.3V4Z

14,15 DRAM_RST#
PX@ R5160 49.9_0402_1%
PX@ R455 10_0402_1%
DRAM_RST
PX@ C469 120P_0402_50V8J
PX@ R5161 5.1K_0402_1%

Place close to GPU (within 25mm)
and place componment close to each other

PX@ U666C U2
GDDR5/DDR3

M_DA0	K27	DQA0_0	MAA0_0/MAA_0	K17	M_MA0
M_DA1	J29	DQA0_1	MAA0_1/MAA_1	J20	M_MA1
M_DA2	H30	DQA0_2	MAA0_2/MAA_2	H23	M_MA2
M_DA3	H32	DQA0_3	MAA0_3/MAA_3	G23	M_MA3
M_DA4	G29	DQA0_4	MAA0_4/MAA_4	G24	M_MA4
M_DA5	F28	DQA0_5	MAA0_5/MAA_5	H24	M_MA5
M_DA6	F32	DQA0_6	MAA0_6/MAA_6	J19	M_MA6
M_DA7	F30	DQA0_7	MAA0_7/MAA_7	K19	M_MA7
M_DA8	C30	DQA0_8	MAA0_8/MAA_13	G20	M_MA13
M_DA9	F27	DQA0_9	MAA0_9/MAA_15	L17	M_MA15
M_DA10	A28	DQA0_10			
M_DA11	C29	DQA0_11	MAA1_0/MAA_8	J14	M_MA8
M_DA12	E27	DQA0_12	MAA1_1/MAA_9	K14	M_MA9
M_DA13	G26	DQA0_13	MAA1_2/MAA_10	J11	M_MA10
M_DA14	D26	DQA0_14	MAA1_3/MAA_11	J13	M_MA11
M_DA15	F25	DQA0_15	MAA1_4/MAA_12	H11	M_MA12
M_DA16	A25	DQA0_16	MAA1_5/MAA_BA2	G11	M_BA2 14,15
M_DA17	C25	DQA0_17	MAA1_6/MAA_BA0	J16	M_BA0 14,15
M_DA18	E25	DQA0_18	MAA1_7/MAA_BA1	L15	M_BA1 14,15
M_DA19	D24	DQA0_19	MAA1_8/MAA_14	G14	M_MA14
M_DA20	E23	DQA0_20	MAA1_9/RSVD	L16	
M_DA21	F23	DQA0_21			
M_DA22	D22	DQA0_22	WCKA0_0/DQMA0_0	E32	M_DQM0
M_DA23	F21	DQA0_23	WCKA0B_0/DQMA0_1	E30	M_DQM1
M_DA24	E21	DQA0_24	WCKA0_1/DQMA0_2	A21	M_DQM2
M_DA25	D20	DQA0_25	WCKA0B_1/DQMA0_3	C21	M_DQM3
M_DA26	F19	DQA0_26	WCKA1_0/DQMA1_0	E13	M_DQM4
M_DA27	A19	DQA0_27	WCKA1B_0/DQMA1_1	D12	M_DQM5
M_DA28	D18	DQA0_28	WCKA1_1/DQMA1_2	E3	M_DQM6
M_DA29	F17	DQA0_29	WCKA1B_1/DQMA1_3	F4	M_DQM7
M_DA30	A17	DQA0_30			
M_DA31	C17	DQA0_31	EDCA0_0/QSA0_0	H28	M_DQS0
M_DA32	E17	DQA1_0	EDCA0_1/QSA0_1	C27	M_DQS1
M_DA33	D16	DQA1_1	EDCA0_2/QSA0_2	A23	M_DQS2
M_DA34	F15	DQA1_2	EDCA0_3/QSA0_3	E19	M_DQS3
M_DA35	A15	DQA1_3	EDCA1_0/QSA1_0	E15	M_DQS4
M_DA36	D14	DQA1_4	EDCA1_1/QSA1_1	D10	M_DQS5
M_DA37	F13	DQA1_5	EDCA1_2/QSA1_2	D6	M_DQS6
M_DA38	A13	DQA1_6	EDCA1_3/QSA1_3	G5	M_DQS7
M_DA39	C13	DQA1_7			
M_DA40	E11	DQA1_8	DDBIA0_0/QSA0_0B	H27	M_DQS#0
M_DA41	A11	DQA1_9	DDBIA0_1/QSA0_1B	A27	M_DQS#1
M_DA42	C11	DQA1_10	DDBIA0_2/QSA0_2B	C23	M_DQS#2
M_DA43	F11	DQA1_11	DDBIA0_3/QSA0_3B	C19	M_DQS#3
M_DA44	A9	DQA1_12	DDBIA1_0/QSA1_0B	C15	M_DQS#4
M_DA45	C9	DQA1_13	DDBIA1_1/QSA1_1B	E9	M_DQS#5
M_DA46	F9	DQA1_14	DDBIA1_2/QSA1_2B	C5	M_DQS#6
M_DA47	D8	DQA1_15	DDBIA1_3/QSA1_3B	H4	M_DQS#7
M_DA48	E7	DQA1_16			
M_DA49	A7	DQA1_17	ADBIA0/ODTA0	L18	VRAM_ODT0 VRAM_ODT0 14
M_DA50	C7	DQA1_18	ADBIA1/ODTA1	K16	VRAM_ODT1 VRAM_ODT1 15
M_DA51	F7	DQA1_19			
M_DA52	A5	DQA1_20	CLKA0	H26	M_CLK0 M_CLK0 14
M_DA53	E5	DQA1_21	CLKA0B	H25	M_CLK#0 M_CLK#0 14
M_DA54	C3	DQA1_22			
M_DA55	E1	DQA1_23	CLKA1	G9	M_CLK1 M_CLK1 15
M_DA56	G7	DQA1_24	CLKA1B	H9	M_CLK#1 M_CLK#1 15
M_DA57	G6	DQA1_25			
M_DA58	G1	DQA1_26	RASA0B	G22	M_RAS#0 M_RAS#0 14
M_DA59	G3	DQA1_27	RASA1B	G17	M_RAS#1 M_RAS#1 15
M_DA60	J6	DQA1_28			
M_DA61	J1	DQA1_29	CASA0B	G19	M_CAS#0 M_CAS#0 14
M_DA62	J3	DQA1_30	CASA1B	G16	M_CAS#1 M_CAS#1 15
M_DA63	J5	DQA1_31			
			CSA0B_0	H22	M_CS#0 M_CS#0 14
+MVREFDA	K26	MVREFDA	CSA0B_1	J22	
+MVREFSA	J26	MVREFSA			
	J25		CSA1B_0	G13	M_CS#1 M_CS#1 15
	K25	NC#J25	CSA1B_1	K13	
		MEM_CALRP0			
			CKEA0	K20	M_CKE0 M_CKE0 14
			CKEA1	J17	M_CKE1 M_CKE1 15
DRAM_RST	L10	DRAM_RST			
			WEA0B	G25	M_WE#0 M_WE#0 14
			WEA1B	H10	M_WE#1 M_WE#1 15
	K8	CLKTESTA			
	L7	CLKTESTB			

MEMORY INTERFACE

R5162 1 PX@ 2 120_0402_1%

R460 @ 1 2 51.1_0402_1% C542 @1 2 0.1U_0402_16V4Z
R373 @ 1 2 51.1_0402_1% C541 @1 2 0.1U_0402_16V4Z

Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation,if not need, DNI.

216-0841018 A0 SUN PRO-S3

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Compal Electronics, Inc.

Title: SUN_MEM

Size: Custom | Document Number: LA-A331P | Rev: 0.1

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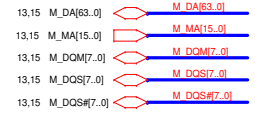
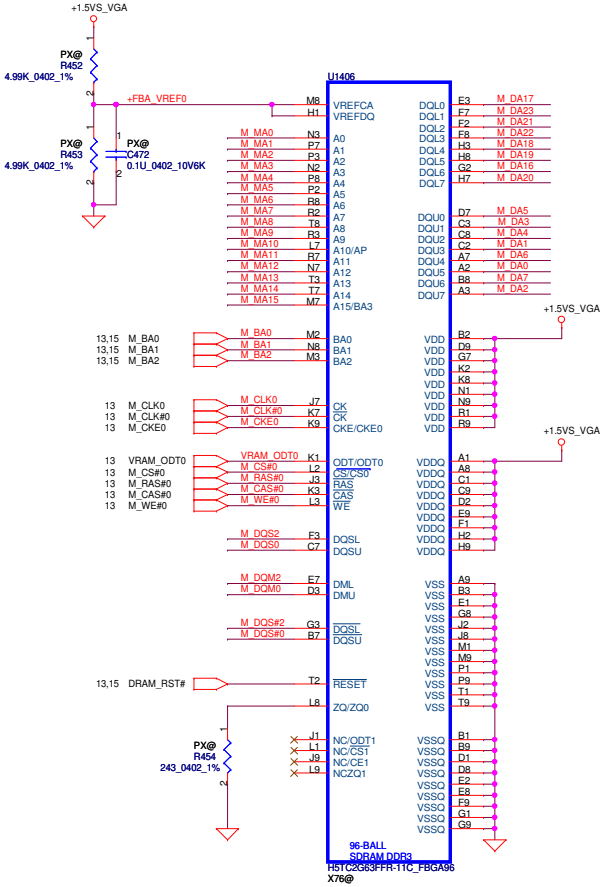
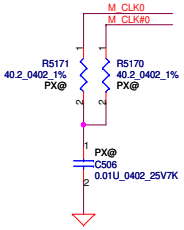
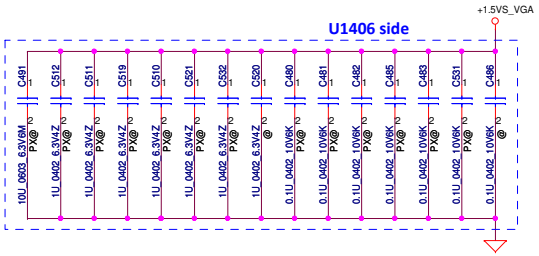
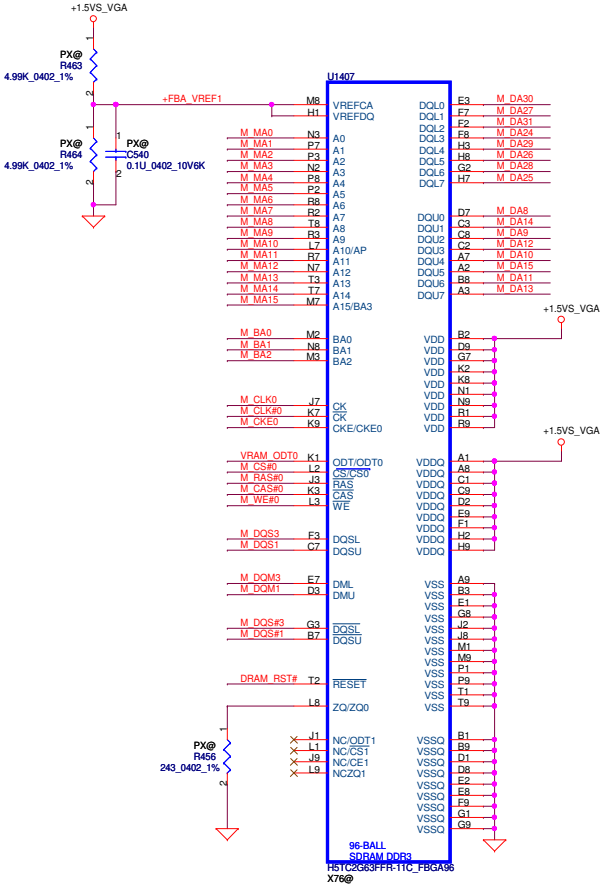
Memory Partition A - Lower 32 bits

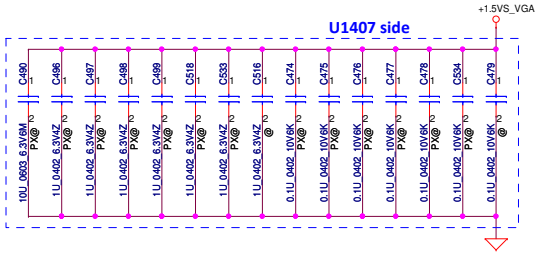












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Compal Electronics, Inc.

Title: SUN_VRAM A Lower

Size: Custom | Document Number: LA-A331P | Rev: 0.1

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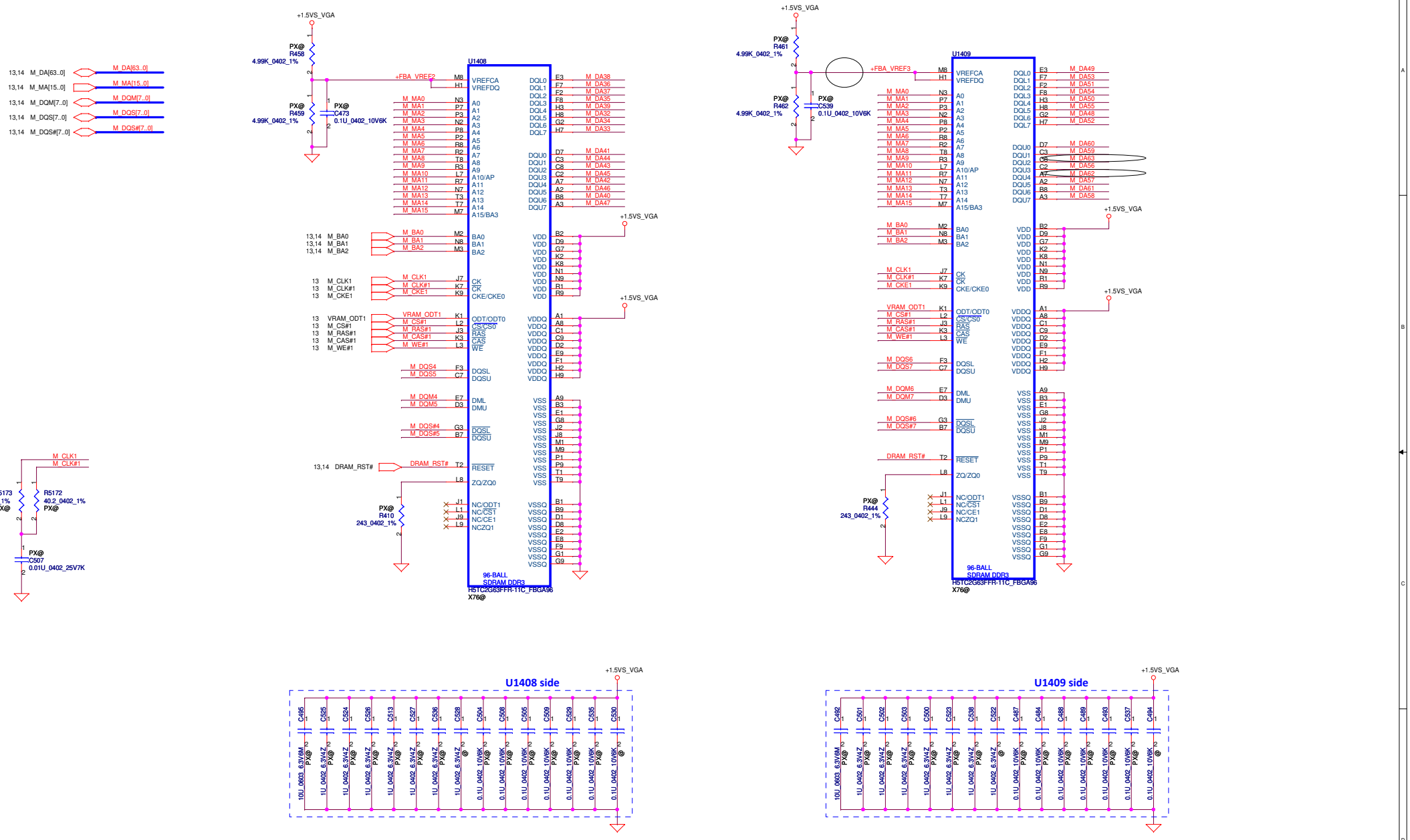
Memory Partition A – Upper 32 bits



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Compal Electronics, Inc.

Title: **SUN_VRAM A Upper**

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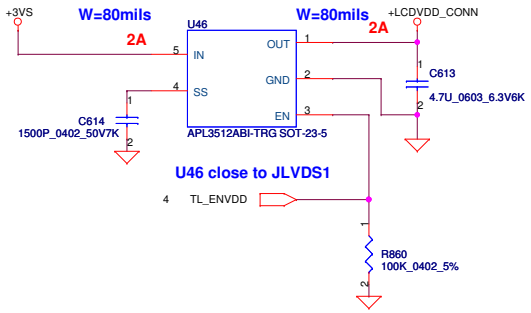
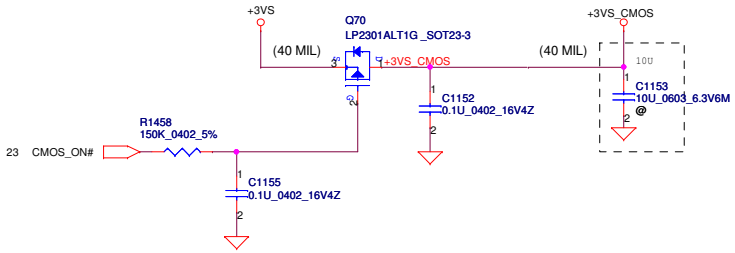
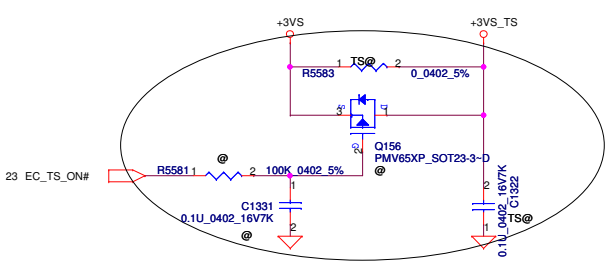
Date: Monday, February 04, 2013 | Sheet 15 of 40

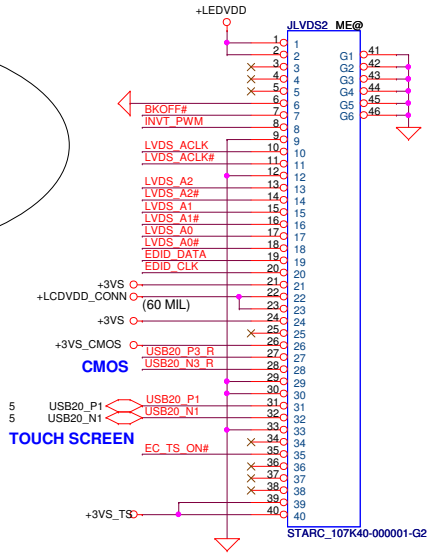
LCD POWER CIRCUIT



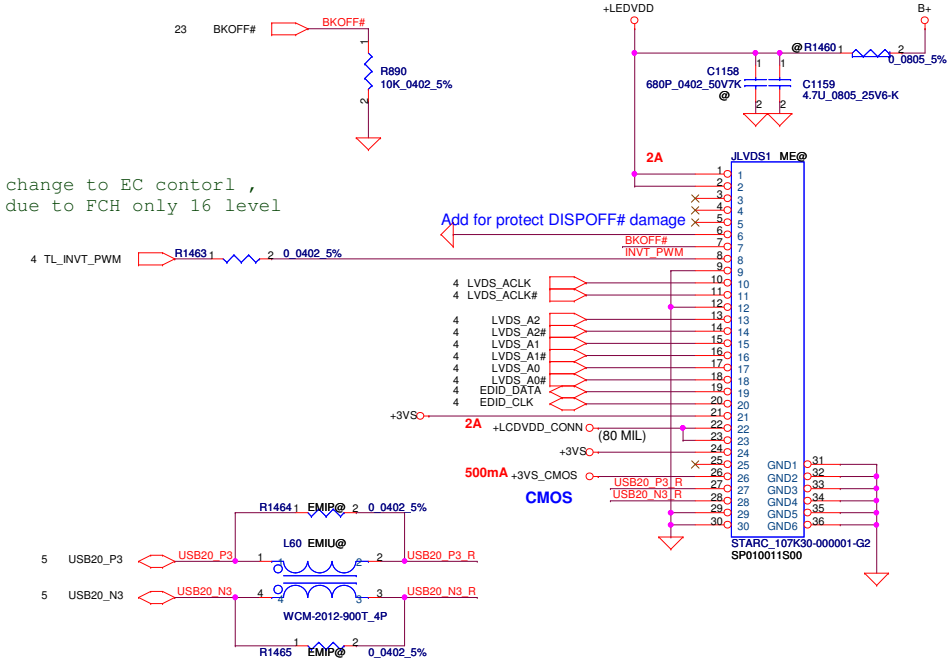
CMOS Camera







VGA LCD/PANEL BD. Conn.



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Compal Electronics, Inc.			
Title	LVDS/CAMERA		
Size: Custom	Document Number: LA-A331P		Rev: 0.1
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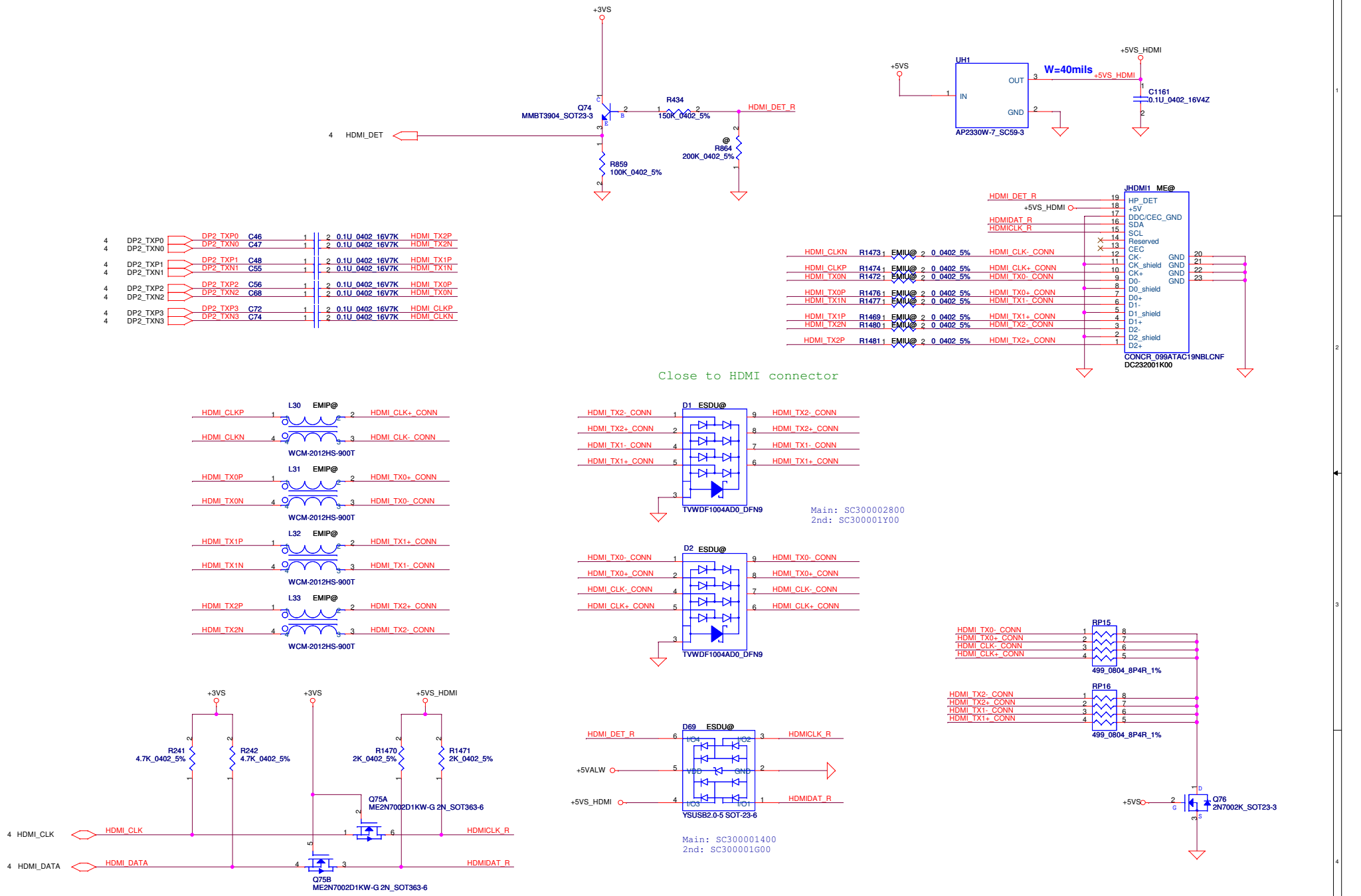

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Compal Electronics, Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
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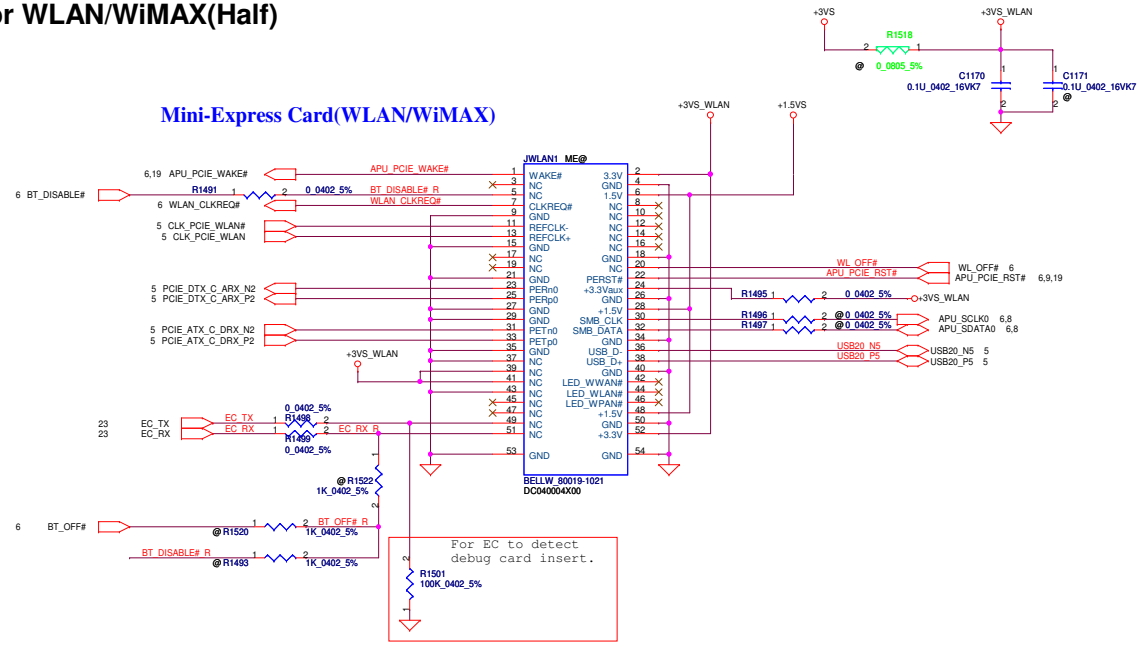
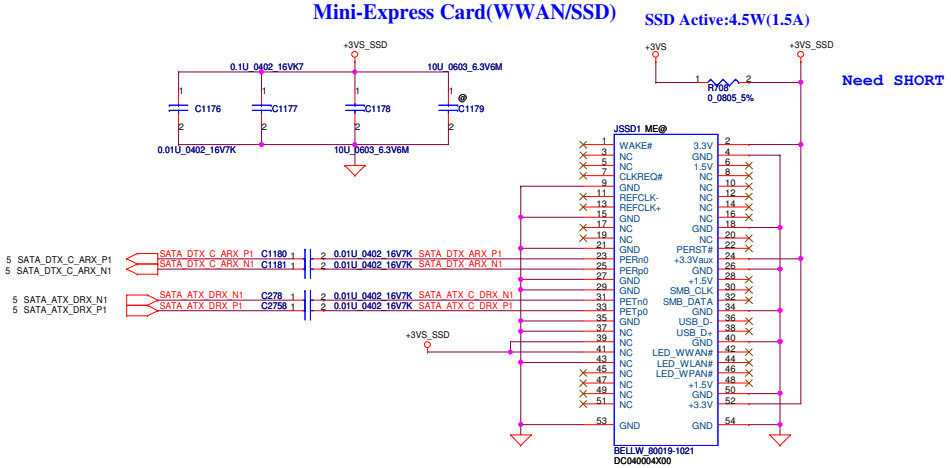
Mini-Express Card for WLAN/WiMAX(Half)



Mini-Express Card for SSD(Full)



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Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: LA-A331P		Rev: 0.1
Date: Monday, February 04, 2013	Sheet 18 of 40		

+3_LAN Rising time (10%~90%) >1mS and <100mS

+3VALW — W=60mils — R709 0_0805_5% — 370mA — +3V_LAN

+3V_LAN
C1195 4.7U_0603_6.3V6K SWR@
C1196 0.1U_0402_16V4Z SWR@
These caps close to U47 : Pin 23

+3V_LAN
C1268 0.1U_0402_16VK7
C1274 0.1U_0402_16VK7
These caps close to U1201 : Pin 11,32

+LAN_REGOUT W=60mils
R1240 LDO@ 0_0603_5%
L35 2.2UH +-5% NLC252018T-2R2J-N SWR@
W=60mils
+LAN_VDD10
C1277 0.1U_0402_16VK7 LDO@
C1187 4.7U_0603_6.3V6K SWR@
C1184 0.1U_0402_10V6K SWR@
C1201 C1202 C1203 C1204 C1205 C1206 C1207 0.1U_0402_16VK7
(Should be place within 200 mils)
These components close to U47 : Pin 24
These components close to U47 : Pin 3,8,22,30
1uF reserved on Pin 22

+3V_LAN — R2220 @ 10K_0402_5% — LAN_WAKE#
EC pin29 Internal PU

U47 8111@
5 PCIE_DTX_C_ARX_P1 — C1183 0.1U_0402_16V7K — PCIE_DTX_ARX_P1
5 PCIE_DTX_C_ARX_N1 — C1186 0.1U_0402_16V7K — PCIE_DTX_ARX_N1
6,9,18 APU_PCIE_RST#
23 LAN_WAKE# — R1508 0_0402_5% — R1509 @ 0_0402_5% — 6,18 APU_PCIE_WAKE#
ISOLATEB
PCIE_WAKE#_R
+LAN_VDD10
+3V_LAN
+LAN_REGOUT
T37
23 LAN_PWRDN — T49 — LAN_PWRDN
LAN_XTALI
LAN_XTALO
+LAN_VDD10
LAN_RST
+3V_LAN
HSOP HSON PERSTB ISOLATEB LANWAKEB DVDD10 VDDREG REGOUT LED2 LED1/GPIO LED0 CKXTAL1 CKXTAL2 AVDD10 RSET AVDD33 GND
425mA
MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10 MDIP3 MDIN3 AVDD33 CLKREQB HSIP HSIN REFCLK_P REFCLK_N
MDI0+ MDI0- +LAN_VDD10 MDI1+ MDI1- MDI2+ MDI2- +LAN_VDD10 MDI3+ MDI3- +3V_LAN LAN_CLKREQ# PCIE_ATX_C_DRX_P1 PCIE_ATX_C_DRX_N1 CLK_PCIE_LAN CLK_PCIE_LAN#
LAN_CLKREQ# 6
PCIE_ATX_C_DRX_P1 5
PCIE_ATX_C_DRX_N1 5
CLK_PCIE_LAN 5
CLK_PCIE_LAN# 5
RTL8111GUS-CG_QFN32_4X4

+3VS — R1238 1K_0402_5% — ISOLATEB — R1242 15K_0402_5%
R1513 2.49K_0402_1%

U47 8106@
RTL8106 EUS-CG
SA00006N900

C1204 15P_0402_50V8J
Y4 25MHZ_12PF_7V25000012
C1205 15P_0402_50V8J
LAN_XTALI
LAN_XTALO

D34 ESDU@
MDI2+ MDI3+ MDI3- MDI2-
AZC099-04S.R7G_SOT23-6
Place Close to T71

Main: SC300001400
2nd: SC300001G00

D35 ESDU@
MDI1+ MDI0+ MDI0- MDI1-
AZC099-04S.R7G_SOT23-6
Place Close to T72

T71
MDI3+ MDI3- MDI2+ MDI2-
MDO3+ MDO3- MCT MCT MDO2+ MDO2-
MHPC_NS681612A
8111@
Main: SP050007T00
2nd: SP050007K00

T72
MDI0+ MDI0- MDI1+ MDI1-
MDO0+ MDO0- MCT MCT MDO1+ MDO1-
MHPC_NS681612A

C1207 0.01U_0402_16V7K

R1521 75_0805_5%
C1206 10P_0603_50V EMIP@
CHASSIS1_GND
DL2 BS4200N-C-LV_SMB-F2 GAS@
Place Close to T71,T72

JRJ1
MDO0+ MDO0- MDO1+ MDO2+ MDO2- MDO1- MDO3+ MDO3-
PR1+ PR1- PR2+ PR3+ PR3- PR2- PR4+ PR4-
GND GND GND GND
CHASSIS1_GND
ME@
SANTA_130460-3
DC231112261

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

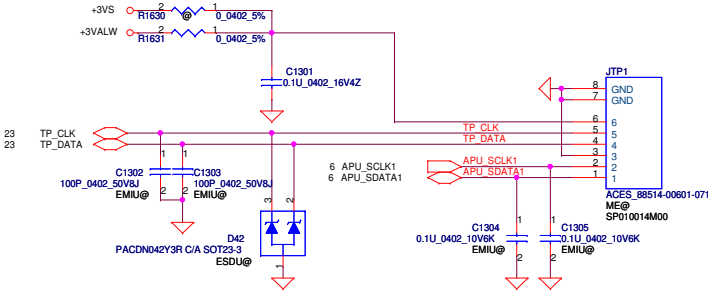
Title: LAN-RTL8111F/8105E

Size	Document Number	Rev
C	LA-A331P	0.1

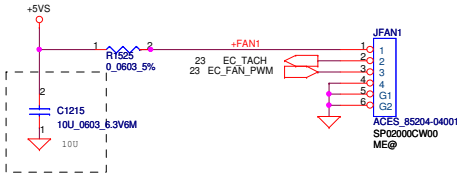
Date: Monday, February 04, 2013 Sheet 19 of 40

INT_KBD Conn.

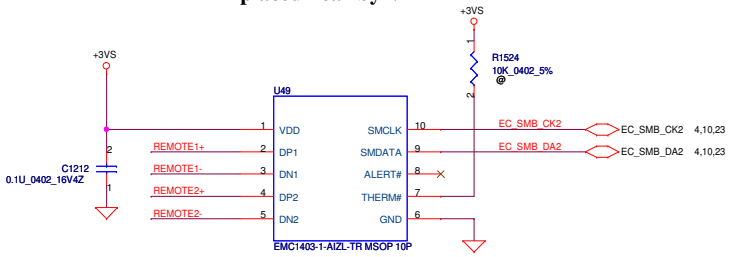
Touch PAD Module



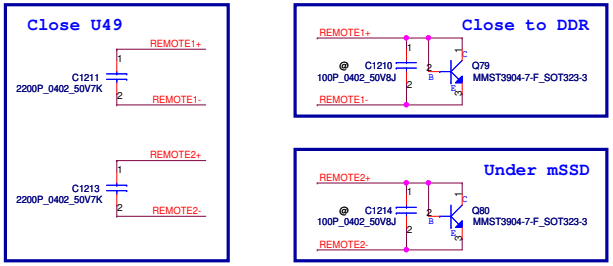
FAN1 Conn



SMSC thermal sensor placed near by VRAM

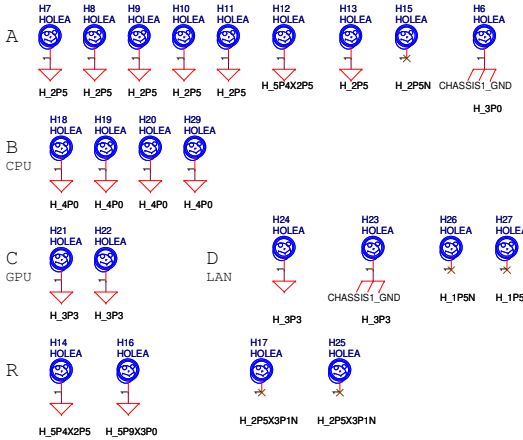


Address 1001_101xb



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Screw Hole



PCB Fedical Mark PAD

FD1 FD2 FD3 FD4

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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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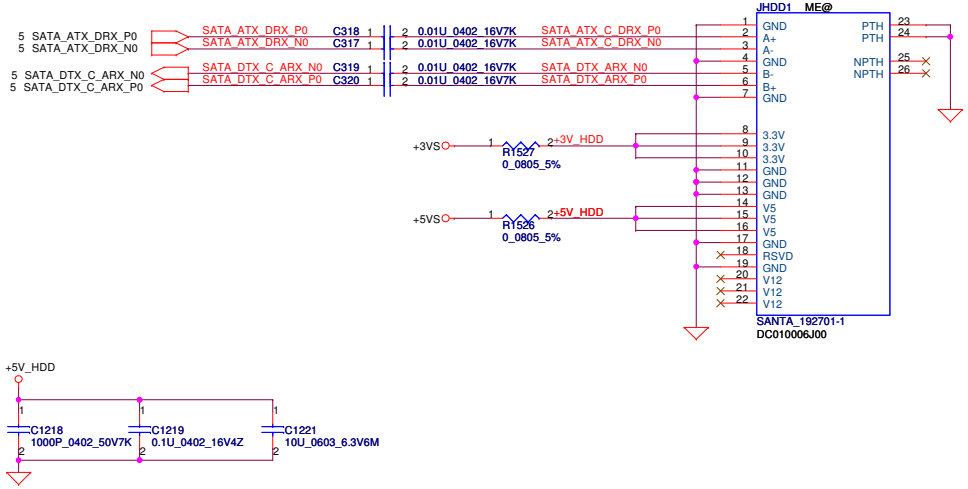
Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

Size	Document Number	Rev
Custom	LA-A331P	0.1

Date: Monday, February 04, 2013 Sheet 20 of 40

SATA HDD Conn.



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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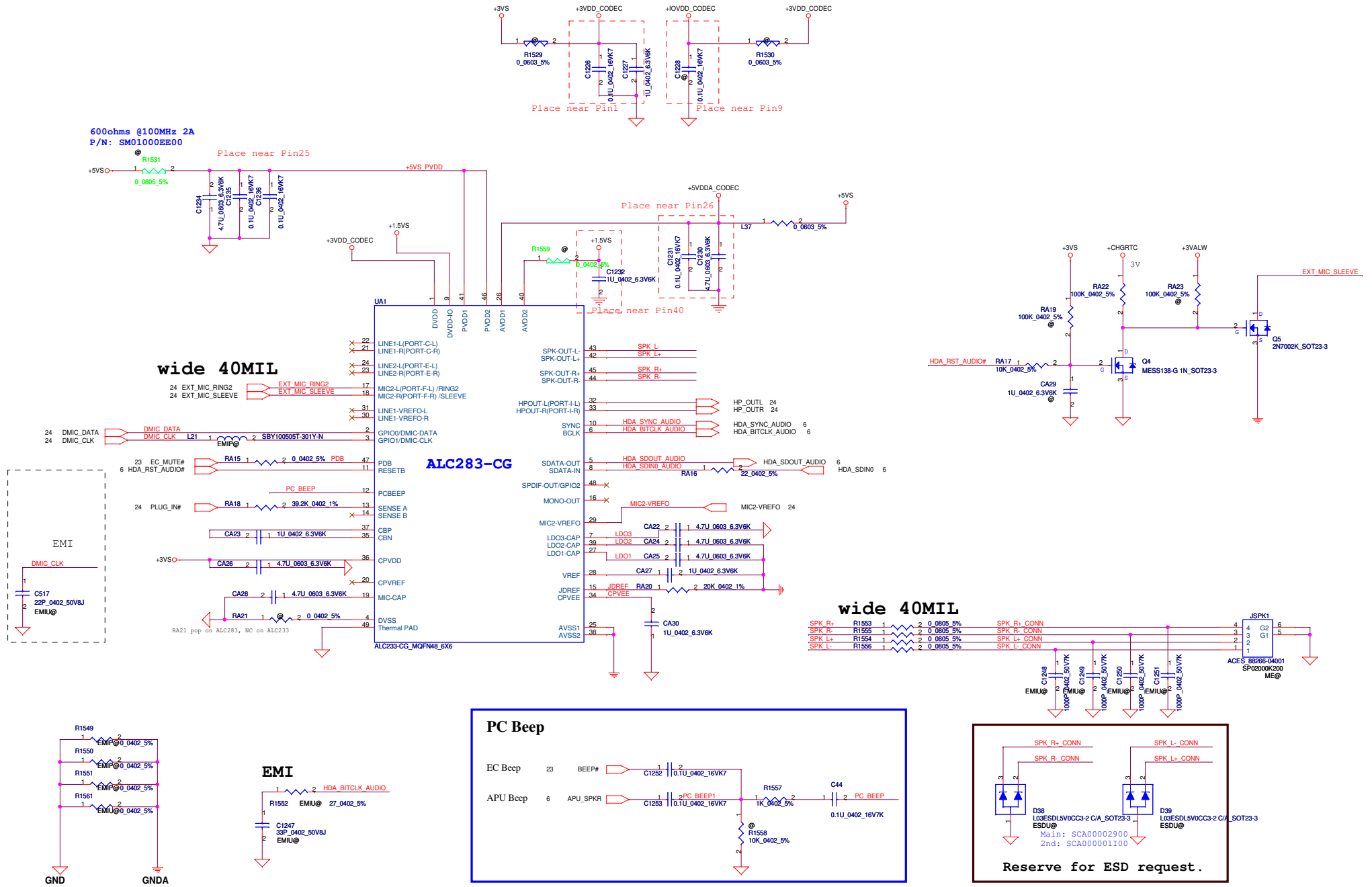
Compal Electronics, Inc.

Title: HDD Connector

Size	Document Number	Rev
Custom	LA-A331P	0.1

Date: Monday, February 04, 2013 Sheet 21 of 40



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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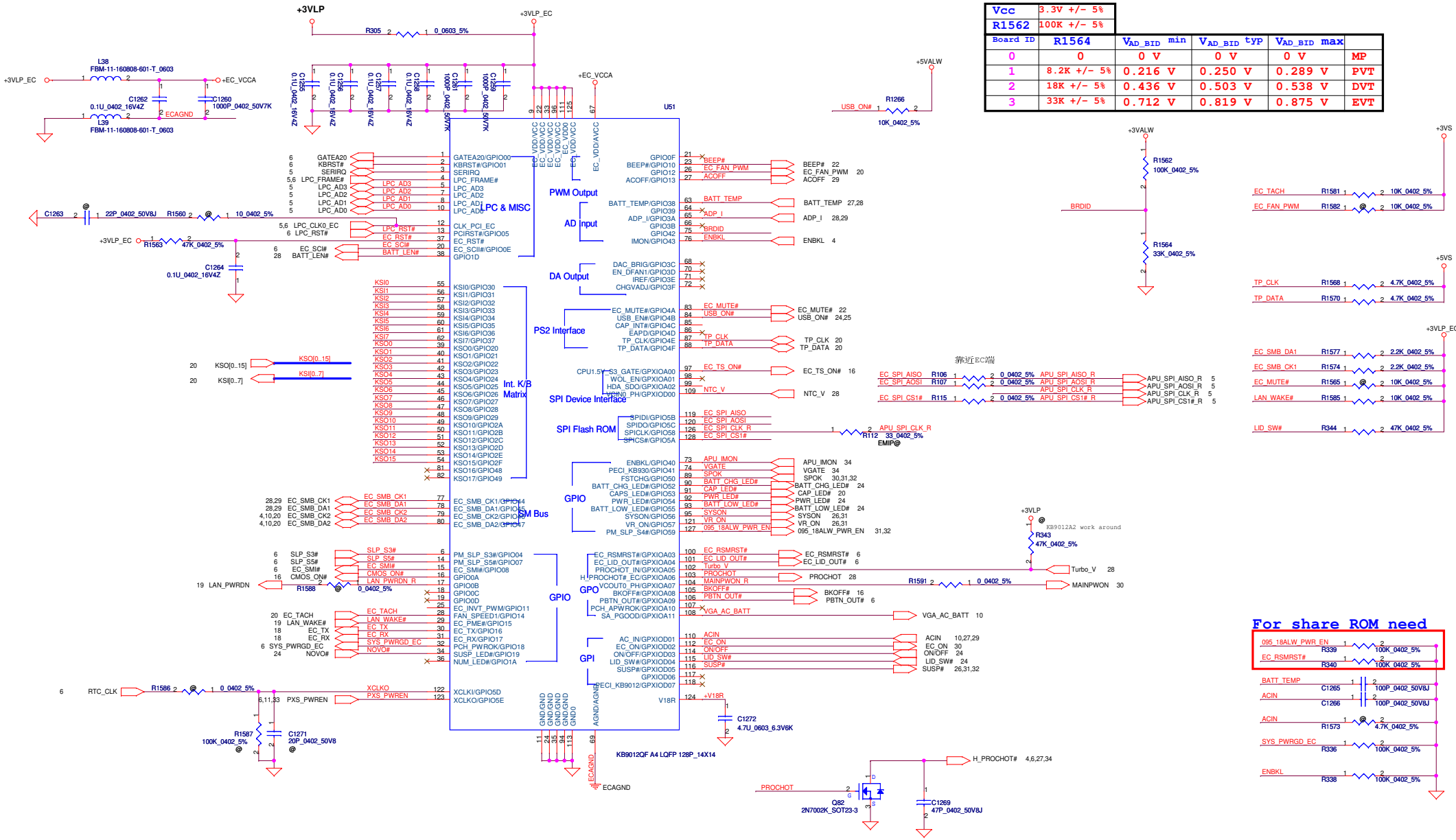
Compal Electronics, Inc.	
Title	HD Audio Codec_ALC259Q-VC
Size: Custom	Document Number: LA-A321PR01
Rev	0.1
Date: Monday, February 04, 2013	Sheet 22 of 40



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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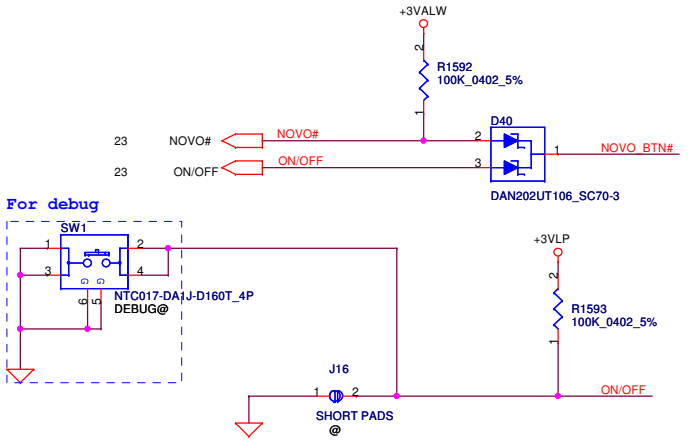
Compal Electronics, Inc.

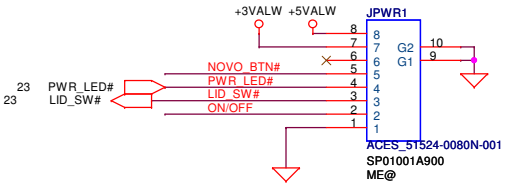
Title: BIOS & EC I/O Port

Size: Custom | Document Number: LA-A331P | Rev: 0.1

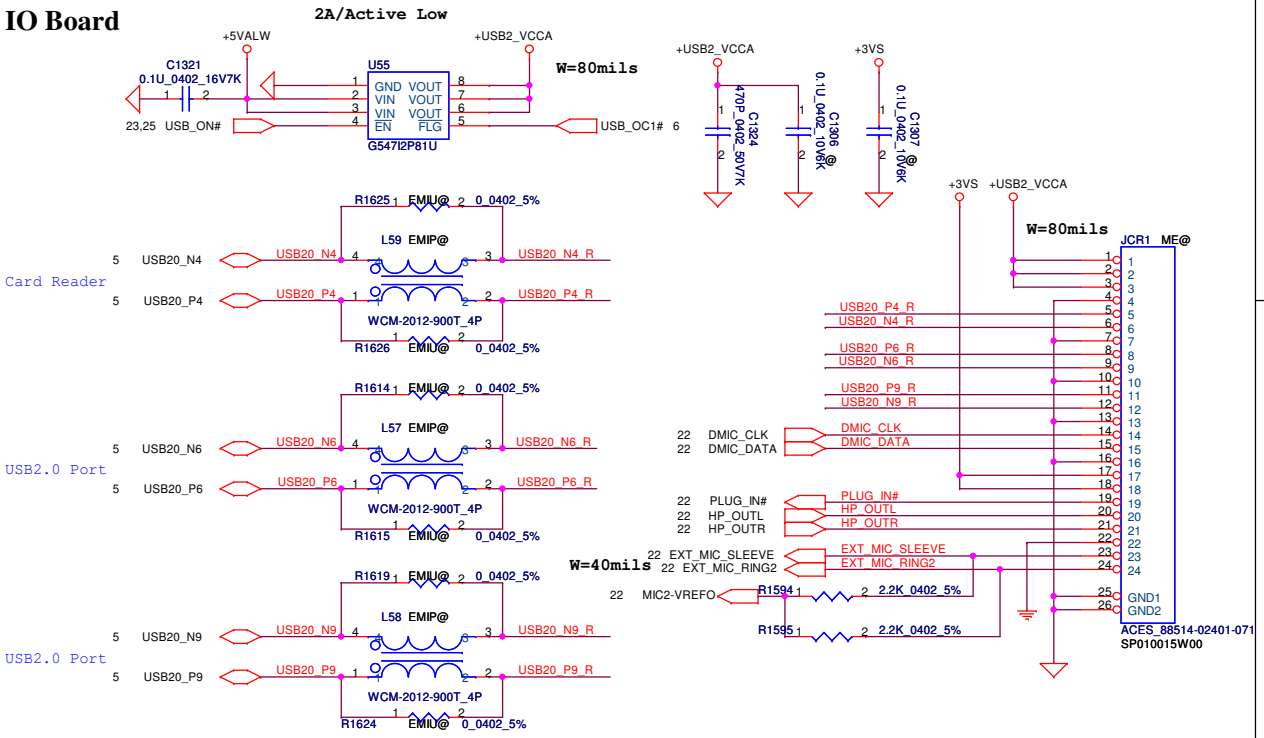
Date: Monday, February 04, 2013 | Sheet 23 of 40



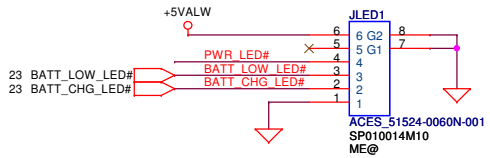
Power Board



IO Board



LED Board



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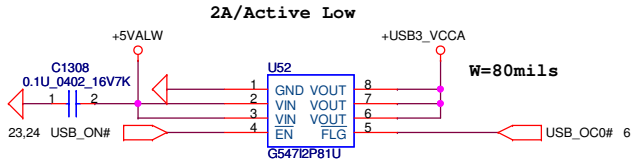
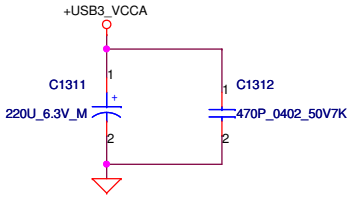
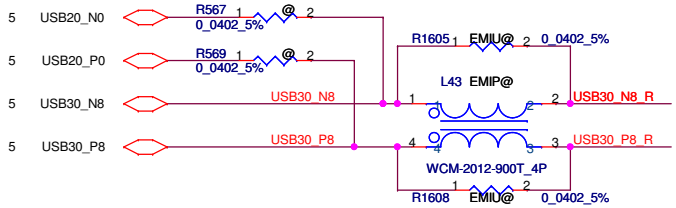
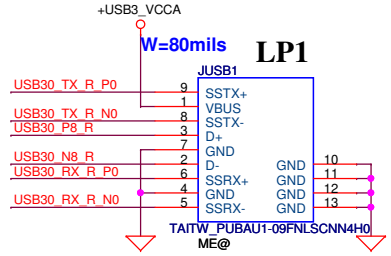
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: Custom	Document Number: LA-A331P		Rev: 0.1
Date: Monday, February 04, 2013	Sheet 24 of 40		

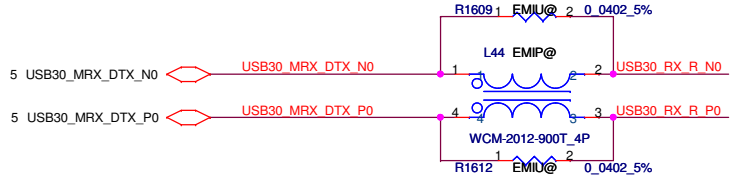


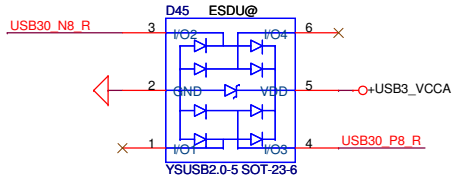


Co-Lay with USB2.0 only

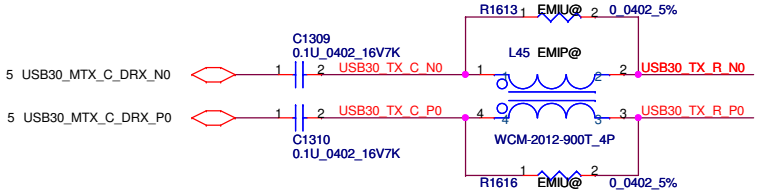




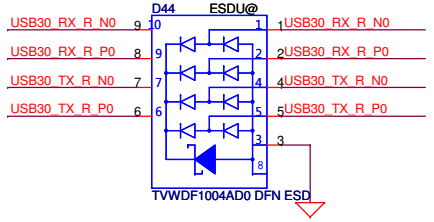




Main: SC300001400
2nd: SC300001G00



Place TX AC coupling Cap (C1309,C1310). Close to connector



Main: SC300002800
2nd: SC300001Y00

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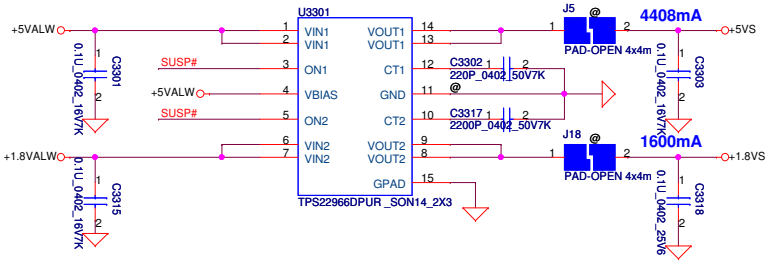
Compal Electronics, Inc.

Title: **USB3.0 ports**

Size: Custom | Document Number: **LA-A331P** | Rev: 0.1

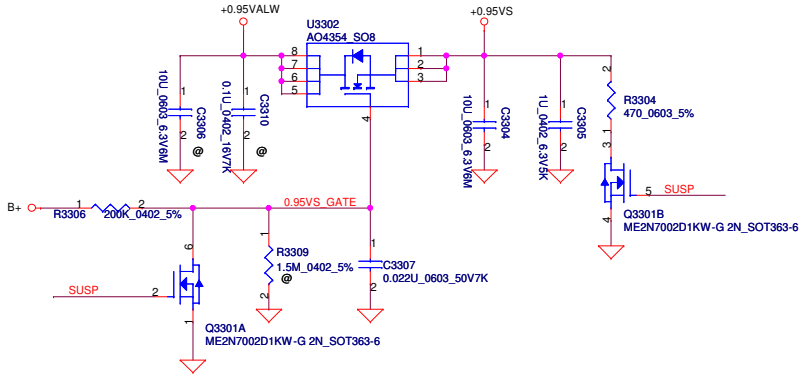
Date: Monday, February 04, 2013 | Sheet 25 of 40

+5VALW to +5VS (4.408A) / +1.8VALW to +1.8VS (2A)

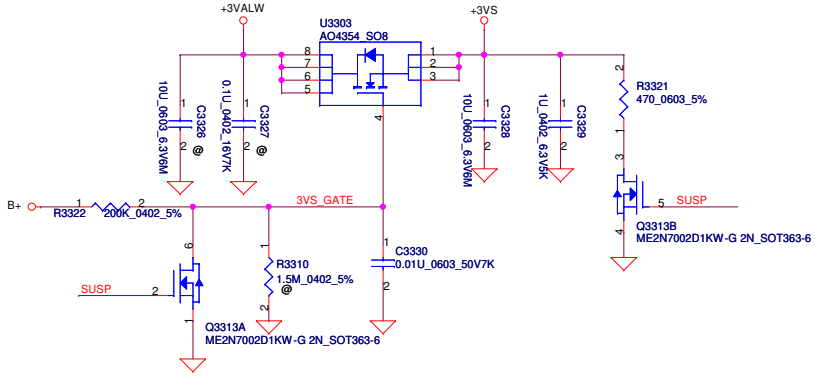


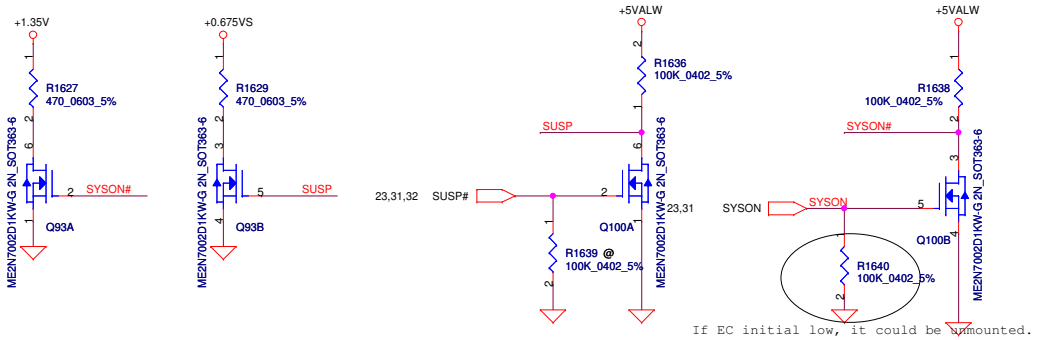
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, AOZ1331 (engineering sample available on 2013/Jan/18)

+0.95VALW TO +0.95VS (5.6A)



+3VALW to +3VS (5.036A)





If EC initial low, it could be unmounted.

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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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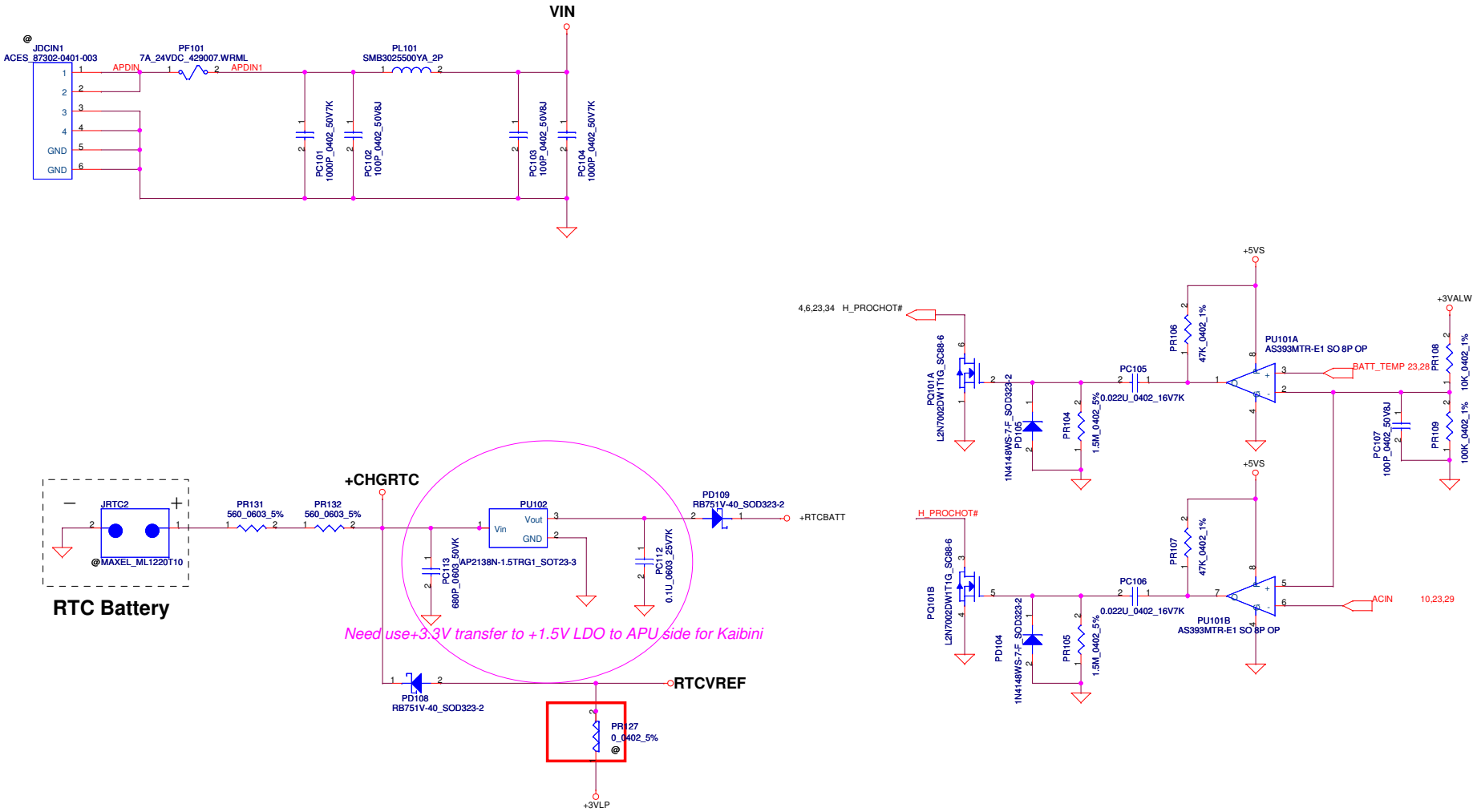
Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
Custom	LA-A331P	0.1

Date: Monday, February 04, 2013 Sheet 26 of 40



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: PWR-DCIN / Vin Detector

Size: Custom | Document Number: C38-AMD KABINI Schematic | Rev: 0.1

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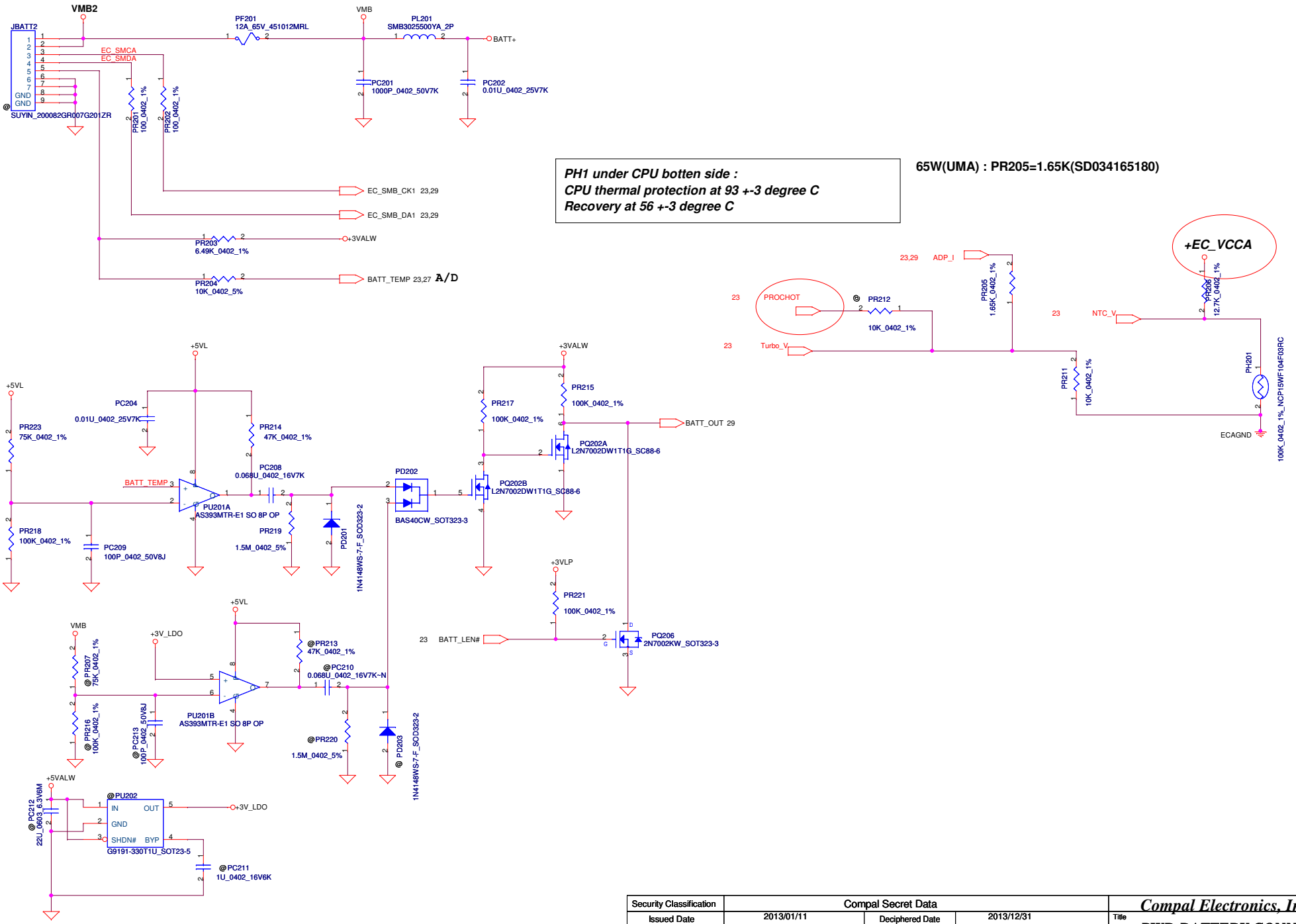
JBATT2 Just for 14"



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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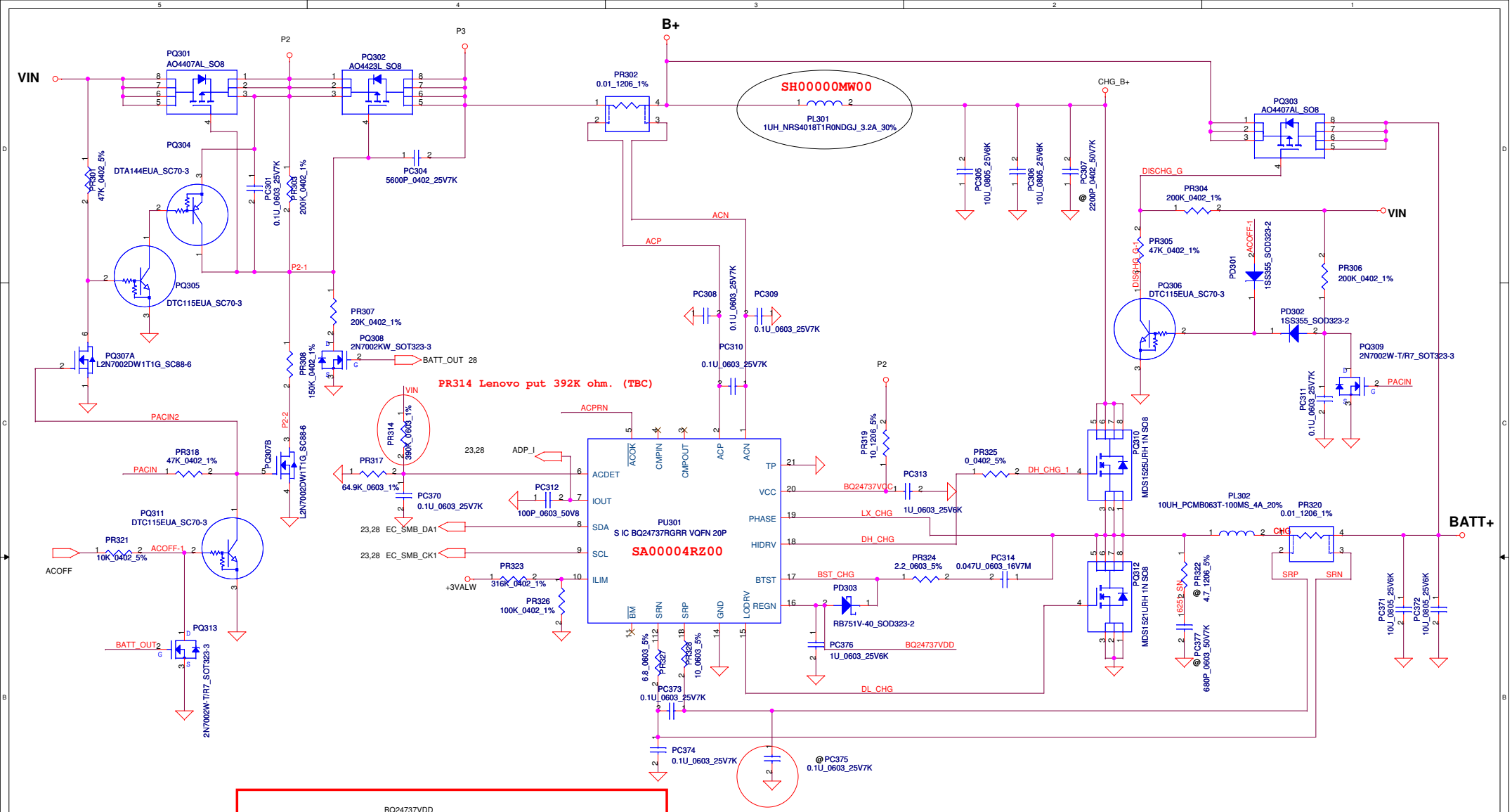
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: C38-AMD KABINI Schematic | Rev: 0.1

Date: Monday, February 04, 2013 | Sheet 28 of 40



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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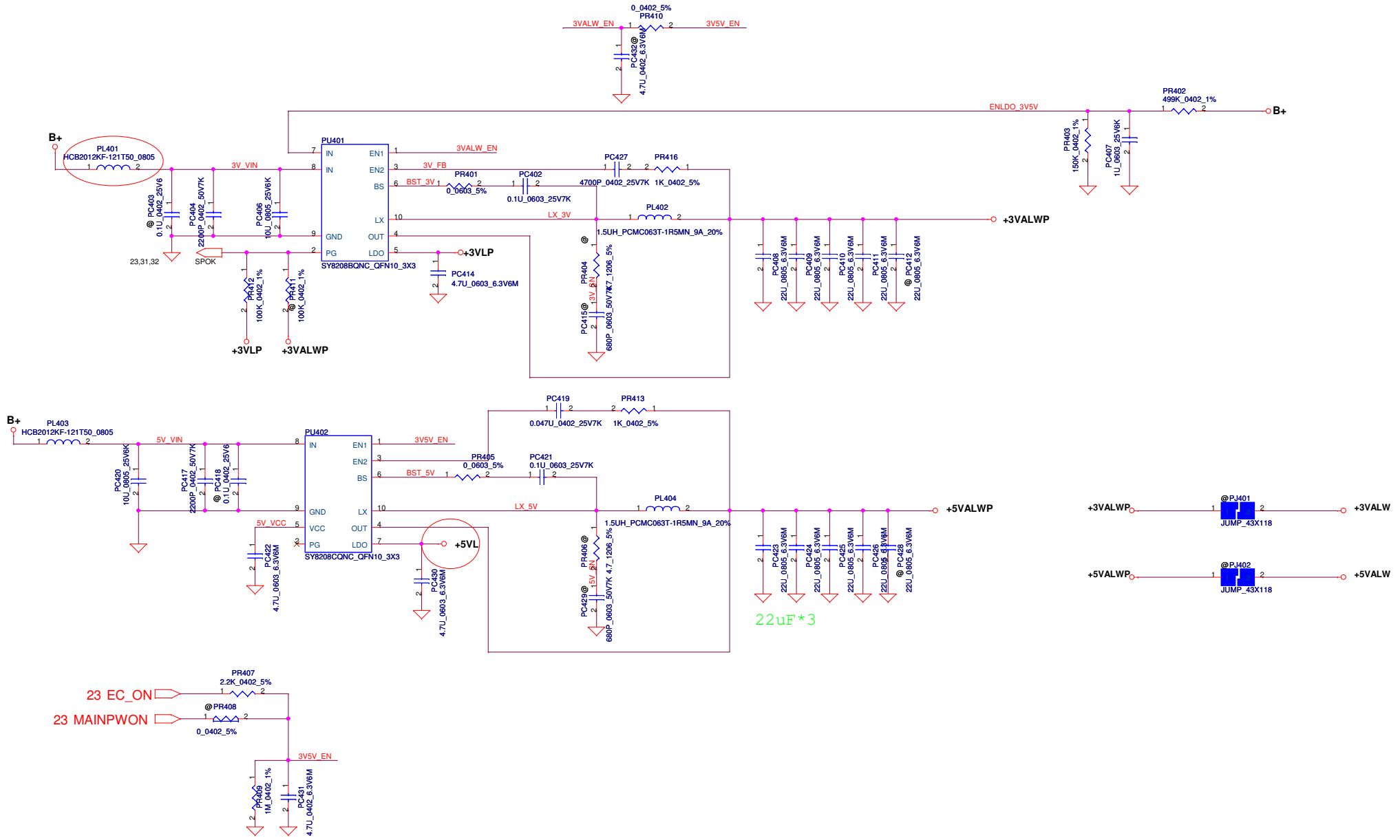
Compal Electronics, Inc.

Title: PWR-CHARGER

Size	Document Number	Rev
	C38-AMD KABINI Schematic	0.1

Date: Monday, February 04, 2013 | Sheet 29 of 40



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

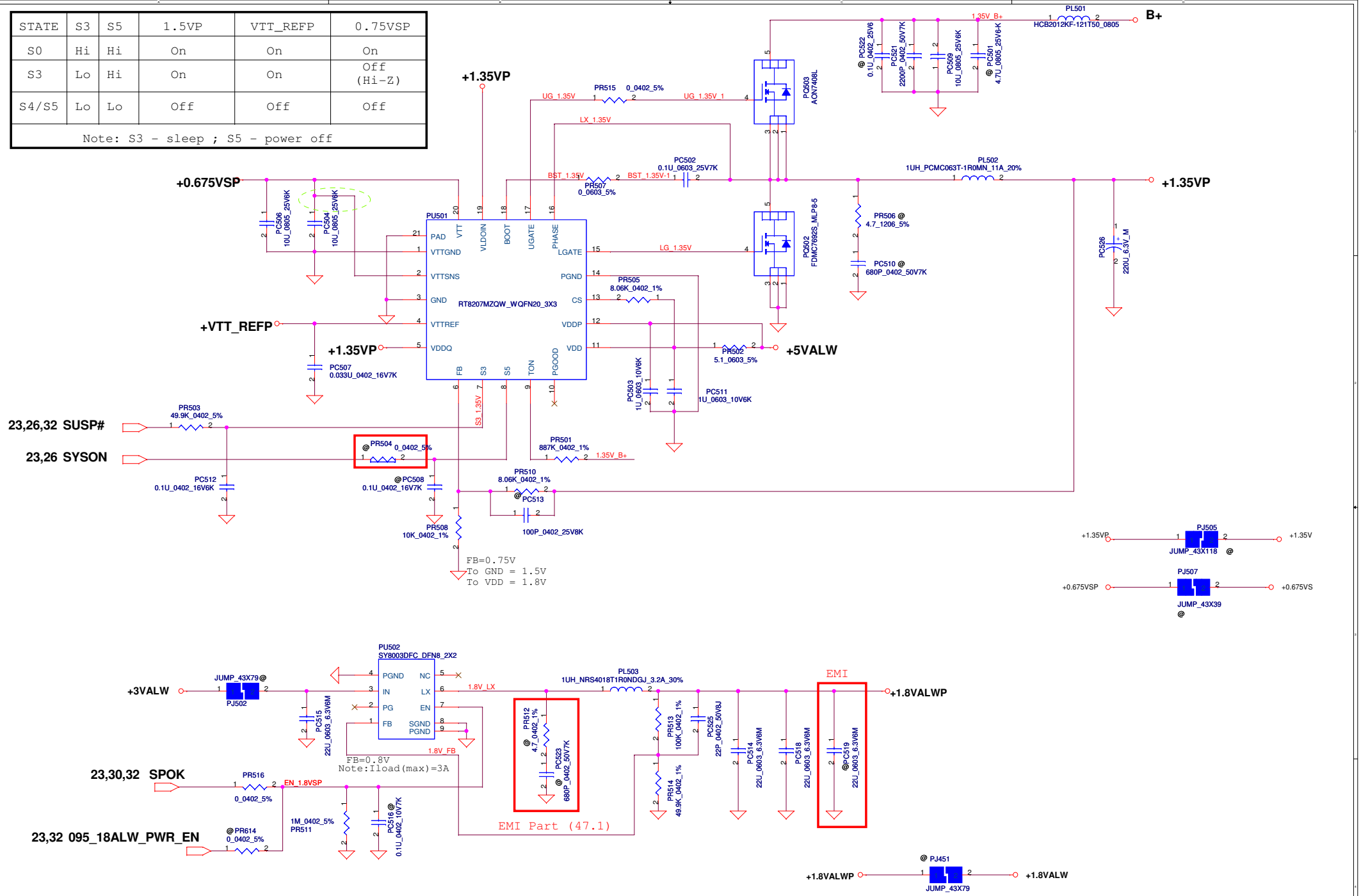
Title: PWR-+3VALW/+5VALW

Size: Custom | Document Number: C38-AMD KABINI Schematic | Rev: 0.1

Date: Monday, February 04, 2013 | Sheet 30 of 40

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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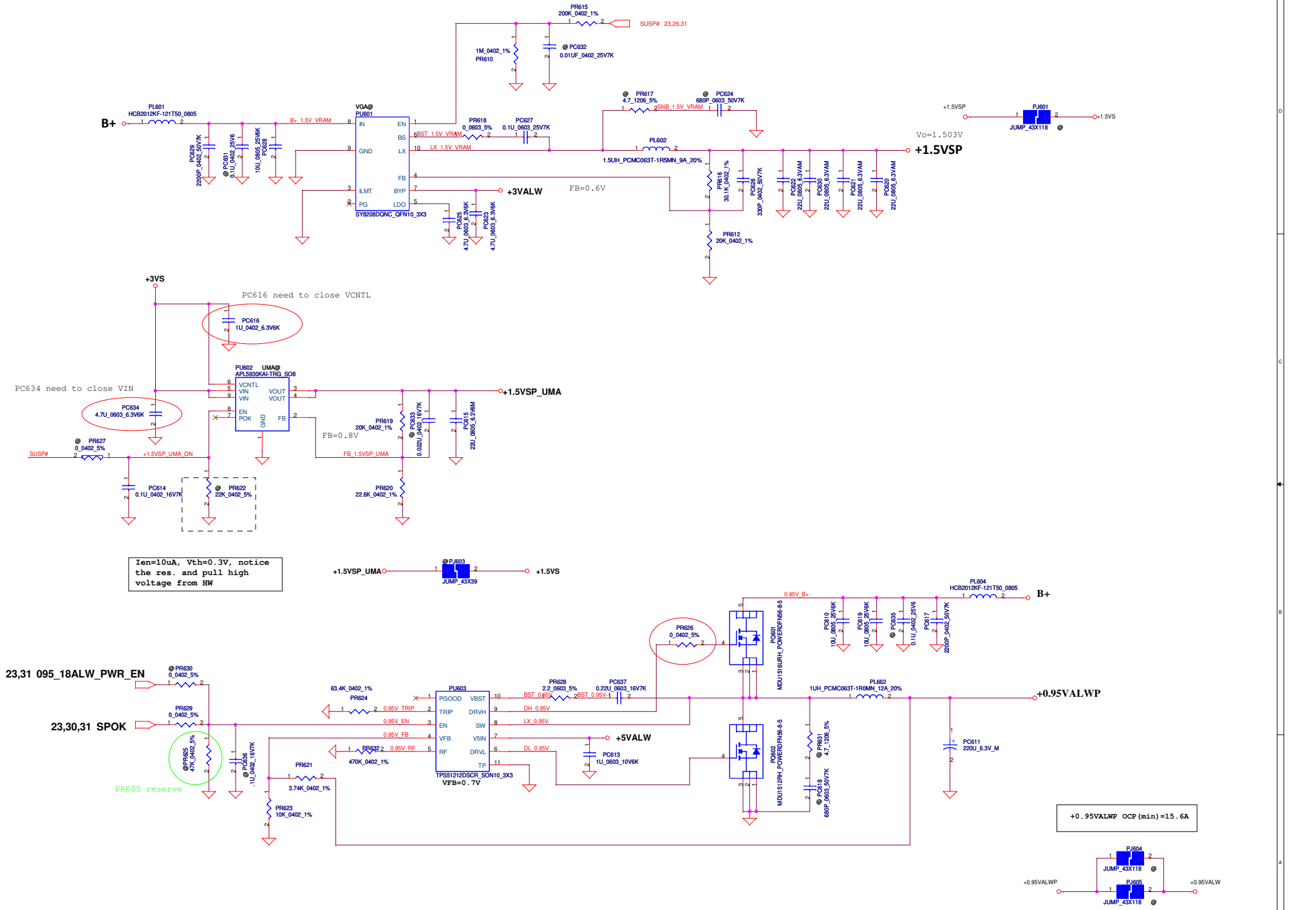
Compal Electronics, Inc.

Title: PWR-+1.35VP/+1.8VSP

Size: Custom | Document Number: C38-AMD KABINI Schematic | Rev: 0.1

Date: Monday, February 04, 2013 | Sheet 31 of 40



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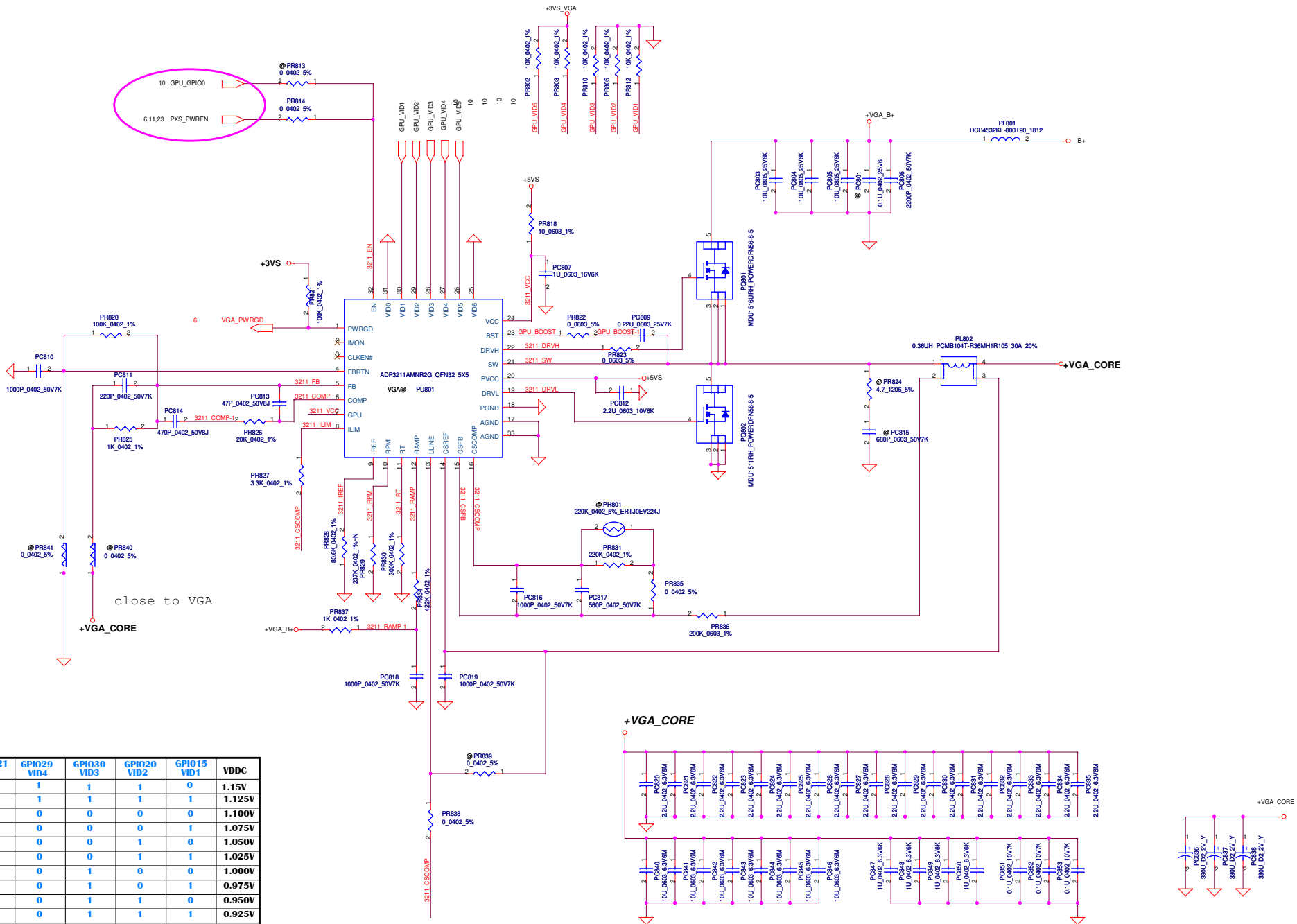
Compal Electronics, Inc.

Title: +1.5VSP(VRAM)

Size	Document Number	Rev
C	C38-AMD KABINI Schematic	0.1

Date: Monday, February 04, 2013 Sheet 32 of 40



GPIO21 VID5	GPIO29 VID4	GPIO30 VID3	GPIO20 VID2	GPIO15 VID1	VDDC	
0	1	1	1	0	1.15V	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	Default
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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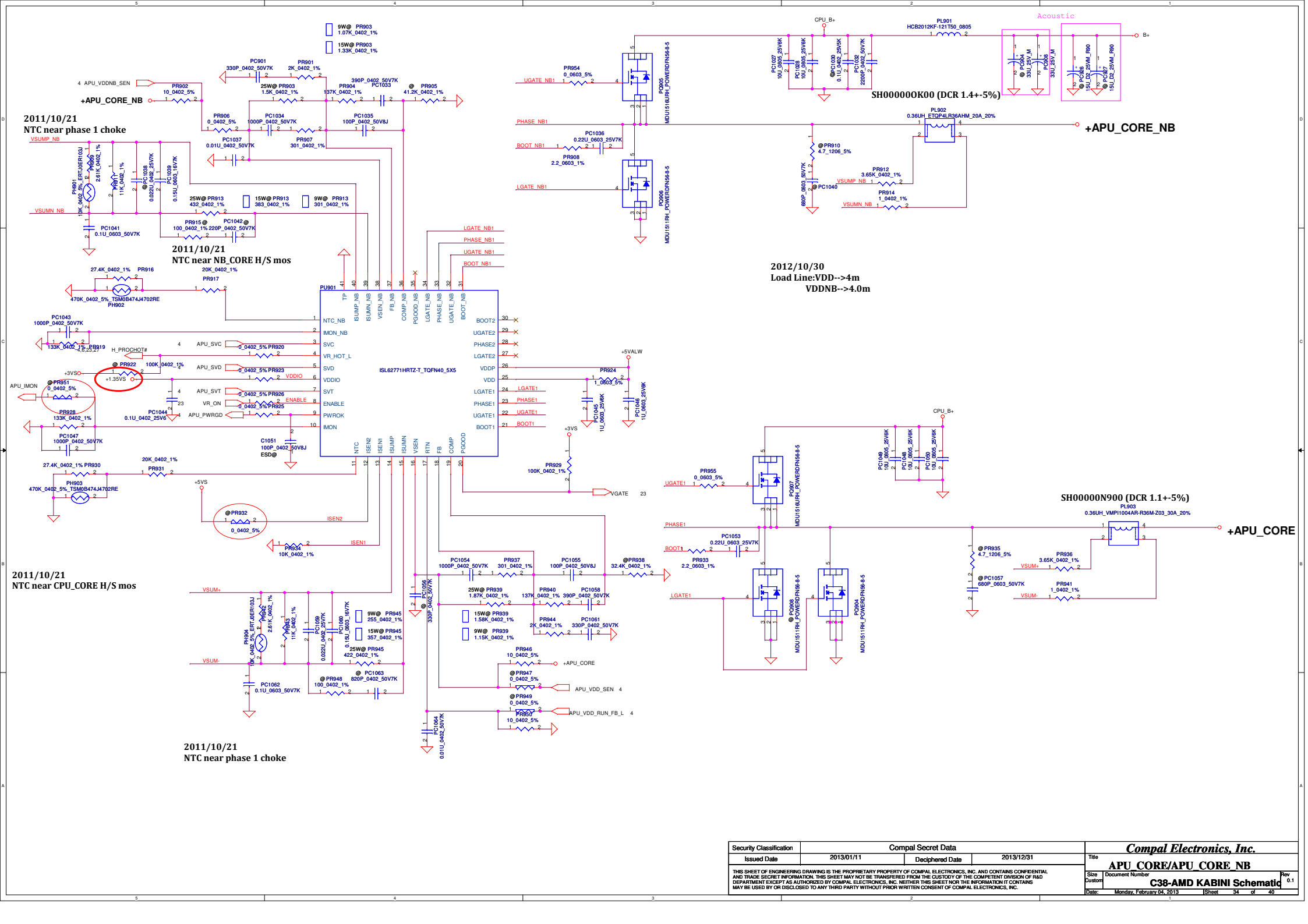
Compal Electronics, Inc.

Title: PWR-VGA_CORE

Size: C | Document Number: C38-AMD KABIN Schematic | Rev: 0.1

Date: Monday, February 04, 2013 | Sheet 33 of 40



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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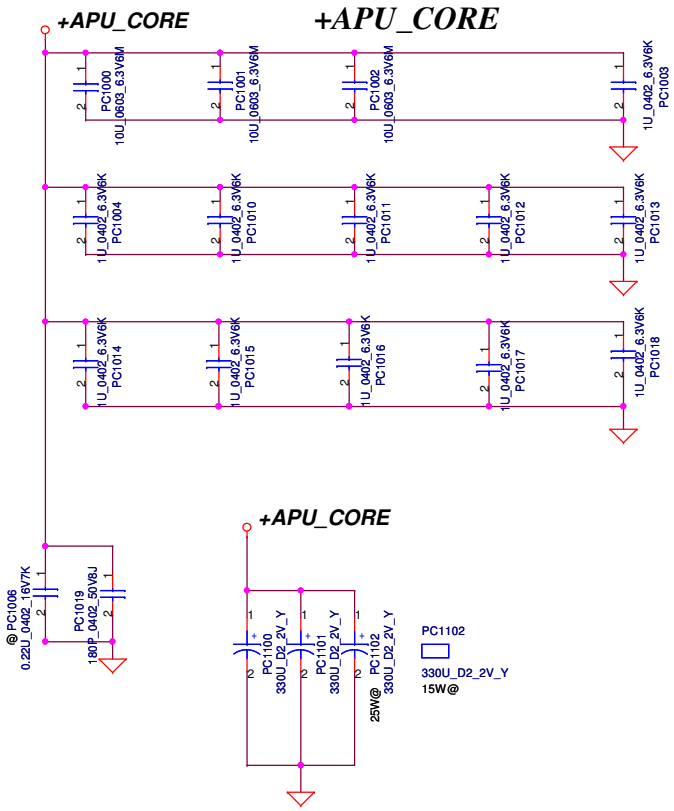
Compal Electronics, Inc.

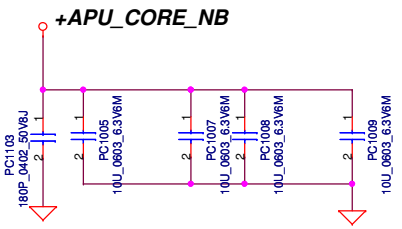
Title: APU_CORE/APU_CORE_NB

Size: Custom | Document Number: C38-AMD KABINI Schematic | Rev: 0.1

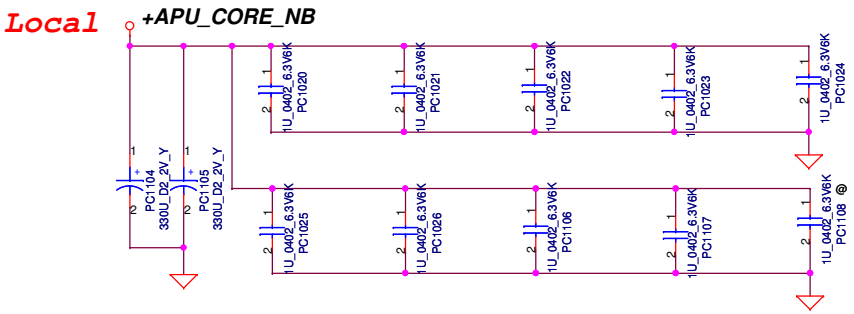
Date: Monday, February 04, 2013 | Sheet 34 of 40

CPU_Core output CAP (Including MLCC) 36.4





GFX output CAP (Including MLCC) 36.5



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: PWR-PROCESSOR DECOUPLING

Size	Document Number	Rev
A3	C38-AMD KABINI Schematic	0.1

Date: Monday, February 04, 2013 | Sheet 35 of 40

Version change list (P.I.R. List)

Item	Modify List	PG#	Reason for change	Date	Phase
1					
2					
3					
4					
5					
6					
7					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **PIR (PWR)**

Size: Custom | Document Number: **C38-AMD KABINI Schematic** | Rev: 0.1

Date: Monday, February 04, 2013 | Sheet 36 of 40

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For share rom	28	Change SYS_PWRGD_EC from pin 86 to pin 32	12/17	DVT
2	For 095VS_PWR_EN pull down	28	Add R207	12/17	DVT
3	For VBIAS first raise up	12, 32	Change U1895V, U35P, U1895P VBIAS from +5VALW to VL	12/17	DVT
4	For follow VIWGP design	27	Change JUSB3 pin define	12/18	DVT
5	For Audio Precision	31	Change CA36, CA46 from 1U to 2.2U	12/21	DVT
6	For SYS_PWRGD_EC pull down	28	Add R208	12/24	DVT
7	For share rom	28	Change R1575, R1576 to 100K	12/24	DVT
8	For reserve EC +3VL	28 05	Add J11, J12 and modify +3VALW to +3V_EC	12/24	DVT
9	For share ROM	05	modify ROM net-name & resistor value	12/24	DVT
10	For common VIWGP design	22	modify R106, R107 to 22ohm	12/24	DVT
11	For power S3 reduction	28	Change EC_INVT_PWM to ADP_ID_CLOSE	12/25	DVT
12	For common VIWGP design	23	Change JODD1 symbol	12/27	DVT
13	For reserve wake on wlan function	26	Add R1500	12/27	DVT
14	For 1.5VS discharge	32	Change R339 to 0ohm, mount Q23 & R1461	12/29	DVT
15	For AMD suggest	4	Change R576 to 0ohm	12/29	DVT
16	For VGA sequence	12	Delete R123 & C40, change C28, C27 to 2200P	12/29	DVT
17	For +3VALW APU Power Consumption	7	Add R582	01/03	DVT
18	For ESD request	22 28 40	Add C600, C601, PC6601, PC6602	01/03	DVT

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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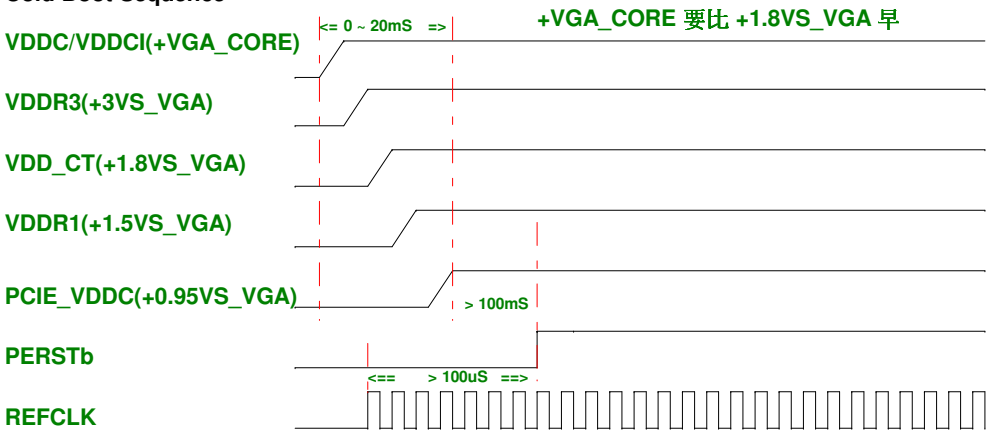
Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1
Date: Monday, February 04, 2013 | Sheet 37 of 40

Power-Up/Down Sequence

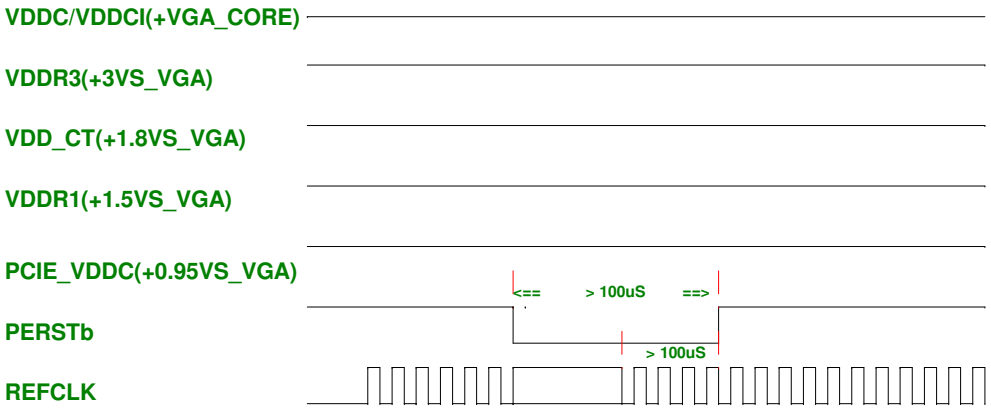
"Sun" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

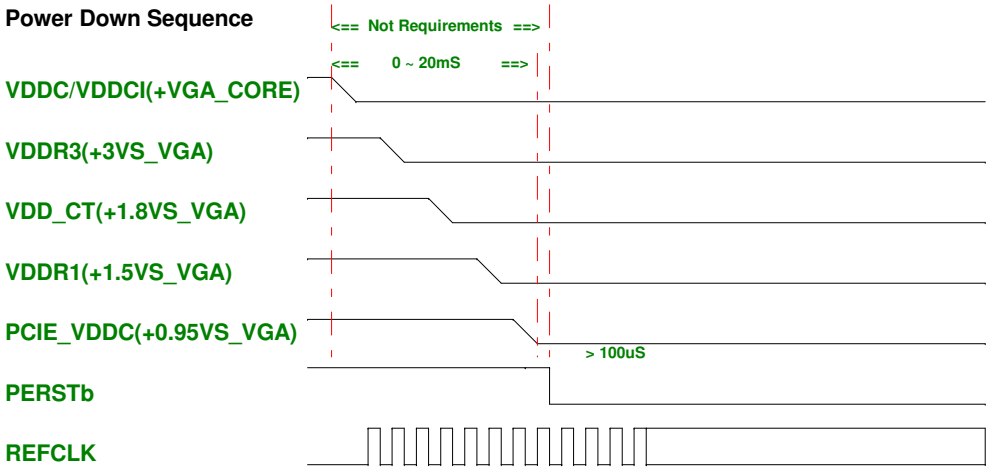
Cold Boot Sequence



Warm Boot Sequence



Power Down Sequence



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Compal Electronics, Inc.

Title: VGA Notes List

Size	Document Number	Rev
Custom	LA-A331P	0.1

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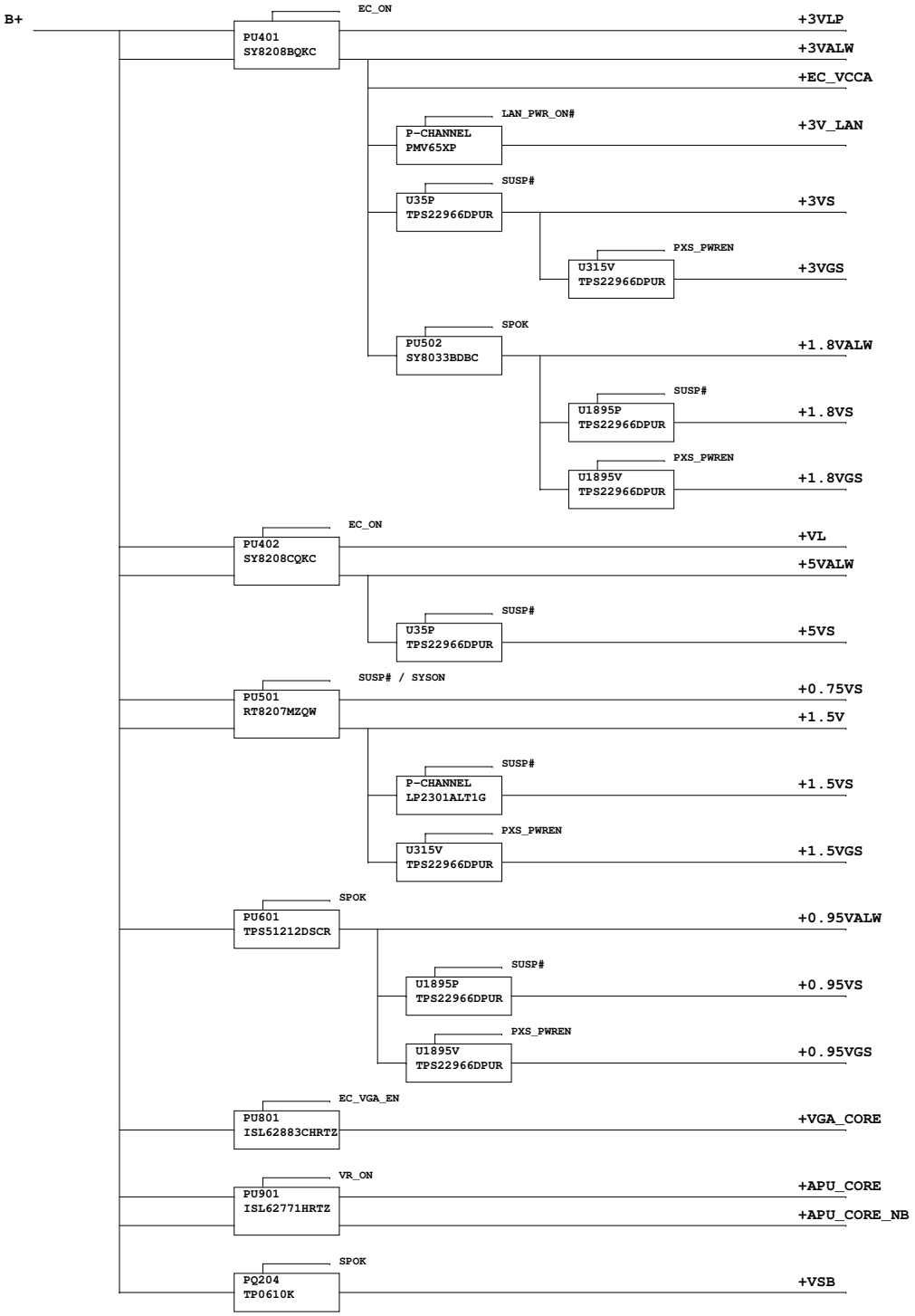

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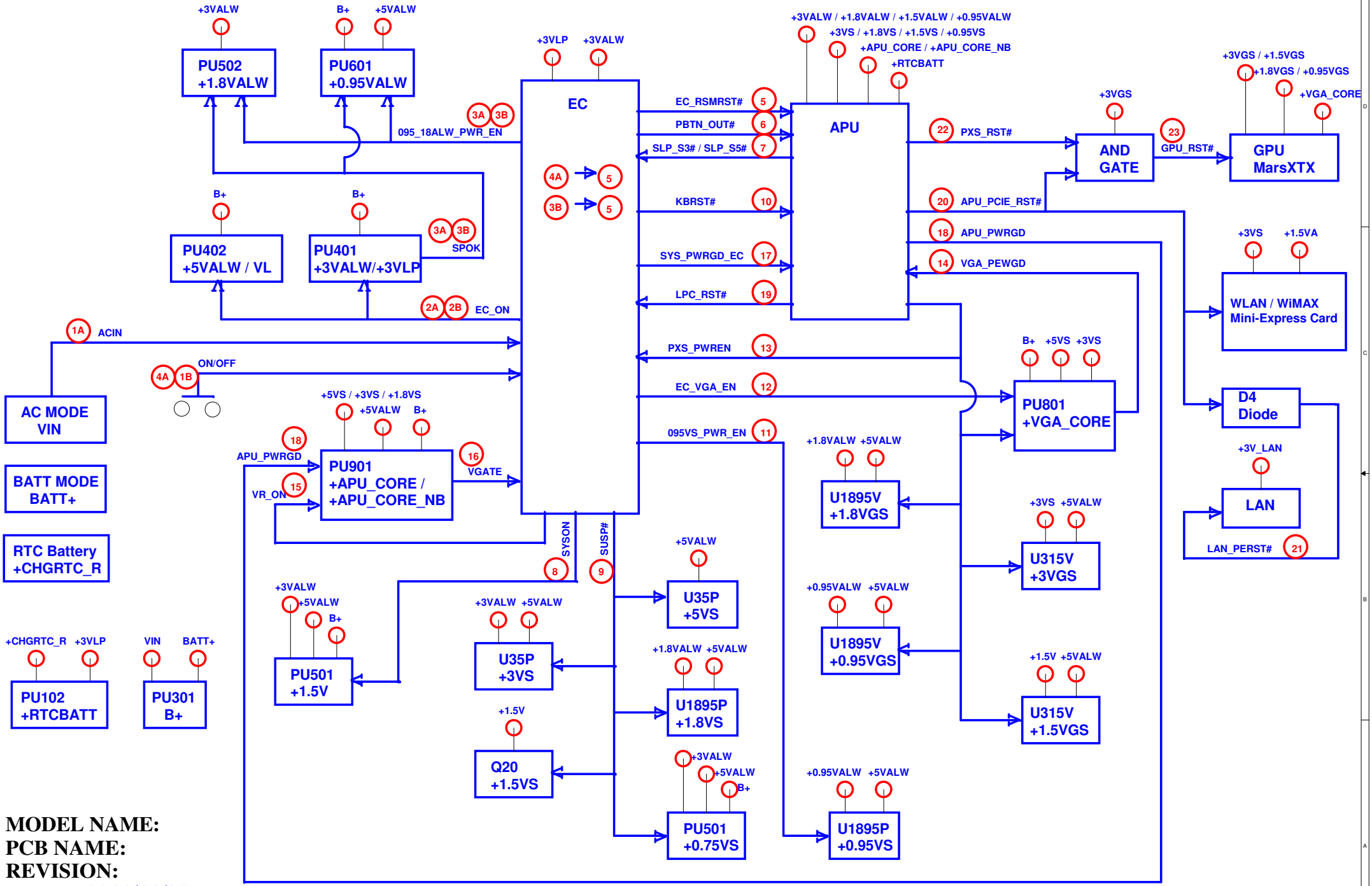
Compal Electronics, Inc.

Title: **Power Map**

Size	Document Number	Rev
Custom	LA-A331P	0.1

Date: Monday, February 04, 2013 | Sheet 39 of 40



MODEL NAME:
PCB NAME:
REVISION:
DATE: *2011/11/23*

COMPAL CONFIDENTIAL

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Title: ***Power sequence***

Size	Document Number	Rev
Custom		0.1

Date: Sheet of