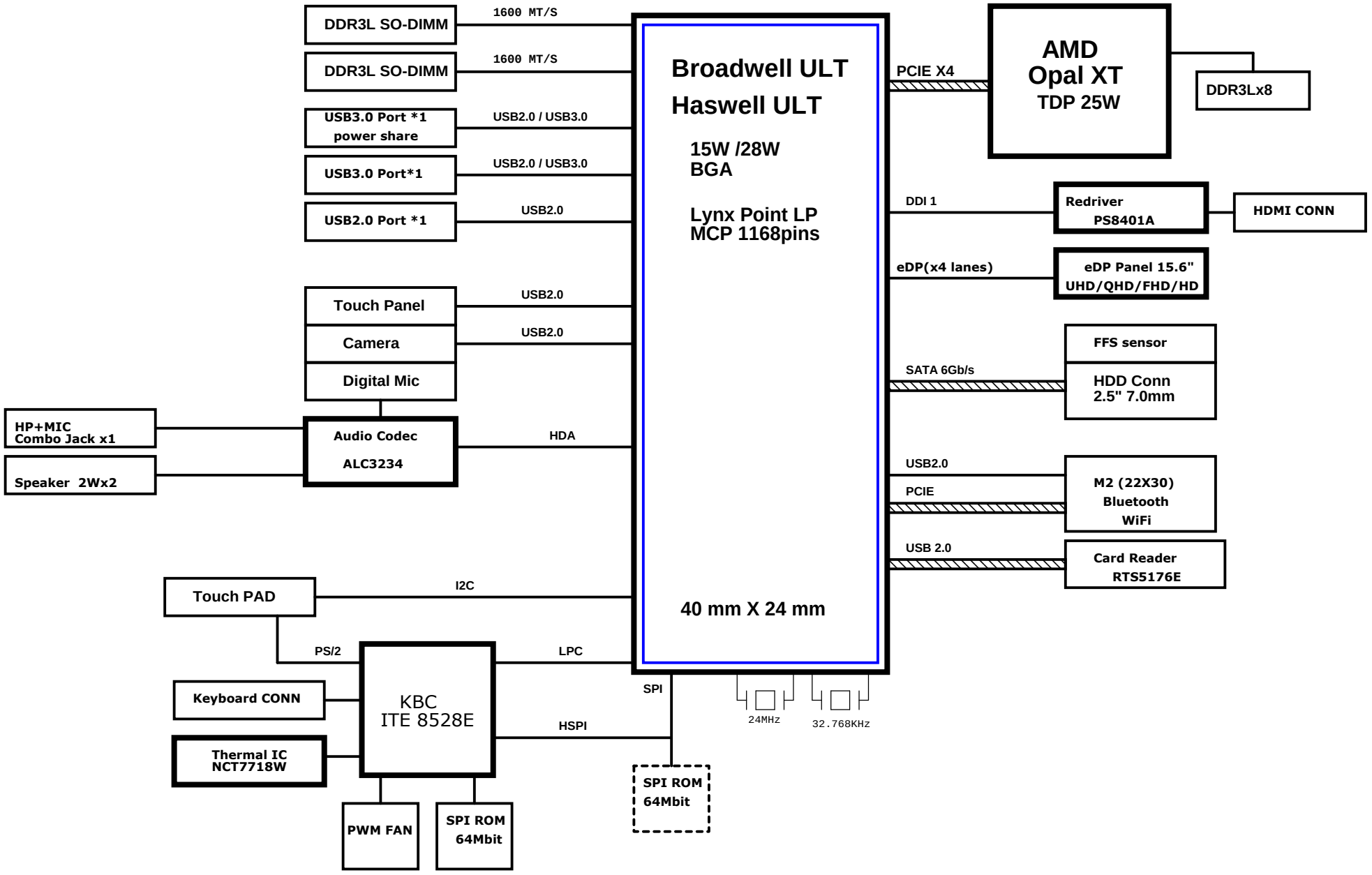
AM6 BLOCK DIAGRAM



Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Block Diagram	A

Date: Monday, May 05, 2014 Sheet 1 of 58

HSIO Port	USB3.0	PCIE	SATA
1	USB3.0_1 Left Power Share		
2	USB3.0_2 Right		
3	USB3.0_3 X	PCIE1 X	
4	USB3.0_4 X	PCIE2 X	
5		PCIE3 X	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 X
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

PCIE CLK
CLK0 X
CLK1 X
CLK2 X
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

USB2.0
USB2.0_0 Left Power Share
USB2.0_1 Right /w 3.0
USB2.0_2 Right
USB2.0_3 Card Reader
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 X

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Size	Document Number	Rev
	PORT ASSIGNMENT	A

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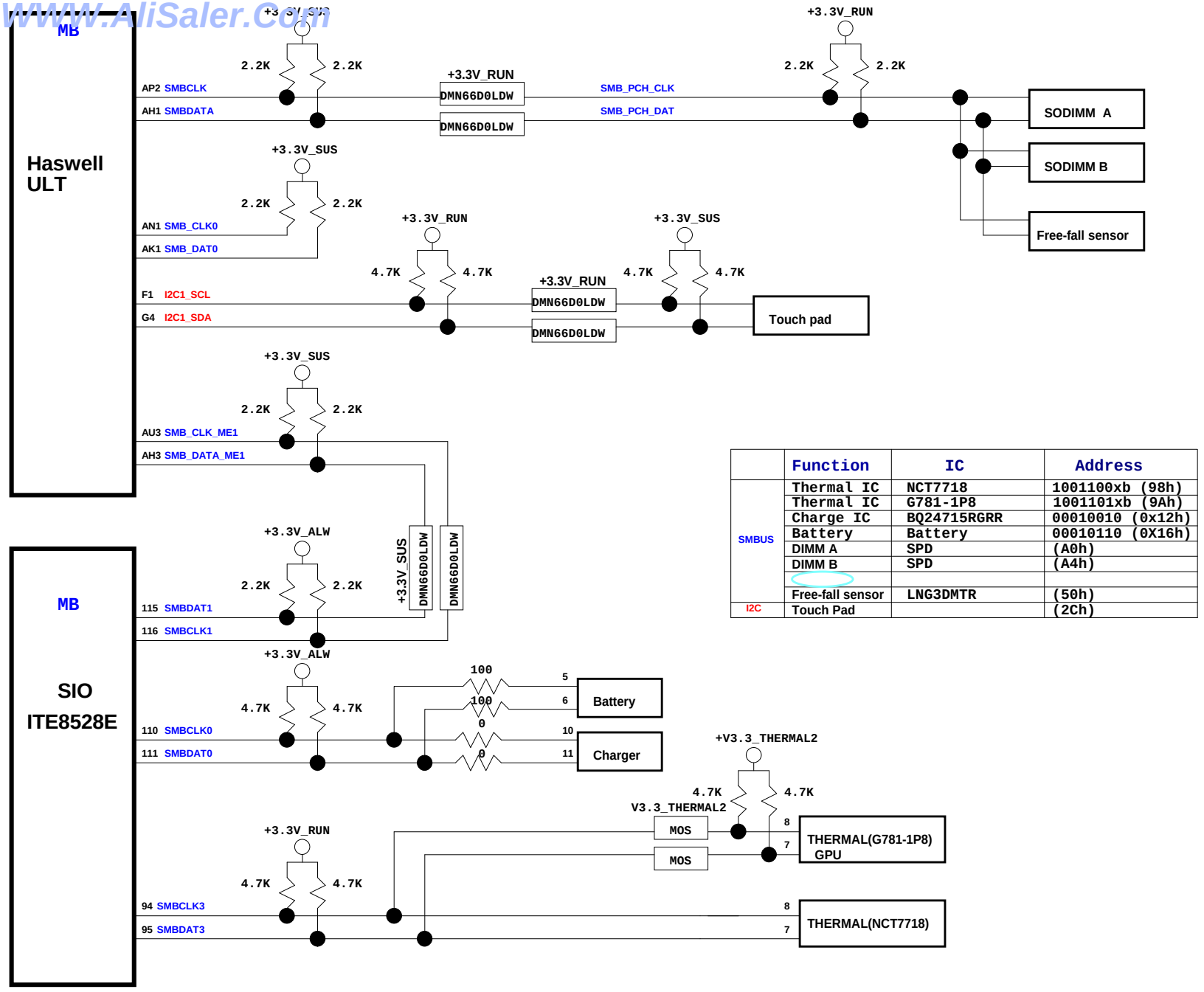

	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	BQ24715RGRR	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	DIMM A	SPD	(A0h)
	DIMM B	SPD	(A4h)
	Free-fall sensor	LNG3DMTR	(50h)
I2C	Touch Pad		(2Ch)

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Size	Document Number	Rev
	SMBUS	A

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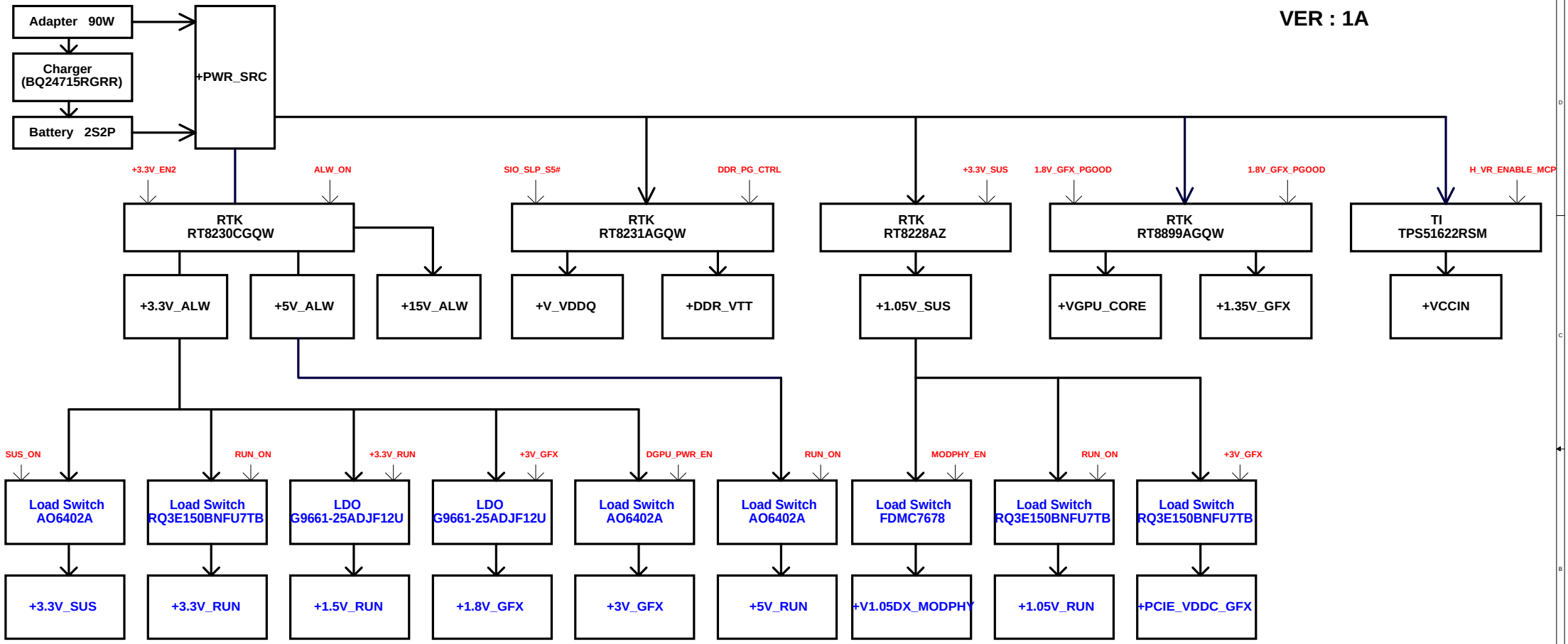
VER : 1A



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PROJECT : AM6

Size	Document Number	Rev
	Power Block Diagram	A

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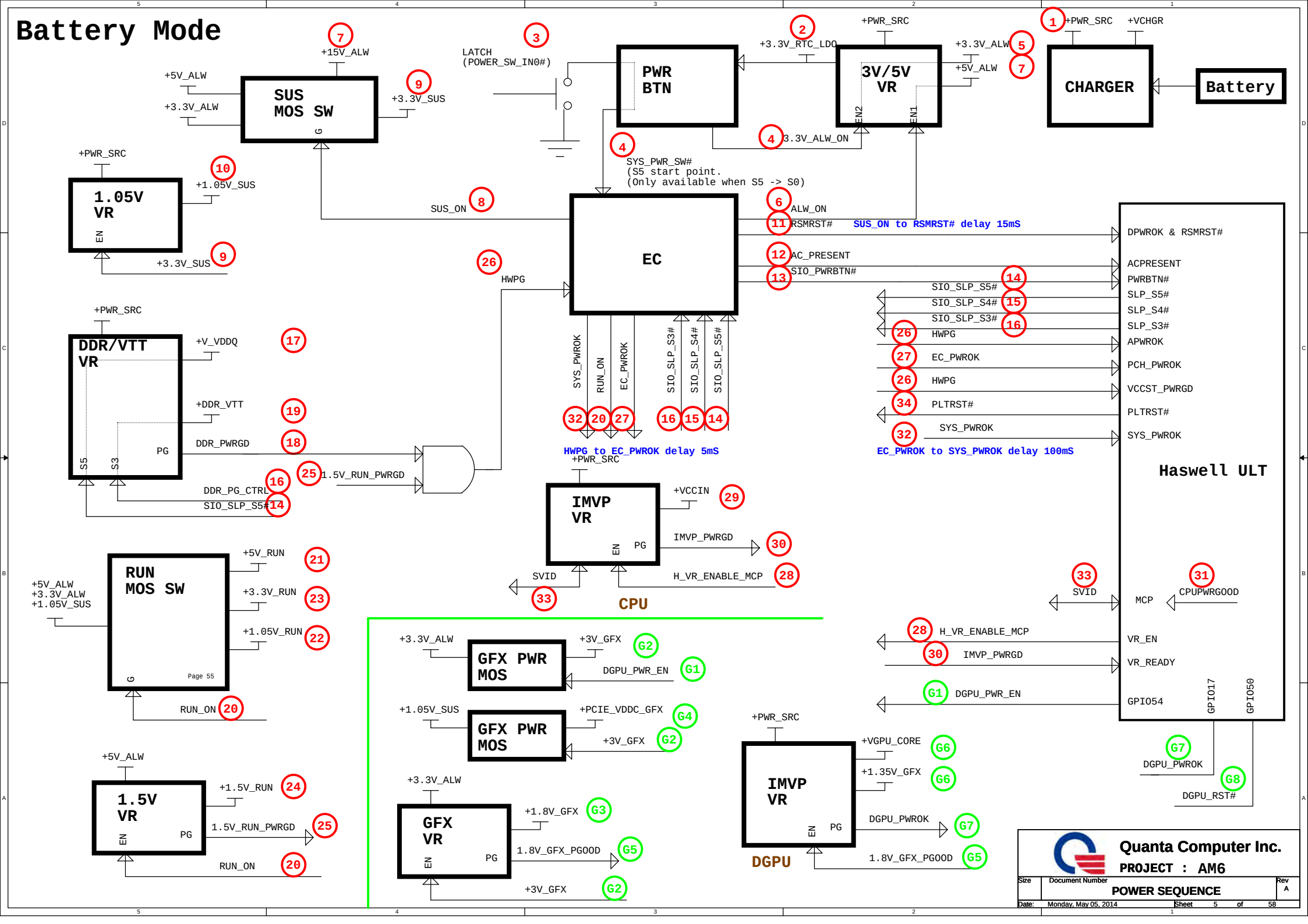
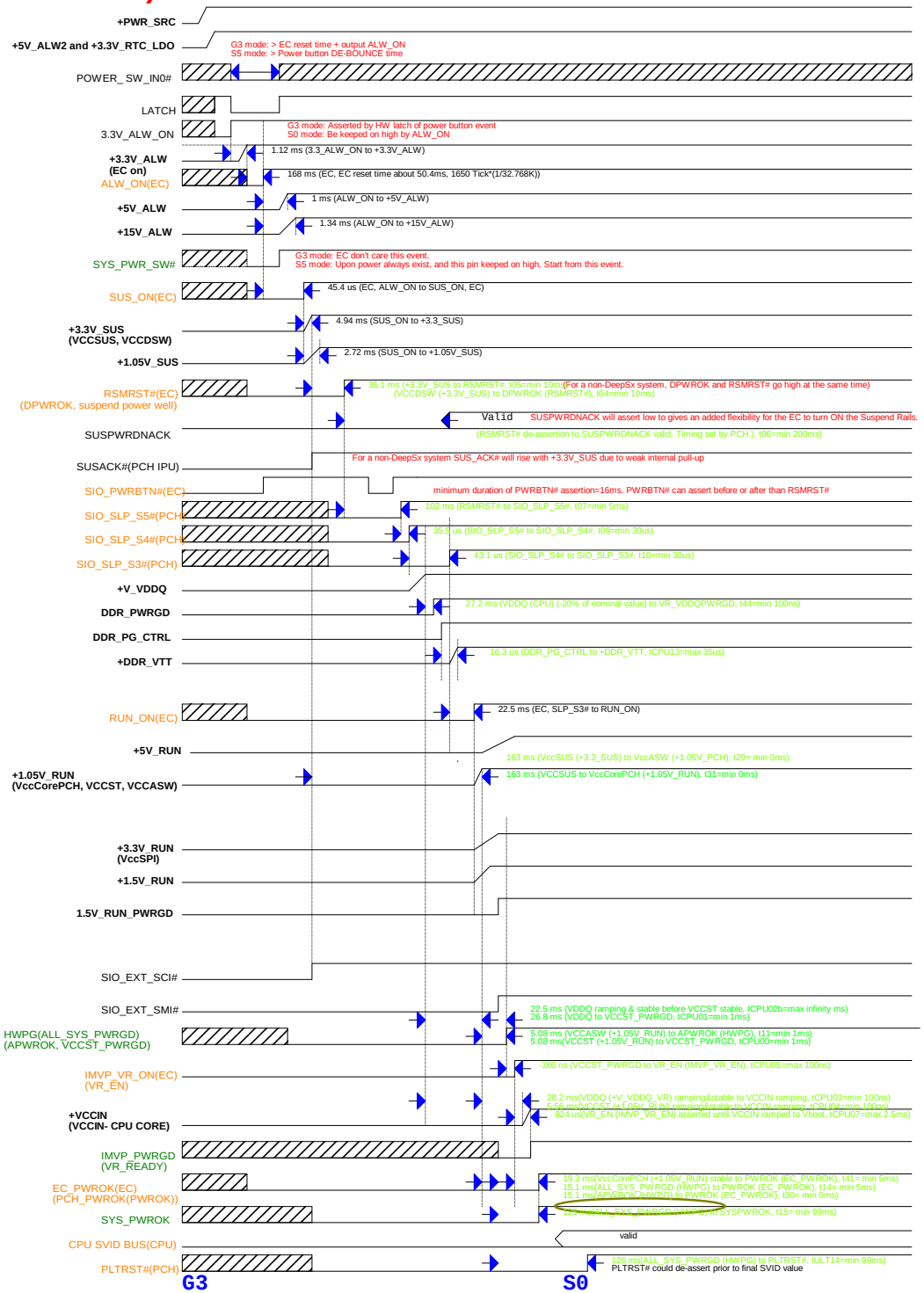
Battery Mode



Power Sequence (G3 to S0)

Shark Bay ULT PSS, 490828, Rev1.1



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Size	Document Number	Rev
	G3 to S0	A
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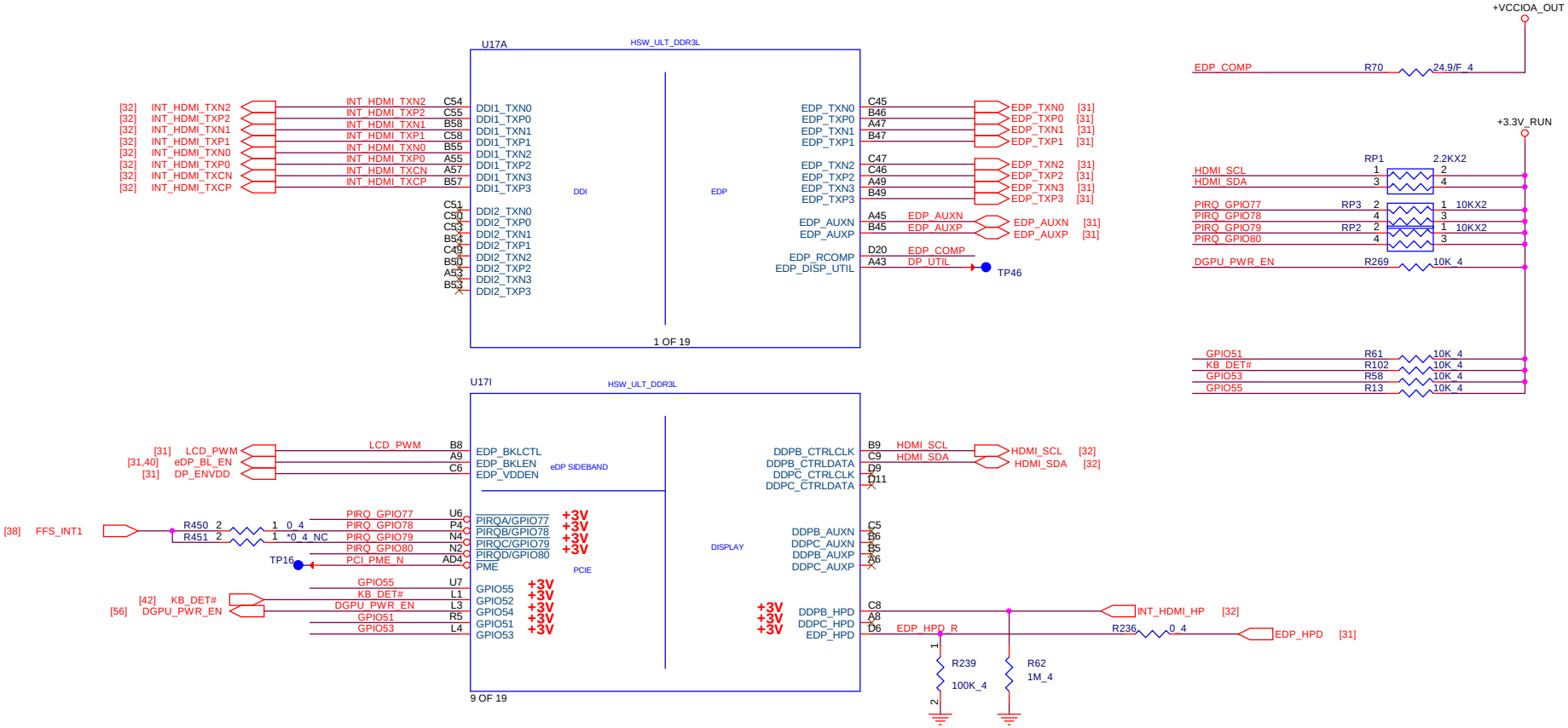
Haswell ULT (DISPLAY)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DDPB_CTRLDATA	Port B Detected	PCH_PWROK	0 = Port B is not detected. 1 = Port B is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. PU 2.2K to +3.3V_RUN
DDPC_CTRLDATA	Port C Detected	PCH_PWROK	0 = Port C is not detected. 1 = Port C is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. NC

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	Haswell ULT 1/12	A

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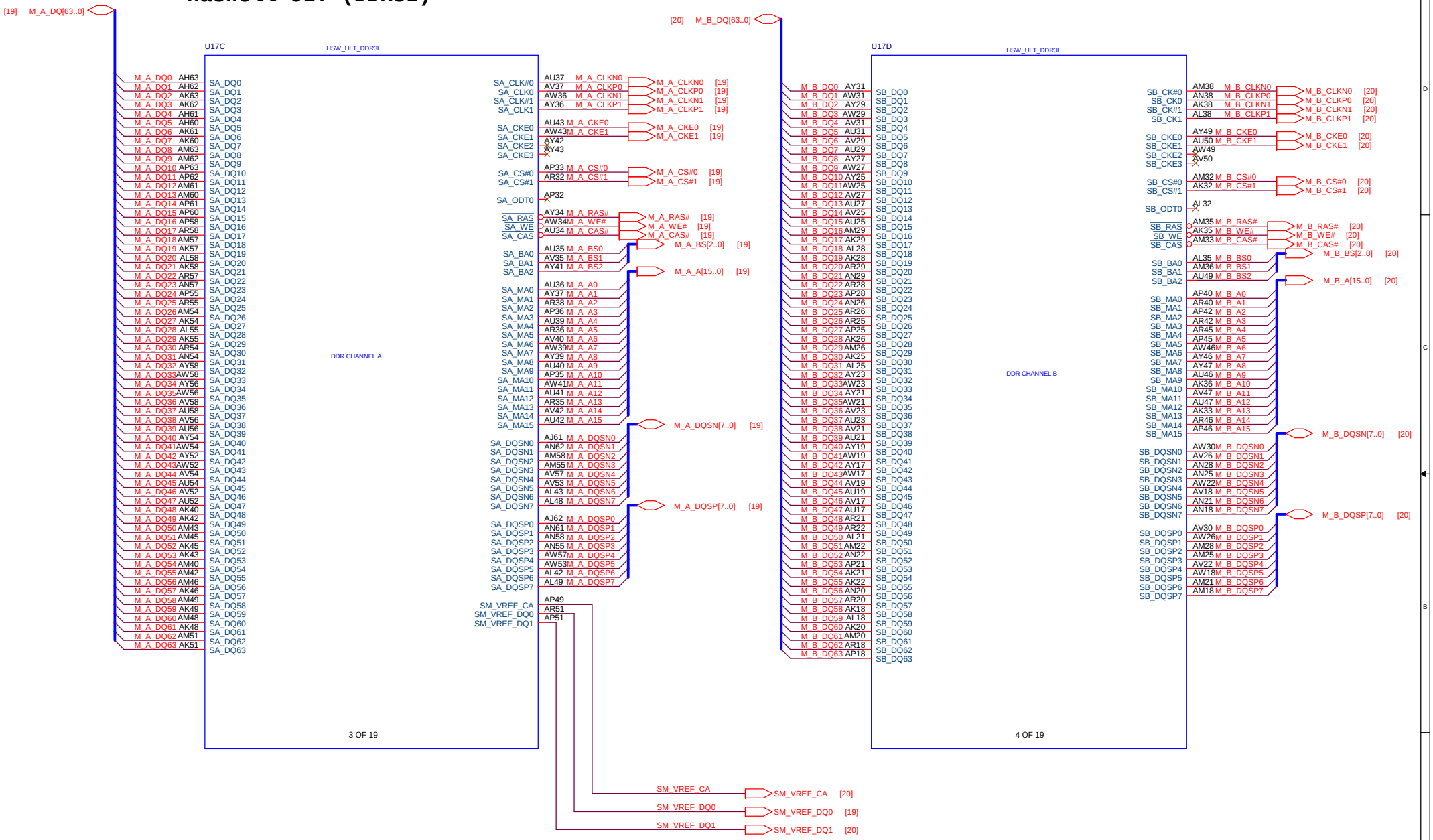
Haswell ULT (DDR3L)



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Haswell ULT 2/12	Rev: A
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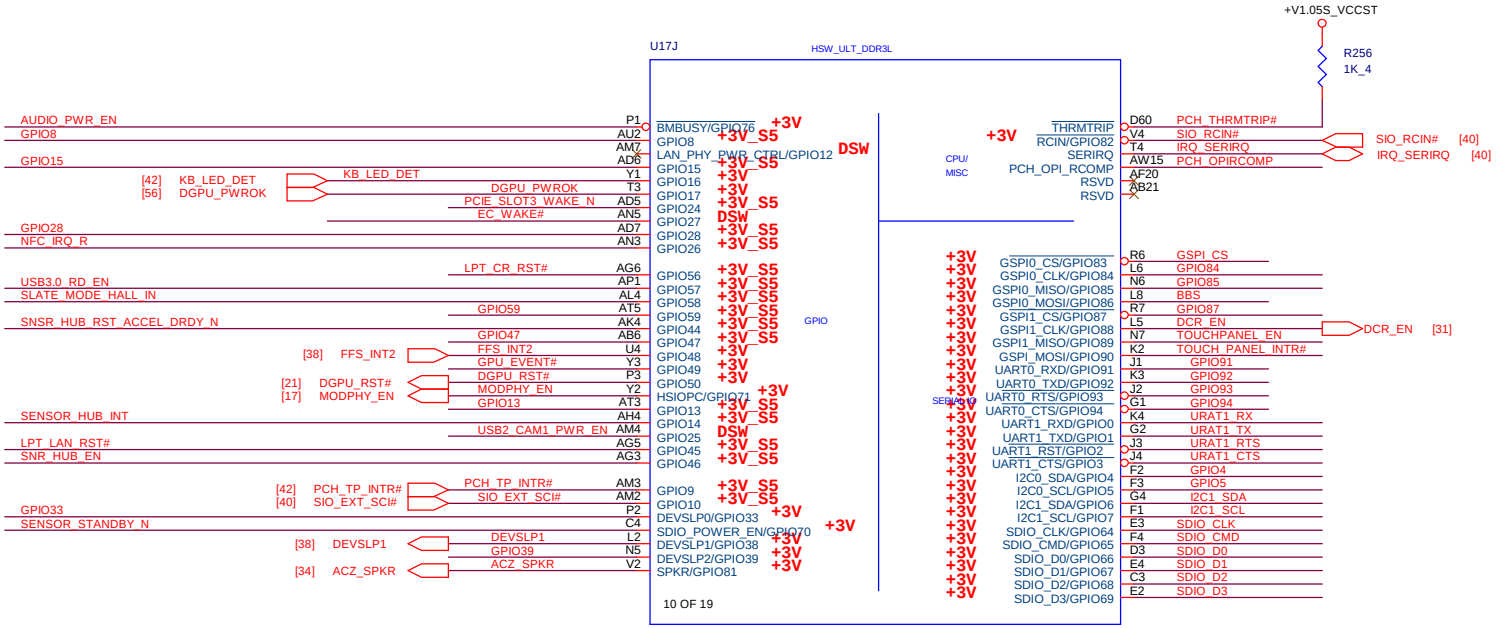
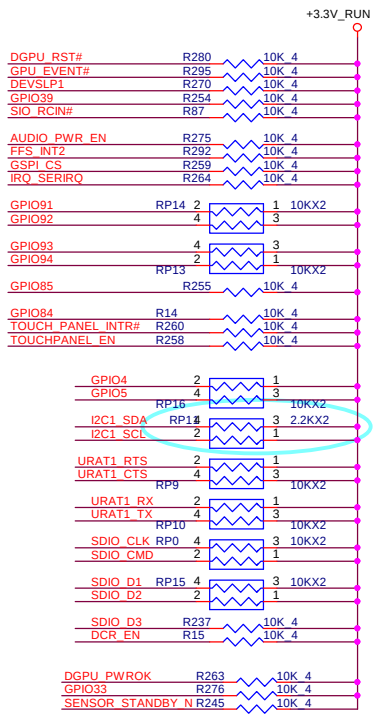
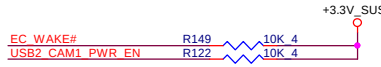
Hasswell ULT(GPIO,LPIO,MISC)

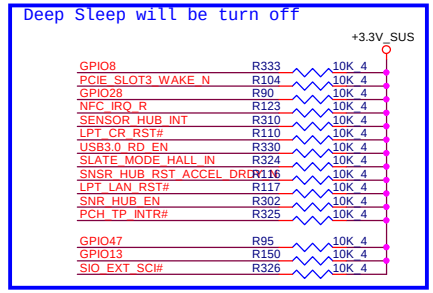


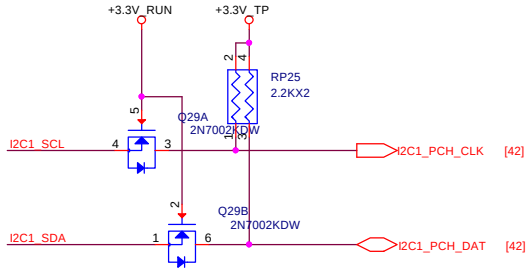


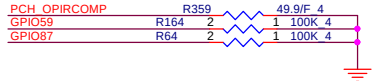


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO15	TLS Confidentiality	RSMRST#	0 = Disable 1 = Enable	This signal has a weak internal pull-down.
SPKR/GPIO81	No Reboot mode	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down. NA
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = SPI 1 = LPC	This signal has a weak internal pull-down.
SDIO_D0/GPIO66	Top Swap Override	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down.







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	Haswell ULT 3/12	A

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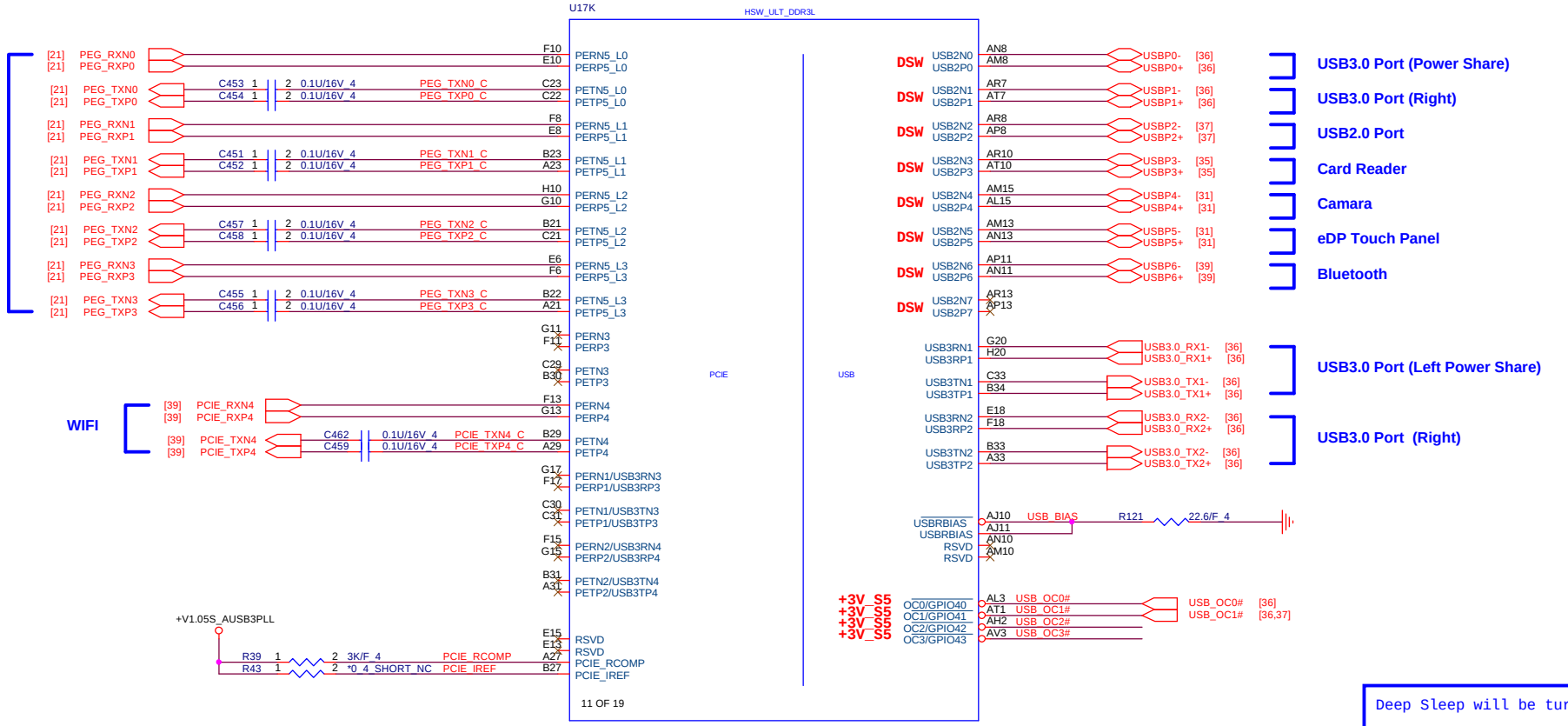
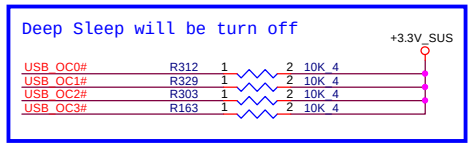
Haswell ULT (PCIE,USB)





Overcurrent Pin Setting

Pin	Default Port Mapping	AM6 setting
OC0#	Port 0, Port 1	Port 0
OC1#	Port 2, Port 3	Port 1, Port 2
OC2#	Port 4, Port 5	no use
OC3#	Port 6, Port 7	no use

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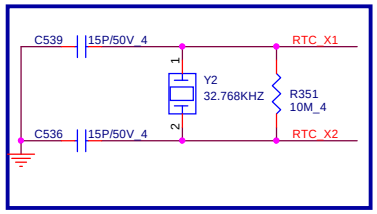
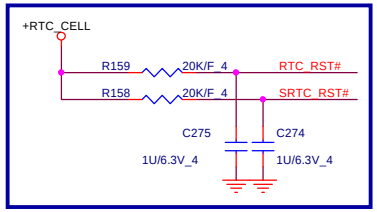
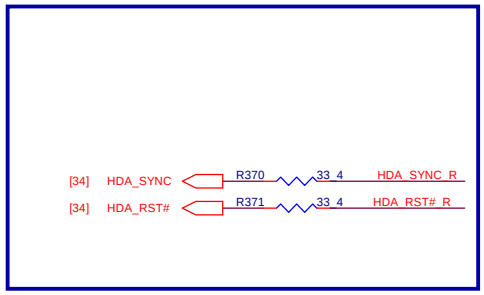
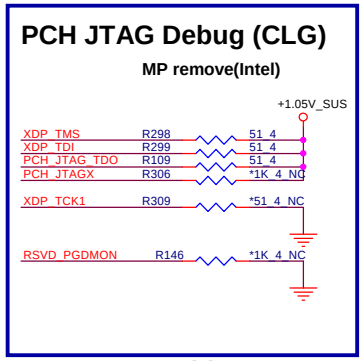
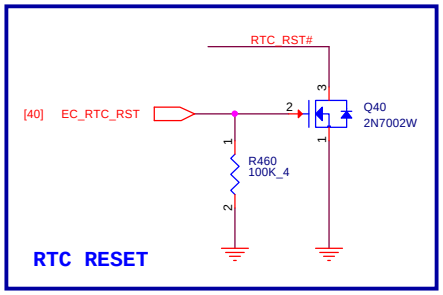
Haswell ULT (RTC, HDA, JTAG, SATA)

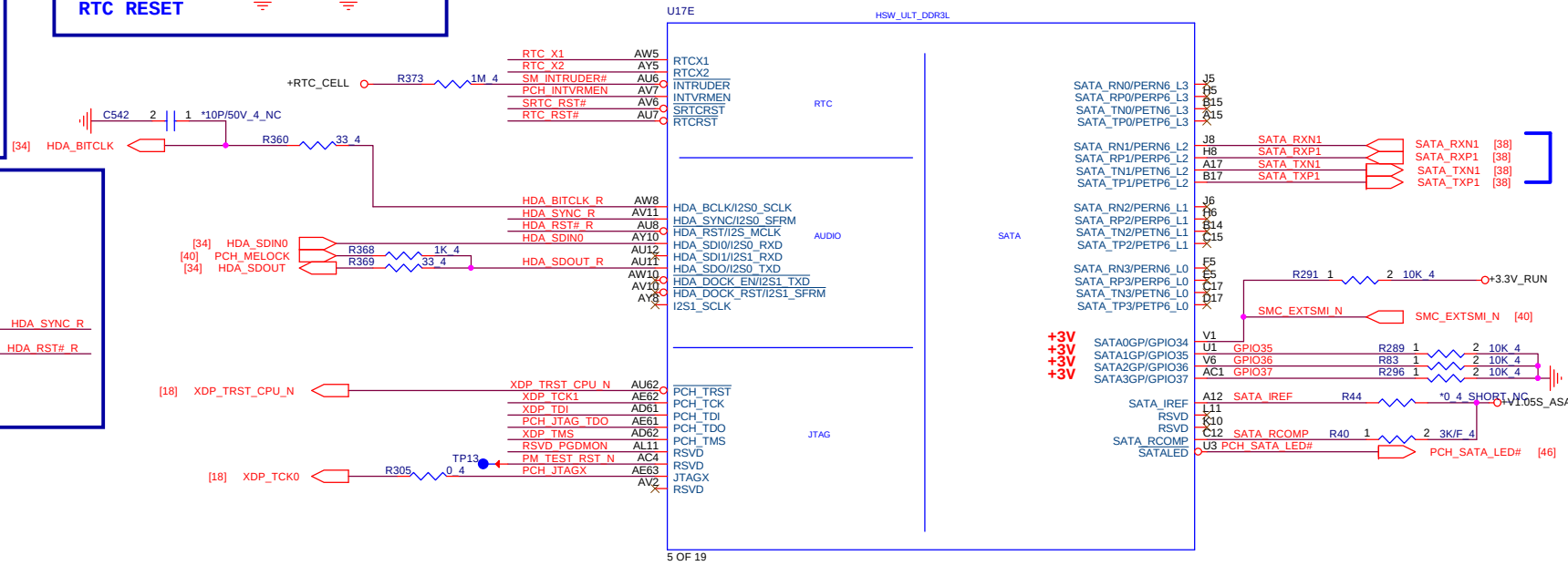












DFXTESTMODE
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = Security Effect (Int PD) 1 = Can be Override	This signal has a weak internal pull-down. The internal pull-down is disabled after PLTRST# deasserts
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Integrated VRMs disabled. 1 = Integrated VRMs enabled.	+RTC_CELL R157 *330K_4_NC PCH_INTVRMEN R147 330K_4 **An external resistor is required**

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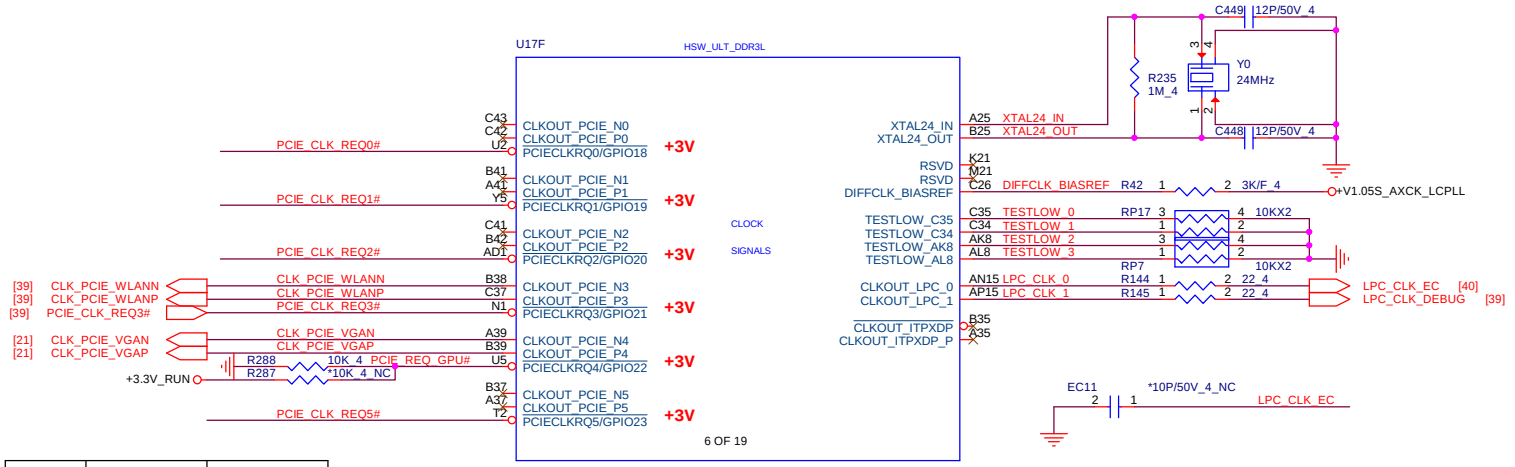
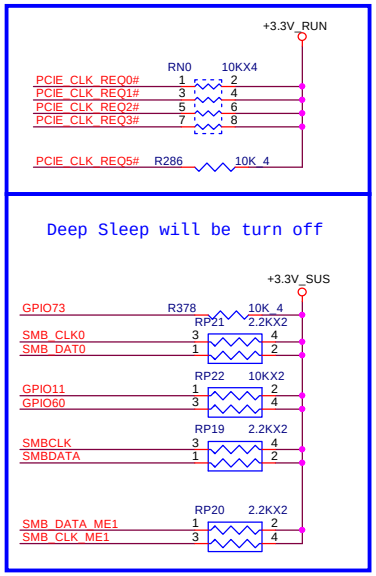
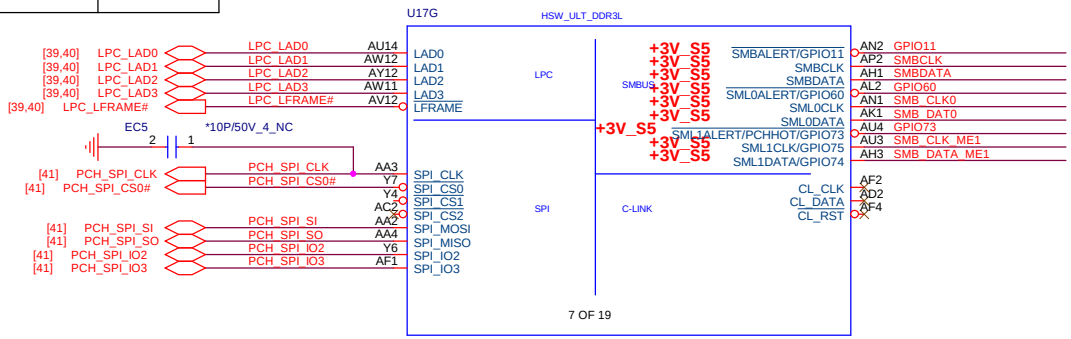
Haswell ULT (CLK)

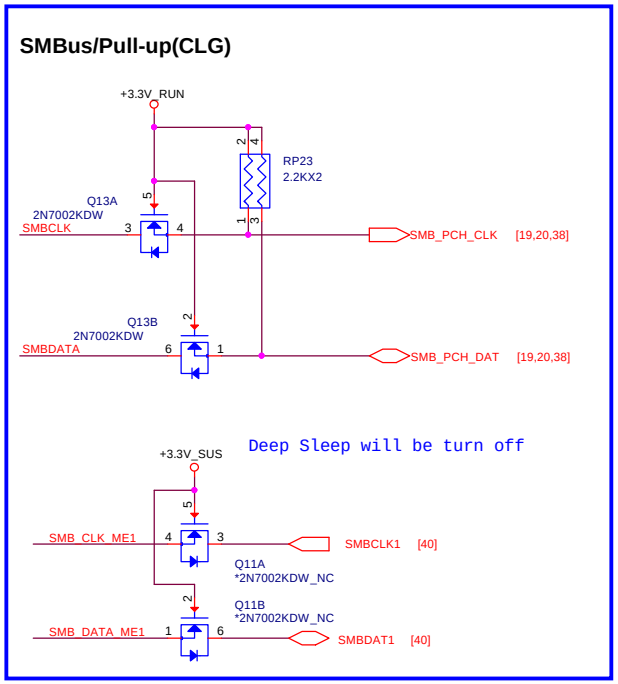




	UMA	Discrete
R288	*10K_4_NC	10K_4
R287	10K_4	*10K_4_NC

Haswell ULT (LPC/SPI/SMB/CLINK)





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	Haswell ULT 6/12	A

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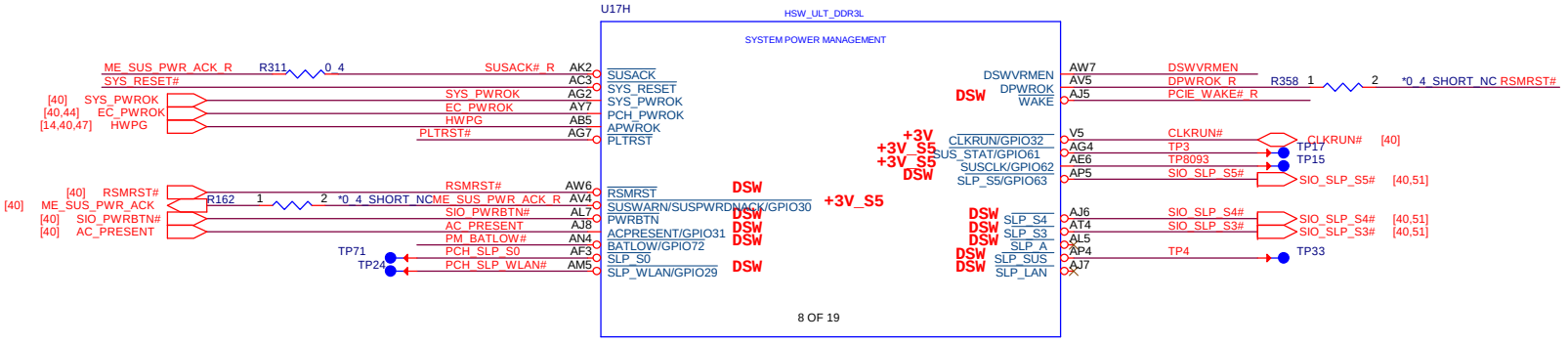
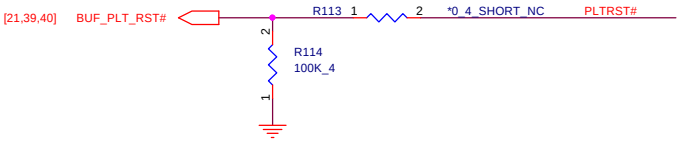
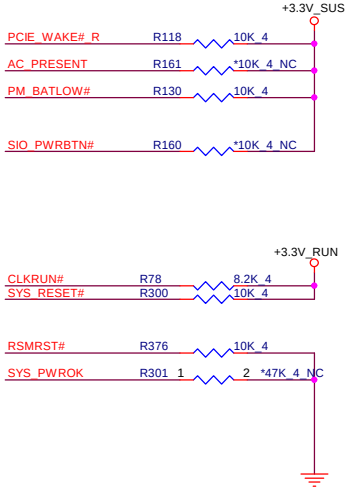
Haswell ULT (SYSTEM POWER MANAGEMENT)

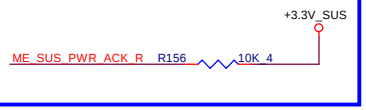




PCH Pull-high/low(CLG)



Deep Sleep will be turn off



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	1. This signal is always sampled. 2. This signal is in the RTC well.

+RTC_CELL 330K_4 R372 DSWVRMEN

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Haswell ULT MCP(POWER)

CPU VDDQ

Haswell ULT 15W & 28W: 1.4A

6X10UF MLCC
4X2.2UF MLCC

+V_VDDQ
C284 10U/4V_6
C283 10U/4V_6
C279 10U/4V_6
C278 10U/4V_6
C286 10U/4V_6
C280 10U/4V_6
C270 1U/6.3V_4
C273 1U/6.3V_4
C271 2.1U/16V_4
C272 2.1U/16V_4

+V1.05S_VCCST
R243 10K_4
[13,40,47] HWPG
SDM10K45-7-F
VCCST_PWRGD

+VCCIOA_OUT
VCOMP_OUT(+VCCIOA_OUT) only be used to connect eDP_RCOMP.

[54] H_VR_ENABLE_MCP
R242 10K_4
[54] IMVP_PWRGD
C464 0.1U/16V_4
+V1.05S_VCCST
R6 *10K_4_NC IMVP_PWRGD

+V1.05S_VCCST
+VCCIN
AC22 VCCST
AE22 VCCST
AE23 VCCST

+V1.05V_RUN
R94 *0_8_SHORT_NC
+V1.05S_VCCST

+V1.05S_VCCST

U17L HSW_ULT_DDR3L

+V_VDDQ
L59 RSVD
J58 RSVD
AH26 VDDQ
AJ31 VDDQ
AJ33 VDDQ
AJ37 VDDQ
AN33 VDDQ
AP43 VDDQ
AR48 VDDQ
AY35 VDDQ
AY40 VDDQ
AY44 VDDQ
AY50 VDDQ

1.4A

+VCCIN
F59 VCC
N58 RSVD
AC58 RSVD

VCCSENSE
E63 VCC_SENSE
TP43 +VCCIO_OUT
A59 RSVD
E20 VCCIO_OUT
AD23 VCCIOA_OUT
AA23 RSVD
AE58 RSVD
RSVD
VCOMP_OUT

H_CPU_SVIDALRT# L62 VIDALERT
VR_SVID_CLK N63 VIDSCLK
VR_SVID_DATA L63 VIDSOUT
B59 VCCST_PWRGD
H_VR_ENABLE_MCP F60 VR_EN
IMVP_PWRGD C59 VR_READY
D63 VSS
FIVR_EN_BUF H59 PWR_DEBUG
P62 VSS
TP10 MCP_RSVD_69 P60 RSVD_TP
TP12 MCP_RSVD_70 P61 RSVD_TP
TP58 MCP_RSVD_71 N59 RSVD_TP
TP59 MCP_RSVD_72 N61 RSVD_TP
T59 RSVD
AD60 RSVD
AD59 RSVD
AA59 RSVD
AE60 RSVD
AC59 RSVD
AG58 RSVD
U58 RSVD
V59 RSVD

HSW ULT POWER

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CPU VCC

Haswell ULT 15W : 32A
28W : 40A

24 X 10UF(0603 MLCC)

+VCCIN
C36 VCC
C40 VCC
C44 VCC
C48 VCC
C52 VCC
C56 VCC
E23 VCC
E25 VCC
E27 VCC
E29 VCC
E31 VCC
E33 VCC
E35 VCC
E37 VCC
E39 VCC
E41 VCC
E43 VCC
E45 VCC
E47 VCC
E49 VCC
E51 VCC
E53 VCC
E55 VCC
E57 VCC
F24 VCC
F28 VCC
F32 VCC
F36 VCC
F40 VCC
F44 VCC
F48 VCC
F52 VCC
F56 VCC
G23 VCC
G25 VCC
G27 VCC
G29 VCC
G31 VCC
G33 VCC
G35 VCC
G37 VCC
G39 VCC
G41 VCC
G43 VCC
G45 VCC
G47 VCC
G49 VCC
G51 VCC
G53 VCC
G55 VCC
G57 VCC
H23 VCC
J23 VCC
K23 VCC
K57 VCC
L22 VCC
M23 VCC
M57 VCC
P57 VCC
U57 VCC
W57 VCC

C210 10U/4V_6
C199 10U/4V_6
C181 10U/4V_6
C182 10U/4V_6
C219 10U/4V_6
C214 10U/4V_6
C168 10U/4V_6
C201 10U/4V_6
C169 10U/4V_6
C170 10U/4V_6
C185 10U/4V_6
C200 10U/4V_6
C166 10U/4V_6
C167 10U/4V_6
C203 10U/4V_6
C183 10U/4V_6
C202 10U/4V_6
C226 10U/4V_6
C186 10U/4V_6
C209 10U/4V_6
C213 10U/4V_6
C204 10U/4V_6
C171 10U/4V_6
C184 10U/4V_6

C218 100P/50V_4
C224 100P/50V_4
C229 100P/50V_4
C162 100P/50V_4

R262 100/F_4 +VCCIN
VCCSENSE VCCSENSE [54]
FIVR_EN_BUF R77 150_6 +V1.05S_VCCST

SVID ALERT

+V1.05S_VCCST
CLOSE TO CPU
R283 75_4
C485 0.1U/16V_4
H_CPU_SVIDALRT# R285 43_4 VR_SVID_ALERT# [54]

SVID DATA

+V1.05S_VCCST
CLOSE TO CPU
R284 130_4
C488 0.1U/16V_4
+V1.05S_VCCST
CLOSE TO VR
R7 130_4
C47 0.1U/16V_4
VR_SVID_DATA VR_SVID_DATA [54]

SVID CLK

+V1.05S_VCCST
CLOSE TO VR
R8 54.9/F_4
C49 0.1U/16V_4
VR_SVID_CLK VR_SVID_CLK [54]

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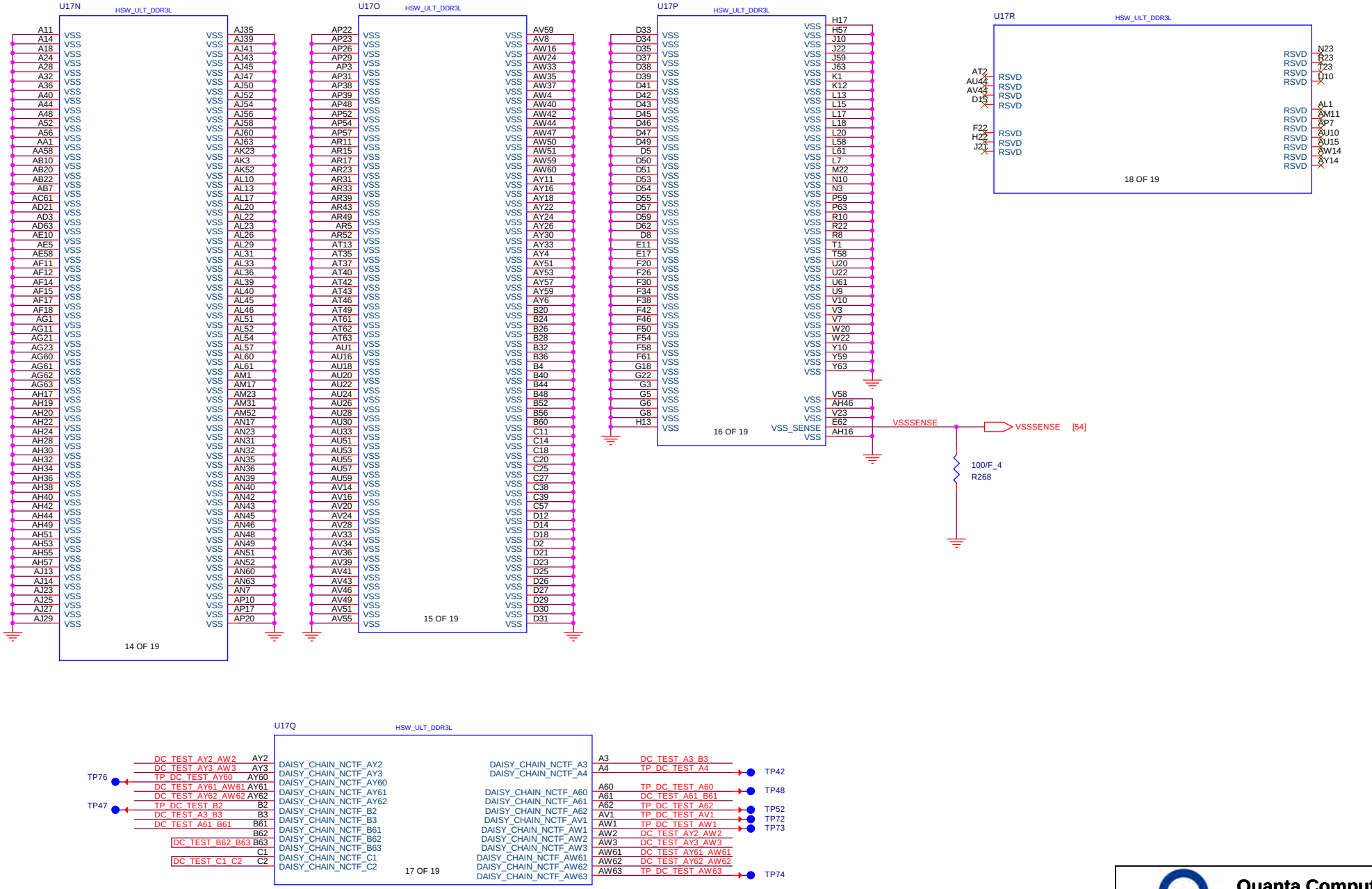
Haswell ULT (GND)



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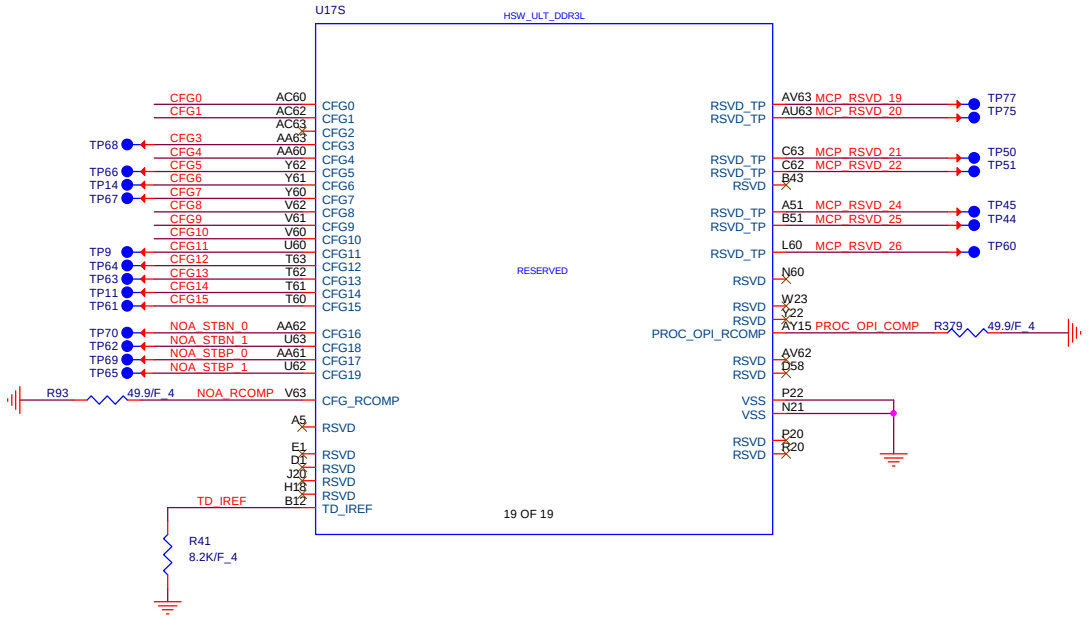


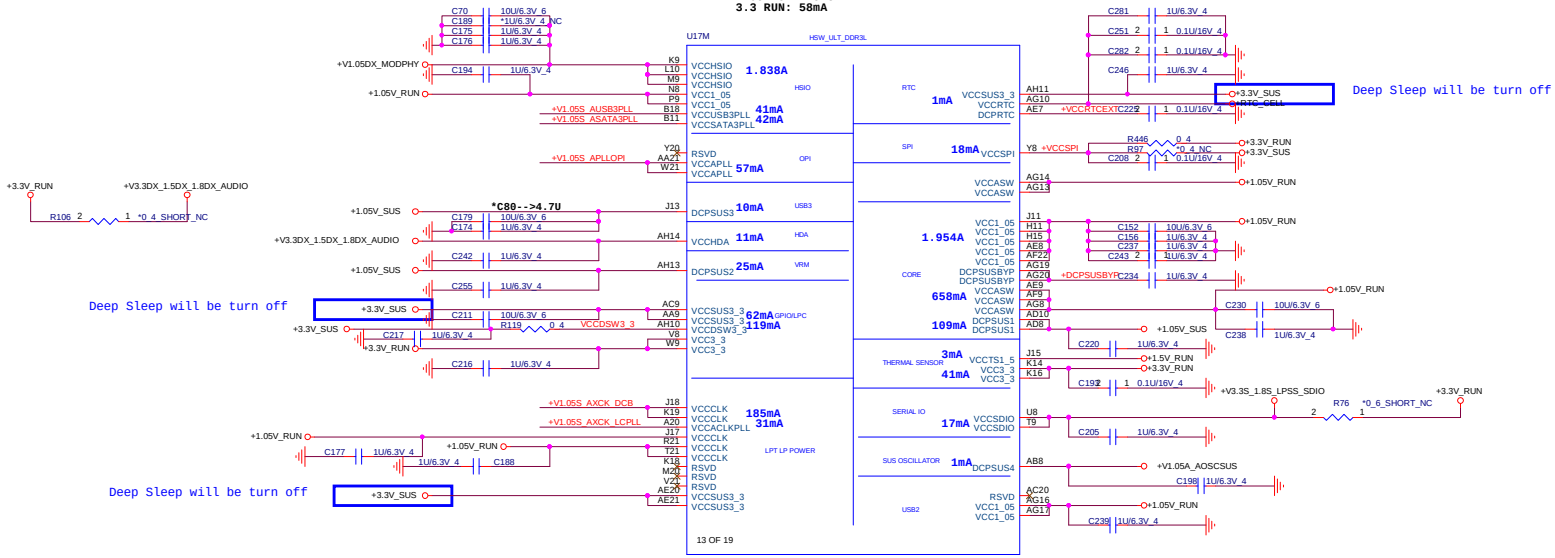
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

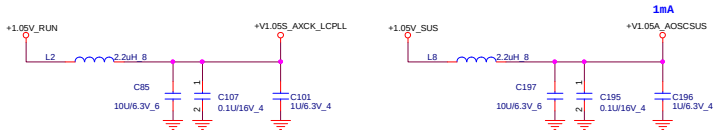
	1	0	
CFG0 Reserved	(DEFAULT) NORMAL OPERATION		CFG0 R108 *1K_4_NC
CFG1 Reserved	(DEFAULT) NORMAL OPERATION		CFG1 R297 *1K_4_NC
CFG2 Reserved	(DEFAULT) NORMAL OPERATION		
CFG3 MSR Privacy Bit Feature	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R293 *1K_4_NC
CFG4 eDP enable	Disabled	Enabled	CFG4 R107 1K_4
CFG[19:5] Reserved	(DEFAULT) NORMAL OPERATION		CFG8 R92 *1K_4_NC
			CFG9 R294 *1K_4_NC
			CFG10 R100 *1K_4_NC

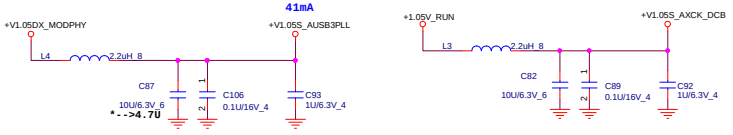
Haswell ULT PCH(POWER)

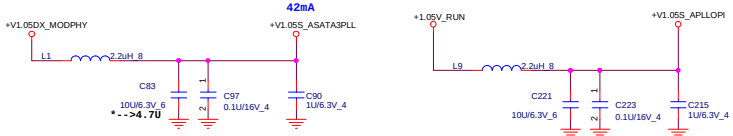
3.3 SUS: 205mA
1.05 SUS: 2066mA
1.05 RUN: 2578mA
3.3 RUN: 58mA

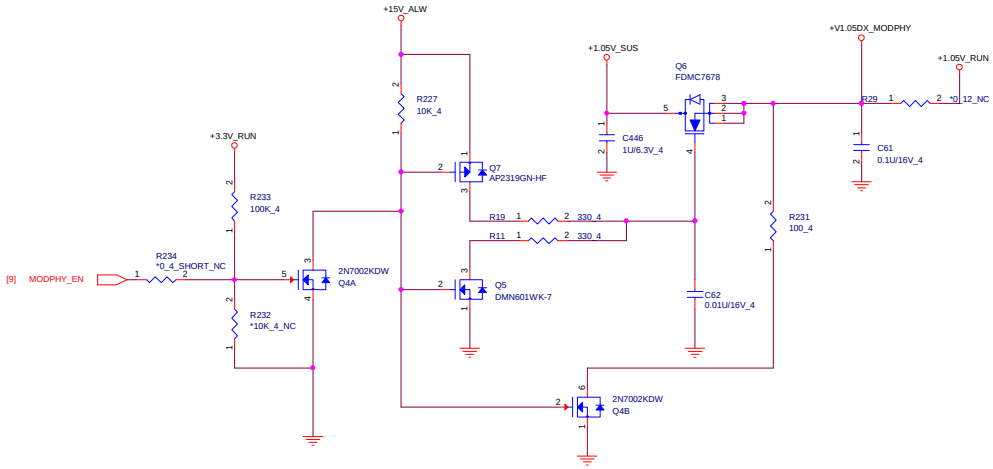


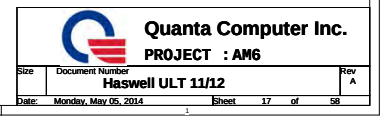
boot strap capacitor	VCCDSW3_3 C233 0.47U/6.3V_4 +DCPSUSBYP

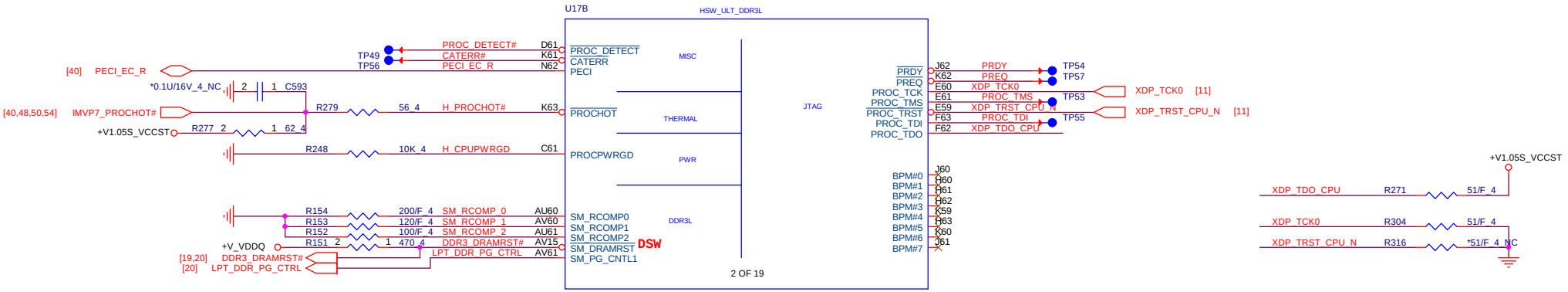












Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	Haswell ULT 12/12	A
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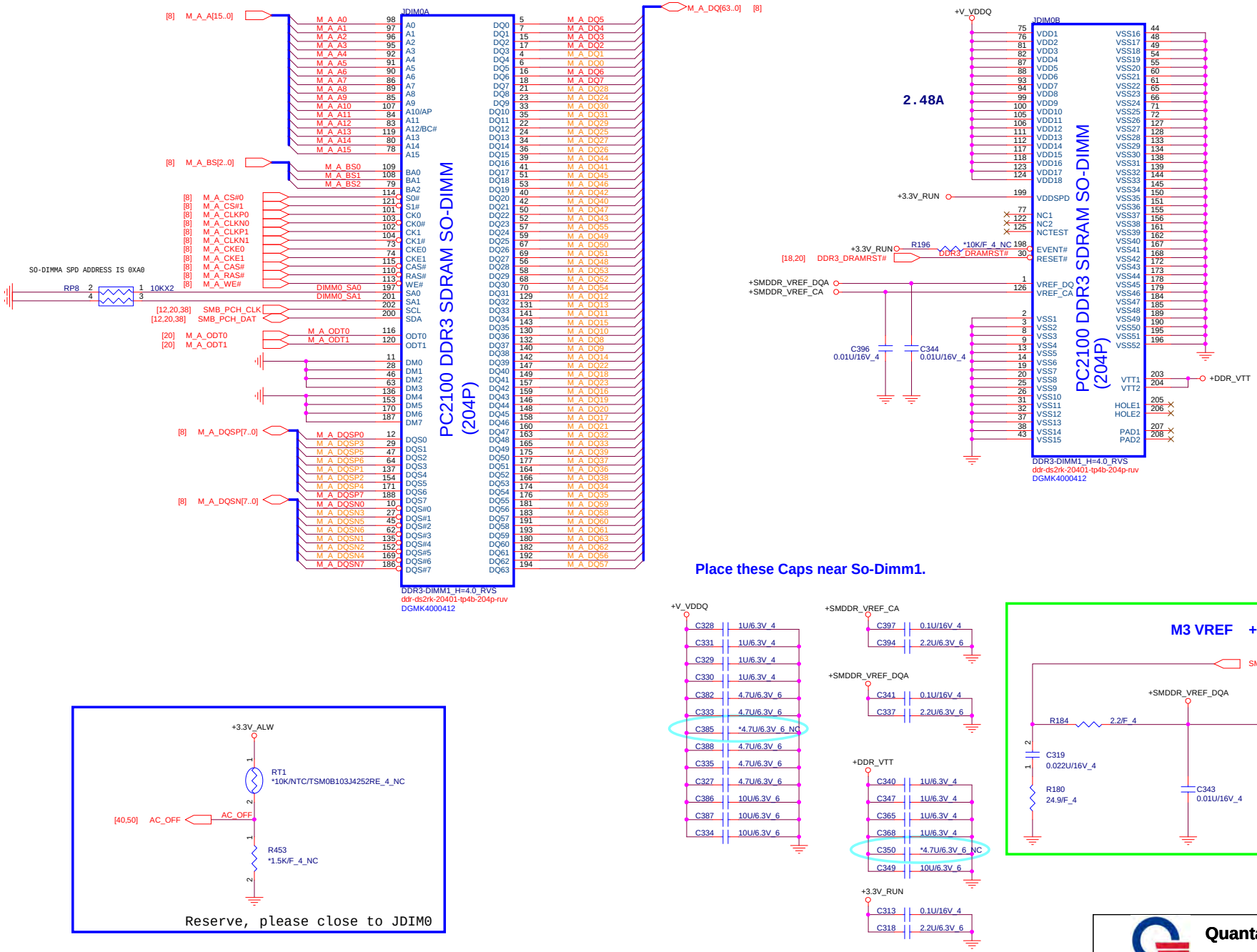
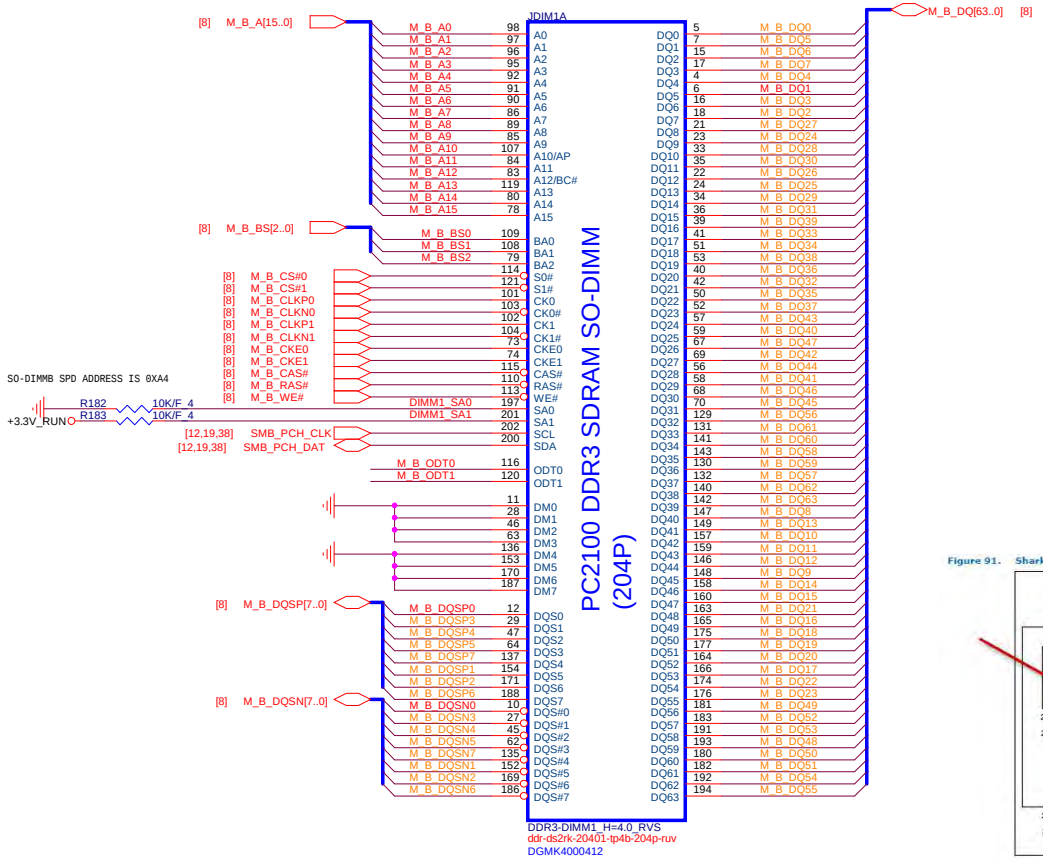


Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: DDR3 DIMM1-RVS (4.0H)	Rev: A
Date: Monday, May 05, 2014	Sheet 19 of 58	



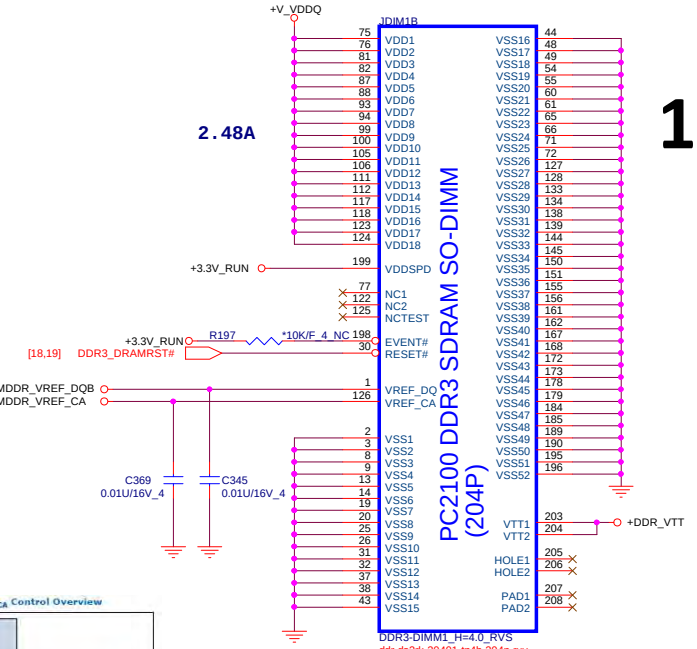
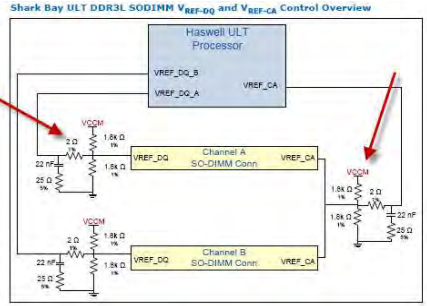
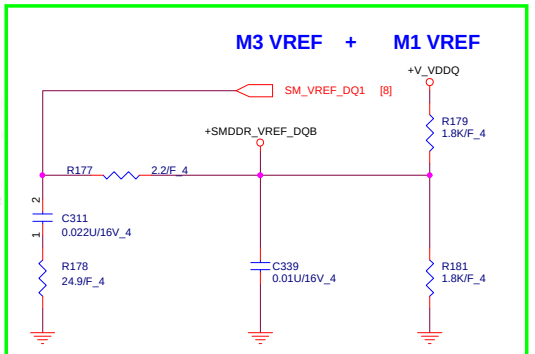
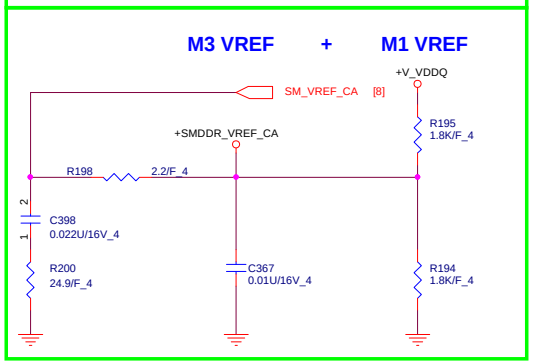


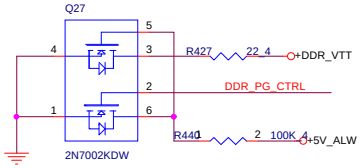
Figure 91. Shark Bay ULT DDR3L SODIMM V_{REF-DQ} and V_{REF-CA} Control Overview



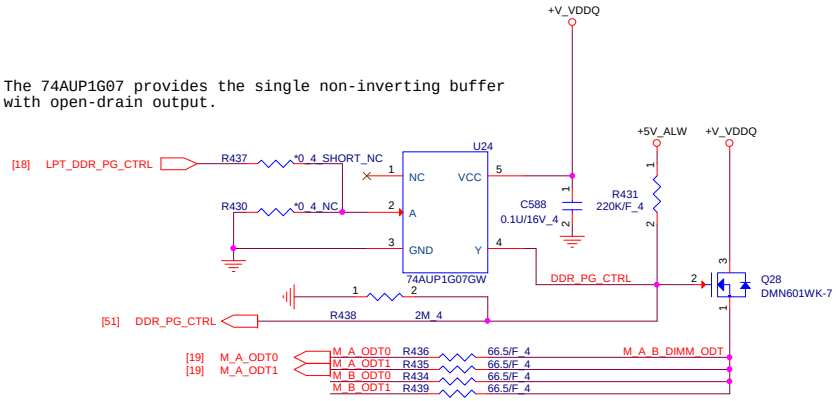




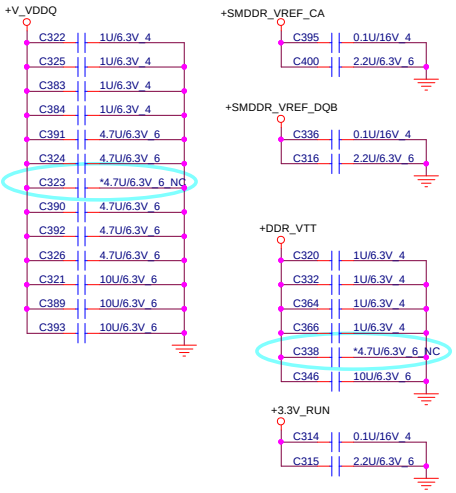
DDR3L SODIMM ODT GENERATION



The 74AUP1G07 provides the single non-inverting buffer with open-drain output.



Place these Caps near So-Dimm2.



Quanta Computer Inc.

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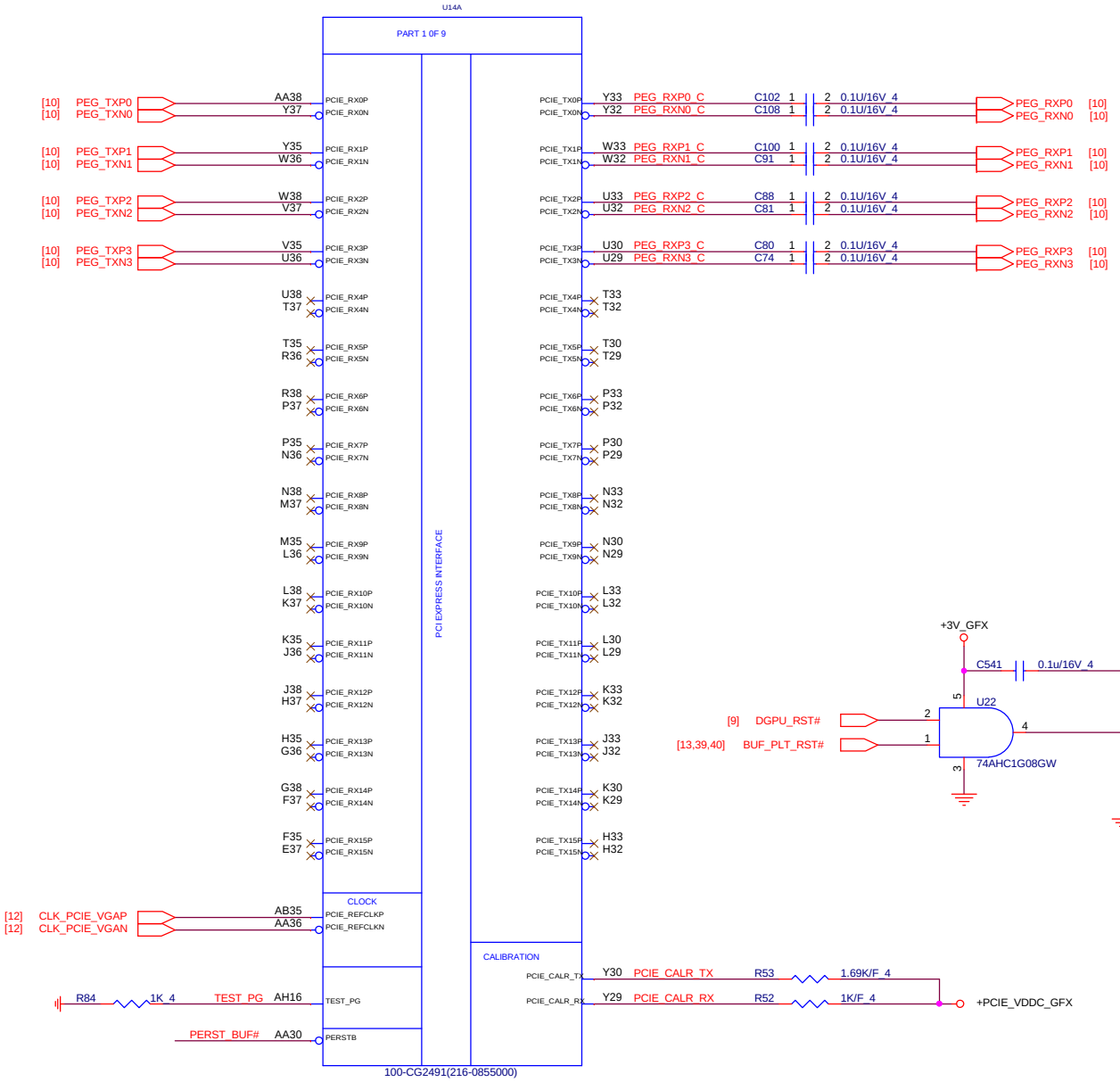
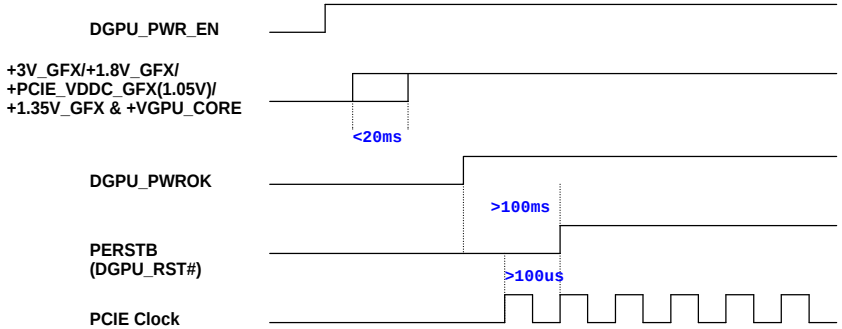


Opal XT Power-on sequence



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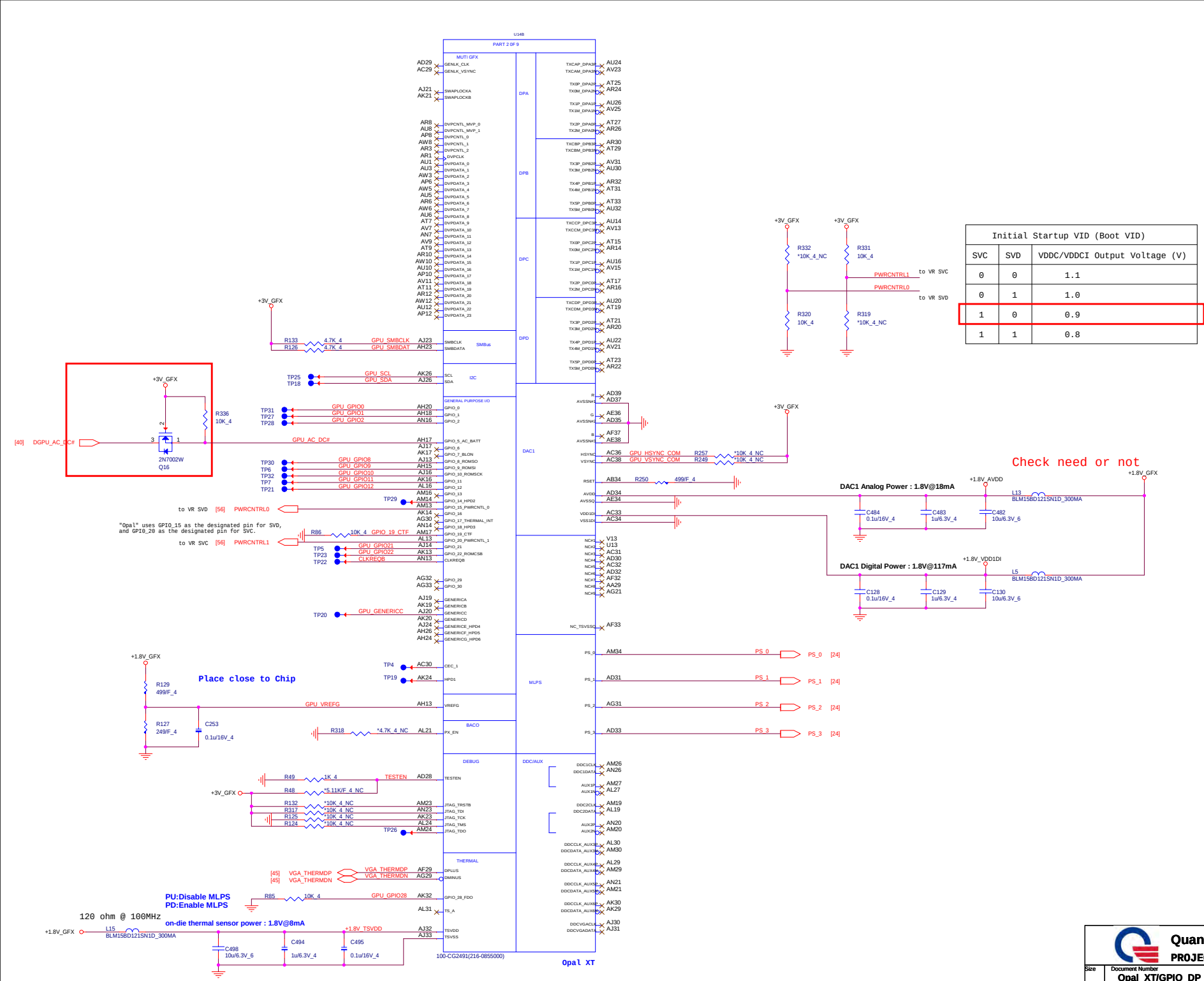

Initial Startup VID (Boot VID)		
SVC	SVD	VDDC/VDDCI Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

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	Opal_XT/GPIO_DP_CRT_I2C		A
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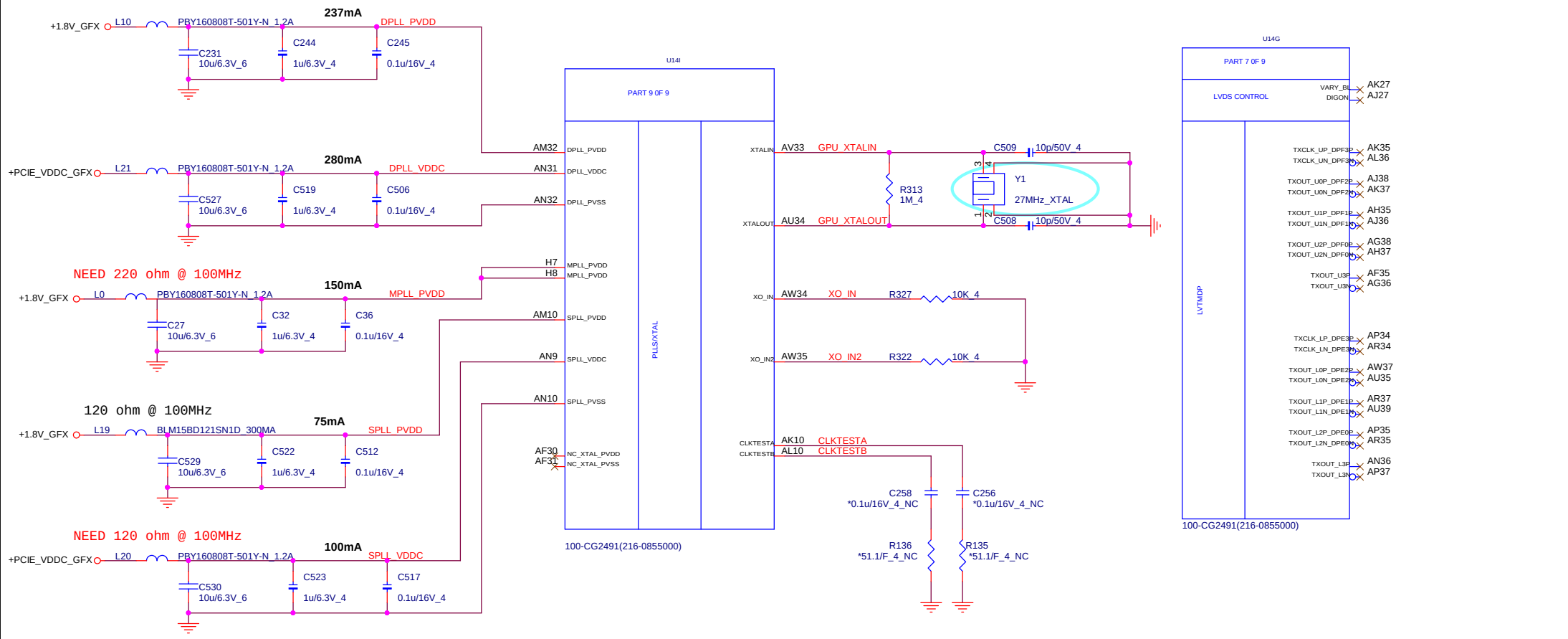

Quanta Computer Inc.

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Size	Document Number	Rev
	Opal_XT/XTAL_LVDS	A
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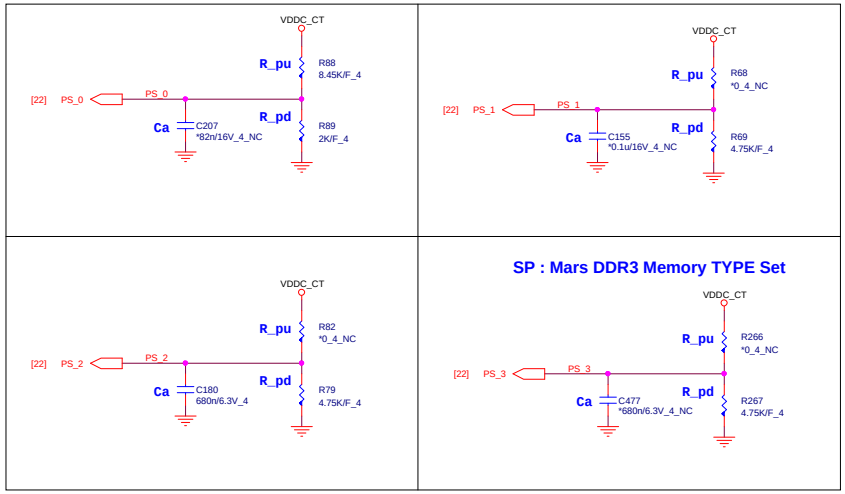


MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	00000
PS_3	11XXX

MLPS

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	NA

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

R_pu/R_pd	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

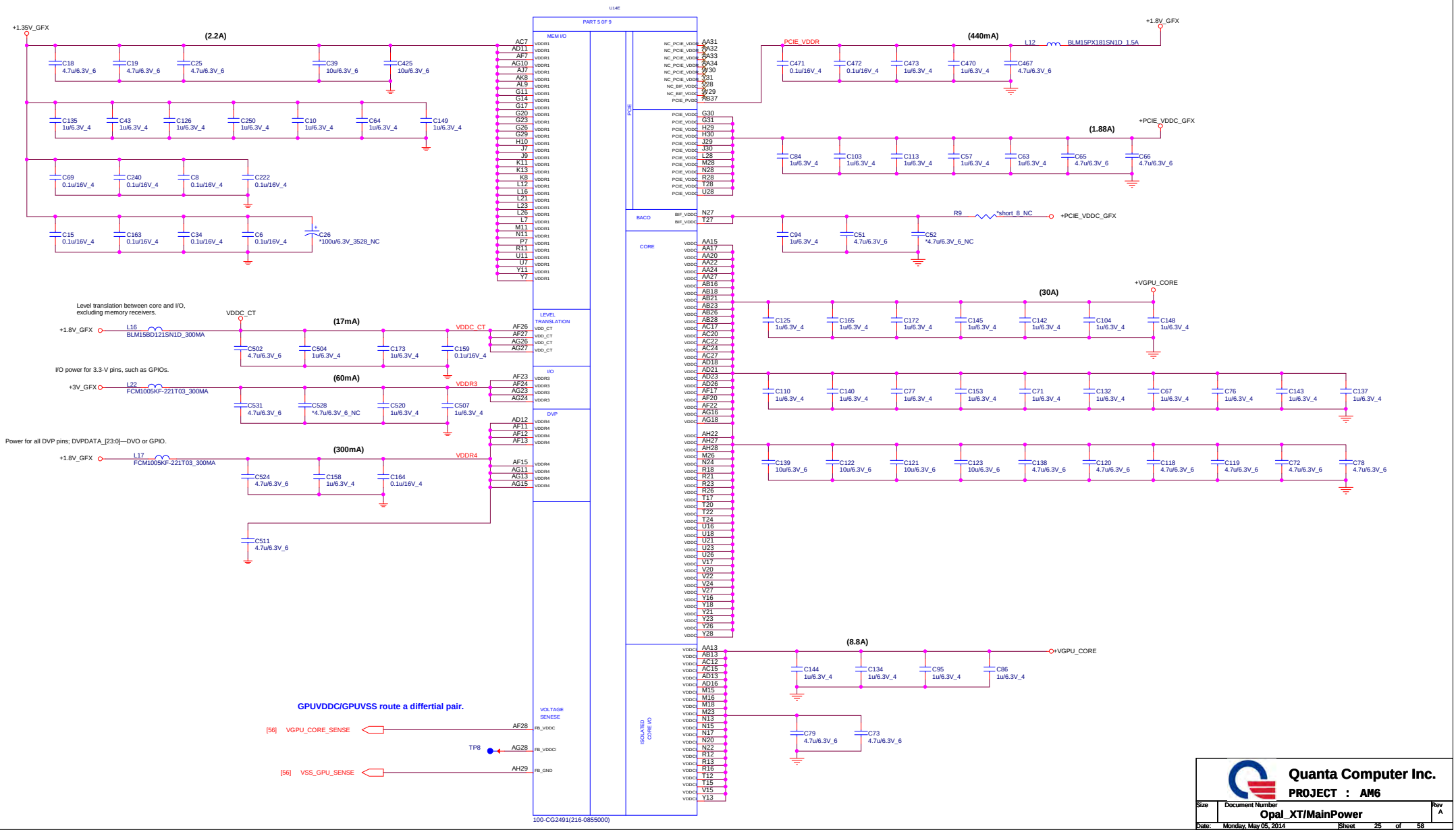
MLPS Bit	Strap Name	AM6 Settings	AM6 Settings	Description	AMD Recommended Settings
PS_0[1]	ROM_CONFIG[0]	1	Memory Aperture Size Select : 256MB	Serial ROM type or Memory Aperture Size Select If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size.	Design dependent, SIZE ROM_CONFIG[2:0] 128MB 000 256MB 001 64MB 010 Reserved 011
PS_0[2]	ROM_CONFIG[1]	0			
PS_0[3]	ROM_CONFIG[2]	0			
PS_0[4]	N/A	1	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	1	All endpoints are usable.	the strap option indicates the number of audio-capable display outputs.	Design dependent
PS_1[1]	STRAP_BIF_GEN3_EN_A	0	PCIe GEN3 is not supported. (use GEN2)	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent
PS_1[2]	STRAP_BIF_CLK_PM_EN	0	The CLKREQB power management capability is disabled	Determines whether or not the PCIe reference clock power management capability 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	0	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1	The transmitter full-swing is enabled	Control the transmitter full-/ half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	1	Tx deemphasis enabled.	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent
PS_2[1]	N/A	0	Reserved.	Reserved.	N/A
PS_2[2]	N/A	0	Reserved.	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	0	Disable the external BIOS ROM device.	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent
PS_2[4]	STRAP_BIF_VGA_DIS	0	Standalone dGPU design	VGA disable determines whether or not the card will be recognized as the system's VGA controller 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	Standalone dGPU design = 0 AMD PowerXpress design = 1
PS_2[5]	N/A	0	Reserved.	Reserved.	N/A
PS_3[1]	BOARD_CONFIG[0]	X	VRAM vendor BOARD_CONFIG[2:0] Hynix 000 default Micron 001 Samsung 010	Board configuration related strapping, such as for memory ID	Design dependent
PS_3[2]	BOARD_CONFIG[1]	X			
PS_3[3]	BOARD_CONFIG[2]	X			
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	1	No usable endpoints.	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	1			

System Memory Aperture size

GPIO9 BIOSROM	SIZE	GPIO13 ROM_CONFIG2	GPIO12 ROM_CONFIG1	GPIO11 ROM_CONFIG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1

Opal USE

Vendor	Vendor P/N	STN B/S P/N	Size	MLPS
Hynix	H5TC4G63AFR-11C (256M*16)	AKD5PGWTW11 * 8	4GB	000
Micron	MT41J256M16HA-093G:E (256M*16)	AKD5PZSTL02 * 8	4GB	001
Samsung	K4W4G1646D-BC1A (256M*16)	AKD5PGWT500 * 8	4GB	010



Quanta Computer Inc.		
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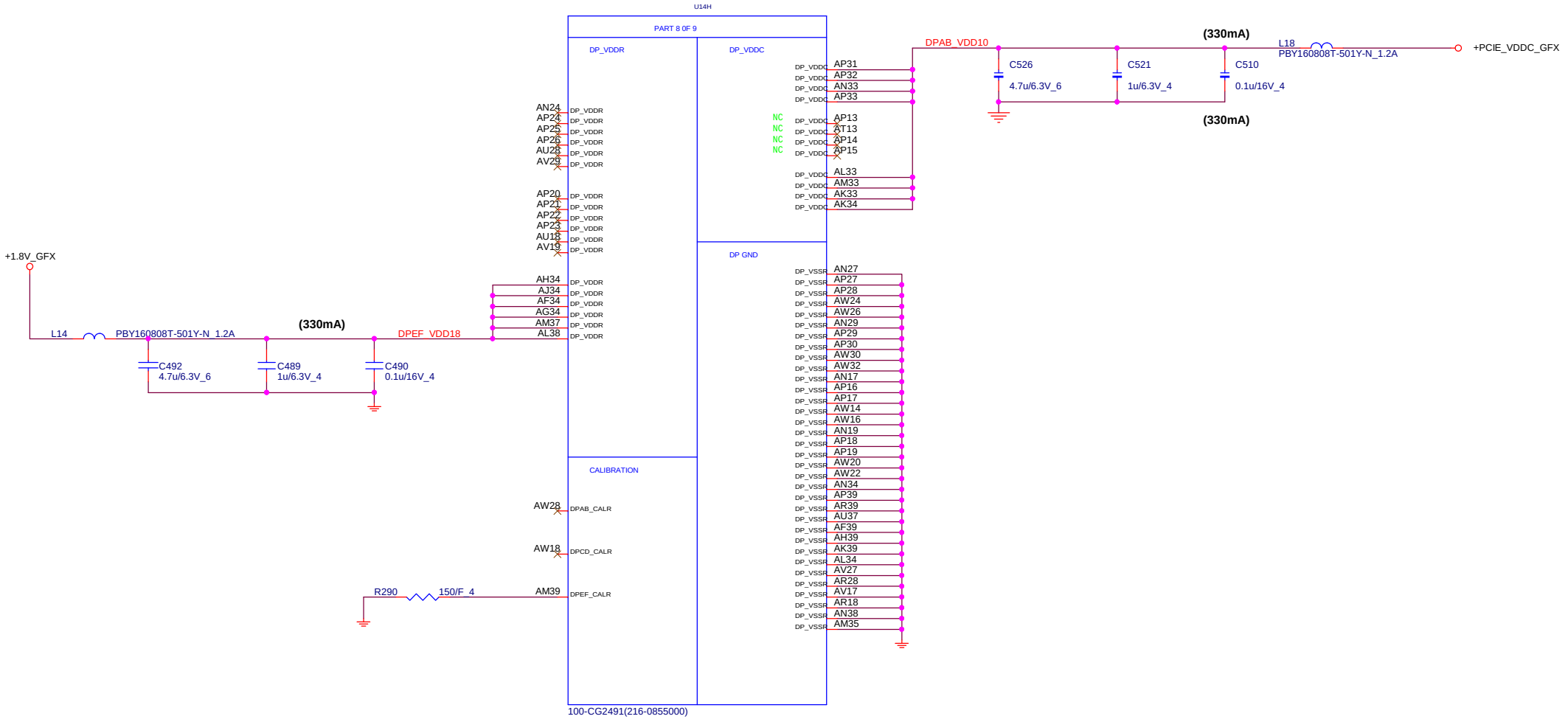

Quanta Computer Inc.		
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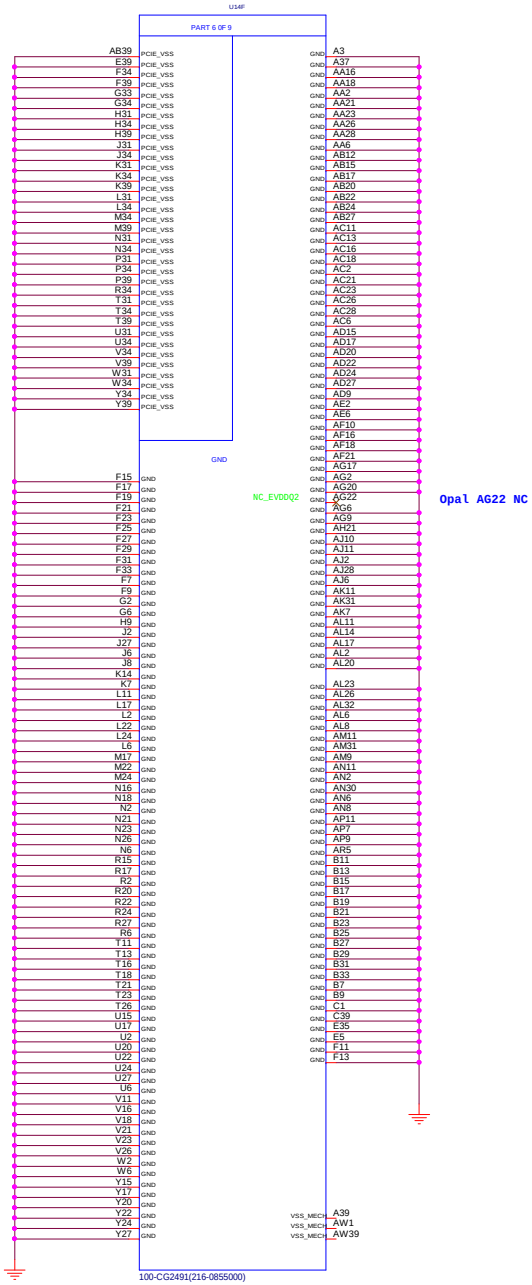
<VGA>



Opal AG22 NC

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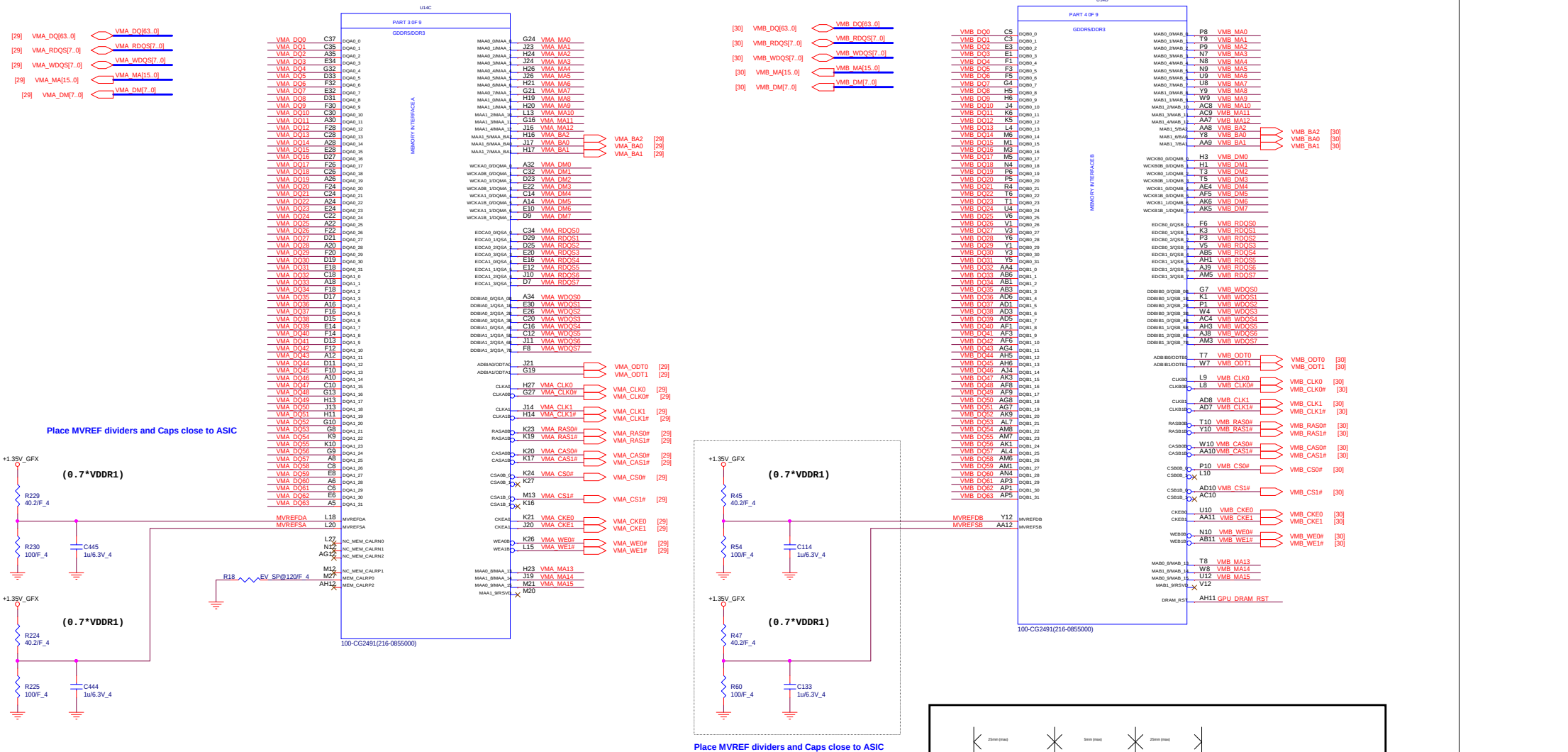
<VGA>



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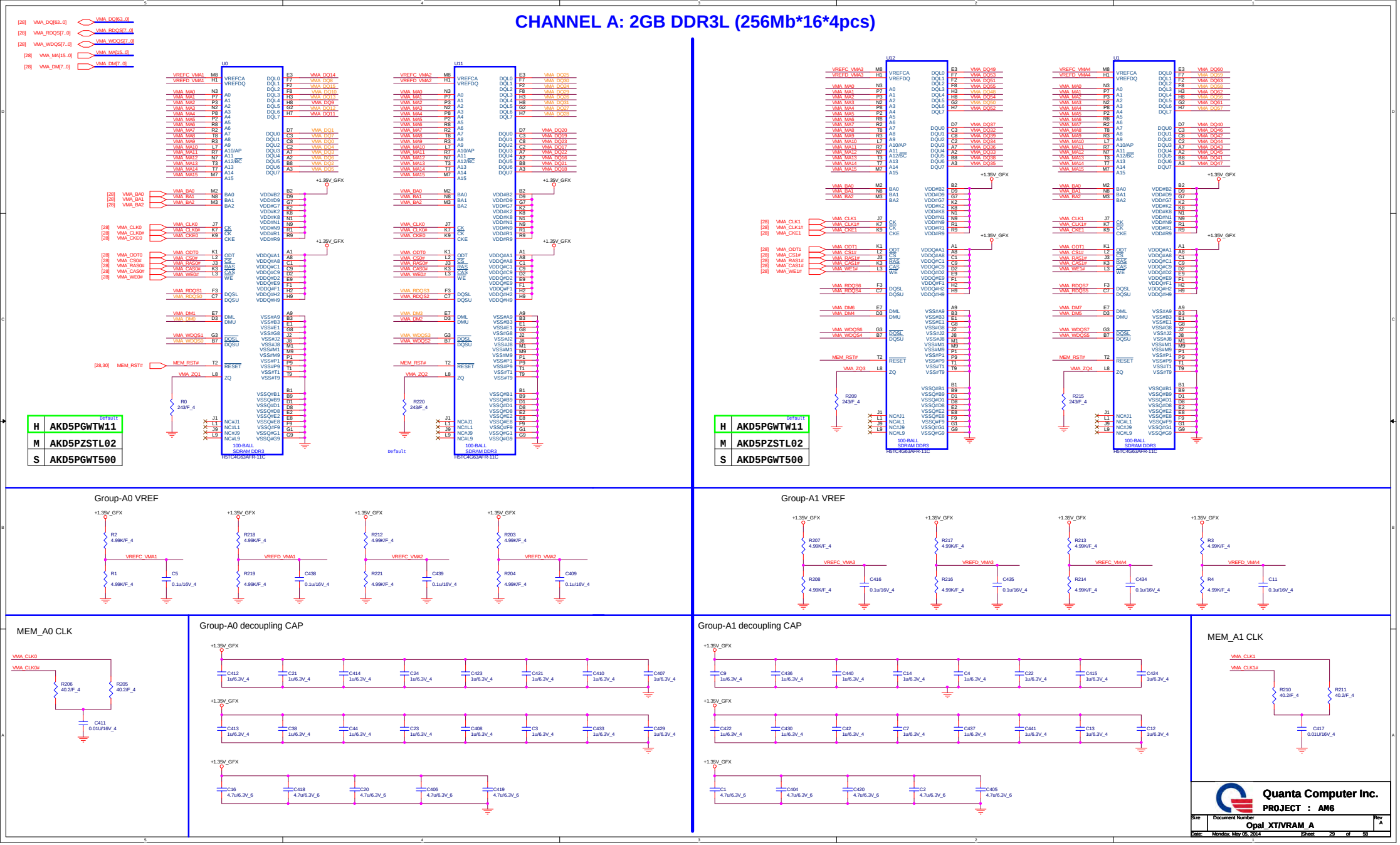
CHANNEL A: 2GB DDR3L (256Mb*16*4pcs)



Group-A0 VREF

Group-A1 VREF

MEM_A0 CLK

Group-A0 decoupling CAP

Group-A1 decoupling CAP

MEM_A1 CLK

Quanta Computer Inc.
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CHANNEL B: 2GB DDR3L (256Mb*16*4pcs)

	Default
H	AKD5PGWTW11
M	AKD5PZSTL02
S	AKD5PGWT500

BOT Down

TOP Down

TOP Up

BOT Up

Group-B0 VREF

Group-B1 VREF

MEM_B0 CLK

Group-B0 decoupling CAP

Group-B1 decoupling CAP

MEM_B1 CLK

Quanta Computer Inc.

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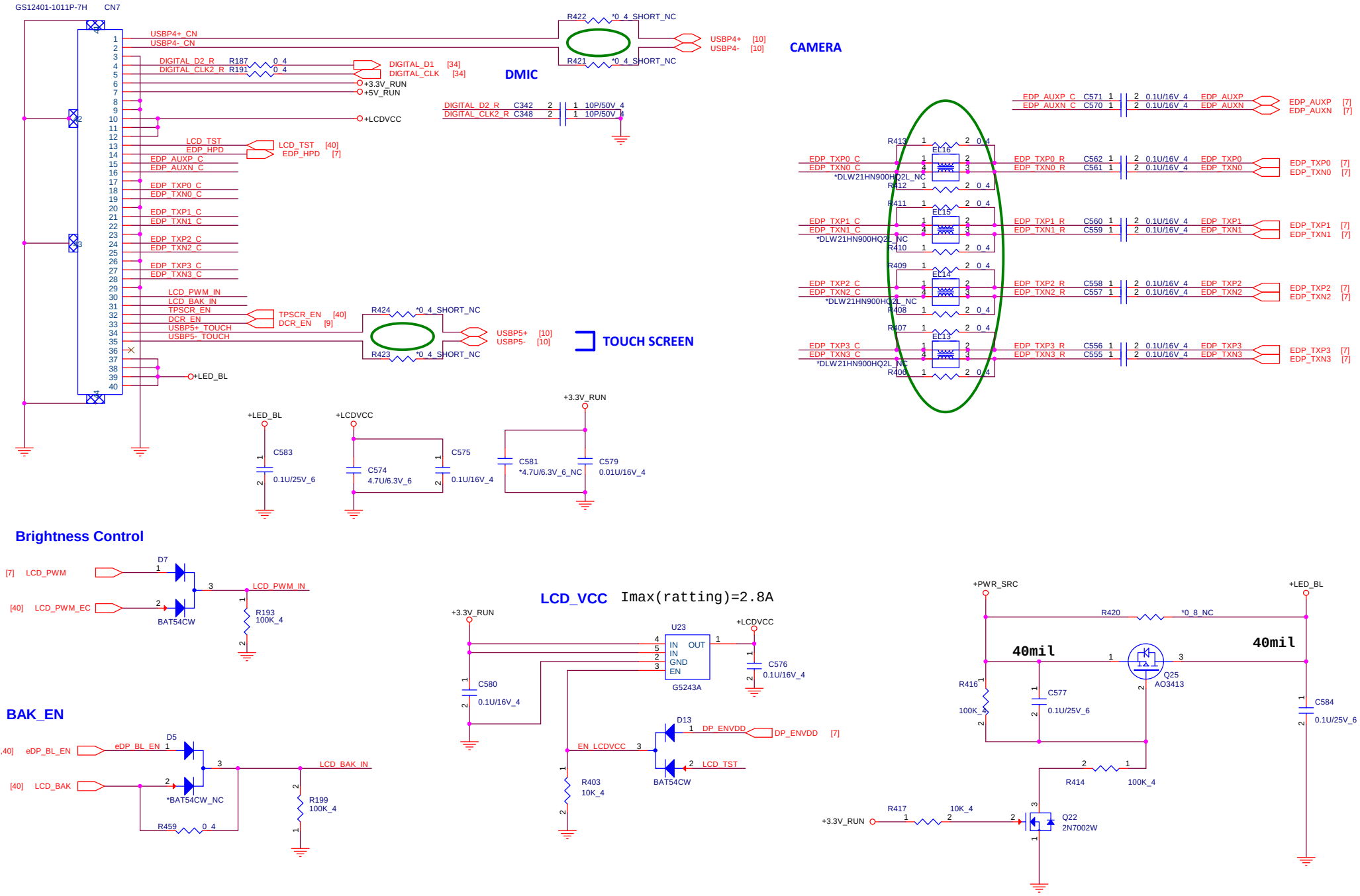
GS12401-1011P-7H CN7
USBP4+_CN
USBP4-_CN
R422 *0_4_SHORT_NC
R421 *0_4_SHORT_NC
USBP4+ [10]
USBP4- [10]
DIGITAL_D2_R R187 0_4
DIGITAL_CLK2_R R191 0_4
DIGITAL_D1 [34]
DIGITAL_CLK [34]
+3.3V_RUN
+5V_RUN
DMIC
DIGITAL_D2_R C342 2 1 10P/50V_4
DIGITAL_CLK2_R C348 2 1 10P/50V_4
+LCDVCC
LCD_TST
EDP_HPD
LCD_TST [40]
EDP_HPD [7]
EDP_AUXP_C
EDP_AUXN_C
EDP_TXP0_C
EDP_TXN0_C
EDP_TXP1_C
EDP_TXN1_C
EDP_TXP2_C
EDP_TXN2_C
EDP_TXP3_C
EDP_TXN3_C
LCD_PWM_IN
LCD_BAK_IN
TPSCR_EN
DCR_EN
TPSCR_EN [40]
DCR_EN [9]
USBP5+_TOUCH
USBP5-_TOUCH
R424 *0_4_SHORT_NC
R423 *0_4_SHORT_NC
USBP5+ [10]
USBP5- [10]
TOUCH SCREEN
+LED_BL
C583 0.1U/25V_6
C574 4.7U/6.3V_6
C575 0.1U/16V_4
C581 *4.7U/6.3V_6_NC
C579 0.01U/16V_4
CAMERA
EDP_AUXP_C C571 0.1U/16V_4 EDP_AUXP
EDP_AUXN_C C570 0.1U/16V_4 EDP_AUXN
EDP_AUXP [7]
EDP_AUXN [7]
EDP_TXP0_C
EDP_TXN0_C
*DLW21HN900HQ2L_NC
EDP_TXP0_R C562 0.1U/16V_4 EDP_TXP0
EDP_TXN0_R C561 0.1U/16V_4 EDP_TXN0
EDP_TXP0 [7]
EDP_TXN0 [7]
EDP_TXP1_C
EDP_TXN1_C
EDP_TXP1_R C560 0.1U/16V_4 EDP_TXP1
EDP_TXN1_R C559 0.1U/16V_4 EDP_TXN1
EDP_TXP1 [7]
EDP_TXN1 [7]
EDP_TXP2_C
EDP_TXN2_C
EDP_TXP2_R C558 0.1U/16V_4 EDP_TXP2
EDP_TXN2_R C557 0.1U/16V_4 EDP_TXN2
EDP_TXP2 [7]
EDP_TXN2 [7]
EDP_TXP3_C
EDP_TXN3_C
EDP_TXP3_R C556 0.1U/16V_4 EDP_TXP3
EDP_TXN3_R C555 0.1U/16V_4 EDP_TXN3
EDP_TXP3 [7]
EDP_TXN3 [7]
Brightness Control
[7] LCD_PWM
[40] LCD_PWM_EC
D7
BAT54CW
LCD_PWM_IN
R193 100K_4
BAK_EN
[7,40] eDP_BL_EN
[40] LCD_BAK
D5
*BAT54CW_NC
LCD_BAK_IN
R459 0_4
R199 100K_4
LCD_VCC Imax(ratting)=2.8A
+3.3V_RUN
U23
IN OUT
IN
GND
EN
G5243A
+LCDVCC
C580 0.1U/16V_4
C576 0.1U/16V_4
D13
DP_ENVDD
DP_ENVDD [7]
EN_LCDVCC
LCD_TST
BAT54CW
R403 10K_4
+PWR_SRC
+LED_BL
R420 *0_8_NC
40mil
40mil
Q25 AO3413
R416 100K_4
C577 0.1U/25V_6
C584 0.1U/25V_6
R414 100K_4
R417 10K_4
+3.3V_RUN
Q22 2N7002W
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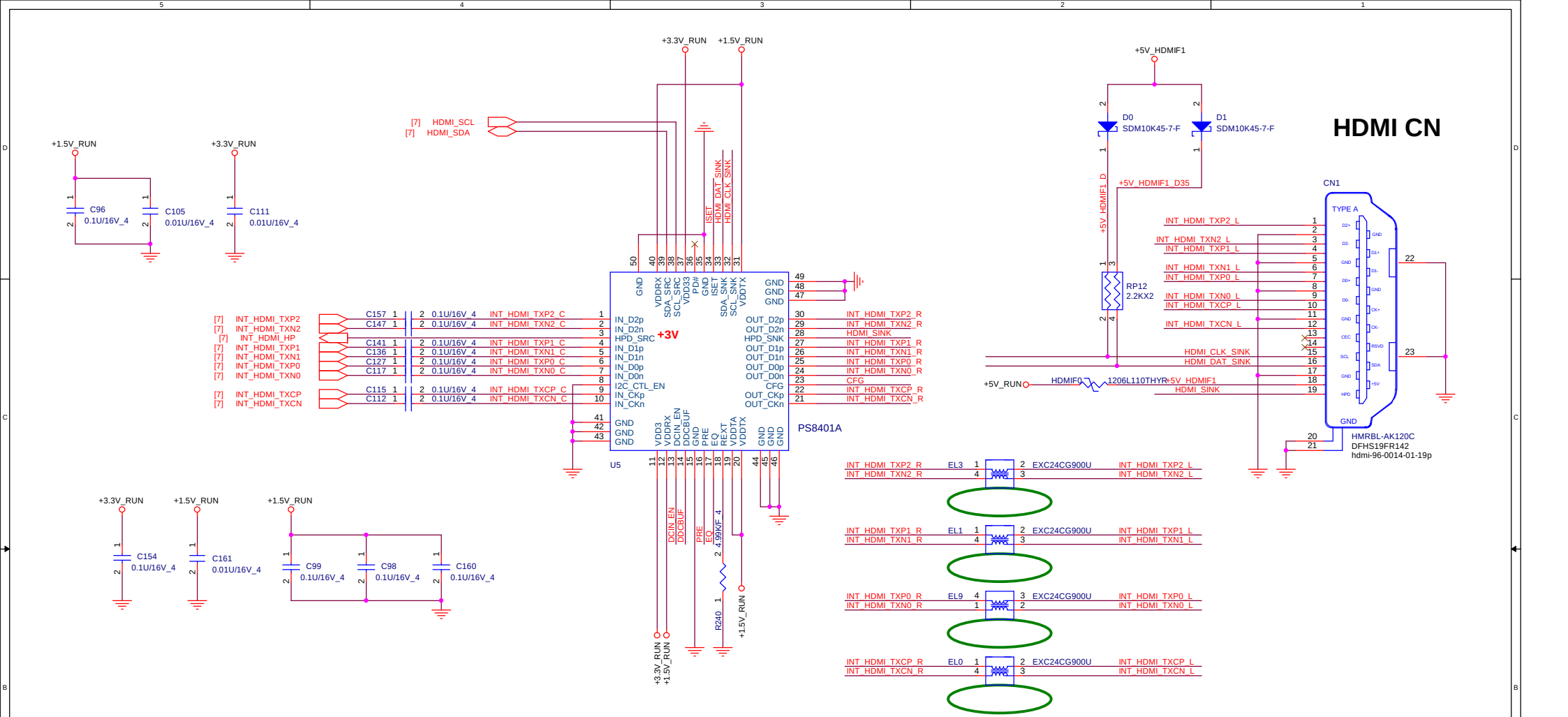


3 Level Input:
L:LOW,internal pull down
H:HIGH, external pull up
M:(VDD3)/2, both external pill-up and pull-down

DC coupling enable

Int pull-down 150k , 3.3V IO

L:default,AC coupling input
H:DC coupling input

enable active DDC buffer

Int pull-down 150k , 3.3V IO

L:default,passive DDC pass-through without internal pull up
H:active DDC buffer with internal pull up
M:active DDC buffer without internal pull up

Receiver equalization setting

Int pull-down 150k , 3.3V IO

L:programmable EQ for channel loss up to 12.4dB
H:programmable EQ for channel loss up to 4.3dB
M:programmable EQ for channel loss up to 8.6dB

configuration pin

Int pull-down 150k , 3.3V IO

L:HDMI ID disable
H:HDMI ID enable

Output pre-emphasis setting

Int pull-down 150k , 3.3V IO

L:no pre-emphasis
H:1.6dB pre-emphasis
M:2.5dB pre-emphasis

TMDS output swing adjustment

Int pull-down 150k , 3.3V IO

L:default
H:increase +13%
M:increase -13%

Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: HDMI	Rev: A
Date: Monday, May 05, 2014	Sheet 32 of 58	

H8
*H-C158D158N_NC

H6
*H-C158D158N_NC

H20
*h-o114x98d114x98n_NC

H1
*H-TC236BC197D98P2_NC

H0
*H-TC236BC197D98P2_NC

H7
*H-TC236BC197D98P2_NC

H4
*H-TC236BC197D98P2_NC

H9
*O-AM6-2_NC

H10
*h-c236i158d118p2_NC

H11
*h-c236i158d118p2_NC

H3
*h-c236i158d118p2_NC

H14
*h-c236i158d118p2_NC

H2
*H-TC236BC197D98P2_NC

H13
*O-AM6-1_NC

H12
*H-C118X98D118X98N_NC

H5
*H-C118X98D118X98N_NC

Bracket

HOLE0

*intel-CPU-bracket_NC

H17
H-TC217BC141D141PT

NGFF NUT

NUT

H15
H-TC217BC141D141PT

H16
H-TC217BC141D141PT

H18
H-TC217BC141D141PT

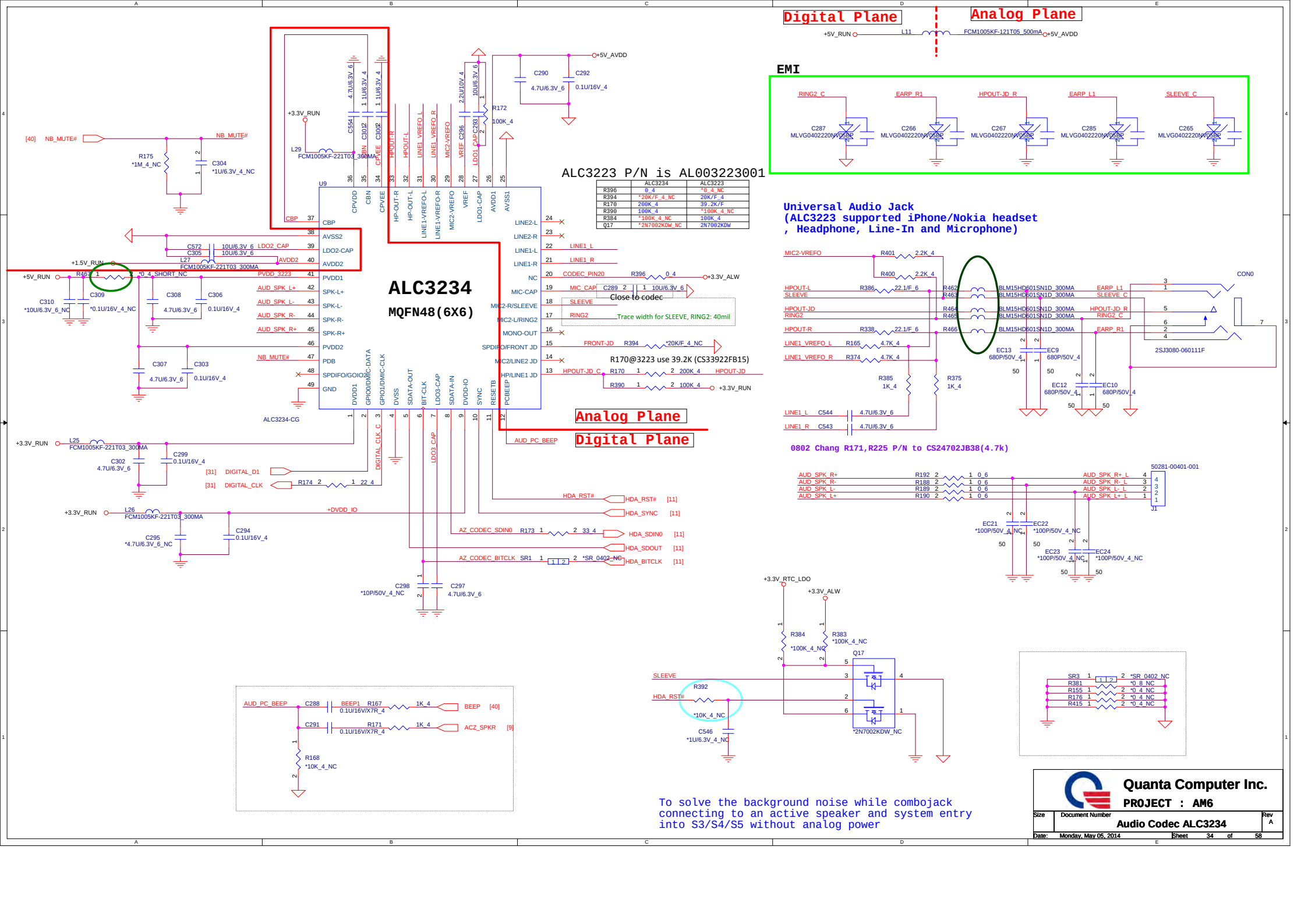
H19
H-TC217BC141D141PT

Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Hole	A

Date: Monday, May 05, 2014 Sheet 33 of 58


Digital Plane
Analog Plane
+5V_RUN
L11
FCM1005KF-121T05_500mA
+5V_AVDD
EMI
RING2_C
EARP_R1
HPOUT-JD_R
EARP_L1
SLEEVE_C
C287
C266
C267
C285
C265
MLVG0402220NV05BE
ALC3223 P/N is AL003223001
ALC3234
ALC3223
R396
0_4
*0_4_NC
R394
*20K/F_4_NC
20K/F_4
R170
200K_4
39.2K/F
R390
100K_4
*100K_4_NC
R384
*100K_4_NC
100K_4
Q17
*2N7002KDW_NC
2N7002KDW
ALC3234
MQFN48(6X6)
ALC3234-CG
Universal Audio Jack
(ALC3223 supported iPhone/Nokia headset
, Headphone, Line-In and Microphone)
Close to codec
Trace width for SLEEVE, RING2: 40mil
R170@3223 use 39.2K (CS33922FB15)
0802 Chang R171,R225 P/N to CS24702JB38(4.7k)
2SJ3080-060111F
50281-00401-001
To solve the background noise while combojack
connecting to an active speaker and system entry
into S3/S4/S5 without analog power
Quanta Computer Inc.
PROJECT : AM6
Audio Codec ALC3234
Monday, May 05, 2014
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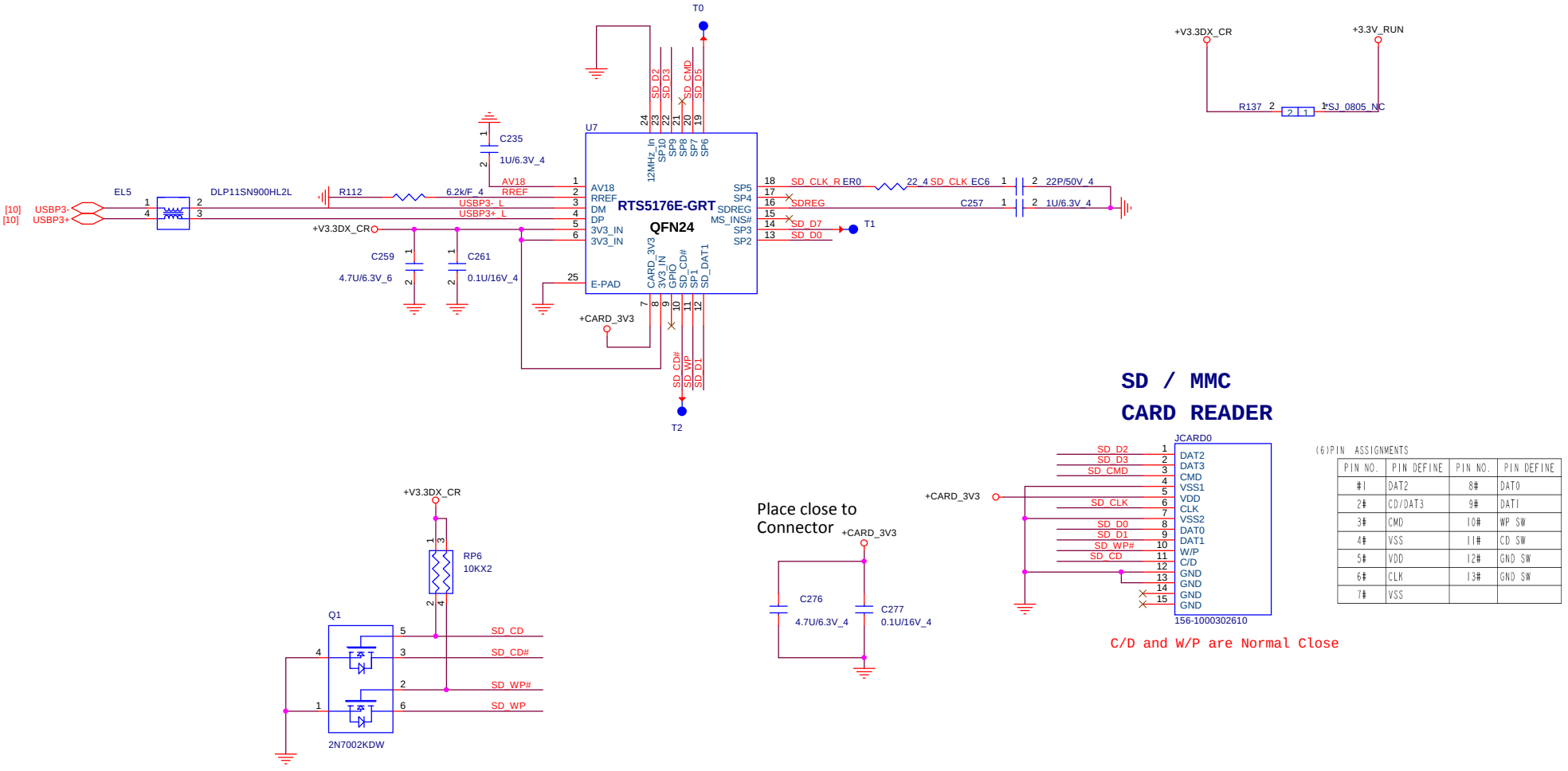


Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Card Reader RTS5176E	Rev: A
Date: Monday, May 05, 2014	Sheet 35 of 58	

USB3.0 Power Share

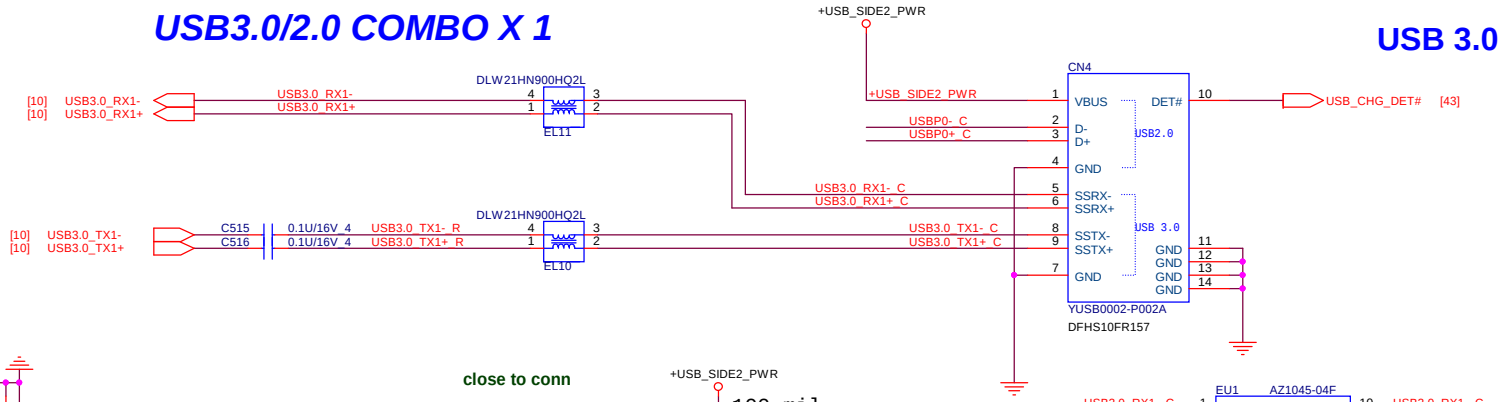
USB Power share

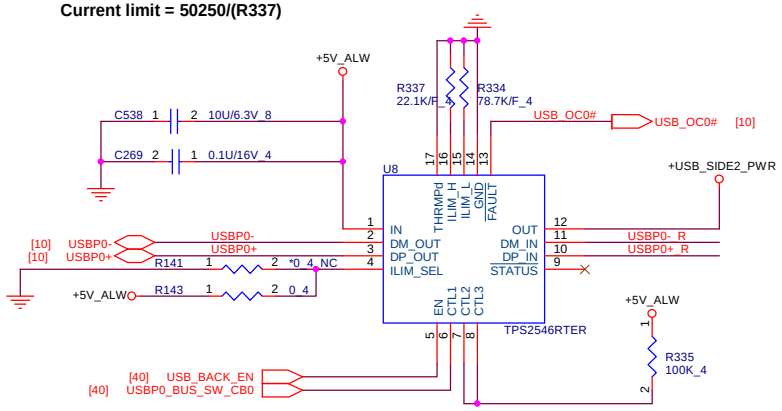
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.2

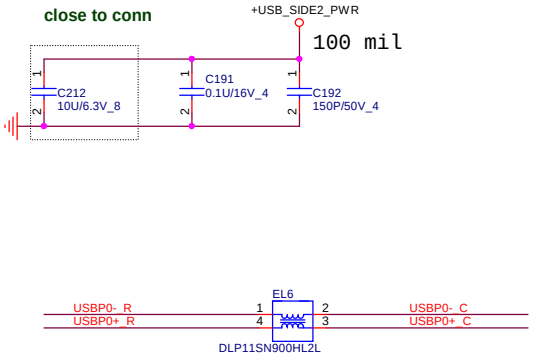
	R337	mA	
OC limitation	100k ohm	504	
	22.1k ohm	2274	Applied Now

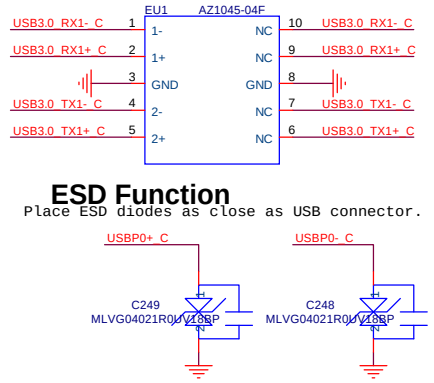
Current limit = 50250/(R337)

USB3.0/2.0 COMBO X 1







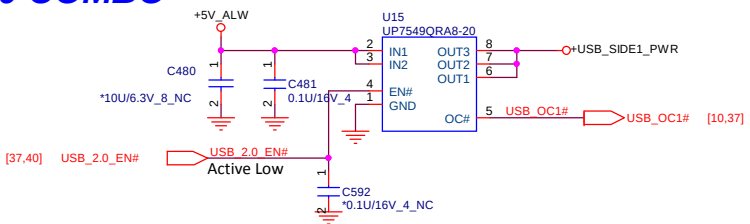


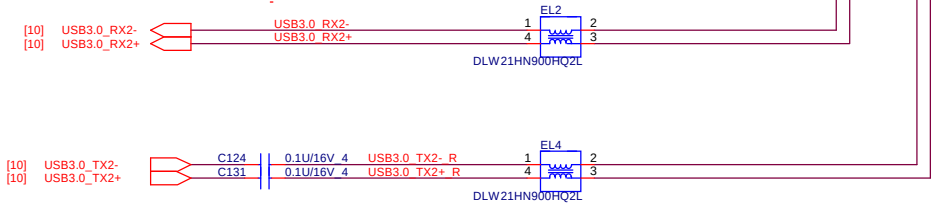
ESD Function

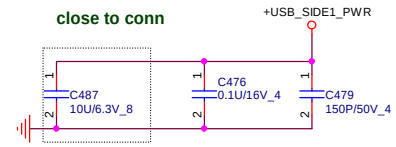
Place ESD diodes as close as USB connector.

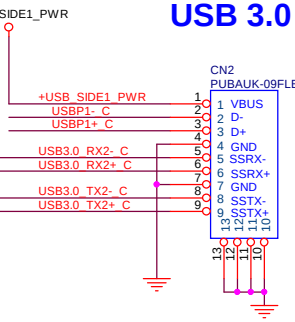
USB3.0/2.0 COMBO

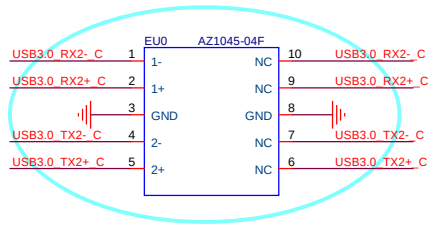
M15 Design Requirement:
I continuous 1.5A ; OC 2.0A





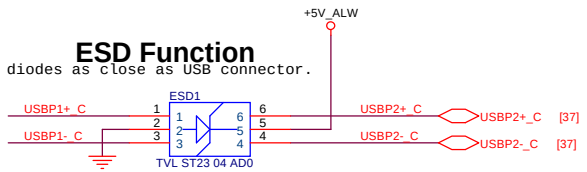






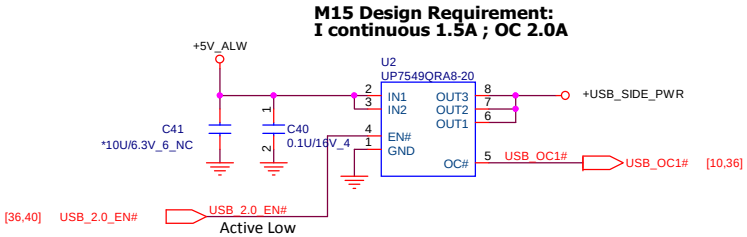
ESD Function

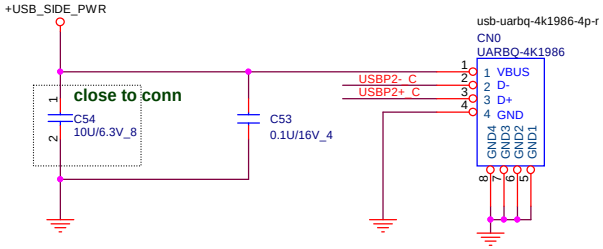
Place ESD diodes as close as USB connector.

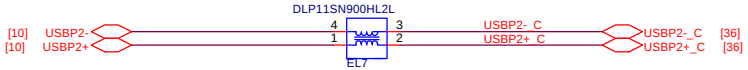


Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: USB3/USB Charger	Rev: A
Date: Monday, May 05, 2014	Sheet 36 of 58	

USB2.0 X1







Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: USB2*1	Rev: A
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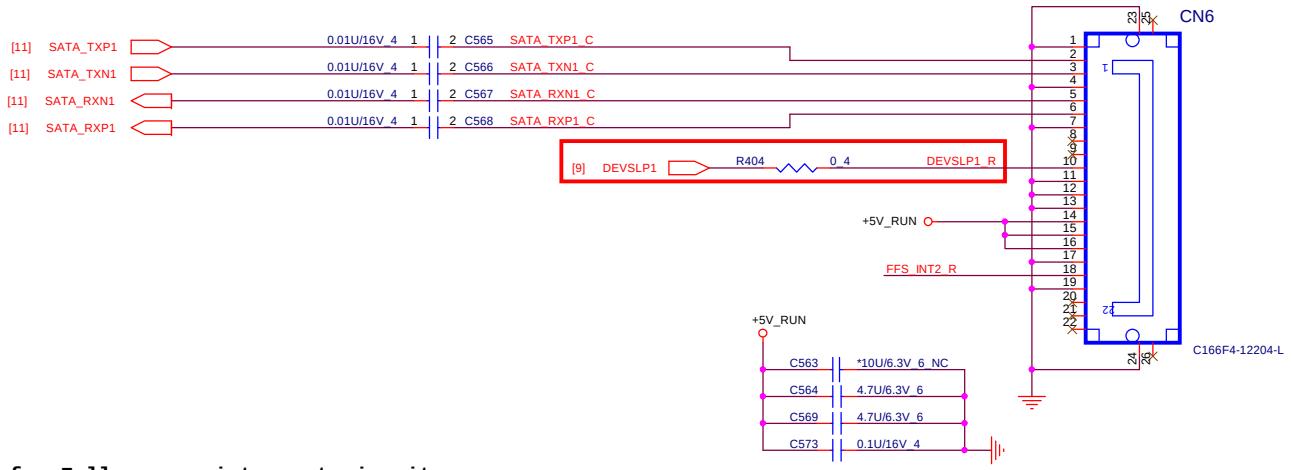
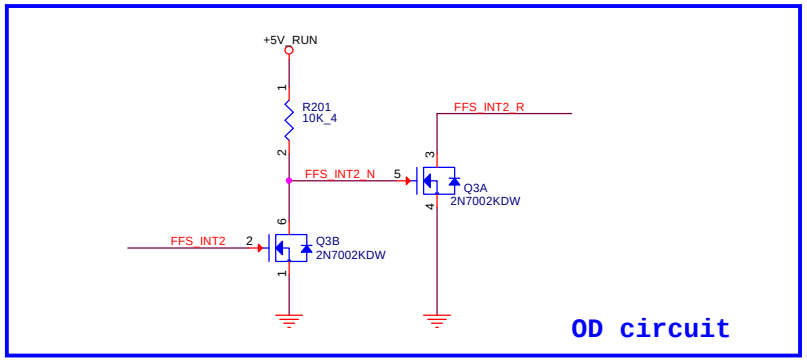
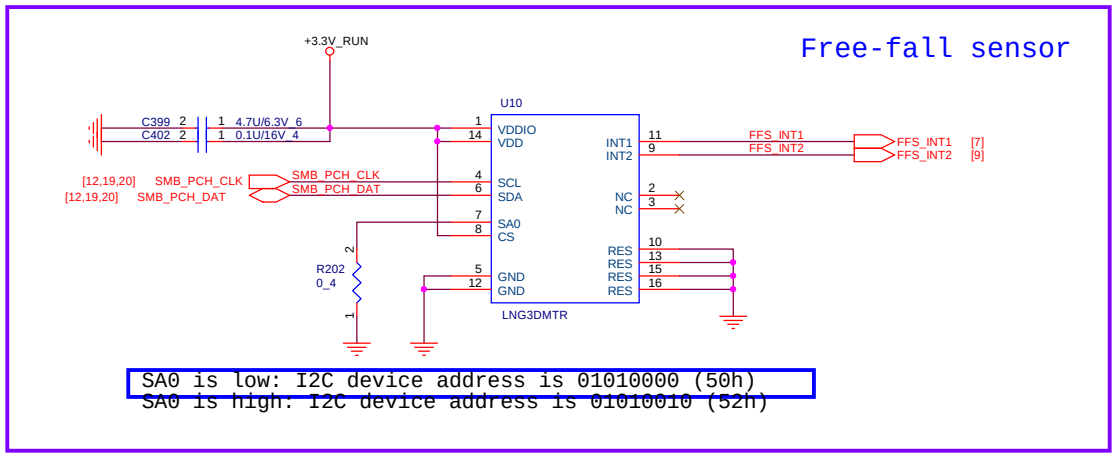
SATA HDD Connector



If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit





Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	SATA HDD/Accelerometer	A

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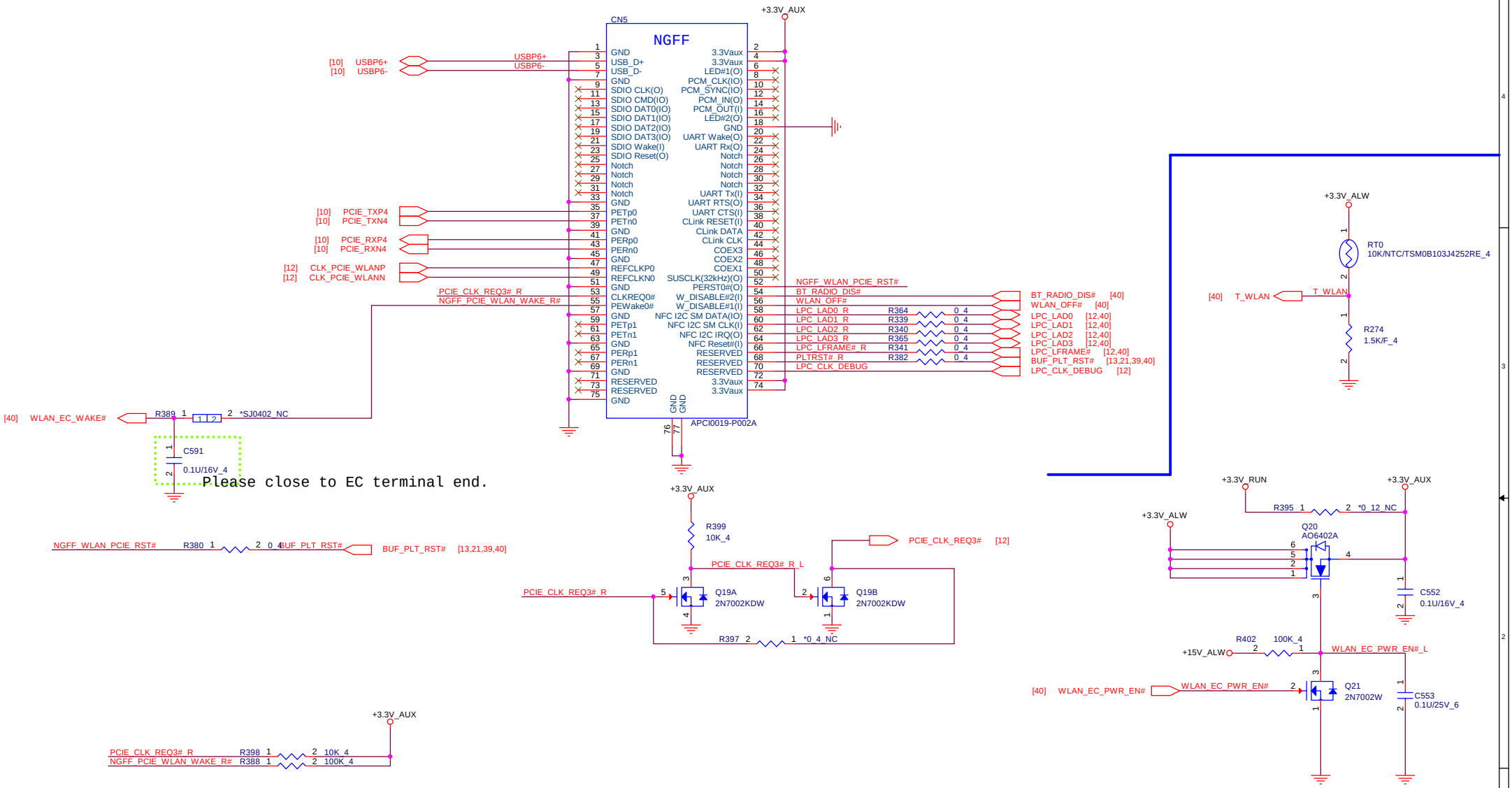
NGFF Wifi/BT connector



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Wifi/BT NGFF	Rev: A
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Place these caps close to ITE8528.

IT8528

U19
IT8528E/FX

SM BUS
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
PECI/SMCLK2/GPF6(3)
SMDAT2/GPF7(3)

PS/2
PS2CLK0/TMB0/CEC/GPF0
PS2DAT0/TMB1/GPF1
PS2CLK2/GPF4
PS2DAT2/GPF5

GPIO

LPC
LAD0/GPM0(3)
LAD1/GPM1(3)
LAD2/GPM2(3)
LAD3/GPM3(3)
LPCRST#/GPD2
LPCCLK/GPM4(3)
LFRAME#/GPM5(3)
LPCPD#/GPE6
GA20/GPB5(3)
SERIRQ/GPM6(3)
ECSMI#/GPD4(3)
ECSC#/GPD3
WRST#
KBRST#/GPB6(3)
PWUREQ#/BBO/SMCLK2ALT/GPC7(3)

CIR
CRX0/GPC0
CTX0/TMA0/GPB2(3)

PWM
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
TACH0A/GPD6(3)
TACH1A/TMA1/GPD7(3)
TMRI0/GPC4(3)
TMRI1/GPC6(3)

UART port
DAC4/DCD0#/GPJ4(3)
FDIO3/DSR0#/GPG6
GINT/CTS0#/GPD5
PS2DAT1/RTS0#/GPF3
DAC5/RIG0#/GPJ5(3)
PS2CLK1/DTR0#/GPF2
TXD/SOUT0/GPB1
RXD/SIN0/GPB0
ADC5/DCD1#/GPI5(3)
ADC6/DSR1#/GPI6(3)
ADC7/CTS1#/GPI7(3)
RTS1#/GPE5
PWM7/RIG1#/GPA7
FDIO2/DTR1#/SBUSY/GPG1/ID7(Dn)
CTX1/SOUT1/GPH2/SMDAT3/ID2
CRX1/SIN1/SMCLK3/GPH1/ID1

WAKE UP
PWRSW/GPE4(3)
RI1#/GPD0(3)
RI2#/GPD1
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7

EXTERNAL SERIAL FLASH
FSCK
FSCE#
FMOSI
FMISO

SPI ENABLE
KSO16/SMOSI/GPC3(3)
KSO17/SMISO/GPC5(3)
PWM6/SSCK/GPA6
SSCE0#/GPG2
SSCE1#/GPG0(Up)

A/D D/A
ADC0/GPI0(3)
ADC1/GPI1(3)
ADC2/GPI2(3)
ADC3/GPI3(3)
ADC4/GPI4(3)
TACH2/HDIO2/GPJ0(3)
HDIO3/GPJ1(3)
DAC2/TACH0B/GPJ2(3)
DAC3/TACH1B/GPJ3(3)

KBMX
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15

CLOCK
CK32KE/GPJ7(3)
CK32K/GPJ6(3)

GPJ7 can be configured as GPO only if "Crystal-Free" feature is activated.

It is necessary to connect this pin to the ground if "Crystal-Free" feature is activated and GPJ6 is not configured as GPI/GPO.

Charge ,BAT PCH

Thermal, ALS

Board ID Straps

100K/F_4: CS41002FB28
45.3K/F_4: CS34532FB18
24.3K/F_4: CS32432FB19
12K/F_4 : CS31202FB15
6.49K/F_4: CS26492FB23
1.65K/F_4: CS21652FB29

BD0		
000	0.5V_PU 100K	HSW UMA
001	1.0V_PU 45.3K	HSW DIS
010	1.5V_PU 24.3K	BDW UMA
100	2.0V_PU 12K	BDW DIS
101	2.5V_PU 6.49K	
110	3.0V_PU 1.65K	
111	0V_NO PU	

BD1		
000	0.5V_PU 100K	EVT (X00)
001	1.0V_PU 45.3K	DVT1 (X01)
010	1.5V_PU 24.3K	DVT2 (X02)
100	2.0V_PU 12K	Pilot Build (A00)
101	2.5V_PU 6.49K	
110	3.0V_PU 1.65K	
111	0V_NO PU	

Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	SIO (ITE8528H)	A
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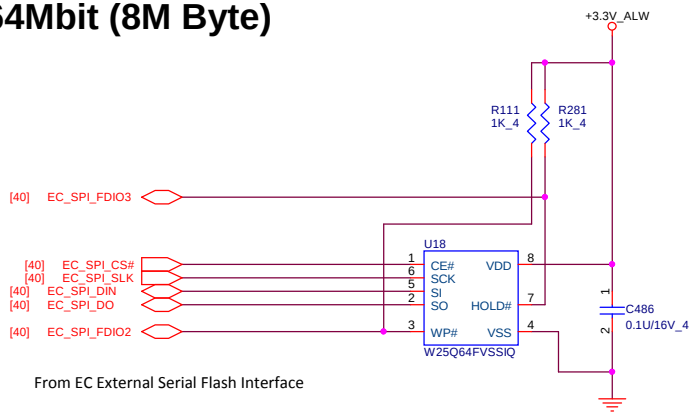
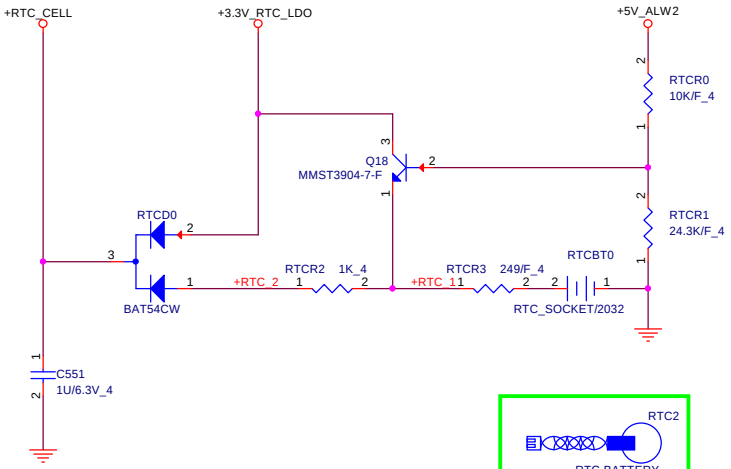
For EC 64Mbit (8M Byte)



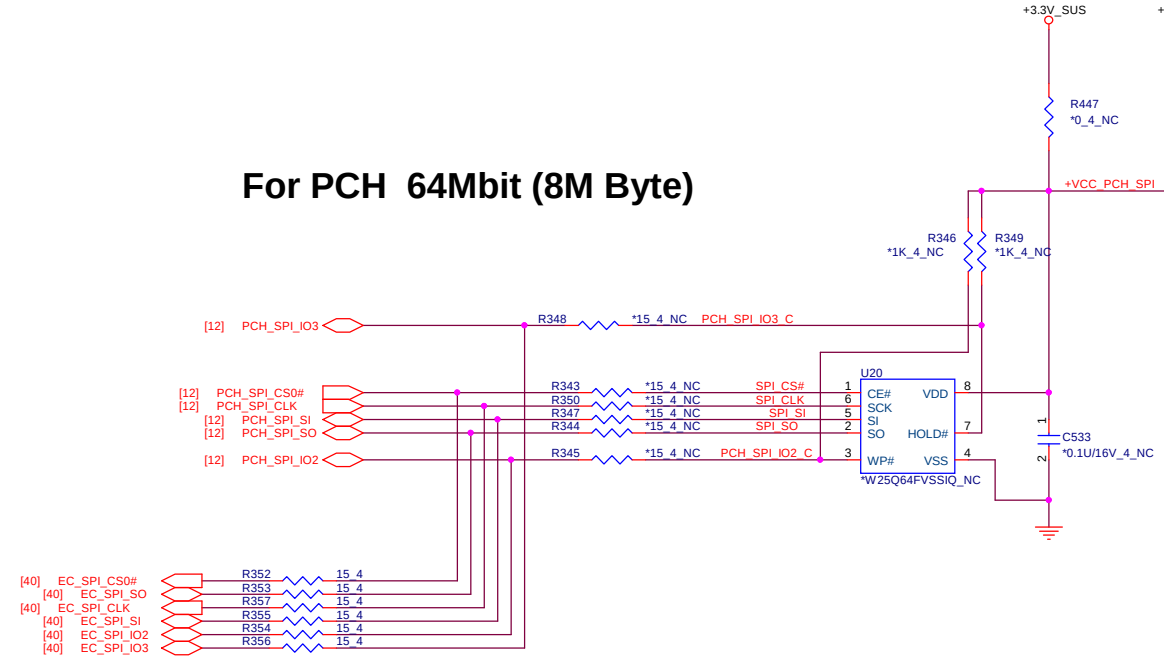
From EC External Serial Flash Interface

RTC BATTERY



5*[24.3/(24.3+10)]-0.8=2.74V
RTC Battery Charger when lower than 2.74V

For PCH 64Mbit (8M Byte)



To EC Slave Interface

Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	FLASH / RTC	A
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Keyboard Connector

[40] MY[0..16] MY[0..16]

[40] MX[0..7] MX[0..7]

CN8

196504-30041-3
196528-30041-3-30p-I

[7] KB_DET# KB_DET#

MX7 MX6 MX4 MX2 MX5 MX1 MX3 MX0 MY5 MY4 MY7 MY6 MY8 MY3 MY1 MY2 MY0 MY12 MY16 MY15 MY13 MY14 MY9 MY11 MY10

Vi(on_max)= -1.7V
Vi(off_min)=-0.5

+5V_RUN

Q24
LTA014YUBFS8TL
47K
10K

[40] CAP_LED CAP_LED
High Active

Q23
2N7002W

330_4 R405

CAP_LED_L

4.85mA

BREATH_LED

BREATH_PWRLED# LED0 PWR_LED# R_R5 620_4 +5V_ALW
LED_White

[40] BREATH_LED BREATH_LED

Q8
2N7002W

MY1	C356	1	2	100P/50V_4
MY2	C374	1	2	100P/50V_4
MY4	C377	1	2	100P/50V_4
MY0	C355	1	2	100P/50V_4
MX4	C362	1	2	100P/50V_4
MX6	C381	1	2	100P/50V_4
MX3	C360	1	2	100P/50V_4
MX2	C380	1	2	100P/50V_4
MY5	C359	1	2	100P/50V_4
MY6	C376	1	2	100P/50V_4
MY3	C375	1	2	100P/50V_4
MY7	C358	1	2	100P/50V_4
MY8	C357	1	2	100P/50V_4
MY9	C352	1	2	100P/50V_4
MY10	C351	1	2	100P/50V_4
MY11	C370	1	2	100P/50V_4
MX7	C363	1	2	100P/50V_4
MX0	C378	1	2	100P/50V_4
MX5	C361	1	2	100P/50V_4
MX1	C379	1	2	100P/50V_4
MY12	C373	1	2	100P/50V_4
MY13	C353	1	2	100P/50V_4
MY14	C371	1	2	100P/50V_4
MY15	C372	1	2	100P/50V_4
MY16	C354	1	2	100P/50V_4

+3.3V_TP

25 mils

R425
*0_4_SHORT_NC

+3.3V_TP_PWR

C585 0.1U/16V_4

CN9

[9] I2C1_PCH_DAT
[9] I2C1_PCH_CLK

I2C1_PCH_DAT
I2C1_PCH_CLK

TP_INTR#
TP_DIS#

[40] TP_DIS#
[40] TPDATA
[40] TPCLK

R433 0_4
R429 0_4

TPDATA-1
TPCLK-1

C586 10P/50V_4
C587 10P/50V_4

50503-00841-001
88513-0801-8p-I
DFFC08FR029

+3.3V_TP

R432 4.7K_4 TPDATA
R428 4.7K_4 TPCLK

Key board illumination

+KB_LED power trace width >10 mil

+5V_RUN 1206L050YR +KB_LED
FS0 1206

+KB_LED
51601-0040m-v01-4p-I
DFFC04FR122
51601-0040M-V01

[9] KB_LED_DET KB_LED_DET R419 100K_4 KB_LED_DET_R

LED_PWM

R418 200K_4

C582 0.1U/16V_4

J0

Q26
2N7002K

LED_PWM

[40] KB_BACKLITE_EN KB_BACKLITE_EN

KB BL CONN will be changed to 51601-0040M-V01 at PT stage

Touch Pad Connector

+3.3V_TP

R449
*100K_4_NC

[9] PCH_TP_INTR#

*2N7002W_NC
Q38

R458
0_4

TP_INTR#

[40] TP_INTR#

+3.3V_TP

R456
*33_6_NC

Q37B
*2N7002KDW_NC

[40] TP_PWR_EN#

+15V_ALW

R452
*100K_4_NC

Q37A
*2N7002KDW_NC

+3.3V_SUS +3.3V_TP

R457 0_6

Q39
*2N7002K_NC

C589
*0.1U/16V_4_NC

TP_PWR_EN

C590
*0.1U/16V_4_NC

Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	KB/CLK Gen/FAN/TP	A

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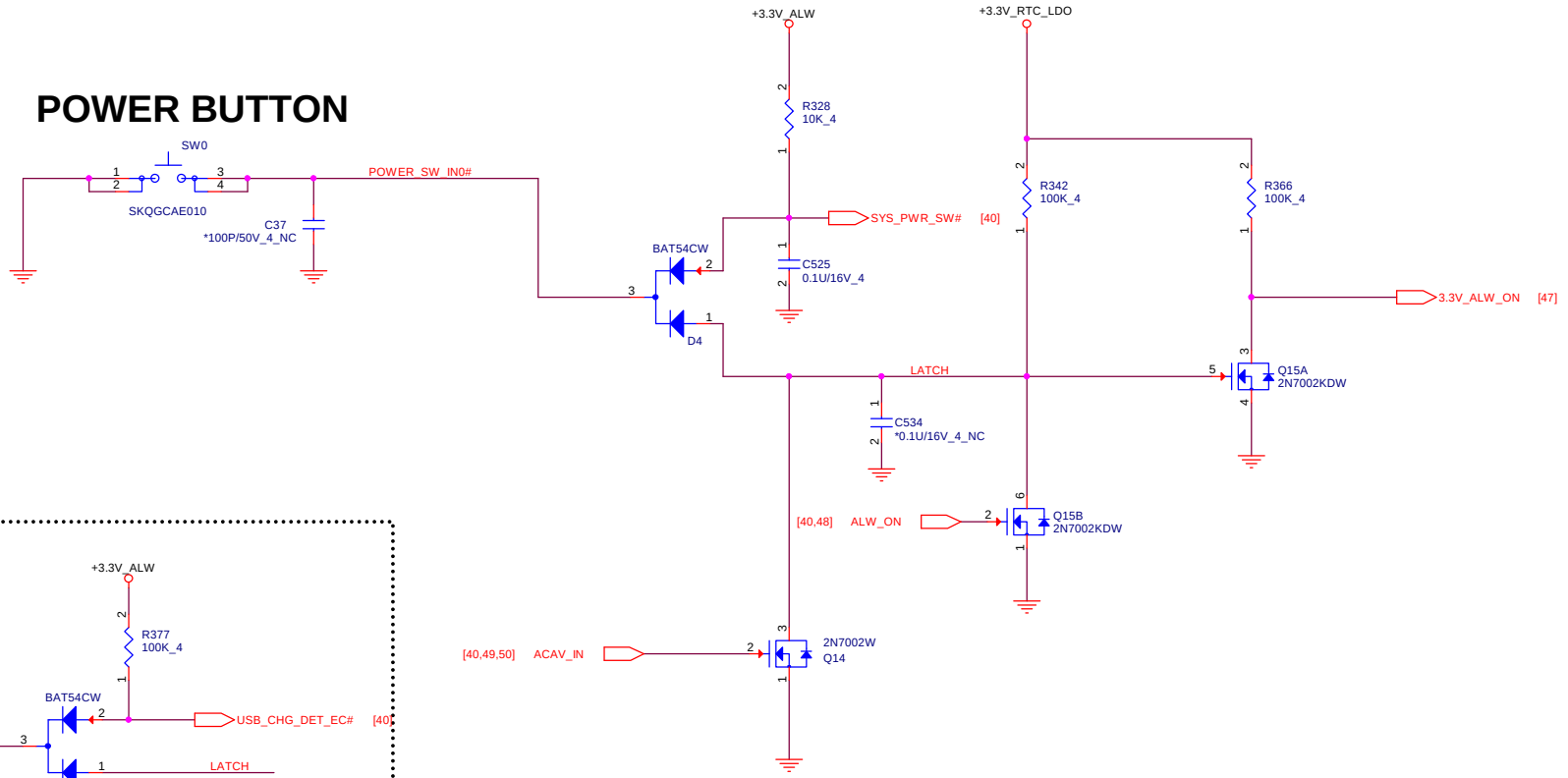
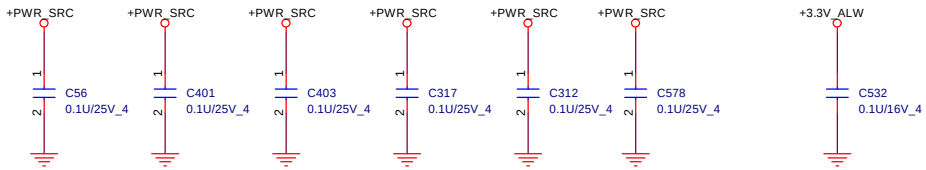
3VALW ON POWER LOGIC

POWER BUTTON



Stitching Capacitors



Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	3VALW ON POWER LOGIC	A

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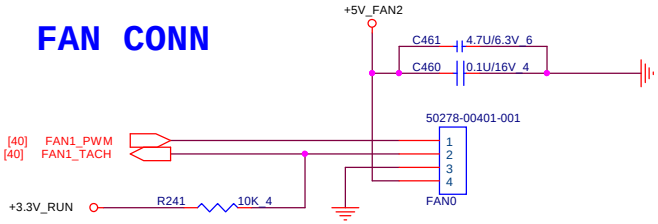
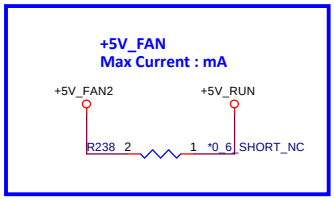
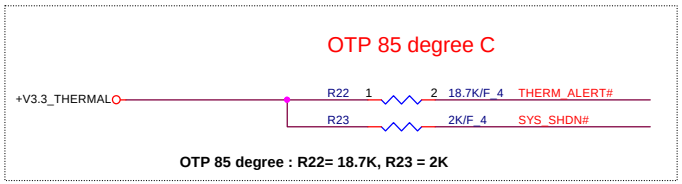
FAN CONN



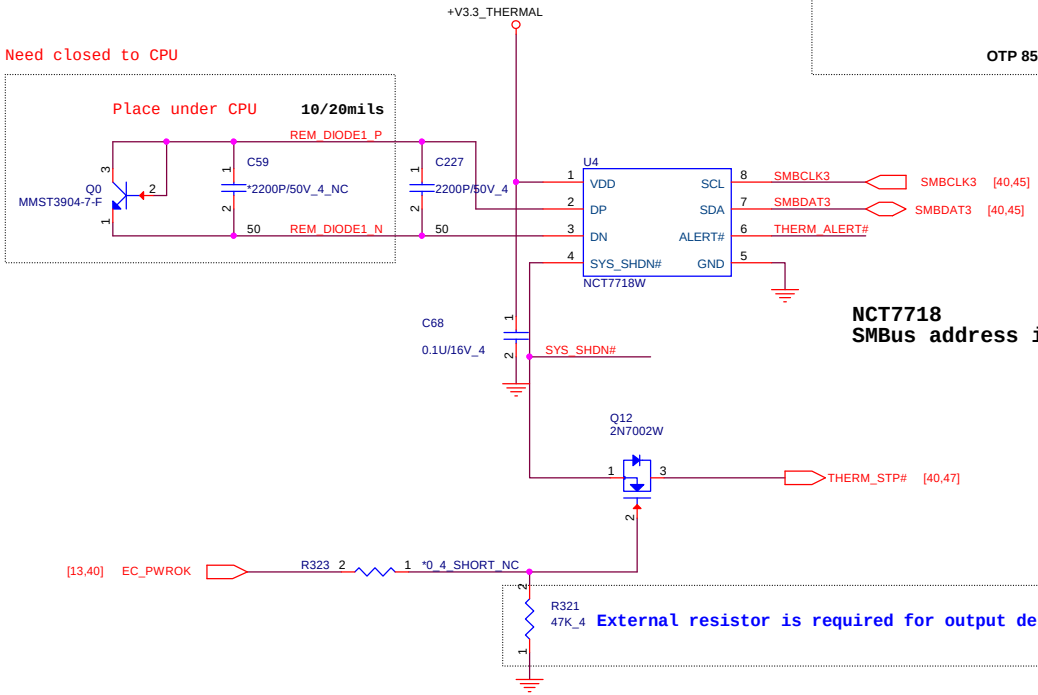


THERMAL IC

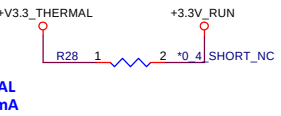


OTP 85 degree : R22= 18.7K, R23 = 2K

SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C



NCT7718
SMBus address is 1001100xb (98h) (x is R/W bit).



+V3.3_THERMAL
Max Current :mA

Quanta Computer Inc.
PROJECT : AM6

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	FAN & THERMAL	A

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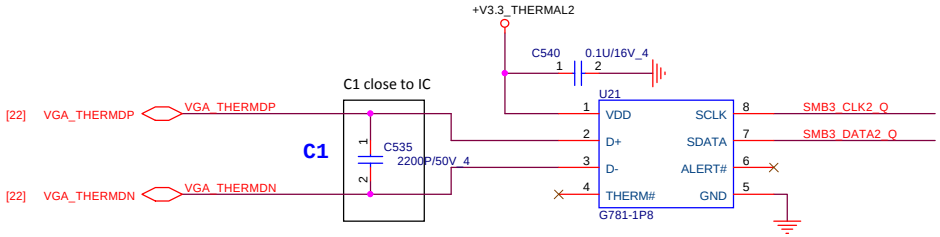
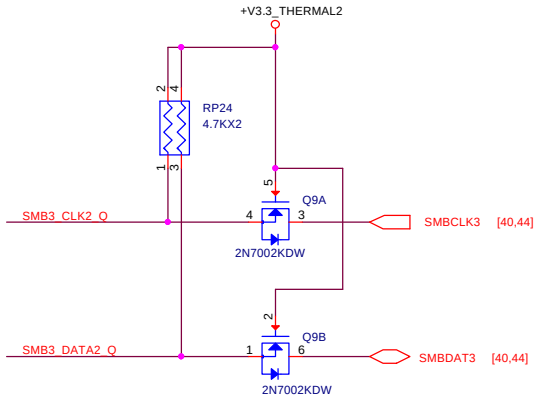
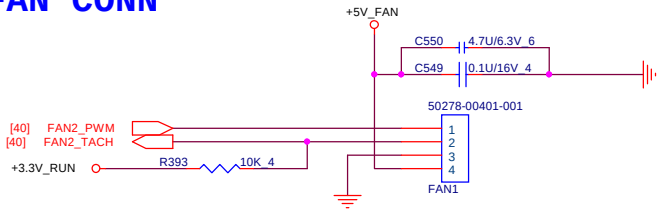
For GPU use

G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).

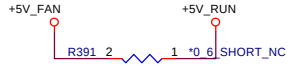


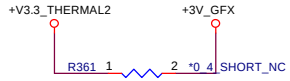


FAN CONN



+5V_FAN
Max Current : mA





+V3.3_THERMAL
Max Current :mA

Quanta Computer Inc.		
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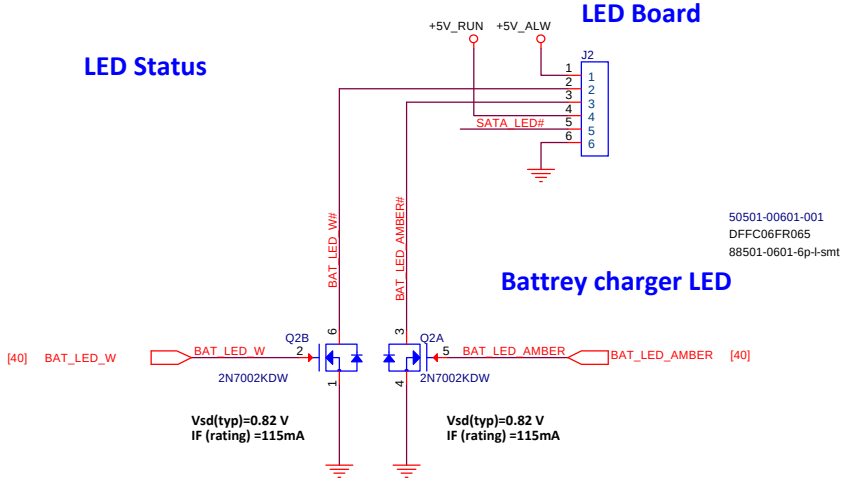
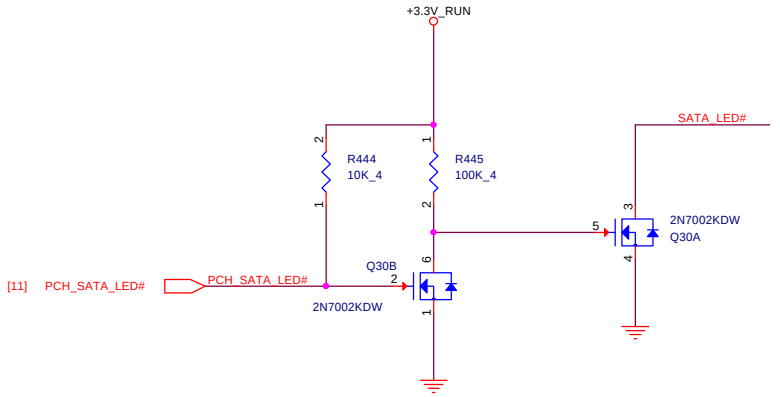
LED Board

LED Status



HDD activity LED.



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: LED	Rev: A
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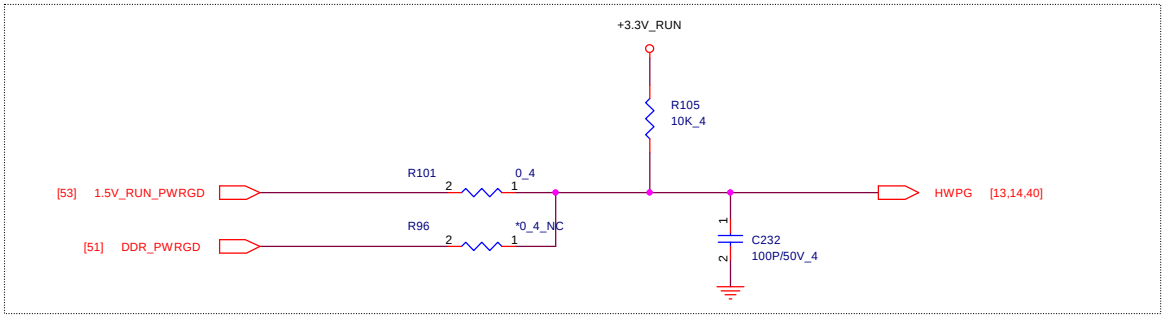

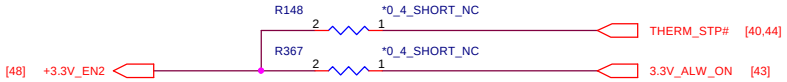

Quanta Computer Inc.

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Size	Document Number	Rev
	System Reset Circuit	A

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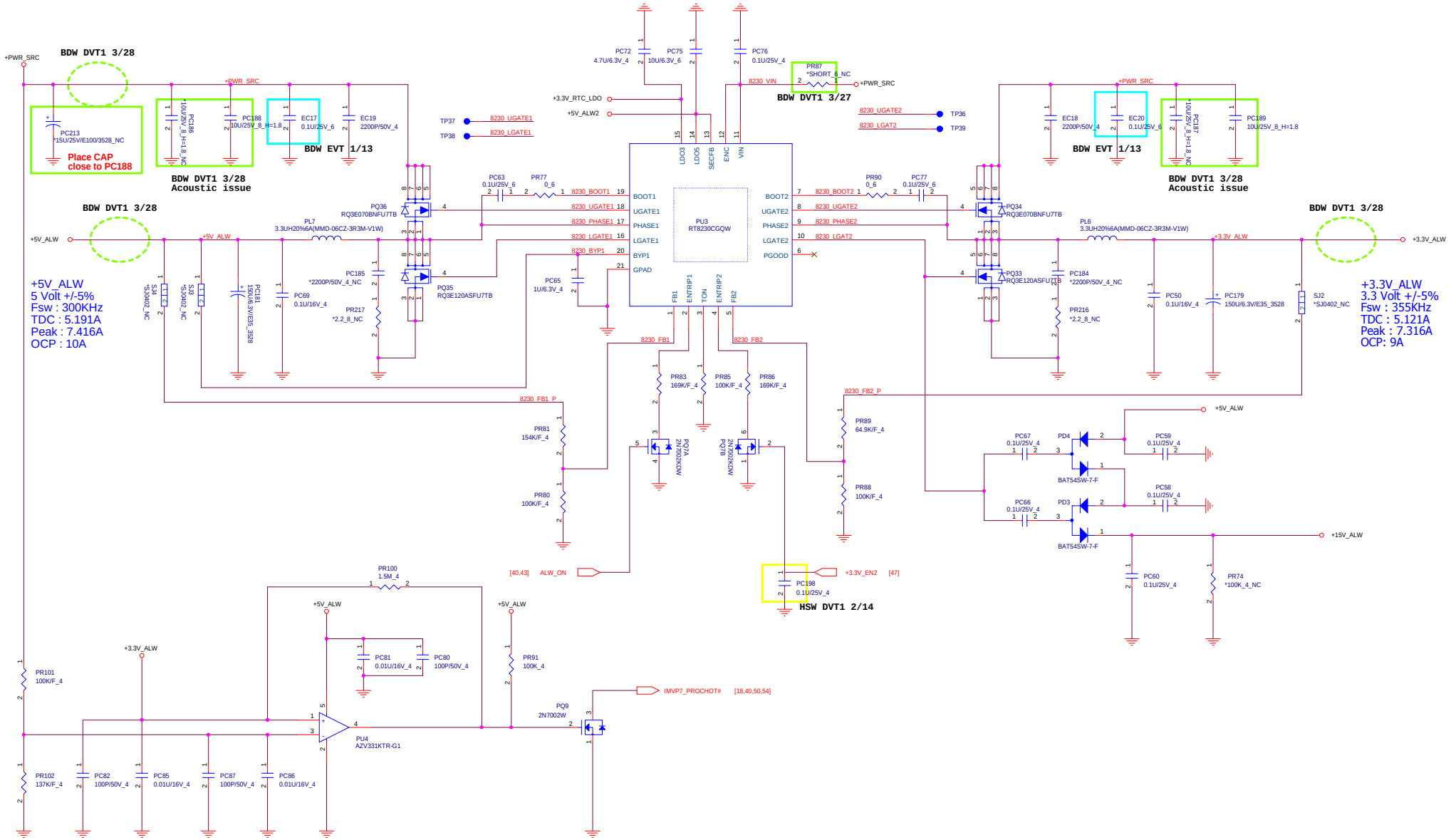

Quanta Computer Inc.		
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Size	Document Number: 3V/5V (RT8230CGQW)	Rev: A
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BDW EVT 1/16
EMI request

EC38 4700P/50V_4
PC191 0.1U/25V_4
PC194 1000P/50V_4
PC193 2200P/50V_4
+VCHGR

JBAT0
51202-00901-V01
DFHD09MR104
gs73091-10272-7h-9p-luv_ab

SMBCLK0_B PR105 100_4 SMBCLK0 → SMBCLK0 [40,50]
SMBDAT0_B PR97 100_4 SMBDAT0 → SMBDAT0 [40,50]
PR98 100_4 → PBAT_PRES# [40]

+3.3V_ALW
PR96 10K_4

+DCIN_JACK
EC28 0.01U/25V_4
EC27 4700P/50V_4
EC26 68P/50V_4
Reserve for EMI Solution

FL0 MHC2012S800UBP(80,5A)
+DC_IN
PC168 2200P/50V_4
PC167 1000P/50V_4
PC166 0.1U/25V_4
PC170 0.1U/25V_4

+5V_ALW2
PR53 100K_4
PQ0 2N7002W
PQ1 2N7002W
[40,43,50] ACAV_IN

For Hiccup mode
BDW DVT1 3/5
PR52 6.8K_4
PR51 6.8K_4
PR50 *0_4_NC

PBAT_PRES#
ESD0 *TVL ST23 04 AD0_NC
SMBCLK0
SMBDAT0
+3.3V_ALW

BDW EVT 1/16
EMI request
+DC_IN_SS
EC33 4700P/50V_4
EC7 0.1U/25V_4
EC8 1000P/50V_4
+DC_IN
EC29 *10P/50V_4_NC
Reserve for EMI Solution

CN3
Adapter2+ 5 +DCIN_JACK
Adapter1+ 4
PSID 3 DOCK_PSID
Adapter2- 2
Adapter1- 1
50291-0050N-002

FL1 BLM15AG102SN1D(1000,200MA)
EOD part
HSW DVT1 2/14

PQ21 FDV301N_G
PR54 33_4
PS_ID [40]
PD0 DA204UGT106
PR57 2.2K_4
PR199 10K_4
+5V_ALW2
PR197 100K_4
PQ23 MMST3904-7-F
PR198 15K_4
PC169 100P/50V_4

Quanta Computer Inc.		
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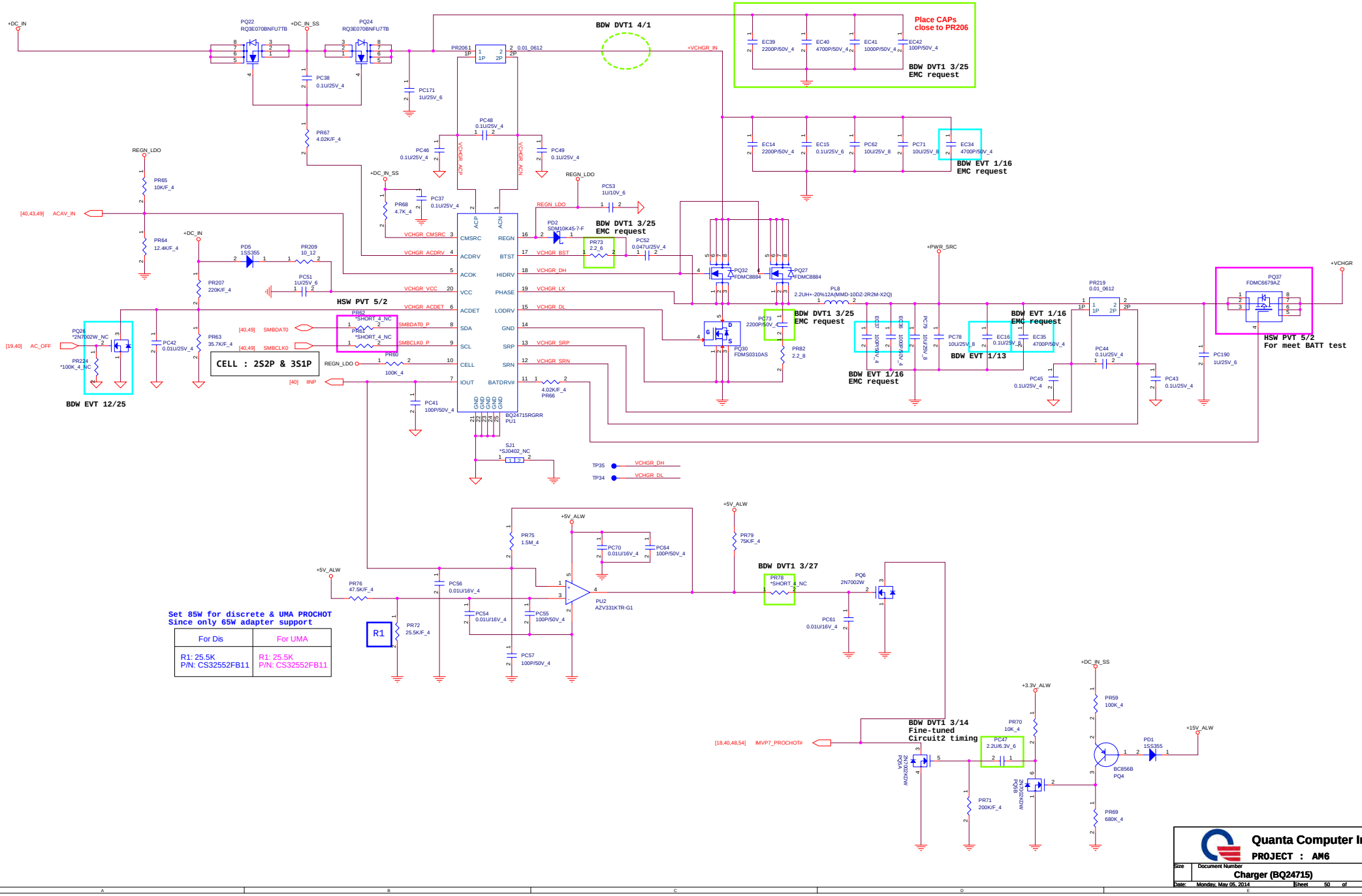
BDW DVT1 4/1
Place CAPs close to PR206
BDW DVT1 3/25 EMC request
BDW EVT 1/16 EMC request
BDW DVT1 3/25 EMC request
HSW PVT 5/2
BDW EVT 1/16 EMC request
BDW EVT 1/13
HSW PVT 5/2 For meet BATT test
BDW EVT 12/25
CELL : 2S2P & 3S1P
BDW DVT1 3/27
BDW DVT1 3/14 Fine-tuned Circuit2 timing
Set 85W for discrete & UMA PROCHOT Since only 65W adapter support
For Dis
For UMA
R1: 25.5K P/N: CS32552FB11
R1: 25.5K P/N: CS32552FB11
Quanta Computer Inc.
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Charger (BQ24715)
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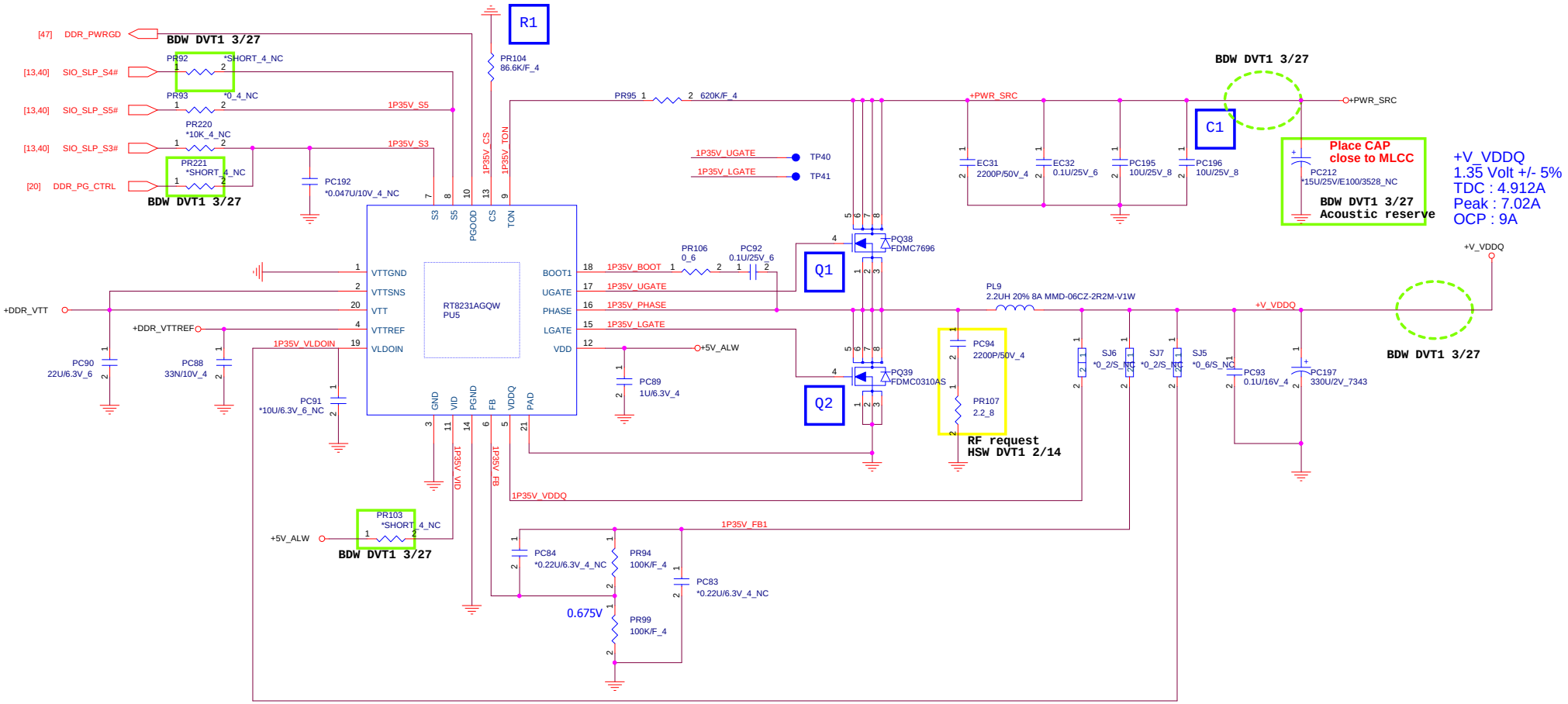

Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: 1.35_DDR/0.675(RT8231)	Rev: A
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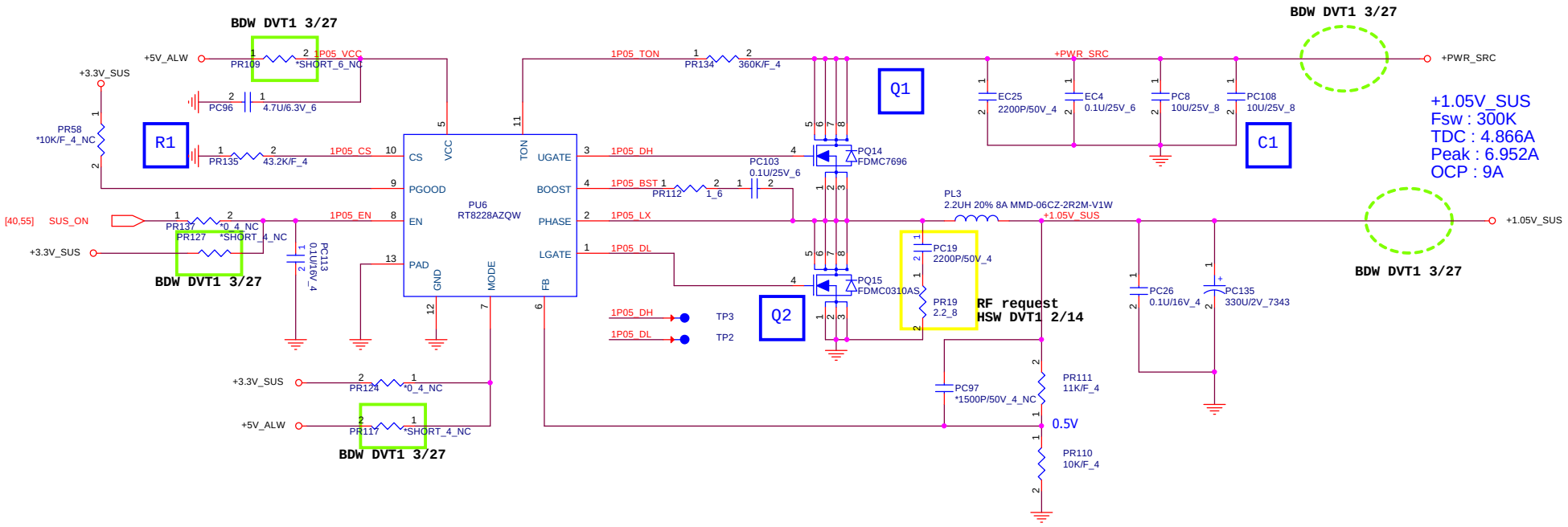

Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: 1.05V_SUS (RT8228AZ)	Rev: A
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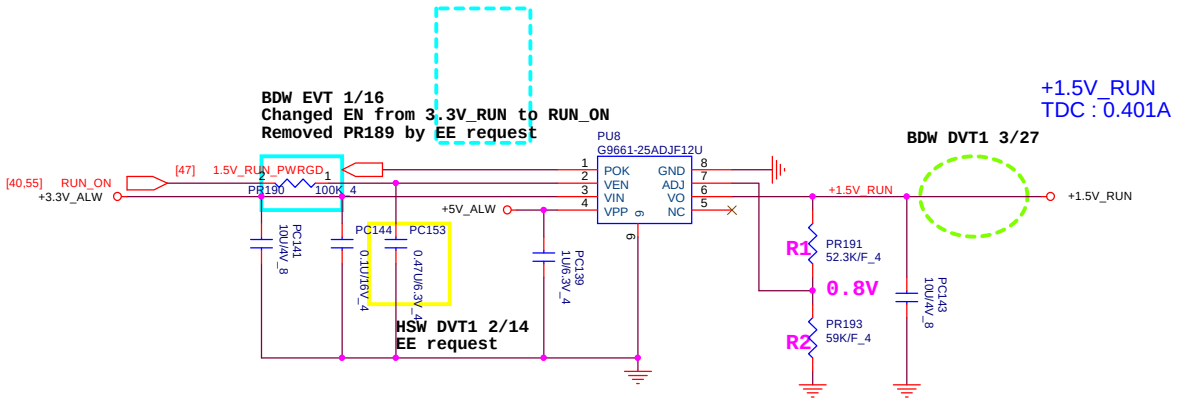

Quanta Computer Inc.		
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Size	Document Number: +1.5V_RUN (G9661-25ADJF12U)	Rev: A
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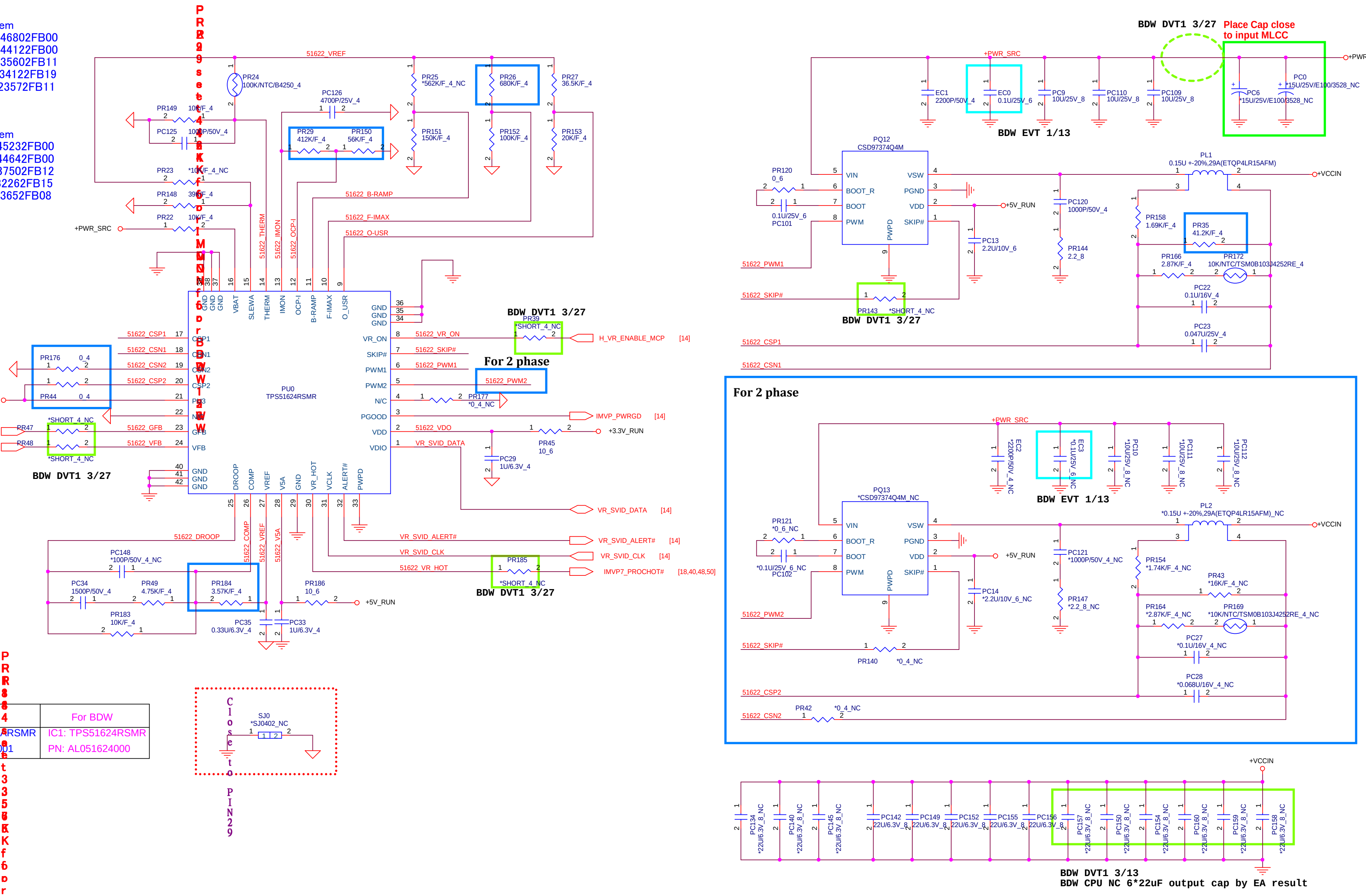
For BDW 15W change item
PR26 680k --> CS46802FB00
PR29 412k --> CS44122FB00
PR150 56k --> CS35602FB11
PR35 41.2k --> CS34122FB19
PR184 3.57k --> CS23572FB11

For BDW 28W change item
PR26 523k --> CS45232FB00
PR29 464k --> CS44642FB00
PR150 75k --> CS37502FB12
PR35 22.6k --> CS32262FB15
PR184 3.65k --> CS23652FB08



For HSW	For BDW
IC1: TPS51622ARSMR	IC1: TPS51624RSMR
PN: AL051622001	PN: AL051624000

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Size	Document Number	Rev
	CPU Core (TPS51624RSMR)	A

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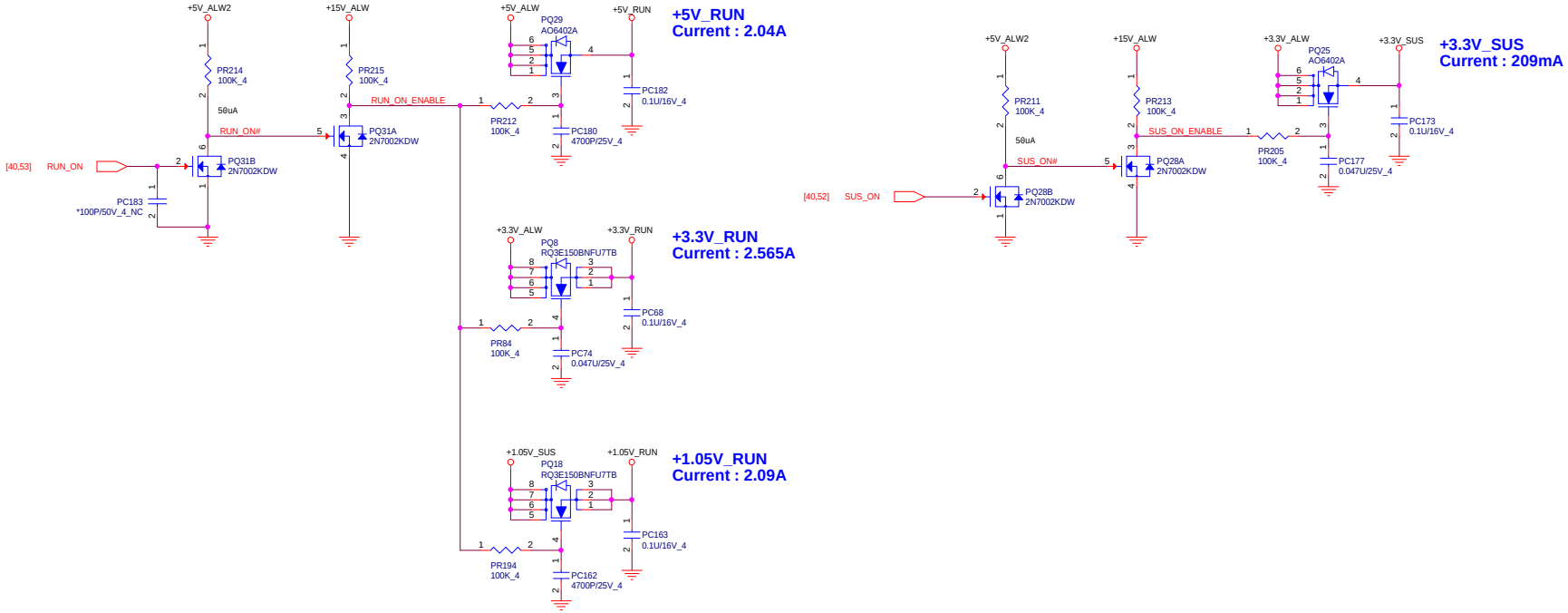

Quanta Computer Inc.		
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	SUS_RUN Power Switch	A
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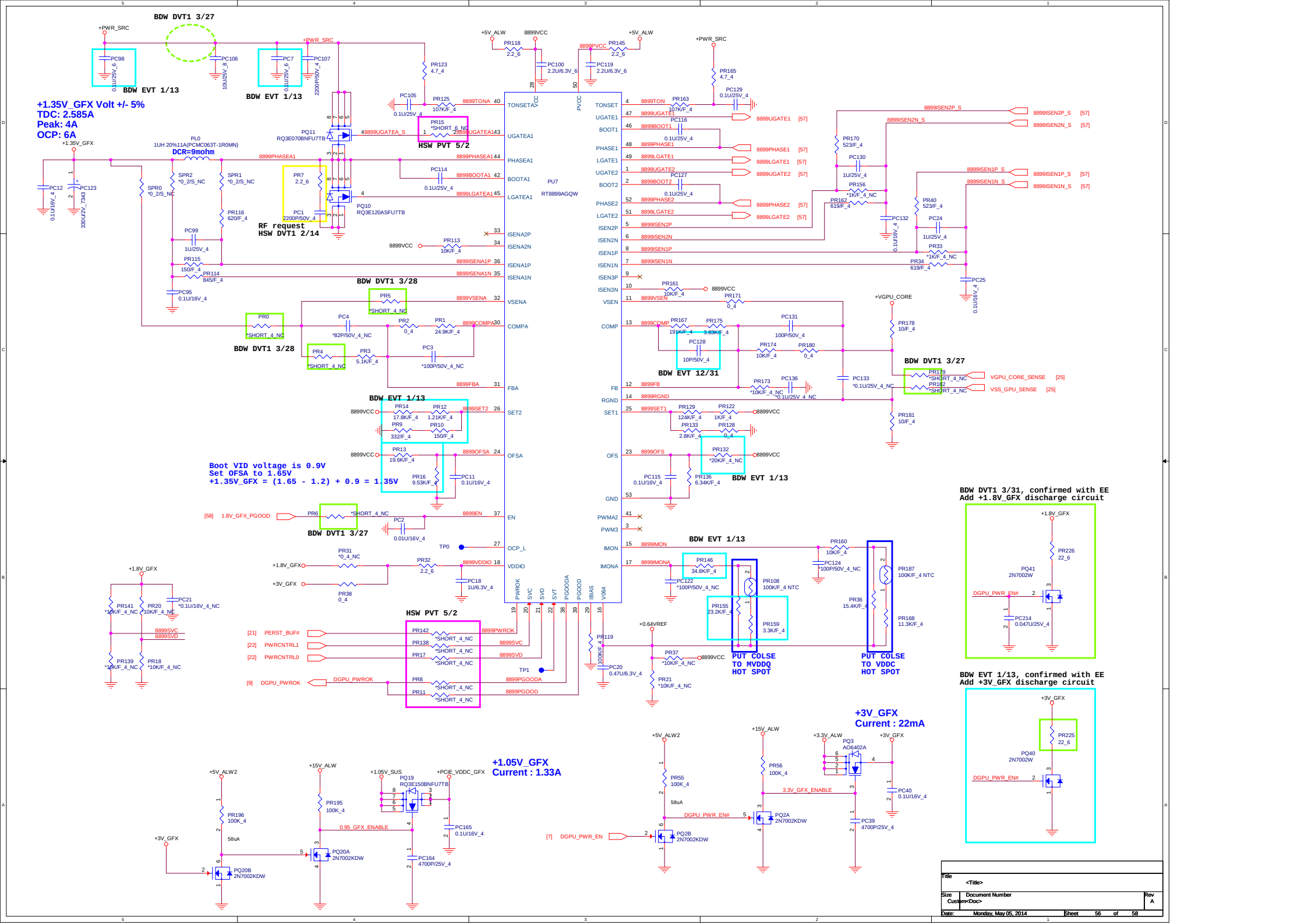
BDW DVT1 3/27
BDW EVT 1/13
+1.35V_GFX Volt +/- 5%
TDC: 2.585A
Peak: 4A
OCP: 6A
DCR=9mohm
RF request
HSW DVT1 2/14
HSW PVT 5/2
BDW DVT1 3/28
BDW EVT 12/31
Boot VID voltage is 0.9V
Set OFSA to 1.65V
+1.35V_GFX = (1.65 - 1.2) + 0.9 = 1.35V
PUT COLSE TO MVDDQ HOT SPOT
PUT COLSE TO VDDC HOT SPOT
BDW DVT1 3/31, confirmed with EE
Add +1.8V_GFX discharge circuit
BDW EVT 1/13, confirmed with EE
Add +3V_GFX discharge circuit
+3V_GFX Current : 22mA
+1.05V_GFX Current : 1.33A
Title
<Title>
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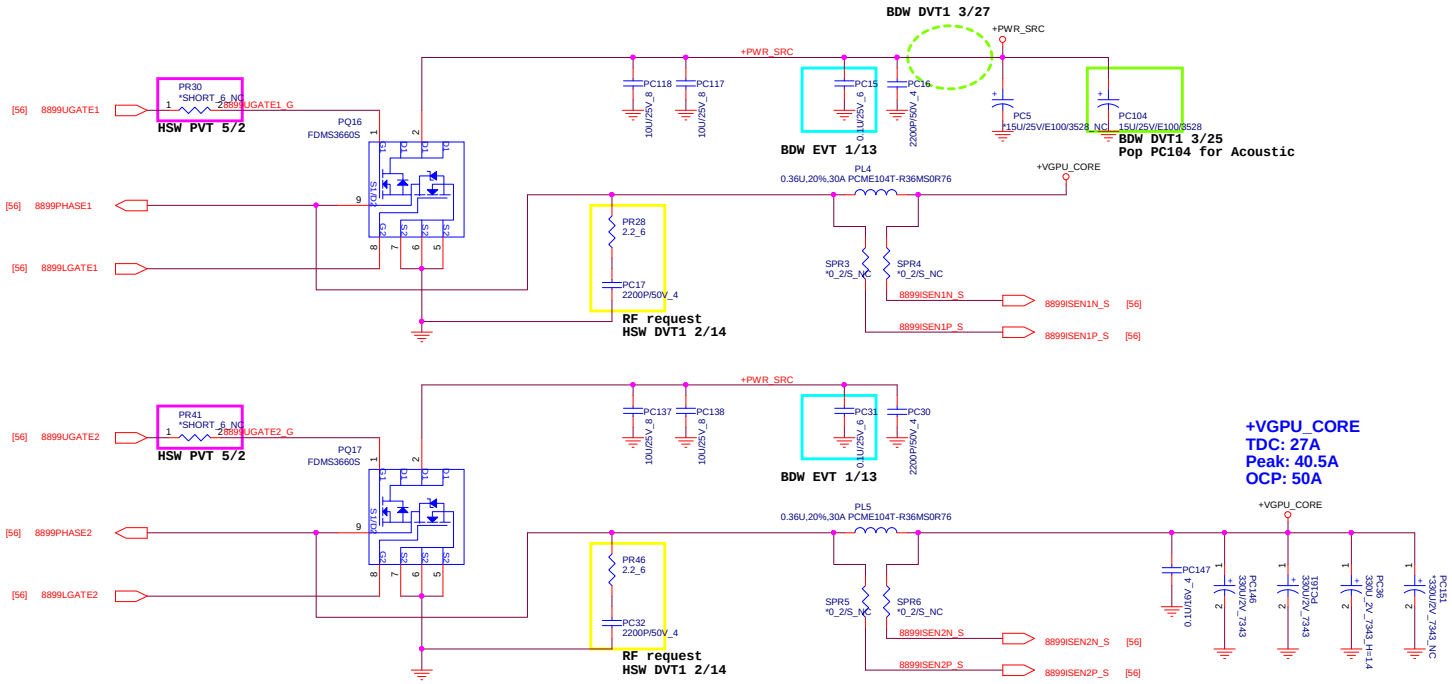

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Size	Document Number	Rev
Custom	<Doc>	A
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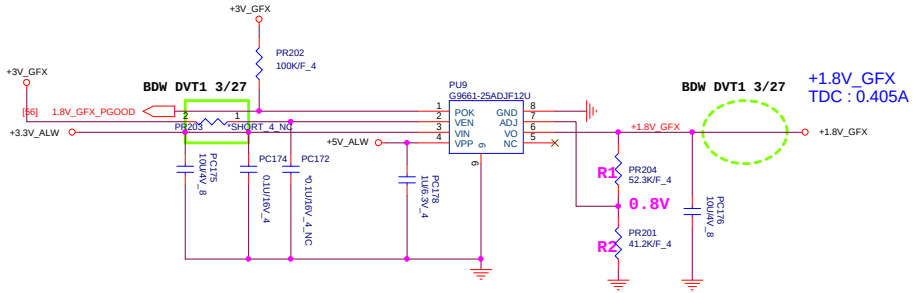

Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: A
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