HuaQin Confidential

NB2950_MB&DB Schematics Document

Intel JSL Lake-Processor with LPDDR4x MD

REV1.0

2020-0622

Author	
Reviewer	
Approver	

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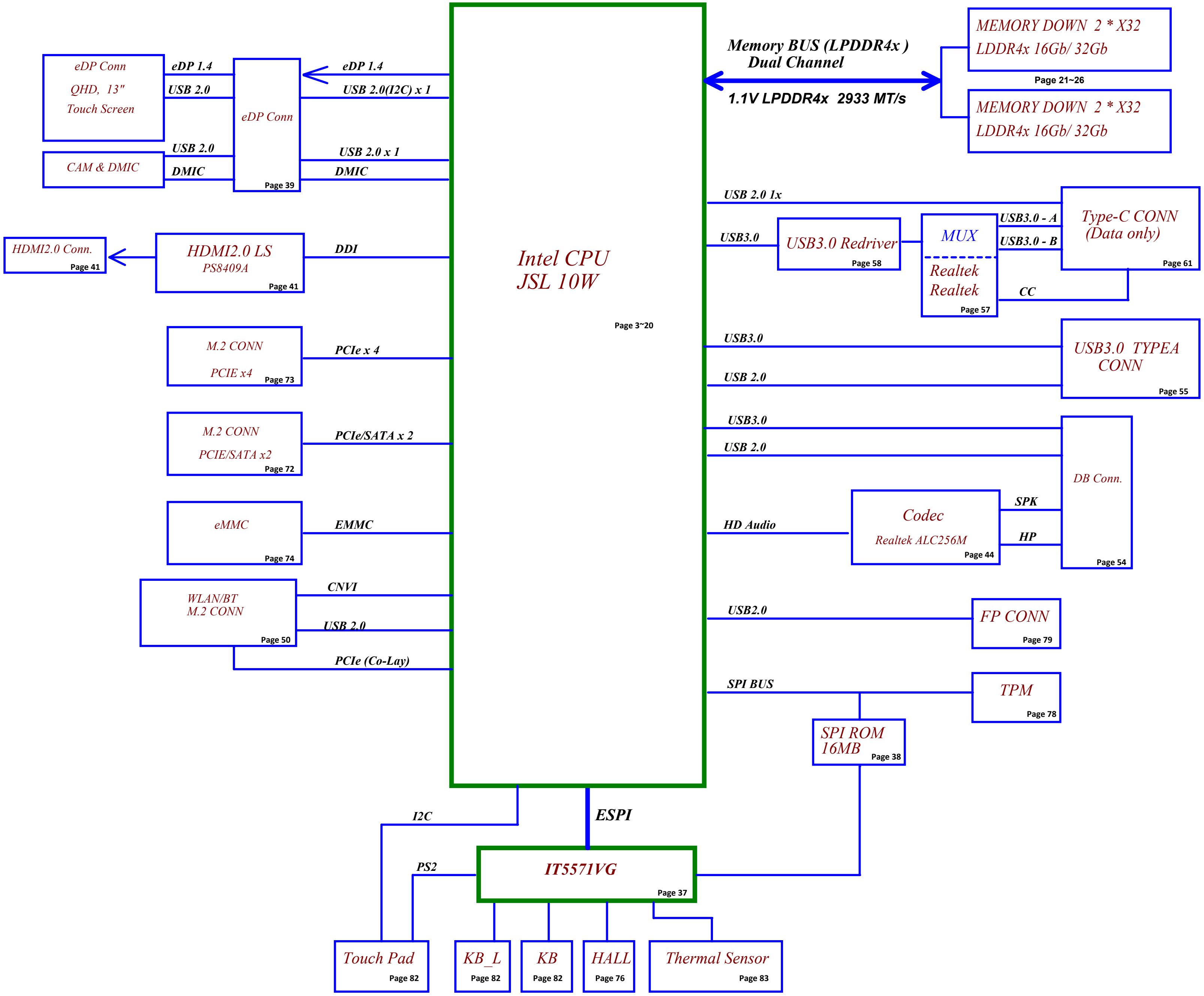

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Page name: **Block Diagram**

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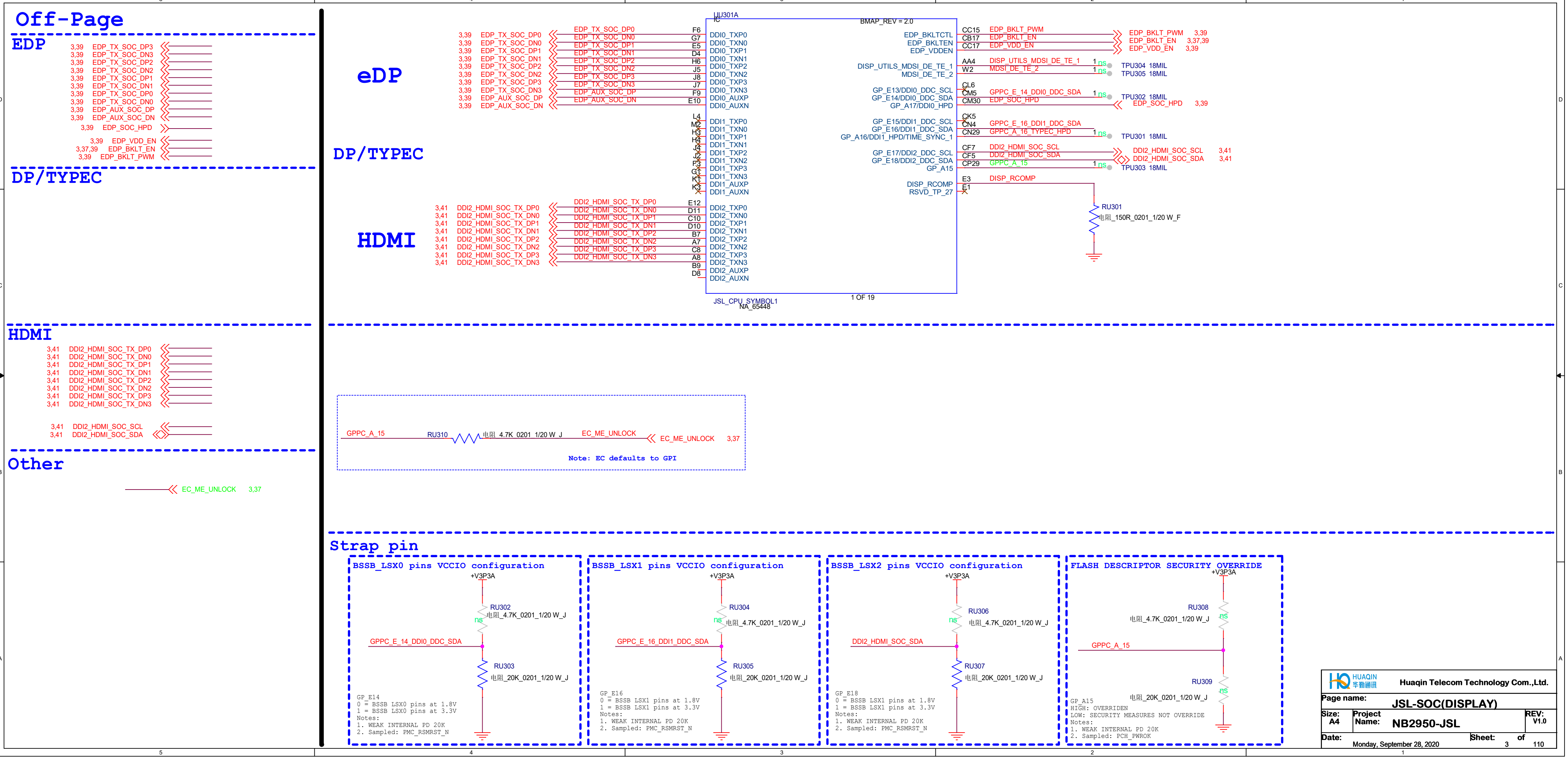

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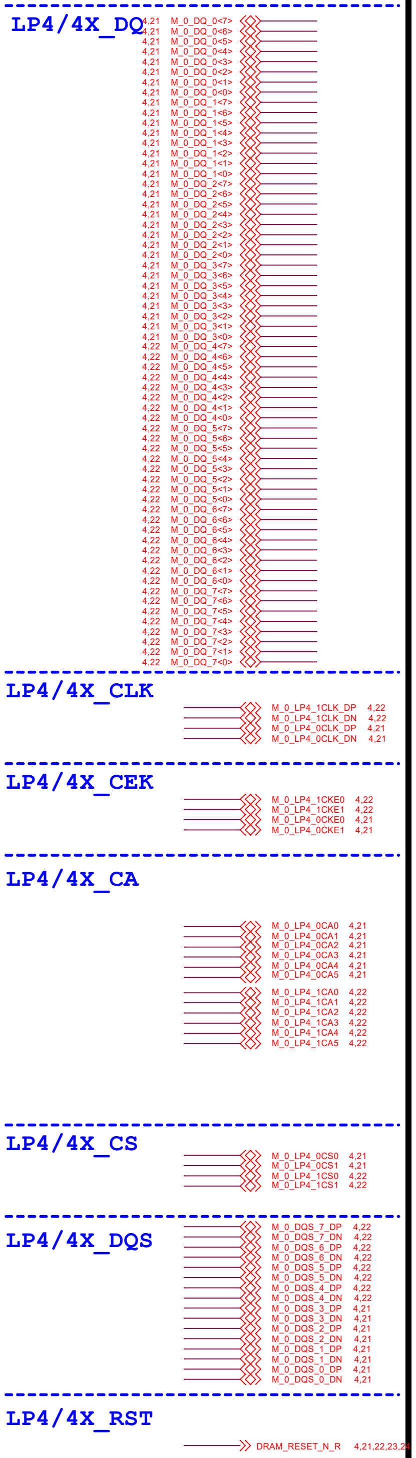
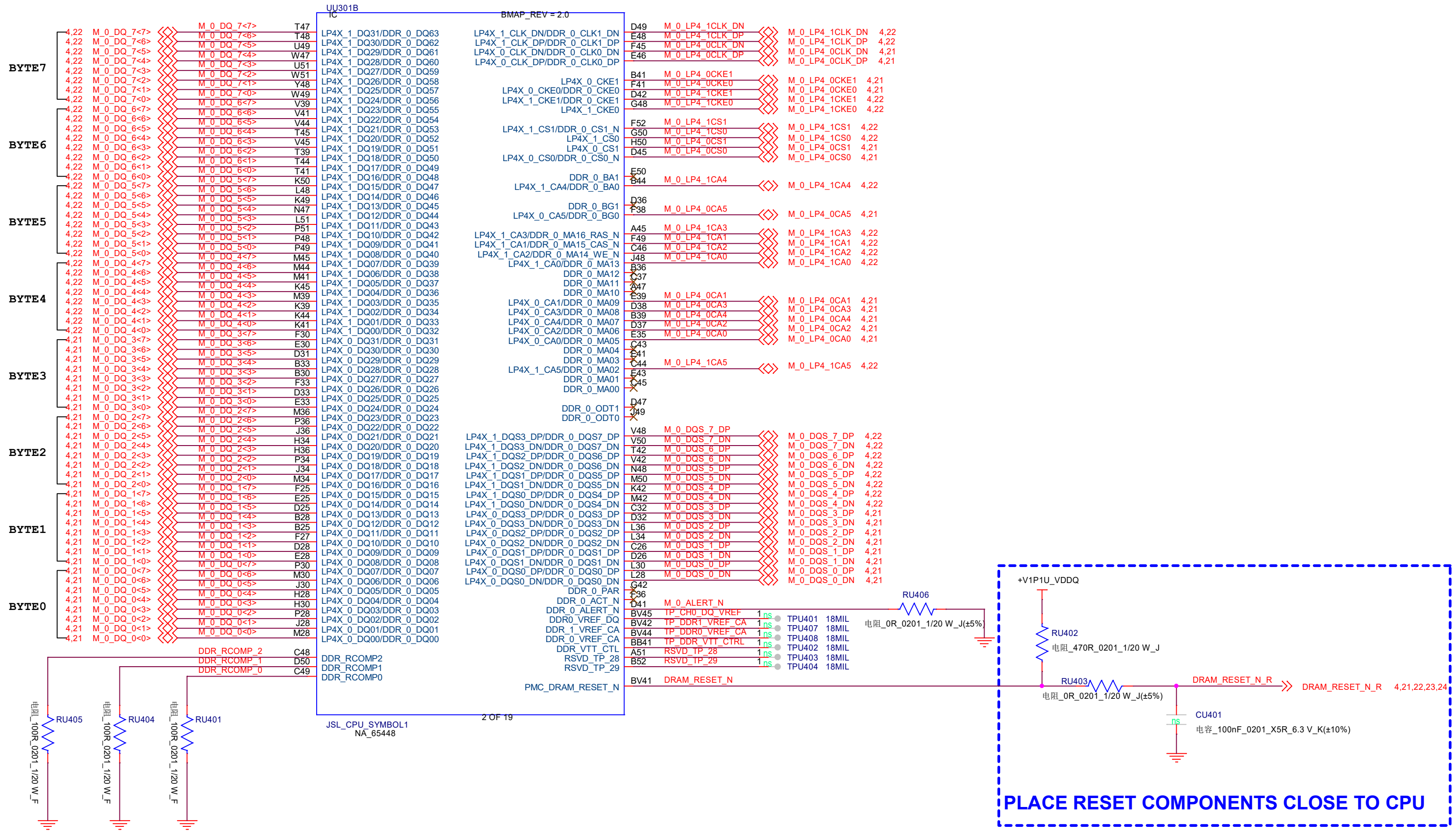


SOC_LP4/4X_CHA

DDR = LPDDR4/4X



PLACE RESET COMPONENTS CLOSE TO CPU

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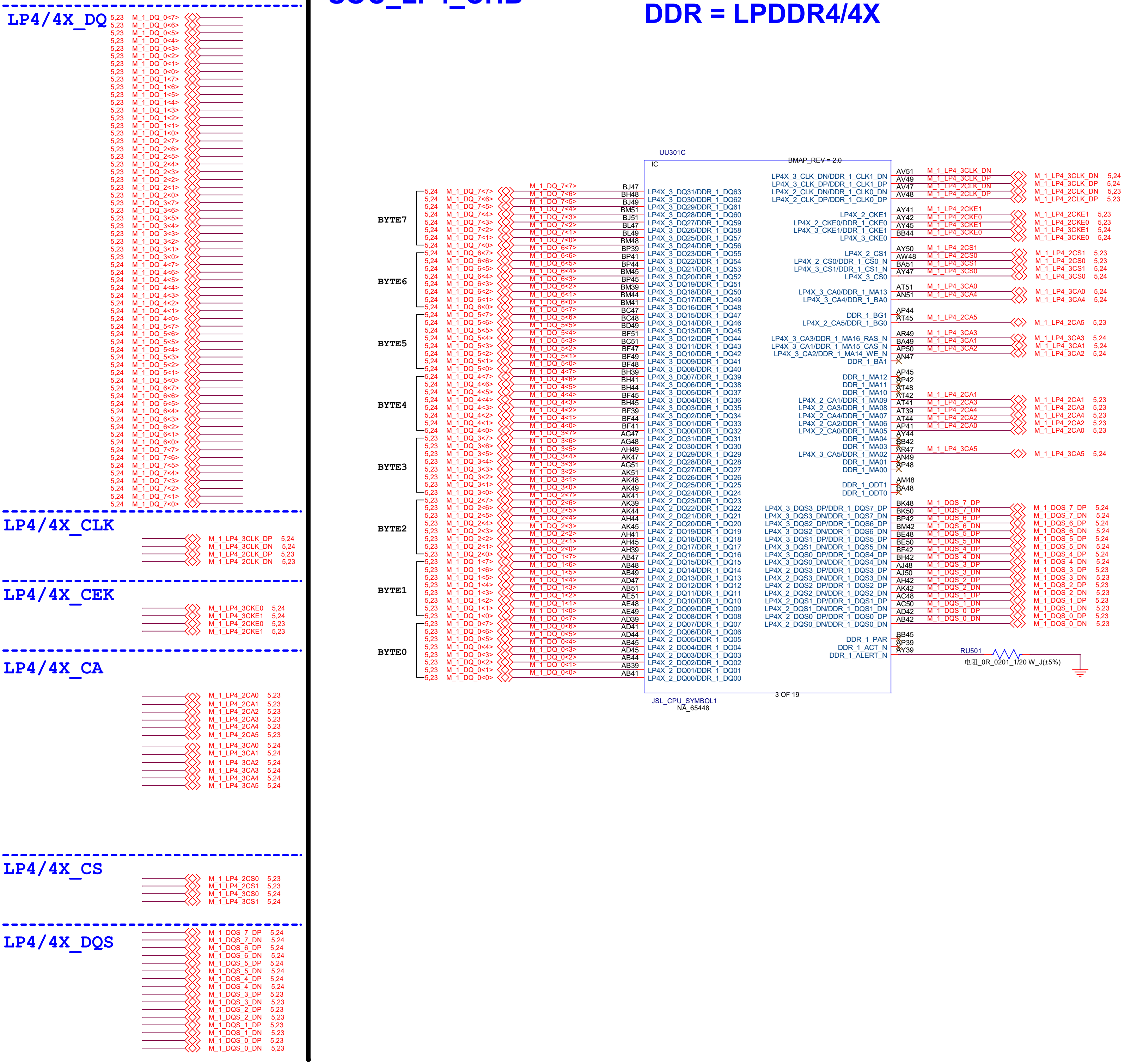
SOC_LP4_CHB

DDR = LPDDR4/4X



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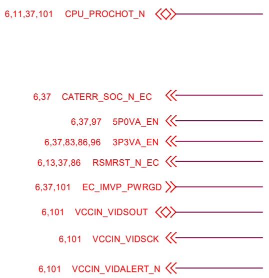

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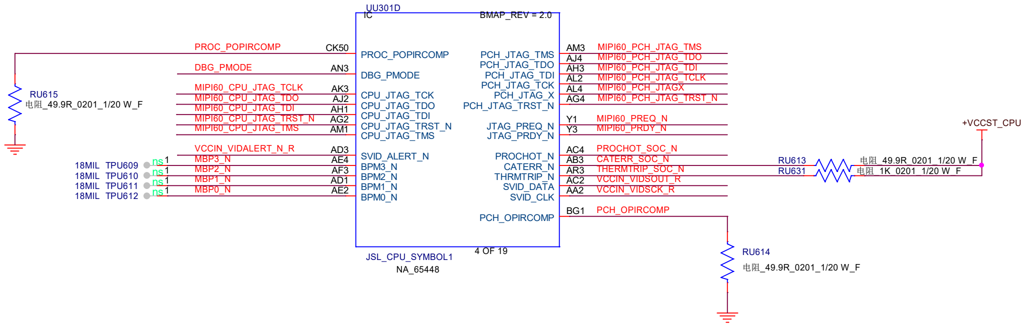
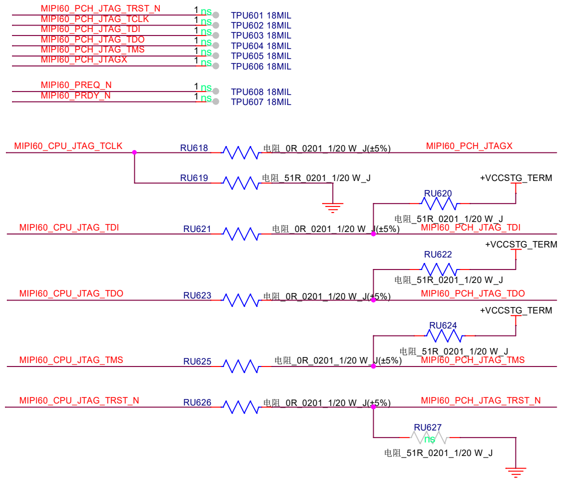
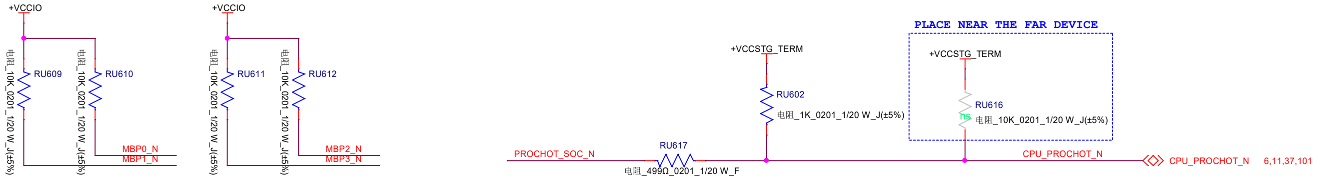


MIPI_60





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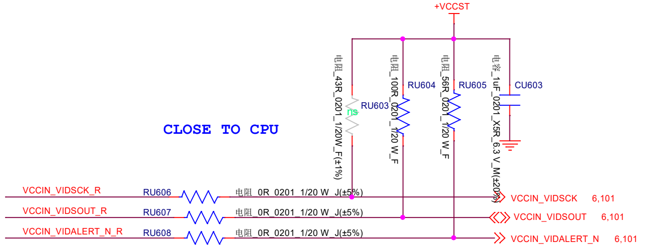

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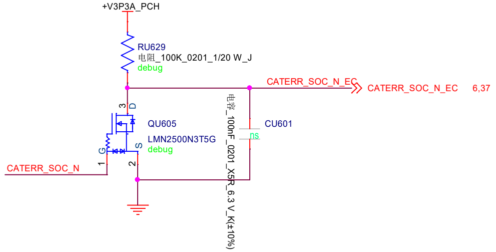

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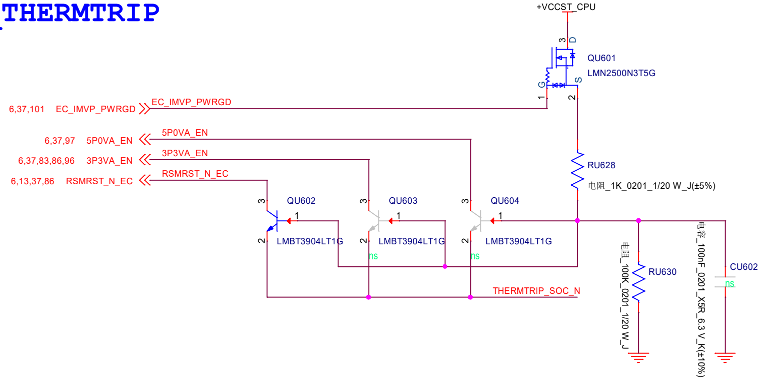

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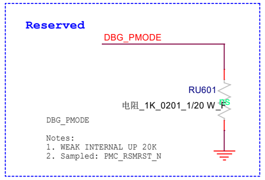

DBG_PMODE

Notes:
1. WEAK INTERNAL UP 20K
2. Sampled: PMC_RSMRST_N

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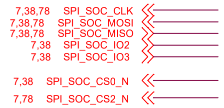
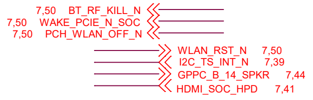
SPI



ESPI

Other



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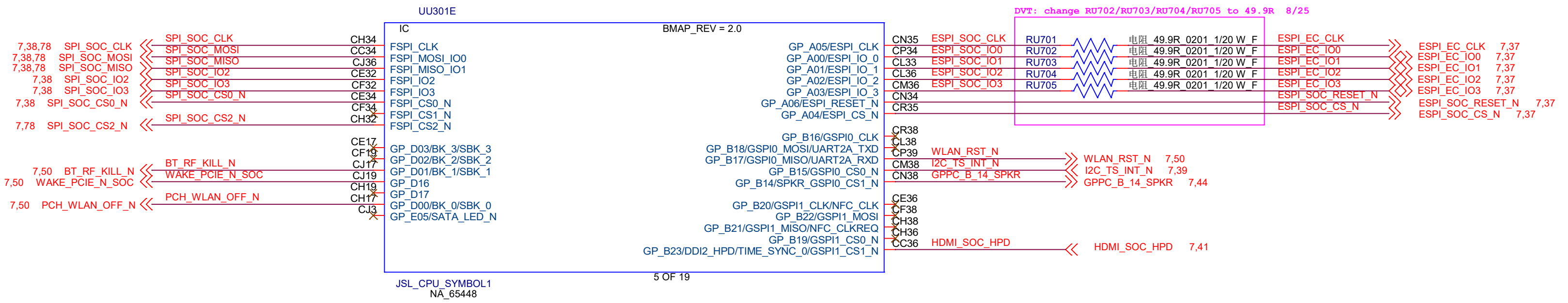

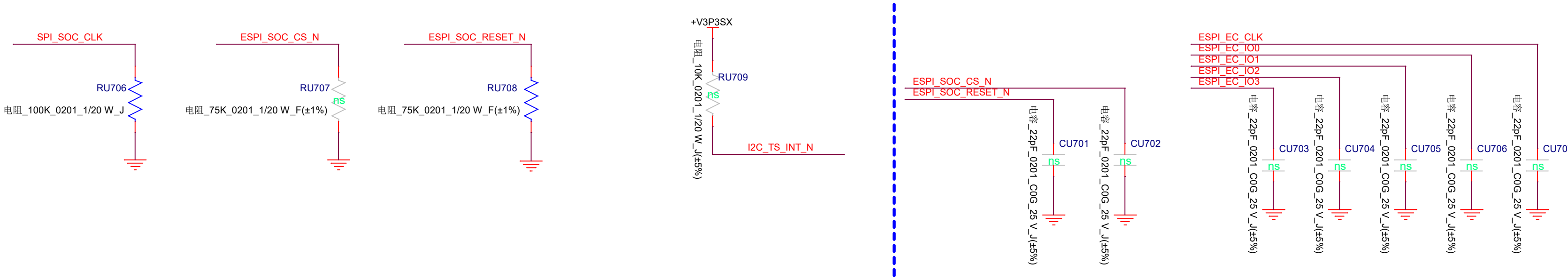

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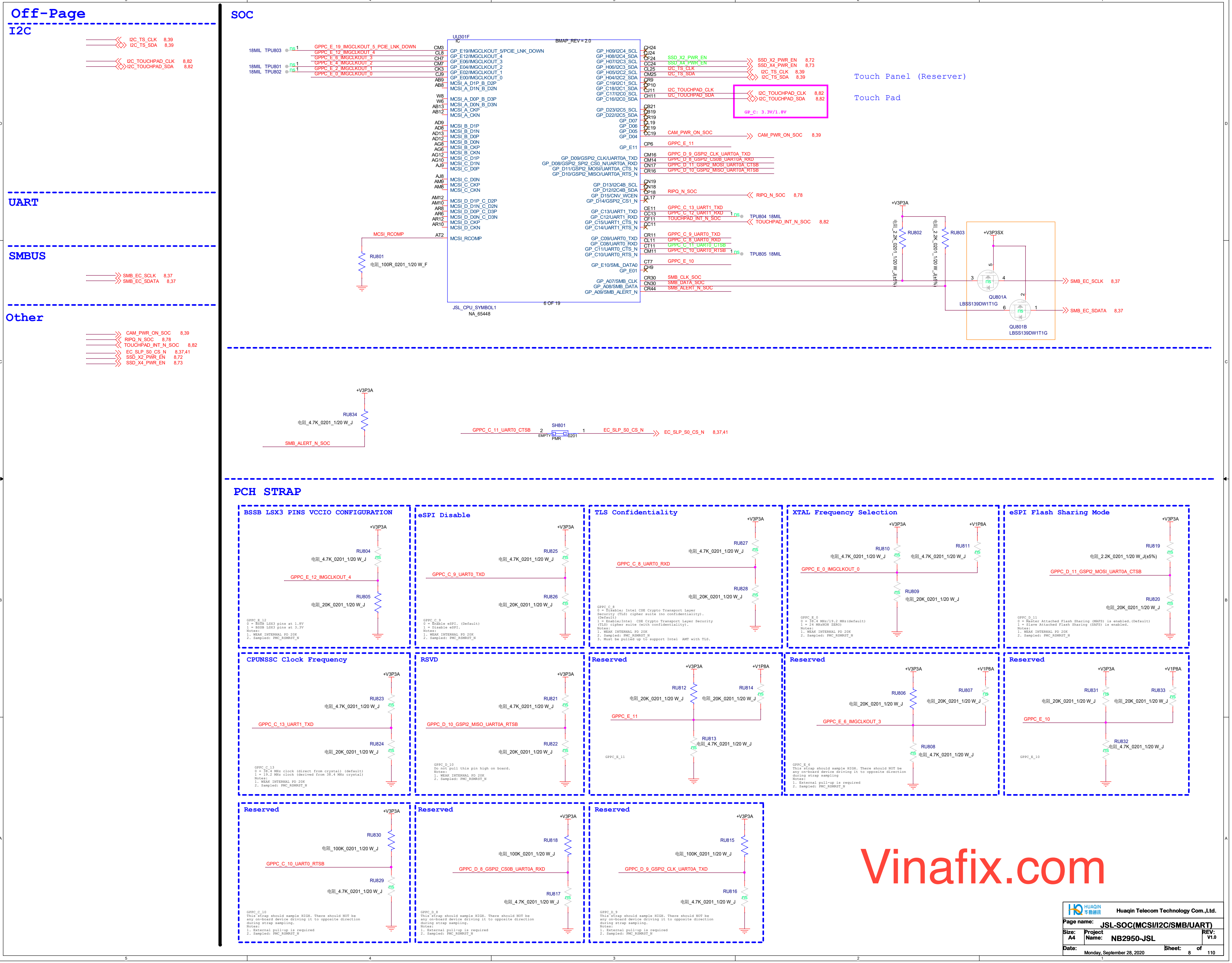

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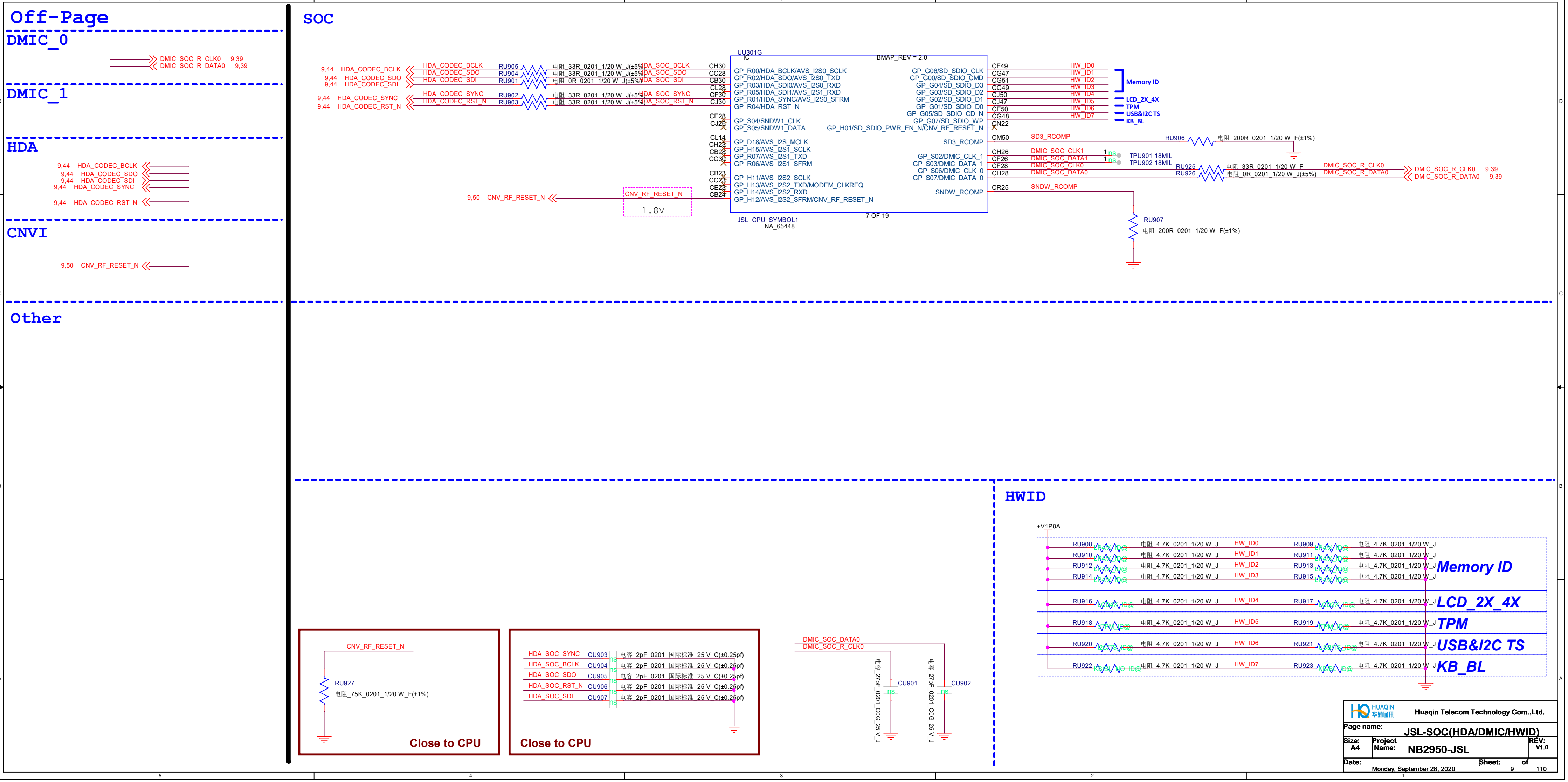

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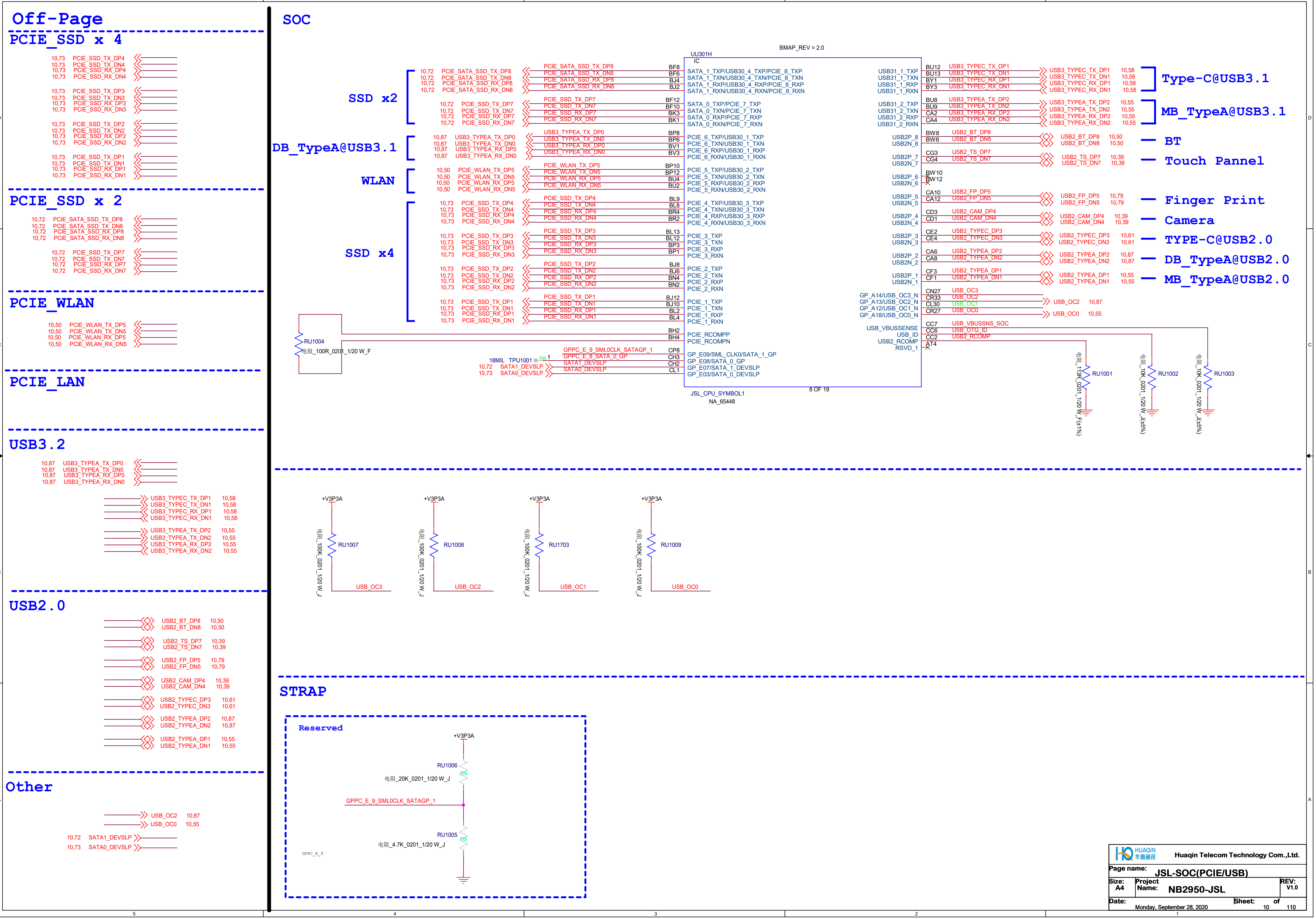

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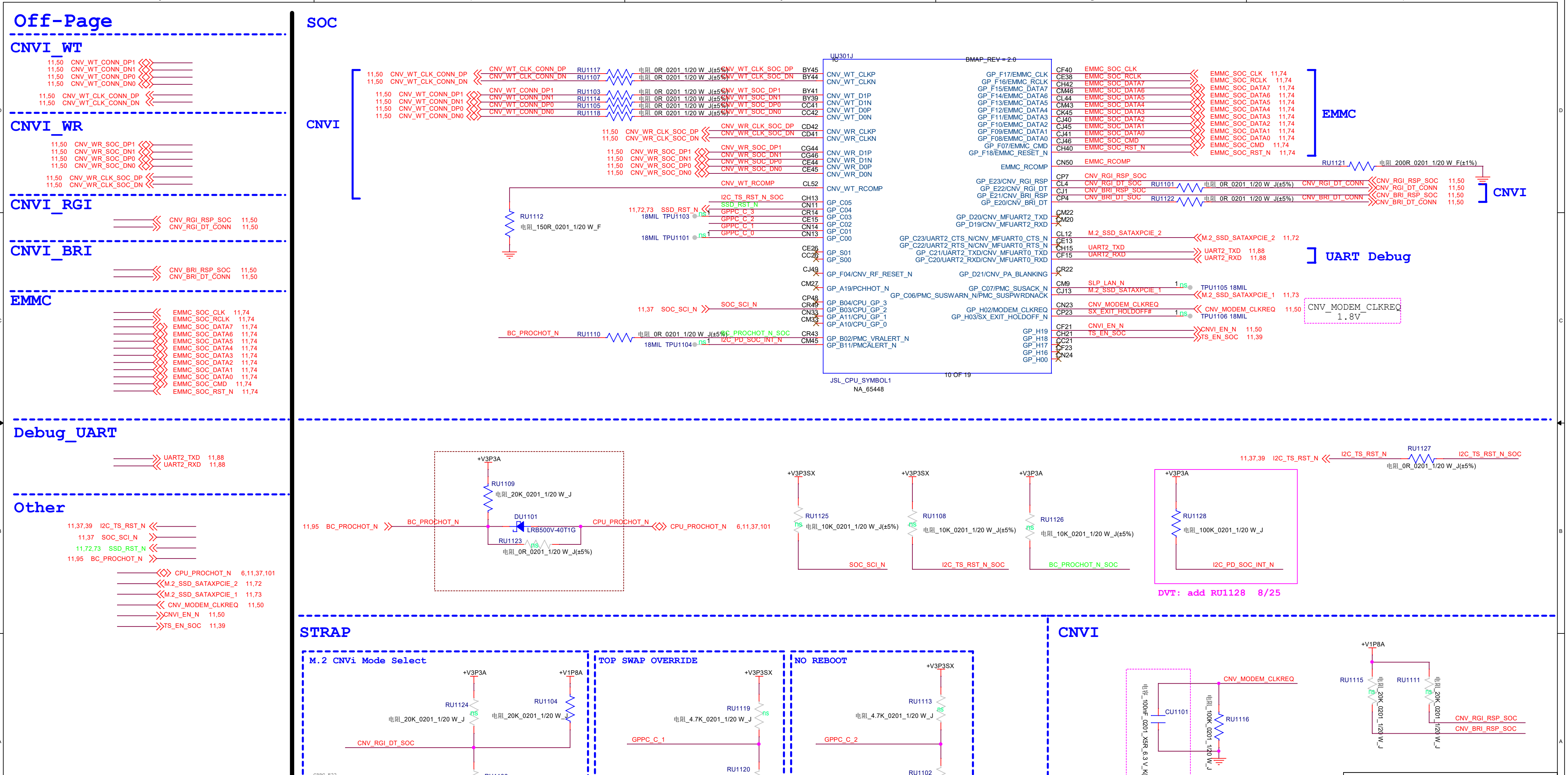

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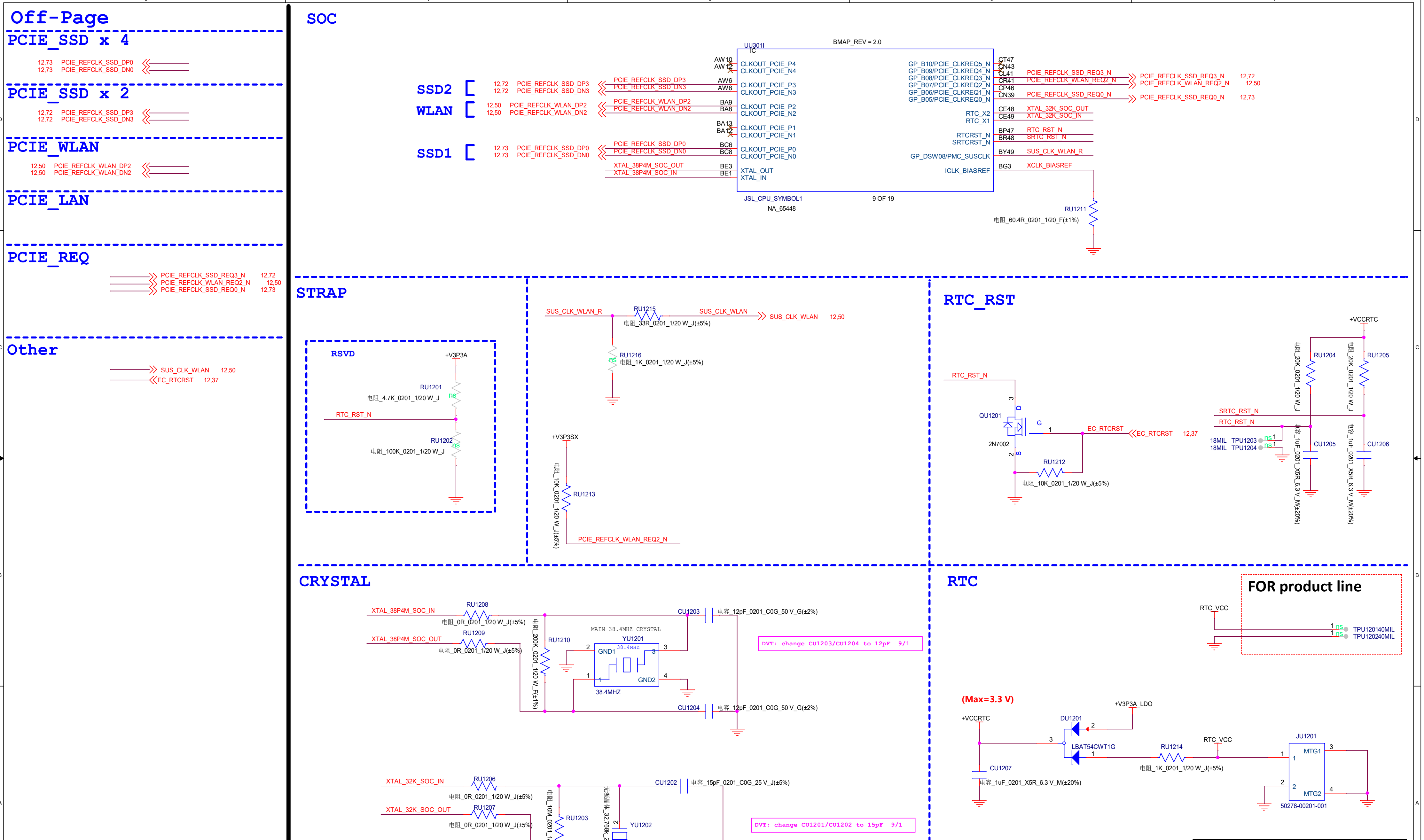

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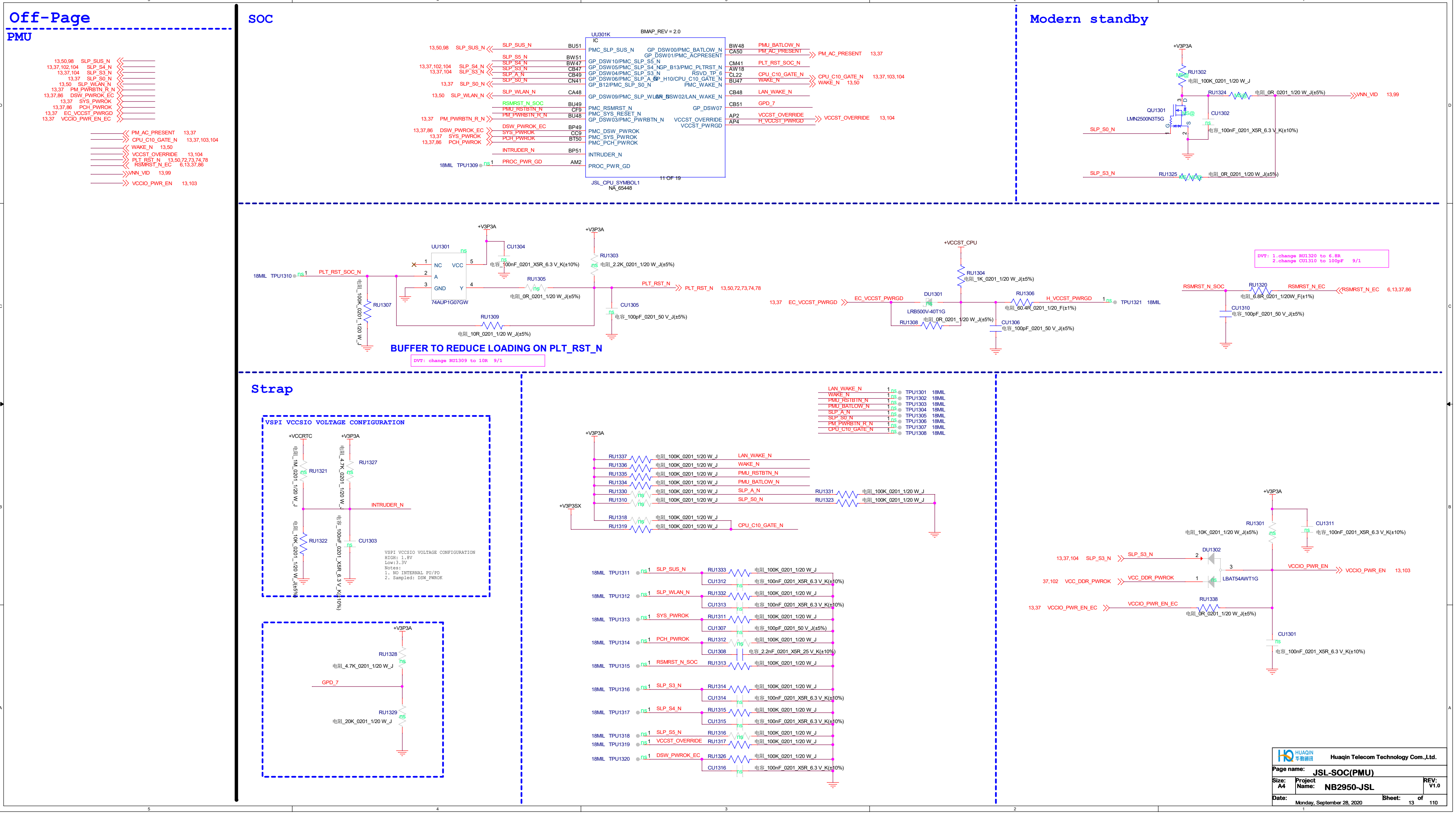

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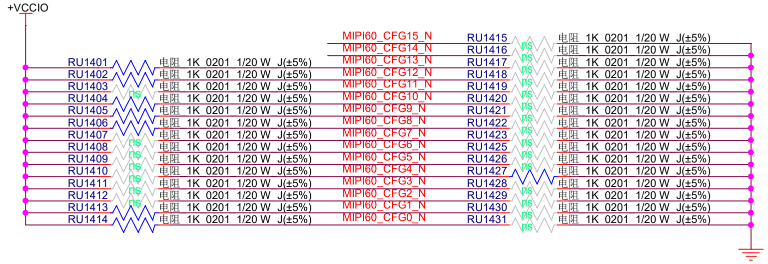
RESERVED SIGNALS

CFG Signals Functionality and Termination



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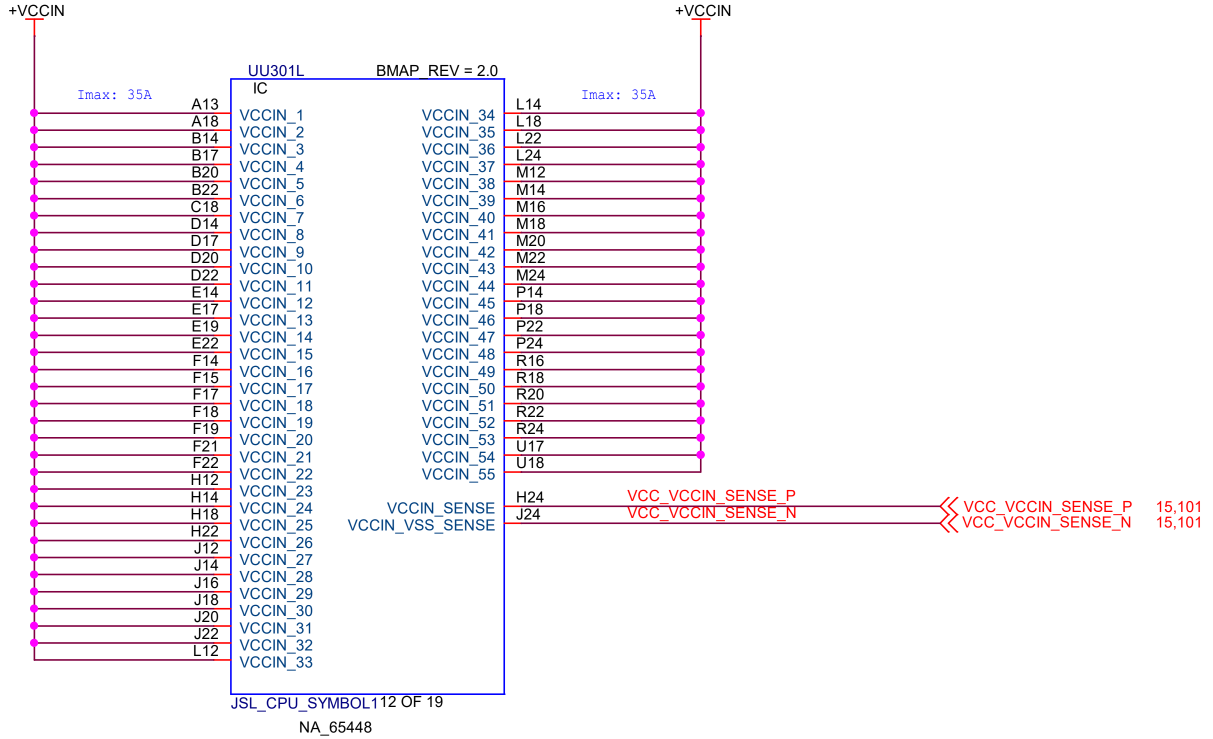
VCCIN_SENSE

CPU POWER



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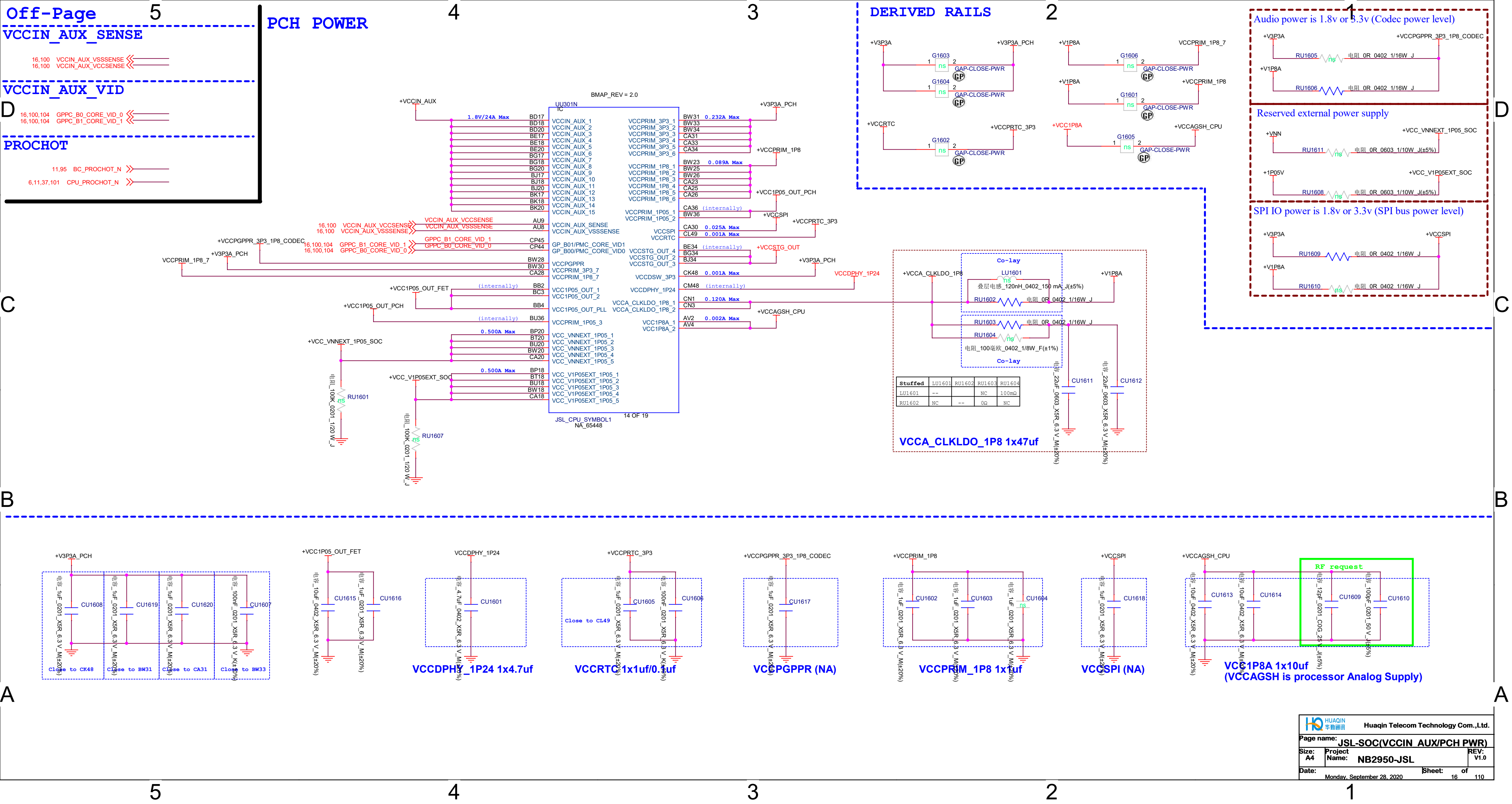

Stuffed	LU1601	RU1602	RU1603	RU1604
LU1601	--		NC	100mΩ
RU1602	NC	--	0Ω	NC

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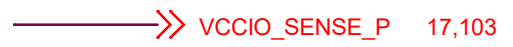
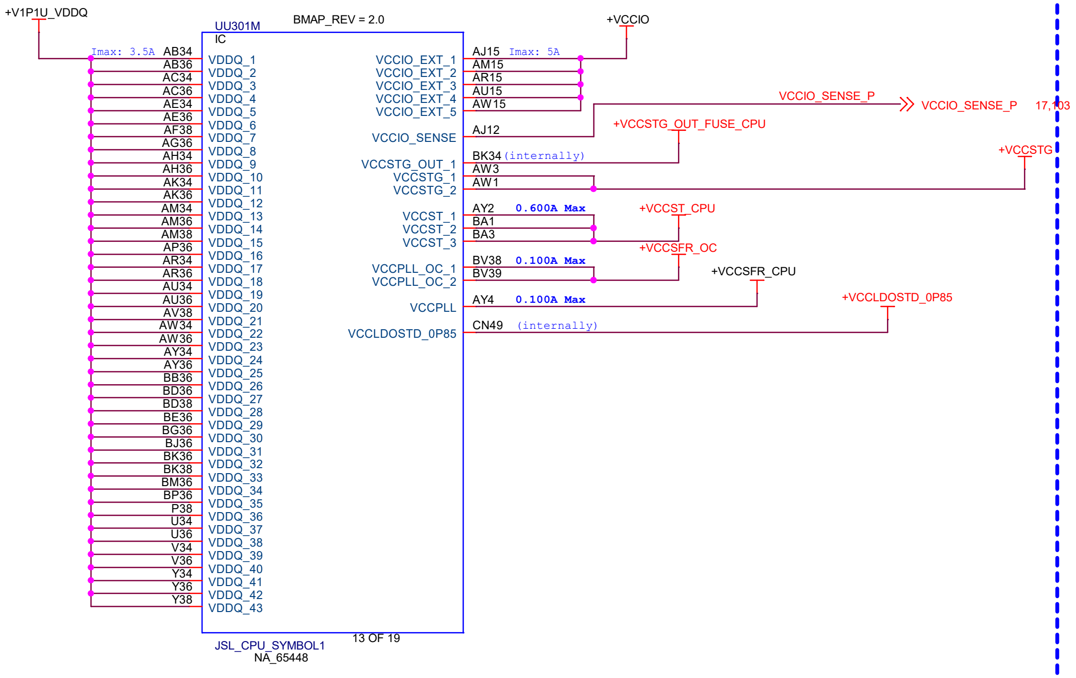
VCCIO_SENSE



CPU POWER



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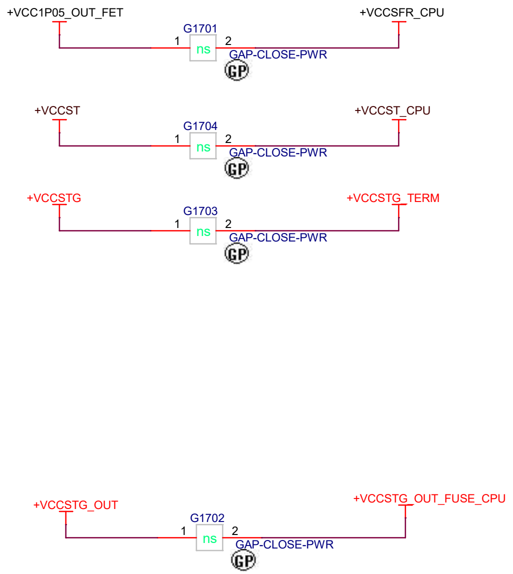

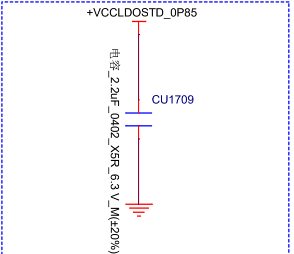

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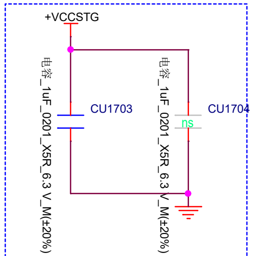
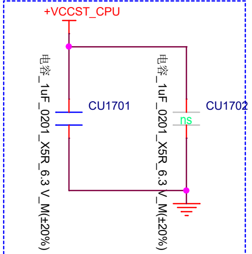


VCCSTG 1x1uf



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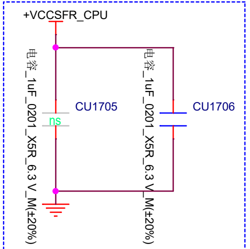

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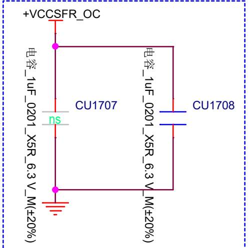

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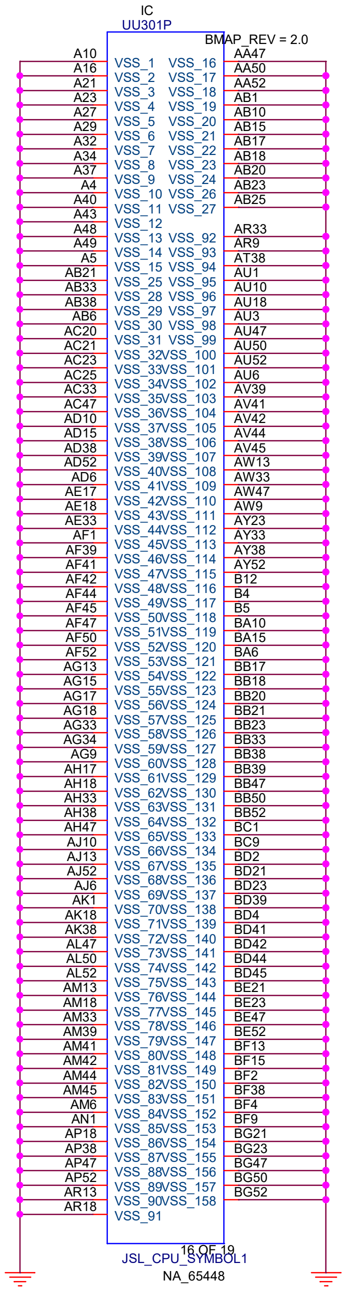

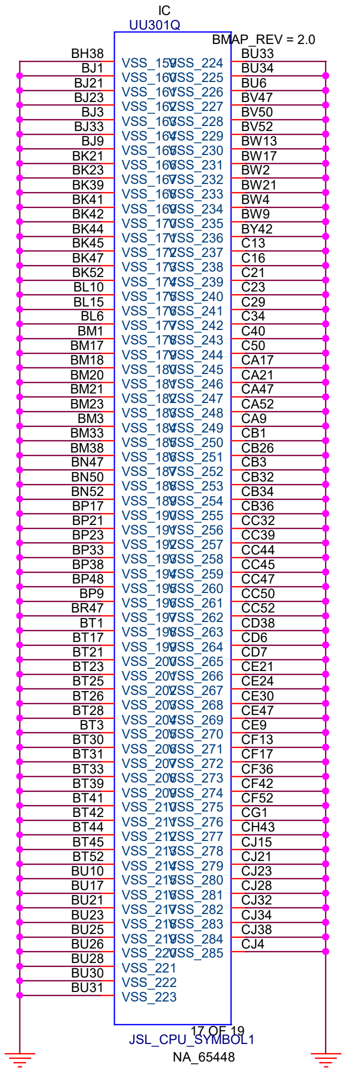

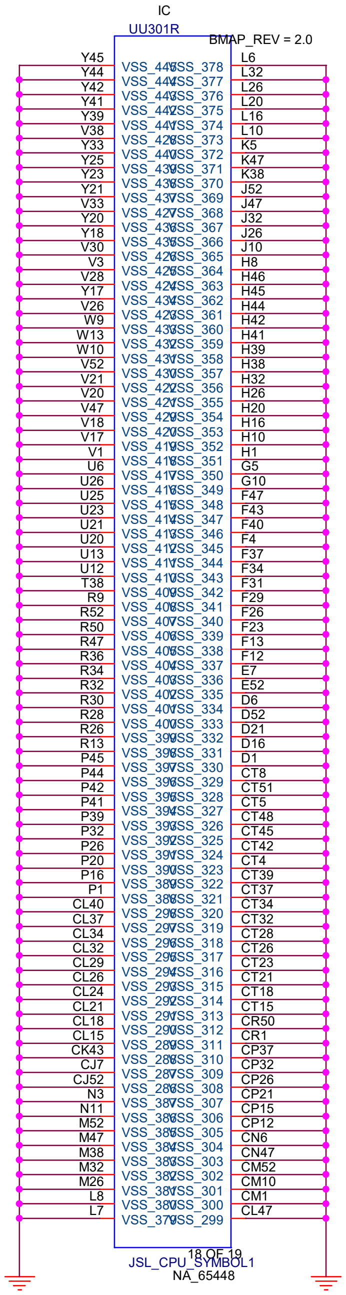

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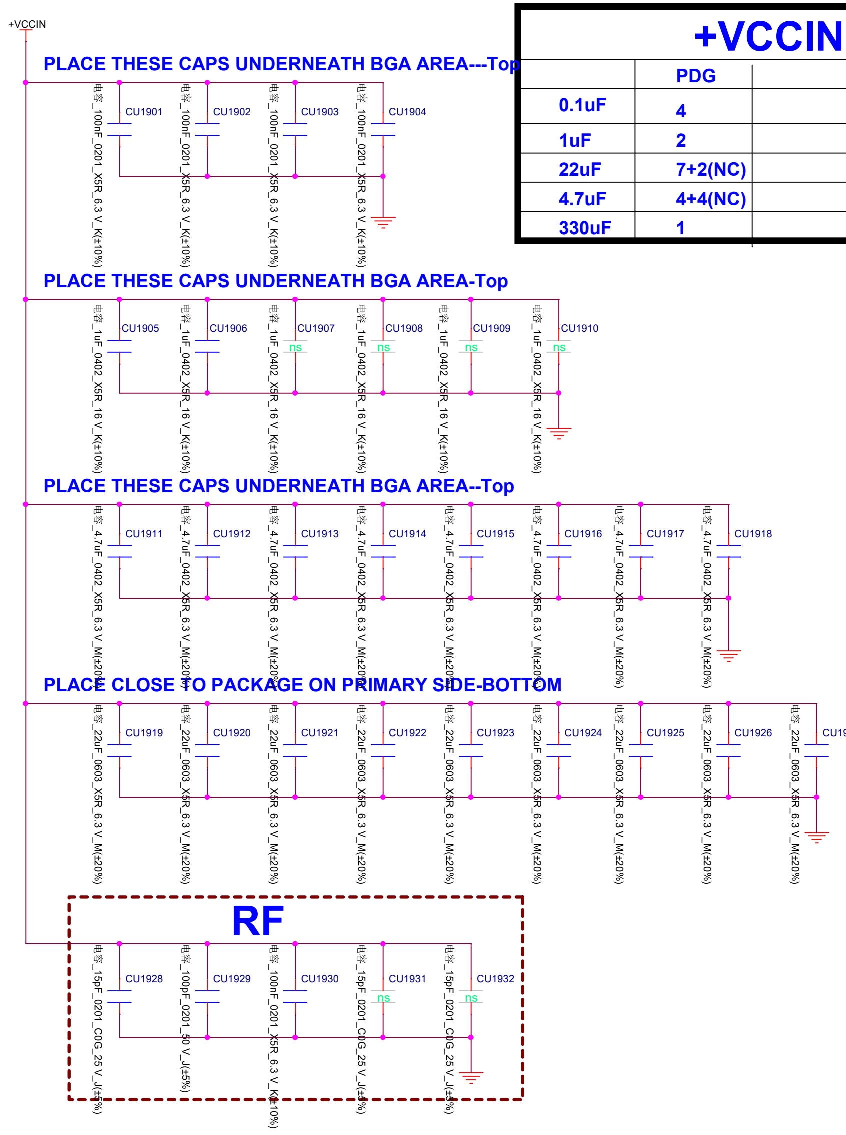
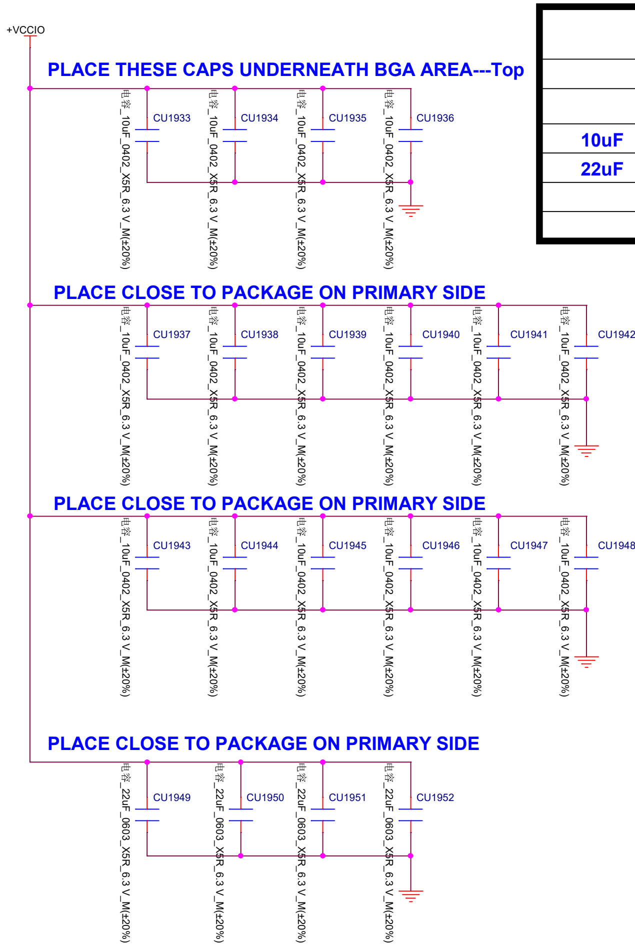


+VCCIN

	PDG		S1
0.1uF	4		4
1uF	2		2
22uF	7+2(NC)		7+2(NC)
4.7uF	4+4(NC)		4+4(NC)
330uF	1		1



+VCCIO

	PDG		S1
10uF	12+4		16
22uF	4		4

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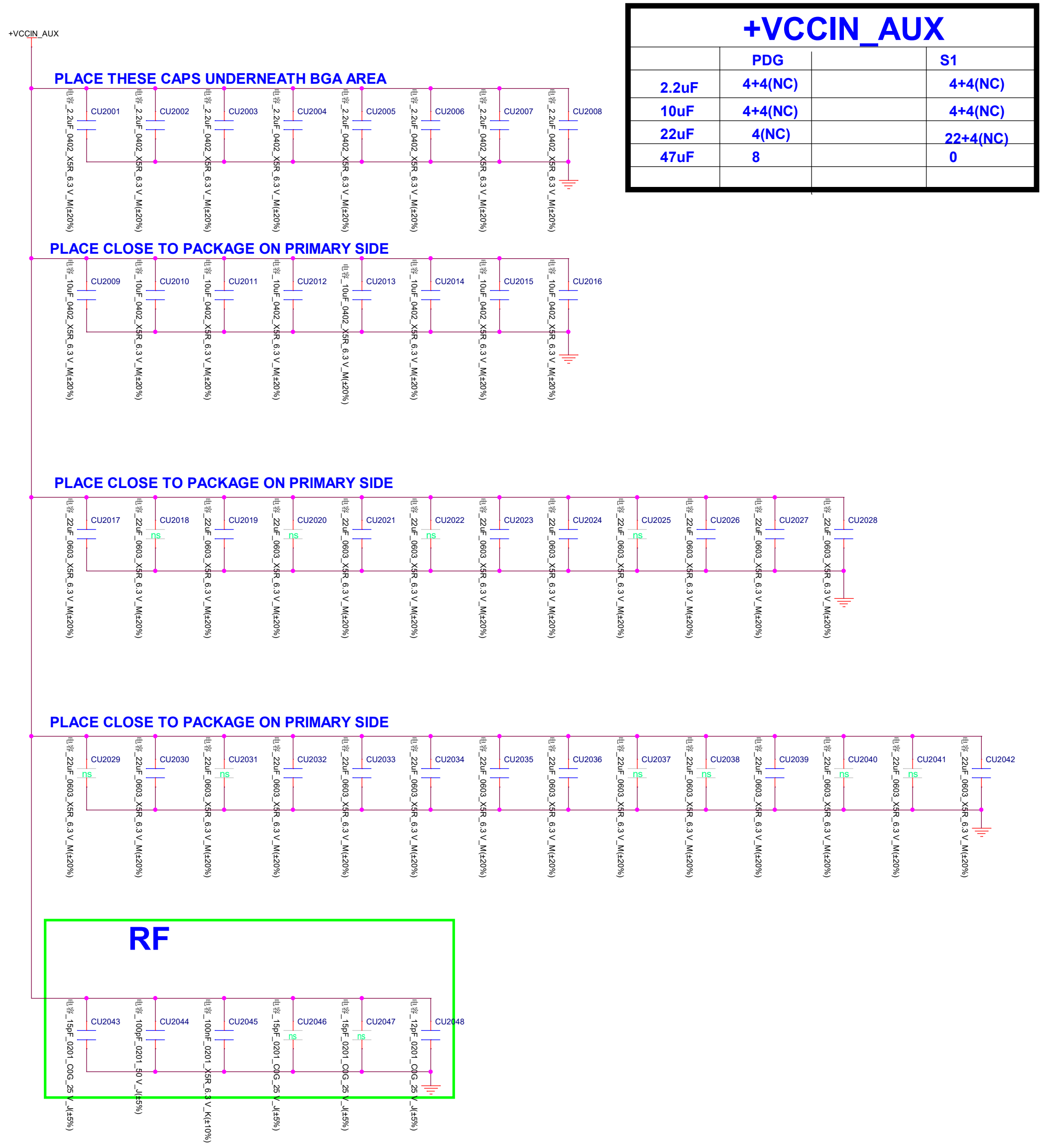
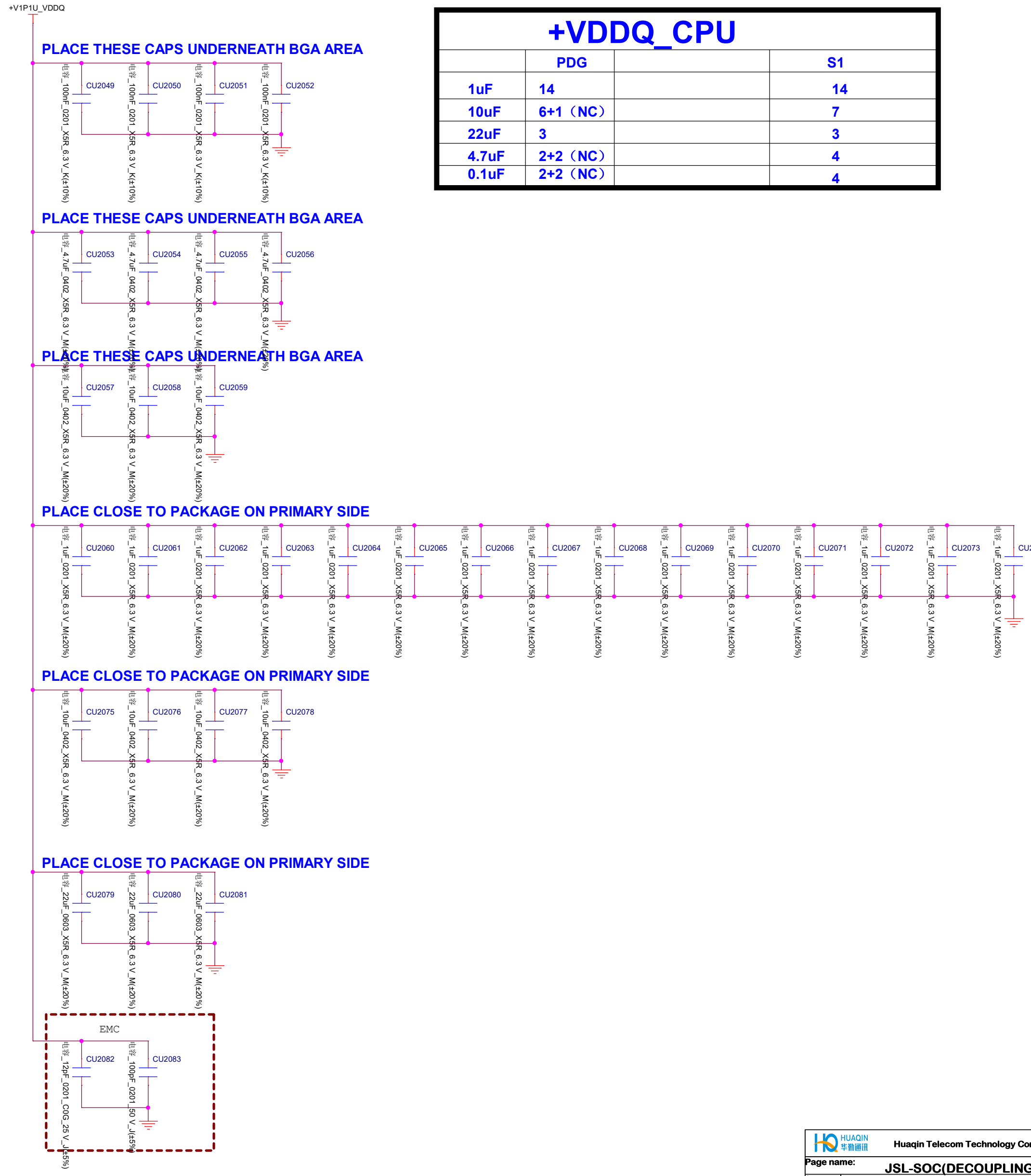


+VCCIN_AUX

	PDG		S1
2.2uF	4+4(NC)		4+4(NC)
10uF	4+4(NC)		4+4(NC)
22uF	4(NC)		22+4(NC)
47uF	8		0



+VDDQ_CPU

	PDG		S1
1uF	14		14
10uF	6+1（NC）		7
22uF	3		3
4.7uF	2+2（NC）		4
0.1uF	2+2（NC）		4

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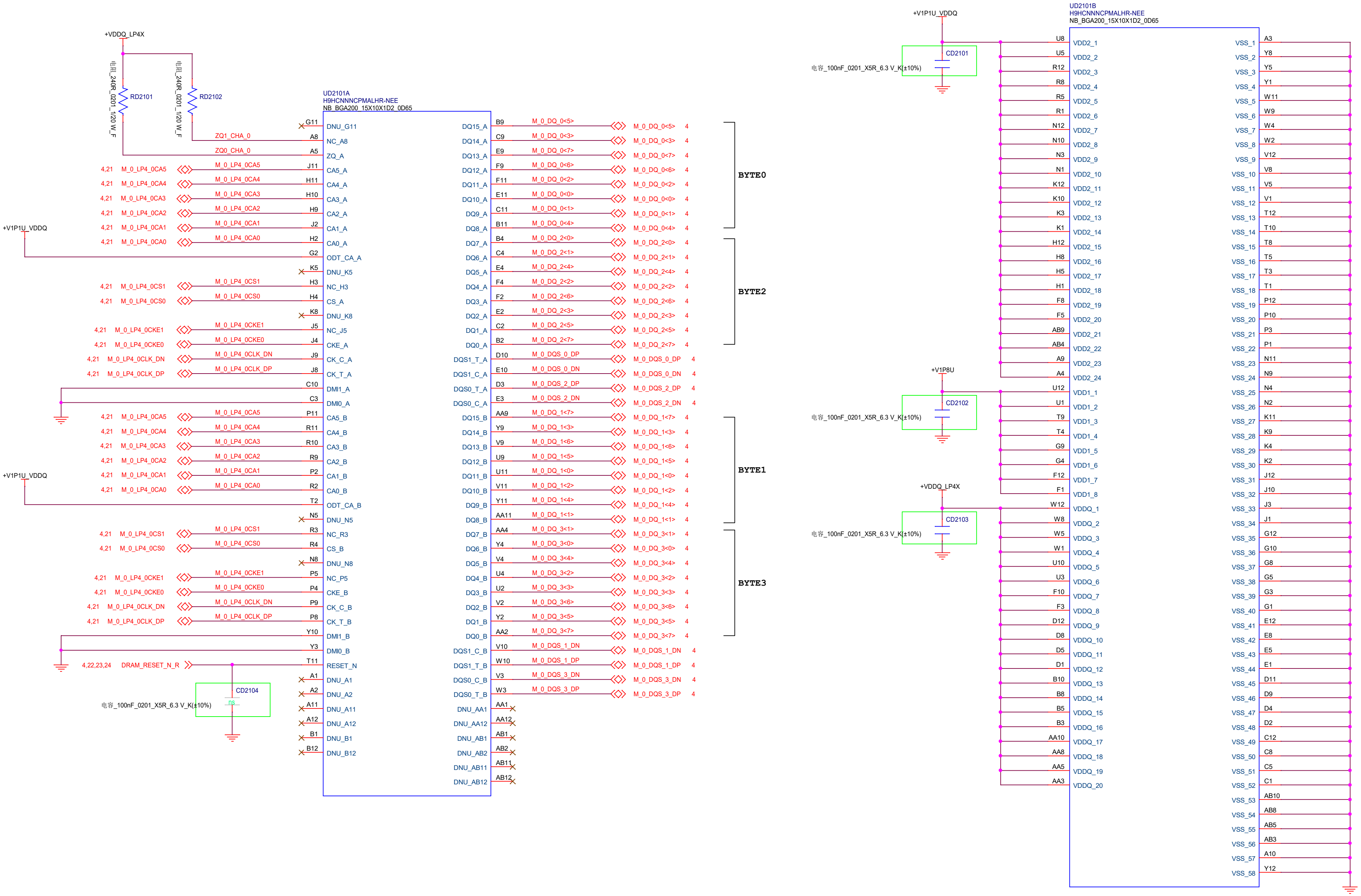
CHA-1



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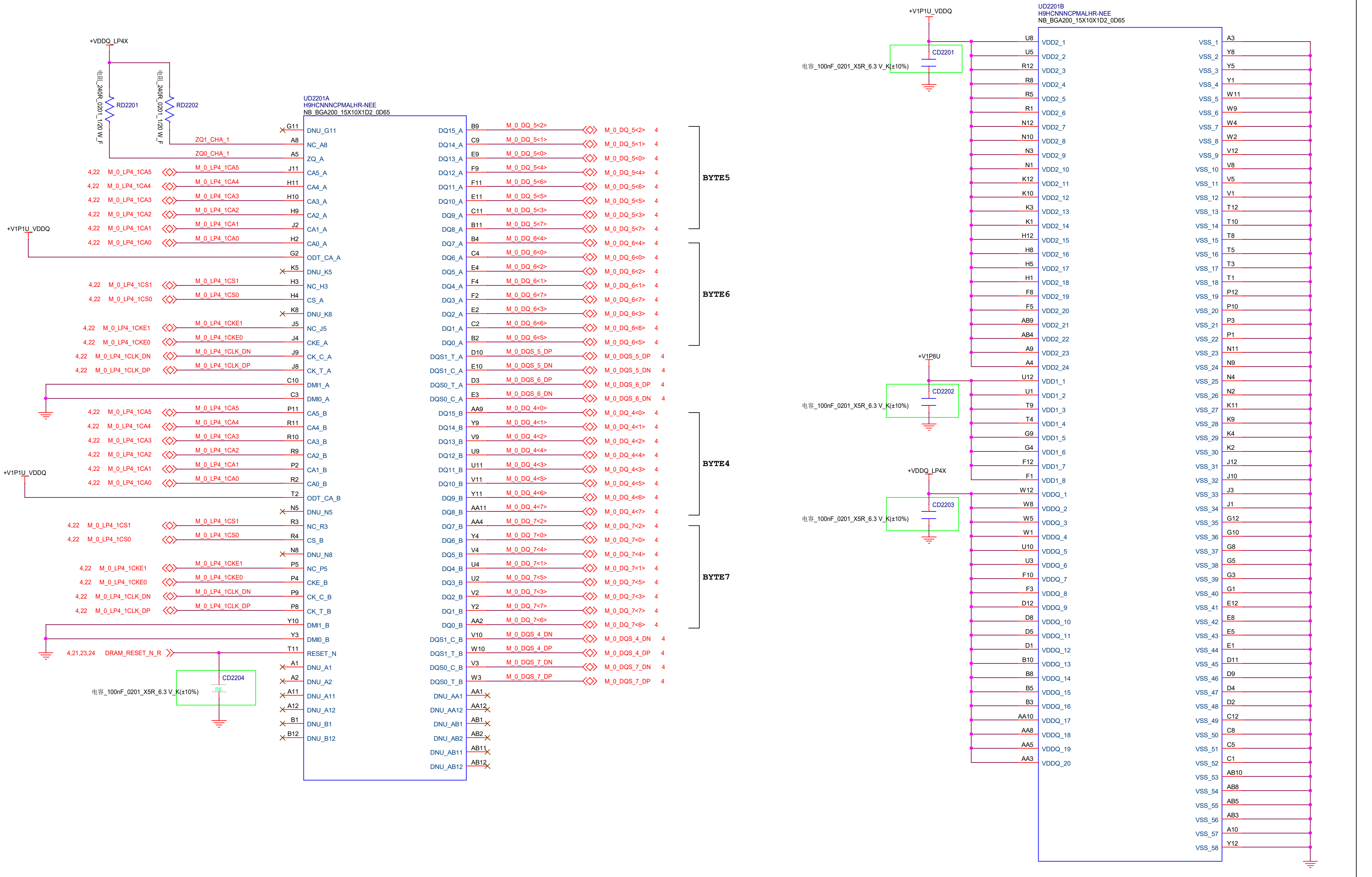
CHA-2



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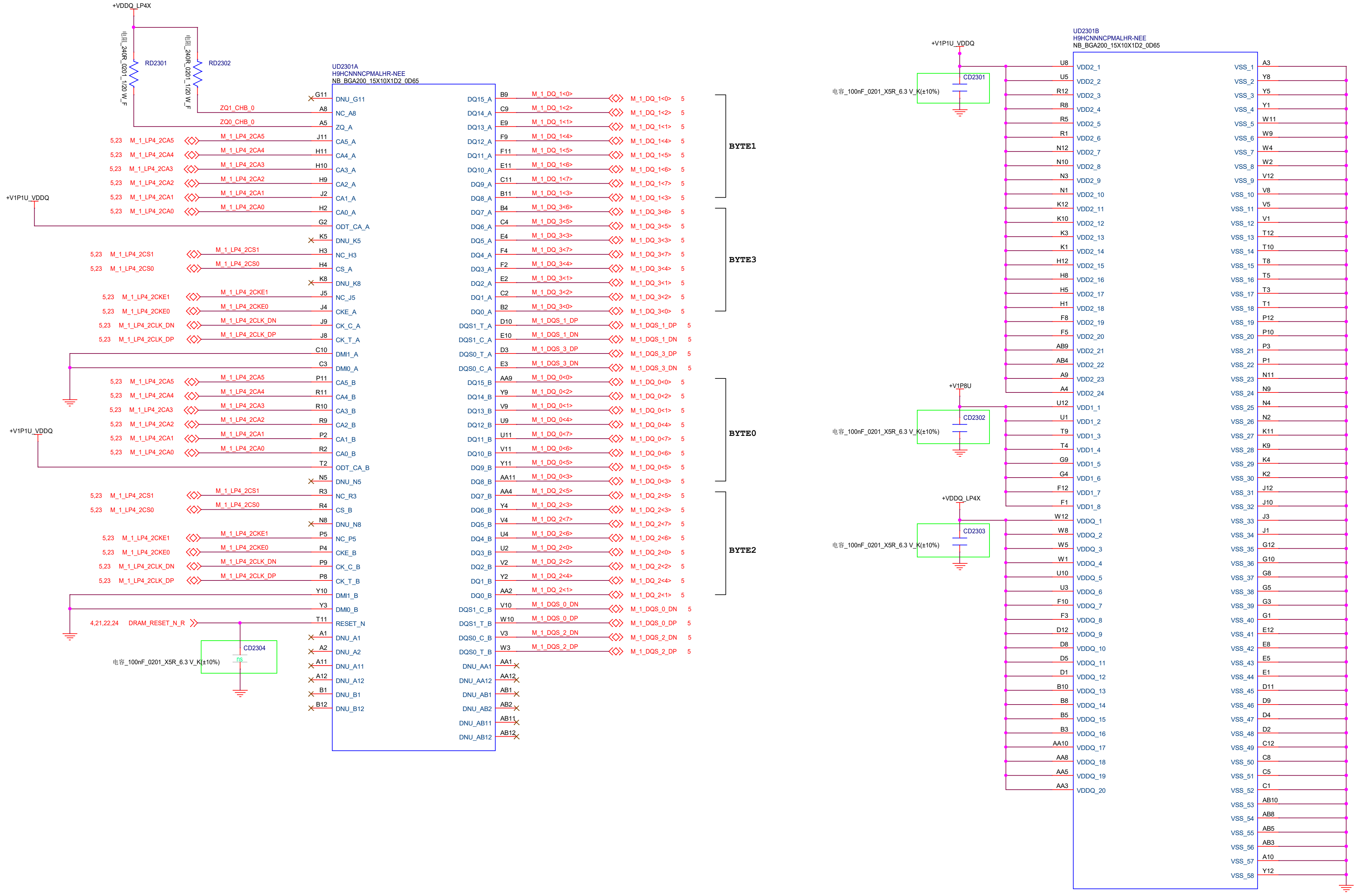
CHB-1



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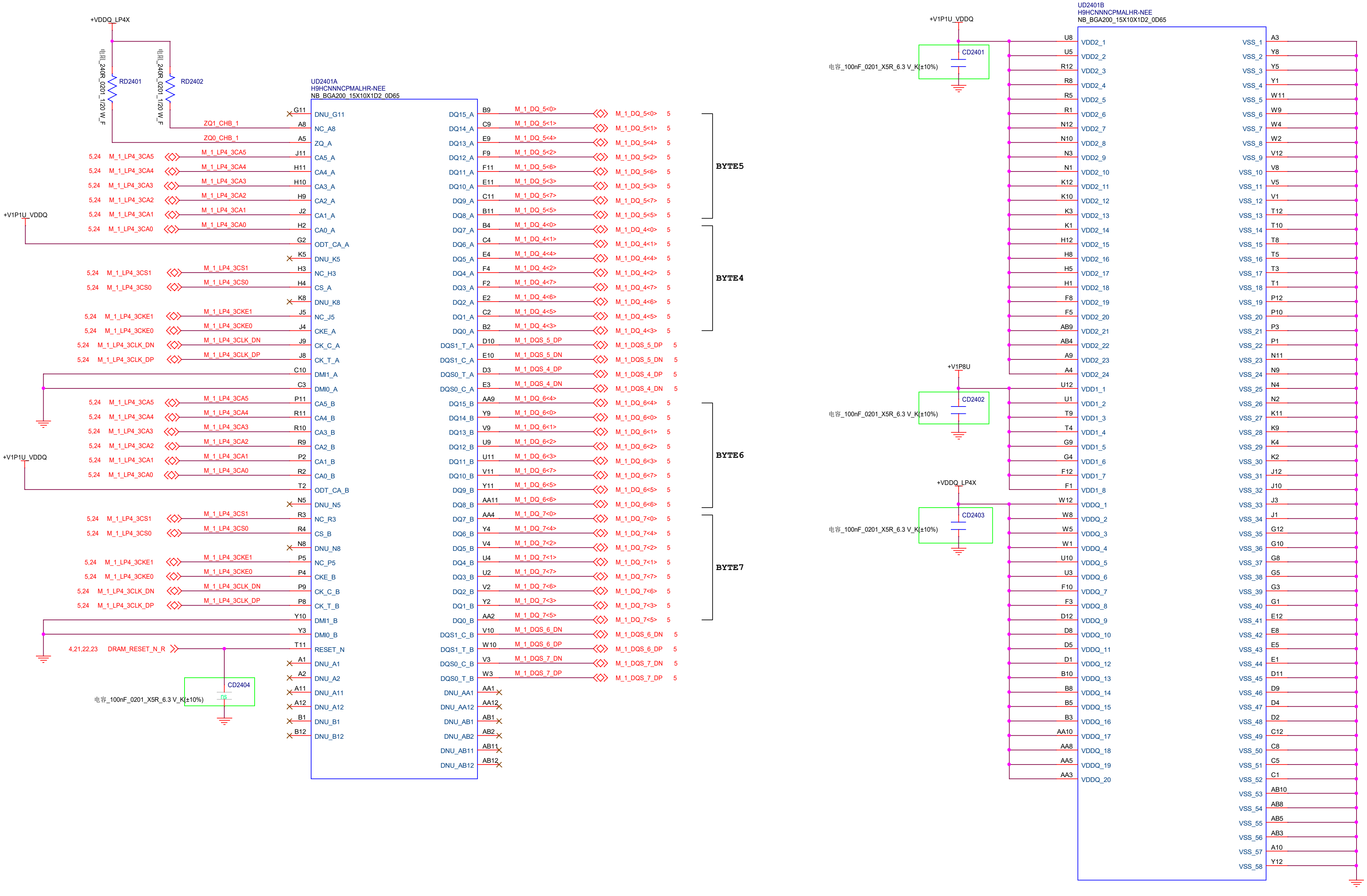
CHB-2



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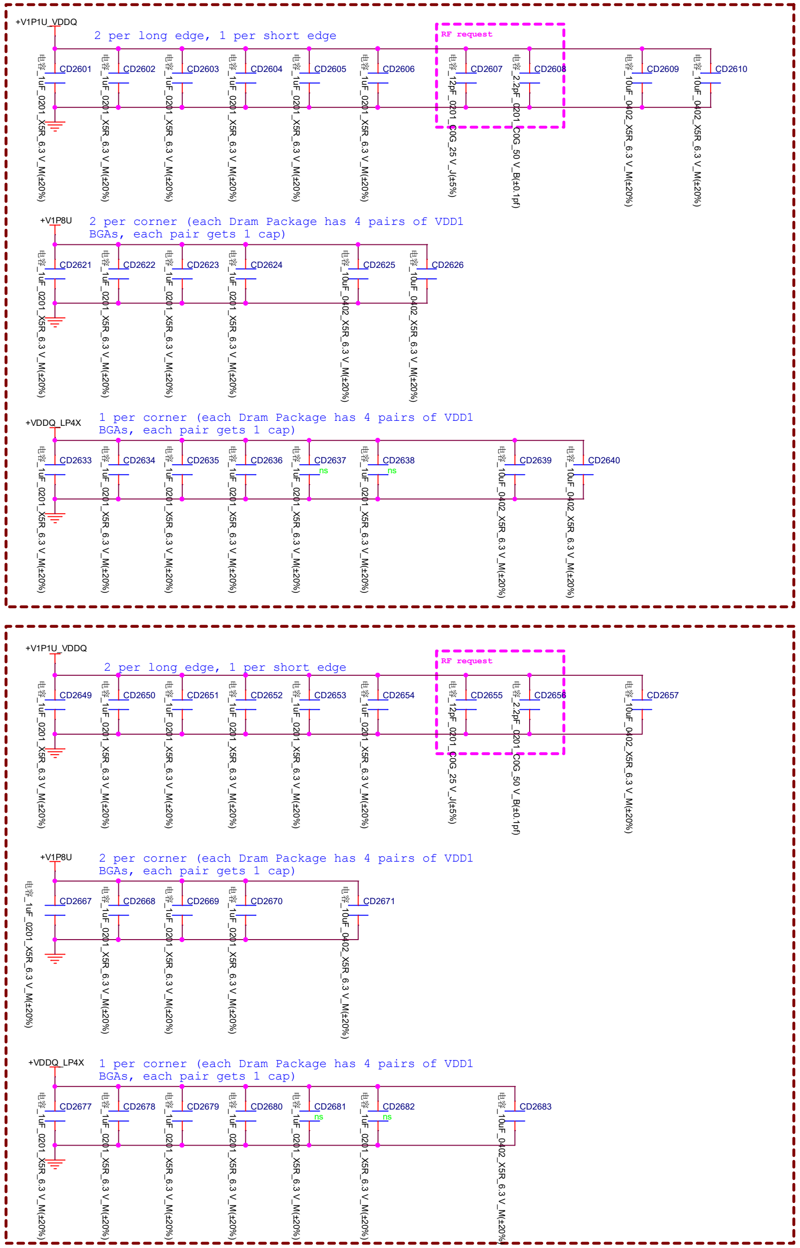
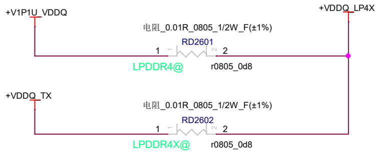
DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL A



DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL B



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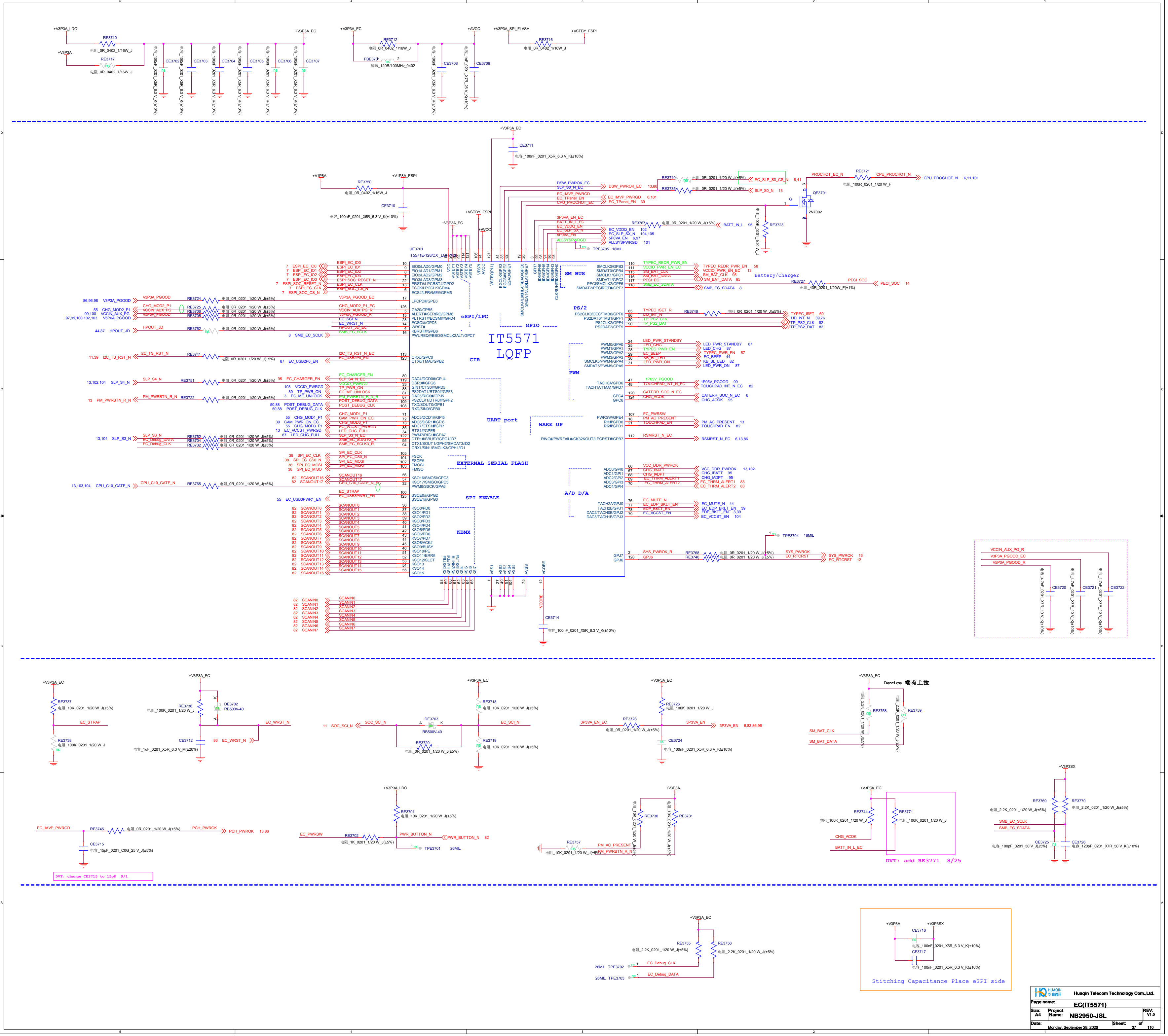

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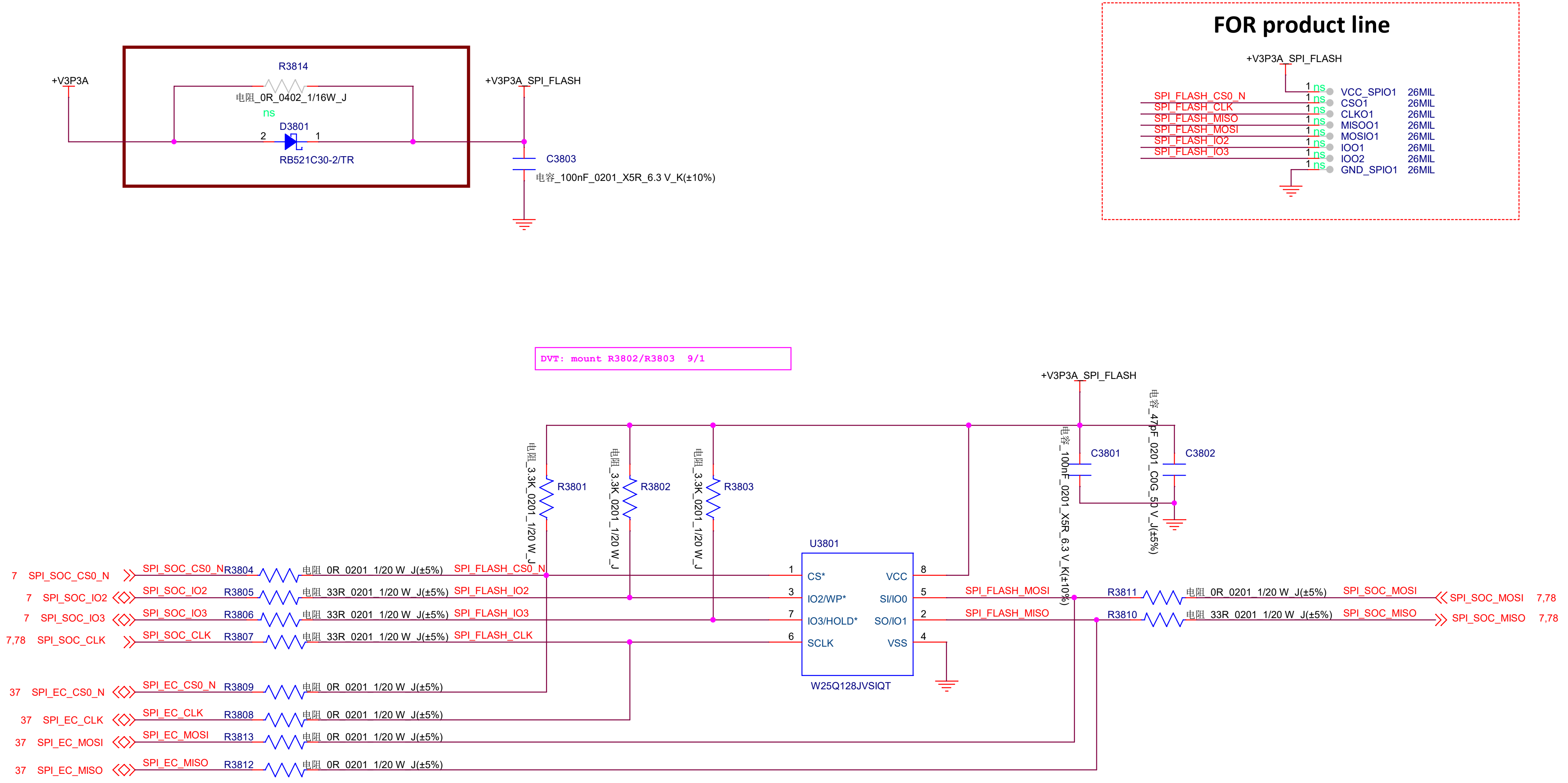

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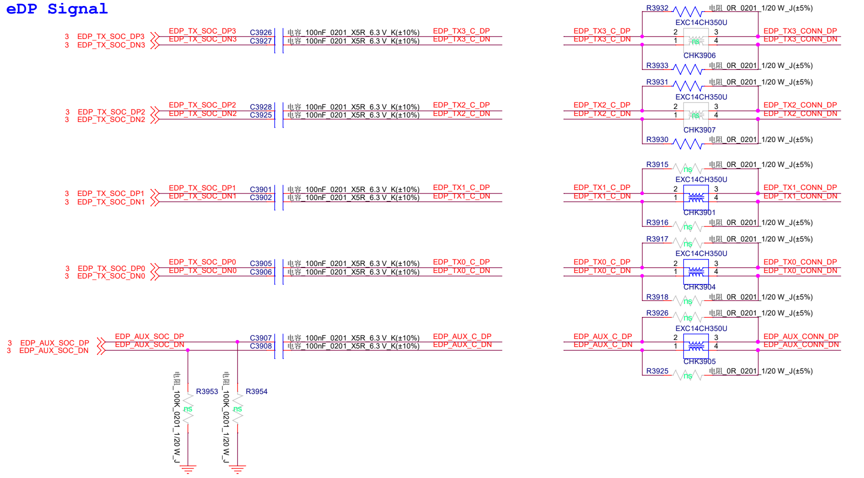
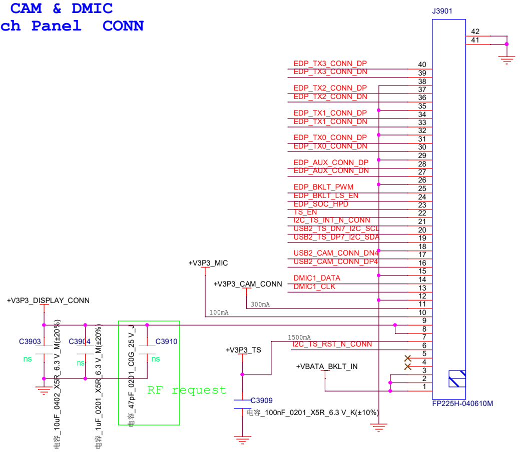
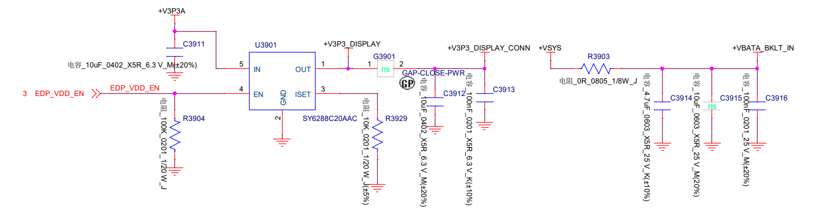
eDP Signal



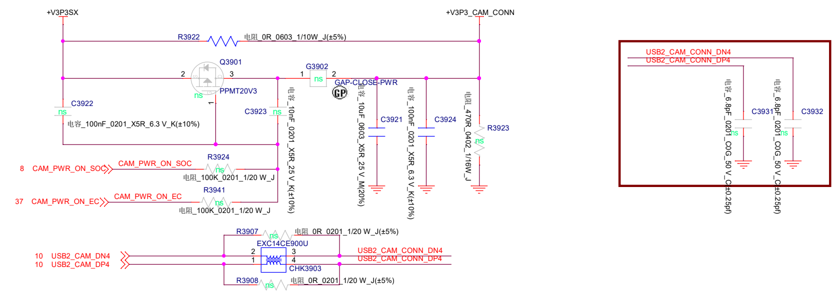
eDP & CAM & DMIC & Touch Panel CONN



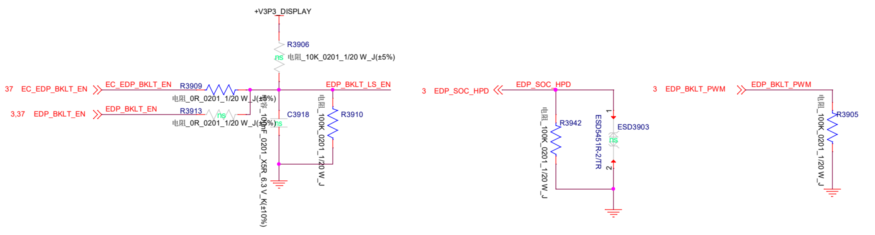
eDP VCC & BL Power



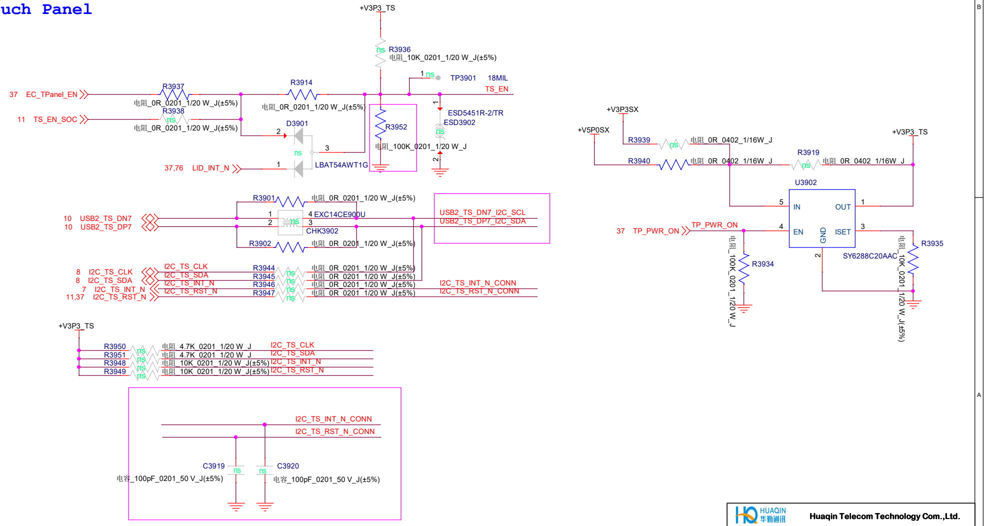
CAM Power



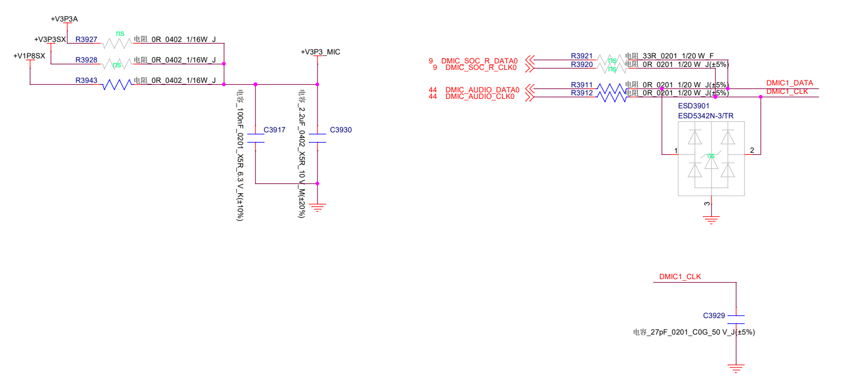
eDP Control



Touch Panel



MIC



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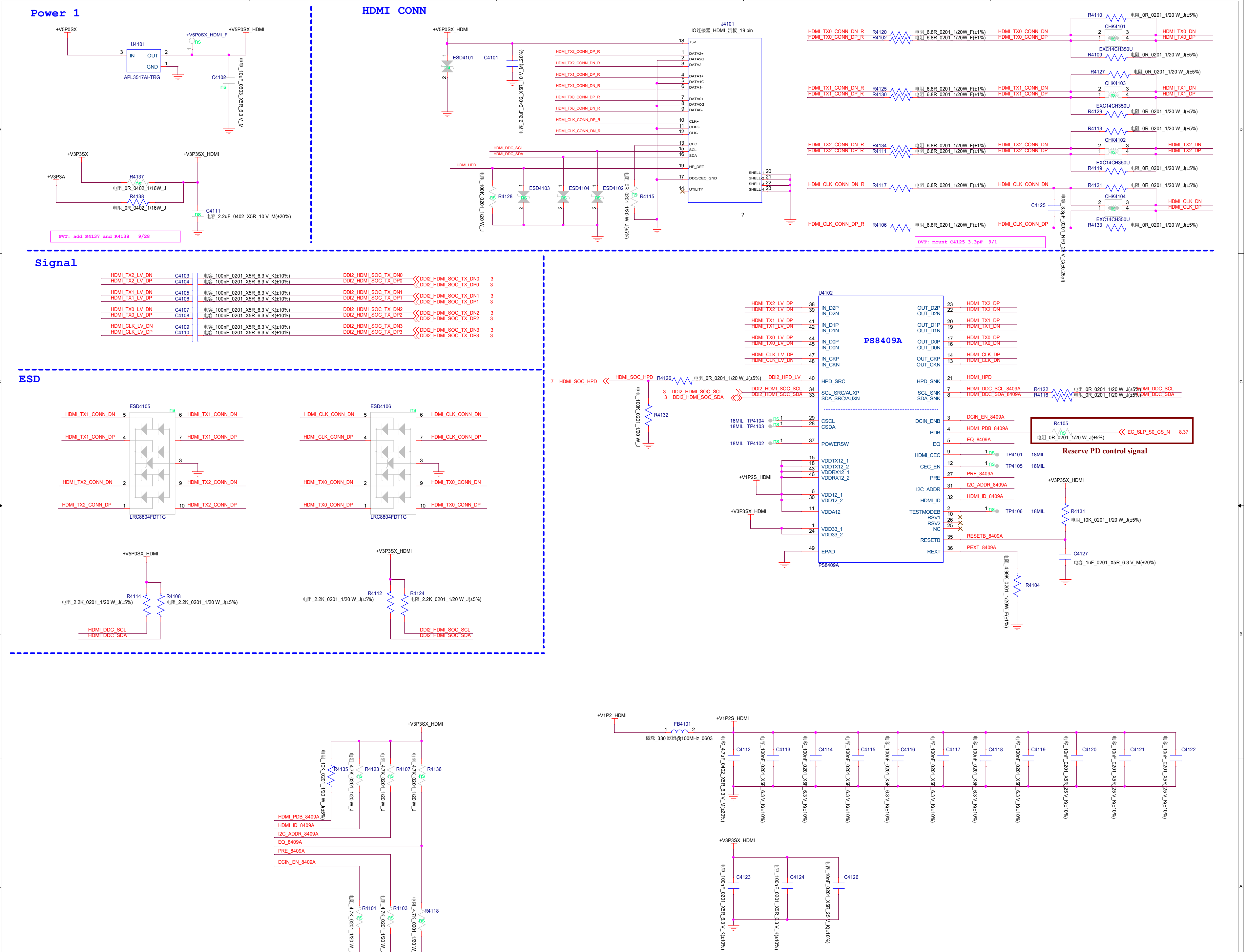

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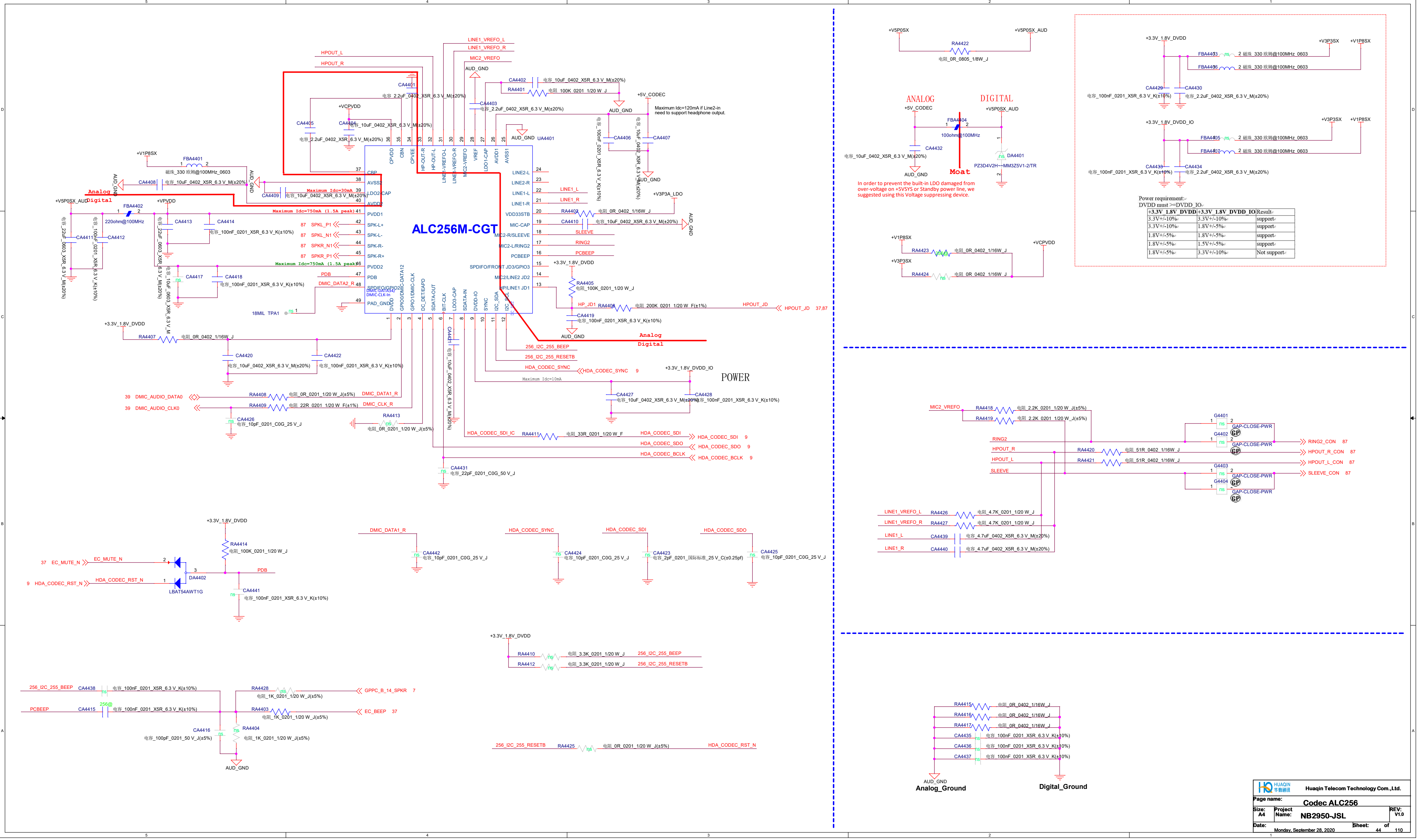

Power requirement:
DVDD must >=DVDD_IO

+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

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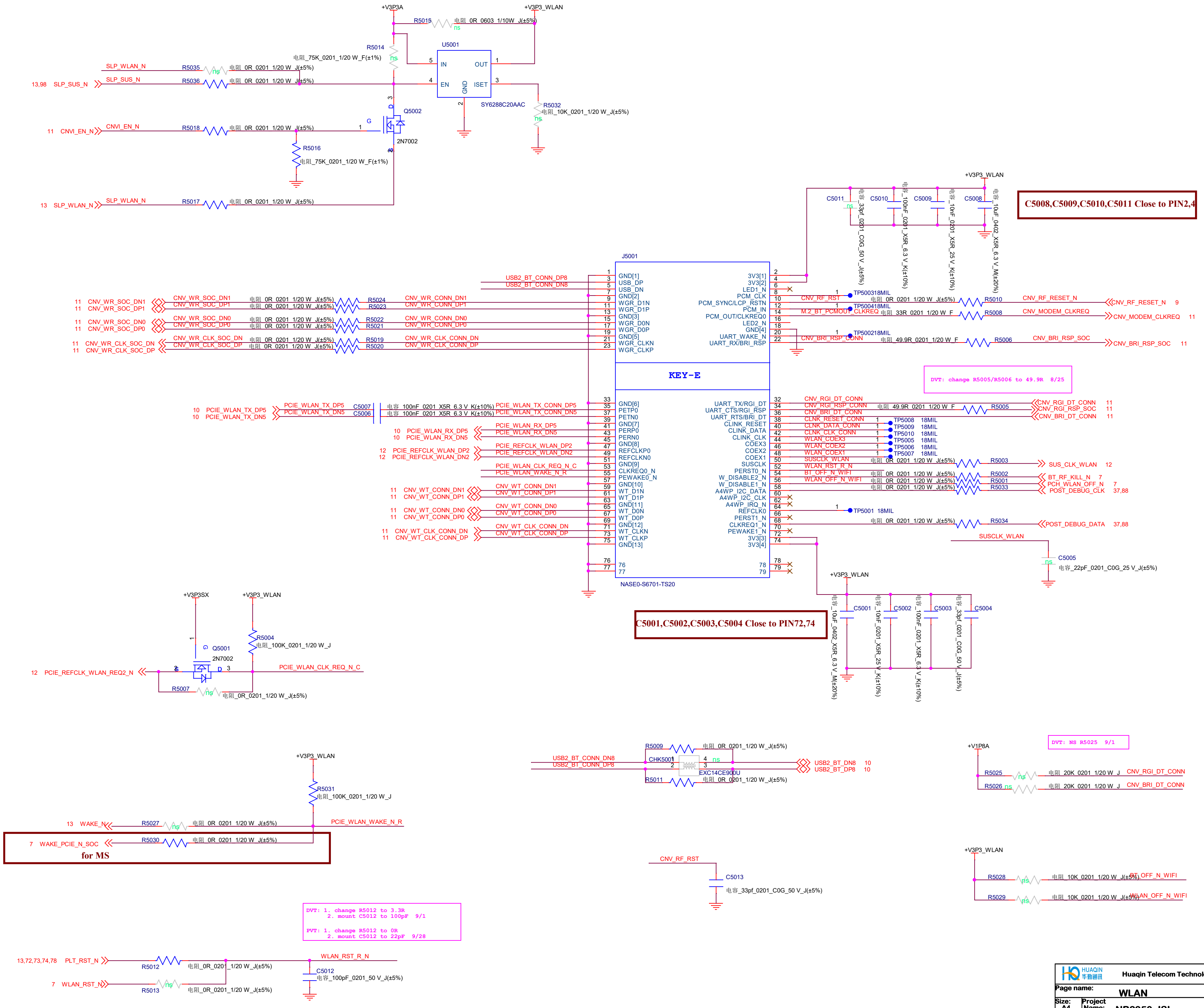

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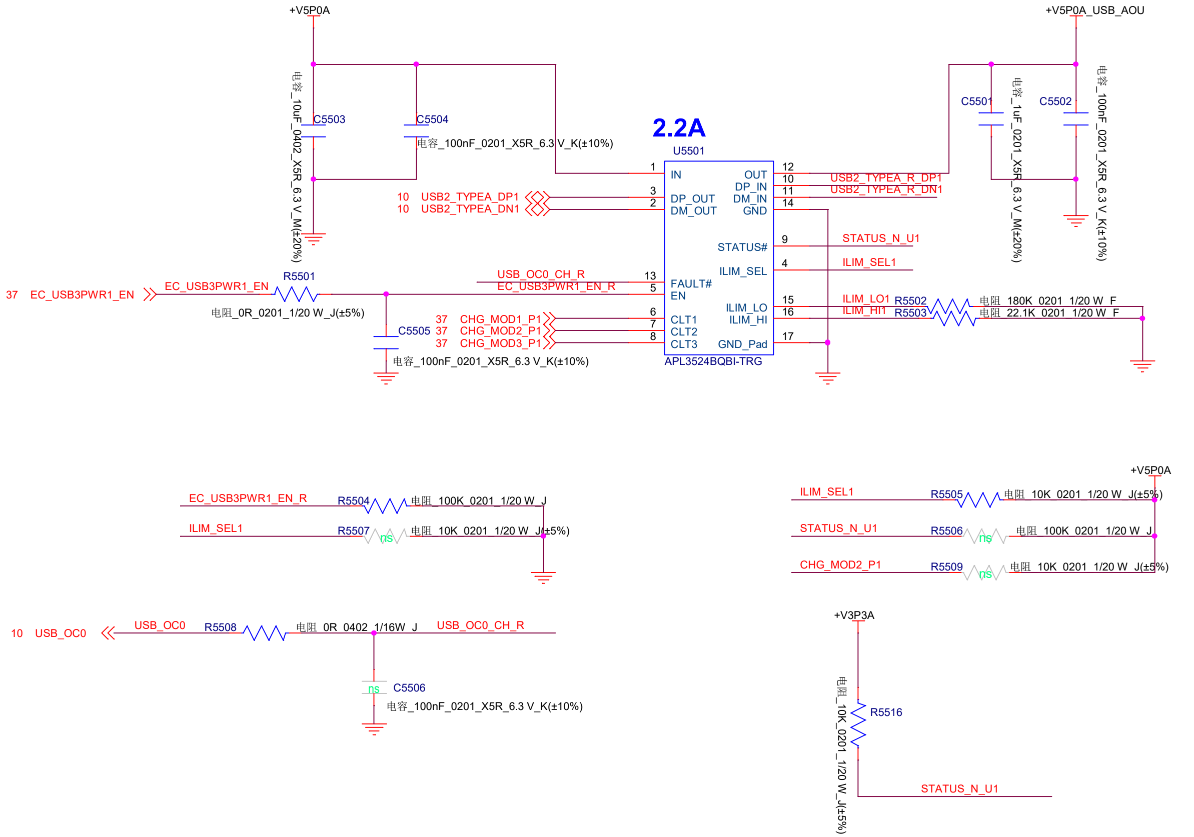
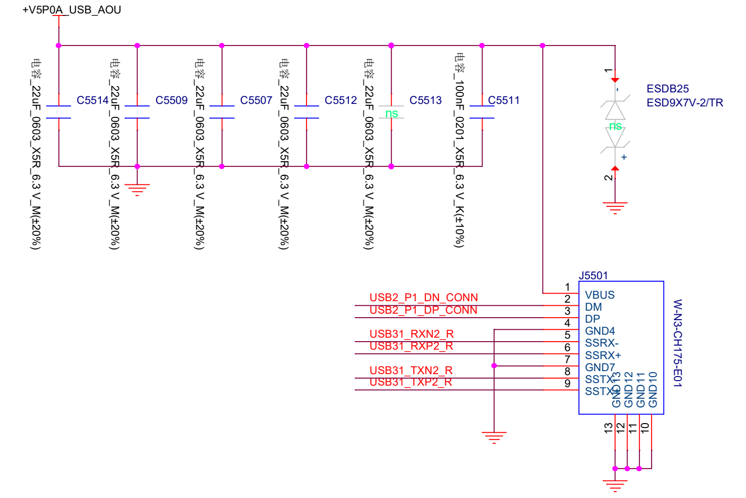
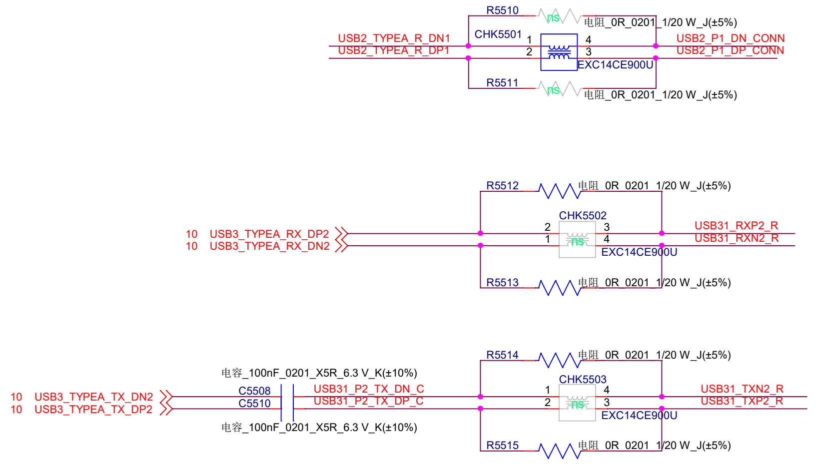
USB3.1 POWER Port



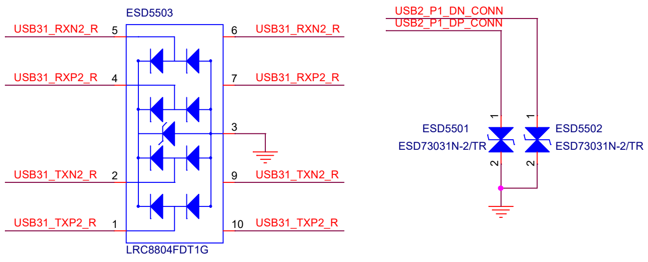
USB3.1 Connector



USB3.1 Signal



USB3.1 ESD



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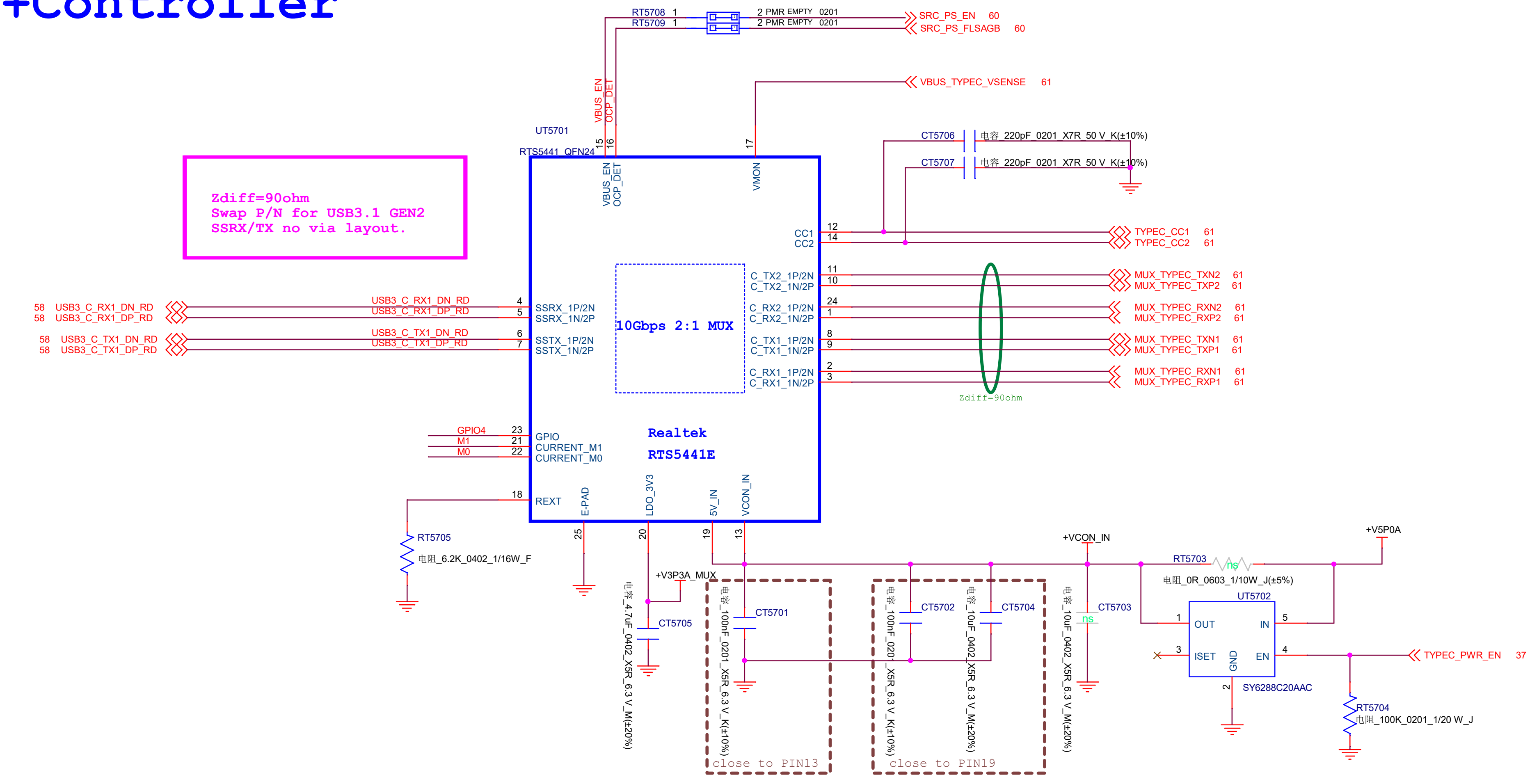
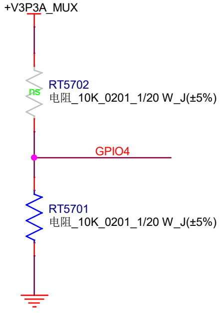
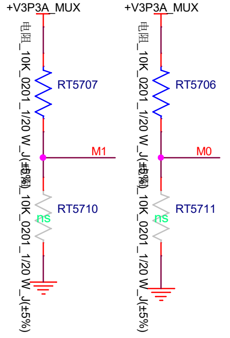
Mux+Controller







	M1	M0	Note
Rp:900mA	0	1	RT34/RT30 mount,RT32/RT35 don't mount
Rp:1.5A	1	0	RT32/RT35 mount,RT34/RT30 don't mount
Rp:3.0A	1	1	RT32/RT30 mount,RT34/RT35 don't mount

Rp configuration

Rp:3.0A (now)

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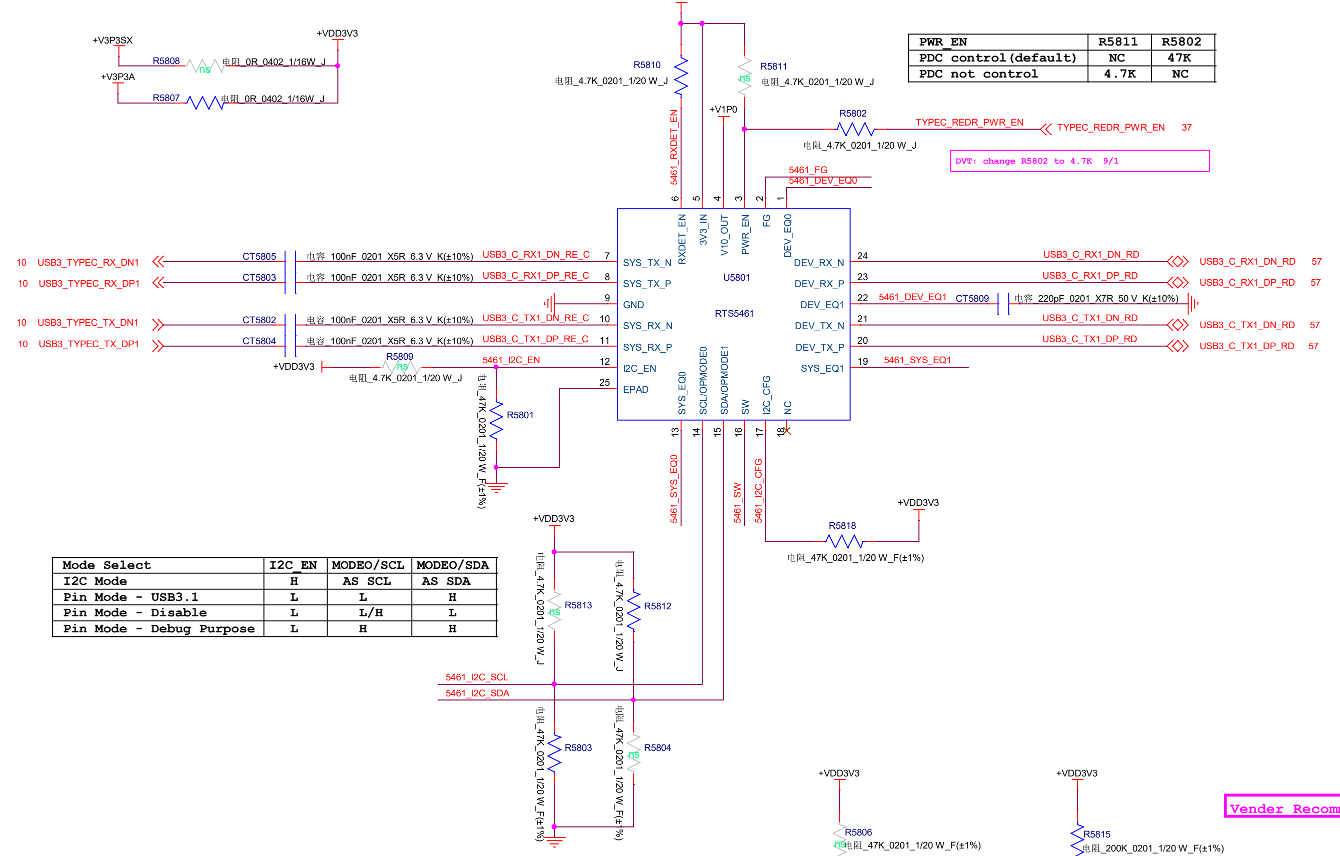
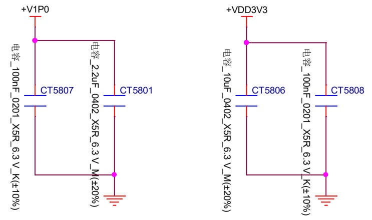
Redriver



PWR_EN	R5811	R5802
PDC control(default)	NC	47K
PDC not control	4.7K	NC

Mode Select	I2C_EN	MODEO/SCL	MODEO/SDA
I2C Mode	H	AS SCL	AS SDA
Pin Mode - USB3.1	L	L	H
Pin Mode - Disable	L	L/H	L
Pin Mode - Debug Purpose	L	H	H



5641_EQX	Rpu	Rpd
L	NC	1K
ML	200K	NC
MH	47K	NC
H	1K	NC

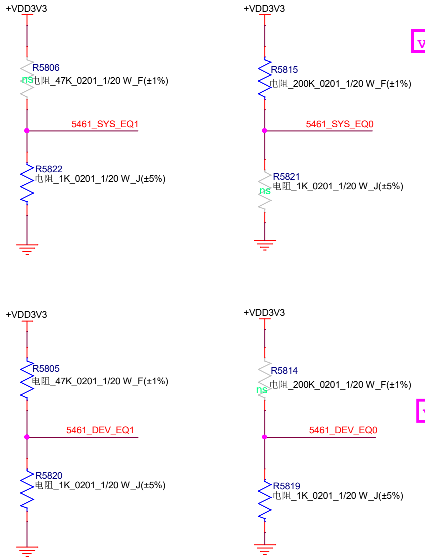


Table 5-3 Host SSTX Channel Equalization Configuration Table

Vender Recommend

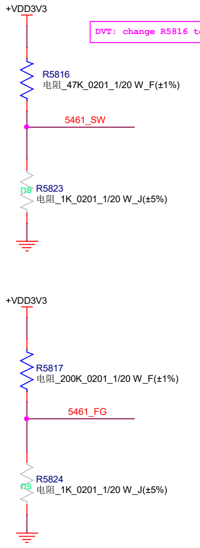
Host SSTX channel EQ Setting	SYS_EQ1 pin	SYS_EQ0 pin	EQ@2.5GHz (dB)	EQ@5GHz (dB)
0	L	L	-0.3	-0.2
1	L	ML	0.5	1.8
2	L	MH	1.3	3.6
3	L	H	2.2	5.2
4	ML	L	3.2	6.6
5	ML	ML	4.1	7.8
6	ML	MH	5.0	8.9
7	ML	H	5.9	9.8
8	MH	L	6.8	10.3
9	MH	ML	7.6	11.0
10	MH	MH	8.3	11.5
11	MH	H	9.0	12.1
12	H	L	9.7	12.4
13	H	ML	10.3	12.9
14	H	MH	10.9	13.2
15	H	H	11.4	13.6

Table 5-4 Host SSRX Channel Equalization Configuration Table

Vender Recommend

Host SSRX channel EQ Setting	DEV_EQ1 pin	DEV_EQ0 pin	EQ@2.5GHz (dB)	EQ@5GHz (dB)
0	L	L	-0.3	-0.2
1	L	ML	0.5	1.8
2	L	MH	1.3	3.6
3	L	H	2.2	5.2
4	ML	L	3.2	6.6
5	ML	ML	4.1	7.8
6	ML	MH	5.0	8.9
7	ML	H	5.9	9.8
8	MH	L	6.8	10.3
9	MH	ML	7.6	11.0
10	MH	MH	8.3	11.5
11	MH	H	9.0	12.1
12	H	L	9.7	12.4
13	H	ML	10.3	12.9
14	H	MH	10.9	13.2
15	H	H	11.4	13.6

DVT: change R5816 to 47K 9/1



SW	R5816	R5823	
900mvpp	NC	1K	
1000mvpp	200K	NC	Default
1100mvpp	47K	NC	
1200mvpp	1K	NC	

FG	R5817	R5824	
-1db	NC	1K	
0db	200K	NC	Default
1dB	47K	NC	
2dB	1K	NC	

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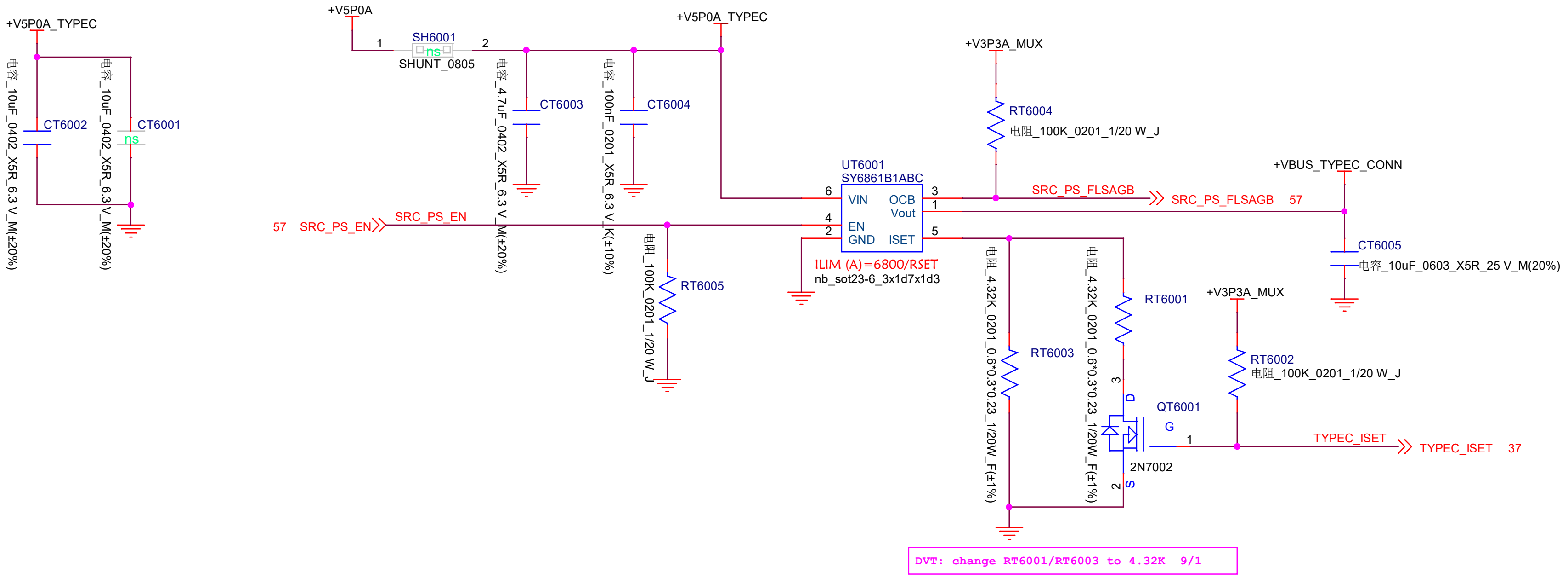
TYPEC Output



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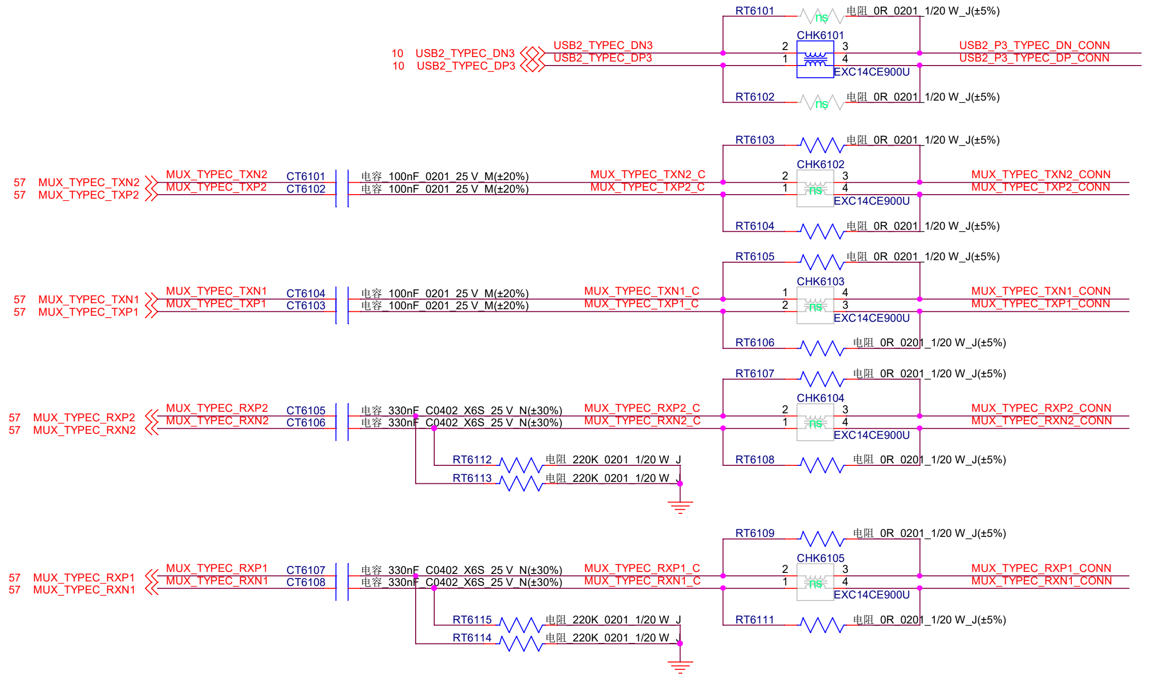
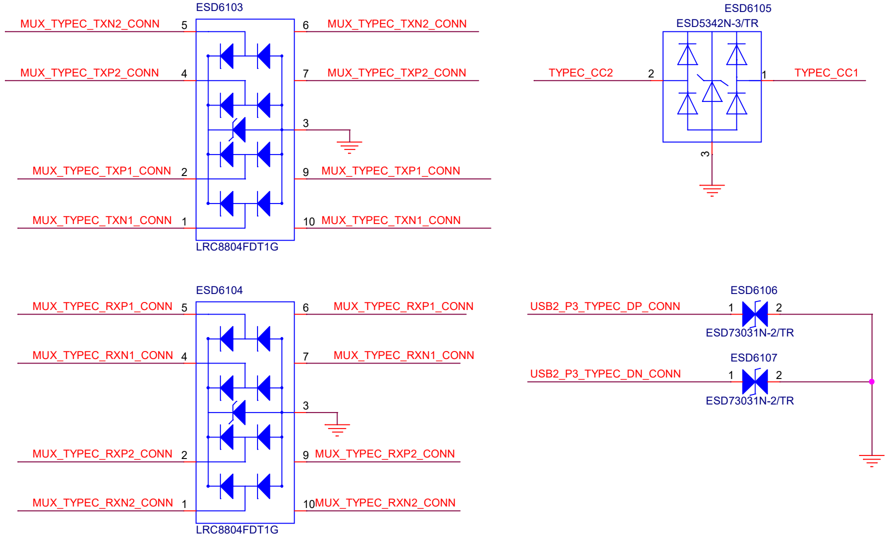
TYPE-C Signal



TYPE-C ESD



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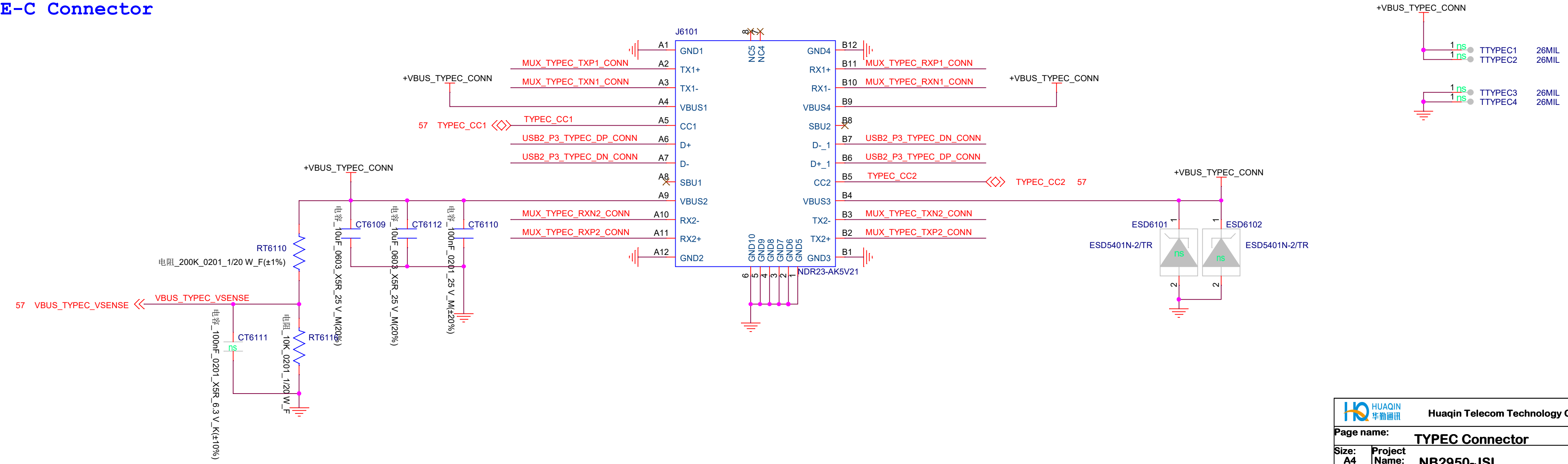

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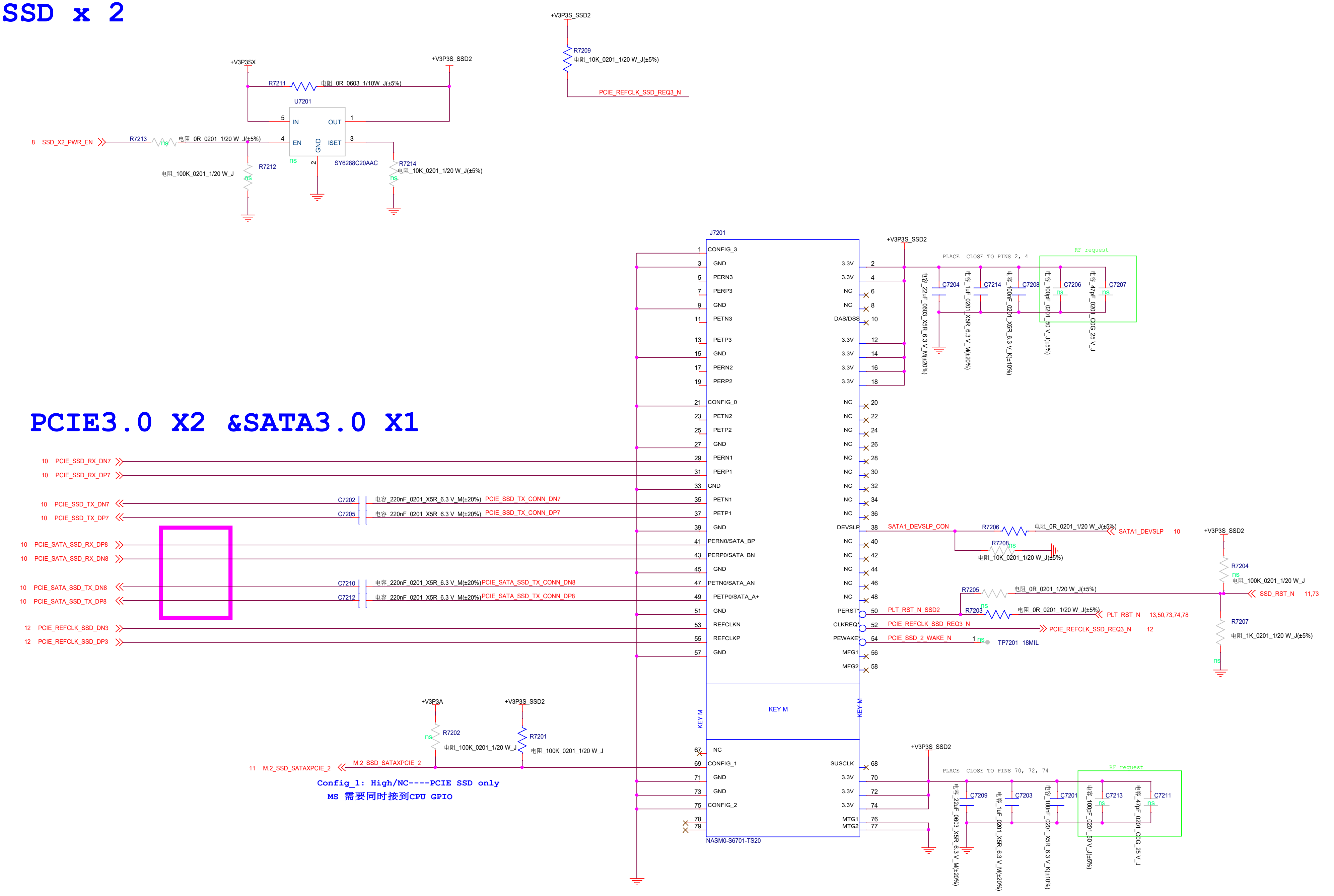
SSD x 2

PCIE3.0 X2 &SATA3.0 X1



Config_1: High/NC----PCIE SSD only

MS 需要同时接到CPU GPIO

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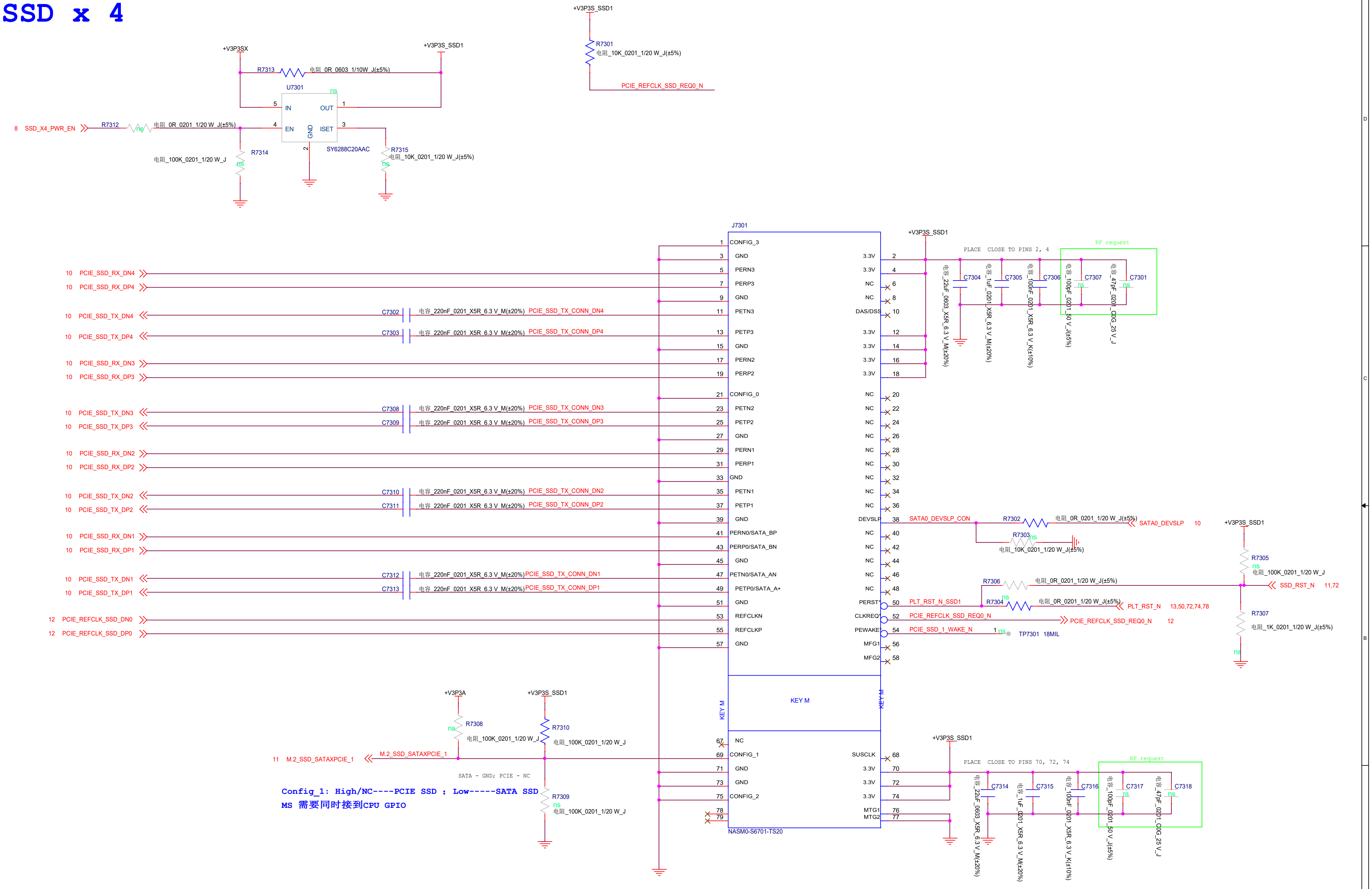
SSD x 4



Config_1: High/NC----PCIE SSD ; Low-----SATA SSD
MS 需要同时接到CPU GPIO

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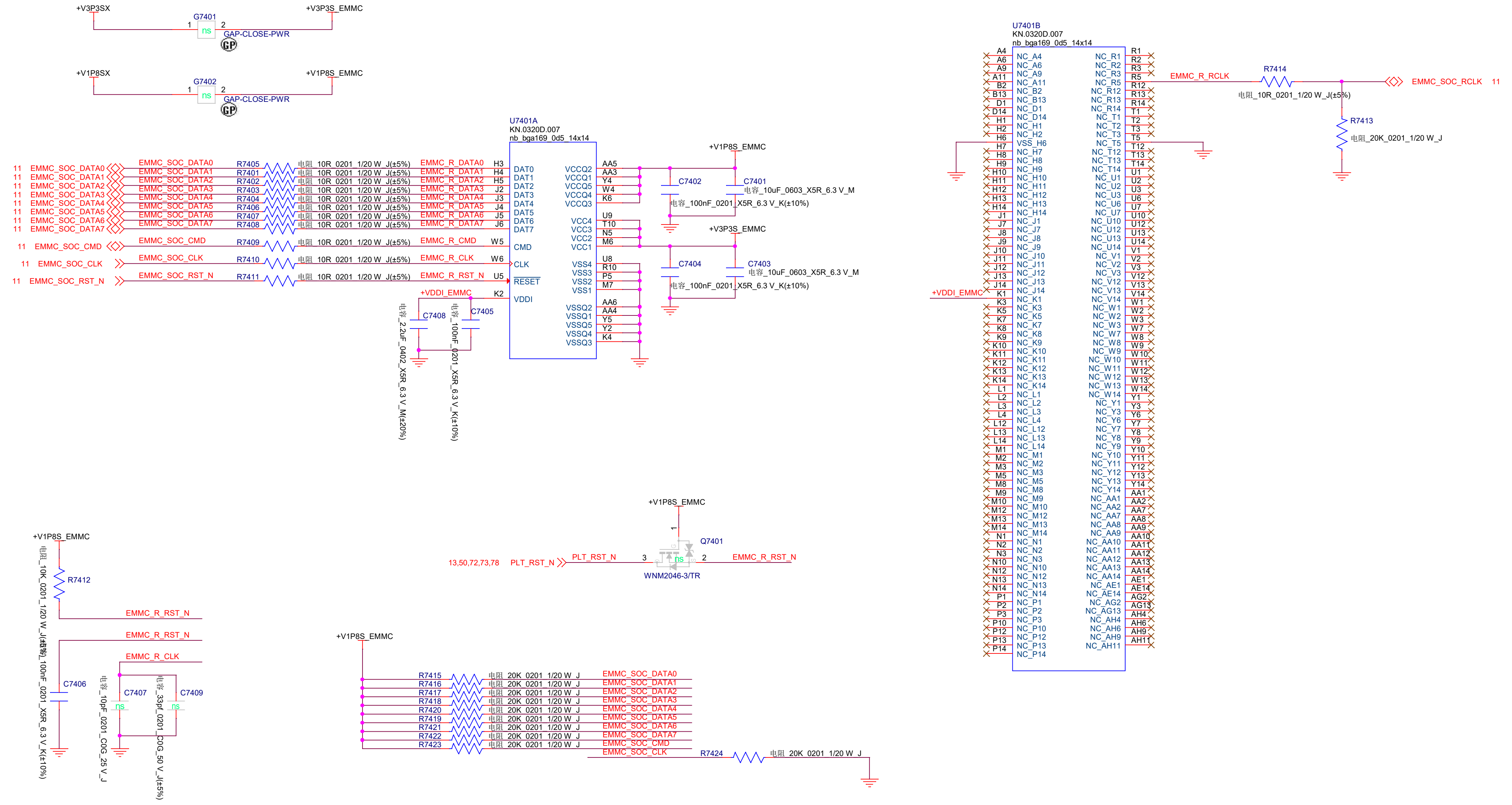

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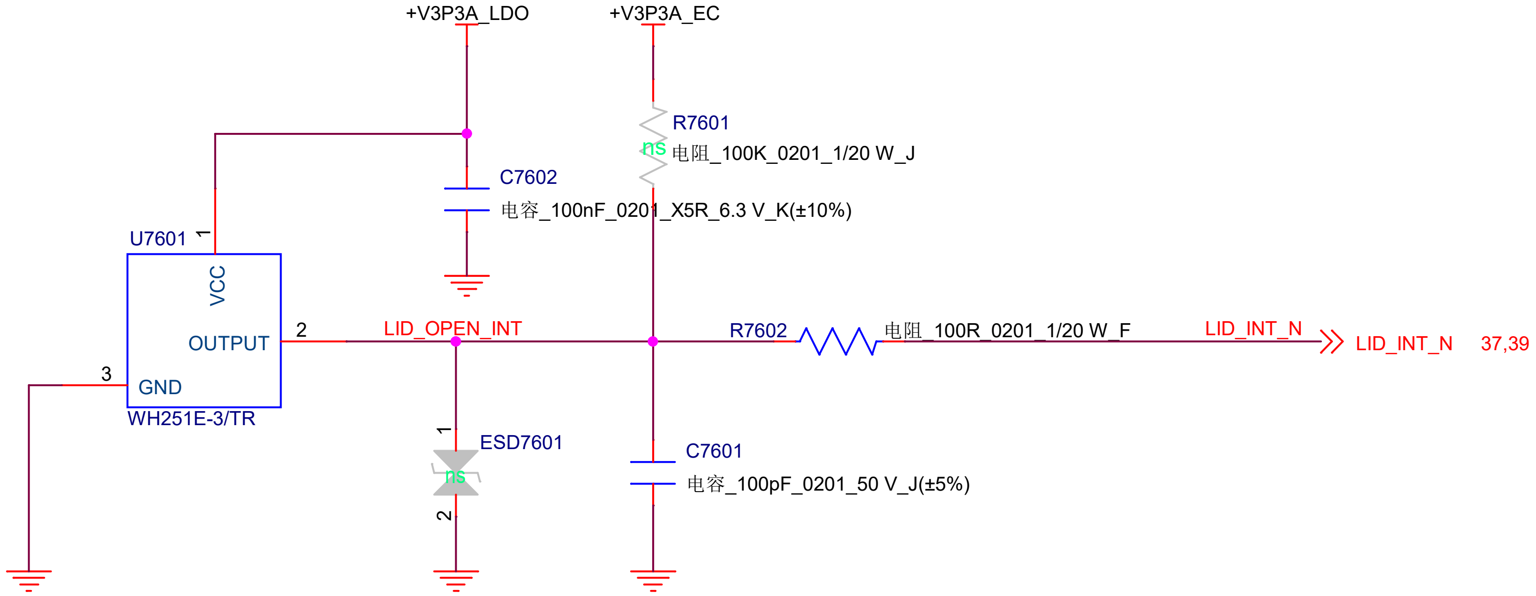
HALL



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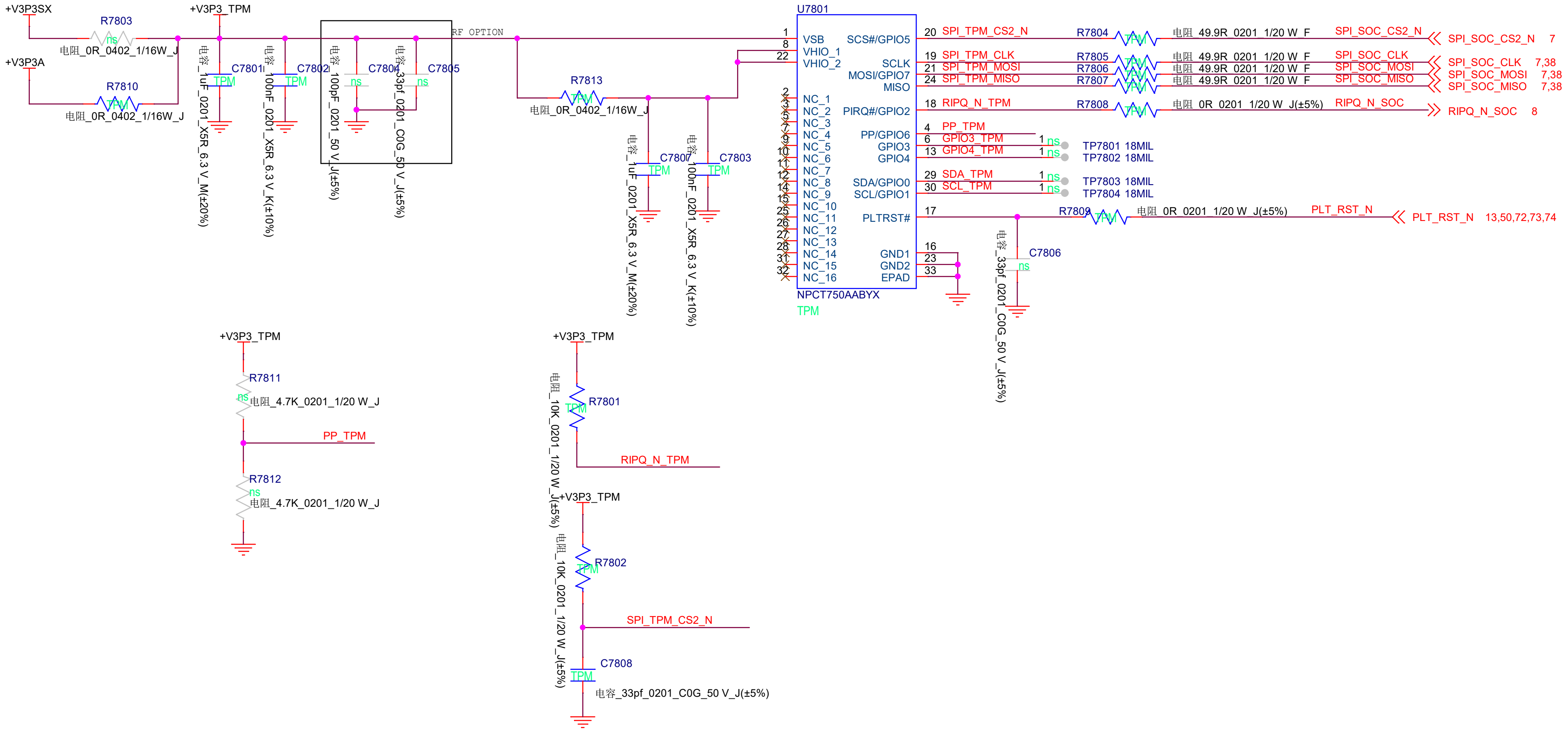

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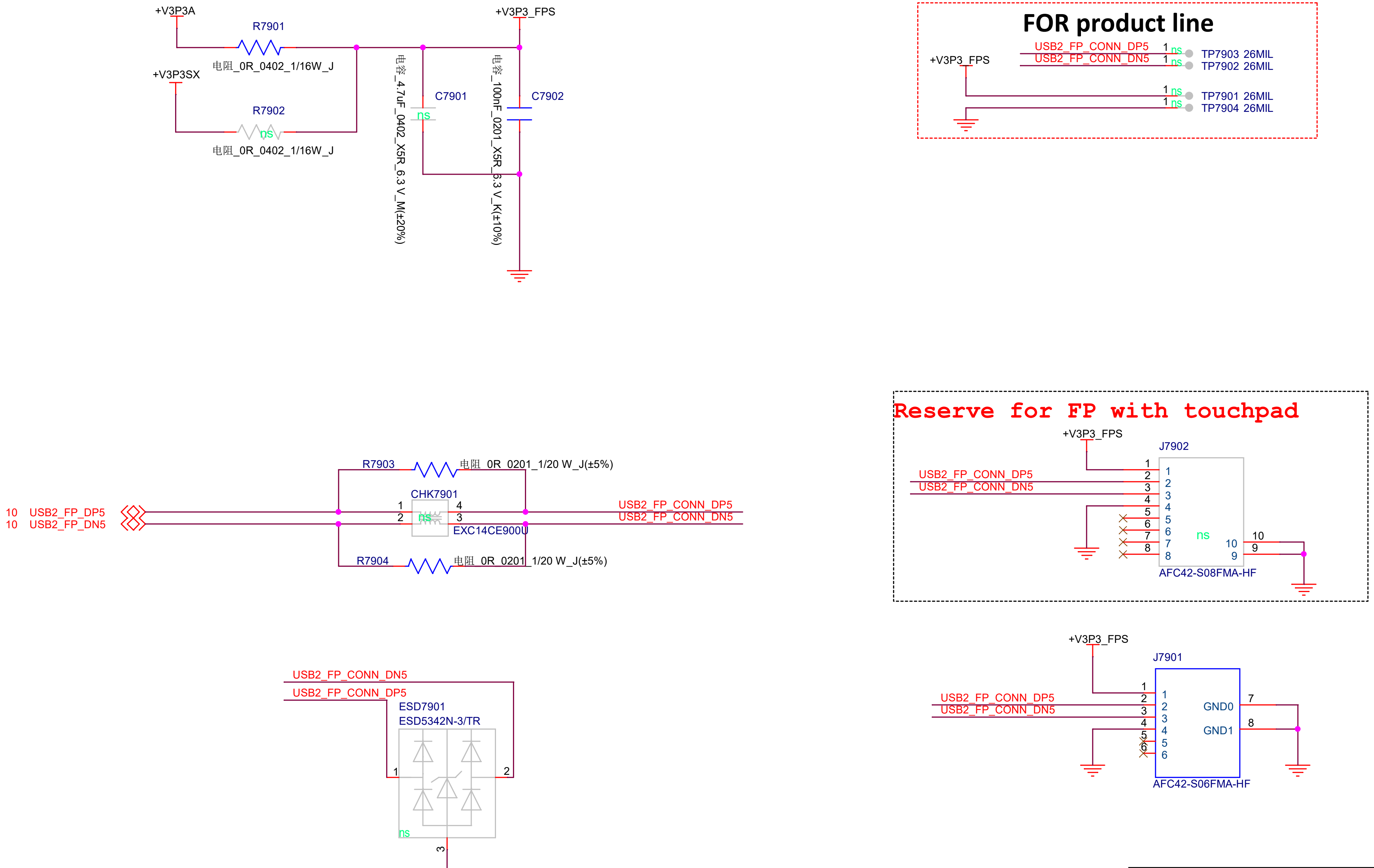
Finger Print



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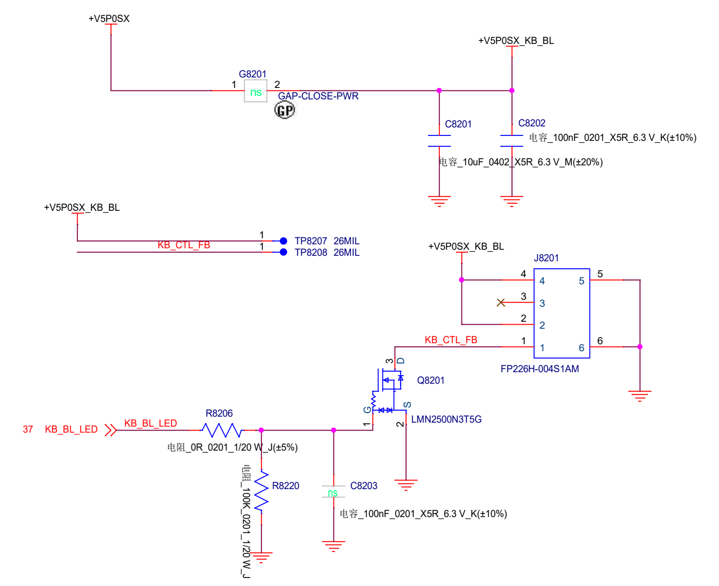
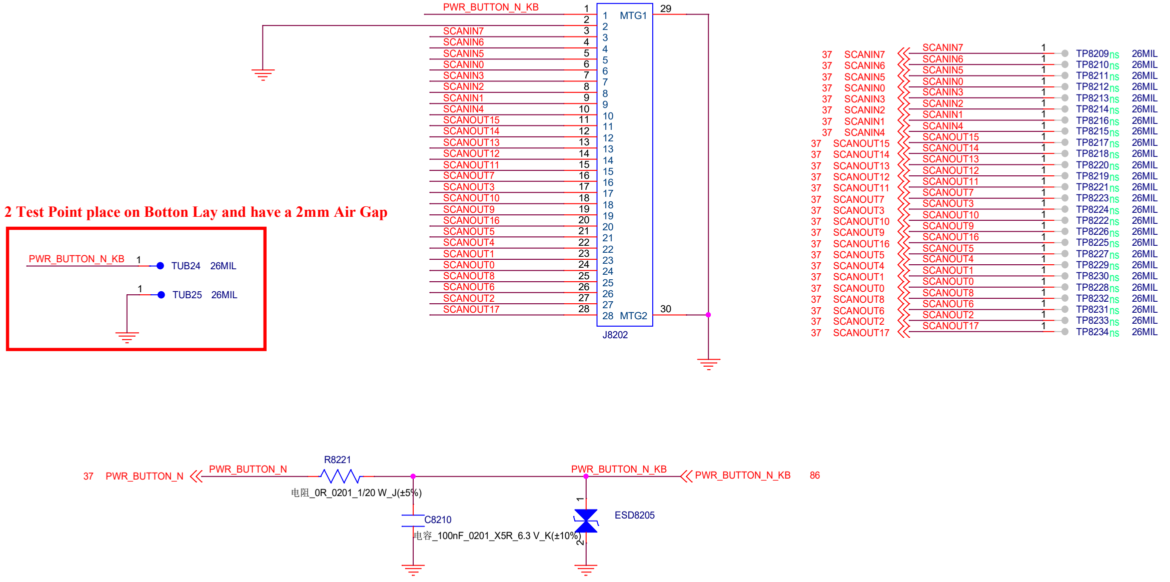
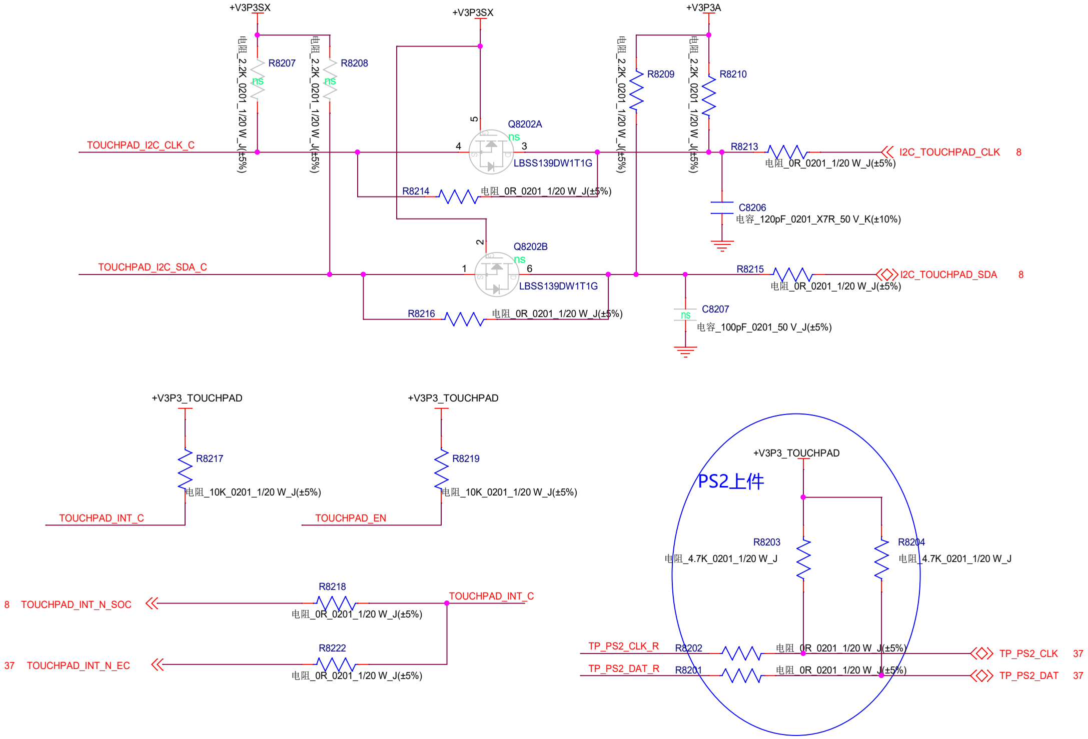
KB Backlight



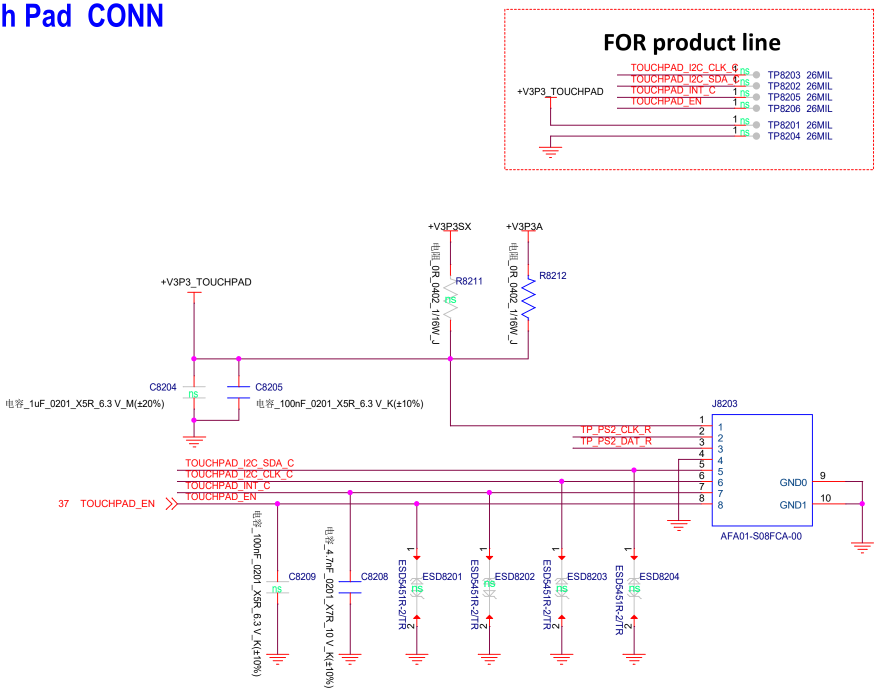
KB CONN



Touch Pad



Touch Pad CONN



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Page name:	KB CON/BL/TouchPad	
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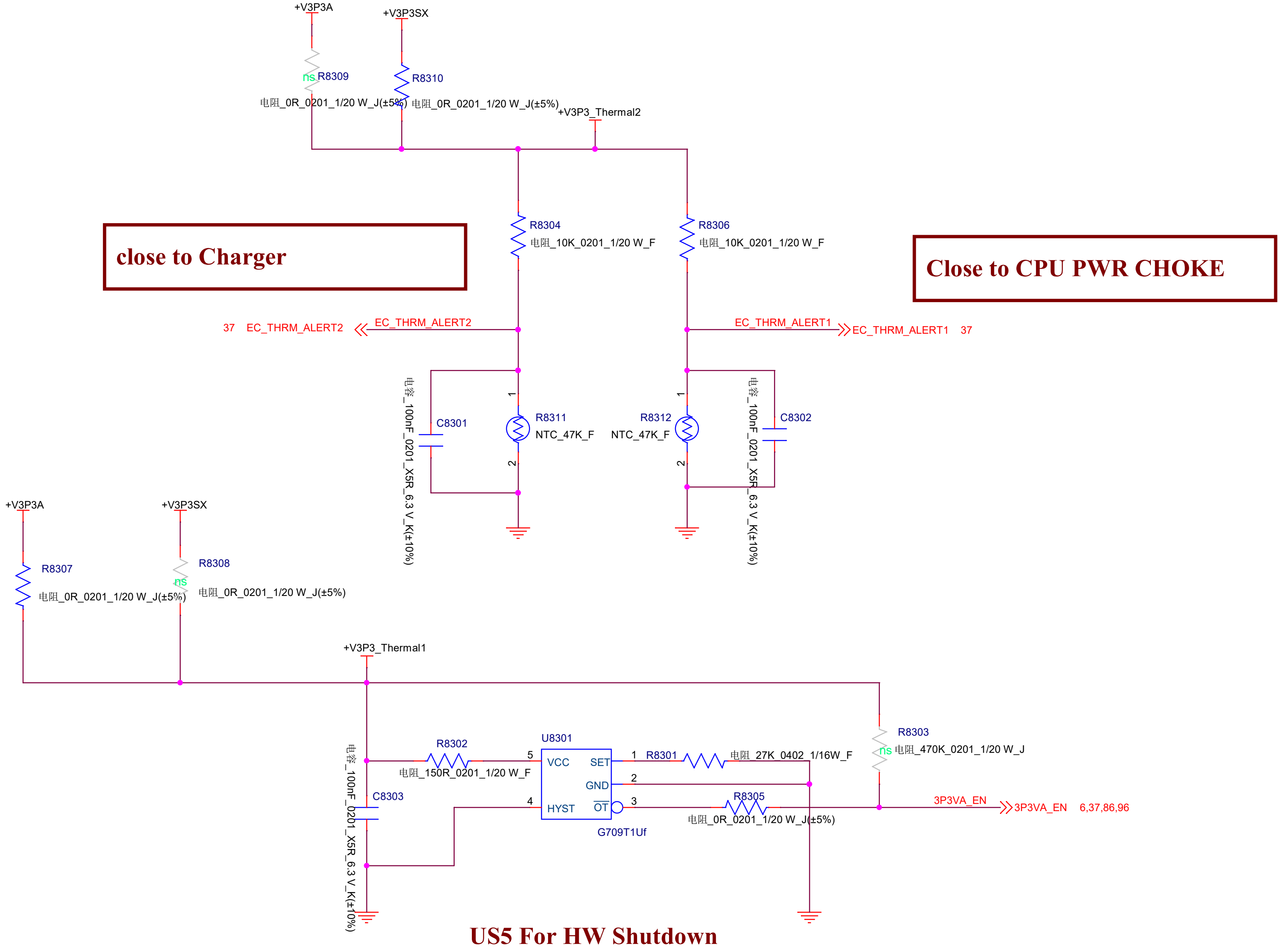
REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces



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Page name:	Thermal sensor		
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Size: A4	**Project Name:** NB2950-JSL			**REV:** V1.0
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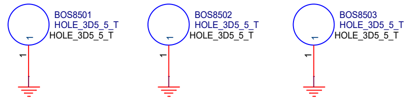
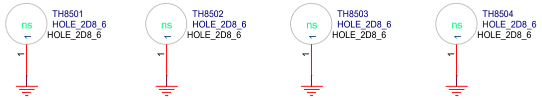
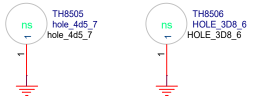
Thermal Pad BOSS *3



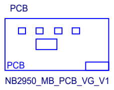
HOLE *4



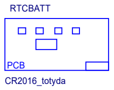
HOLE *2



PCB



RTC



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Page name: **Hole/ Mark**

Size: A4
Project Name: **NB2950-JSL**
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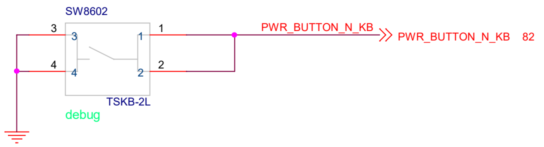
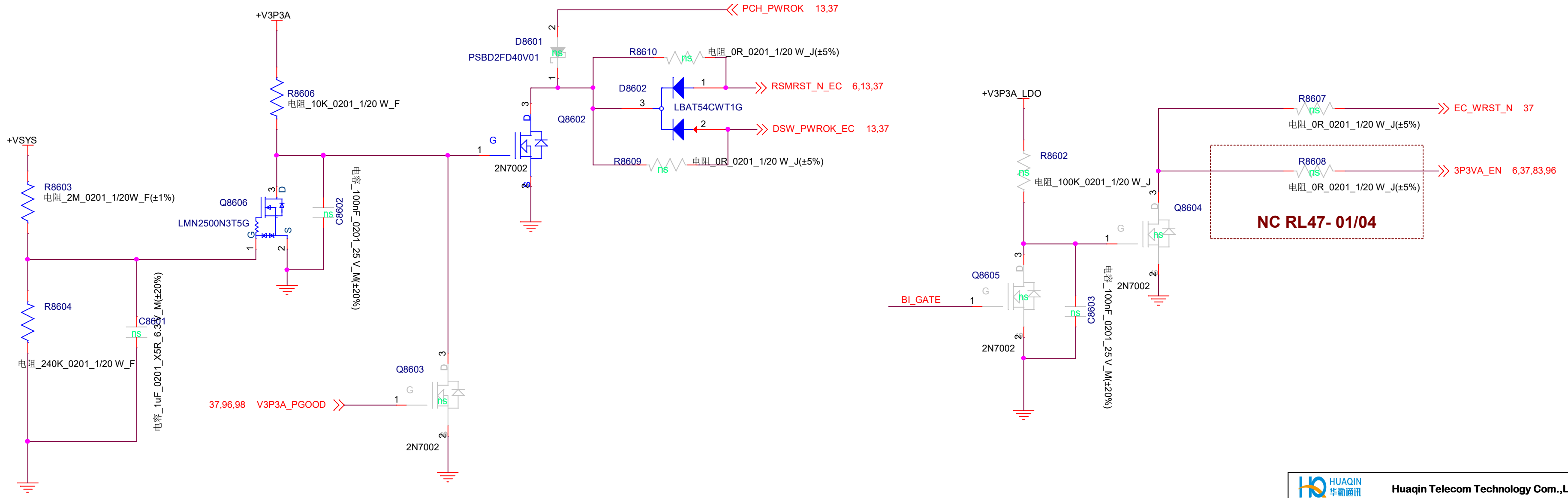
Reset BUTTON

Open door BUTTON

Debug BUTTON



Abnormal PD logic



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Page name: **Logic Circuit**

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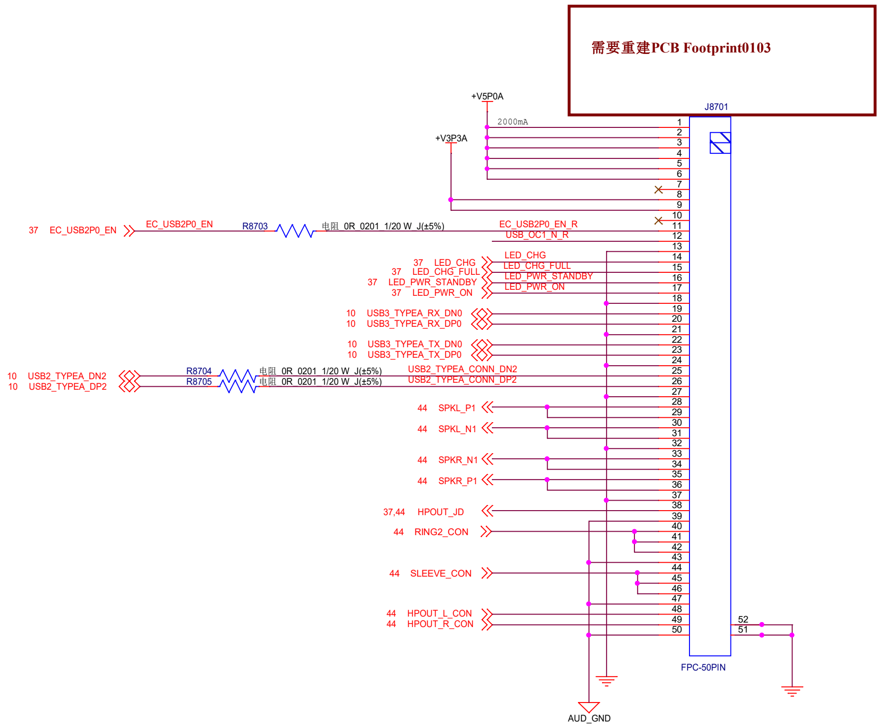
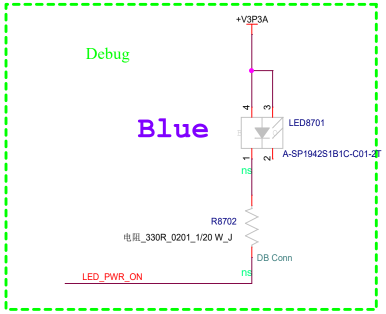
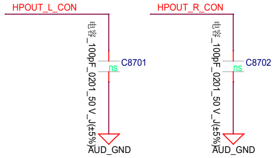
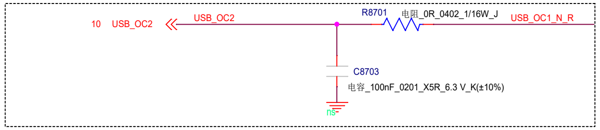
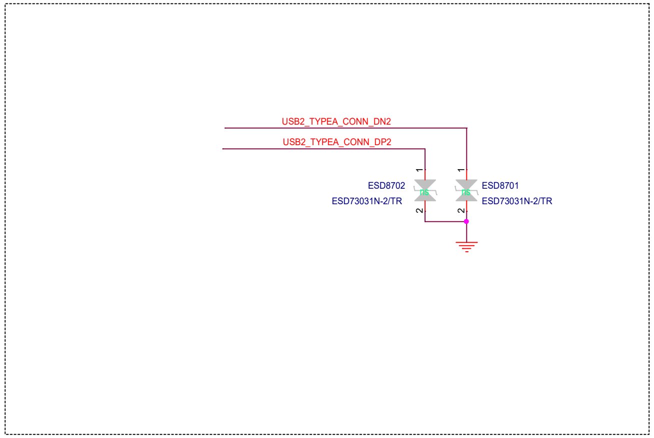


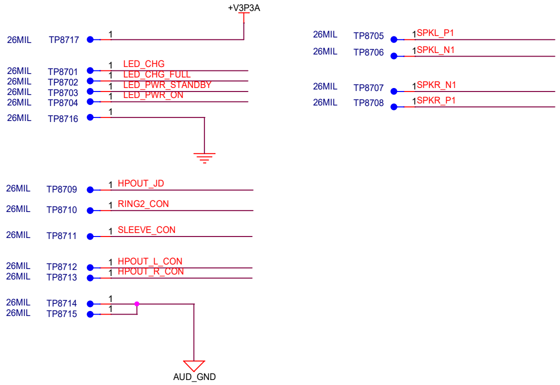








FOR product line



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Page name: **DB CONNECTOR**

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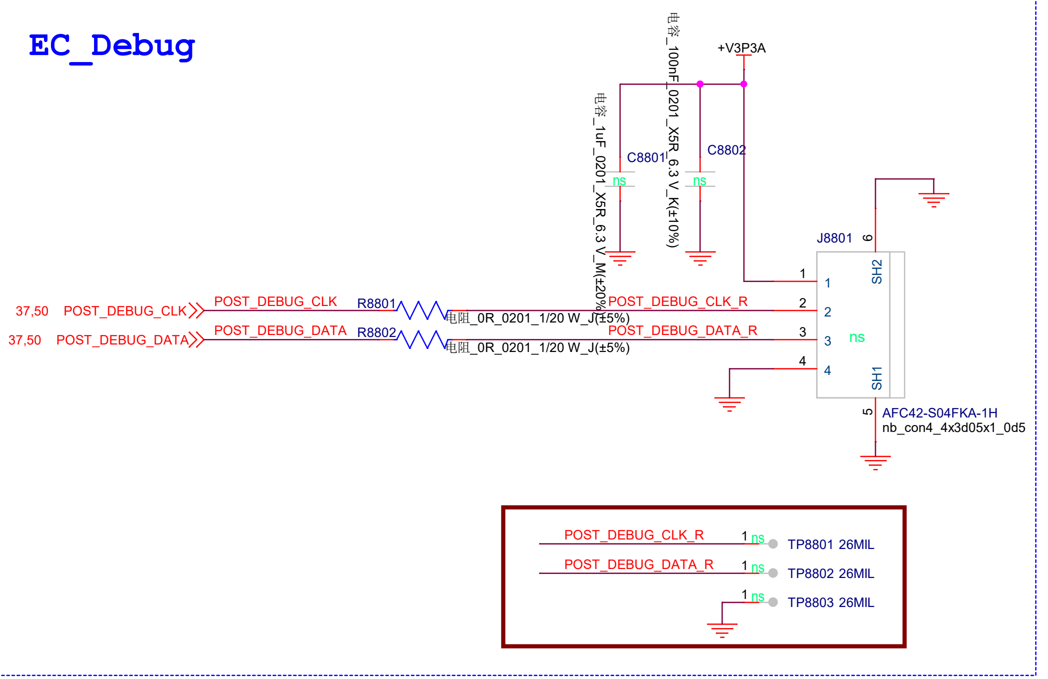
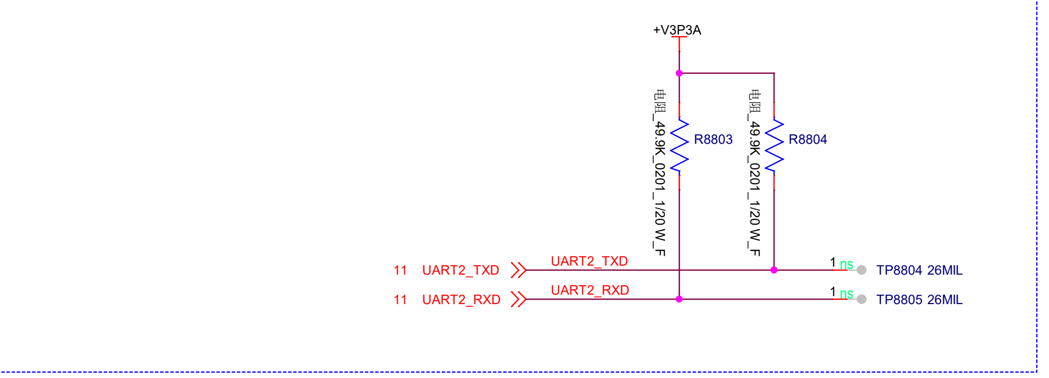
EC_Debug



System_UART_Debug



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Page name: **Debug Conn**

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Page name: **BLANK**

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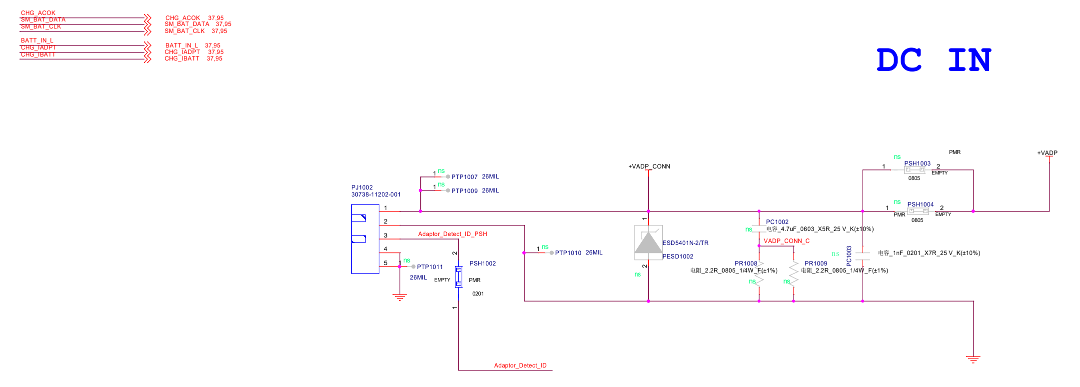
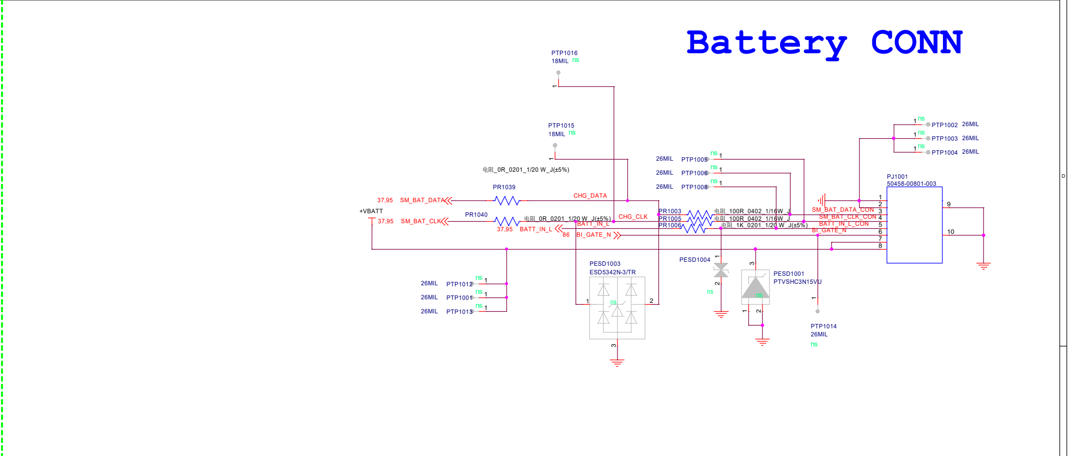
DC IN

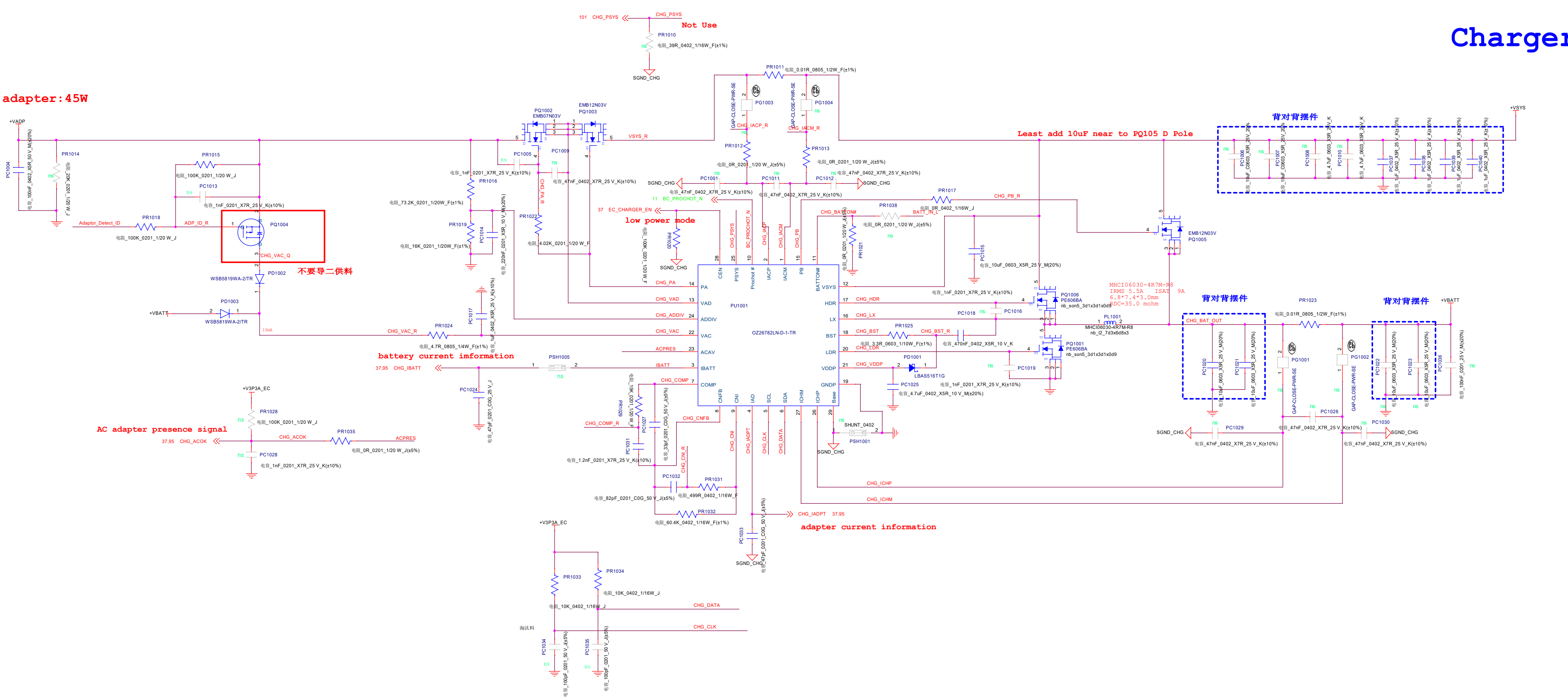


Battery CONN



Charger

adapter:45W



HUAQIN 华勤通讯 Huaqin Telecom Technology Com.,Ltd.
Page name: POWER DELIVERY_CHARGER
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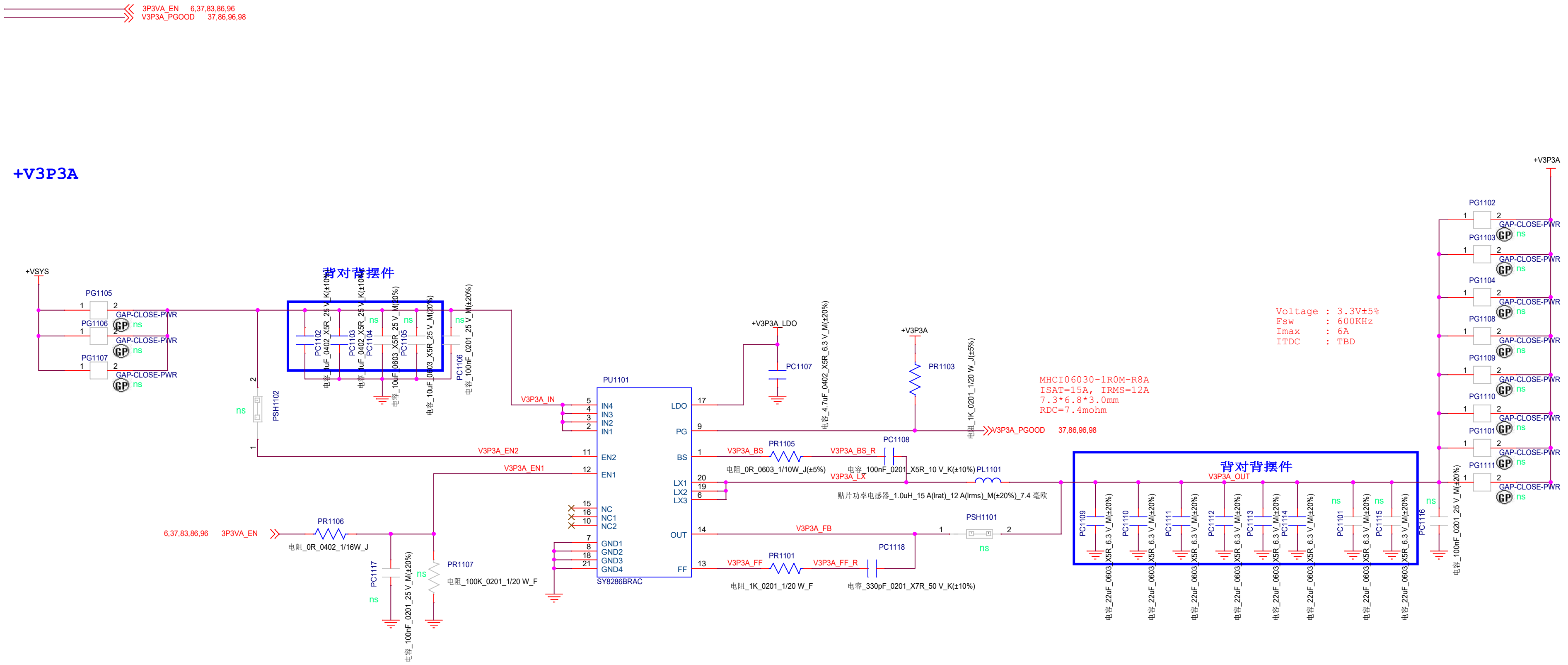

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Page name: POWER DELIVERY_V3P3A		
Size: A4	**Project Name:** NB2950-JSL	**REV:** V1.0
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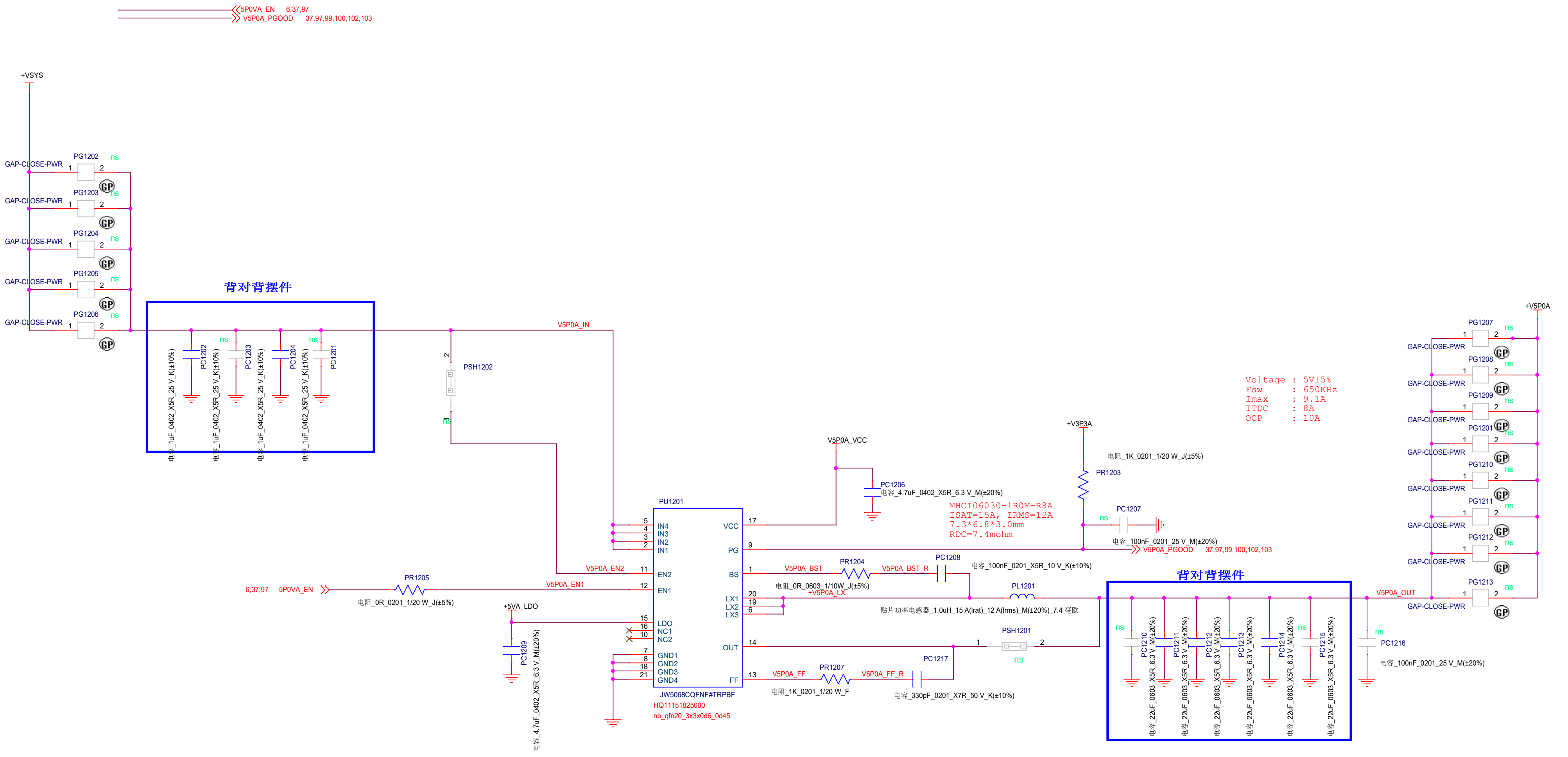

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Page name: POWER DELIVERY_5V

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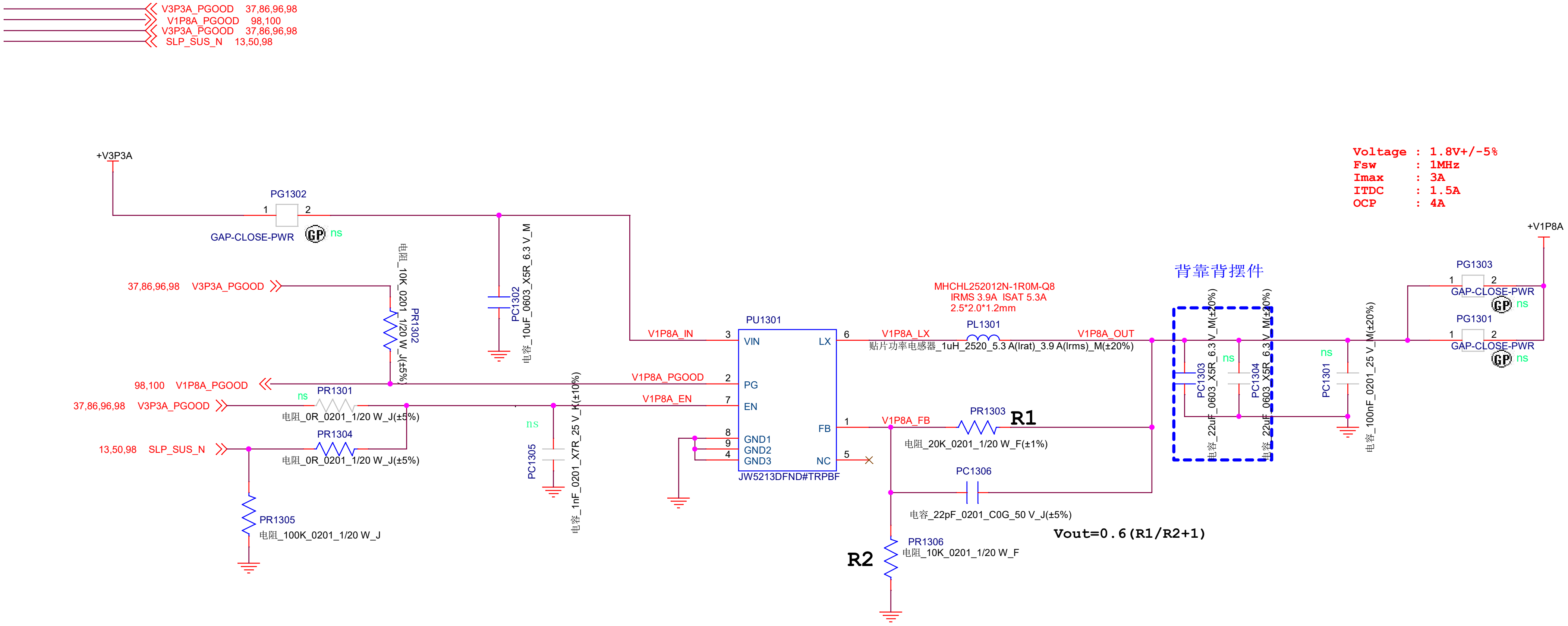

Voltage : 1.8V+/-5%
Fsw : 1MHz
Imax : 3A
ITDC : 1.5A
OCP : 4A

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Page name: POWER DELIVERY_V1P8A

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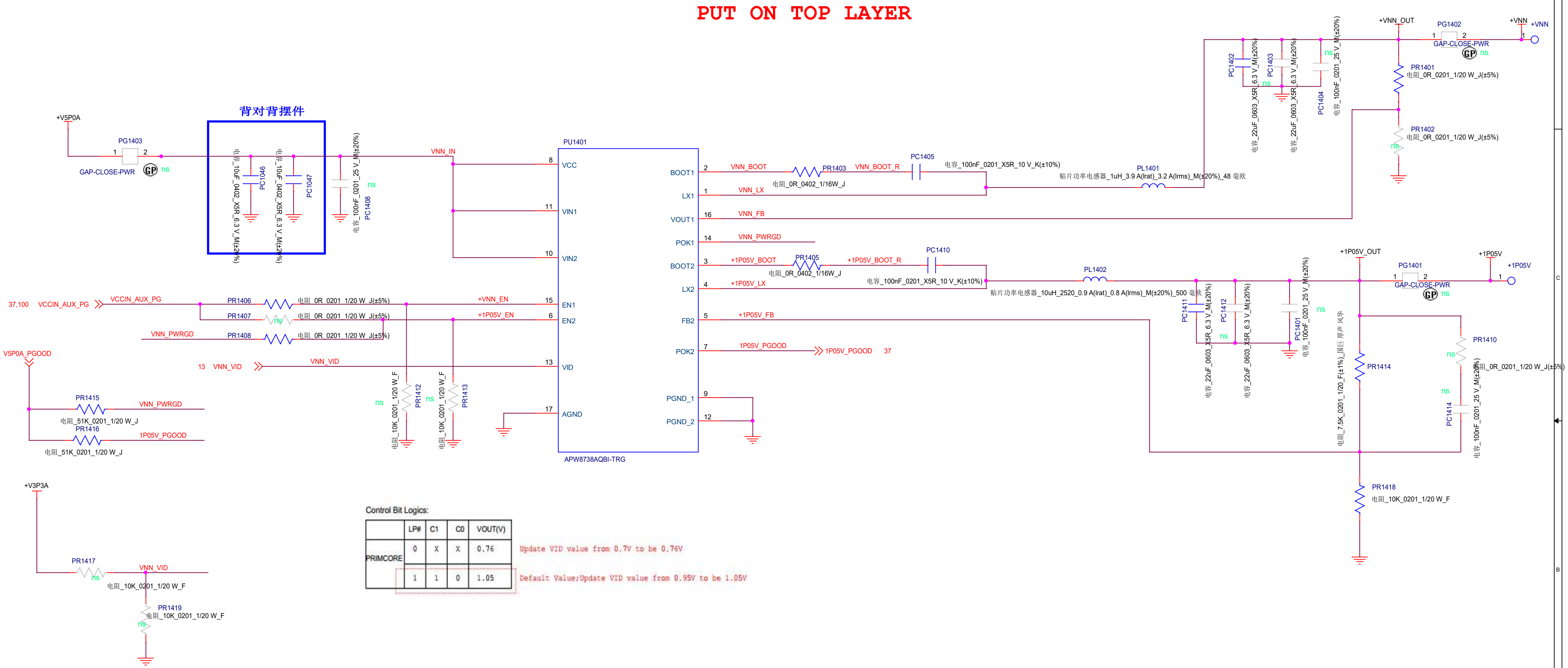
PUT ON TOP LAYER



Control Bit Logics:

	LP#	C1	C0	VOUT(V)
PRIMCORE	0	X	X	0.76
	1	1	0	1.05

Update VID value from 0.7V to be 0.76V

Default Value;Update VID value from 0.95V to be 1.05V

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Page name: **POWER VNN&1P05V**

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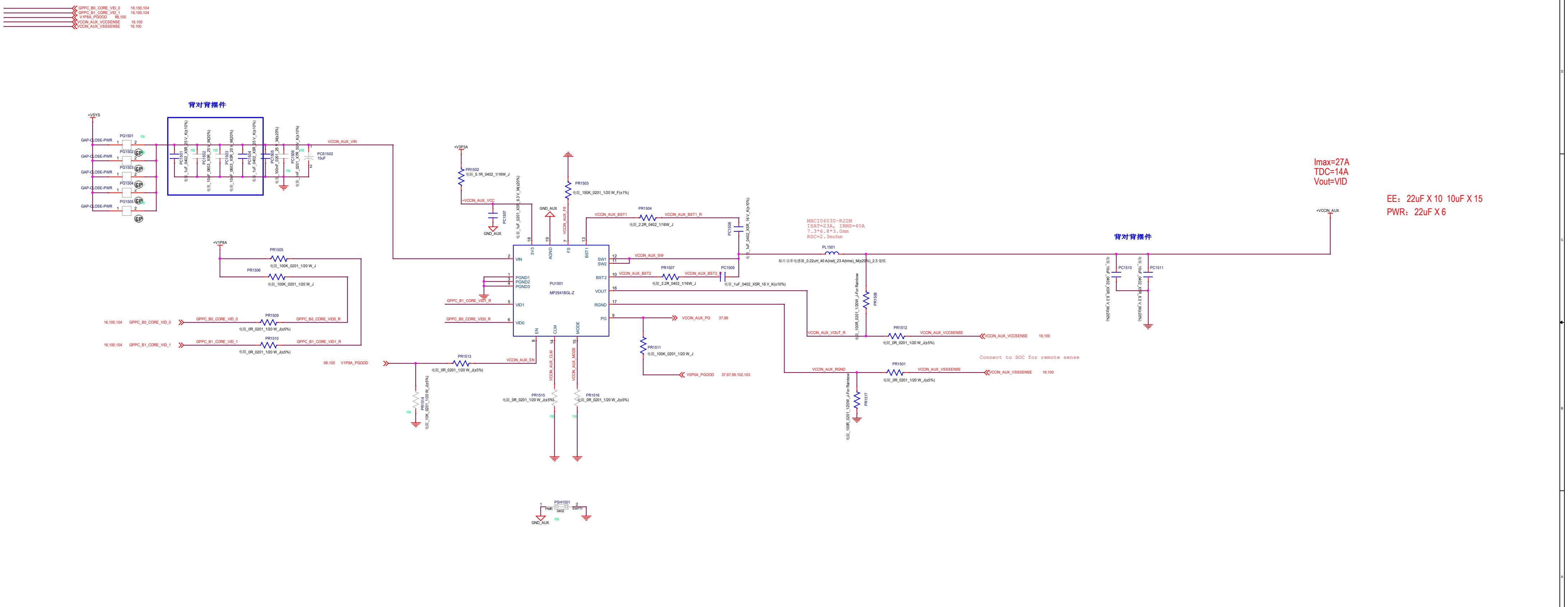

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Page name:	POWER DELIVERY VCCIN AUX	
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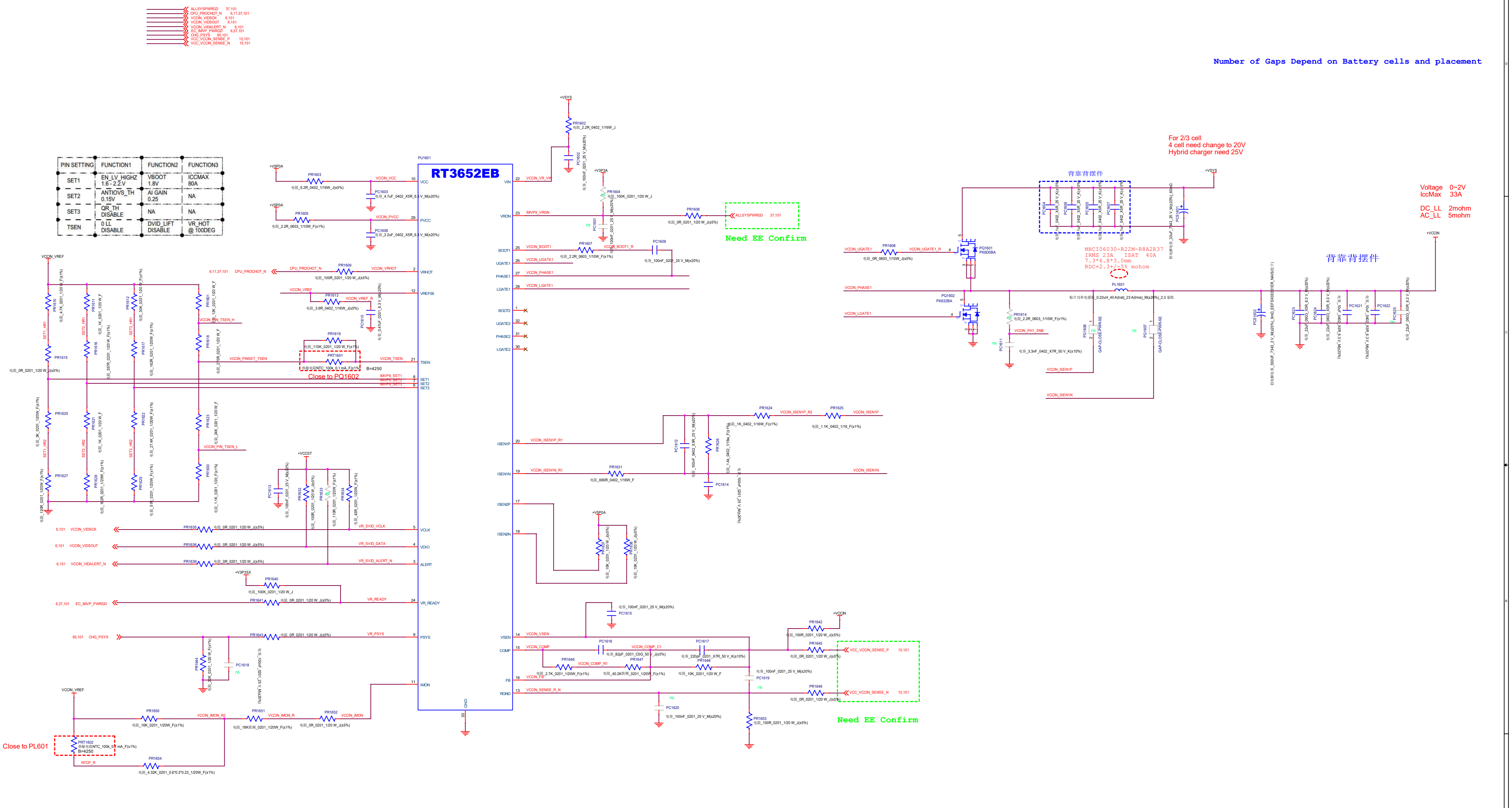
Number of Gaps Depend on Battery cells and placement

PIN SETTING	FUNCTION1	FUNCTION2	FUNCTION3
SET1	EN_LV_HIGHZ 1.6 - 2.2.V	VBOOT 1.8V	ICCMAX 80A
SET2	ANTIOVS_TH 0.15V	AI GAIN 0.25	NA
SET3	QR_TH DISABLE	NA	NA
TSEN	0 LL DISABLE	DVID_LIFT DISABLE	VR_HOT @ 100DEG



HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	POWER DELIVERY IMVP	
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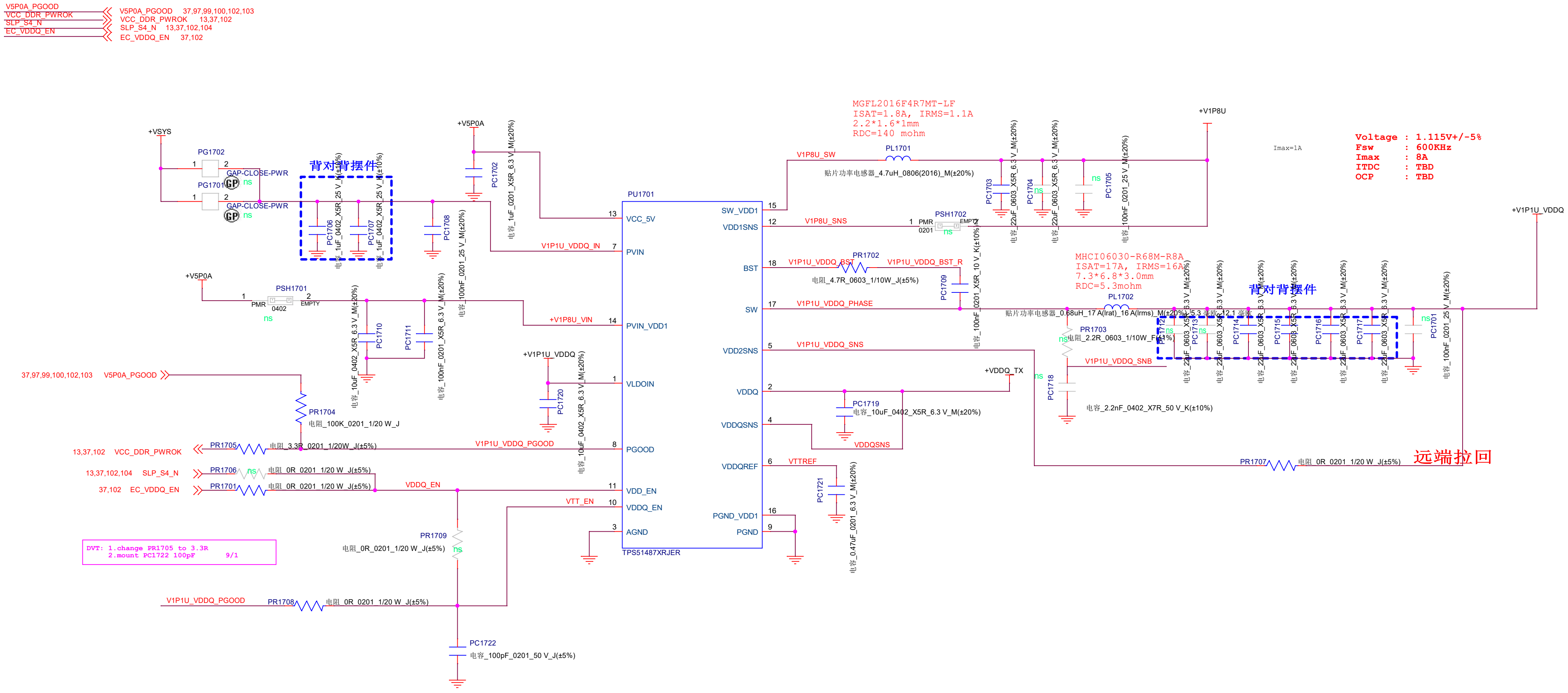

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Page name: **POWER DELIVERY_VDDQ**

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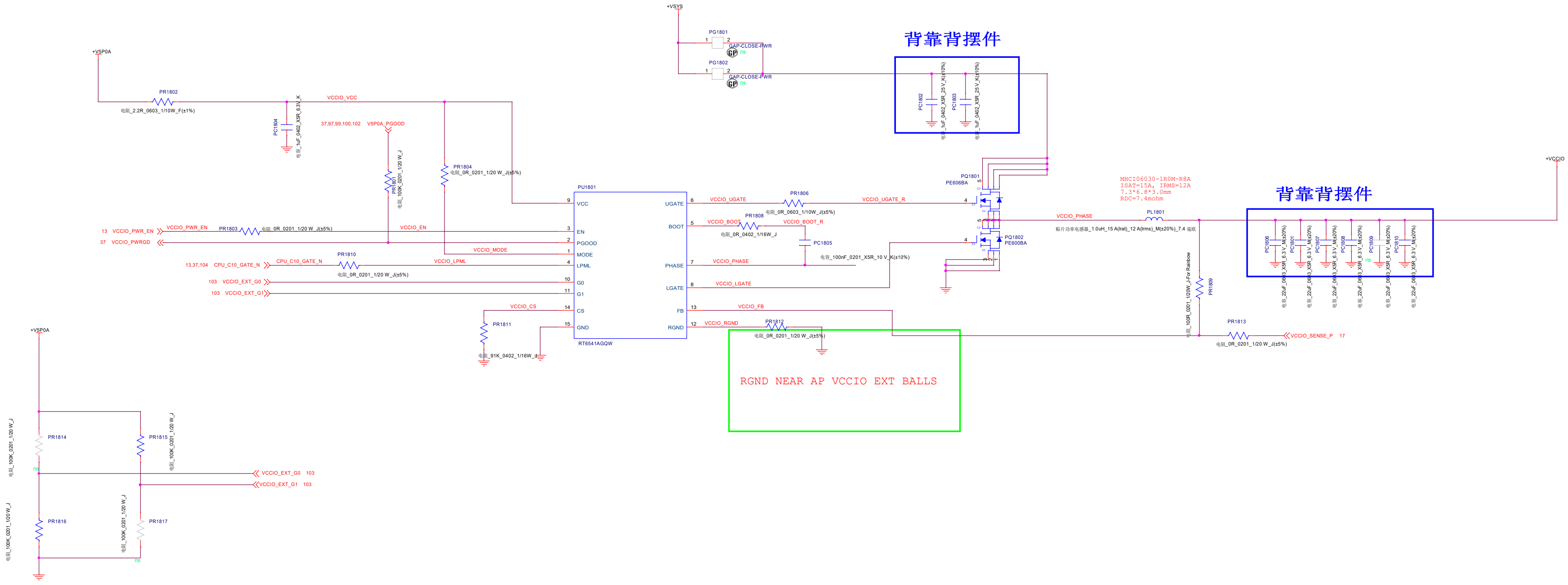

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Page name: POWER_VCCIO

Size: A4 Project Name: NB2950-JSL REV: V1.0

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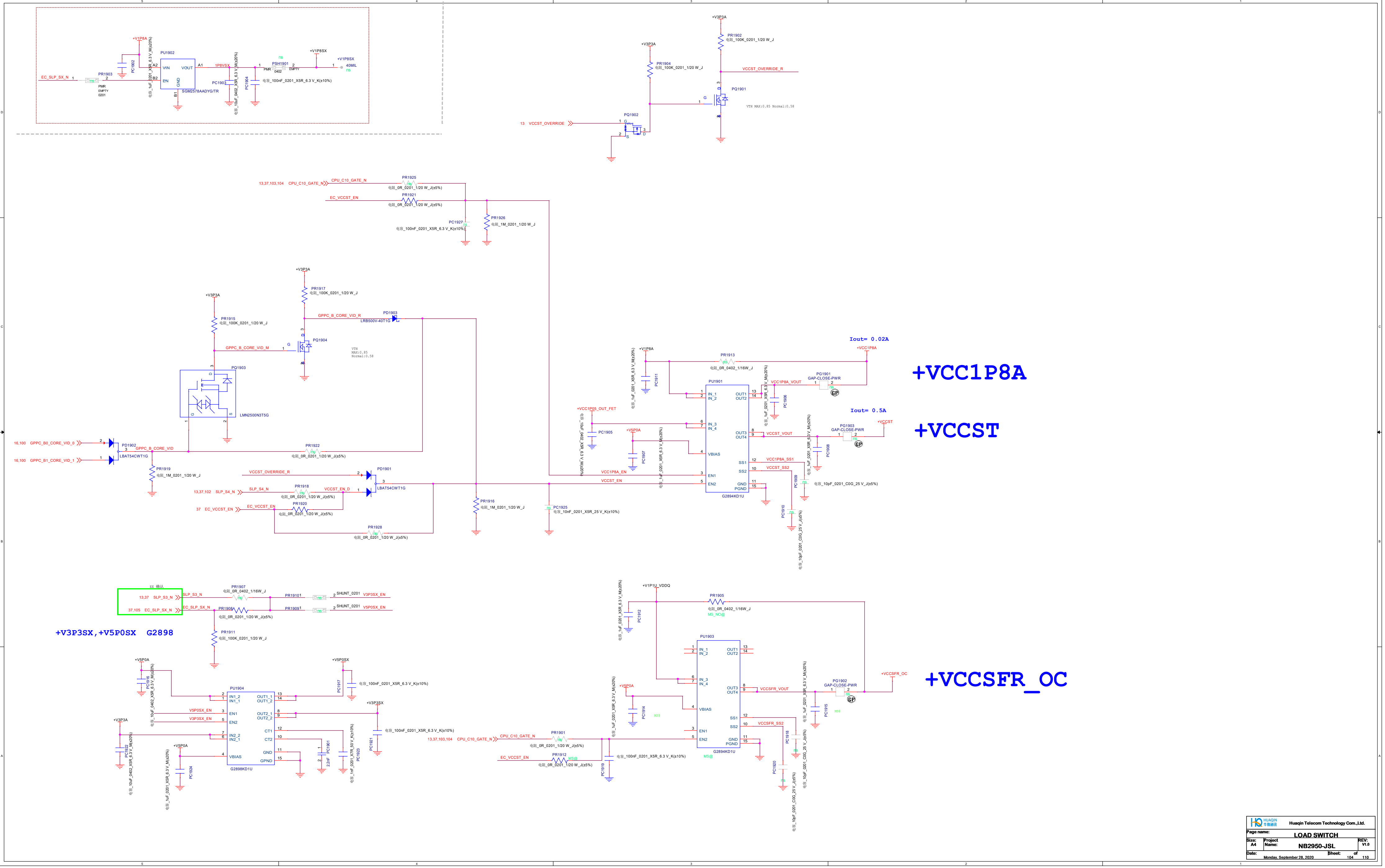

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Page name: LOAD SWITCH

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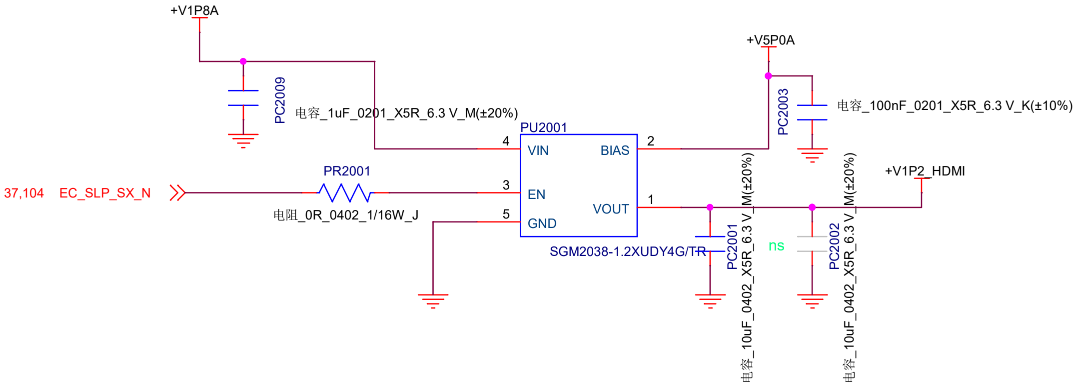

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Page name: **POWER_1P2V_HDMI**

Size: **A4**

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