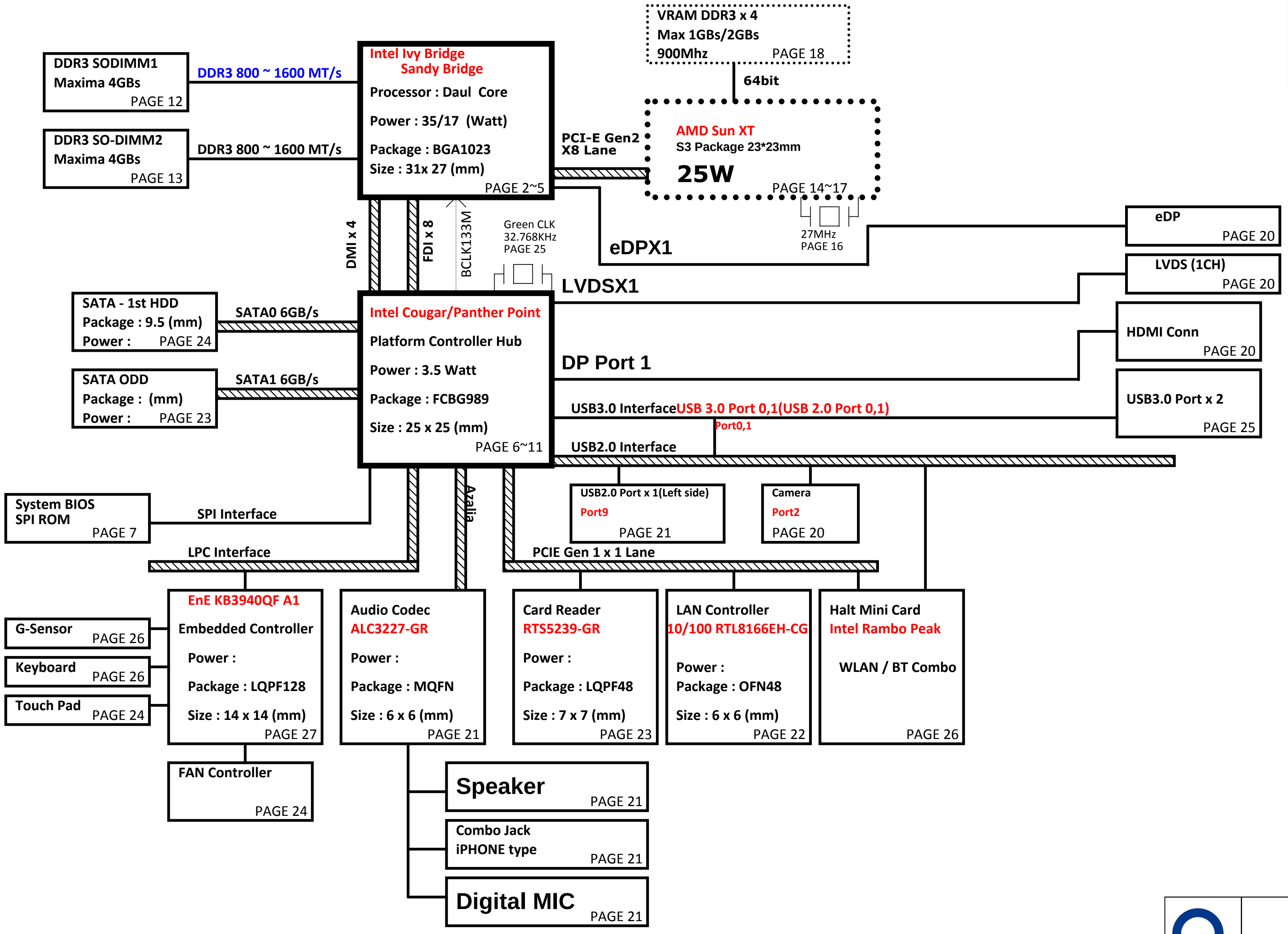
U81 DIS/UMA (14"/15.6") Ultra/Slim Intel Chief River Platform Block Diagram

PCB 6L STACK UP

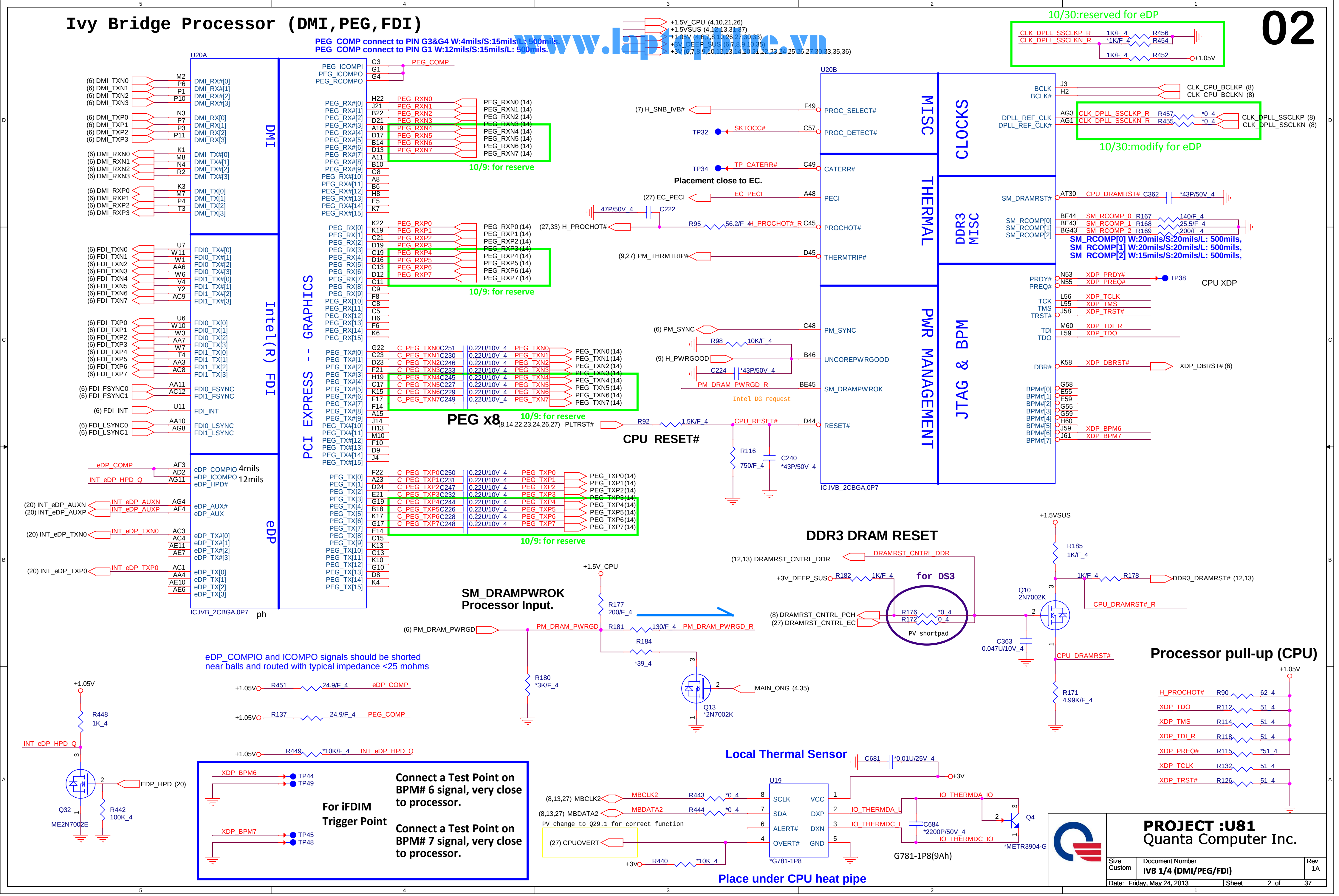
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



PROJECT :U81
Quanta Computer Inc.

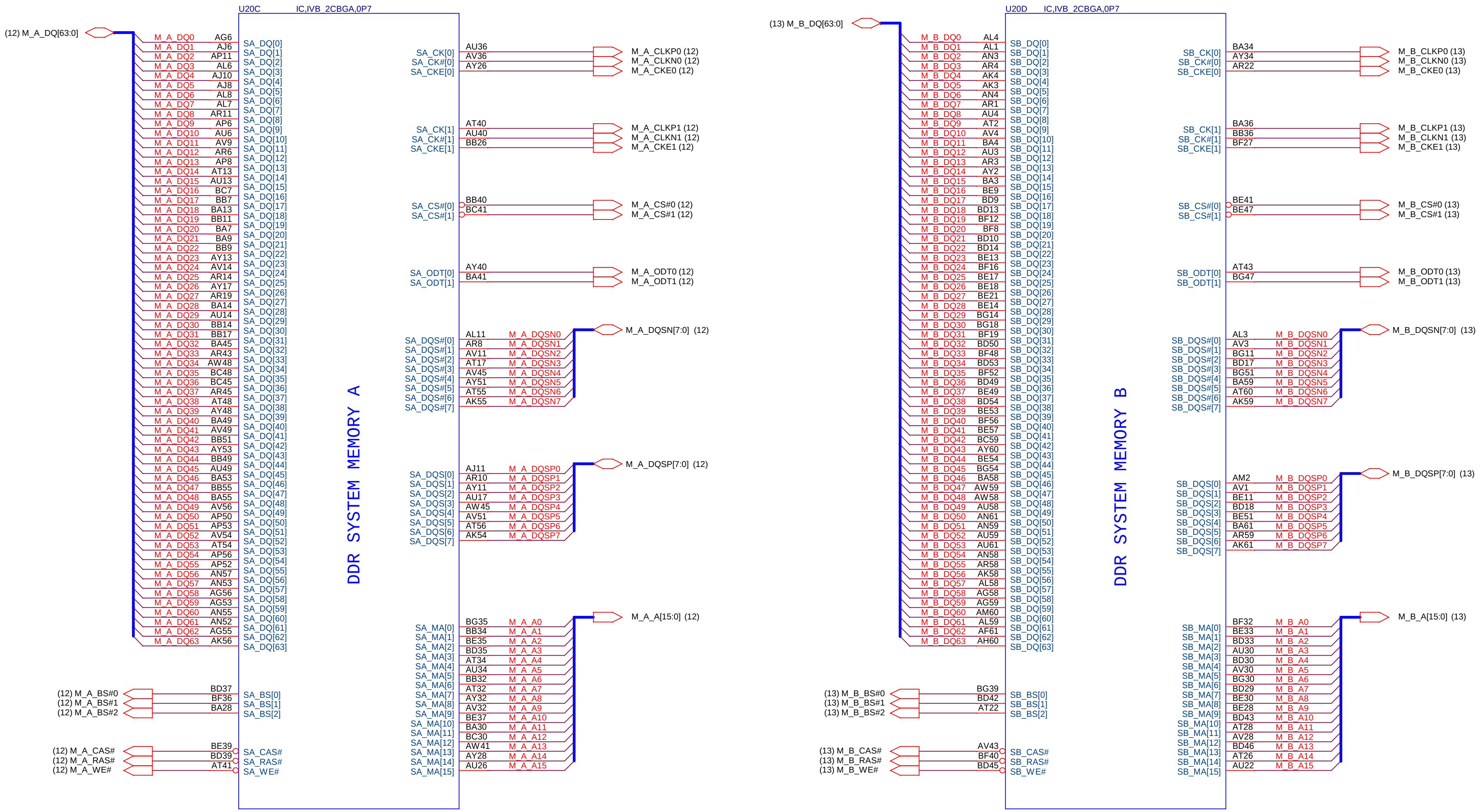
Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Friday, May 24, 2013 | Sheet 1 of 37



Ivy Bridge Processor (DMI,PEG,FDI)
02
www.laptopvic.vn
PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.
10/30:reserved for eDP
10/30:modify for eDP
U20A
U20B
DMI
Intel(R) FDI
eDP
PCI EXPRESS -- GRAPHICS
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
10/9: for reserve
PEG x8
Placement close to EC.
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,
CPU XDP
Intel DG request
CPU RESET#
IC,IVB_2CBGA,0P7
DDR3 DRAM RESET
for DS3
PV shortpad
SM_DRAMPWROK
Processor Input.
eDP_COMPIO and ICOMPO signals should be shorted
near balls and routed with typical impedance <25 mohms
4mils
12mils
Processor pull-up (CPU)
Local Thermal Sensor
Place under CPU heat pipe
For iFDIM
Trigger Point
Connect a Test Point on
BPM# 6 signal, very close
to processor.
Connect a Test Point on
BPM# 7 signal, very close
to processor.
PV change to Q29.1 for correct function
G781-1P8(9Ah)
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number
IVB 1/4 (DMI/PEG/FDI)
Rev 1A
Date: Friday, May 24, 2013
Sheet 2 of 37

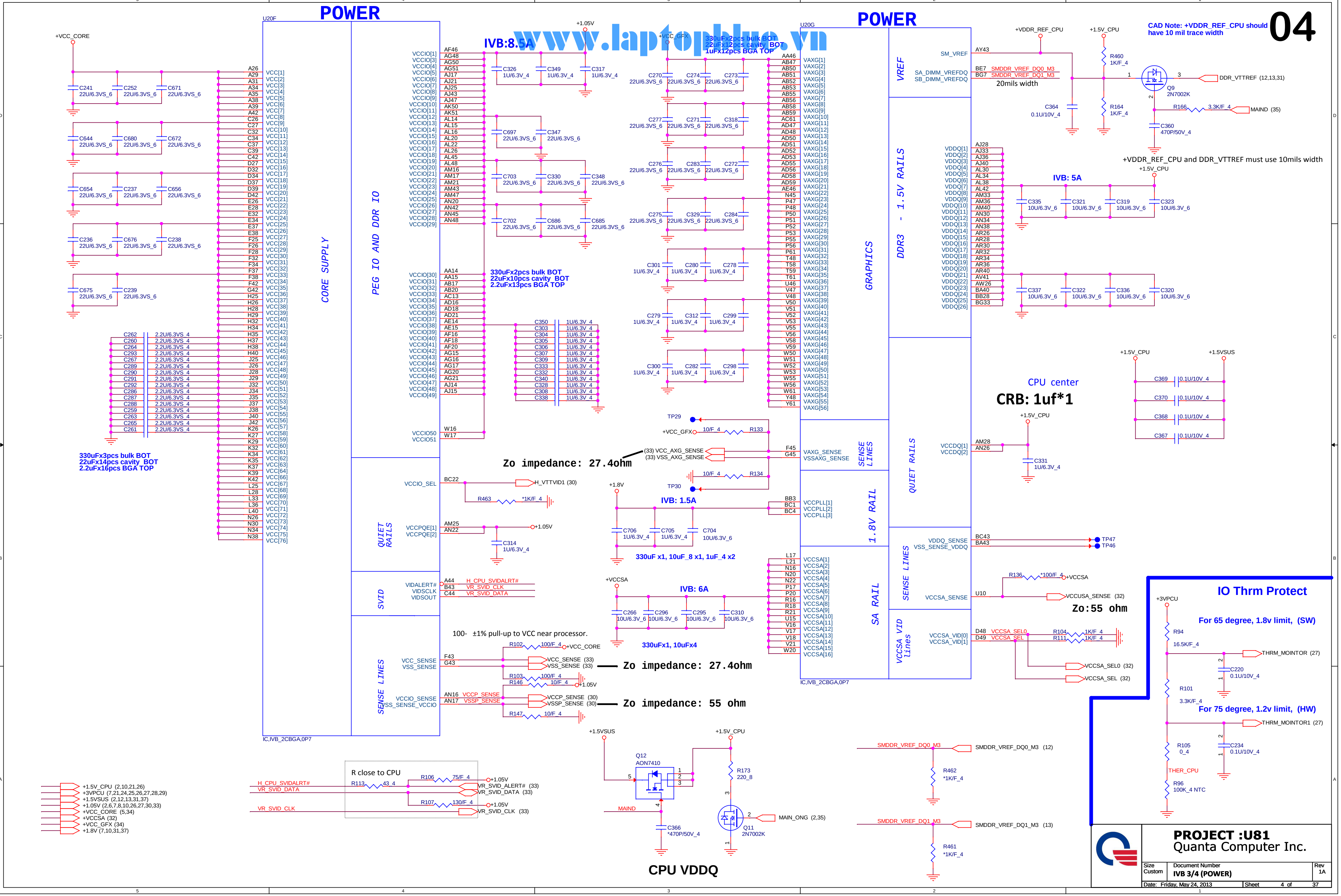
Ivy Bridge Processor (DDR3)



PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IVB 2/4 (DDR3 I/F)	1A

Date: Friday, May 24, 2013 | Sheet 3 of 37


POWER
U20F
CORE SUPPLY
PEG IO AND DDR IO
+VCC_CORE
+1.05V
IVB:8.5A
330uFx2pcs bulk BOT
22uFx10pcs cavity_BOT
2.2uFx13pcs BGA TOP
330uFx3pcs bulk BOT
22uFx14pcs cavity_BOT
2.2uFx16pcs BGA TOP
QUIET RAILS
SVID
SENSE LINES
VCCIO_SEL
H_VTTVID1 (30)
VCCPQE[1]
VCCPQE[2]
VIDALERT#
VIDSCLK
VIDSOUT
H_CPU_SVIDALRT#
VR_SVID_CLK
VR_SVID_DATA
100- ±1% pull-up to VCC near processor.
VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSS_SENSE_VCCIO
VCCP_SENSE (30)
VSSP_SENSE (30)
Zo impedance: 27.4ohm
Zo impedance: 55 ohm
IC,IVB_2CBGA,0P7
POWER
U20G
+VCC_GFX
330uFx2pcs bulk BOT
22uFx12pcs cavity_BOT
1uFx12pcs BGA TOP
GRAPHICS
VREF
DDR3 - 1.5V RAILS
SENSE LINES
1.8V RAIL
SA RAIL
VCCSA VID lines
QUIET RAILS
VAXG_SENSE
VSSAXG_SENSE
(33) VCC_AXG_SENSE
(33) VSS_AXG_SENSE
IVB: 1.5A
330uF x1, 10uF_8 x1, 1uF_4 x2
IVB: 6A
330uFx1, 10uFx4
+VCCSA
VCCSA_SENSE
VCCUSA_SENSE (32)
Zo:55 ohm
VCCSA_SEL0 (32)
VCCSA_SEL (32)
SM_VREF
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
SMDDR_VREF_DQ0_M3
SMDDR_VREF_DQ1_M3
20mils width
+VDDR_REF_CPU
+1.5V_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
DDR_VTTREF (12,13,31)
MAIND (35)
Q9 2N7002K
+VDDR_REF_CPU and DDR_VTTREF must use 10mils width
IVB: 5A
VDDQ_SENSE
VSS_SENSE_VDDQ
TP47
TP46
CPU center
CRB: 1uf*1
+1.5VSUS
IO Thrm Protect
+3VPCU
For 65 degree, 1.8v limit, (SW)
For 75 degree, 1.2v limit, (HW)
THRM_MOINTOR (27)
THRM_MOINTOR1 (27)
THER_CPU
R96 100K_4 NTC
SMDDR_VREF_DQ0_M3 (12)
SMDDR_VREF_DQ1_M3 (13)
Q12 AON7410
Q11 2N7002K
MAIN_ONG (2,35)
MAIND
CPU VDDQ
R close to CPU
H_CPU_SVIDALRT# (33)
VR_SVID_DATA (33)
VR_SVID_CLK (33)
+1.5V_CPU (2,10,21,26)
+3VPCU (7,21,24,25,26,27,28,29)
+1.5VSUS (2,12,13,31,37)
+1.05V (2,6,7,8,10,26,27,30,33)
+VCC_CORE (5,34)
+VCCSA (32)
+VCC_GFX (34)
+1.8V (7,10,31,37)
04
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number IVB 3/4 (POWER)
Rev 1A
Date: Friday, May 24, 2013
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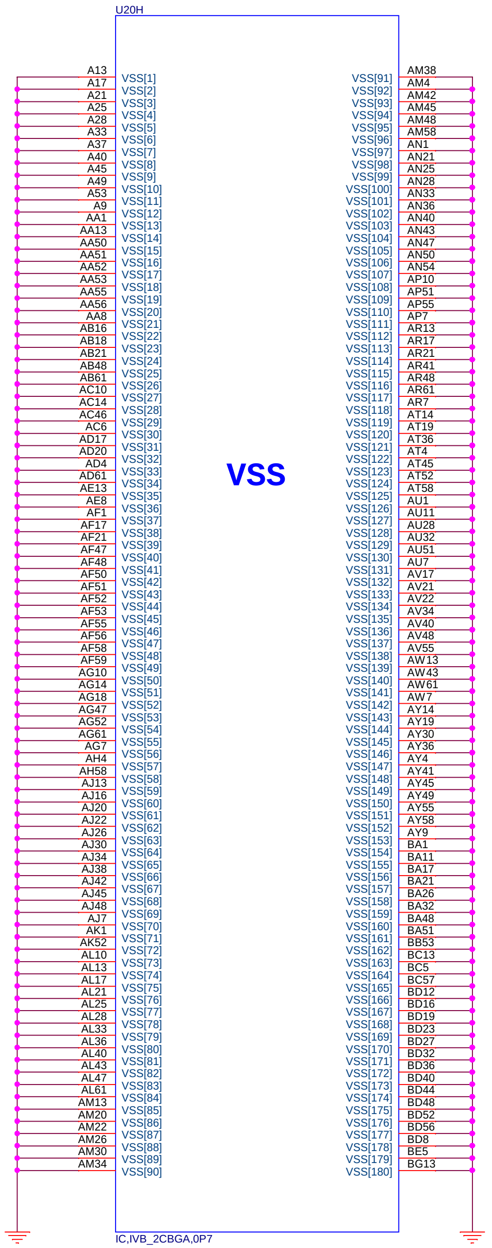
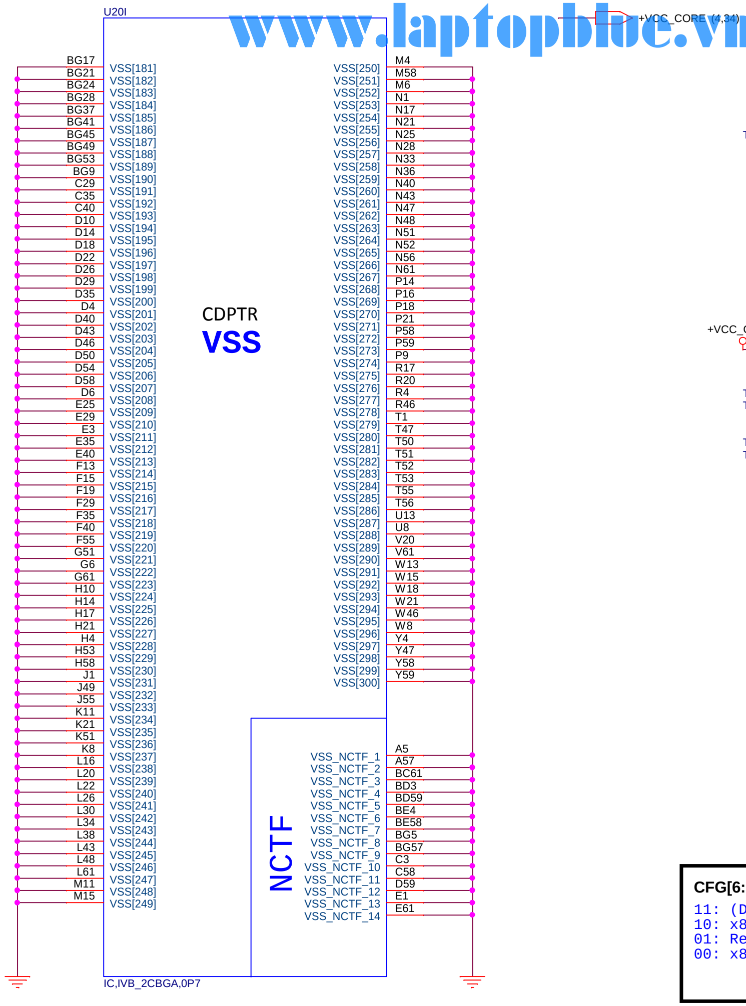
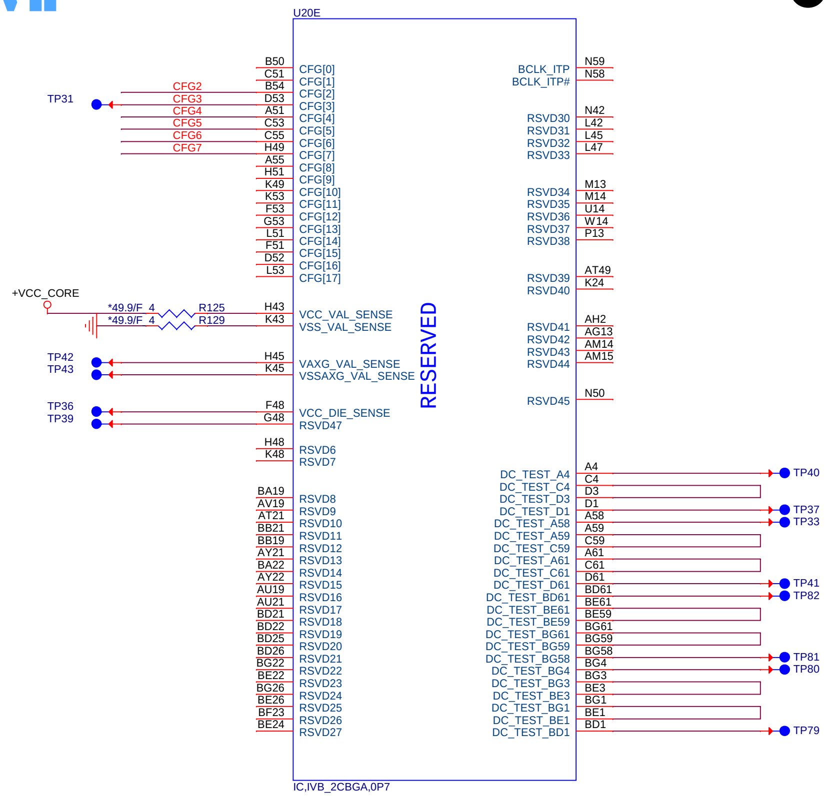
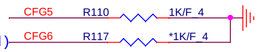






CFG[6:5] (PCIE Port Bifurcation Straps)

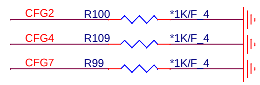
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



PROJECT :U81
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Size	Document Number	Rev
Custom	IVB 4/4 (RSV,GND)	1A

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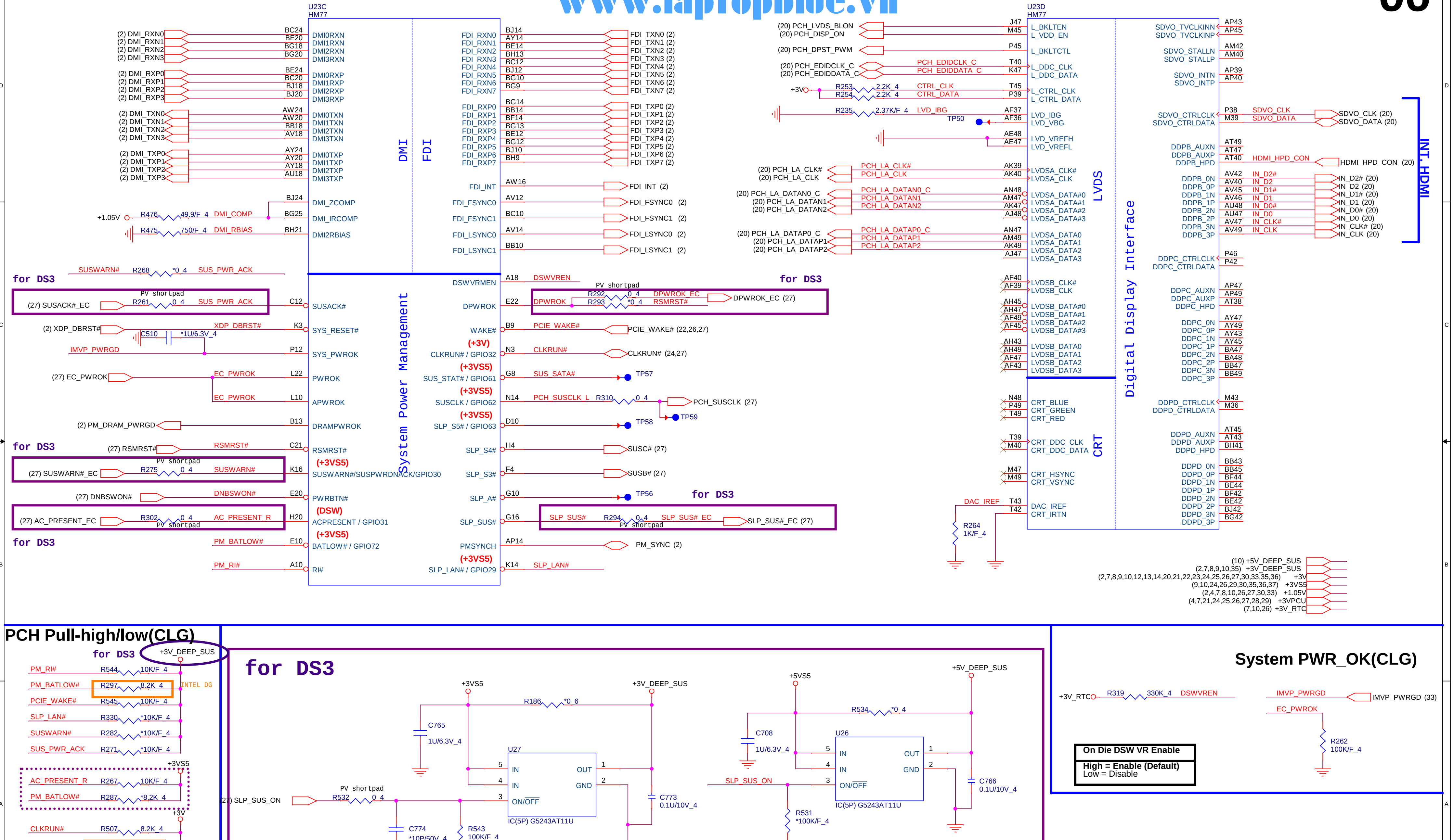
Cougar Point/Panther Point (DMI,FDI,PM)

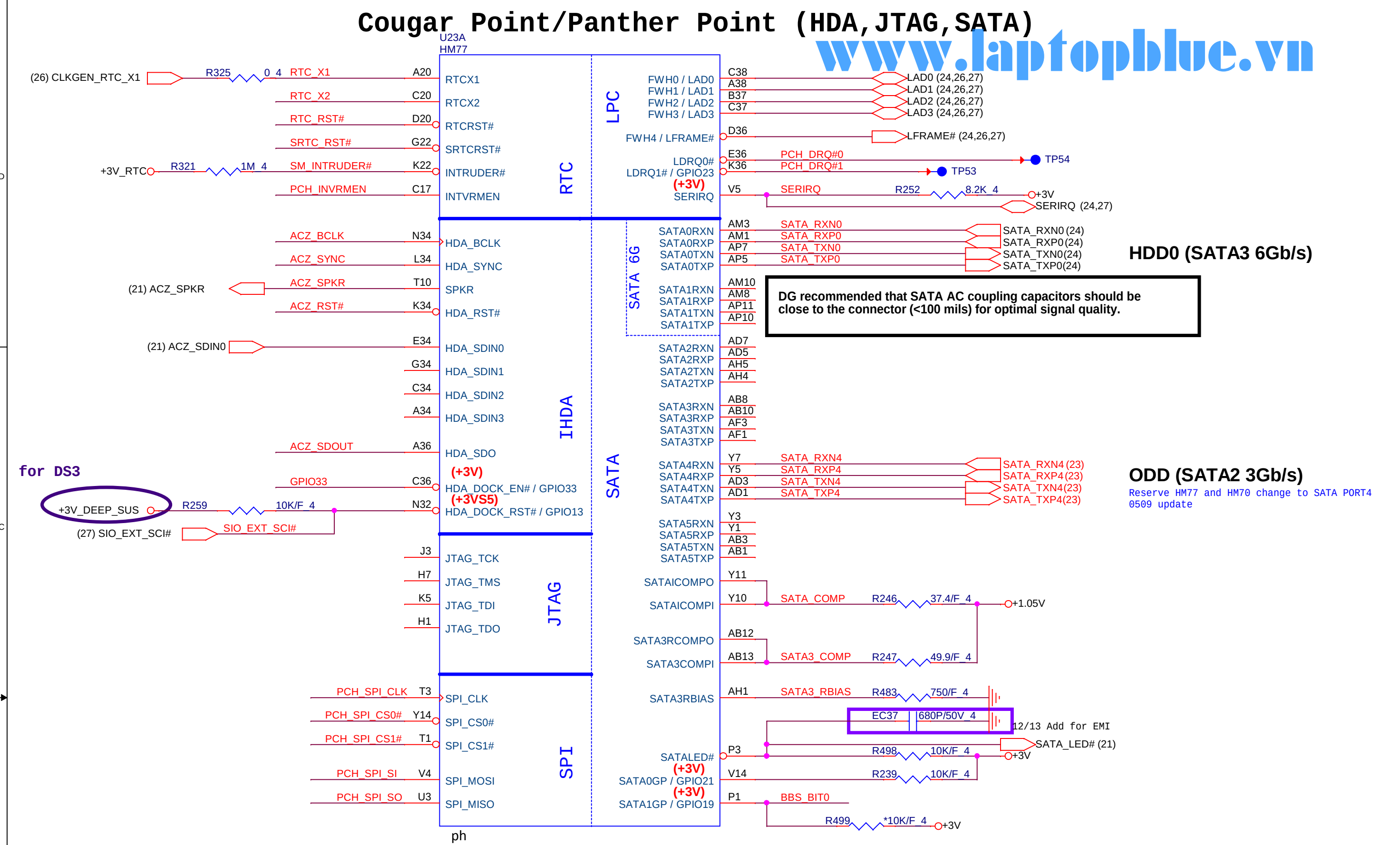
Cougar Point/Panther Point (LVDS,DDI)

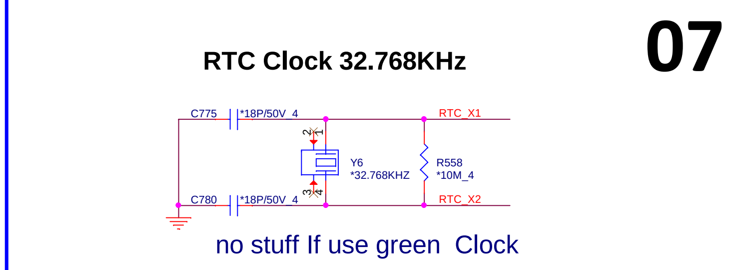


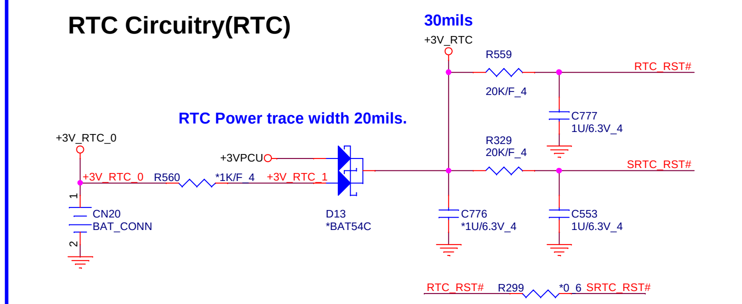
PROJECT :U81
Quanta Computer Inc.

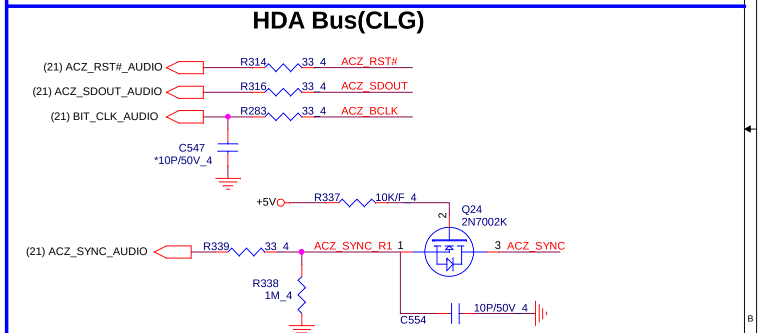
Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Friday, May 24, 2013	Sheet 6 of 37	

Cougar Point/Panther Point (HDA,JTAG,SATA)



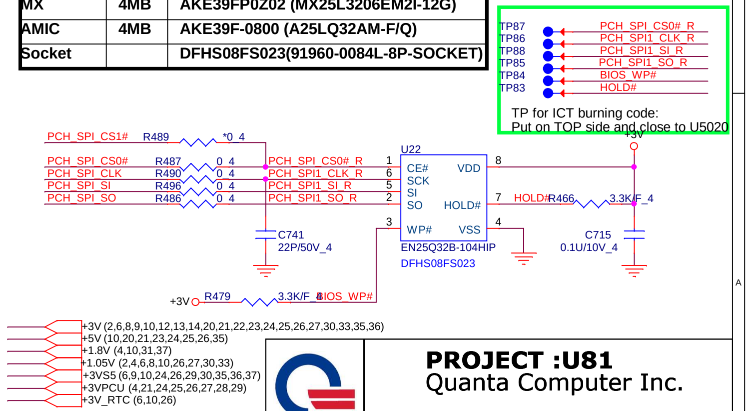






Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023(91960-0084L-8P-SOCKET)

PCH SPI ROM(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R237 *1K/F_4 ACZ_SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R529 *1K/F_4, R527 10K/F_4, PCI_GNT3# (8)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R320 330K_4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	BIOS_WP# R471 0_4 GPIO33
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 0 0 LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# R502 *1K/F_4 BBS_BIT0 R517 *1K/F_4 BBS_BIT1 (8)
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R472 *1K/F_4 NV_ALE (8)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R473 2.2K_4 R474 1K/F_4 NV_CLE (9), H_SNB_IVB# (2)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	for DS3 +3V_DEEP_SUS R335 1K/F_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V_DEEP_SUS R322 *1K/F_4 ACZ_SDOUT R313 0_4 GPIO33_EC (27)
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

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Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
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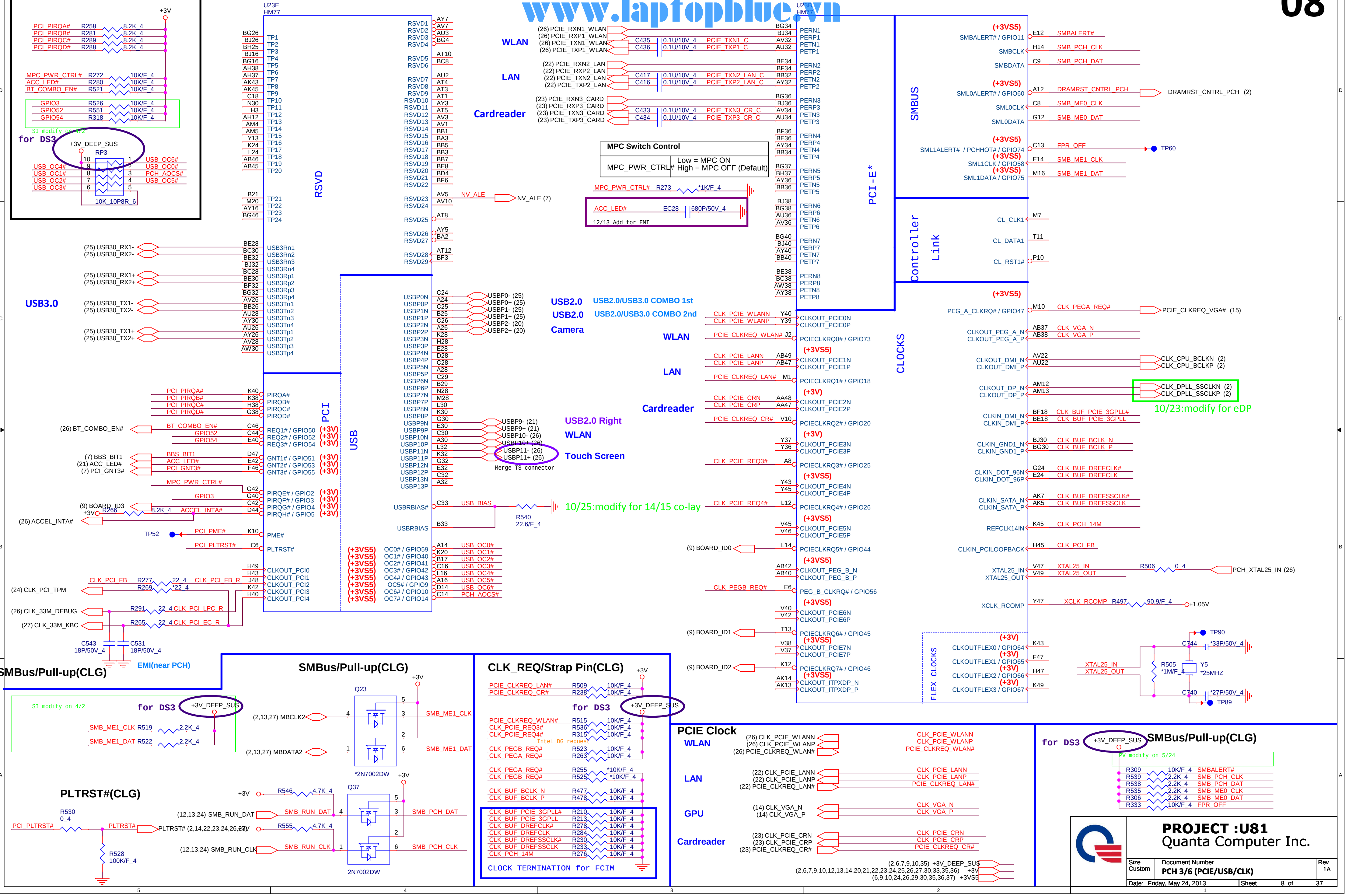
Cougar Point-M/Panther Point (PCI,USB,NVRAM)

Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08



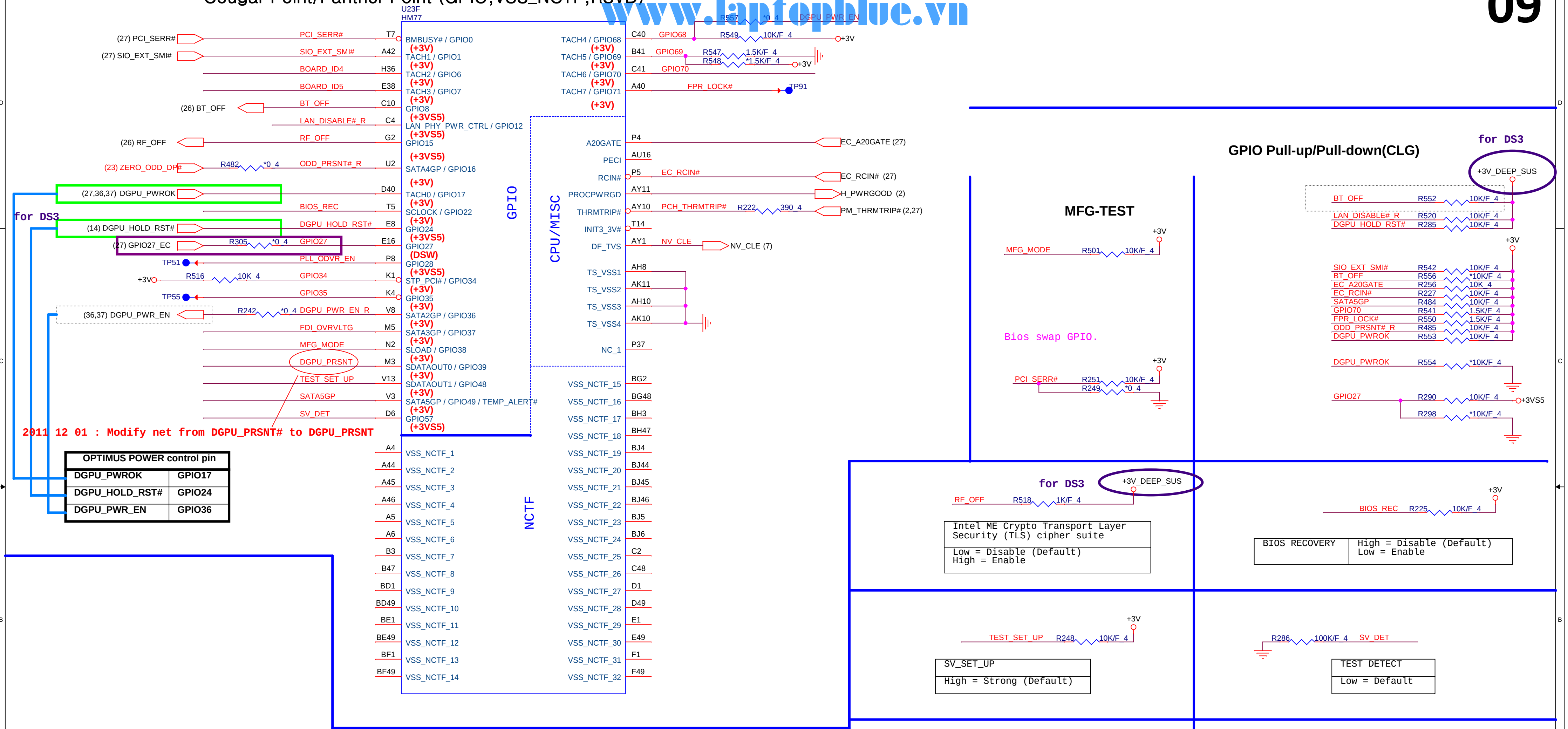
PROJECT :U81

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A

Date: Friday, May 24, 2013 Sheet 8 of 37

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

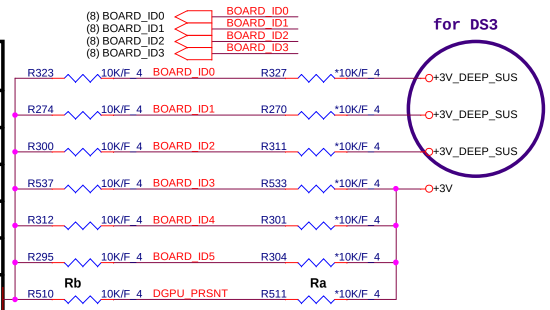
TEST DETECT
Low = Default

SATA2GP/GPIO36	Reserved only

FDI TERMINATION VOLTAGE OVERRIDE	Reserved only

Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4 14": 0 15": 1	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0 UMA: 0 DIS: 1
U81 UMA	0	0	0	0	0	0
U81 SWG	0	0	0	0	0	1
14"	0	0	0	0	0	0
15.6"	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

(2,6,7,8,10,35) +3V_DEEP_SUS
(2,6,7,8,10,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36) +3V
(6,10,24,26,29,30,35,36,37) +3VS5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

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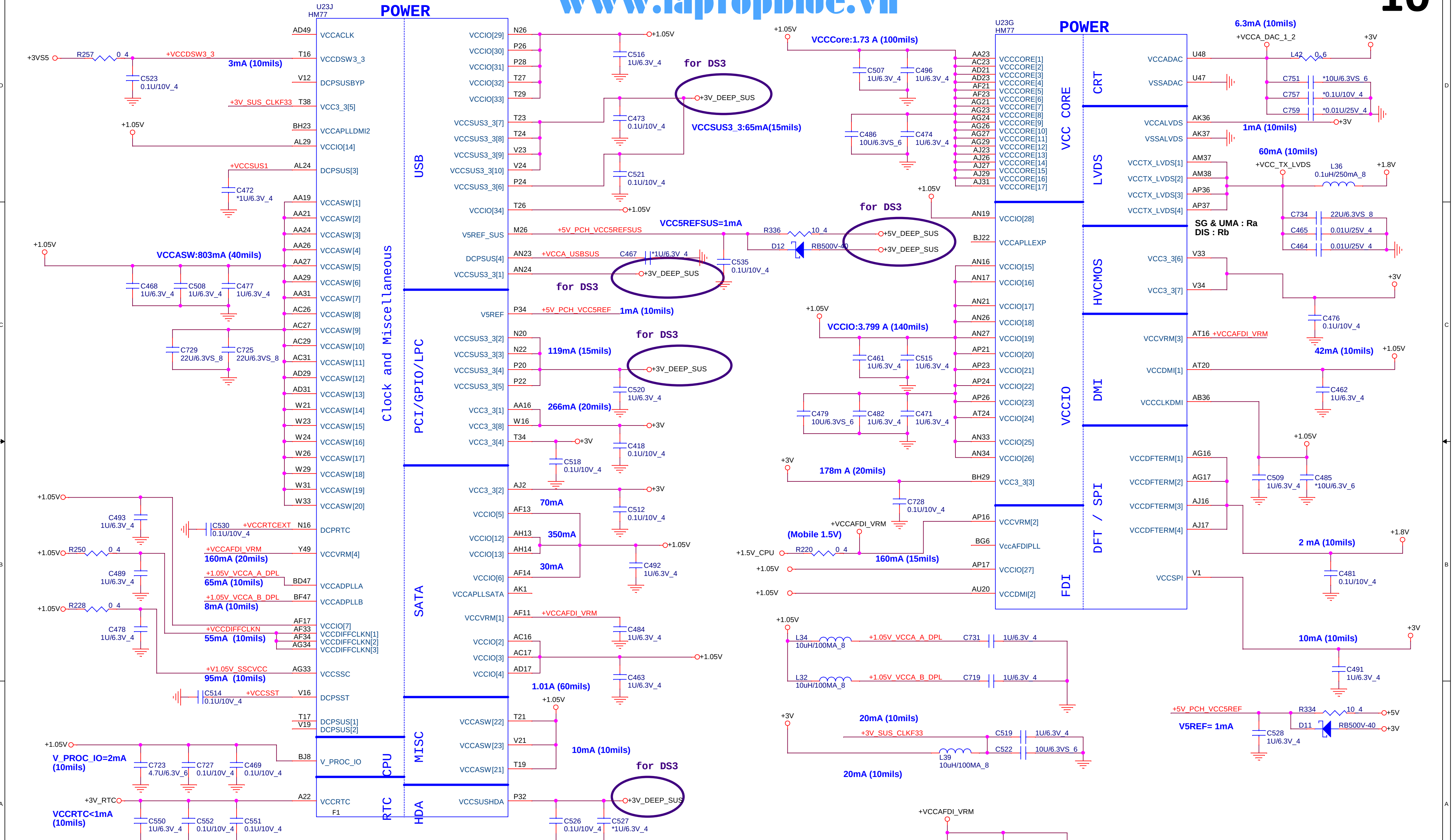

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Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

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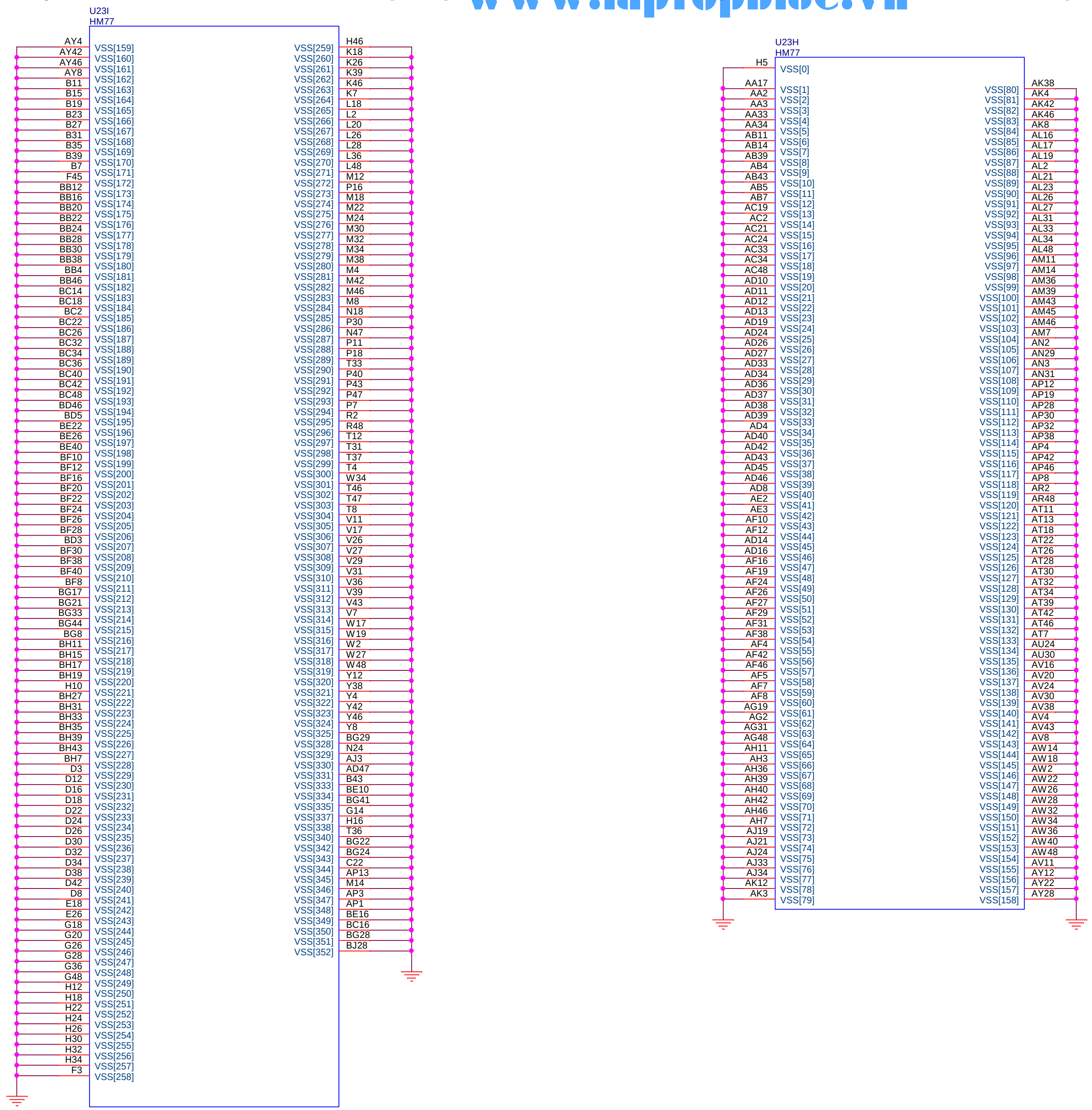
Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)



PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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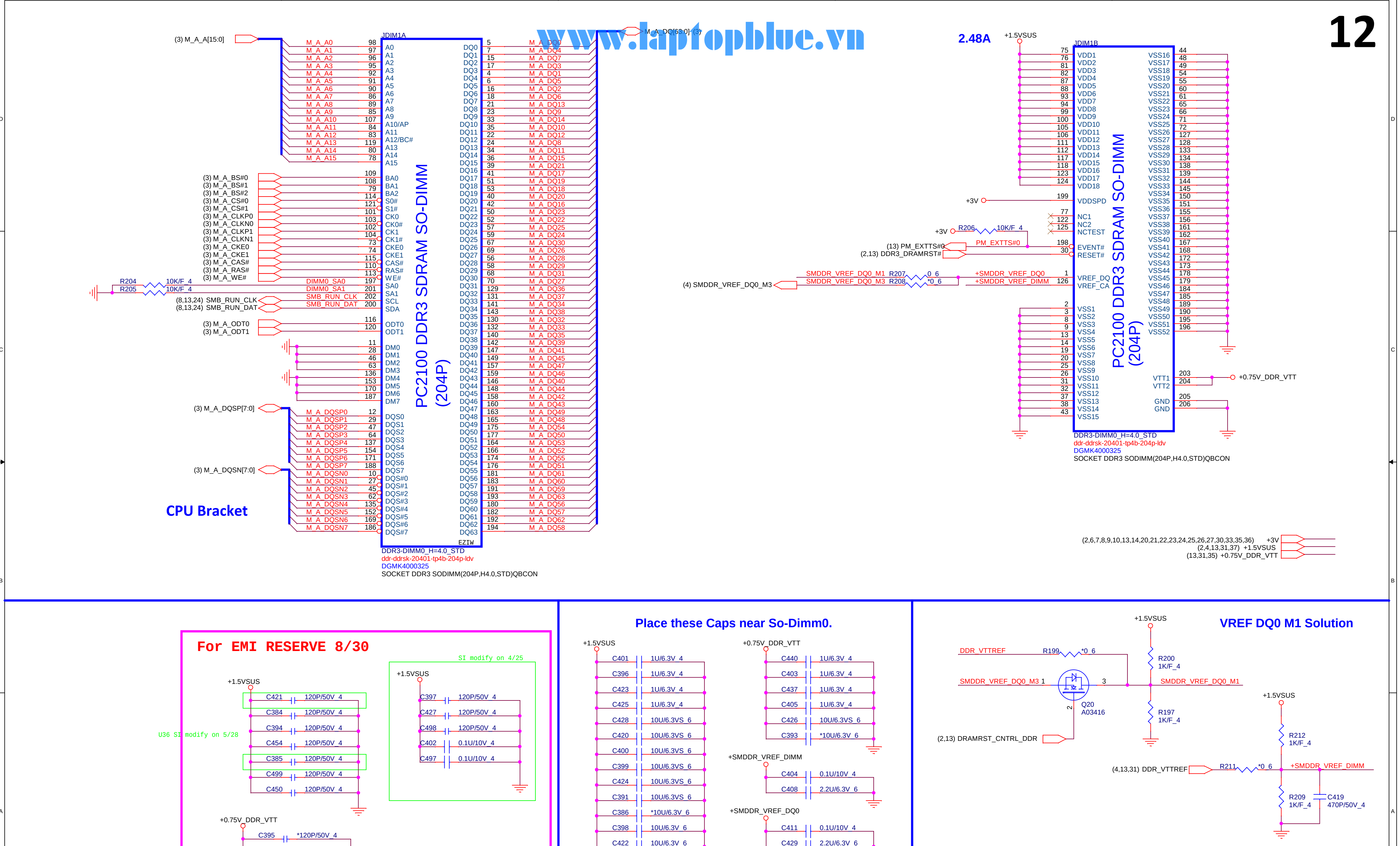
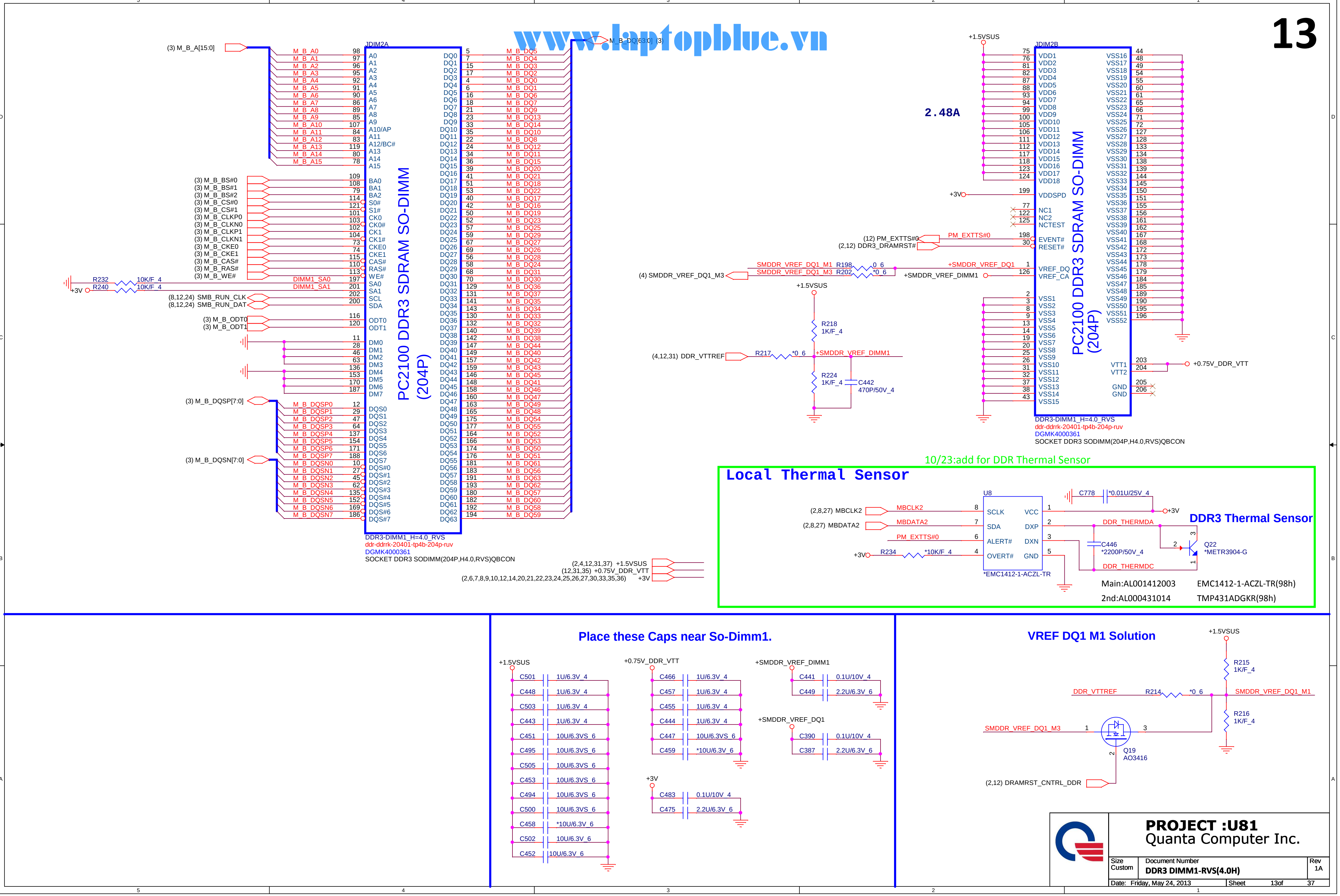


PROJECT :U81 Quanta Computer Inc.		
Size Custom	Document Number DDR3 DIMM0-STD(4.0H)	Rev 1A
Date: Friday, May 24, 2013	Sheet 12 of 37	



www.laptopblue.vn
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
(3) M_B_A[15:0]
(3) M_B_DQ[63:0]
(3) M_B_BS#0
(3) M_B_BS#1
(3) M_B_BS#2
(3) M_B_CS#0
(3) M_B_CS#1
(3) M_B_CLKP0
(3) M_B_CLKN0
(3) M_B_CLKP1
(3) M_B_CLKN1
(3) M_B_CKE0
(3) M_B_CKE1
(3) M_B_CAS#
(3) M_B_RAS#
(3) M_B_WE#
R232 10K/F_4
R240 10K/F_4
DIMM1_SA0
DIMM1_SA1
(8,12,24) SMB_RUN_CLK
(8,12,24) SMB_RUN_DAT
(3) M_B_ODT0
(3) M_B_ODT1
(3) M_B_DQSP[7:0]
(3) M_B_DQSN[7:0]
DDR3-DIMM1_H=4.0_RVS
ddr-ddrrk-20401-tp4b-204p-ruv
DGMK4000361
SOCKET DDR3 SODIMM(204P,H4.0,RVS)QBCON
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
+1.5VSUS
2.48A
+3V
(12) PM_EXTTS#0
(2,12) DDR3_DRAMRST#
PM_EXTTS#0
SMDDR_VREF_DQ1_M1 R198 0_6
SMDDR_VREF_DQ1_M3 R202 *0_6
+SMDDR_VREF_DQ1
(4) SMDDR_VREF_DQ1_M3
+SMDDR_VREF_DIMM1
R218 1K/F_4
(4,12,31) DDR_VTTREF
R217 *0_6
R224 1K/F_4
C442 470P/50V_4
+0.75V_DDR_VTT
DDR3-DIMM1_H=4.0_RVS
ddr-ddrrk-20401-tp4b-204p-ruv
DGMK4000361
SOCKET DDR3 SODIMM(204P,H4.0,RVS)QBCON
(2,4,12,31,37) +1.5VSUS
(12,31,35) +0.75V_DDR_VTT
(2,6,7,8,9,10,12,14,20,21,22,23,24,25,26,27,30,33,35,36) +3V
10/23:add for DDR Thermal Sensor
Local Thermal Sensor
U8
C778 *0.01U/25V_4
(2,8,27) MBCLK2
(2,8,27) MBDATA2
MBCLK2
MBDATA2
PM_EXTTS#0
R234 *10K/F_4
SCLK VCC
SDA DXP
ALERT# DXN
OVERT# GND
*EMC1412-1-ACZL-TR
DDR3 Thermal Sensor
DDR_THERMDA
DDR_THERMDC
C446 *2200P/50V_4
Q22 *METR3904-G
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
Place these Caps near So-Dimm1.
C501 1U/6.3V_4
C448 1U/6.3V_4
C503 1U/6.3V_4
C443 1U/6.3V_4
C451 10U/6.3VS_6
C495 10U/6.3VS_6
C505 10U/6.3VS_6
C453 10U/6.3VS_6
C494 10U/6.3VS_6
C500 10U/6.3VS_6
C458 *10U/6.3V_6
C502 10U/6.3V_6
C452 10U/6.3V_6
C466 1U/6.3V_4
C457 1U/6.3V_4
C455 1U/6.3V_4
C444 1U/6.3V_4
C447 10U/6.3VS_6
C459 *10U/6.3V_6
C483 0.1U/10V_4
C475 2.2U/6.3V_6
+SMDDR_VREF_DIMM1
C441 0.1U/10V_4
C449 2.2U/6.3V_6
+SMDDR_VREF_DQ1
C390 0.1U/10V_4
C387 2.2U/6.3V_6
VREF DQ1 M1 Solution
R215 1K/F_4
DDR_VTTREF R214 *0_6 SMDDR_VREF_DQ1_M1
R216 1K/F_4
SMDDR_VREF_DQ1_M3
Q19 AO3416
(2,12) DRAMRST_CNTRL_DDR
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number DDR3 DIMM1-RVS(4.0H)
Rev 1A
Date: Friday, May 24, 2013
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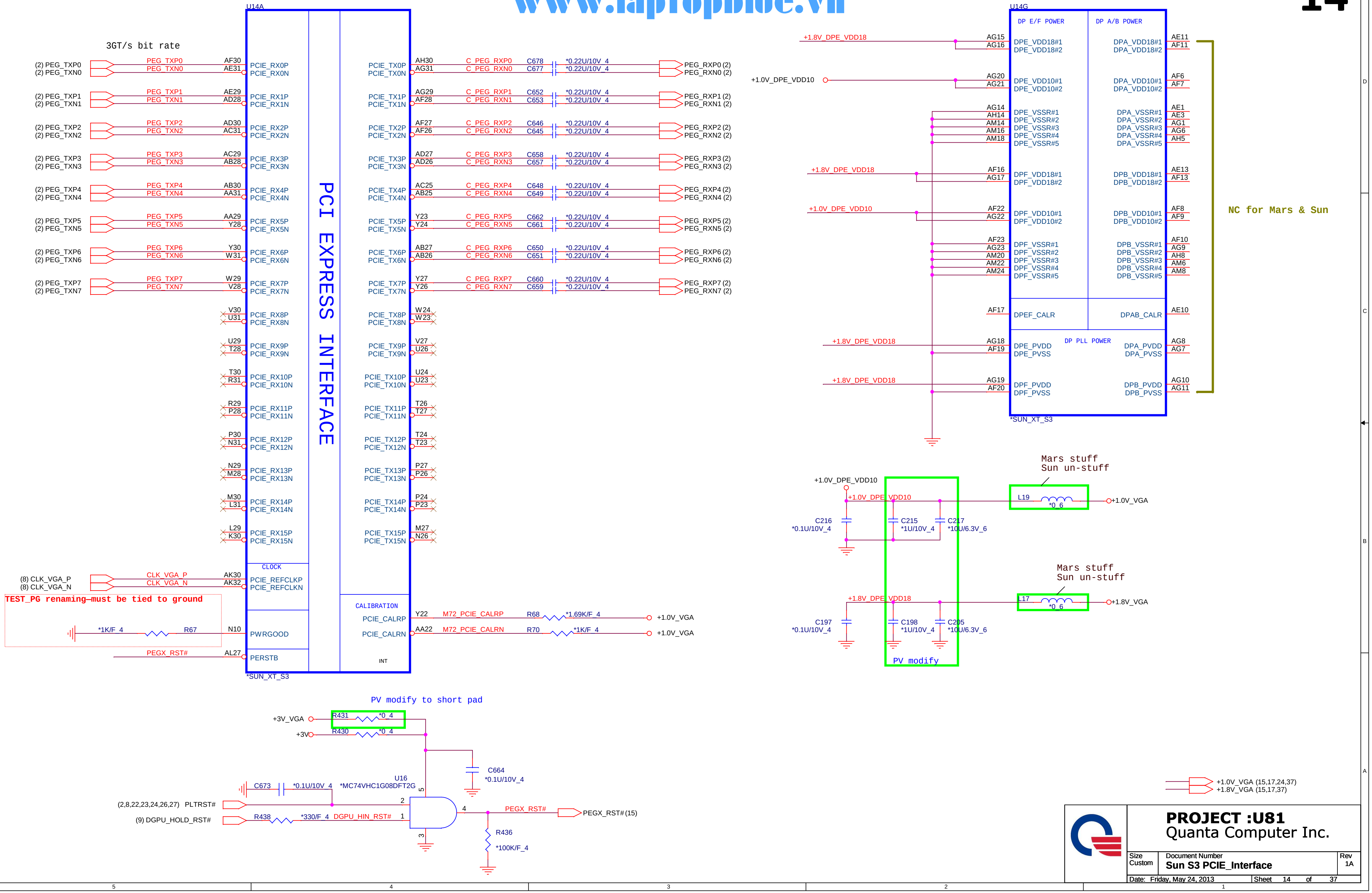

PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 PCIE_Interface	1A

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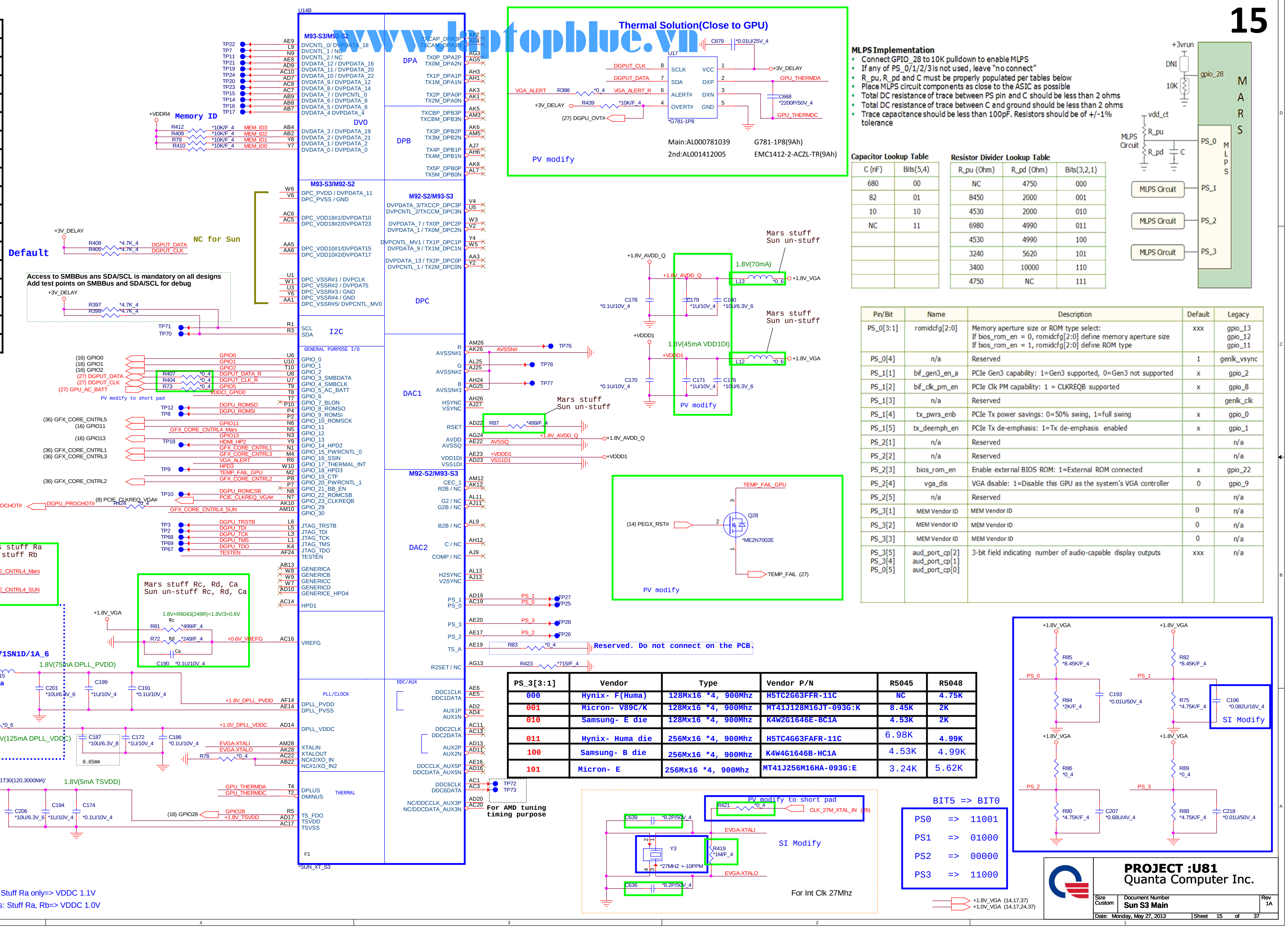
GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

PS_3[3:1]	Vendor	Type	Vendor P/N	R5045	R5048
000	Hynix- F(Huma)	128Mx16 *4, 900Mhz	H5TC2G63FFR-11C	NC	4.75K
001	Micron- V89C/K	128Mx16 *4, 900Mhz	MT41J128M16JT-093G:K	8.45K	2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4W2G1646E-BC1A	4.53K	2K
011	Hynix- Huma die	256Mx16 *4, 900Mhz	H5TC4G63FAFR-11C	6.98K	4.99K
100	Samsung- B die	256Mx16 *4, 900Mhz	K4W4G1646B-HC1A	4.53K	4.99K
101	Micron- E	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K	5.62K

BIT5 => BIT0

PS0	=>	11001
PS1	=>	01000
PS2	=>	00000
PS3	=>	11000

SI Modify

PROJECT :U81
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Size: Custom | Document Number: Sun S3 Main | Rev: 1A
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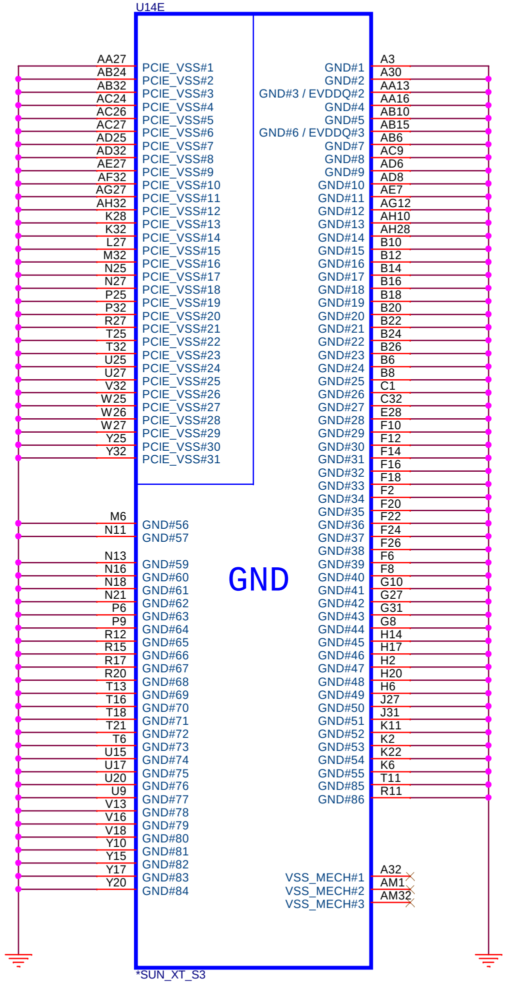
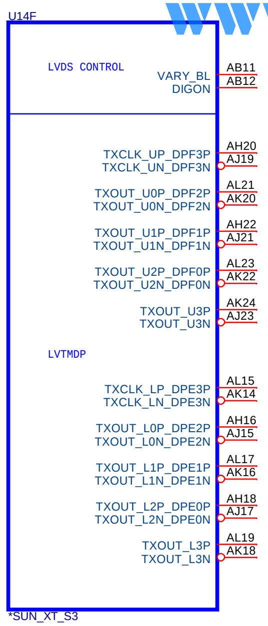




RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

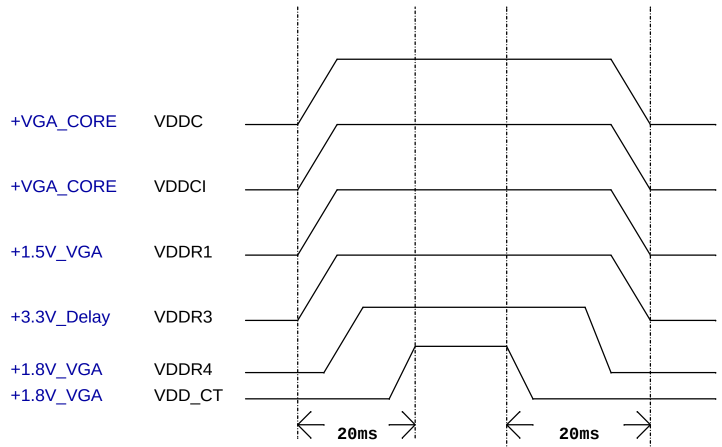
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

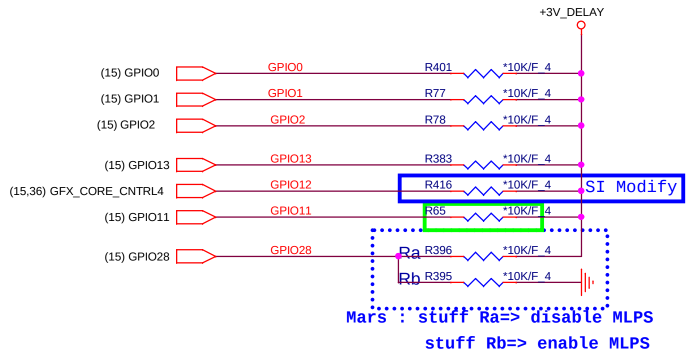
Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



+3V_DELAY (15,17)

PROJECT :U81
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Size	Document Number	Rev
Custom	Sun S3 GND / LVDS/ Straps	1A

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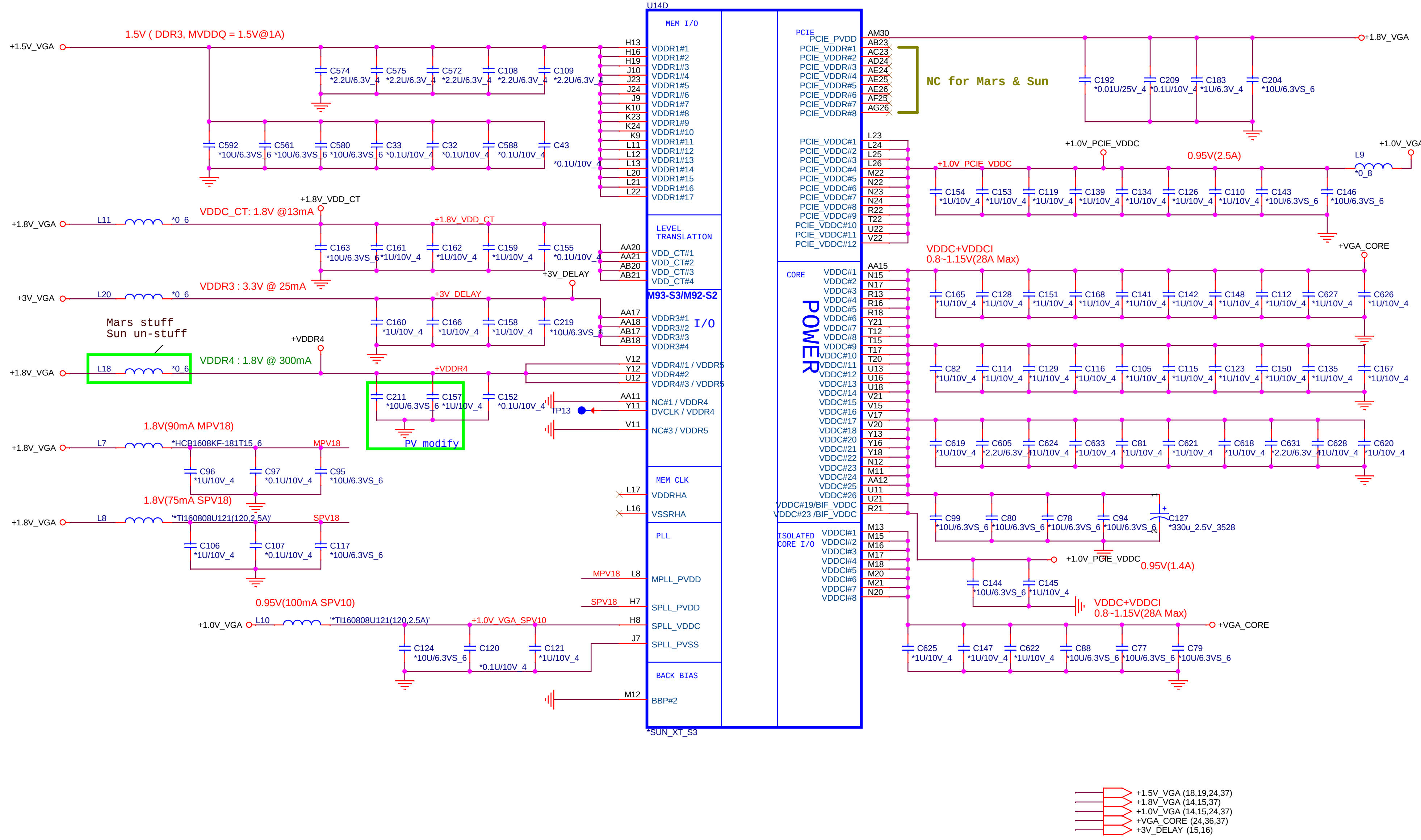

PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 Power_and_NC	1A

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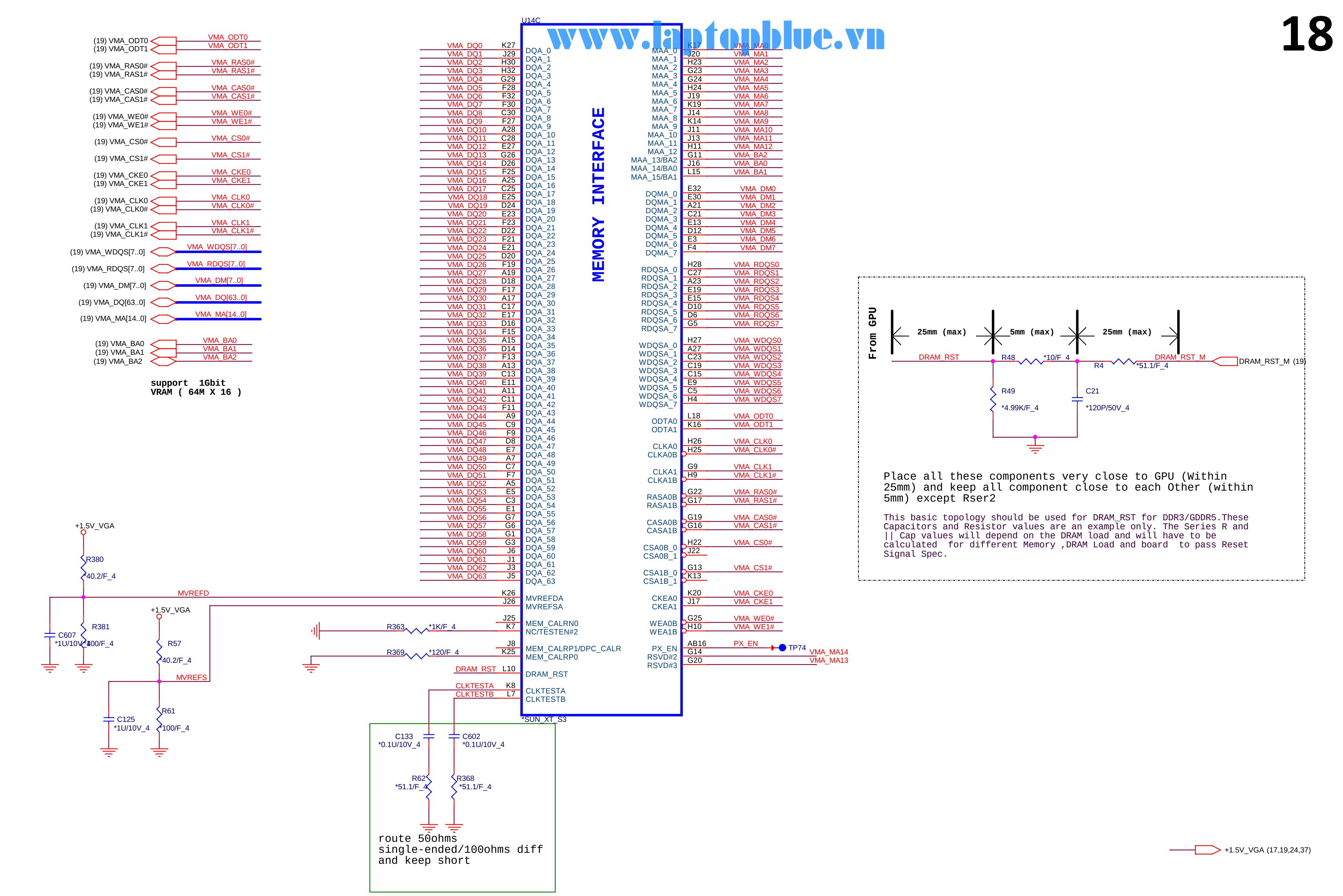

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 MEM_Interface	1A

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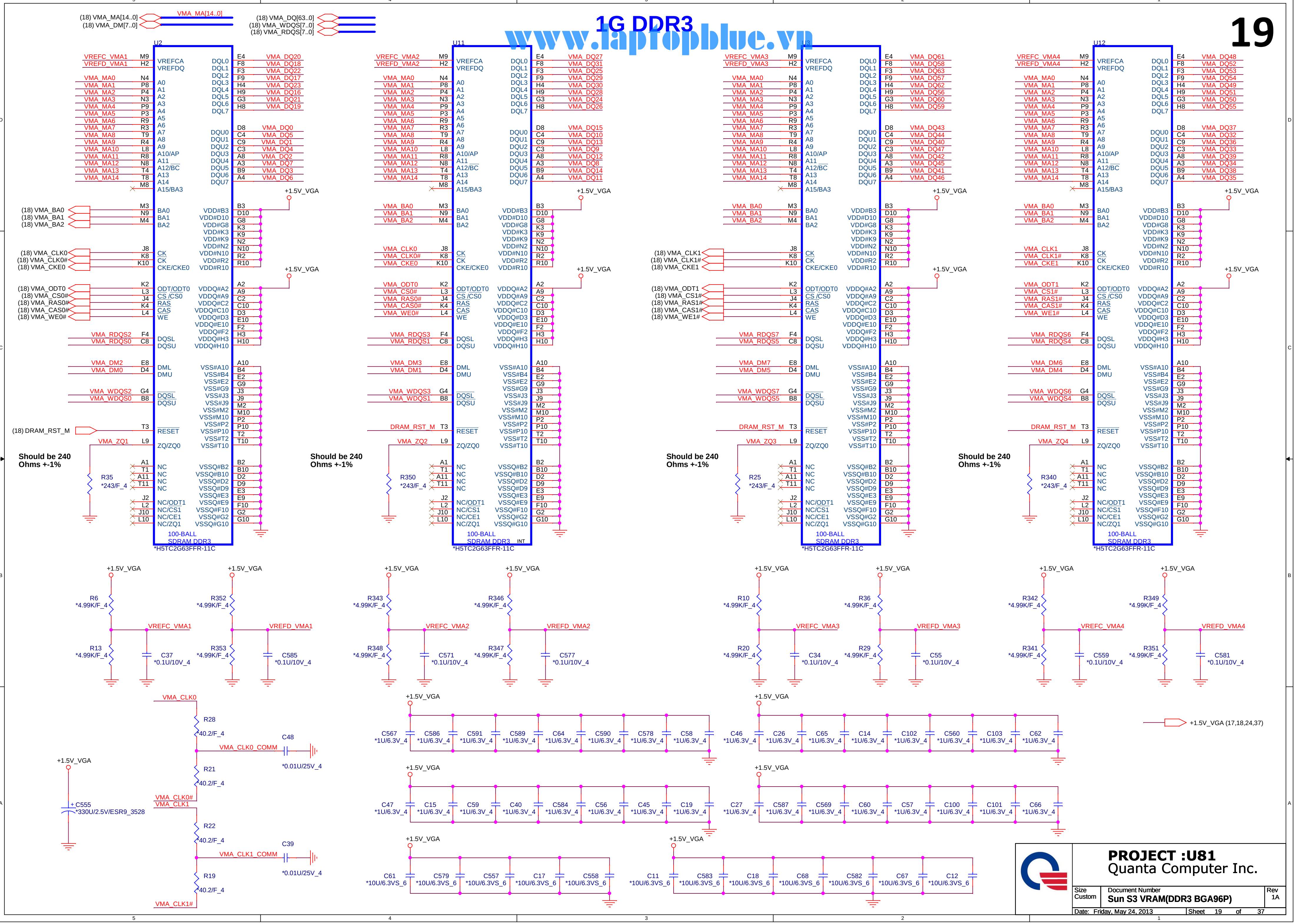

1G DDR3
www.laptopblue.vn
19
U2
U11
U3
U12
VREFCA
VREFDQ
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15/BA3
BA0 BA1 BA2
CK
CK
CKE/CKE0
ODT/ODT0
CS /CS0
RAS
CAS
WE
DQSL
DQSU
DML
DMU
RESET
ZQ/ZQ0
NC
NC/ODT1
NC/CS1
NC/CE1
NC/ZQ1
100-BALL
SDRAM DDR3
*H5TC2G63FFR-11C
+1.5V_VGA
(18) VMA_MA[14..0]
(18) VMA_DM[7..0]
(18) VMA_DQ[63..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]
(18) DRAM_RST_M
Should be 240 Ohms +-1%
R35 *243/F_4
R350 *243/F_4
R25 *243/F_4
R340 *243/F_4
VREFC_VMA1
VREFD_VMA1
VREFC_VMA2
VREFD_VMA2
VREFC_VMA3
VREFD_VMA3
VREFC_VMA4
VREFD_VMA4
*4.99K/F_4
*0.1U/10V_4
VMA_CLK0
VMA_CLK0#
VMA_CLK0_COMM
VMA_CLK1
VMA_CLK1#
VMA_CLK1_COMM
R28 40.2/F_4
R21 40.2/F_4
R22 40.2/F_4
R19 40.2/F_4
C48 *0.01U/25V_4
C39 *0.01U/25V_4
C555 *330U/2.5V/ESR9_3528
*1U/6.3V_4
*10U/6.3VS_6
+1.5V_VGA (17,18,24,37)
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number
Sun S3 VRAM(DDR3 BGA96P)
Rev 1A
Date: Friday, May 24, 2013
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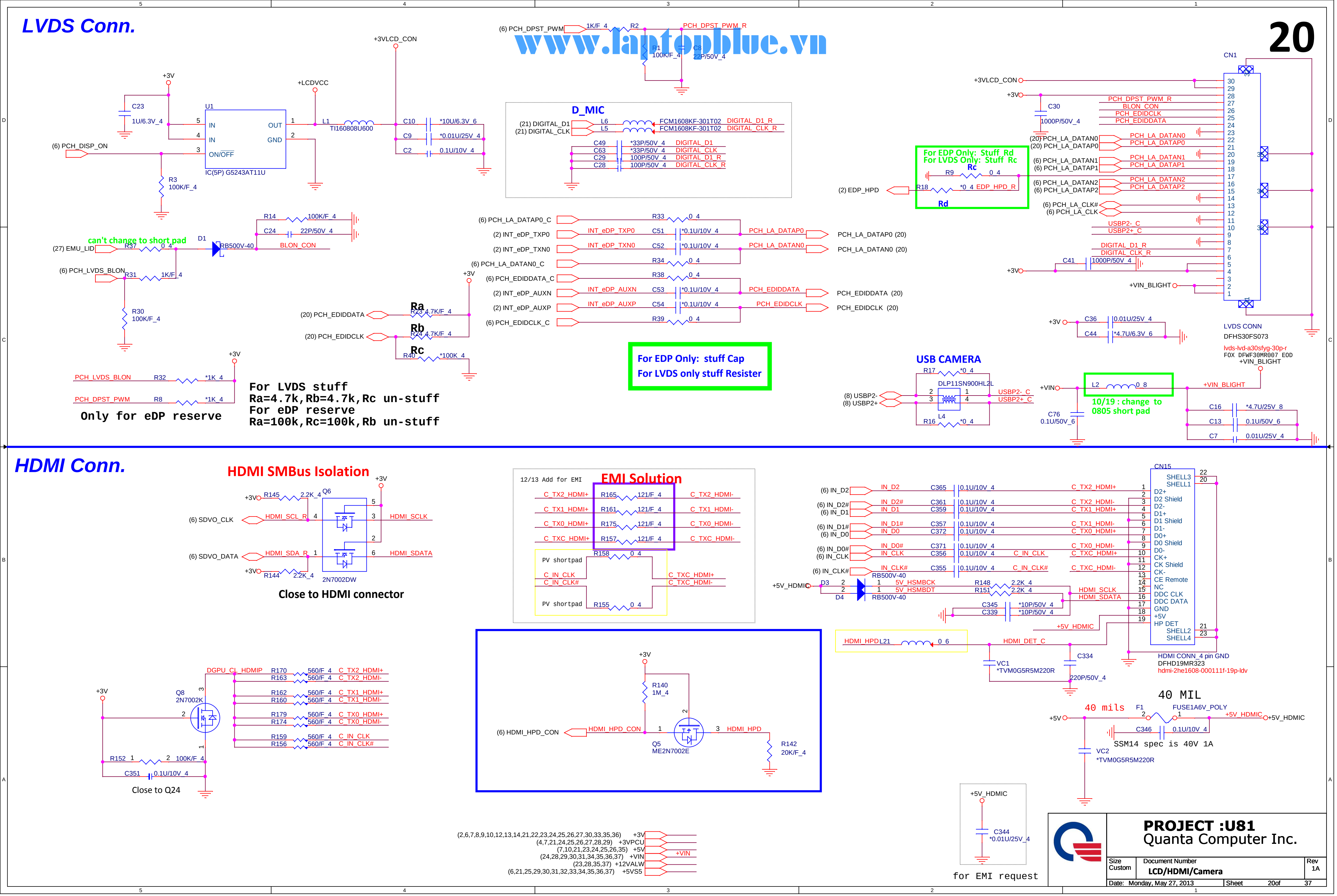
20
LVDS Conn.
www.laptopblue.vn
D_MIC
For EDP Only: Stuff Rd
For LVDS Only: Stuff Rc
can't change to short pad
Ra
Rb
Rc
For EDP Only: stuff Cap
For LVDS only stuff Resister
USB CAMERA
10/19 : change to 0805 short pad
Only for eDP reserve
For LVDS stuff
Ra=4.7k,Rb=4.7k,Rc un-stuff
For eDP reserve
Ra=100k,Rc=100k,Rb un-stuff
LVDS CONN
DFHS30FS073
HDMI Conn.
HDMI SMBus Isolation
Close to HDMI connector
12/13 Add for EMI
EMI Solution
PV shortpad
Close to Q24
HDMI CONN_4 pin GND
DFHD19MR323
40 MIL
40 mils
SSM14 spec is 40V 1A
for EMI request
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number
LCD/HDMI/Camera
Rev 1A
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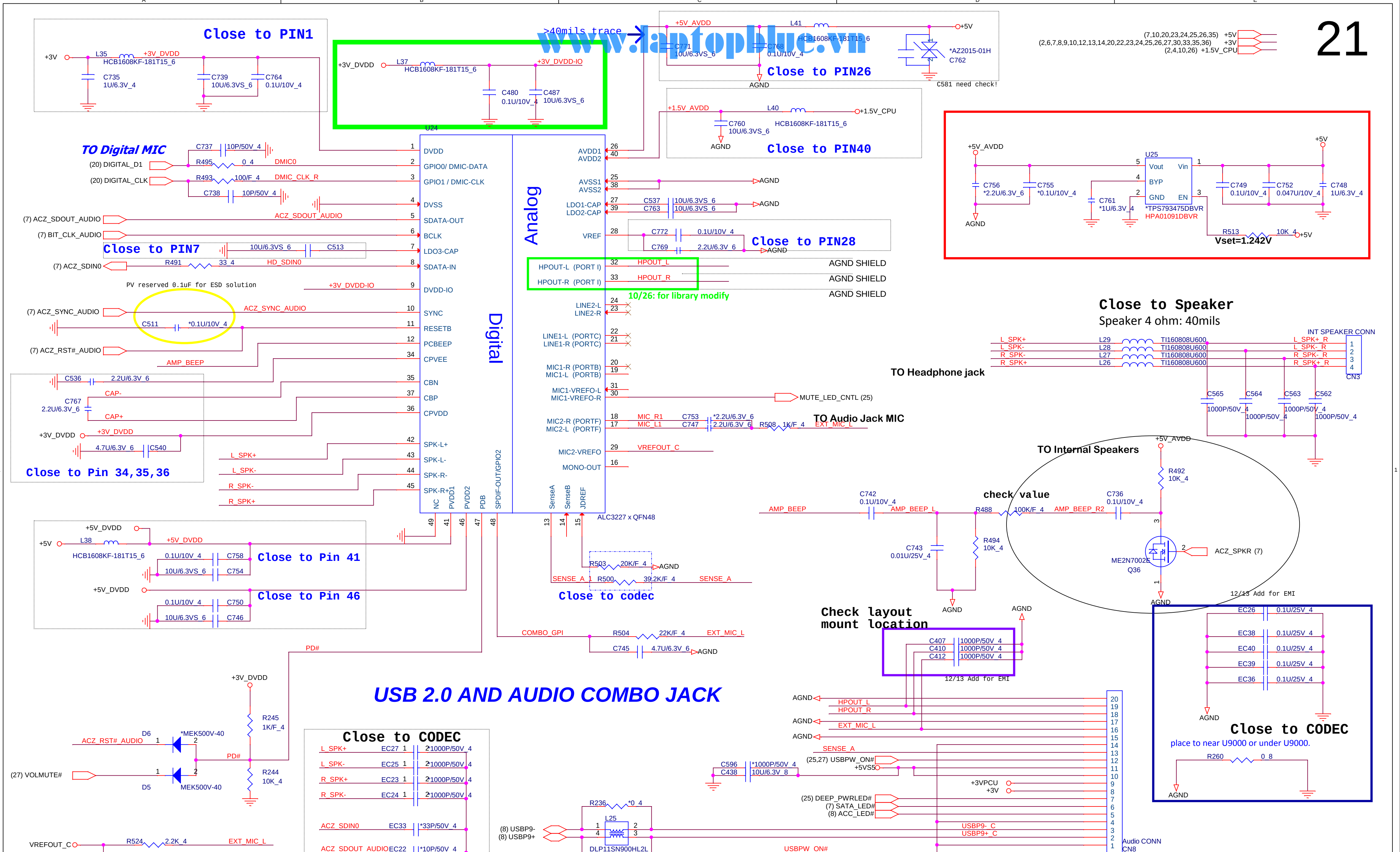

PROJECT :U81

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC 3227/D-MIC	1A

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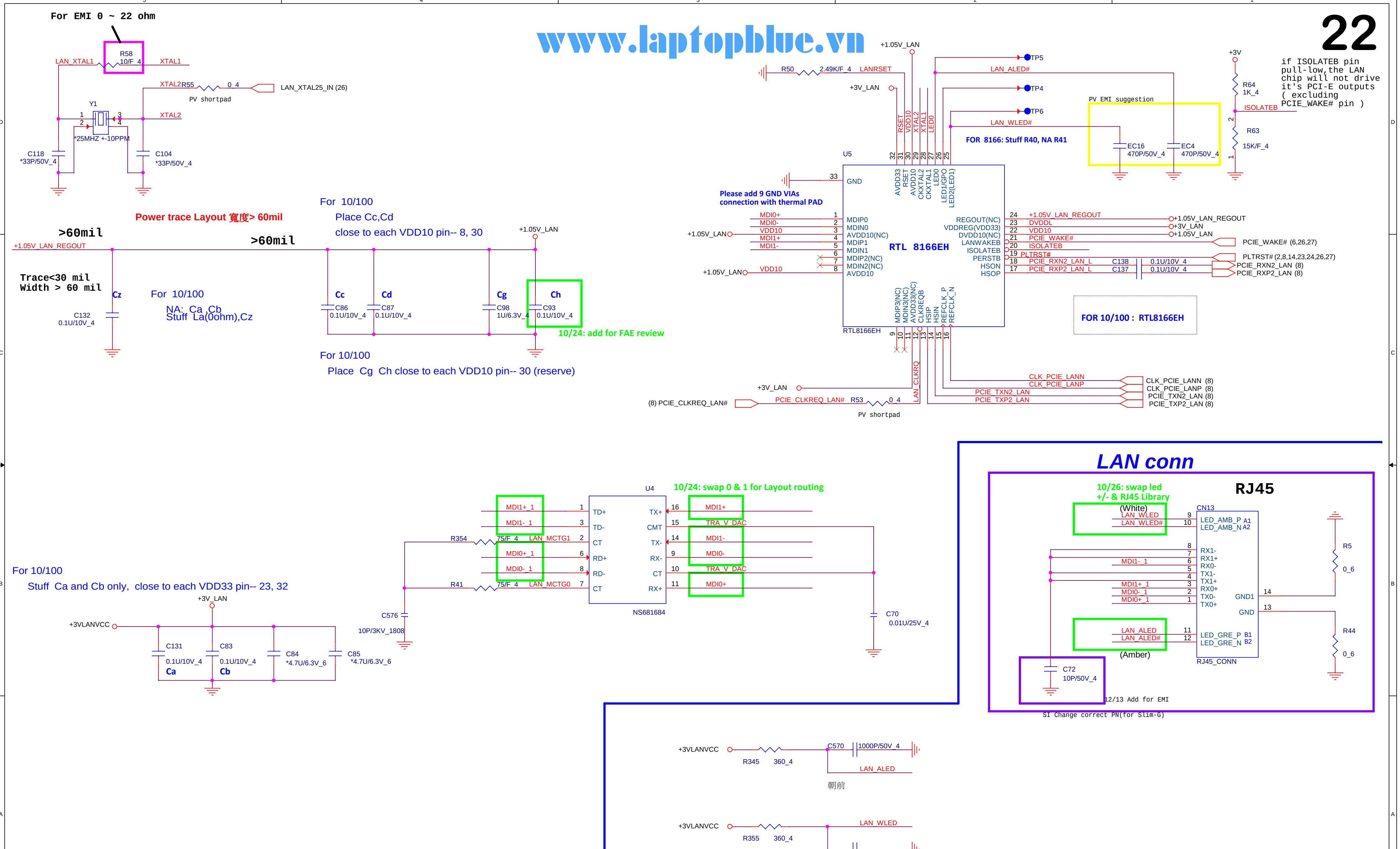

PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN RTL8166EH /RJ45 conn	1A

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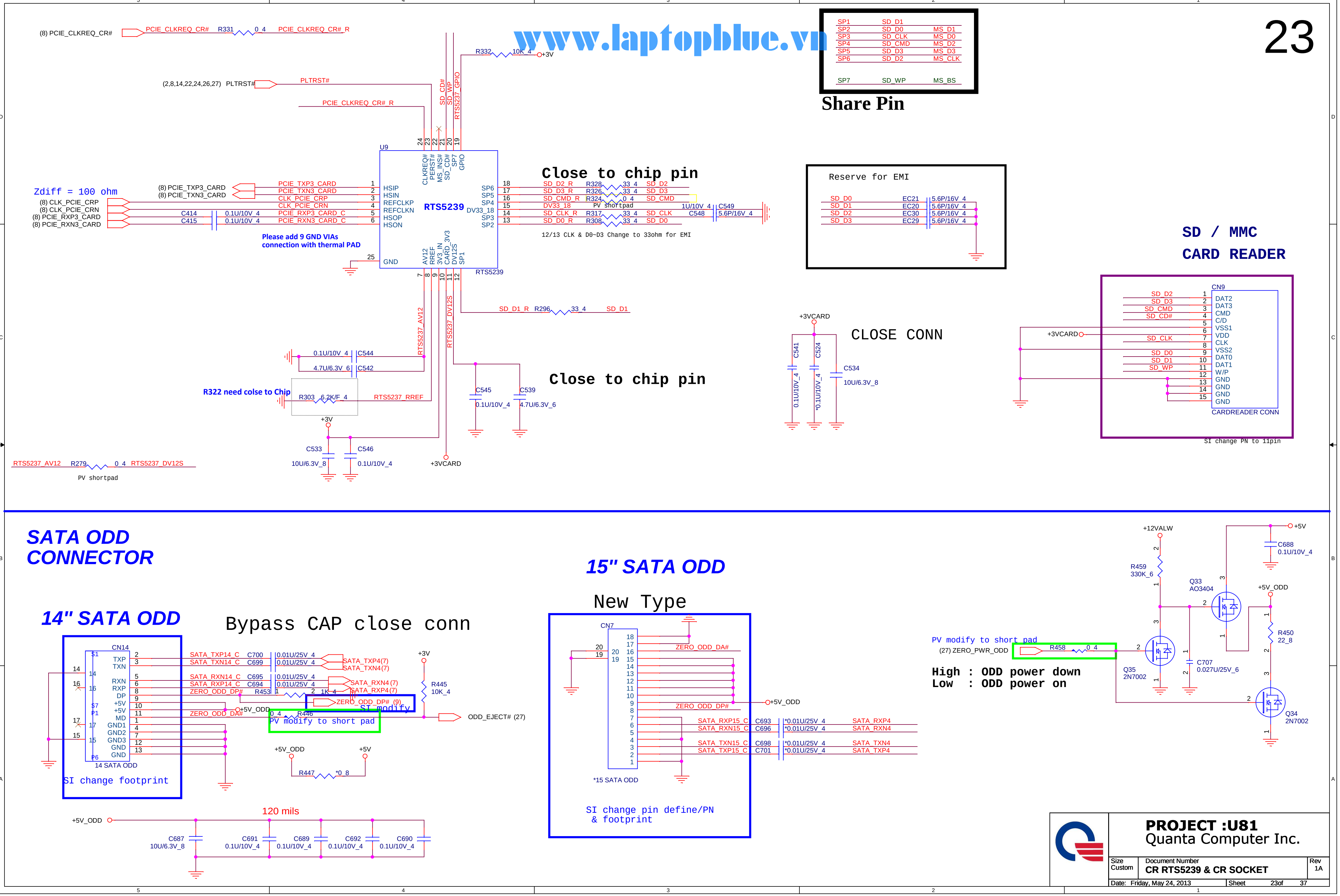
23
www.laptopblue.vn
Share Pin
SP1 SD_D1
SP2 SD_D0 MS_D1
SP3 SD_CLK MS_D0
SP4 SD_CMD MS_D2
SP5 SD_D3 MS_D3
SP6 SD_D2 MS_CLK
SP7 SD_WP MS_BS
Close to chip pin
RTS5239
U9
Zdiff = 100 ohm
Please add 9 GND VIAs connection with thermal PAD
12/13 CLK & D0~D3 Change to 33ohm for EMI
Reserve for EMI
SD / MMC CARD READER
CLOSE CONN
R322 need colse to Chip
PV shortpad
CARDREADER CONN
SI change PN to 11pin
SATA ODD CONNECTOR
14" SATA ODD
Bypass CAP close conn
SI change footprint
15" SATA ODD
New Type
SI change pin define/PN & footprint
PV modify to short pad
SI modify
120 mils
High : ODD power down
Low : ODD power on
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number
CR RTS5239 & CR SOCKET
Rev 1A
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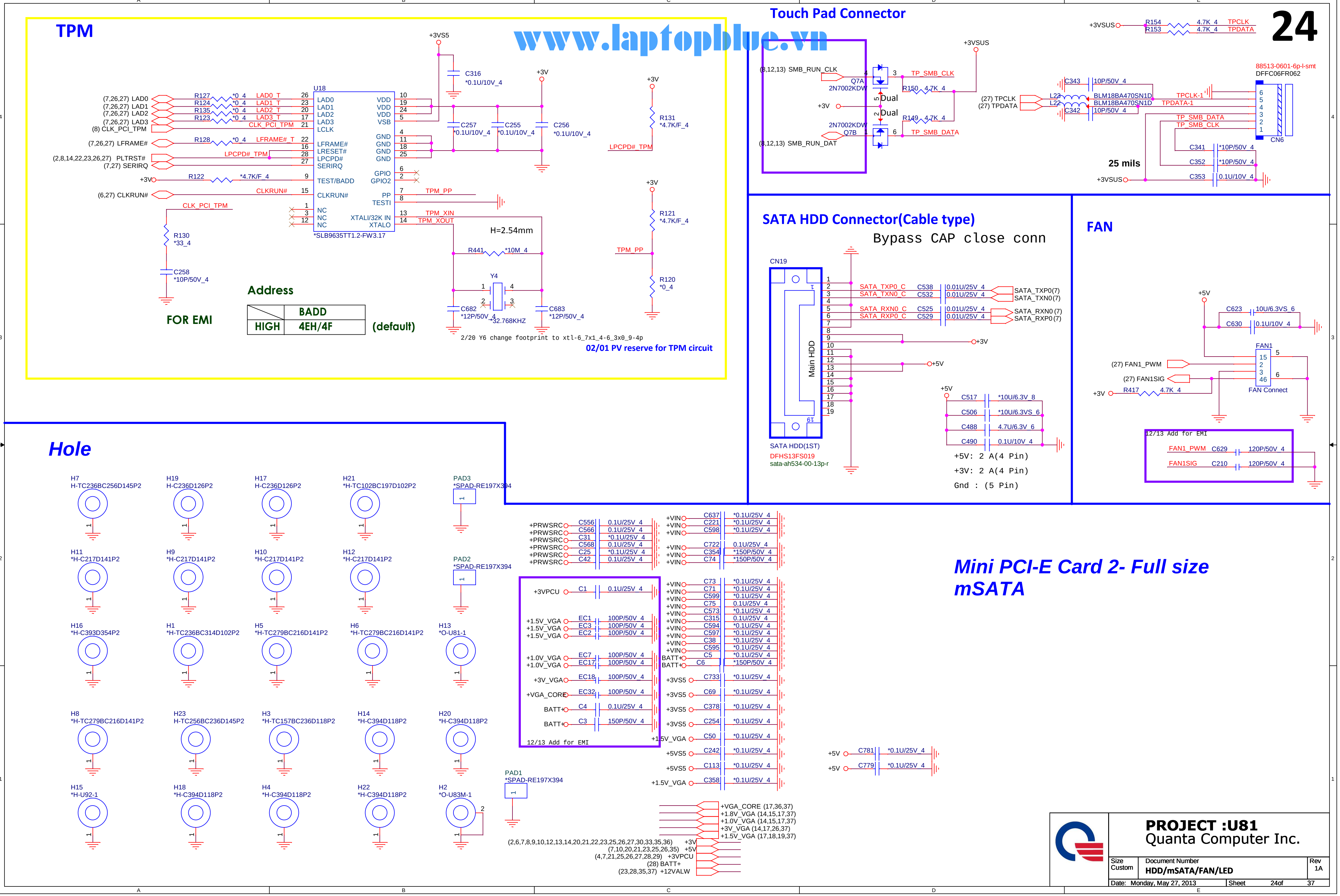
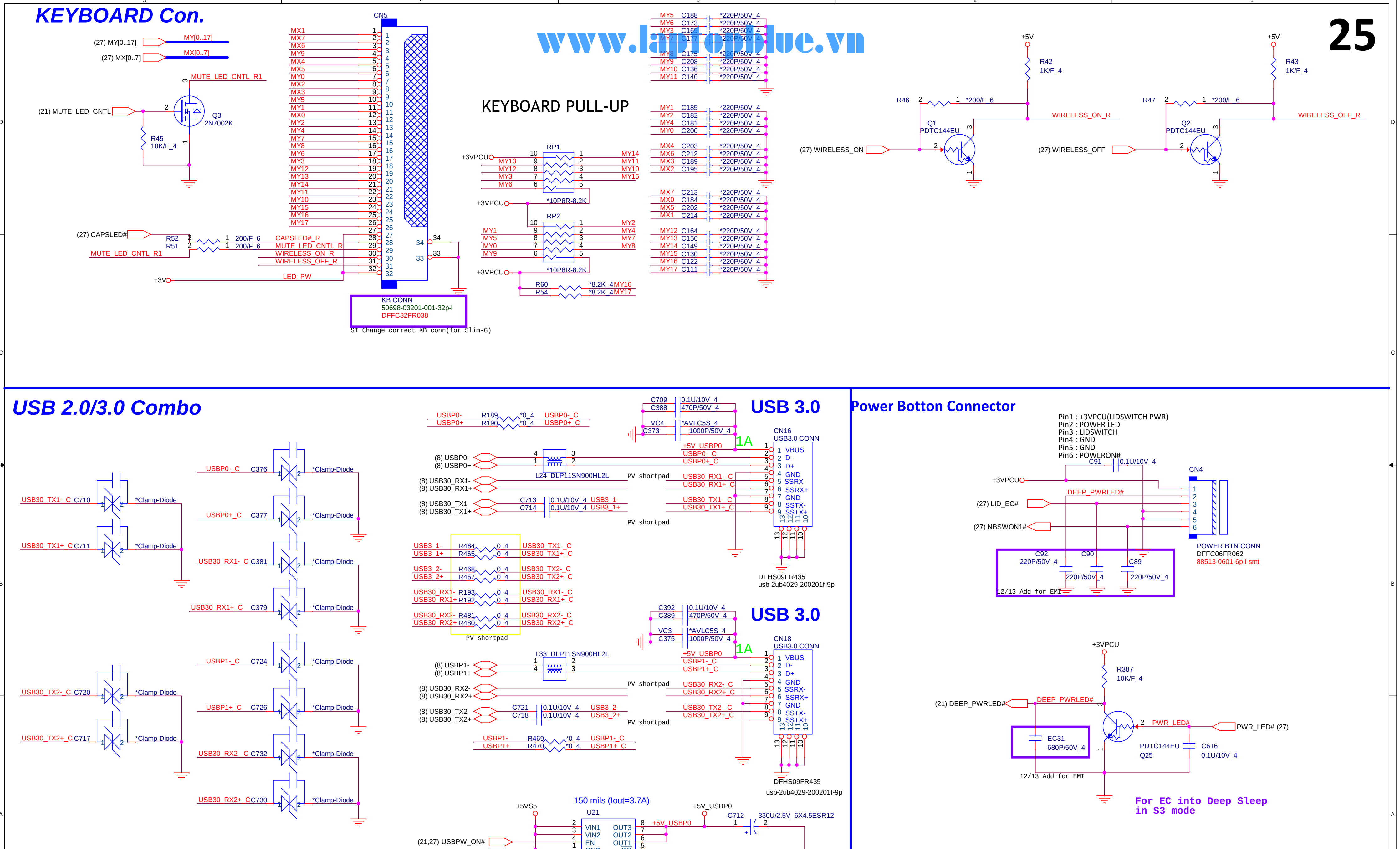
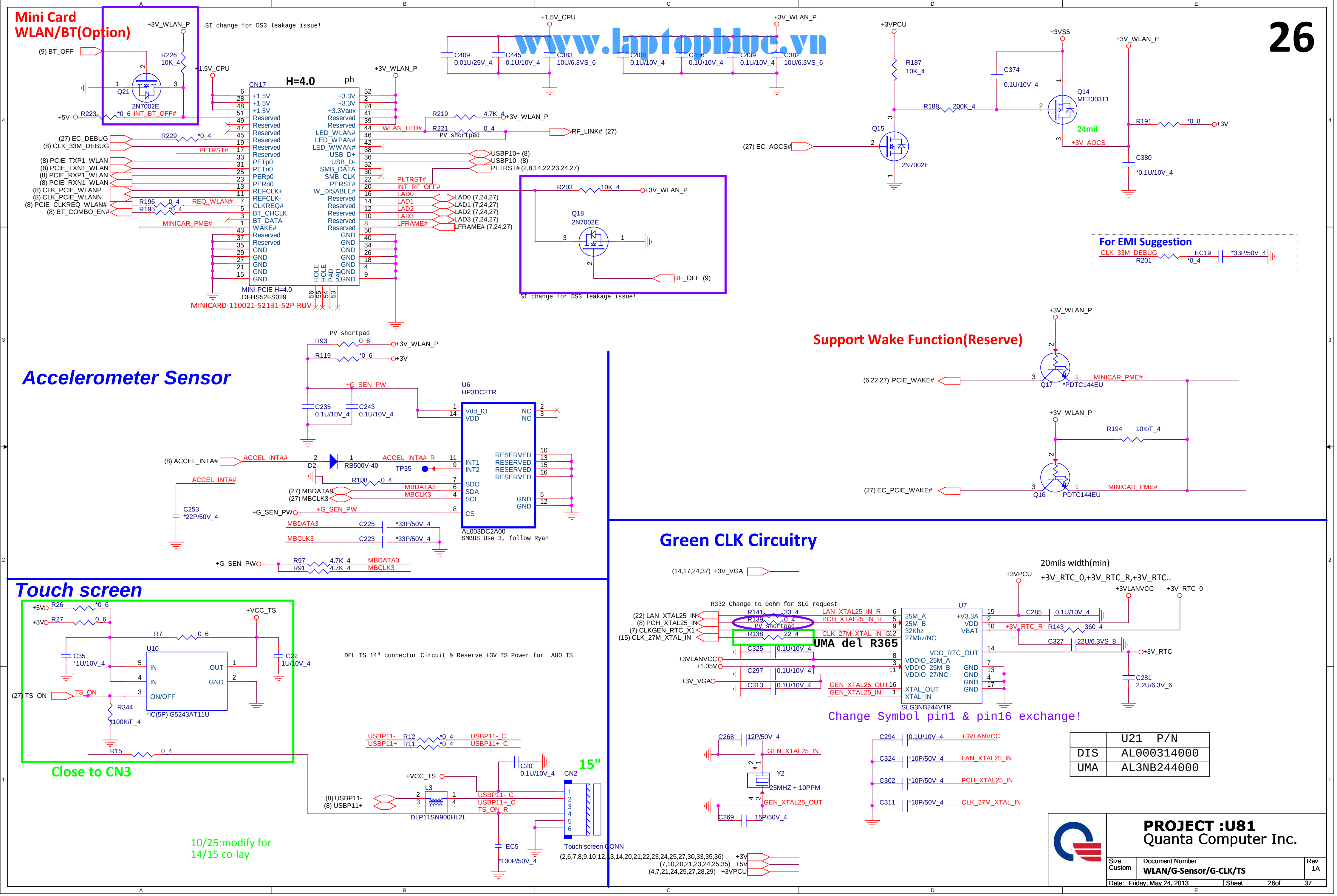

24
TPM
www.laptopblue.vn
+3VS5
C316 *0.1U/10V_4
+3V
U18
(7,26,27) LAD0
(7,26,27) LAD1
(7,26,27) LAD2
(7,26,27) LAD3
(8) CLK_PCI_TPM
(7,26,27) LFRAME#
(2,8,14,22,23,26,27) PLTRST#
(7,27) SERIRQ
(6,27) CLKRUN#
R127 *0_4 LAD0_T
R124 *0_4 LAD1_T
R135 *0_4 LAD2_T
R123 *0_4 LAD3_T
CLK_PCI_TPM
R128 *0_4 LFRAME#_T
LPCPD#_TPM
R122 *4.7K/F_4
CLKRUN#
LAD0 LAD1 LAD2 LAD3 LCLK
LFRAME# LRESET# LPCPD# SERIRQ
TEST/BADD
CLKRUN#
NC NC NC
VDD VDD VDD VSB
GND GND GND GND
GPIO GPIO2
PP TESTI
XTALI/32K IN XTALO
*SLB9635TT1.2-FW3.17
C257 *0.1U/10V_4
C255 *0.1U/10V_4
C256 *0.1U/10V_4
TPM_PP
TPM_XIN
TPM_XOUT
H=2.54mm
R441 *10M_4
Y4
*32.768KHZ
C682 *12P/50V_4
C683 *12P/50V_4
R131 *4.7K/F_4
LPCPD#_TPM
R121 *4.7K/F_4
TPM_PP
R120 *0_4
R130 *33_4
C258 *10P/50V_4
FOR EMI
Address
BADD
HIGH 4EH/4F
(default)
2/20 Y6 change footprint to xtl-6_7x1_4-6_3x0_9-4p
02/01 PV reserve for TPM circuit
Touch Pad Connector
(8,12,13) SMB_RUN_CLK
Q7A 2N7002KDW
Dual
Q7B 2N7002KDW
(8,12,13) SMB_RUN_DAT
+3VSUS
TP_SMB_CLK
R150 4.7K_4
R149 4.7K_4
TP_SMB_DATA
R154 4.7K_4 TPCLK
R153 4.7K_4 TPDATA
(27) TPCLK
(27) TPDATA
C343 10P/50V_4
L23 L22 BLM18BA470SN1D
C342 10P/50V_4
TPCLK-1
TPDATA-1
TP_SMB_DATA
TP_SMB_CLK
88513-0601-6p-l-smt
DFFC06FR062
CN6
C341 *10P/50V_4
C352 *10P/50V_4
C353 0.1U/10V_4
25 mils
SATA HDD Connector(Cable type)
Bypass CAP close conn
CN19
SATA_TXP0_C C538 0.01U/25V_4 SATA_TXP0(7)
SATA_TXN0_C C532 0.01U/25V_4 SATA_TXN0(7)
SATA_RXN0_C C525 0.01U/25V_4 SATA_RXN0(7)
SATA_RXP0_C C529 0.01U/25V_4 SATA_RXP0(7)
Main HDD
+3V
+5V
C517 *10U/6.3V_8
C506 *10U/6.3VS_6
C488 4.7U/6.3V_6
C490 0.1U/10V_4
SATA HDD(1ST)
DFHS13FS019
sata-ah534-00-13p-r
+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)
FAN
C623 10U/6.3VS_6
C630 0.1U/10V_4
FAN1
(27) FAN1_PWM
(27) FAN1SIG
R417 4.7K_4
FAN Connect
12/13 Add for EMI
FAN1_PWM C629 120P/50V_4
FAN1SIG C210 120P/50V_4
Hole
H7 H-TC236BC256D145P2
H19 H-C236D126P2
H17 H-C236D126P2
H21 *H-TC102BC197D102P2
PAD3 *SPAD-RE197X394
H11 *H-C217D141P2
H9 *H-C217D141P2
H10 *H-C217D141P2
H12 *H-C217D141P2
PAD2 *SPAD-RE197X394
H16 *H-C393D354P2
H1 *H-TC236BC314D102P2
H5 *H-TC279BC216D141P2
H6 *H-TC279BC216D141P2
H13 *O-U81-1
H8 *H-TC279BC216D141P2
H23 H-TC256BC236D145P2
H3 *H-TC157BC236D118P2
H14 *H-C394D118P2
H20 *H-C394D118P2
PAD1 *SPAD-RE197X394
H15 *H-U92-1
H18 *H-C394D118P2
H4 *H-C394D118P2
H22 *H-C394D118P2
H2 *O-U83M-1
+PRWSRC C556 0.1U/25V_4
+PRWSRC C566 0.1U/25V_4
+PRWSRC C31 *0.1U/25V_4
+PRWSRC C568 0.1U/25V_4
+PRWSRC C25 *0.1U/25V_4
+PRWSRC C42 0.1U/25V_4
+3VPCU C1 0.1U/25V_4
+1.5V_VGA EC1 100P/50V_4
+1.5V_VGA EC3 100P/50V_4
+1.5V_VGA EC2 100P/50V_4
+1.0V_VGA EC7 100P/50V_4
+1.0V_VGA EC17 100P/50V_4
+3V_VGA EC18 100P/50V_4
+VGA_CORE EC32 100P/50V_4
BATT+ C4 0.1U/25V_4
BATT+ C3 150P/50V_4
12/13 Add for EMI
+VIN C637 *0.1U/25V_4
+VIN C221 *0.1U/25V_4
+VIN C598 *0.1U/25V_4
+VIN C722 0.1U/25V_4
+VIN C354 *150P/50V_4
+VIN C74 *150P/50V_4
+VIN C73 *0.1U/25V_4
+VIN C71 *0.1U/25V_4
+VIN C599 *0.1U/25V_4
+VIN C75 0.1U/25V_4
+VIN C573 *0.1U/25V_4
+VIN C315 0.1U/25V_4
+VIN C594 *0.1U/25V_4
+VIN C597 *0.1U/25V_4
+VIN C38 *0.1U/25V_4
+VIN C595 *0.1U/25V_4
+VIN C5 *0.1U/25V_4
BATT+ C6 *150P/50V_4
+3VS5 C733 *0.1U/25V_4
+3VS5 C69 *0.1U/25V_4
+3VS5 C378 *0.1U/25V_4
+3VS5 C254 *0.1U/25V_4
+1.5V_VGA C50 *0.1U/25V_4
+5VS5 C242 *0.1U/25V_4
+5VS5 C113 *0.1U/25V_4
+1.5V_VGA C358 *0.1U/25V_4
+5V C781 *0.1U/25V_4
+5V C779 *0.1U/25V_4
Mini PCI-E Card 2- Full size
mSATA
+VGA_CORE (17,36,37)
+1.8V_VGA (14,15,17,37)
+1.0V_VGA (14,15,17,37)
+3V_VGA (14,17,26,37)
+1.5V_VGA (17,18,19,37)
(2,6,7,8,9,10,12,13,14,20,21,22,23,25,26,27,30,33,35,36) +3V
(7,10,20,21,23,25,26,35) +5V
(4,7,21,25,26,27,28,29) +3VPCU
(28) BATT+
(23,28,35,37) +12VALW
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number HDD/mSATA/FAN/LED
Rev 1A
Date: Monday, May 27, 2013
Sheet 24 of 37



PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0/KB	1A
Date: Monday, May 27, 2013	Sheet 25 of 37	



26
Mini Card WLAN/BT(Option)
SI change for DS3 leakage issue!
www.laptopblue.vn
H=4.0
MINI PCIE H=4.0
DFHS52FS029
MINICARD-110021-52131-52P-RUV
PV shortpad
For EMI Suggestion
Support Wake Function(Reserve)
Accelerometer Sensor
U6
HP3DC2TR
AL003DC2A00
SMBUS Use 3, follow Ryan
Green CLK Circuitry
20mils width(min)
+3V_RTC_0,+3V_RTC_R,+3V_RTC..
R332 Change to 0ohm for SLG request
UMA del R365
SLG3NB244VTR
Change Symbol pin1 & pin16 exchange!
U21 P/N
DIS AL000314000
UMA AL3NB244000
Touch screen
Close to CN3
DEL TS 14" connector Circuit & Reserve +3V TS Power for AUO TS
15"
Touch screen CONN
10/25:modify for 14/15 co-lay
PROJECT :U81
Quanta Computer Inc.
Size Custom
Document Number WLAN/G-Sensor/G-CLK/TS
Rev 1A
Date: Friday, May 24, 2013
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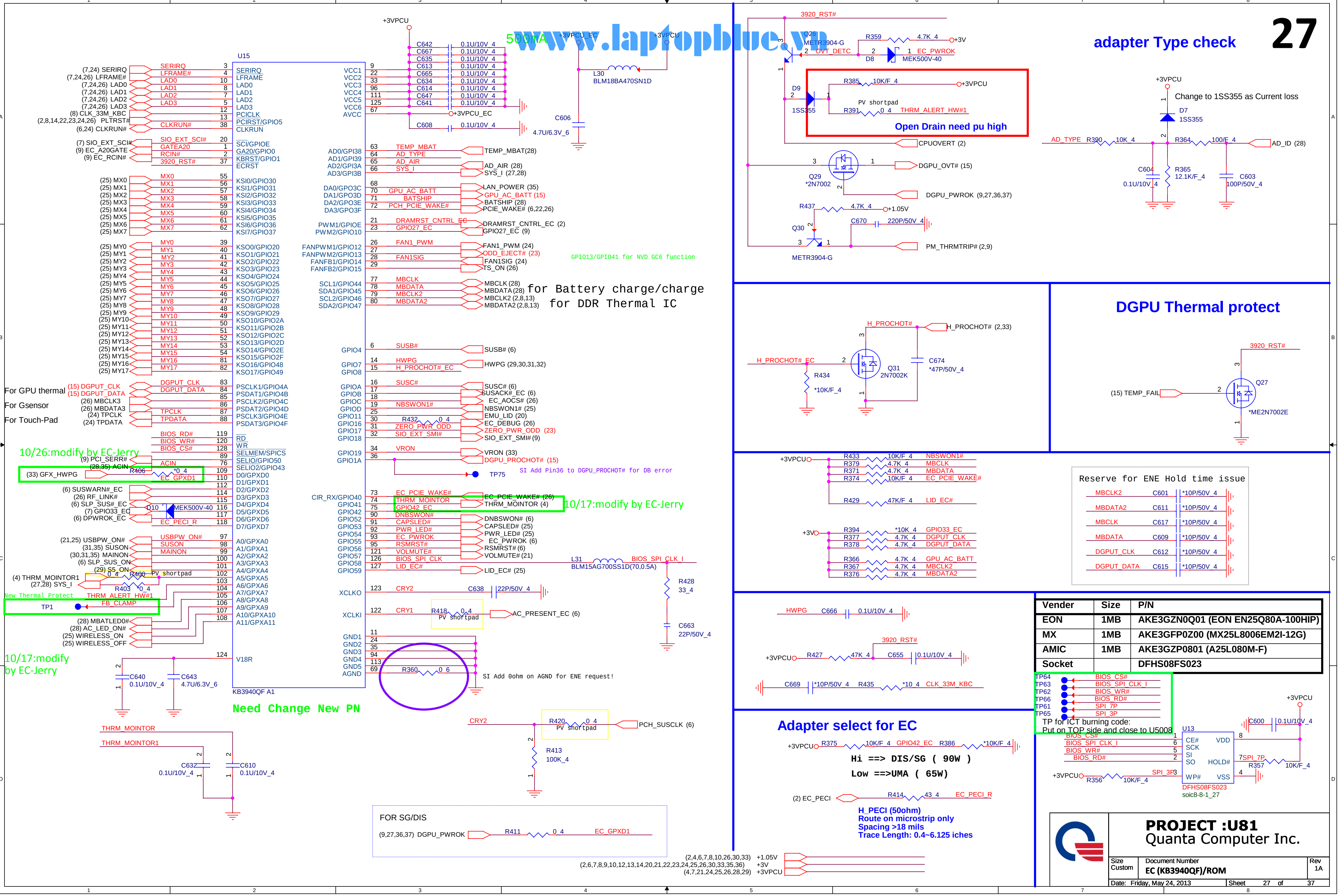

Vender	Size	P/N
EON	1MB	AKE3GZN0Q01 (EON EN25Q80A-100HIP)
MX	1MB	AKE3GFP0Z00 (MX25L8006EM2I-12G)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

PROJECT :U81
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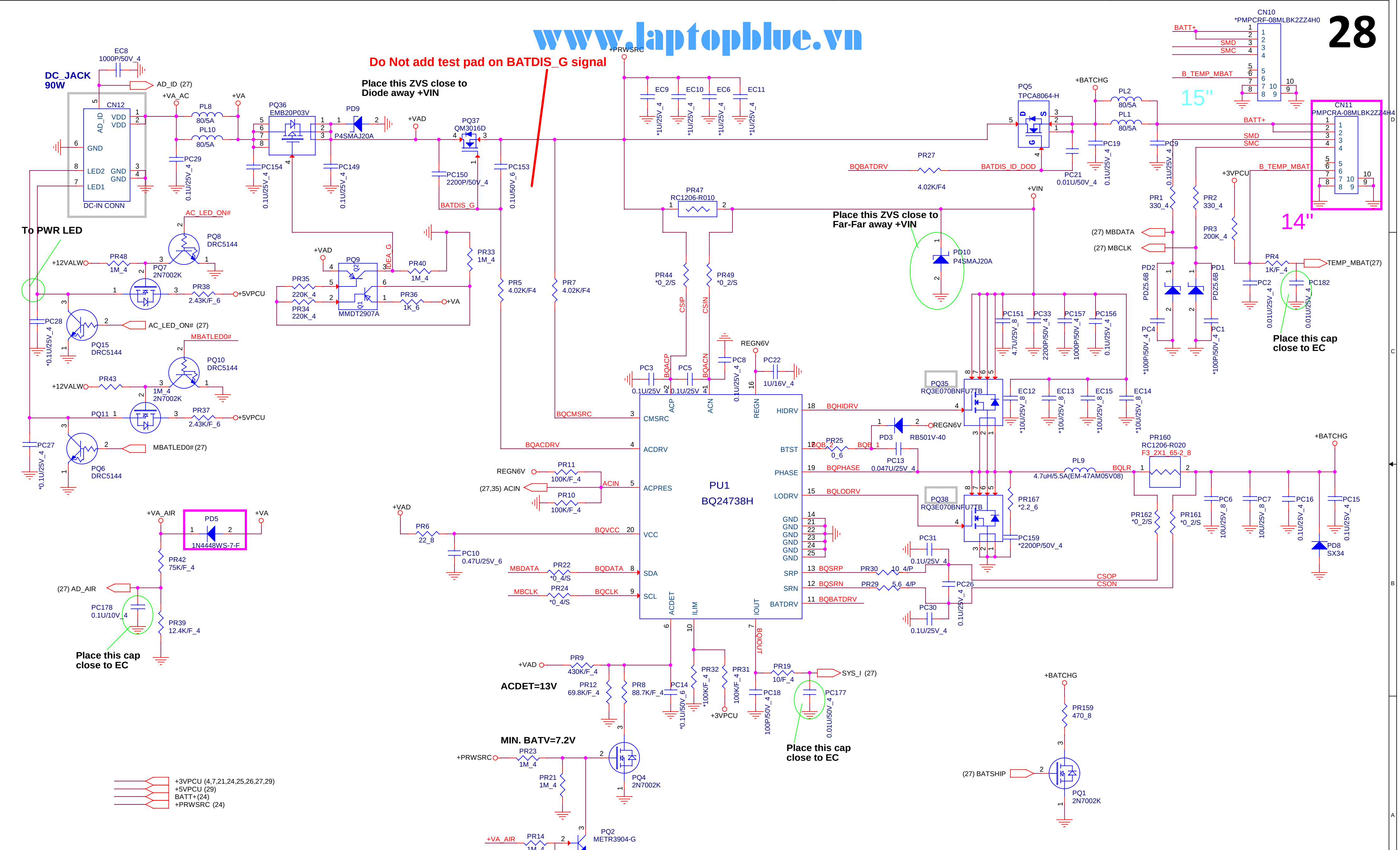
Size	Document Number	Rev
Custom	EC (KB3940QF)/ROM	1A

Date: Friday, May 24, 2013 Sheet 27 of 37



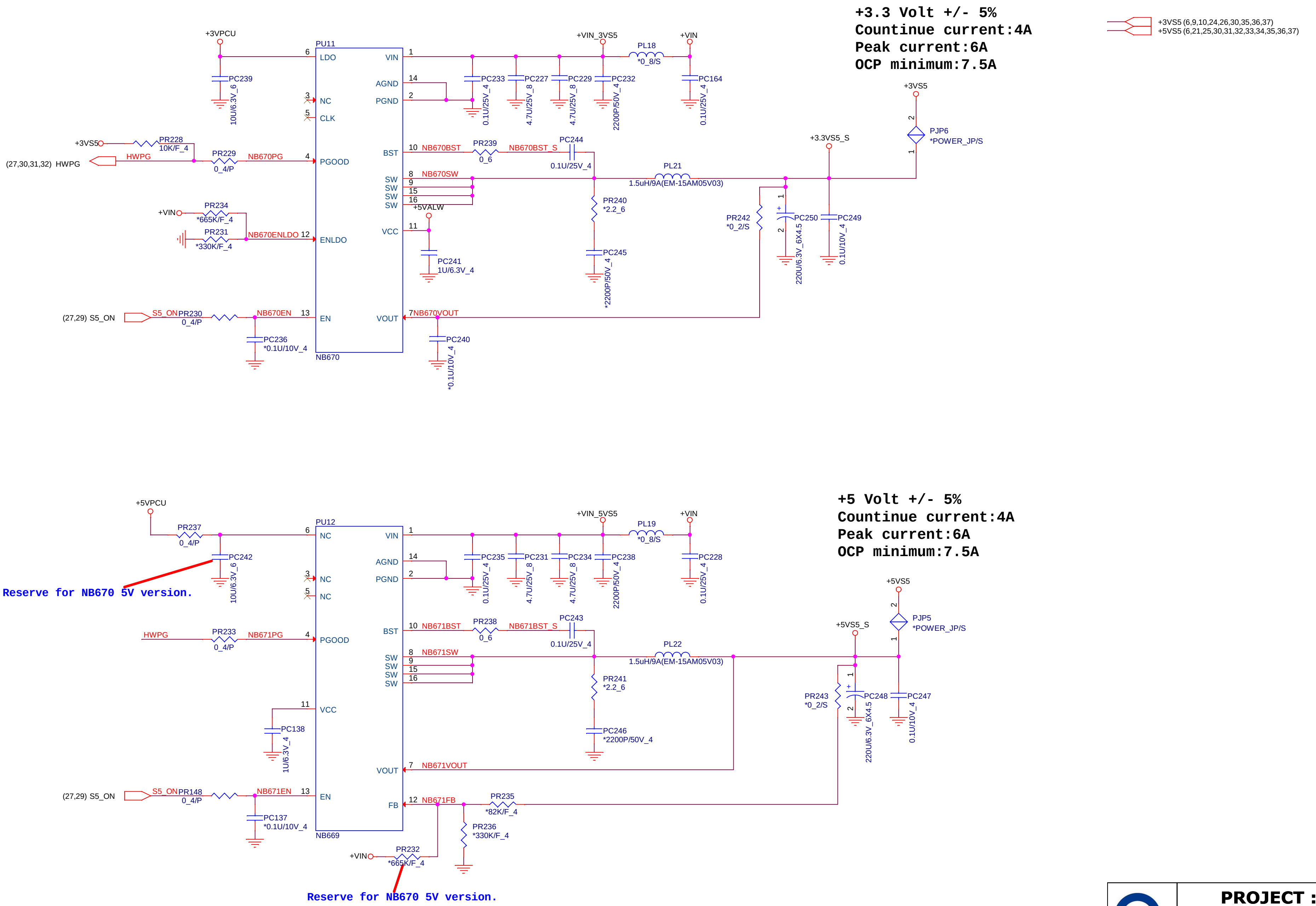
PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (BQ24738)	1A

Date: Friday, May 24, 2013 | Sheet 28 of 37

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

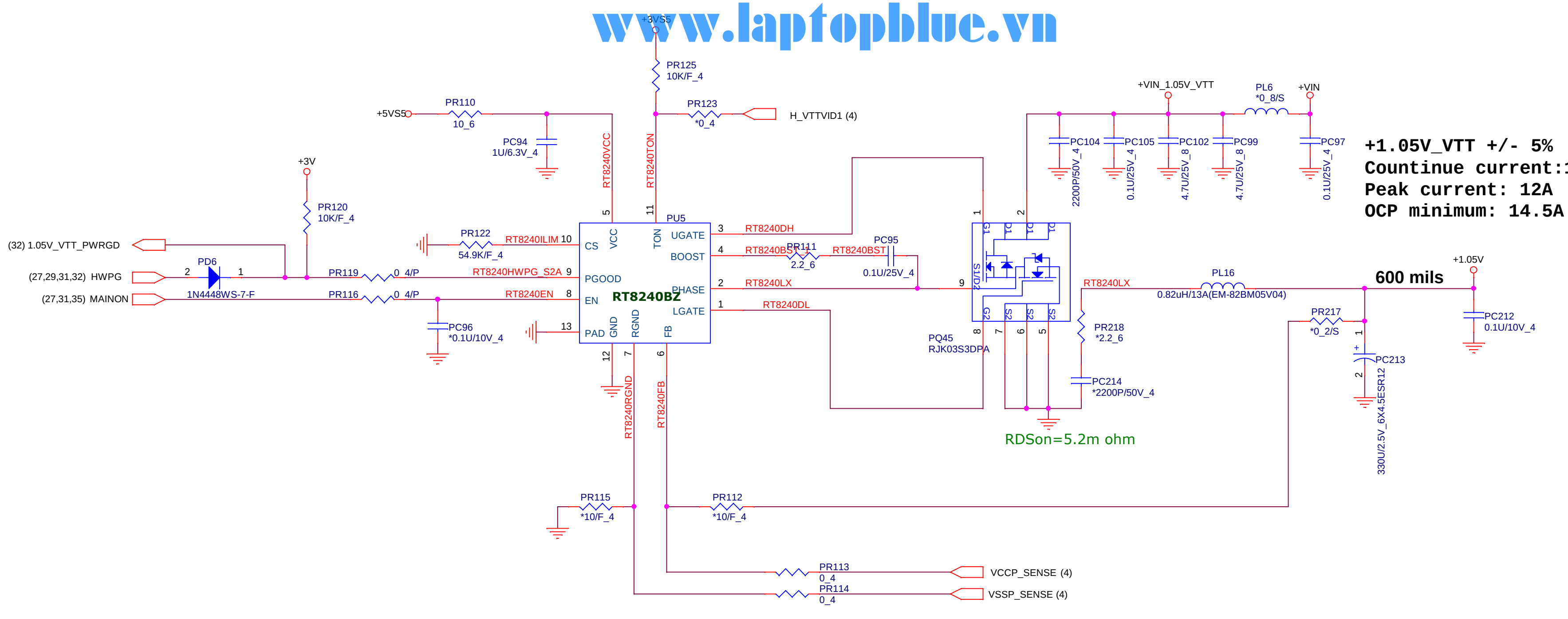
+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(NB669/NB670)	1A

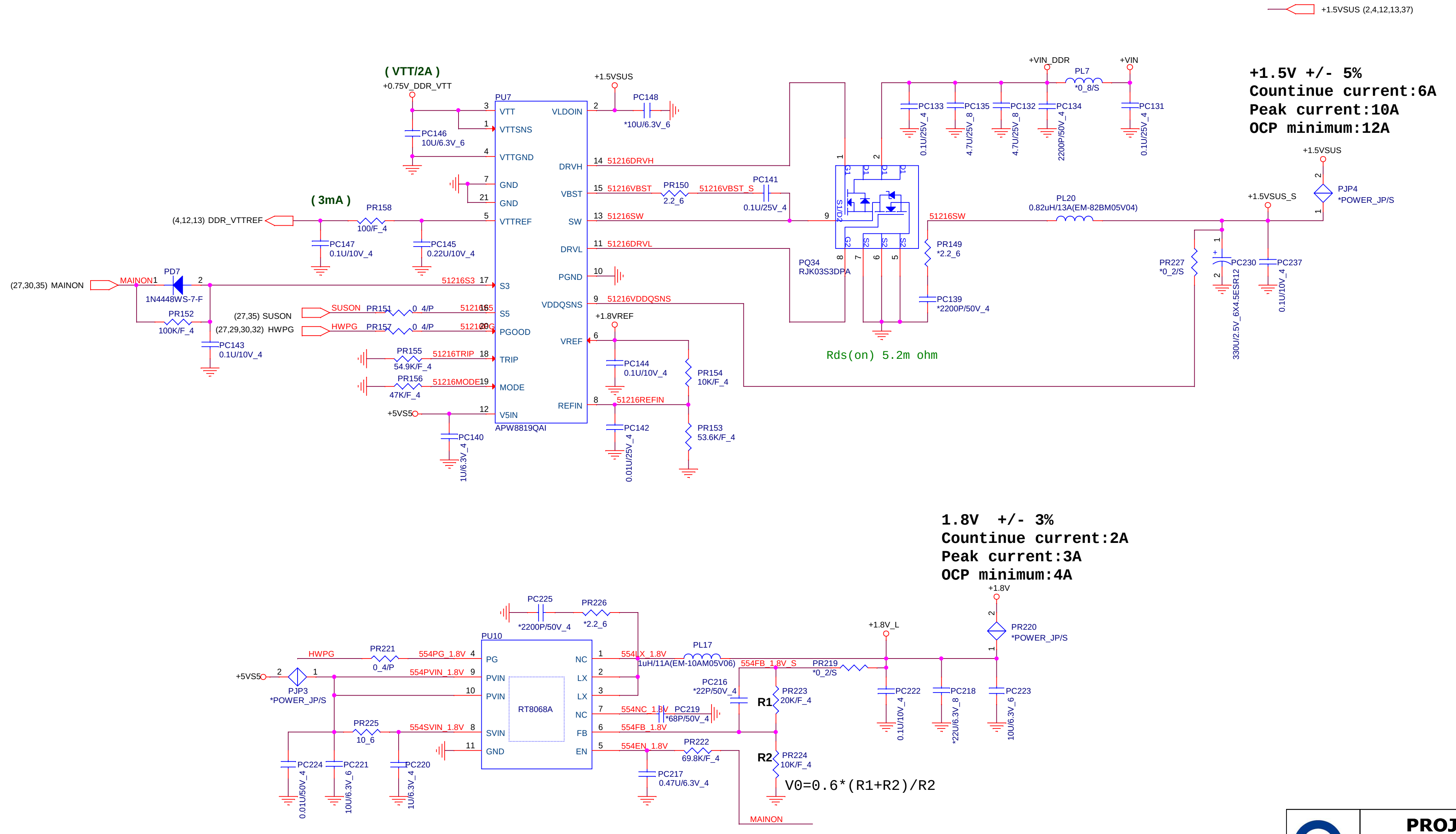
Date: Friday, May 24, 2013 Sheet 29 of 37



+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

+1.05V (2,4,6,7,8,10,26,27,33)

PROJECT :U81 Quanta Computer Inc.		
Size: Custom	Document Number: 1.05V(RT8240BZ)	Rev: 1A
Date: Friday, May 24, 2013	Sheet 30 of 37	



PROJECT :U81

Quanta Computer Inc.

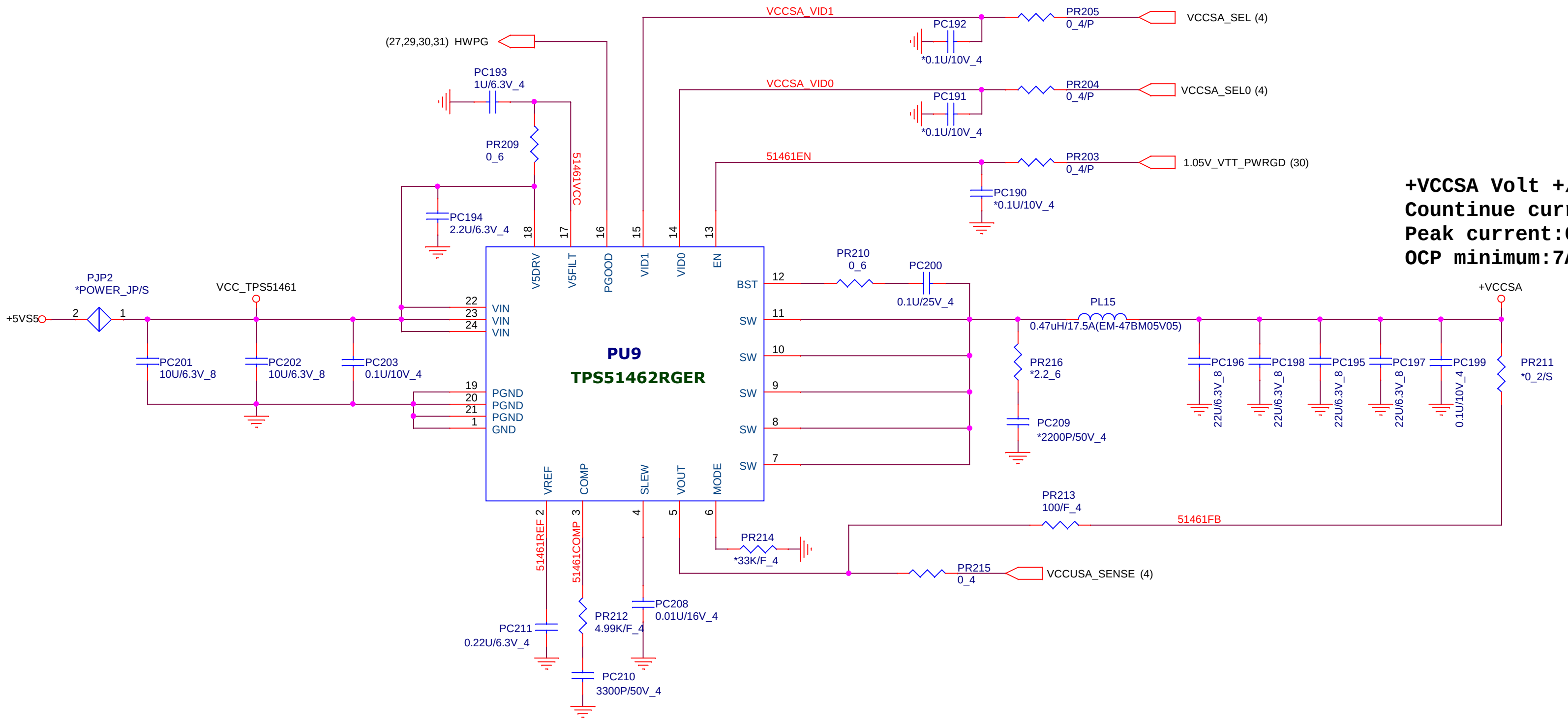
Size	Document Number	Rev
Custom	DDR3 (APW8819)	1A

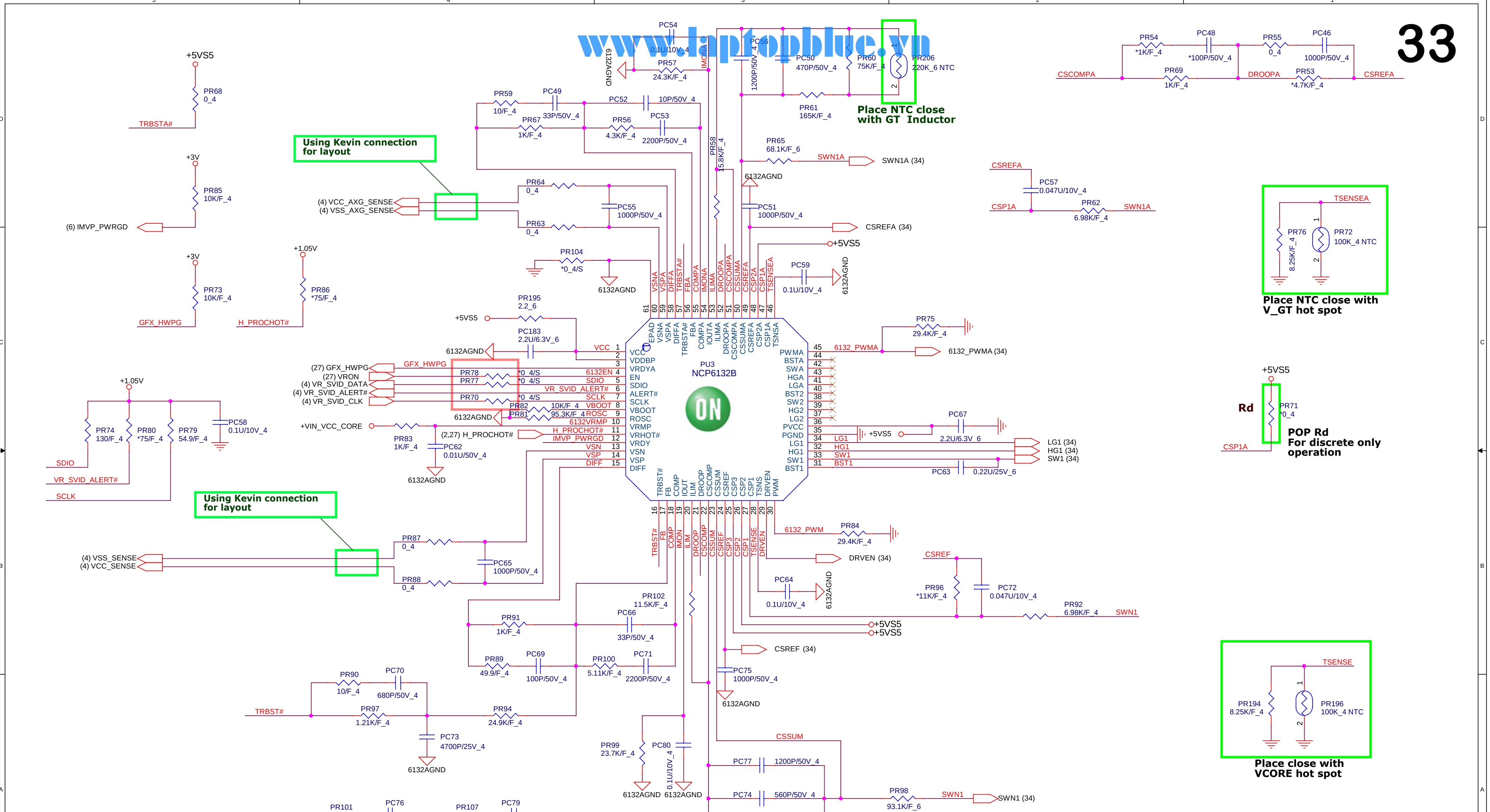
TPS51462RGER/AL051462000

For CPU SV system agent
voltage slew rate of 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A





PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core1 (NCP6132B)	1A

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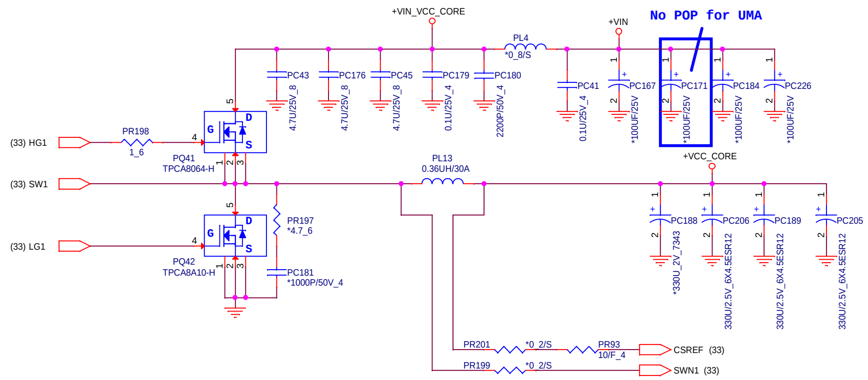
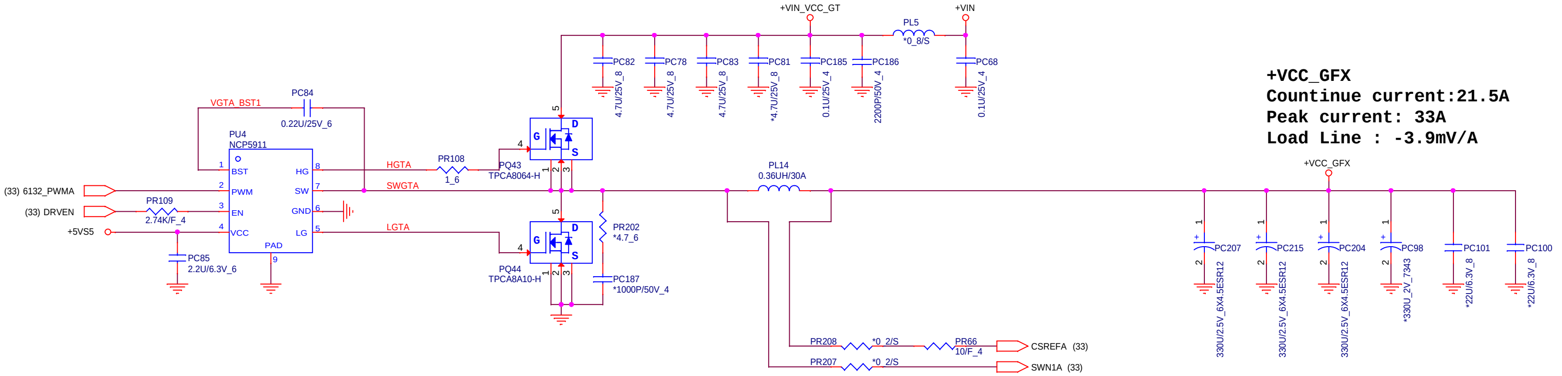
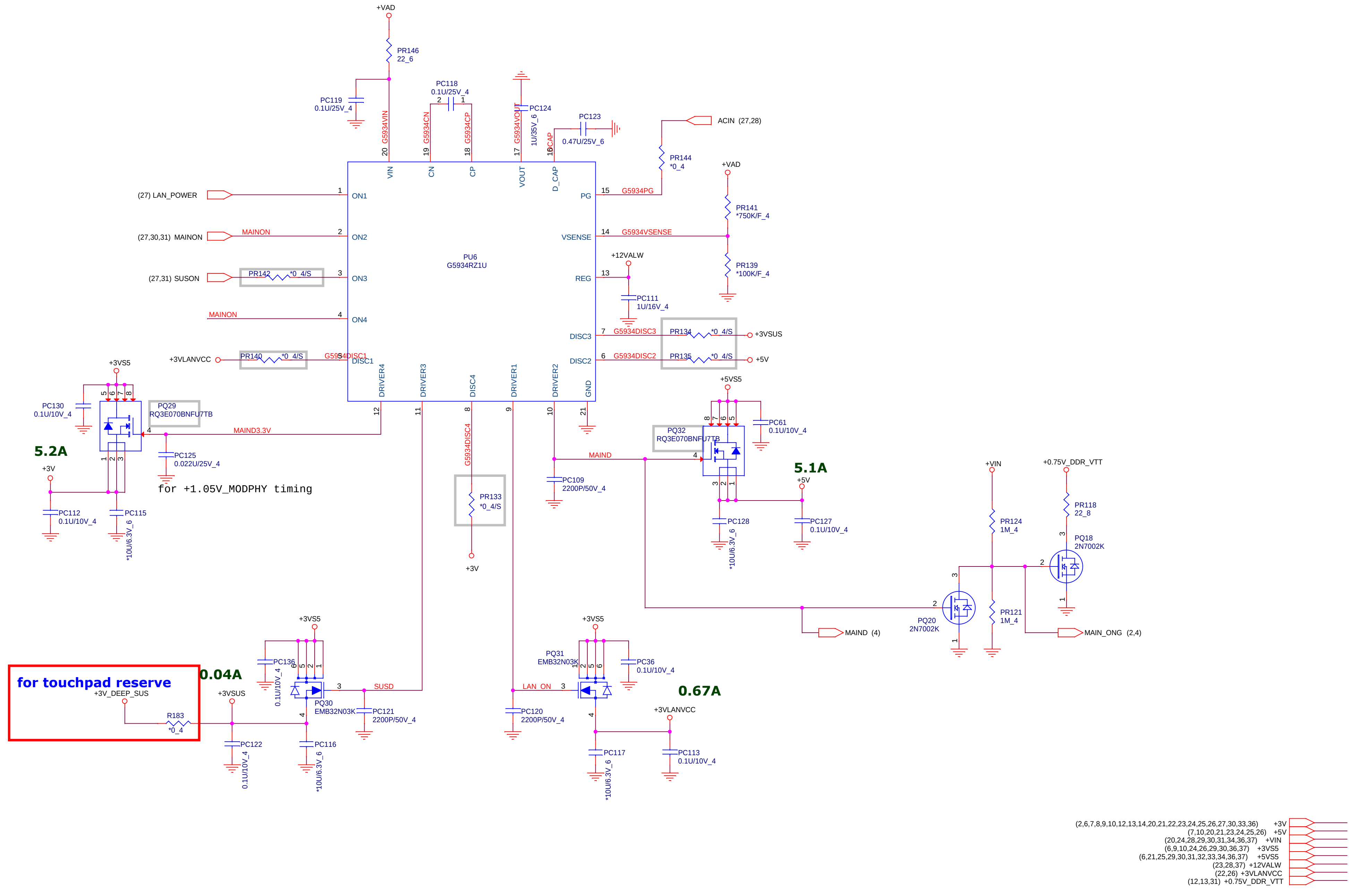


+VCC_CORE (ULV 17W)

Countinue current:16A
Peak current: 33A
Load Line : -2.9mV/A



+VCC_GFX
Countinue current:21.5A
Peak current: 33A
Load Line : -3.9mV/A



PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A

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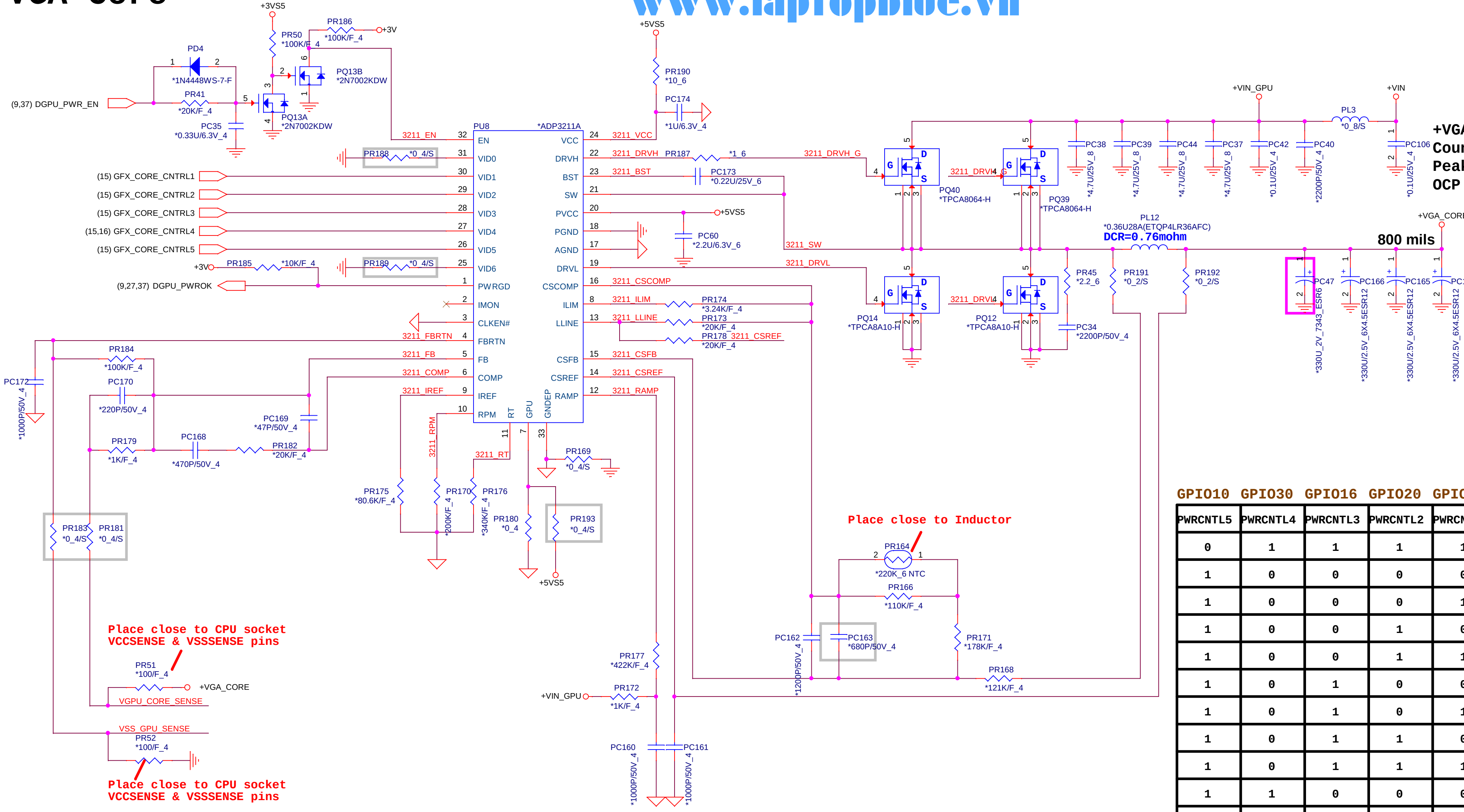
VGA Core



+VGA +/- 5%
Countinue current:21A
Peak current:27A
OCP minimum 33A

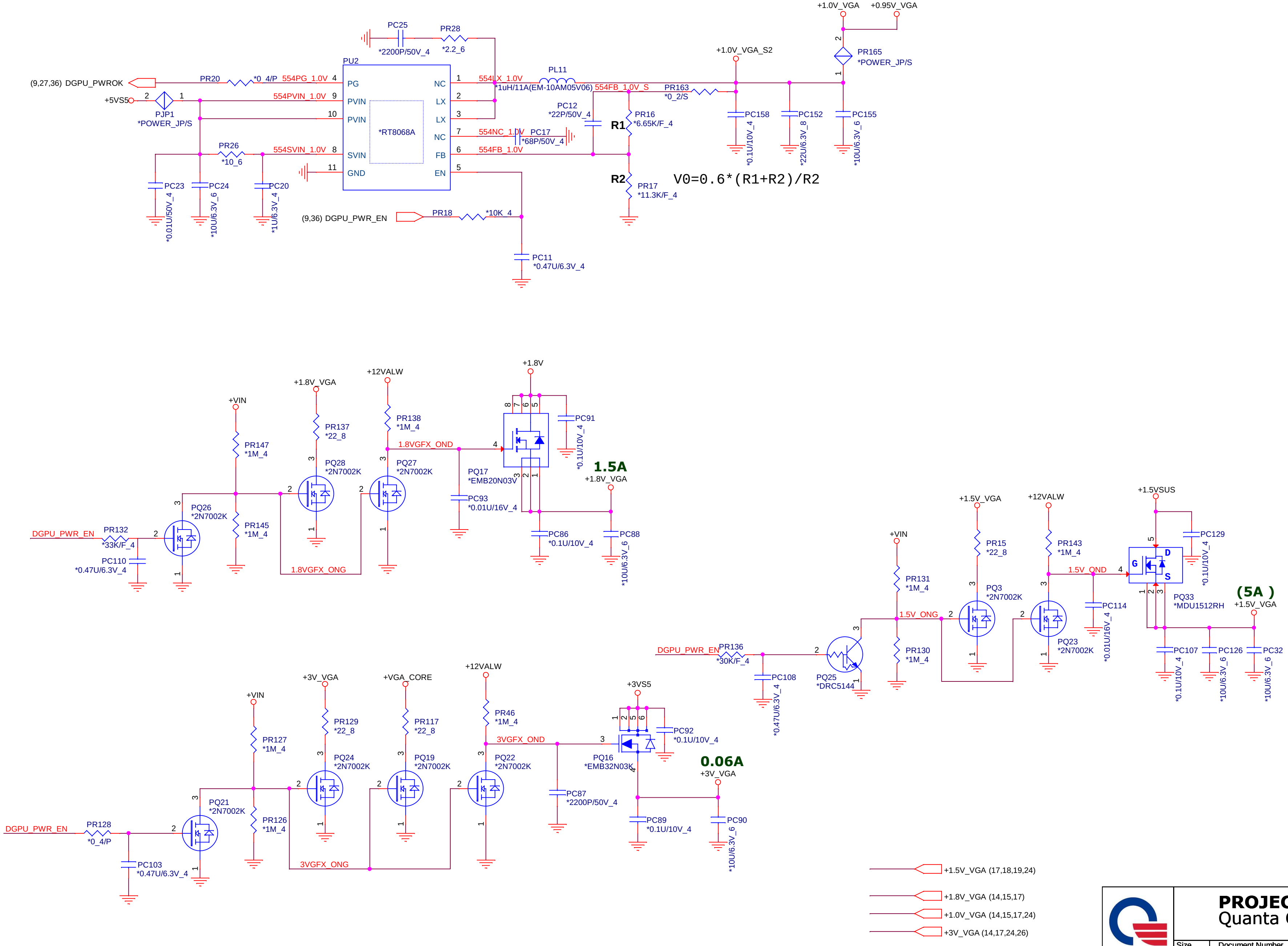
GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V Default
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

PROJECT :U81
Quanta Computer Inc.

Size: Custom | Document Number: +VGACORE (ADP3211) | Rev: 1A

VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V_VGA/1.8V_VGA/3V_VGA	1A
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