LCFC

NM_B681 M/B Schematics Document

AMD FP5 Raven Ridge SoC with DDRIV

AMD R17M-P1-50/R18M-M2-60

2017-09-6

REV:1.0

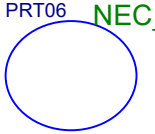
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	Cover Page		
Size: Custom	Document Number: 330ARR		Rev: 1.0
Date: Friday, March 23, 2018	Sheet 1 of 52		

PRT06 NEC_UMA@

0_0402_5%
SD02800008J

PRT06 NEC_R17@



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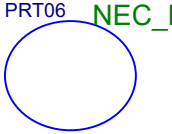

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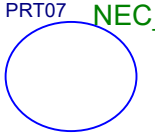

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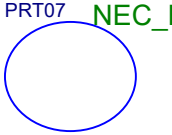

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PRT08 NEC_R18@

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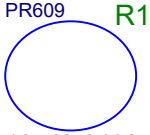
PR609 R18@



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Size A	Document Number <Doc>	Rev 1.0
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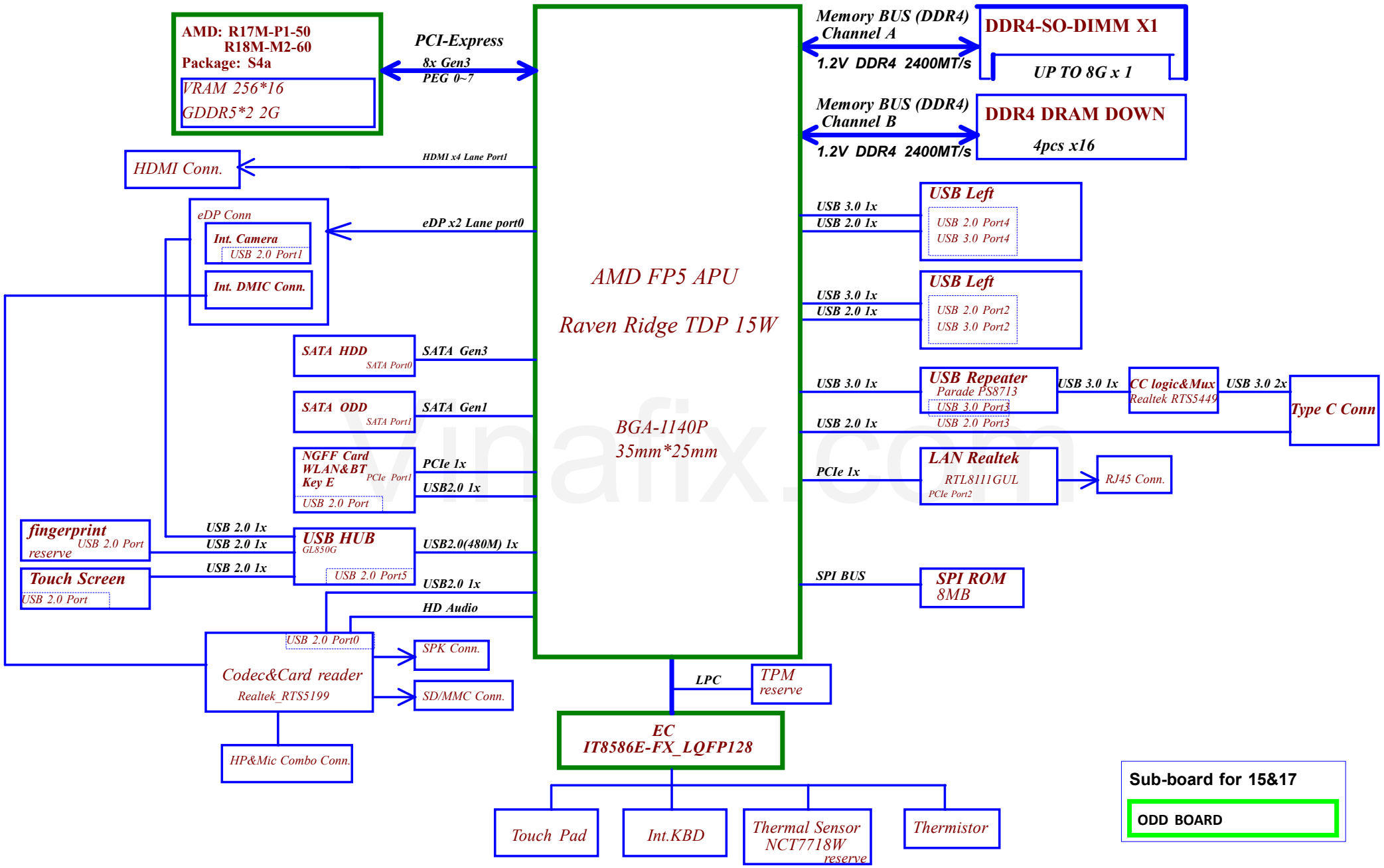

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **Block Diagram**

Size	Document Number	Rev
Custom	330ARR	1.0

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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.9VALW	+1.2V	+5VS +3VS +1.8VS +0.9VS +0.6VS +2.5VS +VDDC_VDD +VDDCR_SOC +VDDC +VDDCI +3VGS +1.8VGS +1.35VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

I2C Control Table

	SOURCE	Device
TP_I2C0_SCL TP_I2C0_SDA	APU +3VALW	Touch Pad +3VS

APU I2C address

Device		Address
Elan: SA469 D 22 HA	69x104x1 0	?
Synaptics: T M P3255 008	69x104x1 0	?

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8586 +3VL	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586 +3VL	X	X		X	X	V +3VS	X	X	V
EC_SMB_CK3 EC_SMB_DA3	IT8586 +3VS	V +3VS_VGA	X		X	X	X	V	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X

EC SM Bus1 address

Device	Address
Battery	?
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
PMIC	0X34
Thermal Sensor	1001_100xb(reserve)

EC SM Bus3 address

Device	Address
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

APU SM Bus address

Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

Port List

HSIO Port		Device
GPP	0	WLAN
	1	LAN
	2	N/A
	3	N/A
	4	N/A
	5	N/A
	6	HDD
	7	ODD
GFX	0	GPU
	1	
	2	
	3	
	4	
	5	
	6	
	7	
USB3.0	0	N/A
	1	Type C
	2	LEFT USB (3.0) lower
	3	LEFT USB (3.0) upper
	4	N/A
USB2.0	0	Card Reader
	1	Type C
	2	LEFT USB (3.0) lower
	3	LEFT USB (3.0) upper
	4	USB HUB(Camera,FP,Touch)
	5	BT

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
EMC@	EMC Part
EMC_NS@	EMC reserve Part
RF@	RF Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
R17M-P1@	R17M-P1-50 SKU part
R18M-M2@	R18M-M2-60 SKU part
TPM@	TPM part
KBL@	Keyboard backlight part
HDT@	HDT Debug part
REDRV@	Redriver part
USB_HUB@	USB HUB part
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
HDMI@	HDMI Logo

VRAM (S2G@, M2G@, H2G@)

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Title: **Notes List**

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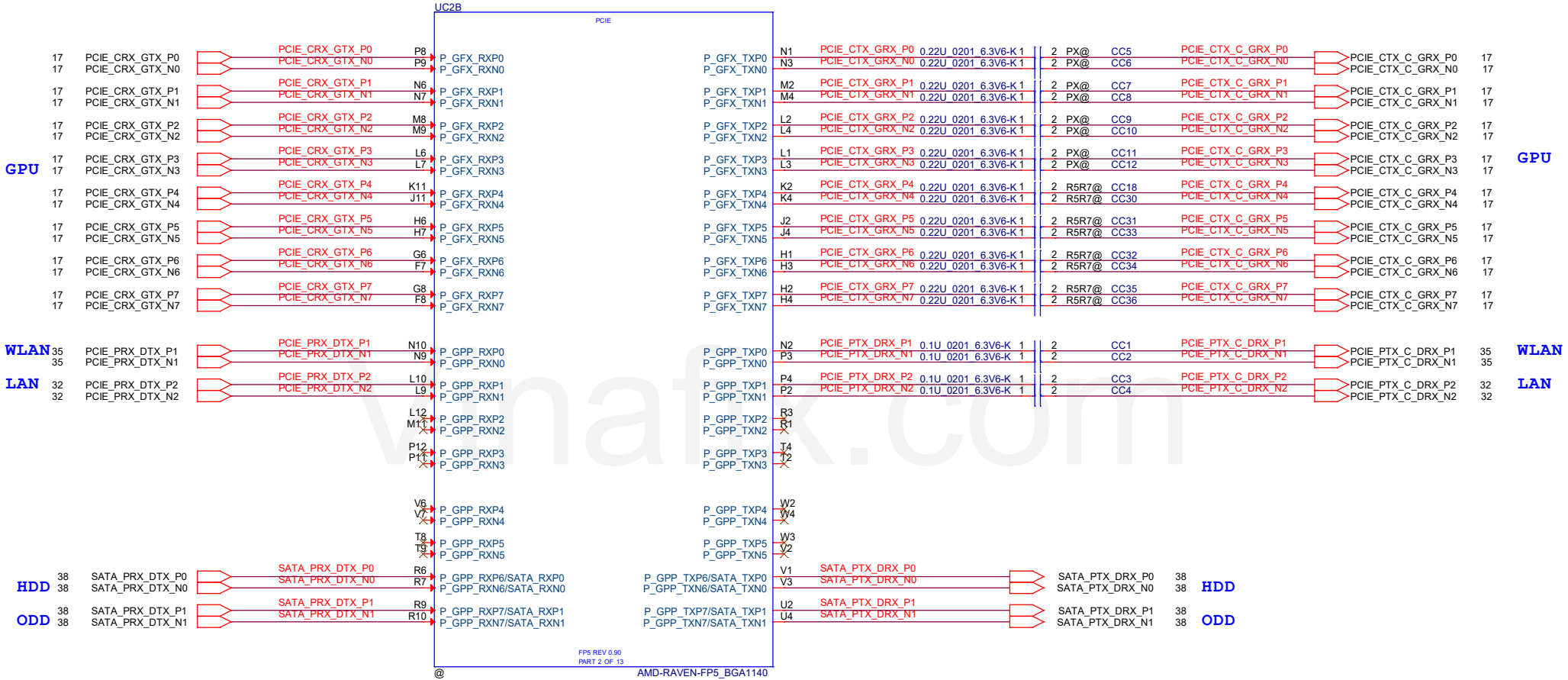

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Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **FP5 (PCIE SATA I/F)**

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DQ bit swapping is allowed in a byte lane.

APU	SO-DIMM	DRAM
DA32	DQ39	UD3.1
DA33	DQ36	UD3.6
DA34	DQ35	UD3.2
DA35	DQ34	UD3.7
DA36	DQ37	UD3.5
DA37	DQ32	UD3.3
DA38	DQ38	UD3.4
DA39	DQ33	UD3.0
DA40	DQ45	UD3.15
DA41	DQ44	UD3.9
DA42	DQ47	UD3.14
DA43	DQ46	UD3.8
DA44	DQ40	UD3.13
DA45	DQ41	UD3.11
DA46	DQ43	UD3.12
DA47	DQ42	UD3.10
DA48	DQ55	UD4.0
DA49	DQ49	UD4.3
DA50	DQ54	UD4.2
DA51	DQ48	UD4.7
DA52	DQ53	UD4.5
DA53	DQ52	UD4.1
DA54	DQ50	UD4.6
DA55	DQ51	UD4.4
DA56	DQ61	UD4.14
DA57	DQ56	UD4.10
DA58	DQ63	UD4.11
DA59	DQ58	UD4.12
DA60	DQ60	UD4.13
DA61	DQ57	UD4.9
DA62	DQ59	UD4.15
DA63	DQ62	UD4.8

APU	SO-DIMM	DRAM
DA0	DQ2	UD1.0
DA1	DQ7	UD1.3
DA2	DQ6	UD1.4
DA3	DQ0	UD1.5
DA4	DQ1	UD1.2
DA5	DQ5	UD1.7
DA6	DQ4	UD1.1
DA7	DQ3	UD1.6
DA8	DQ12	UD1.11
DA9	DQ13	UD1.9
DA10	DQ11	UD1.12
DA11	DQ10	UD1.14
DA12	DQ9	UD1.13
DA13	DQ8	UD1.15
DA14	DQ15	UD1.8
DA15	DQ14	UD1.10
DA16	DQ20	UD2.7
DA17	DQ16	UD2.3
DA18	DQ19	UD2.4
DA19	DQ18	UD2.1
DA20	DQ17	UD2.0
DA21	DQ21	UD2.2
DA22	DQ22	UD2.6
DA23	DQ23	UD2.5
DA24	DQ24	UD2.9
DA25	DQ28	UD2.11
DA26	DQ30	UD2.12
DA27	DQ26	UD2.8
DA28	DQ25	UD2.13
DA29	DQ29	UD2.15
DA30	DQ27	UD2.14
DA31	DQ31	UD2.10

SO-DIMM

Memory down

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Title: FP5 (MEM)

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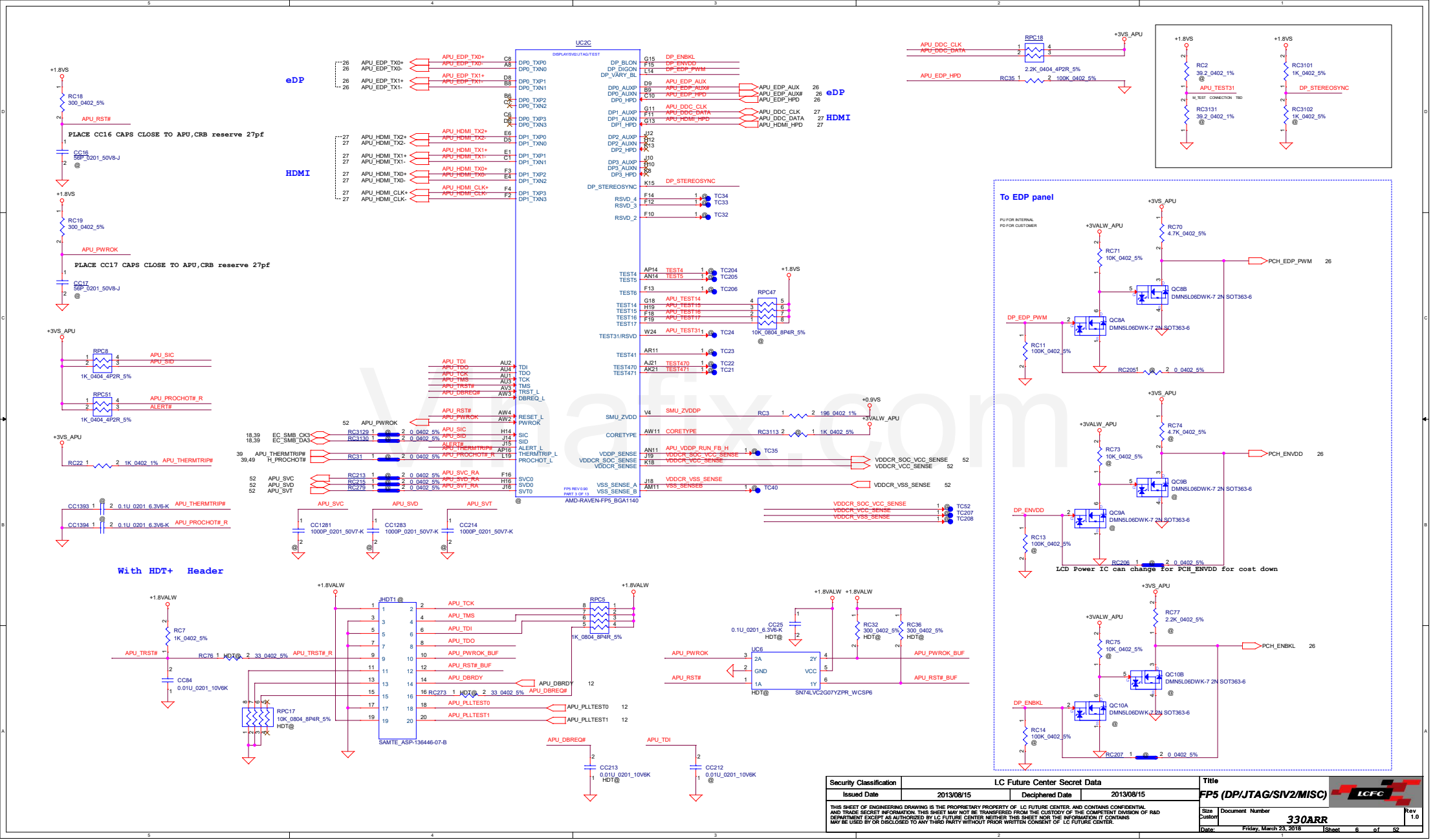
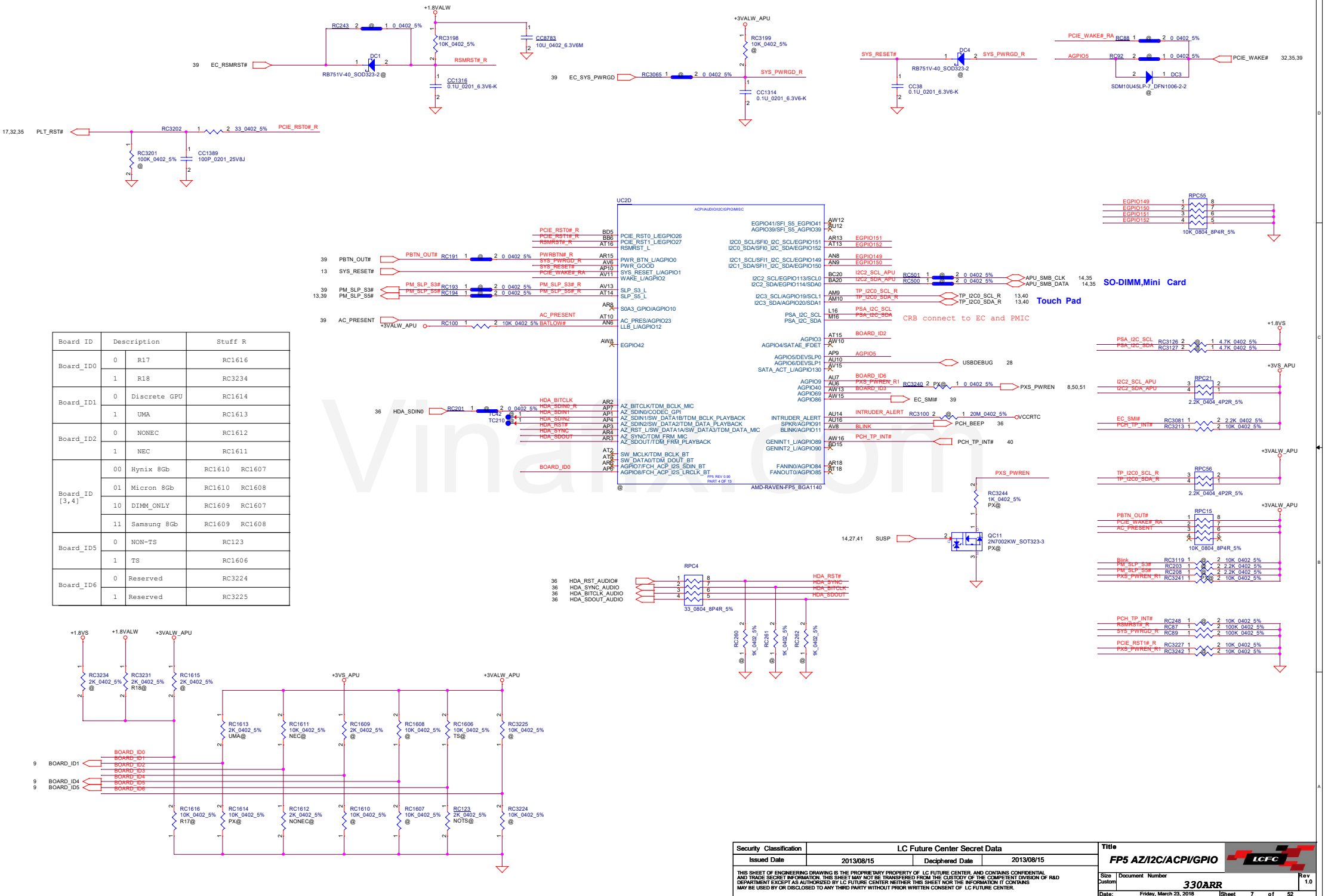


Title: FP5 (DP/JTAG/SIV2/MISC)
Size: Custom | Document Number: 330ARR | Rev: 1.0
Date: Friday, March 23, 2018 | Sheet 6 of 52



Board_ID	Description		Stuff R
Board_ID0	0	R17	RC1616
	1	R18	RC3234
Board_ID1	0	Discrete GPU	RC1614
	1	UMA	RC1613
Board_ID2	0	NONEC	RC1612
	1	NEC	RC1611
Board_ID [3,4]	00	Hynix 8Gb	RC1610 RC1607
	01	Micron 8Gb	RC1610 RC1608
	10	DIMM_ONLY	RC1609 RC1607
	11	Samsung 8Gb	RC1609 RC1608
Board_ID5	0	NON-TS	RC123
	1	TS	RC1606
Board_ID6	0	Reserved	RC3224
	1	Reserved	RC3225

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Title: FP5 AZ/I2C/ACPI/GPIO

Size: Custom | Document Number: 330ARR | Rev: 1.0

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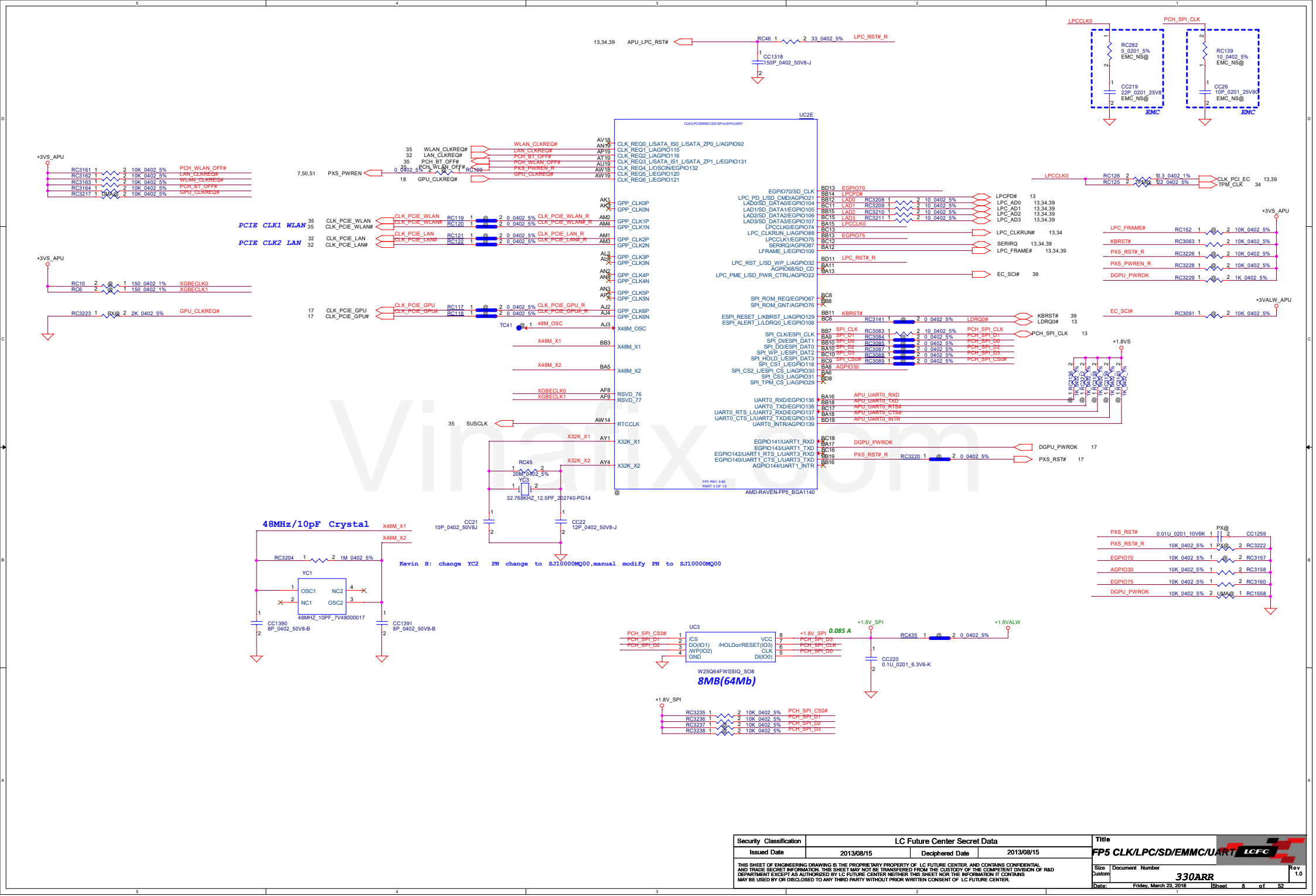

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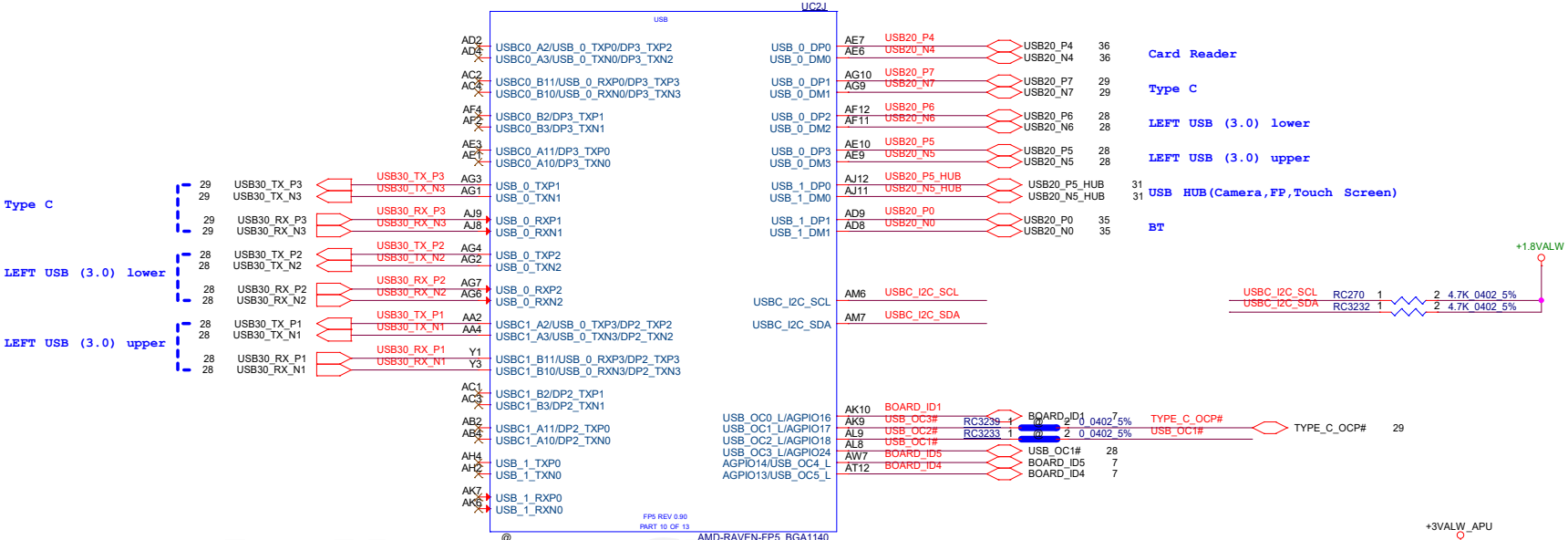
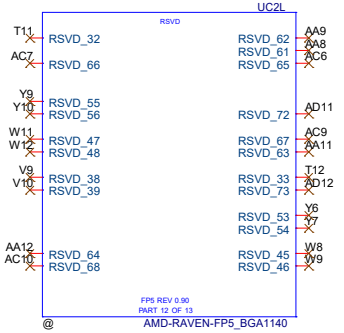
Title	FP5 CLK/LPC/SD/EMMC/UART		
Size: Custom	Document Number: 330ARR		Rev: 1.0
Date: Friday, March 23, 2018	Sheet 8 of 52		





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **FP5 USB/WIFI**

Size	Document Number	Rev
Custom	330ARR	1.0

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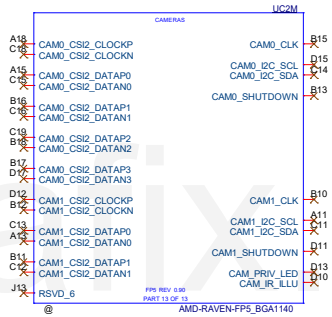

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **FP5 CAM**

Size	Document Number	Rev
C	330ARR	1.0

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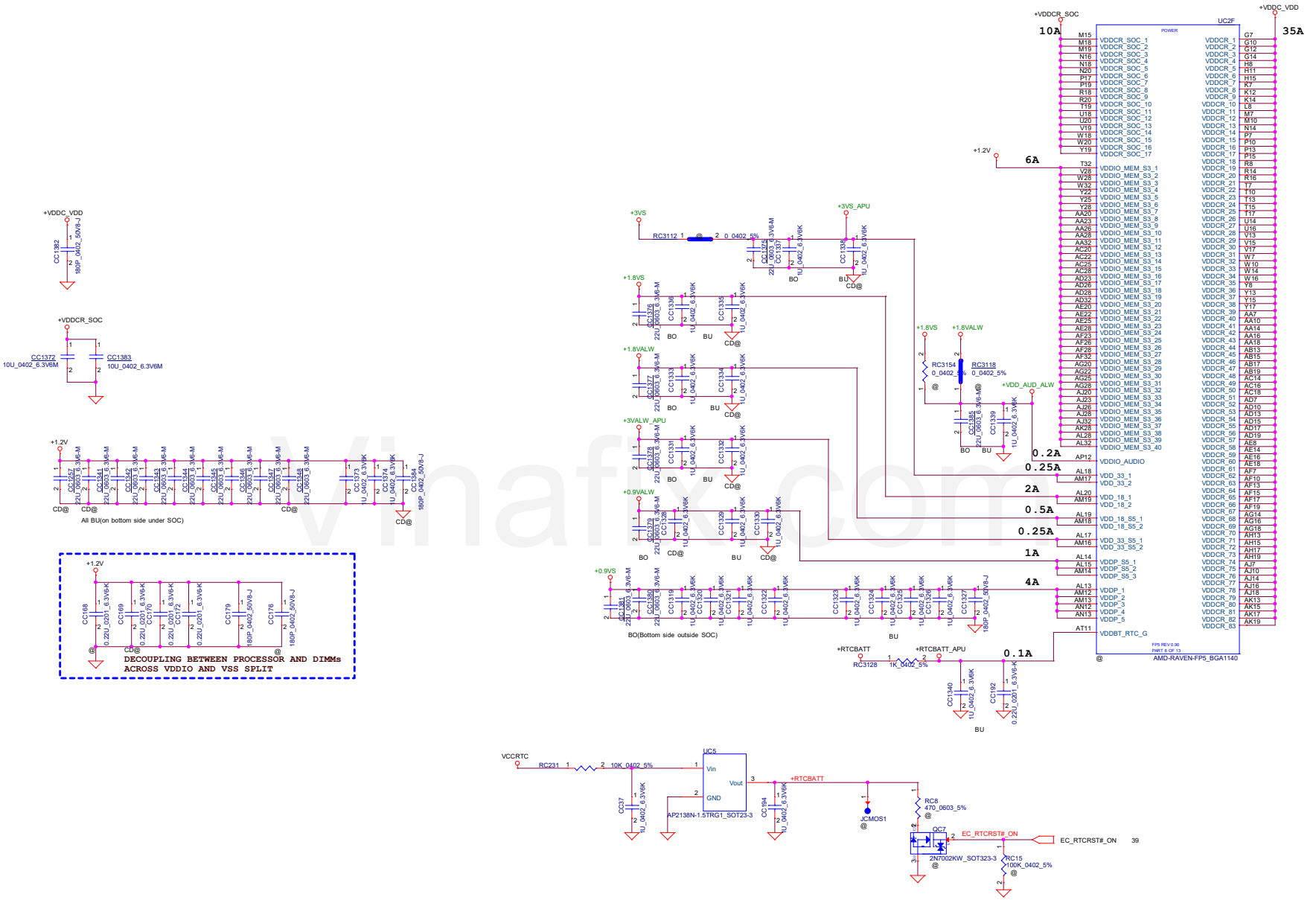

Security Classification	LC Future Center Secret Data		
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Title: FP5 POWER

Size	Document Number	Rev
Custom	330ARR	1.0

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Title: **FP5 GND**

Size	Document Number	Rev
C	330ARR	1.0
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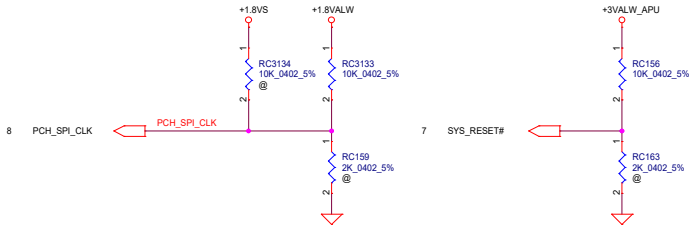
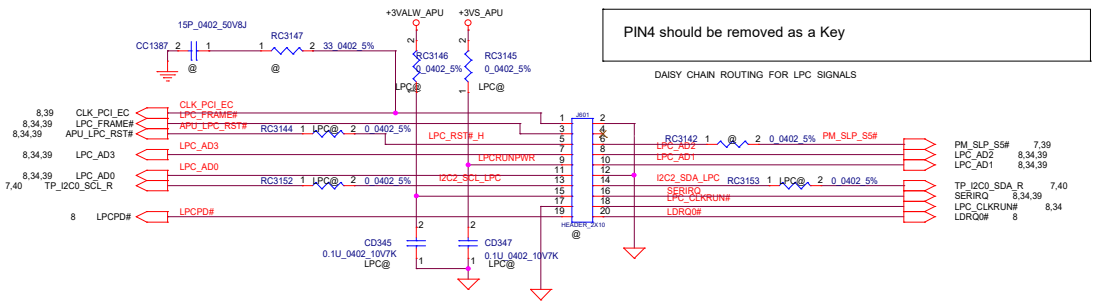
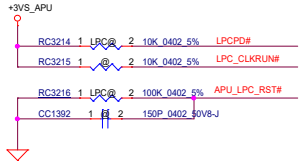


STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

LPC ROM EMULATOR HEADER





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: *FP5 Straps*

Size	Document Number	Rev
C	330ARR	1.0

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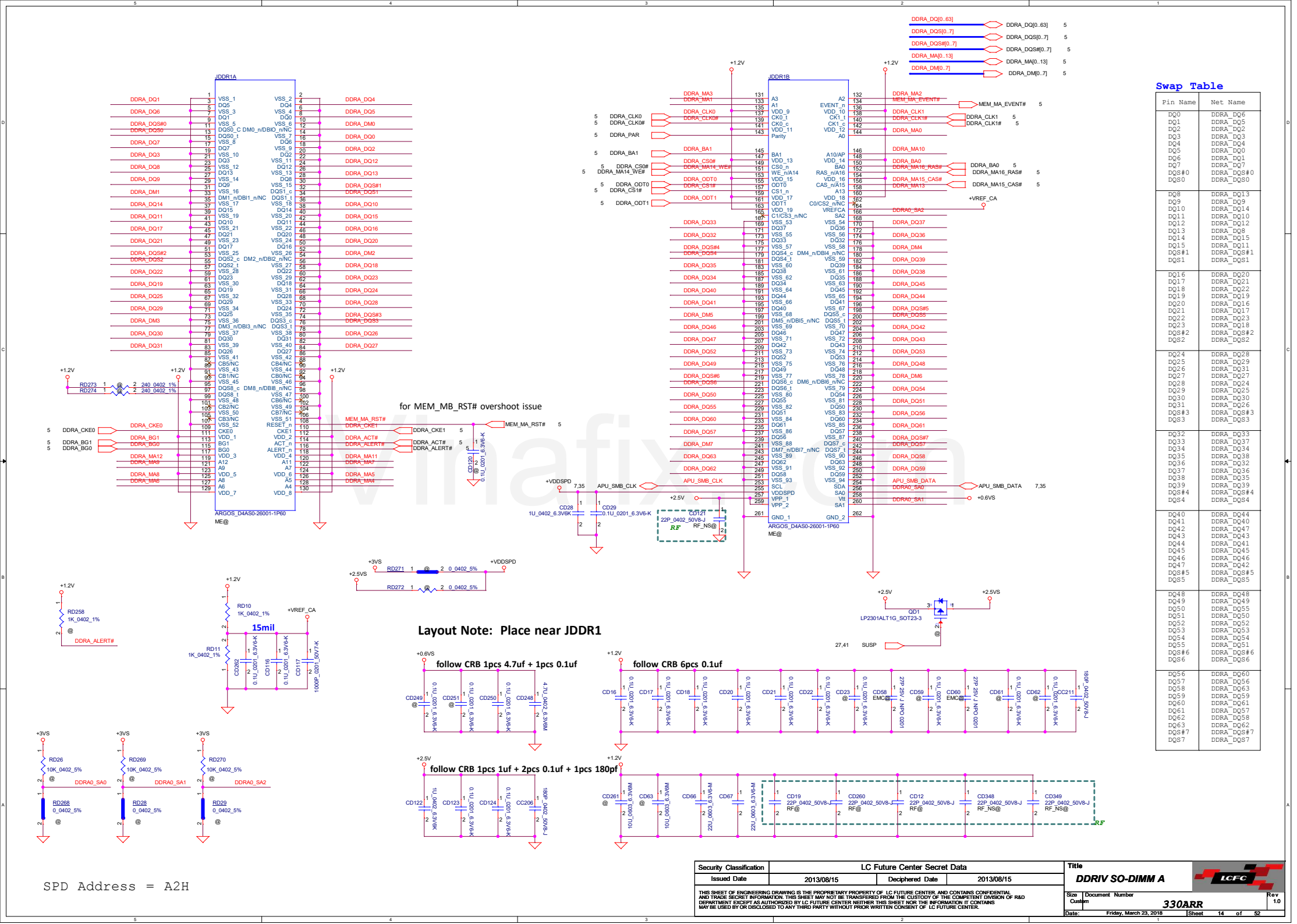

Swap Table

Pin Name	Net Name
DQ0	DDRA_DQ6
DQ1	DDRA_DQ5
DQ2	DDRA_DQ2
DQ3	DDRA_DQ3
DQ4	DDRA_DQ4
DQ5	DDRA_DQ0
DQ6	DDRA_DQ1
DQ7	DDRA_DQ7
DQS#0	DDRA_DQS#0
DQS0	DDRA_DQS0
DQ8	DDRA_DQ13
DQ9	DDRA_DQ9
DQ10	DDRA_DQ14
DQ11	DDRA_DQ10
DQ12	DDRA_DQ12
DQ13	DDRA_DQ8
DQ14	DDRA_DQ15
DQ15	DDRA_DQ11
DQS#1	DDRA_DQS#1
DQS1	DDRA_DQS1
DQ16	DDRA_DQ20
DQ17	DDRA_DQ21
DQ18	DDRA_DQ22
DQ19	DDRA_DQ19
DQ20	DDRA_DQ16
DQ21	DDRA_DQ17
DQ22	DDRA_DQ23
DQ23	DDRA_DQ18
DQS#2	DDRA_DQS#2
DQS2	DDRA_DQS2
DQ24	DDRA_DQ28
DQ25	DDRA_DQ29
DQ26	DDRA_DQ31
DQ27	DDRA_DQ27
DQ28	DDRA_DQ24
DQ29	DDRA_DQ25
DQ30	DDRA_DQ30
DQ31	DDRA_DQ26
DQS#3	DDRA_DQS#3
DQS3	DDRA_DQS3
DQ32	DDRA_DQ33
DQ33	DDRA_DQ37
DQ34	DDRA_DQ34
DQ35	DDRA_DQ38
DQ36	DDRA_DQ32
DQ37	DDRA_DQ36
DQ38	DDRA_DQ35
DQ39	DDRA_DQ30
DQS#4	DDRA_DQS#4
DQS4	DDRA_DQS4
DQ40	DDRA_DQ44
DQ41	DDRA_DQ40
DQ42	DDRA_DQ47
DQ43	DDRA_DQ43
DQ44	DDRA_DQ41
DQ45	DDRA_DQ45
DQ46	DDRA_DQ46
DQ47	DDRA_DQ42
DQS#5	DDRA_DQS#5
DQS5	DDRA_DQS5
DQ48	DDRA_DQ48
DQ49	DDRA_DQ49
DQ50	DDRA_DQ55
DQ51	DDRA_DQ50
DQ52	DDRA_DQ52
DQ53	DDRA_DQ53
DQ54	DDRA_DQ54
DQ55	DDRA_DQ51
DQS#6	DDRA_DQS#6
DQS6	DDRA_DQS6
DQ56	DDRA_DQ60
DQ57	DDRA_DQ56
DQ58	DDRA_DQ63
DQ59	DDRA_DQ61
DQ60	DDRA_DQ61
DQ61	DDRA_DQ57
DQ62	DDRA_DQ58
DQ63	DDRA_DQ62
DQS#7	DDRA_DQS#7
DQS7	DDRA_DQS7

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Title	DDRIV SO-DIMM A		
Size: Custom	Document Number: 330ARR		Rev: 1.0
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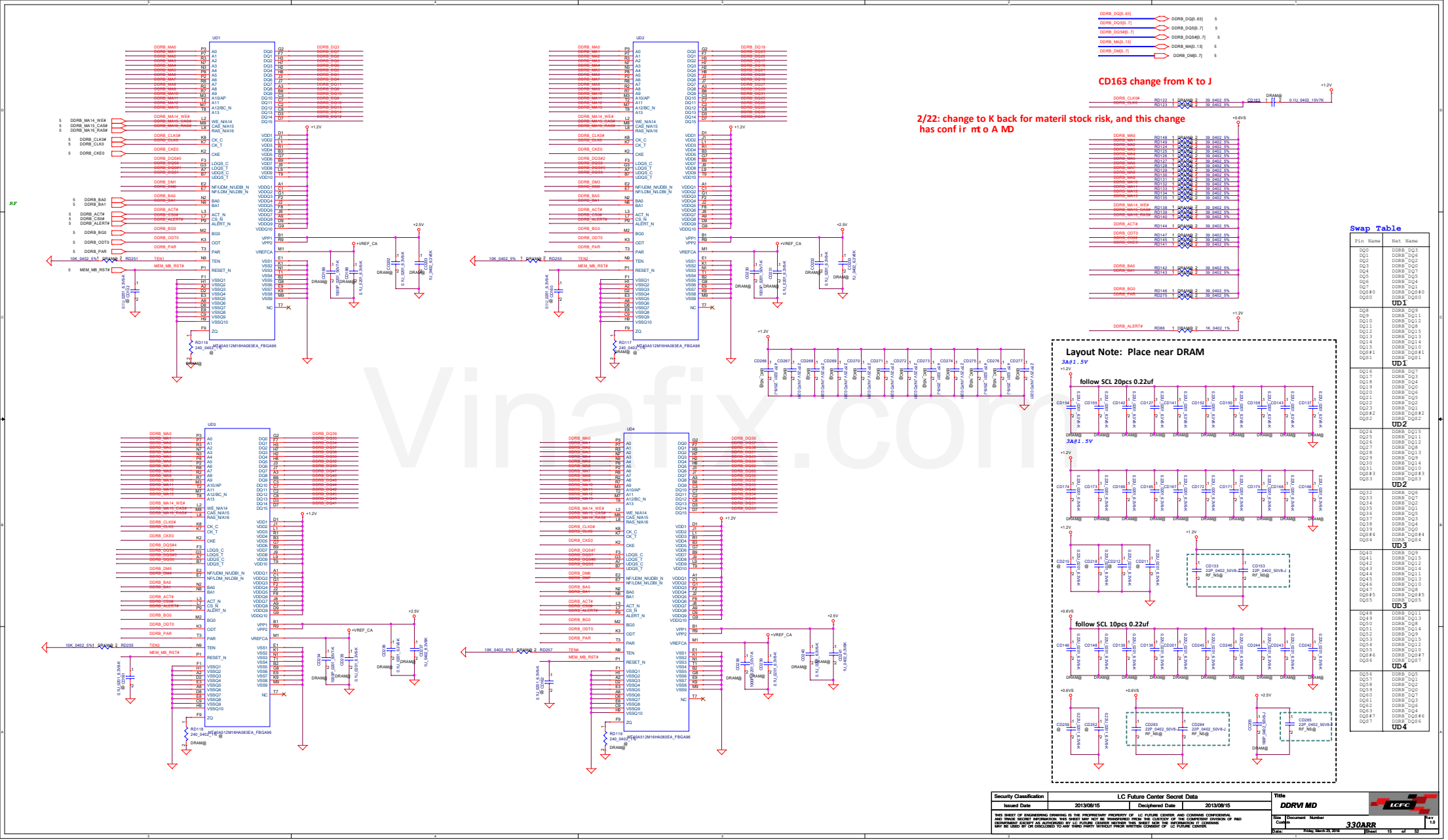
DDRB_DQ[0..63]
DDRB_DQS[0..7]
DDRB_DQS#[0..7]
DDRB_MA[0..15]
DDRB_DM[0..7]
DDRB_DQ[0..63] 5
DDRB_DQS[0..7] 5
DDRB_DQS#[0..7] 5
DDRB_MA[0..13] 5
DDRB_DM[0..7] 5
CD163 change from K to J
2/22: change to K back for materil stock risk, and this change has confir mt o A MD
UD1
UD2
UD3
UD4
MT40A512M16HA083EA_FBGA96
Swap Table
Pin Name
Net Name
DQ0 DDRB_DQ3
DQ1 DDRB_DQ6
DQ2 DDRB_DQ2
DQ3 DDRB_DQ7
DQ4 DDRB_DQ5
DQ5 DDRB_DQ4
DQ6 DDRB_DQ1
DQ7 DDRB_DQ0
DQM0 DDRB_DQS#0
DQS0 DDRB_DQS0
UD1
DQ8 DDRB_DQ9
DQ9 DDRB_DQ11
DQ10 DDRB_DQ12
DQ11 DDRB_DQ8
DQ12 DDRB_DQ15
DQ13 DDRB_DQ13
DQ14 DDRB_DQ14
DQ15 DDRB_DQ10
DQS#1 DDRB_DQS#1
DQS1 DDRB_DQS1
UD1
DQ16 DDRB_DQ7
DQ17 DDRB_DQ3
DQ18 DDRB_DQ4
DQ19 DDRB_DQ0
DQ20 DDRB_DQ6
DQ21 DDRB_DQ5
DQ22 DDRB_DQ2
DQ23 DDRB_DQ1
DQS#2 DDRB_DQS#2
DQS2 DDRB_DQS2
UD2
DQ24 DDRB_DQ15
DQ25 DDRB_DQ11
DQ26 DDRB_DQ12
DQ27 DDRB_DQ8
DQ28 DDRB_DQ13
DQ29 DDRB_DQ9
DQ30 DDRB_DQ14
DQ31 DDRB_DQ10
DQS#3 DDRB_DQS#3
DQS3 DDRB_DQS3
UD2
DQ32 DDRB_DQ6
DQ33 DDRB_DQ7
DQ34 DDRB_DQ2
DQ35 DDRB_DQ1
DQ36 DDRB_DQ4
DQ37 DDRB_DQ3
DQ38 DDRB_DQ4
DQ39 DDRB_DQ0
DQS#4 DDRB_DQS#4
DQS4 DDRB_DQS4
UD3
DQ40 DDRB_DQ9
DQ41 DDRB_DQ15
DQ42 DDRB_DQ12
DQ43 DDRB_DQ14
DQ44 DDRB_DQ11
DQ45 DDRB_DQ13
DQ46 DDRB_DQ10
DQ47 DDRB_DQ8
DQS#5 DDRB_DQS#5
DQS5 DDRB_DQS5
UD3
DQ48 DDRB_DQ13
DQ49 DDRB_DQ11
DQ50 DDRB_DQ9
DQ51 DDRB_DQ14
DQ52 DDRB_DQ8
DQ53 DDRB_DQ15
DQ54 DDRB_DQ12
DQ55 DDRB_DQ10
DQS#6 DDRB_DQS#7
DQS6 DDRB_DQS7
UD4
DQ56 DDRB_DQ5
DQ57 DDRB_DQ1
DQ58 DDRB_DQ2
DQ59 DDRB_DQ0
DQ60 DDRB_DQ7
DQ61 DDRB_DQ3
DQ62 DDRB_DQ6
DQ63 DDRB_DQ4
DQS#7 DDRB_DQS#6
DQS7 DDRB_DQS6
UD4
Layout Note: Place near DRAM
3A@1.5V
follow SCL 20pcs 0.22uf
3A@1.5V
follow SCL 10pcs 0.22uf
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/15
Deciphered Date
2013/08/15
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Title
DDRVI MD
Size
Custom
Document Number
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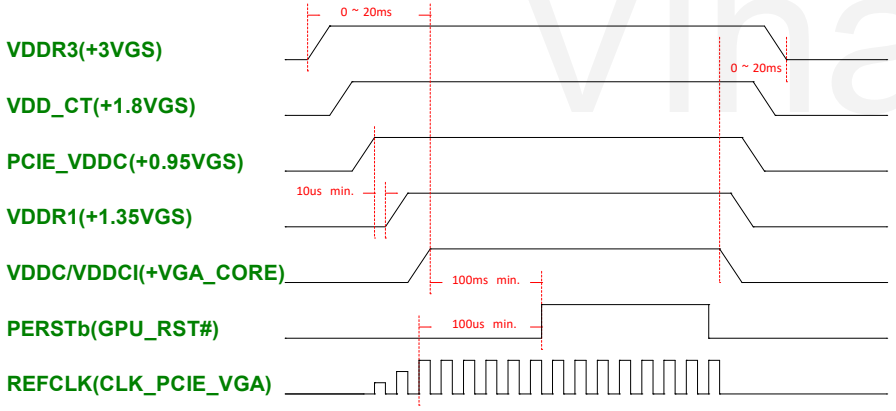
Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.
It is recommended that the 3.3-V rail ramp up first.
The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.
The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μ s).
For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

GPU	Memory Type		BOARD_CONFIG[2:0] DBGDATA_[5..3]	VRAM ID PS_3[3:1]	Stuff R
R17M-P1-50	8Gb GDDR5 256M x 32 (UV3/UV4)	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	000	NA	RV1307 RV1304 RV1298
		Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	001	NA	RV1307 RV1304 RV1297
		Micron MT51J256M32HF-70:A 6.0Gbps@1.35V	010	NA	RV1307 RV1303 RV1298
R18M-M2-60	8Gb GDDR5 256M x 32 (UV3/UV4)	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	NA	000	RV1415(NC) RV1418(4.75K)
		Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	NA	001	RV1415(8.45K) RV1418(2K)
		Micron MT51J256M32HF-70:A 6.0Gbps@1.35V	NA	010	RV1415(4.53K) RV1418(2K)

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Title: VGA Notes List

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4 PCIE_CTX_C_GRX_P[0..7]
4 PCIE_CTX_C_GRX_N[0..7]

PCIE_CRX_GTX_P[0..7] 4
PCIE_CRX_GTX_N[0..7] 4

UV1B
symbol2

PCIE_CTX_C_GRX_P0	AT41	PCIE_RX0P	PCIE_TX0P	AV35	PCIE_CRX_C_GTX_P0	PX@	CV1	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P0
PCIE_CTX_C_GRX_N0	AT40	PCIE_RX0N	PCIE_TX0N	AU35	PCIE_CRX_C_GTX_N0	PX@	CV2	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N0
PCIE_CTX_C_GRX_P1	AR41	PCIE_RX1P	PCIE_TX1P	AU38	PCIE_CRX_C_GTX_P1	PX@	CV3	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P1
PCIE_CTX_C_GRX_N1	AR40	PCIE_RX1N	PCIE_TX1N	AU39	PCIE_CRX_C_GTX_N1	PX@	CV4	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N1
PCIE_CTX_C_GRX_P2	AP41	PCIE_RX2P	PCIE_TX2P	AR37	PCIE_CRX_C_GTX_P2	PX@	CV5	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P2
PCIE_CTX_C_GRX_N2	AP40	PCIE_RX2N	PCIE_TX2N	AR38	PCIE_CRX_C_GTX_N2	PX@	CV6	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N2
PCIE_CTX_C_GRX_P3	AM41	PCIE_RX3P	PCIE_TX3P	AN37	PCIE_CRX_C_GTX_P3	PX@	CV7	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P3
PCIE_CTX_C_GRX_N3	AM40	PCIE_RX3N	PCIE_TX3N	AN38	PCIE_CRX_C_GTX_N3	PX@	CV8	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N3
PCIE_CTX_C_GRX_P4	AL41	PCIE_RX4P	PCIE_TX4P	AL37	PCIE_CRX_C_GTX_P4	R5R7@	CV1411	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P4
PCIE_CTX_C_GRX_N4	AL40	PCIE_RX4N	PCIE_TX4N	AL38	PCIE_CRX_C_GTX_N4	R5R7@	CV1381	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N4
PCIE_CTX_C_GRX_P5	AK41	PCIE_RX5P	PCIE_TX5P	AJ37	PCIE_CRX_C_GTX_P5	R5R7@	CV1431	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P5
PCIE_CTX_C_GRX_N5	AK40	PCIE_RX5N	PCIE_TX5N	AJ38	PCIE_CRX_C_GTX_N5	R5R7@	CV1361	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N5
PCIE_CTX_C_GRX_P6	AJ41	PCIE_RX6P	PCIE_TX6P	AG37	PCIE_CRX_C_GTX_P6	R5R7@	CV1401	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P6
PCIE_CTX_C_GRX_N6	AJ40	PCIE_RX6N	PCIE_TX6N	AG38	PCIE_CRX_C_GTX_N6	R5R7@	CV1421	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N6
PCIE_CTX_C_GRX_P7	AH41	PCIE_RX7P	PCIE_TX7P	AE37	PCIE_CRX_C_GTX_P7	R5R7@	CV1371	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_P7
PCIE_CTX_C_GRX_N7	AH40	PCIE_RX7N	PCIE_TX7N	AE38	PCIE_CRX_C_GTX_N7	R5R7@	CV1391	2 0.22U 0201 6.3V6-K	PCIE_CRX_GTX_N7

8 CLK_PCIE_GPU
8 CLK_PCIE_GPU#

CLK_PCIE_GPU	AV33	PCIE_REFCLKP	PERSTB	AV41	GPU_RST#	GPU_RST#	18
CLK_PCIE_GPU#	AU33	PCIE_REFCLKN	PX_EN	AC41	PX_EN	RV1226 1 @ 2 1K_0402_5%	
			PCIE_ZVSS	AU41	PCIE_ZVSS	RV1228 1 PX@ 2 200_0402_1%	

REV 0.91
216-0905018-C3_FCBGA769
@

PX_EN: On/off regulator control signal for BACO mode, internal pull down.
High(3.3V)--switches the regulators off. (enter BACO mode)
Low(0V)--switches the regulators on. (Default)
Can be left unconnected if not used.

+3VALW
+3VGS
+3V_GATE
RV1430 1 @ 2 0_0402_5%
RV1429 1 @ 2 0_0402_5%

RV1236 1 @ 2 0_0402_5%
+3V_GATE
CV122
0.1U_0201_6.3V6-K
@

UV5
8 PXS_RST#
7,32,35 PLT_RST#
PXS_RST#
PLT_RST#
IN1
IN2
VCC
GND
OUT
GPU_RST#
MC74VHC1G08DFT2G_SC70-5
PX@
RV1227
100K_0402_5%
PX@

Need confirm if can NC UV5/RV1227
and stuff RV1236--Brooks 0708

51 VR_VGA_PWRGD
GPU_RST#
VR_VGA_PWRGD
DV6
LBAT54AWT1G_SOT323-3
PX@
VGA_PWROK
VGA_PWROK 51

VR_VGA_PWRGD RV1404 1 @ 2 0_0402_5% DGPU_PWROK 8

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Title: R17M-P1-50_PCIE
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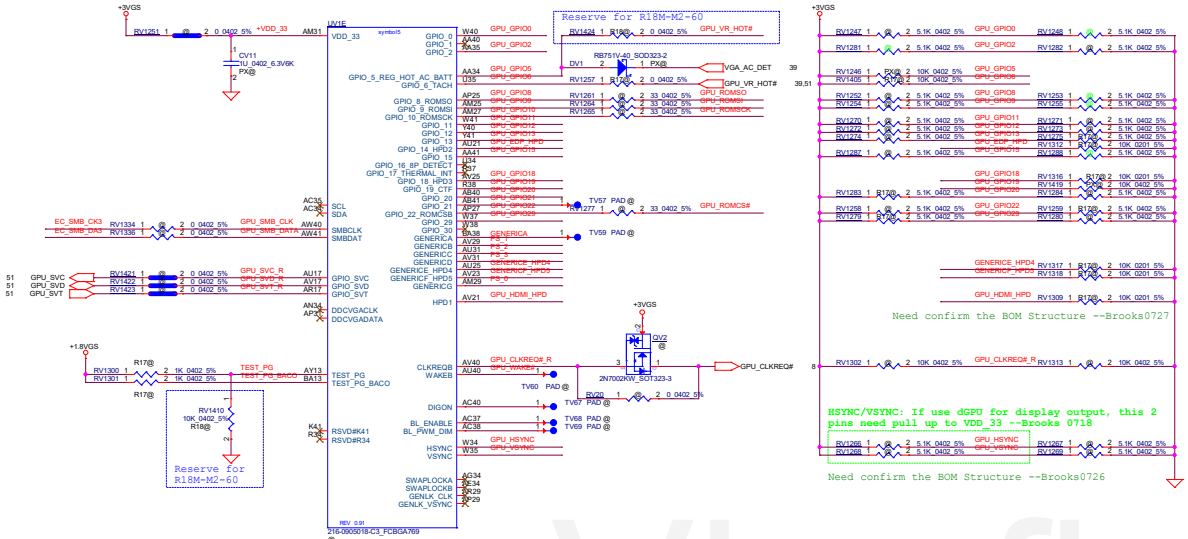


CONFIGURATION STRAPS R17M-P1-50

Any external circuit using these pins must not conflict with the logic level required by the strap after power up until PCIe reset gets de-asserted.

RECOMMENDED SETTINGS
0 = PULL-DOWN TO GND
1 = PULL-UP TO POWER
X = DESIGN DEPENDENT
NA = NOT APPLICABLE

Strap Name	Pin Name	Description	GPU Default	Recommended Settings
TX_HALF_SWING	GPIO_0	Controls the transmitter full/half swing mode. 0: The transmitter fullswing is enabled. 1: The transmitter halfswing is enabled.	0 (Internal pulldown)	0
BIF_GEN3_EN_A	GPIO_2	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.	1 (Internal pull-up)	x
BIF_CLK_PM_EN	GPIO_8 _ROMSO	0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.	0 (Internal pulldown)	1
Reserved	GPIO_9 _ROMSI	Reserved	0 (Internal pulldown)	Must default to 0 for production.
ROM_CONFIG [2:0]	GPIO_13 GPIO_12 GPIO_11	If BIOS_ROM_EN = 1, defines the ROM type. If BIOS_ROM_EN = 0, defines the primary memory aperture size. 001 = 256MB	101 (Internal pull-up /pull-down)	x
Reserved	GPIO_15	Reserved	0 (Internal pulldown)	Must default to 0 for production.
TX_DEEMPH_EN	GPIO_20	PCI Express transmitter de-emphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.	0 (Internal pulldown)	1
BIOS_ROM_EN	GPIO_22 _ROMCSB	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.	1 (Internal pull-up)	x
BIF_VGA_DIS	GPIO_29	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller(for headless designs)	0 (Internal pulldown)	x
Special Usage [1] Special Usage [0]	HSYNC VSYNC	Special usage 00	0 (Internal pulldown)	x
AUD_PORT _CONN[2:0]	DBGDATA_2 DBGDATA_1 DBGDATA_0	Determine the maximum number of digital display audio endpoints that will be presented to the OS and user. 111: No usable endpoints 110: One usable endpoint 101: Two usable endpoints 100: Three usable endpoints 011: Four usable endpoints 010: Five usable endpoints 001: Six usable endpoints 000: All endpoints are usable 111	0 (Internal pulldown)	x
BOARD_CONFIG [2:0]	DBGDATA_5 DBGDATA_4 DBGDATA_3	Provides an option to specify certain board-level specifics to the VBIOS or driver. 000 = Samsung 8Gb 001 = Hynix 8Gb 010 = Micron 8Gb	0 (Internal pulldown)	x
SMBUS_ADDR [1:0]	DBGDATA_7 DBGDATA_6	Provide a strap option to change the SMBUS slave address of the GPU. 00: 0x40 01: 0x41 10: 0x42 11: 0x43 01	0 (Internal pulldown)	X (Strap the address to 0x41 if no conflict)

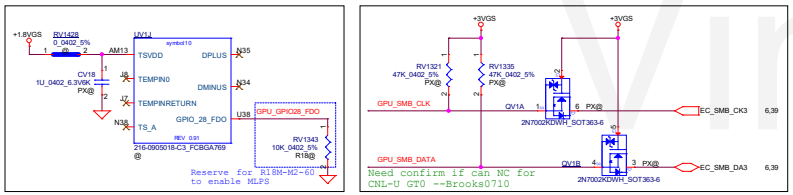
Note: To change the straps from the default values, use pull-up or pull-down resistors of 5.1Kohm (5%) on the PCB

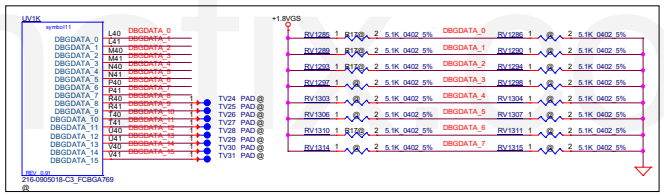
CONFIGURATION STRAPS R18M-M2-60

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

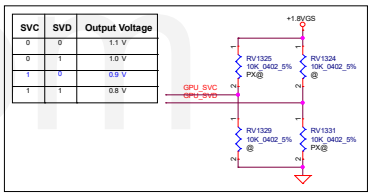
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

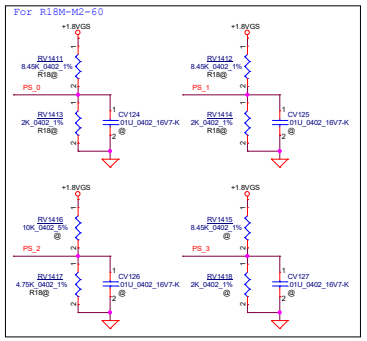
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 001 = 256MB	x
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= GEN3 is supported	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_ FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	x
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	x
PS_2[4]	N/A	Reserved	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Samsung 8Gb 001 = Hynix 8Gb 010 = Micron 8Gb	x
PS_3[4]	N/A	Reserved	1
PS_3[5]	N/A	Reserved	1

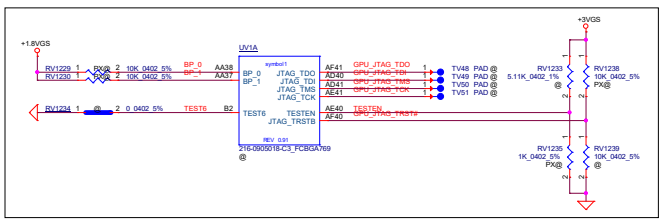


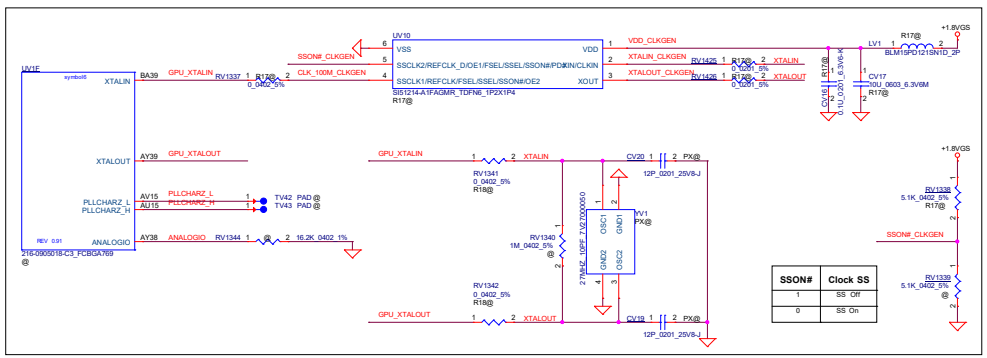


SVC	SVD	Output Voltage
0	0	1.1 V
0	1	1.0 V
1	0	0.9 V
1	1	0.8 V

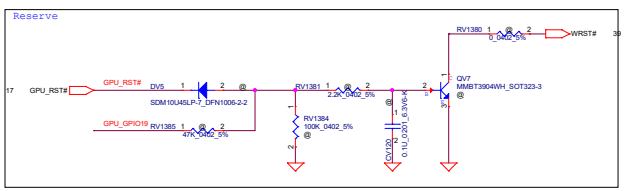


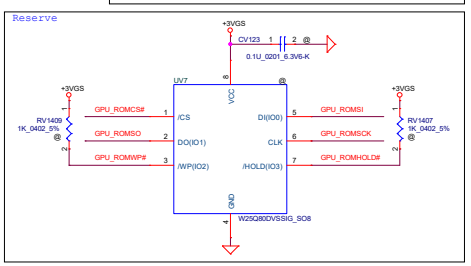






SSON#	Clock SS
1	SS Off
0	SS On





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Title: R17M-P1-50_VRAM I/F

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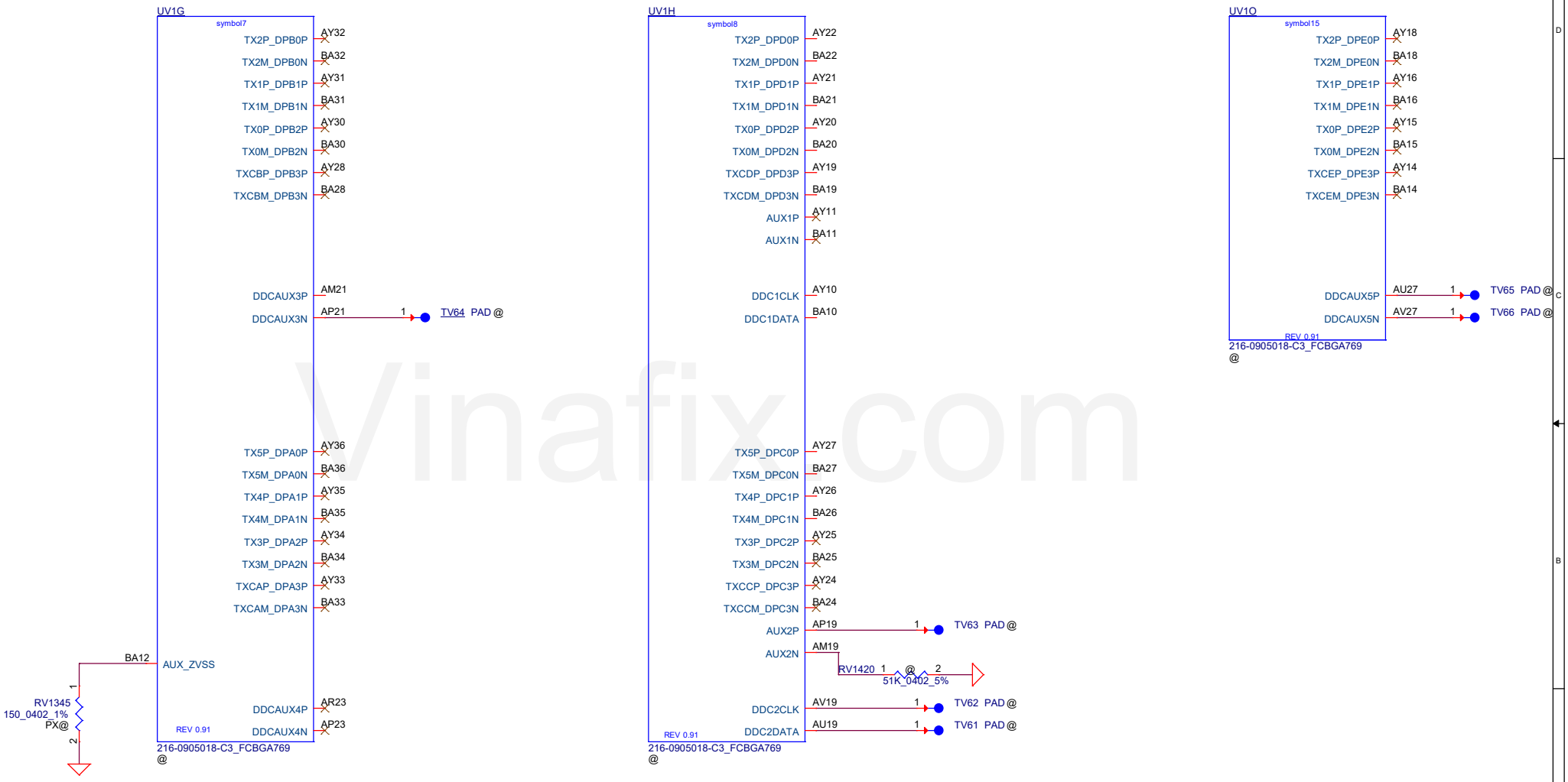

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Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: R17M-P1-50_GPIO

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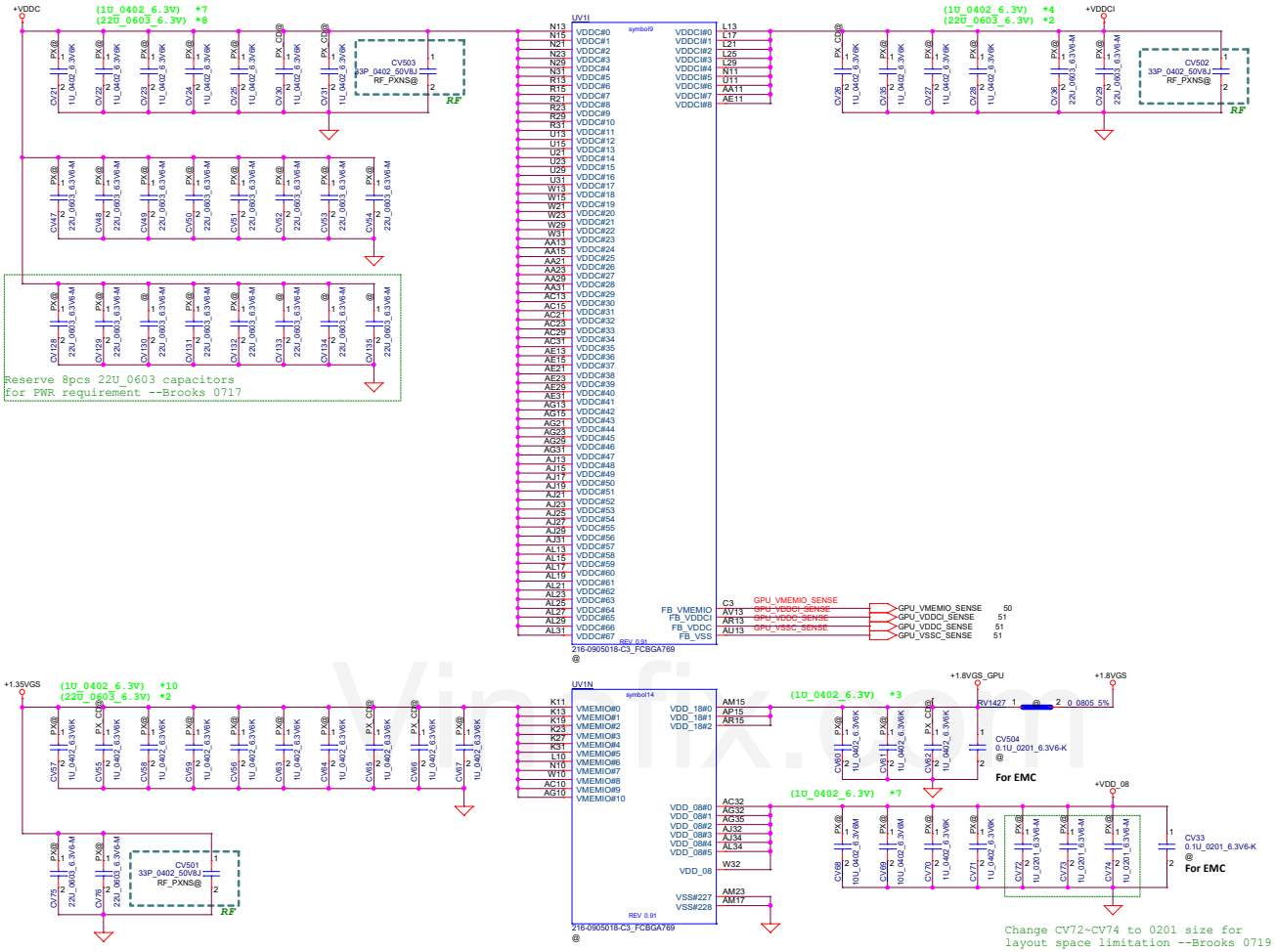

+3VALW TO +3VGS

+3VGS /10mA

MOS. AO3402 VGS
MAX is 12V

+1.8VALW TO +1.8VGS

+1.8VGS /1.0A Rdson<65mohm
Backup is AO3420

Discharge

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Title: *R17M-P1-50_DIGITAL OUT*

Size: Custom | Document Number: *330ARR* | Rev: 1.0

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Title: **R17M-P1-50_PWR**

Size	Document Number	Rev
Custom	330ARR	1.0

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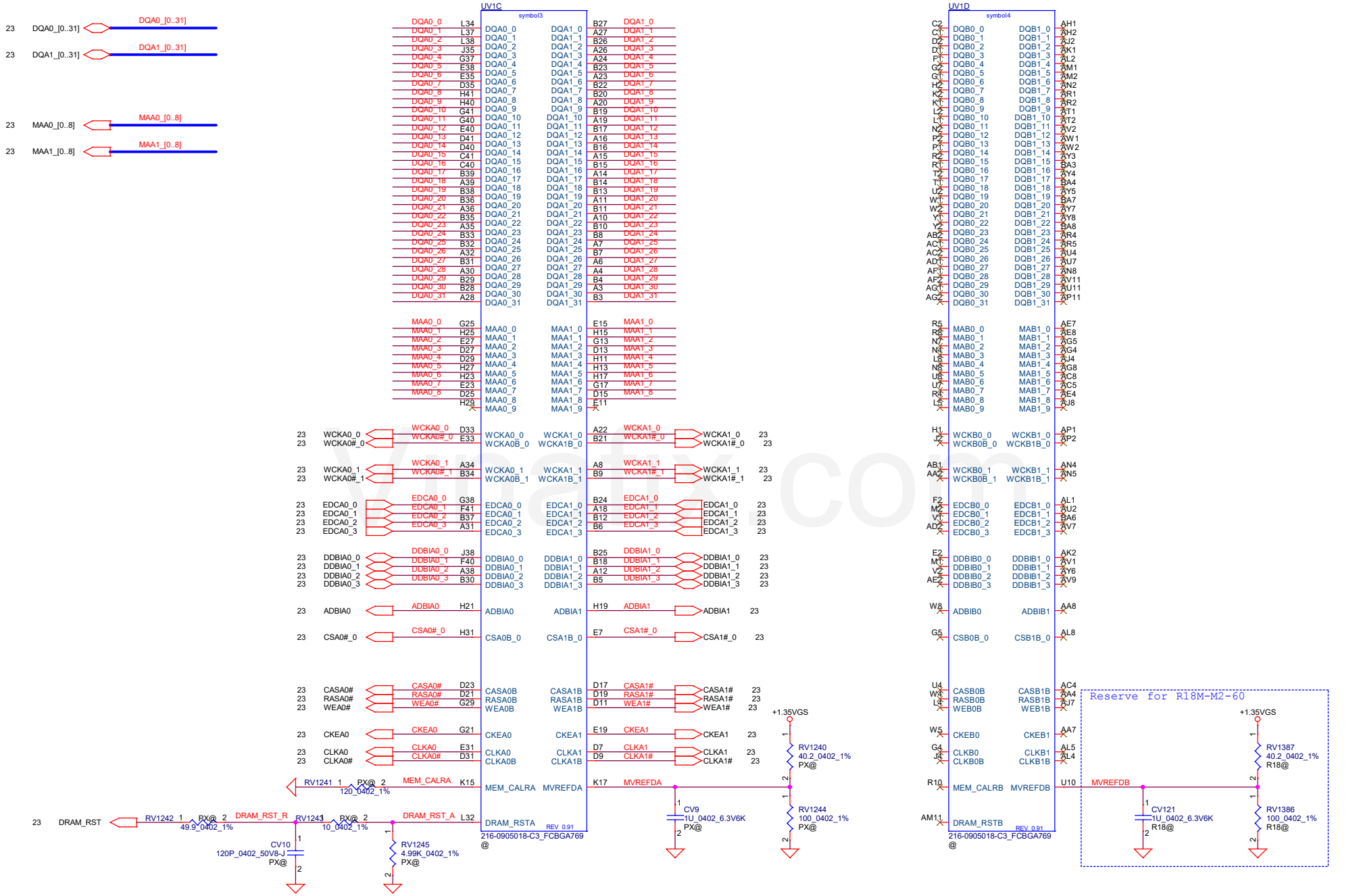

Title: **R17M-P1-50_VSS**

Size	Document Number	Rev
Custom	330ARR	1.0

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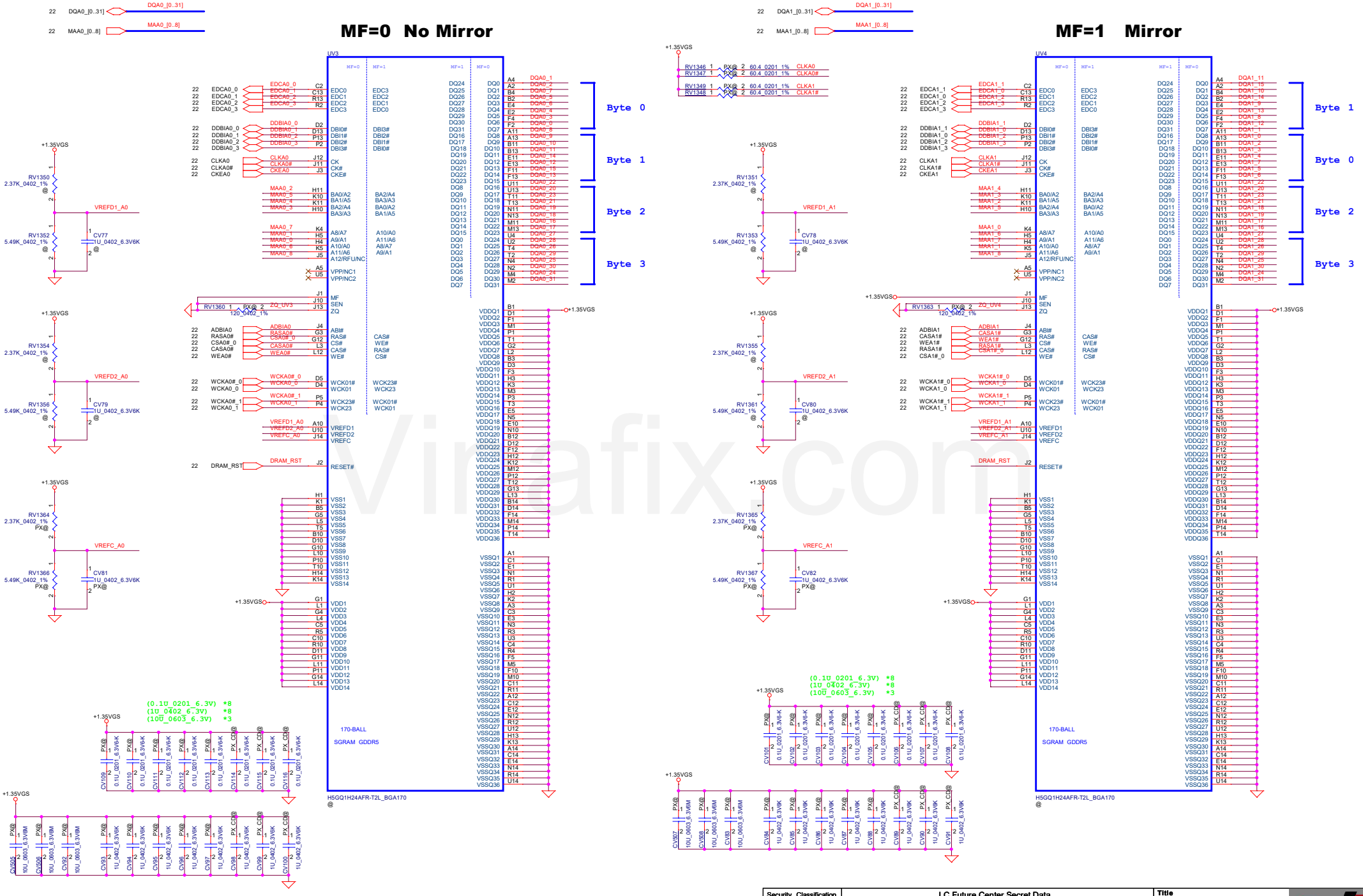

Title: R17M-P1-50_GDDR5 VRAM1
Size: Custom
Document Number: 330ARR
Rev: 1.0
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Title: R17M-P1-50_GDDR5 VRAM2

Size	Document Number	Rev
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Security Classification	LC Future Center Secret Data		
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Title

R17M-P1-50_Sequence

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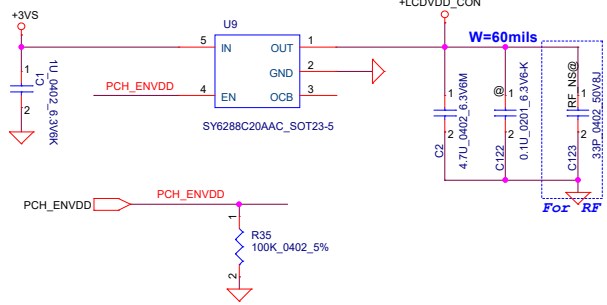
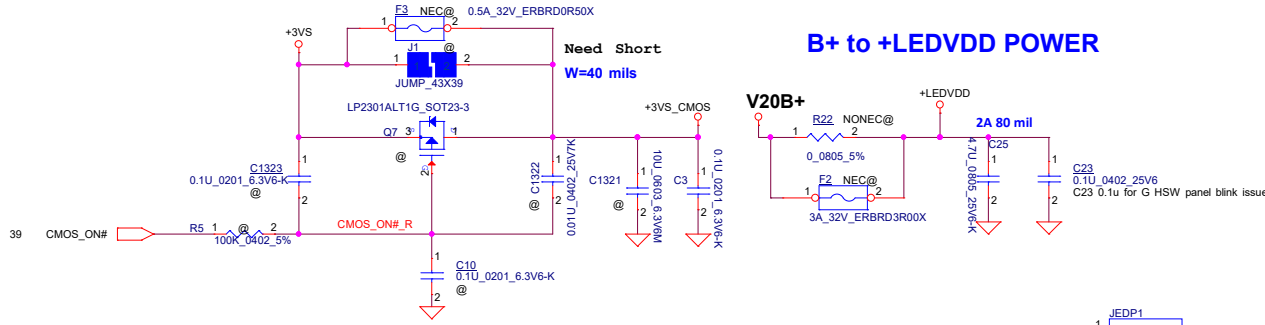
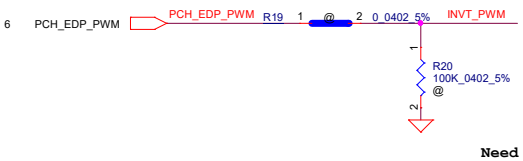
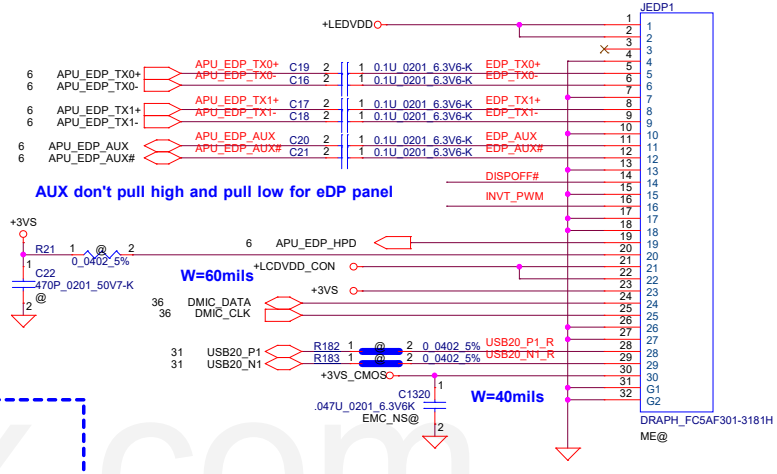
LCD POWER CIRCUIT



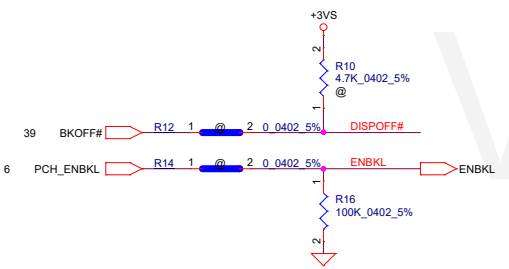
B+ to +LEDVDD POWER



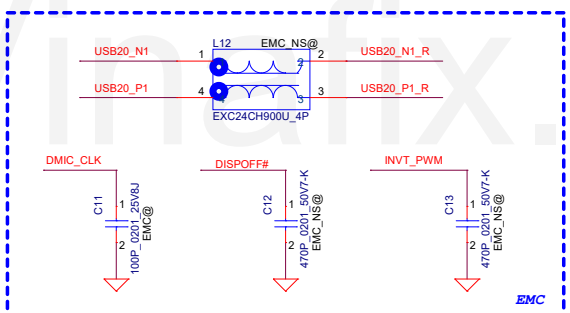




Need Short

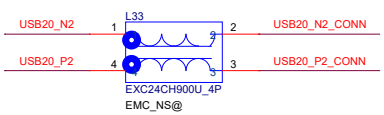


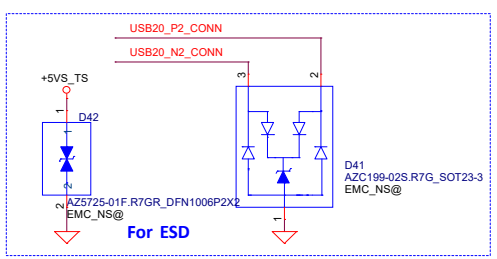
CMOS Camera

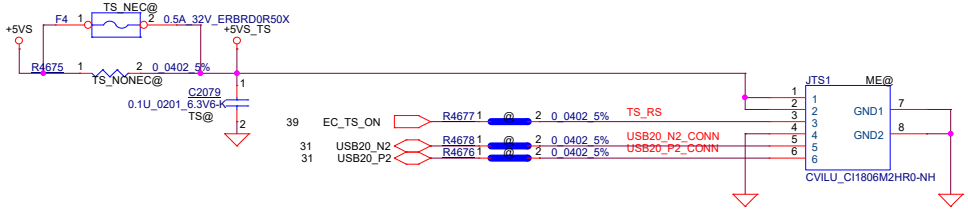


Touch Screen

Touch Screen







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: eDP/CMOS/TS

Size	Document Number	Rev
Custom	330ARR	1.0

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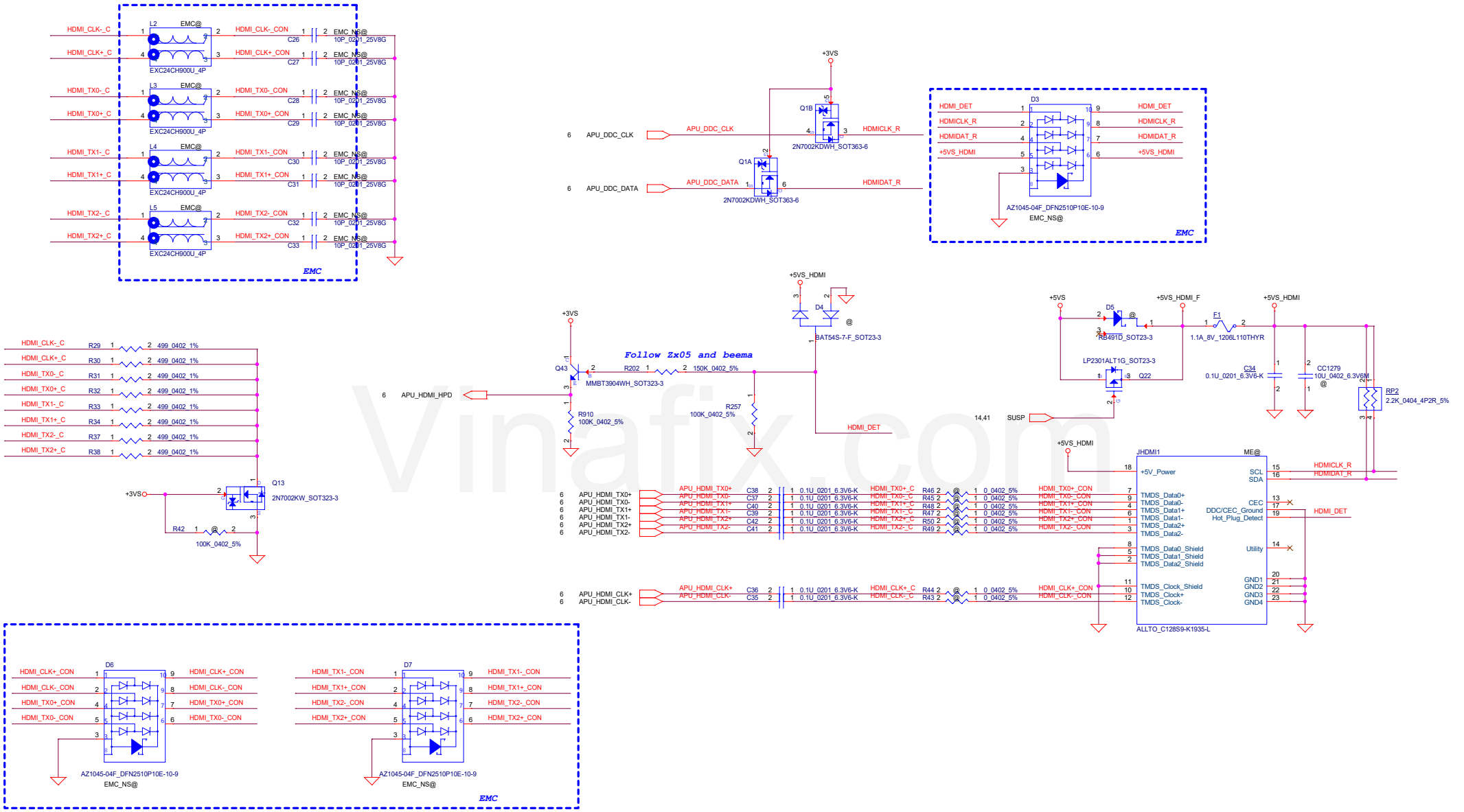

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	HDMI_CONN		
Size	Document Number		Rev
Custom	330ARR		1.0
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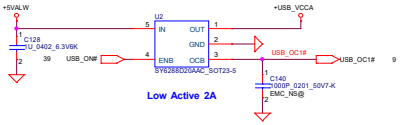
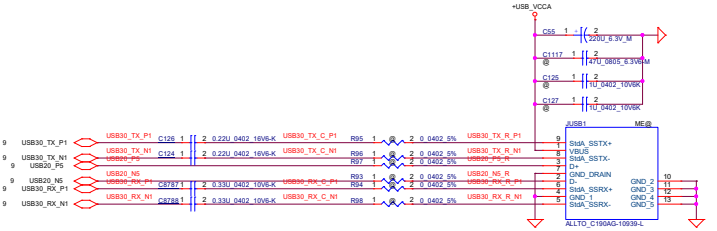
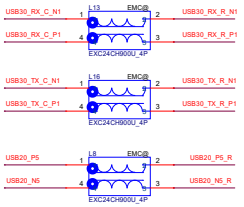
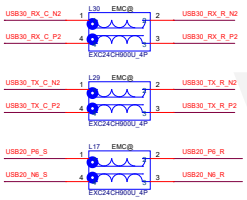
LEFT SIDE USB3.0 PORT x2

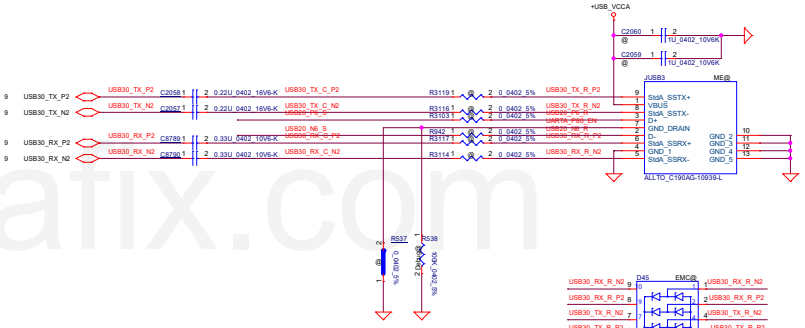


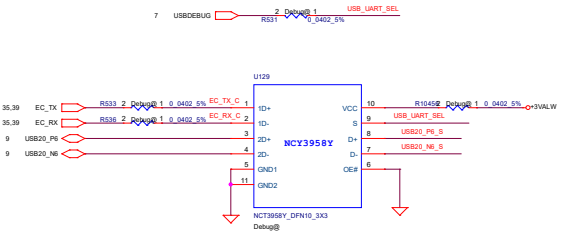


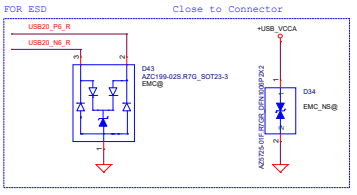


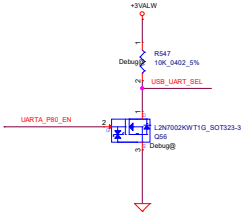
For USB Debug Function











USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UART_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D1(+/-) to 1D(+/-)
L	H	D1(+/-) to 2D(+/-)

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: **USB3.0 PORT (LEFT)**

Size	Document Number	Rev
A3	330ARR	1.0

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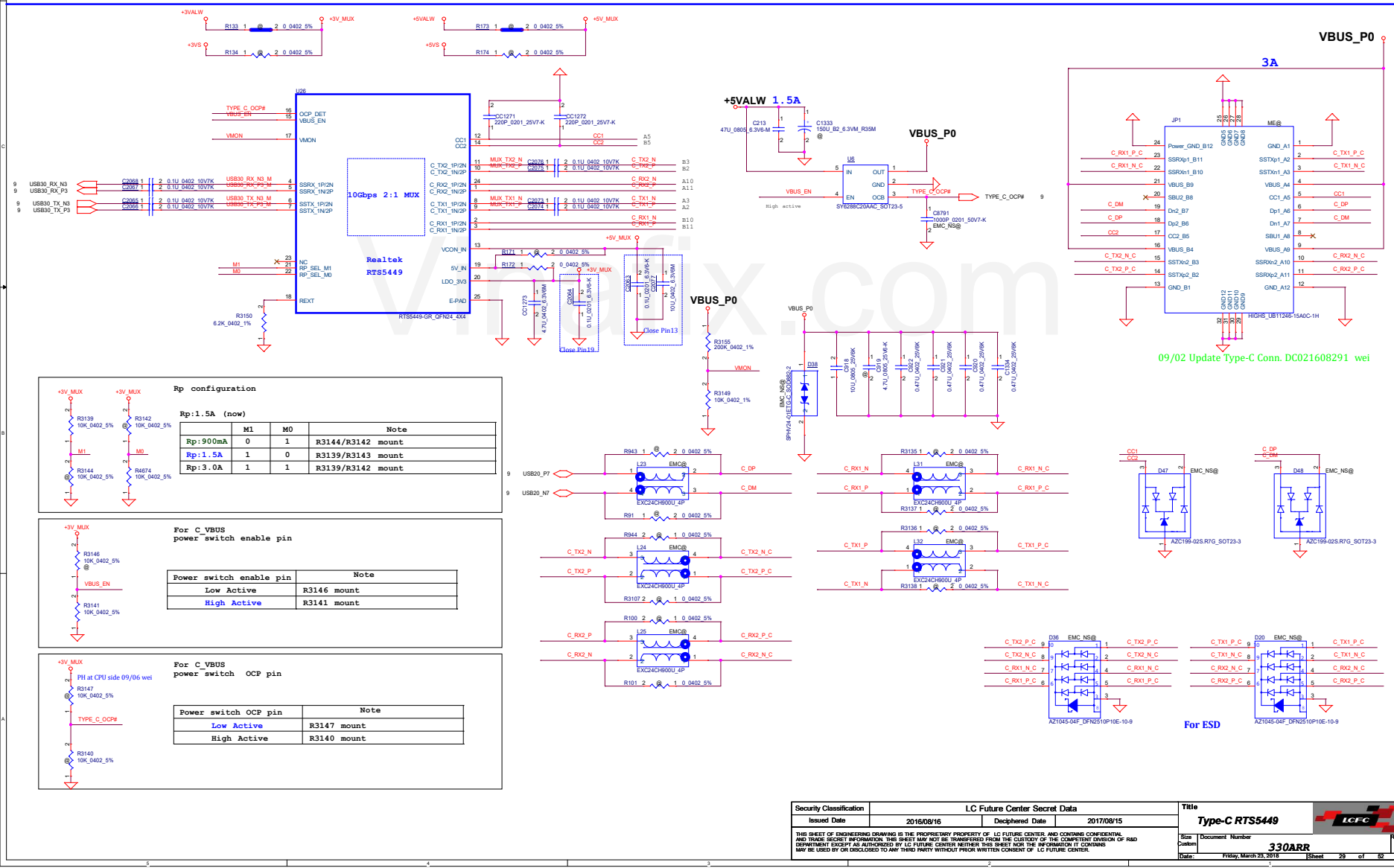
Remove type-c redriver



Rp configuration

Rp:1.5A (now)

	M1	M0	Note
Rp:900mA	0	1	R3144/R3142 mount
Rp:1.5A	1	0	R3139/R3143 mount
Rp:3.0A	1	1	R3139/R3142 mount

For C_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount

For C_VBUS power switch OCP pin

PH at CPU side 09/06 wei

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	Type-C RTS5449		
Size	Document Number		Rev
Custom	330ARR		1.0
Date:	Friday, March 23, 2018	Sheet	29 of 62

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title

Blank

Size	Document Number	Rev
B	330ARR	1.0

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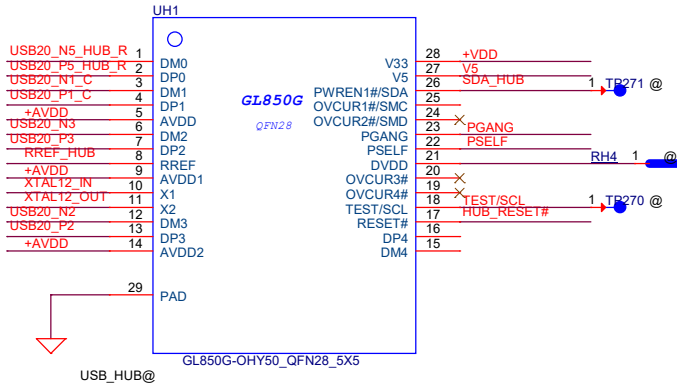
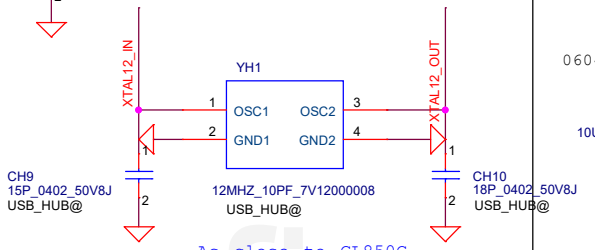
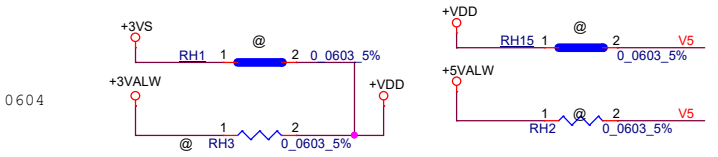
for USB HUB update to OHY50, manual modify PN to GL850G-OHY50



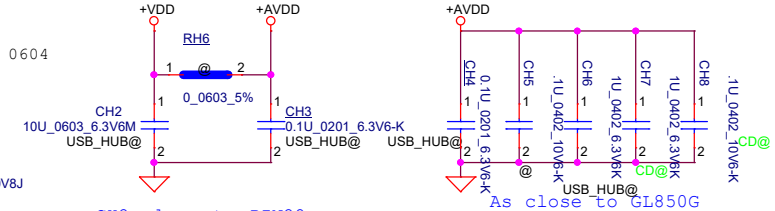
PORT1	Camera
PORT2	FP
PORT3	Touch Screen



As close to GL850G



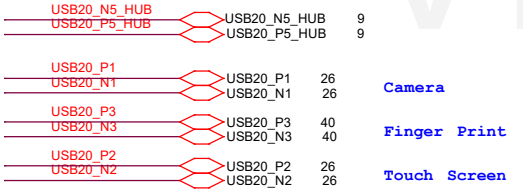
** External regulator mode:
RH1 install,RH2 non-install,RH15 install
Internal regulator mode:
RH1 non-install,RH2 install,RH15 non-install

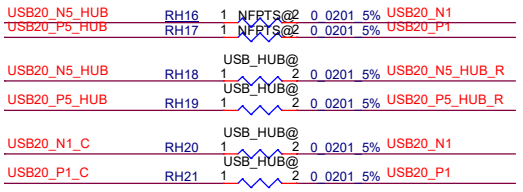


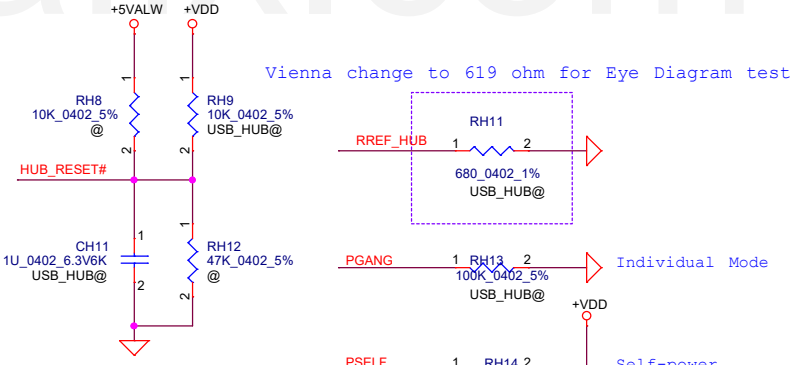
CH2 close to PIN28

As close to GL850G

CH3 PIN5 CH4/CH5 PIN9 CH6/CH15 PIN14







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	USB HUB		
Size	Document Number		Rev
B	330ARR		1.0
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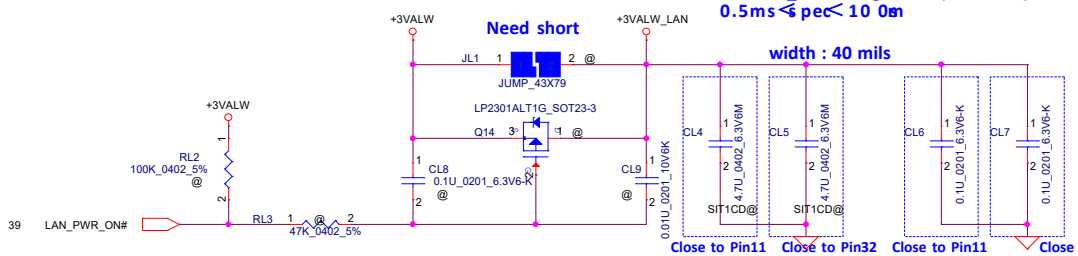
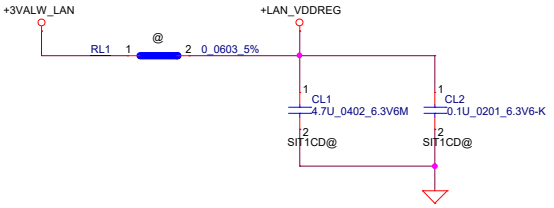
+3VALW TO +3VALW_LAN

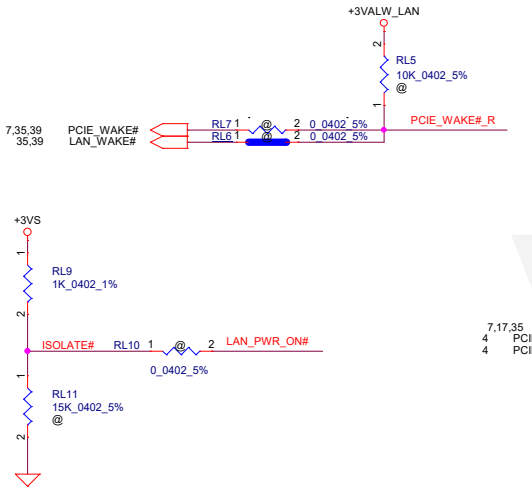
+3VALW_LAN rising time (10%~90%)
0.5ms < spec < 10 0ms

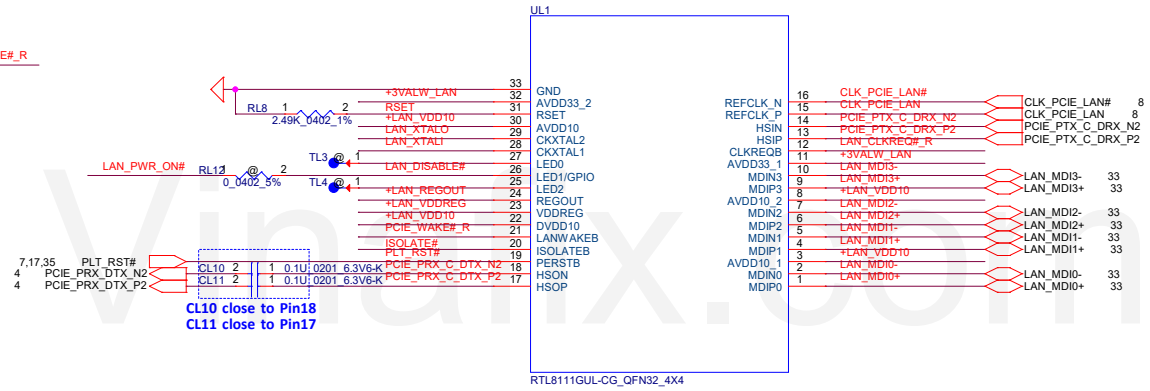
Need short

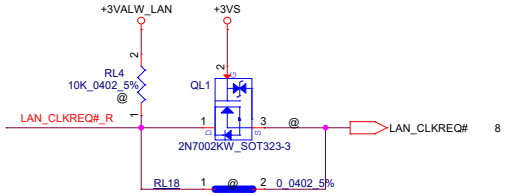
width : 40 mils





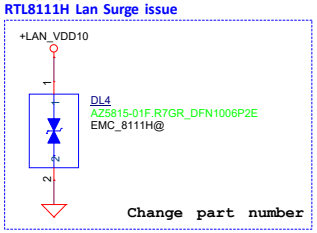


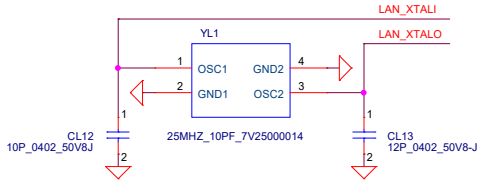




APU CLKREQ all both 3VS power plane

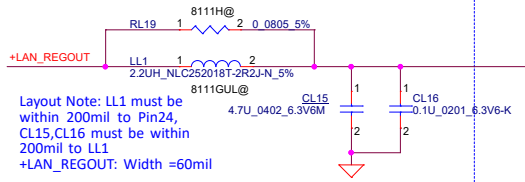
2018/01/24: add AZ5815-01F.R7GR for RTL8111H Lan Surge issue



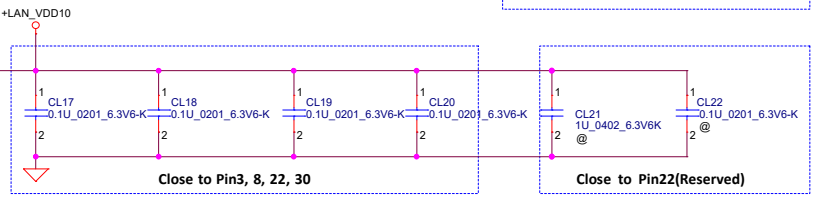


follow G CarrizoL 10pf

For RTL8111GUL/ RTL8106EUL (SWR mode)
For RTL8111H (LDO mode) RL19 stuf f



Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_RTL8111GUL

Size	Document Number	Rev
Custom	330ARR	1.0

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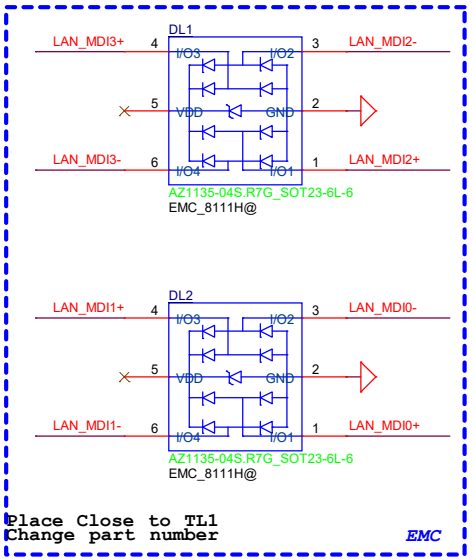

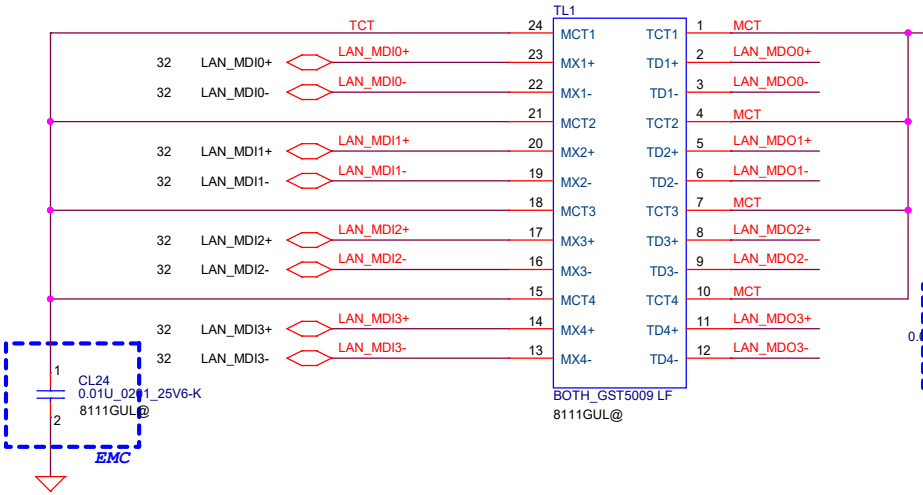

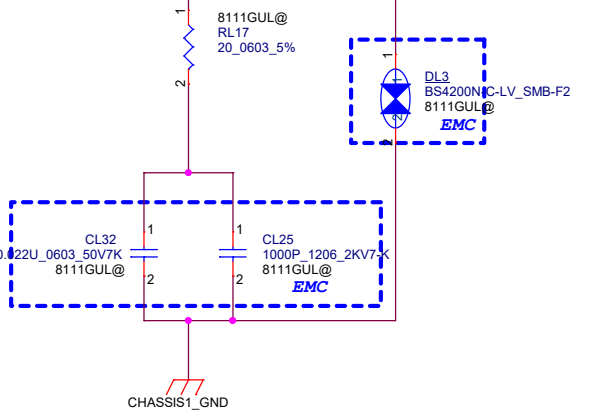

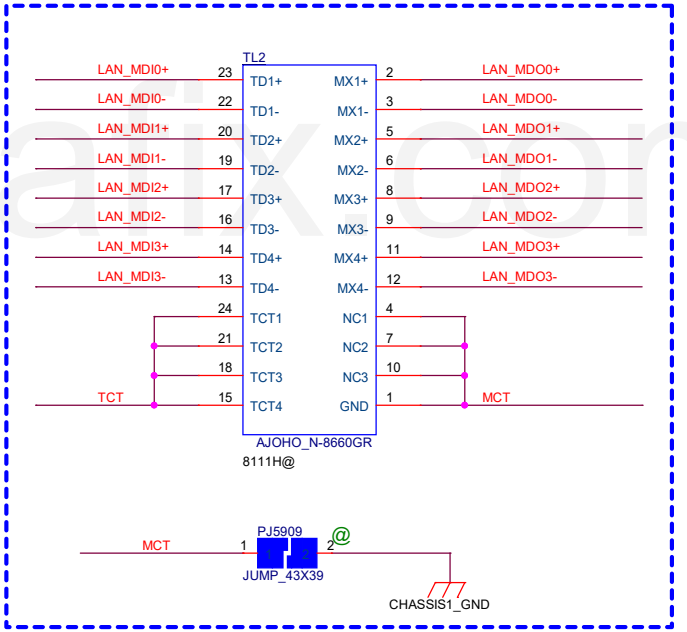

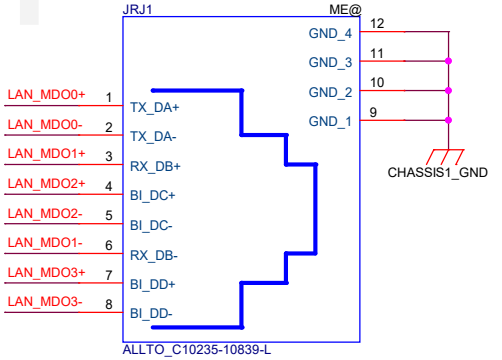

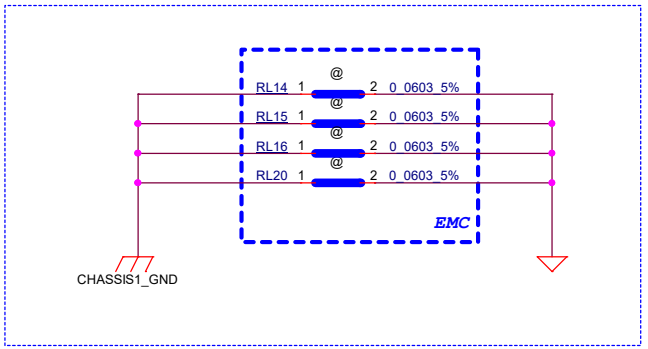

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **LAN_Transformer**

Size	Document Number	Rev
Custom	330ARR	1.0

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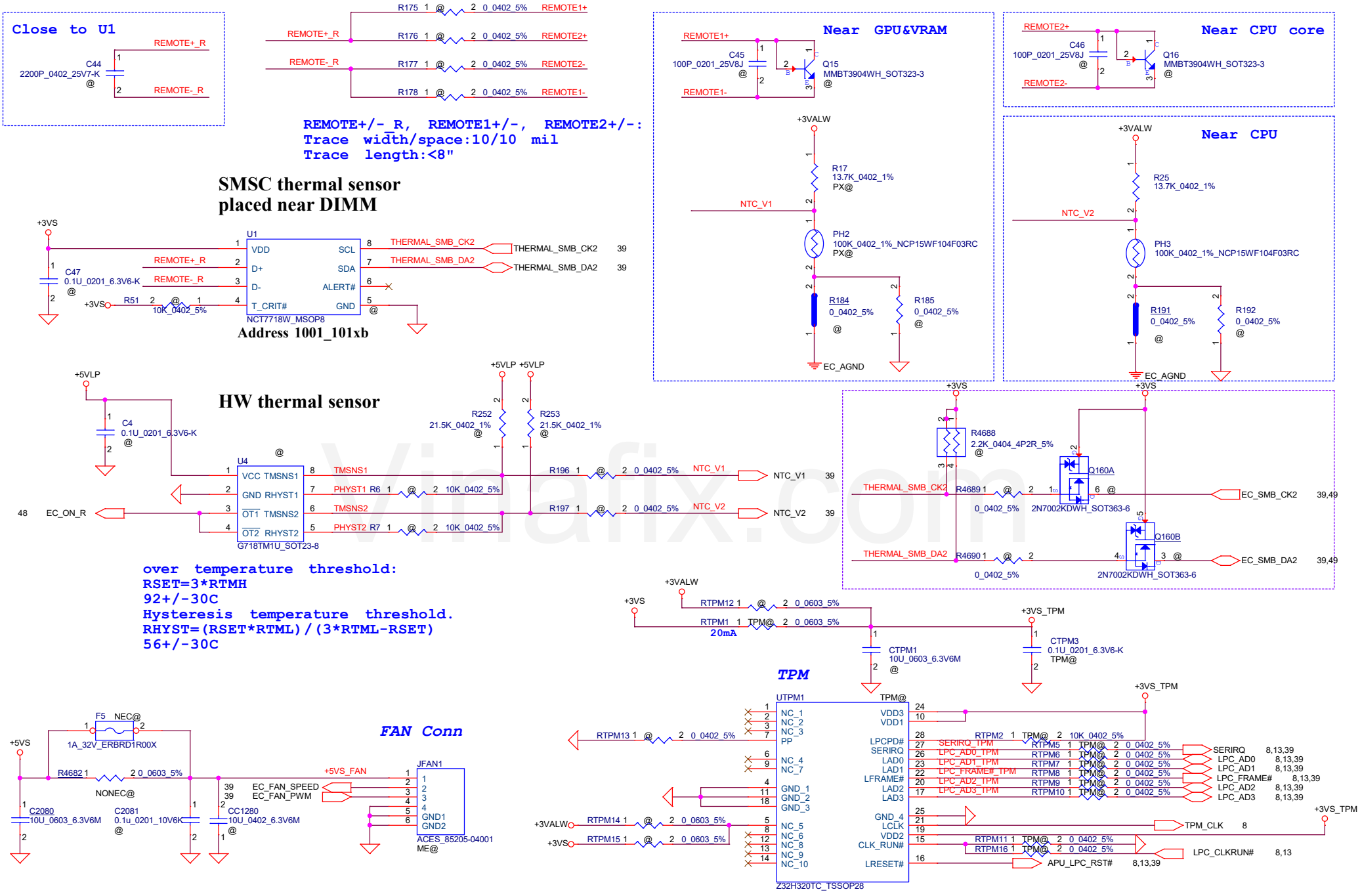

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	Thermal sensor/FAN CONN/TPM		
Size	Document Number		Rev
Custom	330ARR		1.0
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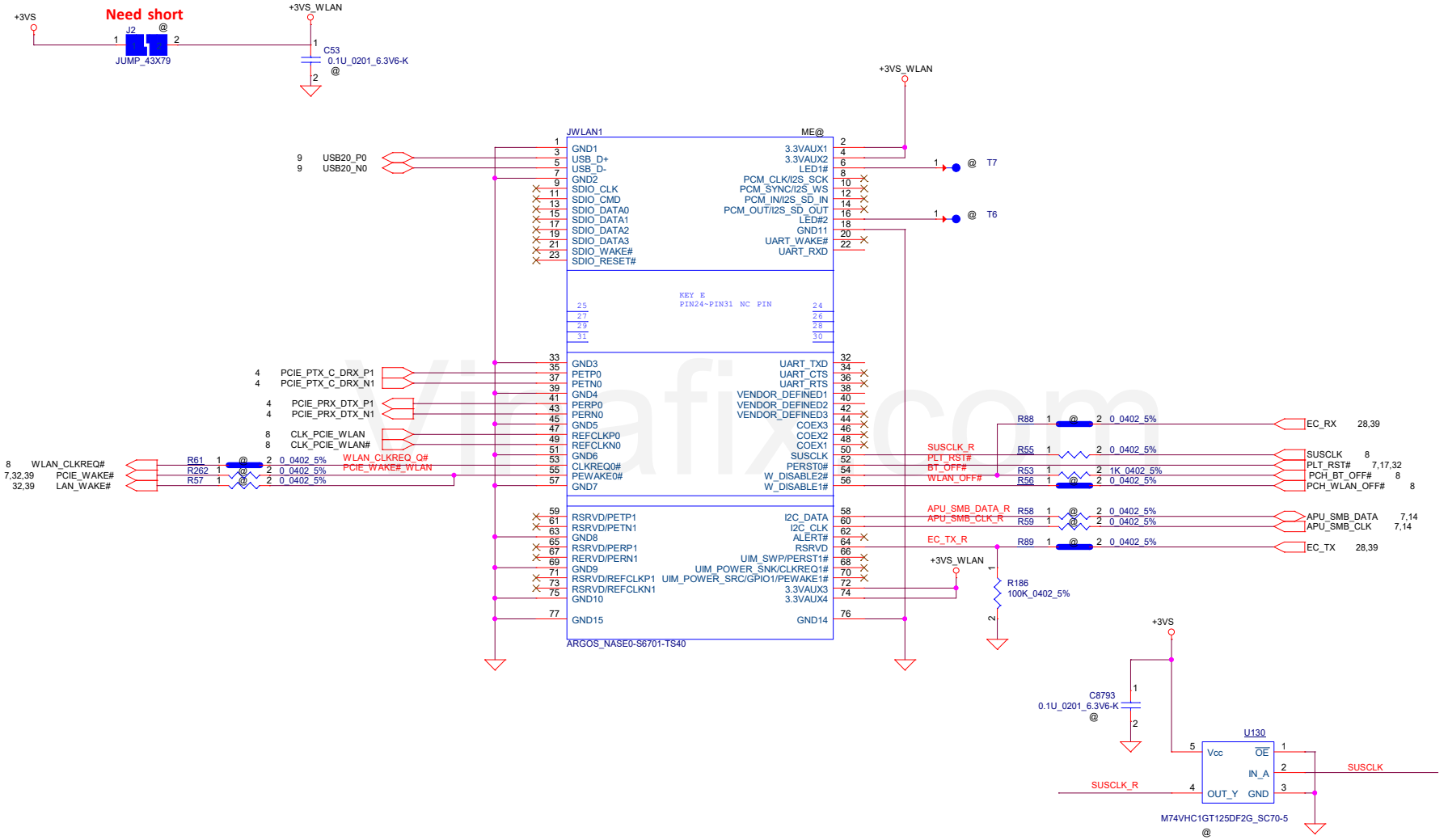
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **NGFF WLAN**

Size	Document Number	Rev
Custom	330ARR	1.0
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Digital power for HDA link

Analog power for mixers, & IO ports

Power supply for full-bridge left/Right channel

8/29 Add +1.8VS Circuit for Audio wei

Analog power for DACs, ADCs

Digital power for digital I/O circuit

ABR USB leakage issue, card reader power need 3VALW

Power for combo jack depop circuit at system shutdown mode

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

8/16 Update Audio Jack P/N SP011509163 wei

Audio Jack

8/16 Update Audio Jack P/N DC021608101 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

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Title: Codec & CR_RTS5199

Size: Custom | Document Number: 330ARR | Rev: 1.0

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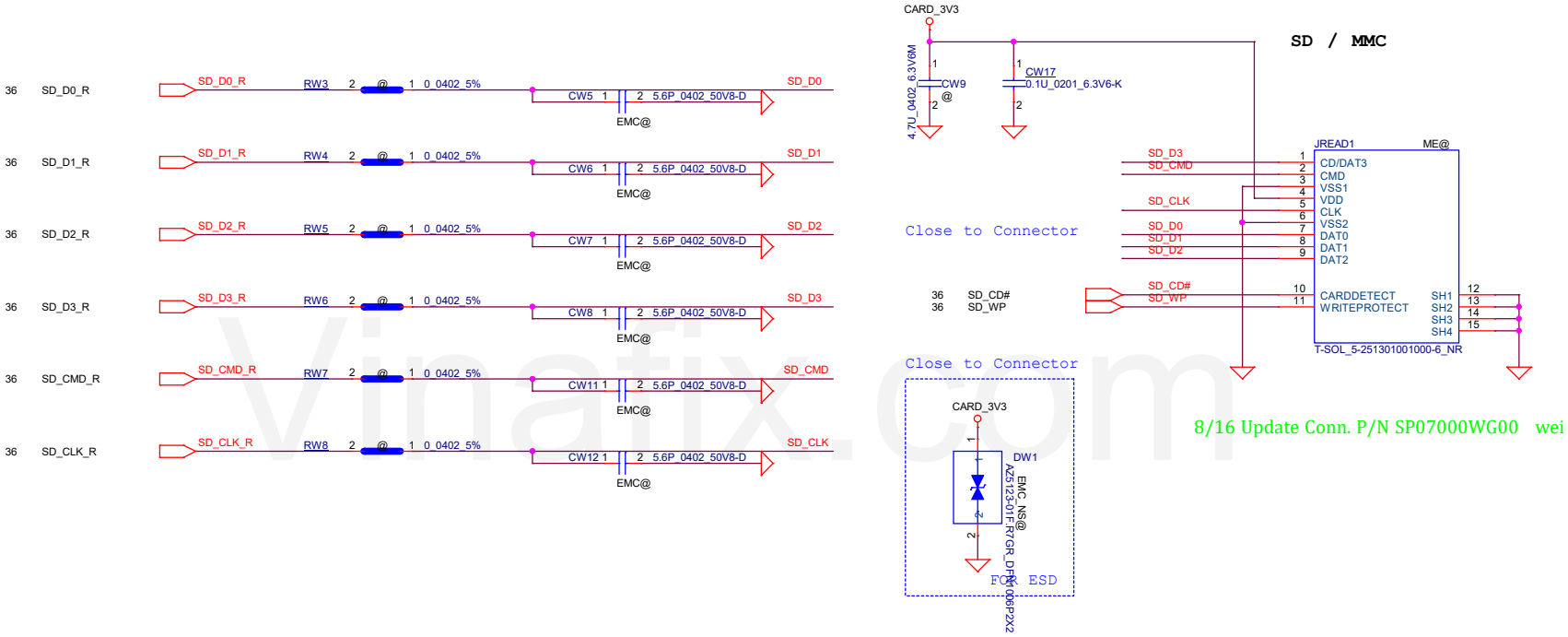

8/16 Update Conn. P/N SP07000WG00 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: **Cardreader**

Size	Document Number	Rev
Custom	330ARR	1.0

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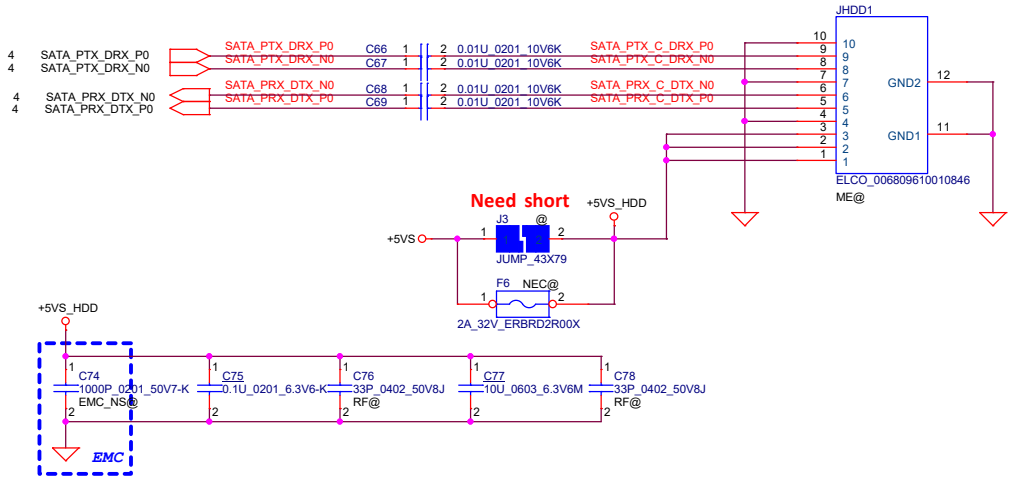
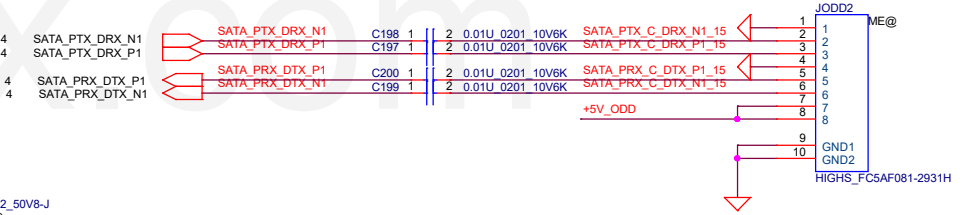
SATA HDD Conn.



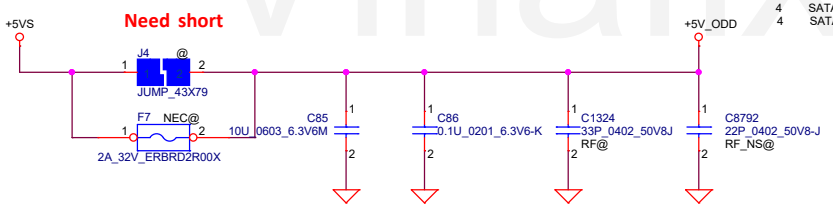
FOR 15"

SATA ODD FFC Conn

SATA 15 ODD P/N pin assgin is different from G SKL



+5VS to +5V_ODD



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title			
HDD/ODD CONN			
Size: Custom	Document Number: 330ARR		Rev: 1.0
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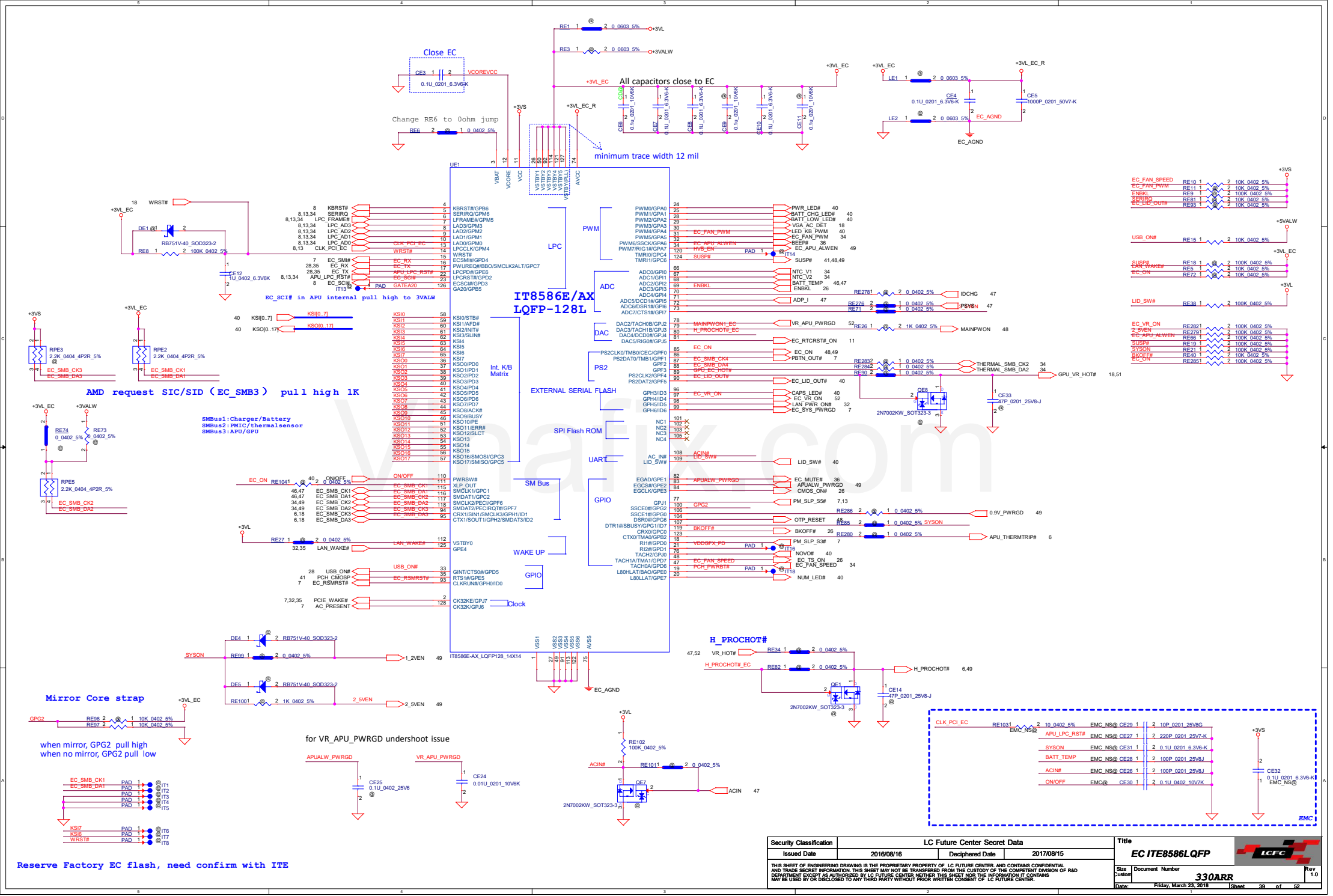
Close EC
Change RE6 to 0ohm jump
All capacitors close to EC
minimum trace width 12 mil
IT8586E/AX
LQFP-128L
EC_SCI# in APU internal pull high to 3VALW
AMD request SIC/SID（EC_SMB3） pull high 1K
SMBus1:Charger/Battery
SMBus2:PMIC/thermalsensor
SMBus3:APU/GPU
Mirror Core strap
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
for VR_APU_PWRGD undershoot issue
H_PROCHOT#
Reserve Factory EC flash, need confirm with ITE
EMC
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
Int. K/B Matrix
Security Classification
LC Future Center Secret Data
Issued Date
2016/08/16
Deciphered Date
2017/08/15
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Title
EC ITE8586LQFP
Size
Custom
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1.0
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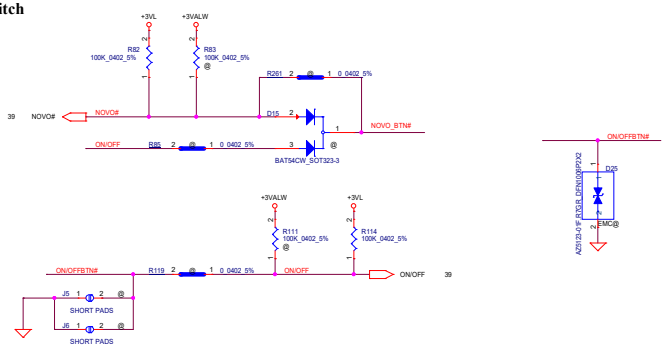
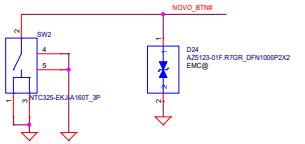
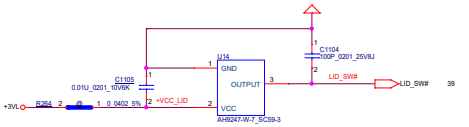
ON/OFF switch



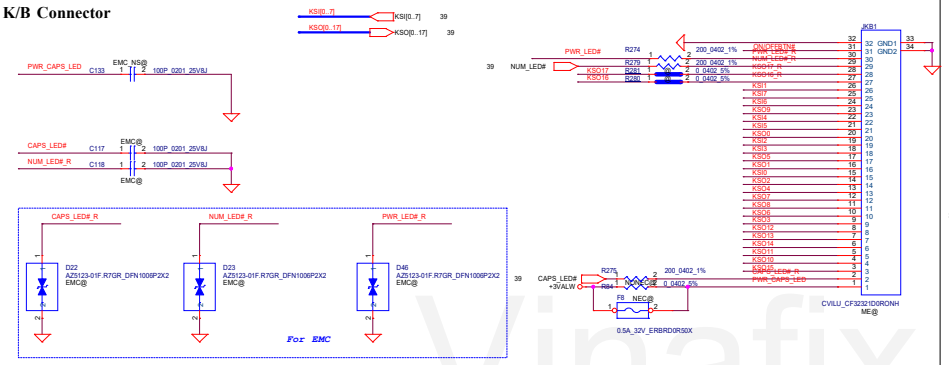
Novo button



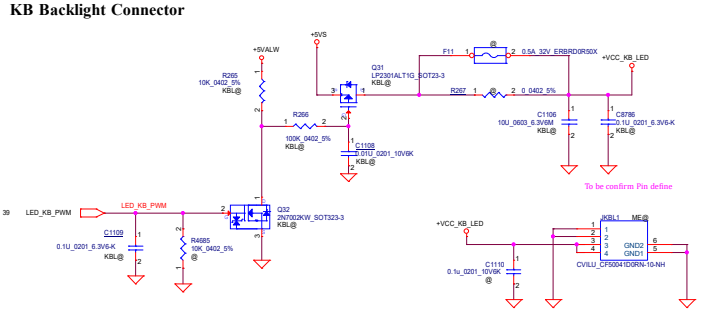
LID switch



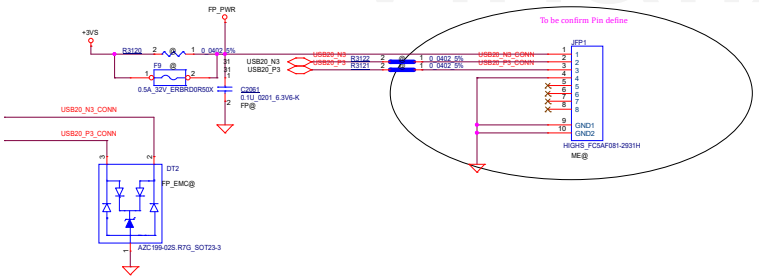
K/B Connector



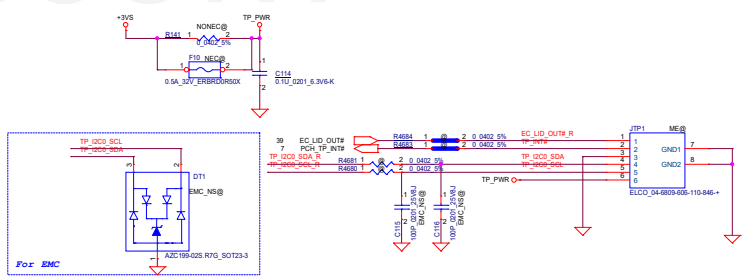
KB Backlight Connector

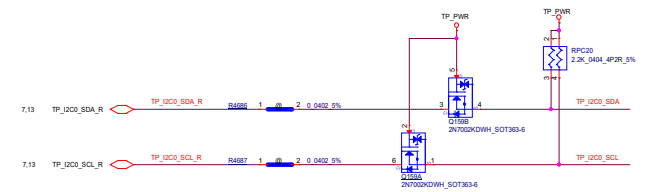


Finger Print Connector



TP/B Connector





Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

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Title: KBD/PWR/IO/LED/TP Conn.

Size	Document Number	Rev
Custom	330ARR	1.0
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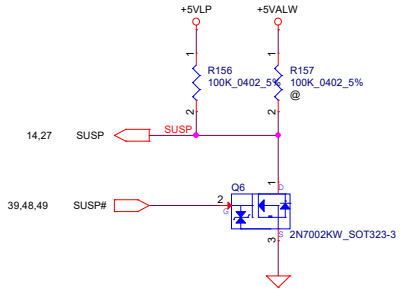
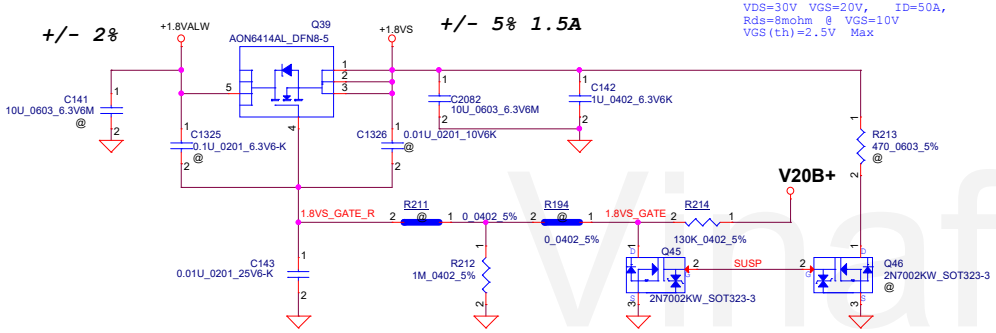


+1.8VALW to +1.8VS

+/- 2%

+/- 5% 1.5A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max



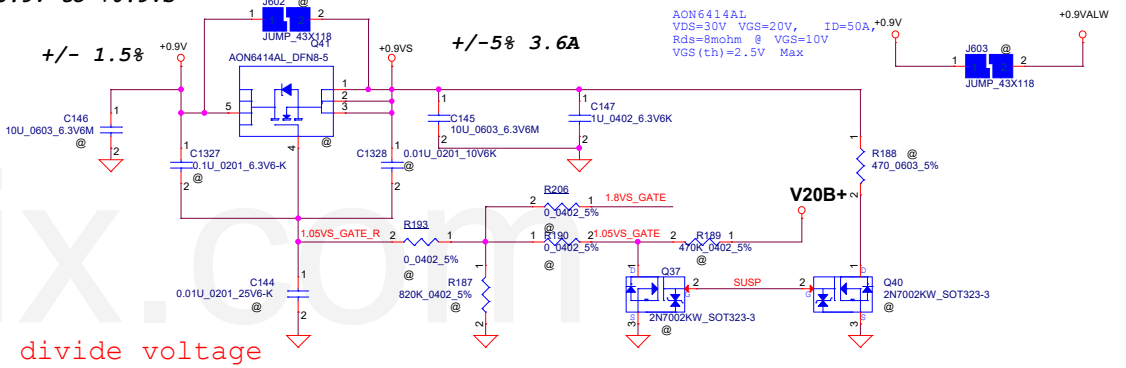
20VSB will change to 6V in DC mode, careful the Res divide voltage

+0.9V to +0.9VS

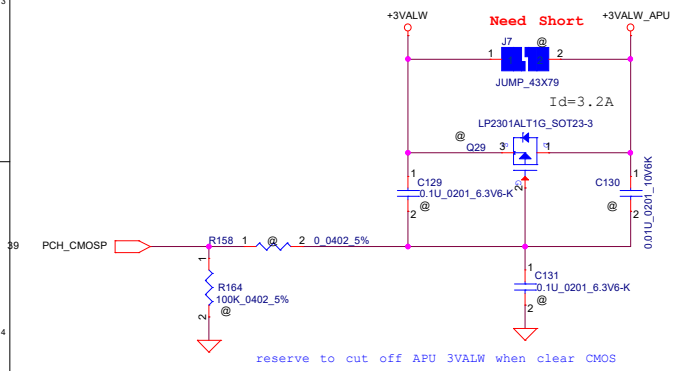
+/- 1.5%

+/-5% 3.6A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

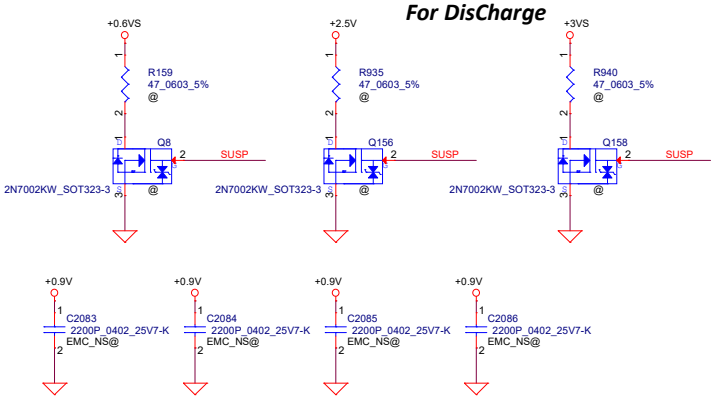


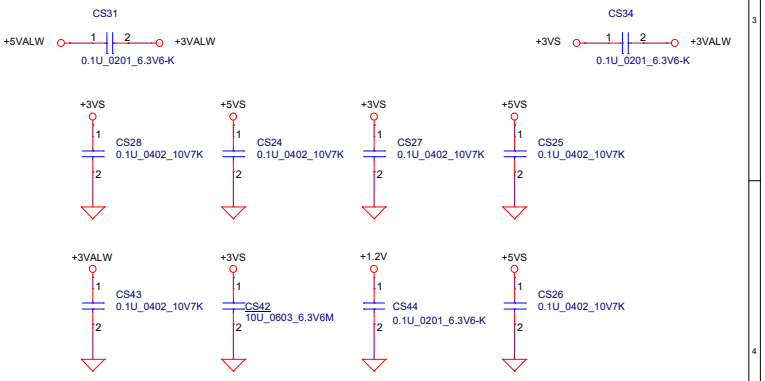
+3VALW to +3VALW_APU



reserve to cut off APU 3VALW when clear CMOS

For DisCharge





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: DC V TO VS INTERFACE

Size	Document Number	Rev
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CPU Thermal Holex3

H11 HOLEA — pad_c6p0d4p0
H12 HOLEA — pad_c6p0d4p0
H13 HOLEA — pad_c6p0d4p0

GPU Thermal Holex2

H8 HOLEA — pad_c8p0d3p3
H9 HOLEA — pad_c8p0d3p3

Close to RJ45

H4 HOLEA — CHASSIS1_GND, pad_ct7p0b8p0d3p0

Close to Audio jack

H3 HOLEA — pad_ct7p0b8p0d3p0

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

WLAN Standoff

H5 HOLEA — pad_o2p6x2p9d2p6x2p9n
H6 HOLEA — PAD_CB5P5D2P5
H7 HOLEA — pad_c2p5d2p5n
H10 HOLEA — pad_c8p0d3p3
H14 HOLEA — pad_c3p3d3p3n
H15 HOLEA — PAD_CT7P0D3P0
H16 HOLEA — pad_d2p5
H17 HOLEA — pad_d2p5
H18 HOLEA — PAD_C2P5D2P5N

USB3.0 Shielding

SH1 ME@ — SPRING_FINGER_6.2X1.64
SH2 ME@ — SPRING_FINGER_6.2X1.64
SH3 ME@ — SPRING_FINGER_6.2X1.64
SH4 ME@ — SPRING_FINGER_6.2X1.64
SH5 ME@ — SPRING_FINGER_6.2X1.64
SH6 ME@ — SPRING_FINGER_6.2X1.64

DDR4 Shielding

SH12 ME@ — SPRING_FINGER_6.2X1.64
SH7 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH8 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 ME@ — SPRING_FINGER_6.2X1.64
SH9 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	Hole		
Size B	Document Number	330ARR	Rev 1.0
Date:	Friday, March 23, 2018	Sheet 42 of 52	

UL1 8111H@
RTL8111H-CG
SA000074W00
LAN Chip

UC2
RAVEN RIDGE YM2700C4T4MFBA
R7@
SA00008QB10

UC2
RAVEN RIDGE YM2500C4T4MFBA
R5@
SA00008QA10

UC2
RAVEN RIDGE YM2200C4T2OFB
R3@
SA00008UR10
APU type

UV1 R17@
216-0905018-C3_FCBGA769
SA00008DT20

UV1 R18@
216-0915006_FCBGA769
SA00008XC00
GPU

ZZZ3 HDMI@
HDMI PN
RO00000040J
HDMI Royalty

ZZZ9 DRAM_S4G@
Samsung
X7645A12004

ZZZ2 DRAM_M4G@
Micron
X7645A12006

ZZZ7 DRAM_H4G@
Hynix
X7645A12005
DRAM X76 BOM

ZZZ5 S8GX2@
Samsung
X7645A12002

ZZZ8 H8GX2@
Hynix
X7645A12001

ZZZ12 M8GX2@
Micron
X7645A12003

ZZZ4 S8GX2R18@
Samsung
X7645A12009

ZZZ6 H8GX2R18@
Hynix
X7645A12007

ZZZ10 M8GX2R18@
Micron
X7645A12008
VRAM X76 BOM

UD1 MD_S8Gb@
K4A8G165WC-BCTD
SA00008PE00

UD2 MD_S8Gb@
K4A8G165WC-BCTD
SA00008PE00

UD3 MD_S8Gb@
K4A8G165WC-BCTD
SA00008PE00

UD4 MD_S8Gb@
K4A8G165WC-BCTD
SA00008PE00

RC1608 MD_S8Gb@
10K_0402_5%
SD028100283

RC1609 MD_S8Gb@
2K_0402_5%
SD028200183
DRAM_Samsung 4G

UV3 S8G_VR@
K4G80325FB-HC28
SA000081C00

UV4 S8G_VR@
K4G80325FB-HC28
SA000081C00

RV1307 S8G_VR@
5.1K_0402_5%
SD028510183

RV1304 S8G_VR@
5.1K_0402_5%
SD028510183

RV1298 S8G_VR@
5.1K_0402_5%
SD028510183
VRAM_Samsung 8GX2

UD1 MD_H8Gb@
H5AN8G6NAFR-UHC
SA00007X200

UD2 MD_H8Gb@
H5AN8G6NAFR-UHC
SA00007X200

UD3 MD_H8Gb@
H5AN8G6NAFR-UHC
SA00007X200

UD4 MD_H8Gb@
H5AN8G6NAFR-UHC
SA00007X200

RC1610 MD_H8Gb@
10K_0402_5%
SD028100283

RC1607 MD_H8Gb@
10K_0402_5%
SD028100283
DRAM_Hynix 4G

UV3 H8G_VR@
H5GC8H24MJR-R0C
SA000081600

UV4 H8G_VR@
H5GC8H24MJR-R0C
SA000081600

RV1307 H8G_VR@
5.1K_0402_5%
SD028510183

RV1304 H8G_VR@
5.1K_0402_5%
SD028510183

RV1297 H8G_VR@
5.1K_0402_5%
SD028510183
VRAM_Hynix 8GX2

UD1 MD_M8Gb@
MT40A512M16LY-075:E
SA00008F930

UD2 MD_M8Gb@
MT40A512M16LY-075:E
SA00008F930

UD3 MD_M8Gb@
MT40A512M16LY-075:E
SA00008F930

UD4 MD_M8Gb@
MT40A512M16LY-075:E
SA00008F930

RC1610 MD_M8Gb@
10K_0402_5%
SD028100283

RC1608 MD_M8Gb@
10K_0402_5%
SD028100283
DRAM_Micron 4G

UV3 M8G_VR@
MT51J256M32HF-70:A
SA000081700

UV4 M8G_VR@
MT51J256M32HF-70:A
SA000081700

RV1307 M8G_VR@
5.1K_0402_5%
SD028510183

RV1303 M8G_VR@
5.1K_0402_5%
SD028510183

RV1298 M8G_VR@
5.1K_0402_5%
SD028510183
VRAM_Micron 8GX2

RC1609 DIMM_ONLY@
2K_0402_5%
SD028200183

RC1607 DIMM_ONLY@
10K_0402_5%
SD028100283
DIMM ONLY

UV3 S8G_VRR18@
K4G80325FB-HC28
SA000081C00

UV4 S8G_VRR18@
K4G80325FB-HC28
SA000081C00

RV1418 S8G_VRR18@
4.75K_0402_1%
SD03447518J
VRAM_Samsung 8GX2 R18

ZZZ13
PCB PN
DAZ18700100
PCB_MB

UV3 H8G_VRR18@
H5GC8H24MJR-R0C
SA000081600

UV4 H8G_VRR18@
H5GC8H24MJR-R0C
SA000081600

RV1415 H8G_VRR18@
8.45K_0402_1%
SD000011R00

RV1418 H8G_VRR18@
2K_0402_1%
SD03420018J
VRAM_Hynix 8GX2 R18

UV3 M8G_VRR18@
MT51J256M32HF-70:A
SA000081700

UV4 M8G_VRR18@
MT51J256M32HF-70:A
SA000081700

RV1415 M8G_VRR18@
4.53K_0402_1%
SD03445318J

RV1418 M8G_VRR18@
2K_0402_1%
SD03420018J
VRAM_Micron 8GX2 R18

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *Virtual symbol*

Size	Document Number	Rev
Custom	330ARR	1.0
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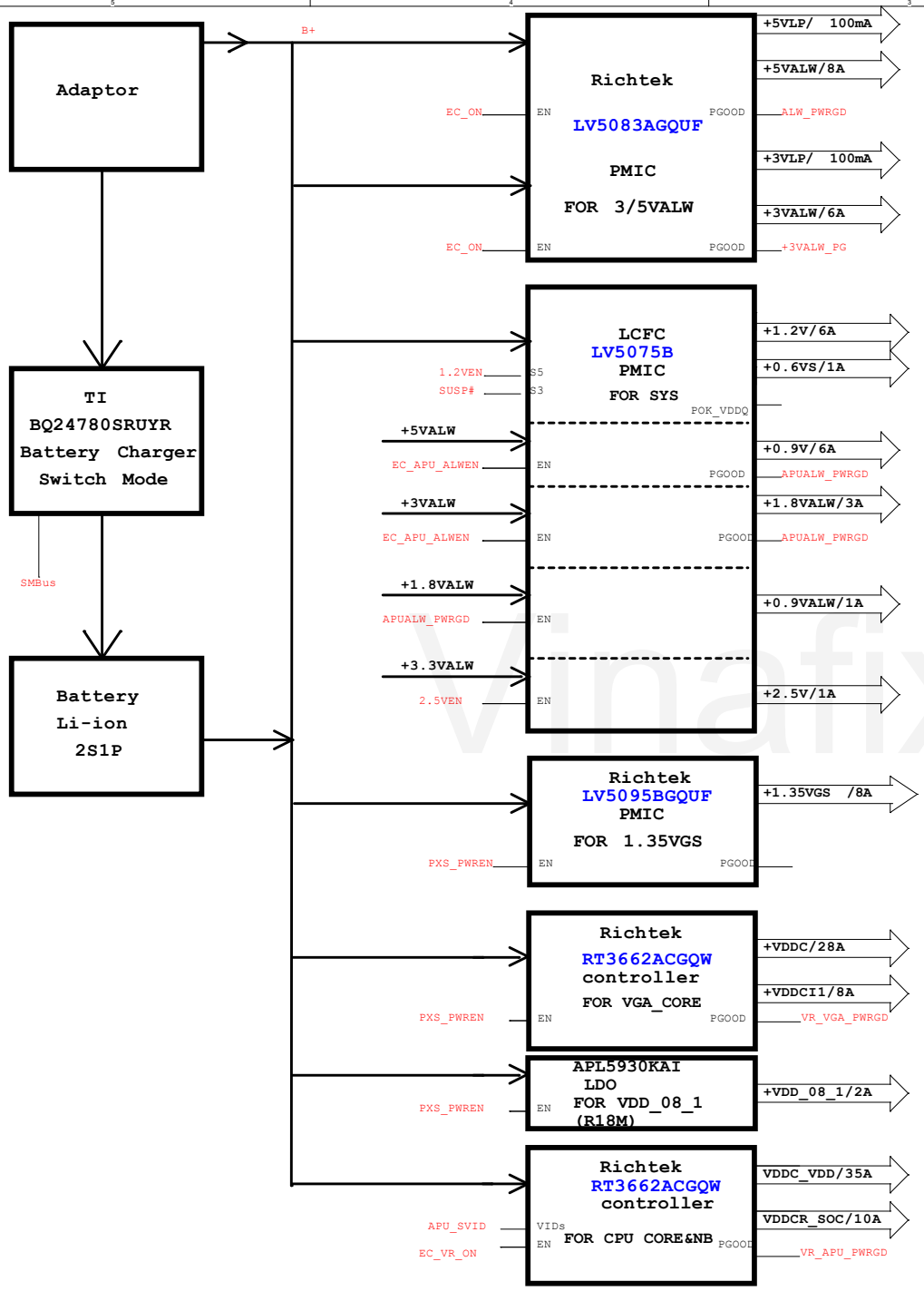
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title

Power sequence Block

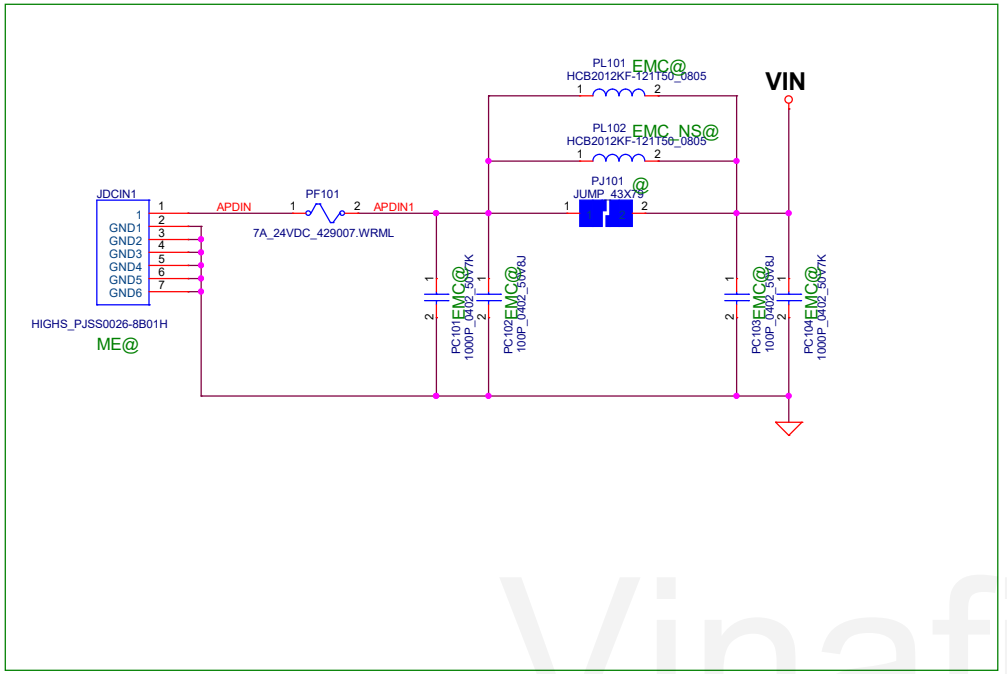
Size: Custom	Document Number: ***330G-ARR***	Rev: 1.0
Date: Friday, March 23, 2018	Sheet 44 of 52	

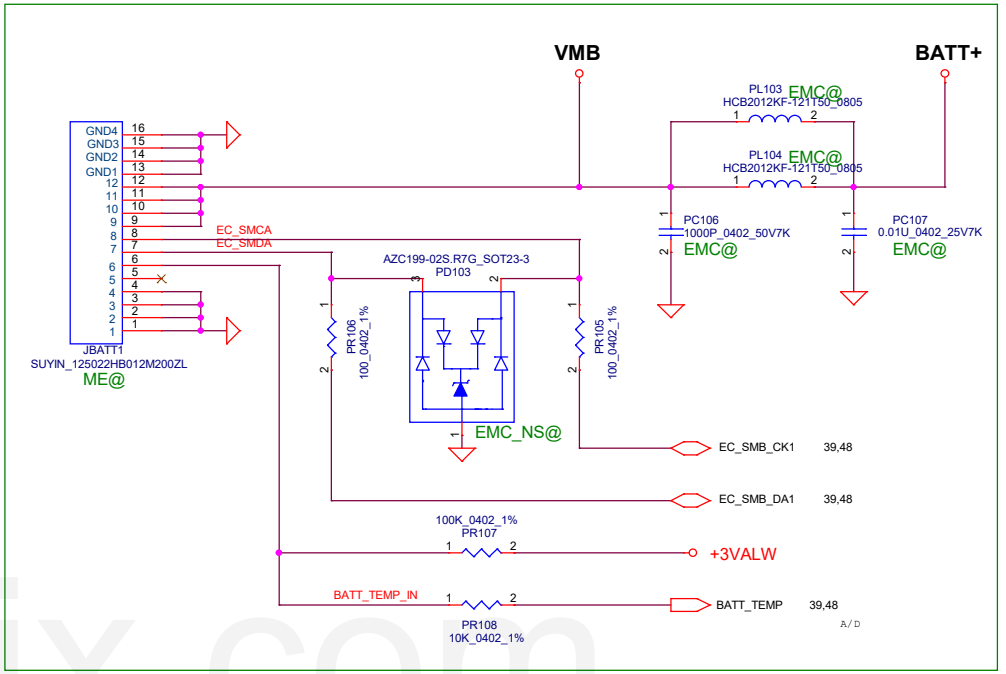


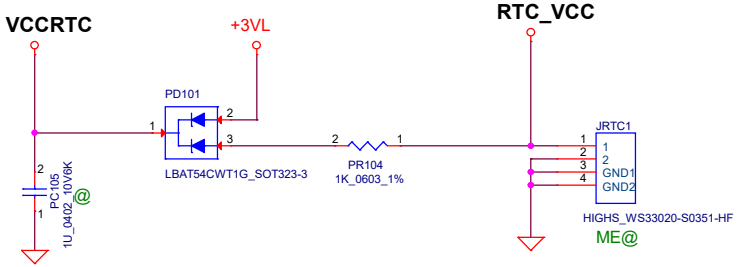
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

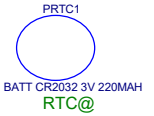
Title: **Power Diagram**

Size	Document Number	Rev
Custom	330G-ARR	1.0
Date: Friday, March 23, 2018	Sheet 45 of 53	









GC02001YB00-35mm cable , delete when layout

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **DCIN / RTC**

Size	Document Number	Rev
Custom	330G-ARR	1.0
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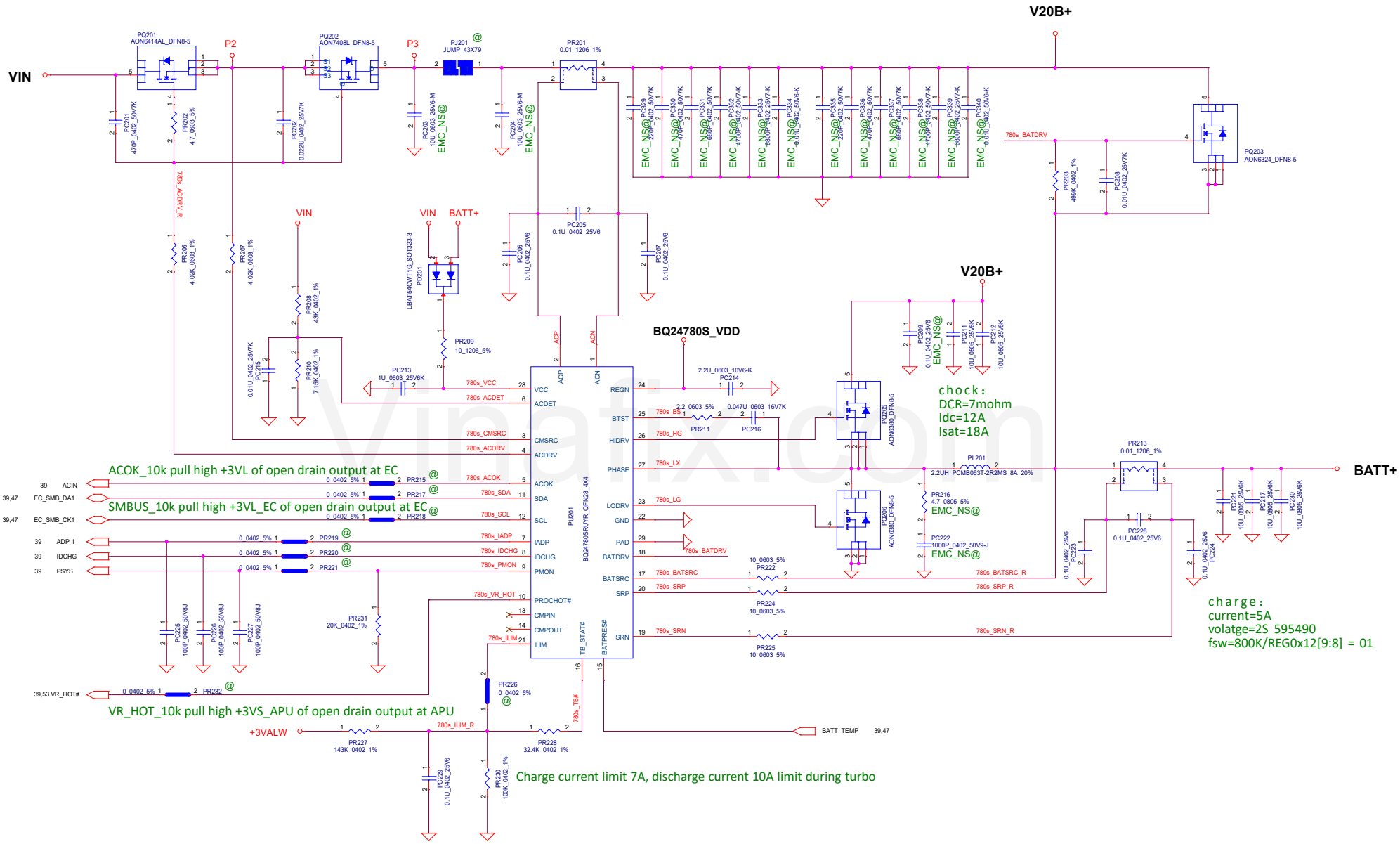
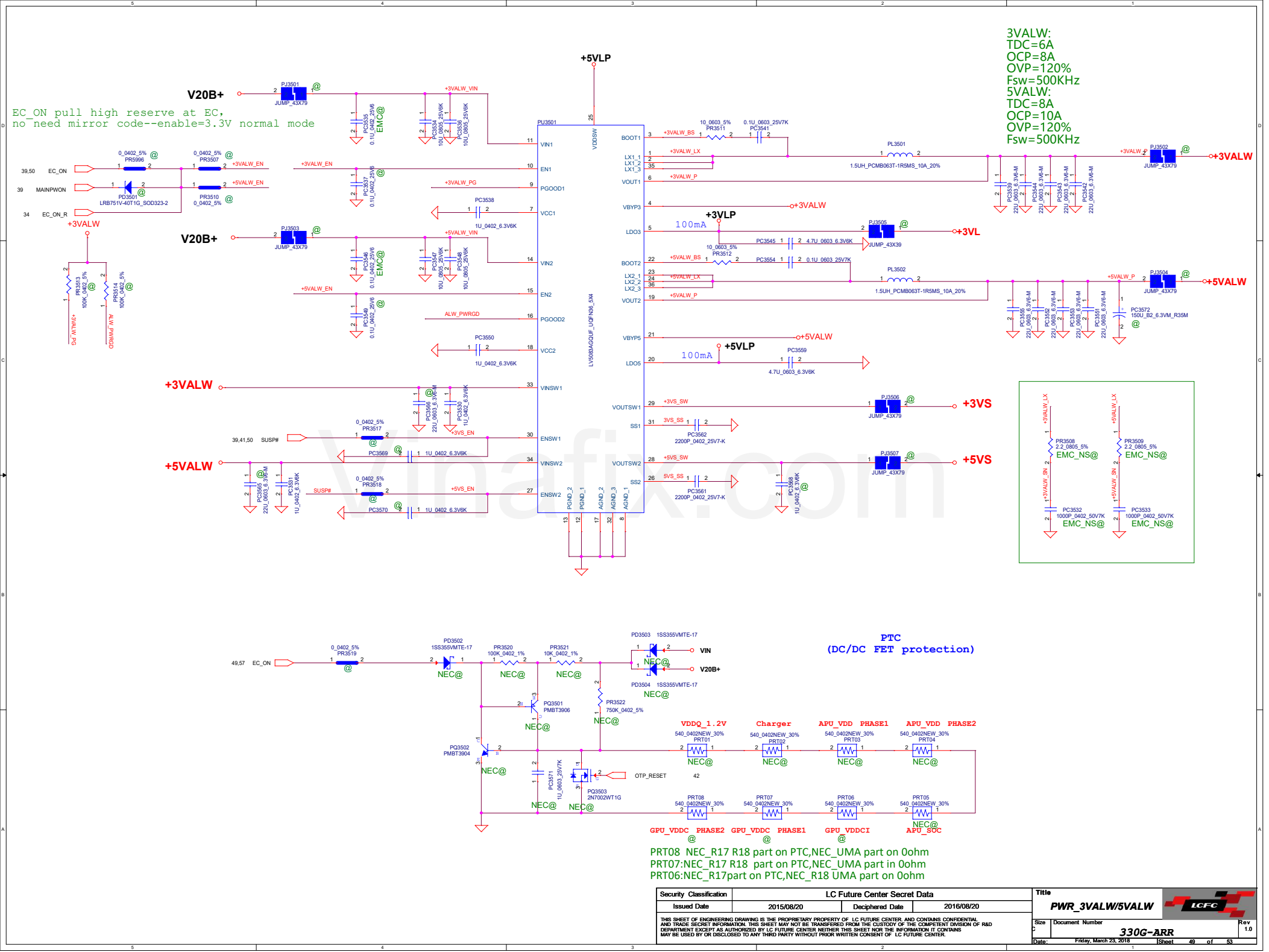


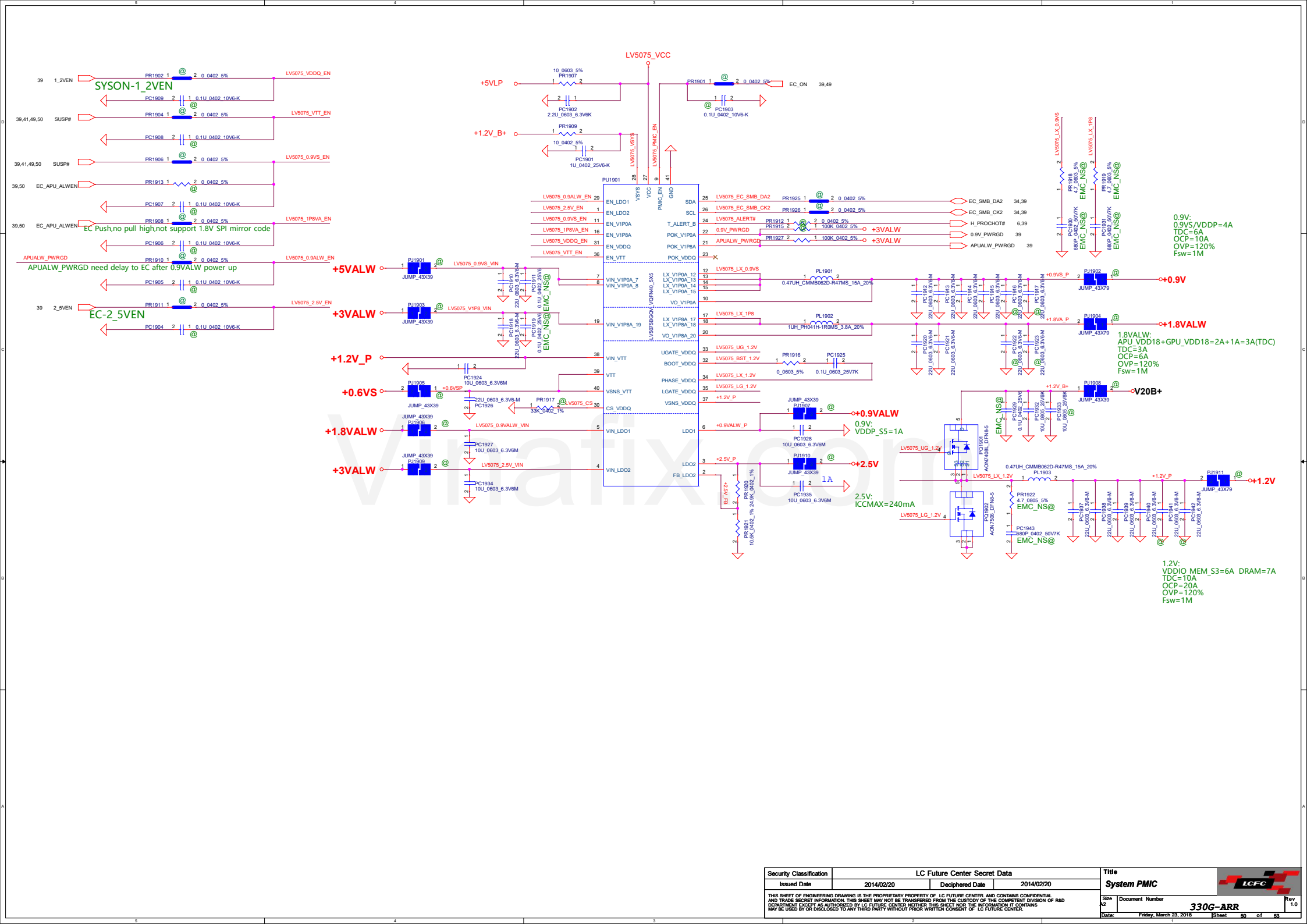
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	CHARGER		
Size	Document Number		Rev
C	330G-ARR		1.0
Date:	Friday, March 23, 2018	Sheet	48 of 53



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	330G-ARR		1.0
Date:	Friday, March 23, 2018	Sheet	49 of 53



Security Classification	LC Future Center Secret Data		
Issued Date	2014/02/20	Deciphered Date	2014/02/20

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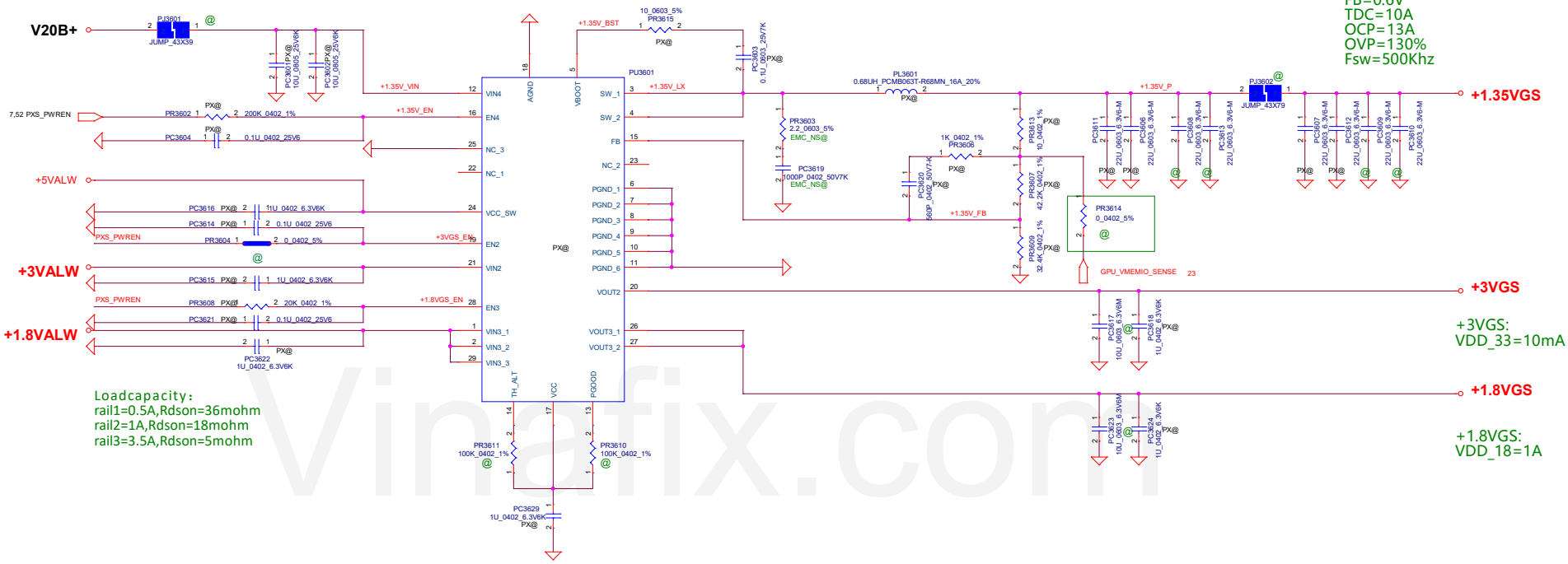
Title	System PMIC		
Size	Document Number		Rev
A2	330G-ARR		1.0
Date:	Friday, March 23, 2018	Sheet	50 of 53

modify symbol PN:SA00008WM00, S IC LV5095BGQUF UQFN 29P PMIC need update new SYMBOL



+1.35VGS:
VMEMIO=2A/8A memory=6A
FB=0.6V
TDC=10A
OCP=13A
OVP=130%
Fsw=500Khz

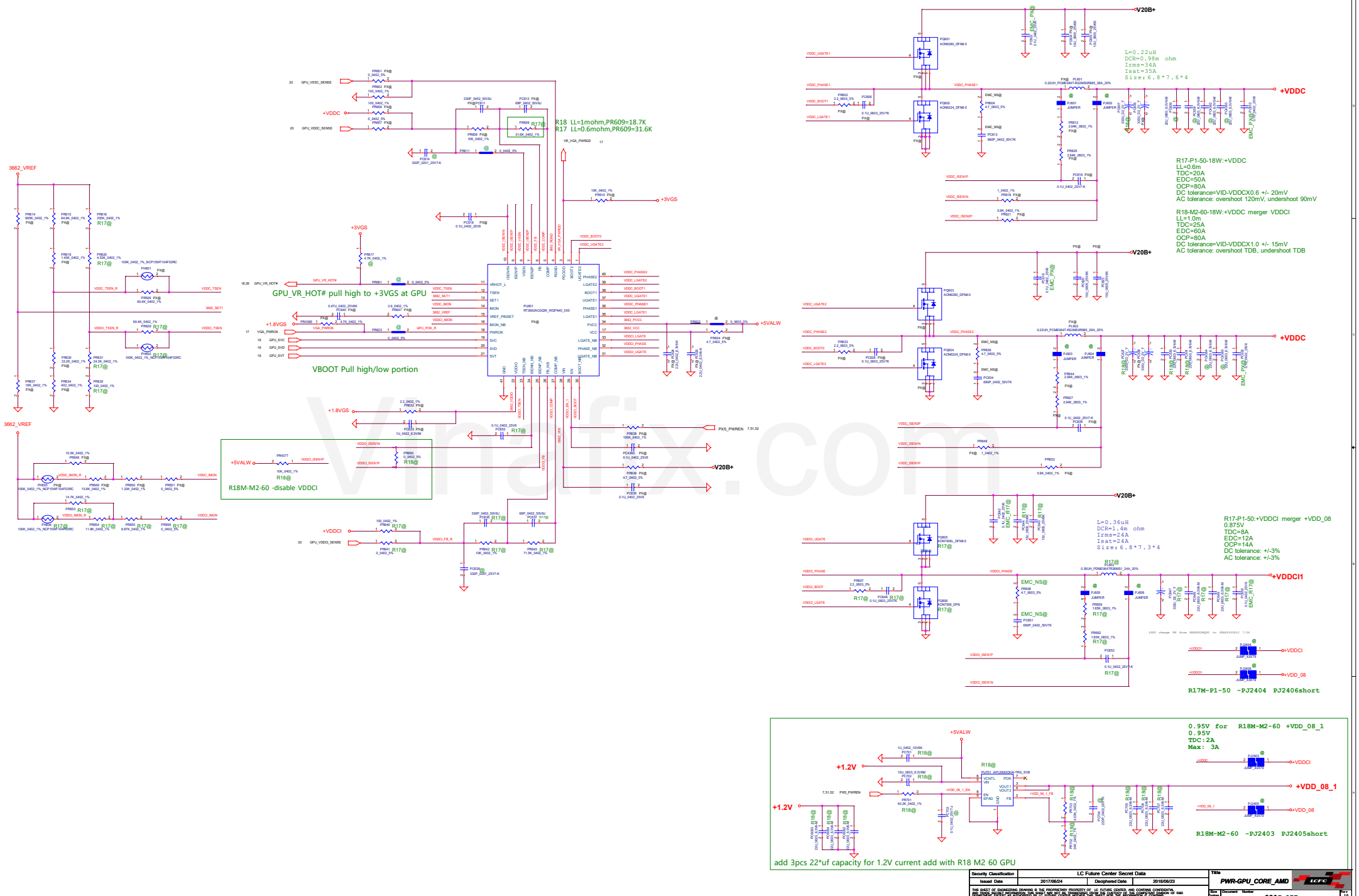
+3VGS:
VDD_33=10mA

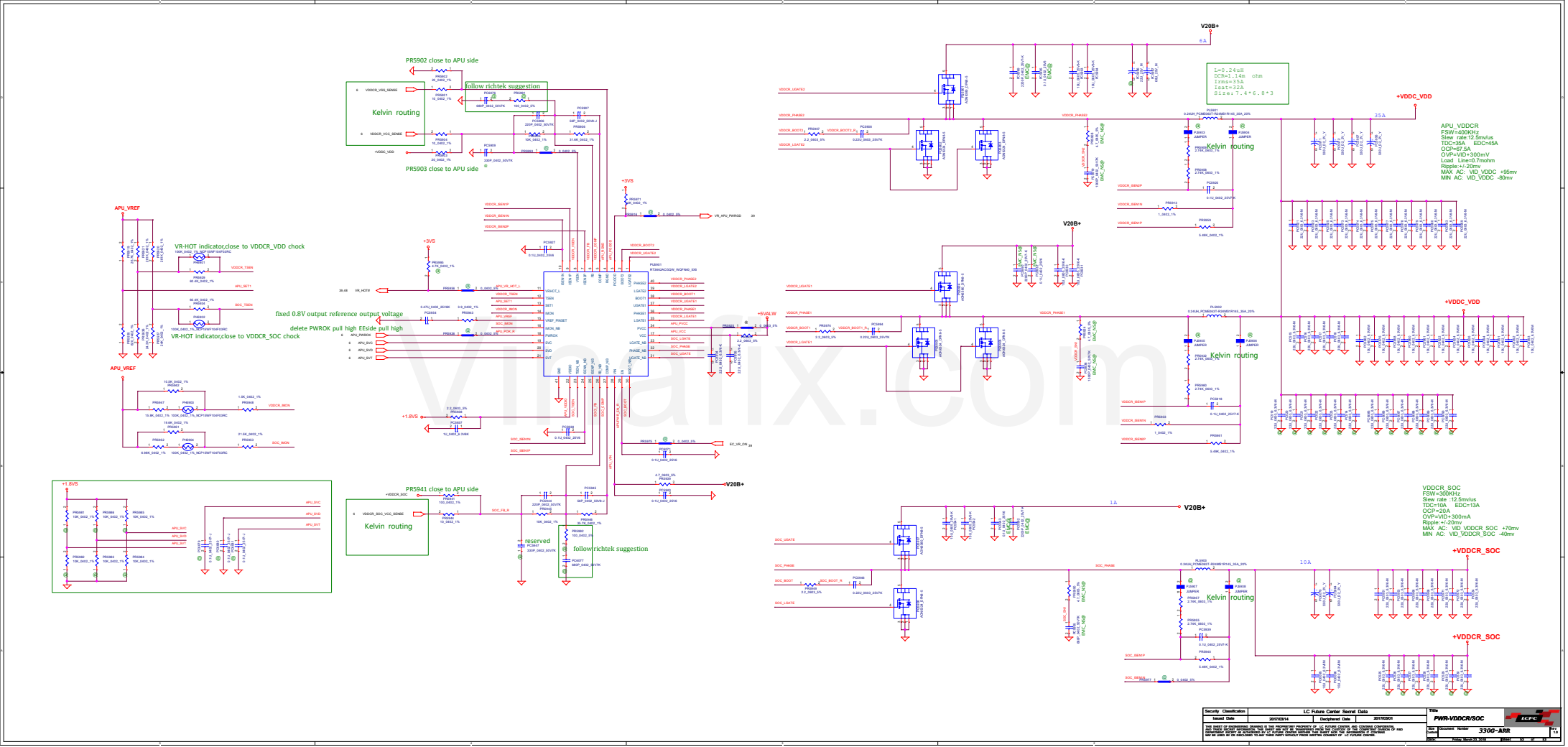
+1.8VGS:
VDD_18=1A

Loadcapacity:
rail1=0.5A,Rdson=36mohm
rail2=1A,Rdson=18mohm
rail3=3.5A,Rdson=5mohm

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	PWR_1.35VGS		
Size	Document Number		Rev
A2	330G-ARR		1.0
Date:	Friday, March 23, 2018	Sheet 51 of 53	


3662_VREF
GPU_VR_HOT# pull high to +3VGS at GPU
VBOOT Pull high/low portion
R18M-M2-60 -disable VDDCI
R18 LL=1mohm,PR609=18.7K
R17 LL=0.6mohm,PR609=31.6K
L=0.22uH
DCR=0.98m ohm
Irms=34A
Isat=35A
Size:6.8*7.6*4
+VDDC
R17-P1-50-18W:+VDDC
LL=0.6m
TDC=20A
EDC=50A
OCP=80A
DC tolerance=VID-VDDCX0.6 +/- 20mV
AC tolerance: overshoot 120mV, undershoot 90mV
R18-M2-60-18W:+VDDC merger VDDCI
LL=1.0m
TDC=25A
EDC=60A
OCP=80A
DC tolerance=VID-VDDCX1.0 +/- 15mV
AC tolerance: overshoot TDB, undershoot TDB
L=0.36uH
DCR=1.4m ohm
Irms=24A
Isat=24A
Size:6.8*7.3*4
+VDDCI1
R17-P1-50:+VDDCI merger +VDD_08
0.875V
TDC=8A
EDC=12A
OCP=14A
DC tolerance: +/-3%
AC tolerance: +/-3%
R17M-P1-50 -PJ2404 PJ2406short
0.95V for R18M-M2-60 +VDD_08_1
0.95V
TDC:2A
Max: 3A
+VDD_08_1
R18M-M2-60 -PJ2403 PJ2405short
add 3pcs 22*uf capacity for 1.2V current add with R18 M2 60 GPU
330G-ARR


PR5902 close to APU side
follow richtek suggestion
Kelvin routing
PR5903 close to APU side
APU_VREF
VR-HOT indicator,close to VDDCR_VDD chock
VR-HOT indicator,close to VDDCR_SOC chock
fixed 0.8V output reference output voltage
delete PWROK pull high ESide pull high
+3VS
+1.8VS
+5VALW
+V20B+
PR5941 close to APU side
reserved
follow richtek suggestion
V20B+
6A
L=0.24uH
DCR=1.14m ohm
Irms=35A
Isat=32A
Size:7.4*6.8*3
+VDDC_VDD
35A
APU_VDDCR
FSW=400KHz
Slew rate:12.5mv/us
TDC=35A EDC=45A
OCP=67.5A
OVP=VID+300mV
Load Line=0.7mohm
Ripple:+/-20mv
MAX AC: VID_VDDC +95mv
MIN AC: VID_VDDC -80mv
Kelvin routing
1A
10A
VDDCR_SOC
FSW=300KHz
Slew rate :12.5mv/us
TDC=10A EDC=13A
OCP=20A
OVP=VID+300mA
Ripple:+/-20mv
MAX AC: VID_VDDCR_SOC +70mv
MIN AC: VID_VDDCR_SOC -40mv
+VDDCR_SOC
PWR-VDDCR/SOC
330G-ARR
LC Future Center Secret Data
2017/03/14
2017/03/01
Tuesday, March 21, 2017