Hades_840M_ULT
Schematics Document

HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

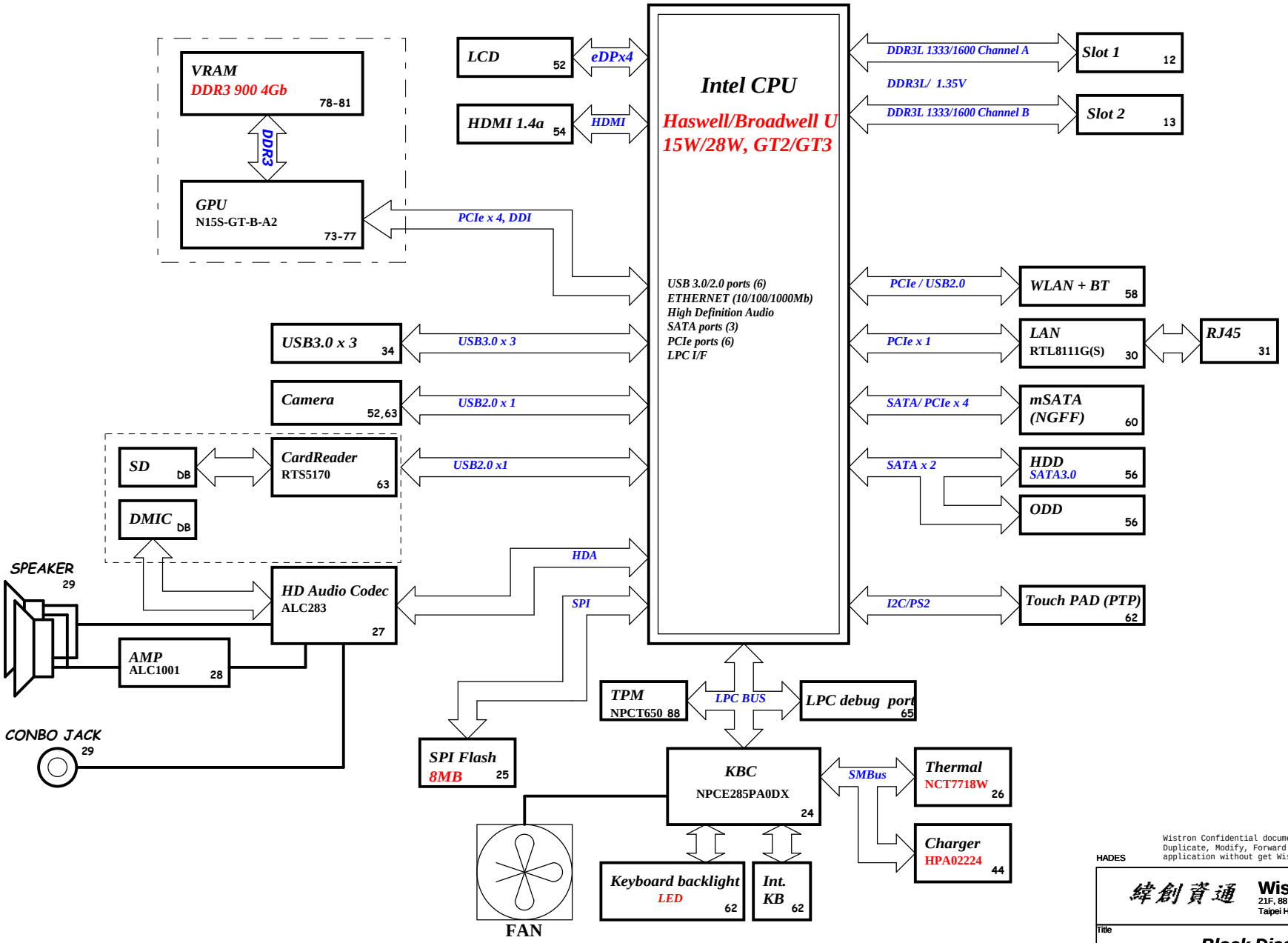
Title: Cover Page

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 1 of 102

Hades ULV Board Block Diagram

Project code : 4PD02F010001
PCB P/N : 14205
Revision : -1



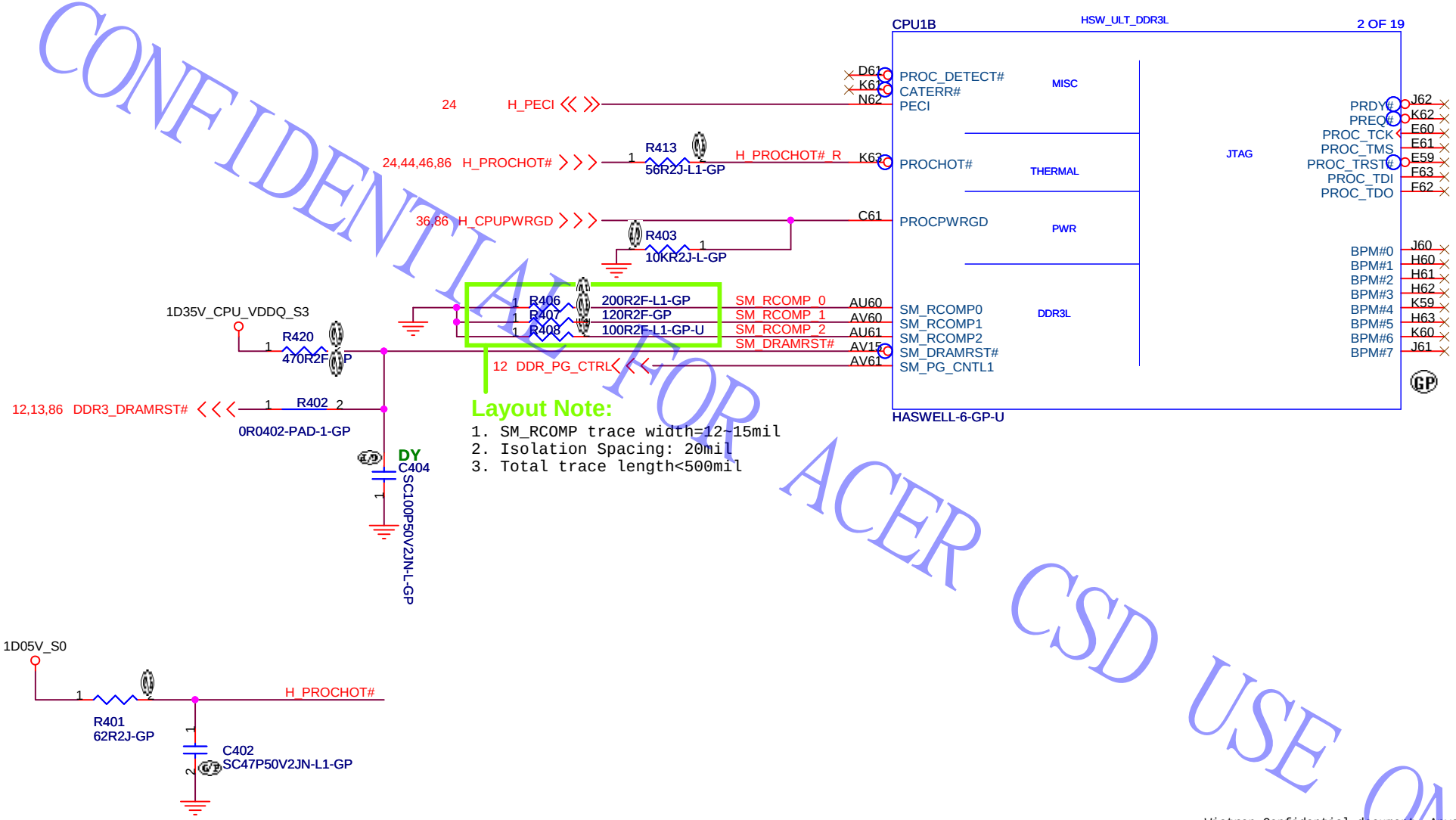
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Thursday, May 22, 2014 | Sheet 2 of 102



HADES

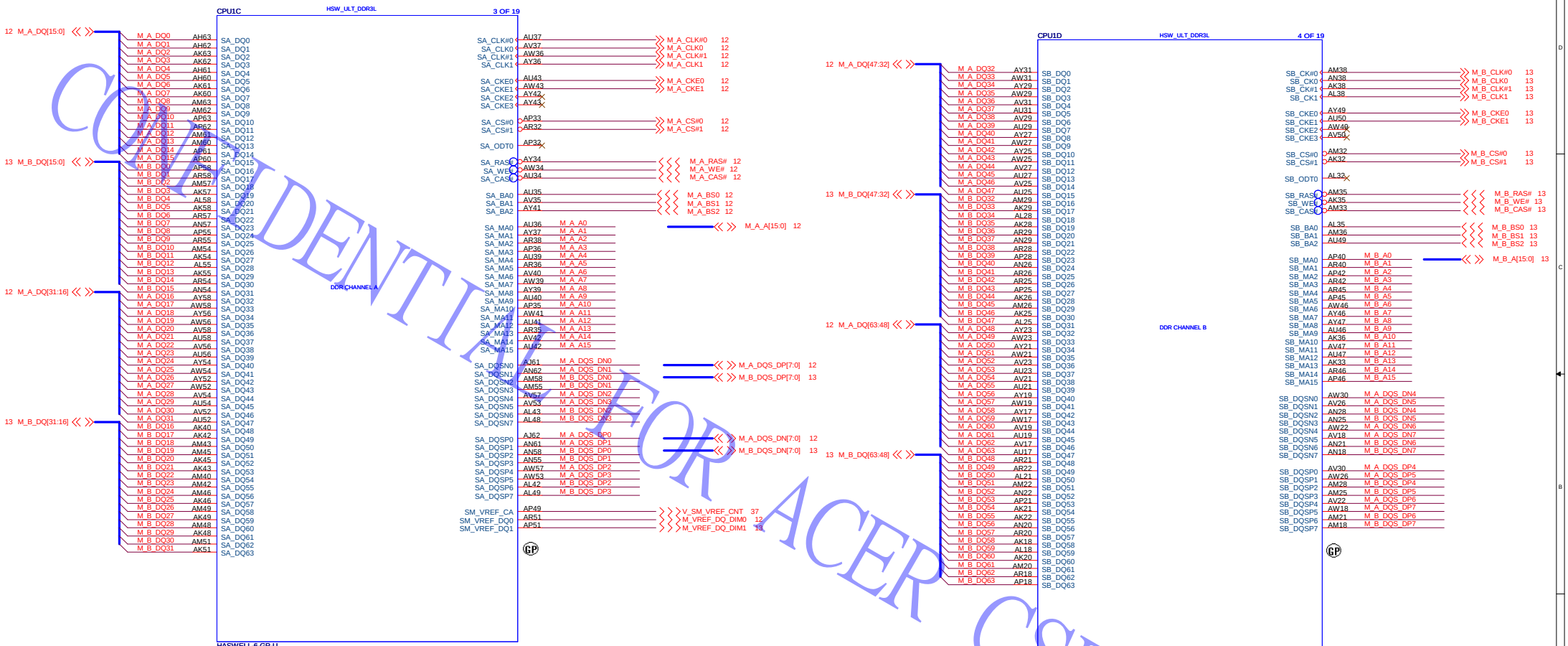
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THERMAL/CLOCK/PM)

Size: A4 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 4 of 102

SSID = CPU



HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (DDR)***

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

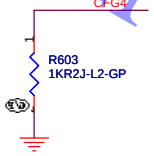
Date: Wednesday, April 30, 2014 Sheet 5 of 102

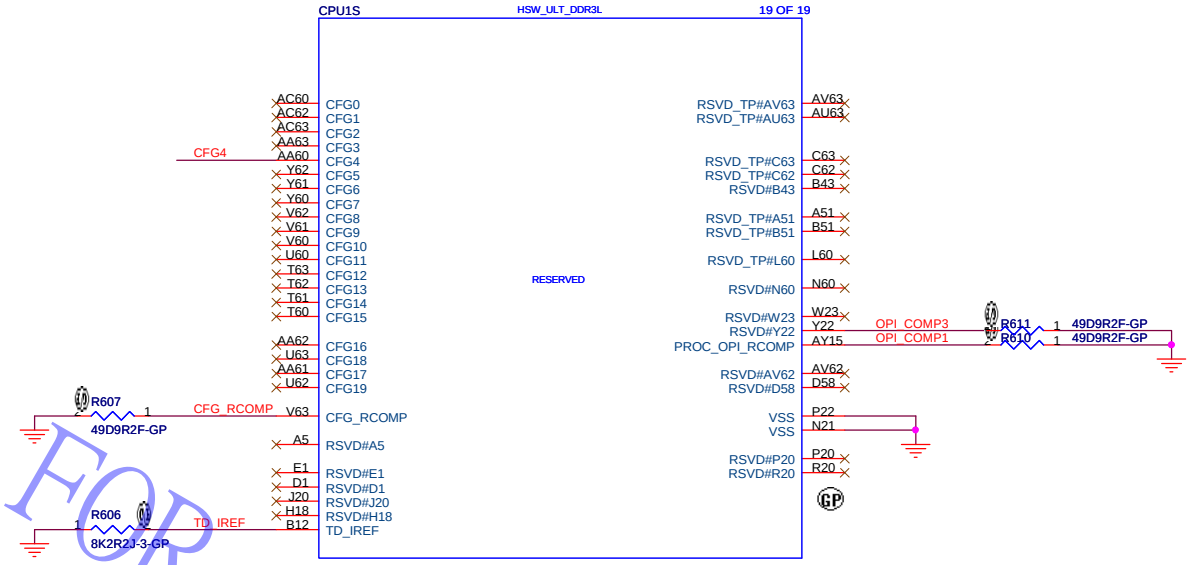
SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✔
CFG[19:0]		Please refer to the *Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)* .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

eDP Enable	
CFG4	1:Disable 0:Enable





Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

HADES

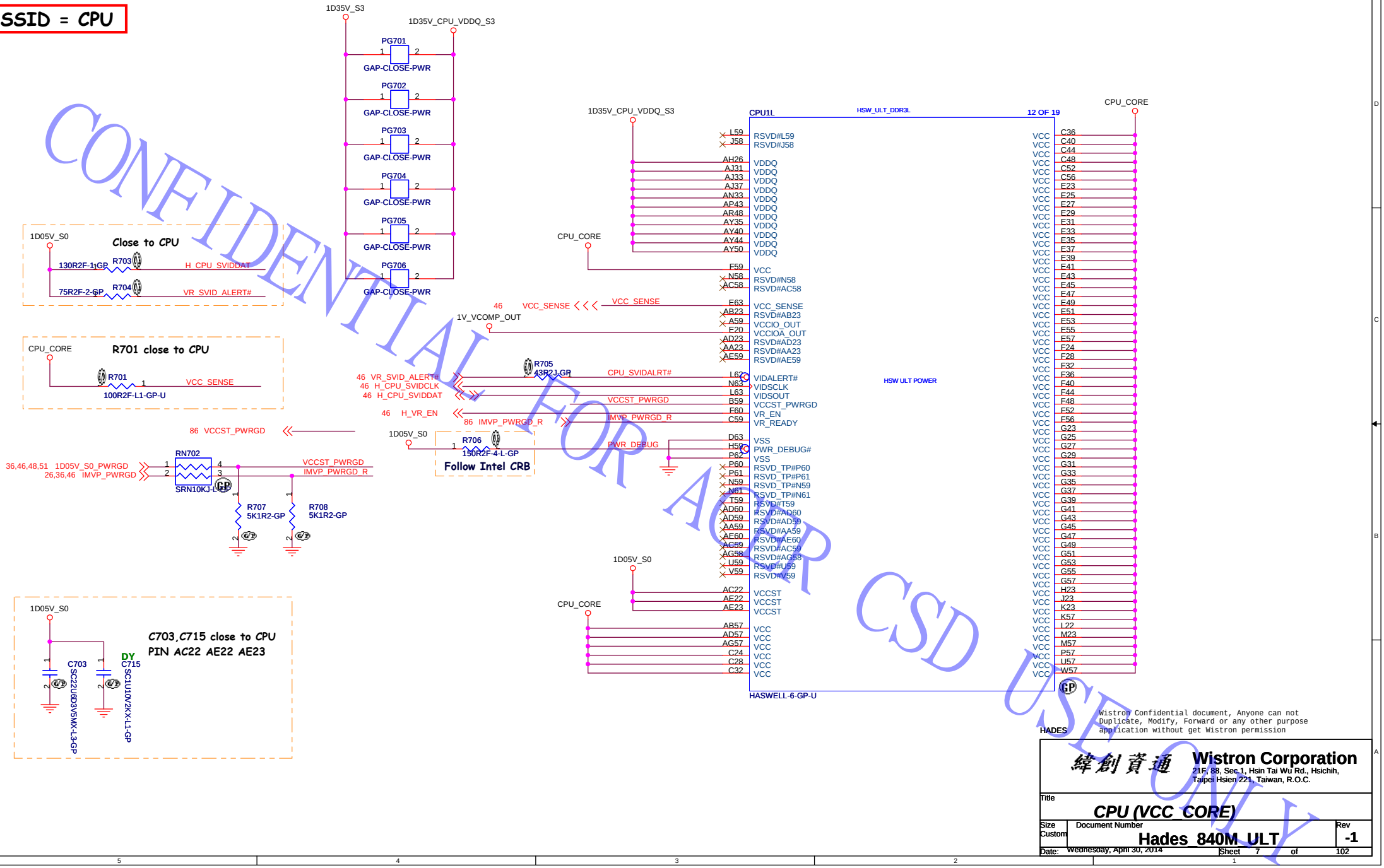
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CFG)

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 6 of 102

SSID = CPU



HADES

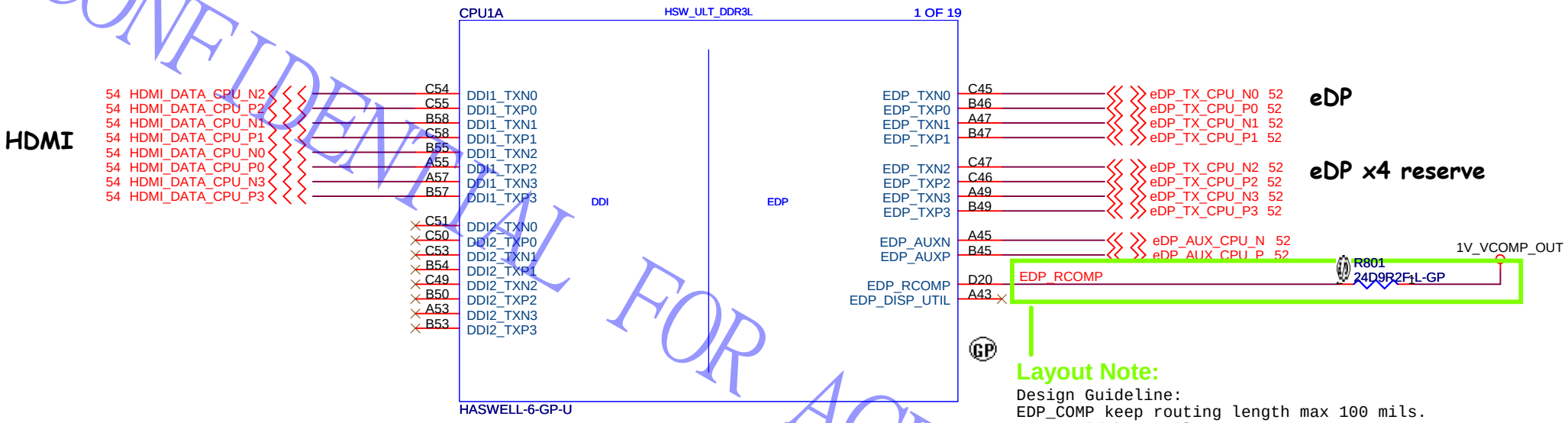
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 7 of 102

SSID = CPU



Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

HADES

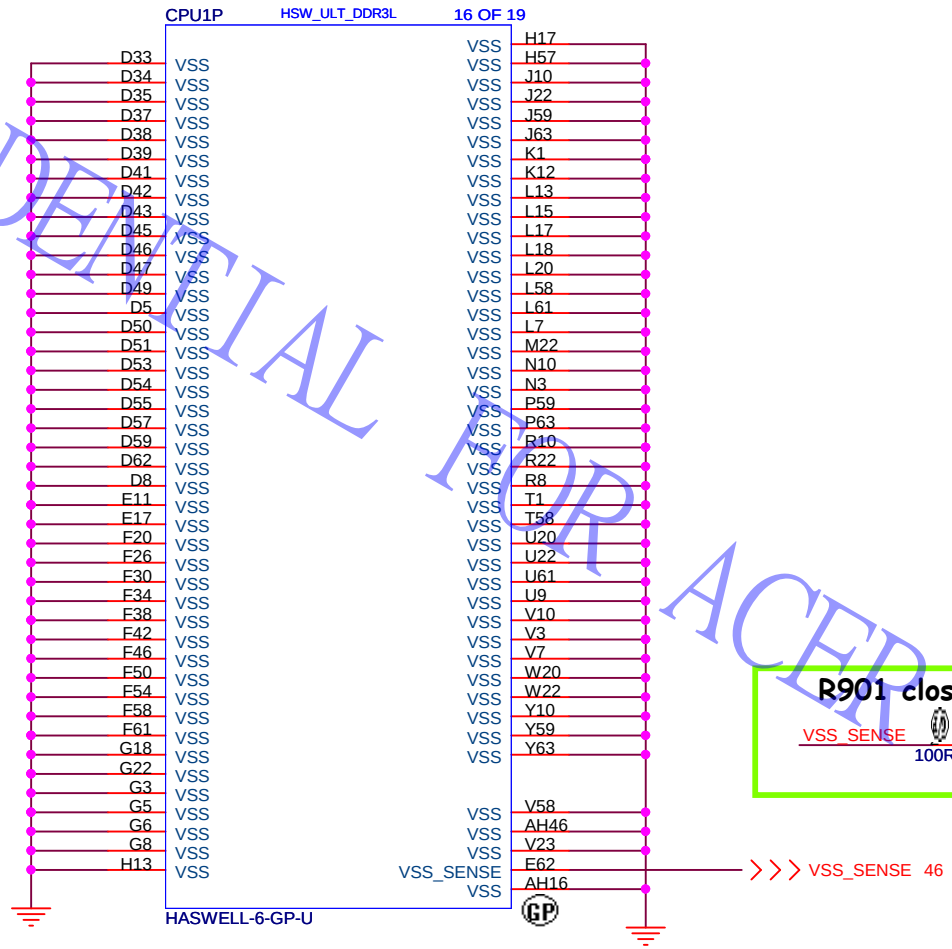
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP)

Size: A4 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 8 of 102

SSID = CPU



VSS_SENSE 46

R901 close to CPU

VSS_SENSE — R901 1 — 100R2F-L1-GP-U

Layout Note:

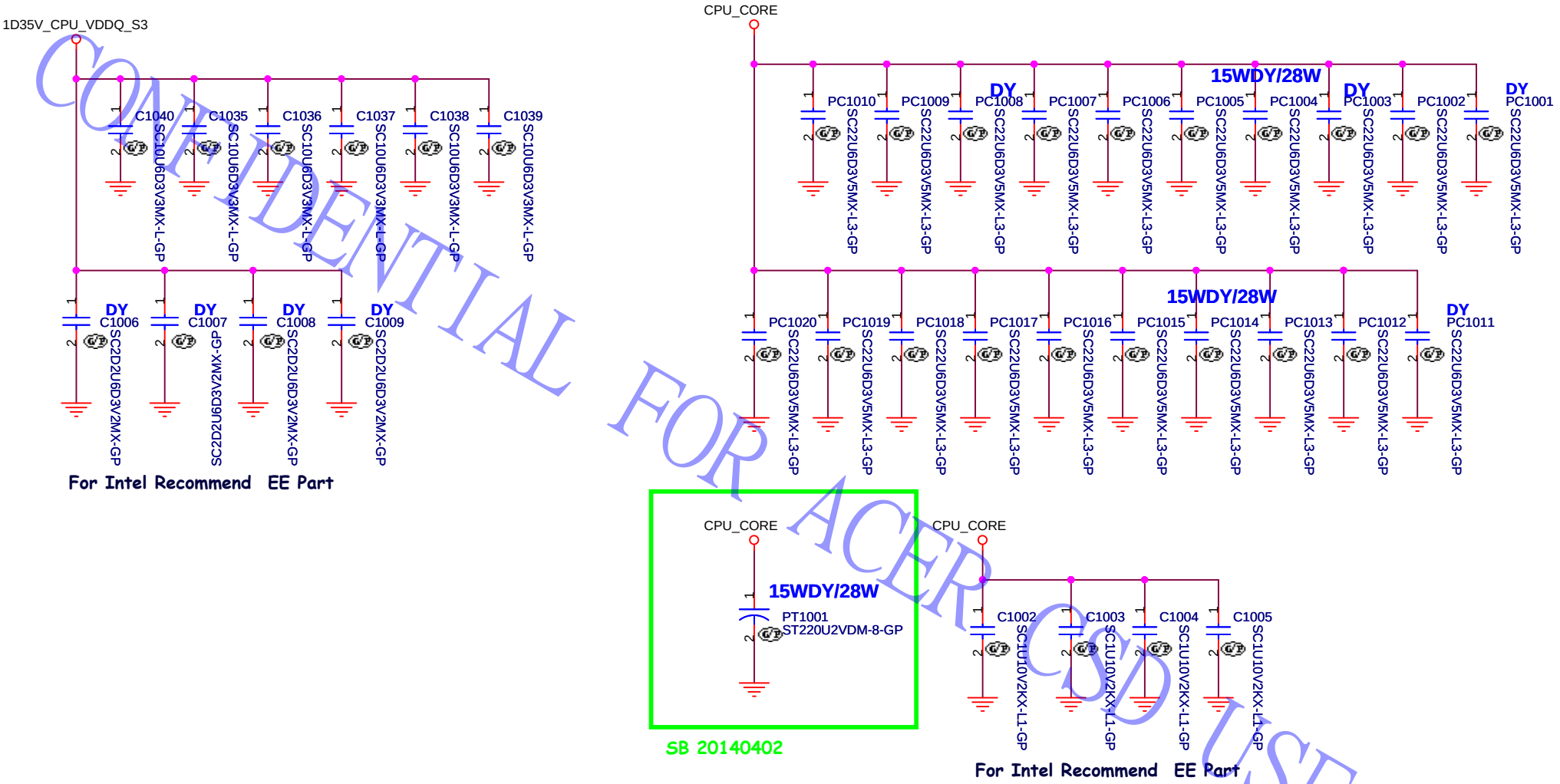
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 9 of 102



HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

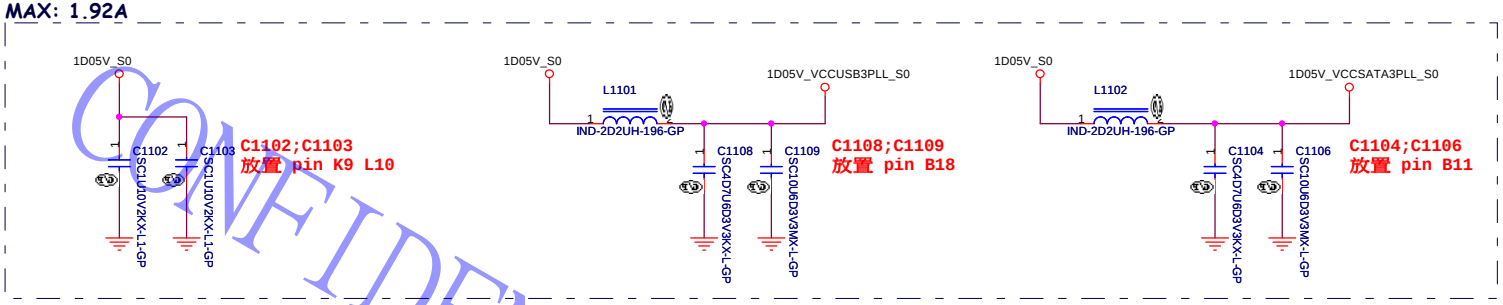
Title: **CPU (Power CAP1)**

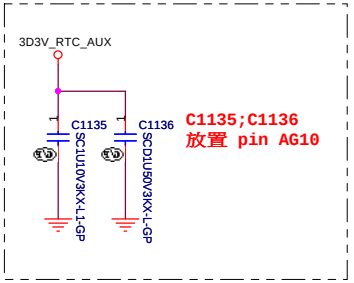
Size	Document Number	Rev
A4	Hades 840M ULT	-1

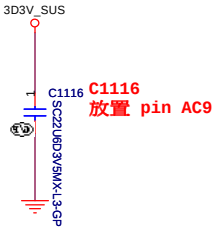
Date: Wednesday, April 30, 2014 Sheet 10 of 102

擺放電容的位置請參考 Page 21,每個位置如下

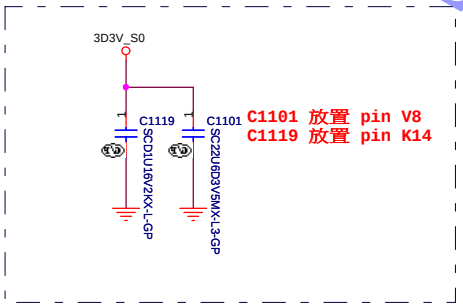
MAX: 1.92A

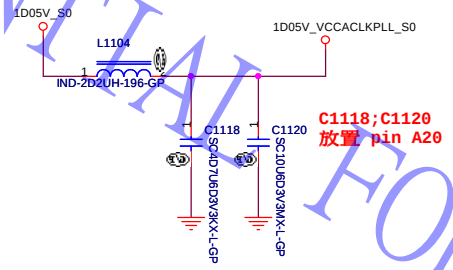




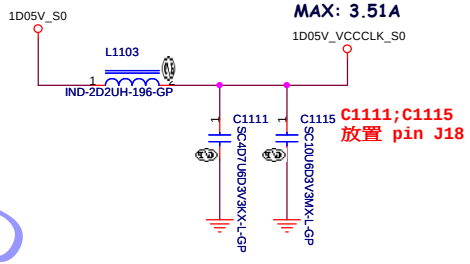


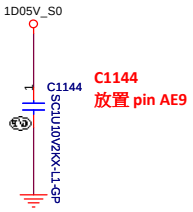
MAX: 0.285A

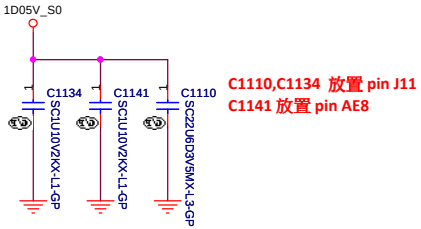




MAX: 3.51A







HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP2)

Size: Custom | Document Number: Hades 840M ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 11 of 102

SSID = MEMORY

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM Memory Connectivity and Topology
ODT Signal Connectivity and Support
For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDQ through FET and resistor. The reason for this additional ODT-control circuitry on the platform is to save power dissipation by turning off VDDQ to VTT path during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-DPC platform will be encoded in the write command and use RTT_NOM = Off and RTT_WR = (60,120) Ohm.

- CPU ODT output would be NOCON
- SODIMM ODT input should be tied to VDDQ through a FET and a resistor to support low power states.

DDR3L SODIMM ODT GENERATION

ODT resistor must be 66.5 ohm

Thermal EVENT

Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

Place these caps close to VTT1 and VTT2.

Close RAM1 CA & DQ pin

Q1202 Q1203限用於84.05067.031
因為此刻Vth為1V

For Intel Recommend Close to DIMM

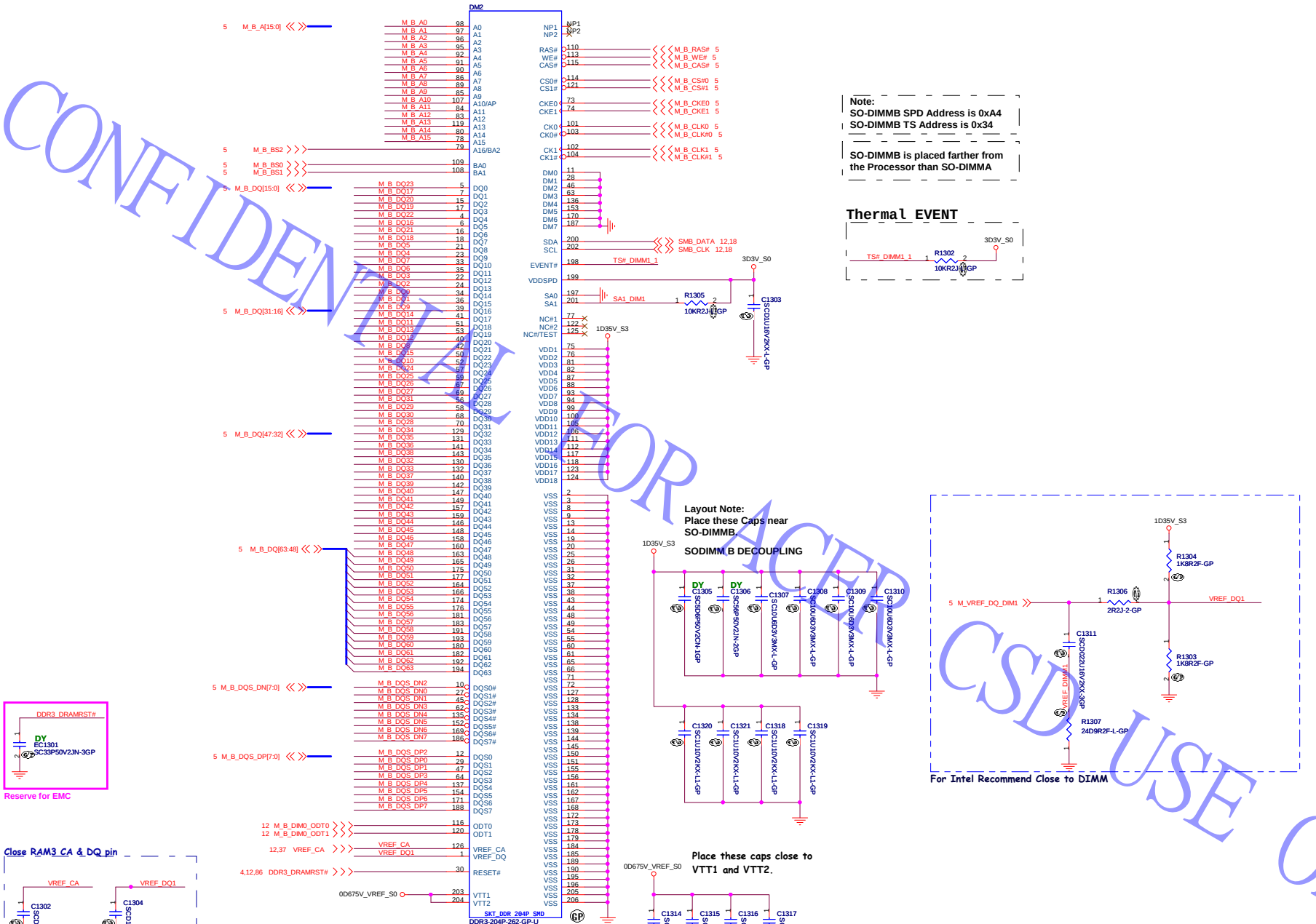
62.10024.S61
2ND = 62.10024.M51
3RD = 62.10024.Q71
4TH = 62.10017.I21

HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1
Size: A2 | Document Number: Hades_840M_ULT | Rev: -1
Date: Wednesday, April 30, 2014 | Sheet 12 of 102

SSID = MEMORY



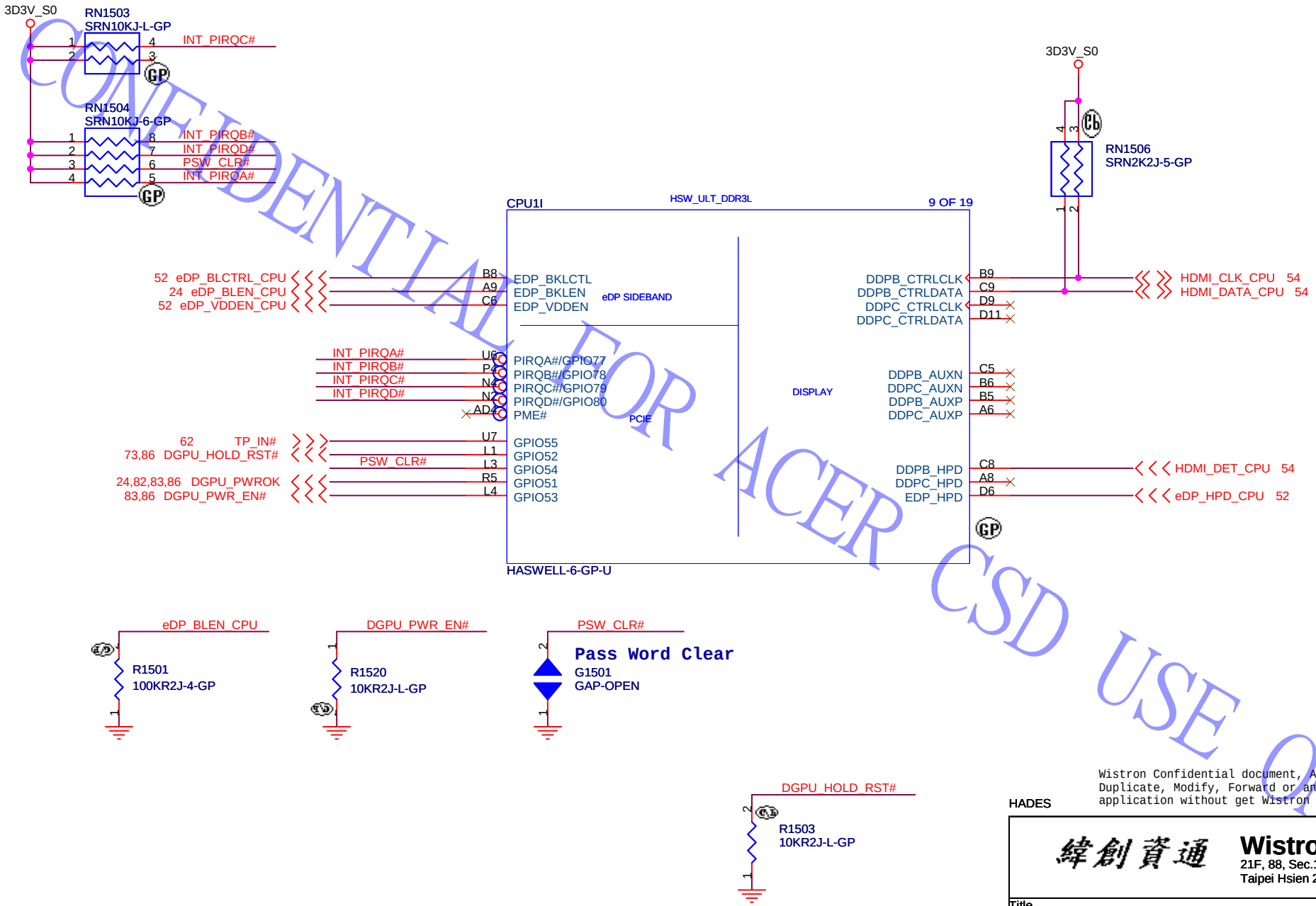
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size: Custom | Document Number: **Hades_840M_ULT** | Rev: **-1**

Date: Wednesday, April 30, 2014 | Sheet 13 of 102



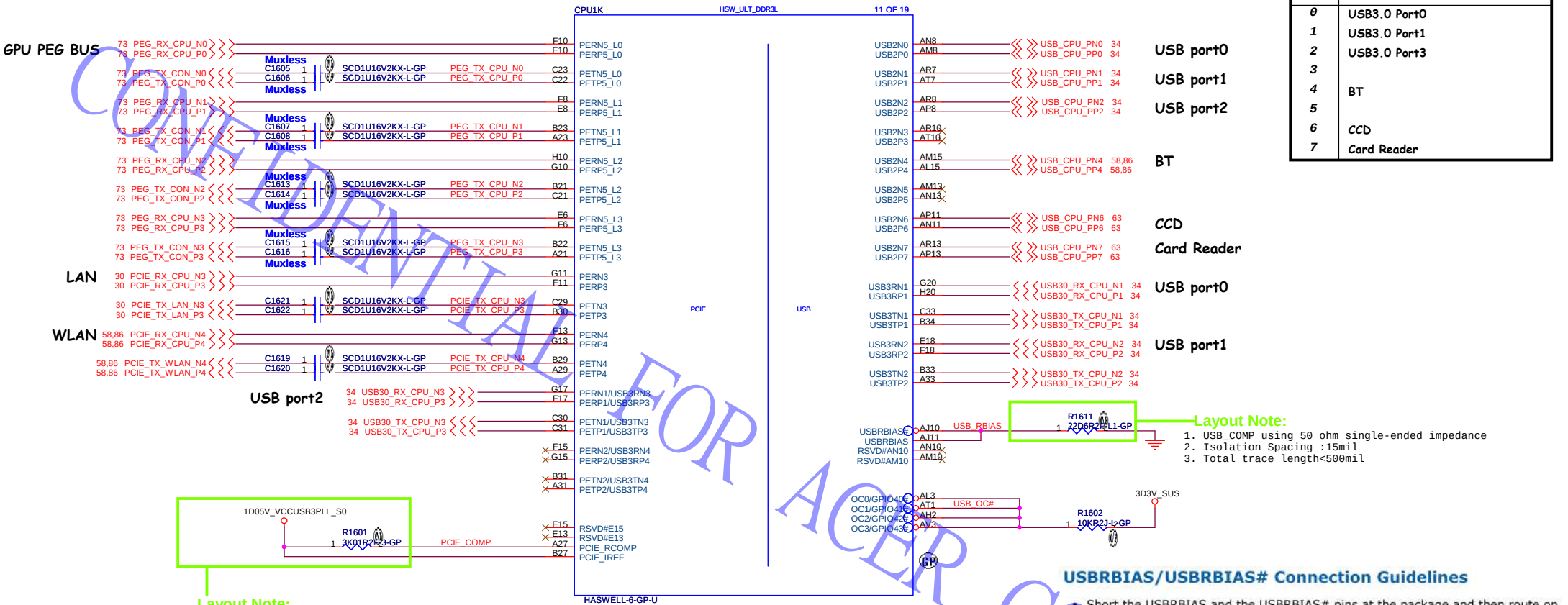
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU(EDP SIDEBAND/GPIO/DDI)***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 15 of 102



USB Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port3
3	
4	BT
5	
6	CCD
7	Card Reader

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

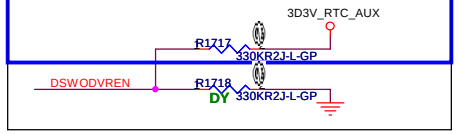
Title: **CPU (PCI/USB)**

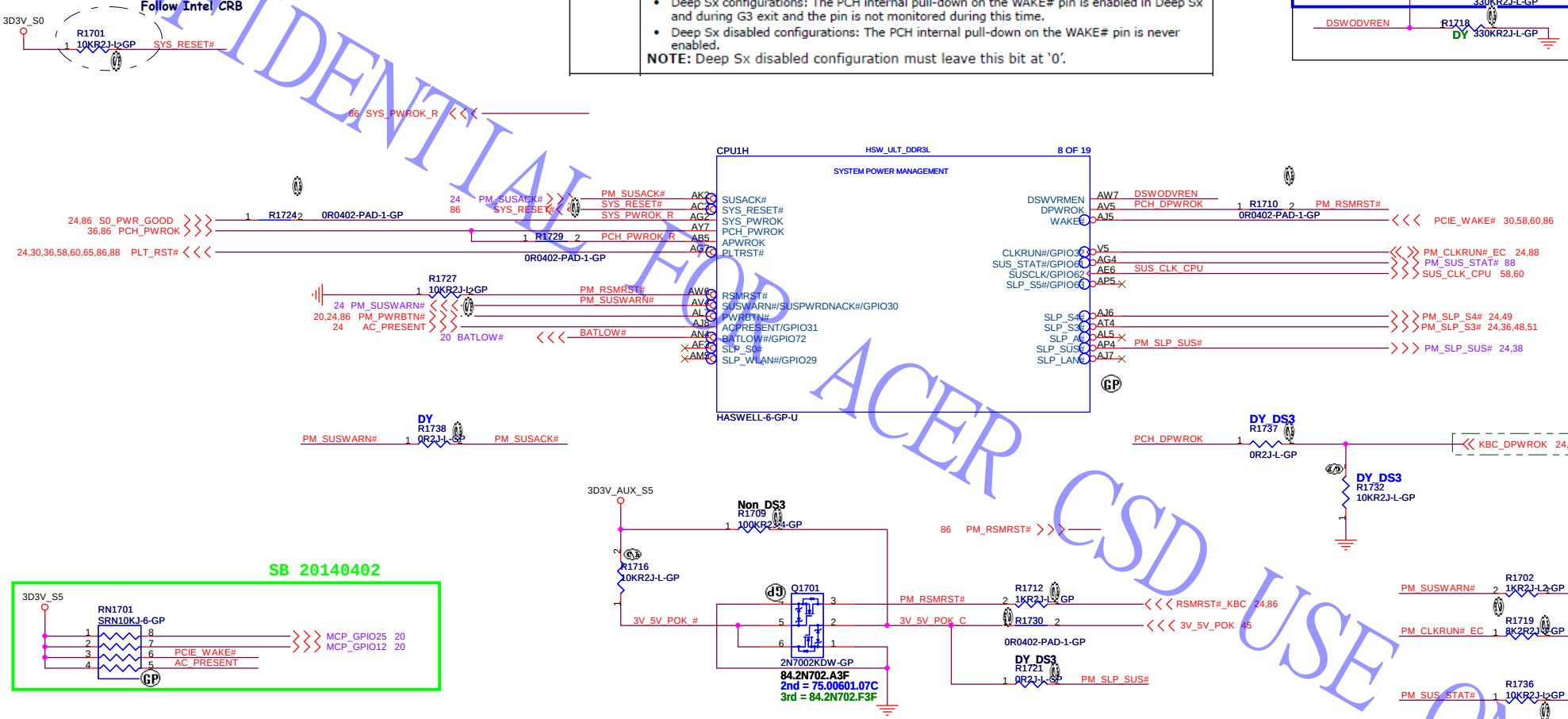
Size	Document Number	Rev
A3	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 16 of 102

Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled





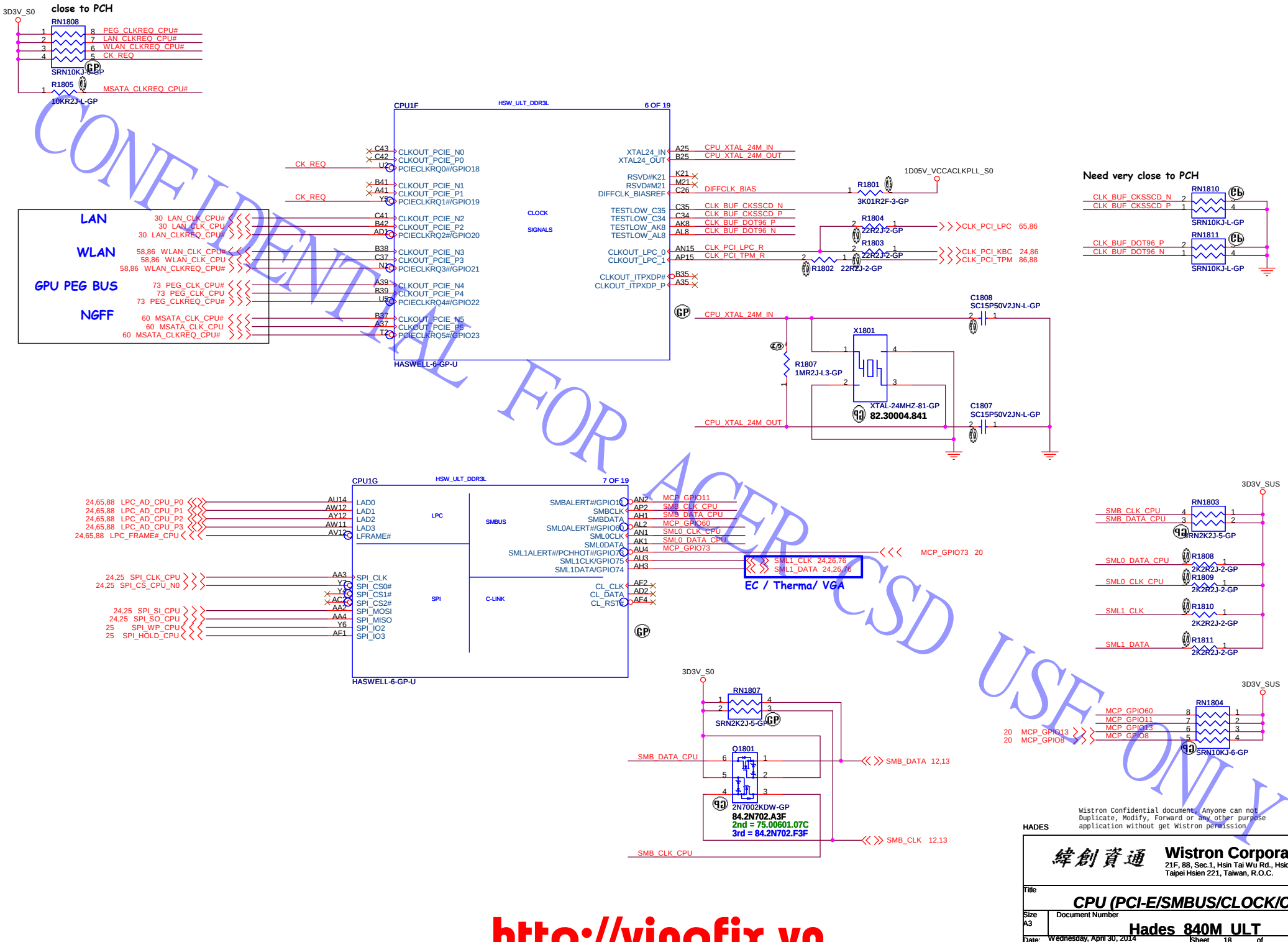
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DMI/FDI/PM)**

Size	Document Number	Rev
A3	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 17 of 102


close to PCH
3D3V_S0
RN1808
PEG_CLKREQ_CPU#
LAN_CLKREQ_CPU#
WLAN_CLKREQ_CPU#
CK_REQ
SRN10KJ-6-GP
R1805
10KR2J-L-GP
MSATA_CLKREQ_CPU#
CPU1F
HSW_ULT_DDR3L
6 OF 19
CLOCK
SIGNALS
HASWELL-6-GP-U
LAN
WLAN
GPU PEG BUS
NGFF
30 LAN_CLK_CPU#
30 LAN_CLK_CPU
30 LAN_CLKREQ_CPU#
58,86 WLAN_CLK_CPU#
58,86 WLAN_CLK_CPU
58,86 WLAN_CLKREQ_CPU#
73 PEG_CLK_CPU#
73 PEG_CLK_CPU
73 PEG_CLKREQ_CPU#
60 MSATA_CLK_CPU#
60 MSATA_CLK_CPU
60 MSATA_CLKREQ_CPU#
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
PCIECLKRQ0#/GPIO18
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
PCIECLKRQ1#/GPIO19
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
PCIECLKRQ2#/GPIO20
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
PCIECLKRQ3#/GPIO21
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
PCIECLKRQ4#/GPIO22
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
PCIECLKRQ5#/GPIO23
XTAL24_IN
XTAL24_OUT
CPU_XTAL_24M_IN
CPU_XTAL_24M_OUT
RSVD#K21
RSVD#M21
DIFFCLK_BIASREF
DIFFCLK_BIAS
1D05V_VCCACLKPLL_S0
R1801
3K01R2F-3-GP
TESTLOW_C35
TESTLOW_C34
TESTLOW_AK8
TESTLOW_AL8
CLK_BUF_CKSSCD_N
CLK_BUF_CKSSCD_P
CLK_BUF_DOT96_P
CLK_BUF_DOT96_N
R1804
22R2J-2-GP
CLK_PCI_LPC 65,86
CLKOUT_LPC_0
CLKOUT_LPC_1
CLK_PCI_LPC_R
CLK_PCI_TPM_R
R1803
CLK_PCI_KBC 24,86
CLK_PCI_TPM 86,88
R1802
CLKOUT_ITPXDP#
CLKOUT_ITPXDP_P
Need very close to PCH
RN1810
RN1811
SRN10KJ-L-GP
C1808
SC15P50V2JN-L-GP
X1801
R1807
1MR2J-L3-GP
XTAL-24MHZ-81-GP
82.30004.841
C1807
CPU1G
HSW_ULT_DDR3L
7 OF 19
LPC
SMBUS
SPI
C-LINK
LAD0
LAD1
LAD2
LAD3
LFRAME#
24,65,88 LPC_AD_CPU_P0
24,65,88 LPC_AD_CPU_P1
24,65,88 LPC_AD_CPU_P2
24,65,88 LPC_AD_CPU_P3
24,65,88 LPC_FRAME#_CPU
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_CS2#
SPI_MOSI
SPI_MISO
SPI_IO2
SPI_IO3
24,25 SPI_CLK_CPU
24,25 SPI_CS_CPU_N0
24,25 SPI_SI_CPU
24,25 SPI_SO_CPU
25 SPI_WP_CPU
25 SPI_HOLD_CPU
SMBALERT#/GPIO10
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO7
SML1CLK/GPIO75
SML1DATA/GPIO74
CL_CLK
CL_DATA
CL_RST
MCP_GPIO11
SMB_CLK_CPU
SMB_DATA_CPU
MCP_GPIO60
MCP_GPIO73
SML1_CLK 24,26,76
SML1_DATA 24,26,76
MCP_GPIO73 20
EC / Therma/ VGA
3D3V_SUS
RN1803
SRN2K2J-5-GP
SML0_DATA_CPU
SML0_CLK_CPU
SML1_CLK
SML1_DATA
R1808
R1809
R1810
R1811
2K2R2J-2-GP
3D3V_S0
RN1807
Q1801
2N7002KDW-GP
84.2N702.A3F
2nd = 75.00601.07C
3rd = 84.2N702.F3F
SMB_DATA 12,13
SMB_CLK 12,13
RN1804
SRN10KJ-6-GP
20 MCP_GPIO13
20 MCP_GPIO8
CONFIDENTIAL FOR ACER CSD USE ONLY
Wistron Confidential document. Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission.
HADES
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PCI-E/SMBUS/CLOCK/CL)
Size A3
Document Number
Hades 840M ULT
Rev -1
Date: Wednesday, April 30, 2014
Sheet 18 of 102
http://vinafix.vn

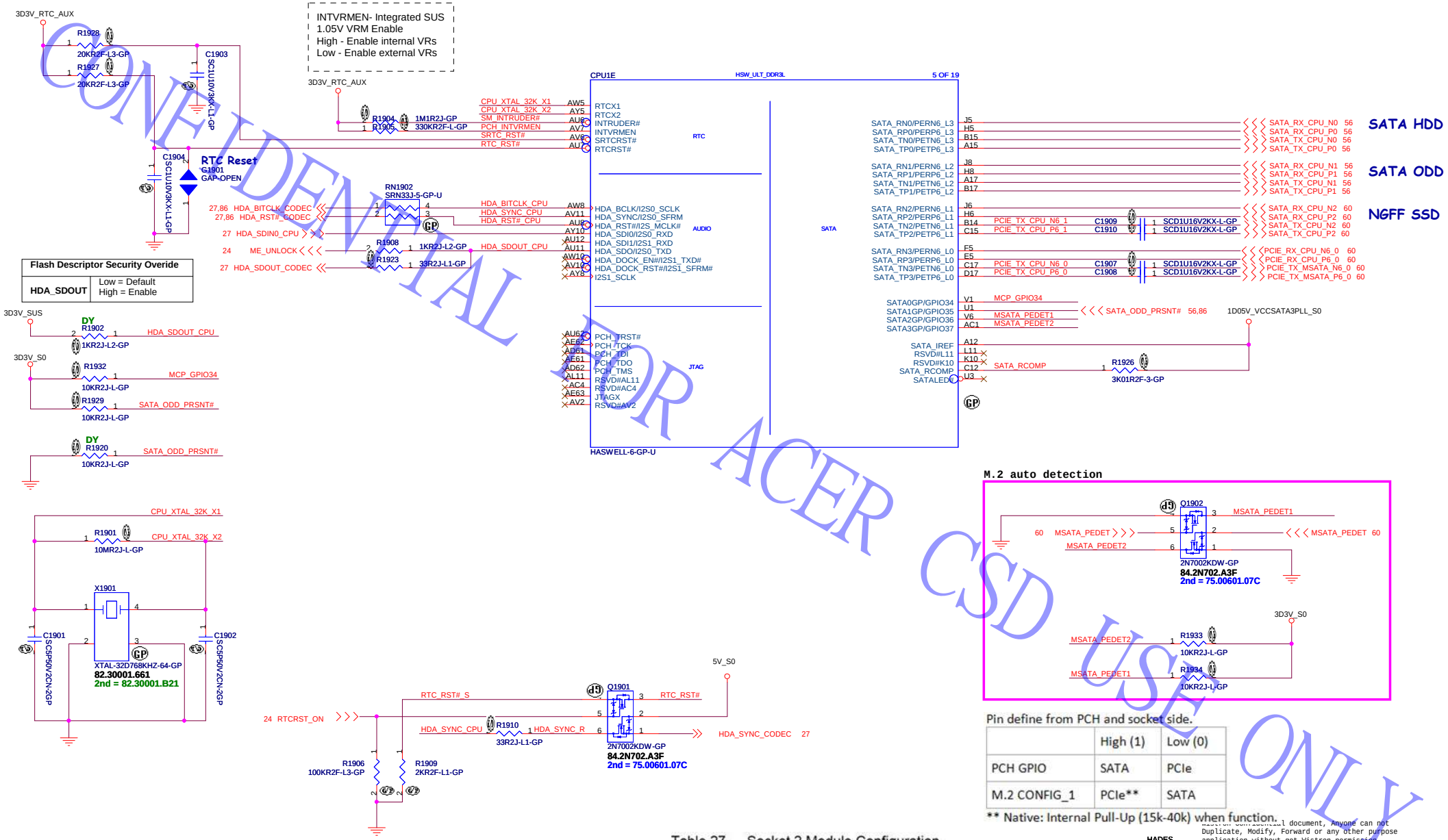
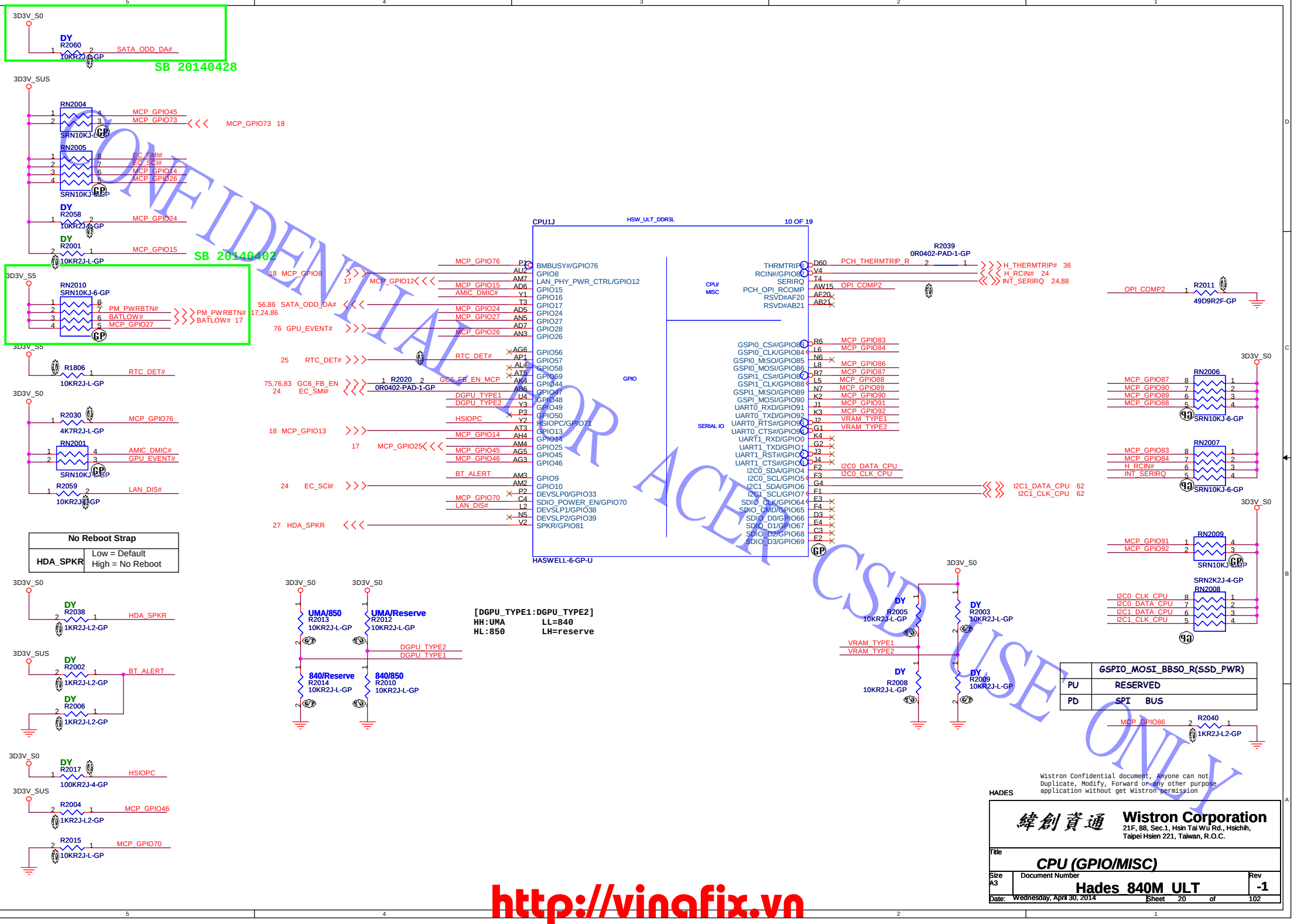


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

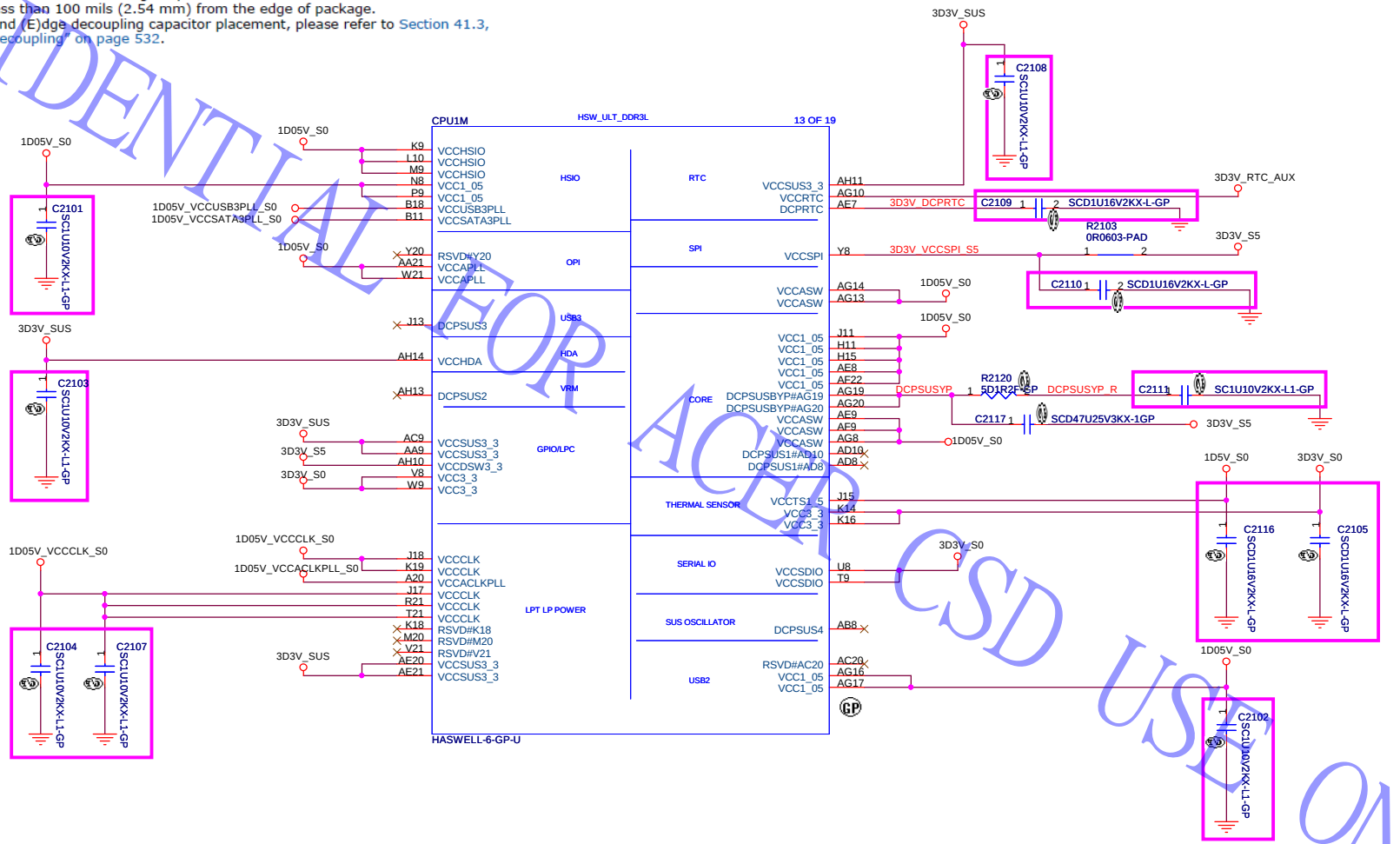
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/LPC/SATA/HDA)
Size: Custom | Document Number: Hades_840M_ULT | Rev: -1
Date: Wednesday, April 30, 2014 | Sheet 19 of 102


SB 20140428
SB 20140402
CPU1J
HSW_ULT_DDR3L
10 OF 19
HASWELL-6-GP-U
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
[DGPU_TYPE1:DGPU_TYPE2]
HH:UMA LL=840
HL:850 LH=reserve
GSPIO_MOSI_BBSO_R(SSD_PWR)
PU RESERVED
PD SPI BUS
CONFIDENTIAL FOR ACER CSD USE ONLY
Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission
HADES
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU (GPIO/MISC)
Hades_840M_ULT
-1
Wednesday, April 30, 2014
20
102
http://vinafix.vn

Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



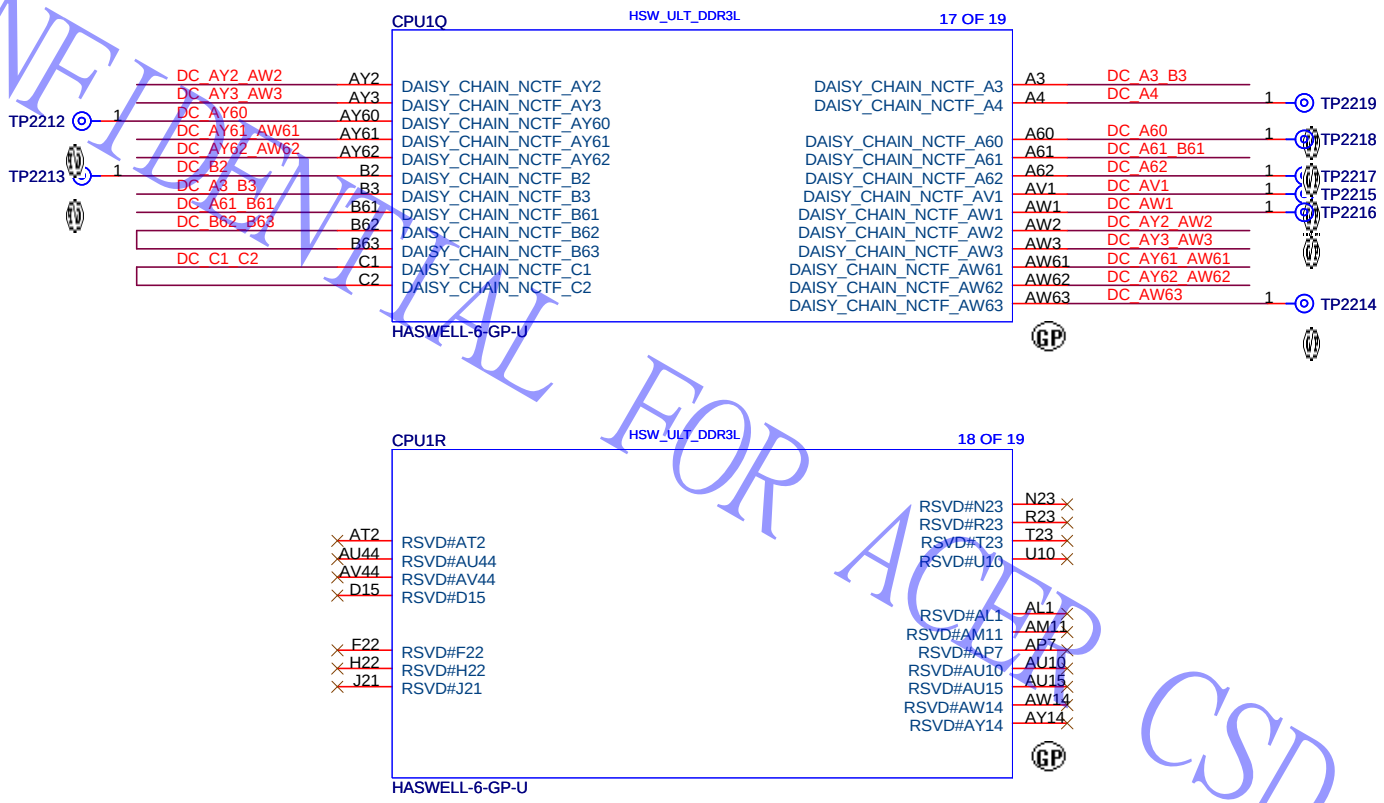
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

Size	Document Number	Rev
A3	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 21 of 102



HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (RSVD)***

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1
Date: Wednesday, April 30, 2014	Sheet 22 of 102	

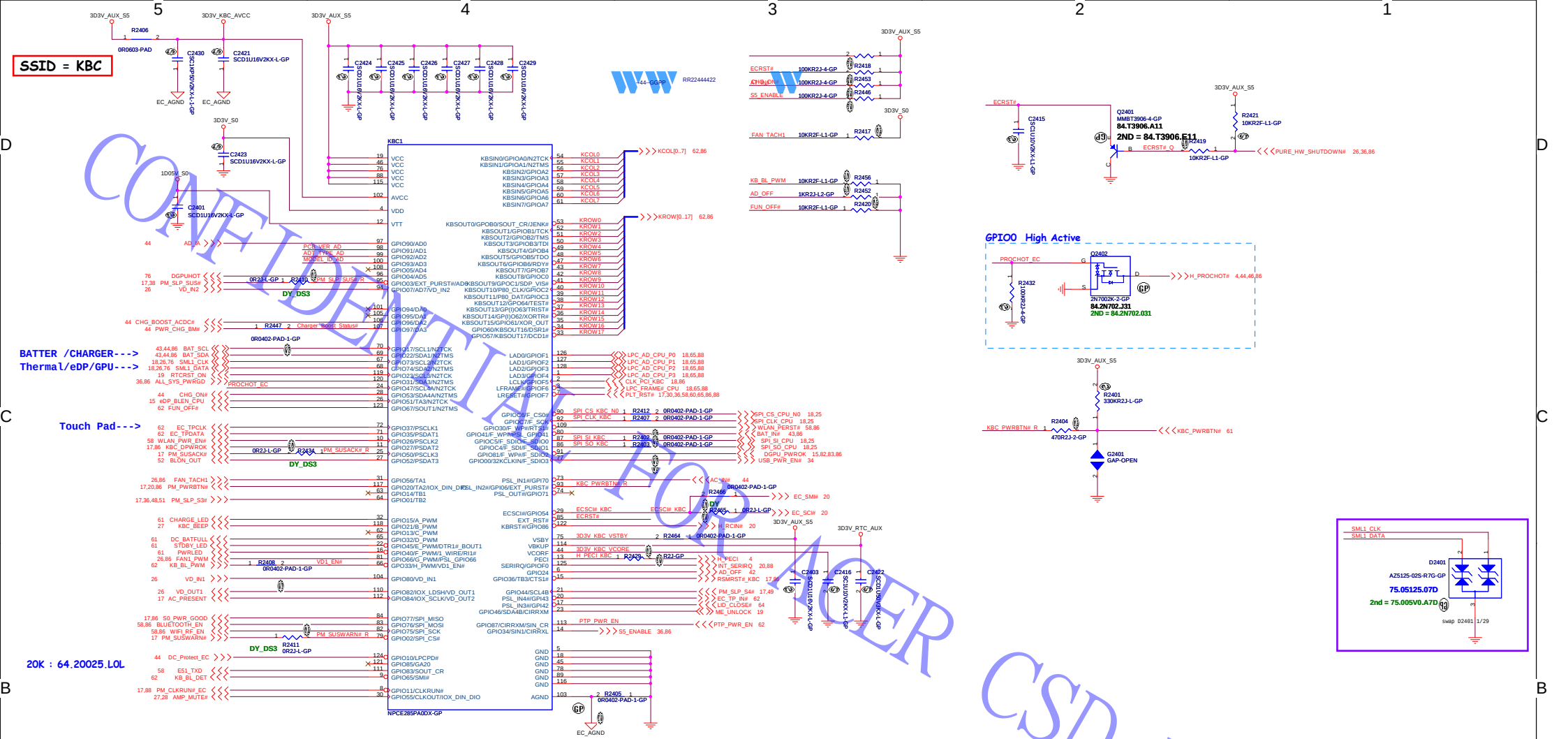
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VSS)**

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 23 of 102



Model_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
VA30	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V	
Hades UMA	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
Hades DIS 840	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
Hades DIS 850	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.363 V
Hades DIS 860	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V	< 2.123 V
Poseidon DIS 840	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V	< 1.934 V
Poseidon DIS 860	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V	< 1.758 V
Poseidon DIS 850	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.000 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.5592	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.8312	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.0695	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.3146	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	>= 1.542 V	< 1.842 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V	< 1.126 V

HADES

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_ITE8587

Size: A2 | Document Number: Hades_840M_ULT | Rev: -1

Date: Friday, May 16, 2014 | Sheet 24 of 102

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)
1ST= 072.02564.0001(AMIC A25LQ64M)
2ND=072.25B64.0001(Gigadevice GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
72.25647.00A (MXIC MX25L6473EM2I)

Figure 28-1. SPI Topology (Single Device)

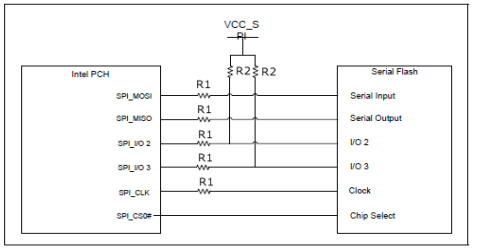
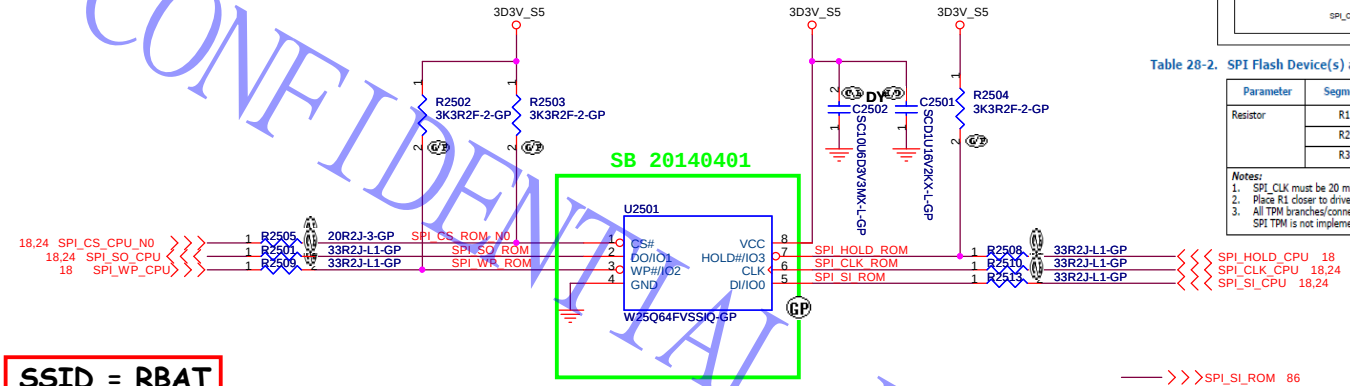


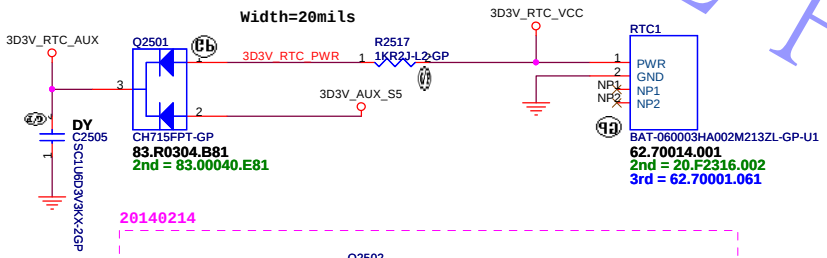
Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

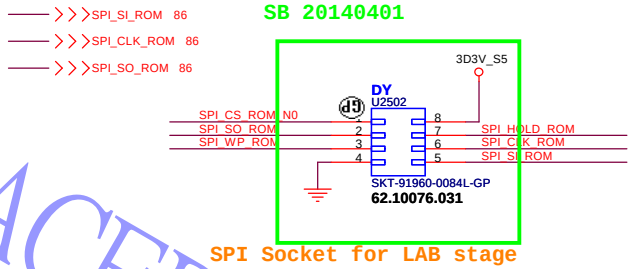
Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

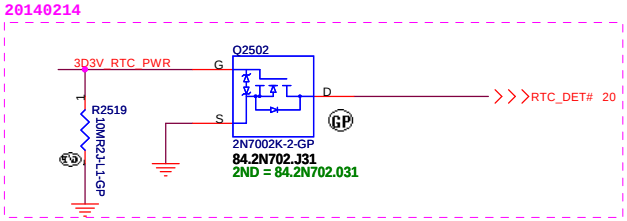
Notes:
1. SPI_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively damping the undershoot and overshoot.
3. All TPM branches/connections (TPM_MOSI, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as NC if SPI TPM is not implemented.



SSID = RBAT







HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC

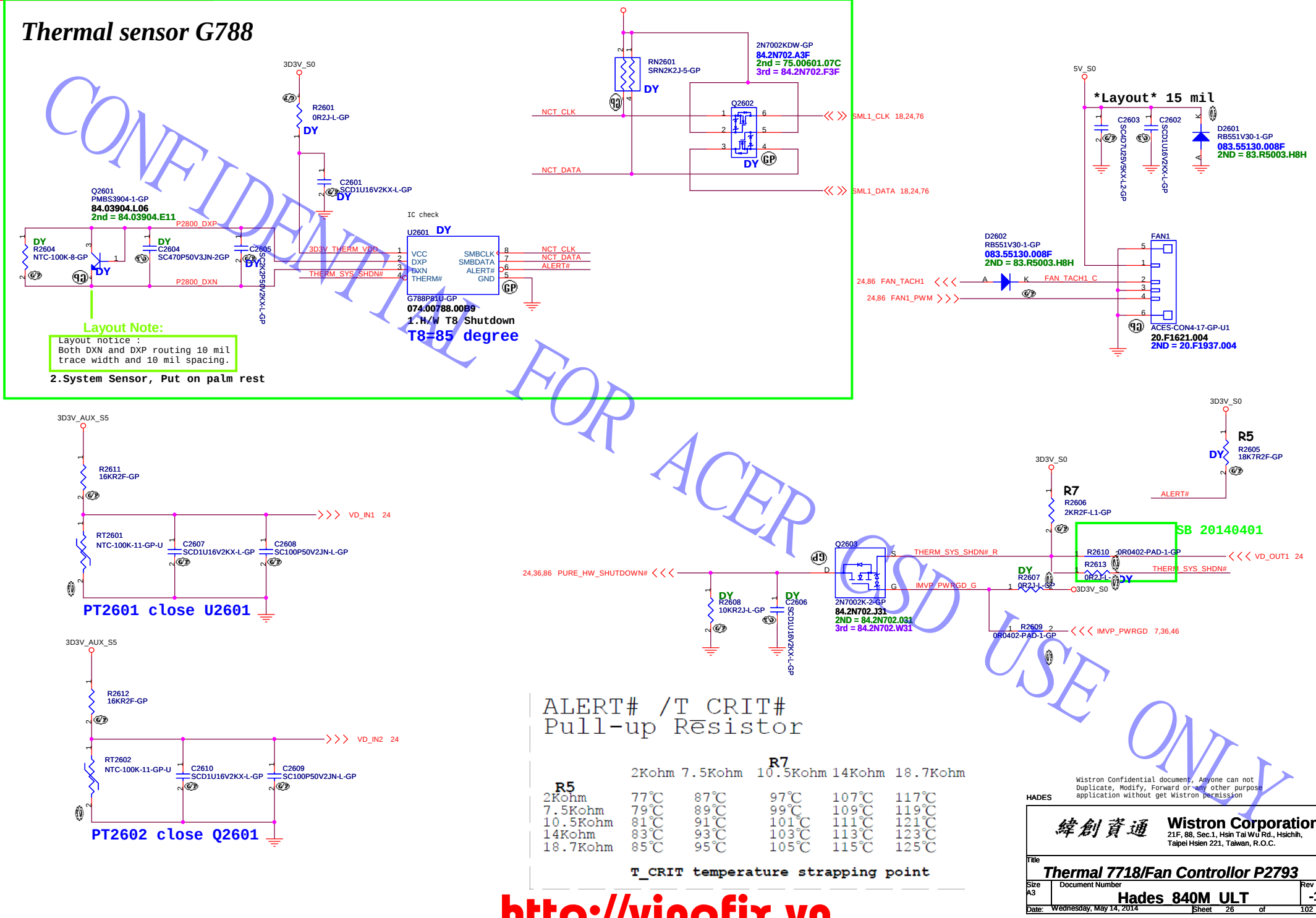
Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 25 of 102

SSID = Thermal

SB 20140401

Thermal sensor G788



ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

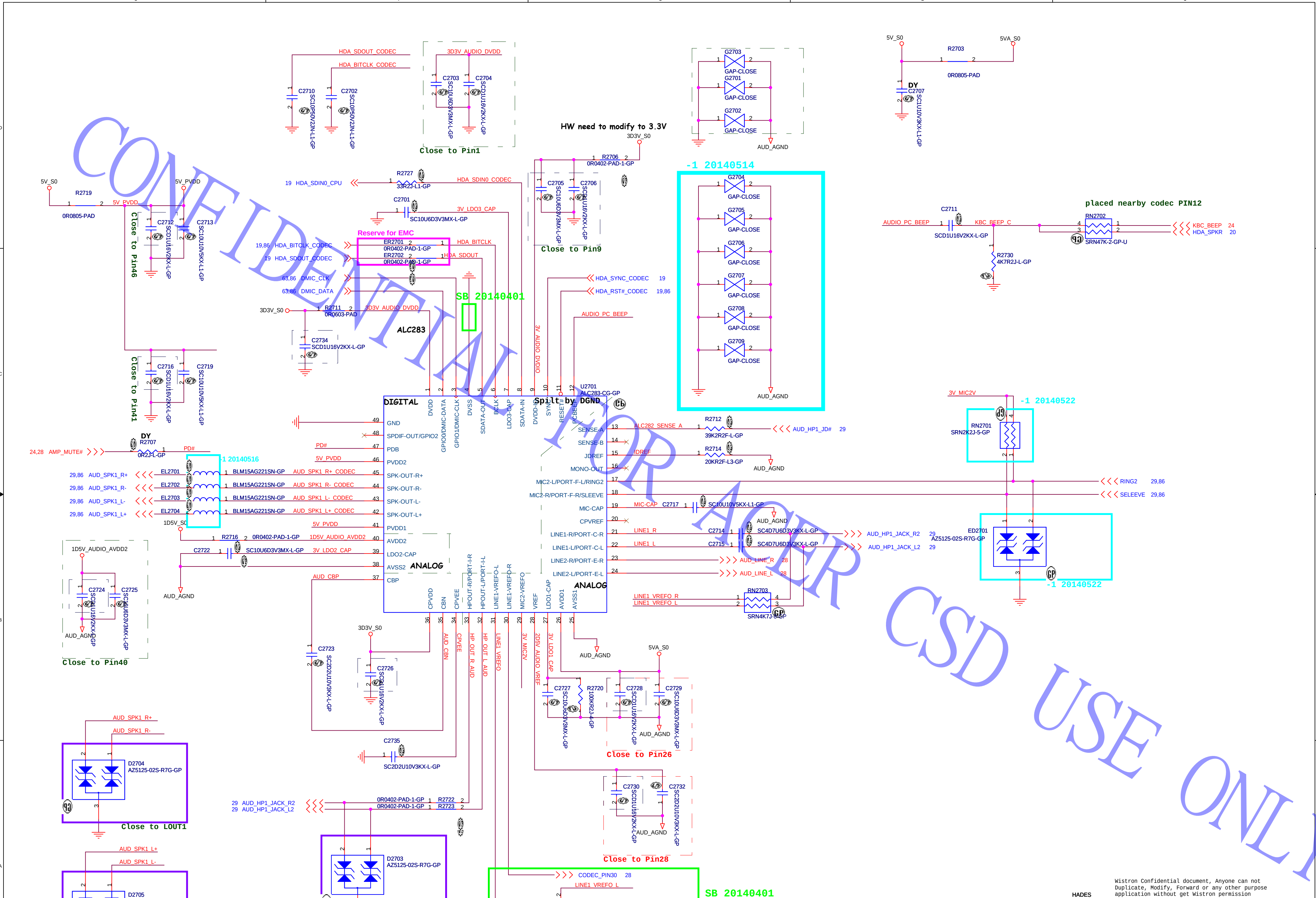
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, May 14, 2014 | Sheet 26 of 102

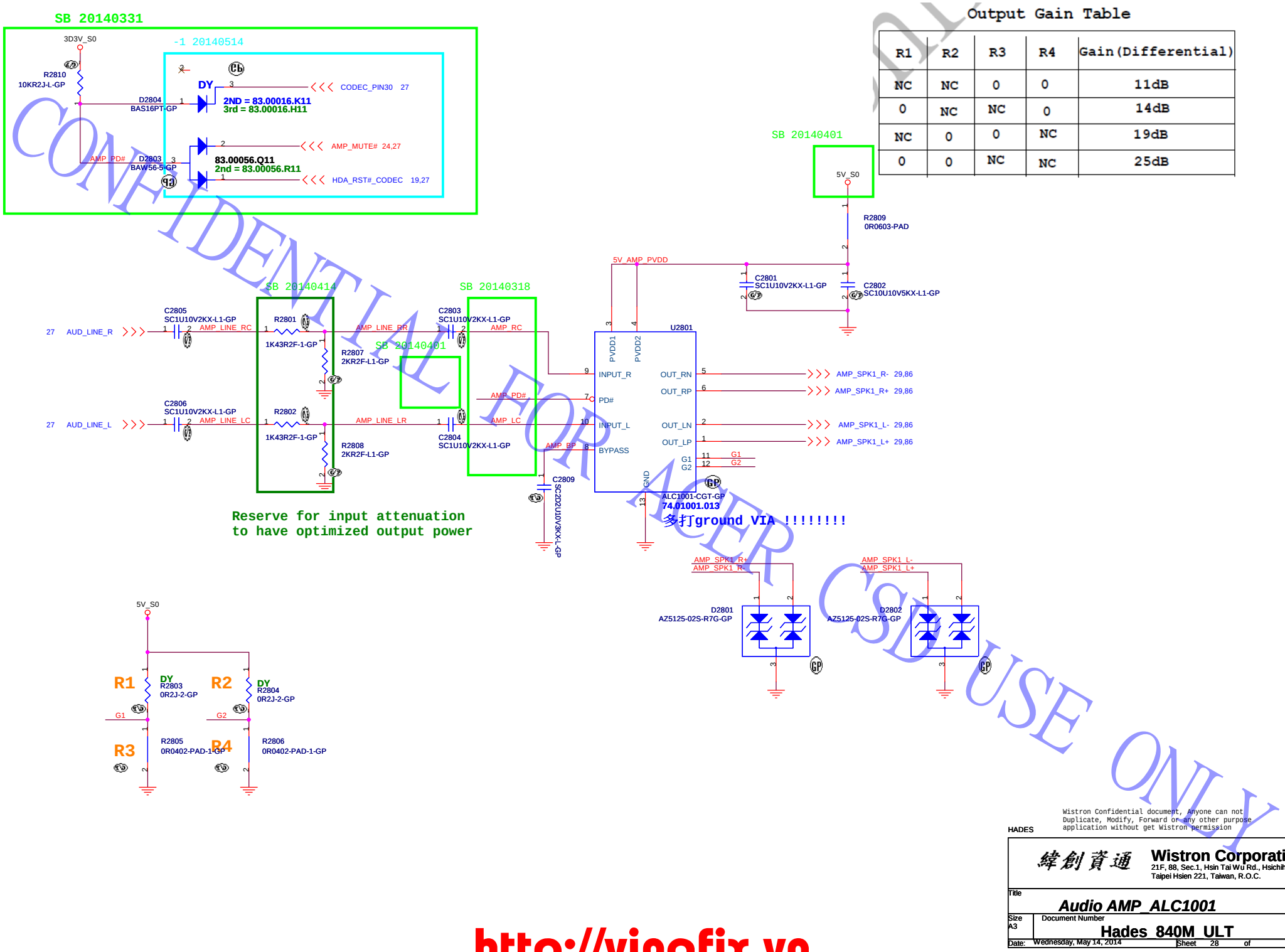


Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission

HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Codec_ALC283	
Size C	Document Number: Hades_840M_ULT	Rev -1
Date: Thursday, May 22, 2014	Sheet 27 of 102	



Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

Reserve for input attenuation
to have optimized output power

HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio AMP_ALC1001

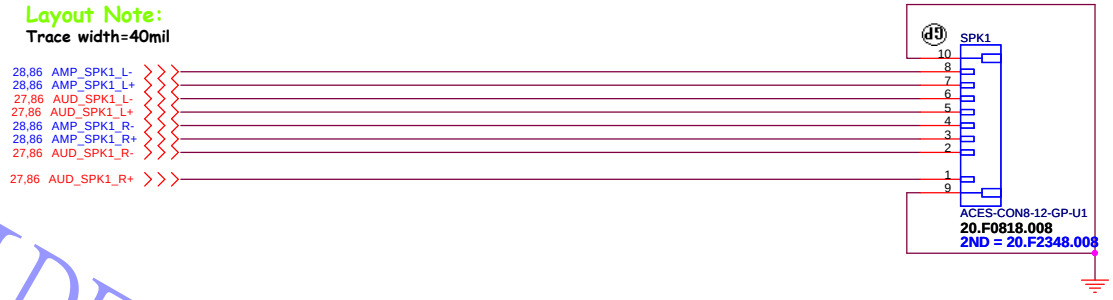
Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, May 14, 2014 | Sheet 28 of 102

SSID = AUDIO

Speaker

Layout Note:
Trace width=40mil

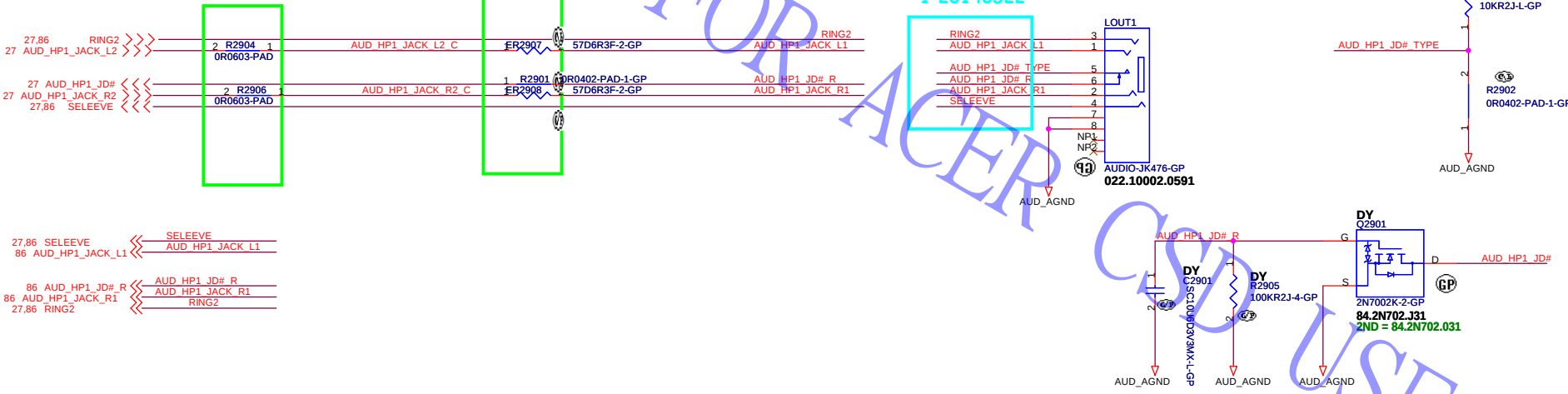


Combo Jack

SB 20140410

SB 20140410

-1 20140522



HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

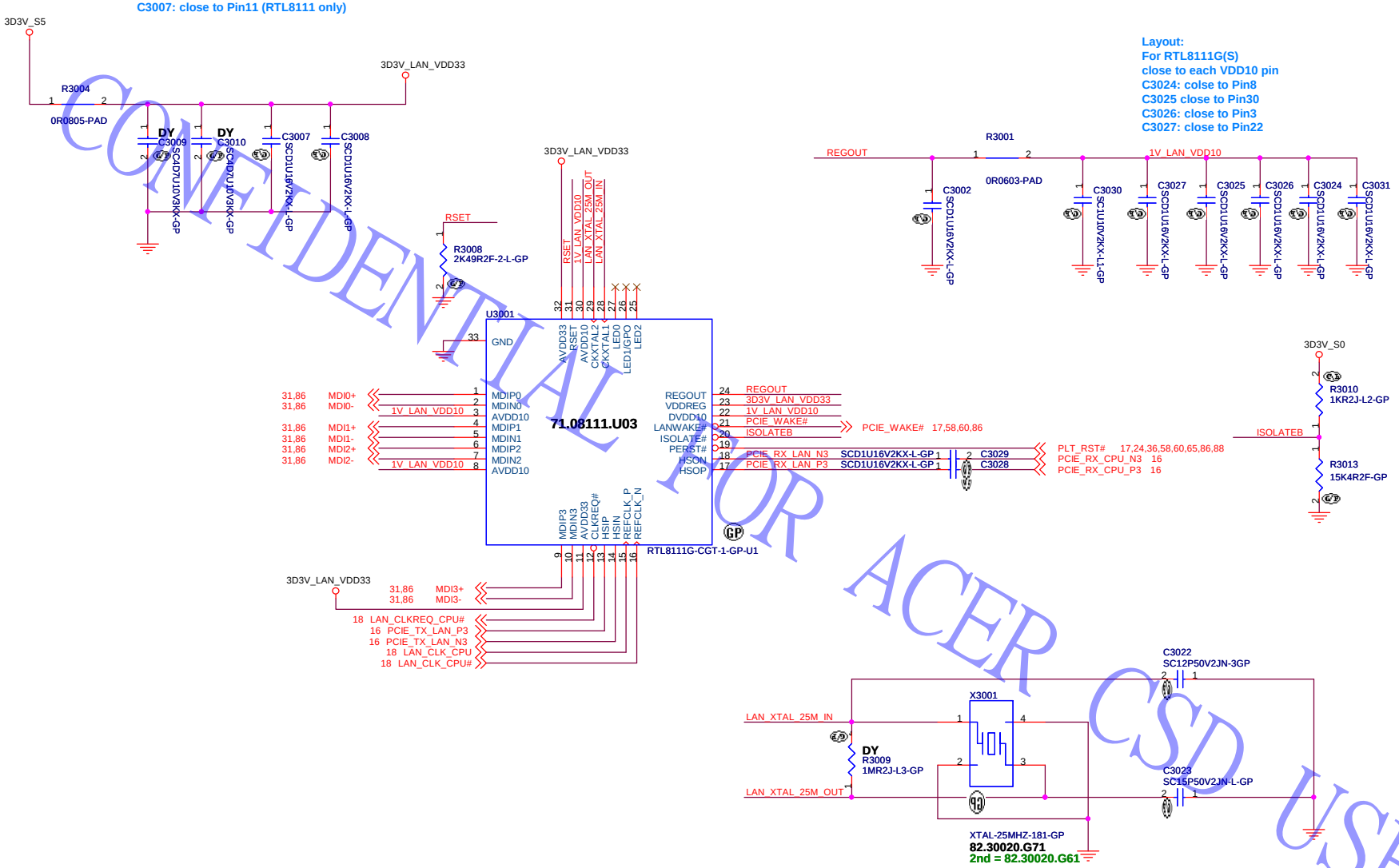
Size: Custom | Document Number: Hades 840M ULT | Rev: -1

Date: Thursday, May 22, 2014 | Sheet 29 of 102

40 mils

C3008: close to Pin32
C3007: close to Pin11 (RTL8111 only)

Layout:
For RTL8111G(S)
close to each VDD10 pin
C3024: colse to Pin8
C3025 close to Pin30
C3026: close to Pin3
C3027: close to Pin22



HADES

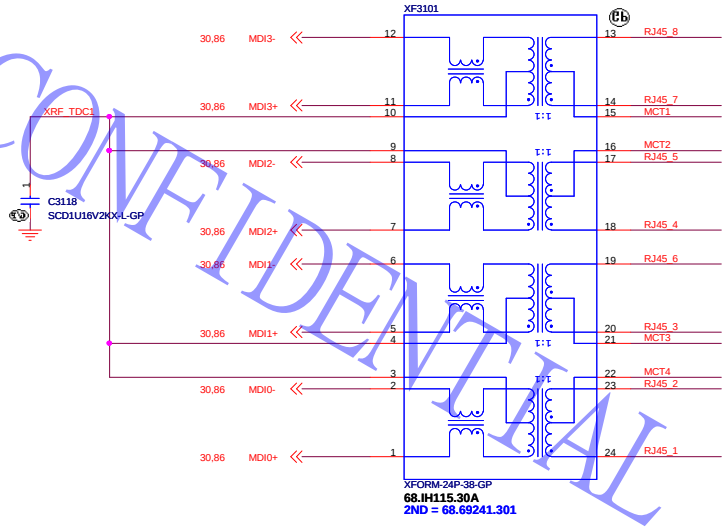
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

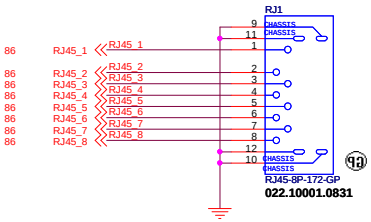
Title: LAN (RTL8111G(S))

Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

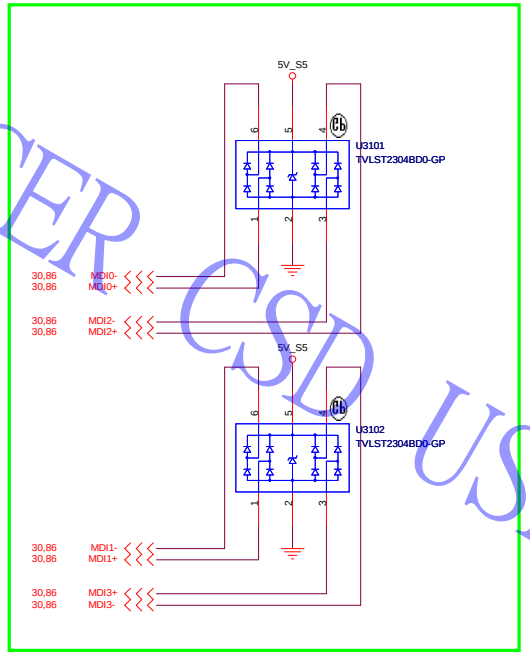
Date: Wednesday, April 30, 2014 | Sheet 30 of 102

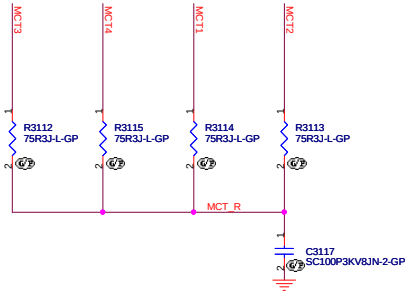
SSID = LAN





SB 20140328 FOR POE ISSUE





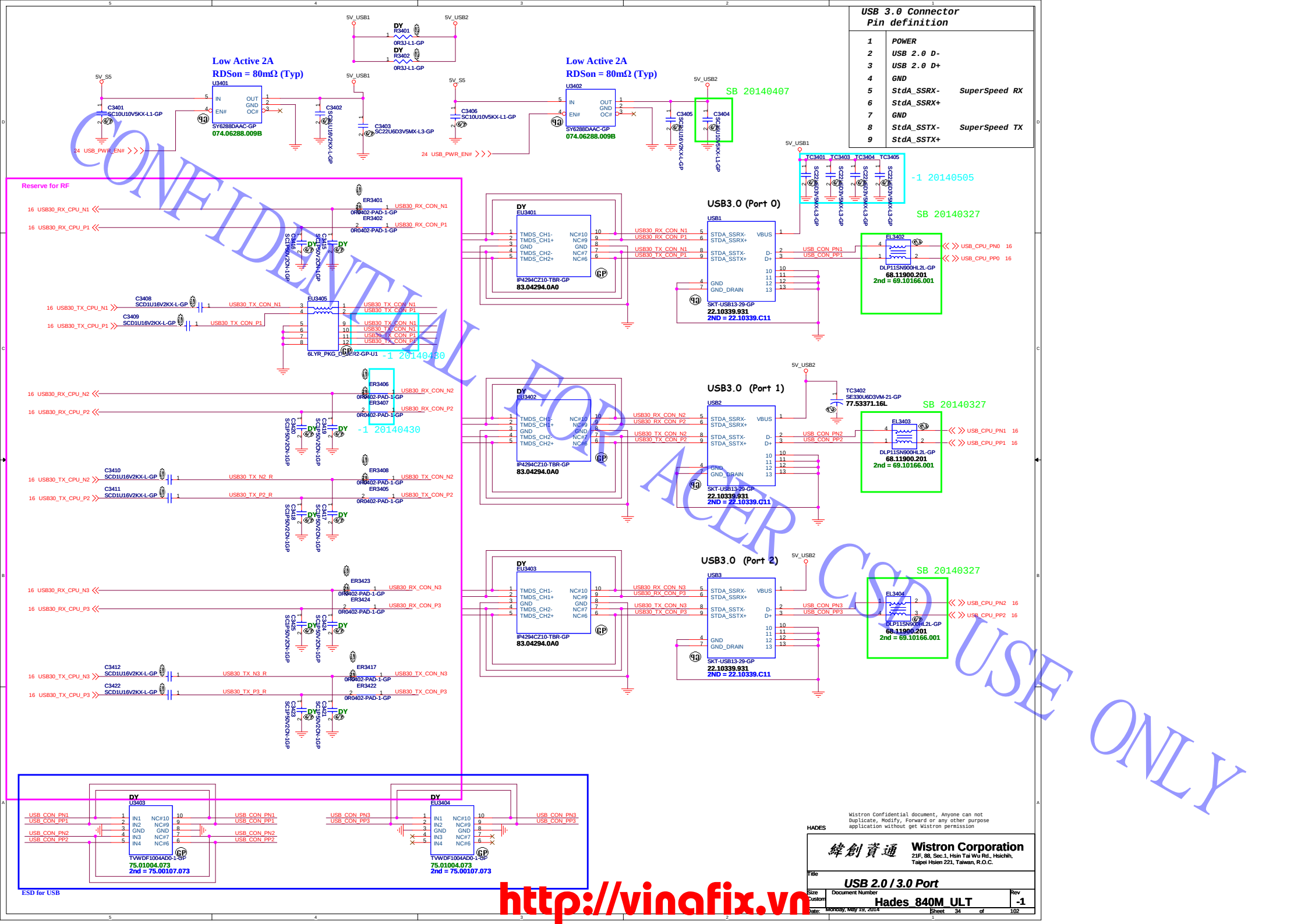
HADES

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

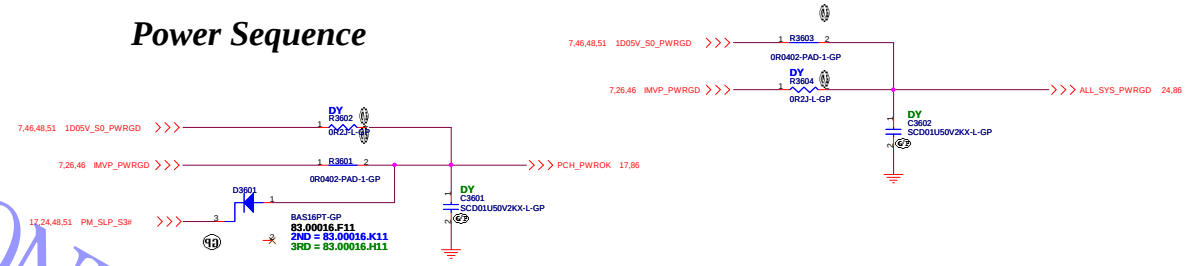
Title: (LAN+VGA) CONNECTOR

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

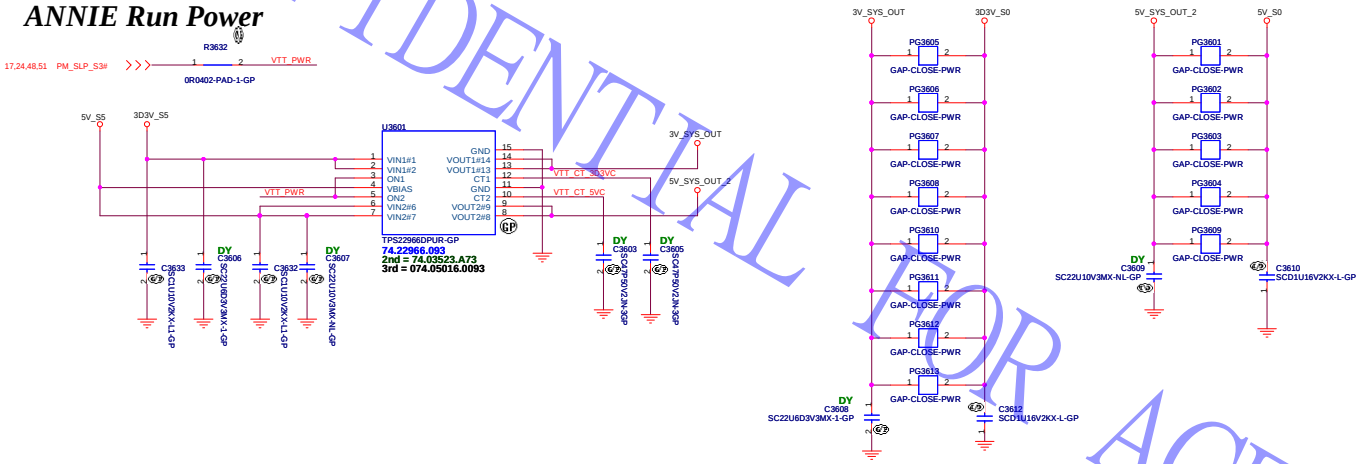
Date: Wednesday, April 30, 2014 | Sheet 31 of 102


USB 3.0 Connector Pin definition
1 POWER
2 USB 2.0 D-
3 USB 2.0 D+
4 GND
5 StdA_SSRX- SuperSpeed RX
6 StdA_SSRX+
7 GND
8 StdA_SSTX- SuperSpeed TX
9 StdA_SSTX+
Low Active 2A
RDSon = 80mΩ (Typ)
SY6288DAAC-GP
074.06288.009B
SB 20140407
Reserve for RF
USB3.0 (Port 0)
USB3.0 (Port 1)
USB3.0 (Port 2)
SB 20140327
-1 20140505
-1 20140430
SKT-USB13-29-GP
22.10339.931
2ND = 22.10339.C11
DLP11SN900HL2L-GP
68.11900.201
2nd = 69.10166.001
IP4294CZ10-TBR-GP
83.04294.0A0
TVWDF1004AD0-1-GP
75.01004.073
2nd = 75.00107.073
ESD for USB
CONFIDENTIAL FOR ACER CSD USE ONLY
Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission
HADES
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
USB 2.0 / 3.0 Port
Hades_840M_ULT
-1
Monday, May 19, 2014
Sheet 34 of 102
http://vinafix.vn

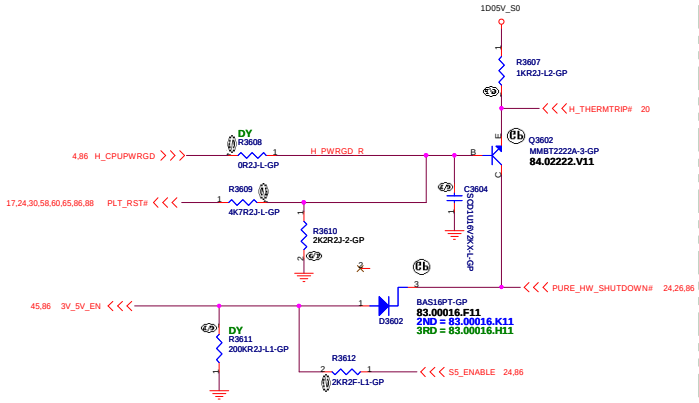
Power Sequence

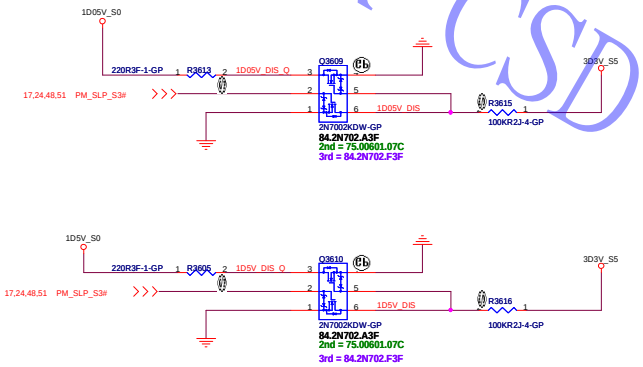


ANNIE Run Power



Discharge circuit





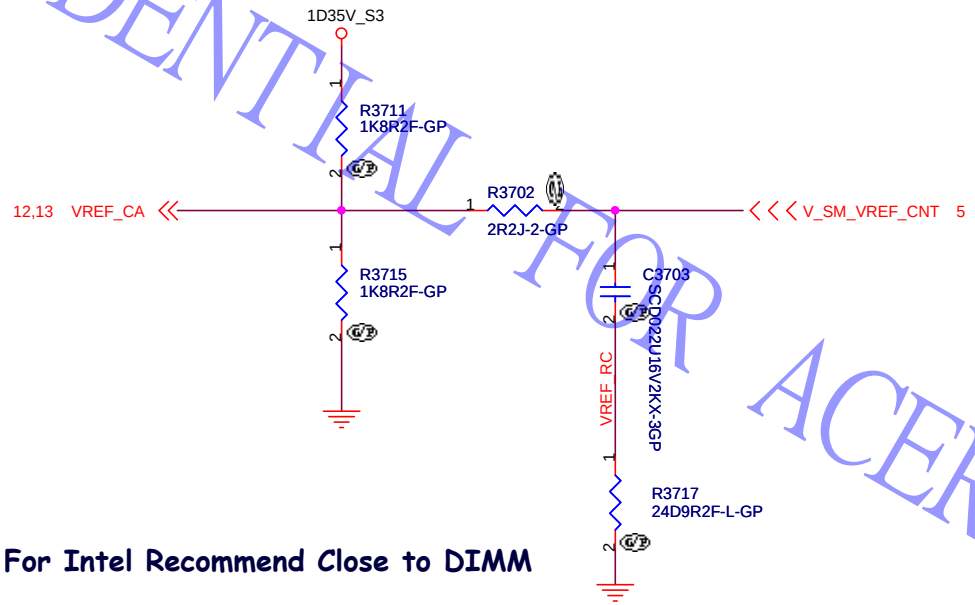
HADES

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, May 14, 2014 | Sheet 36 of 102



For Intel Recommend Close to DIMM

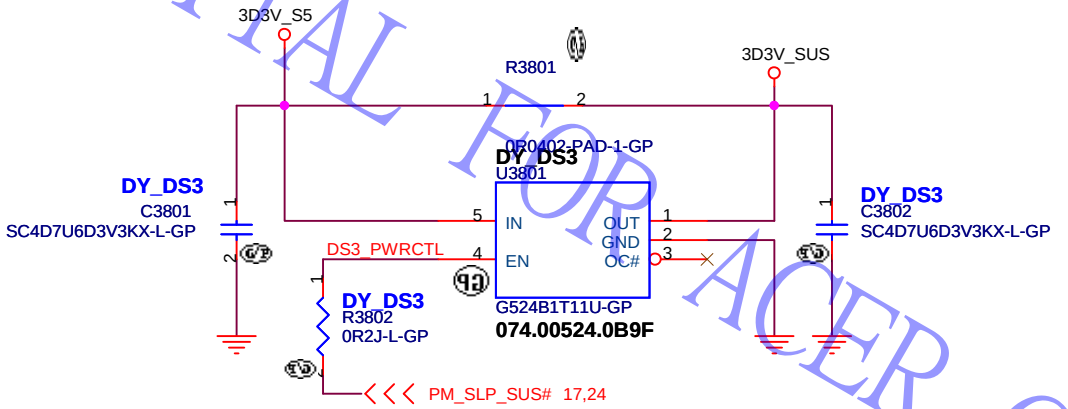
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER OCP / S3 reduction

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, October 30, 2013 | Sheet 37 of 102



HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

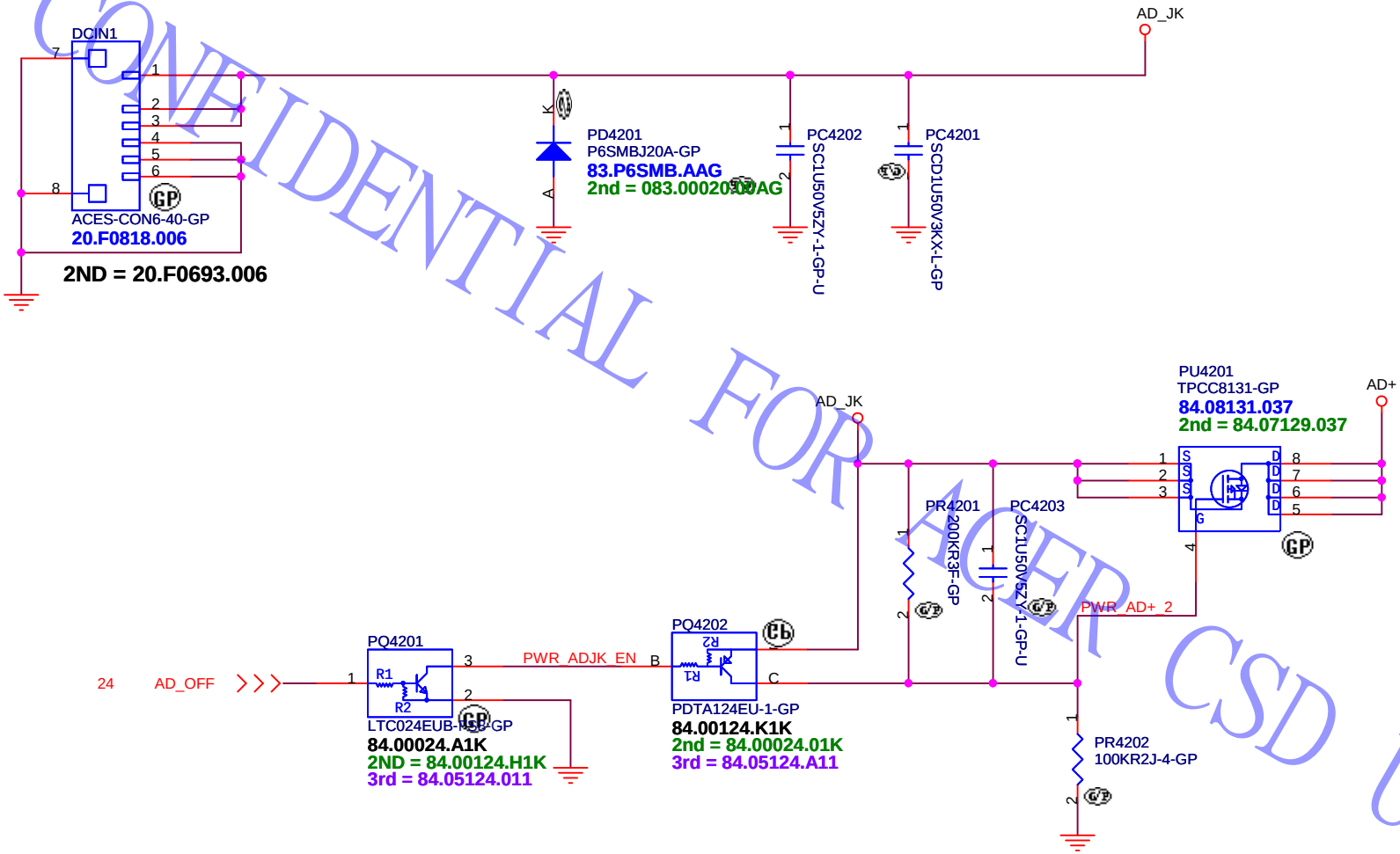
Title: ***DS3***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 38 of 102

ANNIE solution

Adaptor in to generate DCBATOUT



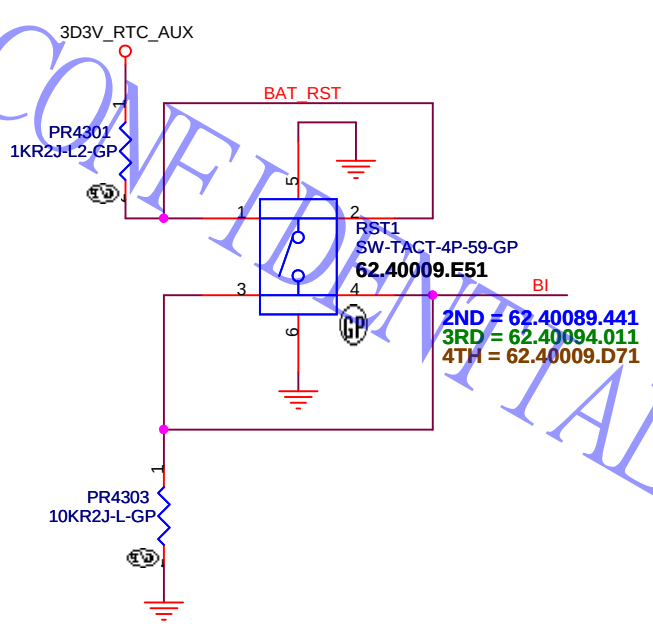
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A4	Hades_840M_ULT	-1
Date: Friday, May 16, 2014	Sheet 42 of 102	

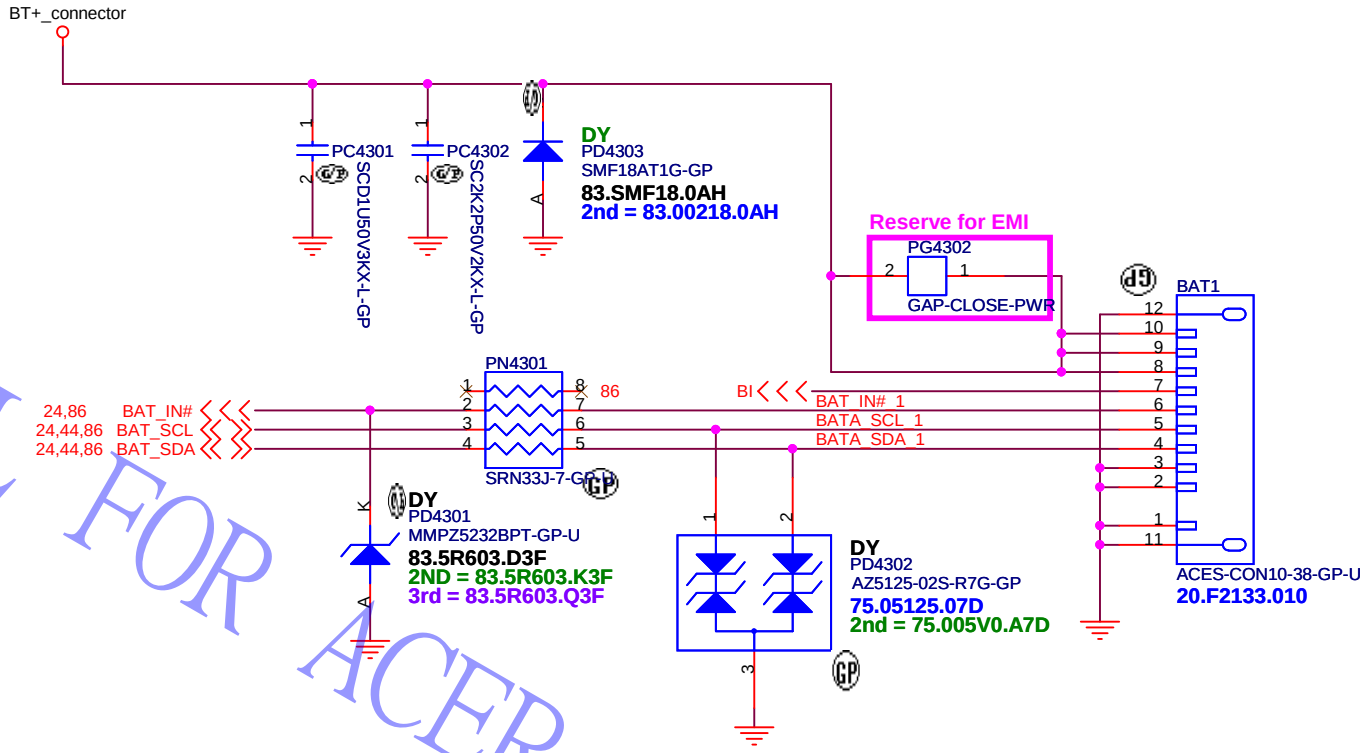
Battery Reset



SB 20140401

Battery Insert

Battery Connector



HADES

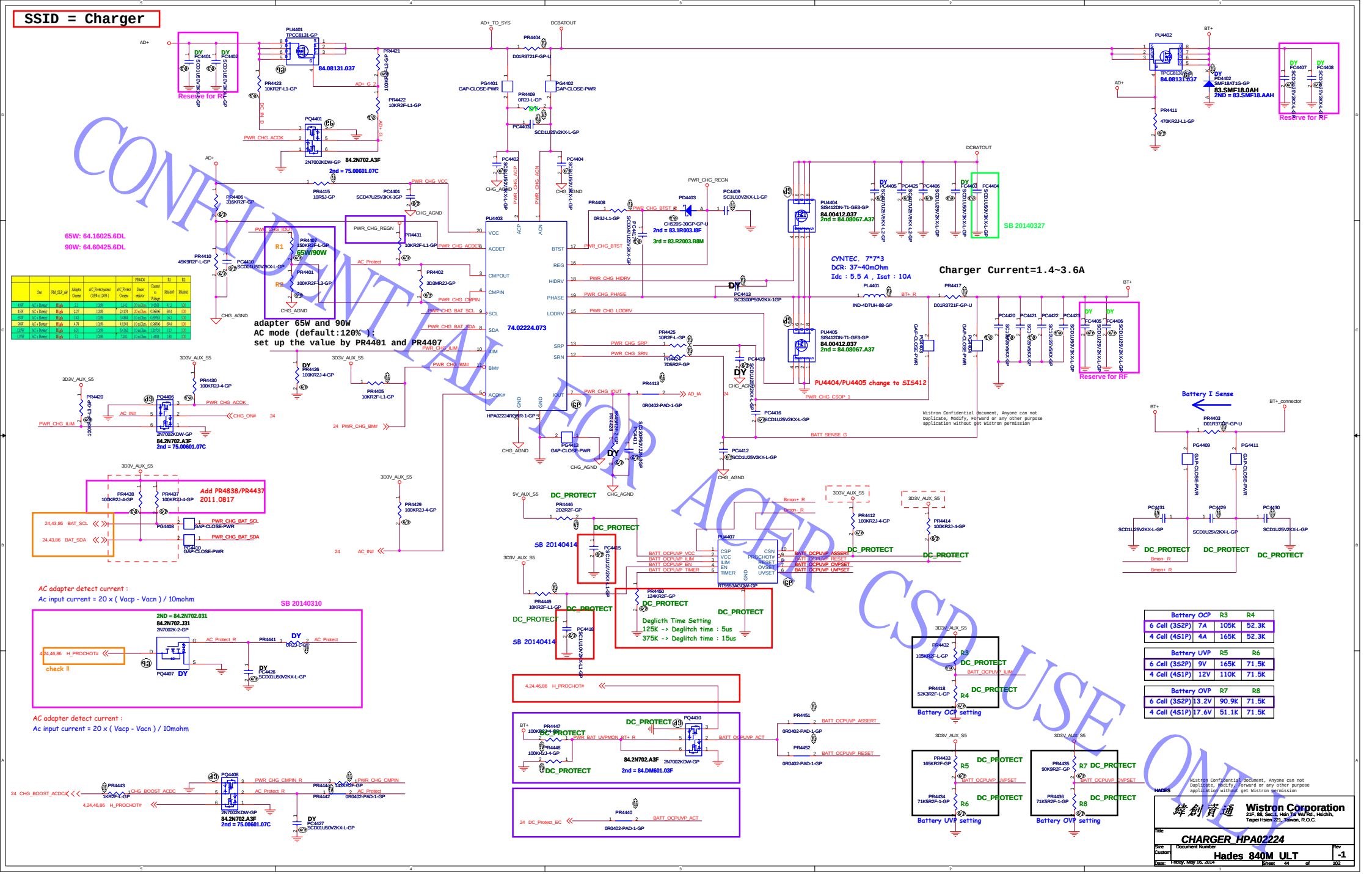
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 43 of 102

SSID = Charger

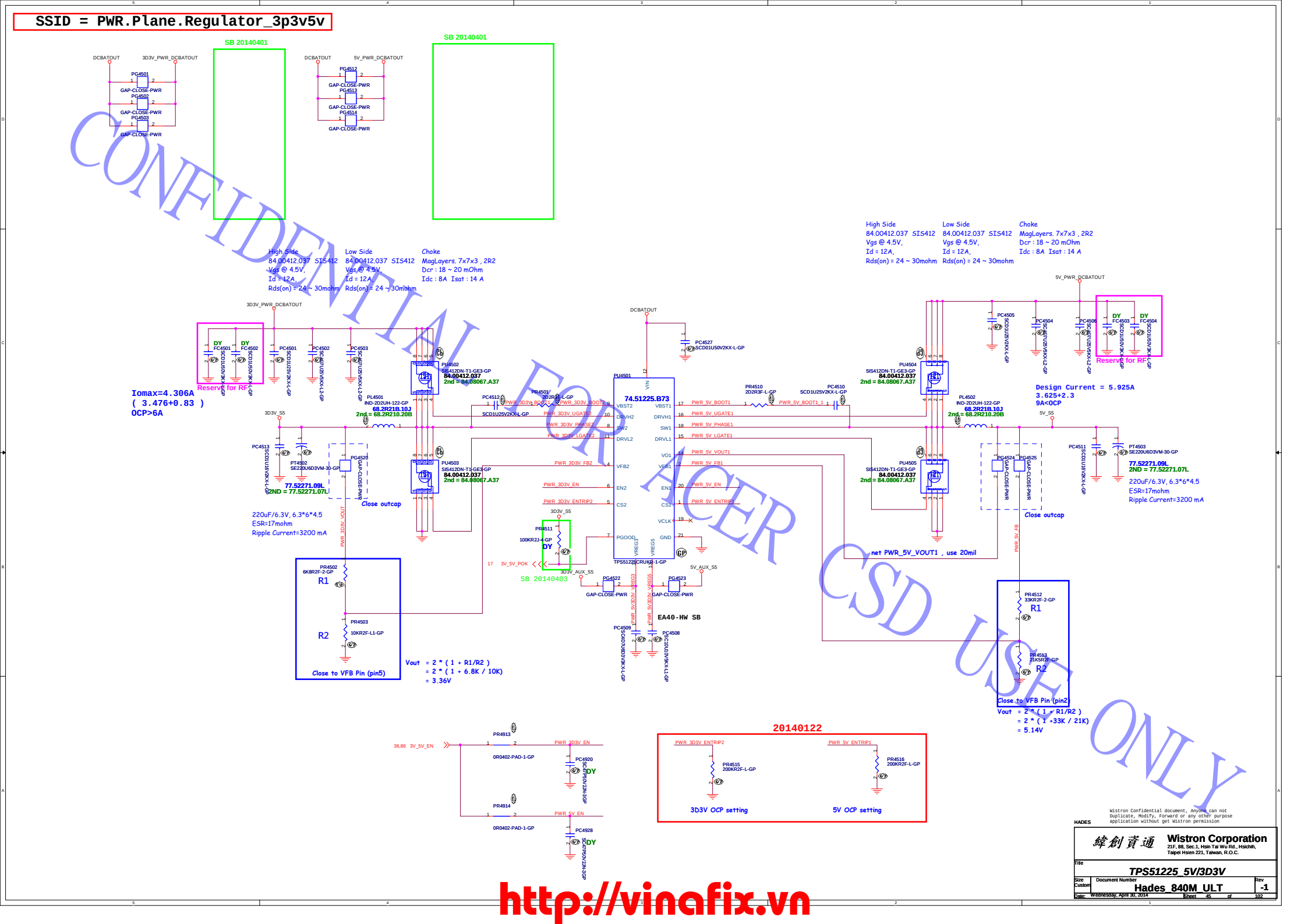


Battery OCP	R3	R4
6 Cell (3S2P)	7A	105K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP	R7	R8
6 Cell (3S2P)	13.2V	90.9K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

SSID = PWR.Plane.Regulator_3p3v5v



HADES

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

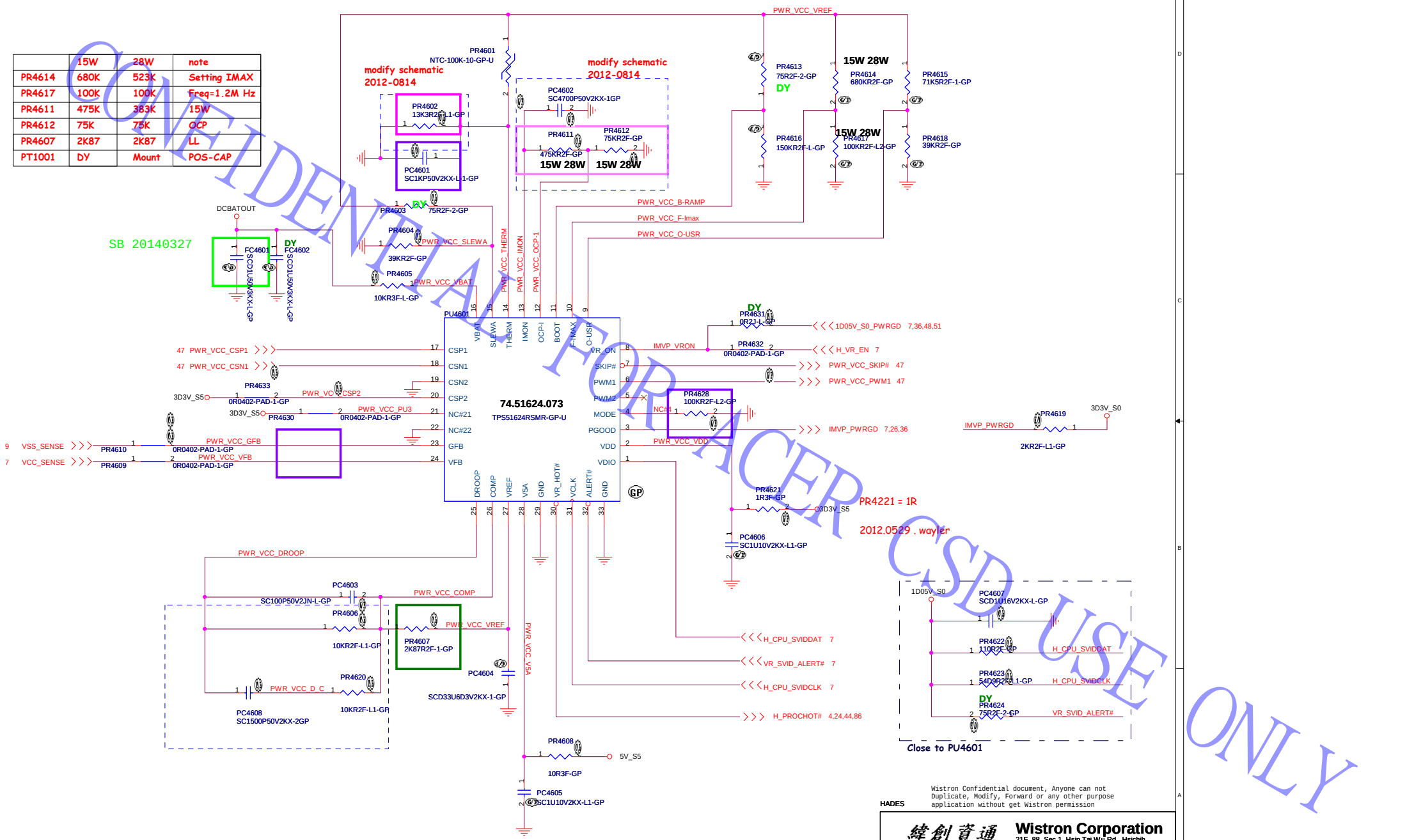
Title: TPS51225_5V/3D3V

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 45 of 102

SSID = CPU.Regulator

	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCP
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP



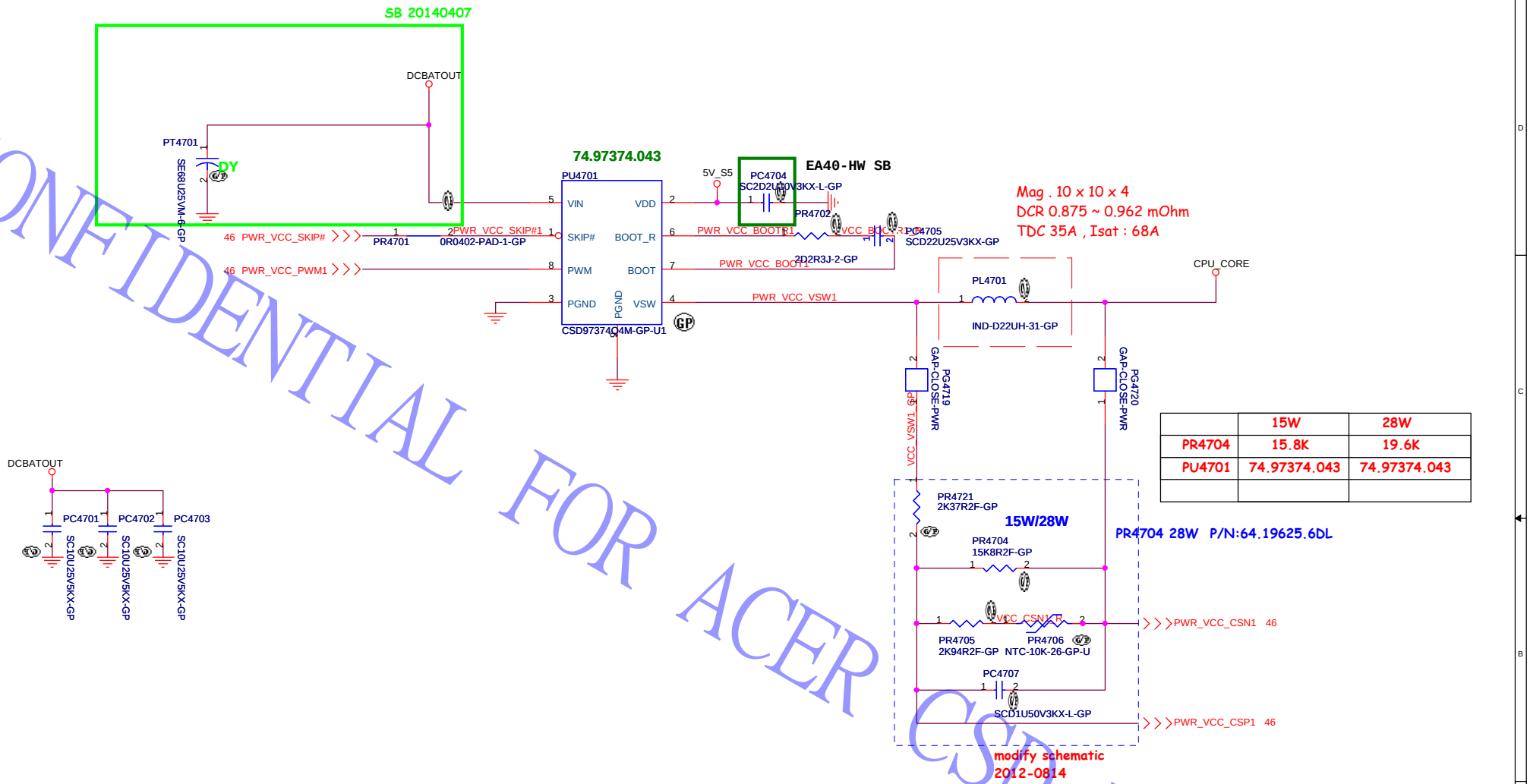
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51624_CPUCORE(1/2)

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Thursday, May 15, 2014 | Sheet 46 of 102



	15W	28W
PR4704	15.8K	19.6K
PU4701	74.97374.043	74.97374.043

HADES

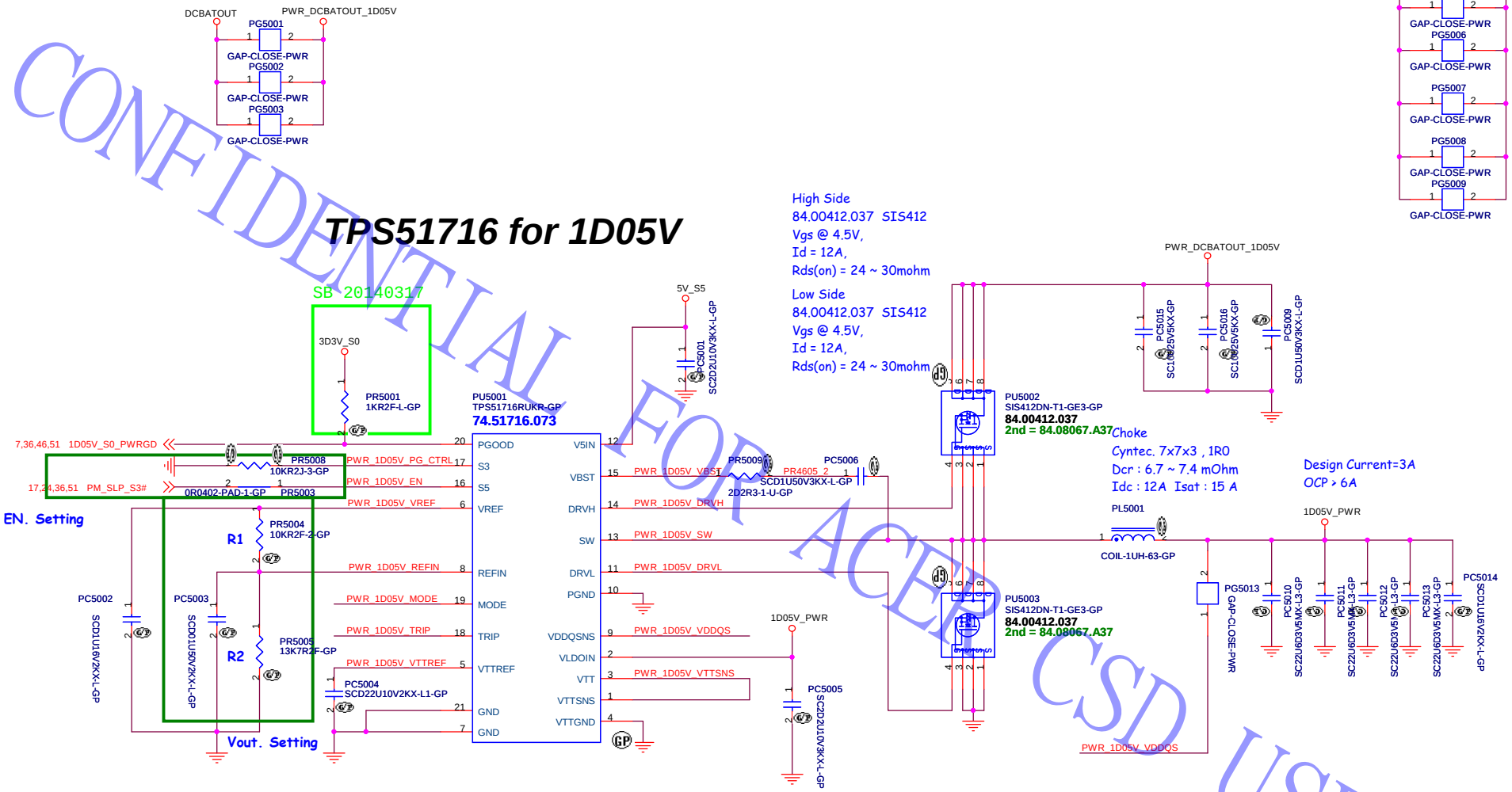
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51624_CPUCORE(2/2)

Size: B | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 47 of 102

TPS51716 for 1D05V



MODE

PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

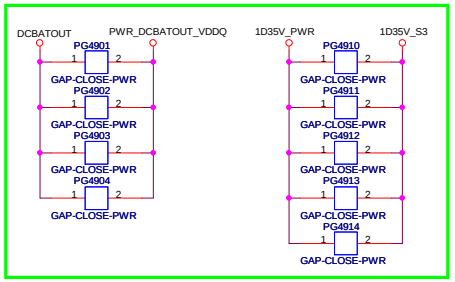
Title: DC to DC_1D05V(SY8208D)

Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Friday, May 16, 2014 | Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p2v0p6v

RT8231 for VDDQ



SB 20140328

OCP setting

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Choke
Cyntec. 7x7x3 , 1R0
Dcr : 6.7 ~ 7.4 mOhm
Idc : 12A Isat : 15 A

IccMAX = 4.4A
OCP > 8A

Close to pin23

Close to pin23

SB 20140328

Iomax=1A
OCP>1.5A

PU4901 change to RT8207M

Close to output cap pin1, not inside of the output cap

Vout=0.675 x (1+R1/R2)
=0.675 x (1+20/20)
=1.35

Close to PIN9

EA40-HW 1

+0.675VS
Iomax: 1.2A

SB 20140328

HADES

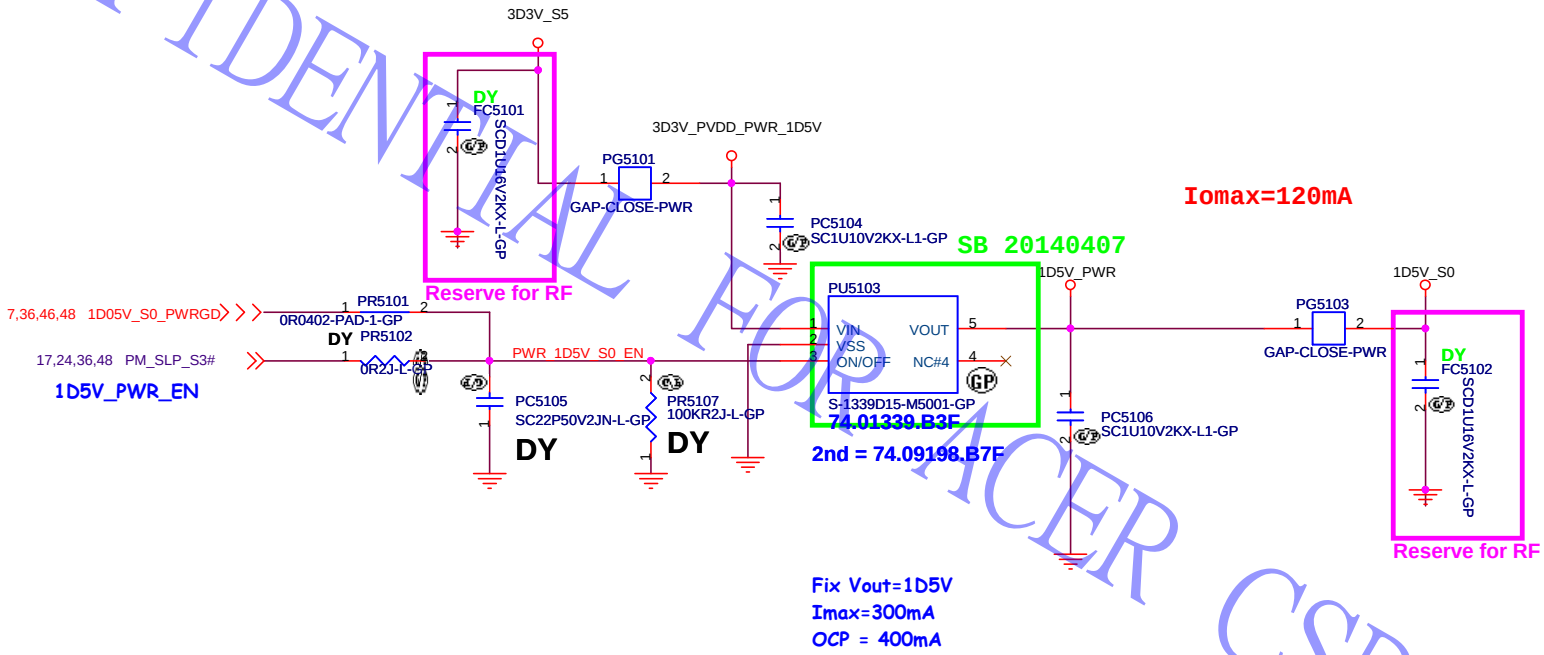
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231(VDDQ_VTT)

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 49 of 102

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



HADES

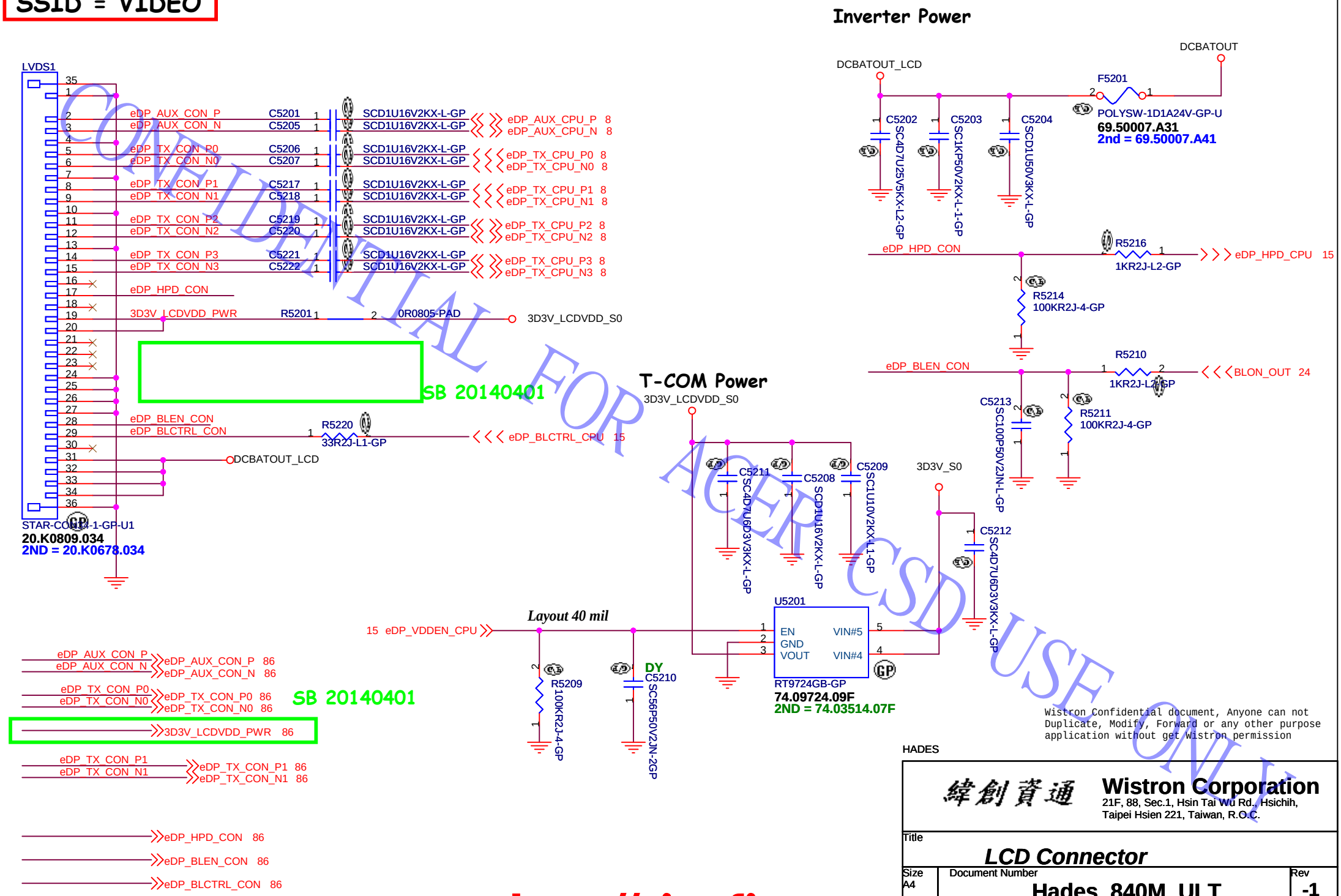
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D5V_S0 SYW232*

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Thursday, May 15, 2014 Sheet 51 of 102

SSID = VIDEO



HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

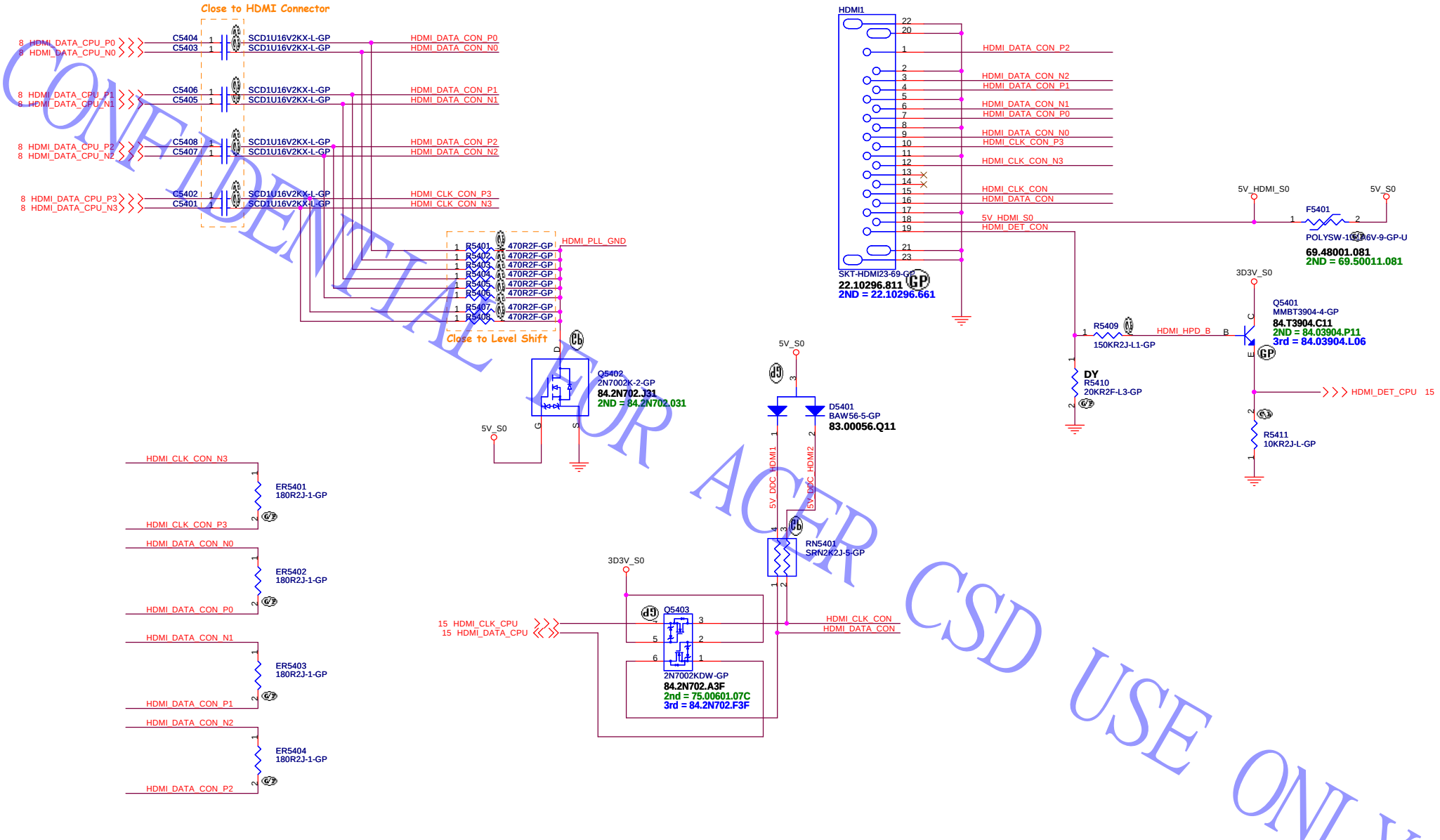
Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 52 of 102

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN



HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

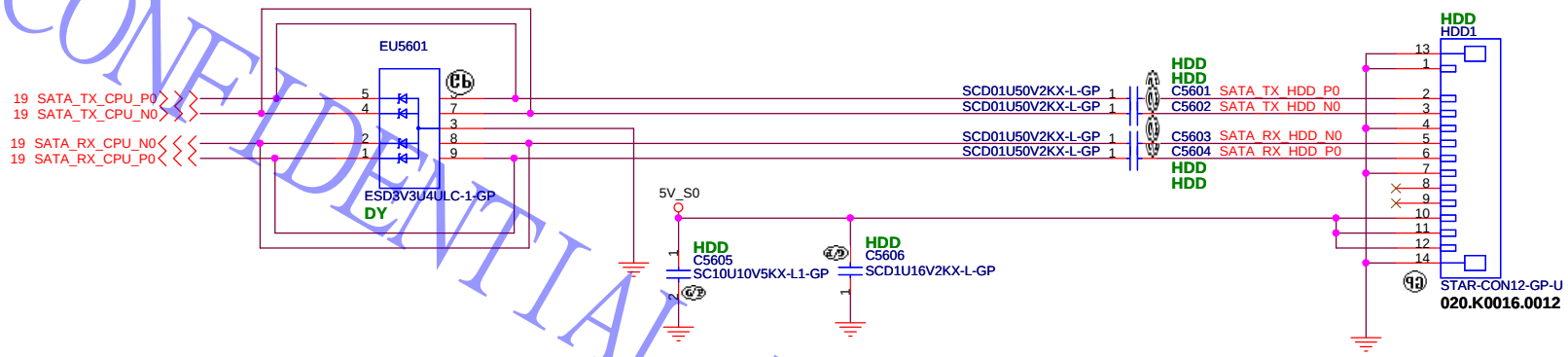
Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Hades_840M_ULT	-1

Date: Friday, May 09, 2014 Sheet 54 of 102

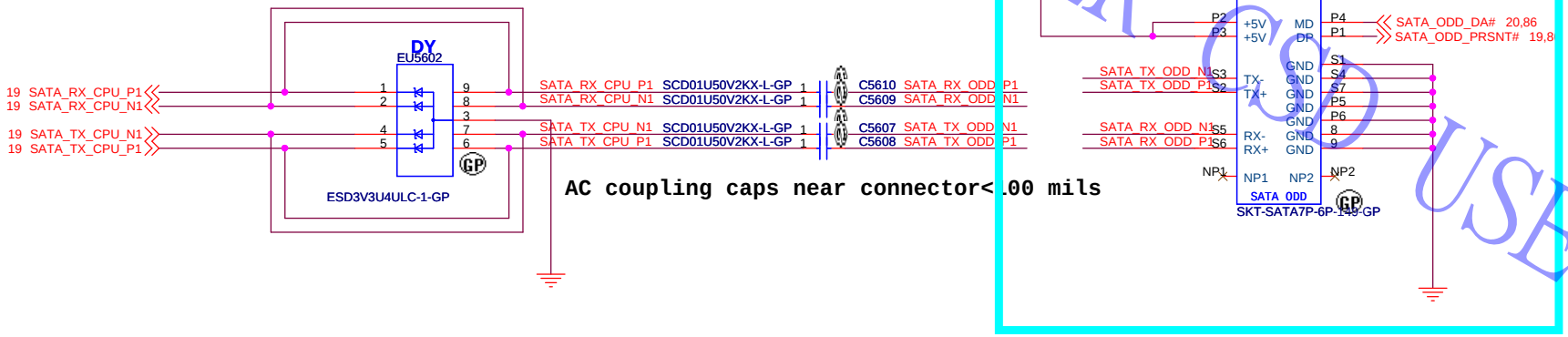
SSID = SATA

SATA HDD Connector

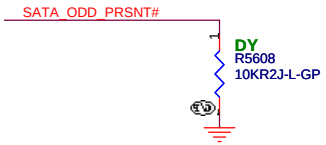


AC coupling caps near connector<100 mils

SATA ODD Connector



AC coupling caps near connector<100 mils



-1 20140516

HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

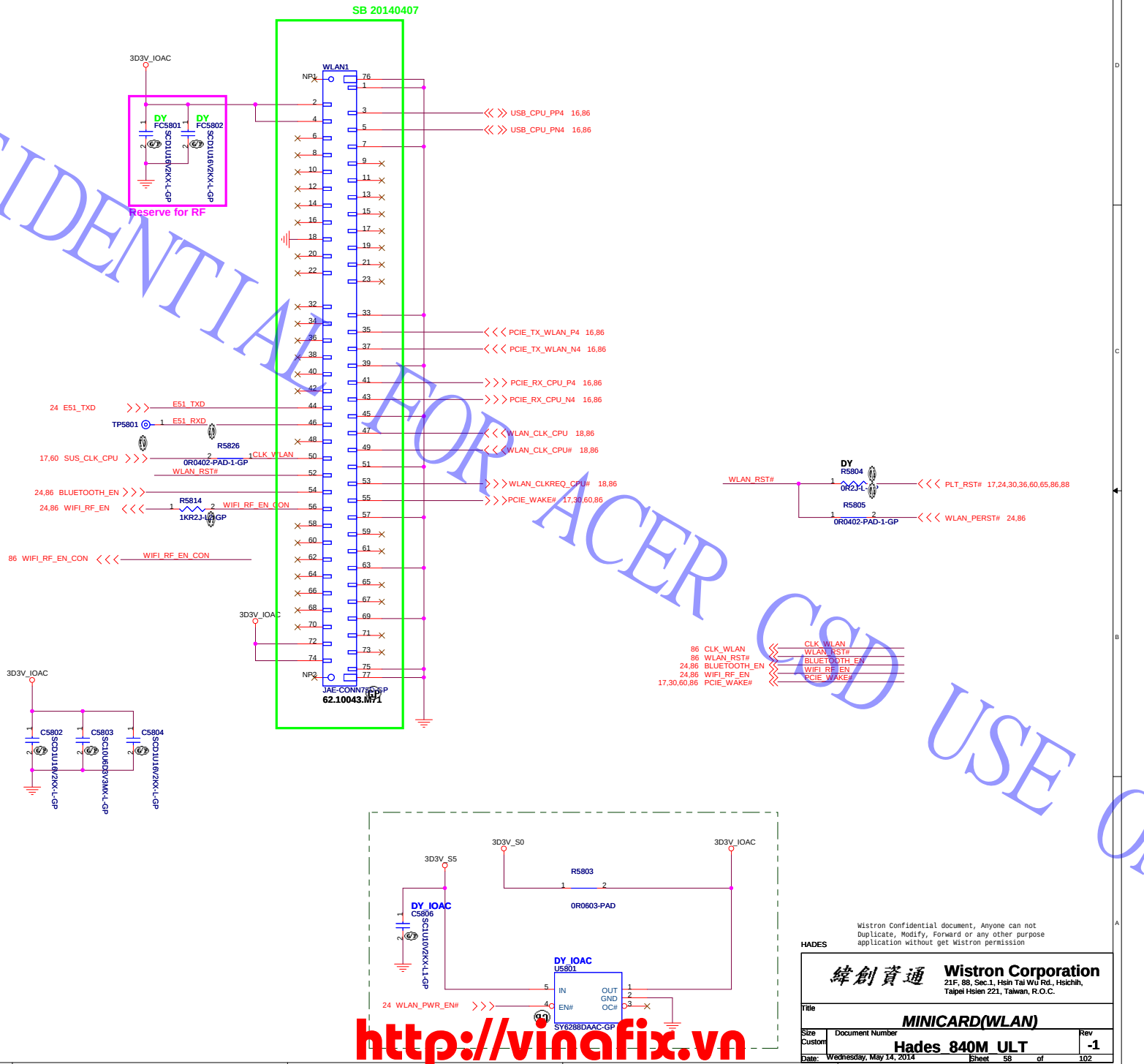
Title: ***HDD / ODD***

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Friday, January 10, 2014 Sheet 56 of 102

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

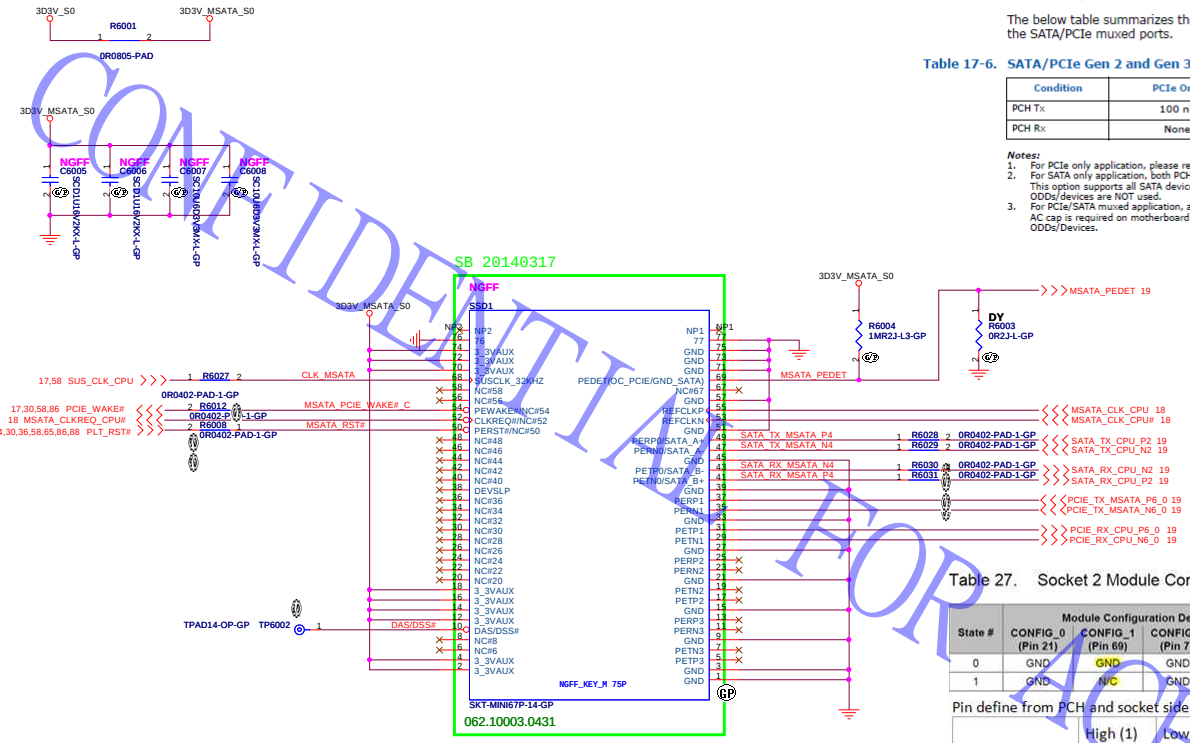
Title: MINICARD(WLAN)

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Wednesday, May 14, 2014 Sheet 58 of 102

SSID = m-SATA

Mini Card Connector (NGFF m-SATA)



17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

Notes:
1. For PCIe only application, please refer to the PCIe guidelines for details.
2. For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
3. For PCIe/SATA muxed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

HADES

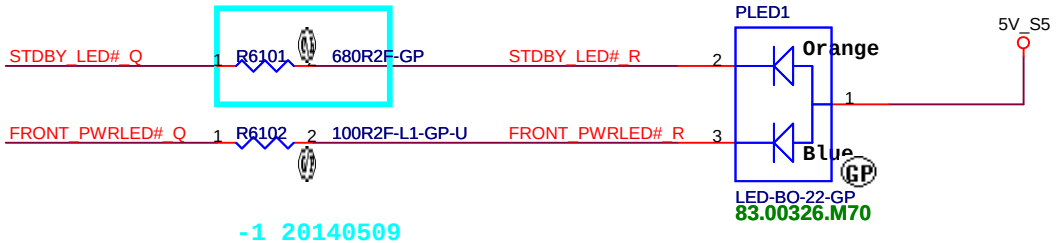
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: m-SATA Connector

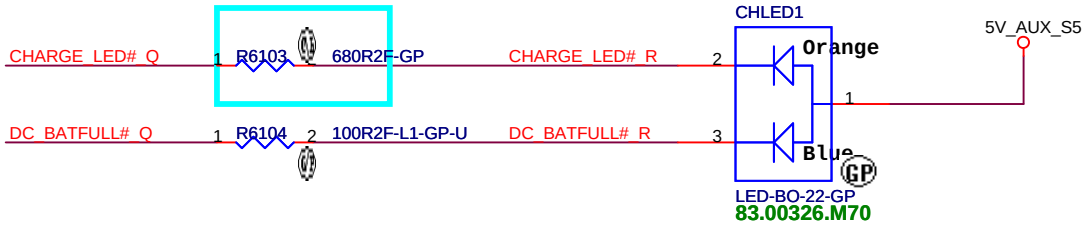
Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Wednesday, [illegible] Sheet 60 of 102

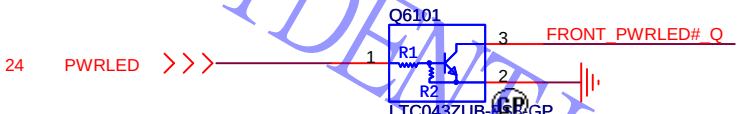
SSID = User.Interface



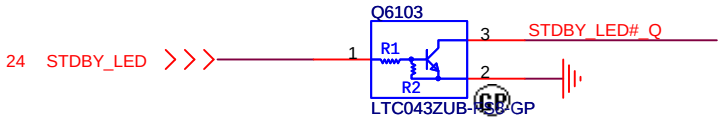
-1 20140509



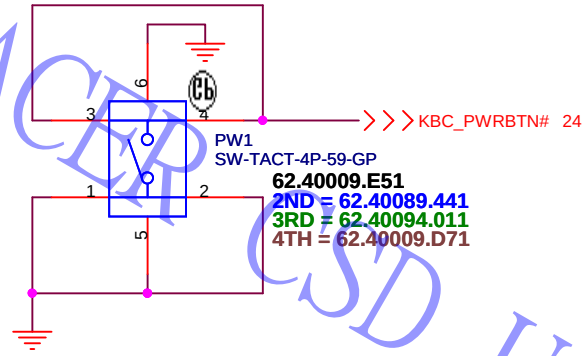
Power Button_LED



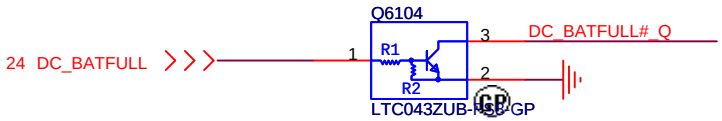
Power STDBY_LED



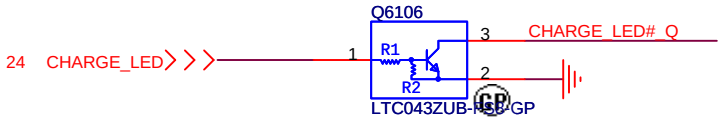
Power Button



Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

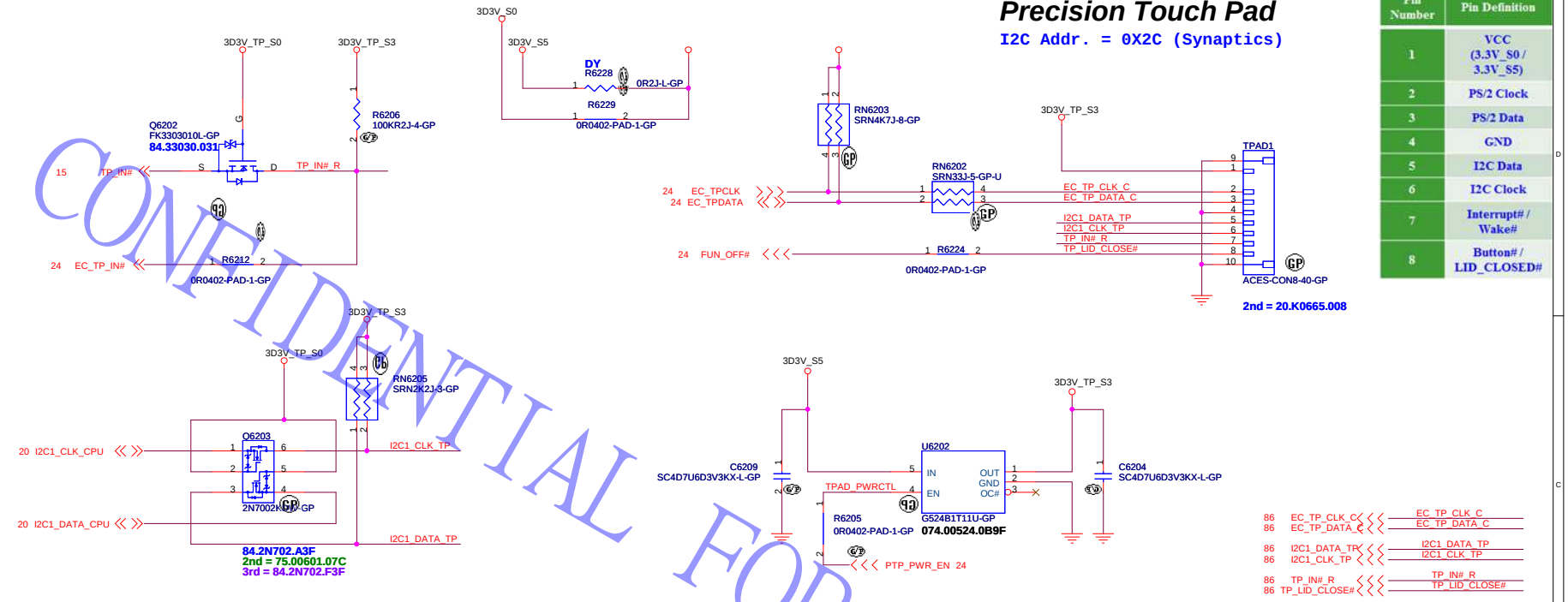
Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Friday, May 09, 2014 Sheet 61 of 102

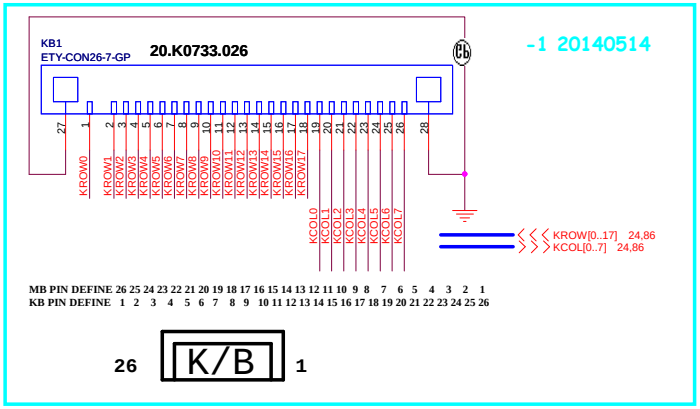
Precision Touch Pad

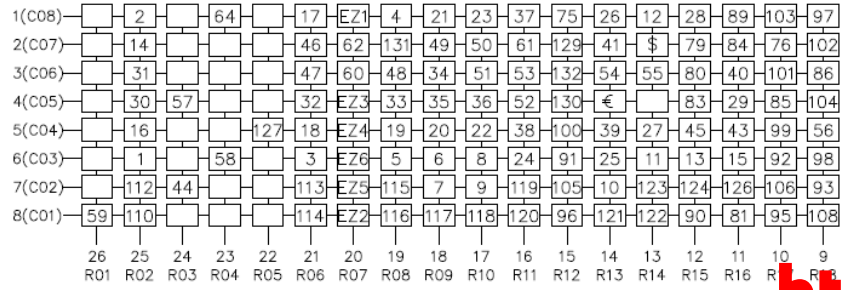
I2C Addr. = 0X2C (Synaptics)

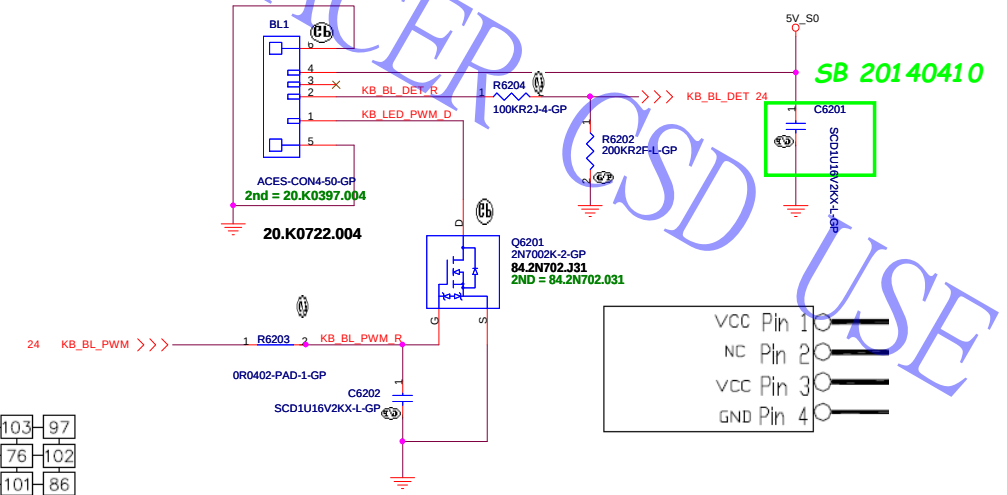
Pin Number	Pin Definition
1	VCC (3.3V_S0 / 3.3V_S5)
2	PS/2 Clock
3	PS/2 Data
4	GND
5	I2C Data
6	I2C Clock
7	Interrupt# / Wake#
8	Button# / LID_CLOSED#



Internal KeyBoard Connector







HADES

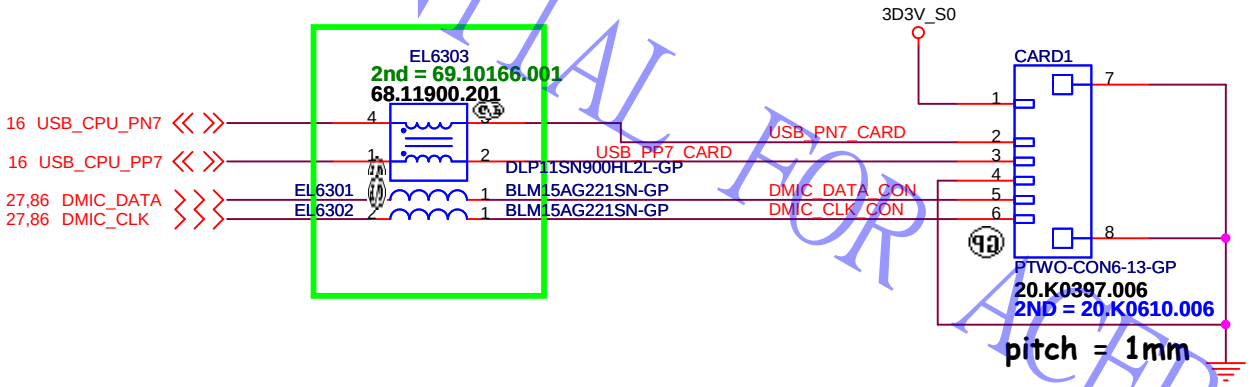
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

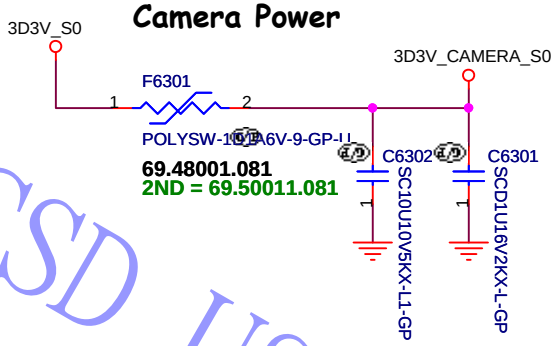
Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Friday, May 16, 2014 Sheet 62 of 102

SB 20140327

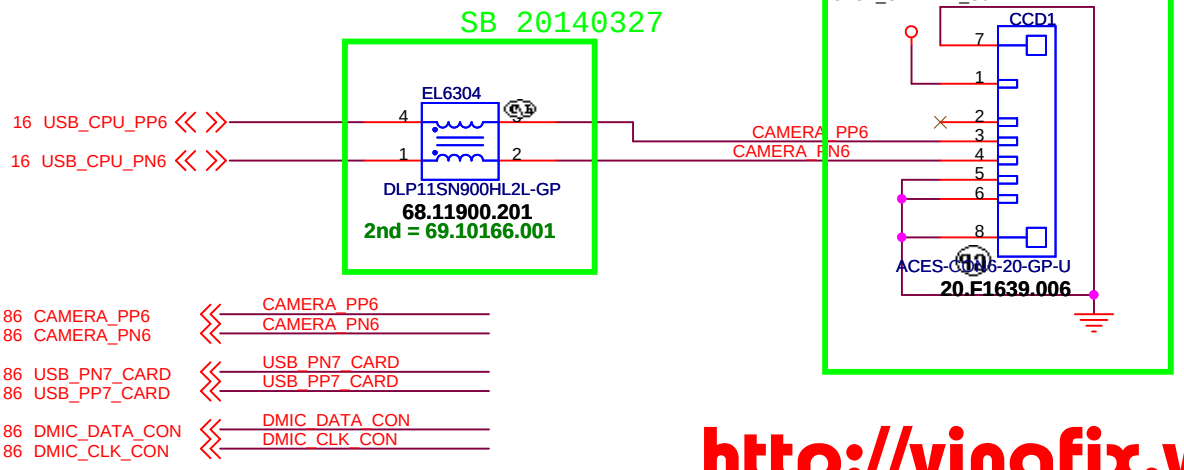


Camera Power



SB 20140328

SB 20140327



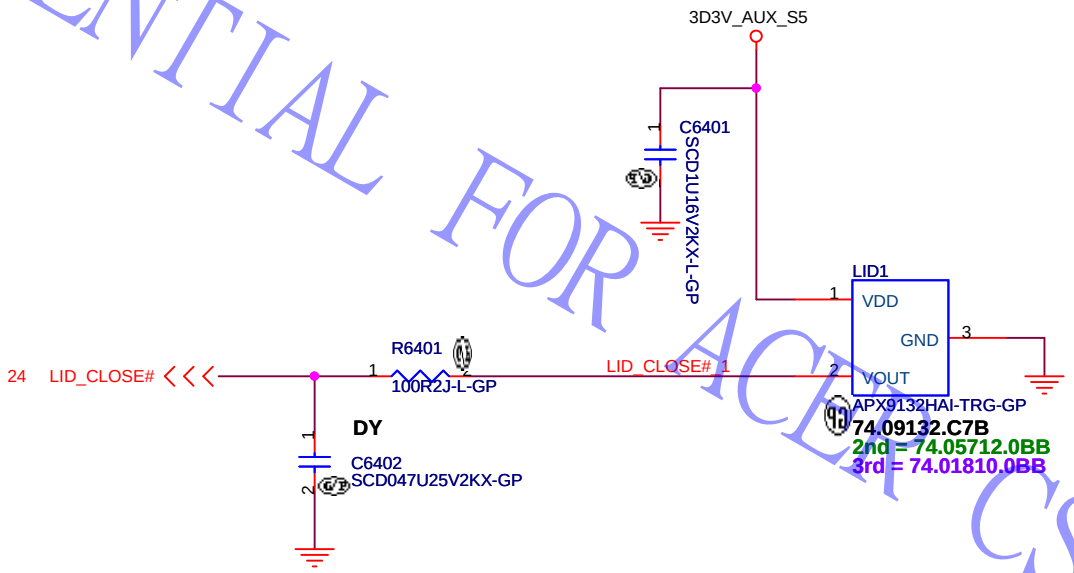
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Friday, May 16, 2014 Sheet 63 of 102



HADES

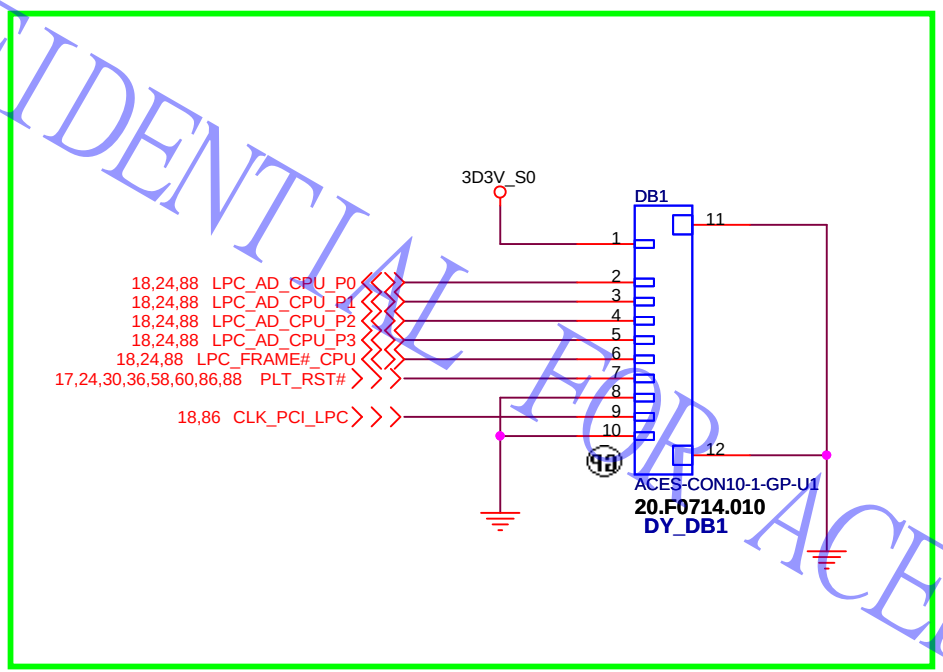
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Friday, May 16, 2014 Sheet 64 of 102

SB 20140401



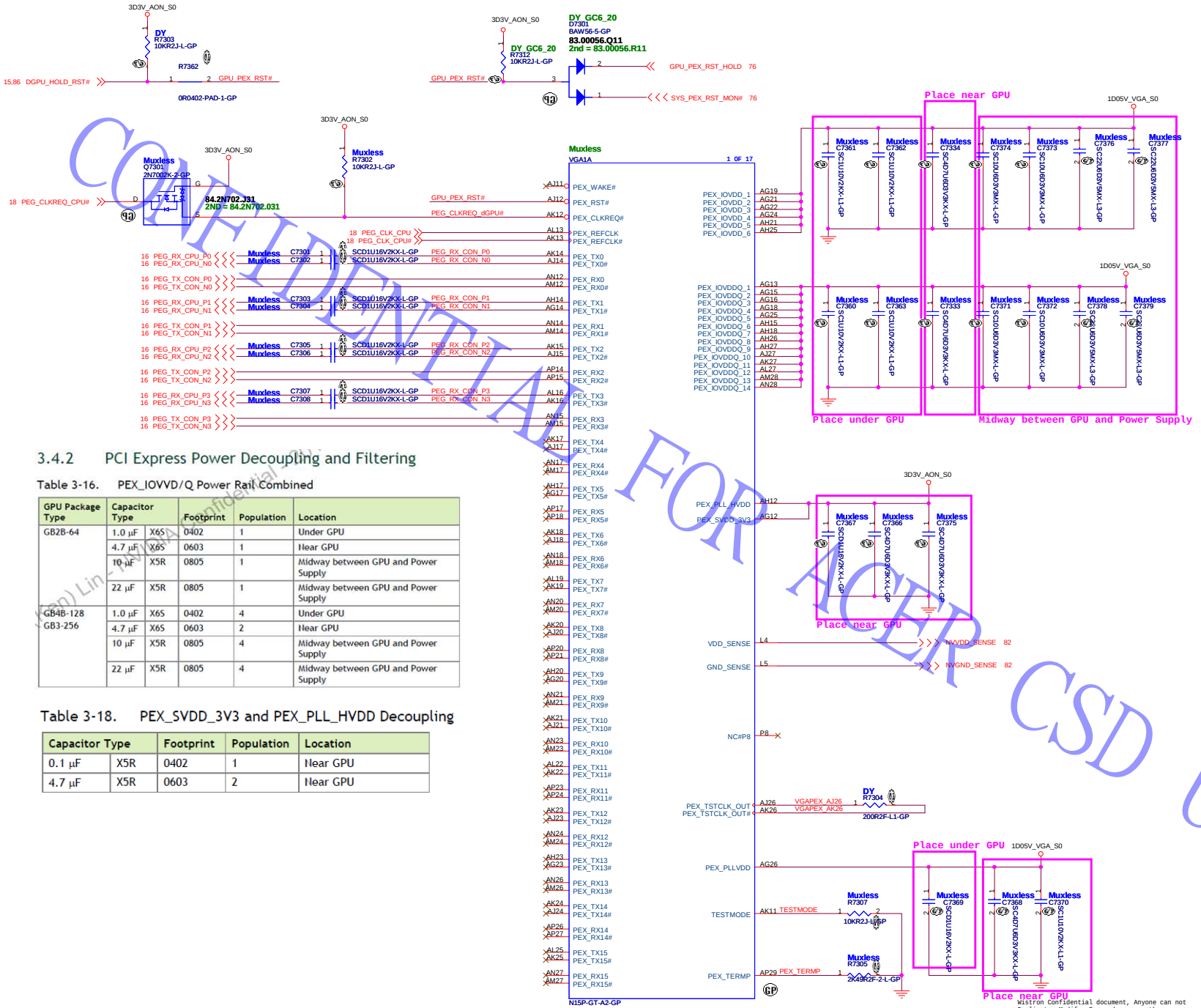
HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 65 of 102



3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVVD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 µF	X5R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

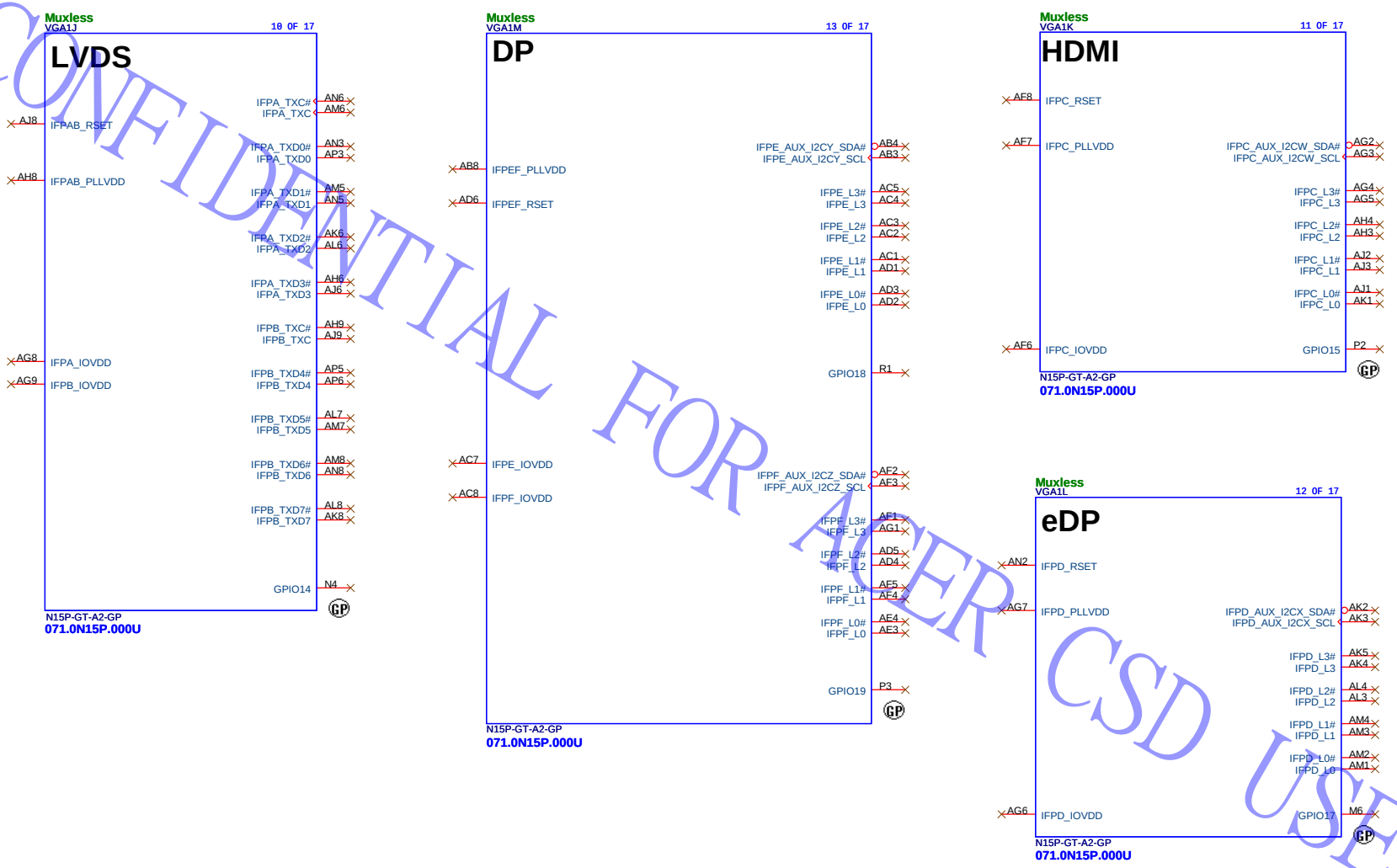
HADES

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(PEG)

Size: D | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 73 of 102



HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (DIGITALOUT)**

Size	Document Number	Rev
A3	Hades 840M ULT	-1

Date: Wednesday, April 30, 2014 Sheet 74 of 102

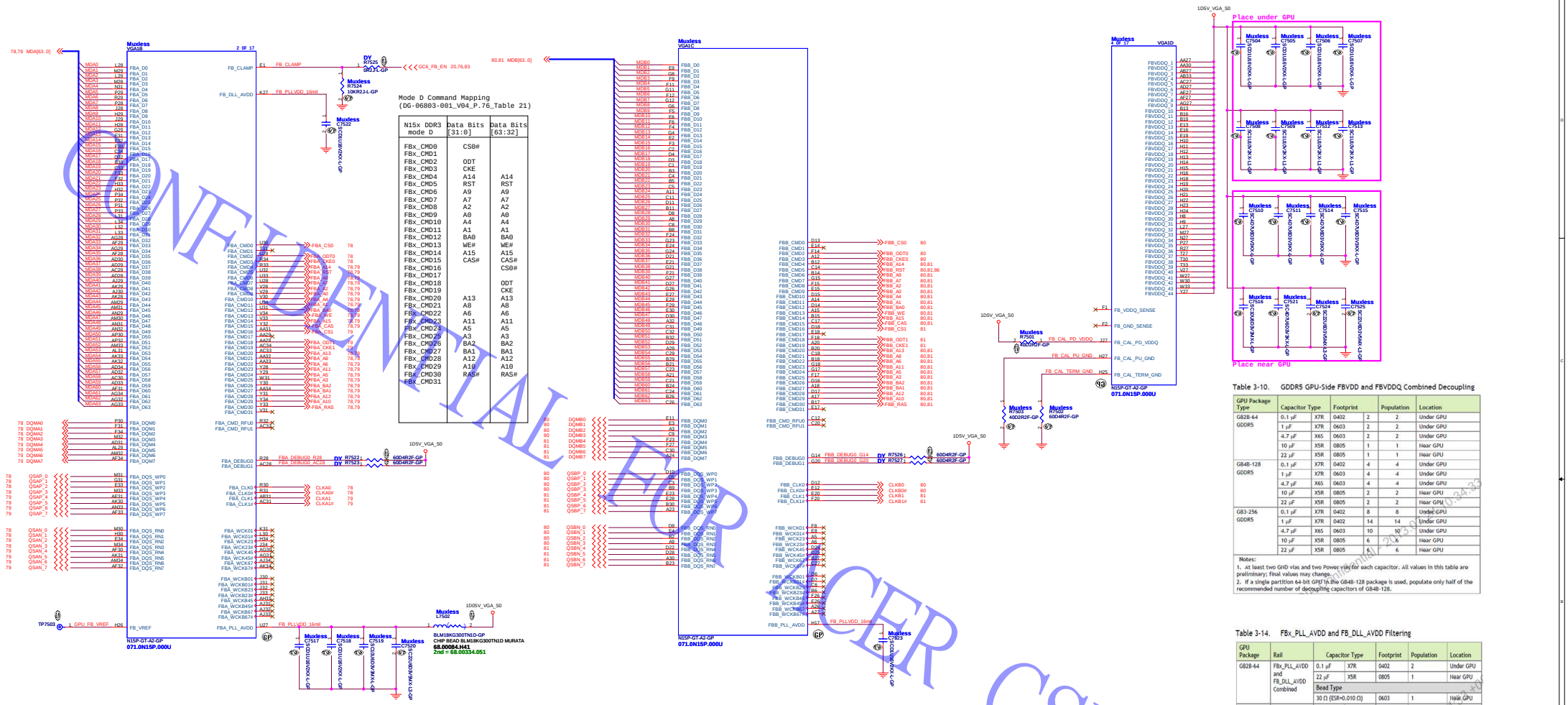


Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 GDDR5	0.1 µF X7R	0402	2	Under GPU
	1 µF X7R	0603	2	Under GPU
	4.7 µF X6S	0603	2	Under GPU
	10 µF X5R	0805	1	Near GPU
	22 µF X5R	0805	1	Near GPU
GB4B-128 GDDR5	0.1 µF X7R	0402	4	Under GPU
	1 µF X7R	0603	4	Under GPU
	4.7 µF X6S	0603	4	Under GPU
	10 µF X5R	0805	2	Near GPU
	22 µF X5R	0805	2	Near GPU
GB3-256 GDDR5	0.1 µF X7R	0402	8	Under GPU
	1 µF X7R	0402	14	Under GPU
	4.7 µF X6S	0603	10	Under GPU
	10 µF X5R	0805	6	Near GPU
	22 µF X5R	0805	6	Near GPU

Notes:
1. At least two GND vias and two Power vias for each capacitor. All values in this table are preliminary; final values may change.
2. If a single partition 64-bit GPU in the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.

Table 3-14. FBx_PLL_AVDD and FB_DLL_AVDD Filtering

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF X7R	0402	2	Under GPU
		22 µF X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU
GB4B-128	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF X7R	0402	3 (1 per ball)	Under GPU
		22 µF X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU
GB3-256	FBx_PLL_AVDD	0.1 µF X7R	0402	4 (1 per ball)	Under GPU
		22 µF X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU

Note: Filtering for FB_PLL_DLL_AVDD on GB3-256 is combined with PLL filtering in section 3.9.2.

HADES

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F)
Size: Custom
Document Number: Hades_840M_ULT
Rev: -1
Date: Tuesday, May 13, 2014
Sheet 19 of 102

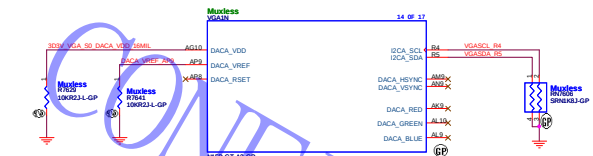
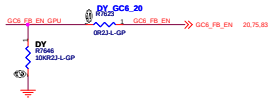


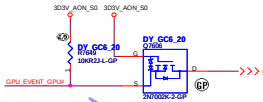
Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05)		0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

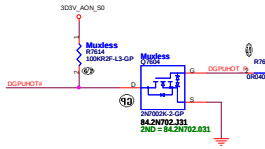
GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	SP_PLLVDD + VID_PLLVDD	0.1 µF	X7R	0402	1 per ball	Under GPU
		4.7 µF	X5R	0603	1	Near GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)		0603	1	Near GPU



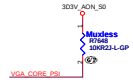


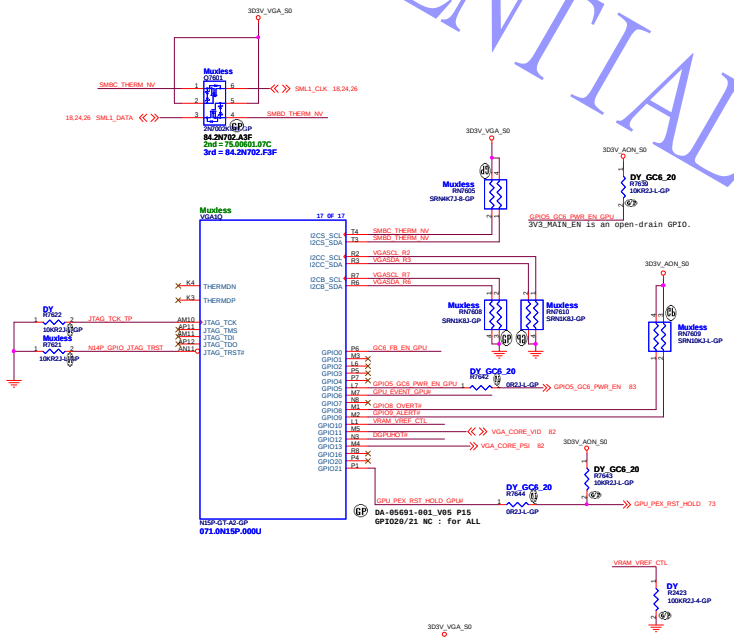
20140423

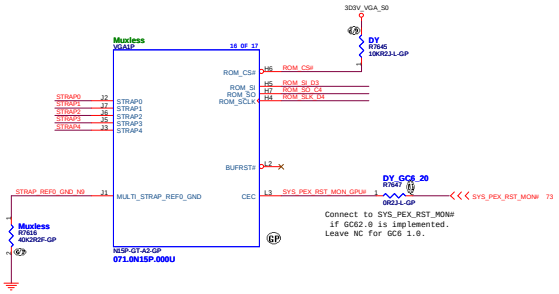
Follow N15x GPU design guide and implement OVERT function

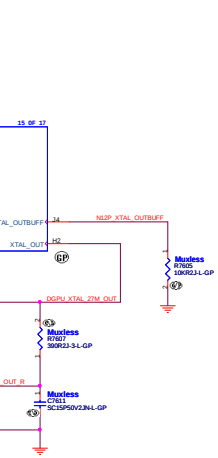


GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON









DDR3	1.5V/ 1.5V	Single Rank	Hynix	H5TC4G63AFR-11C	A-die	0x0	1000	N/A	Production candidate
			Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production candidate
			Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	N/A	Post-production candidate

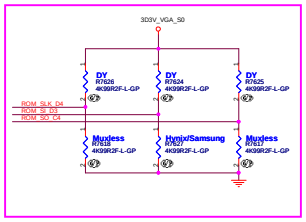
Table 113. Resistance Mapping to Hex Values

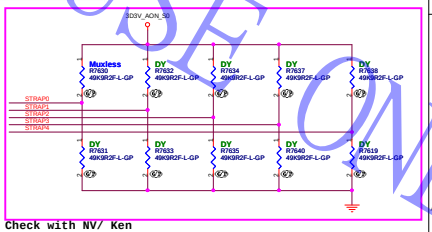
Resistor Values	Pull-up to VDD33	Pull-down to GND	
4.99 k	1000	0000	Hynix
10.0 k	1001	0001	
15.0 k	1010	0010	Samsung
20.0 k	1011	0011	
24.9 k	1100	0100	
30.1 k	1101	0101	
34.8 k	1110	0110	
45.3 k	1111	0111	

4.99Kohm	64.49915.6DL
10Kohm	64.10025.L0L
15Kohm	64.15025.6DL
20Kohm	64.20025.6DL
24.9Kohm	64.24925.6DL
30.1Kohm	64.30125.6DL
34.8Kohm	64.34825.6DL
45Kohm	64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			





Check with NV/ Ken

Hynix	H5TC4G63AFR-11C	A-die	0x0	1000
Micron	MT41J256M16HA-093G:E	E-die	0x1	1000
Samsung	K4W4G1646D-BC1A	D-die	0x2	1000

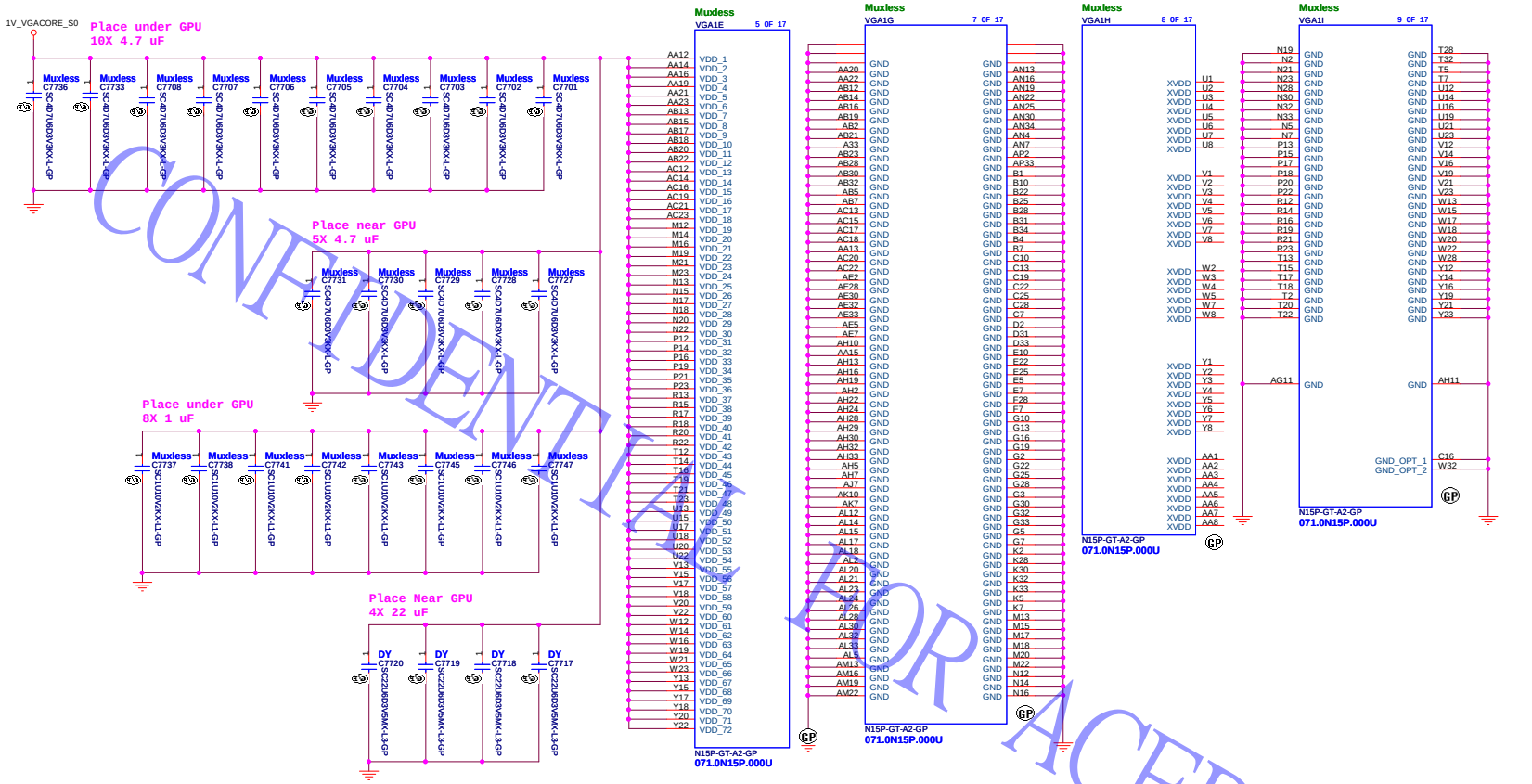
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (GPIO/STRAP)

Size	Document Number	Rev
Custom	Hades 840M_ULT	-1

Date: Monday, May 19, 2014 Sheet 78 of 102



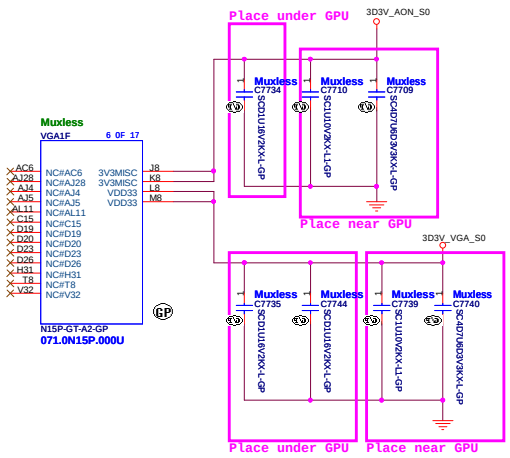


Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ
GB4B-128	4.7 µF	X6S	0603	15	15	Under GPU	
	1 µF	X6S	0402	8	8	Under GPU	
	22 µF	X5R	0805	14	7	Near GPU	See Note 2
	4.7 µF				5	Near GPU	
	330 µF	POS	7343	2	2	Near GPU	ESR ≤ 6 mΩ
GB3-256	0.1 µF	X7R	0402	20	20	Under GPU	
	4.7 µF	X6S	0603	40	40	Under GPU	
	10 µF	X5R	0805	4	4	Near GPU	
	22 µF	X5R	0805	11	11	Near GPU	
	100 µF	X5R	1206	4	0	Near GPU	
	330 µF	POS	7343	4	4	Near GPU	ESR ≤ 6 mΩ

Notes:
1. Generally the decoupling capacitor footprint requirement will remain the same but the population may get updated or may differ per GPU SKU. Always refer to the latest PUH for any NVVDD decoupling requirement update for specific GPU SKUs.
2. Combine / co-layout two 0805 footprints into each of the POSCAP footprint. So a total of four 0805 footprints should be placed inside the two POSCAP foot prints, allocating fourteen 0805 footprints total.

Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

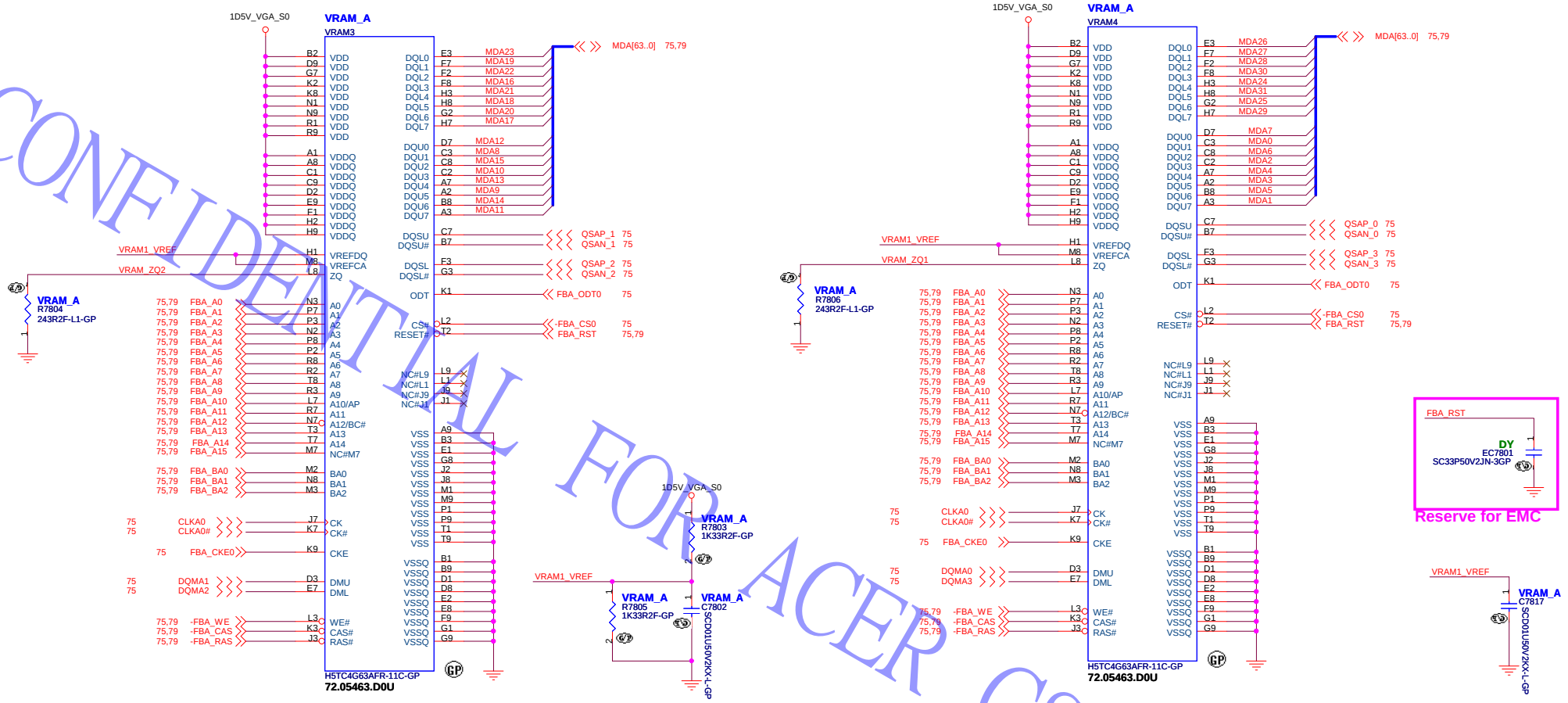
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (POWER/GND)

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, July 30, 2014 | Sheet 77 of 102



FOR VRAM3

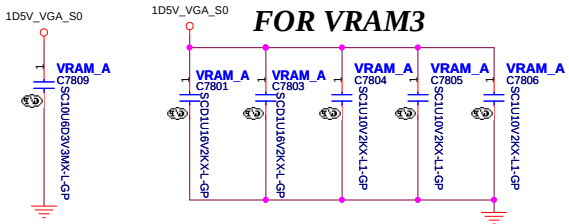
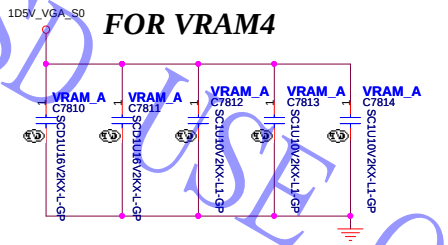


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

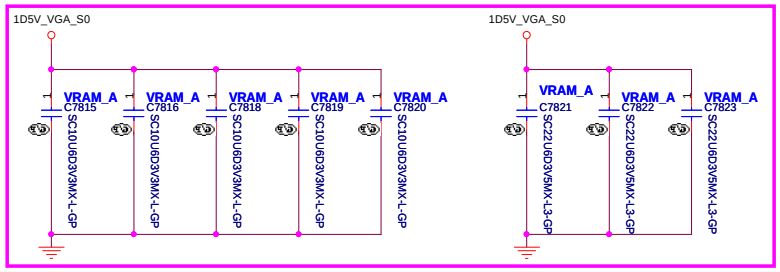
Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

FOR VRAM4



0214/02/27



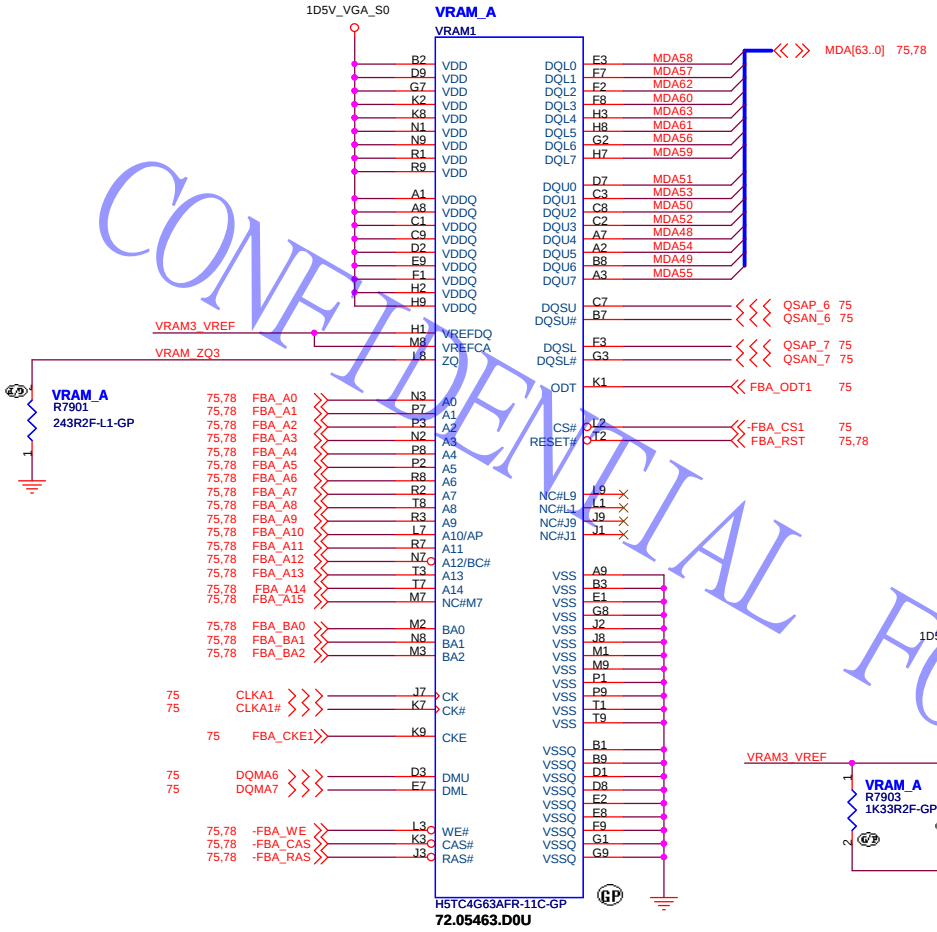
HADES

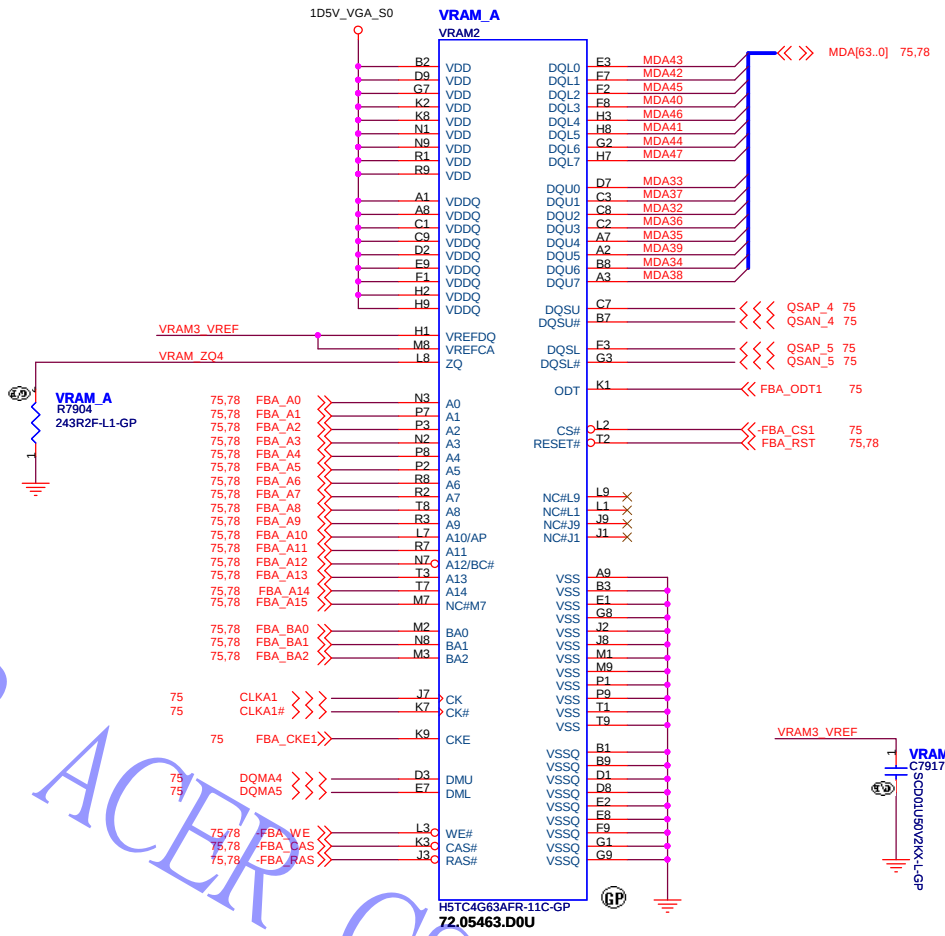
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

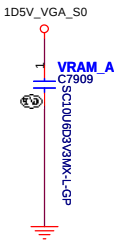
Title: **GPU-VRAM1,2 (1/4)**

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 78 of 102







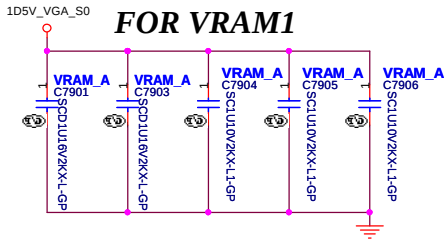
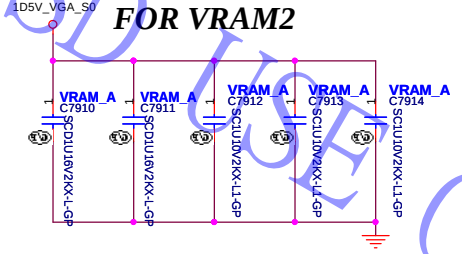


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



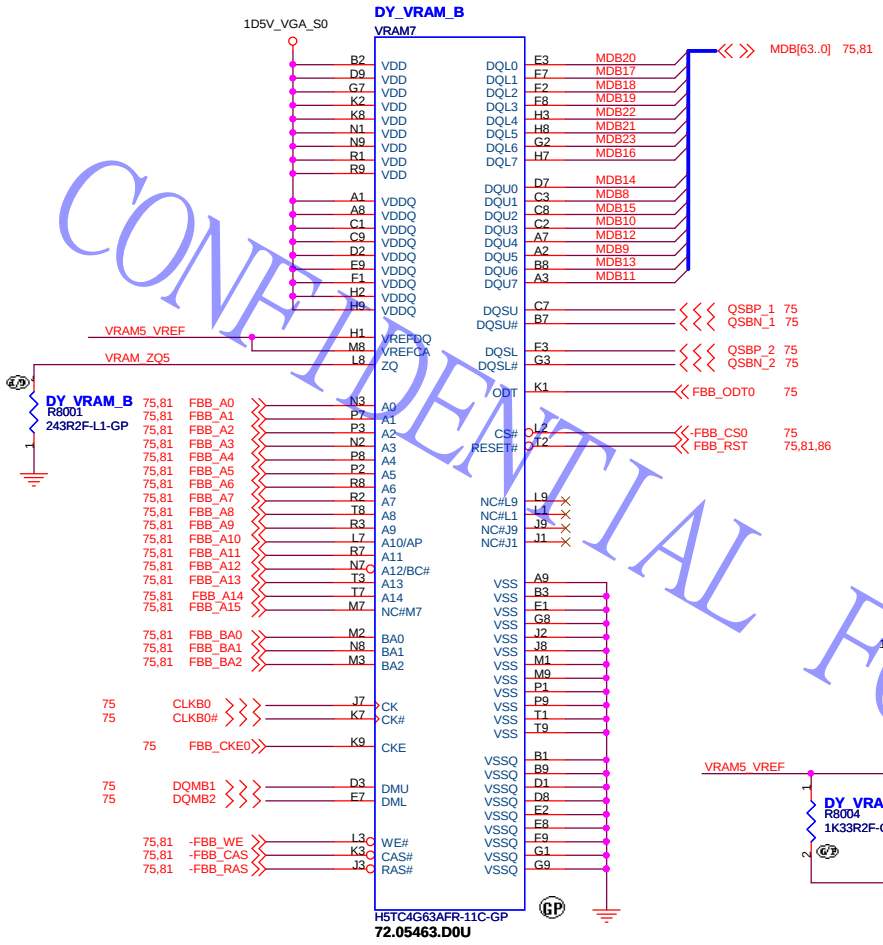
HADES

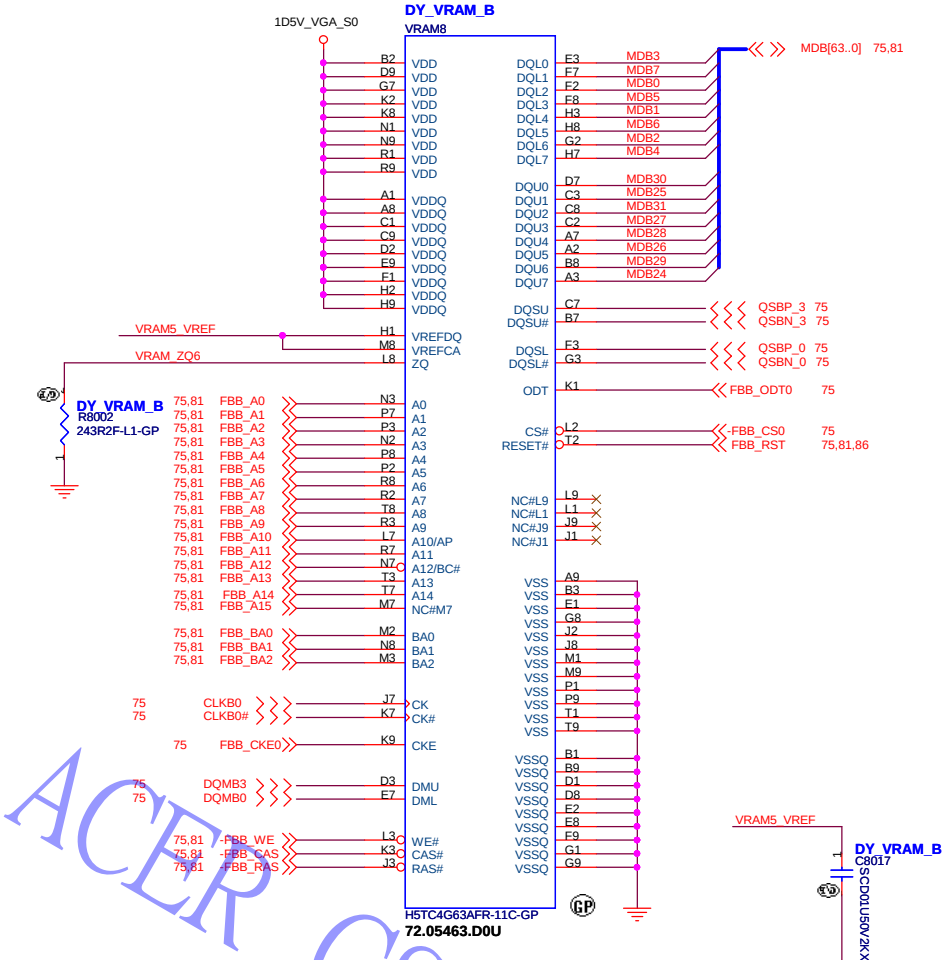
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

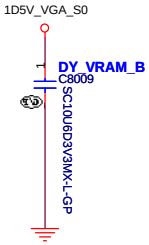
Title: **GPU-VRAM3,4 (2/4)**

Size	Document Number	Rev
Custom	Hades 840M ULT	-1

Date: Wednesday, April 30, 2014 Sheet 79 of 102







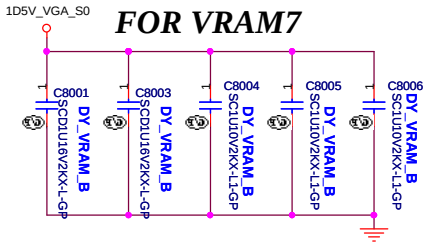
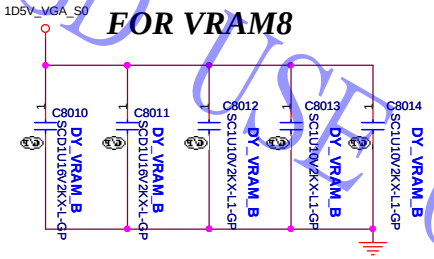


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separato					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



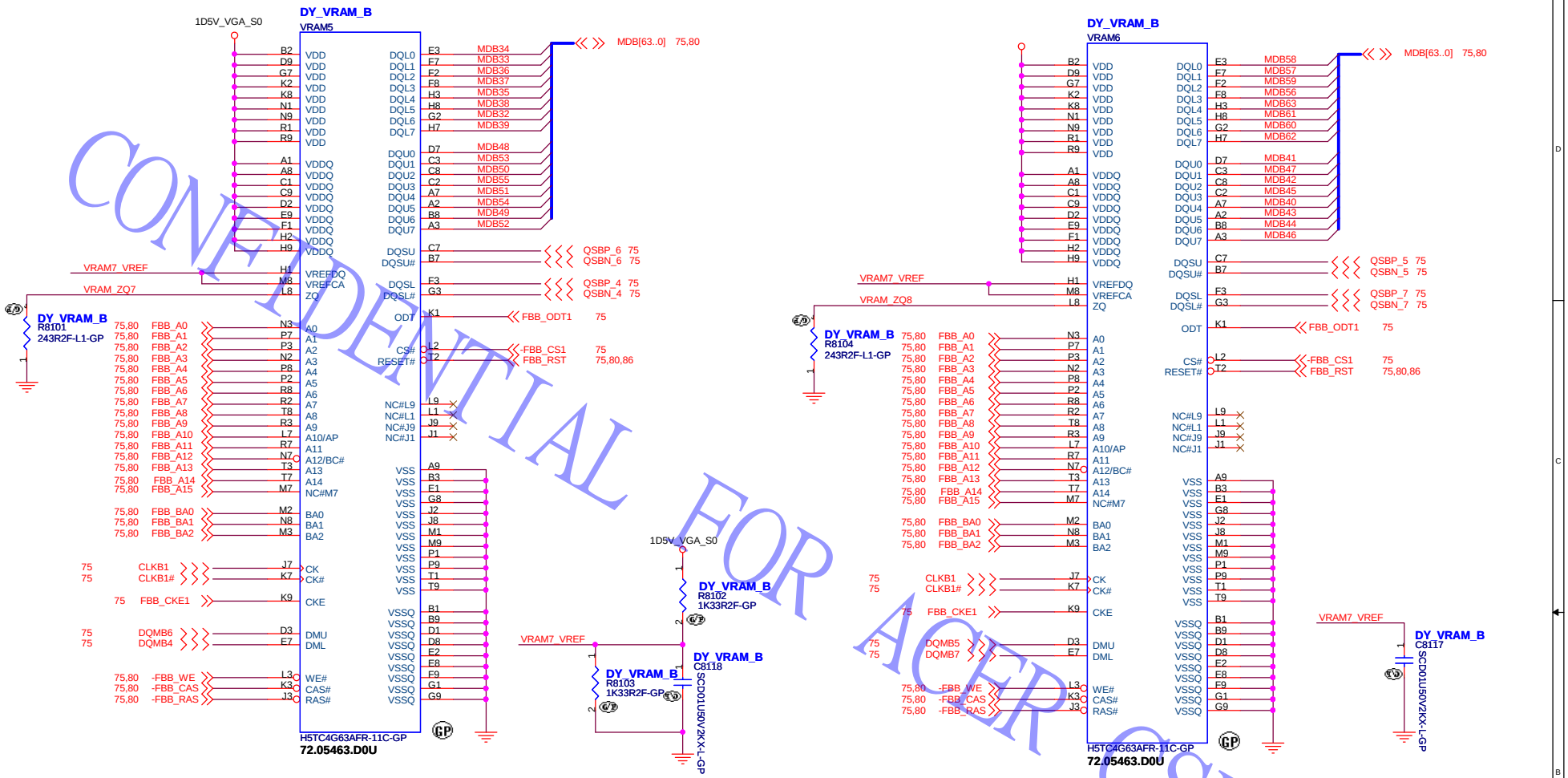
HADES

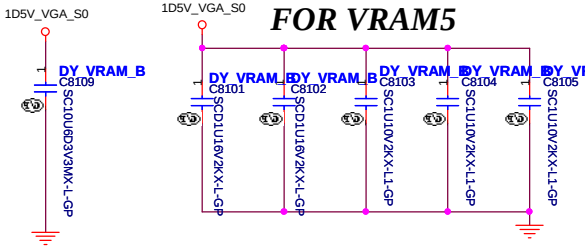
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM5,6 (3/4)**

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 80 of 102



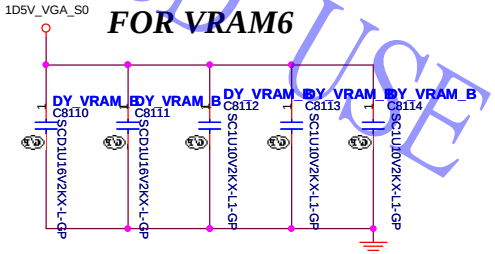


FOR VRAM5

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



FOR VRAM6

HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 81 of 102

VGA : N15P GT
Config : B
EDP-Continuous : 49A
EDP-Peak : 76A

	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF

RT8813AGQW-GP

OCP setting
PR8224 15K 'OCP = 102A

20140122
Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A
PL8201 IND-036UH-42-GP

20140122
Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A
PL8202 IND-036UH-42-GP

20140122
Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A
PL8203 IND-036UH-42-GP

470uF/2V, 7.5 x 4.5 x 2.1
ESR=9mohm
Ripple Current=3000 mA

SB 20140327

HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

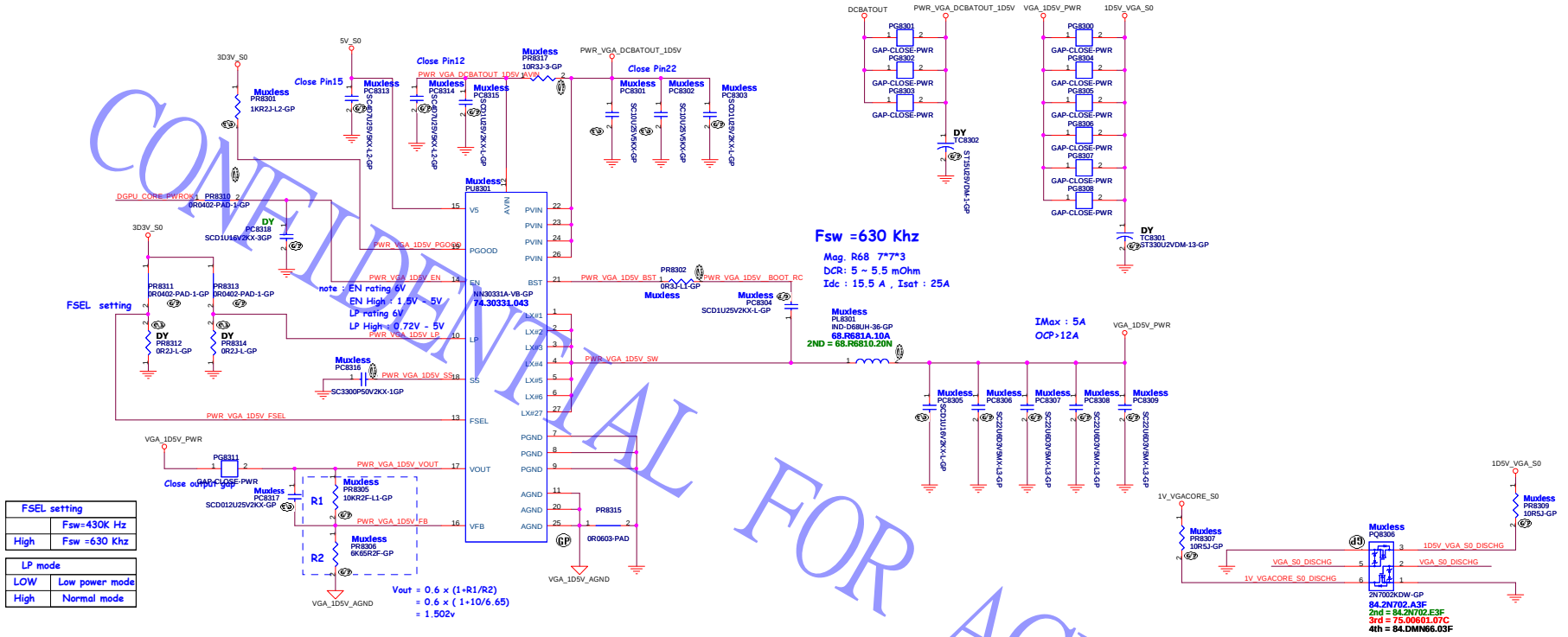
Title: RT8812A VGA CORE

Size: Custom | Document Number: Hades 840M ULT | Rev: -1

Date: Thursday, May 22, 2014 | Sheet 82 of 102

NN30331A for VGA_1D5V(For VRAM DDR3)

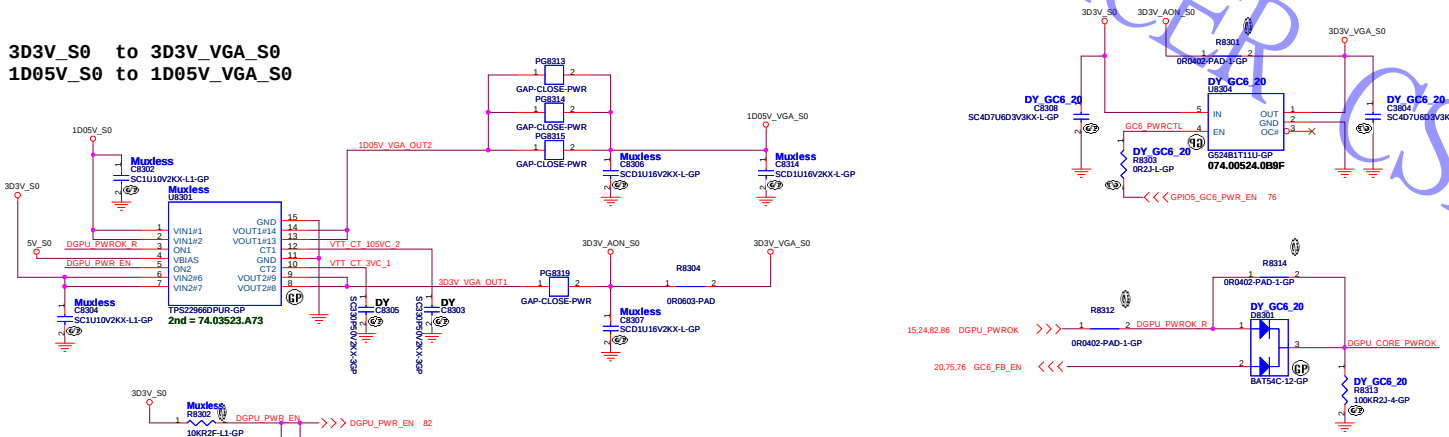
VGA_CORE&1D05V_VGA_S0 Discharge Circuit



FSEL setting	
	Fsw=430K Hz
High	Fsw =630 Khz

LP mode	
LOW	Low power mode
High	Normal mode

3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



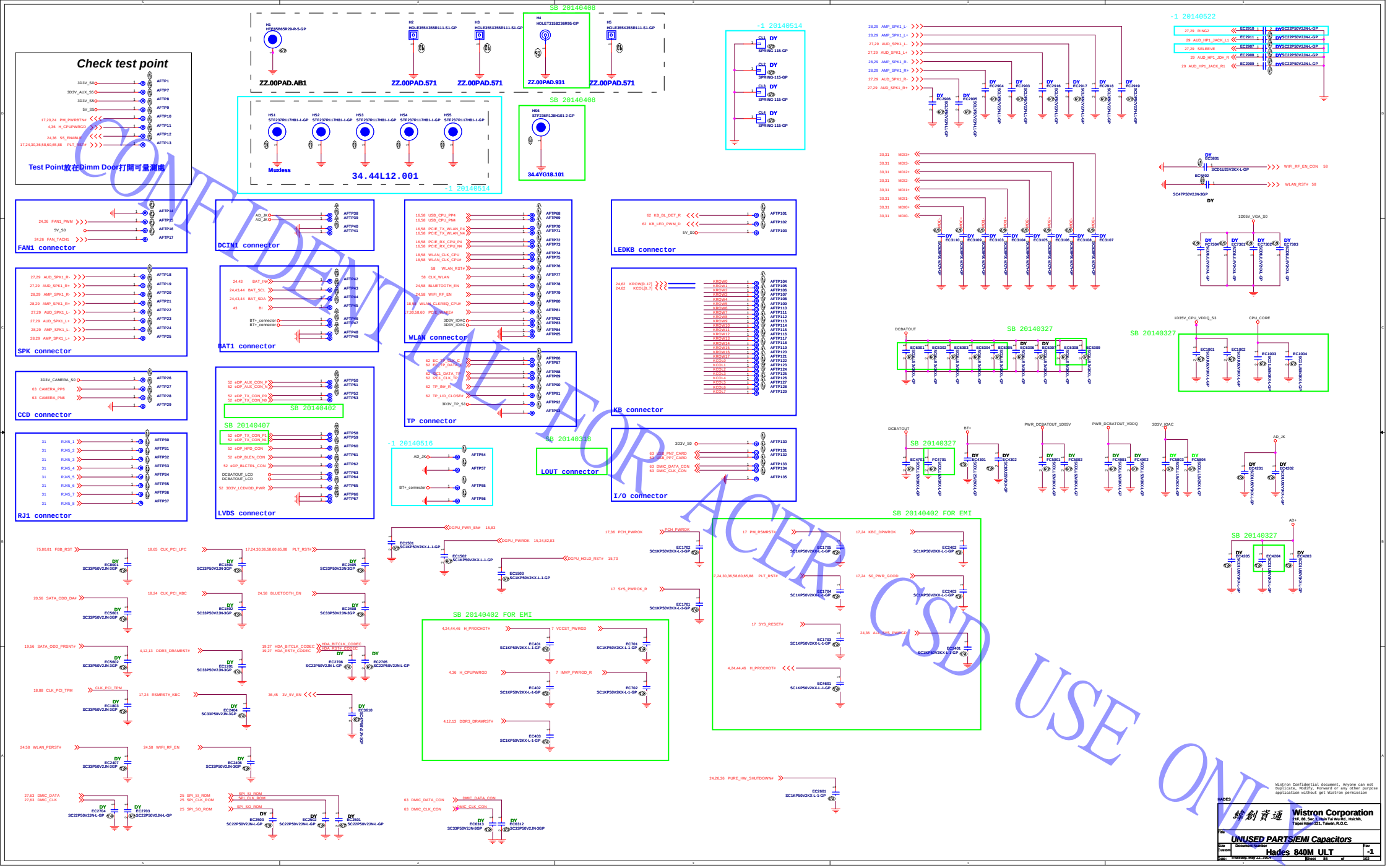
HADES

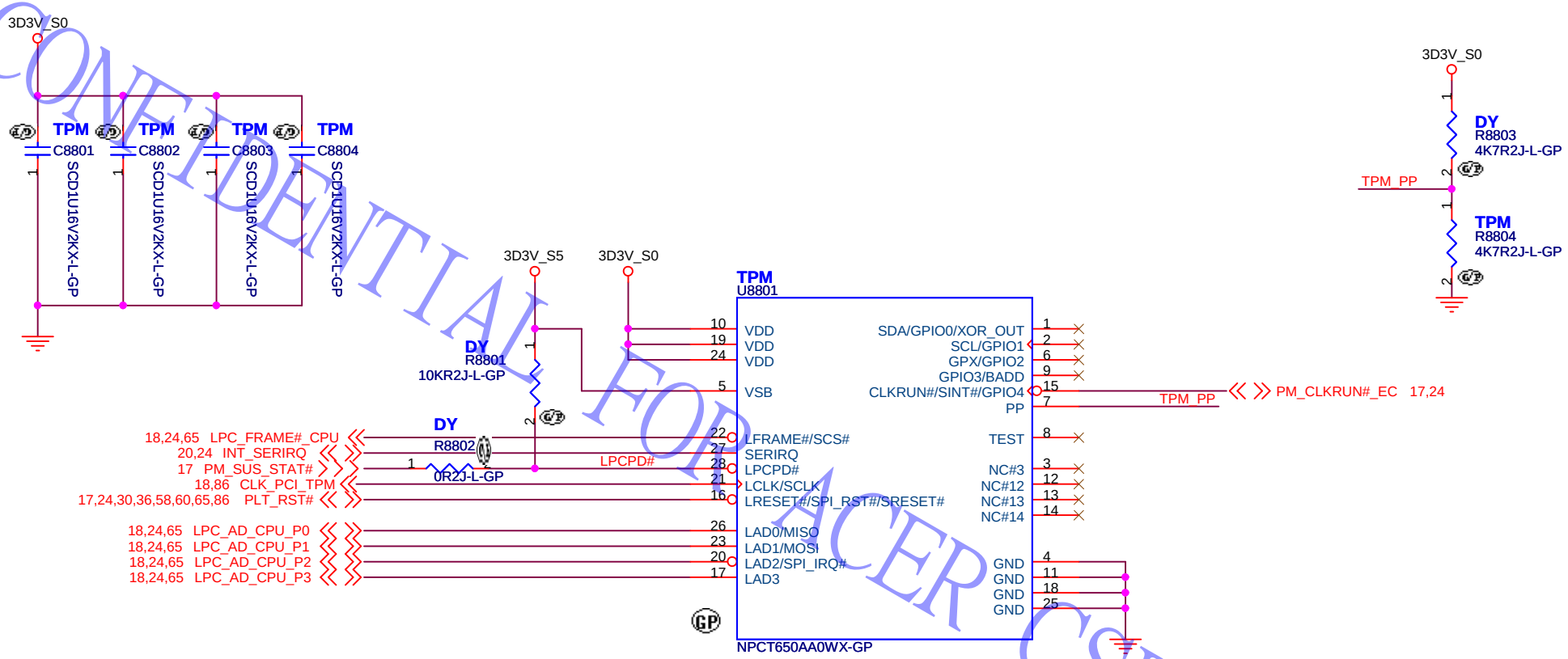
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Thursday, May 22, 2014 | Sheet 83 of 102


Check test point
Test Point放在Dimm Door打開可量測處
ZZ.00PAD.AB1
ZZ.00PAD.571
ZZ.00PAD.571
ZZ.00PAD.931
ZZ.00PAD.571
Muxless
34.44L12.001
34.4YG18.101
FAN1 connector
DCIN1 connector
BAT1 connector
SPK connector
CCD connector
RJ1 connector
LVDS connector
WLAN connector
TP connector
LEDKB connector
KB connector
I/O connector
LOUT connector
SB 20140402
SB 20140407
SB 20140408
SB 20140514
SB 20140516
SB 20140318
SB 20140327
SB 20140402 FOR EMI
-1 20140514
-1 20140516
-1 20140522
CONFIDENTIAL FOR ACER CSD USE ONLY
UNUSED PARTS/EMI Capacitors
Wistron Corporation
Hades 840M ULT
http://vinafix.vn



HADES

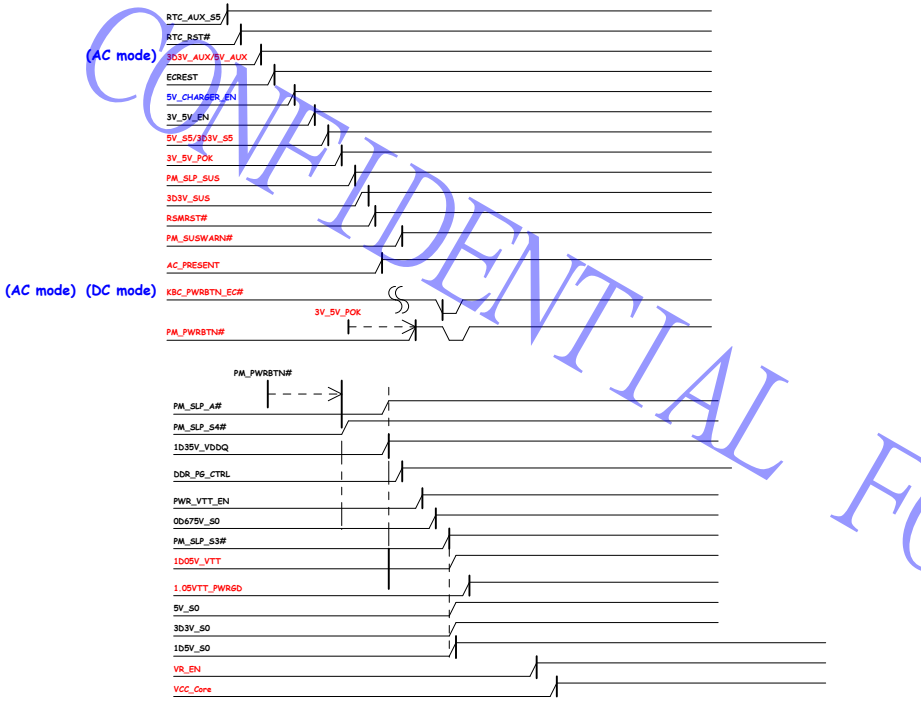
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

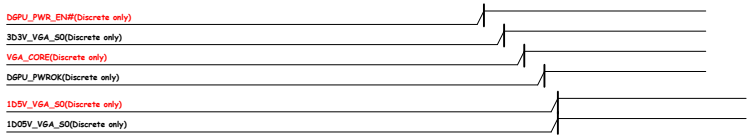
Title: ***TPM (SLB655T)***

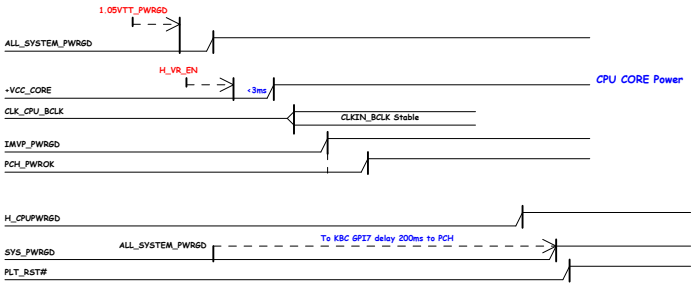
Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Tuesday, May 06, 2014 Sheet 88 of 102

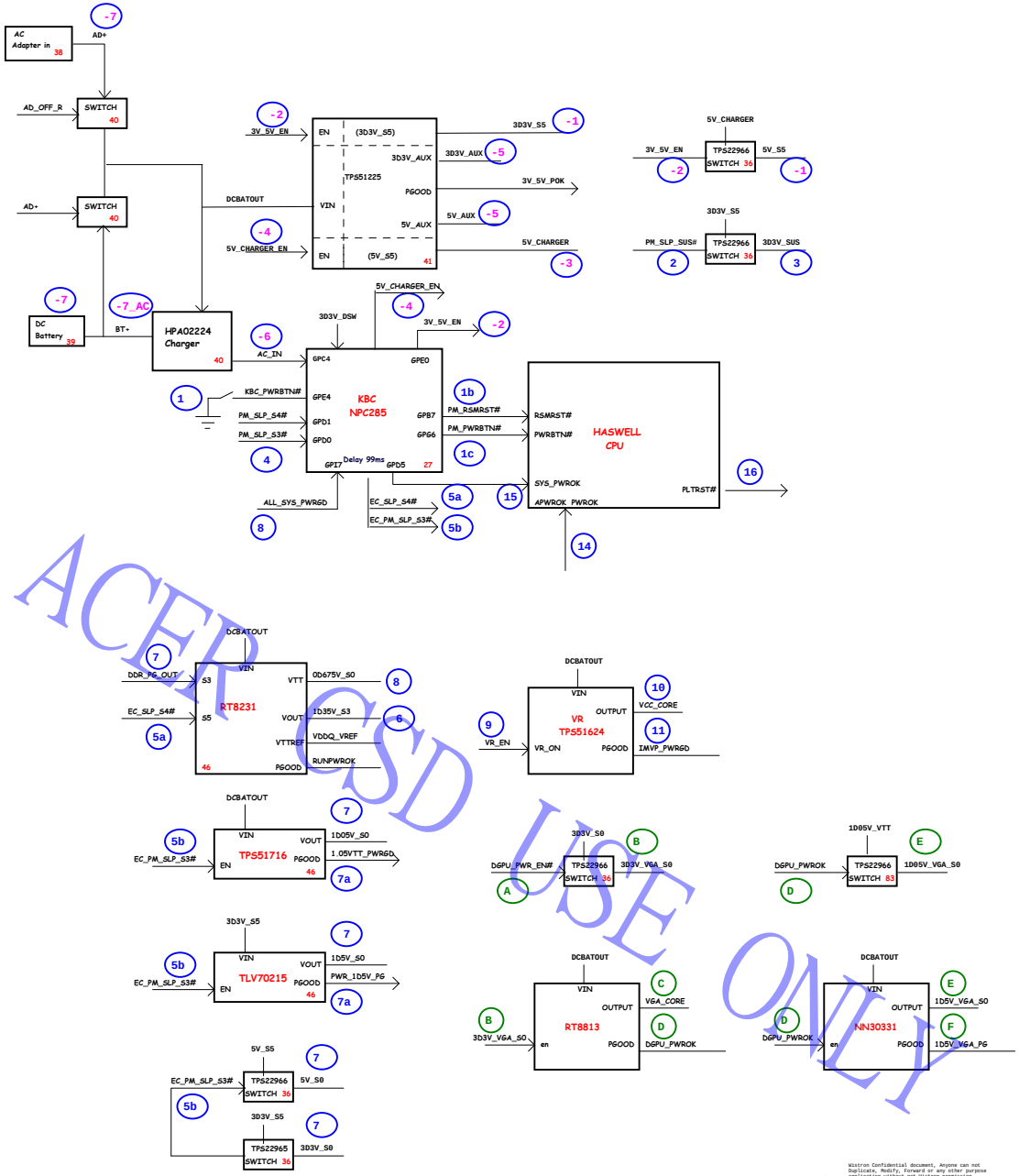
Intel-Power Up Sequence







HASWELL POWER UP SEQUENCE DIAGRAM



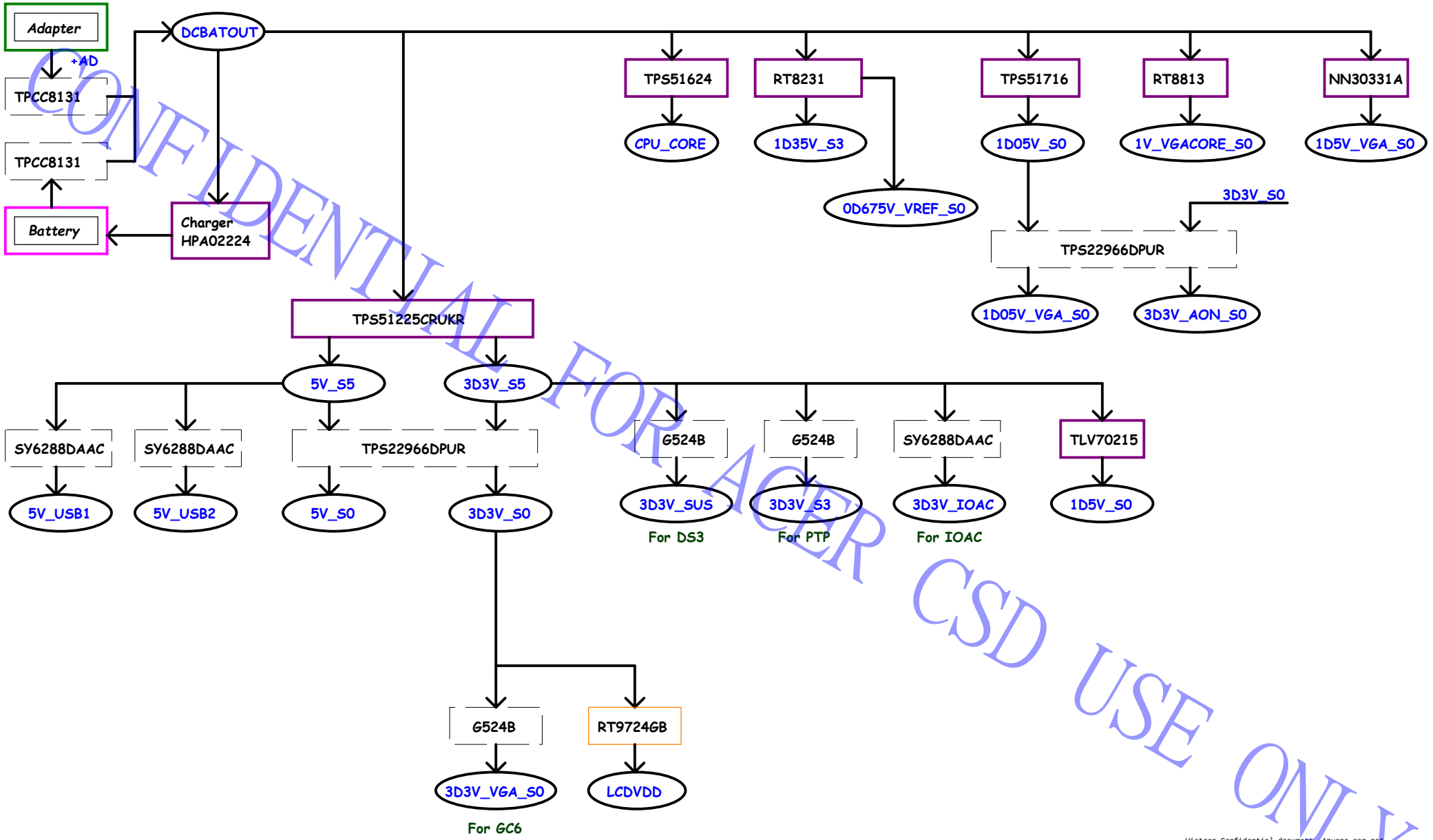
HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size: A3 | Document Number: Hades 840M ULT | Rev: -1

Date: Wednesday, April 24, 2013 | Sheet 59 of 102



HADES

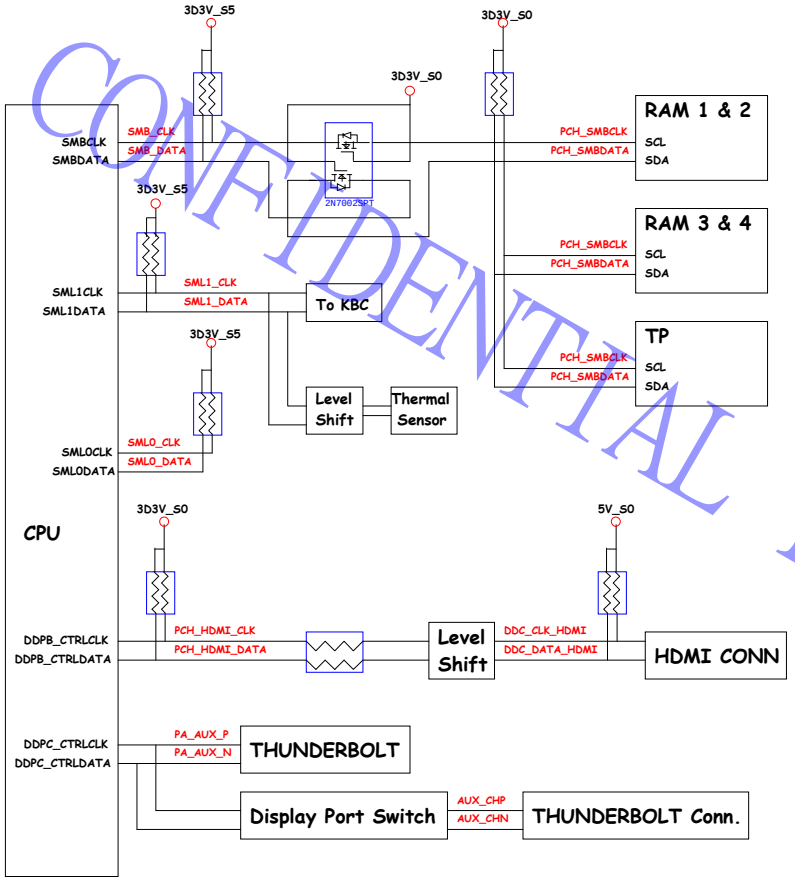
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

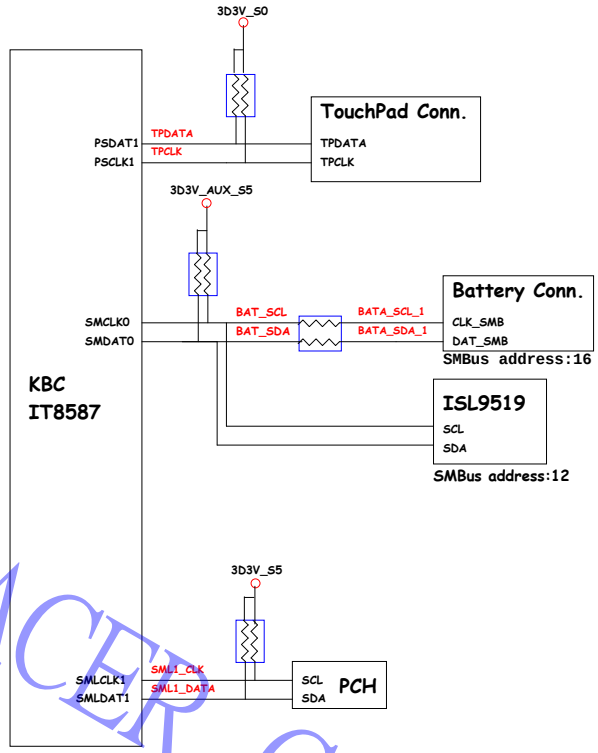
Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 100 of 102

PCH SMBus Block Diagram



KBC SMBus Block Diagram



HADES

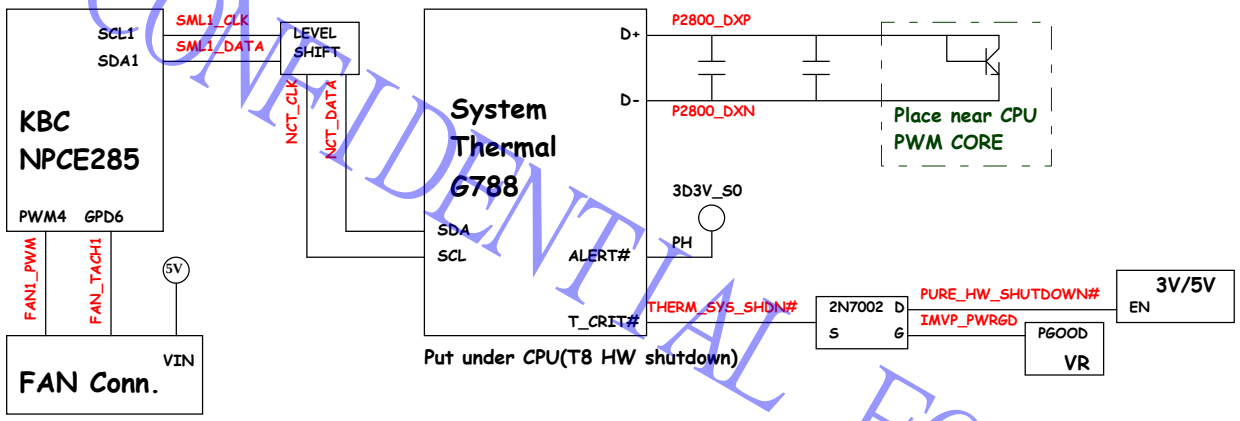
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

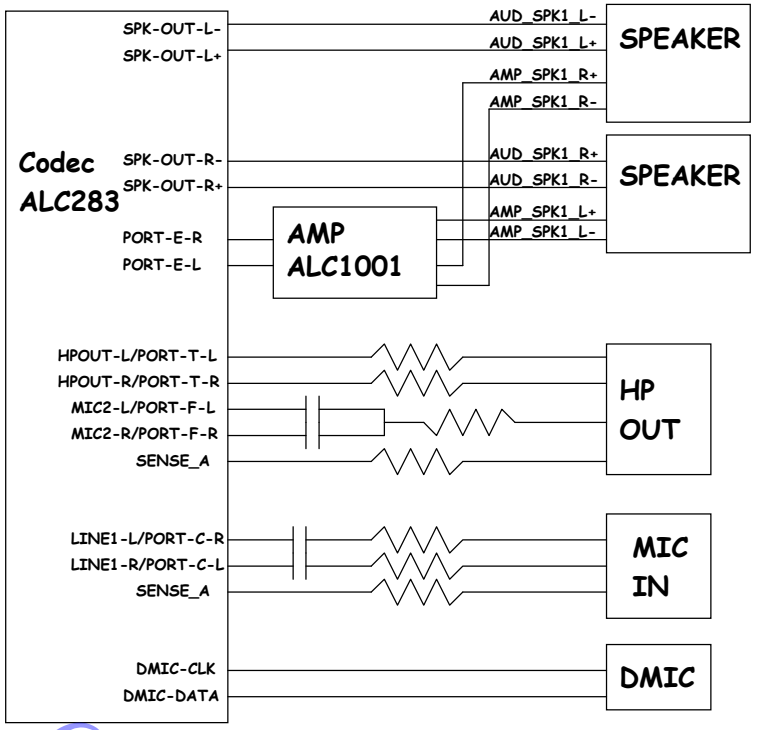
Size	Document Number	Rev
A2	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 101 of 102

Thermal Block Diagram



Audio Block Diagram



HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	THERMAL/AUDIO BLOCK DIAGRAM	
Size: Custom	Document Number: Hades_840M_ULT	Rev: -1
Date: Wednesday, April 30, 2014	Sheet 102 of 102	