LV315GM Schematics

Gemini Lake

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DY	***DUMMY***
DY-EMC	***Follow EMC team request (DY)***
EMC-TEST	***Follow EMC team request (ASM)***

BOM1

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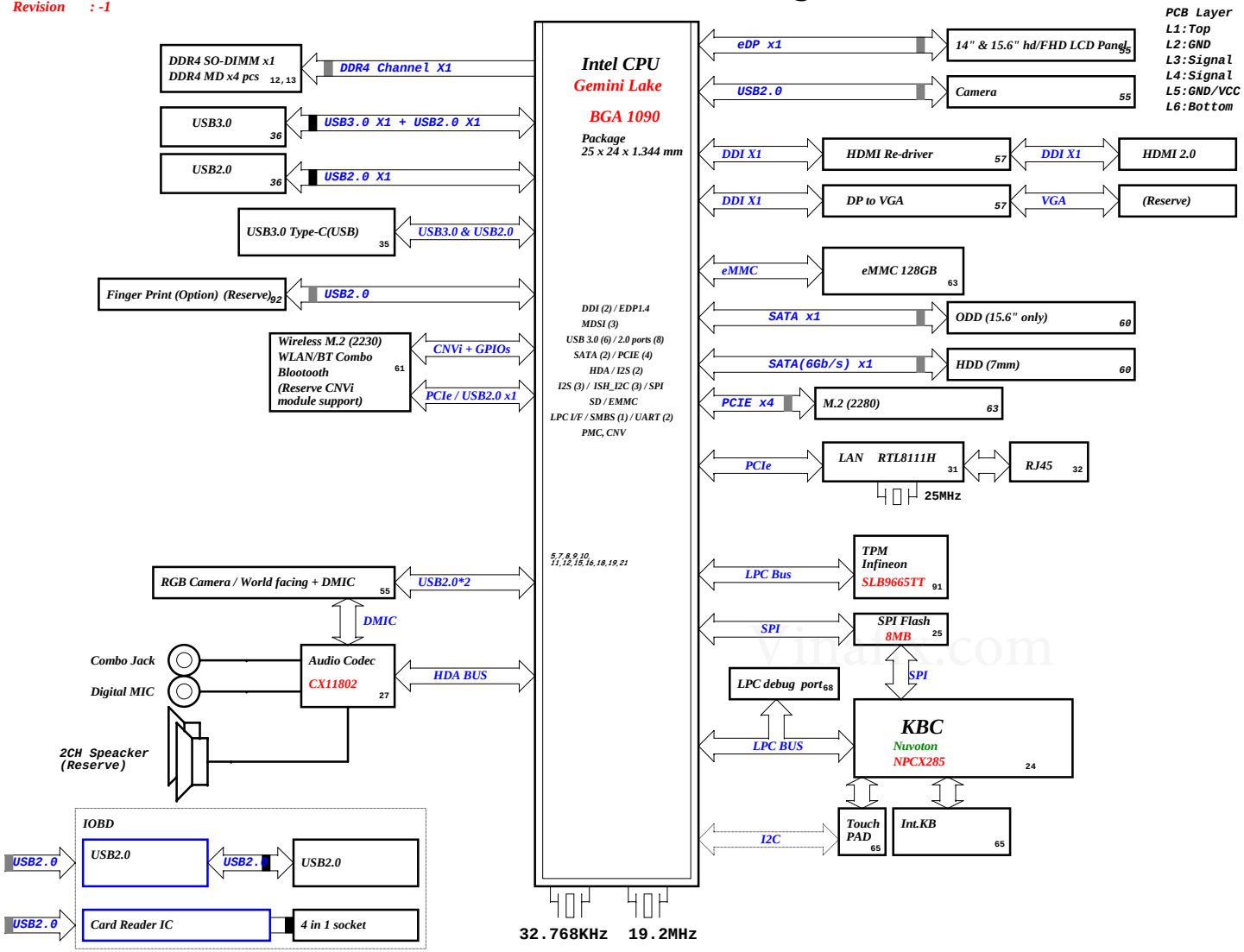
Title: ***Cover Page***

Size: A3 | Document Number: LV315GM MB | Rev: -1

Date: Friday, March 30, 2018 | Sheet 1 of 106

Project code : 4PD0DG010001
PCB P/N : 17839
Revision : -1

Gemini Lake Board Block Diagram



CHARGER HPA02224	44
INPUTS	OUTPUTS
19V_DCBATOUT	BT+

SYSTEM DC/DC TPS51225BRUKR	45
INPUTS	OUTPUTS
19V_DCBATOUT	5V_S5 3D3V_S5

CPU PMIC RT5092AGQW-GP	46
INPUTS	OUTPUTS
19V_DCBATOUT	1D8V_S5 1D2V_S5 1D05V_S0

SYSTEM DC/DC RT9610BZQW	47
INPUTS	OUTPUTS
5V_S5	1V_CPU_VCGI

DDR4 RT9610BZQW	51
INPUTS	OUTPUTS
5V_S5	1D2V_CPU_VDDQ_S3

DDR4 PMIC RT5092AGQW-GP	46
INPUTS	OUTPUTS
3D3V_S5	2D5V_S3

SYSTEM Load switch G2898KD1U	40
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0

BOM1

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Title: Block Diagram

Size: A2 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 2 of 106

SSID = CPU

Blanking

BOM1

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Title: *CPU (Reserved)*

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 3 of 106

SSID = CPU

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BOM1

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Title	CPU (Reserved)	
Size A4	Document Number LV315GM MB	Rev -1
Date: Friday, March 30, 2018	Sheet 4 of 106	

SSID = CPU

CPU1A

1 OF 13

DDR4_LP3_LP4

GEMINI-LAKE-GP

DDR0

CPU1B

2 OF 13

DDR1

MEM_CH0_ODT0->BD39
DEL: M_A_ODT0_20170615

WE# /A14
CAS#/A15
RAS#/A16

WE# /A14
CAS#/A15
RAS#/A16

Layout Notes:
DDR RCOMP trace W/S=15/15mil, and length <500mil

0220 Rename net
SM_RCOMP_1
SM_RCOMP_0
R503 110R2F-GP
R504 110R2F-GP
#567247 #82 Figure 5-1 system memory resistive compensation

ZZ.00CPU.131

BOM1

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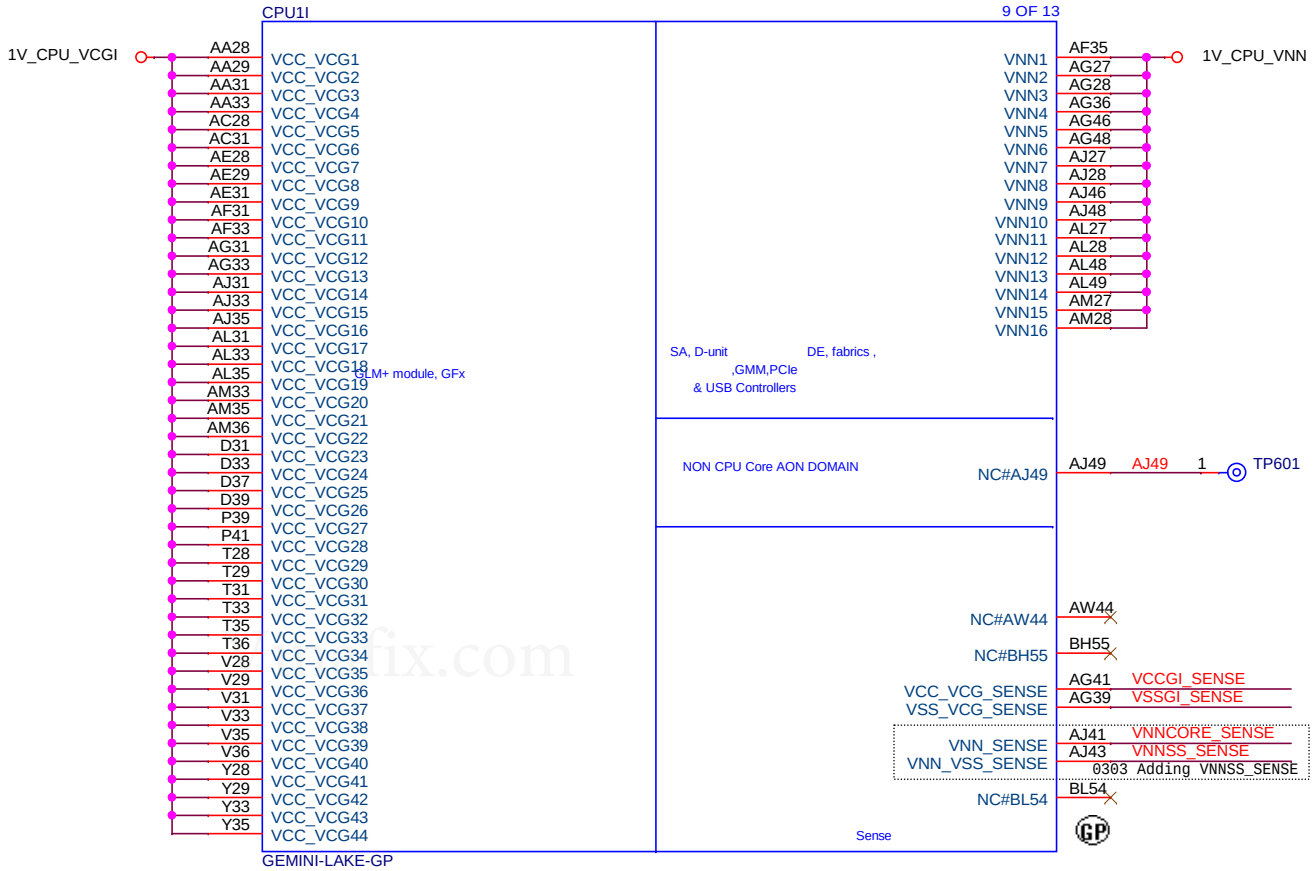
Title: CPU (DDR)

Size: A2 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 5 of 106

SSID = CPU PDG P54

47 VSSGI_SENSE
47 VCCGI_SENSE
50 VNNCORE_SENSE
50 VNNSS_SENSE



BOM1

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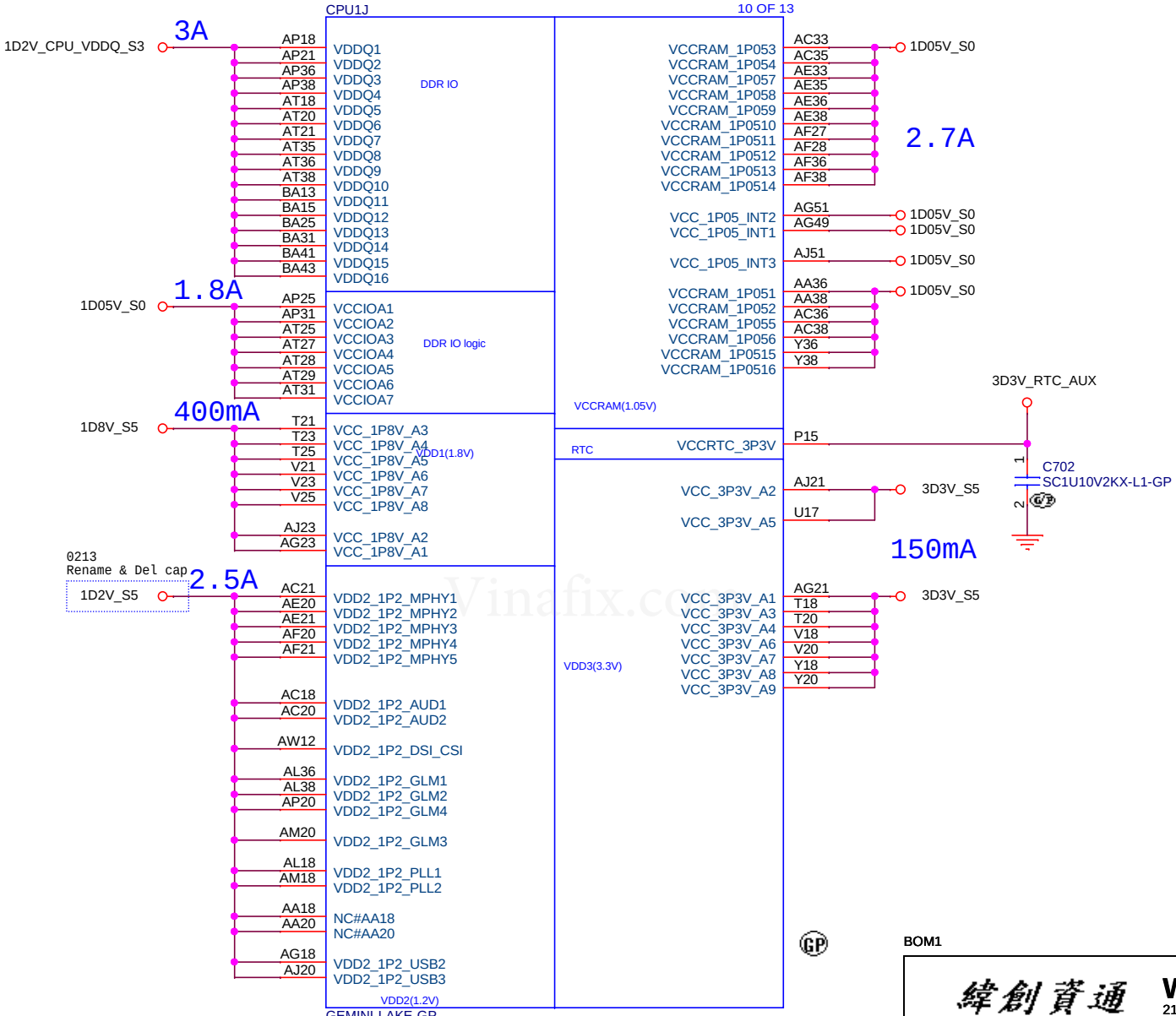
Title: ***CPU (VCCGI/VNN/Others)***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 6 of 106

SSID = CPU



@ Tie VCCIOA to VDDQ for LPDDR4 designs
@ Tie VCCIOA to VCCRAM_1P05 for DDR4 designs

ZZ.00CPU.131

BOM1

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Title: **CPU (VDDQ/VCCIO/Others)**

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 7 of 106

SSID = CPU

VGA

20170505 Change Net name

56 VGA_DATA_CPU_P0
56 VGA_DATA_CPU_N0
56 VGA_DATA_CPU_P1
56 VGA_DATA_CPU_N1
56 VGA_AUX_CPU_P
56 VGA_AUX_CPU_N
56 VGA_HPD_CPU

HDMI

57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_DET_CPU

EDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_BLEN_CPU
55 eDP_VDDEN_CPU
55 eDP_HPD_CPU
55 eDP_BLCTRL_CPU

15 GPIO42_FLASH_OVR
24 ME_UNLOCK

20170505 Change Net name

VGA

VGA_DATA_CPU_P0 AH1
VGA_DATA_CPU_N0 AH3
VGA_DATA_CPU_P1 AE2
VGA_DATA_CPU_N1 AE3
AJ2
AJ3
AG2
AG3
VGA_AUX_CPU_P AC12
VGA_AUX_CPU_N AC10
VGA_HPD_CPU C39
B43
C43

3D3V_S5
R808 10KR2J-L-GP

20170505 Change Net name

3.3V (default)

CPU1C
3 OF 13
DDI0_TXP_0
DDI0_TXN_0
DDI0_TXP_1
DDI0_TXN_1
DDI0_TXP_2
DDI0_TXN_2
DDI0_TXP_3
DDI0_TXN_3
DDI0_AUXP
DDI0_AUXN
HV_DDI0_HPD
DDI0_DDC_SCL
DDI0_DDC_SDA
DDI0/DDI_B

MDSI
MDSI_A_CLKP AL2
MDSI_A_CLKN AM3
MDSI_C_CLKP AG13
MDSI_C_CLKN AG12
MDSI_A_DP_0 AN5
MDSI_A_DN_0 AN7
MDSI_A_DP_1 AJ15
MDSI_A_DN_1 AJ17
MDSI_A_DP_2 AJ7
MDSI_A_DN_2 AJ5
MDSI_A_DP_3 AJ10
MDSI_A_DN_3 AJ12
MDSI_C_DP_0 AG15
MDSI_C_DN_0 AG17
MDSI_C_DP_1 AG8
MDSI_C_DN_1 AG10
MDSI_C_DP_2 AG7
MDSI_C_DN_2 AG5
MDSI_C_DP_3 AE15
MDSI_C_DN_3 AE17

HDMI

HDMI_DDI_TX_P0 AA2
HDMI_DDI_TX_N0 AA3
HDMI_DDI_TX_P1 Y3
HDMI_DDI_TX_N1 Y1
HDMI_DDI_TX_P2 AD1
HDMI_DDI_TX_N2 AD3
HDMI_DDI_TX_P3 AC2
HDMI_DDI_TX_N3 AC3
AC7
AC5
HDMI_SCL_CPU C42
HDMI_SDA_CPU A42
HDMI_DET_CPU C38

3D3V_S0
R809 10KR2J-L-GP
SC_1018
RN802 Do Not Stuff DY

1.8V level
3.3V (default)

DDI1_TXP_0
DDI1_TXN_0
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_3
DDI1_TXN_3
DDI1_AUXP
DDI1_AUXN
DDI1_DDC_SCL
DDI1_DDC_SDA
HV_DDI1_HPD
DDI1/DDI_C

MIPI_I2C_SCL R53
MIPI_I2C_SDA R54

0214 change net name
0214 Adding R811
0216 Adding GPIO 43

GPIO_43
GPIO_42
MDSI_C_TE
MDSI_A_TE
T53 GPIO43_DSI_TE2
T55 GPIO42_FLASH_OVR
TP801
R811 0R402-DB-GP
ME_UNLOCK

MDSI_RCOMP AL5
R810 150R2F-4-L-GP

MDSI_A_TE:
If MIPI DSI is not implemented, leave them NC.

Layout Notes:
layout W/S=10/15mil, length <1000mil.

EDP

1D8V_S0
R807 100KR2J-4-GP

eDP_HPD_CPU
0222 Change PN
Q802 PJA138KA-GP
eDP_HPD_CPU_D
084.00138.0A31

HV_DDIX_HPD
It is required to enable internal 20k pull up resistor on the HV_DDI2_HPD signals by BIOS.

20170505 Add

1.8V (default)

eDP_TX_CPU_P0 AE12
eDP_TX_CPU_N0 AE13
eDP_TX_CPU_P1 AC15
eDP_TX_CPU_N1 AC17
AE10
AE8
AE5
AE7
eDP_AUX_CPU_P W17
eDP_AUX_CPU_N W15
eDP_HPD_CPU D B39
eDP_BLCTRL_CPU_E B41
eDP_BLEN_CPU C40
eDP_VDDEN_CPU_E C41
EDP_RCOMP_P AA5
EDP_RCOMP_N AA7

EDP_TXP_0
EDP_TXN_0
EDP_TXP_1
EDP_TXN_1
EDP_TXP_2
EDP_TXN_2
EDP_TXP_3
EDP_TXN_3
EDP_AUXP
EDP_AUXN
HV_DDI2_HPD
PNL0_BKLCTL
PNL0_BKLTEN
PNL0_VDDEN
EDP_RCOMP_P
EDP_RCOMP#
GEMINI-LAKE-GP
eDP/DDI_A

R801 100R2F-L-GP-U
#567247 #253 Table15-6
eDP signals disable guideline

Layout Notes:
Impedance 85 Ohm and space 20mil, length <400mil.

3D3V_S0 1D8V_S0
RN801 SRN2K2J-1-GP
eDP_BLCTRL_CPU_B
eDP_BLCTRL_CPU
Q803 LMBT3904LT1G-GP
eDP_BLCTRL_CPU_E
84.T3904.H11

3D3V_S0 1D8V_S0
RN803 SRN2K2J-1-GP
eDP_VDDEN_CPU_B
eDP_VDDEN_CPU
Q804 LMBT3904LT1G-GP
eDP_VDDEN_CPU_E
0213 change net
84.T3904.H11

15.1.2.5HPD Implementation
The hot-plug detect output from eDP* sink device is a 3.3V active high signal. Since the input on the processor is a 3.3V active low signal, a logic inversion circuit is required on the motherboard. Fi gure 15-7 shows an example of this implementation.

BOM1

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Title: CPU (DDI/EDP/MDSI)
Size: Custom
Document Number: LV315GM MB
Rev: -1
Date: Monday, April 09, 2018
Sheet 8 of 106

SSID = CPU

Blanking

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (MCSI/Camera)

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 9 of 106

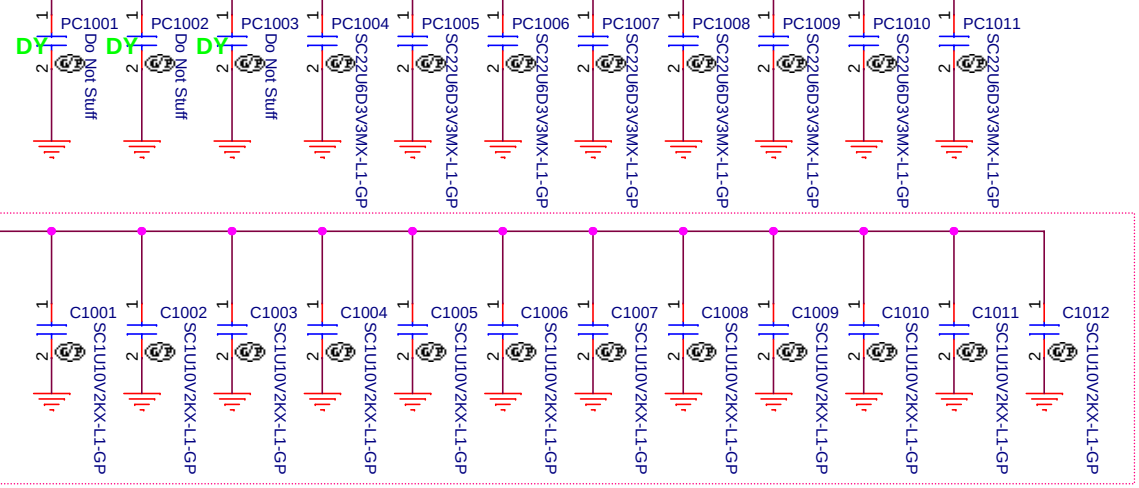
SSID = CPU

VCCGI

IccMax = 21 A

1V_CPU_VCGI

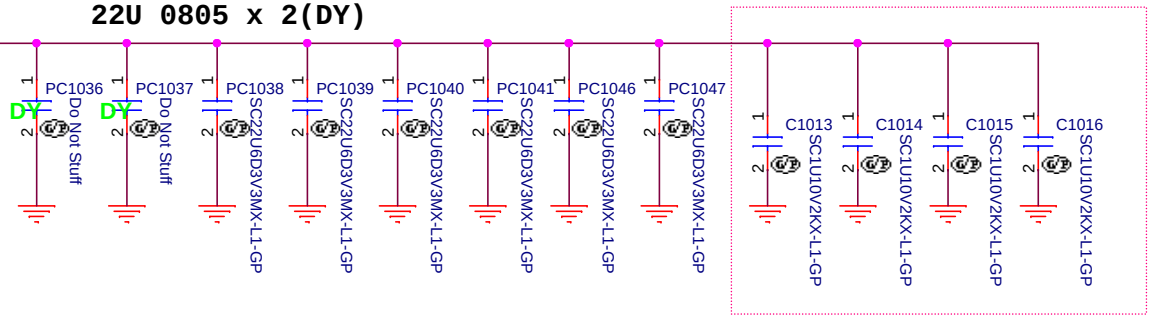
22U 0805 x 25
22U 0805 x 10(DY)



1V_CPU_VNN

VNN

22U 0805 x 10
22U 0805 x 2(DY)



BOM1

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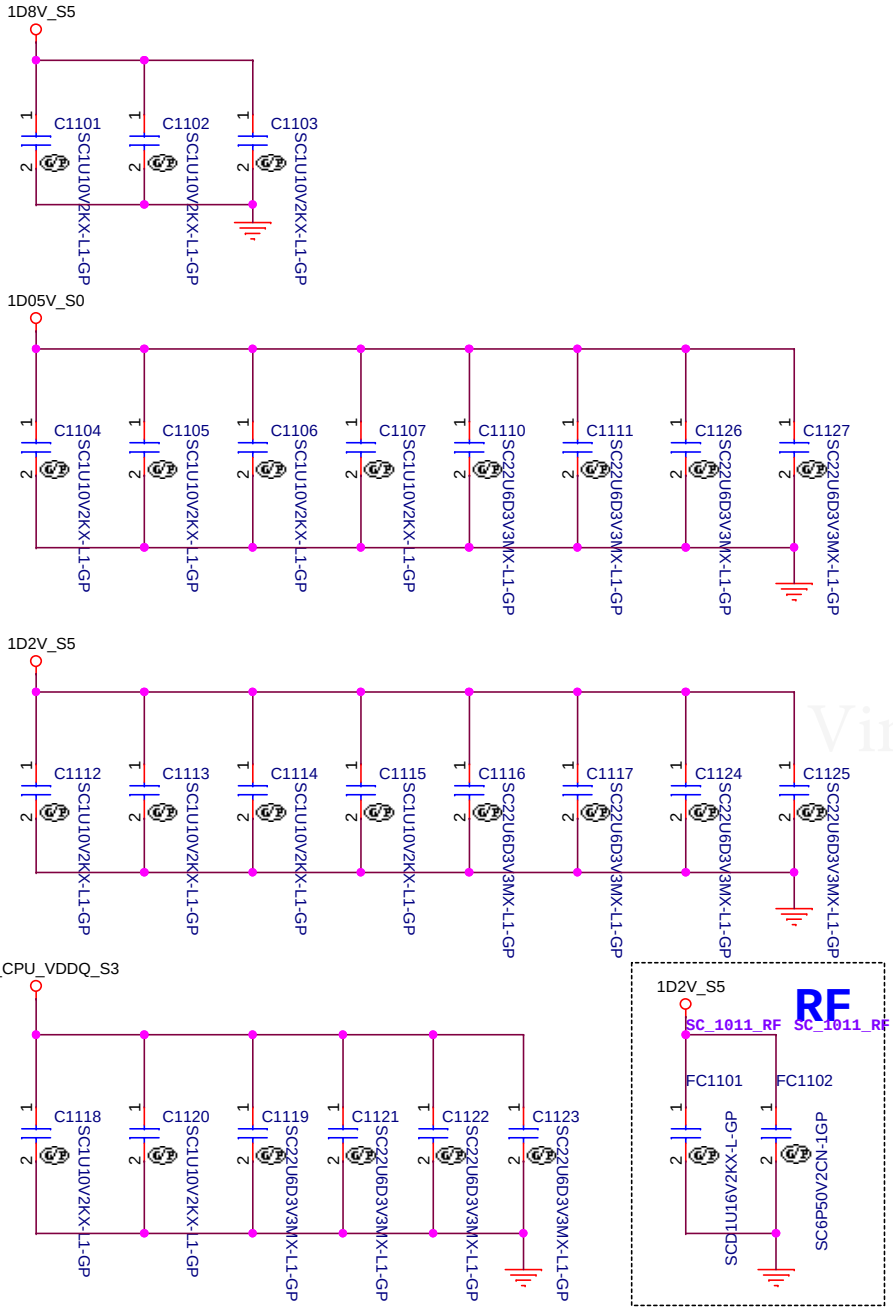
Title	*CPU (Power CAP1)*	
Size A4	Document Number **LV315GM MB**	Rev -1
Date: Monday, April 09, 2018	Sheet 10 of 106	

SSID = CPU



System Rail Name	Power Balls [GND]	Max L from Ball to nearest BSC [0402-1uF]			Max L from Ball to nearest ESC [0402 - 1uF]			Max L from Ball to nearest MLCC [0603 - 22uF *0805 - 22uF #0805 - 47uF]			Max L / R from Ball to VR Bulk [330uF_9mOhm]		
		Back Side Cap	BSC (nH)	Total (nH)	Top Side Edge Cap	ESC (nH)	Total (nH)	Top Side MLCC	MLCC (nH)	Total (nH)	Top Side Bulk	Bulk (nH)	(mΩ)
VCC_1P8V_A	V21,T25,V25,T23,V23,T21 [Y27,Y25,Y23,Y21,T27,V27,P21] AJ23,AG23[AJ25, AG25]	C417 C438 BSC_USB	1.36 0.714 1.29	0.673									
VCCIOA	AT27,AT28,AT29,AT25,AP31,AT 31,AP25 [AM29,AP27,AP28,AP28,AP33, AT33,AP23,AT23,AU28,AM31]	C429 C418	0.475 0.475	0.426	C202 C203	3.72 4.10	3.6	C601 C602	5.12 4.78	4.537			
VDDQ	AP36,AT36,AP38,AT38,AT35,AT 18,AP18,AP21,AT20,AT21,BA43 ,BA41,BA31,BA13,BA15,BA25 [AV39,AR39,AP35,AM38,AT33, AP33,AT23,AR17,AP23,AM23,A M21,AY43,AV33,BC31,AV23,AV 17,AV41,AY41,BC25,AY13,AY15]	C412 C428	0.475 0.523	0.223				*C816 *C817 *C820 *C821	2.06 4.10 1.62 3.30	0.496			
VCCRAM_1P05	AC35,AE35,AE38,AE36,AF28,A F27,AF38,AF36,AC33,AE33 [AE27,AF29,AF40,AG38,AJ38,A C29,AA35,AG35,AJ36,AF25]	C424	0.712					C608	2.89				
VCCRAM_1P05_IO	AA36,AA38,Y36,Y38,AC38,AC3 6 [V38,W39,AF40,W41,T38,AA35]	C405	0.989					C609	3.62				
VDD2_1P24_GLM	AP20,AL38,AL36 [AM21,AR17,AJ38, AJ36]	C415	0.619		C219	1.78		C610 C611	2.10 2.09	1.978			
VDD2_1P24_AUD_ISH_PLL	AM18,AL18 [AJ18, AL17]	C435	0.791					#C823 #C824	1.88 1.88	1.75			
VDD2_1P24_USB2	AJ20,AG18 [AG20, AJ18]	C433	0.747		C217	1.723		C623	2.13				
VDD2_1P24_MPHY	AC21,AE20,AE21,AF20,AF21 [AG20,AF18,AE18,AA23,AC23, AE23,AF23,AA21]	C442	0.667		C218	1.6		C624	2.08				
VDD2_1P24_DSI_CSI	AW12[AW10]							C625	2.22				

電容位置都要在1D2V_S5 Bottom層Power周圍
(預設DY)

BOM1

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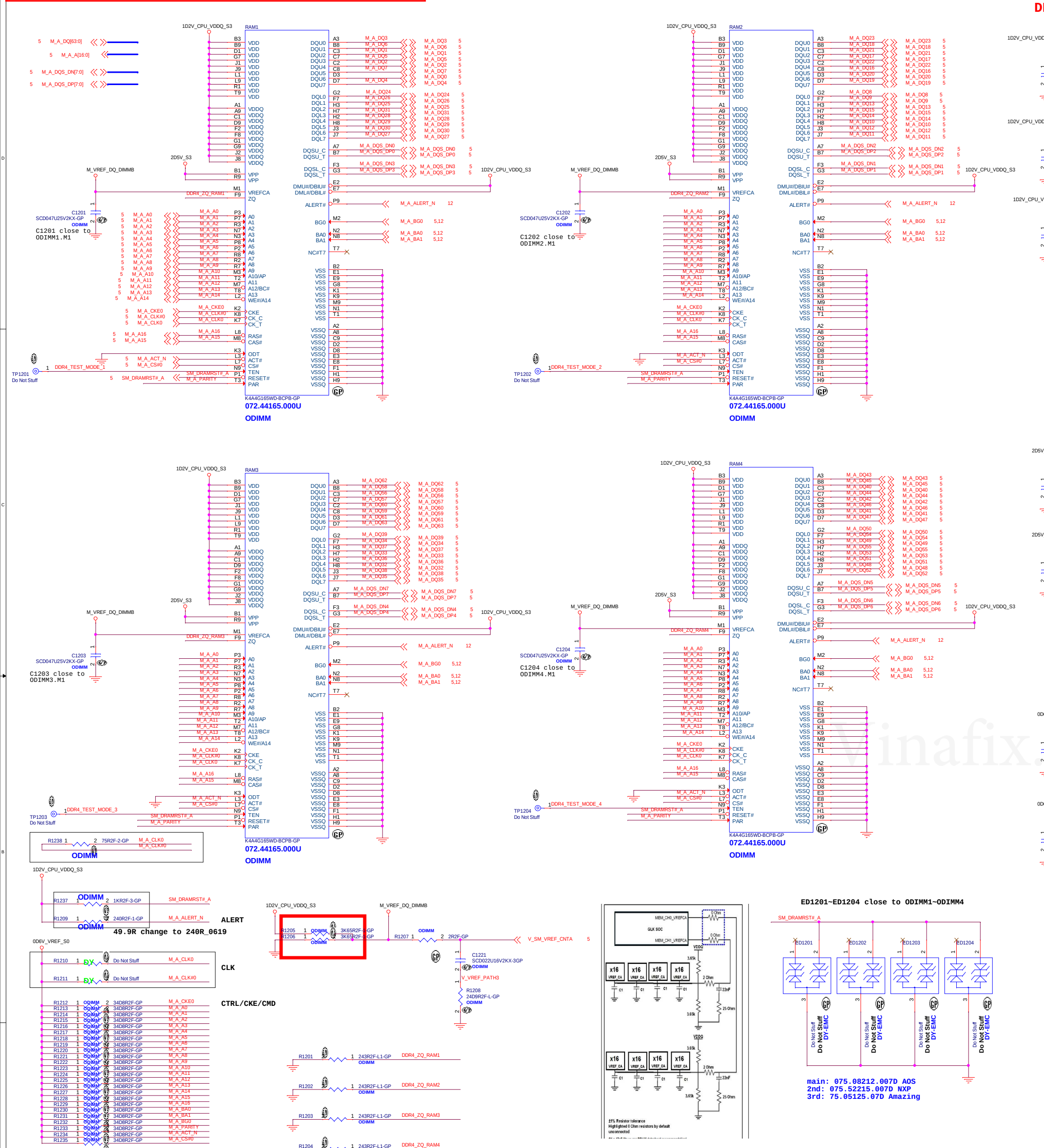
Title: **CPU (Power CAP2)**

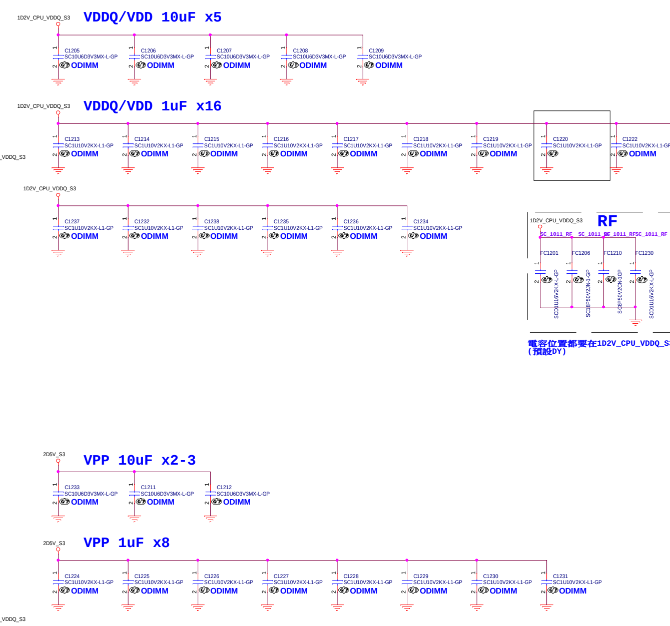
Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 11 of 106

Main Func = DDR4 On Board with Single Rank



DDR4 On Board RAM Power Decouple Cap



5.6.4.3 Routing Guidelines for ODT Signals

ODT Signals pins from SoC MEM_CH0_ODT0,MEM_CH0_ODT1 and MEM_CH1_ODT0,MEM_CH1_ODT1 left unconnected

DRAM ODT Pins are connected to Ground Refer Figure 5-15

Figure 5-15. ODT Signal Connection Diagram

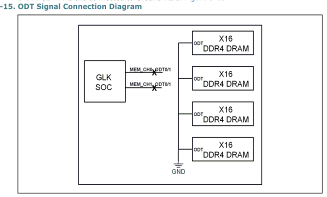


Table 5-14. DDR4 Memory Down (Double-T) Decoupling Recommendation

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR4 Memory Down 1x16 (4 device) Each channel	VDD/VDDQ	4 Per DRAM as close as possible to the VDD pins of DRAM	32x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	10x 10µF (0603)	
	Vpp	2 as near each x16 DRAM device as possible	16x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	5x 10µF (0603)	2
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	4x 10µF (0603)	2

Notes:
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 Memory Down will also be dependent on the DRAM memory requirements itself. Check with DRAM vendor for additional requirements or specifications.

[561280] 4.23.5 KBL-U DDR4 Memory Down Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)
		Distributed around the DRAM devices	5x 10µF (0603)
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)
		Distributed around the DRAM devices	4x 10µF (0603)

BOM1

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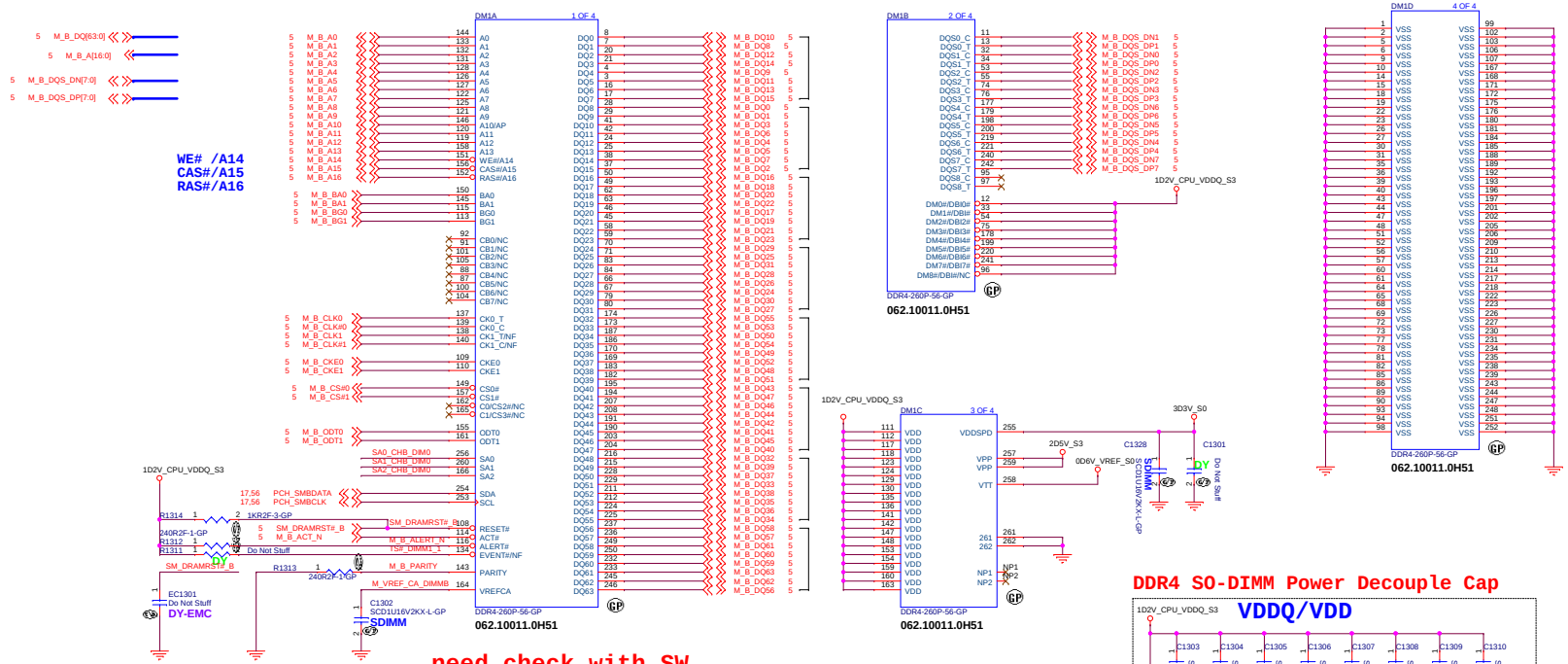
Title	DDR4_MEMORY DOWN	
Size A1	Document Number LV315GM MB	Rev -1
Date: Monday, April 09, 2018	Sheet 12 of 106	



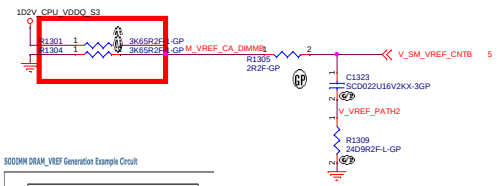


Figure 5-9. SODIMM DRAM_VREF Generation Example Circuit

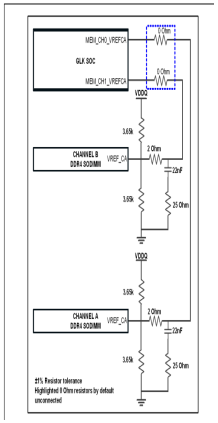


Table 5-9. SODIMM DDR4 VREF Layout Requirements

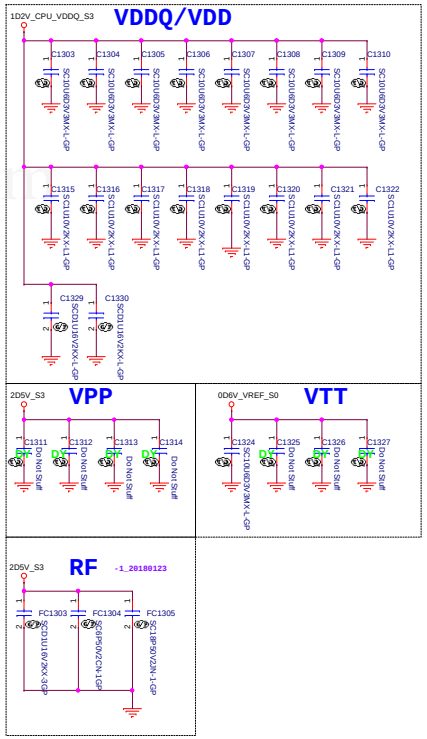
Parameter	Guidelines
VREF Width	15 mils / 0.381 mm in the main route
VREF Spacing	15 mils / 0.381 mm in the main route
MEM_CH0/1_VREFCA	Left unconnected, Provide "0" Ohm series Resistor with "No Stuff"
SODIMM ECC bit signals Pins and DM8 Pin	Should be pulled to VDDQ
VREFDQ	Left unconnected
SODIMM "ALERT" and "EVENT" Pins	Should be pulled to VDDQ WITH 240 Ohm Resistor
SODIMM "Parity" pin	Should be pulled down to GND WITH 240 Ohm Resistor

Table 5-10. DDR4 Decoupling Recommendation for SODIMM

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
			16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	2x - 4x 0.1µF (0402)	
	VTT	On the Vtt island	1x 22µF (0603) or 2x 10µF (0603)	3
				3

Notes:
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 SODIMM will also be dependent on the SODIMM requirements itself. Check with your SODIMM vendor for additional requirements or specifications.

DDR4 SO-DIMM Power Decouple Cap



電容位置都要在SODIMM 2D5V_S3 Power周圍（預設DY）

[561280] 4.23.6 KBL-U DDR4 SODIMM Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		1 placeholder	1x 330µF (7343)
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)
		Place these caps on the VTT plane close to SODIMM	1x 1µF (0402)
	VPP	DRAM Side	2x 10µF (0603)
		DRAM Side	2x 1µF (0402)
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)
		Place close to DIMM	1x 2.2µF (0402)

BOM1

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Title: DDR4_SODIMM

Size: A2 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 13 of 106

SSID = CPU

Blanking

BOM1

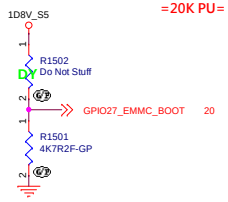
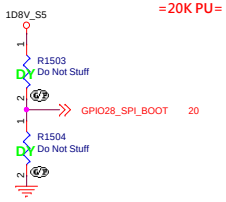
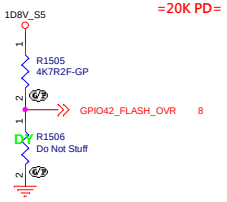
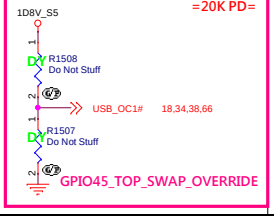
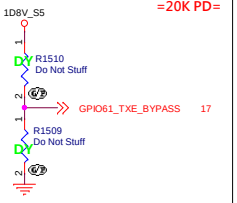
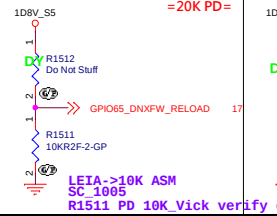
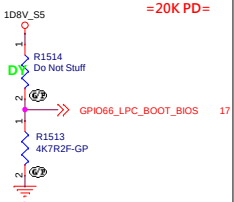
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

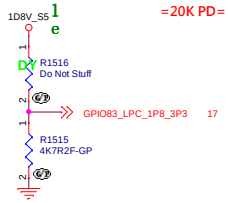
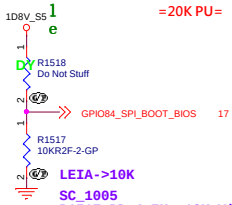
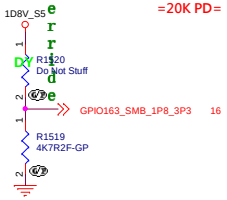
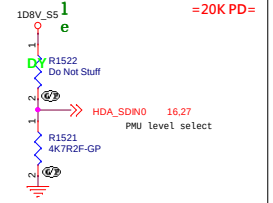
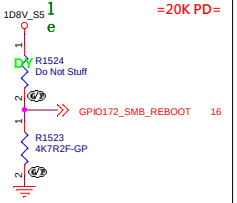
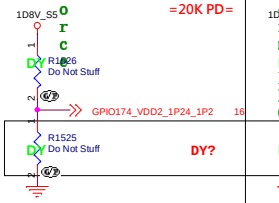
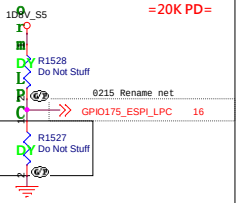
Title: *(Reserved)SODIMM3_SODIMM4*

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 14 of 106

SSID = STRAP

GPIO	GPIO_27	GPIO_28	GPIO_42	GPIO_45	GPIO_61	GPIO_65	GPIO_66
Schematic							
High	Enable =default=	Enable =default=	Override Normal	Enable =debug=	Enable	Force	Boot form LPC
Low	Disable 0213 Change setting	Disable	No Override	Disable =default=	Disable =default=	No Force =default=	No LPC =default=

GPIO	GPIO_83	GPIO_84	GPIO_163	GPIO_168	GPIO_172	GPIO_174	GPIO_175
Schematic							
High	Buffer set 1.8v	Disable boot from SPI	1.8v	1.8v	Enable	1.24v	eSPI mode
Low	Buffer set 3.3v =default=	Enable boot from SPI =default=	3.3v =default=	3.3v =default=	Disable =default=	1.20v =default=	LPC mode =default=

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable ***Note:*** If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Notes:*** 1. DnX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) ***Note:*** The board should strap this low and do not use otherwise
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_163	AVS_I2S1_WS_SYNC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.

BOM1

緯創資通 Wistron Corporation
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Title: CPU(STRAP)

Size: Custom | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 15 of 106

SSID = PCH

SPI ROM

25 SPI_MISO_ROM
25 SPI_MOSI_ROM
25 SPI_WP_ROM
25 SPI_HOLD_ROM
25 SPI_CS_CPU_N0
25 SPI_CLK_ROM

EMMC

63 EMMC_RCLK
63 EMMC_CLK
63 EMMC_D0
63 EMMC_D1
63 EMMC_D2
63 EMMC_D3
63 EMMC_D4
63 EMMC_D5
63 EMMC_D6
63 EMMC_D7
63 EMMC_CMD
63 EMMC_RST#

SB_remove EMMC_PWR_EN#_0803

STRAP

15 GPIO163_SMB_1P8_3P3
15 GPIO172_SMB_REBOOT
15 GPIO174_VDD2_1P24_1P2
15 GPIO175_ESPI_LPC

0215 Rename net

24 LPC_CLK_KBC
68 LPC_CLK_DBG
91 LPC_CLK_TPM

CPU1G — 7 OF 13 — GEMINI-LAKE-GP

AUDIO-AVS
C26 AVS_I2S0_MCLK
B25 AVS_I2S0_BCLK
C25 AVS_I2S0_WS_SYNC
C24 AVS_I2S0_SDI GPIO_159 / Delay Vref switch
B23 AVS_I2S0_SDO
M23 AVS_I2S1_MCLK
L21 AVS_I2S1_BCLK
J21 AVS_I2S1_WS_SYNC GPIO_163 / SMBus 1.8v / 3,3v mode
M21 AVS_I2S1_SDI GPIO_164 / Stall boot FSM for debug
P23 AVS_I2S1_SDO

GPIO163_SMB_1P8_3P3

HDA_BCLK A22 AVS_HDA_BCLK
HDA_SYNC C23 AVS_HDA_WS_SYNC
HDA_SDIN0 B21 AVS_HDA_SDI GPIO_168 / PMU 1.8v 3.3v mode
HDA_SDO C22 AVS_HDA_SDO
HDA_CODEC_RST# C21 AVS_HDA_RST#

TP1601

GPIO172_SMB_REBOOT B19 AVS_DMIC_CLK_A1
C20 AVS_DMIC_CLK_B1 GPIO_172 / SMbus no reboot
C19 AVS_DMIC_DATA_1
GPIO174_VDD2_1P24_1P2 C18 AVS_DMIC_CLK_AB2 GPIO_174 / VDD2 1.24v, 1.2v mode
GPIO175_ESPI_LPC A18 AVS_DMIC_DATA_2 GPIO_175 / eSPI, LPC mode

SDCARD
SDCARD_CLK L29
SDCARD_D0 M29
SDCARD_D1 P29
SDCARD_D2 M27
SDCARD_D3 P27
SDCARD_CMD L27
SDCARD_CD# L25
SDCARD_LVL_WP P25
SDCARD_PWR_DWN# L23
SDCARD_RCOMP J25

1.8V / 3.3V
1.8V
1.8V / 3.3V
1.8V

intel PDG (567247 ver1.2)
Deleted SD Card Section

LPC/eSPI
LPC_CLKOUT0 C37 LPC_CLK_KBC_R
LPC_CLKOUT1 A38 LPC_CLK_DBG_R
LPC_AD0 A34 LPC_AD_CPU_P0
LPC_AD1 C34 LPC_AD_CPU_P1
LPC_AD2 B35 LPC_AD_CPU_P2
LPC_AD3 C35 LPC_AD_CPU_P3
LPC_CLKRUN# C33 LPC_CLKRUN#_CPU
LPC_FRAME# B33 LPC_FRAME#_CPU
LPC_SERIRQ B37 LPC_SERIRQ_CPU

R1603 33R2J-2-GP
RN1601 SRN33J-5-GP-U
SC_1018
R1602.R1624->RN1601
Debug

0213
Rename LPC_SERIRQ PIN to LPC_SERIRQ_CPU
Rename LPC_CLKRUN# PIN to LPC_CLKRUN_CPU#

eMMC
EMMC_CLK J13 EMMC_CLK
EMMC_RCLK L15 EMMC_RCLK
EMMC_D0 M19 EMMC_D0
EMMC_D1 H19 EMMC_D1
EMMC_D2 J19 EMMC_D2
EMMC_D3 P17 EMMC_D3
EMMC_D4 P19 EMMC_D4
EMMC_D5 J15 EMMC_D5
EMMC_D6 L17 EMMC_D6
EMMC_D7 M17 EMMC_D7
EMMC_CMD M13 EMMC_CMD
EMMC_RST# U44 EMMC_RST#
EMMC_PWR_EN# G51 EMMC_PWR_EN#
EMMC_RCOMP L13 EMMC_RCOMP

SB_Add TP1602_0803
TP1602

Layout Note:
W/S=10/8, length <500 mil
R1605
200R2F-L-GP
0213
Rename net.
Moving Res to CPU side

FAST_SPI
FST_SPI_CLK B29 SPI_CLK_CPU
FST_SPI_MOSI_IO0 B31 SPI_SI_CPU
FST_SPI_MISO_IO1 C30 SPI_SO_CPU
FST_SPI_IO2 A30 SPI_WP_CPU
FST_SPI_IO3 C29 SPI_HOLD_CPU
FST_SPI_CS0# C31 SPI_CS_CPU_N0
FST_SPI_CS1# C32

R1604 0R402-DB-GP SPI_CLK_ROM
R1611 0R402-DB-GP SPI_MOSI_ROM
R1612 0R402-DB-GP SPI_MISO_ROM
R1613 0R402-DB-GP SPI_WP_ROM
R1614 0R402-DB-GP SPI_HOLD_ROM

24,91 LPC_SERIRQ — R1621 0R0402-PAD LPC_SERIRQ_CPU
91 LPC_CLKRUN# — R1618 0R0402-PAD LPC_CLKRUN#_CPU
24,68,91 LPC_FRAME# — R1623 0R0402-PAD LPC_FRAME#_CPU

SC_1023
24,68,91 LPC_AD0 — R1622 0R0402-PAD LPC_AD_CPU_P0
24,68,91 LPC_AD1 — R1617 0R0402-PAD LPC_AD_CPU_P1
24,68,91 LPC_AD2 — R1620 0R0402-PAD LPC_AD_CPU_P2
24,68,91 LPC_AD3 — R1619 0R0402-PAD LPC_AD_CPU_P3

3D3V_S0
SC_PU 0926
EMMC_PWR_EN# R1630 20KR2J-L2-GP
24 LPC_CLKRUN#_CPU — LPC_CLKRUN#_CPU R1625 10KR2J-L-GP
PU 0516
LPC_FRAME#_CPU R1631 Do Not Stuff
LPC_SERIRQ_CPU R1632 Do Not Stuff
-1_1212
reserve pull high resistor R1631.R1632 for leakage

LPC_CLK_KBC
SC_1011_RF
FC1601
SC6P50V2CN-1GP

Change location next phase
Location FC1601 change to C1601_0712

27 HDA_SYNC
27 HDA_BCLK
27 HDA_SDO
15,27 HDA_SDIN0
27 HDA_CODEC_RST#

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (AVS/EMMC/SD/LPC/ESPI)
Size: A3 | Document Number: LV315GM MB | Rev: -1
Date: Monday, April 09, 2018 | Sheet 16 of 106

SSID = CPU

SC_1005
R1720 PH 4.7K_Vick verify ok

Del R1705.R1706 next stage (SB)
SB:Del R1705.R1706_0712

CPU1F

6 OF 13

LPSS_I2C
LPSS_SPI
LPSS_UART
LPSS SMBus
CNVI

GEMINI-LAKE-GP

15 GPIO83_LPC_1P8_3P3
15 GPIO84_SPI_BOOT_BIOS
15 GPIO61_TXE_BYPASS
15 GPIO65_DNXFW_RELOAD
15 GPIO66_LPC_BOOT_BIOS

For Touch Pad 1.8v
I2C_TP_CLK
I2C_TP_DATA

3D3V_S5
R1701 1KR2J-1-GP
3.3v
I2C7_TP_CLK
I2C7_TP_DATA

CRT 3.3v
SMB_ALERT#_CPU
MEM_SMBCLK
MEM_SMBDATA

3.3V / 1.8V

SIO_I2C0_SCL
SIO_I2C0_SDA
SIO_I2C1_SCL
SIO_I2C1_SDA
SIO_I2C2_SCL
SIO_I2C2_SDA
SIO_I2C3_SCL
SIO_I2C3_SDA
SIO_I2C4_SCL
SIO_I2C4_SDA
SIO_I2C5_SCL
SIO_I2C5_SDA
SIO_I2C6_SCL
SIO_I2C6_SDA
SIO_I2C7_SCL
SIO_I2C7_SDA
SMB_ALERT#
SMB_CLK
SMB_DATA

GPIO_177 / WC_PRESENT

GPIO_79 / spare 6
GPIO_83 / LPC 1.8v 3.3v mode
GPIO_80 / EXI Boot
GPIO_81 / Halts early boot for debug
GPIO_84 / SPI boot BIOS
GPIO_89 / Stall boot FSM for debug
GPIO_85 / Enable metal password
GPIO_86 / SVID Enable
GPIO_87 / XTAL

SIO_SPI_0_CLK
SIO_SPI_0_TXD
SIO_SPI_0_RXD
SIO_SPI_0_FS0
SIO_SPI_0_FS1
SIO_SPI_2_CLK
SIO_SPI_2_TXD
SIO_SPI_2_RXD
SIO_SPI_2_FS0
SIO_SPI_2_FS1
SIO_SPI_2_FS2

GPIO83_LPC_1P8_3P3
SIO_SPI_0_FS0
XDP_BOOT_HALT
GPIO84_SPI_BOOT_BIOS
SIO_SPI_2_FS0
SIO_SPI_2_FS1
R1709 10KR2J-L-GP
TP1701
R1720 4K7R2J-L-GP
R1721 4K7R2J-L-GP
R1722 10KR2J-L-GP
1D8V_S5

SC_1003_reserve
-1_1222 ASM
0213 Change net
0216 Del GPIO62

GPIO_61 / CSE ROM
GPIO_62 / RTC clock time bypass
GPIO_65 / DNX FW
GPIO_66 / LPC boot BIOS

SIO_UART0_TXD
SIO_UART0_RXD
SIO_UART0_RTS#
SIO_UART0_CTS#
SIO_UART2_TXD
SIO_UART2_RXD
SIO_UART2_RTS#
SIO_UART2_CTS#

GPIO61_TXE_BYPASS
GPIO65_DNXFW_RELOAD
GPIO66_LPC_BOOT_BIOS
R1702 DY
R1703 DY
Do Not Stuff
TP1703 XDP_UART_RXD
TP1702 XDP_UART_TXD

0216 DY
0216 Change Res link

-1_1123

CLKIN_XTAL_LCP_L
EL1701 Do Not Stuff DY-EMC
CLKIN_XTAL_LCP
EC1701 Do Not Stuff DY-EMC
ER1701 Do Not Stuff DY-EMC

SC_0914
CLKIN_XTAL_LCP reserved R.C.L

SB_0728
remove CNVi function

CNVi Companion RF
M.2 module

CNV_WGR_CLK_P
CNV_WGR_CLK#
CNV_WGR_D0_P
CNV_WGR_D0#
CNV_WGR_D1_P
CNV_WGR_D1#
CNV_WT_CLK_P
CNV_WT_CLK#
CNV_WT_D0_P
CNV_WT_D0#
CNV_WT_D1_P
CNV_WT_D1#
CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
CNV_RF_RESET#
CNV_WT_RCOMP

GPIO_191 / eSPI Flash Sharing Mode
GPIO_192 / Spare 5
GPIO_193 / XTAL startup
GPIO_194 / Spare 7
GPIO_195 / Spare 8
GPIO_196 / Spare 9

61 CLKIN_XTAL_LCP_L
61 XTAL_CLKREQ

from module

SB_0810_Add CNVi TP
TP1704 CNV_BRI_DT
TP1705 CNV_BRI_RSP
TP1706 CNV_RGI_DT
TP1707 CNV_RGI_RSP
TP1708 CNV_RF_RESET#
R1704 CNV_WT_RCOMP 150R2F-1-GP

If CNVi interface is not used, Left open for all signals except CNV_WT_RCOMP_SB_0728

3D3V_S5
3D3V_S0
R1707 1KR2J-1-GP
R1708 1KR2J-1-GP
RN1709 SRN10KJ-5-GP
Q1705 SSM6N7002KFU-GP
MEM_SMBDATA
MEM_SMBCLK
PCH_SMBDATA 13,56
PCH_SMBCLK 13,56
075.67002.007C

For Touch Pad
RN1703 Do Not Stuff DY
Q1704 Do Not Stuff DY
RN1708 Do Not Stuff DY
I2C_TP_DATA
I2C_TP_CLK
TP_I2C_CLK_D
TP_I2C_DATA_D
65 TP_I2C_DATA_D
65 TP_I2C_CLK_D

RN1711 SRN4K7J-8-GP
RN1712 SRN2K2J-1-GP
Q1706 SSM6N7002KFU-GP
I2C7_TP_DATA
I2C7_TP_CLK
075.67002.007C

SB -> DY RN1703.RN1708.Q1704
Change RN1712 from 4K7 to 2K2 (vendor suggestion)
ASM RN1711.RN1712.Q1706
for Q1704 circuit leakage issue

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (I2C/SMB/SPI/UART/CNVI)
Size: A3
Document Number: LV315GM MB
Rev: -1
Date: Monday, April 09, 2018
Sheet 17 of 106

SSID = PCH

USB3.0 Type A

HDD

TypeC

LAN

WLAN

M.2 PCIe SSD

BT

RGB camera

CARD READER

USB2.0 Port2

USB2.0 Port1

TypeC

check clock mapping_mi0414

TX CAP Close to CONN_0531

SB_0721

SB_0821 R1809 change from 100K to 10K

ODD

3.3V / 1.8V

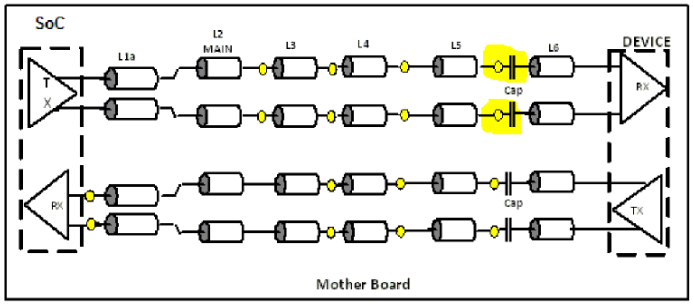
TOUCH PANEL

Finger print

mi 0419
USB_OC pin
port1(AOU)&PORT2???

ZZ.00CPU.131

Figure 9-8. PCI Express* Device Down Topology



PCIE_WAKE[3:0]_N	I	V1P8/V3P3	PCIe* Wake Signals
PCIE_CLKREQ[3:0]_N	I/O	V1P8/V3P3	**PCIE Clock Request**: Used for devices that need to request one of the four output clocks. Each clock request maps to the matching clock output (for example, PCI_CLKREQ[0] maps to PCIE_CLKP/N[0]). These signals are multiplexed and may be used by other functions.

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB3/USB2)

Size: A2 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 18 of 106

SSID = PCH

APS debug port

1.8v

32kHZ for CNVi pin50

need check with SW

SC_0922
XTAL add 33R

32.768 kHz

19.2 MHz

SB_18pF

	C1803(Cg)	C1804(Cd)
NDK 082.30003.0221	18pF	18pF
EPSON 082.30003.0191	18pF	18pF

main: 082.30003.0221
2nd: 082.30003.0191

main: 082.30001.0181
2nd: 082.30001.0171
3th: 082.30039.0051

19.2MHz SPEC
TPPM ± 30 ppm
CLOAD(MAX) 12pF

	C1901	C1902
HARMONY 082.30001.0181	15pF	15pF
TXC 082.30001.0171	15pF	15pF
HOSONIC 082.30039.0051	15pF	15pF

Layout Note:
place on bottom side

Do Not Stuff

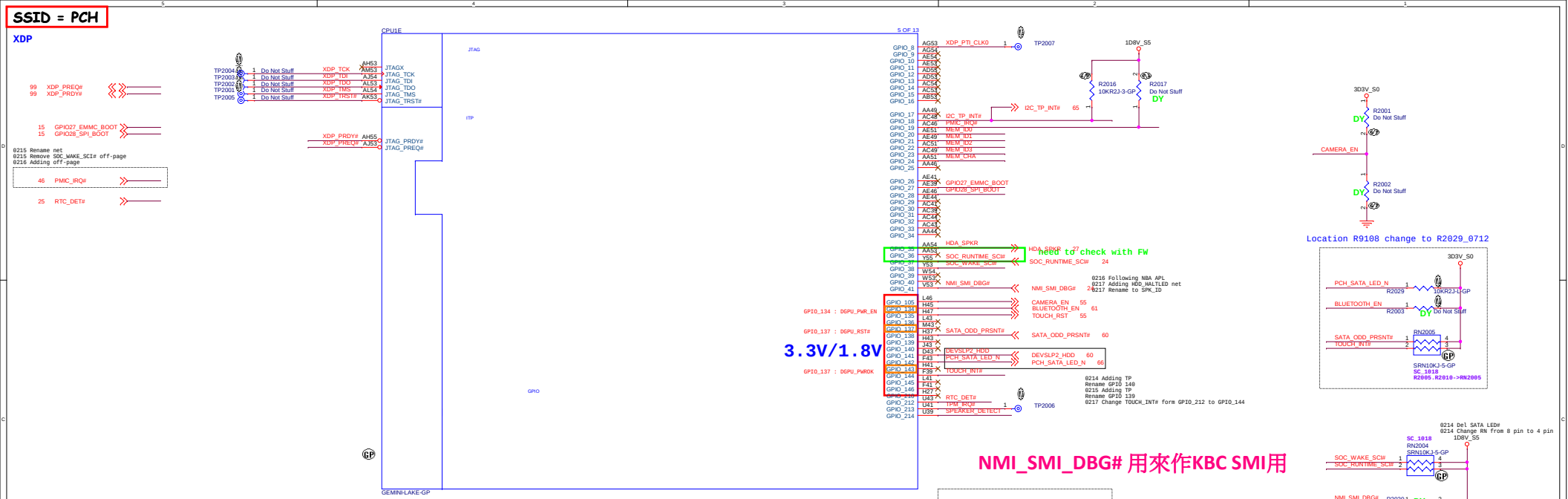
BOM1

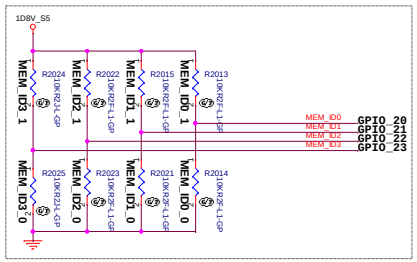
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

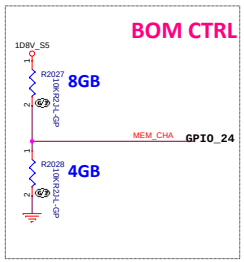
Title: CPU (PMU/PMC/SVID/RTC/MISC)

Size: A3 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 19 of 106







SB_MODIFY_0711

-1_MODIFY_20180125

0=L,1=H

RAMID	MD_ID3	MD_ID2	MD_ID1	MD_ID0	LENOVO PN	VENDOR PN	WISTRON PN	VENDOR	Density
0	0	0	0	0			SO-DIMM Only	SO-DIMM Only	PD
1	0	0	0	1			SM30L08877	MICRON	4GB
2	0	0	1	0			SM30N71798	SAMSUNG	4GB
3	0	0	1	1			SM30L08875	SK HYNIX	4GB
4	0	1	0	0					
5	0	1	0	1					

13.2 SATA Signal Description

13.2.1 SATA Signal Groups

Table 13-3. SATA Signal Groups

Group	Signal Name	Direction/ Reference	Description
GPIO	**SATA_GP0** (GPIO_138)	I/O V1P8A	Serial ATA Port [0] General Purpose.
	SATA_GP1 (GPIO_139)	I/O V1P8A	Serial ATA Port [1] General Purpose.
	SATA_DEVSLP0 (GPIO_140)	O V1P8A	Serial ATA Port [0] Device Sleep.
	SATA_DEVSLP1 (GPIO_141)	O V1P8A	Serial ATA Port [1] Device Sleep.
	SATA_LED_NSATA_LED_N (GPIO_142)	O V1P8A	LED
SATA Transmit	**SATA_P0_TXN** **SATA_P0_TXP** **SATA_P1_USB3_P5_TXN** **SATA_P1_USB3_P5_TXP**	O V1P24A	Differential Transmit Pair.
SATA Receive	**SATA_P0_RXN** **SATA_P0_RXP** **SATA_P1_USB3_P5_RXN** **SATA_P1_USB3_P5_RXP**	I V1P24A	Differential Receive Pair.

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO/JTAG/ITP)

Size: A2 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 20 of 106

SSID = CPU

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Reserved)

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 21 of 106

SSID = CPU

Blanking

BOM1

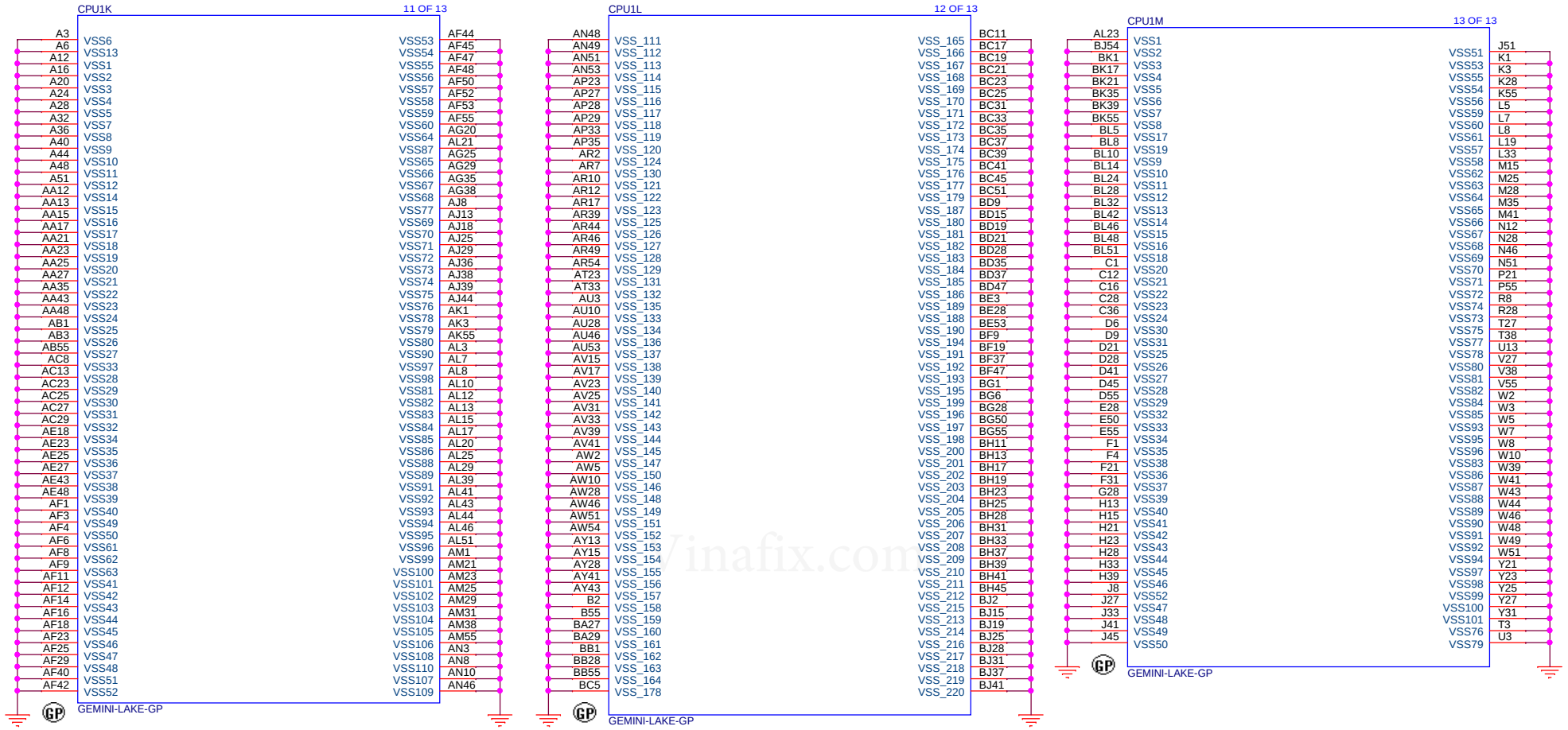
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Reserved)

Size: A4 | Document Number: LV315GM MB | Rev: -1

Date: Friday, March 30, 2018 | Sheet 22 of 106

SSID = CPU



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VSS

Size: Custom | Document Number: LV315GM MB | Rev: -1

Date: Friday, March 30, 2018 | Sheet 23 of 106

SSID = KBC

Model_ID_BOM Ctrl

PCB VERSION A/D(PIN58)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LV315GM (non TYPE-C)	100.0K	10.0K 64.10025.6DL	3.0V
LV315GM (TYPE-C)	100.0K	20.0K 64.20025.1.6L	2.75V
NA	100.0K	33.0K 64.330251.0L	2.48V
NA	100.0K	47.0K 64.470251.6DL	2.24V
NA	100.0K	64.9K 64.649251.6DL	2.0V
NA	100.0K	76.8K 64.768251.6DL	1.87V
NA	100.0K	215.0K 64.215351.6DL	1.048V

BOM Ctrl_Model

-1_1229

SPEC: ADT PWR Detection Function V1 3

PCB VERSION

PCB VERSION A/D(PIN58)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-1M	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

BOM Ctrl_Model

DELTA Model:ADP65FD BB-PD03 ADP

PIN 3 PIN 1 PIN 2

TABLE	
PIN 1	SIGNAL 287~ohm(1% TOLERANCE)
PIN 3	
PIN 2	

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.109V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.234V < ID <= 0.663V	45W

SA

Prevent BIOS data loss solution

84.03906.G11

Do Not Stuff

KBC_PWR_supply at PSL mode.

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

84.03415.A31

84.2N702.J31

EC_GPIO47 High Active

84.2N702.J31

Do Not Stuff
DY-EMC

EC GPIO PH

-1_20180104
RN2403 change from 66.47236.04L
4k7 to 66.22236.04L 2k2 for SMBUS
rise time and falling time fail

SC_0913
R2449 LID_CLOSE# PH 3D3V_AUX_KBC
Change to PH 3D3V_AUX_S5

EC GPIO PL

R2418 ASM
R2420 DY
DG07

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR
Button shut down
(2) 8sec: KBC reset

main: 075.08212.007D AOS
2nd: 075.52215.007D NXP
3rd: 75.05125.07D Amazing

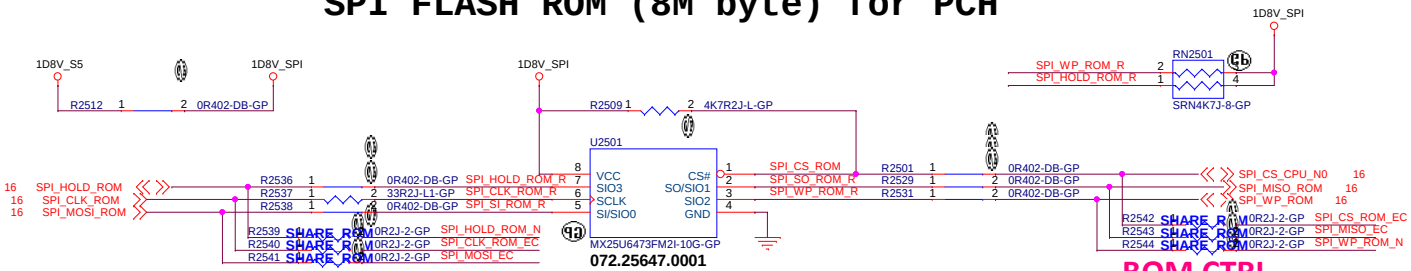
071.05146.M001/SL80N9098BAA品Tray 071.GL835.0003/SL80Q58977AA品Taping
短期:現PSE需求LV315 GM I/O BD(17A62-1)用071.05146.M001/SL80N9098BAA
長期:REALTEK已修改071.05146.M001/SL80N9098BAA為Taping，等Tray盤消耗完，建替代

071.00285.0C0G

Wistron Corporation		
KBC NPCE285		
LV315GM MB		-1

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



BOM CTRL

BIOS
SDV DIP

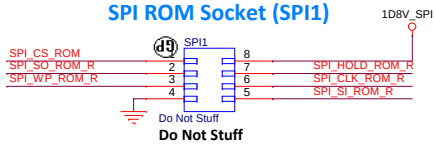
BOM CTRL

LKL-1

SDV ASM

Co-Layout Design on U2501

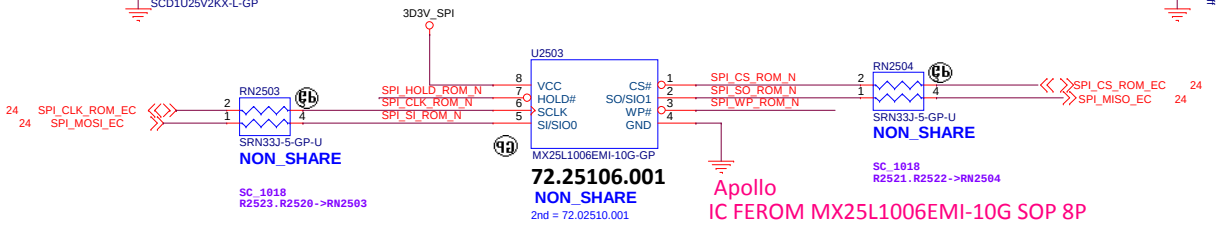
SPI ROM Socket (SPI1)



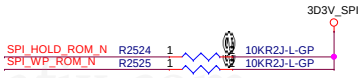
Do Not Stuff

DY

128k byte for FEROM



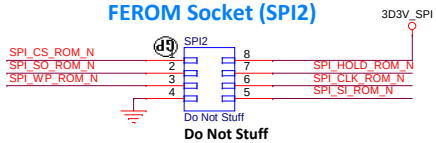
FEROM
SDV DIP



SDV ASM

Co-Layout Design on U2503

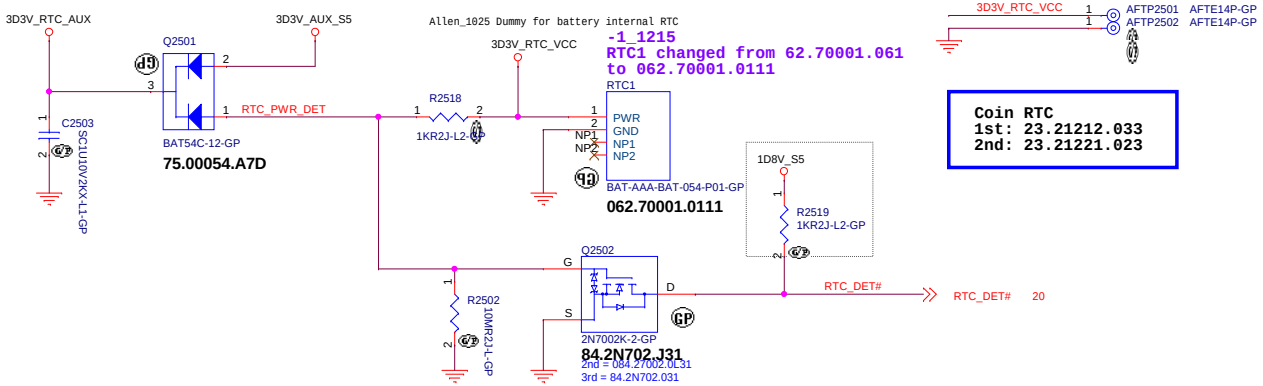
FEROM Socket (SPI2)



Do Not Stuff

DY

SSID = RBAT

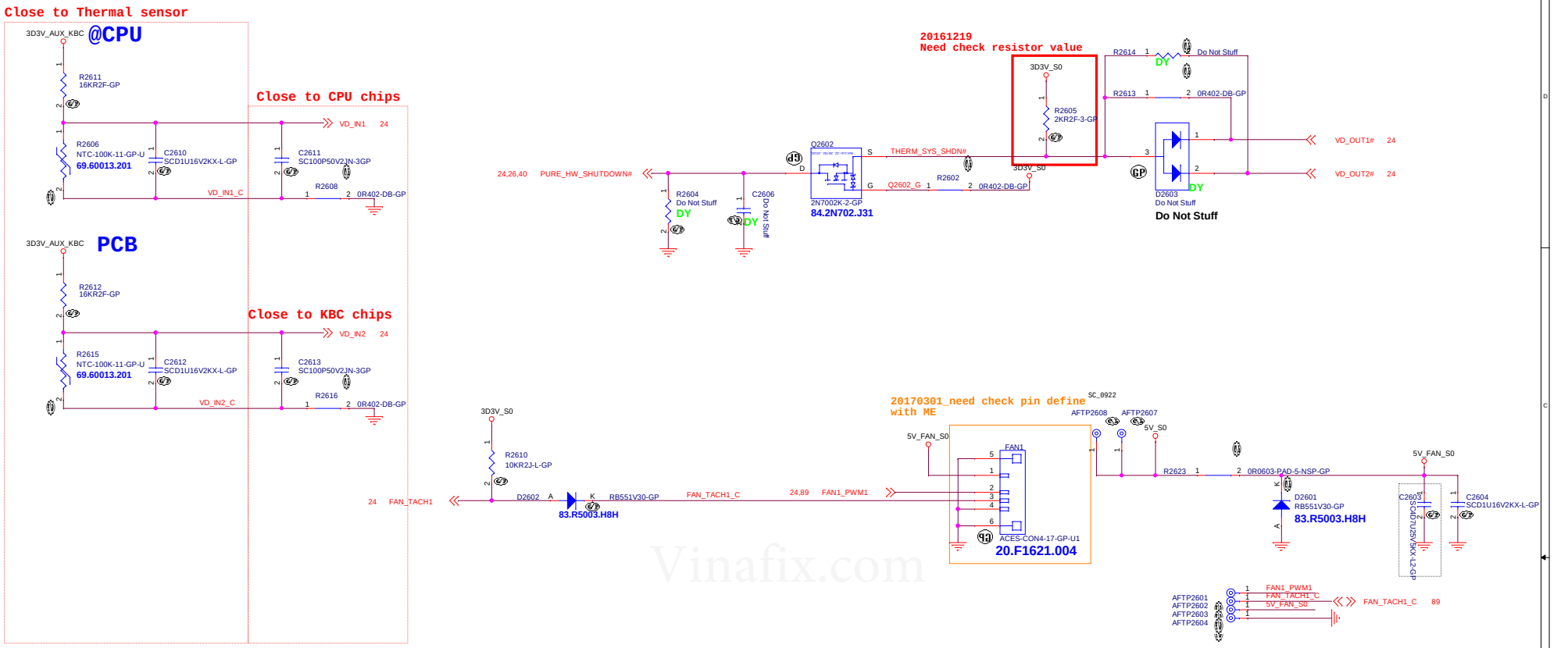


BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash/RTC	
Size A3	Document Number LV315GM MB	Rev -1
Date: Monday, April 09, 2018	Sheet 25 of 106	

Main Func = Thermal Sensor



PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

OBS REASON: Cost of 74.00331.C2F is not competitive. Pls use BCD 74.00331.I2F and TI 74.00331.A2F for instead.

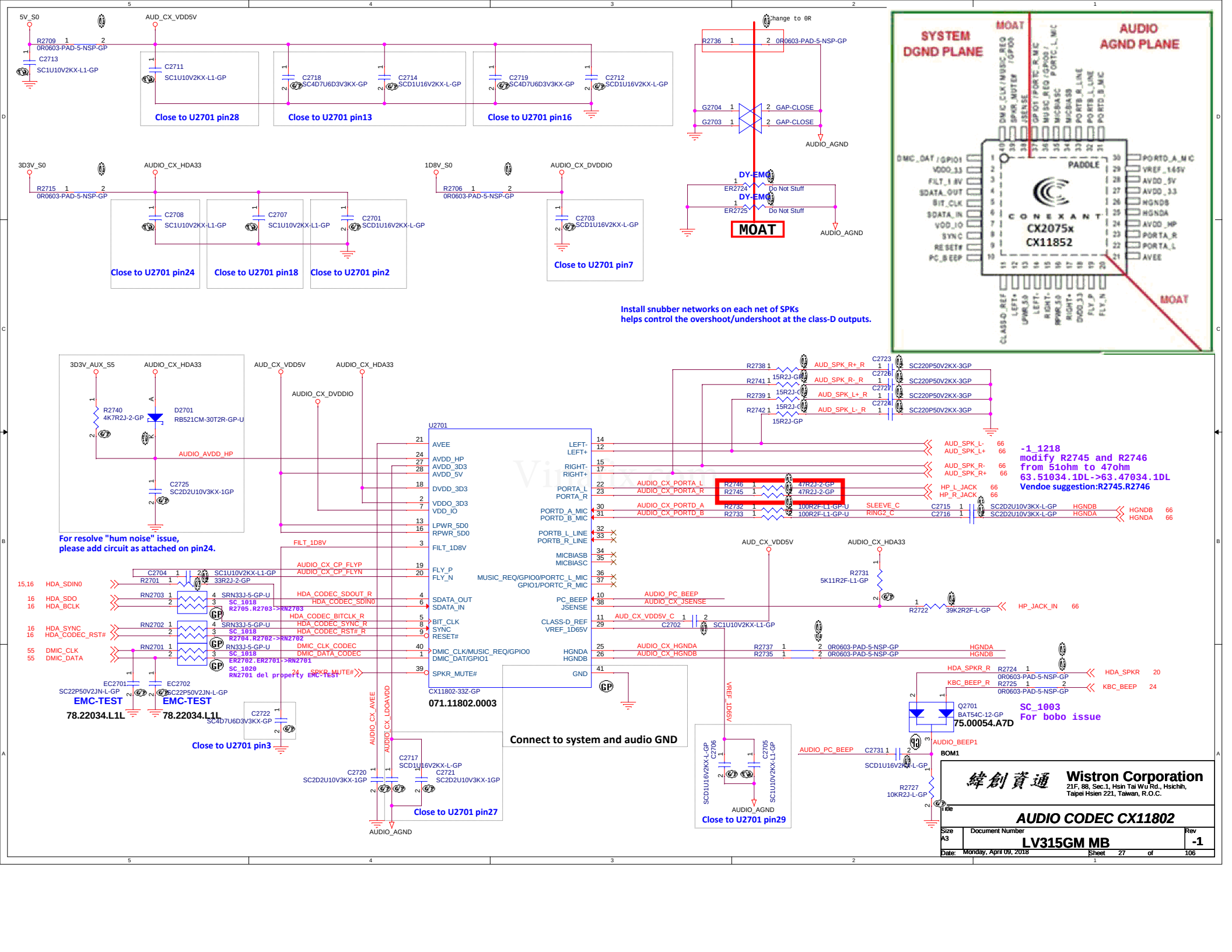
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/FAN

Size: Custom | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 26 of 106


5V_S0
AUD_CX_VDD5V
R2709 1 2 0R0603-PAD-5-NSP-GP
C2713 SC1U10V2KX-L1-GP
C2711 SC1U10V2KX-L1-GP
C2718 SC4D7U6D3V3KX-GP
C2714 SC1U16V2KX-L-GP
C2719 SC4D7U6D3V3KX-GP
C2712 SC1U16V2KX-L-GP
Close to U2701 pin28
Close to U2701 pin13
Close to U2701 pin16
Change to 0R
R2736 1 2 0R0603-PAD-5-NSP-GP
G2704 1 2 GAP-CLOSE
G2703 1 2 GAP-CLOSE
AUDIO_AGND
DY-EMC
ER2724 Do Not Stuff
ER2725 Do Not Stuff
MOAT
AUDIO_AGND
SYSTEM DGND PLANE
MOAT
AUDIO AGND PLANE
PADDLE
CONEXANT
CX2075x
CX11852
MOAT
3D3V_S0
AUDIO_CX_HDA33
R2715 1 2 0R0603-PAD-5-NSP-GP
C2708 SC1U10V2KX-L1-GP
C2707 SC1U10V2KX-L1-GP
C2701 SC1U16V2KX-L-GP
Close to U2701 pin24
Close to U2701 pin18
Close to U2701 pin2
1D8V_S0
AUDIO_CX_DVDDIO
R2706 1 2 0R0603-PAD-5-NSP-GP
C2703 SC1U16V2KX-L-GP
Close to U2701 pin7
Install snubber networks on each net of SPKs
helps control the overshoot/undershoot at the class-D outputs.
3D3V_AUX_S5
AUDIO_CX_HDA33
R2740 4K7R2J-2-GP
D2701 RB521CM-30T2R-GP-U
AUDIO_AVDD_HP
C2725 SC2D2U10V3KX-1GP
For resolve "hum noise" issue,
please add circuit as attached on pin24.
AUD_CX_VDD5V
AUDIO_CX_HDA33
AUDIO_CX_DVDDIO
U2701
CX11802-33Z-GP
071.11802.0003
AVEE
AVDD_HP
AVDD_3D3
AVDD_5V
DVDD_3D3
VDDO_3D3
VDD_IO
LPWR_5D0
RPWR_5D0
FILT_1D8V
FLY_P
FLY_N
SDATA_OUT
SDATA_IN
BIT_CLK
SYNC
RESET#
DMIC_CLK/MUSIC_REQ/GPIO0
DMIC_DAT/GPIO1
SPKR_MUTE#
LEFT-
LEFT+
RIGHT-
RIGHT+
PORTA_L
PORTA_R
PORTD_A_MIC
PORTD_B_MIC
PORTB_L_LINE
PORTB_R_LINE
MICBIASB
MICBIASC
MUSIC_REQ/GPIO0/PORTC_L_MIC
GPIO1/PORTC_R_MIC
PC_BEEP
JSENSE
CLASS-D_REF
VREF_1D65V
HGNDA
HGNDB
GND
R2738 15R2J-GP AUD_SPK_R+_R C2723 SC220P50V2KX-3GP
R2741 15R2J-GP AUD_SPK_R-_R C2726 SC220P50V2KX-3GP
R2739 15R2J-GP AUD_SPK_L+_R C2727 SC220P50V2KX-3GP
R2742 15R2J-GP AUD_SPK_L-_R C2724 SC220P50V2KX-3GP
AUD_SPK_L- 66
AUD_SPK_L+ 66
AUD_SPK_R- 66
AUD_SPK_R+ 66
HP_L_JACK 66
HP_R_JACK 66
-1 1218
modify R2745 and R2746
from 51ohm to 47ohm
63.51034.1DL->63.47034.1DL
Vendoe suggestion:R2745.R2746
AUDIO_CX_PORTA_L
AUDIO_CX_PORTA_R
R2746 47R2J-2-GP
R2745 47R2J-2-GP
AUDIO_CX_PORTD_A
AUDIO_CX_PORTD_B
R2732 100R2F-L1-GP-U
R2733 100R2F-L1-GP-U
SLEEVE_C
RING2_C
C2715 SC2D2U10V3KX-L-GP HGNDB
C2716 SC2D2U10V3KX-L-GP HGNDA
HGNDB 66
HGNDA 66
AUD_CX_VDD5V
AUDIO_CX_HDA33
R2731 5K11R2F-L1-GP
R2722 39K2R2F-L-GP
HP_JACK_IN 66
AUDIO_PC_BEEP
AUDIO_CX_JSENSE
AUD_CX_VDD5V_C
C2702 SC1U10V2KX-L1-GP
AUDIO_CX_HGNDA
AUDIO_CX_HGNDB
R2737 0R0603-PAD-5-NSP-GP HGNDA
R2735 0R0603-PAD-5-NSP-GP HGNDB
C2704 SC1U10V2KX-L1-GP
R2701 33R2J-2-GP
AUDIO_CX_CP_FLYP
AUDIO_CX_CP_FLYN
15,16 HDA_SDIN0
16 HDA_SDO
16 HDA_BCLK
16 HDA_SYNC
16 HDA_CODEC_RST#
55 DMIC_CLK
55 DMIC_DATA
RN2703 SRN33J-5-GP-U SC_1018 R2705.R2703->RN2703
RN2702 SRN33J-5-GP-U SC_1018 R2704.R2702->RN2702
RN2701 RN33J-5-GP-U SC_1018 ER2702.ER2701->RN2701 SC_1020 RN2701 del property EMC-TEST
HDA_CODEC_SDOUT_R
HDA_CODEC_SDIN0
HDA_CODEC_BITCLK_R
HDA_CODEC_SYNC_R
HDA_CODEC_RST#_R
DMIC_CLK_CODEC
DMIC_DATA_CODEC
SPKR_MUTE#
EC2701 SC22P50V2JN-L-GP
EC2702 SC22P50V2JN-L-GP
EMC-TEST
78.22034.L1L
EMC-TEST
78.22034.L1L
C2722 SC4D7U6D3V3KX-GP
Close to U2701 pin3
AUDIO_CX_AVEE
AUDIO_CX_LDOAVDD
C2717 SCD1U16V2KX-L-GP
C2720 SC2D2U10V3KX-1GP
C2721 SC2D2U10V3KX-1GP
Close to U2701 pin27
AUDIO_AGND
Connect to system and audio GND
VREF_1D65V
C2706 SCD1U16V2KX-L-GP
C2705 SC1U10V2KX-L1-GP
AUDIO_AGND
Close to U2701 pin29
HDA_SPKR_R R2724 0R0603-PAD-5-NSP-GP HDA_SPKR 20
KBC_BEEP_R R2725 0R0603-PAD-5-NSP-GP KBC_BEEP 24
Q2701 BAT54C-12-GP
75.00054.A7D
SC_1003
For bobo issue
AUDIO_PC_BEEP
C2731 SCD1U16V2KX-L-GP
AUDIO_BEEP1
BOM1
R2727 10KR2J-L-GP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX11802
Size A3
Document Number
LV315GM MB
Rev -1
Date: Monday, April 09, 2018
Sheet 27 of 106

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *(Reserved) Audio AMP*		
Size: A4	Document Number: *LV315GM MB*	Rev: -1
Date: Friday, March 30, 2018	Sheet 28 of 106	

Blanking

BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***AUDIO SPEAKER(RSERVED)***
Size: A4	Document Number: **LV315GM MB**
Rev:	**-1**
Date: Friday, March 30, 2018	Sheet 29 of 106

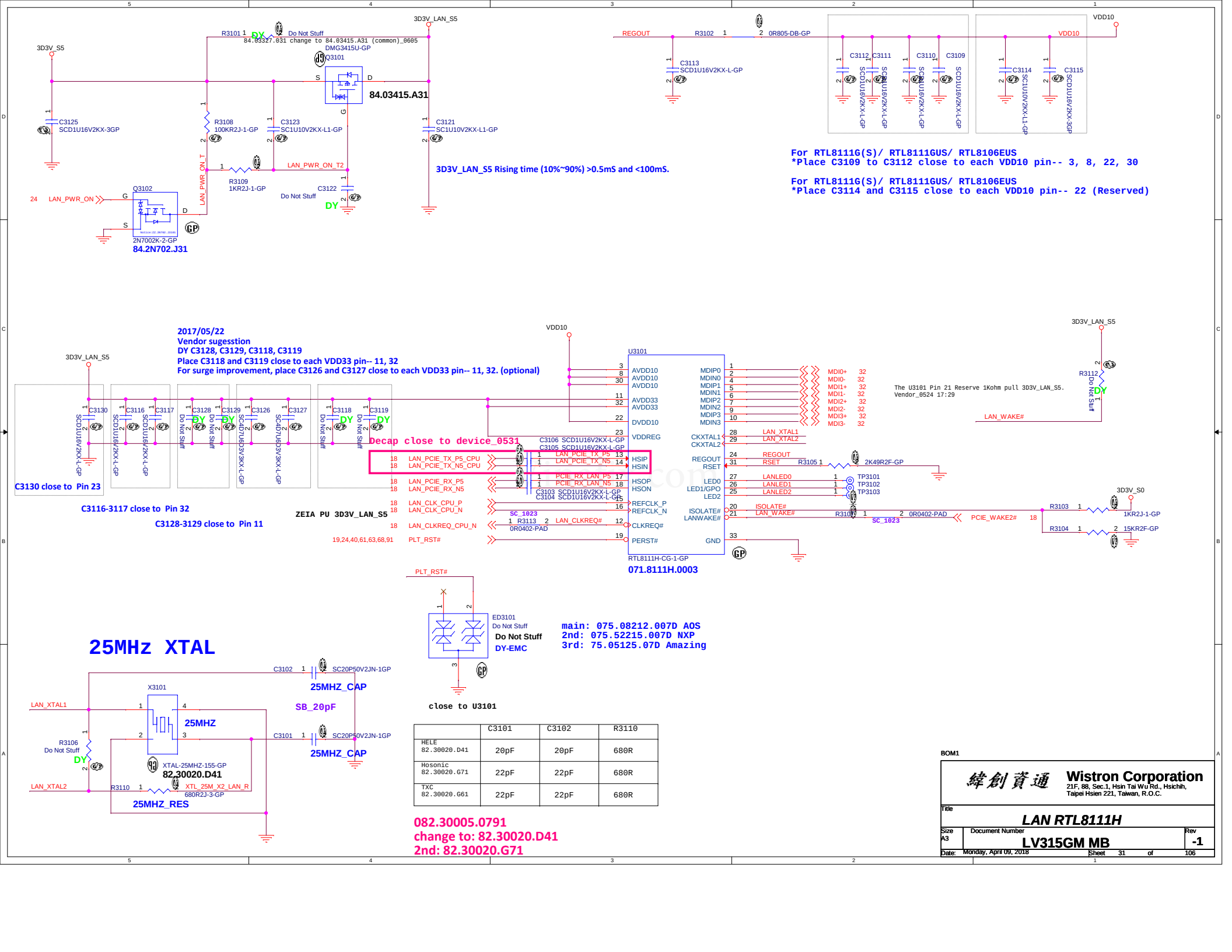
SSID = LOM

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)	
Size A4	Document Number LV315GM MB	Rev -1
Date: Friday, March 30, 2018	Sheet 30 of 106	



	C3101	C3102	R3110
HELE 82.30020.D41	20pF	20pF	680R
Hosonic 82.30020.G71	22pF	22pF	680R
TXC 82.30020.G61	22pF	22pF	680R

082.30005.0791
change to: 82.30020.D41
2nd: 82.30020.G71

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111H

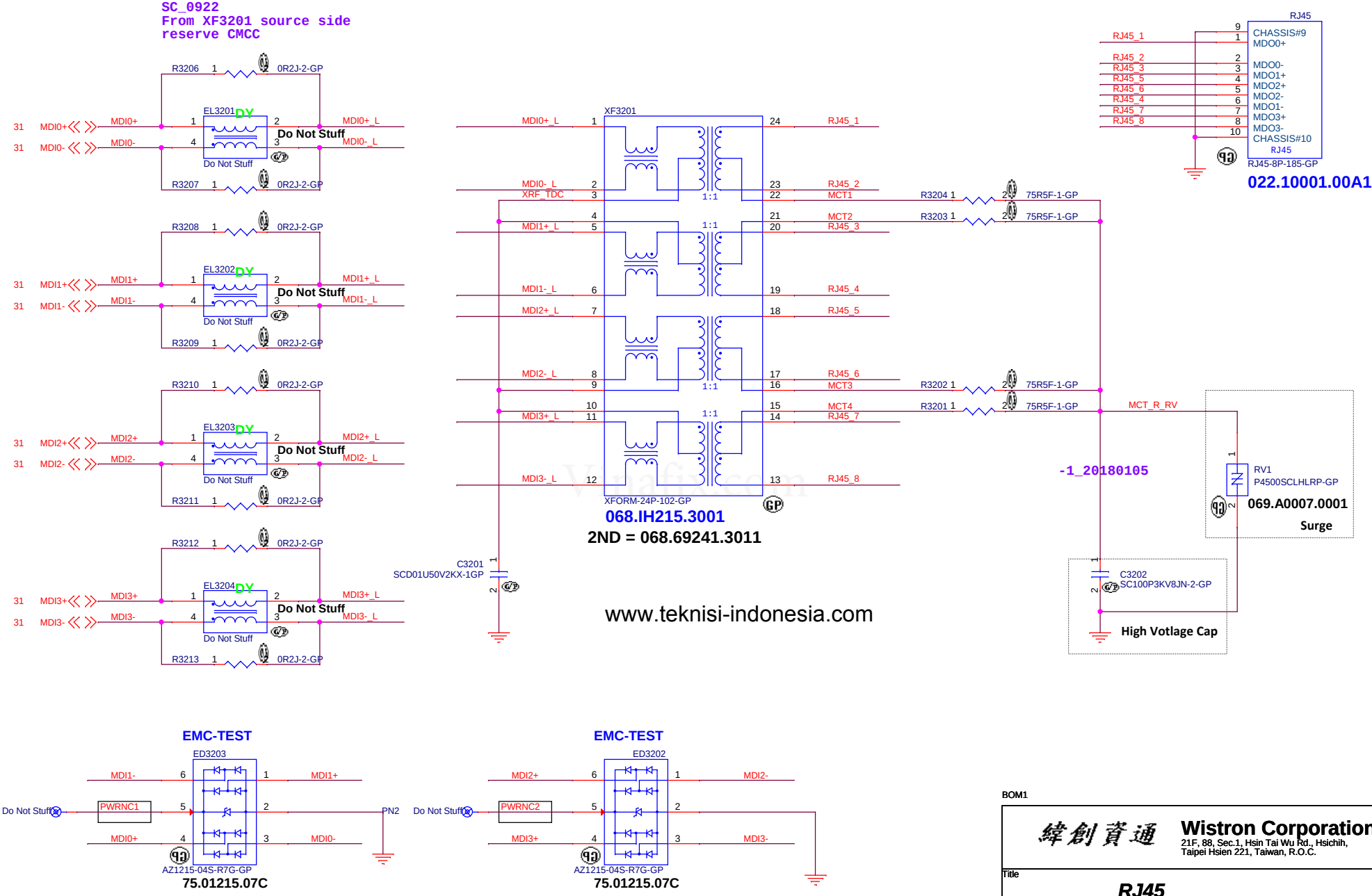
Size: A3 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 31 of 106

10/100M/1000M Lan Transformer

LAN Connector

SC_0922
From XF3201 source side
reserve CMCC



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EMC-TEST

EMC-TEST

main: 75.01215.07C Amazing
2nd: 075.00005.007C LITTELFUSE

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title	RJ45	
Size: Custom	Document Number: LV315GM MB	Rev: -1
Date: Monday, April 09, 2018	Sheet 32 of 106	

Blanking

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

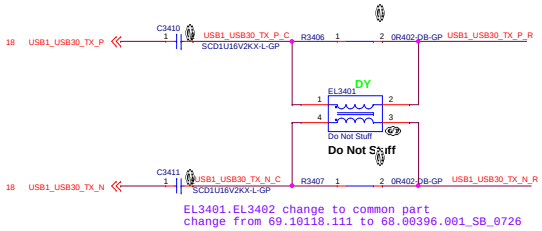
Title: *(RESERVED)*

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 33 of 106

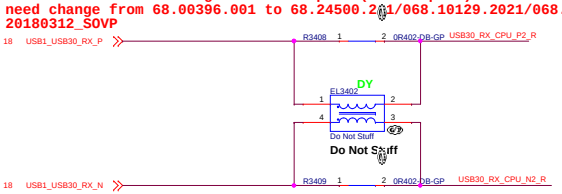
USB Port2, Type A USB2.0

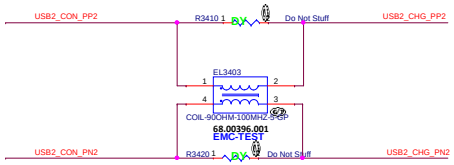
needReserve USB2.0 by pass AOU



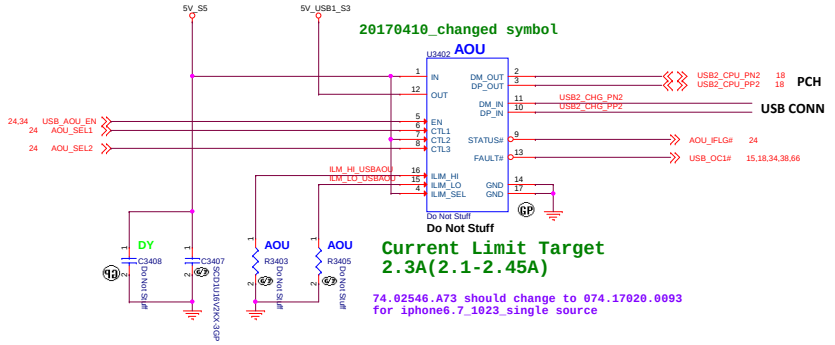
EL3401.EL3402 change to common part
change from 69.10118.111 to 68.00396.001_SB_0726

EL3401.EL3402 need change to common part (USB3.0 part)!!!
need change from 68.00396.001 to 68.24500.241/068.10129.2021/068.01210.2031!!!
20180312_SOVP



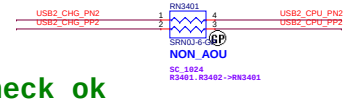


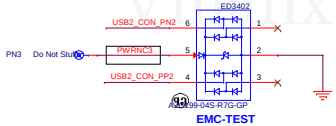
AOU
1ST,
TI, 74.02546.A73
IC PWR SW TPS2546RTER QFN 16P(REV 1.1)
2ND
PERICOM, 074.52546.0A73
IC PWR SW PI5USB2546ZHEX TQFN 16P REV.X



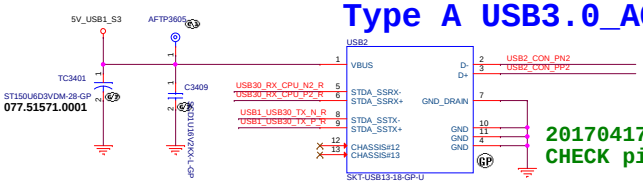
Current Limit Target
2.3A(2.1-2.45A)

74.02546.A73 should change to 074.17020.0093
for iphone6.7_1023_single source





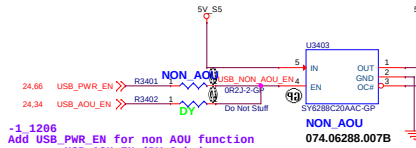
PERICOM circuit check ok



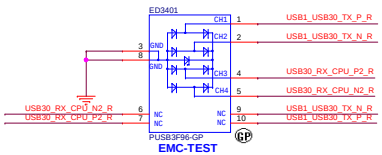
20170417
CHECK pin define again

USB Port2
Type A USB3.0_AOU

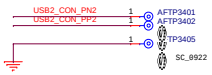
1. When AOU function is N.A, need added USB Current limite /SY6288C20AAC
2. circuit of AOU and USB Current limite /SY6288C20AAC need BOM control, added DY symbol



USB 3.0 Connector Pin definition		
1	*POWER*	
2	*USB 2.0 D-*	
3	*USB 2.0 D+*	
4	*GND*	
5	*StdA_SSRX-*	*SuperSpeed RX*
6	*StdA_SSRX+*	
7	*GND*	
8	*StdA_SSTX-*	*SuperSpeed TX*
9	*StdA_SSTX+*	



main: 075.PUSB3.0073 NXP
2nd: 075.08809.0073 AOS



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CHARGER

Size	Document Number	Rev
A2	LV315GM MB	-1

Date: Monday, April 09, 2018 Sheet 34 of 106

Blanking

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(RESERVED)***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 35 of 106

Blanking

BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***(RESERVED)***
Size: A4	Document Number: **LV315GM MB**
Rev: **-1**	
Date: Friday, March 30, 2018	Sheet 36 of 106

Blanking

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

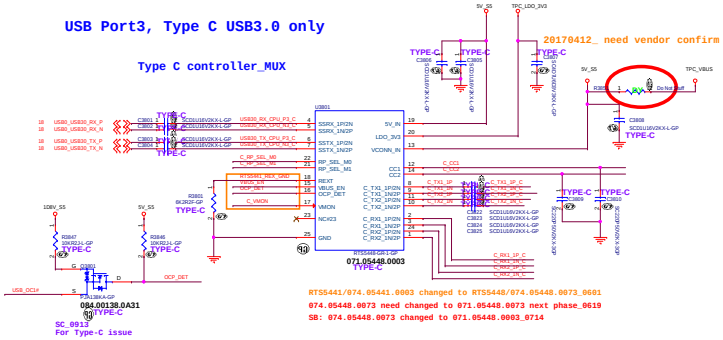
Title: ***(RESERVED)***

Size	Document Number	Rev
A4	LV315GM MB	-1

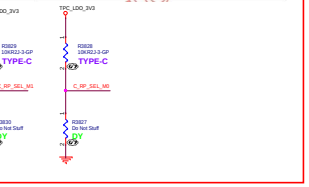
Date: Friday, March 30, 2018 Sheet 37 of 106

USB Port3, Type C USB3.0 only

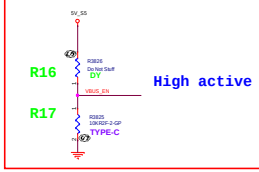
Type C controller_MUX

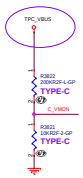


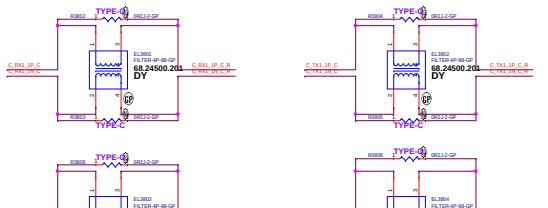
RP_SEL_M0	22	5V Digital I/O	These 2 pins are used for selecting the type-C current modes.
RP_SEL_M1	21		'01' : 900mA
			'10' : 1.5A
			'11' : 3A

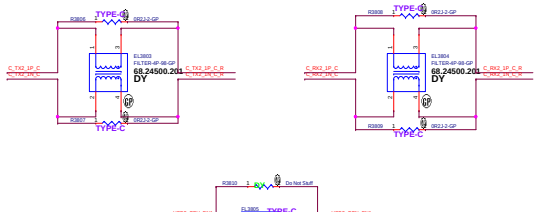


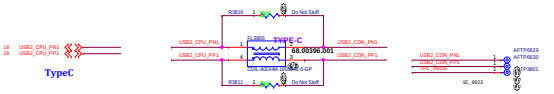
Power switch enable pin	Note
Low Active	R16/R17 mount
High Active	R17 mount,R16 don't mount

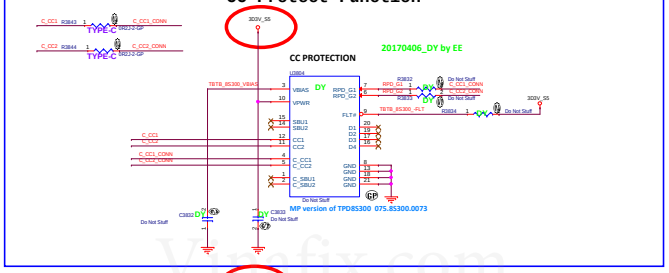




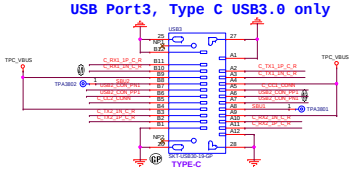


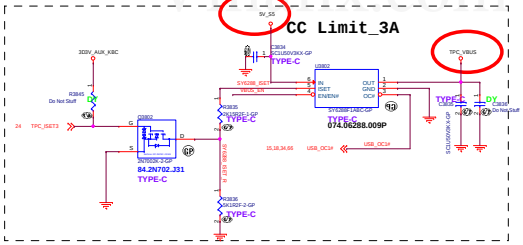




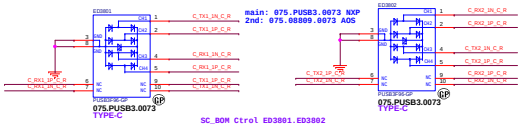


USB Port3, Type C USB3.0 only





Close to CONN



1. AC: 15W/ 3A, 系統功耗不足降至4.5W/ 0.9A
2.DC: 4.5W/ 0.9A

Over-current protection

The SY6288F1/F2 supports Current limit programming. Connect a resistor R_{SET} from ISET pin to ground to program the current limit:

$$I_{LIM}\ (A)=6800/R_{SET}\ (\Omega)$$

The minimum current limit is 0.4A. Current limit beyond 4A is not recommended.

R3835/ 2.15K>>3.16A
R3835/ 2.15K + R3836/ 5.1K >> 0.94A

BOM1

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File	TYPEC USB3.0 ONLY	
Size	Document Number	Rev
A1	LV315GM MB	-1
Date:	Monday, April 04, 2016	Sheet 38 of 106

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BOM1

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Title: (RESERVED)		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 39 of 106	

SSID = Reset.Suspend

Power Sequence

ALL_SYS_PWRGD

PMIC_PWRGD — R4006 (SC_1023, 0R0402-PAD) — ALL_SYS_PWRGD

To EC

To 3V/ 5V Power IC S5 ENABLE

PMIC_THERMTRIP#_R — R4005 0R402-DB-GP — PMIC_THERMTRIP#

PLT_RST# — R4001 1K8R2-GP (20150504) — H_PWRGD_R

R4002 2K2R2J-L1-GP

PLACE CLOSE TO PCH1

Q4002 Allen_0901 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.L11
3rd = 84.T3904.K11

0221 Change PN
D4001 RB551V30-GP
83.R5003.H8H

3V_S5_EN

0221 Rename Net
0309 Del 5V_S5_EN

PURE_HW_SHUTDOWN#

R4004 2KR2F-L1-GP — S5_ENABLE

19,46 PMIC_PWRGD
24 ALL_SYS_PWRGD

0216 Adding off-page
0221 Rename net
0309 Del 5V_S5_EN

45 3V_S5_EN

RUN Power

5V_S0/3D3V_S0

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24 S5_ENABLE
24,26 PURE_HW_SHUTDOWN#
19,46 PMIC_THERMTRIP#
,31,61,63,68,91 PLT_RST#
19,24,46,57 PM_SLP_S3#

5V_S5 — C4007 Do Not Stuff (DY) — C4006 SC1U10V2KX-L1-GP

3D3V_S5 — C4008 Do Not Stuff (DY) — C4009 SC1U10V2KX-L1-GP

U4001 G2898KD1U-GP
VBIAS, IN1#1, IN1#2, IN2#6, IN2#7, EN1, EN2, CT1, CT2, OUT1#13, OUT1#14, OUT2#8, OUT2#9, GND, THERMAL_PAD

074.02898.0093
2nd = 074.22976.0091

SW_5V_S0_CT — C4004 Do Not Stuff (DY)
SW_3D3V_S0_CT — C4001 Do Not Stuff (DY)

5V_SYS_OUT — 3.5A
3V_SYS_OUT — 3A

C4011 SCD1U16V2KX-L1-GP
C4010 SCD1U16V2KX-L1-GP

3V_5V_S0_EN — C4051 SCD1U25V2KX-L1-GP

R4007 0R2J-2-GP — R4008 Do Not Stuff (DY)

PM_SLP_S3#_R — KBC_SLP_S3#_R

-1_1227
C4051 ASM for ESD issue

5V_SYS_OUT — PG4001 PG4002 PG4003 PG4004 — GAP-CLOSE-PWR-6-GP — 5V_S0

1D8V_S0

1D8V_S5 — C4015 SC1U10V2KX-L1-GP

U4002 APE8939GN3-GP
VIN, VIN, VBIAS, EN, VOUT#8, VOUT#7, VOUT#6, GND, VIN

R4059 0R402-DB-GP — 1D8V_S0_EN

R4060 Do Not Stuff — C4017 Do Not Stuff (DY)

1D8V_S0 — 0.5A — C4016 SCD1U16V2KX-L1-GP

074.08939.0093

3V_SYS_OUT — PG4005 PG4006 PG4007 — GAP-CLOSE-PWR-6-GP — 3D3V_S0

PM_SLP_S3# — R4009 0R2J-2-GP — R4061 Do Not Stuff (DY)

24,60 KBC_SLP_S3#

U4003 SNLVC1G08DCKR4-GP
A, B, GND, VCC, Y

R4010 Do Not Stuff (DY)

3V_5V_S0_EN_R

EC4001 SC1KP50V2KX-1GP
EMC-TEST

-1_1229
Add EC4001 1000pF

73.01G08.DHG

Discharge circuit

3D3V_AUX_S5 — R4056 Do Not Stuff (DY) — 3D3V_S5_EN_DCG — Q4001 (Allen_0906)

0221 Rename Net
3V_S5_EN
3D3V_S5_DISCHG

R4048 Do Not Stuff (DY) — 3D3V_S5

Do Not Stuff

Do Not Stuff

DDR3_VCCA_PWRGD
DDR3_DRAM_PWROK
APL have not DDR3_VCCA_PWRGD & COREPWROK control pin.
APL have not DRAM_PWROK control pin.

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (Power Plane EN)

Size: A3 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 40 of 106

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BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *(Reserved)DS3*		
Size: A4	Document Number: *LV315GM MB*	Rev: -1
Date: Friday, March 30, 2018	Sheet 41 of 106	

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

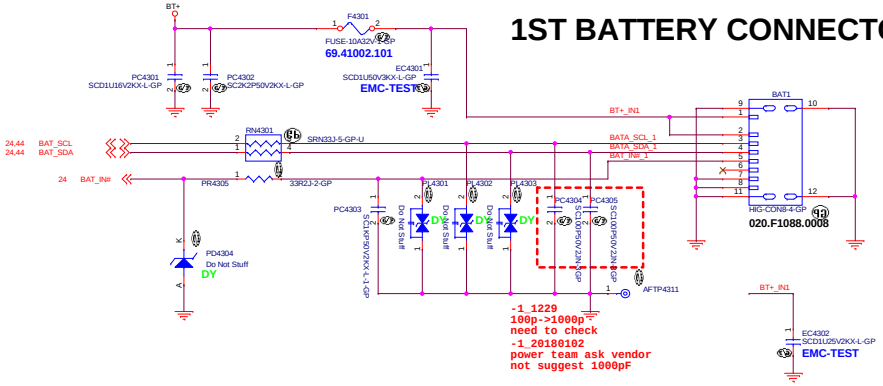
Title: ***Reserved***

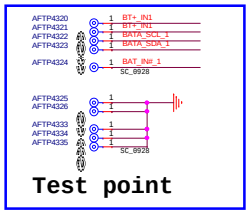
Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 42 of 106

Main Func = ADT Input

1ST BATTERY CONNECTOR



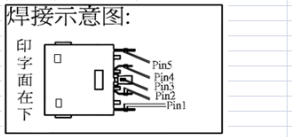


Connector Pin Alignment(Vendor：Suyin,Aces)

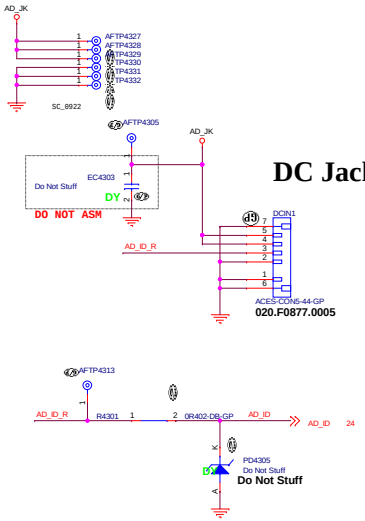
Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

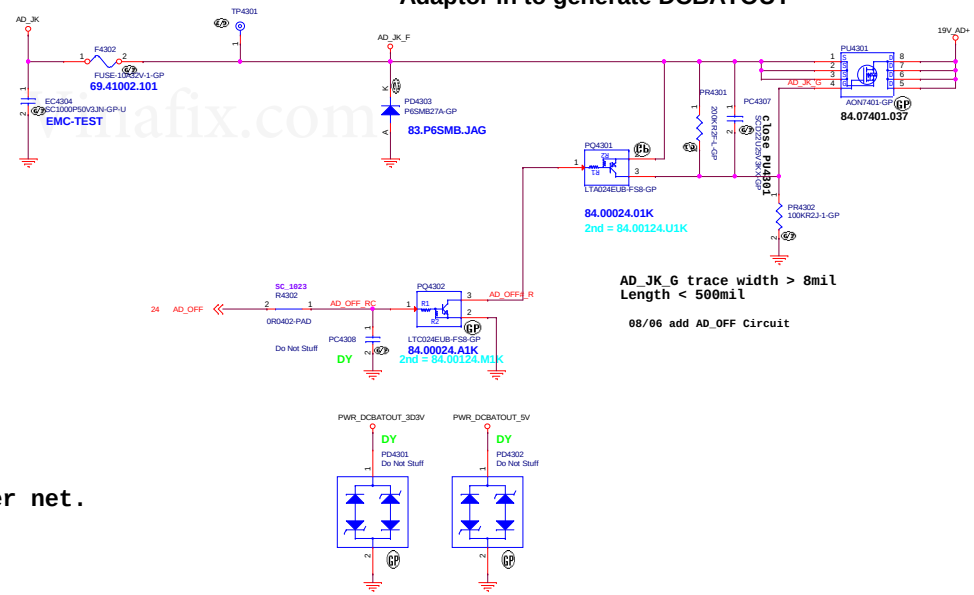
MB_Side		Cable Max. Current
Pin 1	AD_JK_F	UL10064A WG28# (3A)
Pin 2	AD_JK_F	UL10064A WG28# (3A)
Pin 3	AD_ID	UL10064A WG28# (3A)
Pin 4	GND	UL10064A WG26# (3.8A)
Pin 5	GND	UL10064A WG26# (3.8A)



DC Jack



Adaptor in to generate DCBATOUT



DCBATOUT: 2~3 empty-pins between signals or other power net.
(Apply to TNB, LNB)

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 043_DCIN & BATT CONN

Size: Custom | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 43 of 106

OFFPAGE

24,43 BAT_SCL — PR4411 0R0402-PAD — PWR_CHG_CLK
24,43 BAT_SDA — PR4415 0R0402-PAD — PWR_CHG_DATA
24 AD_IA — PR4422 0R0402-PAD — PWR_CHG_IOUT
19,24,46 PROCHOT#_CPU — PR4444 0R0402-PAD — PWR_CHG_PROCHOT#
24 AC_IN# — PR4448 0R0402-PAD — PWR_AC_IN#

SSID = Charger

Check PMOS use AON7401 on page43

Id= -10A
Qg= -22nC
Rdson=14~22mohm

075.67002.007C

Close to 第一顆MOS

SC-0906
83.R2003.A8M
83.RB530.08F
083.52030.008F

83.R2003.A8M

84.07410.A37
2nd = 084.03319.0A31

74.02224.073

Already Pull high on KBC side

PC4419 is close to PU4401 PIN#4

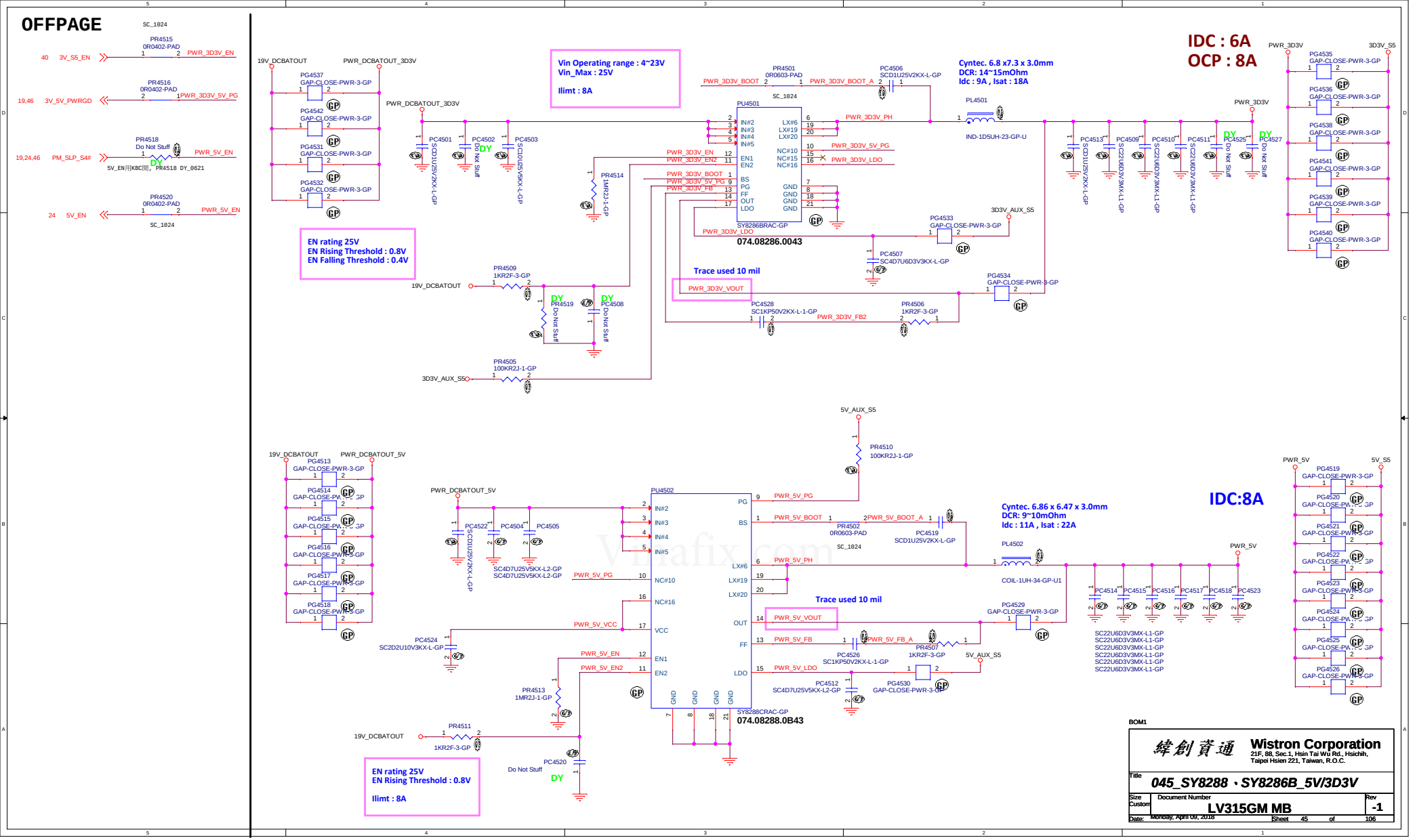
Id= -10A
Qg= -40nC
Rdson=17.6~23mohm

Cyntec, 6.5mm x 6.9mm x 3.0mm
DCR: 28m ~ 33mOhm
Idc : 5.5A , Isat : 6.5A

Charger Current=1.4~3.6A

BOM1

鋒創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	044_CHARGER_ HPA02224RGRR
Size: Custom	Document Number: LV315GM MB
Rev	-1
Date: Monday, April 02, 2018	Sheet 44 of 105



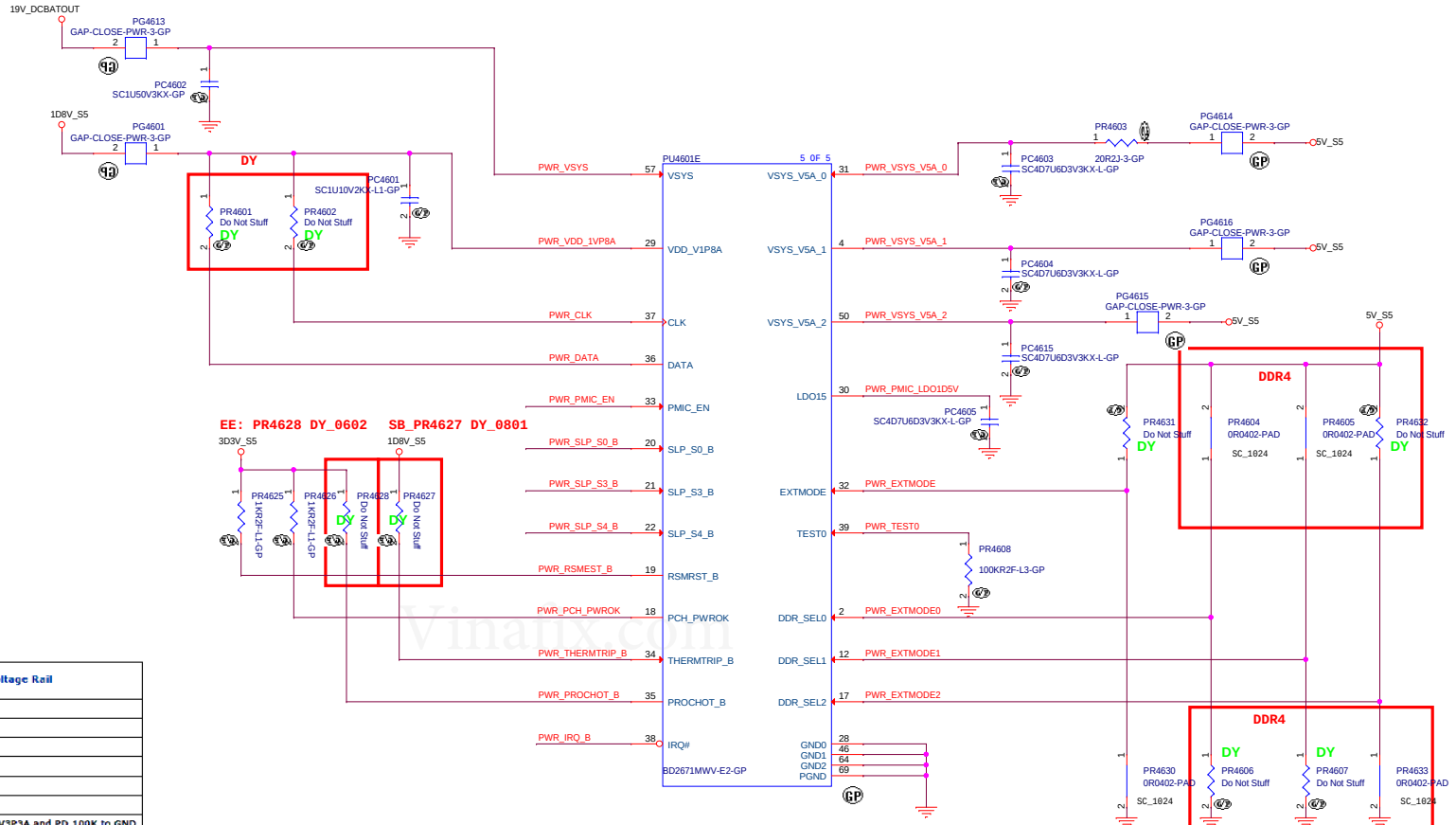
OFFPAGE

SC_1024

19	PMIC_I2C_SCL	PR4609 0R0402-PAD	PWR_CLK
19	PMIC_I2C_SDA	PR4615 0R0402-PAD	PWR_DATA
19,45	3V_5V_PWRGD	PR4616 0R0402-PAD	PWR_PMIC_EN
19	PM_SLP_S0#	PR4617 0R0402-PAD	PWR_SLP_S0_B
19,24,40,57	PM_SLP_S3#	PR4618 0R0402-PAD	PWR_SLP_S3_B
19,24,45	PM_SLP_S4#	PR4619 0R0402-PAD	PWR_SLP_S4_B
19,24	PMIC_RSMRST#	PR4620 0R0402-PAD	PWR_RSMEST_B
19,40	PMIC_PWRGD	PR4621 0R0402-PAD	PWR_PCH_PWROK
19,40	PMIC_THERMTRIP#	PR4622 0R0402-PAD	PWR_THERMTRIP_B
19,24,44	PROCHOT#_CPU	PR4623 0R0402-PAD	PWR_PROCHOT_B
20	PMIC_IRQ#	PR4624 0R0402-PAD	PWR_IRQ_B

Main Func = CPU_CORE

I2C, Other signals



Gemini Lake PMIC and SoC Signal Connections

Gemini Lake PMIC Pin	Gemini Lake SoC Pin Name	SoC Pin	SoC Pin Type	Voltage Rail
IRQ#	TBD	TBD	Input	1.8V (SoC internal)
THERMTRIP#	THERMTRIP_N	J53	Output	1.8V (SoC internal)
PROCHOT#	PROCHOT_N	J54	Input	1.8V (SoC internal)
SLP_S4#	PMU_SLP_S4_N	J49	Output	1.8V (SoC internal)
SLP_S3#	PMU_SLP_S3_N	D51	Output	1.8V (SoC internal)
SLP_S0#	PMU_SLP_S0_N	C52	Output	1.8V (SoC internal)
PCH_PWROK	SoC_PWROK	D25	Input	External PU 20K to V3P3A and PD 100K to GND
RSMRST#	RSM_RST_N	F27	Input	External PU 20K to V3P3A and PD 100K to GND
DATA	PMIC_I2C_SDA	TBD	Input/ Output	1.8V (SoC internal)
CLK	PMIC_I2C_SCL	TBD	Output	1.8V (SoC internal)

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 046_BD2671_I2C

Size: Custom | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 46 of 106

Main Func = CPU_CORE

BUCK2[VCCGI]:1.0V_21A

OFFPAGE

SC_1824

PR4723 0R0402-PAD — VCCGI_SENSE — PWR_VCCGI_FBPC

PR4724 0R0402-PAD — VSSGI_SENSE — PWR_VCCGI_FBNB

19V_DCBATOUT — PWR_DCBATOUT_VCORE

PG4701 GAP-CLOSE-PWR-3-GP

PG4702 GAP-CLOSE-PWR-3-GP

PG4703 GAP-CLOSE-PWR-3-GP

PG4704 GAP-CLOSE-PWR-3-GP

PG4705 GAP-CLOSE-PWR-3-GP

PG4706 GAP-CLOSE-PWR-3-GP

DY — PT4702 Do Not Stuff

5V_S5

PC4705 SC4D7U6D3V3KX-L-GP

SC_1824

PR4701 0R0402-PAD

PWR_VCCGI_PVCC

PWR_VCCGI_PWM_1

PC4716 SC1U10V2KX-L1-GP

MOSFET GATE Driver

PU4701 BD9515NUXE2-GP-U

PVCC, PWM, EN, PAD/PGND, BOOT, HG, SW, LG

PWR_VCCGI_BOOT

PWR_VCCGI_HG

PWR_VCCGI_PH

PWR_VCCGI_LG

SC_1824 PR4720 0R0805-PAD

PC4711 SCD47U25V3KX-1GP

PR4721 — DY — Do Not Stuff — PWR_VCCGI_HG_A

PU4702 FDMS3600-02-RJK0215-COLAY-GP

PWR_DCBATOUT_VCORE

PC4702 PC4703 PC4701 PC4704 SC10U25V6KX-1-GP

ZZ.00215.037

075.07321.0073

ICCMAX=21A

TDC=18A

close choke

VCCGI :1D0V_21A

1V_CPU_VCGI

PC4718 SC22U6D3V3MX-L1-GP

PT4701 SE330U2VDM-4-GP

PU4601A 1 OF 5

VCCGI_PWM — PWR_VCCGI_PWM

VCCGI_DRVEN — PWR_VCCGI_DRVEN

SC_1824 PR4702 0R0402-PAD

PL4701 IND-D22UH-39-GP

TOKO 10 X 11.15 X 4 mm

DCR: 0.64 +-7% m ohm

Idc :32A , Isat : 32A

PR4707 1K1R2F-GP

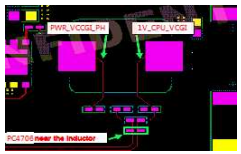
PR4708 2K2R2F-GP

PWR_VCCGI_PHA

PR4719 NTC-10K-27-GP-U

PR4709 6K2R2F-GP

close choke



PWR_VCCGI_PH

PR4722 Do Not Stuff — DY

PWR_VCCGI_SNUB

PC4715 Do Not Stuff — DY

Panasonic 7.3 * 4.3 * 1.9 mm

ESR: 9 m ohm

22uF_6.3V_0805 *8pcs

DY*2pcs

VCCGI_CSP — PWR_VCCGI_CSP

PC4717 SC56P50V2JN-2GP

SC_1824 PR4710 0R0402-PAD

PWR_VCCGI_CSPA

close PMIC

PC4714 SCD047U25V2KX-GP

close choke

PC4706 SCD47U25V3KX-1GP

VCCGI_CSN — PWR_VCCGI_CSN

PR4711 360R2F-GP

PC4707 Do Not Stuff — DY

close PMIC

VCCGI_VOS — PWR_VCCGI_VOS

PC4710 SCD047U25V2KX-GP

PR4716 0R0402-PAD

SC_1824

VCCGI_FBP — PWR_VCCGI_FBP

PR4712 4K3R3F-GP

PWR_VCCGI_FBPA

PR4715 0R0402-PAD

PWR_VCCGI_FBPB

PG4707 GAP-CLOSE-PWR-3-GP — PWR_VCCGI_FBPC

PC4712 Do Not Stuff — DY

SC_1824

PC4713 SC1U10V2KX-L1-GP

VCCGI_FBN — PWR_VCCGI_FBN

PR4713 0R0402-PAD

PWR_VCCGI_FBNA

PG4708 GAP-CLOSE-PWR-3-GP — PWR_VCCGI_FBNB

DY — PC4736 Do Not Stuff

BD2671MWV-E2-GP

EE Check

1V_CPU_VCGI

PR4717 100R2F-L1-GP-U

PR4718 100R2F-L1-GP-U

Change PR4717 next stage_SB_0626

SC-0906

BOM1

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 047_BD2671_VCCGI

Size: A2 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 47 of 108

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BOM1

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Title	***Reserved***
Size: A4	Document Number: **LV315GM MB** — Rev: **-1**
Date: Friday, March 30, 2018	Sheet 48 of 106

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BOM1

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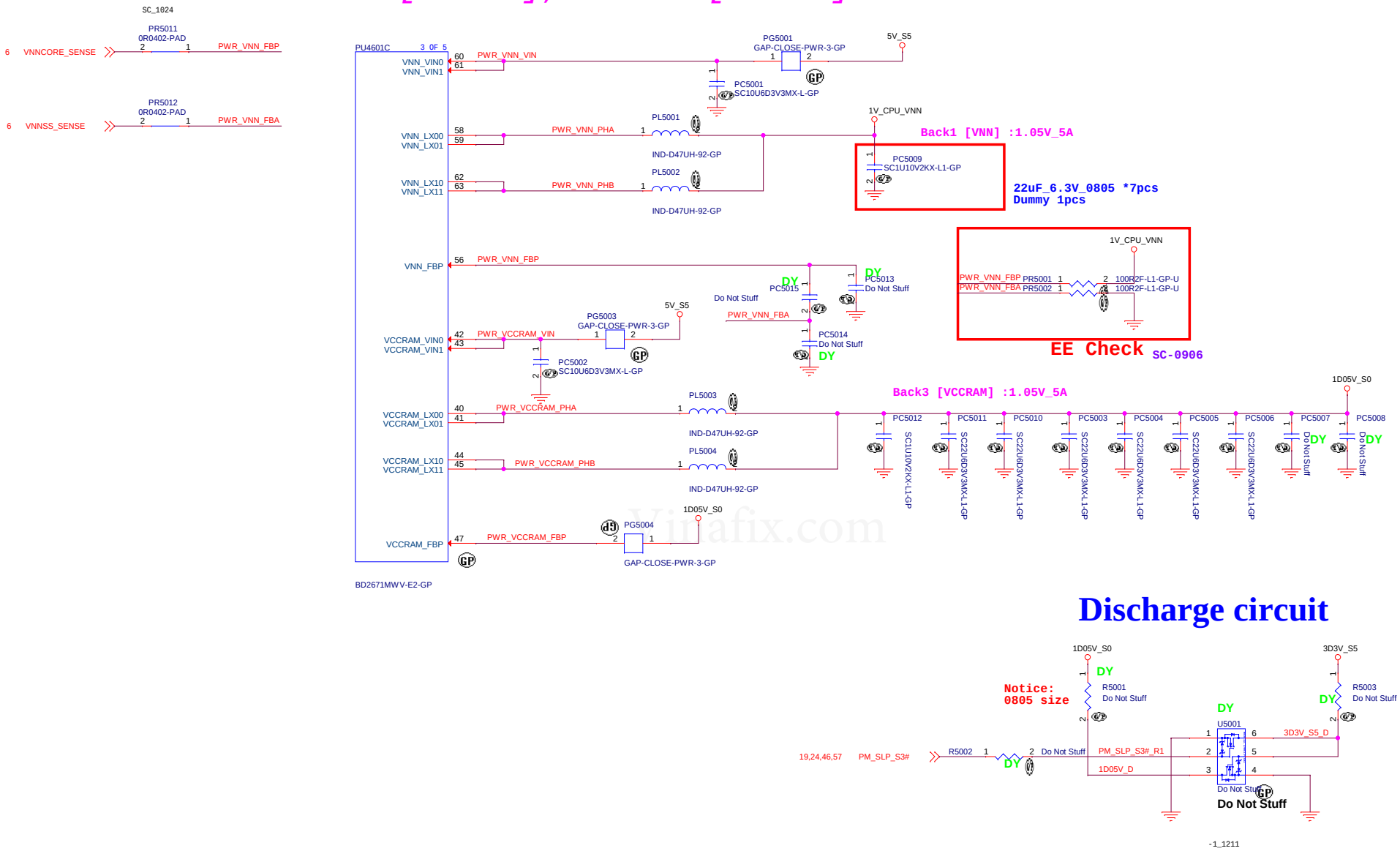
Title	***Reserved***	
Size A4	Document Number **LV315GM MB**	Rev **-1**
Date: Friday, March 30, 2018	Sheet 49 of 106	

OFFPAGE

VNN[BUCK1], VCCRAM[BUCK3]



Discharge circuit

-1_1211

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 050_BD2671_VNN		
Size: A3	Document Number: LV315GM MB	Rev: -1
Date: Monday, April 09, 2018	Sheet 50 of 106	

VDDQ[BUCK6], V1P2A[BUCK5]

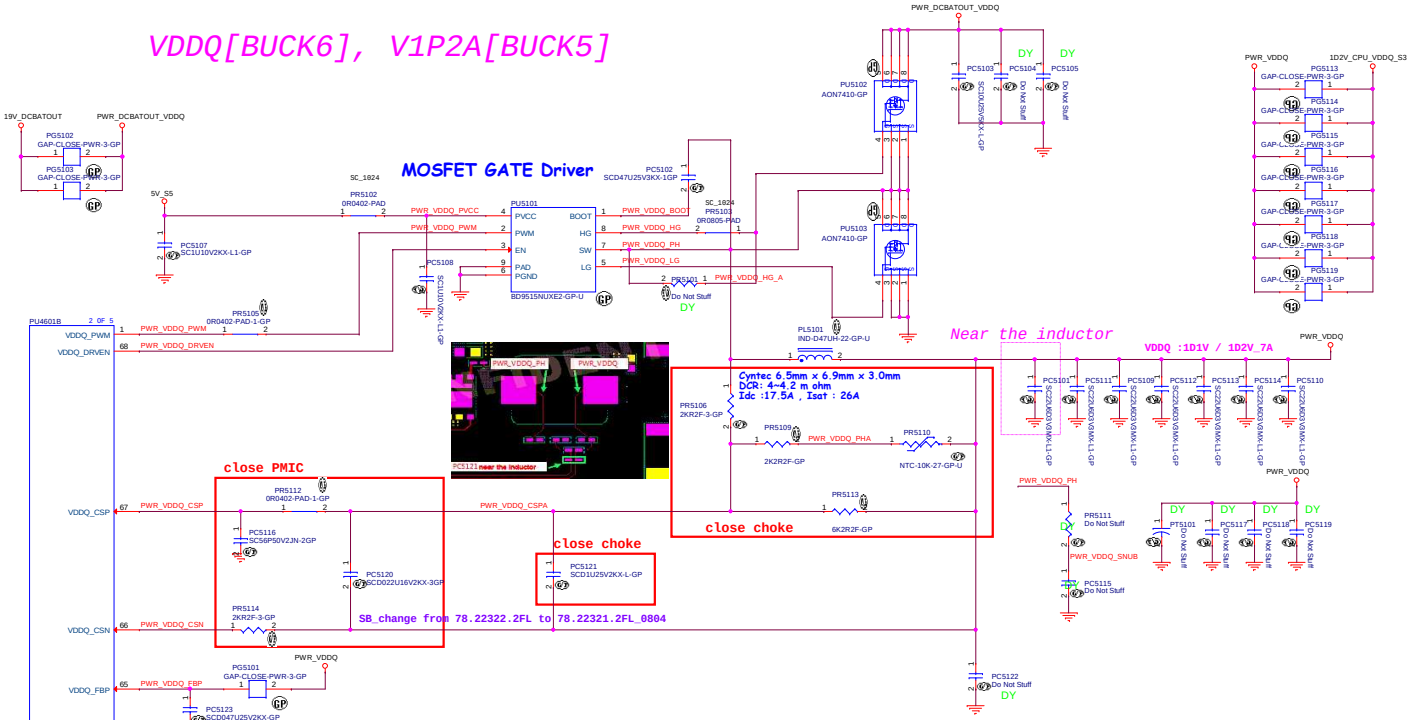


Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

BOM1

Wistron Corporation
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Title: 051_BD2671_VDDQ/VTT

Size	Document Number	Rev
Custom	LV315GM MB	-1
Date: Monday, April 09, 2018	Sheet 51 of 106	

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BOM1

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Title

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Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 52 of 106

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BOM1

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Title: ***Reserved***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 53 of 106	

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BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *(Reserved)1D8V*		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 54 of 106	

3 empty-pins between wire cable(MIC, camera, or other control signals) & coxial cable(LCD panel usage).
(Apply to LNB only)

SSID = VIDEO

change pin define_0601

eDP connector

INVERTER POWER

20170505 Change Net name

69.42402.001

074.06288.007B

Panel BL brightness/Power En/BL En

20170505 Change Net name

20170505 Change Net name

eDP

LCD Panel touch_USB Port0

DMIC

CAMERA_ USB Port4

CAMERA POWER

Layout 40 mil

BOM OPTION

Test point

CAMERA_ USB Port5

LCD Panel touch_USB Port0

main: 75.00199.07C Amazing
2nd: 075.08105.007C AOS

20.K0678.040

Close to eDP connector

DY-EMC

DY-TOUCH

Do Not Stuff

BOM1	
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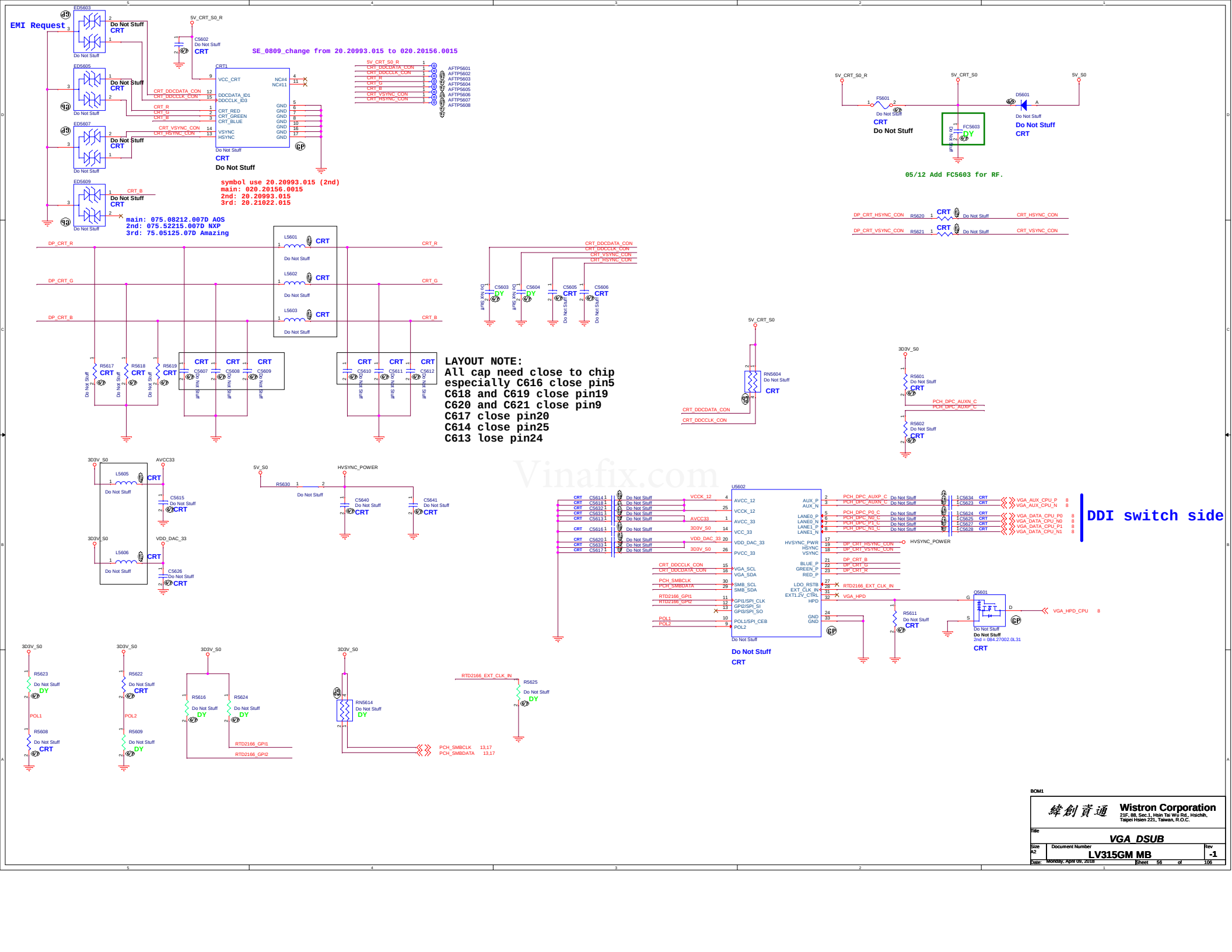
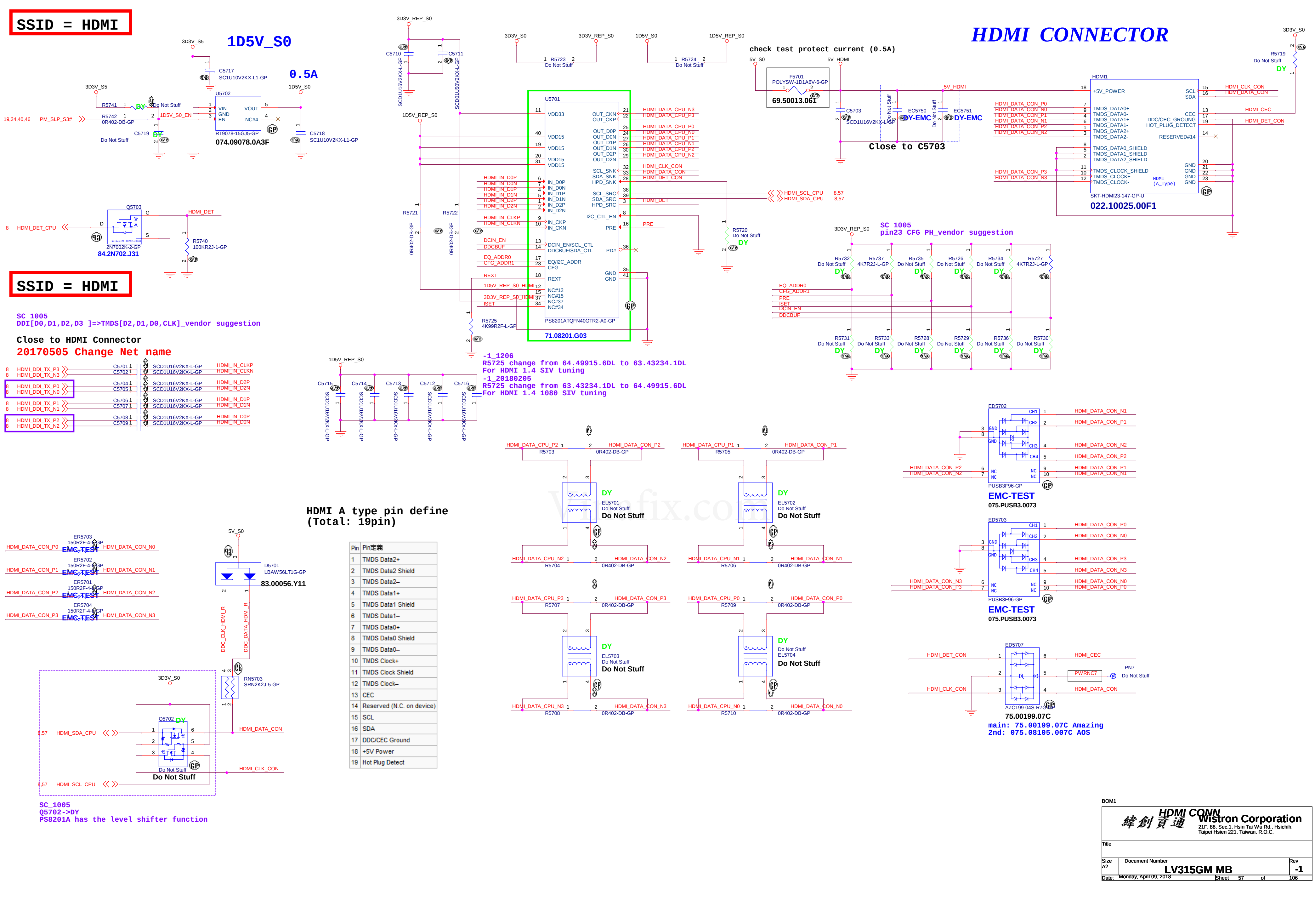
Title	LCD/CAM/DMIC/TOUCH
Size A2	Document Number LV315GM MB Rev -1
Date: Monday, April 09, 2018	Sheet 55 of 106


EMI Request
SE_0809_change from 20.20993.015 to 020.20156.0015
symbol use 20.20993.015 (2nd)
main: 020.20156.0015
2nd: 20.20993.015
3rd: 20.21022.015
main: 075.08212.007D AOS
2nd: 075.52215.007D NXP
3rd: 75.05125.07D Amazing
05/12 Add FC5603 for RF.
LAYOUT NOTE:
All cap need close to chip
especially C616 close pin5
C618 and C619 close pin19
C620 and C621 close pin9
C617 close pin20
C614 close pin25
C613 lose pin24
DDI switch side
Do Not Stuff
CRT
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VGA_DSUB
LV315GM MB
Monday, April 09, 2018

HDMI CONNECTOR



HDMI A type pin define (Total: 19pin)

Pin	Pin定義
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2–
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1–
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock–
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

HDMI CONN

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Size	Document Number	Rev
A2	LV315GM MB	-1

Date: Monday, April 09, 2018 Sheet 57 of 106

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BOM1

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 58 of 106

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BOM1

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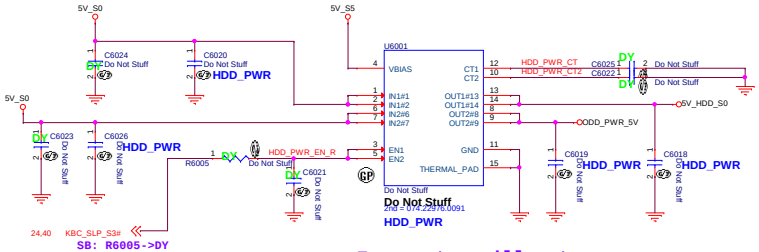
Title: ***RESERVED***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 59 of 106

SSID = SATA

HDD_PWR (Reserved)_SB_0802

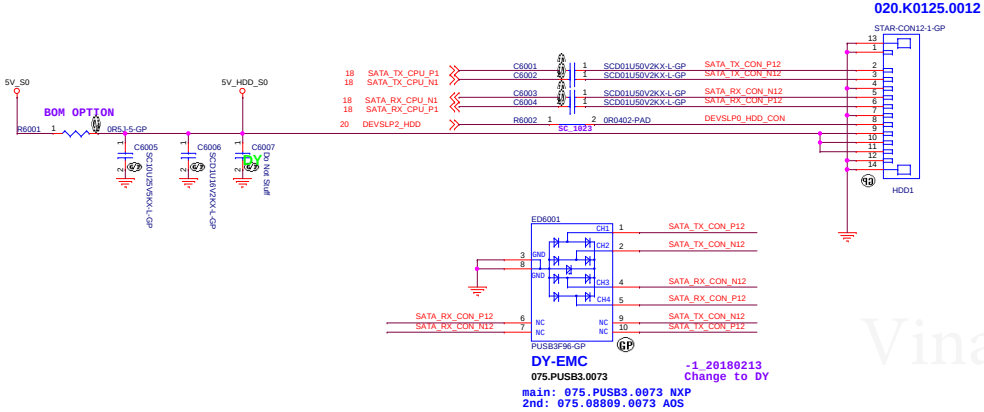


-1_20180202
BOM Control: HDD_PWR->DY

For system will auto power on -> power off after plug in AC issue

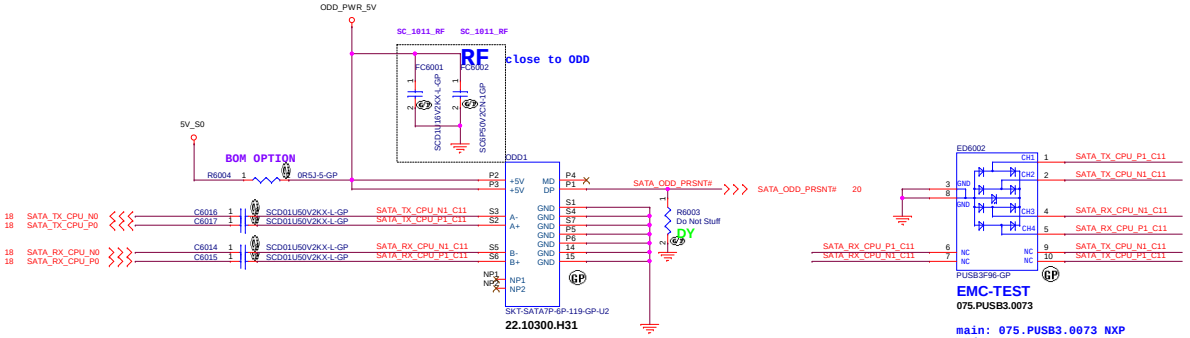
20170526
Change pin follow LV315KBL

020.K0125.0012



DY-EMC
075.PUSB3.0073
-1_20180213
Change to DY

main: 075.PUSB3.0073 NXP
2nd: 075.08809.0073 AOS



EMC-TEST
075.PUSB3.0073

main: 075.PUSB3.0073 NXP
2nd: 075.08809.0073 AOS

BOM1

Wistron Corporation
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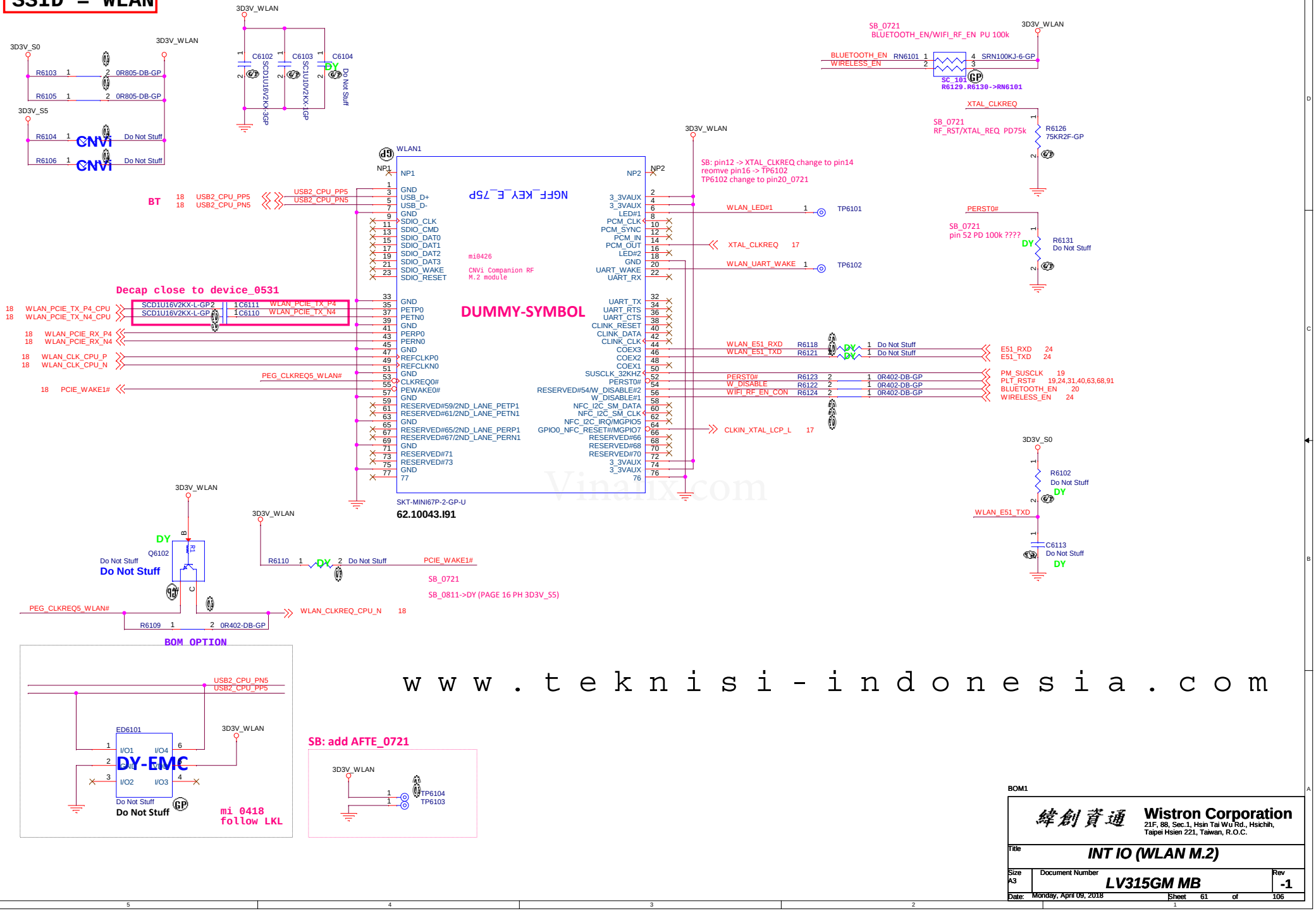
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD

Size: A2 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 60 of 106

SSID = WLAN



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: INT IO (WLAN M.2)		
Size: A3	Document Number: LV315GM MB	Rev: -1
Date: Monday, April 09, 2018	Sheet 61 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation
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Title

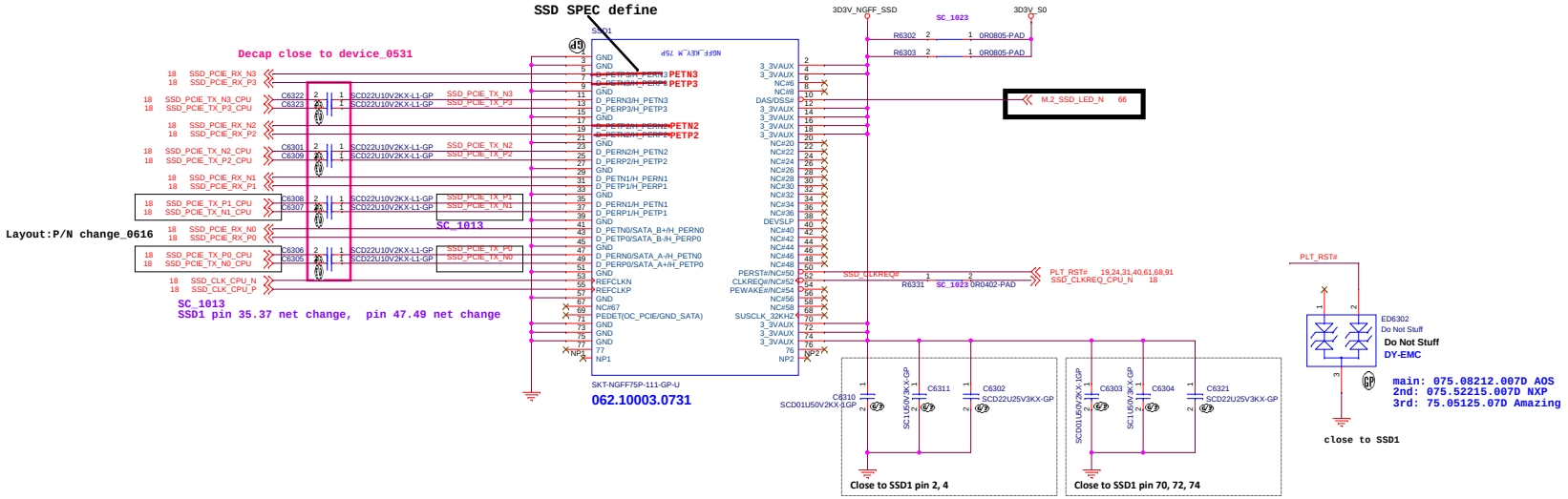
RESERVED

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 62 of 106

Main Func = SSD

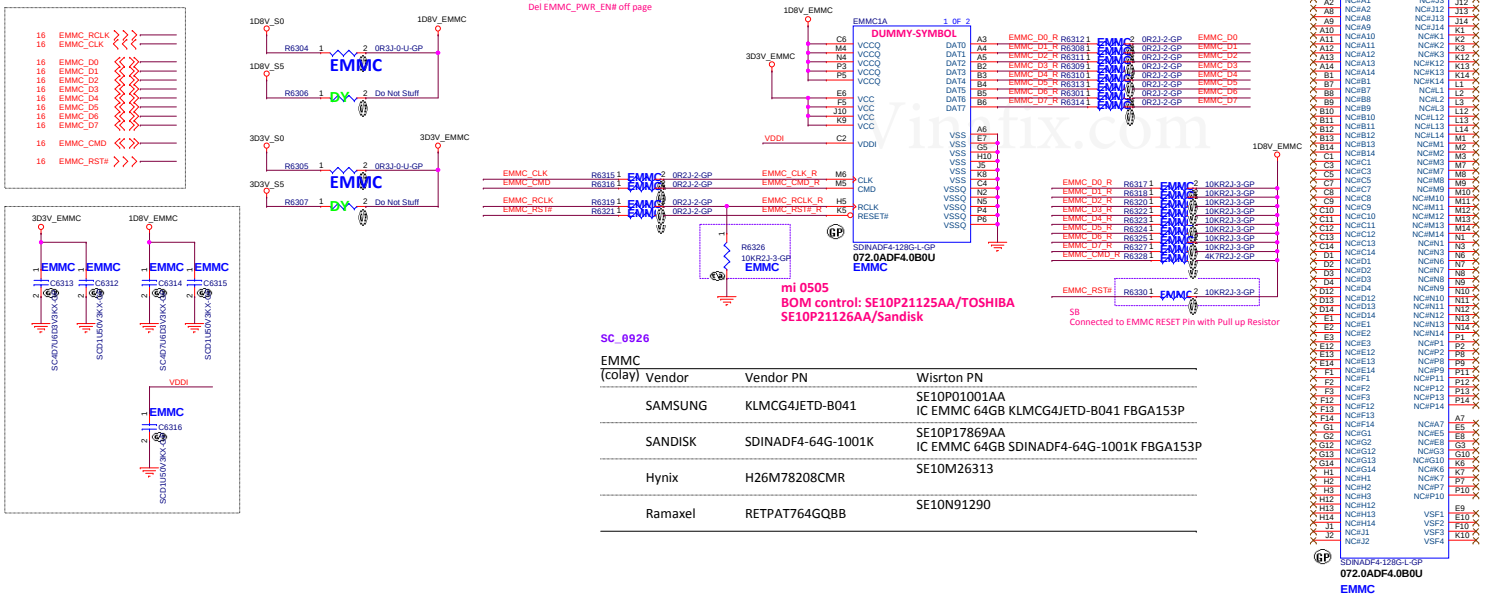
TYPE-M NGFF CARD FOR PCIE SSD/Optane



SSID = eMMC

FVT_reserved EMMC

SB remove U6301 load switch
add 0ohm
Del EMMC_PWR_EN# off page



SC_0926

EMMC

(colay) Vendor	Vendor PN	Wisrton PN
SAMSUNG	KLMCG4JETD-B041	SE10P01001AA IC EMMC 64GB KLMCG4JETD-B041 FBGA153P
SANDISK	SDINADF4-64G-1001K	SE10P17869AA IC EMMC 64GB SDINADF4-64G-1001K FBGA153P
Hynix	H26M78208CMR	SE10M26313
Ramaxel	RETPAT764GQBB	SE10N91290

BOM1

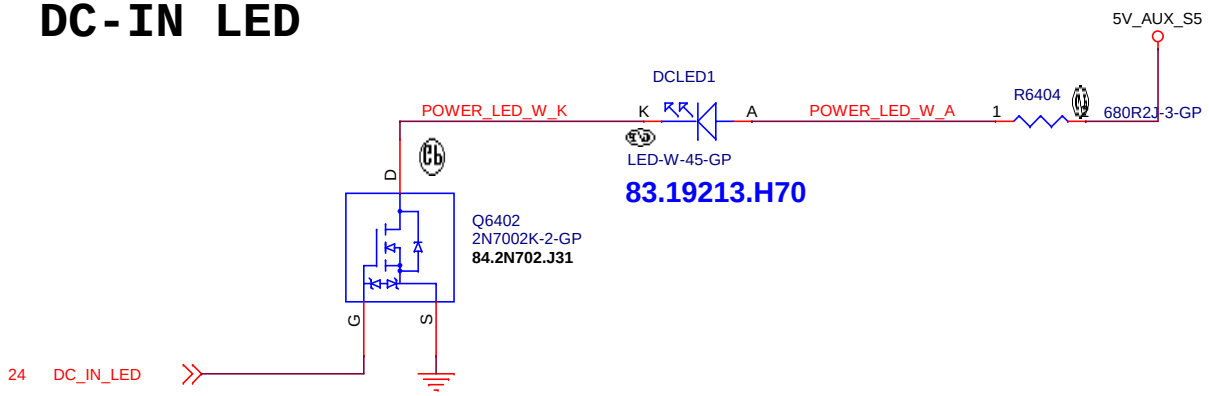
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M.2 SSD SLOT

Size	Document Number	Rev
A2	LV315GM MB	-1

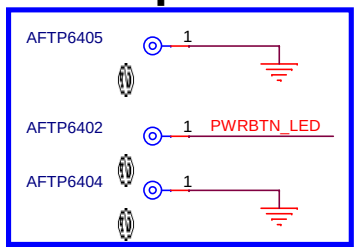
Date: Monday, April 09, 2018 Sheet 63 of 106

DC-IN LED

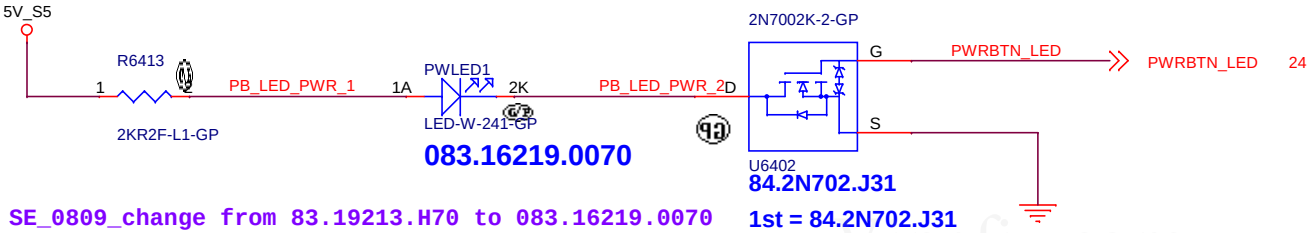


SC_1005
100R->680R
For power consumption: AC_S5 fail

Test point



POWER BTN LED



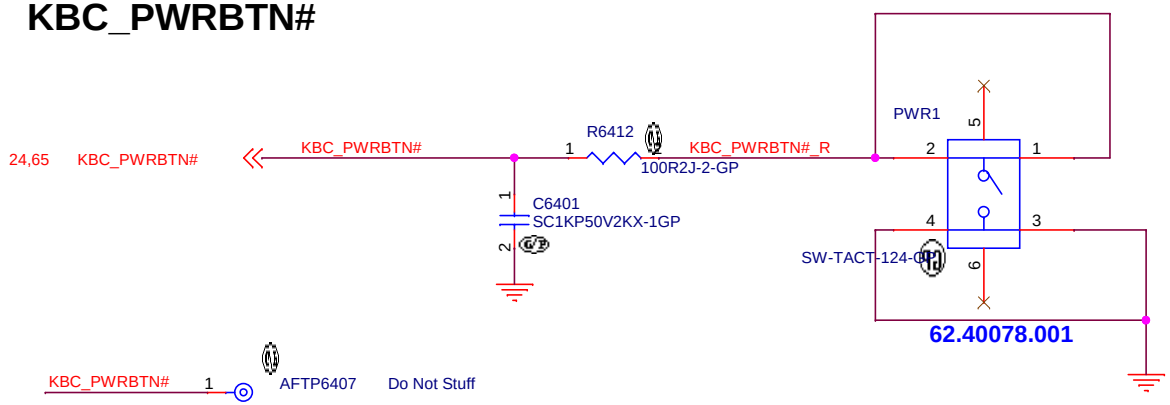
SE_0809_change from 83.19213.H70 to 083.16219.0070

1st = 84.2N702.J31

2nd = 84.2N702.W31

20180326_EC
change R6413 from 63.10134.L0L to 64.20015.L0L
Power button LED too light

KBC_PWRBTN#



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED /POWER BUTTON		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Monday, April 09, 2018	Sheet 64 of 106	

SSID = Touch.Pad

20170427_pin deifine check by Dennis

KB_LED

SC_1023
R6515 add property:KB_BL

Do Not Stuff
KB_BL

SC_0926
KBBL1 020.K0305.0004->020.K0342.0004

click pad

To KBC Pin77

-1_20180205
Add ED6502 for touch pad

-1_1228
EC6508.EC6509 33P->1000P
Add 1000P*2 for LID_CLOSE&TP_INT
for ESD issue
-1_20180104
EC6508.EC6509 1000P->33P
-1_20180112
EC6508-11 33P->100P

SB_Q6508 change D & S

CLOSE keyboard connector

EMC-TEST
75.00199.07C
main: 75.00199.07C Amazing
2nd: 075.08105.007C AOS

TPAD1
main: 020.K0237.0006
2nd: 020.K0002.0006

main: 075.08212.007D AOS
2nd: 075.52215.007D NXP
3rd: 75.05125.07D Amazing

Do Not Stuff
DY-EMC

close to U2402

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCH PAD

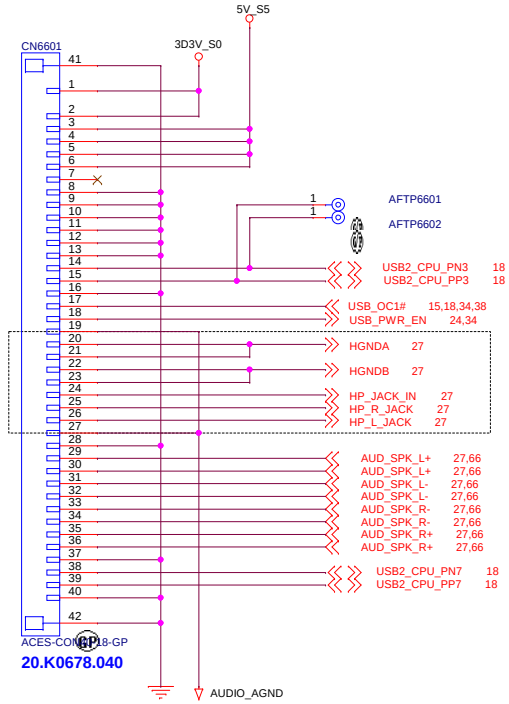
Size: A3 | Document Number: LV315GM MB | Rev: -1

Date: Monday, April 09, 2018 | Sheet 65 of 106

IO CONN

Type A USB3.0
USB Redrive
Card reader

20170421
Cnhange pin define by Dennis



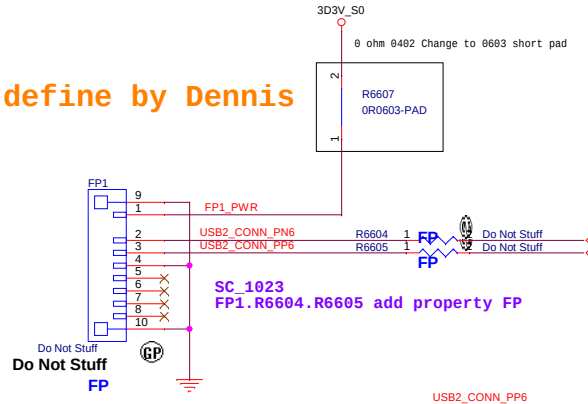
USB PORT

Analog area (AGND plane)

Audio

Cardreader

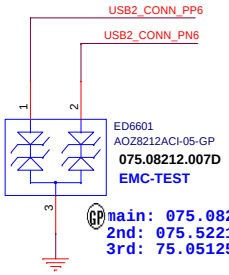
Finger print



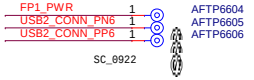
Finger print

SC_1023
FP1.R6604.R6605 add property FP

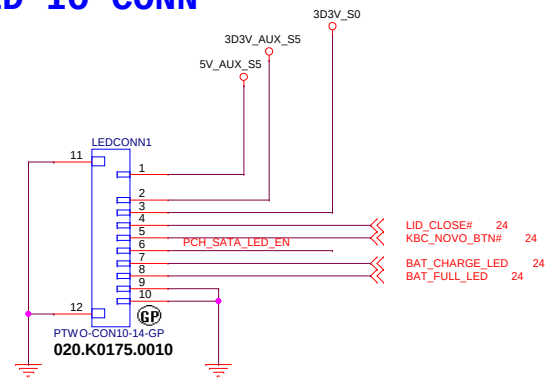
FP1
main: 020.K0032.0008
2nd: 20.K0767.008

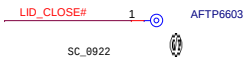


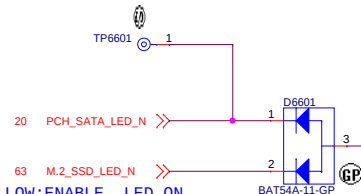
main: 075.08212.007D AOS
2nd: 075.52215.007D NXP
3rd: 75.05125.07D Amazing



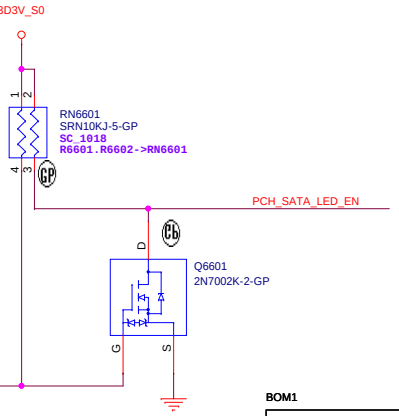
LED IO CONN







LOW:ENABLE, LED ON
HIGH:DISABLE,LED OFF



BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LEDIO_IO BOARD CONN
Size A3 / Document Number	LV315GM MB
Rev	-1
Date: Monday, April 09, 2018	Sheet 66 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

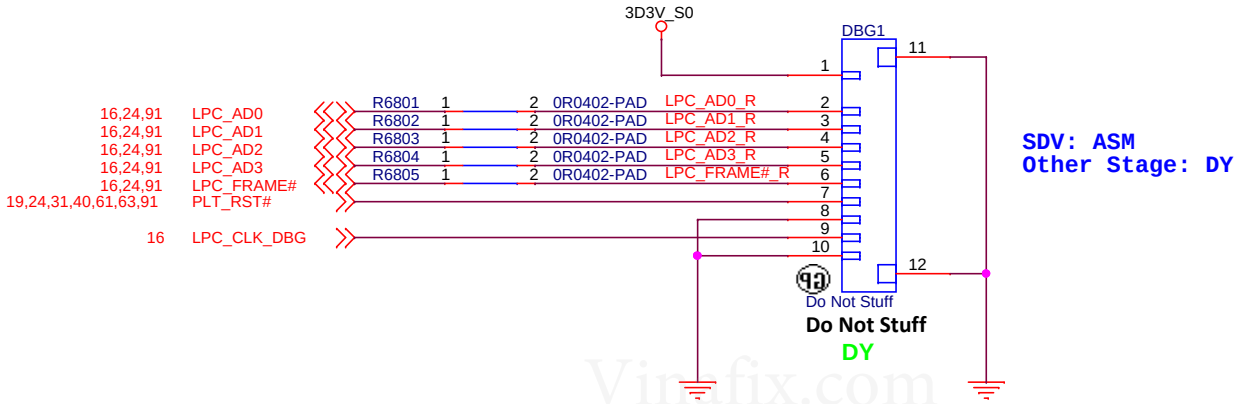
RESERVED

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 67 of 106

Main Func = Debug

Debug Connector



SDV: ASM
Other Stage: DY

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DEBUG CONN		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Monday, April 09, 2018	Sheet 68 of 106	

G-Sensor

1st:ST/ LIS3DETR, 74.00003.BB0
2nd:KX124-1051, wait PN

Blanking

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *G Sensor*		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 69 of 106	

Blanking

BOM1

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Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: -1
Date: Friday, March 30, 2018	Sheet 70 of 106	

Blanking

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Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 71 of 106	

Blanking

BOM1

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Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 72 of 106	

Blanking

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 73 of 106

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 74 of 106	

Blanking

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 75 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *GPU (1/5) PEG*		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 76 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (2/5) DIGITAL*

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 77 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (3/5) VRAM*

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 78 of 106

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*GPU (4/5) GPIO*
Size: A4	Document Number: LV315GM MB — Rev: -1
Date: Friday, March 30, 2018	Sheet 79 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (5/5) PWR/GND

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 80 of 106

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM1,2 (1/4)*		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 81 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*VRAM3,4 (2/4)*
Size: A4	Document Number: LV315GM MB
Rev	-1
Date: Friday, March 30, 2018	Sheet 82 of 106

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*VRAM5,6 (3/4)*
Size: A4	Document Number: LV315GM MB
Rev: -1	
Date: Friday, March 30, 2018	Sheet 83 of 106

Blanking

BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***VRAM7,8 (4/4)***
Size: A4	Document Number: **LV315GM MB** — Rev: **-1**
Date: Friday, March 30, 2018	Sheet 84 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	*VGA_CORE*	
Size A4	Document Number **LV315GM MB**	Rev **-1**
Date: Friday, March 30, 2018	Sheet 85 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DISCRETE VGAPOWER*		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 86 of 106	

Blanking

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserve)***

Size	Document Number	Rev
A4	LV315GM MB	-1

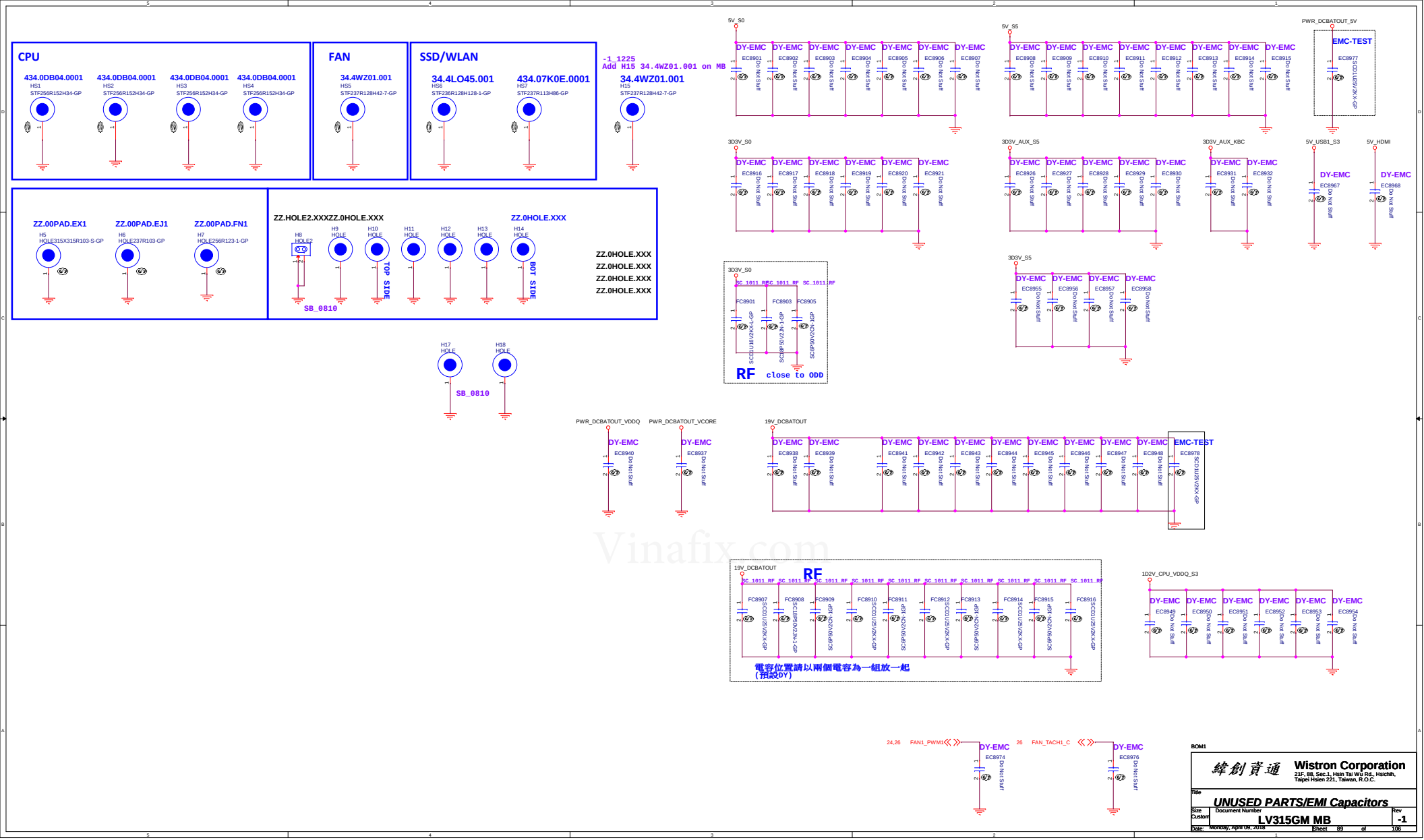
Date: Friday, March 30, 2018 Sheet 87 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserve)*	
Size A4	Document Number LV315GM MB	Rev -1
Date: Friday, March 30, 2018	Sheet 88 of 106	


CPU
434.0DB04.0001
HS1
STF256R152H34-GP
434.0DB04.0001
HS2
STF256R152H34-GP
434.0DB04.0001
HS3
STF256R152H34-GP
434.0DB04.0001
HS4
STF256R152H34-GP
FAN
34.4WZ01.001
HS5
STF237R128H42-7-GP
SSD/WLAN
34.4LO45.001
HS6
STF236R128H128-1-GP
434.07K0E.0001
HS7
STF237R113H86-GP
-1 1225
Add H15 34.4WZ01.001 on MB
34.4WZ01.001
H15
STF237R128H42-7-GP
ZZ.00PAD.EX1
H5
HOLE315X315R103-S-GP
ZZ.00PAD.EJ1
H6
HOLE237R103-GP
ZZ.00PAD.FN1
H7
HOLE256R123-1-GP
ZZ.HOLE2.XXXZZ.0HOLE.XXX
H8
HOLE2
H9
HOLE
H10
HOLE
H11
HOLE
H12
HOLE
H13
HOLE
ZZ.0HOLE.XXX
H14
HOLE
TOP SIDE
BOT SIDE
SB_0810
ZZ.0HOLE.XXX
ZZ.0HOLE.XXX
ZZ.0HOLE.XXX
ZZ.0HOLE.XXX
H17
HOLE
H18
HOLE
SB_0810
5V_S0
5V_S5
PWR_DCBATOUT_5V
EMC-TEST
3D3V_S0
3D3V_AUX_S5
3D3V_AUX_KBC
5V_USB1_S3
5V_HDMI
3D3V_S5
RF
close to ODD
PWR_DCBATOUT_VDDQ
PWR_DCBATOUT_VCORE
19V_DCBATOUT
EMC-TEST
19V_DCBATOUT
RF
電容位置請以兩個電容為一組放一起
(預設DY)
1D2V_CPU_VDDQ_S3
24,26
FAN1_PWM1
26
FAN_TACH1_C
DY-EMC
Do Not Stuff
Vinafix.com
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size
Custom
Document Number
LV315GM MB
Rev
-1
Date: Monday, April 09, 2018
Sheet 89 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

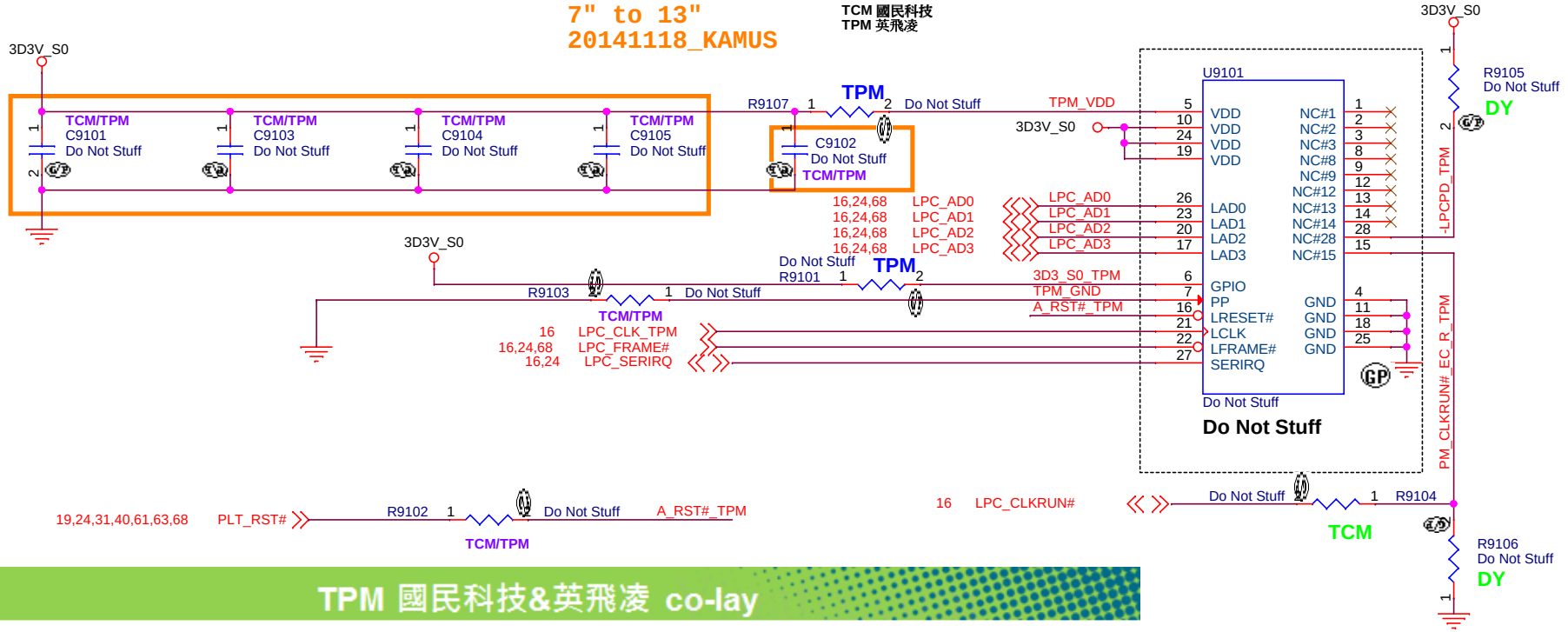
Title: ***RESERVED***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 90 of 106

TPM/TCM

TCM: 071.32320.0B0W TPM: 071.09665.0A0W



TPM 國民科技&英飛凌 co-lay

- The chip are both TSSOP-28 package

Pin define	國民	英飛凌	Remark	Pin define	國民	英飛凌	Remark
1	NC	NC		15	CLKRUN#	NC	0ohm
2	NC	NC		16	LRESET#	LRESET#	
3	NC	NC		17	LAD3	LAD3	
4	GND	GND		18	GND	GND	
5	NC	VDD	0ohm	19	VDD	VDD	
6	NC	GPIO	0ohm	20	LAD2	LAD2	
7	NC	PP	0ohm	21	LCLK	LCLK	33ohm for 國民
8	NC	NC		22	LFRAME#	LFRAME#	
9	NC	NC		23	LAD1	LAD1	
10	VDD	VDD		24	VDD	VDD	
11	GND	GND		25	GND	GND	
12	NC	NC		26	LAD0	LAD0	
13	NC	NC		27	SIRQ	SERIRQ	
14	NC	NC		28	LPCPD#	NC	0ohm

BOM1

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Monday, April 09, 2018	Sheet 91 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *(RESERVED)*		
Size: A4	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 92 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 93 of 106

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 94 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 95 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 96 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: **-1**
Date: Friday, March 30, 2018	Sheet 97 of 106	

Blanking

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **LV315GM MB**	Rev: -1
Date: Friday, March 30, 2018	Sheet 98 of 106	

BOM1

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Monday, April 09, 2018 Sheet 99 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 100 of 106

Blanking

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

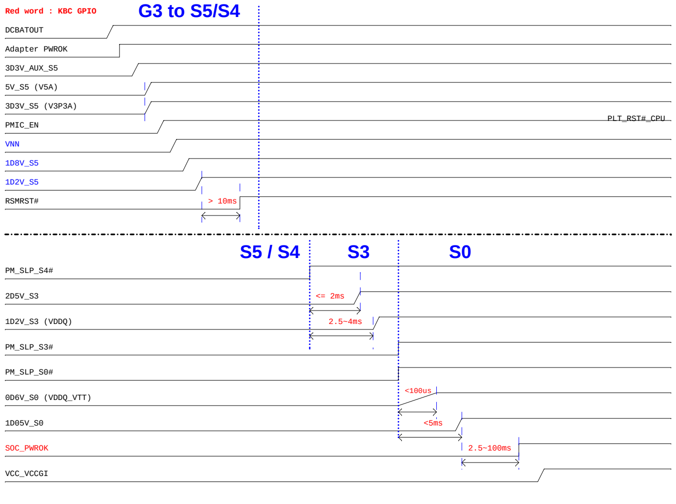
Title

Change History

Size	Document Number	Rev
A4	LV315GM MB	-1

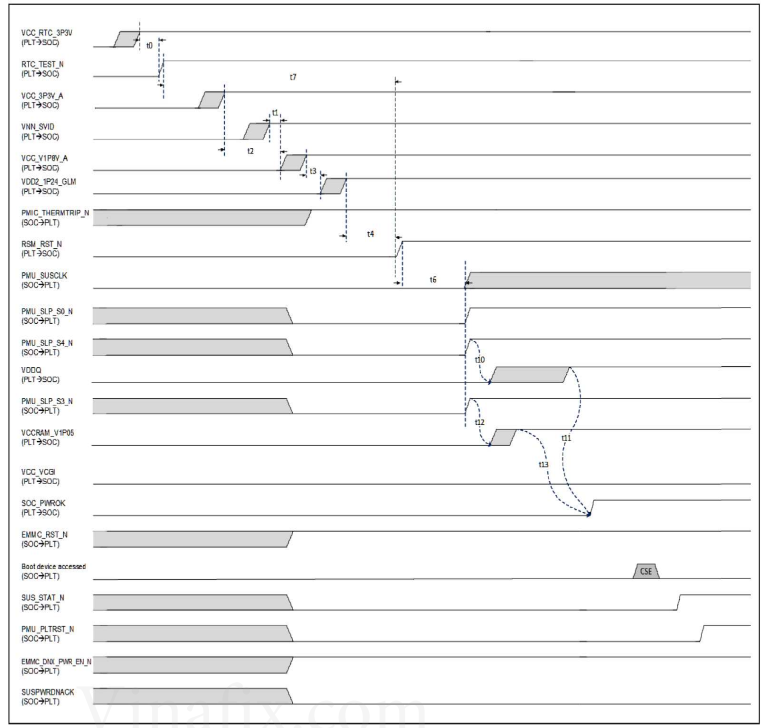
Date: Friday, March 30, 2018 Sheet 101 of 106

Intel-Power Up Sequence

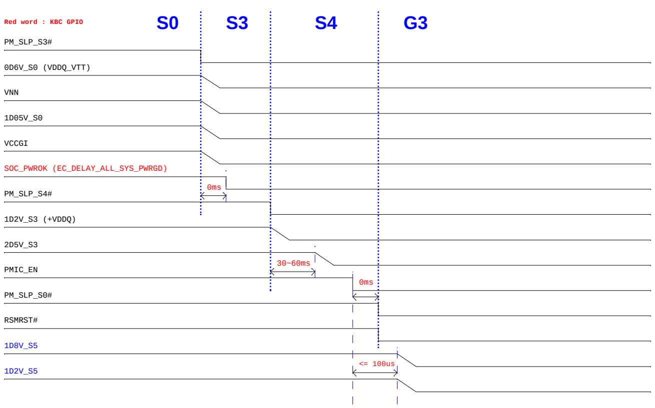


Gemini Lake Sequence

Gemini Lake G3 Cold Boot Power-Up



Intel-Power Down Sequence



PMIC Sequence

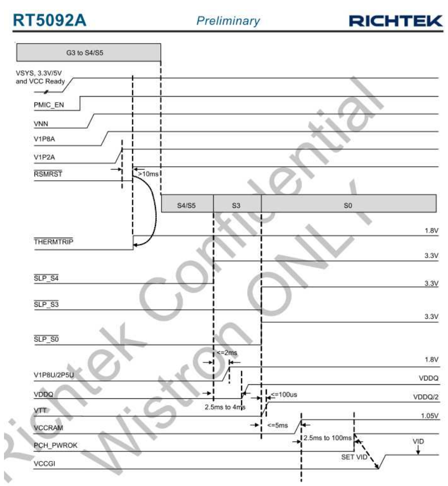
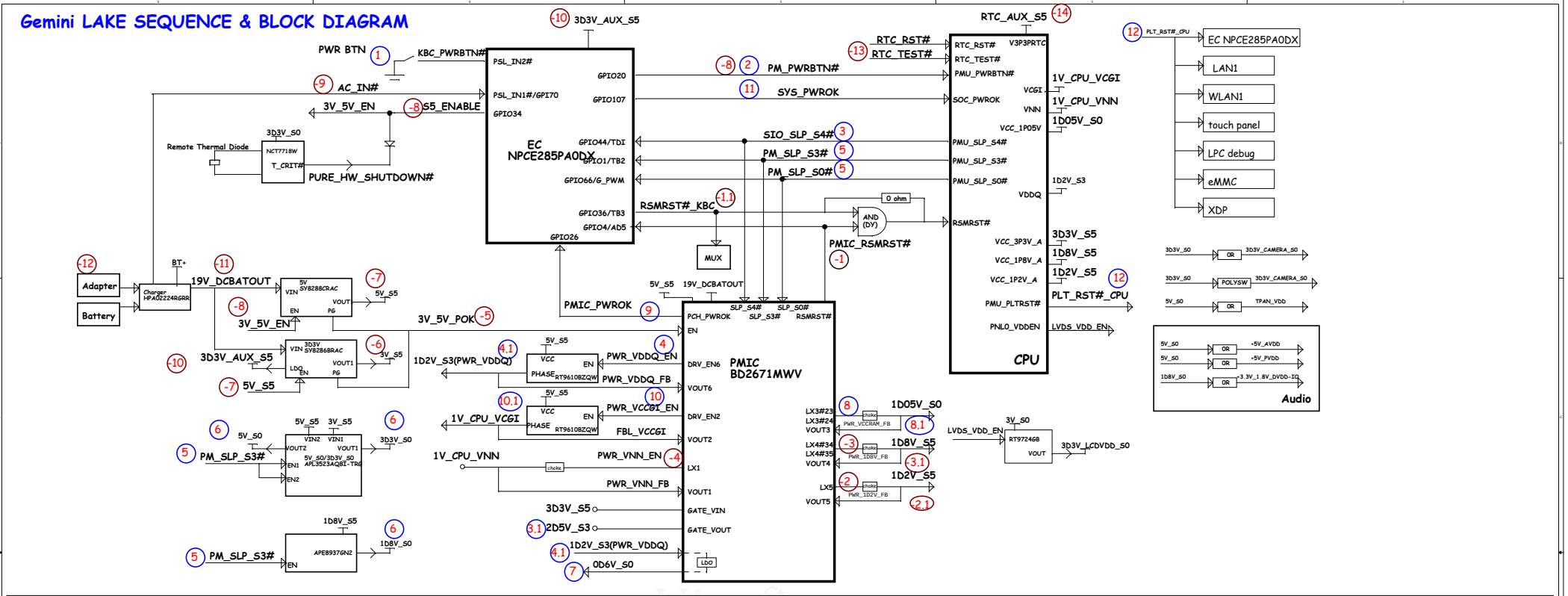
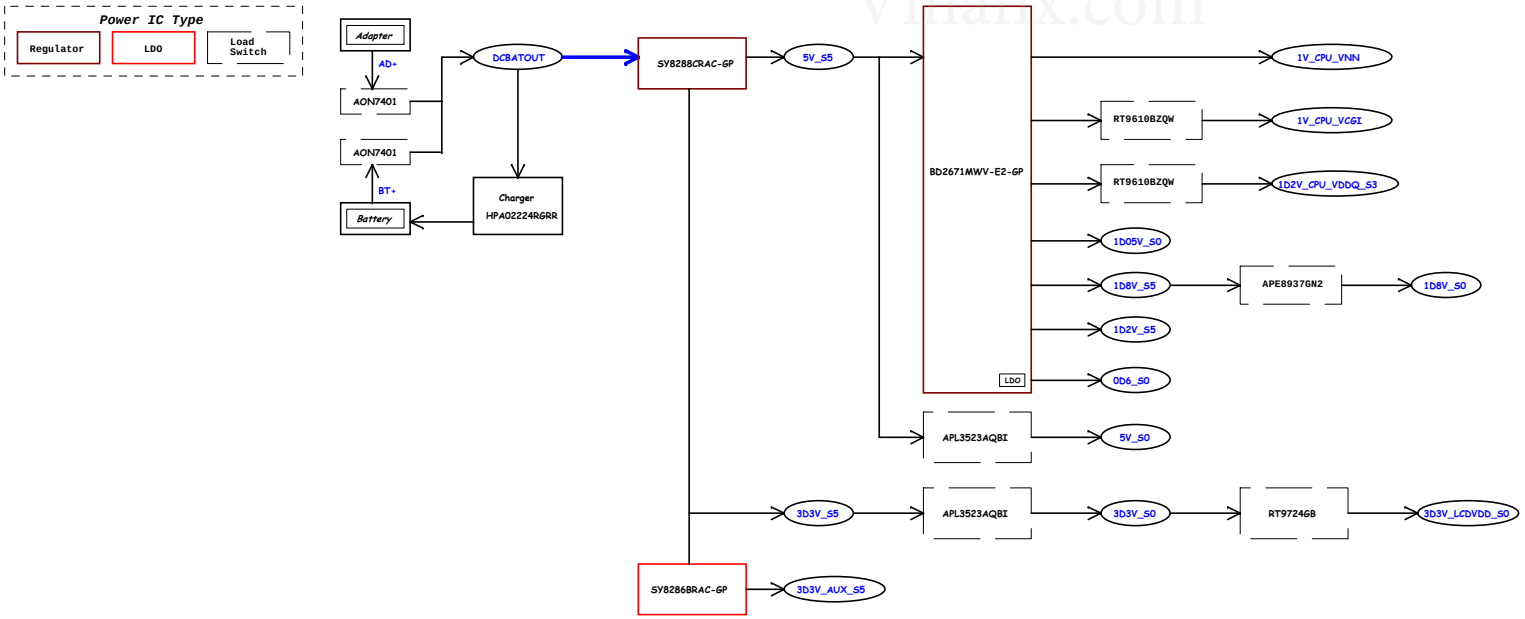


Figure 3. Power on Sequence

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Power Sequence
Size A3 / Document Number	LV315GM MB
Rev	-1
Date	Friday, March 30, 2018
Sheet	102 of 106

Gemini LAKE SEQUENCE & BLOCK DIAGRAM





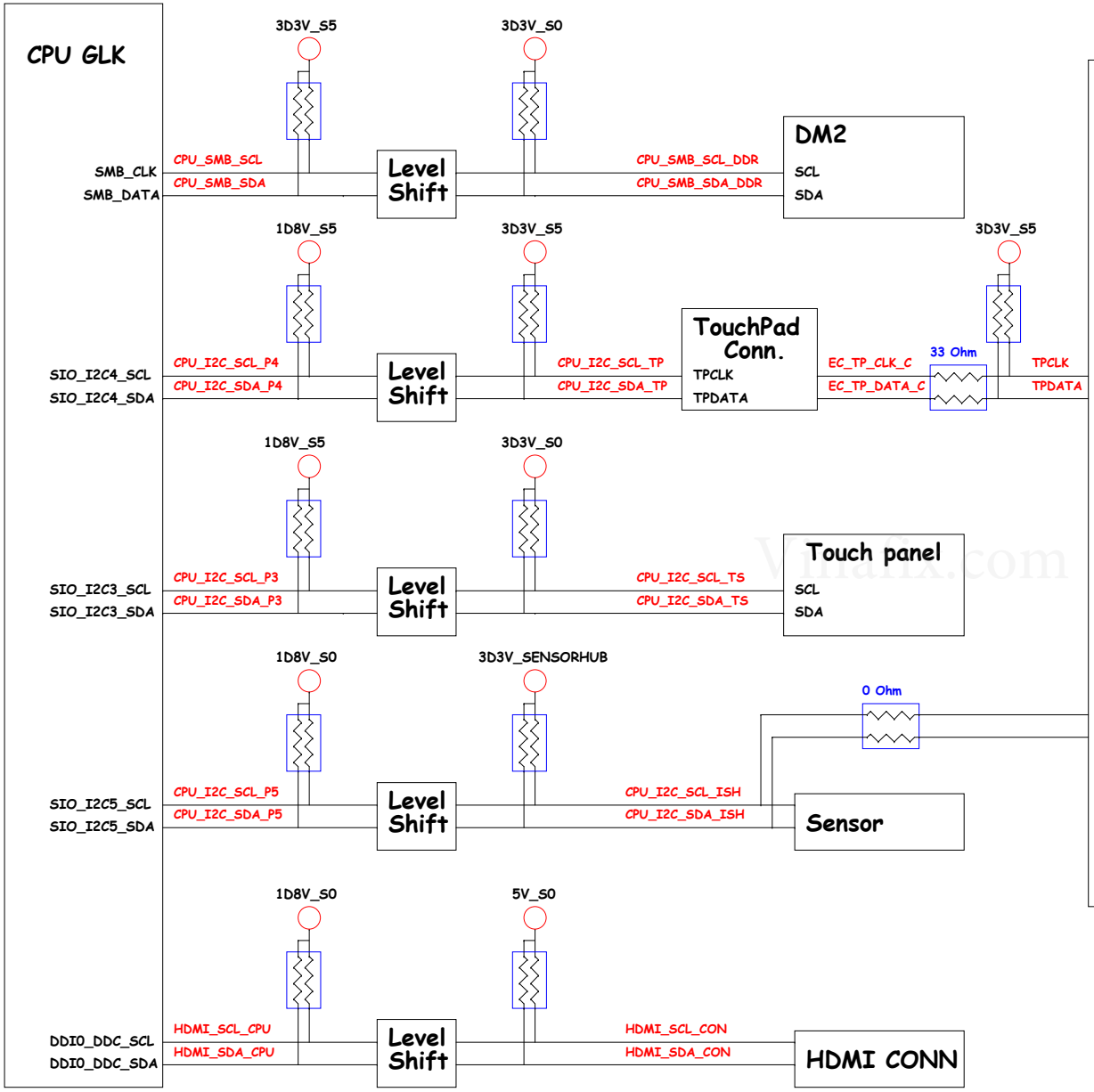
Wistron Corporation

Power Block Diagram

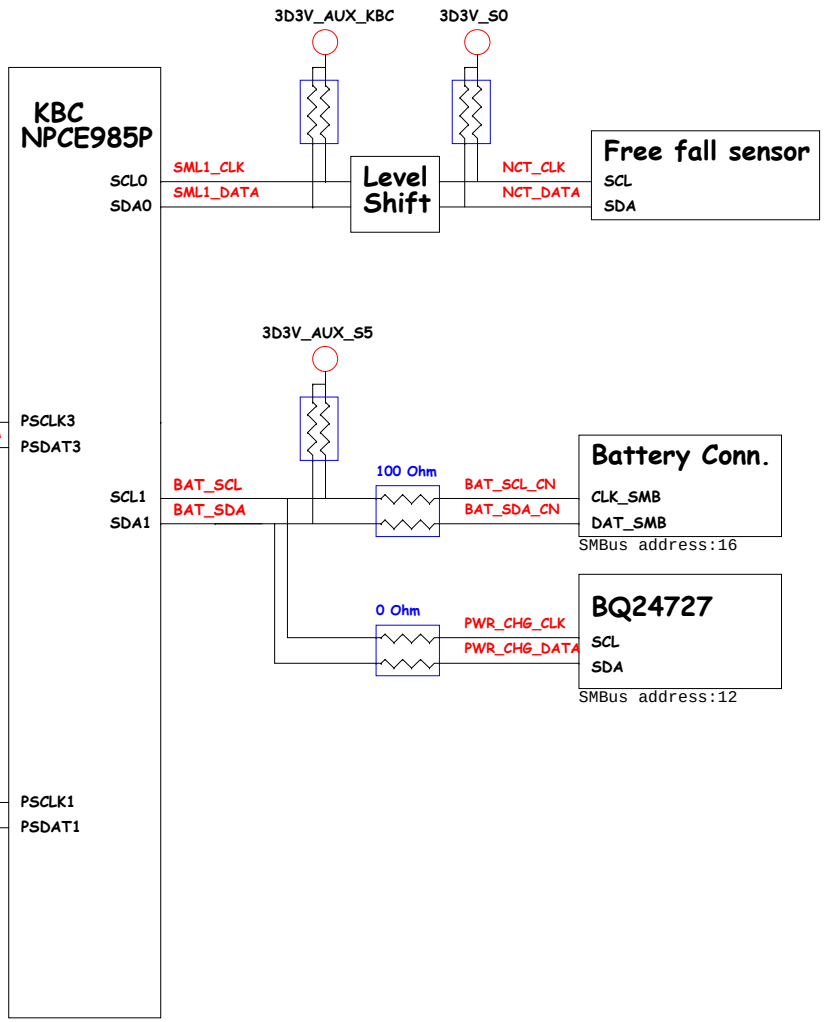
LV315GM MB

-1

PCH SMBus Block Diagram



KBC SMBus Block Diagram



BOM1

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Title: SMBUS BLOCK DIAGRAM		
Size: A3	Document Number: LV315GM MB	Rev: -1
Date: Friday, March 30, 2018	Sheet 104 of 106	

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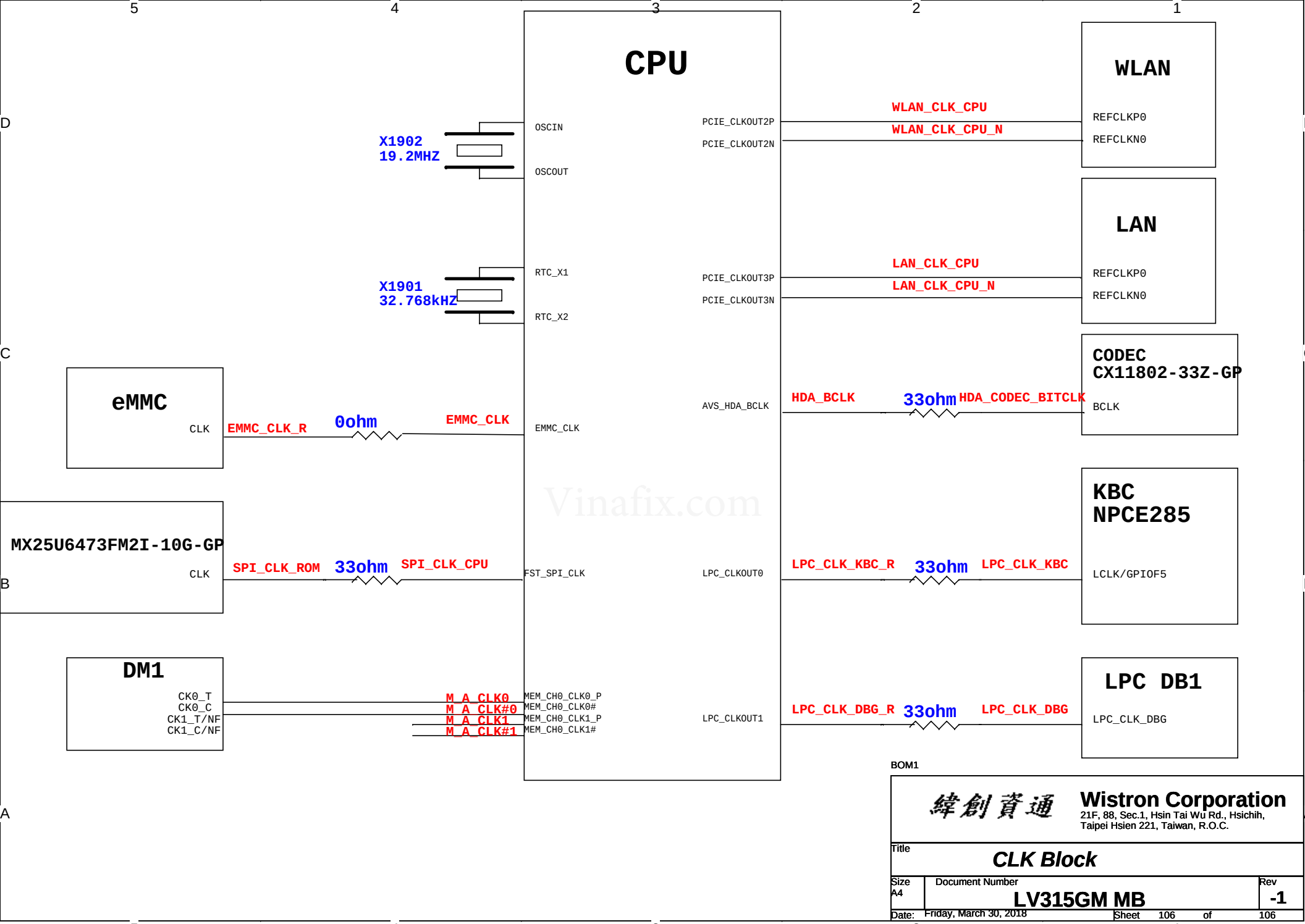
Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 105 of 106



BOM1

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Title: ***CLK Block***

Size	Document Number	Rev
A4	LV315GM MB	-1

Date: Friday, March 30, 2018 Sheet 106 of 106