COMPAL CONFIDENTIAL

MODEL NAME : ZAM80

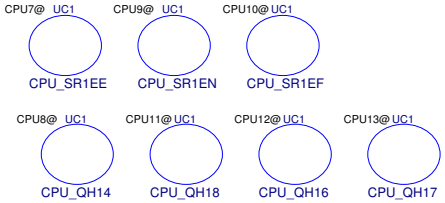
PCB NO : DA8000Z7010

BOM P/N : 4319R831LXX

GPIO MAP: 3.6C

~~CPU2@:SA00007OS0L(S IC A31 CL8065801674128 QG21 C0 1.2G)~~
~~CPU3@:SA00007AM0L(S IC A31 CL8064701614813 QFSY C0 1.6G)~~
~~CPU4@:SA00007UH0L(S IC A31 CL8065801703603 QGHB D0 1.6G)~~
~~CPU5@:SA00007U90L(S IC A31 CL8065801703601 QGH9 D0 1.8G)~~
~~CPU6@:SA00007UG0L(S IC A31 CL8065801703602 QGHA D0 1.6G)~~

HSW CPU:
CPU7@:SA00007MU2L(S IC CL8064701477600 SR1EE D0 2G BGA1168)
CPU9@:SA00007TA0L(S IC CL8064701552900 SR1EN D0 1.9G BGA)
CPU10@:SA00007LO2L(S IC CL8064701477802 SR1EF D0 1.7G BGA)
BDW CPU:
CPU8@:SA00008390L(S IC A31 FH8065801618302 QH14 E0 2.2G)
CPU11@:SA000083D0L(S IC A31 FH8065801620403 QH18 E0 2G)
CPU12@:SA000083B0L(S IC A31 FH8065801620103 QH16 E0 2G)
CPU13@:SA000083C0L(S IC A31 FH8065801620203 QH17 E0 2G)



1 chip XDP debug component list(CXDP@)			
item	Qty	Part reference	Part description
1	2	CC17,CC21	SE00000G880 (S CER CAP 0.1U 25V K X5R 0402)
2	4	RC98,RC99,RC109,RC112	SD028000080 (S RES 1/16W 0 +-5% 0402)
3	4	RC102,RC106,RC113,RC120	SD028100180 (S RES 1/16W 1K +-5% 0402)
4	1	UC7	SA00005X900 (S IC 74CBTLV3126BQ DHVQFN 14P BUS SWITCH)
5	1	JXDP1	SP02000L900 (S W-CONN SAMTEC BSH-030-01-L-D-A-TR 60P)

Huston 15" UMA

Broadwell U

2014-07-16

REV : 1.0 (A00)

@ : Nopop Component
EMC@ : EMI, ESD and RF Component
@EMC@ : EMI, ESD and RF Nopop Component
CXDP@ : XDP Component
VPRO@ : Support VPRO
NVPRO@ : Support NON-VPRO
CONN@ : Connector Component
HSW@ : HSW CPU
BDW@ : BDW CPU

Layout Dell logo

REV: A00
PWB: MOYKF

MB PCB

Part Number	Description
DAZ13M00100	PCB ZAM80 LA-A911P LS-A911P/A912P/A913P 02

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Title: Cover Sheet

Size | Document Number: LA-A911P | Rev: 0.5

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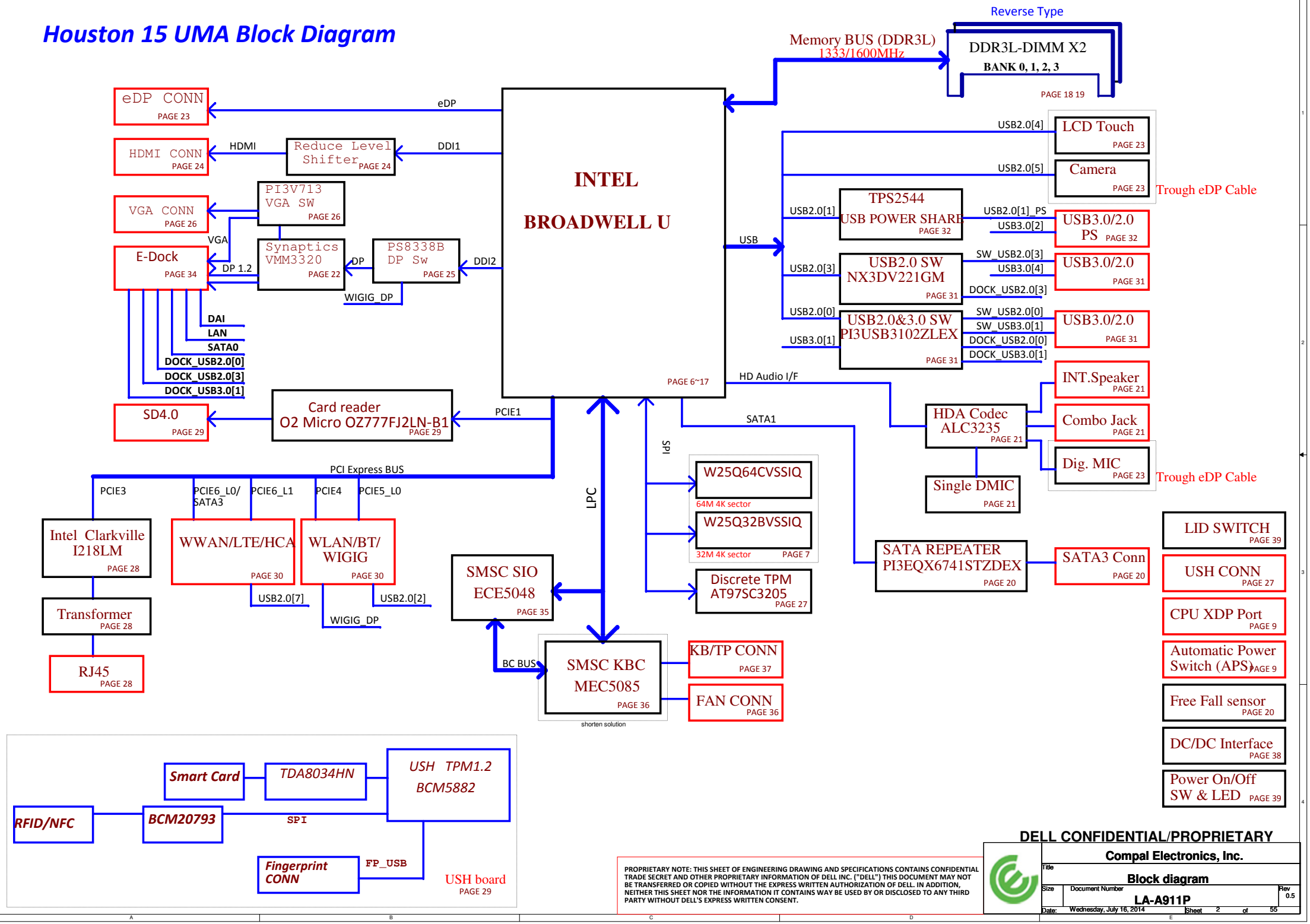
Houston 15 UMA Block Diagram



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Title: Block diagram

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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN
PCIE 5			WIGIG
PCIE 6	L3	SATA 0	JDOCK1 (DOCK)
	L2	SATA 1	JSATA1 (HDD)
	L1	SATA 2	NA
	L0	SATA 3	HCA

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1
	1	JUSB3
	2	BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA

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Title: Port assignment

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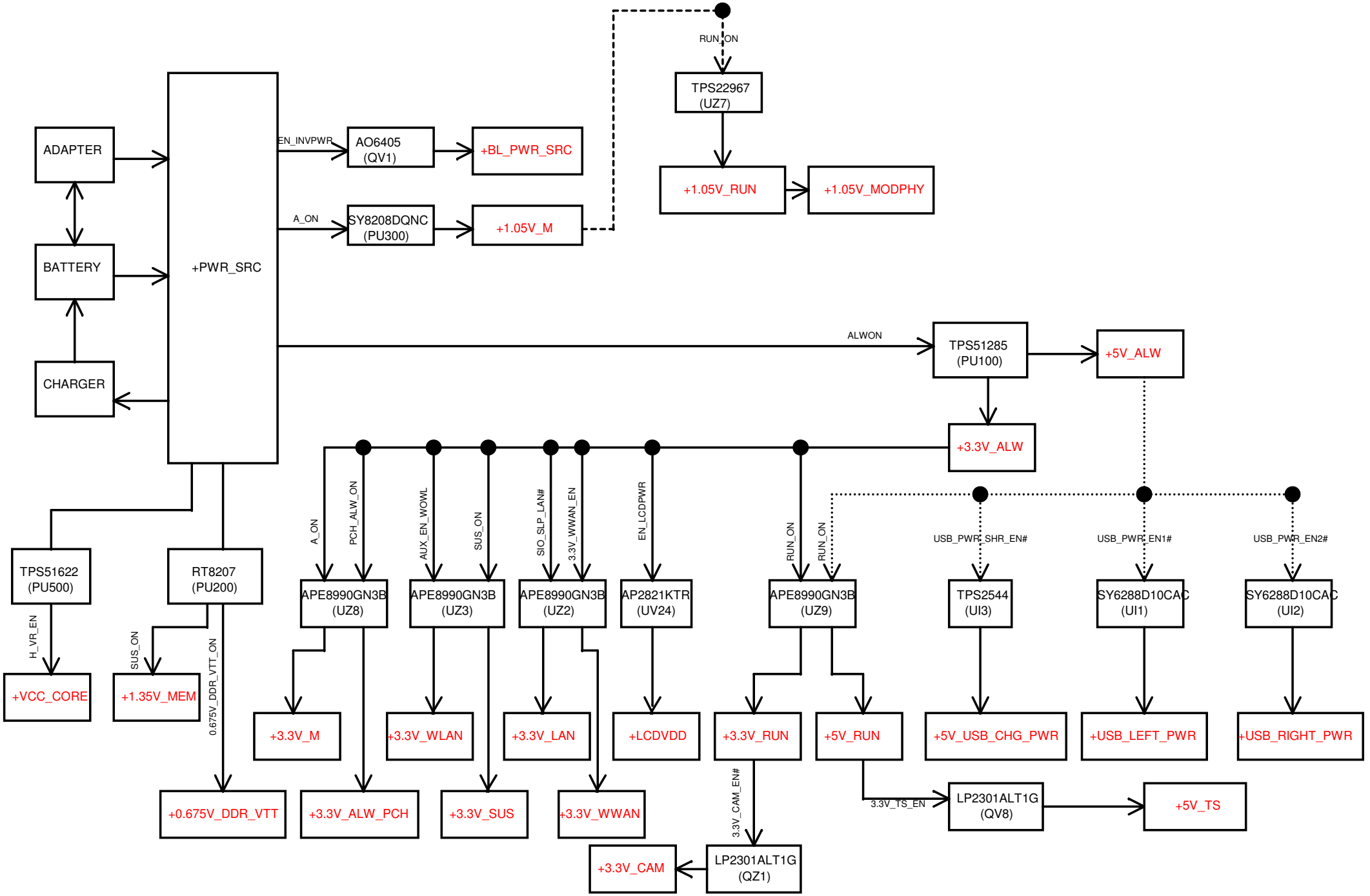

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Title: Power rails

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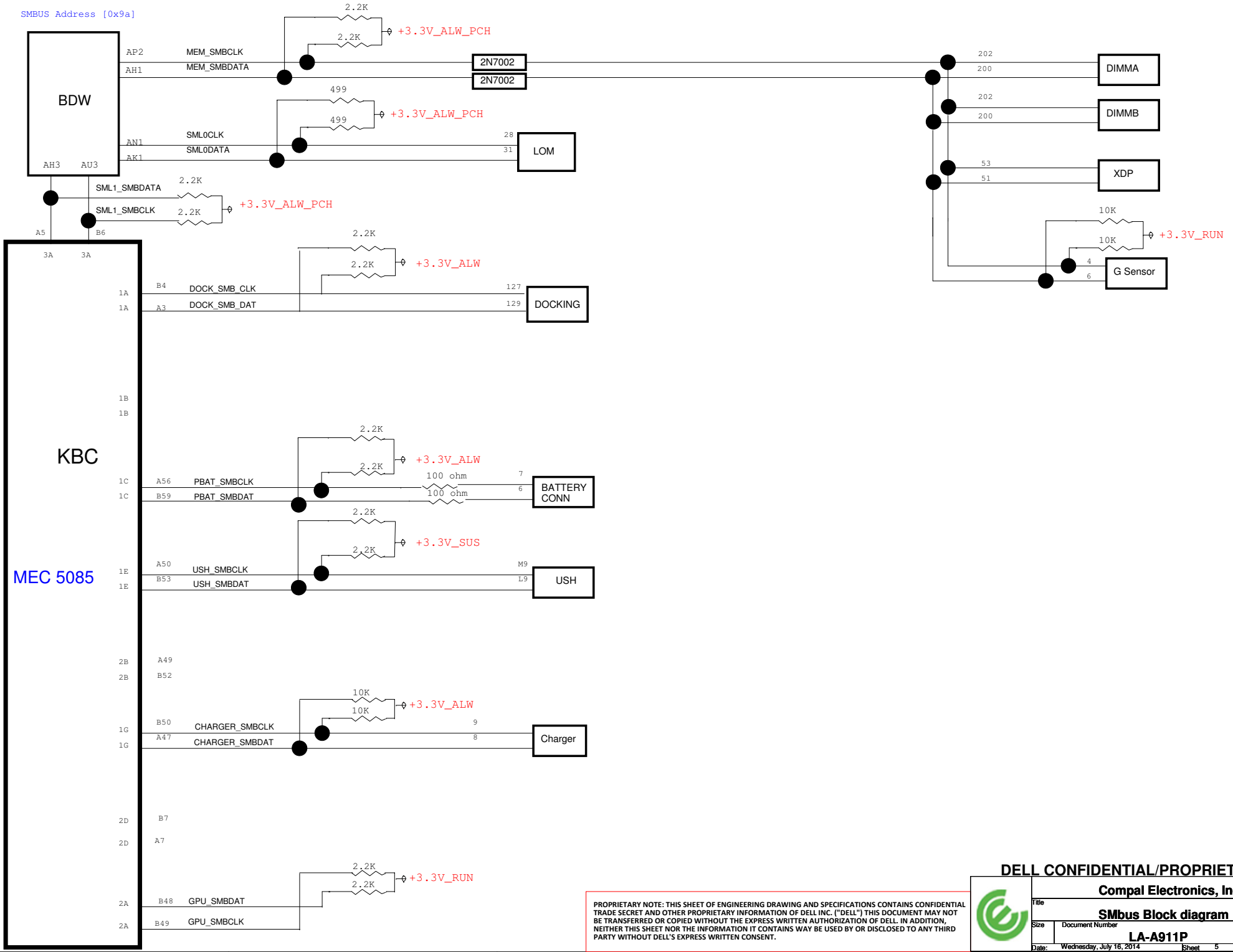

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Size	Document Number: LA-A911P
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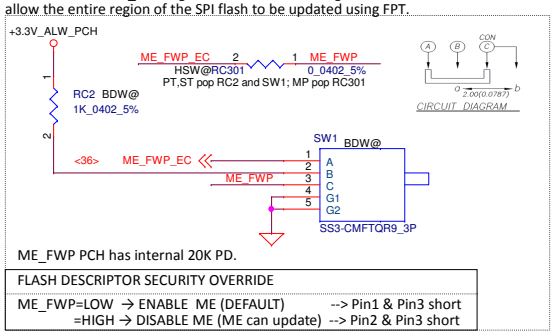
UMA SATA port

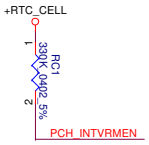
SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H12 Entry	NA	NA	
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H14U_En	NA	NA	
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H15D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H15U_En	NA	Express card	contact to Express card

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

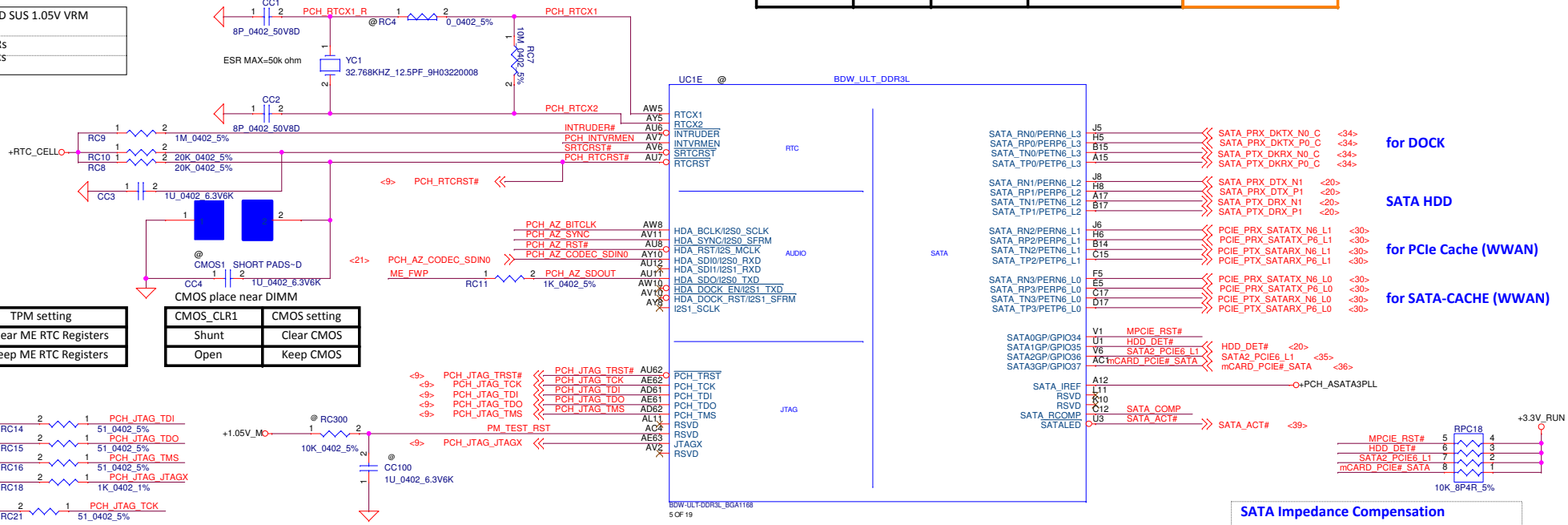


ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE	
ME_FWP=LOW → ENABLE ME (DEFAULT)	--> Pin1 & Pin3 short
=HIGH → DISABLE ME (ME can update)	--> Pin2 & Pin3 short



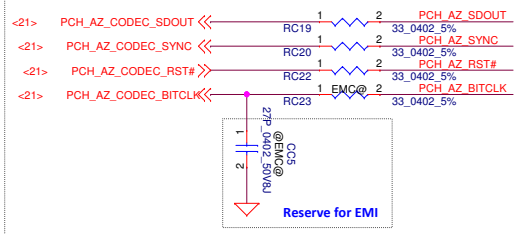
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs



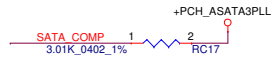
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

HDA for Codec



SATA Impedance Compensation



CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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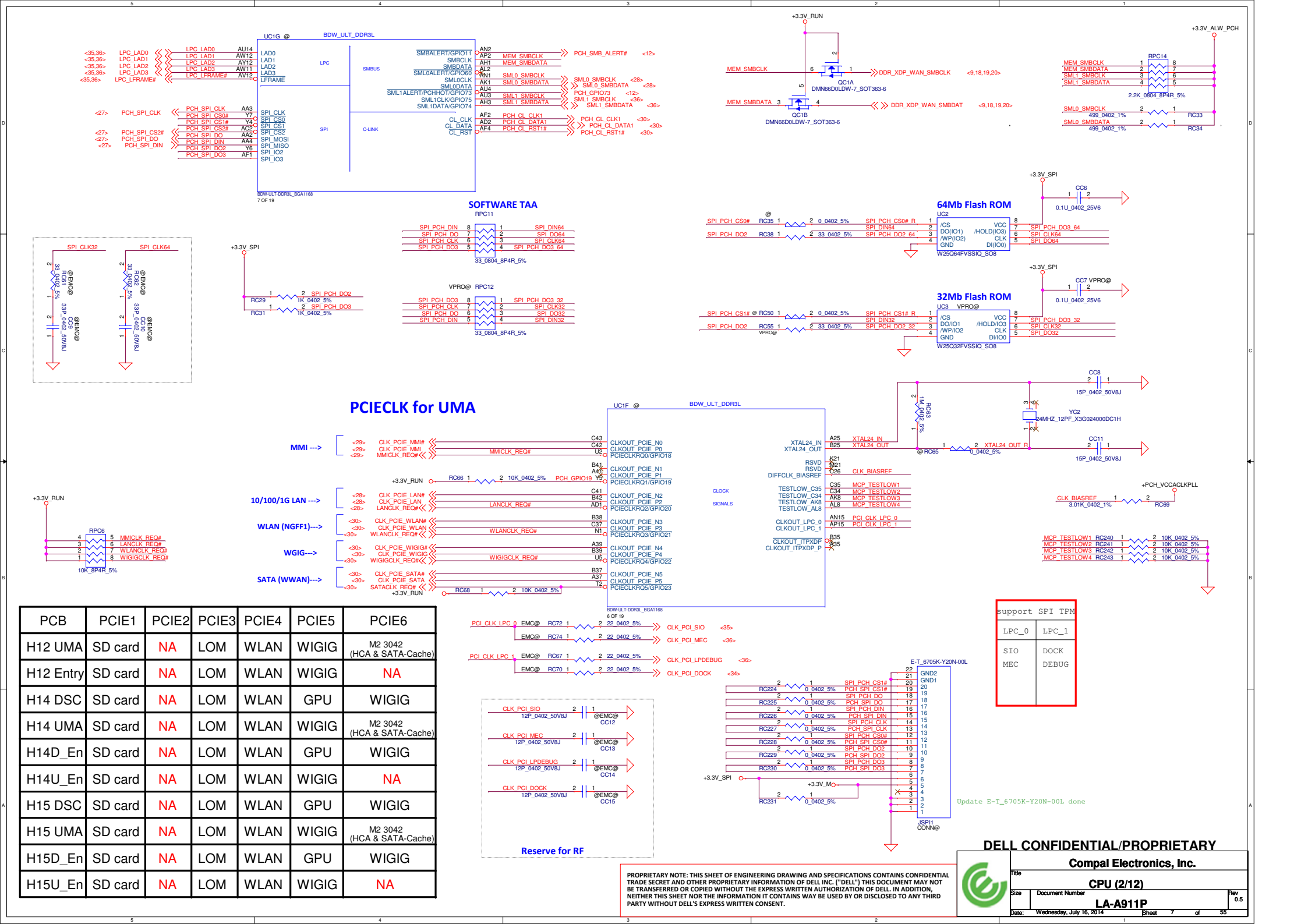

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA

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Title: CPU (2/12)

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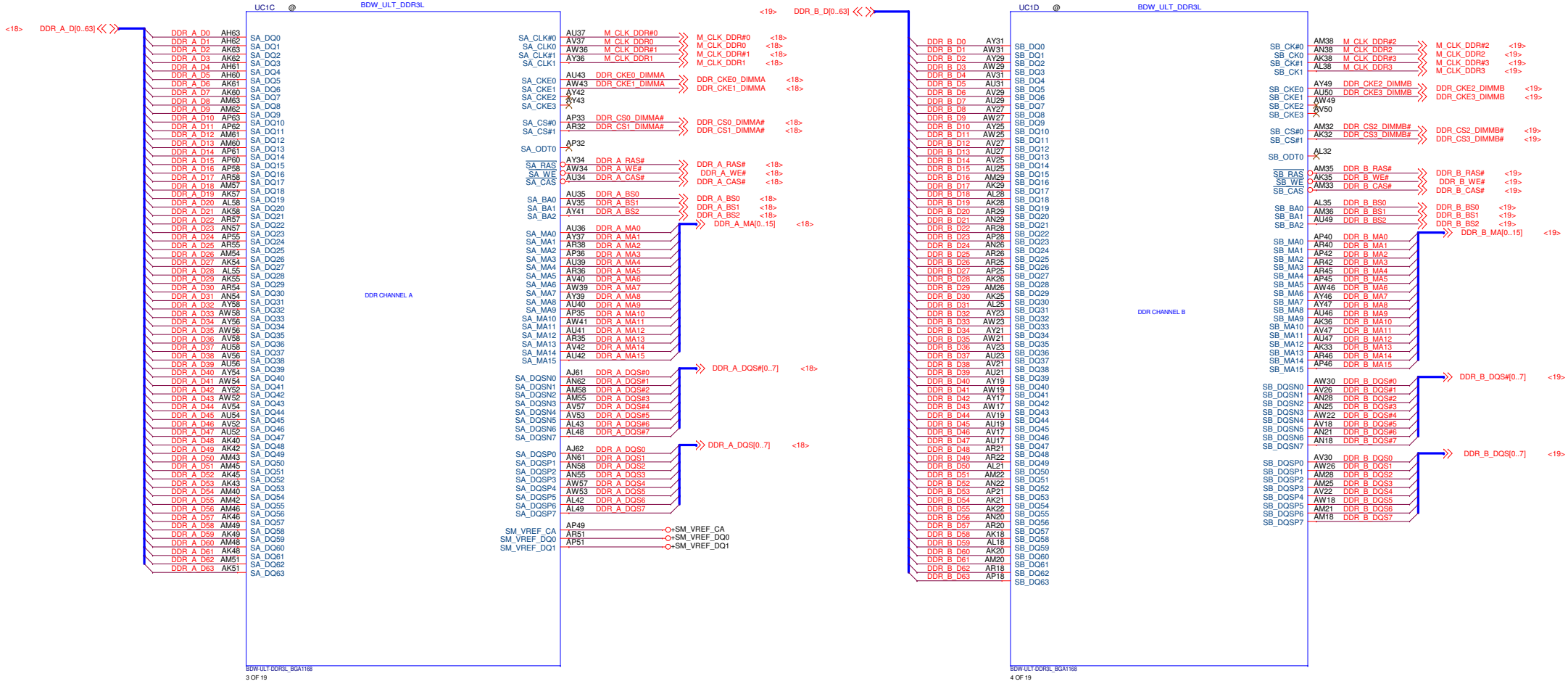

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Title: CPU (3/12)

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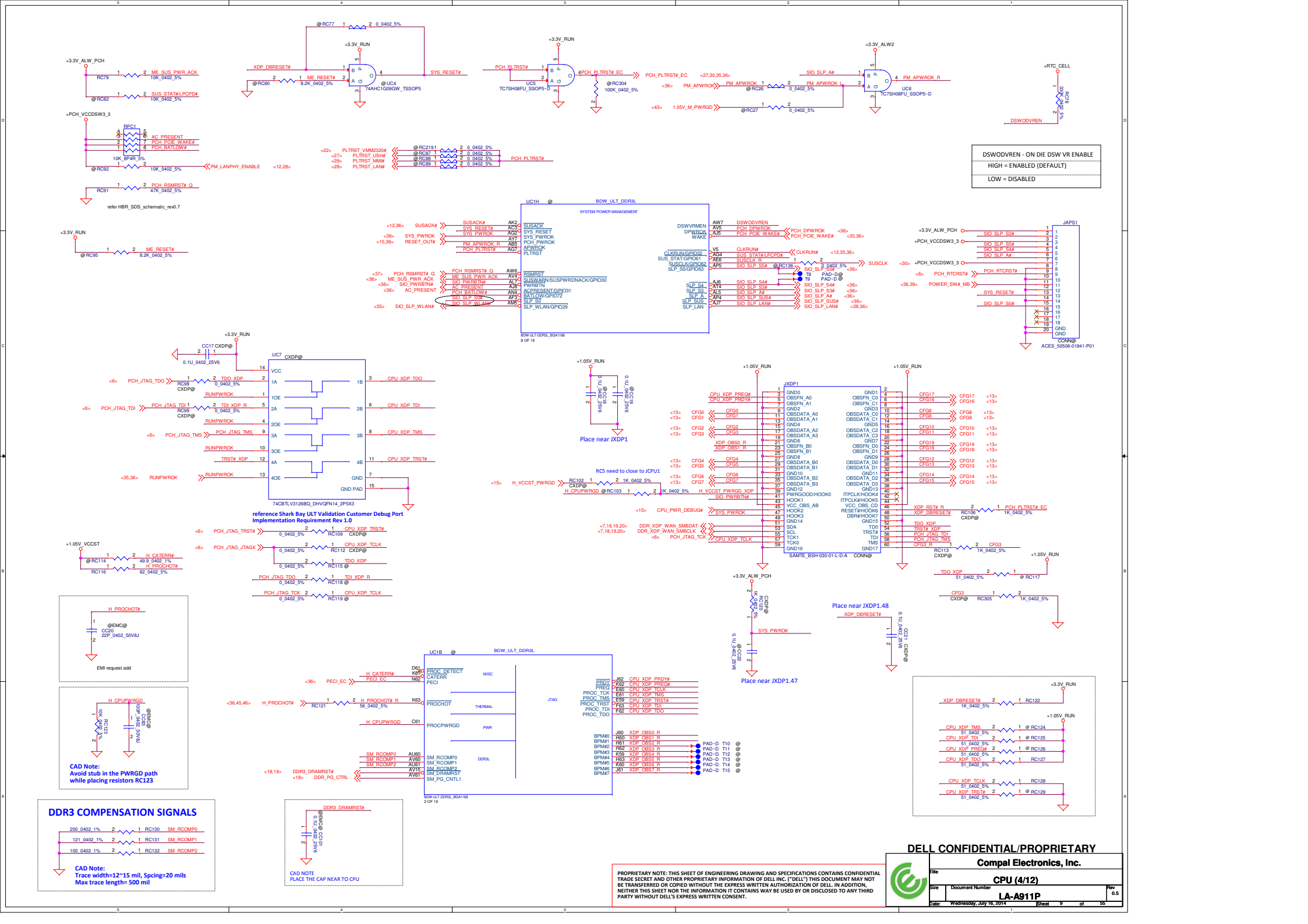
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
DDR3 COMPENSATION SIGNALS
CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC123
CAD NOTE
PLACE THE CAP NEAR TO CPU
reference Shark Bay ULT Validation Customer Debug Port
Implementation Requirement Rev 1.0
Place near JXDP1
Place near JXDP1.48
Place near JXDP1.47
RCS need to close to JCPU1
EMI request add
UC1H @ BDW_ULT_DDR3L
SYSTEM POWER MANAGEMENT
UC1B @ BDW_ULT_DDR3L
UC7 CXDP@
74CBTLV3126BQ_DHVQFN14_2P5X3
JXDP1
SAMTE_BSH-030-01-L-D-A
JAPS1
ACES_50506-01841-P01
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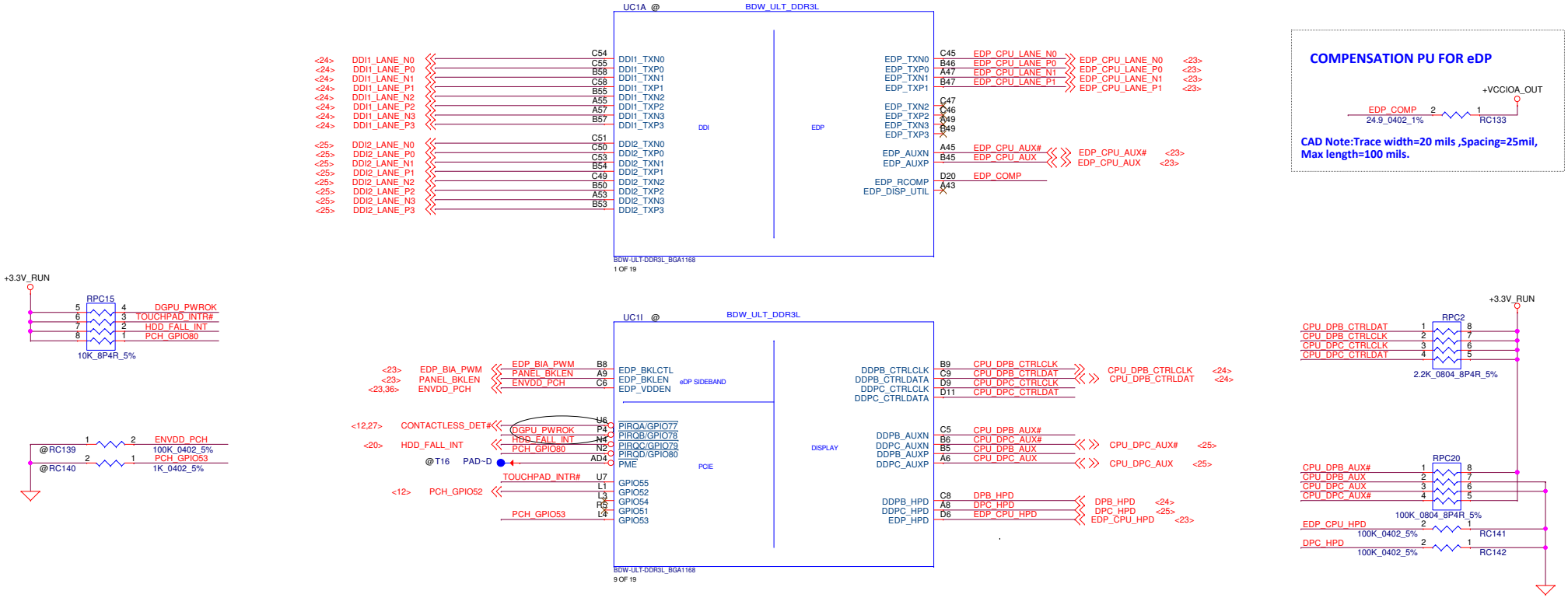

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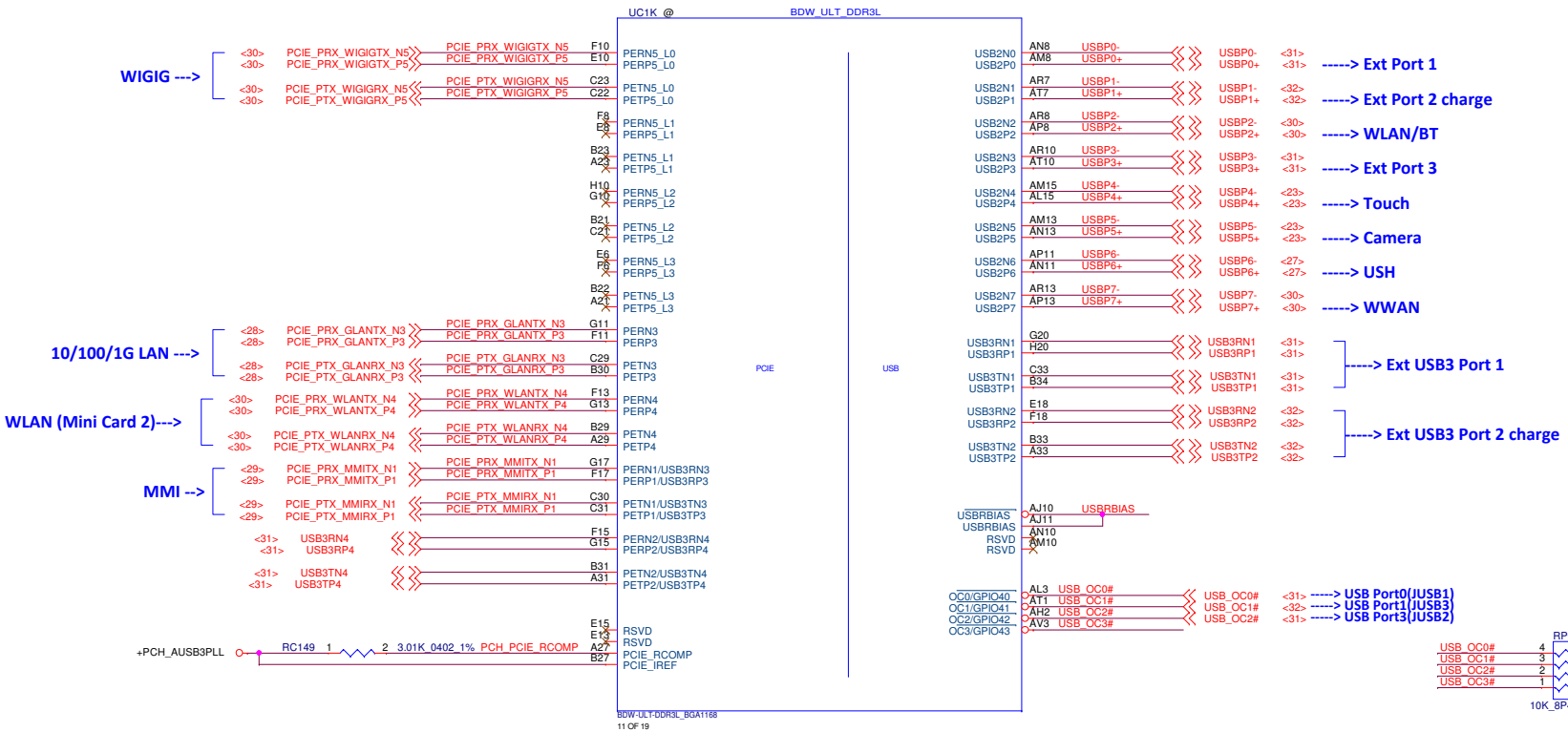
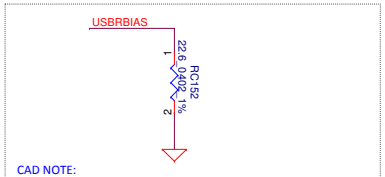
PCIE for UMA



PCB	USB2 7
H12 UMA	WWAN
H12 Entry	NA
H14 DSC	WWAN
H14 UMA	WWAN
H14D_En	NA
H14U_En	NA
H15 DSC	WWAN
H15 UMA	WWAN
H15D_En	NA
H15U_En	NA

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA



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Title: CPU (6/12)

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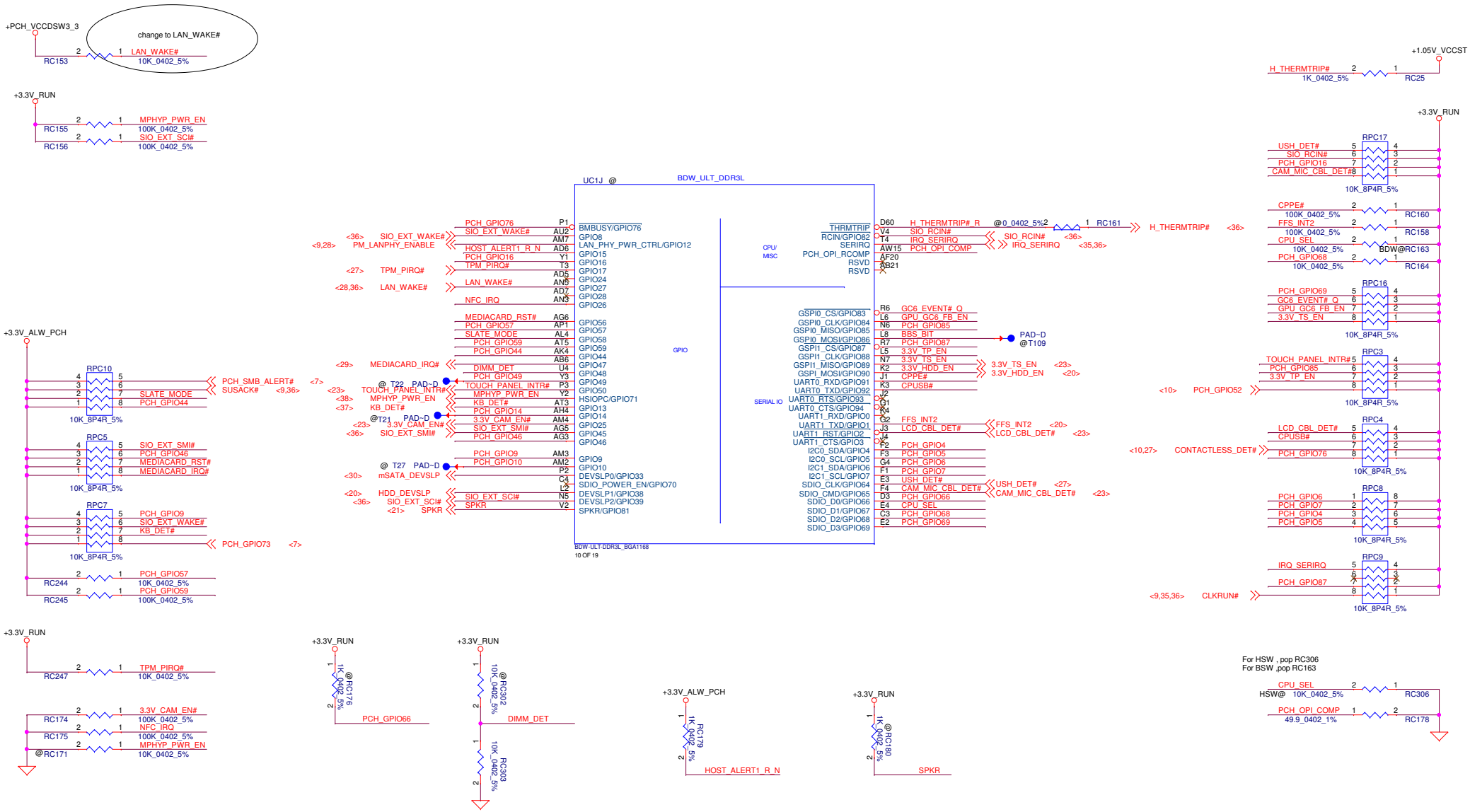

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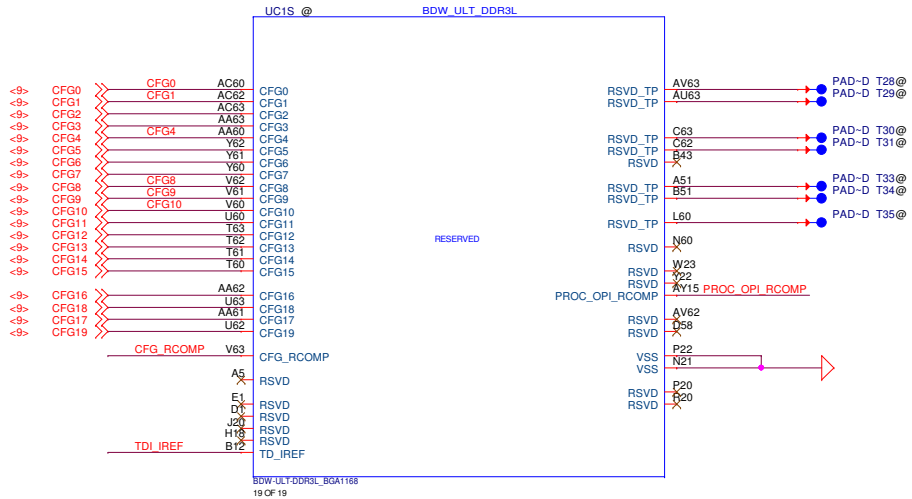
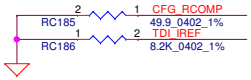
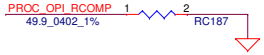
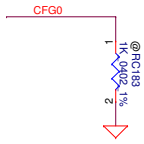
CFG STRAPS for CPU

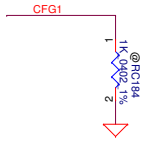




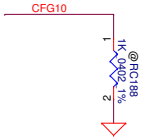


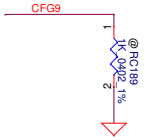


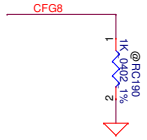
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

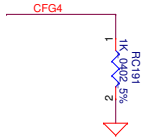


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: CPU (8/12)

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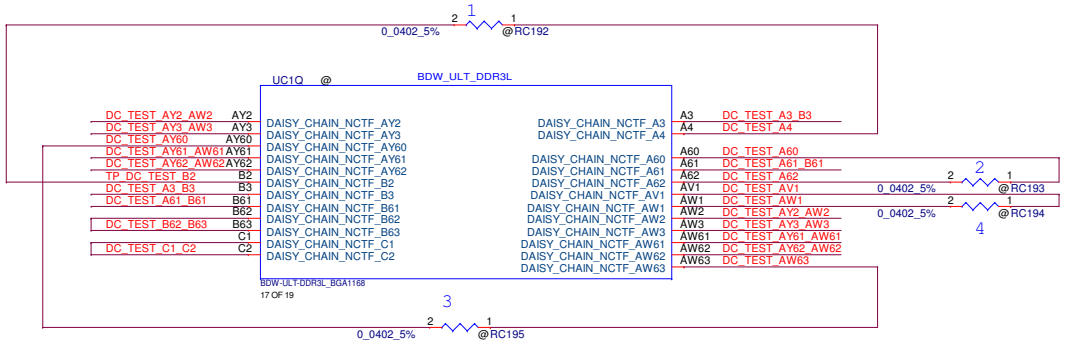
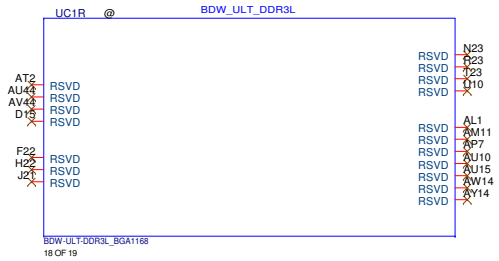


Package Daisy Chain:

1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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Title: CPU (9/12)

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ESD Request

+1.05V_RUN +VCCIO_OUT
@RC196 2 1 0_0603_5%

RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES

+VCC_CORE +1.35V_MEM
@EMC@CC23 1 2 22U_0603_6.3V6M

+1.05V_RUN +VCC_CORE
@EMC@CC79 1 2 22U_0603_6.3V6M
@EMC@CC84 1 2 22U_0603_6.3V6M

+1.05V_RUN +3.3V_RUN
@EMC@CC85 1 2 22U_0603_6.3V6M

H_VCCST_PWRGD
1 @EMC@ 2 CC24 100P_0402_50V8J

+1.35V_MEM

VDDQ DECOUPLING

2.2U_0402_6.3V6M @CC25
2.2U_0402_6.3V6M @CC26
2.2U_0402_6.3V6M CC27
2.2U_0402_6.3V6M CC28
10U_0603_6.3V6M CC29
10U_0603_6.3V6M @CC30
10U_0603_6.3V6M CC31
10U_0603_6.3V6M CC32
10U_0603_6.3V6M @CC33
10U_0603_6.3V6M CC34

+1.05V_RUN
150_0402_5% RC197
CPU_PWR_DEBUG#
10K_0402_5% @RC198

+1.05V_VCCST
10K_0402_5% @RC199
H_VR_EN 1.5K_0402_5% RC201 H_VR_READY

+1.05V_VCCST
+3.3V_ALW
UC8
NC VCC
A
GND Y
@CC35 0.1U_0402_25V6
<9,36> RESET_OUT#
H_VCCST_PWRGD
1K_0402_5% RC202
74AUP1G07GW_TSSOP5

SVID ALERT

+1.05V_VCCST
75_0402_1% RC204
CAD Note: Place the PU resistors close to CPU RC204 close to CPU 300 - 1500mils
<45> VIDALERT_N
43_0402_5% RC207 H_CPU_SVIDALRT#

SVID DATA

+1.05V_VCCST
110_0402_1% RC208
CAD Note: Place the PU resistors close to CPU RC208close to CPU 300 - 1500mils
<45> VIDSOUT VIDSOUT

VCC_SENSE

+VCC_CORE
100_0402_1% RC209
<45> VCCSENSE VCCSENSE
CAD Note: RC209 SHOULD BE PLACED CLOSE TO CPU

+1.05V_RUN +1.05V_VCCST
@PJP23
PAD-OPEN1x1m
22U_0603_6.3V6M CC36
1U_0402_6.3V6K @CC37

+1.35V_MEM +VCC_CORE

UC1L @ BDW_ULT_DDR3L

L59 J59 RSVD
AH26 AJ31 AJ33 AJ37 AN33 AP43 AR48 AY35 AY40 AY44 AY50 VDDQ
F59 N58 AC58 VCC RSVD RSVD
VCCSENSE E63 VCC_SENSE
AB23 RSVD
+VCCIO_OUT A59 VCCIO_OUT
+VCCIOA_OUT E20 VCCIOA_OUT
AD23 AA23 AE59 RSVD RSVD RSVD
H_CPU_SVIDALRT# L62 VIDALERT
<45> VIDSCLK N63 VIDSCLK
L63 VIDSOUT
<9> H_VCCST_PWRGD B59 VCCST_PWRGD
<45> H_VR_EN F60 VR_EN
<45> H_VR_READY C59 VR_READY
HSW ULT POWER
D63 H59 VSS
<9> CPU_PWR_DEBUG# P62 PWR_DEBUG
P60 VSS
@T74 PAD-D P61 RSVD_TP
@T75 PAD-D N59 RSVD_TP
@T76 PAD-D N61 RSVD_TP
@T77 PAD-D T59 RSVD_TP
AD60 AD59 AA59 AE60 AC59 AG59 U59 V59 RSVD
+1.05V_VCCST AC22 AE22 AE23 VCCST
+VCC_CORE AB57 AD57 AG57 C24 C28 C32 VCC
BDW-ULT-DDR3L_BGA1168
12 OF 19

C36 C40 C44 C48 C52 C56 E23 E25 E27 E29 E31 E33 E35 E37 E39 E41 E43 E45 E47 E49 E51 E53 E55 E57 F24 F28 F32 F36 F40 F44 F48 F52 F56 G23 G25 G27 G29 G31 G33 G35 G37 G39 G41 G43 G45 G47 G49 G51 G53 G55 G57 H23 J23 K23 K57 L22 M23 M57 P57 U57 W57 VCC

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Title: CPU (10/12)
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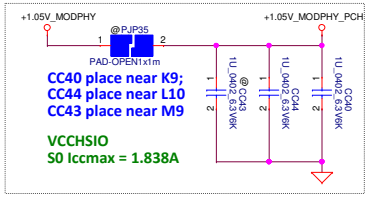
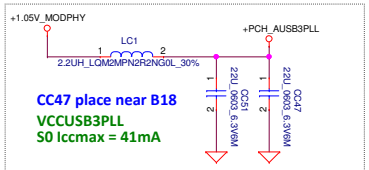
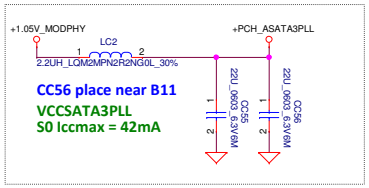
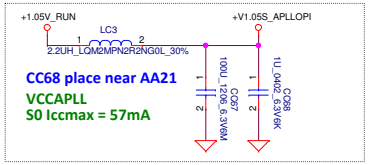
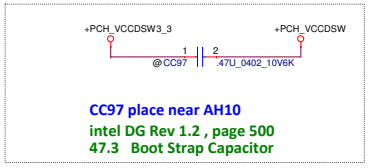
Date: Wednesday, July 16, 2014 Sheet 15 of 55

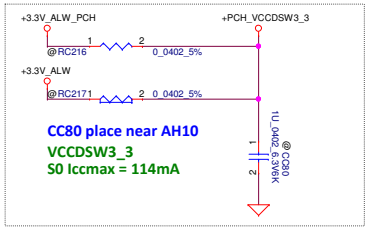


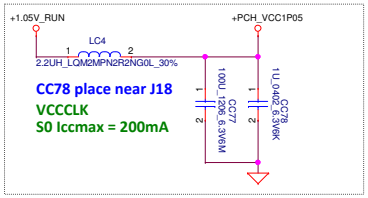


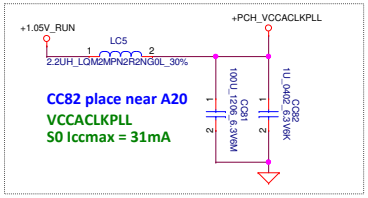


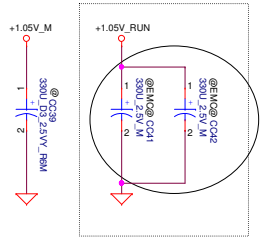


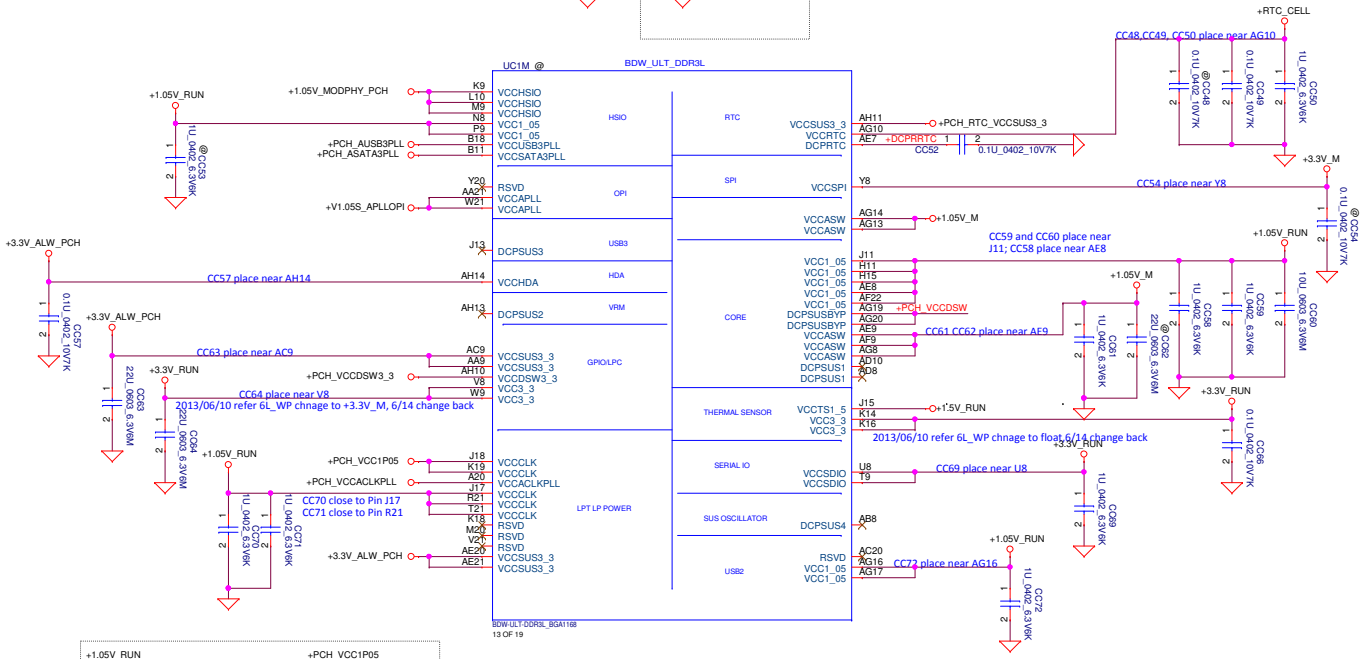


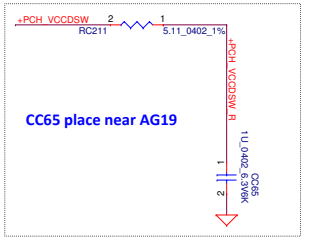


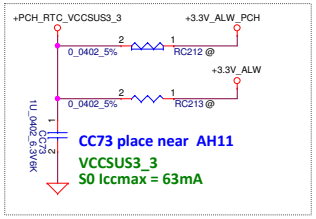












Voltage Rail	Voltage (V)	S0 Iccmax Current (A)[3]	Sx Iccmax Current (A)[3]	Deep Sx Iccmax (A)[3]	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1[4]	1.05	0.109	0.014	0	0
DcpSus2[4]	1.05	0.025	0.001	0	0
DcpSus3[4]	1.05	0.010	0.003	0	0
DcpSus4[4]	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 µA See notes 1, 2

Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

Power Rail Isolation

Voltage Supply	Interface: (power rail isolation required)	PCH Pins sharing power rail
V1.05S	Core	J11, H11, H15, AE8, AF22
	OPI	AA21, W21
	HSIO	K9, L10, N8, P9, B18, B11, M9
	USB2	AG16, AG17
	CLKPLL	A20
	CLK(A)	R21, T21
	CLK(B)	J18, K19
	CLK(C)	J17
V3.3A	GPIO	AC9, AA9, AE20, AE21
	RTC	AH11
	HDA	AH14
V3.3S	GPIO	V8, W9
	SDIO	U8, T9
	Thermal Sensor	K14, K16

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Title: CPU (11/12)

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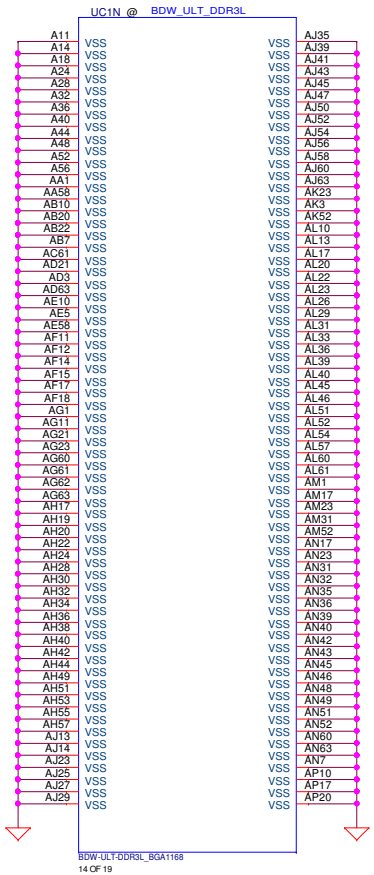

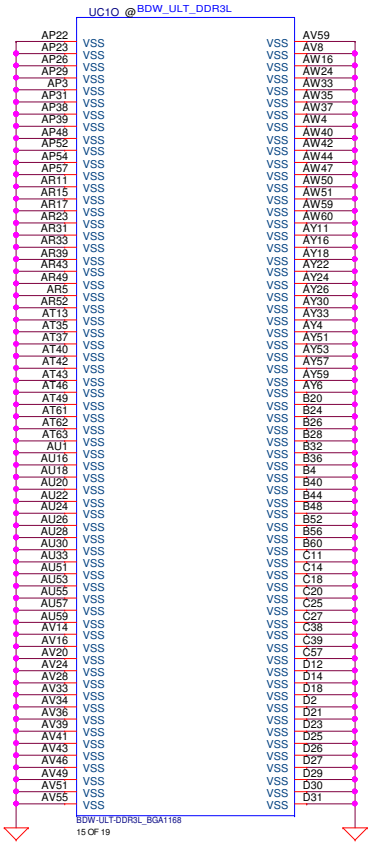

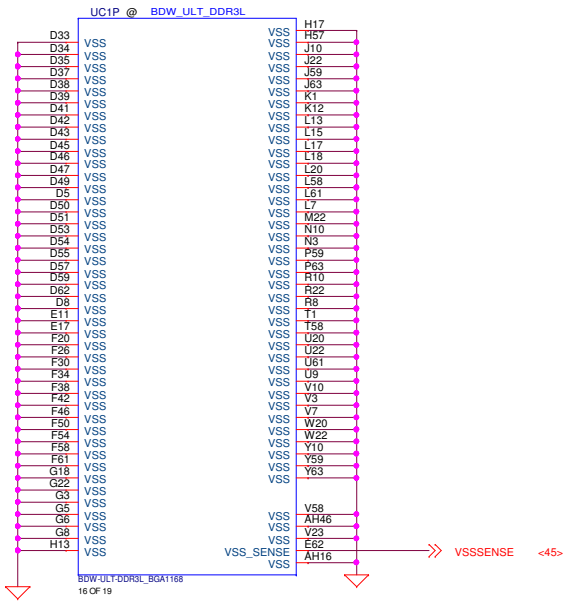

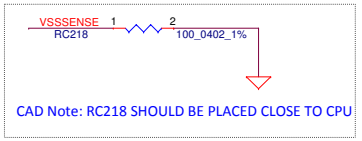

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Title: CPU (12/12)

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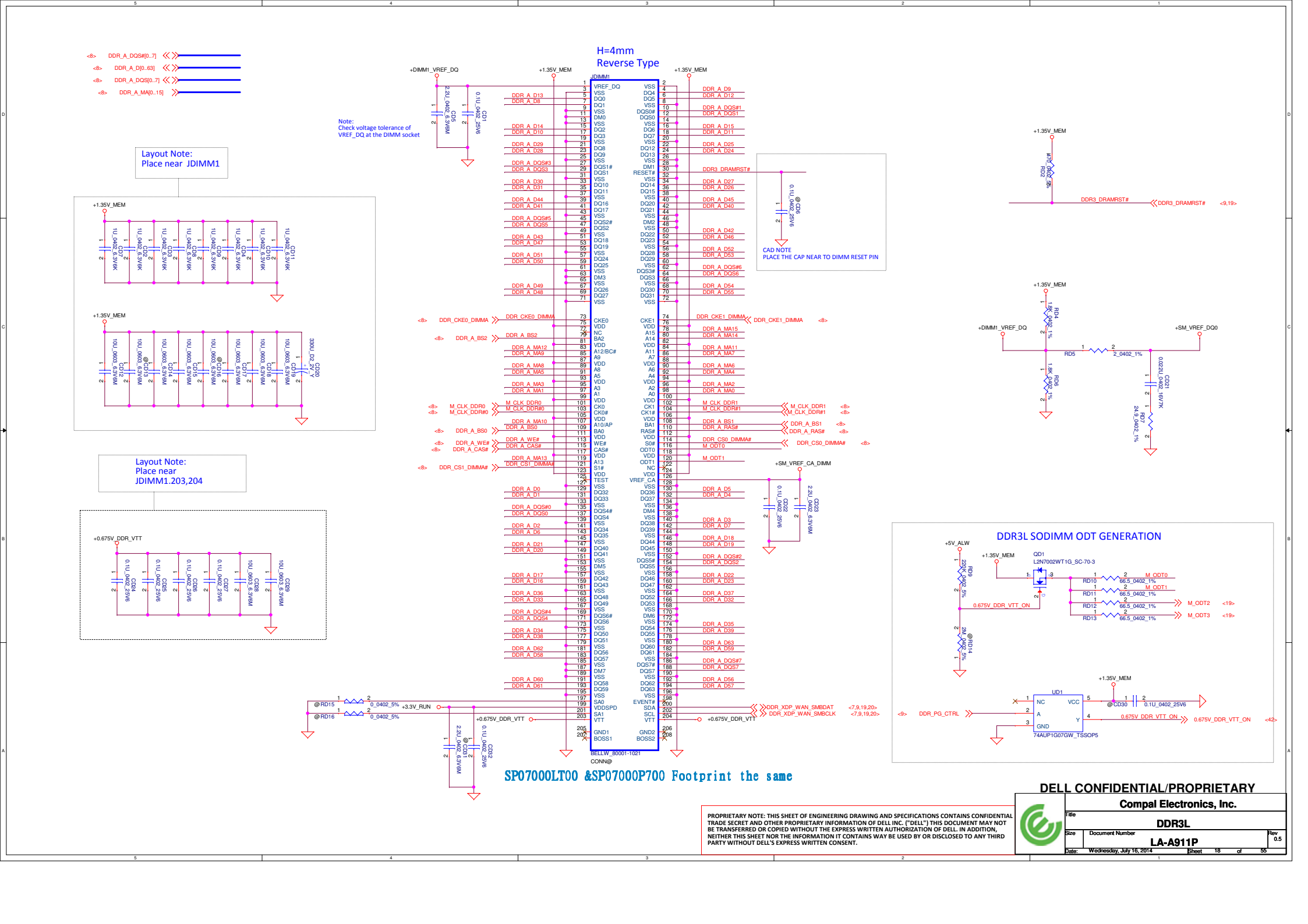

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Title: DDR3L			
Size	Document Number: LA-A911P		Rev: 0.5
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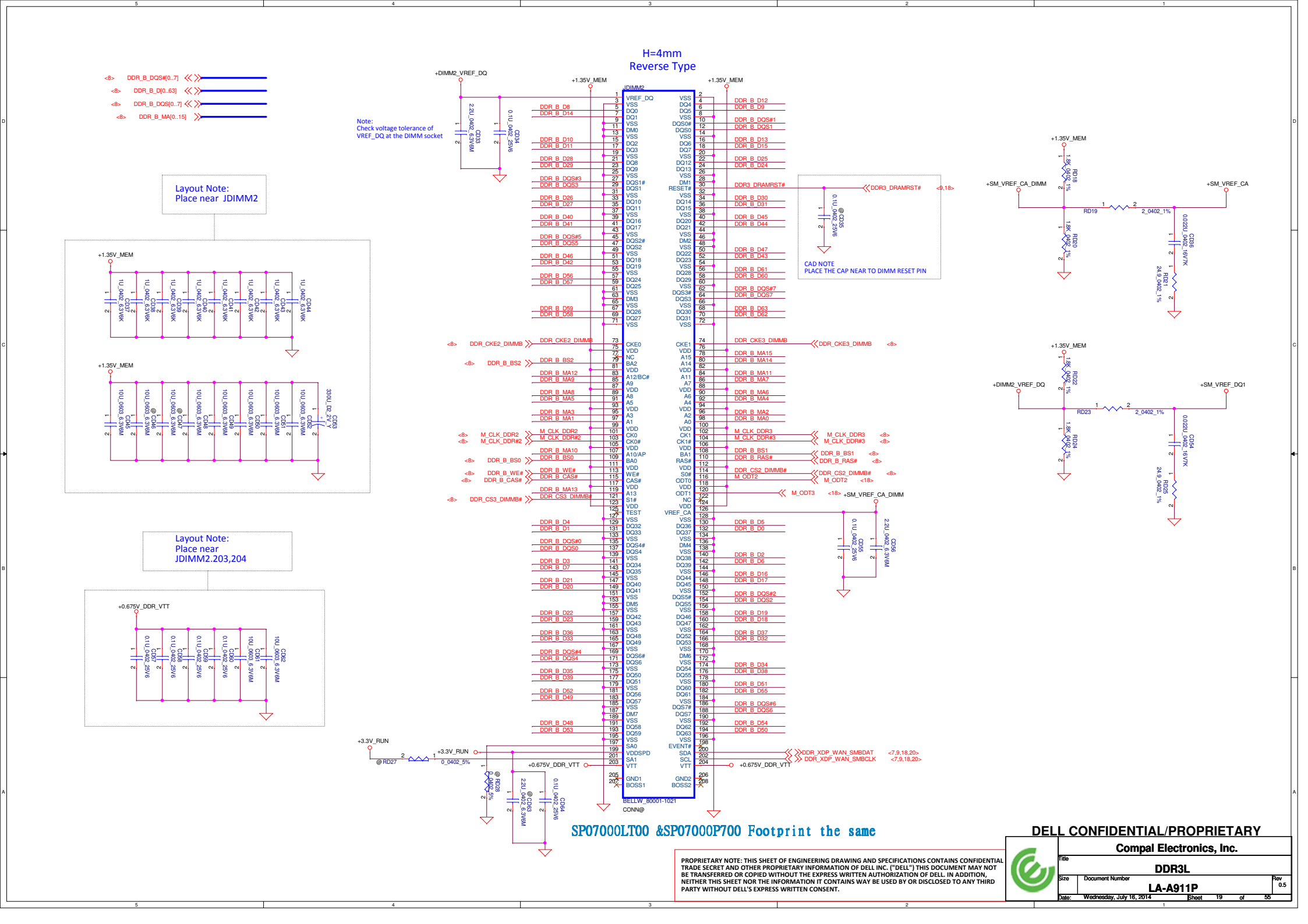

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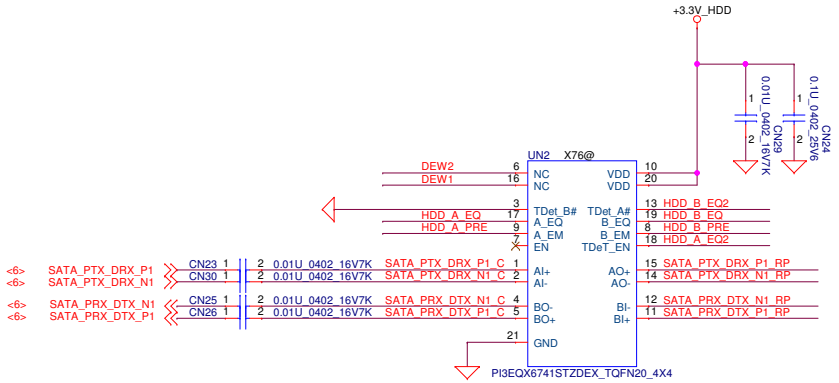
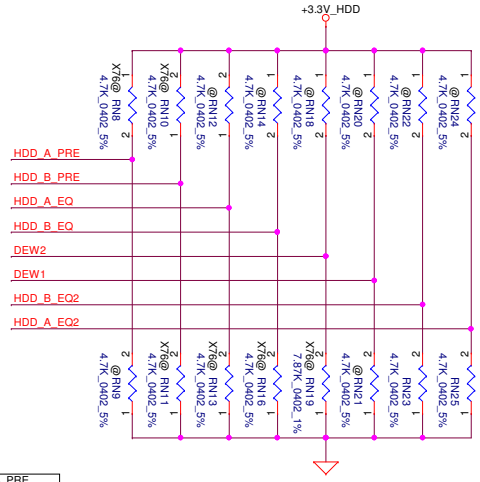
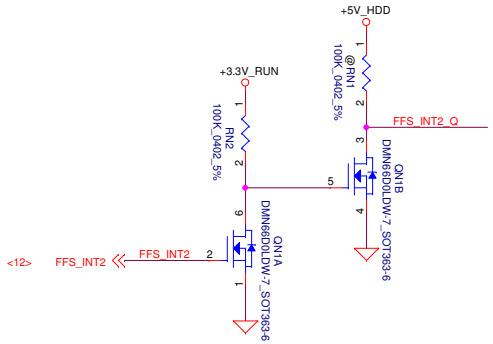
SATA Repeater





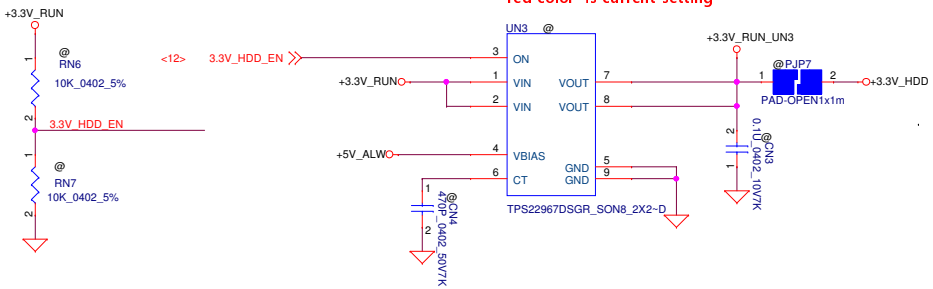


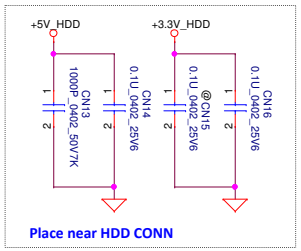
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	NC	PD (RN16)	PD (RN25)	PD (RN23)	NC	NC	NC (IPU)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN25)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN25)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

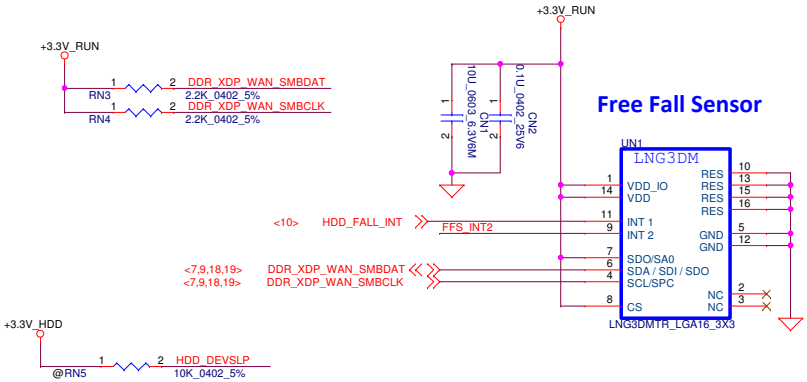
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB			
		1	9dB	9dB	1	1.5dB	1.5dB
						IPU	
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

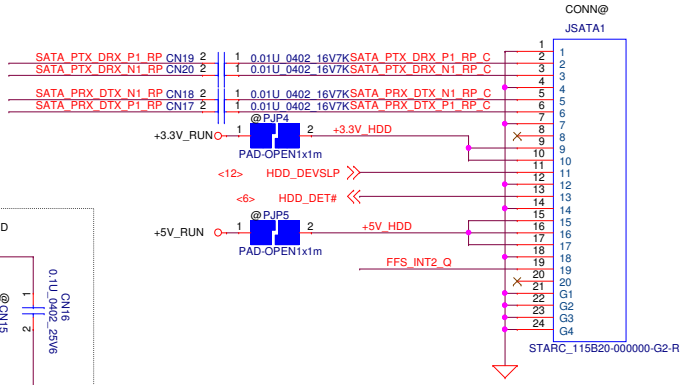
* red color is current setting

* red color is current setting









115B20-000000-G2-R Link done

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Title: HDD CONN

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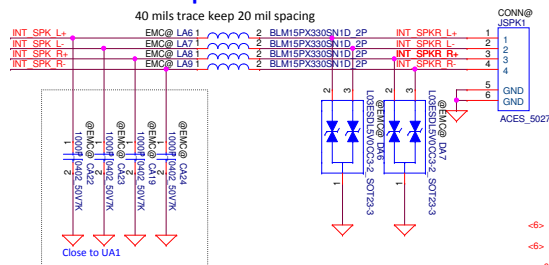
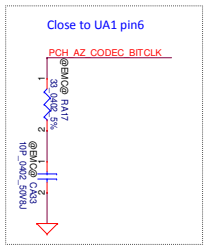
SP02000WI00 LINK DONE

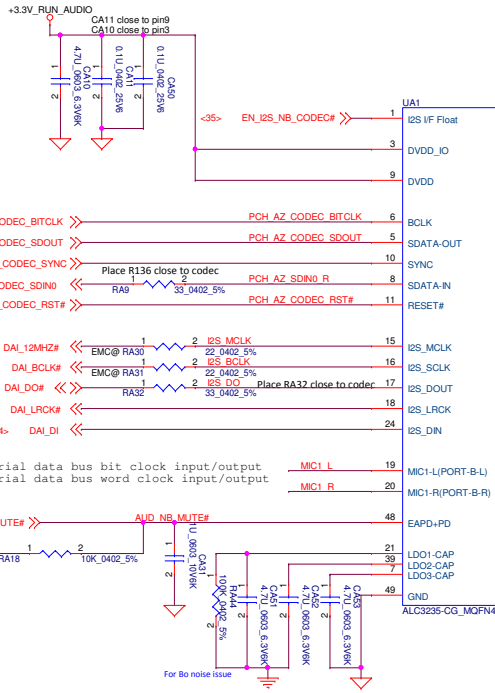
1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

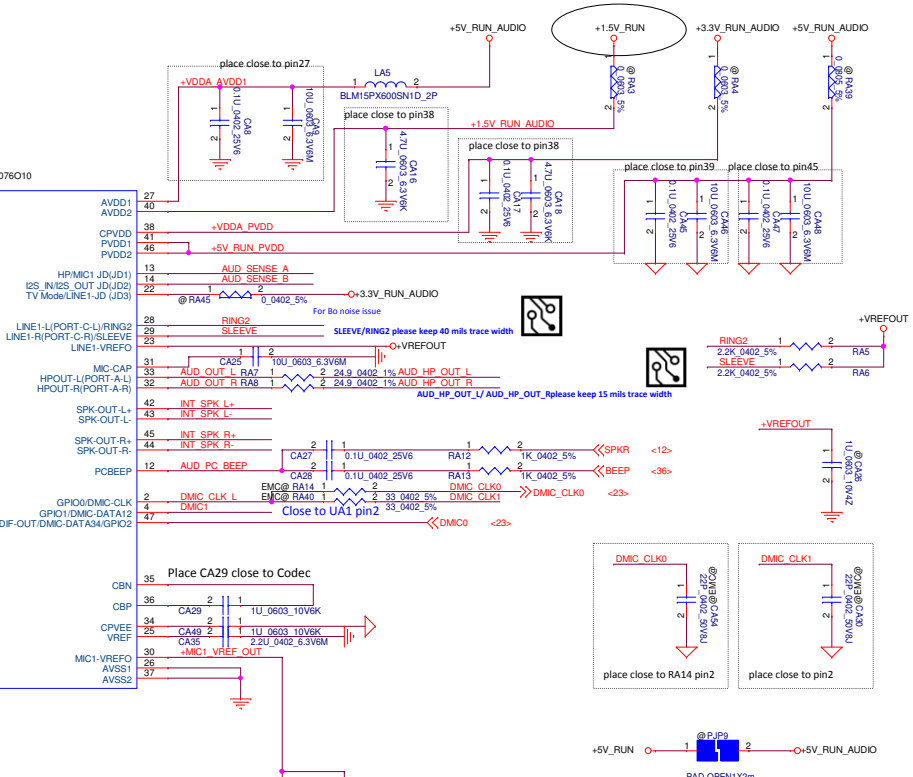
Internal Speakers Header

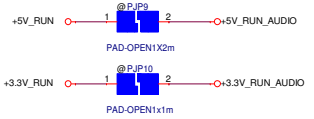
40 mils trace keep 20 mil spacing



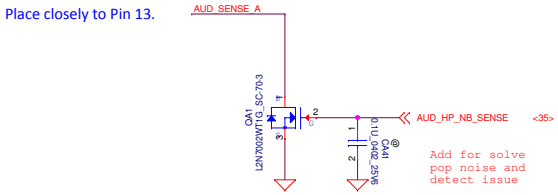


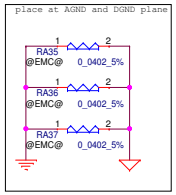


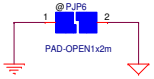


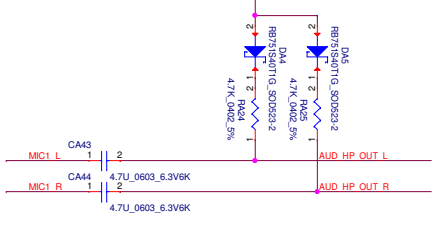


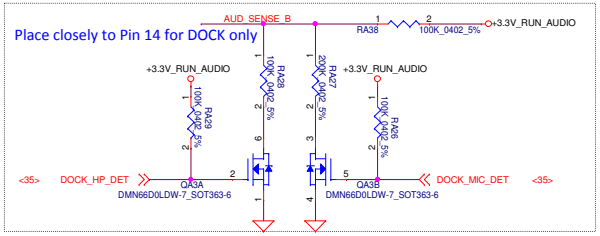
Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

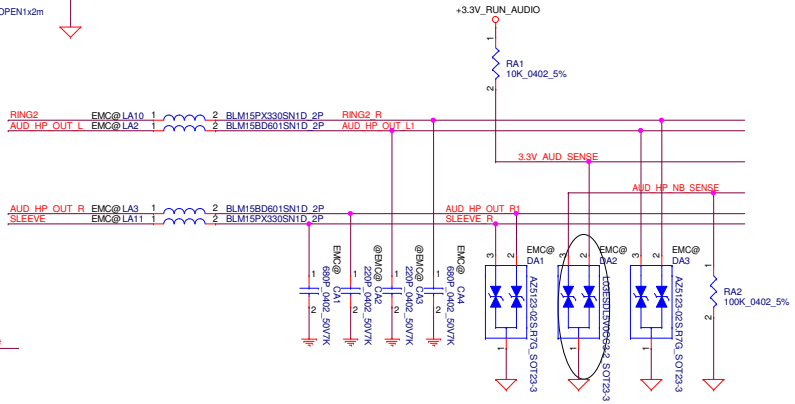


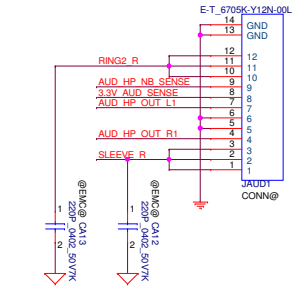


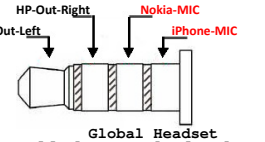






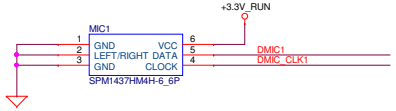


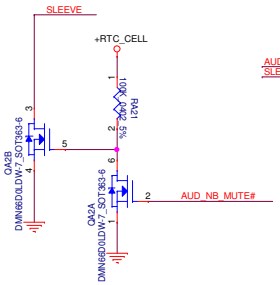




6705K-Y12N-00L LINK DONE

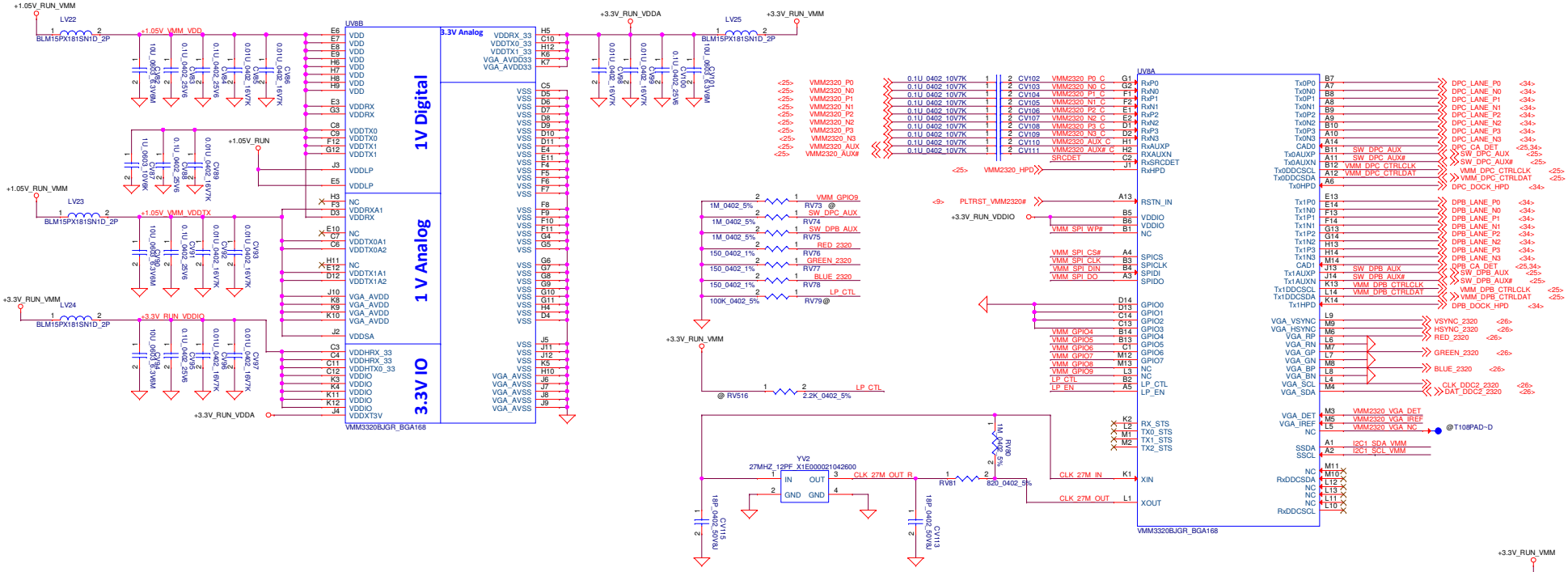
Digital Mic

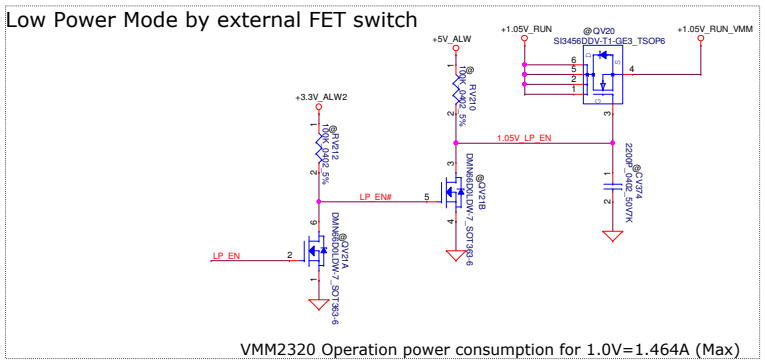


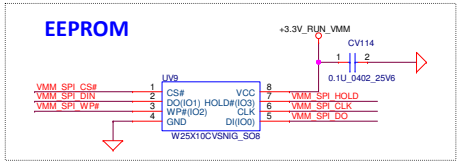


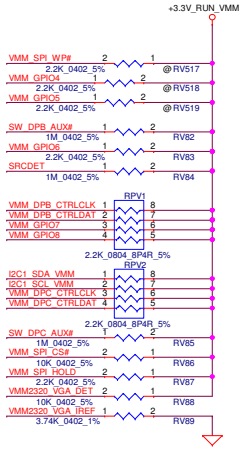
Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

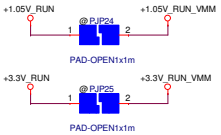
Compal Electronics, Inc.		
Title: Codec ALC3235		
Size	Document Number: LA-A911P	Rev: 0.5
Date: Wednesday, July 16, 2014	Sheet 21 of 55	











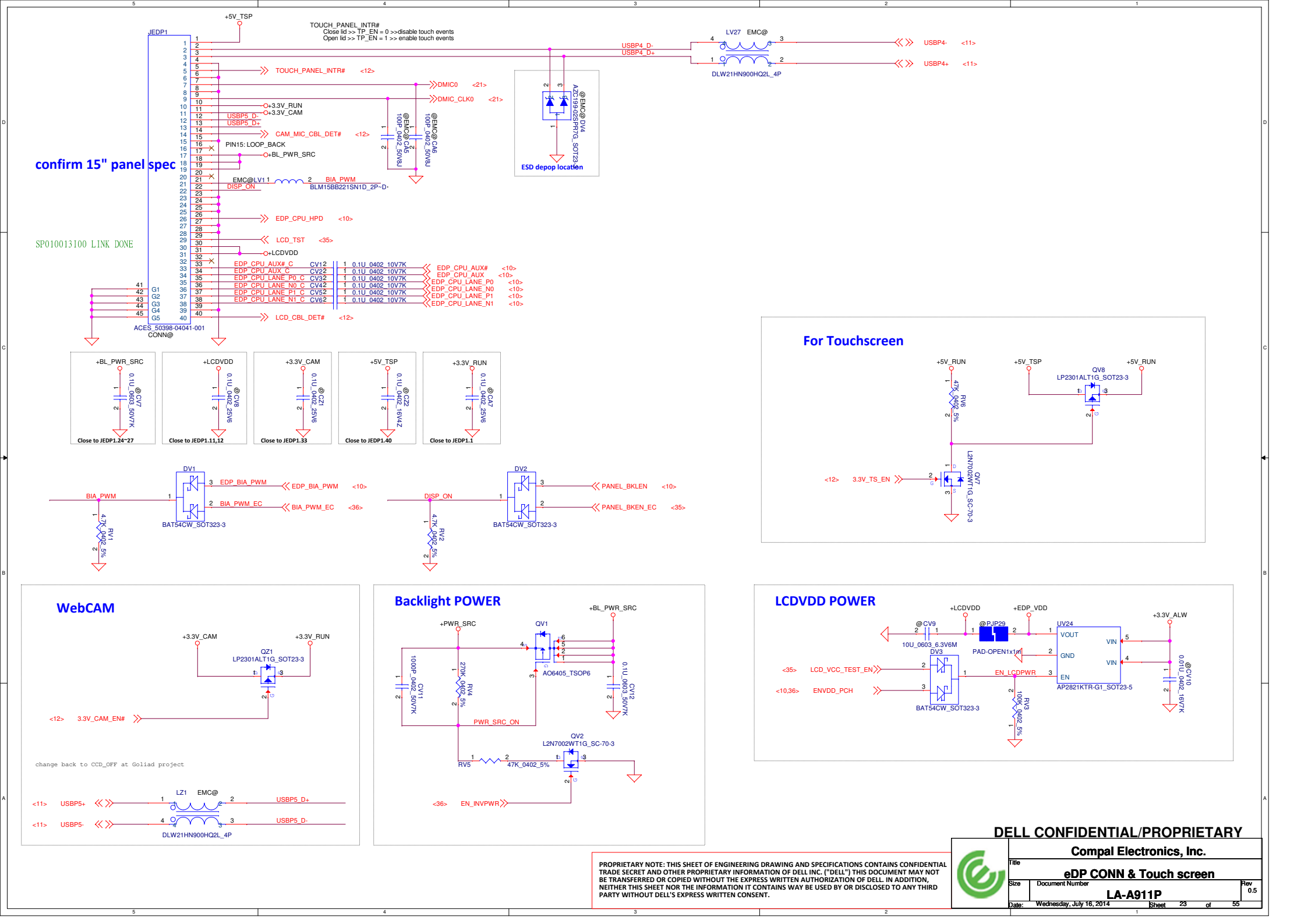
PRODUCT SUMMARY (SI3456DDV)			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[d]	Q_g (Typ.)
30	0.040 at V_{GS} = 10 V	6.3	2.8 nC
	0.050 at V_{GS} = 4.5 V	5.7	

Compal Electronics, Inc.

Title: DP 1.2 MST HUB

Size: | Document Number: LA-A911P | Rev: 0.5

Date: Wednesday, July 16, 2014 | Sheet 22 of 55

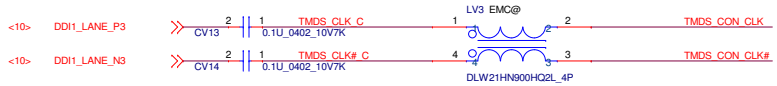


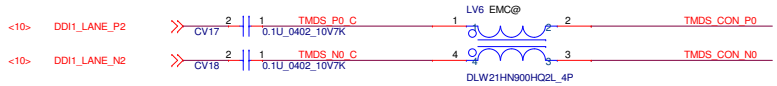
Compal Electronics, Inc.

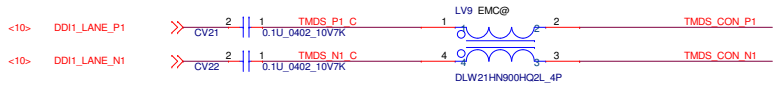
Title: eDP CONN & Touch screen

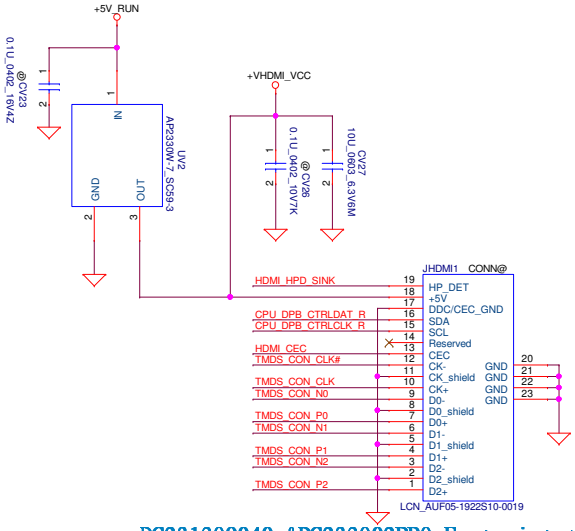
Size | Document Number: LA-A911P | Rev: 0.5

Date: Wednesday, July 16, 2014 | Sheet 23 of 55

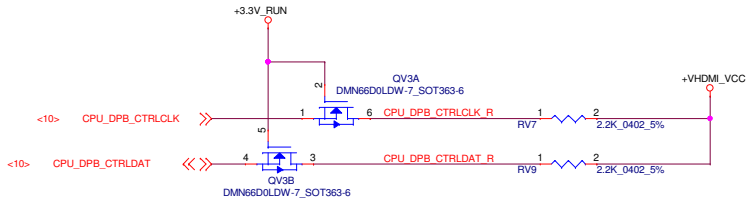


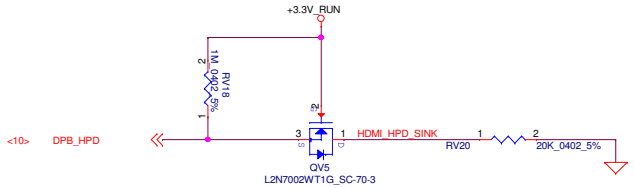


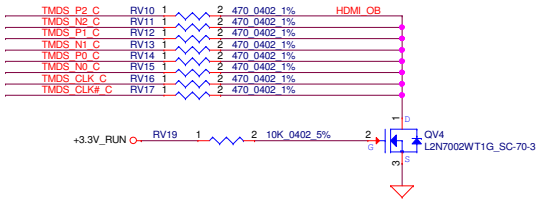




DC231209040 &DC232002PB0 Footprint the same







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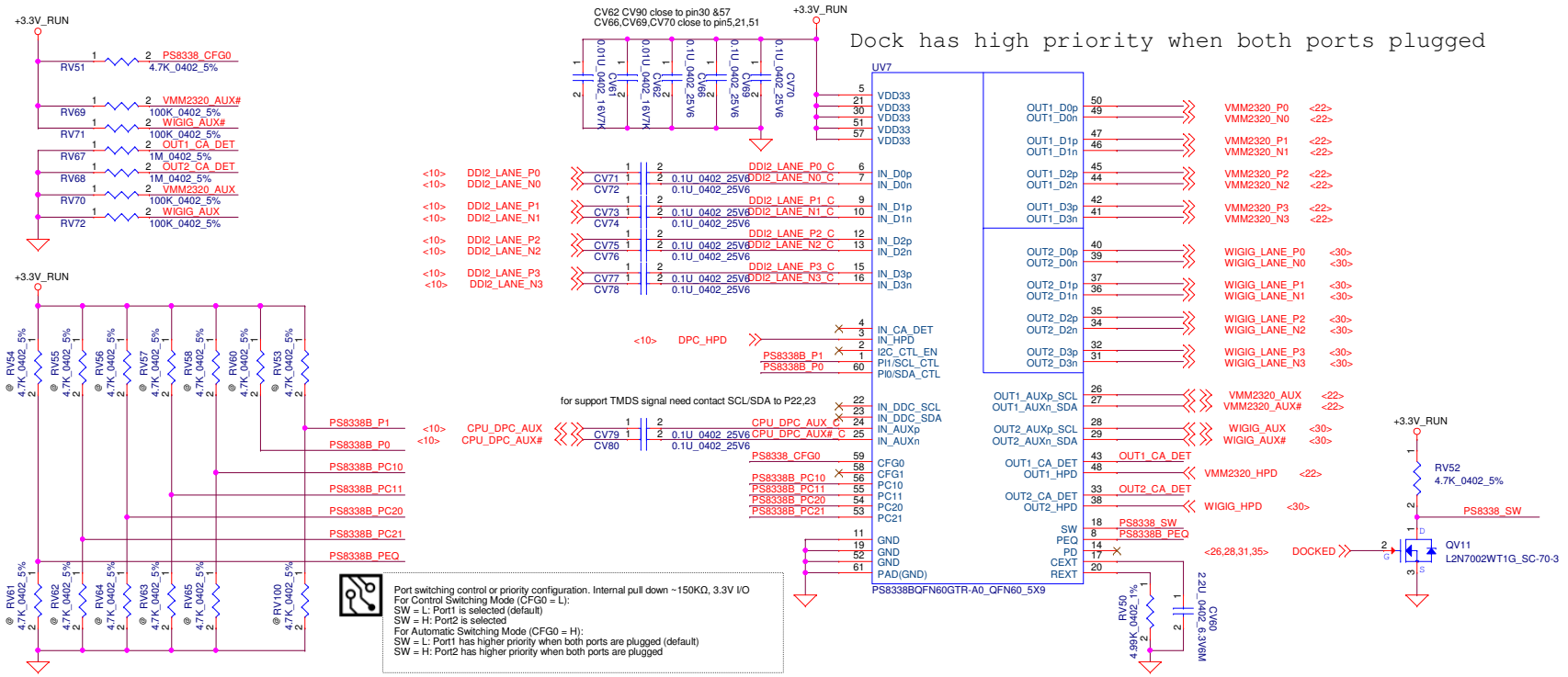
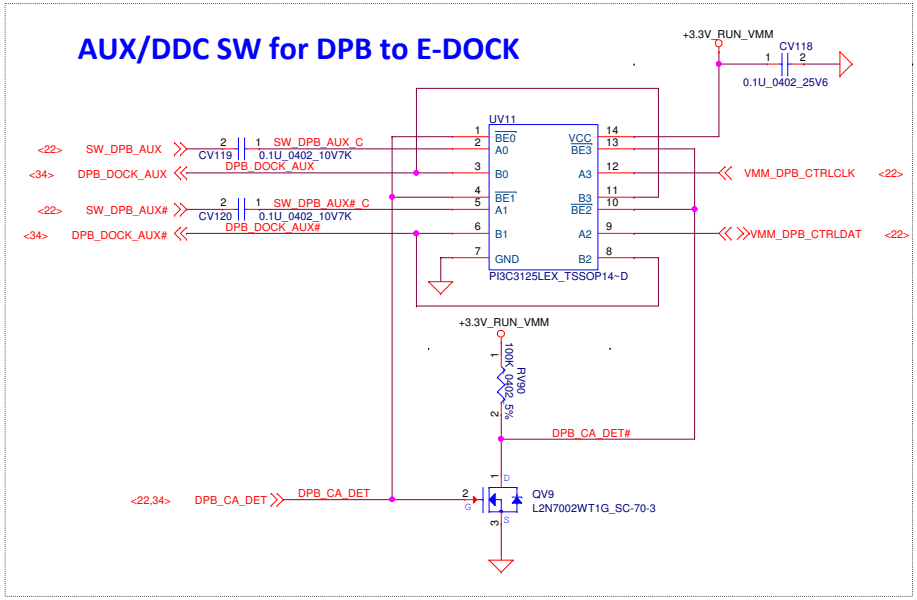
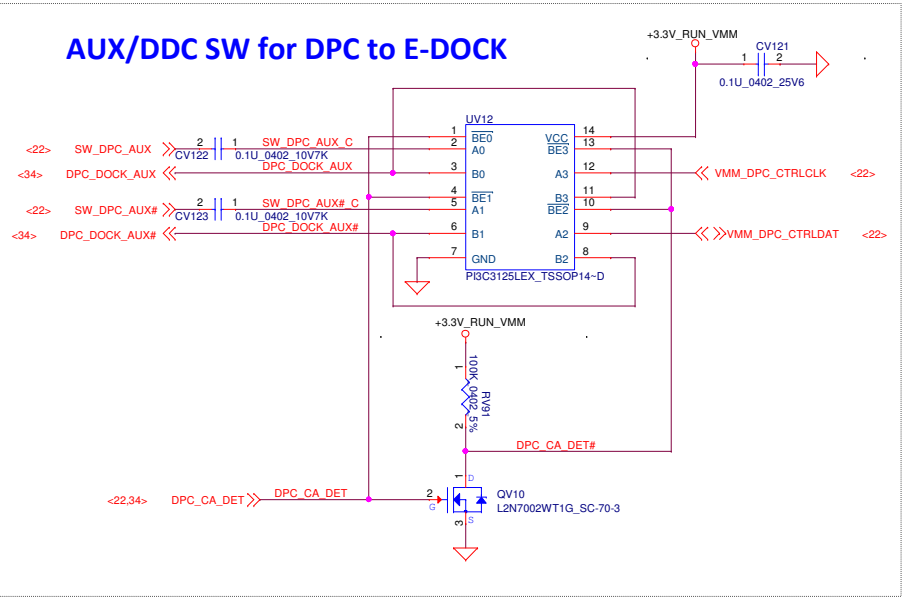
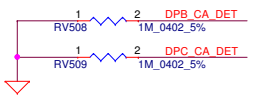
Compal Electronics, Inc.		
Title: HDMI CONN		
Size	Document Number: LA-A911P	Rev: 0.5
Date: Wednesday, July 16, 2014	Sheet 24 of 55	

PCB	DP SWITCH
H12 UMA	PS8339+PS8338
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	PS8338
H14U_En	PS8338
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	PS8338
H15U_En	PS8338









	DP	HDMI
DPB_CA_DET	0	1
DPC_CA_DET	0	1

Compal Electronics, Inc.

Title: DP SW

Size | Document Number: LA-A911P | Rev: 0.5

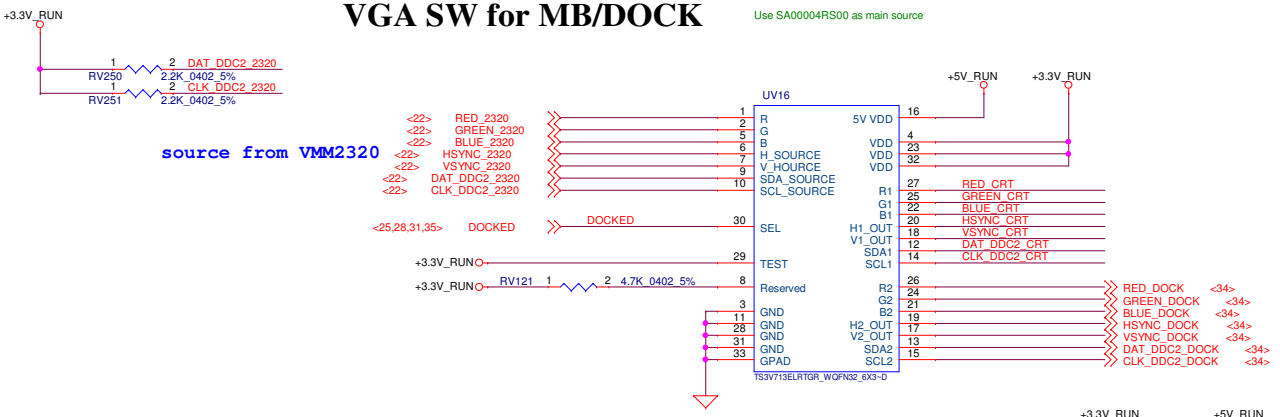
Date: Wednesday, July 16, 2014 | Sheet 25 of 55

VGA SW for MB/DOCK

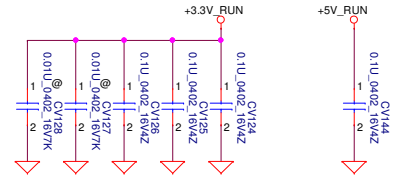
Use SA00004RS00 as main source

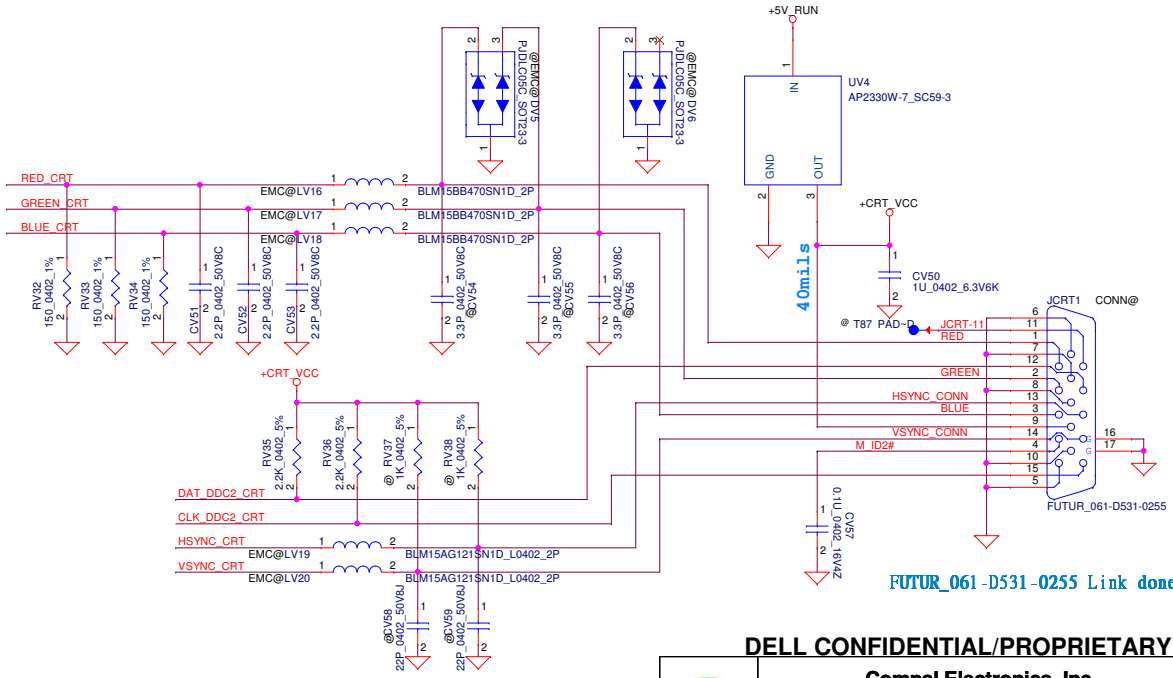
VGA SW

PCB	VGA SWITCH
H12 UMA	NA
H12 Entry	NA
H14 DSC	PI3V713
H14 UMA	PI3V713
H14D_En	NA
H14U_En	NA
H15 DSC	PI3V713
H15 UMA	PI3V713
H15D_En	NA
H15U_En	NA



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR





FUTUR_061-D531-0255 Link done

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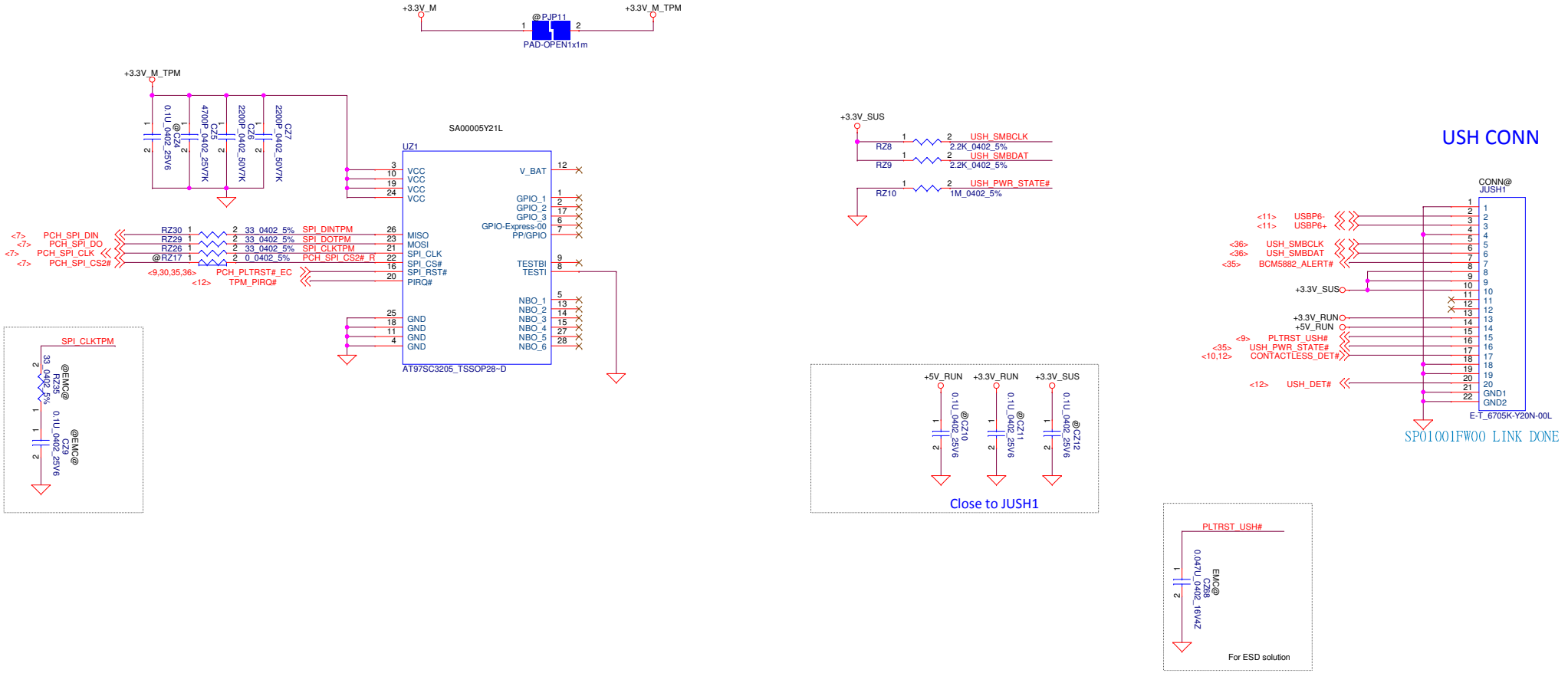
Compal Electronics, Inc.

Title: VGA SW & VGA Conn

Size | Document Number: LA-A911P | Rev: 0.5

Date: Wednesday, July 16, 2014 | Sheet 26 of 55

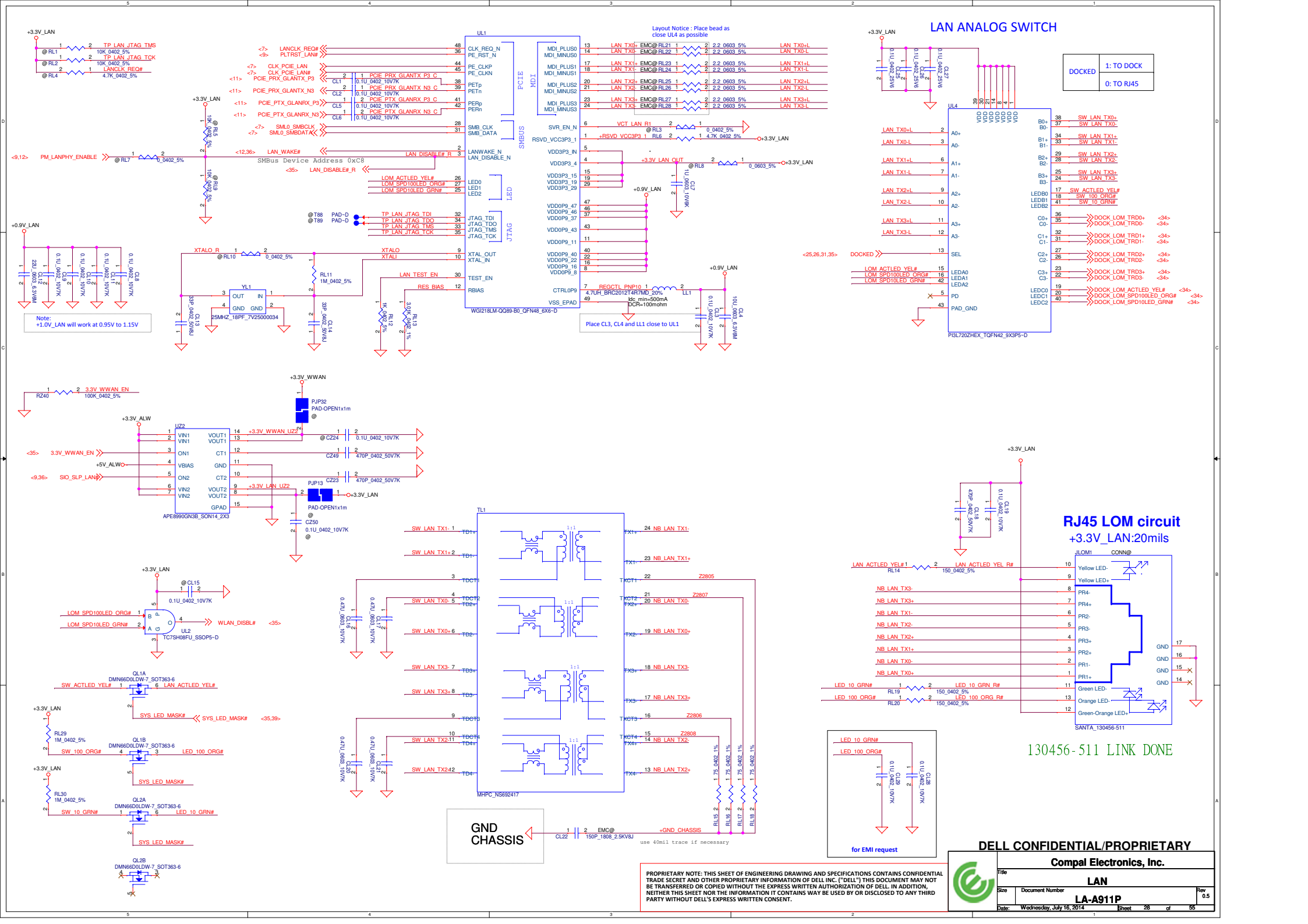


Compal Electronics, Inc.

Title: USH & TPM

Size | Document Number: LA-A911P | Rev: 0.5

Date: Wednesday, July 16, 2014 | Sheet 27 of 55



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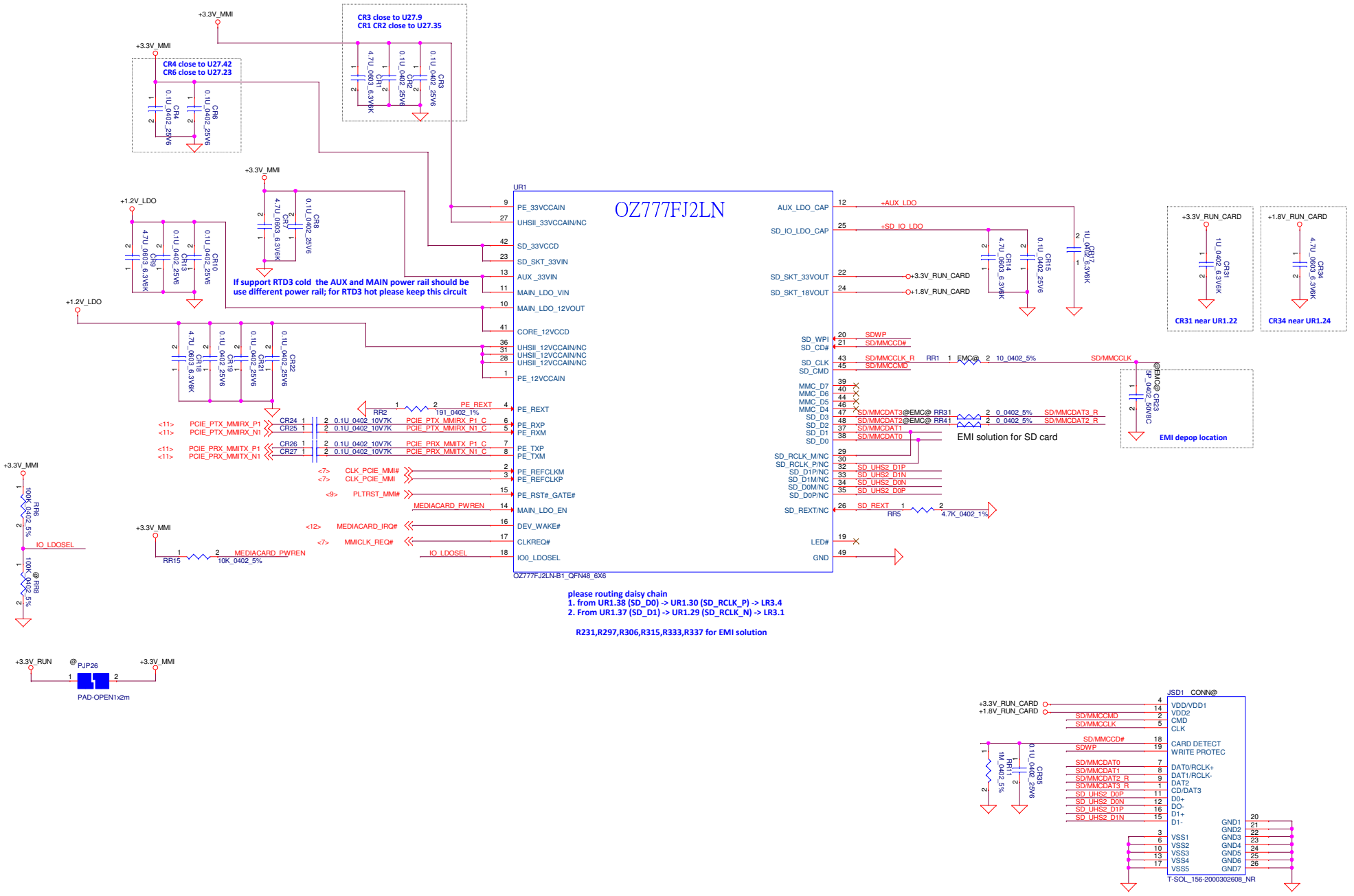

Compal Electronics, Inc.

Title: Card Reader

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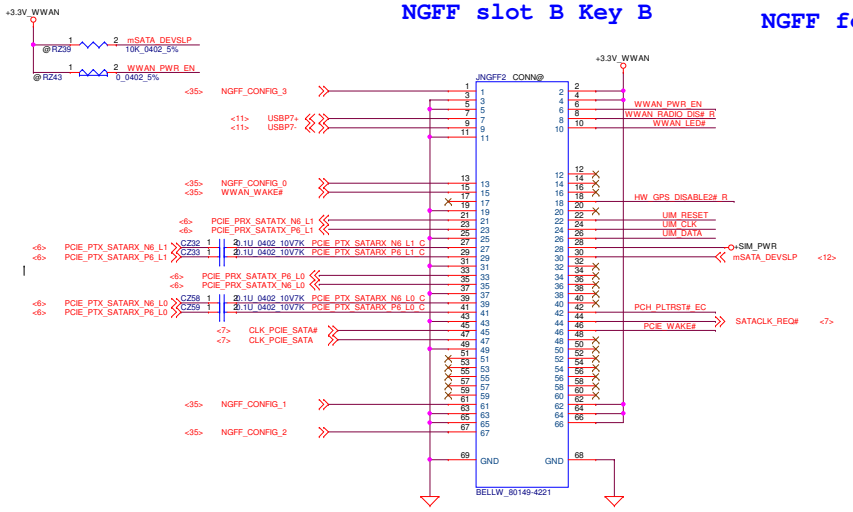
Date: Thursday, July 17, 2014 | Sheet 29 of 55

NGFF slot B Key B

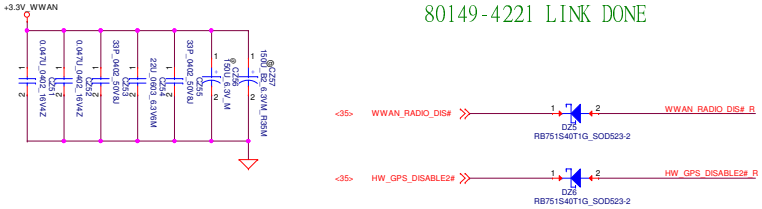
NGFF for UMA

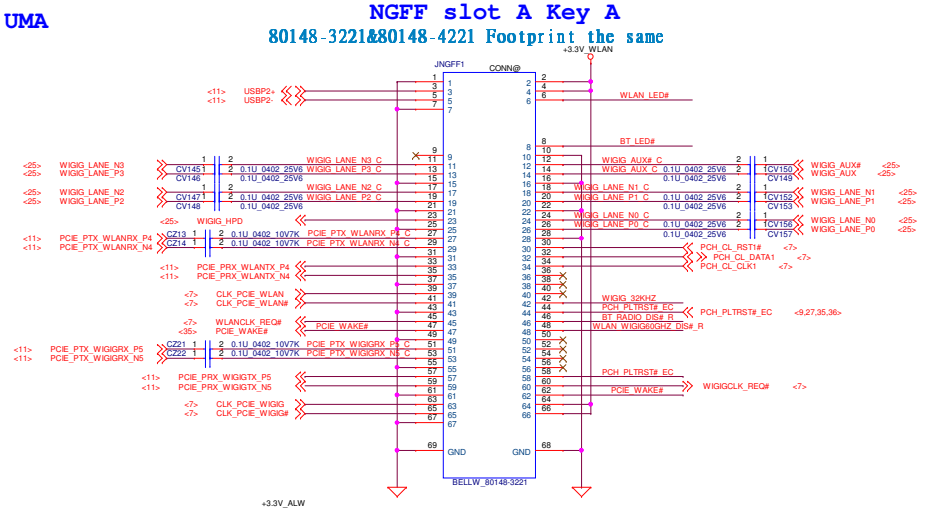
NGFF slot A Key A

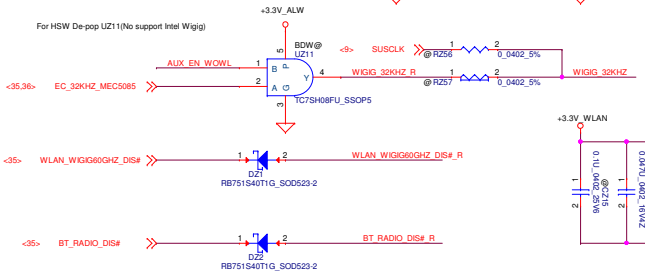
80148-3221&80148-4221 Footprint the same

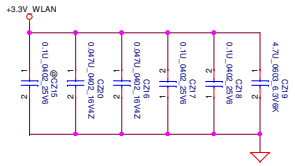


80149-4221 LINK DONE







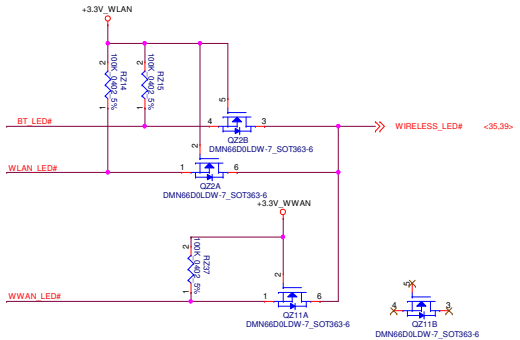


STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
~~0~~	~~GND~~	~~GND~~	~~GND~~	~~GND~~	~~SSD-SATA~~
~~1~~	~~GND~~	~~HIGH~~	~~GND~~	~~GND~~	~~SSD-PCIE(2 lane)~~
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

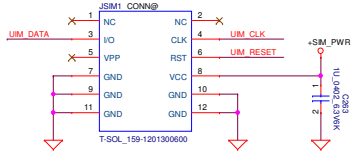
Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

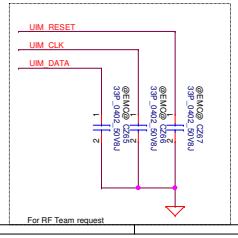
LED control circuit

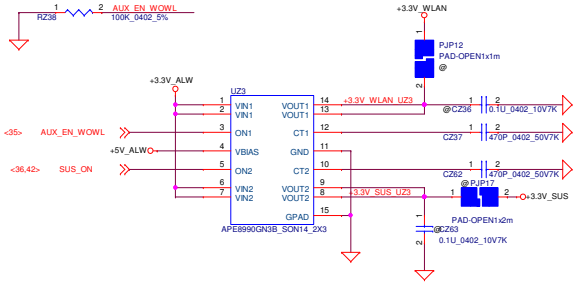


SIM Card Push-Push



T-SOL_159-1201300600 LINK DONE





Compal Electronics, Inc.

Title	NGFF Card	
Size	Document Number: LA-A911P	Rev: 0.5
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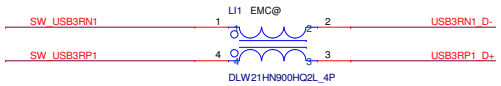
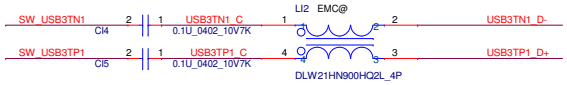
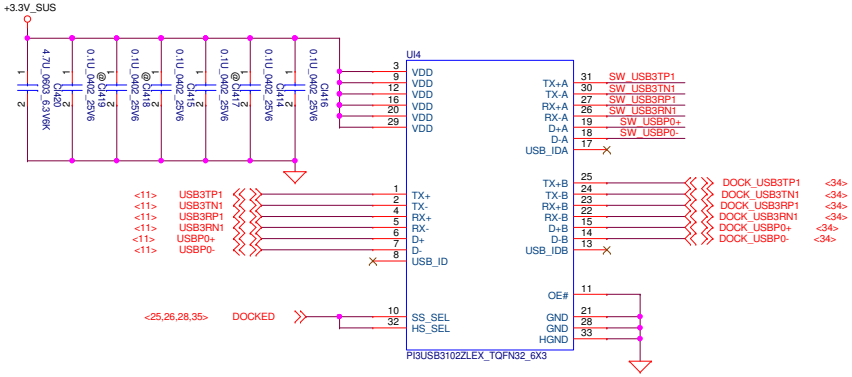
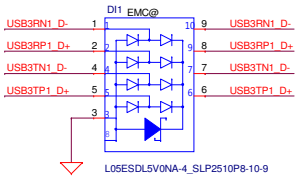


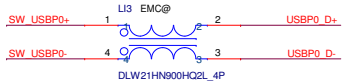




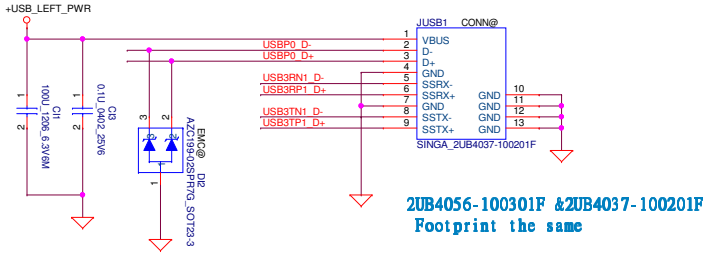
check port mapping

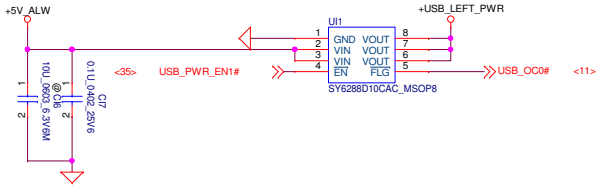
DOCKED	function
1	Dock
0	M/B

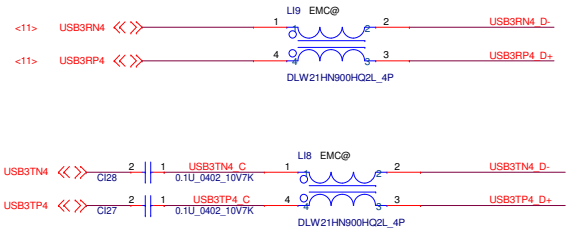


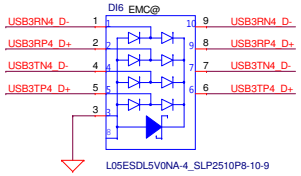


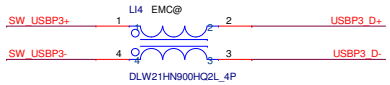
PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA

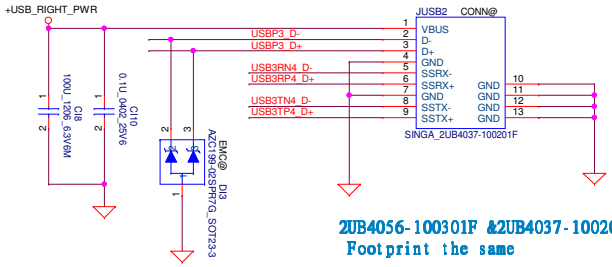


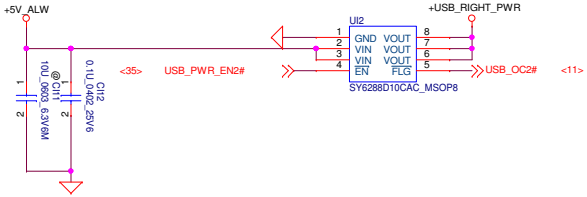


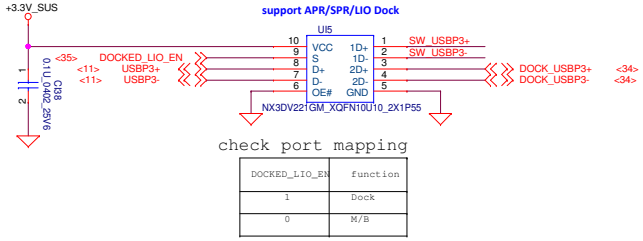












check port mapping

DOCKED_LIO_EN	function
1	Dock
0	M/B

Compal Electronics, Inc.

Title: USB3.0

Size: | Document Number: LA-A911P | Rev: 0.5

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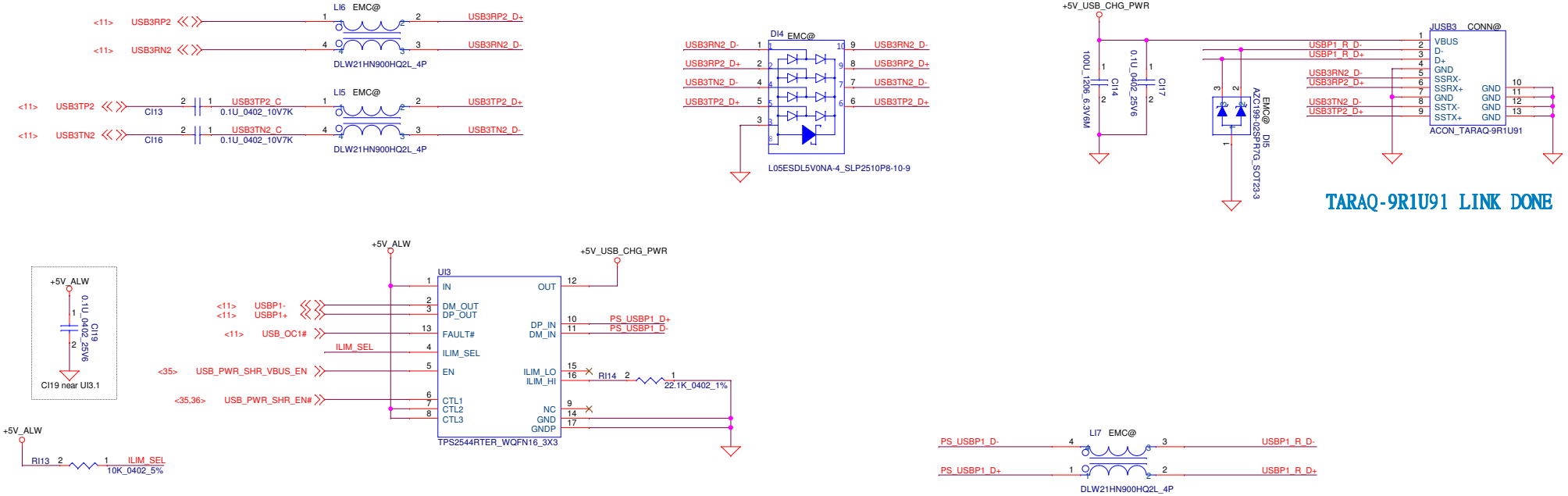

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Title: USB SW

Size | Document Number: LA-A911P | Rev: 0.5

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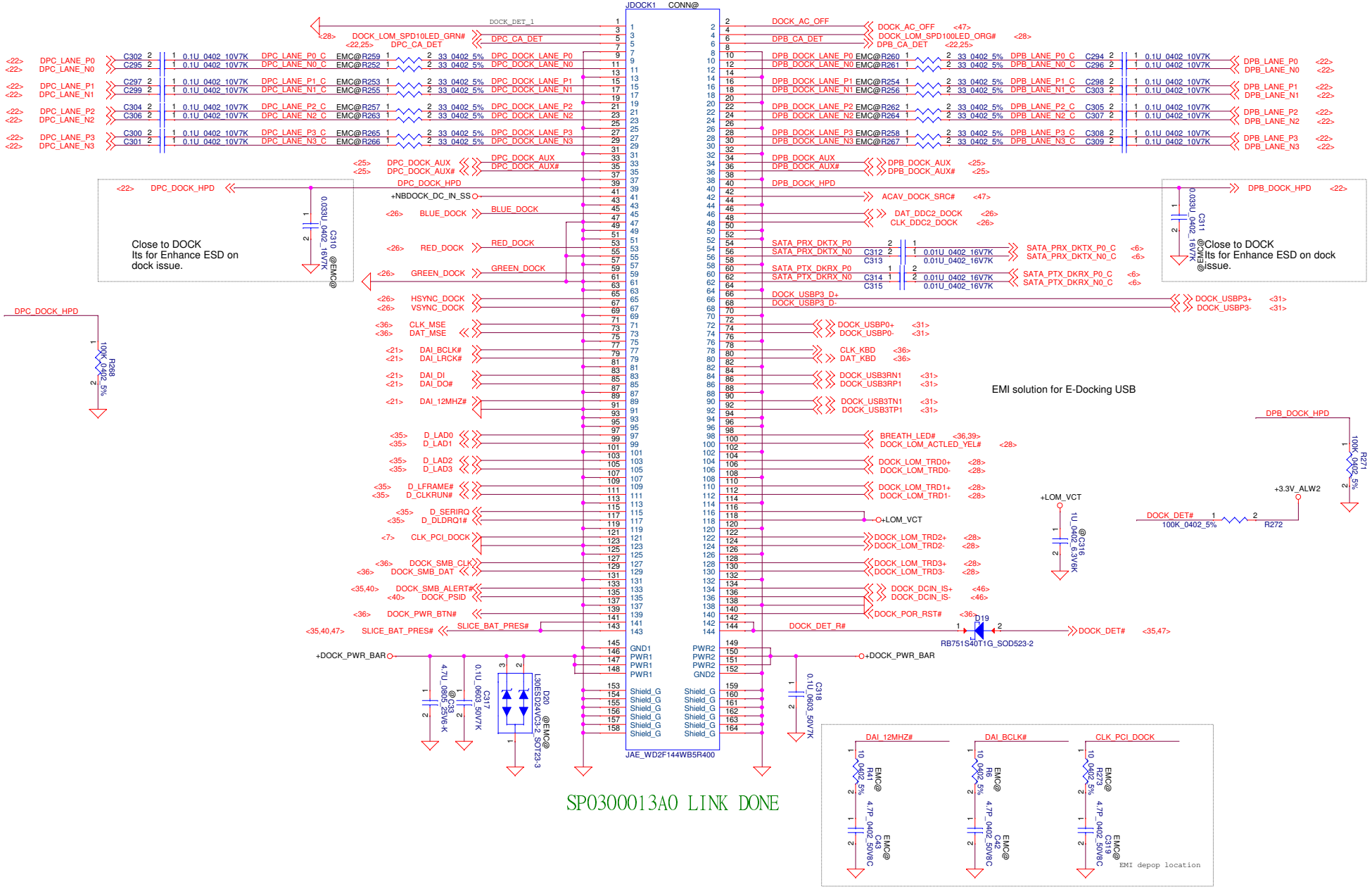
NFC ON USH/B

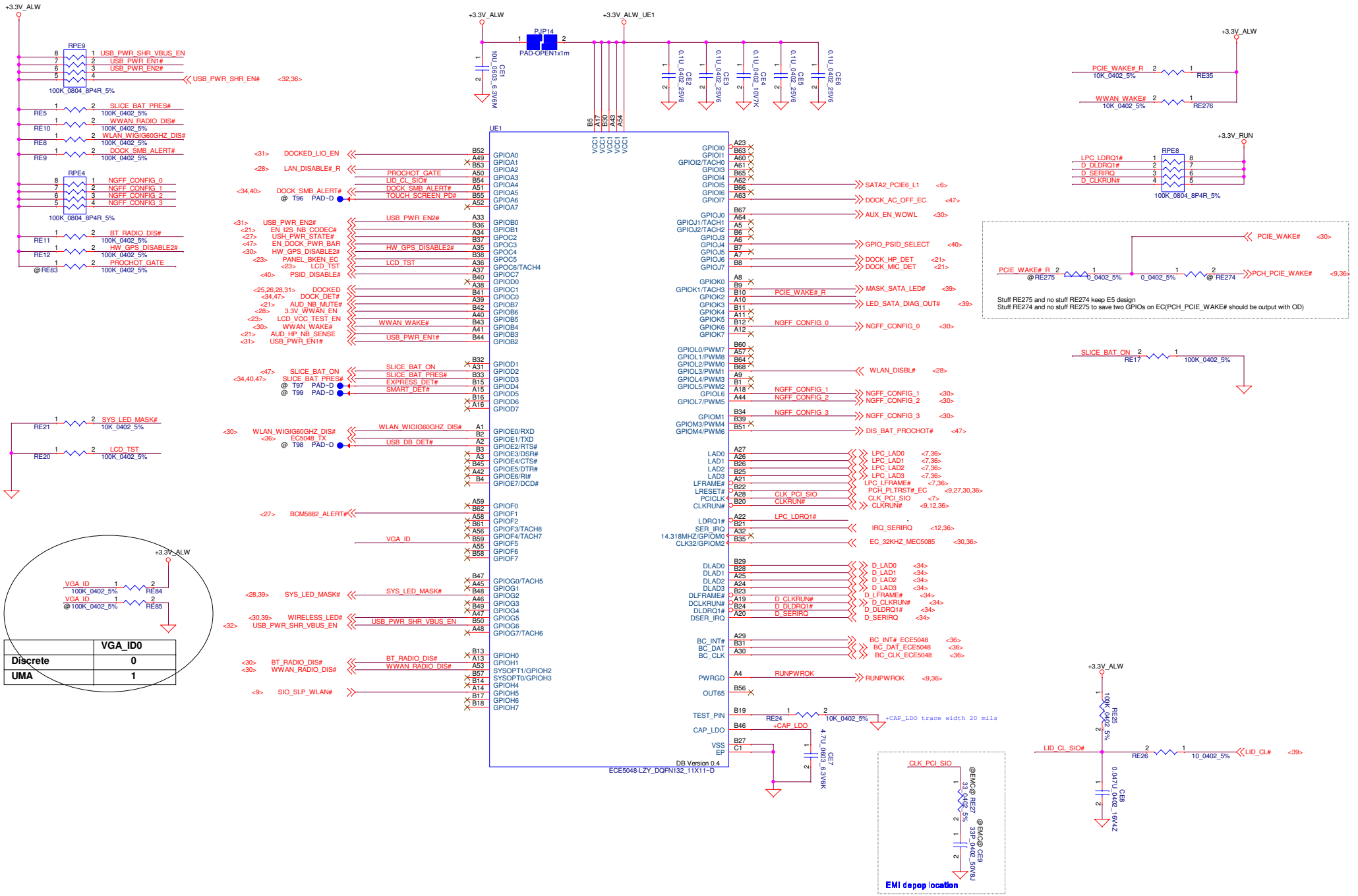


Compal Electronics, Inc.

Title: E-Dock

Size | Document Number: LA-A911P | Rev: 0.5

Date: Wednesday, July 16, 2014 | Sheet 34 of 55



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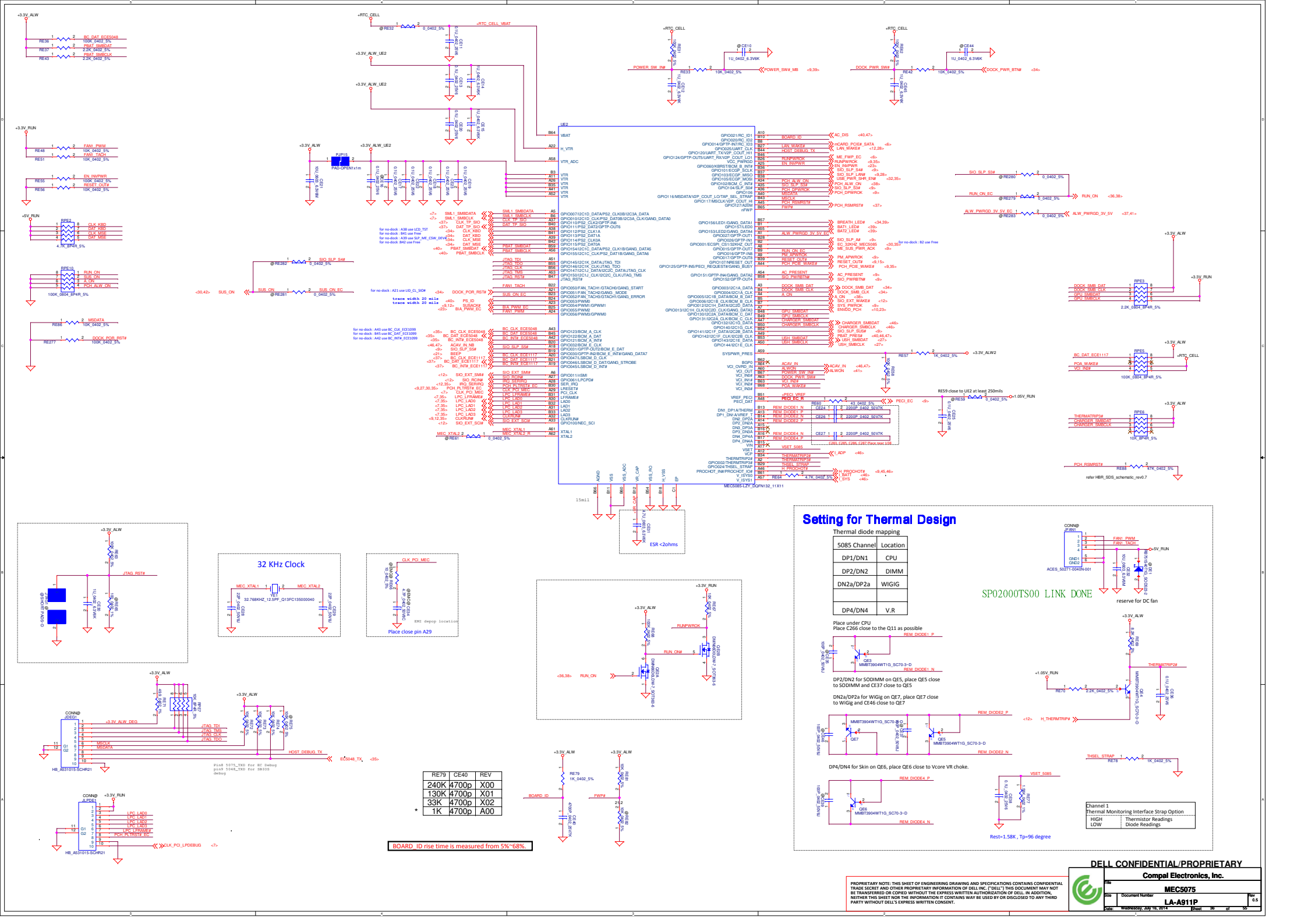
Title	ECE5048
Size	Document Number: LA-A911P
Rev	0.5
Date: Wednesday, July 16, 2014	Sheet 35 of 55


Setting for Thermal Design
Thermal diode mapping
5085 Channel | Location
DP1/DN1 | CPU
DP2/DN2 | DIMM
DN2a/DP2a | WIGIG
DP4/DN4 | V.R
Place under CPU
Place C266 close to the Q11 as possible
DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5
DN2a/DP2a for WiGig on QE7, place QE7 close to WiGig and CE46 close to QE7
DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.
Rest=1.58K , Tp=96 degree
Channel 1
Thermal Monitoring Interface Strap Option
HIGH | Thermistor Readings
LOW | Diode Readings
32 KHz Clock
32.768KHZ_12.5PF_Q13FC1350000040
Place close pin A29
ESR <2ohms
SP02000TS00 LINK DONE
reserve for DC fan
BOARD_ID rise time is measured from 5%~68%.
RE79 | CE40 | REV
240K | 4700p | X00
130K | 4700p | X01
33K | 4700p | X02
1K | 4700p | A00
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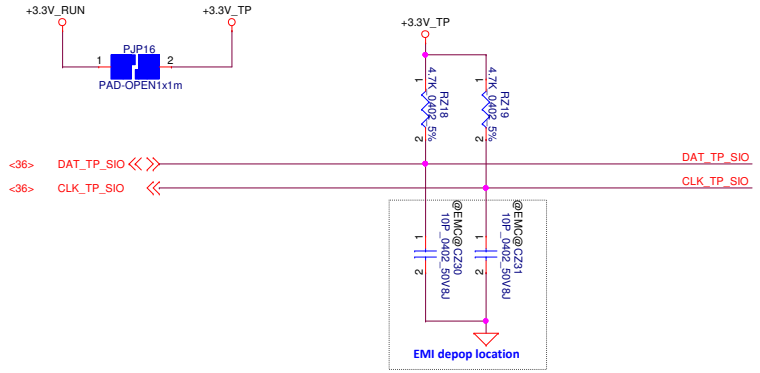
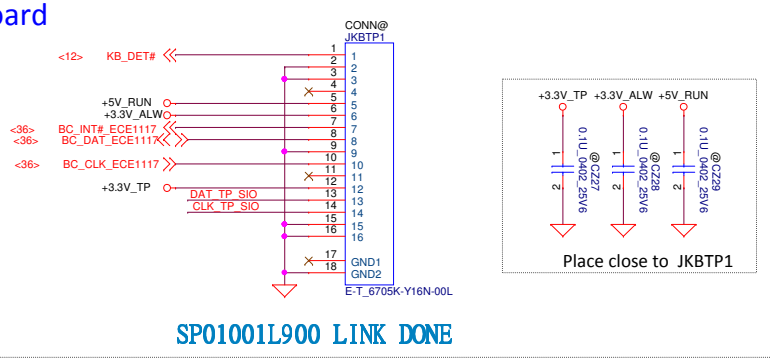
MEC5075
LA-A911P
Wednesday, July 16, 2014

Touch Pad

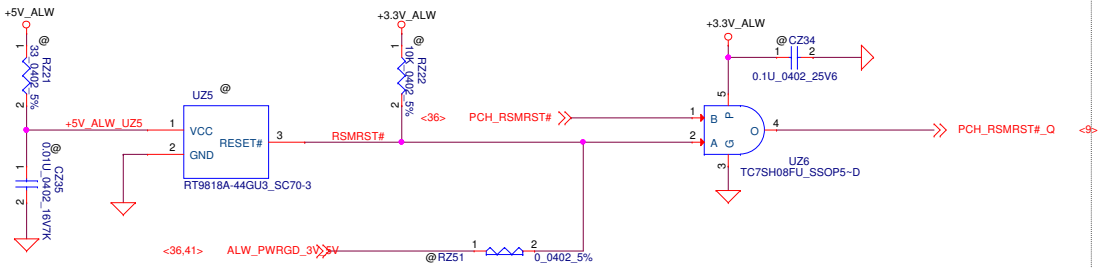


Keyboard



SP01001L900 LINK DONE

RSMRST circuit



@eDP Cable

Part Number	Description
DC02C007A00	H-CONN SET 13M MB-EDP

@eDP Cable w camera

Part Number	Description
DC02C007900	H-CONN SET 13M MB-EDP-CAMERA

@eDP TS Cable w camera

Part Number	Description
DC02C007B00	H-CONN SET 13M MB-EDP-CAMERA-TS

@SATA Cable-Spindle HDD

Part Number	Description
DC02C007800	H-CONN SET 13M MB-SPINDLE HDD

@SATA Cable-mSATA

Part Number	Description
DC02C007700	H-CONN SET 13M MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@RTC BATT

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@KBTP FFC

Part Number	Description
NBX0001JH00	FFC 16P G P0.5 PAD=0.3 66.5MM MB-TP 13M

@Audio Board FFC

Part Number	Description
NBX0001JP00	FFC 12P F P.5 PAD=.35 26.85MM MB-AUDIO/B

@USH Board FFC

Part Number	Description
NBX0001JF00	FFC 26P G P0.5 PAD=0.3 58MM MB-USH/B 13M

@LED Board FFC

Part Number	Description
NBX0001JM00	FFC 10P G P.5 PAD.3 192.5MM MB-LED/B 13M

@PWR Board FFC

Part Number	Description
NBX0001JL00	FFC 6P G P0.5 PAD=0.3 31MM MB-PWR/B 13M

@FP FFC-Validity

Part Number	Description
NBX0001JN00	FFC 8P F P0.5 PAD=0.3 170MM USH/B-FP VALIDITY

@FP FFC-TCS

Part Number	Description
NBX0001JO00	FFC 8P F P0.5 PAD=0.3 164.8MM USH/B-FP_TCS

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

Compal Electronics, Inc.

Title: Keyboard

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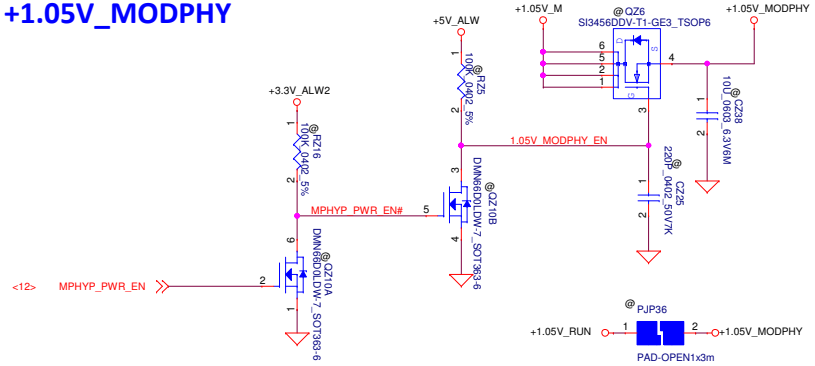
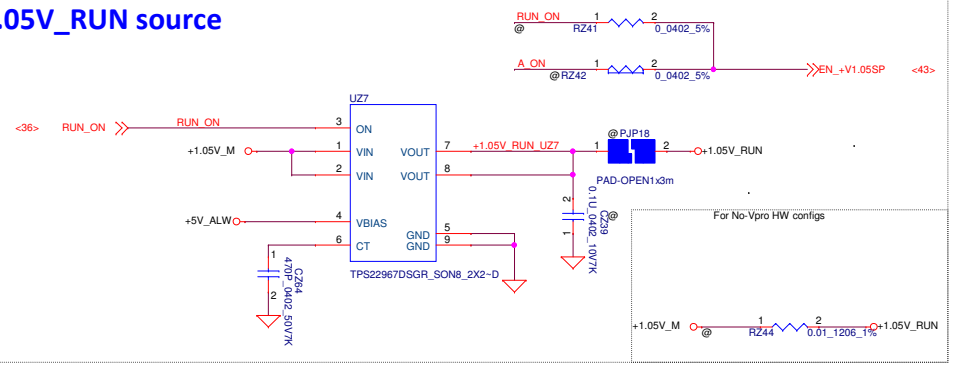
+1.05V_MODPHY

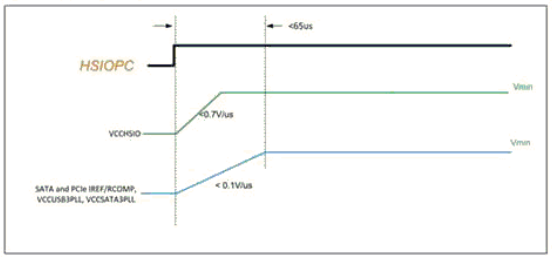


+1.05V_RUN source

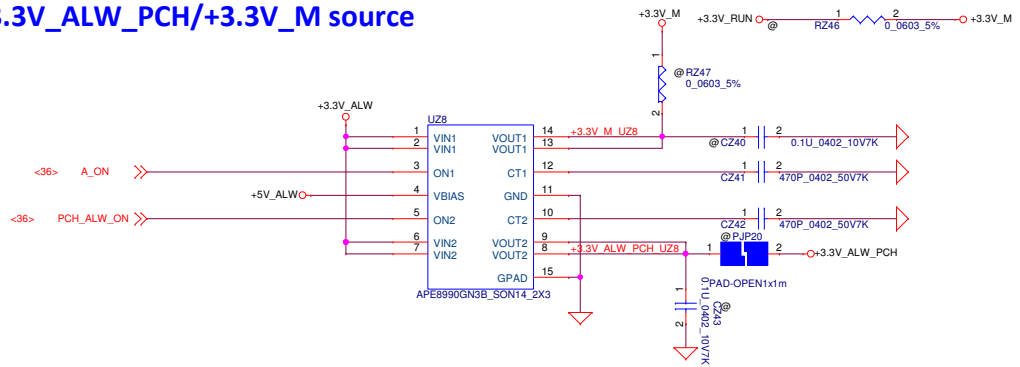


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

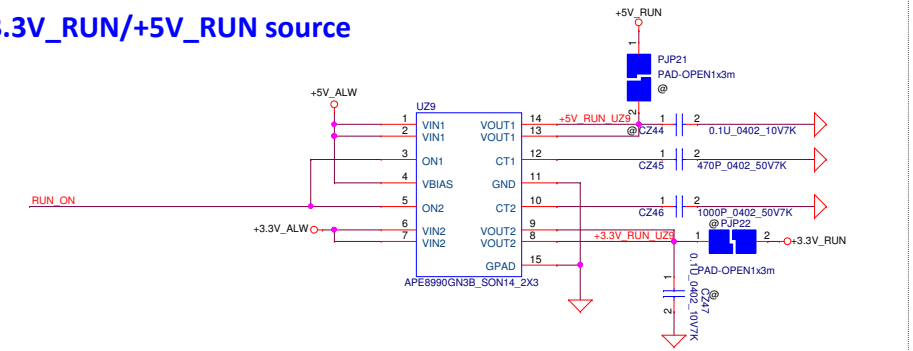
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



+3.3V_ALW_PCH/+3.3V_M source



+3.3V_RUN/+5V_RUN source



Compal Electronics, Inc.

Title: Power control

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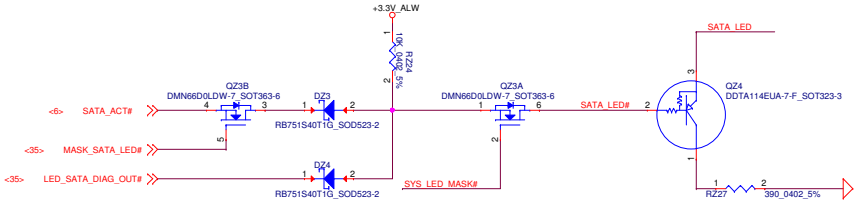
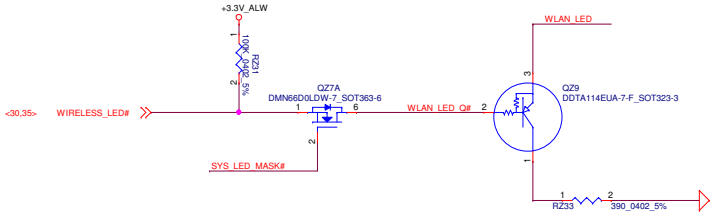
HDD LED solution for White LED

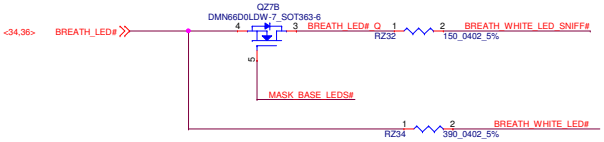


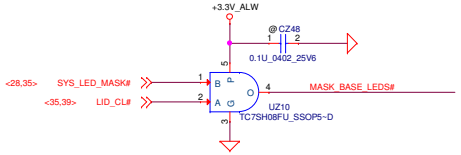
Battery LED

WLAN LED solution for White LED

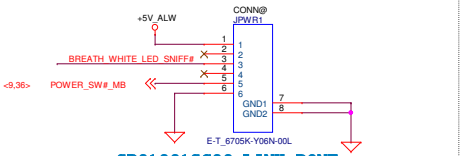


Breath LED



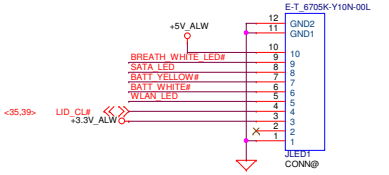


POWER board CONN

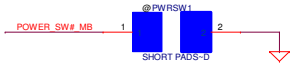


SP01001SC00 LINK DONE

LED board CONN



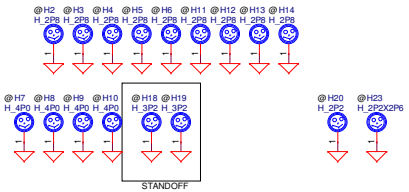
6705K-Y10N-00L LINK DONE



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

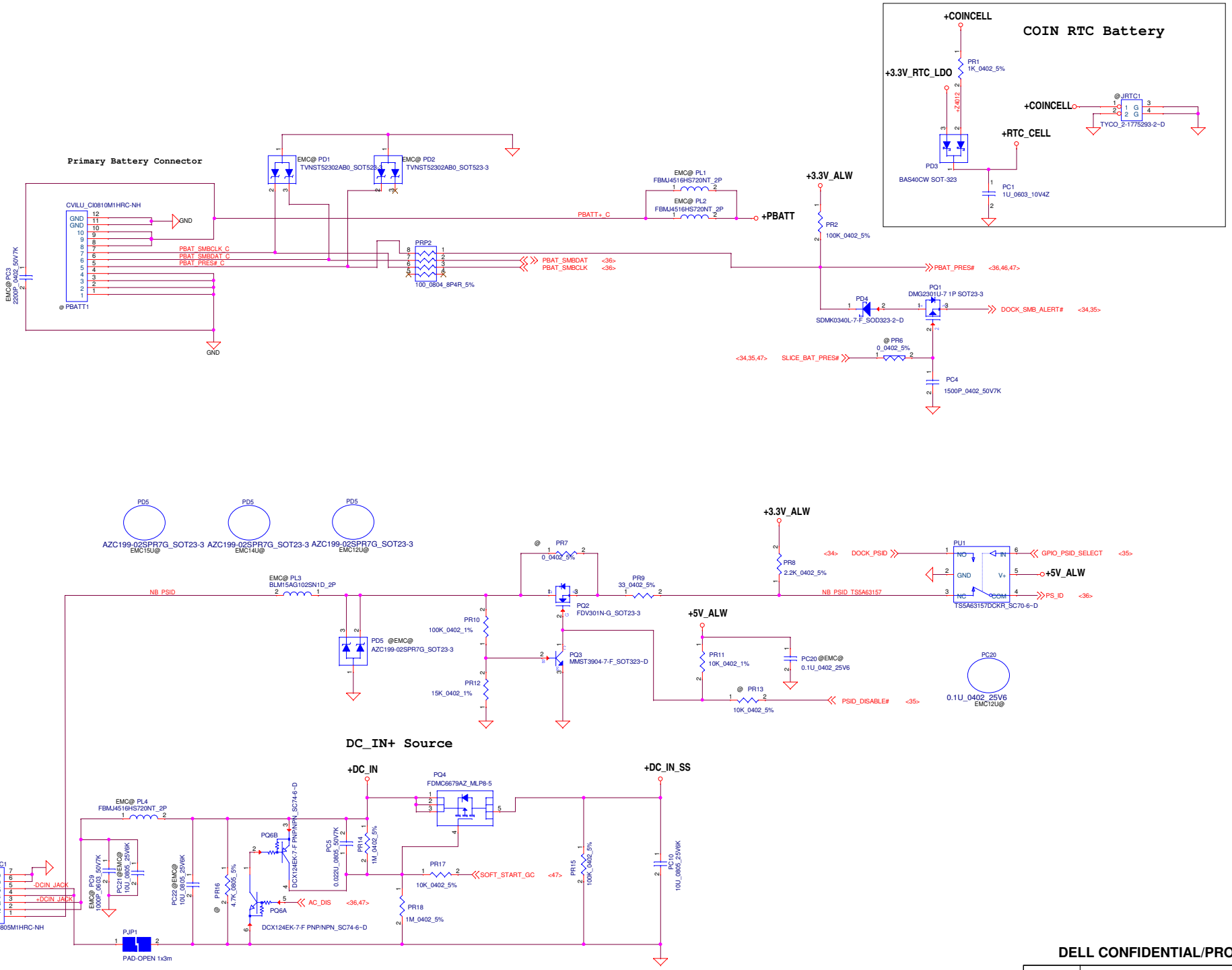


Compal Electronics, Inc.

Title: PAD, LED

Size: | Document Number: LA-A911P | Rev: 0.5

Date: Wednesday, July 16, 2014 | Sheet 39 of 55



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Title: +DCIN		
Size	Document Number: LA-A901P	Rev: 0.3
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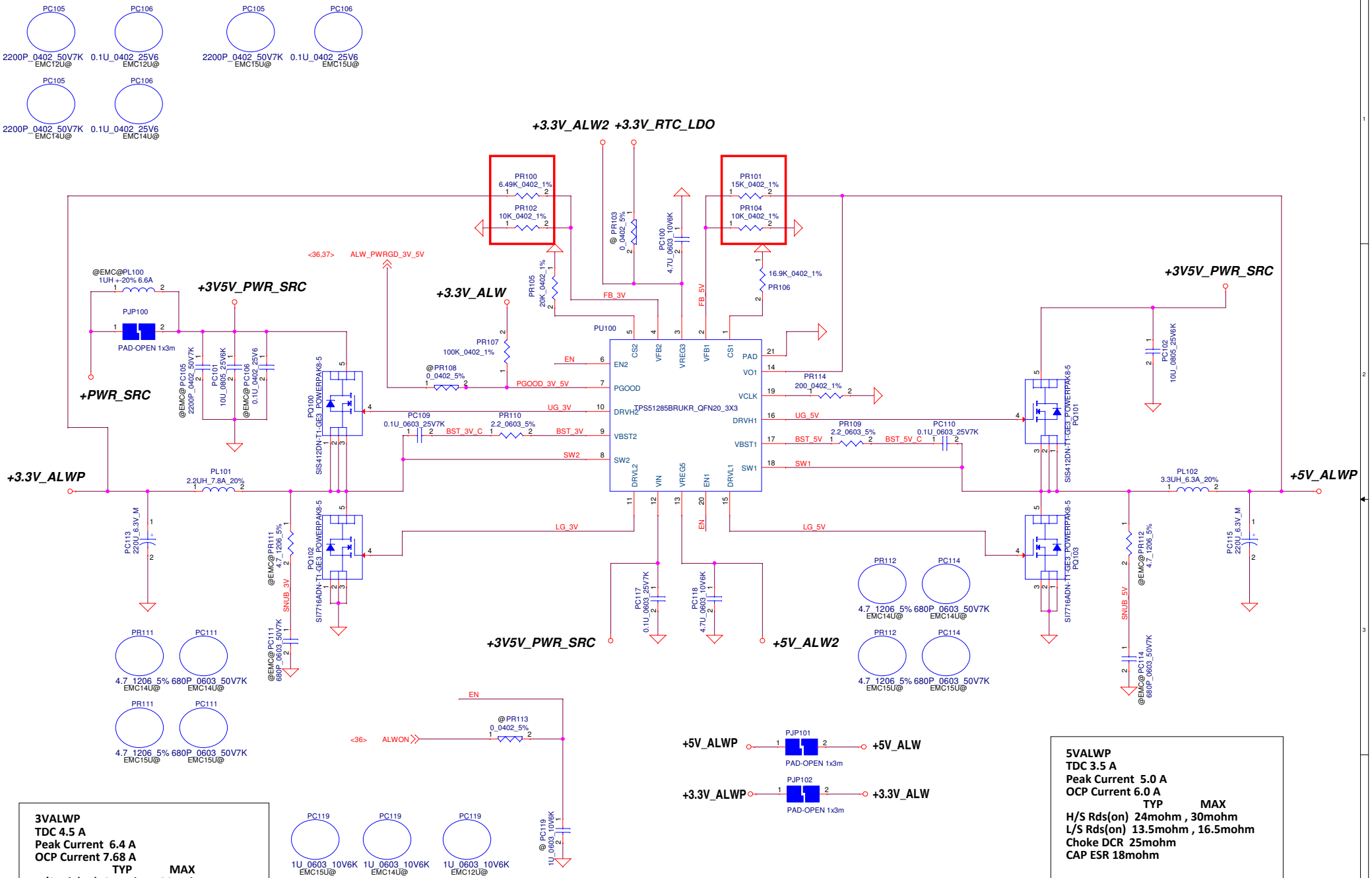

Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size: | Document Number: LA-A901P | Rev: 0.3

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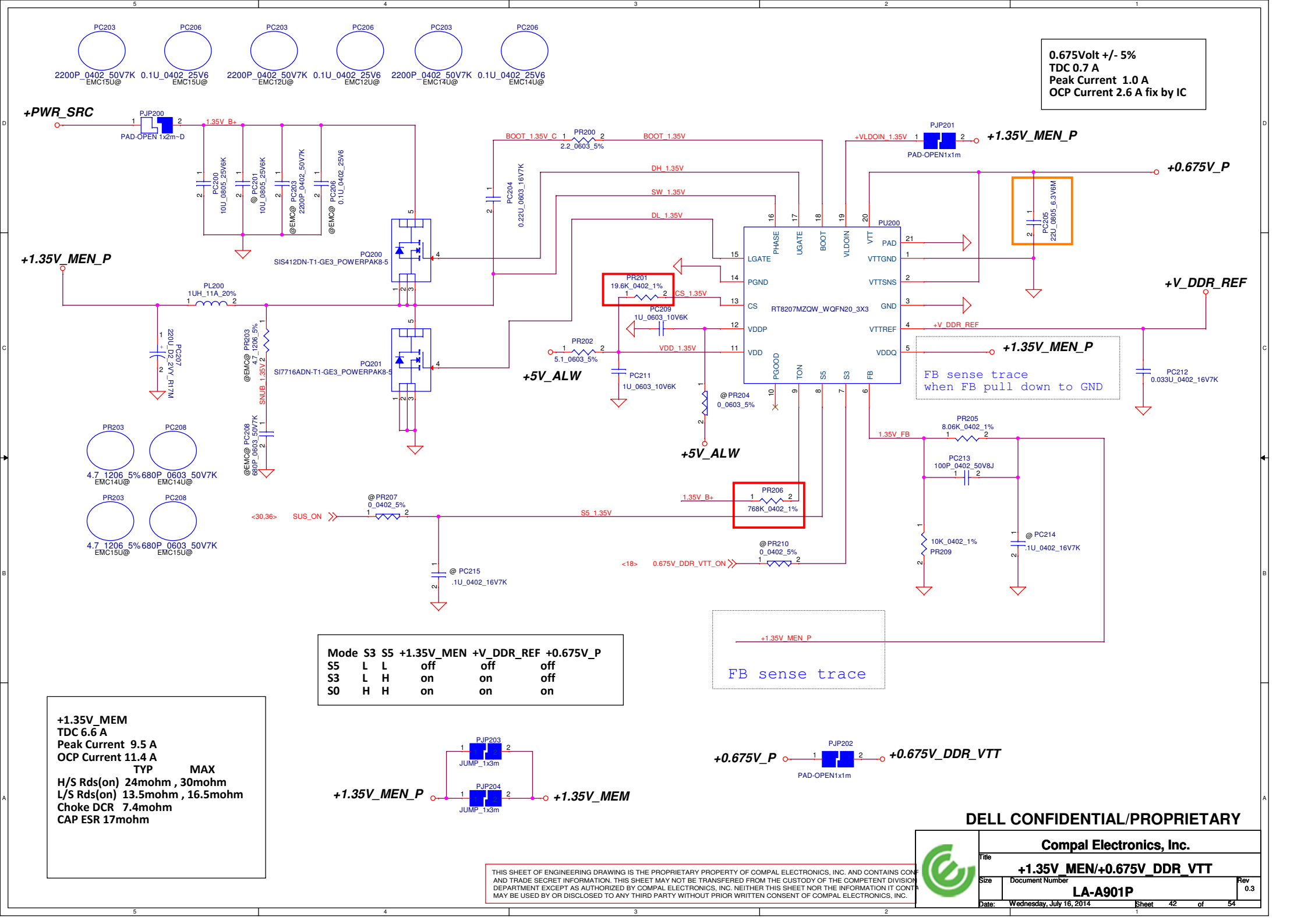
PC203 2200P_0402_50V7K EMC15U@
PC206 0.1U_0402_25V6 EMC15U@
PC203 2200P_0402_50V7K EMC12U@
PC206 0.1U_0402_25V6 EMC12U@
PC203 2200P_0402_50V7K EMC14U@
PC206 0.1U_0402_25V6 EMC14U@
0.675Volt +/- 5%
TDC 0.7 A
Peak Current 1.0 A
OCP Current 2.6 A fix by IC
+PWR_SRC
PJP200 PAD-OPEN 1x2m~D
1.35V_B+
PC200 10U_0805_25V6K
PC201 10U_0805_25V6K
@EMC@ PC203 2200P_0402_50V7K
@EMC@ PC206 0.1U_0402_25V6
+1.35V_MEN_P
PL200 1UH_11A_20%
PC207 220U_D2_2VY_R17M
@EMC@ PR203 4.7_1206_5%
SNUB_1.35V
@EMC@ PC208 680P_0603_50V7K
PR203 4.7_1206_5% EMC14U@
PC208 680P_0603_50V7K EMC14U@
PR203 4.7_1206_5% EMC15U@
PC208 680P_0603_50V7K EMC15U@
PQ200 SIS412DN-T1-GE3_POWERPAK8-5
PQ201 SI7716ADN-T1-GE3_POWERPAK8-5
BOOT_1.35V_C
PR200 2.2_0603_5%
BOOT_1.35V
PC204 0.22U_0603_16V7K
DH_1.35V
SW_1.35V
DL_1.35V
PR201 19.6K_0402_1%
CS_1.35V
PC209 1U_0603_10V6K
PR202 5.1_0603_5%
VDD_1.35V
PC211 1U_0603_10V6K
+5V_ALW
@PR204 0_0603_5%
+5V_ALW
PU200 RT8207MZQW_WQFN20_3X3
PHASE UGATE BOOT VLDOIN VTT PAD VTTGND VTTSNS GND VTTREF VDDQ
LGATE PGND CS VDDP VDD PGOOD TON S5 S3 FB
PJP201 PAD-OPEN1x1m
+VLDOIN_1.35V
+1.35V_MEN_P
+0.675V_P
PC205 22U_0805_6.3V6M
+V_DDR_REF
+V_DDR_REF
+1.35V_MEN_P
FB sense trace
when FB pull down to GND
PC212 0.033U_0402_16V7K
PR205 8.06K_0402_1%
1.35V_FB
PC213 100P_0402_50V8J
10K_0402_1% PR209
@ PC214 .1U_0402_16V7K
@PR207 0_0402_5%
<30,36> SUS_ON
S5_1.35V
1.35V_B+
PR206 768K_0402_1%
@PR210 0_0402_5%
<18> 0.675V_DDR_VTT_ON
@ PC215 .1U_0402_16V7K
+1.35V_MEN_P
FB sense trace
Mode S3 S5 +1.35V_MEN +V_DDR_REF +0.675V_P
S5 L L off off off
S3 L H on on off
S0 H H on on on
+1.35V_MEM
TDC 6.6 A
Peak Current 9.5 A
OCP Current 11.4 A
TYP MAX
H/S Rds(on) 24mohm , 30mohm
L/S Rds(on) 13.5mohm , 16.5mohm
Choke DCR 7.4mohm
CAP ESR 17mohm
PJP203 JUMP_1x3m
+1.35V_MEN_P
PJP204 JUMP_1x3m
+1.35V_MEM
+0.675V_P
PJP202 PAD-OPEN1x1m
+0.675V_DDR_VTT
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Compal Electronics, Inc.
Title +1.35V_MEN/+0.675V_DDR_VTT
Size Document Number LA-A901P Rev 0.3
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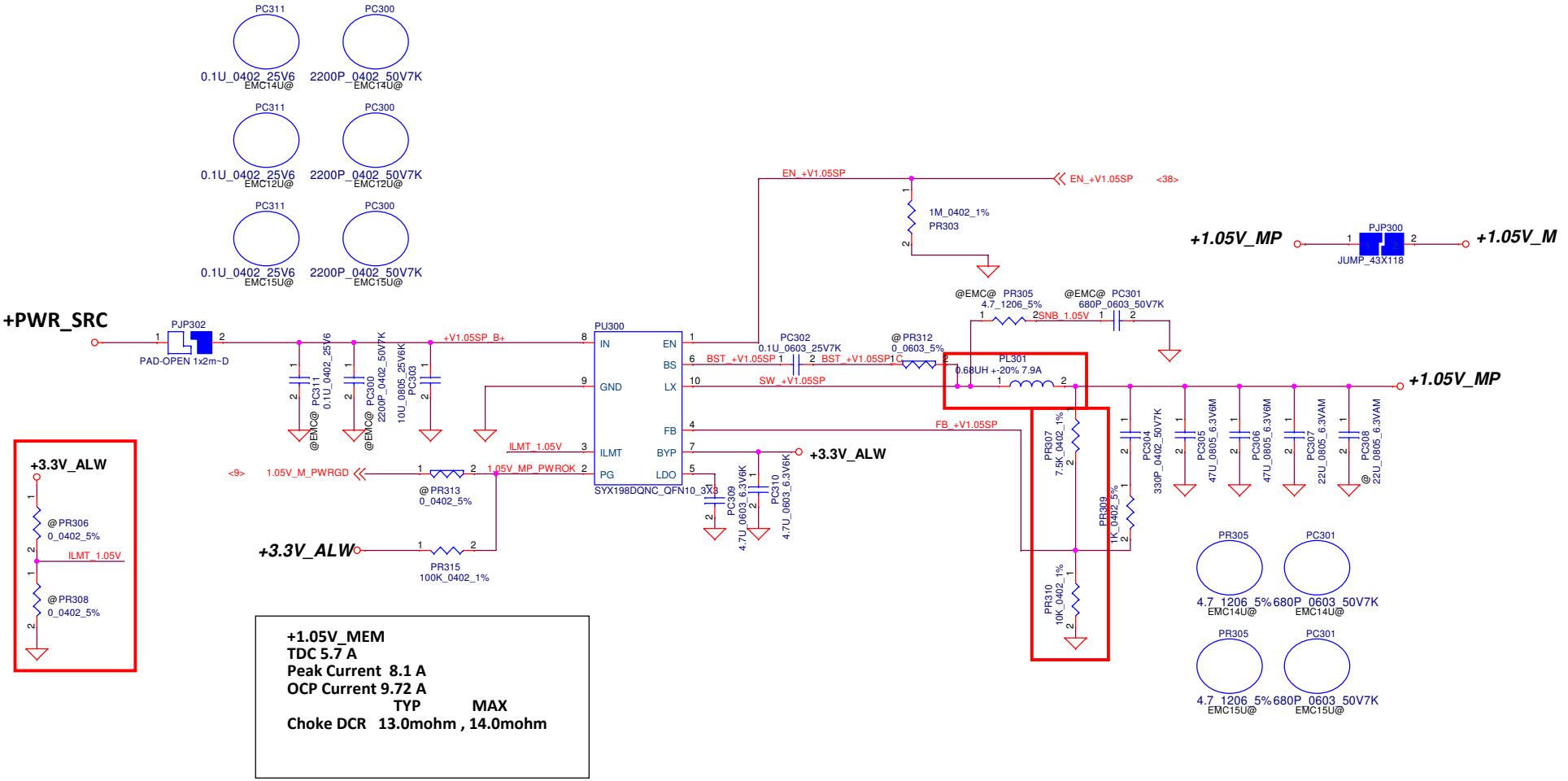

+1.05V_MEM
TDC 5.7 A
Peak Current 8.1 A
OCP Current 9.72 A

	TYP	MAX
Choke DCR	13.0mohm ,	14.0mohm

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Title: +1.05V_M		
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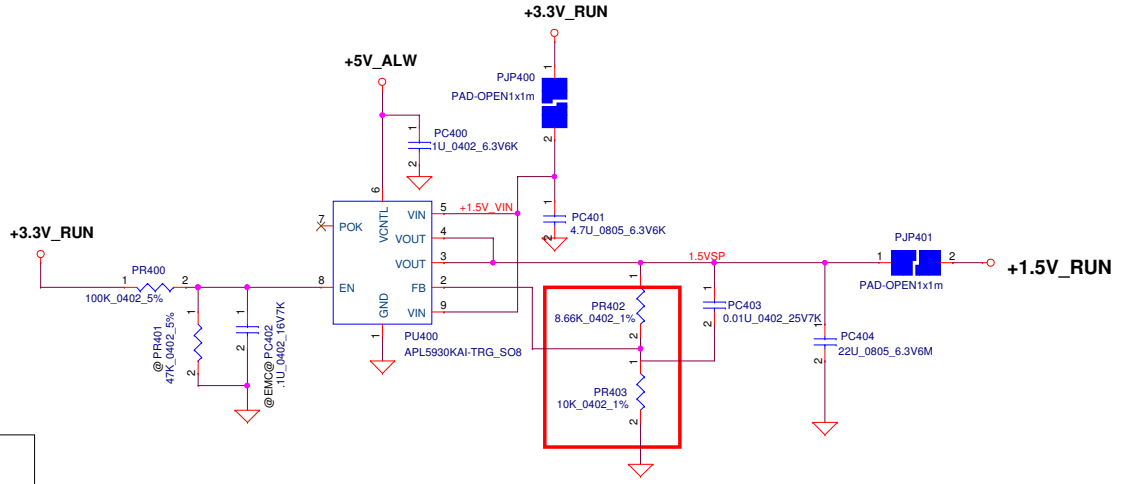

+1.5V_RUN
TDC 0.47 A
Peak Current 0.67 A

Compal Electronics, Inc.		
Title: +1.5V_RUN		
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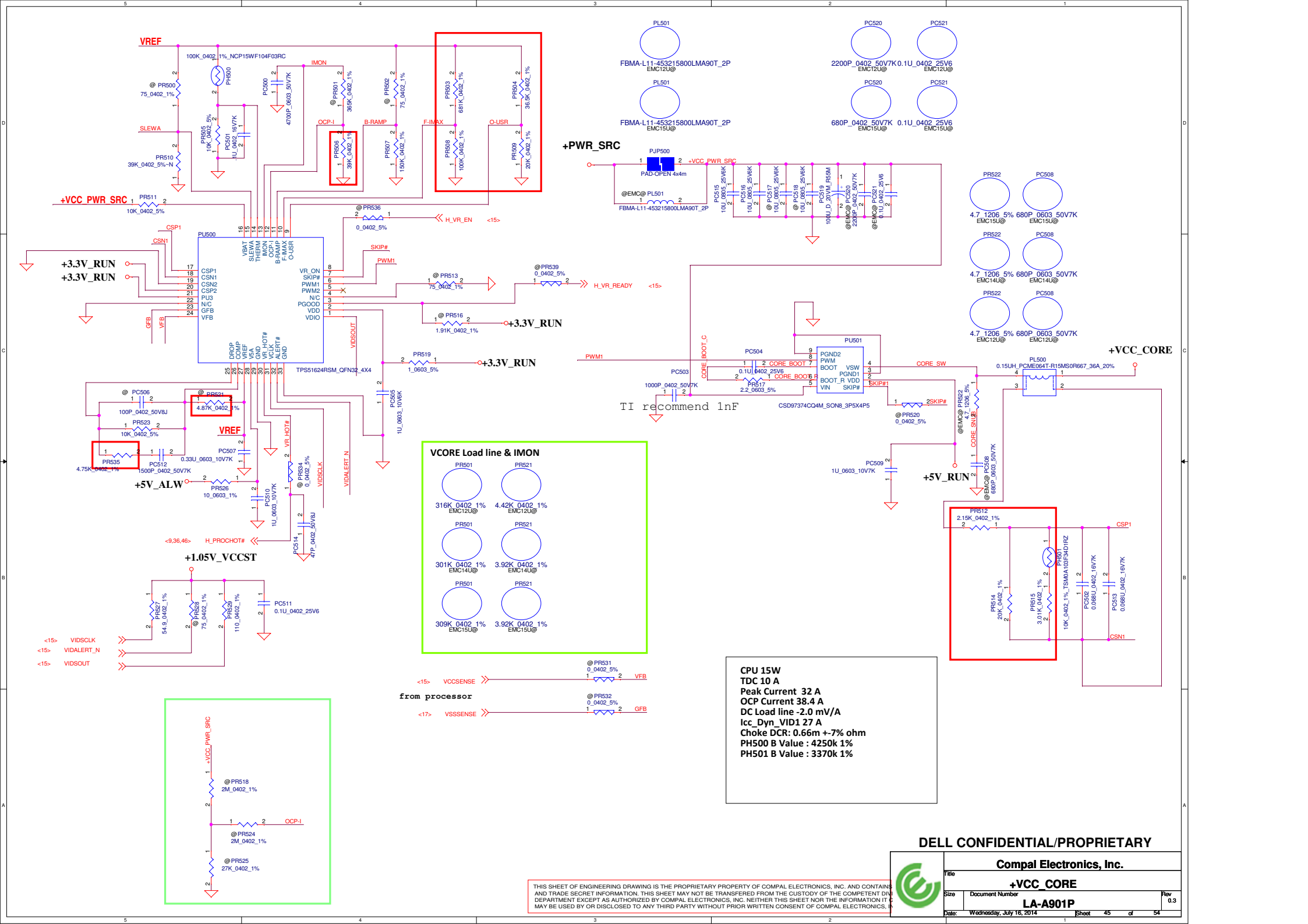

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Title: +VCC_CORE

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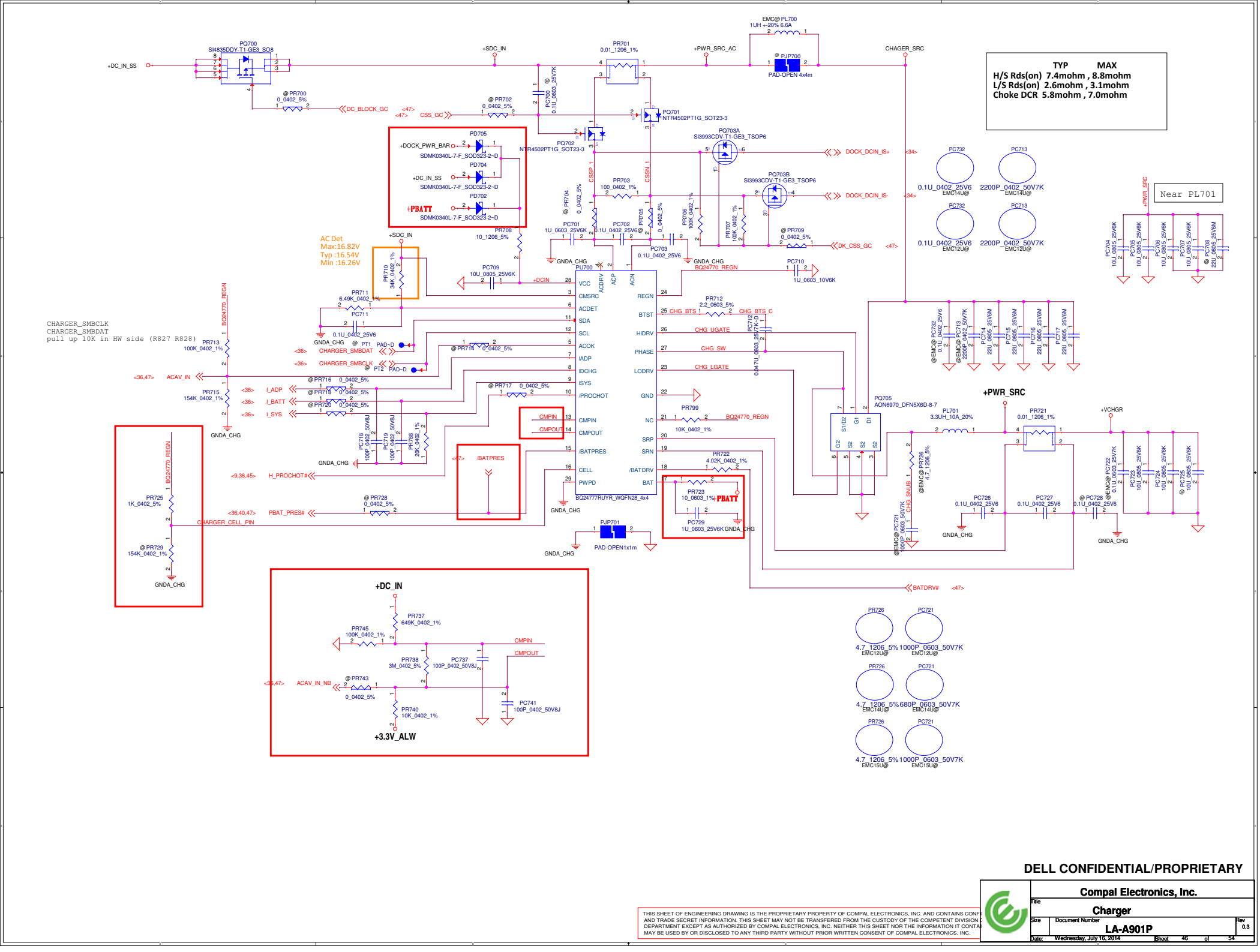
TYP MAX
H/S Rds(on) 7.4mohm , 8.8mohm
L/S Rds(on) 2.6mohm , 3.1mohm
Choke DCR 5.8mohm , 7.0mohm
Near PL701
AC Det
Max:16.82V
Typ :16.54V
Min :16.26V
CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side (R827 R828)
+PWR_SRC
+DC_IN
+3.3V_ALW
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Compal Electronics, Inc.
Charger
LA-A901P
Rev 0.3
Wednesday, July 16, 2014
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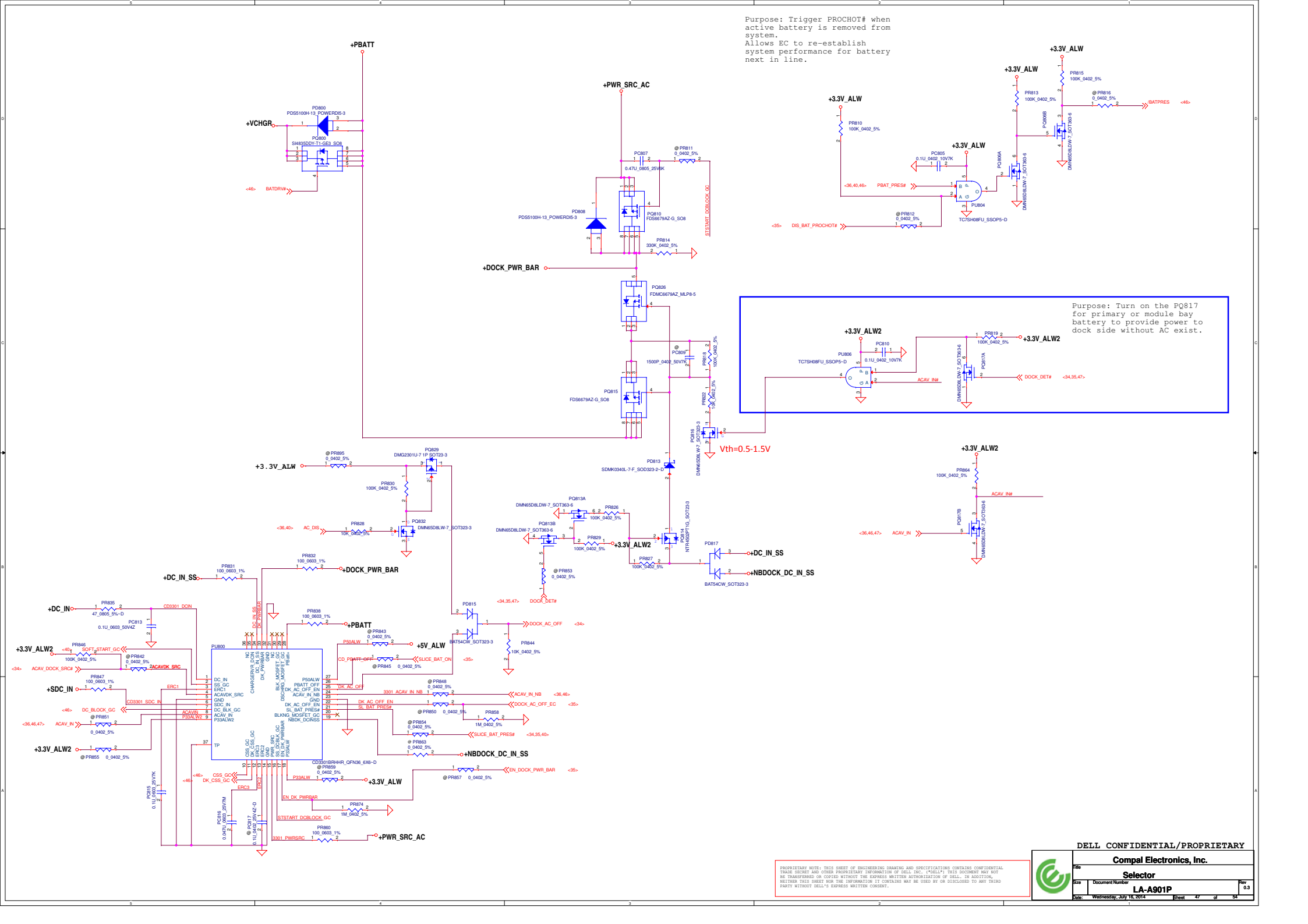
Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.



Compal Electronics, Inc.			
Title: Selector			
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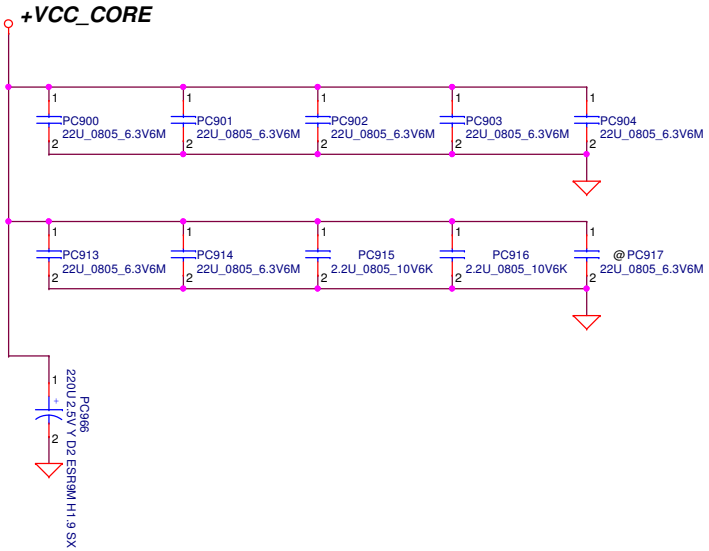

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812 , PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
5	41,43,44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 (0.1uF)	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111,PC111,PR112,PC114,PR203,PC208,PR305,PC301,PR522,PC508, (4.7ohm, 680pF)	X01
10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01
11	46	Charger	12/05	Compal	To reduce leakage current	Remove PD701 Add PD704, PD705	X01
12	46	Charger	3/03	Compal	To set OVP level	depop PR729 change PR725 to 1k	X02
13	46	Charger	3/03	Compal	To set IC function	Remove PC720 Add PR788, PR799	X02
14	40	DCIN	3/03	Compal	For ME change request	Change PBATT1	X02
15	40	DCIN	3/03	Compal	For EMC change request	Add PD5 PC20 PC21 PC22 Remove PC11	X02
16	40	DCIN	3/03	Compal	For ME change request	Change PJPDC1	X02
17	46	Charger	3/20	Compal	To avoid unplug AC shutdown, there is no AC off signal in BIOS set up menu	Change PR710 to 34k Change PR711 to 6.49k	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
18	46	Charger	5/22	TI	To prevent acoustic noise issue	PL701 change from 2.2uH to 3.3uH	X03
19	40	DCIN	5/22	Compal	For ME change request	Change PBATT1	X03

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2(X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2(X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2(X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. add QV20,CZ69,RV210,RV212,QV21 external FET switch circuit 7. UV8 pin B5, B6 change to +3.3V_RUN_VMM 8. LP_CTL add RV516, 2.2K resistor PU to +3.3V_RUN_VMM 9. Depop RV73 10. add LP_EN on UV8.A5 (10/18) 11. depop QV20,CZ69,RV210,RV212, QV21 external FET switch circuit (10/24) 12.RPV2 pin1 & pin2 NC (11/4)	0.2(X01)
5	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV9,LV12,LV27 From SM070003K00 (S COM FI_ CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_ MURATA DLW21HN900HQ2L)	0.2(X01)
6	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, , reserved RC27.	0.2(X01)
7	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2(X01)
8	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2(X01)
9	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2(X01)
10	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
11	7,38	HW	2013/10/17	COMPAL	for UMA DOCK configure, it support has non-VPRO configure.	add PJP33, PJP34 UC3, CC7, RC50, RC55, RPC12, UZ7, CZ64 change to VPRO@	0.2(X01)
12	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2(X01)
13	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	remove QZ5, QZ7.2 & QZ3.2 change to SYS_LED_MASK#	0.2(X01)
14	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	add UN3, CN3, CN4, PJP7 and reserved it.	0.2(X01)
15	30,36	HW	2013/10/17	COMPAL	follow Dell requirement.	add back SUS_ON, change +3.3V_SUS control pin to SIO_SLP_S4# 1. UL3.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 → SUS_ON_EC , RPE10.2 → SUS_ON 3. add RE282(Pop), RE281(depop) 4. add RE279, RE280 (dock only) 5. UE2.B9 → RUN_ON_EC	0.2(X01)
16	23	HW	2013/10/18	COMPAL	follow ESD recommend.	LZ1 change from SM070001N00 to SM070003Y00	0.2(X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4 to replace PCH_GPIO48, remove	0.2(X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2(X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2(X01)
20	30	HW	2013/10/29	COMPAL	New SIM connector has no this pin.	remove UIM_DET on JNGFF2 pin58	0.2(X01)
21	23	HW	2013/10/29	COMPAL	it's designed for Goliad, Houston doesn't need.	remove RZ1	0.2(X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ43, 100k pull up for WWAN_PWR_EN	0.2(X01)
23	38	HW	2013/10/29	COMPAL	for support VPRO & NVPRO BOM option.	remove PJP33, PJP34, PJP19 add RZ44, RZ46, RZ47	0.2(X01)
24	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up (RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2(X01)
25	37	HW	2013/10/29	COMPAL	Dell request.	add RZ48, RZ49, QZ12 depop UZ5, UZ6, RZ21, RZ22, CZ35,RC91 (11/4) add RZ51, change QZ12 from 3904 to 3906. make RPE6 to be NC pin, add RE88 (11/4)	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
26	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2(X01)
27	28	HW	2013/11/04	COMPAL	SSI design will cause LED behavior error.	Change QL1, QL2 contorl pin from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2(X01)
28	21	HW	2013/11/04	COMPAL	EMC request.	Add RA42, RA43.	0.2(X01)
29	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2(X01)
30	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2(X01)
31	30	HW	2013/11/05	COMPAL	follow vender request.	RZ43 from 100K change to 0 ohm	0.2(X01)
32	20	HW	2013/11/06	COMPAL	For SATA repeater setting	RN9,RN11,RN13,RN16 pop 0ohm	0.2(X01)
~~33~~	~~28~~	~~HW~~	~~2013/11/06~~	~~COMPAL~~	~~For EMI request~~	~~RL21~ RL28 change to 5.6 ohm~~	~~0.2(X01)~~
34	21	HW	2013/11/20	COMPAL	follow vender suggest to solve "Bo" noise issue	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.2(X01)
35	12,22	HW	2013/11/20	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM	0.2(X01)
36	22	HW	2013/11/27	COMPAL	To solve CRT display jitter issue	1.LV23,LV25 change from BLM15AX102SN1D to BLM15PX181SN1D 2.CV90,CV101 change from 1uF to 10uF	0.2(X01)
37	36,37	HW	2013/11/27	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2.remove QZ12,RZ48,RZ49,RZ50	0.2(X01)
38	6	HW	2013/11/29	COMPAL	follow intel DG, ESR MAX=50 ohm	Change YC1 from SJ100001K00(S CRYSTAL 32.768KHZ Q13FC1350000400) to SJ10000LD00(S CRYSTAL 32.768KHZ 12.5PF 9H03220008)	0.2(X01)
39	28	HW	2013/11/29	COMPAL	base on LAN EA result to modify R value	Change RL21~RL28 from 5.6K to 2.2K	0.2(X01)
40	22	HW	2013/12/10	COMPAL	follow vender suggestion	1. change LV22,LV24 from SM01000N400(S SUPPRE_ MURATA BLM15AX102SN1D 0402) to SM01000NO00(S SUPPRE_MURATA BLM15PX181SN1D 0402) 2. change CV82, CV94 from 1uF to 10uF 3. UV8 pin D3 from +1.05V_VMM_VDDTX to+1.05V_VMM_VDD. 4. UV8 Pin H3, E10, H11 change to NC 5. Change UV8 pin B5, B6 from +3.3V_RUN_VMM to +3.3V_RUN_VDDIO	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
41	34	HW	2013/12/18	COMPAL	To solve Power leakage issue.	Change R272 from 10K to 100K, and pull up to +3.3V_ALW2	0.2(X01)
42	21	HW	2013/12/18	COMPAL	follow ESD/vender request	1. change RA42, RA43 to LA10, LA1 SM01000NA00(S SUPPRE_ MURATA BLM15PX330SN1D 0402) 2. change RA7, RA8 from 16 to 24.9 ohm 3. DA1 &DA3 change from SCA00002900 to SCA00001B00(S ZEN ROW AZ5123-02S.R7G 3P C/A SOT23) 4.CA4&CA1 change from 220pF(@EMC@) to 680pF(EMC@)	0.2(X01)
43	26	HW	2013/12/18	COMPAL	Base on CRT EA result	change CV51, CV52, CV53 from 12pF to 2.2pF	0.2(X01)
44	20	HW	2013/12/18	COMPAL	For SATA repeater setting	Depop RN9,RN13	0.2(X01)
45	7	HW	2013/12/27	COMPAL	Follow Intel CRB schematic	RC33&RC34 change from 1k ohm to 499 ohm	0.2(X01)
46	6,7,22	HW	2013/12/27	COMPAL	follow xtal vender suggest	1. CC8,CC11 change from 18pF to 15pF 2. CV113,CV115 change from 22pF to 18pF,RV81 change from 0ohm to 820ohm 3. CC1,CC2 change from 18pF to 8pF	0.2(X01)
47	38	HW	2014/02/06	COMPAL	For MODPHY power rail contril by JUMP directly	1.change PJP36 pin1 from +1.05V_M to +1.05V_RUN 2.depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.3(X01)
48	25	HW	2014/02/06	COMPAL	Base on PS8338 datasheet, PI0 have 2 level, PI1 have 3 level	For PI0, delete RV66 For PI1, add RV100 PD to GND	0.3(X01)
49	36	HW	2014/02/10	COMPAL	EC request, for Delray common code reserved.	add RE283(@)	0.3(X01)
50	29	HW	2014/02/27	COMPAL	EMI test fail , back to SSI SD card connector.	change JSD1 from TAITW_PSDCT6-20GLBS1NN4H_19P-T to ALPS_SCDADA0101_19P_NR	0.3(X01)
51	9,16	HW	2014/03/03	COMPAL	follow intel DG 1.2	1.reserved 0.47uF for +PCH_VCCDSW3_3 , near CPU AH10 pin 2.add 10K pull high to +PCH_VCCDSW3_3 for PM_LANPHY_ENABLE, leave RPC1. pin 7 NC	0.3(X01)
52	30	HW	2014/03/05	COMPAL	intel Wigig need 32K clock when DSx	1.Add UZ11&RZ56(@)&RZ57 2.JNGFF1 change to WIGIG_32KHZ from SUSCLK 3.JNGFF2.60 change to NC from SUSCLK	0.3(X01)
53	34	HW	2014/03/05	COMPAL	for EMI requset	1. pop R273,R6,R41,C319,C42,C43 2.R273 change from 33 ohm to 10 ohm 3.C319 change from 4.7pF to 12 pF	0.3(X01)
54	7	HW	2014/05/09	COMPAL	for SMT open soldering issue	JSPI1 change from TYCO_2-2041070-0_20P-T to E-T_6705K-Y20N-00L_20P	0.4(X02)
55	9	HW	2014/05/09	COMPAL	Follow INTEL XDP DG	CFG3 add RC305(XDP@) 1k PD	0.4(X02)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
56	39	HW	2014/05/09	COMPAL	For LED brightness measure	RZ25&RZ33 change from 390 ohm to 220 ohm	0.4(X02)
57	25	HW	2014/05/16	COMPAL	For Display priority issue	add QV11 & pop RV52	0.4(X02)
58	36	HW	2014/05/16	COMPAL	For ST Board ID	RE79 change from 130K to 33K	0.4(X02)
59	30	HW	2014/05/20	COMPAL	For HSW CPU no support Intel Wigig	Depop UZ11	0.4(X02)
60	9	HW	2014/05/20	COMPAL	For ESD request	Add CC101(@EMC@)	0.4(X02)
61	30	HW	2014/05/20	COMPAL	For ESD request	Add CZ68(EMC@)	0.4(X02)
62	12	HW	2014/05/20	COMPAL	For BDW & HSW CPU detect	1. Net name change from PCH_GPIO67 to CPU_SEL 2. add RC163(@) & RC306	0.4(X02)
63	39	HW	2014/05/20	COMPAL	For LED brightness measure	RZ25/RZ33/RZ27/RZ34 change from 220 ohm to 390ohm	0.4(X02)
64	36	HW	2014/07/1	COMPAL	For MP Board ID	RE79 change from 33K to 1K	1.0(A00)
65	6	HW	2014/07/1	COMPAL	Service Mode Switch modify	Change RC2,SW1 to BDW@,RC301 to HSW@	1.0(A00)
66	32	HW	2014/07/1	COMPAL	Change USB Power SW P/N for wake up issue.	Change UI3 P/N to TPS2544	1.0(A00)
67	28	HW	2014/07/1	COMPAL	WLAN can't recognize during enable Unobtrusive mode(BITS152312)	Add 1M PU (RL29,RL30) on LOM_SPD100LED_ORG# & LOM_SPD10LED_GRN#	1.0(A00)
68	29	HW	2014/07/1	COMPAL	JSD1 PAD issue for DFX	Change JSD1 from ALPS_SCDADA0101_NR to T-SOL_156-2000302608_NR-S	1.0(A00)