

Project Name :

Platform : SKYLAKE

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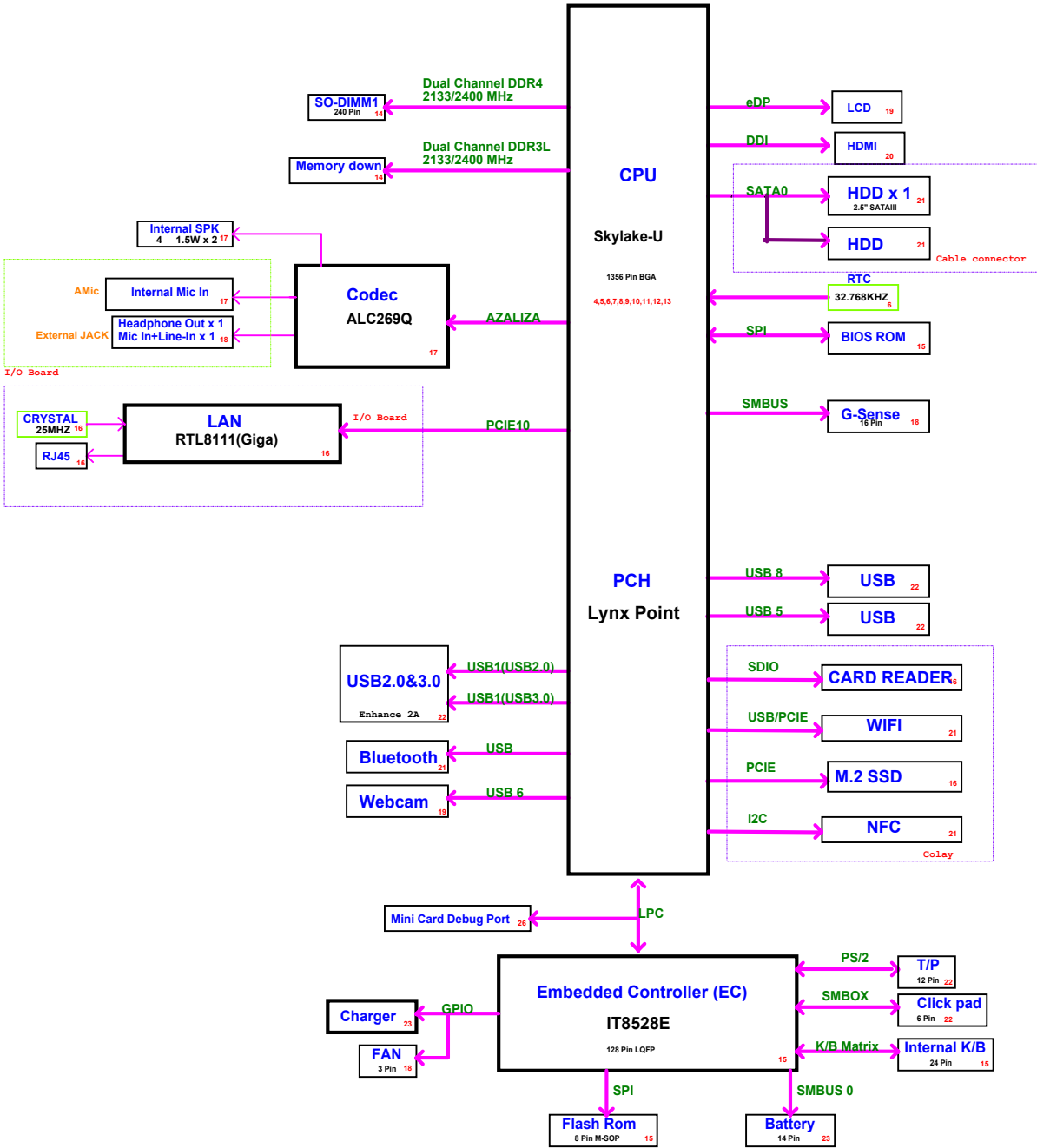
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note
2017-3-15	A				
2017-4-18	B				

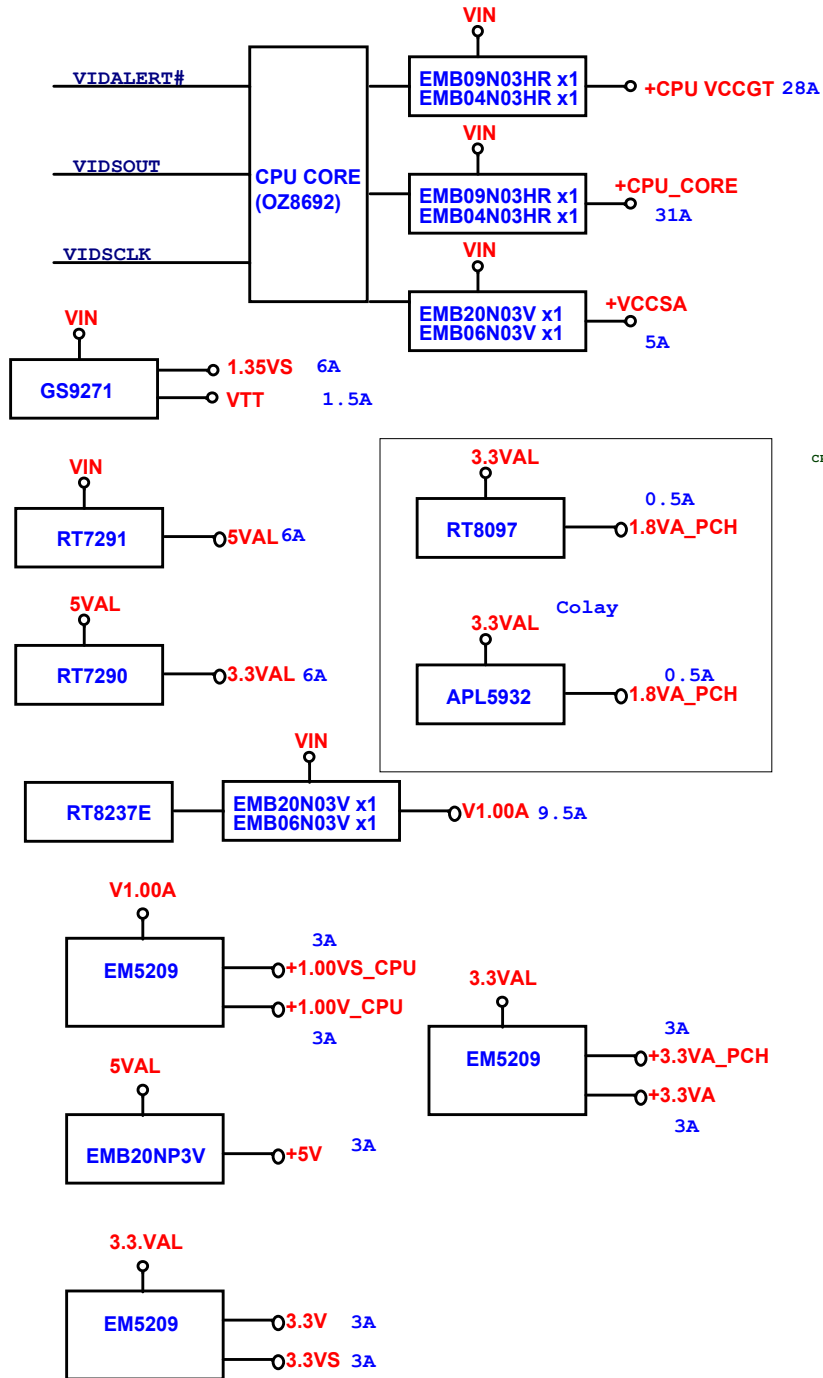
Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

SYSTEM BLOCK DIAGRAM



POWER BLOCK DIAGRAM



System Poewr On Sequence

Adaptor or Battery

PWRSW

+5VAL / +3.3VAL

VCCRTC

RTCST#

* DSW_PWR_EN

+3.3VA

DSW_PWROK

RSMRST#

PWRBTN#

* PM_SLP_S4#

* +3.3VS_ON

* +1.00VS_CPU

+3.3VS

CPU * * * PM_SLP_SUS#_R

EC * +1.8VA_PCH

V1.00A

+3.3VA_PCH

* * * PM_SLP_S3#

* * * PM_SLP_S0_S3#

+1.00V_CPU

* +5V_ON

+3.3V

+5.0v

* +1.35VS_ON

+1.35VS

VCCST_PWRGD

* * * DDR_VTT_CNTL

+0.675V_DDR

* VCORE_ON

+VCCSA

+CPU_CORE

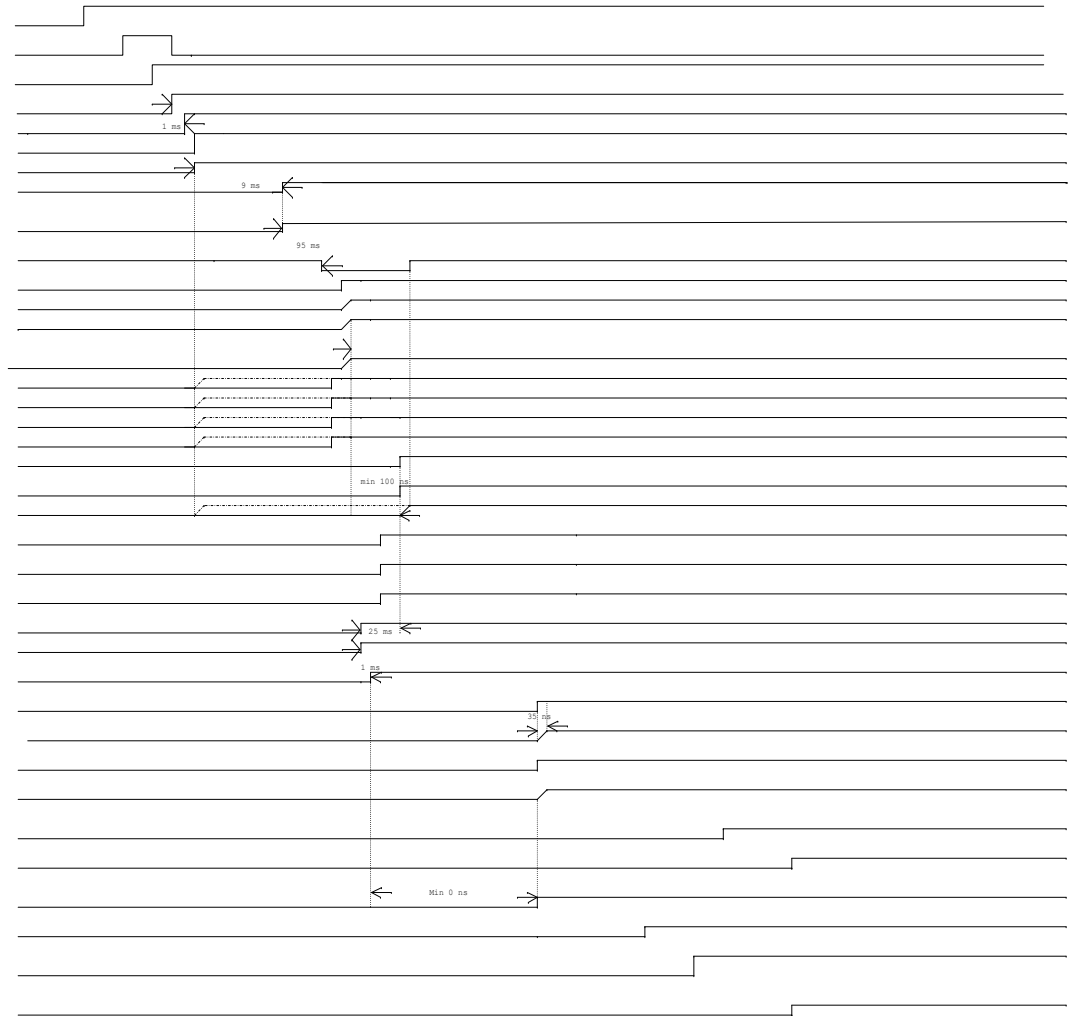
+CPU_VCCGT

* PCH_PWROK

* SYS_PWROK

PLTRST#

DDR_RST#

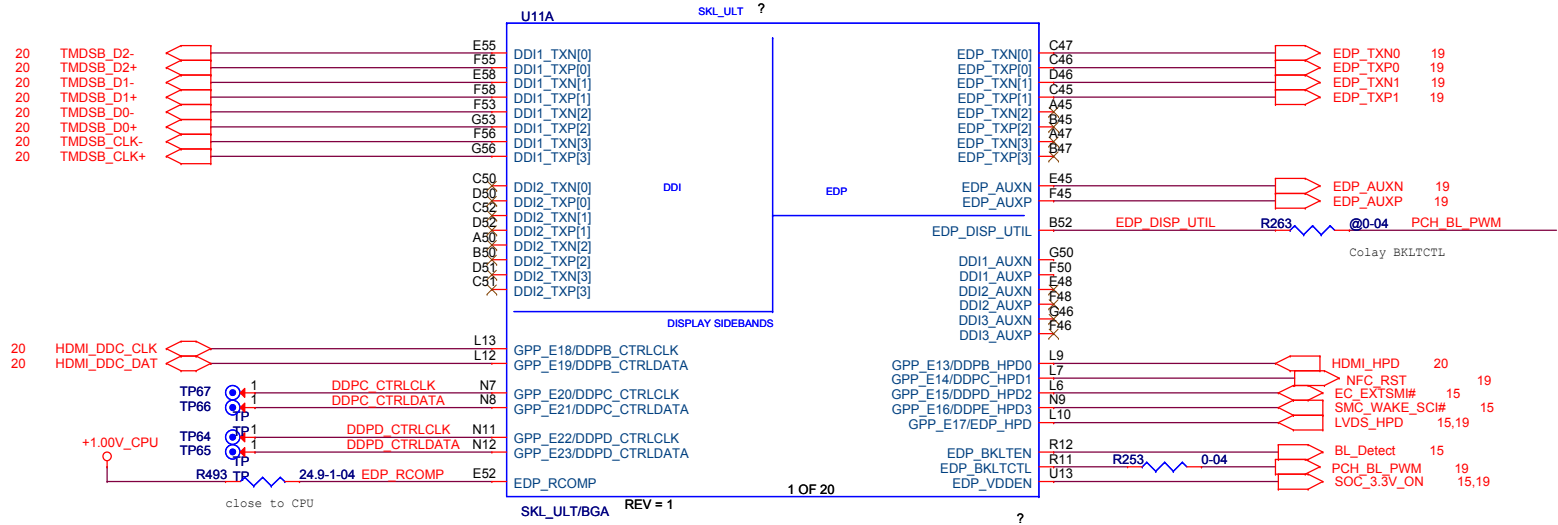


* * * CPU Control Pin (O/P)

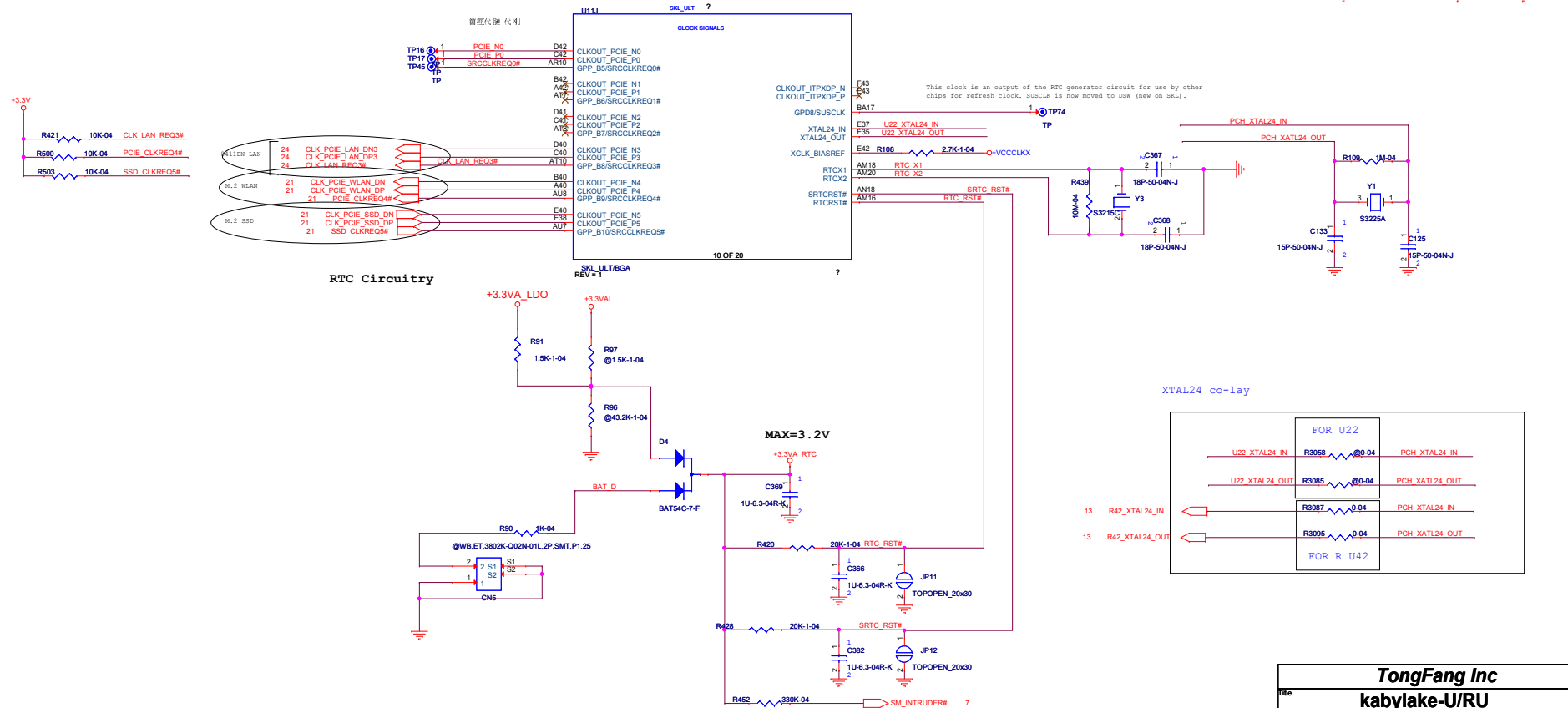
* EC Control Pin (I/P)

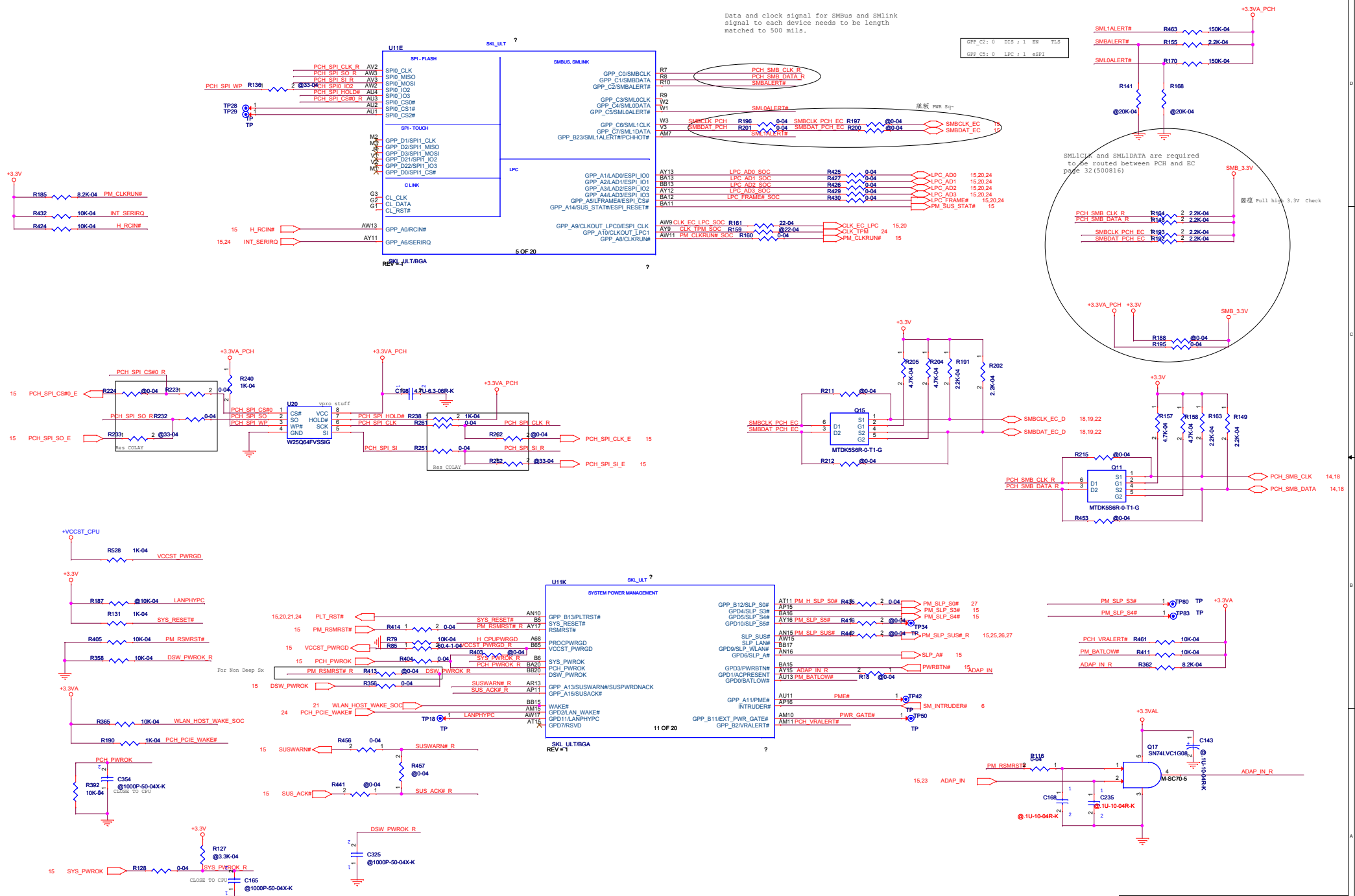
* EC Control Pin (O/P)

To disable DisplayPort* 1 and 2 leave as, No Connect



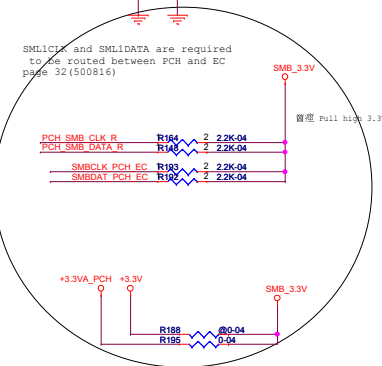
TongFang Inc			
kabylake-U/RU			
Title	Broadwell DDI(1 of 10)		
Size	Custom	Document Number	Rev B
Date:	Tuesday, April 25, 2017	Sheet	4 of 30

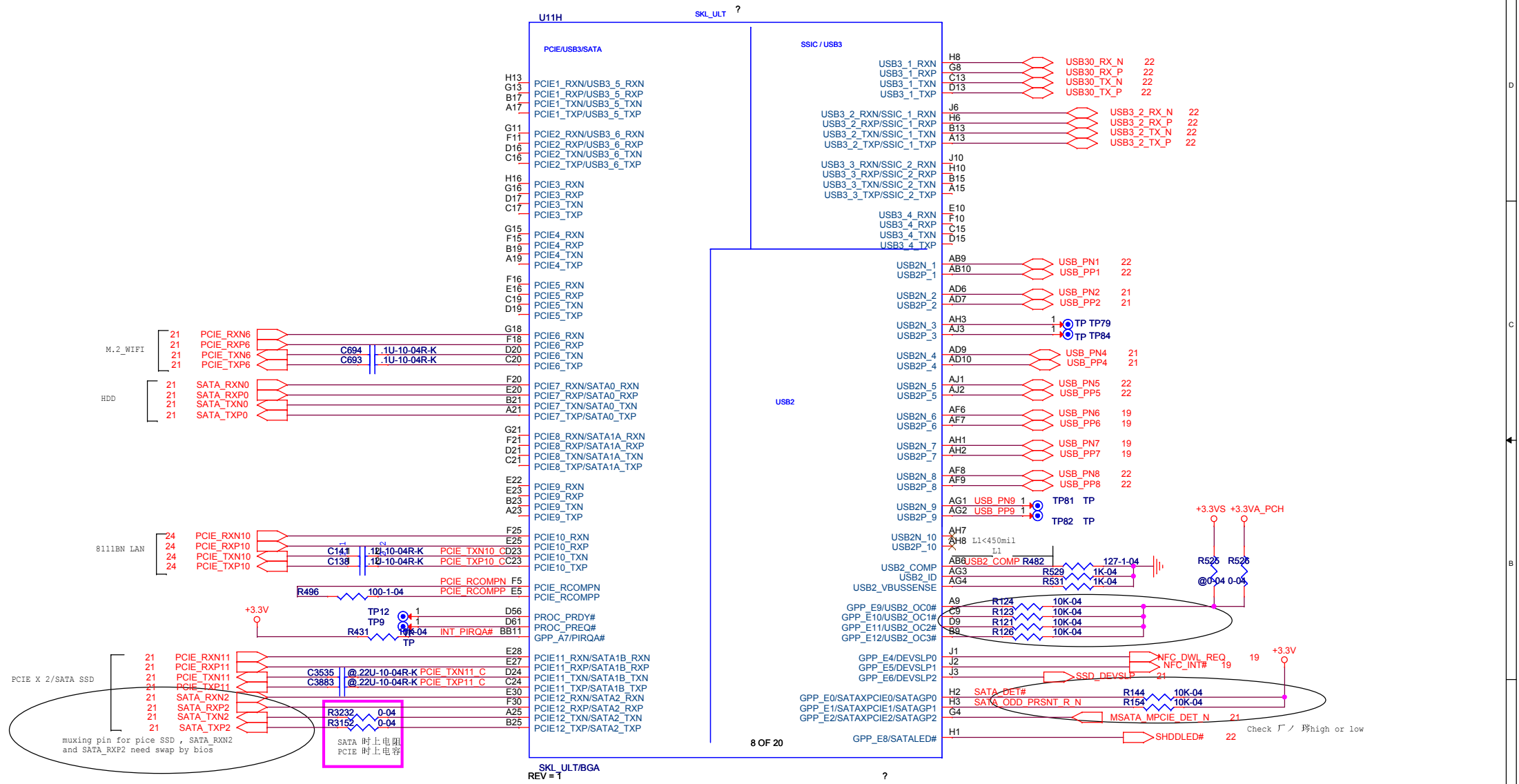


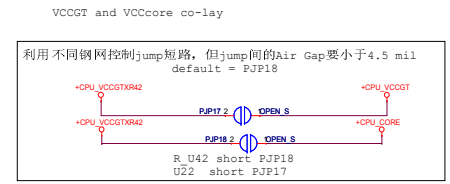
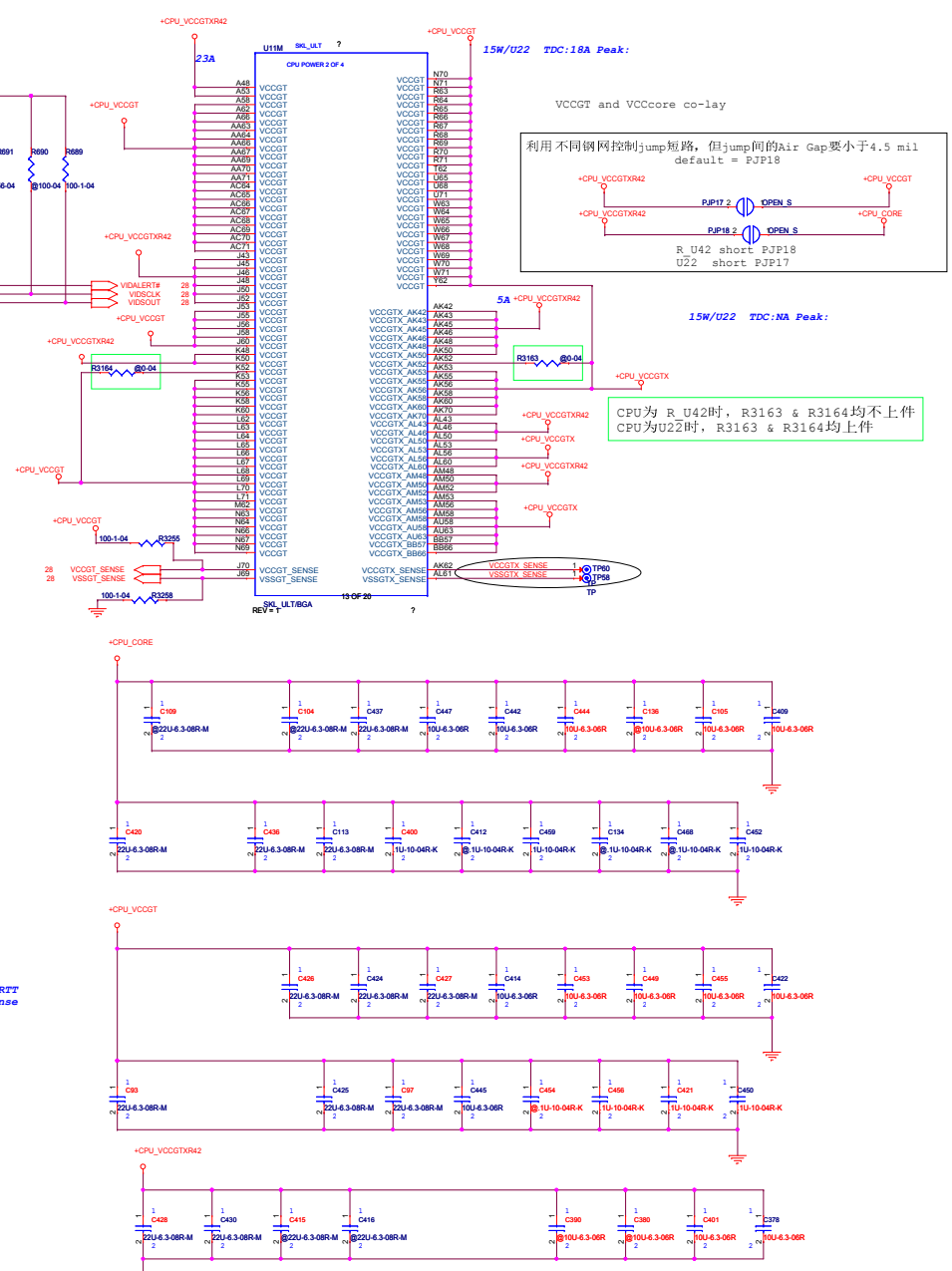
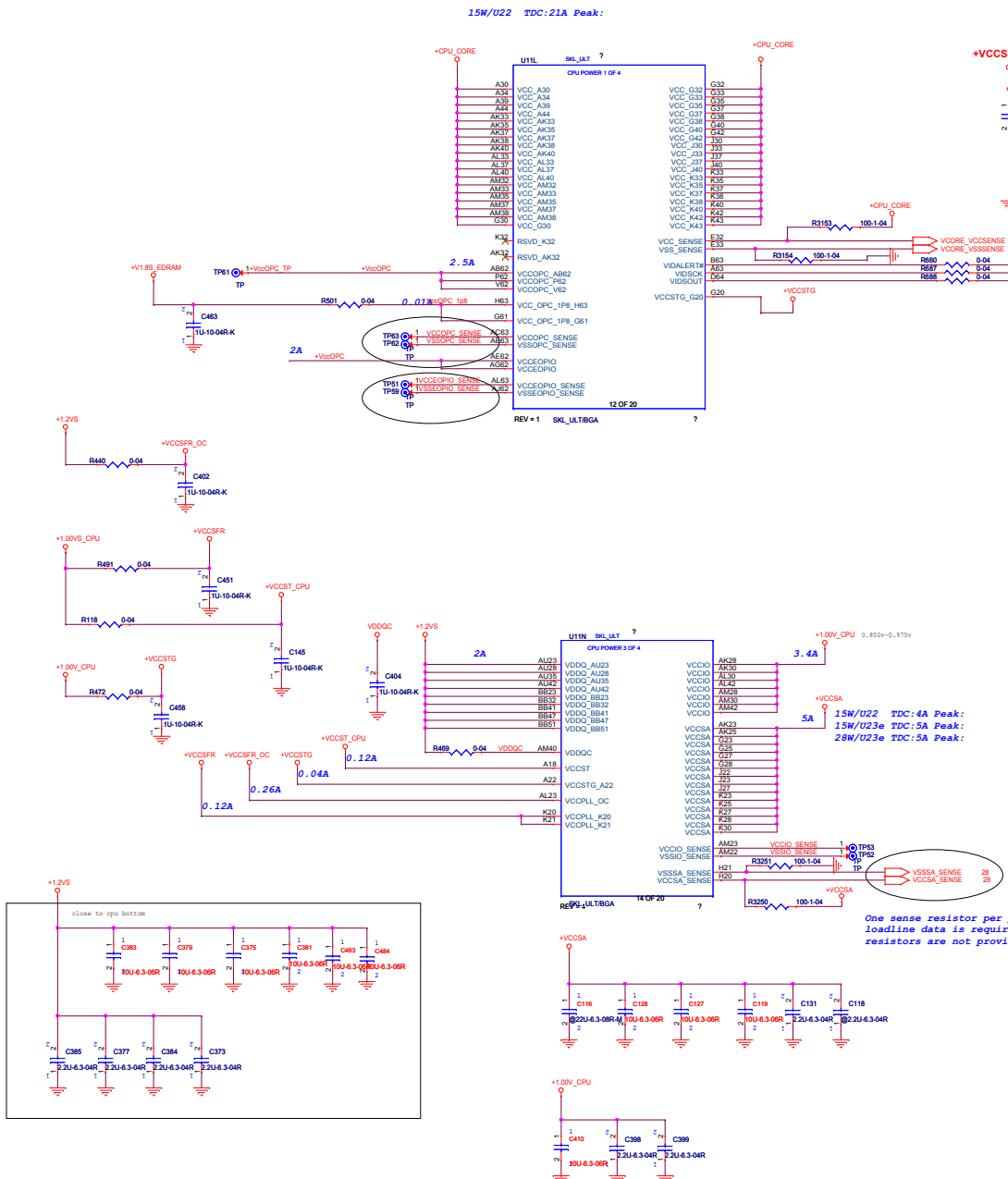


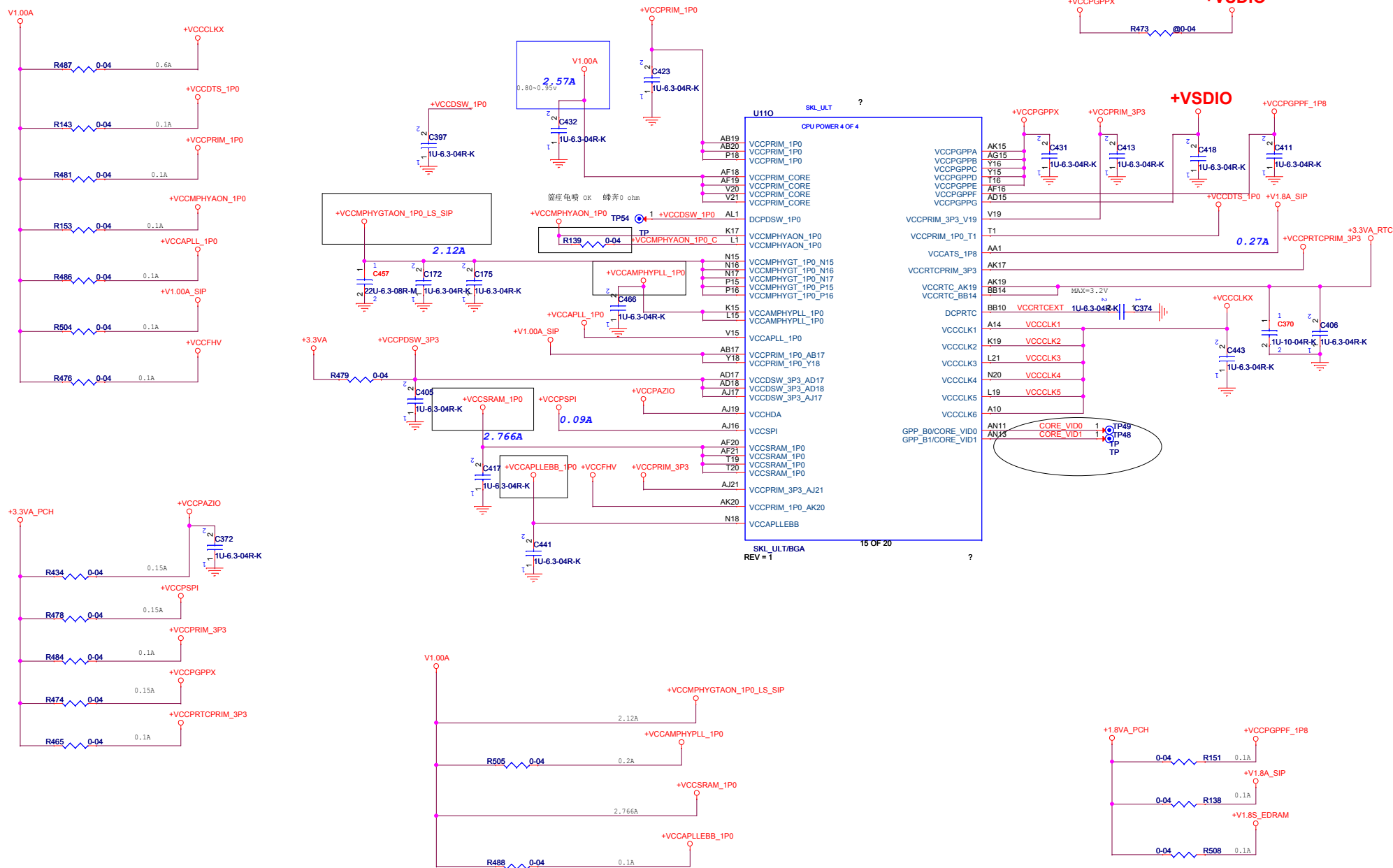
Data and clock signal for SMBus and SMIlink signal to each device needs to be length matched to 500 mills.

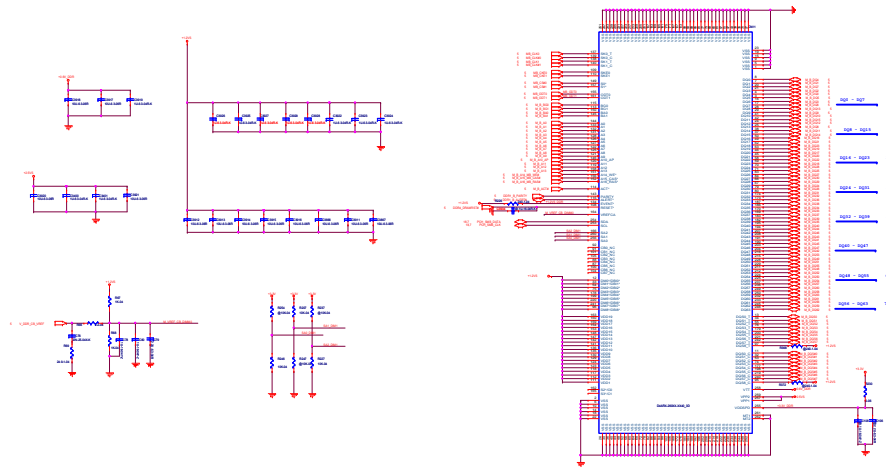
GPP_C2: 0 DIS 1 EN T15
GPP_C3: 0 LPC 1 eSP1



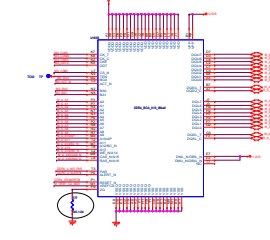
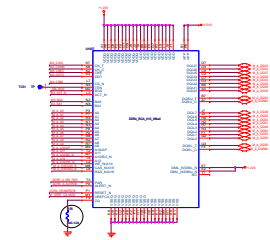
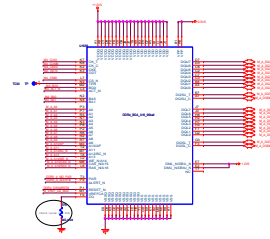
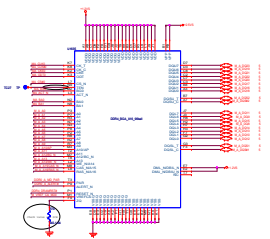
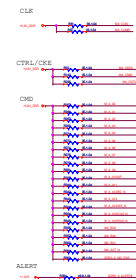
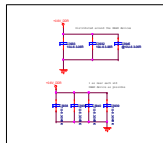
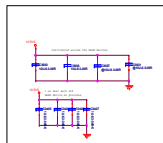
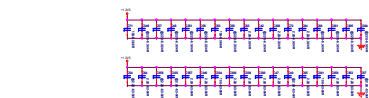
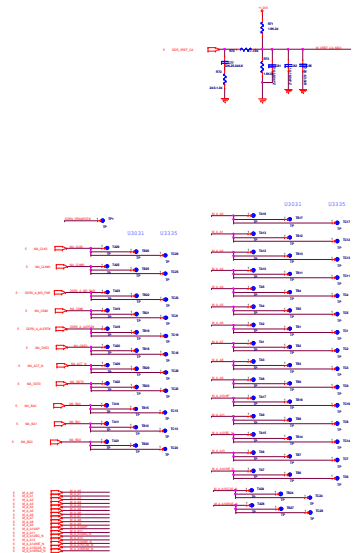




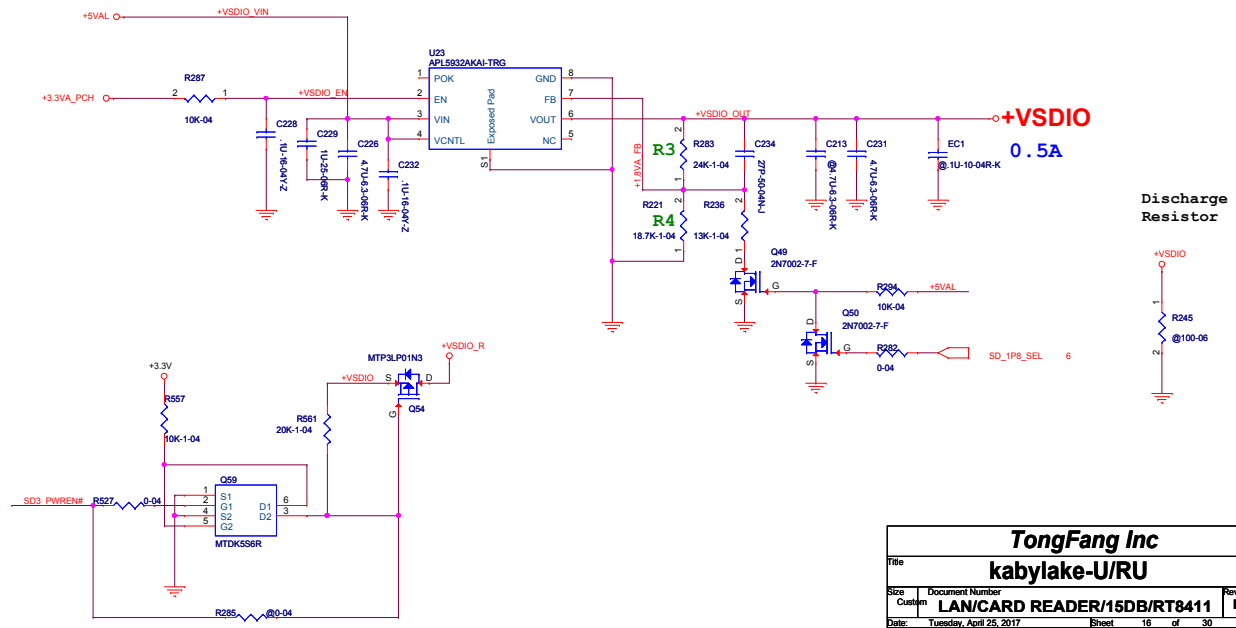
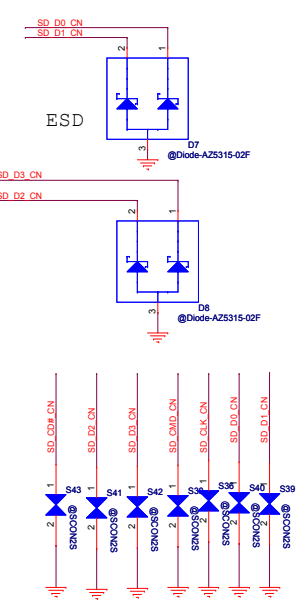
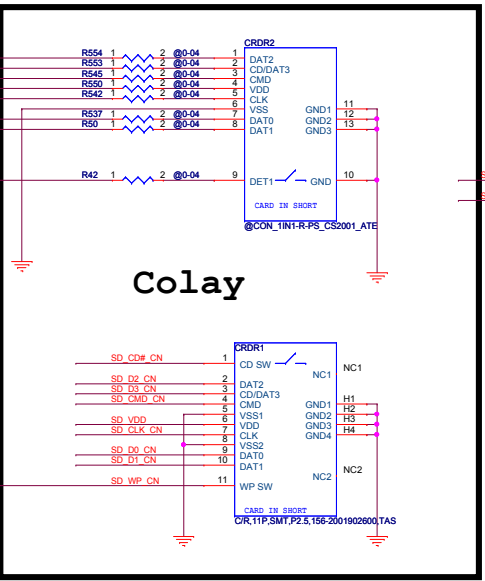
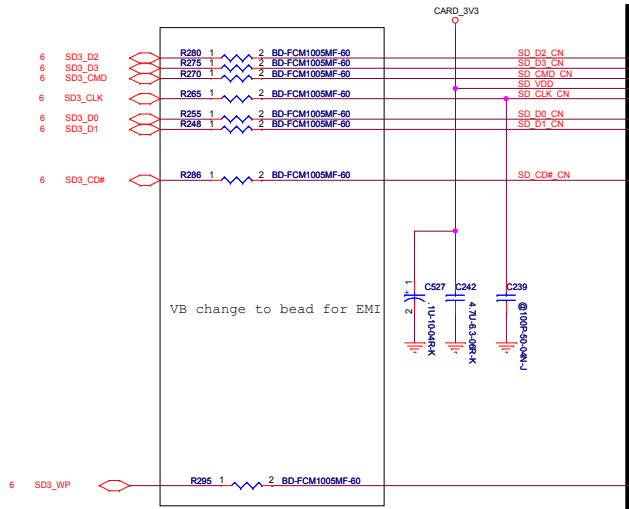
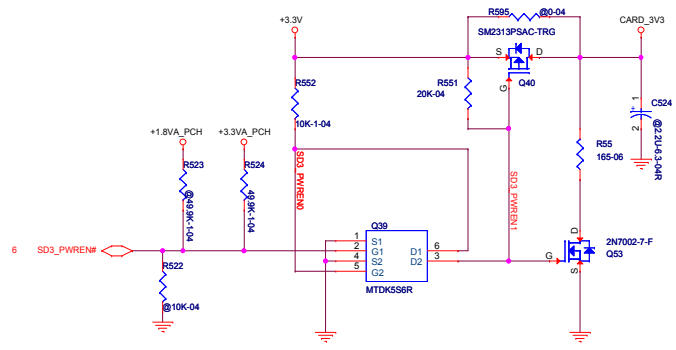




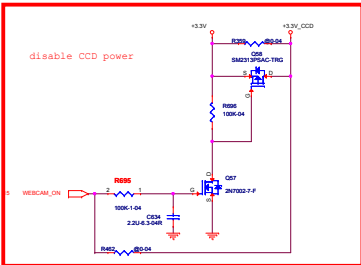
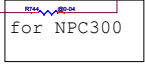
DDR4 Memory Down Double-T



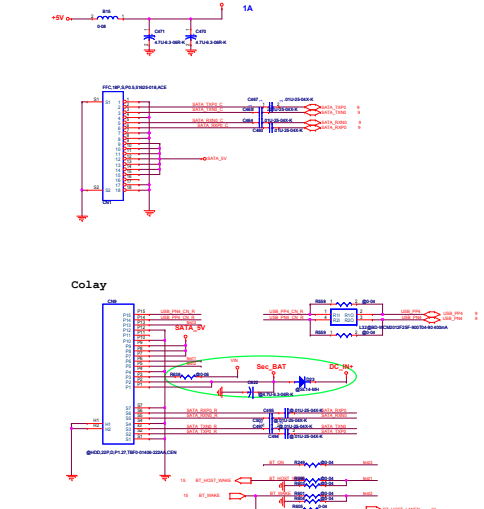
SD POWER



The diagram shows a Wheatstone bridge circuit. It consists of four resistors: R01 (50K-04) at the top left, R02 (10K-04) at the bottom left, R03 (10K-04) at the top right, and R04 (10K-04) at the bottom right. The bridge is powered by a +3.3V supply at the top and ground at the bottom. The output nodes are ACR1 (between R02 and R04) and ACR2 (between R01 and R03).

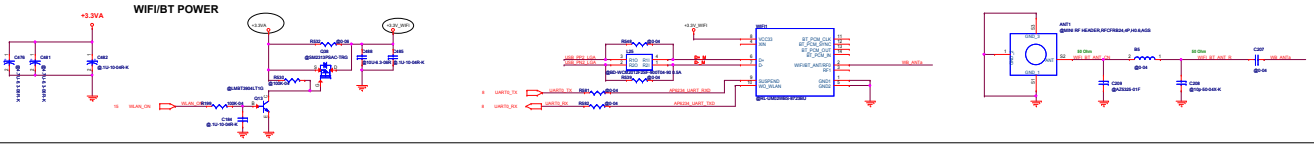


SATA-HDD



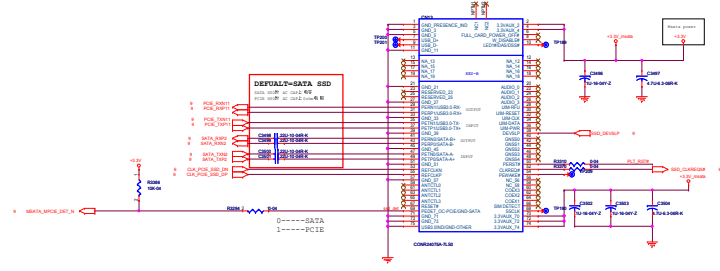
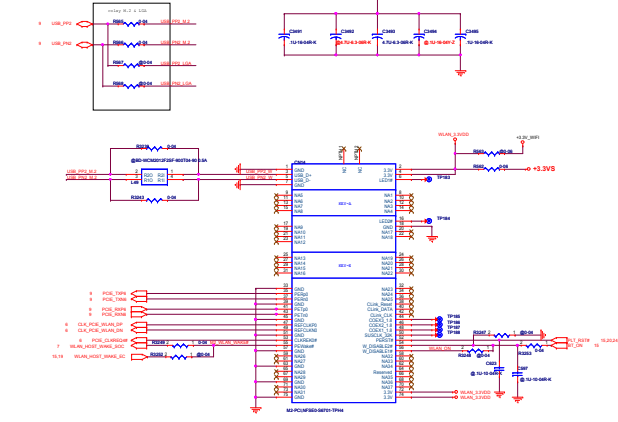
EMMC

WiFi & BT Combo



M.2_SSD

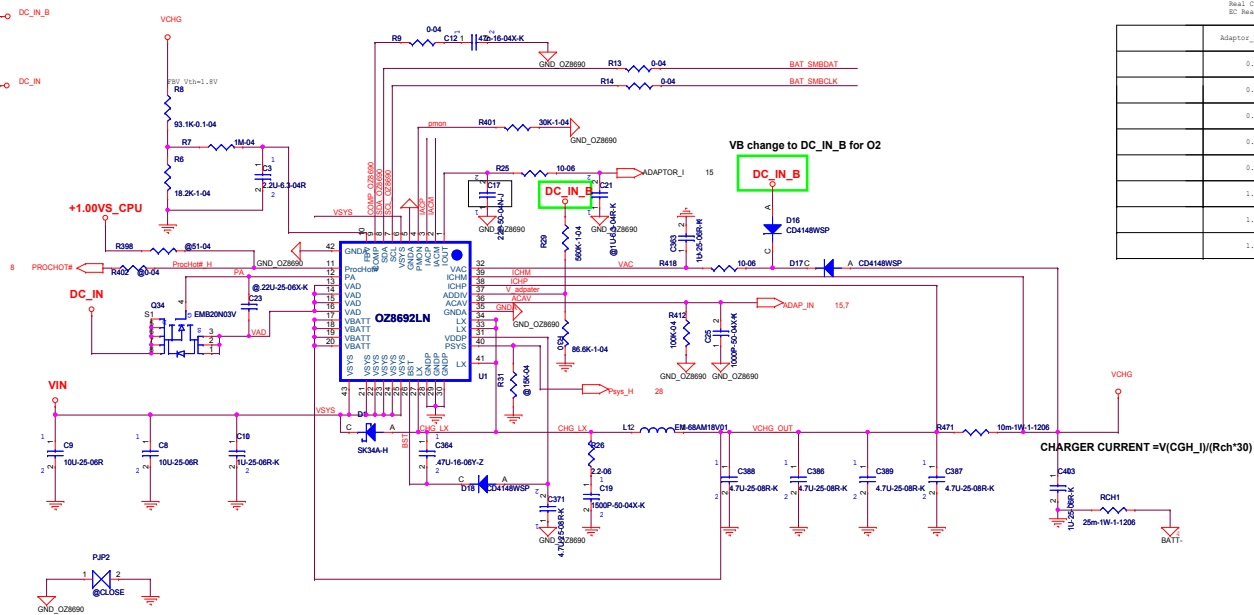
M.2_WLAN



IACP	DC_IN_B
1	4.706
2	4.706
3	4.706
4	4.706
5	4.706
6	4.706
7	4.706
8	4.706
9	4.706
10	4.706
11	4.706
12	4.706
13	4.706
14	4.706
15	4.706
16	4.706
17	4.706
18	4.706
19	4.706
20	4.706
21	4.706
22	4.706
23	4.706
24	4.706
25	4.706
26	4.706
27	4.706
28	4.706
29	4.706
30	4.706
31	4.706
32	4.706
33	4.706
34	4.706
35	4.706
36	4.706
37	4.706
38	4.706
39	4.706
40	4.706
41	4.706
42	4.706
43	4.706
44	4.706
45	4.706
46	4.706
47	4.706
48	4.706
49	4.706
50	4.706
51	4.706
52	4.706
53	4.706
54	4.706
55	4.706
56	4.706
57	4.706
58	4.706
59	4.706
60	4.706
61	4.706
62	4.706
63	4.706
64	4.706
65	4.706
66	4.706
67	4.706
68	4.706
69	4.706
70	4.706
71	4.706
72	4.706
73	4.706
74	4.706
75	4.706
76	4.706
77	4.706
78	4.706
79	4.706
80	4.706
81	4.706
82	4.706
83	4.706
84	4.706
85	4.706
86	4.706
87	4.706
88	4.706
89	4.706
90	4.706
91	4.706
92	4.706
93	4.706
94	4.706
95	4.706
96	4.706
97	4.706
98	4.706
99	4.706
100	4.706

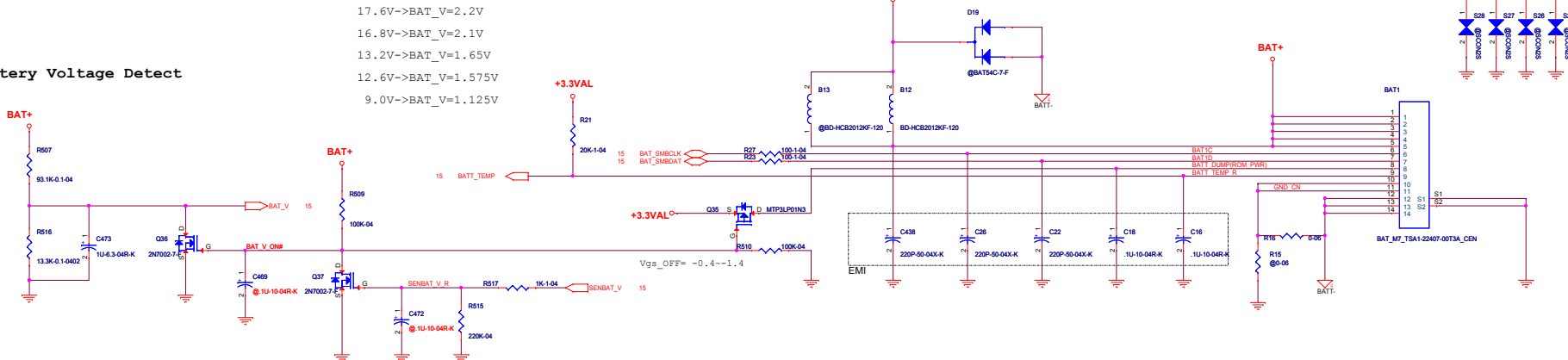
$$\text{Voltage} = 1.674 + 0.1116 \cdot \text{Bat_I}$$

Ideal Voltage	Measured Voltage	Current
0		-6
0.279		-5
0.558		-4
0.837		-3
1.116		-2
1.395		-1
1.674	1.667	0
1.953	1.944	1
2.232	2.224	2
2.511	2.504	3
2.79	2.782	4
3.069	3.062	5
3.348	3.342	6



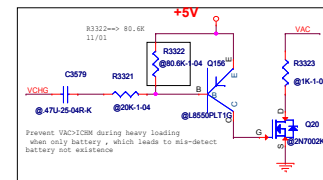
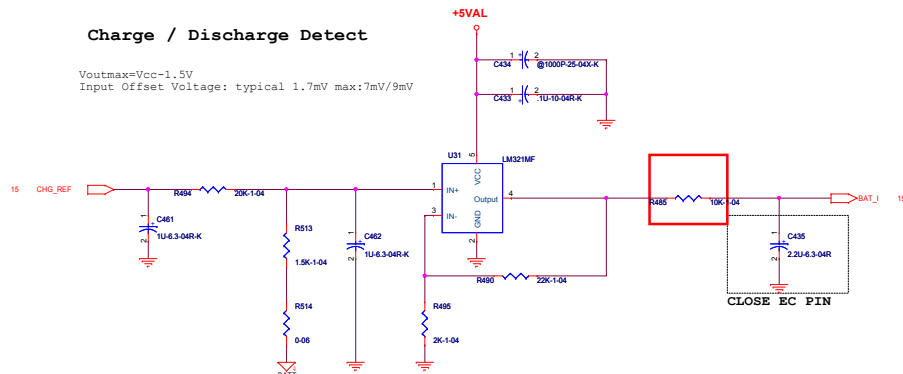
Adaptor_I_DC_Read(V)	Real Current(A)
0.191	0.90
0.386	1.0
0.589	1.5
0.788	2.0
0.985	2.5
1.189	3.0
1.387	3.5
1.585	4.0

Battery Voltage Detect

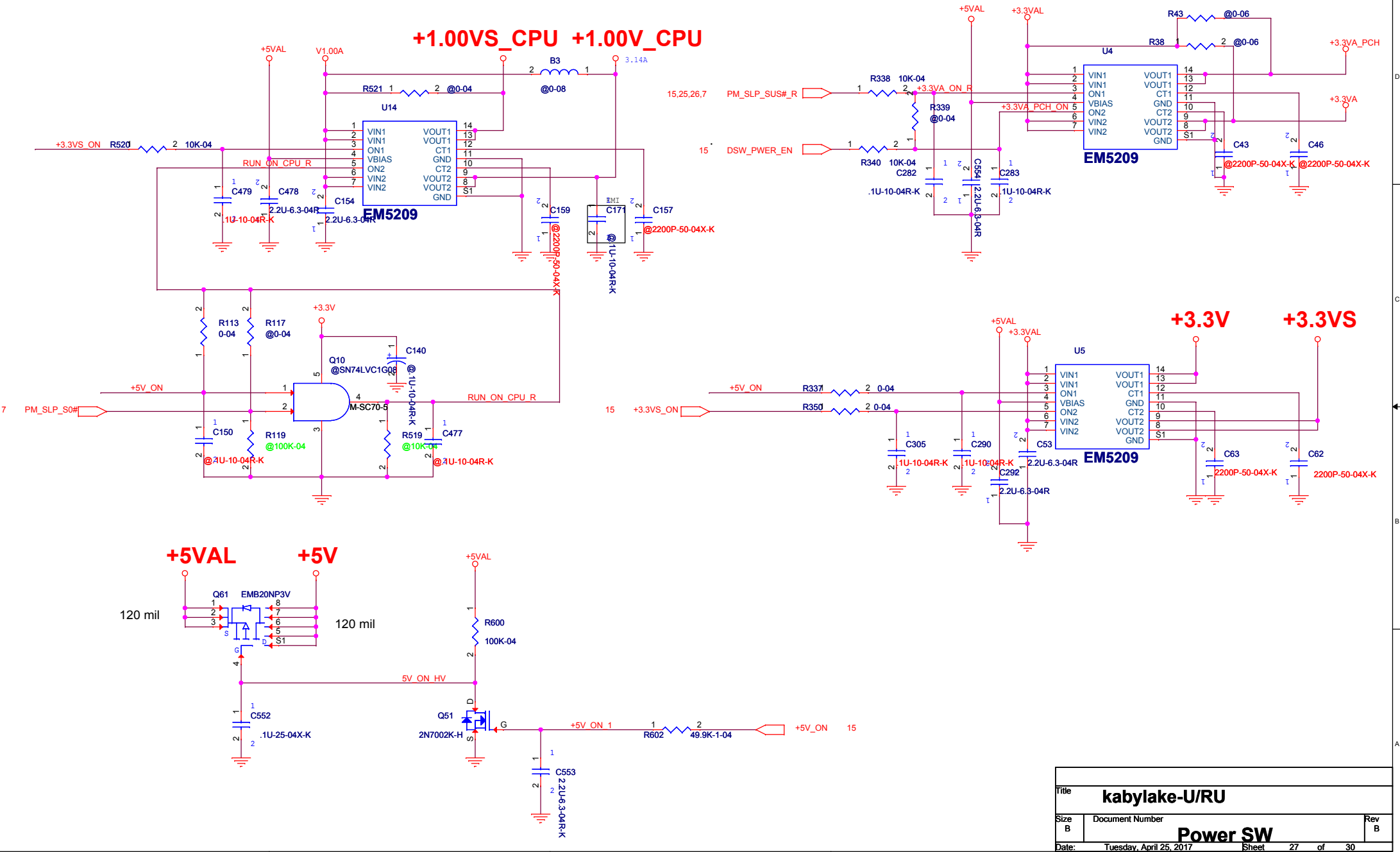


Charge / Discharge Detect

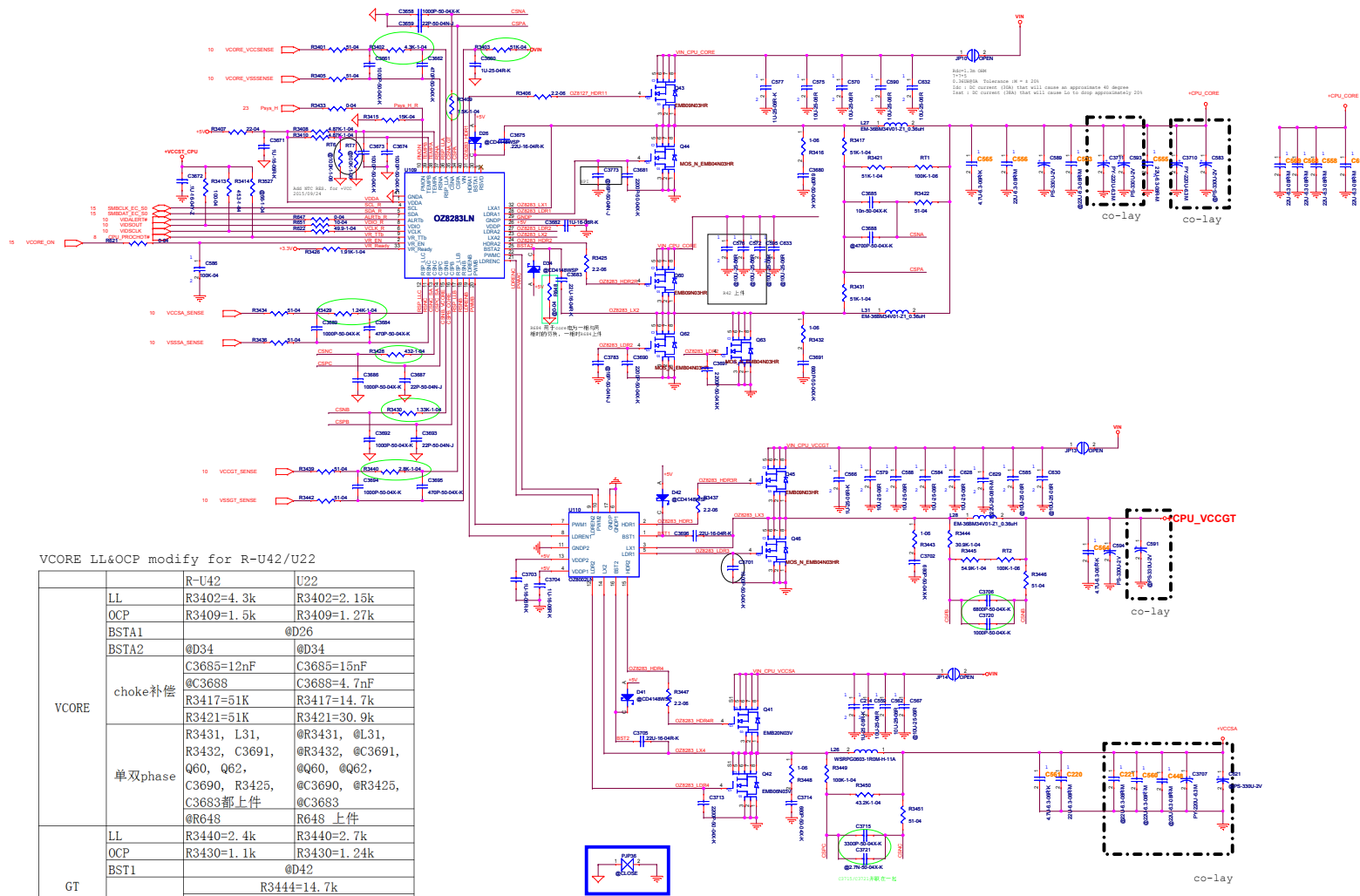
Voutmax=Vcc-1.5V
Input Offset Voltage: typical 1.7mV max:7mV/9mV



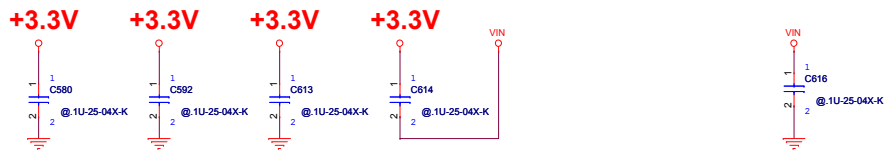
Power switch



Title			kabylake-U/RU
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B		B	
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HIGH SPEED CAP



Title		
kabyake-U/RU		
Size	Document Number	Rev
Customer	EMI_H_CAP	B
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