Compal Confidential

N3V3 Intel Gemini Lake Schematic

COMPAL CONFIDENTIAL
MODEL NAME : EDI55
PCB NO : DA60021O010
BOM P/N : 431ADZ31L01

2018/11/08

Rev 1.0(A00)

ZZZ
DAZ R1
PCB
Part Number = DAZ2ED00100
PCB EDI55 LA-G094P LS-F112P/F114P 02
PCB_DAZ_R1@

ZZZ
DAZ R3
PCB
Part Number = DAZ2ED00101
PCB EDI55 LA-G094P LS-F112P 02 GOLD A31!
PCB_DAZ_R3@

ZZZ
PCB R1
PCB
Part Number = DA60021O010
PCB 2ED LA-G094P REV1 M/B 3
PCB_R1@

ZZZ
PCB R3
PCB
Part Number = DA60021O011
PCB 2ED LA-G094P REV1 M/B GOLD 3 A31 !
PCB_R3@

CPU R1

UC1 SR3RZ_R1@
FH8068003067406 SR3RZ
Part Number = SA0000BEH2L
S IC FH8068003067406 SR3RZ B0 1.1G FCBGA

UC1 SR3S0_R1@
FH8068003067408 SR3S0
Part Number = SA0000BDQ1L
S IC FH8068003067408 SR3S0 B0 1.1G FCBGA

UC1 SR3S1_R1@
FH8068003067417 SR3S1
Part Number = SA0000BEJ0L
S IC FH8068003067417 SR3S1 B0 1.1G

CPU R3

UC1 SR3RZ_R3@
FH8068003067406 SR3RZ
Part Number = SA0000BEH3L
S IC FH8068003067406 SR3RZ B0 1.1G A31!

UC1 SR3S0_R3@
FH8068003067408 SR3S0
Part Number = SA0000BDQ2L
S IC FH8068003067408 SR3S0 B0 1.1G A31!

UC1 SR3S1_R3@
FH8068003067417 SR3S1
Part Number = SA0000BEJ1L
S IC FH8068003067417 SR3S1 B0 1.1G A31!

@ : Un-pop Component
EC@ : EC
EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
ESPI@:ESPI
LPC@:LPC
PCB@:PCB
Lan@: lan component
lan@EMI@:EMI for lan pop component
1000@:Giga
CNVI@: CNVI interface
XDP@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
MMC@ : eMMC / NMMC@: without eMMC
FFS@ : Free Fall Sensor
45@:HDMI logo
N3@/V3@:N3000/V3000

SR3RZ_R3@/SR3S0_R3@/SR3S1_R3 : Pentium/Celeron QC/Celeron DC
S32G_R3@/S64G_R3@/H32G_R3@/H64G_R3@ : eMMC Type

Layout Dell logo

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.
Title: Cover Sheet
Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0
Date: Thursday, November 08, 2018 | Sheet 1 of 39

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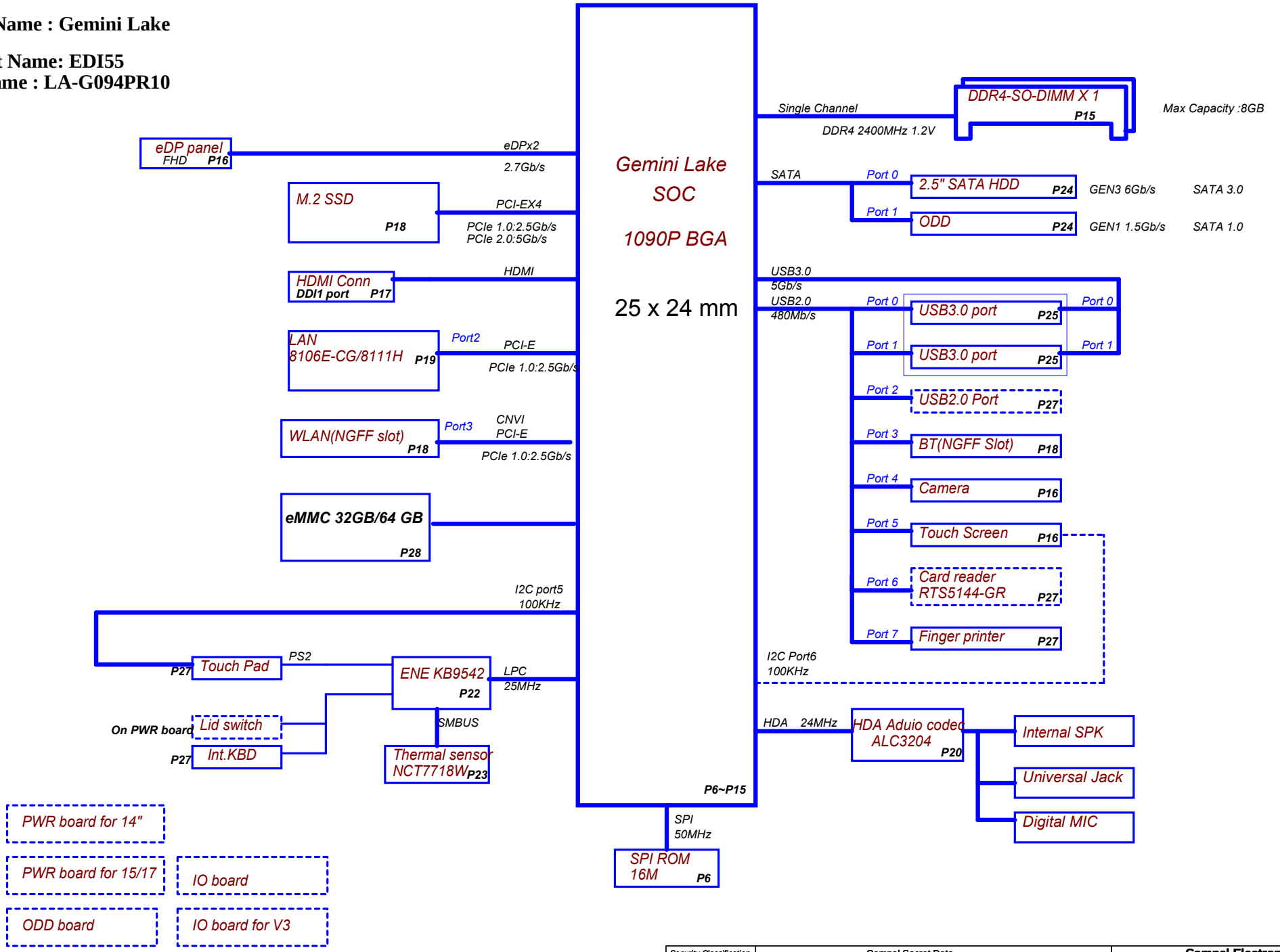
Model Name : Gemini Lake

Project Name: EDI55
File Name : LA-G094PR10



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/09/27	Deciphered Date 2018/07/10	Title: Block Diagrams
			Size: Custom; Document Number: LA-G094PR10; Rev: 1.0
			Date: Thursday, November 08, 2018; Sheet 2 of 39

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.24VALW	+1.2 v Always power rail(SOC L2 , I/O Logic and PLLs)	ON	ON	ON
+1.8V_PRIM	+1.8v Always power rail(SOC all GPIOs)	ON	ON	ON
+3VALW	+3.3v Always power rail(SOC GPIO , I/O Logic ,USB2 PHY)	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.2V	+1.2V power rail for DDR4	ON	ON	ON
+VCC_VCGI	CPU , GFX and ISP logic voltage for SOC	ON	ON	OFF
+VNN	non-Core Logic voltage for SOC	ON	OFF	OFF
+0.6V_DDR_VTT	+0.6V power rail for DDR4 Terminator	ON	OFF	OFF
+1.05VS	+1.05v system power rail(SDRAM and I/O Logic)	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BOM Option Table

BTO Item	BOM Structure
Unpop	@/@RF@
Connector	CONN@
XDP (Debug Port)	XDP@
EMI requirement	EMI@
EMI requirement unpop	@EMI@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Board ID	EC@
N3000/V3000	N3@/V3@
CNVI	CNVI@
Free fall sensor	FFS@
lan 10/100	100@
lan giga	1000@
lan compoent	Lan@
lan EMI compoent	Lan@EMI@
ESPI for EC	ESPI@
LPC for EC	LPC@
TP_WAKE	TP_WAKE/NTP_WAKE
eMMC	MMC@

Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	GLK EVT
1	GLK DVT1
2	GLK DVT2
3	GLK pilot
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

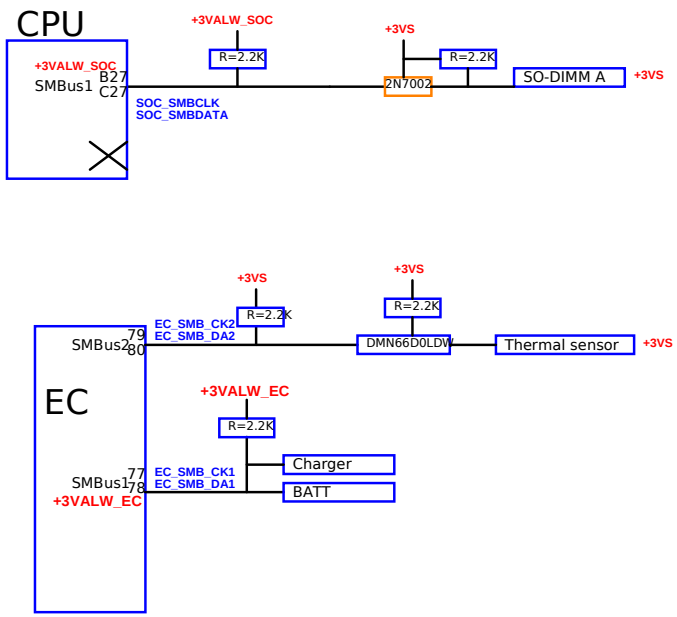
EC SM Bus2 address

Device	Address

SOC SM Bus address

Device		Address
ChannelA	JDIMM1	0xA0(1010 0000).

<SMBus Routing>



HSIO Port Table

GLK BASE I/O SKU			N3V3
USB XHCI Port 0			USB3.0 Port 0
USB XHCI Port 1			USB3.0 Port 1
PCIe-0	X 2	X 4	SSD
PCIe-1			SSD
PCIe-2	X 2		SSD
PCIe-3 / USB XHCI Port 4			SSD
PCIe-4 / USB XHCI Port 3	X 2		WLAN
PCIe-5 / USB XHCI Port 2			LAN
SATA 0	X 2		HDD
SATA 1 / USB XHCI Port 5			ODD
USB Port 0			USB3.0 Port 0
USB Port 1			USB3.0 Port 1
USB Port 2			USB2.0 IO/B
USB Port 3			BT
USB Port 4			Camera
USB Port 5			Touch Screen
USB Port 6			Card Reader
USB Port 7			Fingerprint
VIDEO	eDP		LCD
	DDI0		
	DDI1		HDMI

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Title: Notes List

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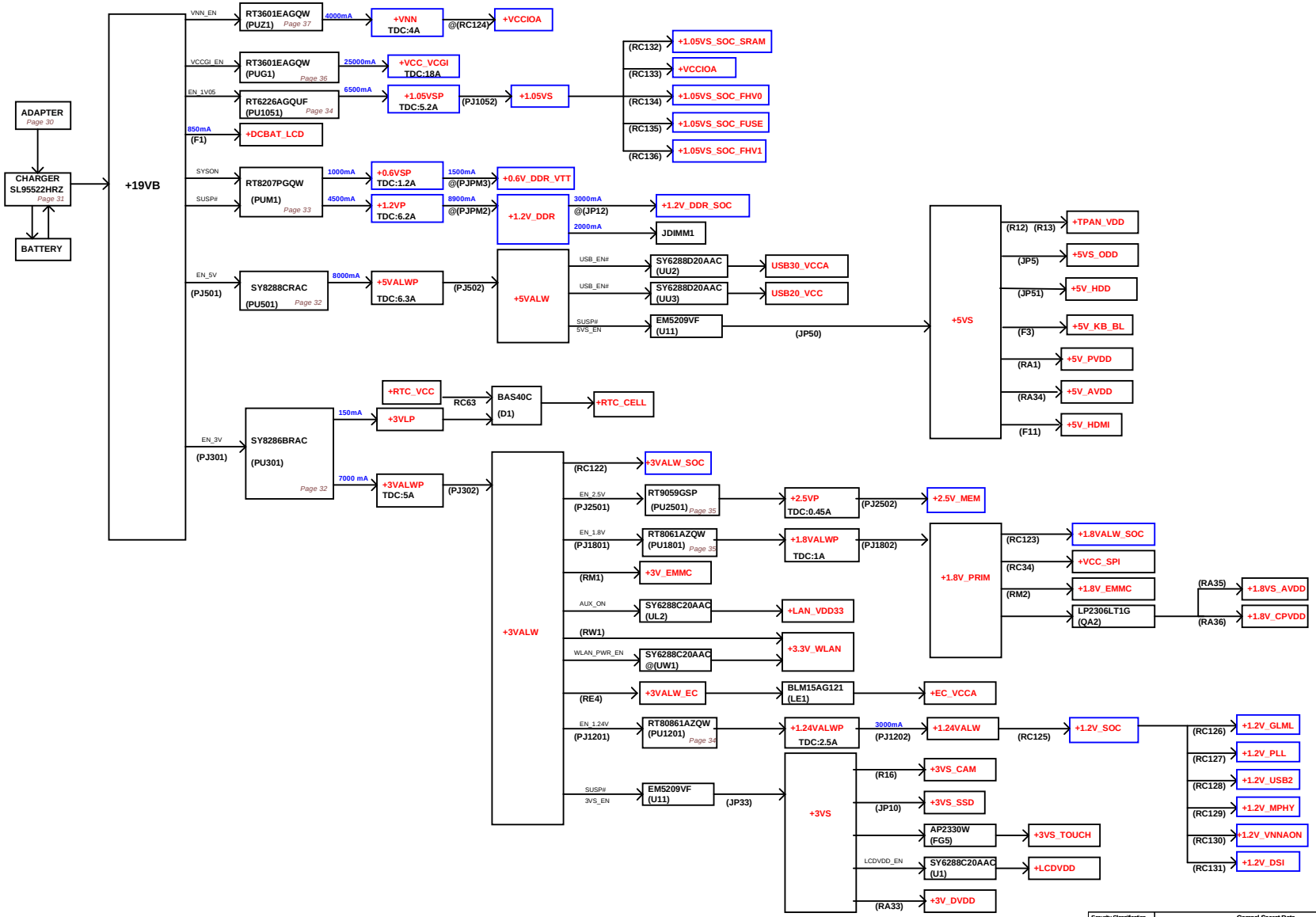
MODEL NAME: *Power Rail Block Diagram*
PCB NAME:
REVISION:
DATE: *2018/01/22*



Security Classification	Compal Secret Data		
Issued Date	2014/13/10	Deciphered Date	2018/01/15

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Title: **P04-Power Rail**

Size | Document Number | Rev 1.0

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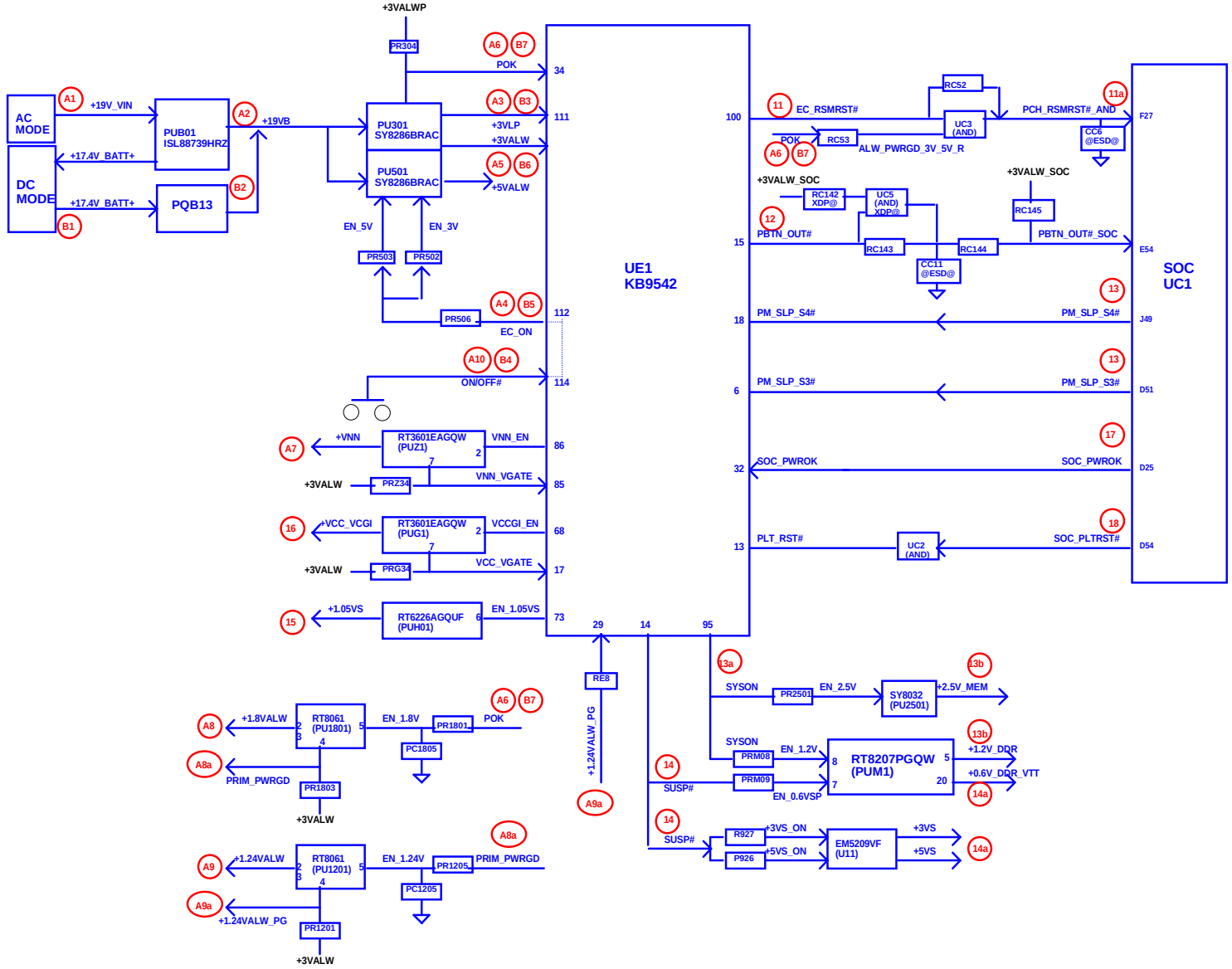
MODEL NAME: *Power Sequence Block Diagram*
PCB NAME:
REVISION: *0.2*
DATE: *2018/01/29*



Security Classification	Compal Secret Data		
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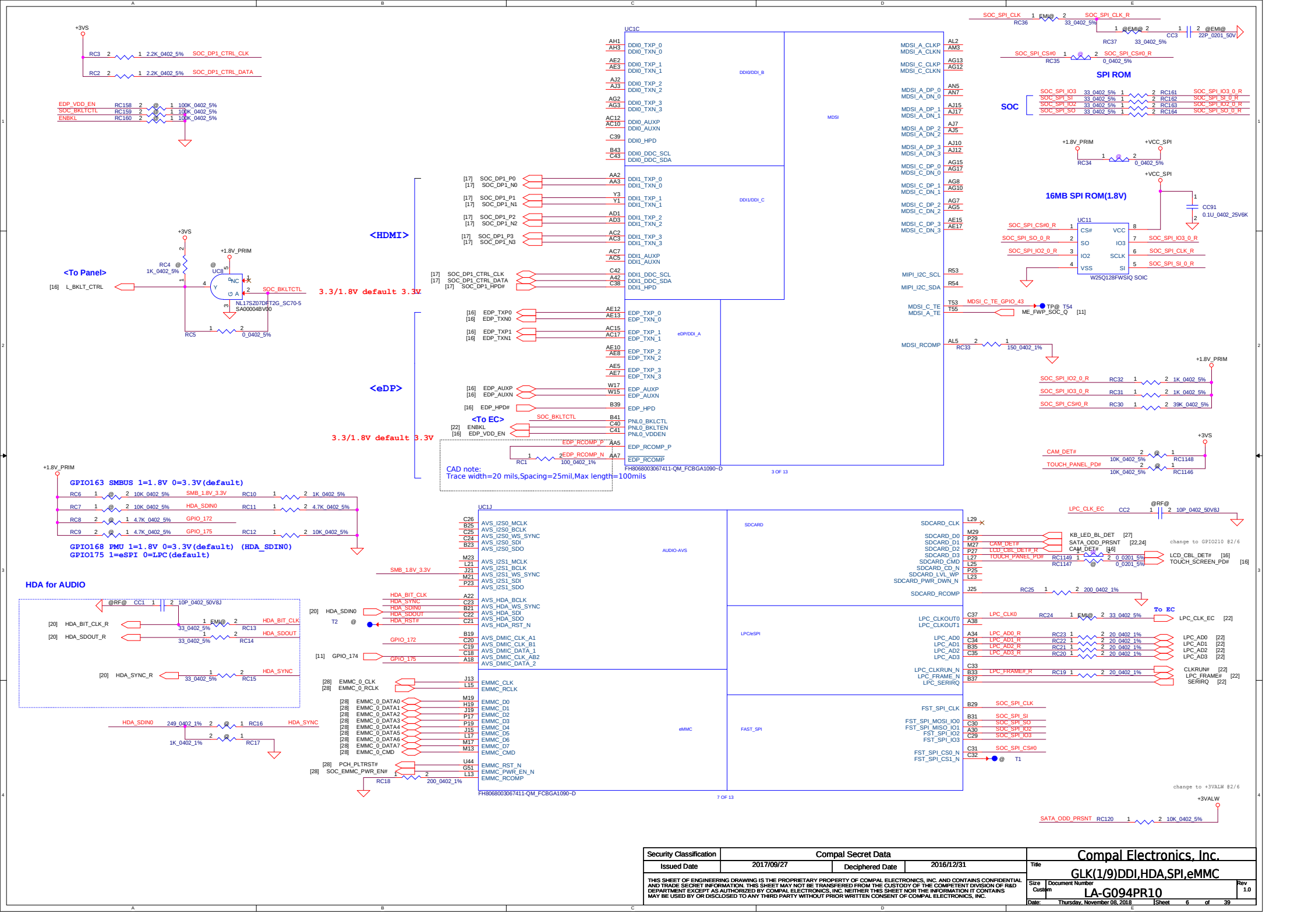
Compal Electronics, Inc.			
Title: P05-Power Sequence Block Diagram			
Size: Custom	Document Number: LA-G094PR10		Rev: 1.0
Date: Thursday, November 08, 2018	Sheet 5 of 39		



Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

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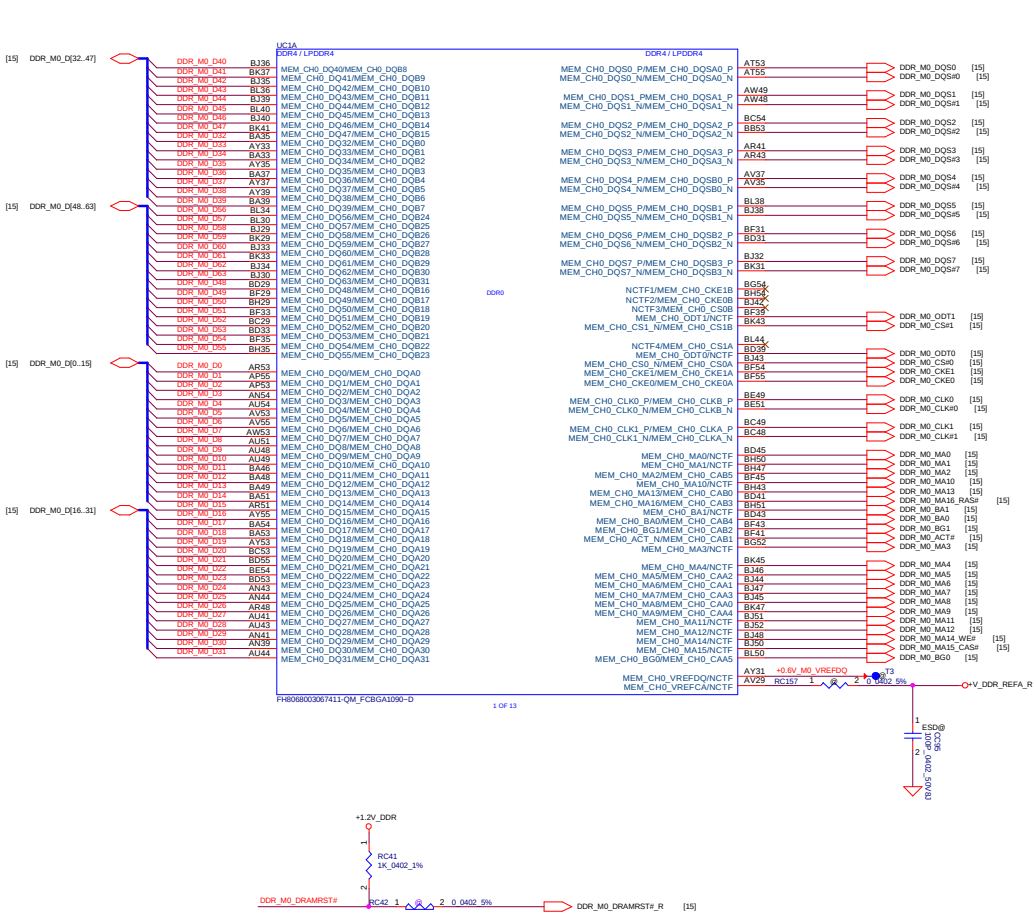
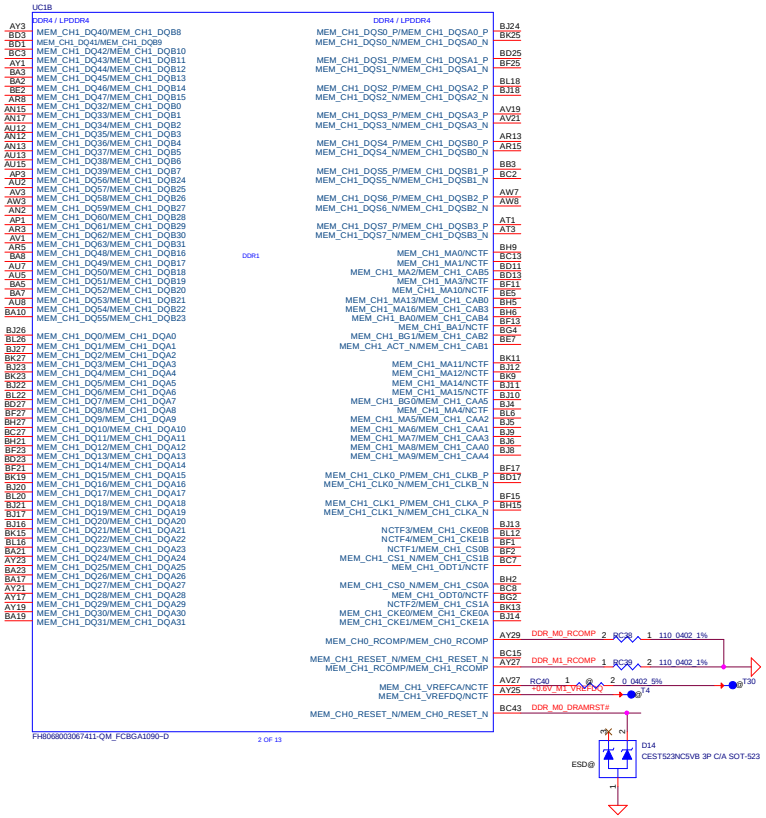
Title: GLK(1/9)DDI,HDA,SPI,eMMC

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

Date: Thursday, November 08, 2018 Sheet 6 of 39





Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: GLK(2/9)Memory

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

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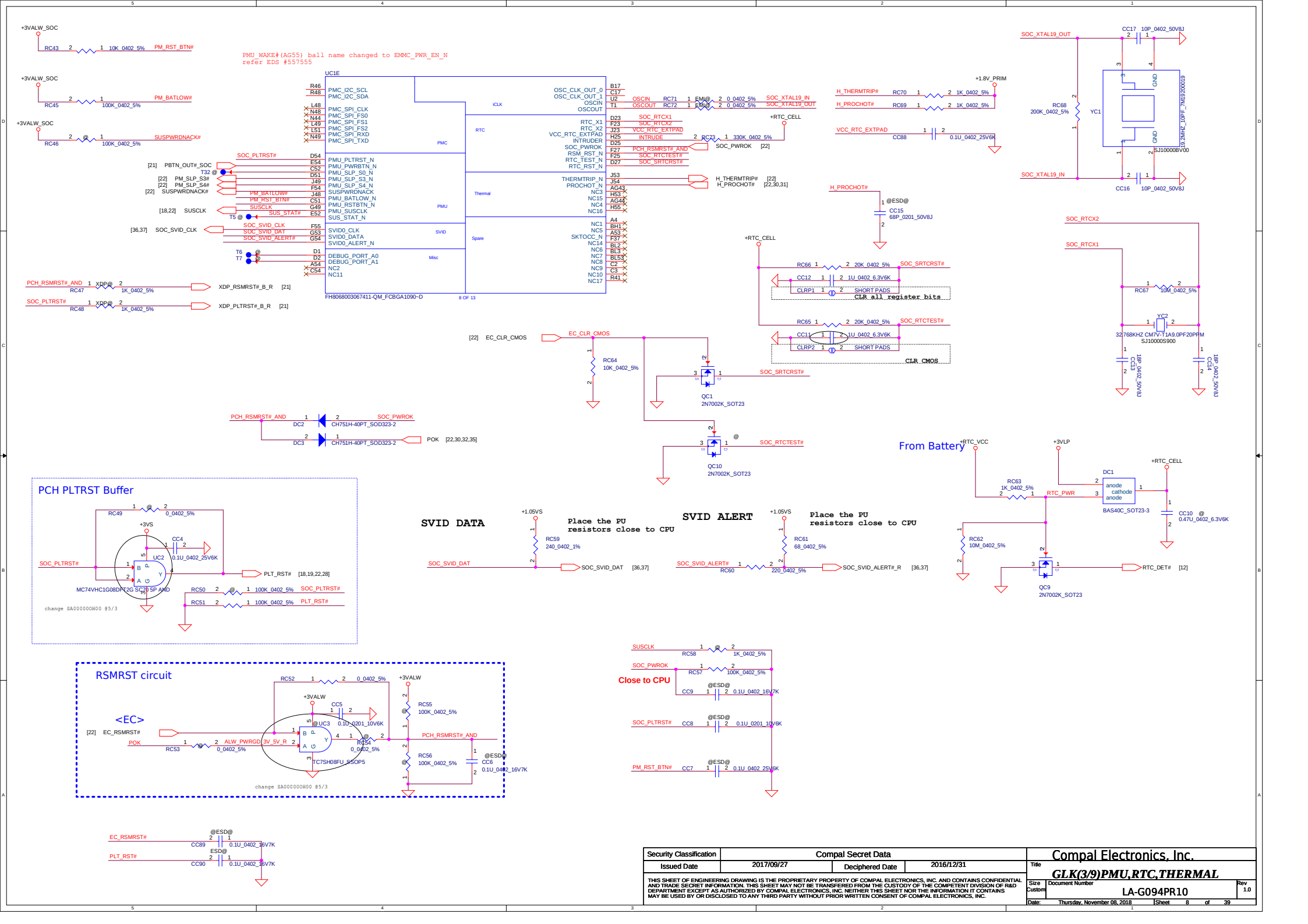
PMU_WAKE#(AG55) ball name changed to EMMC_PWR_EN_N
refer EDS #5557555
UC1E
FH8068003067411-QM_FCBGA1090-D
8 OF 13
PMC
PMU
SVID
Misc
RTC
Thermal
Spare
iCLK
PCH PLTRST Buffer
change SA000000H00 85/3
SVID DATA
Place the PU resistors close to CPU
SVID ALERT
Place the PU resistors close to CPU
From Battery
RSMRST circuit
<EC>
Close to CPU
Security Classification
Compal Secret Data
Issued Date
2017/09/27
Deciphered Date
2016/12/31
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Compal Electronics, Inc.
Title
GLK(3/9)PMU,RTC,THERMAL
Size
Custom
Document Number
LA-G094PR10
Rev
1.0
Date:
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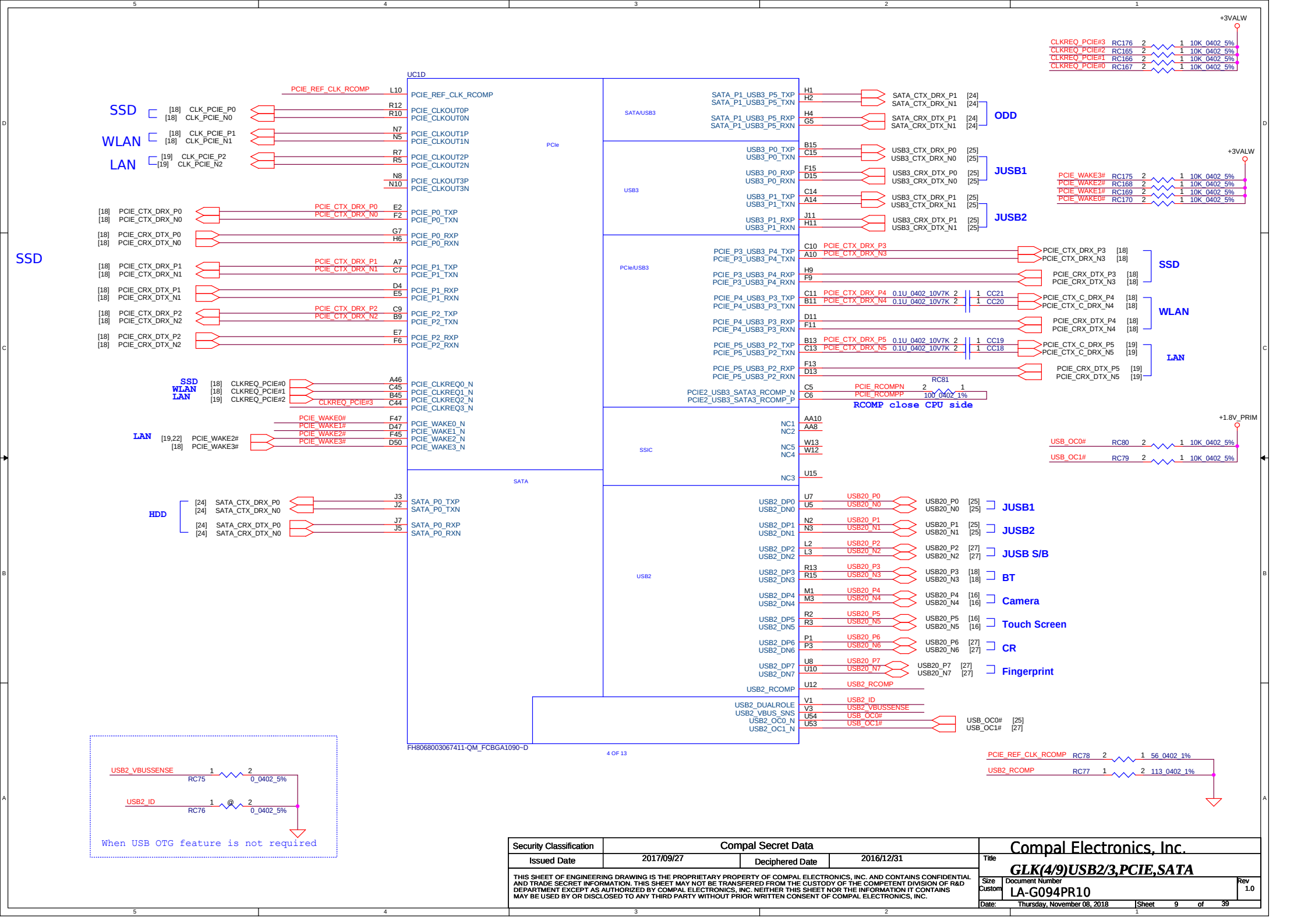

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: GLK(4/9)USB2/3,PCIE,SATA

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

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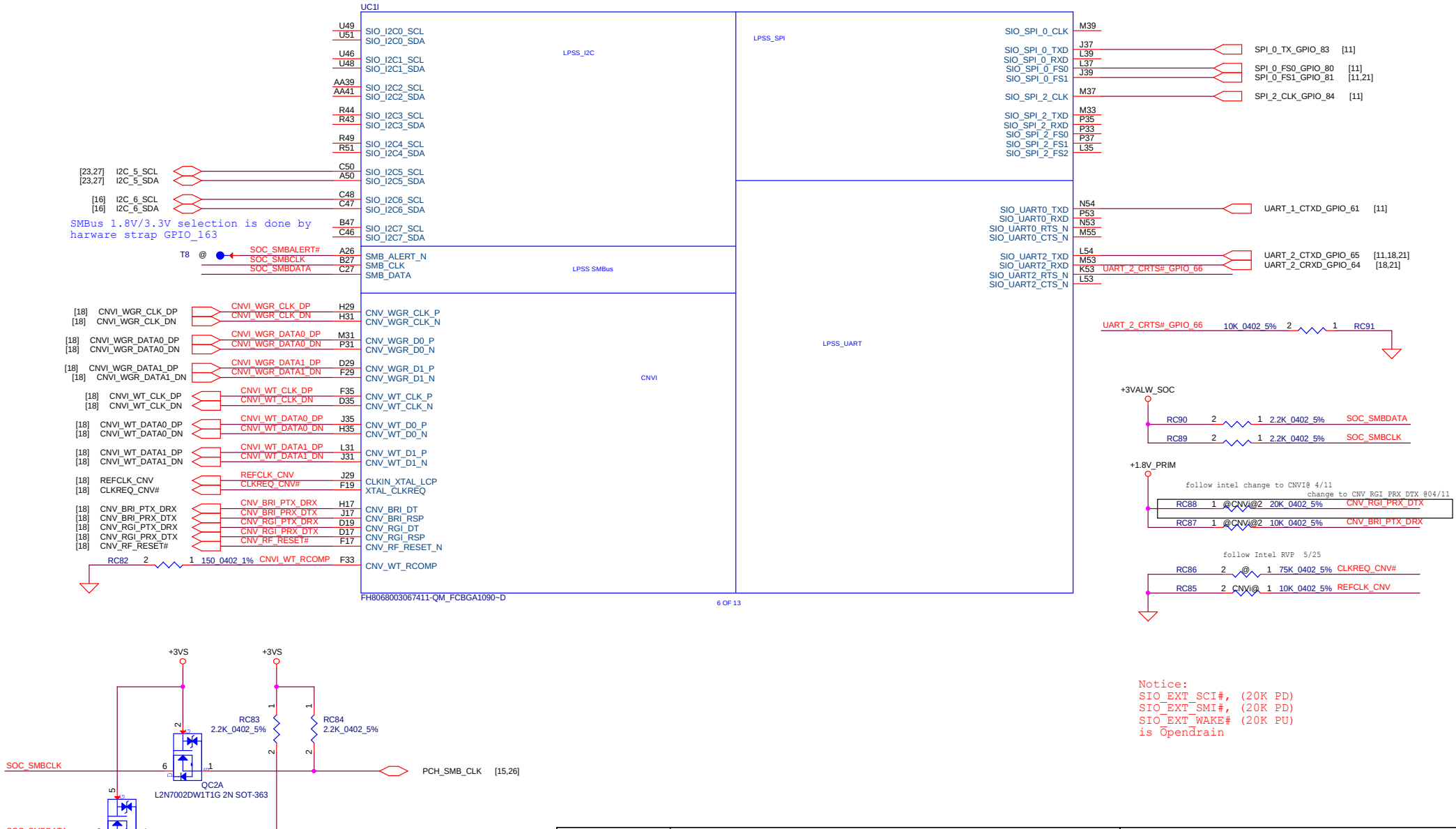

Notice:
SIO_EXT_SCI#, (20K PD)
SIO_EXT_SMI#, (20K PD)
SIO_EXT_WAKE# (20K PU)
is Opendrain

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Title: GLK(5/9)I2C,SMB,CNVi

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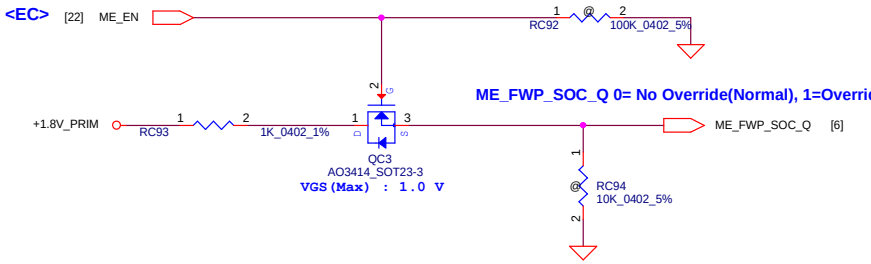
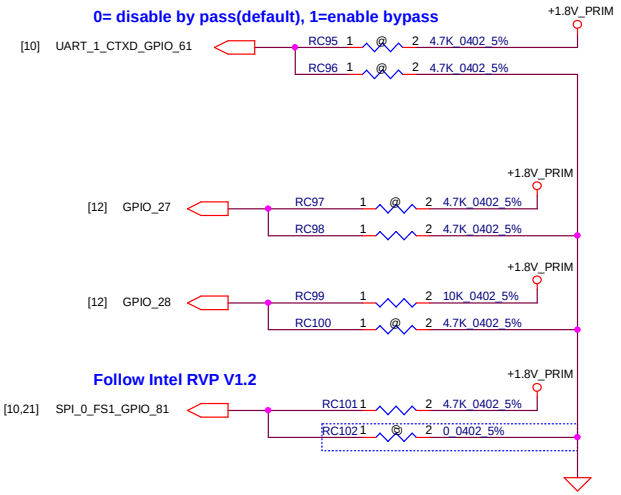
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_87	SIO_SPI_2_FS2	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_89	SIO_SPI_2_TXD	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_159	AVS_I2S0_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_163	AVS_I2S1_WS_SY NC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)

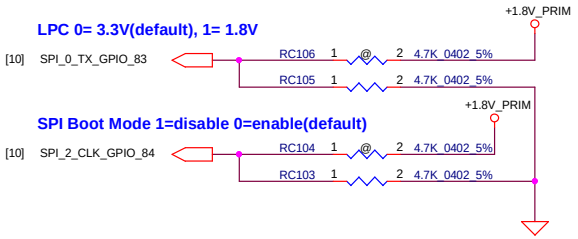
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable ***Note:*** If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_43	MDSI_C_TE	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	USB2_OC0_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.
GPIO_62	SIO_UART0_RTS_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

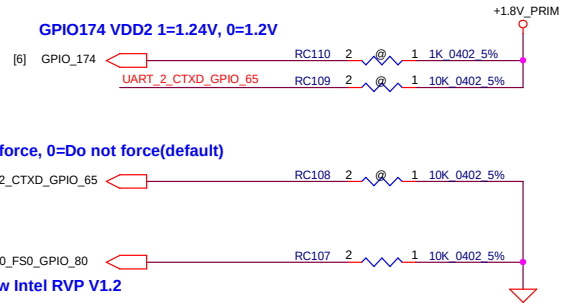
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Notes:*** 1. DnX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would download a new firmware image from a recovery host, over USB, and overwrite the image in the storage media.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) ***Note:*** The board should strap this low and do not use otherwise
GPIO_79	SIO_SPI_0_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_80	SIO_SPI_0_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_81	SIO_SPI_0_FS1	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_85	SIO_SPI_2_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.
GPIO_177	SMB_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_191	CNV_BRI_DT	eSPI Flash Sharing Mode	20K PD	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS; default) Note: if eSPI mode is disabled (eSPI/LPC hard strap(GPIO_175) is set to select LPC) then the eSPI slave attached flash sharing strap must also be set to 0.
GPIO_192	CNV_BRI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_193	CNV_RGI_DT	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_194	CNV_RGI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_195	CNV_RF_RESET_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_196	XTAL_CLKREQ	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.









Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

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Title: *GLK(6/9)GPIO strap*

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

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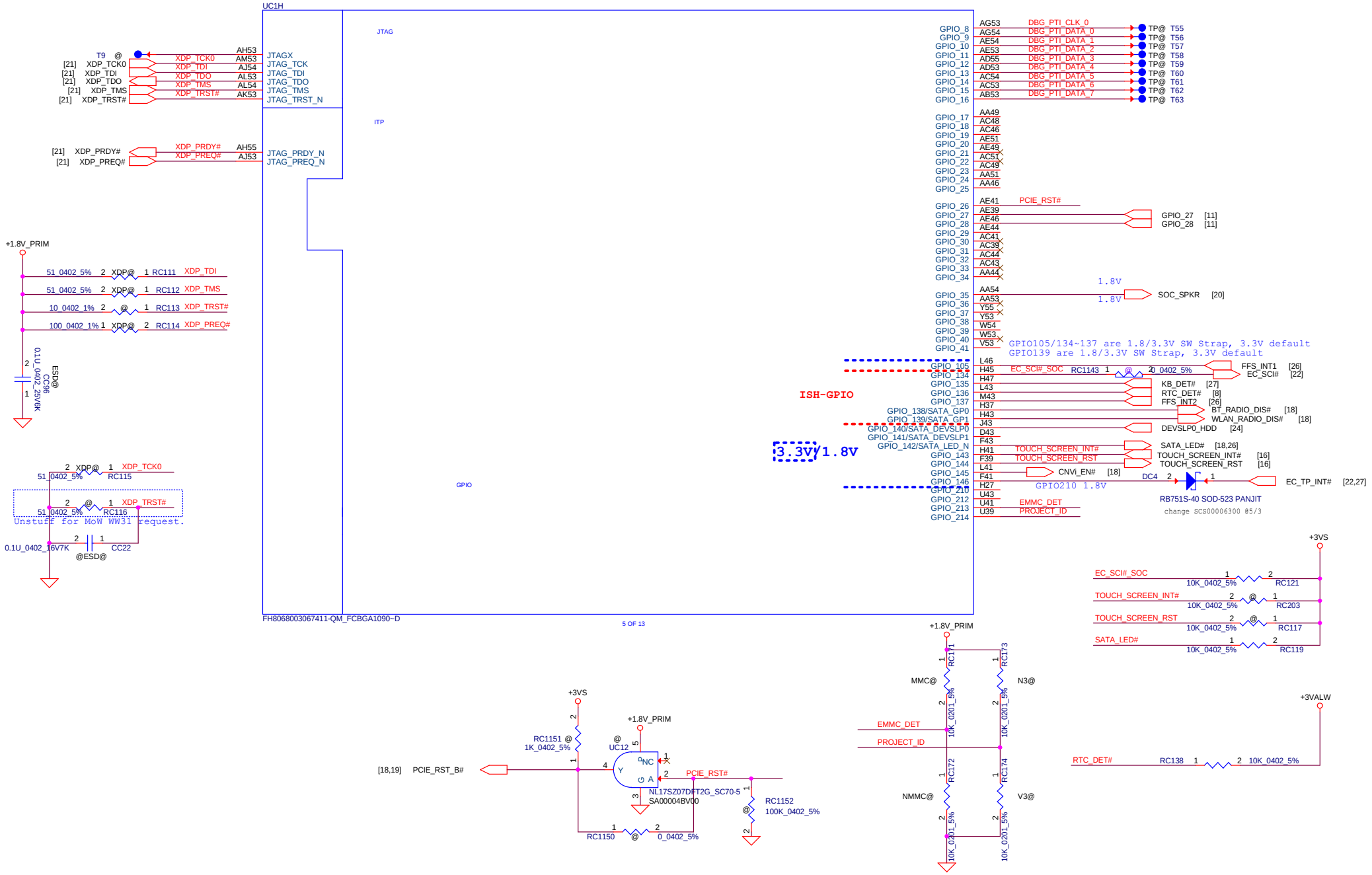

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: *GML(7/9)GPIO,JTAG*

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

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Variable voltage supply to CPU and Graphics Core and ISP logic. SVID and I2C VID are voltage control interface supported.

Max 25A

Max 4A

Variable voltage supply to other (non core) logic

Max 3A

Max 1.5A

Max 0.4A

Fixed voltage rail for all GPIOs

Max 2A

Fixed voltage rail for MPHY Logic

Fixed voltage rail for Audio and ISH I/O Logic

Fixed voltage rail for MIPI* I/Os

Fixed voltage rail for SoC L2

Fixed voltage rail for PLLs

Fixed voltage rail for USB2 I/O

+1.2VALW

Max 1.93A

Max 1.8A

A-Step only support +1.2V.

VCC_1P2V A1,A2 (AA18,AA20 pin) is only for MIPI-CSI or MIPI-DSI function.

Max 2.7A

Max 4.8A

Max 4.5A

Fixed voltage rail for SRAM and I/O Logic

Max 6uA

Fixed Voltage rail for RTC

Max 0.15A

Fixed voltage rail for GPIO, I/O logic, and USB2 PHY

Close Soc pin AK25,AJ25

Close Soc pin AM28

CC52 close to UC1

CC58 close to UC1

change back to 0402 @04/17

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Issued Date	2017/09/27	Deciphered Date	2016/12/31

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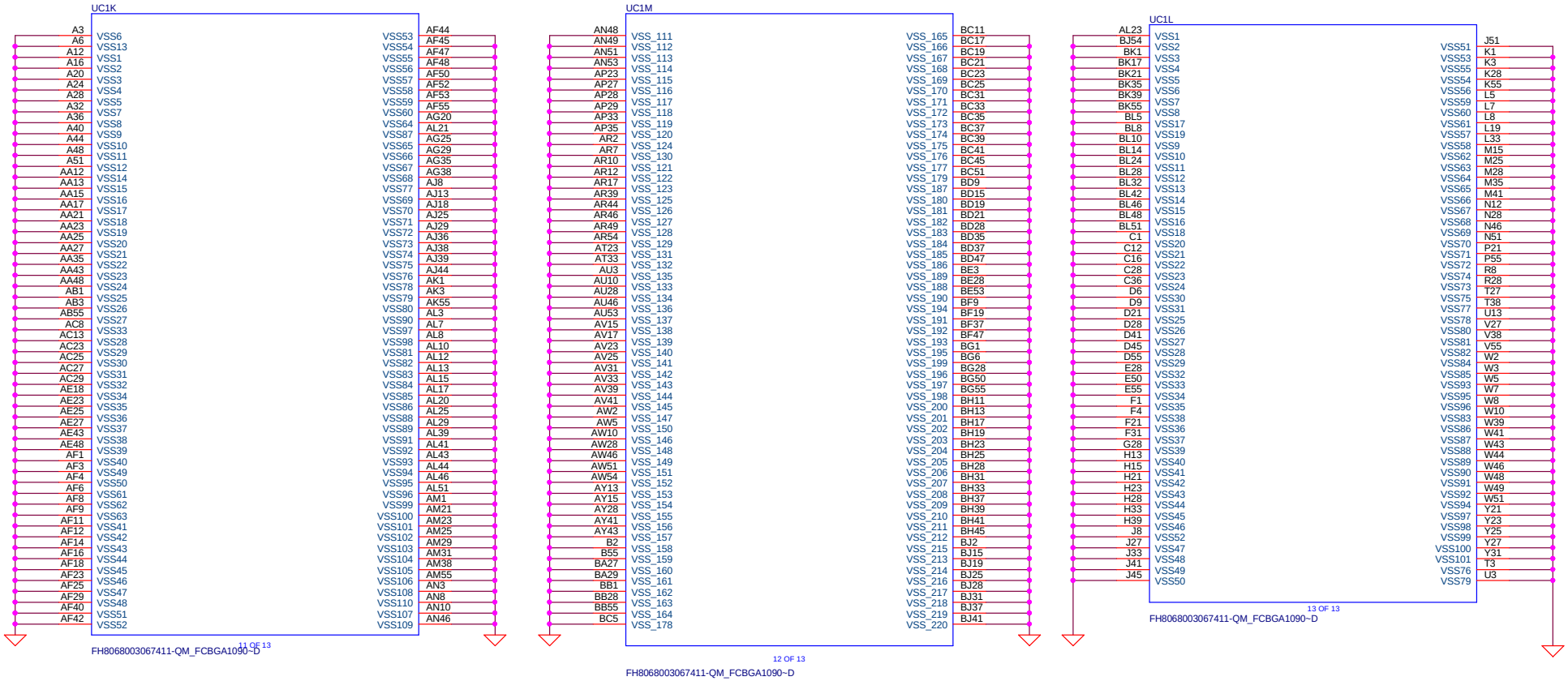
Compal Electronics, Inc.

Title: GLK(8/9)Power

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 13 of 39



Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: *GLK(9/9)GND*

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

Date: Thursday, November 08, 2018 Sheet 14 of 39

Main Func = DDR

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

add by esd require 1/17

All VREF traces should have 10 mil trace width

20mil

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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Compal Electronics, Inc.

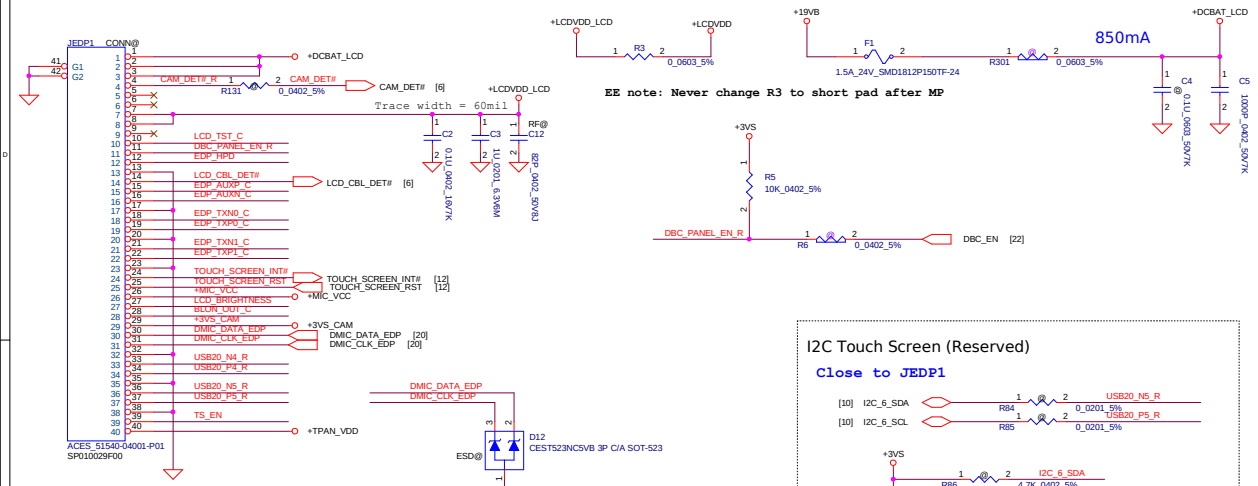
Title: DDR4 DIMMA_RVS

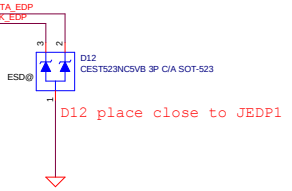
Size: Document Number: LA-G094PR10 Rev: 1.0

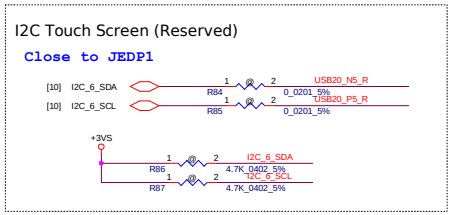
Date: Thursday, November 08, 2018 Sheet 15 of 39

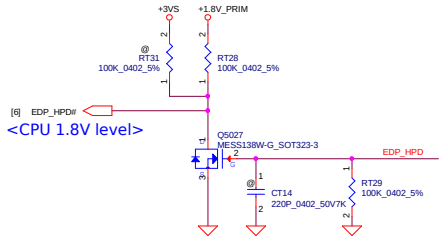
Main Func = LCD

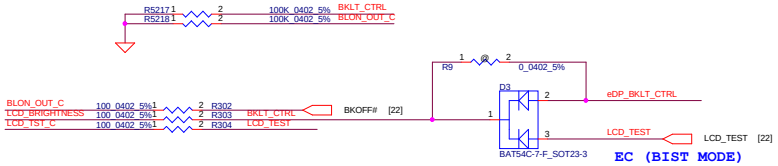
INVERTER POWER

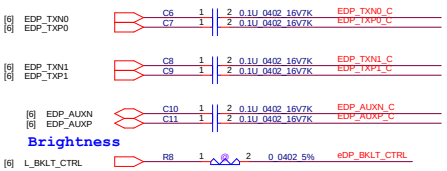


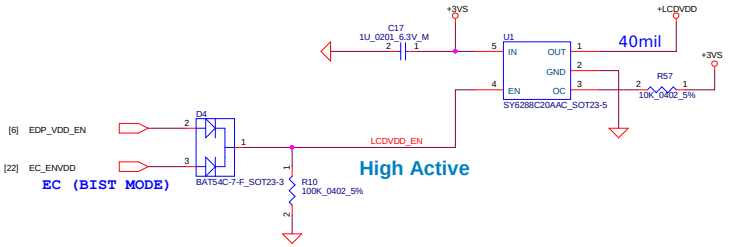


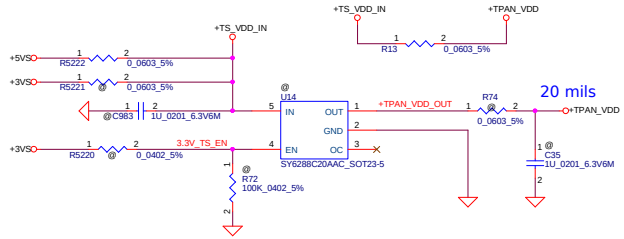




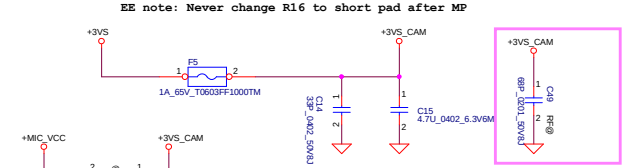


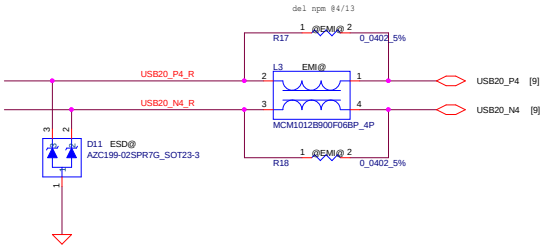






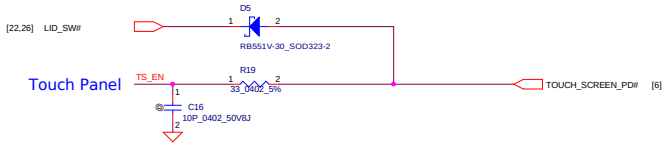
Main Func = CAM

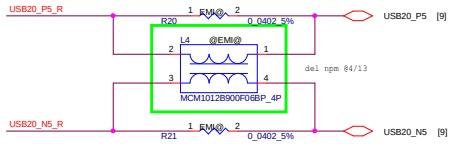


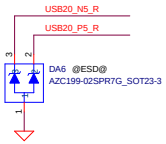


D11 place close to JEDP1

Main Func = TS







Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: LCD/Cam/MIC/T.Panel

Document Number: LA-G094PR10

Rev: 1.0

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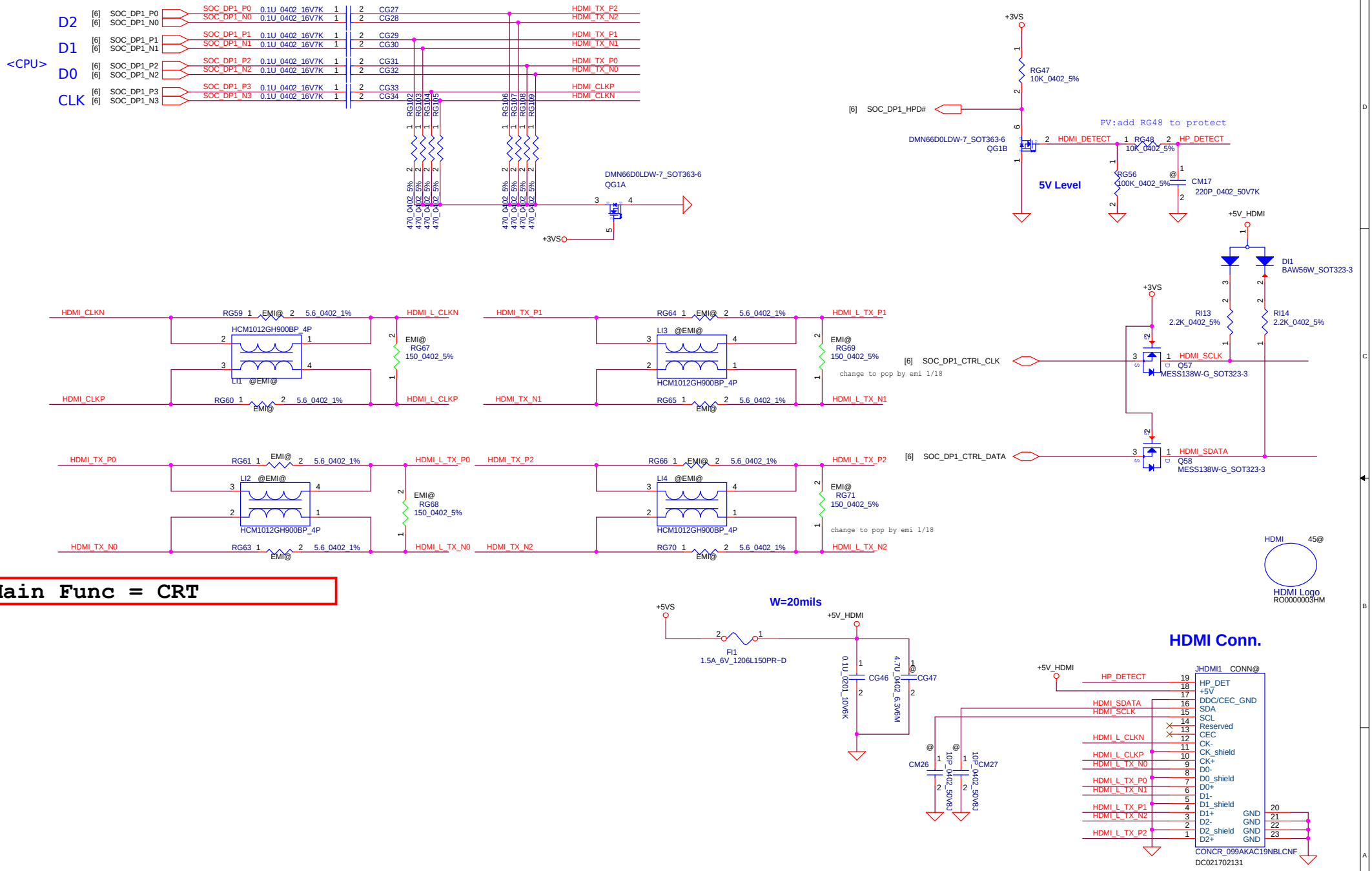

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.

Title: **HDMI Conn/Level shift**

Size	Document Number	Rev
	LA-G094PR10	1.0

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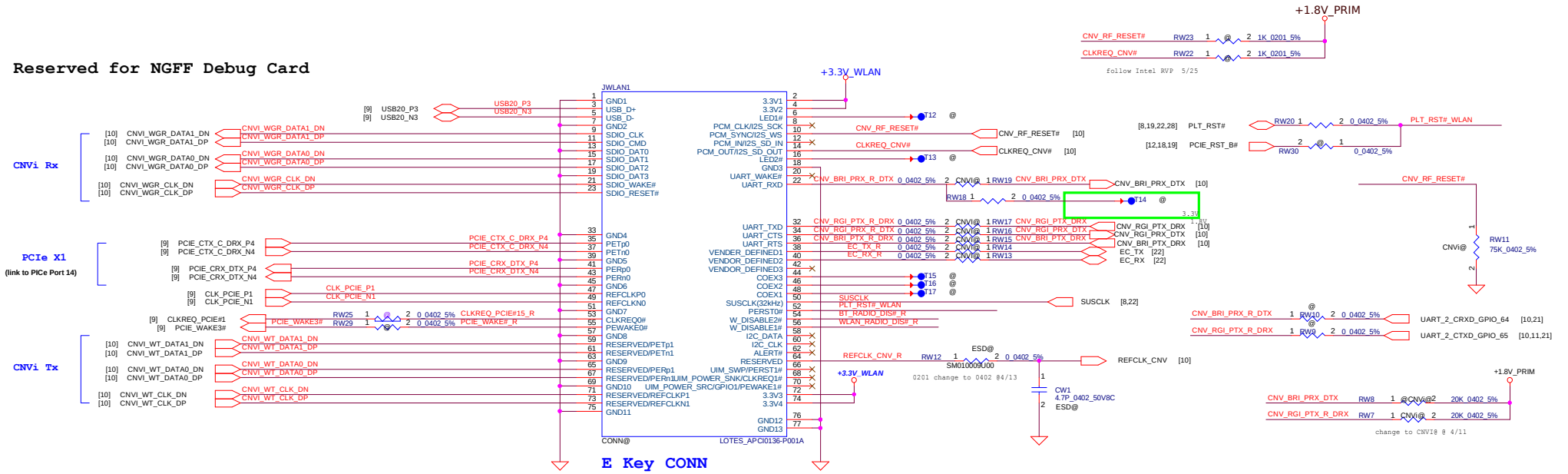
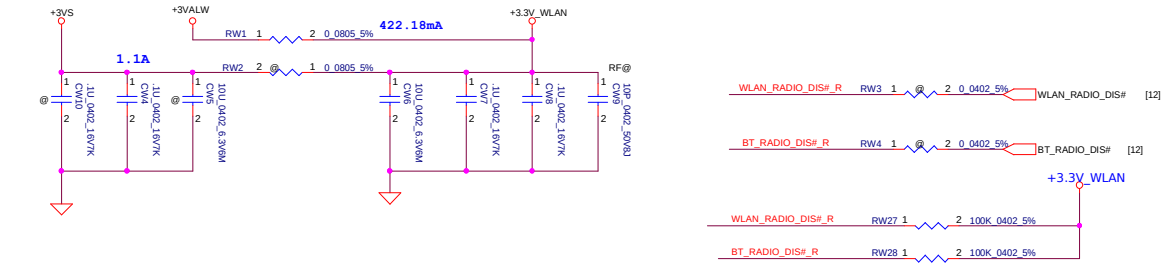
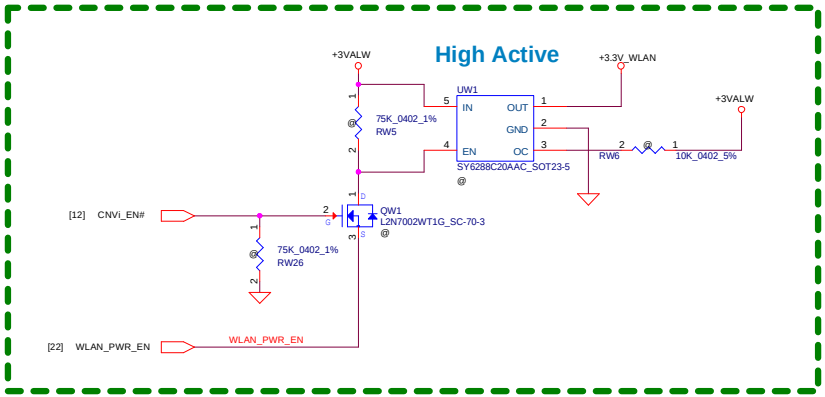
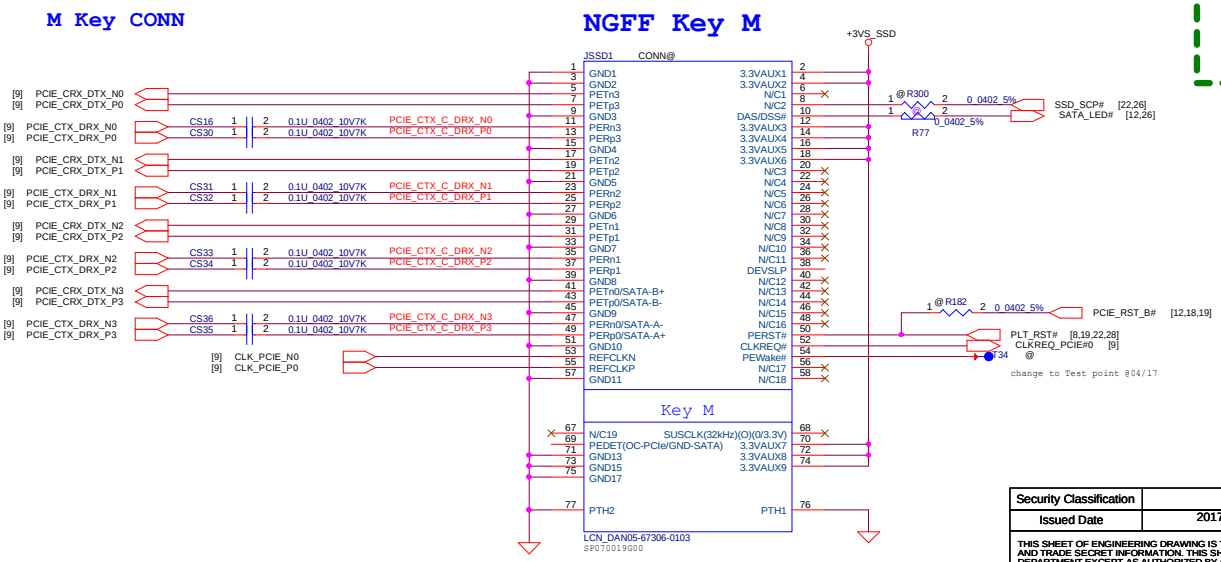
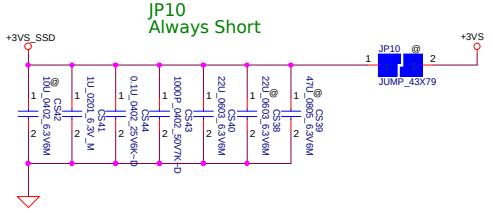
Reserved for NGFF Debug Card











Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.

Title: **WLAN-BT/SSD Conn**

Size	Document Number	Rev
	LA-G094PR10	1.0

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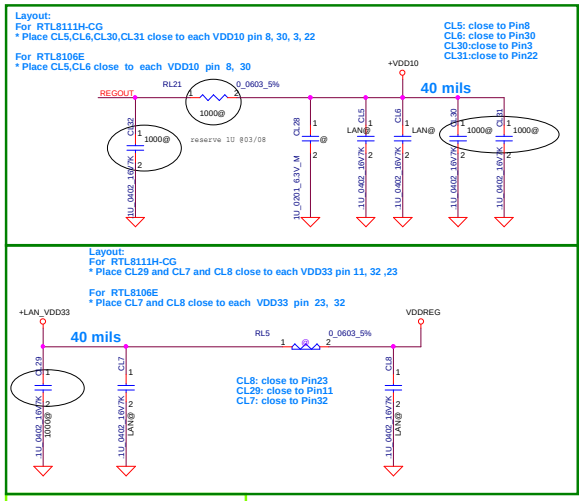
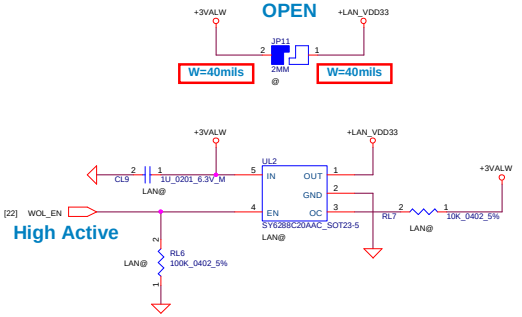
Main Func = LAN

LAN Chip (10/100/1000M)



+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



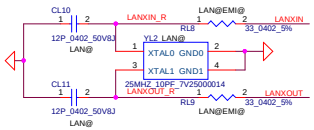
UL1 1000@

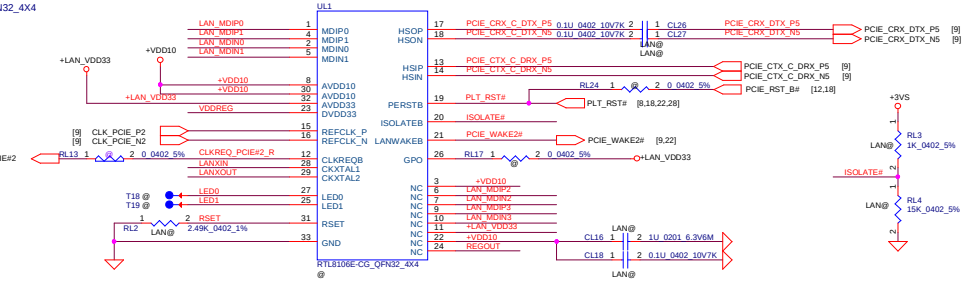
RTL8111H-CG QFN 32P E-LAN CTRL
SA000080P00

UL1

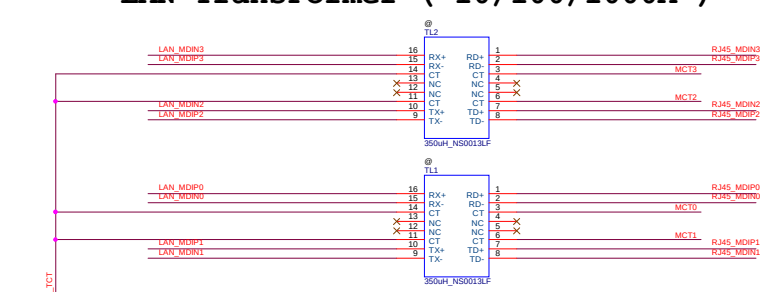
RTL8106E-CG_QFN32_4X4
SA000065Y00
100@

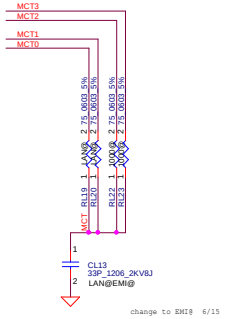
RTL8106E-CG
SA000065Y00
LDO mode
10/100M





LAN TransFormer (10/100/1000M)





Layout note:
30 mil spacing between MDI differential pairs.

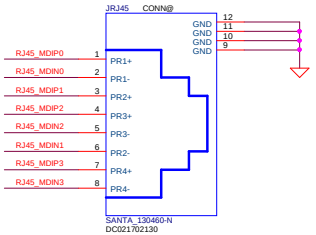
Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF

TL1
MHPC_NS681611H
SP050009800
100@

TL1
MHPC_NS681611H
SP050009800
1000@

TL2
MHPC_NS681611H
SP050009800
1000@



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.	
Title	LAN RTL8106E-CG
Size	Document Number: LA-G094PR10
Rev	1.0
Date:	Thursday, November 08, 2018
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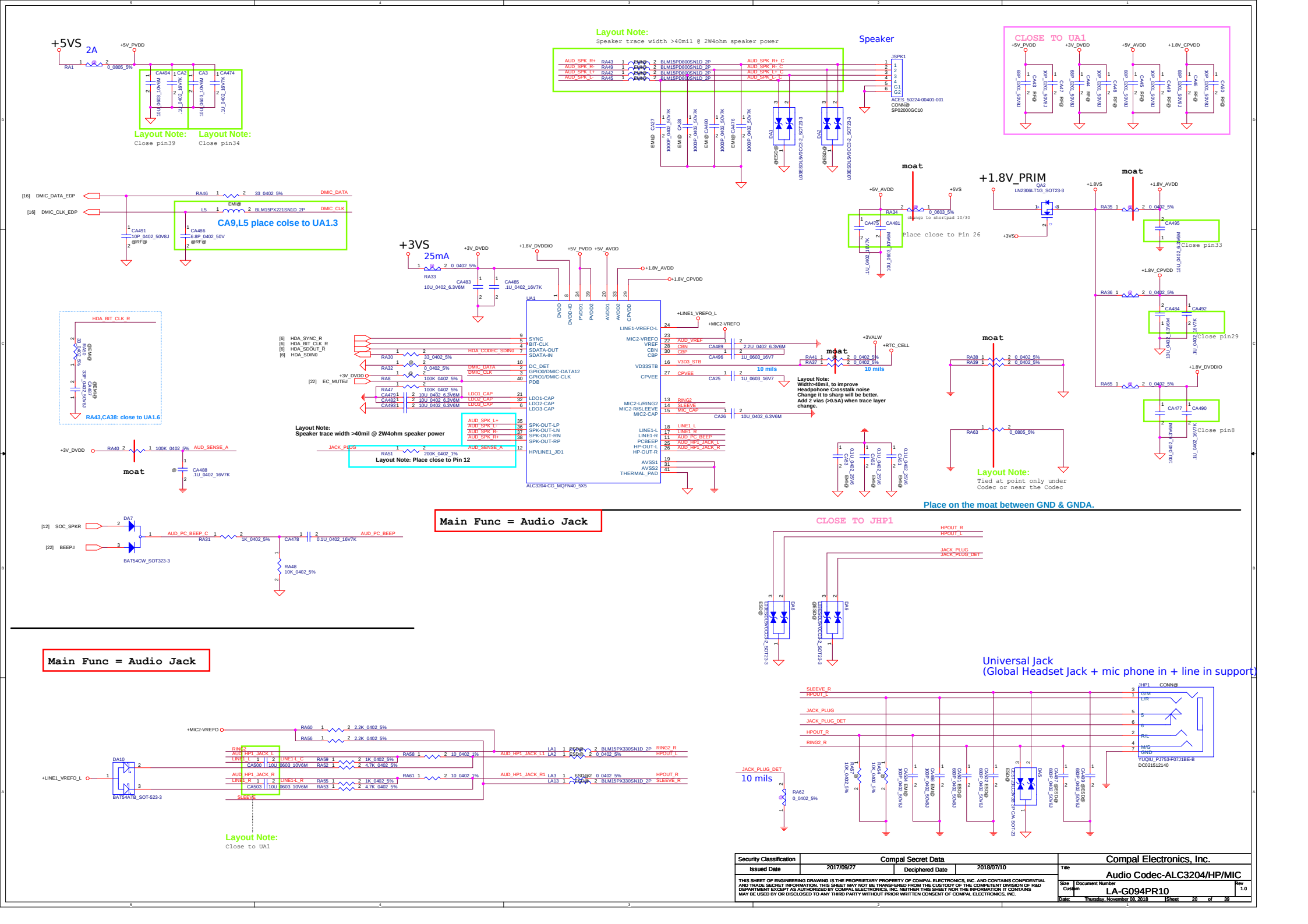

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

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Compal Electronics, Inc.

Title: Audio Codec-ALC3204/HP/MIC

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

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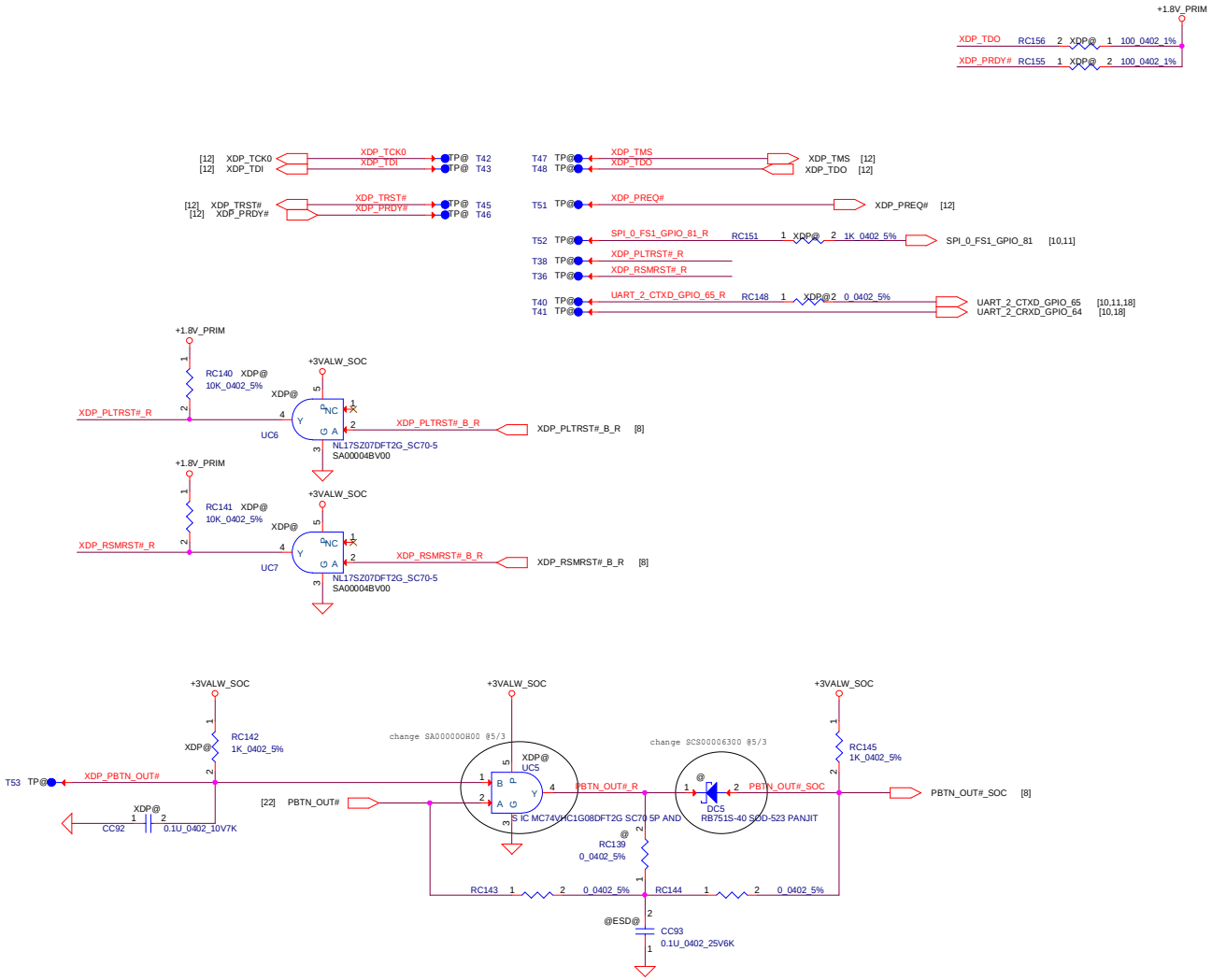

Table 167. MIPI-60 Connector Pinout

Pin	MIPI-60 Signal Name	Target Signal Name	I/O	Pin	MIPI-60 Signal Name	Target Signal Name	I/O
1	VREF_DEBUG	V1P8	NA	2	TMS/TMSC	JTAG_TMS	O
3	TCK	JTAG_TCK	O	4	TDO/EXTA	JTAG_TDO	I
5	TDI/EXTB	JTAG_TDI	O	6	nRESET	PMU_RSTBTN_N. Refer to Figure 171	O
7	RTCK/EXTC	PMU_PLTRST_N	I	8	TRST_PD	10kOhm Pull-Down to GND	NA
9	nTRST/EXTD	JTAG_TRST_N	O	10	EXTE/TRIGIN	JTAG_PREQ_N	O
11	EXTF/TRIGOUT	JTAG_PRDY_N	I	12	VREF_TRACE	V1P8	NA
13	TRC_CLK0	GPIO_0	I	14	TRC_CLK1	GPIO_18[1]	I
15	Target Presence Detect	Strapping resistor of SIO_SPI_2_TXD/ GPIO_123 Refer to Figure 220	NA	16	GND	GND	NA
17	TRC_DATA0[0]	GND	NA	18	TRC_DATA1[0]/ TRC_DATA0[20]	GPIO_19[1]	I
19	TRC_DATA0[1]	GPIO_1	I/O	20	TRC_DATA1[1]/ TRC_DATA0[21]	GPIO_20[1]	I
21	TRC_DATA0[2]	GPIO_2	I/O	22	TRC_DATA1[2]/ TRC_DATA0[22]	GPIO_21[1]	I
23	TRC_DATA0[3]	GPIO_3	I/O	24	TRC_DATA1[3]/ TRC_DATA0[23]	GPIO_22[1]	I
25	TRC_DATA0[4]	GPIO_4	I/O	26	TRC_DATA1[4]/ TRC_DATA0[24]	GPIO_23[1]	I
27	TRC_DATA0[5]	GPIO_5	I/O	28	TRC_DATA1[5]/ TRC_DATA0[25]	GPIO_24[1]	I
29	TRC_DATA0[6]	GPIO_6	I/O	30	TRC_DATA1[6]/ TRC_DATA0[26]	GPIO_25[1]	I
31	TRC_DATA0[7]	GPIO_7	I/O	32	TRC_DATA1[7]/ TRC_DATA0[27]	GPIO_26[1]	I
33	TRC_DATA0[8]	GPIO_8	I/O	34	TRC_DATA1[8]/ TRC_DATA0[28]	Connect to Pin 6 (RESET_BTN_N)	O
35	TRC_DATA0[9]	GPIO_10	I/O	36	TRC_DATA1[9]/ TRC_DATA0[29]	Strapping resistor of GP_SSP_0_FS1/ GPIO_106 (BOOT_HALT_N Strap) Refer to Figure 220	O
37	TRC_DATA3[0]/ TRC_DATA0[10]	GPIO_11	I/O	38	TRC_DATA2[0]/ TRC_DATA1[10]/ TRC_DATA0[30]	Connect to Pin 7 (PMU_PLTRST_N)	I
39	TRC_DATA3[1]/ TRC_DATA0[11]	GPIO_12	I/O	40	TRC_DATA2[1]/ TRC_DATA1[11]/ TRC_DATA0[31]	POWER_BTN_N	O
41	TRC_DATA3[2]/ TRC_DATA0[12]	GPIO_13	I/O	42	TRC_DATA2[2]/ TRC_DATA1[12]/ TRC_DATA0[32]	RSMRST_N	I
43	TRC_DATA3[3]/ TRC_DATA0[13]	GPIO_14	I/O	44	TRC_DATA2[3]/ TRC_DATA1[13]/ TRC_DATA0[33]	GPIO_28[1]	I
45	TRC_DATA3[4]/ TRC_DATA0[14]	GPIO_15	I/O	46	TRC_DATA2[4]/ TRC_DATA1[14]/ TRC_DATA0[34]	GPIO_29[1]	I
47	TRC_DATA3[5]/ TRC_DATA0[15]	GPIO_16	I/O	48	TRC_DATA2[5]/ TRC_DATA1[15]/ TRC_DATA0[35]	I2C_SCL	I/O
49	TRC_DATA3[6]/ TRC_DATA0[16]	GPIO_17	I/O	50	TRC_DATA2[6]/ TRC_DATA1[16]/ TRC_DATA0[36]	I2C_SDA	I/O
51	TRC_DATA3[7]/ TRC_DATA0[17]	No Connect	NA	52	TRC_DATA2[7]/ TRC_DATA1[17]/ TRC_DATA0[37]	GPIO_30[1]	I
53	TRC_DATA3[8]/ TRC_DATA0[18]	No Connect	NA	54	TRC_DATA2[08]/ TRC_DATA1[18]/ TRC_DATA0[38]	UART1_TXD/GPIO_43	I
55	TRC_DATA3[9]/ TRC_DATA0[19]	No Connect	NA	56	TRC_DATA2[9]/ TRC_DATA1[19]/ TRC_DATA0[39]	UART1_RXD/GPIO_42	O
57	GND	GND	NA	58	GND	GND	NA
59	TRC_CLK3	GPIO_9	I	60	TRC_CLK2	GPIO_27[1]	I

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: *XDP debug port*

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

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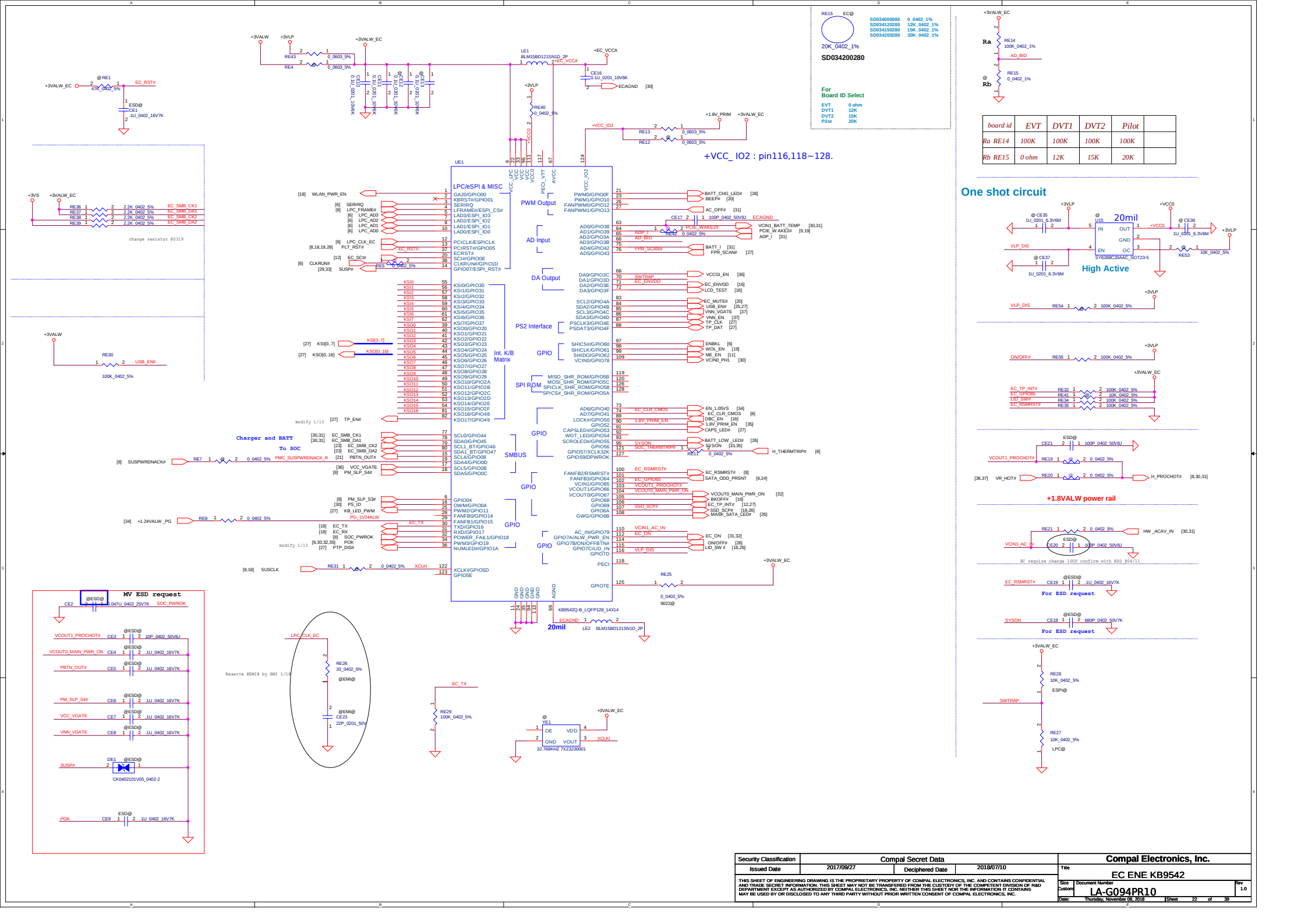

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

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Compal Electronics, Inc.

Title: EC ENE KB9542

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

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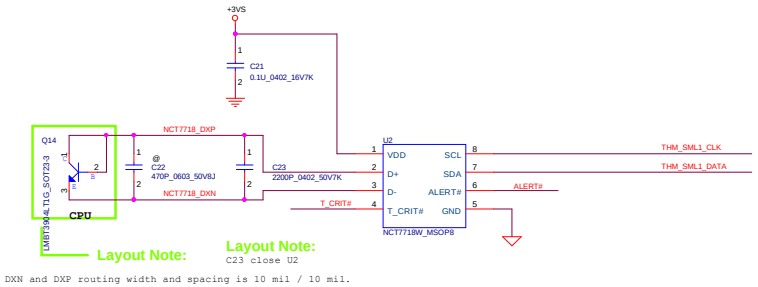
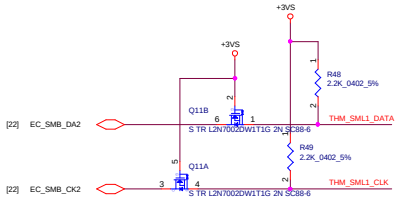
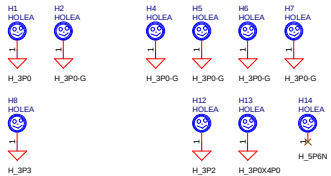
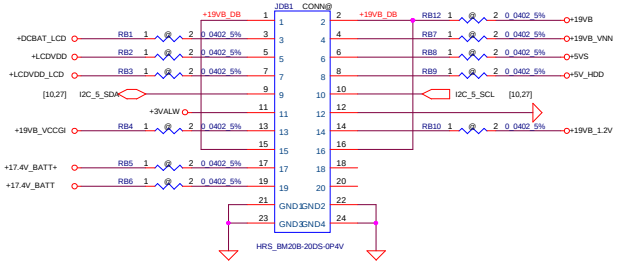
Main Func = Thermal



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125







RB1 Close to R301
RB2 Close to R3
RB3 Close to R3
RB4 Close to PJPG1
RB5 Close to PJP3
RB6 Close to PJP3

RB12 Close to PJPH02
RB7 Close to PJPZ1
RB8 Close to RS32
RB9 Close to RS32
RB10 Close to PJPM01

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

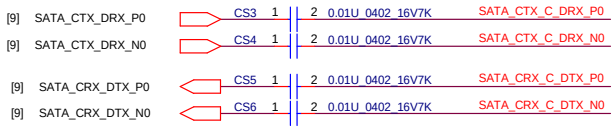
Compal Electronics, Inc.

Title: Thermal/Screw hole

Size | Document Number: LA-G094PR10 | Rev: 1.0

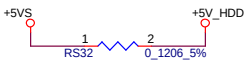
Date: Thursday, November 08, 2018 | Sheet 23 of 39

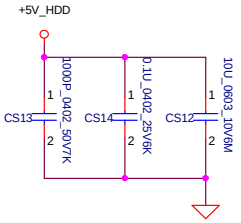
Main Func = HDD

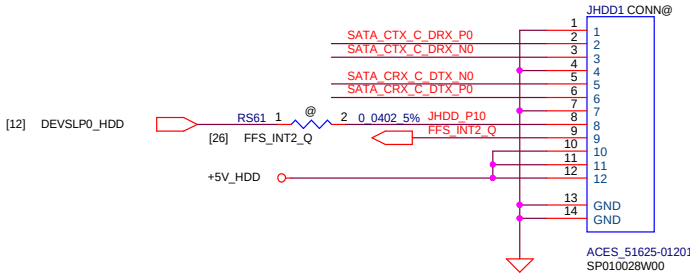


+5V_HDD Source

60 mils

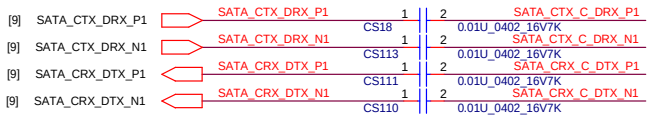




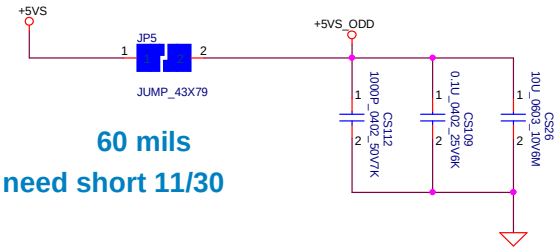


Main Func = ODD

SOC TX
SOC RX

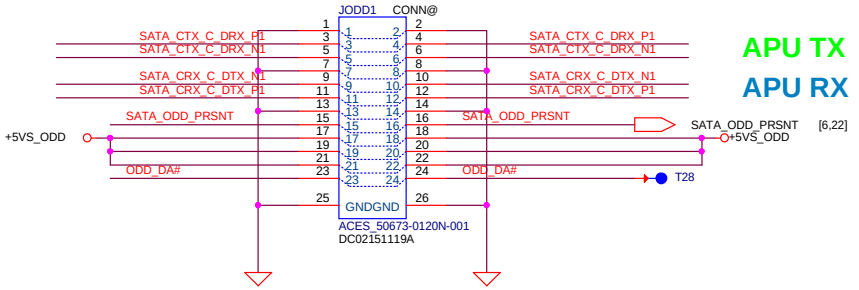


ODD Power Control



60 mils
need short 11/30

SATA ODD Connector (FFC Type)



APU TX
APU RX

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

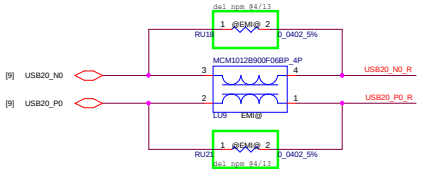
Compal Electronics, Inc.

Title: HDD/ODD Conn

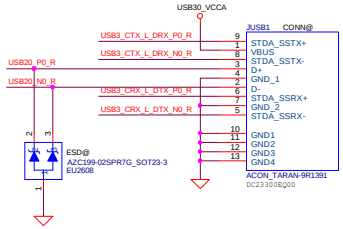
Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

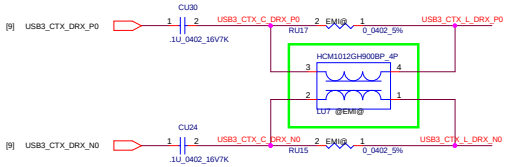
Date: Thursday, November 08, 2018 | Sheet 24 of 39

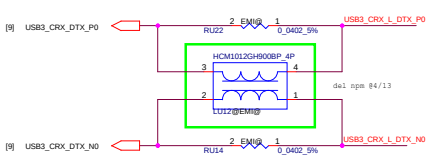
Main Func = USB3.0 Port1



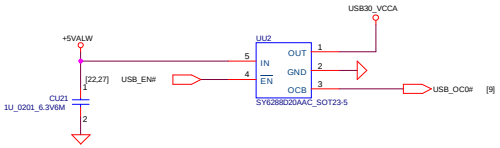
USB3.0 Port1

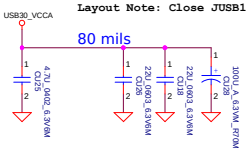


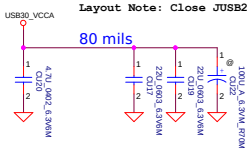




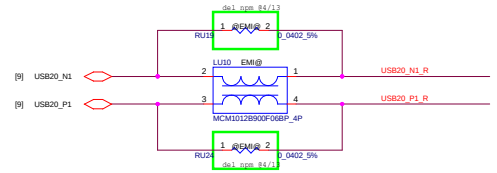
Maximum Output Current 2A



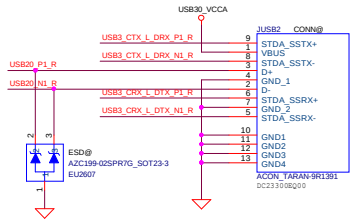


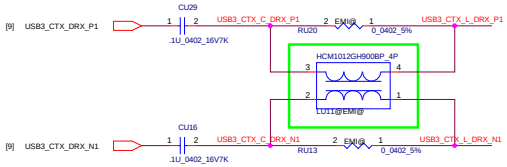


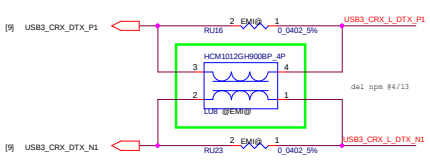
Main Func = USB3.0 Port2



USB3.0 Port2







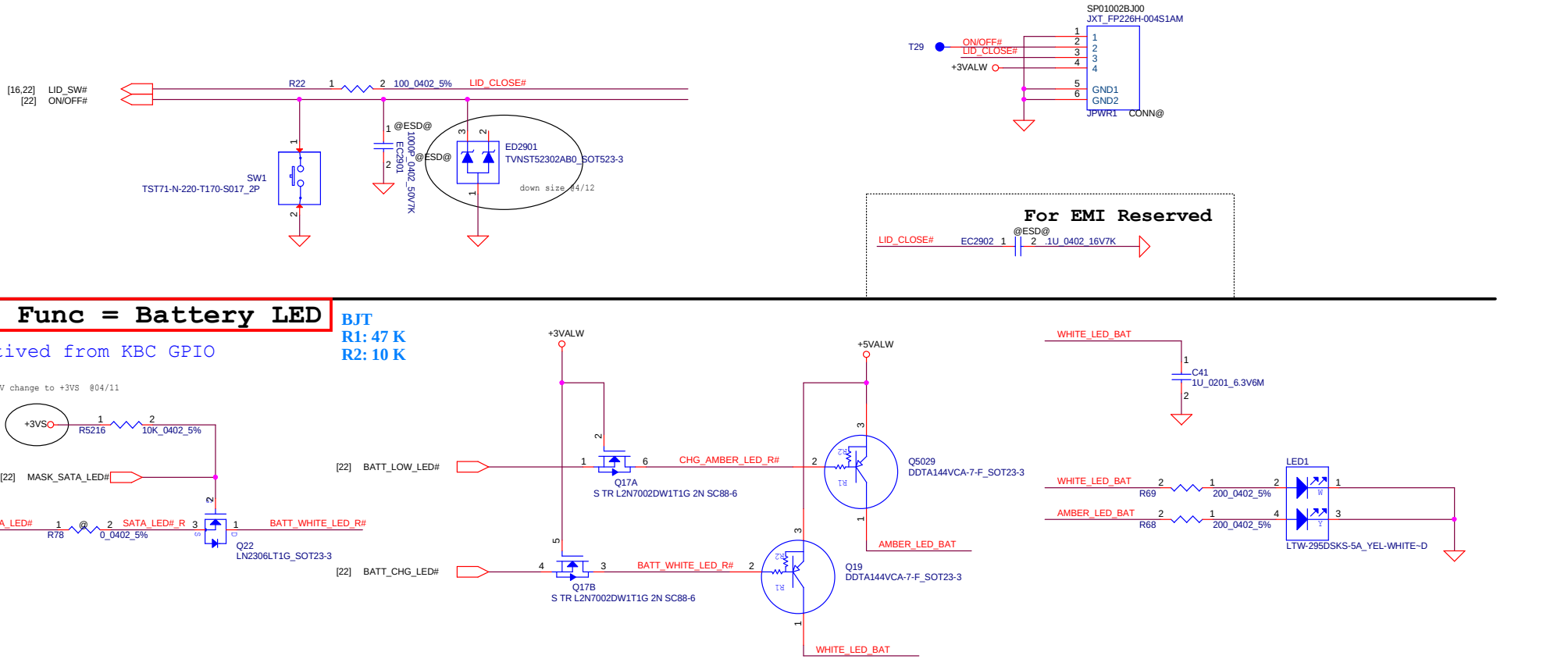
Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.

Title: USB 3.0 Conn

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 25 of 39



Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

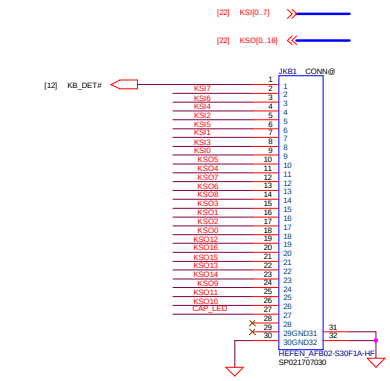
Compal Electronics, Inc.

Title: PWRBTN_LID Conn/LED/FFS

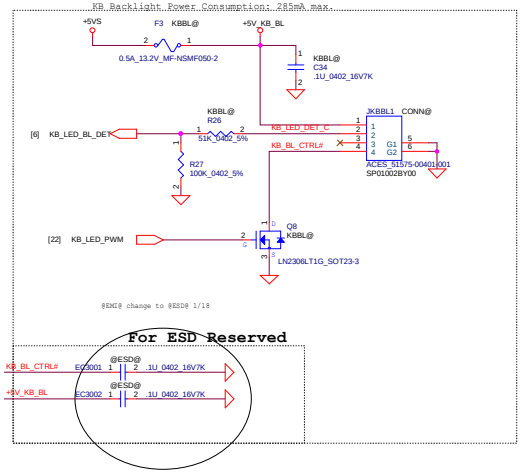
Size	Document Number	Rev
Custom	LA-G094PR10	1.0

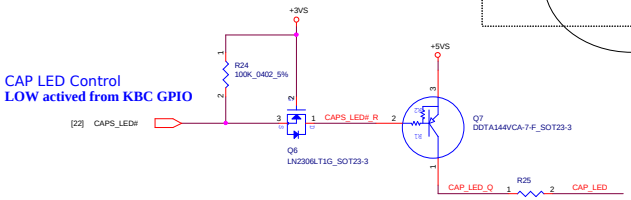
Date: Thursday, November 08, 2018 Sheet 26 of 39

Main Func = KB

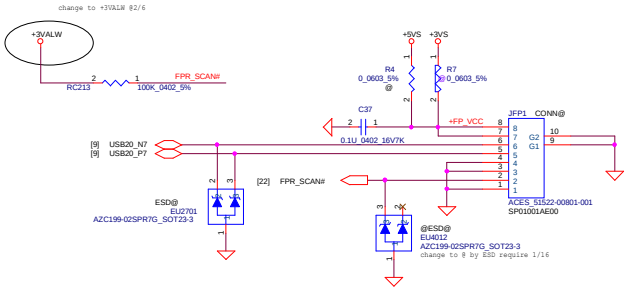


Keyboard Backlight (Reserved)

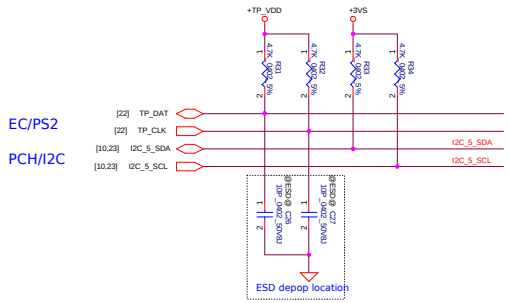


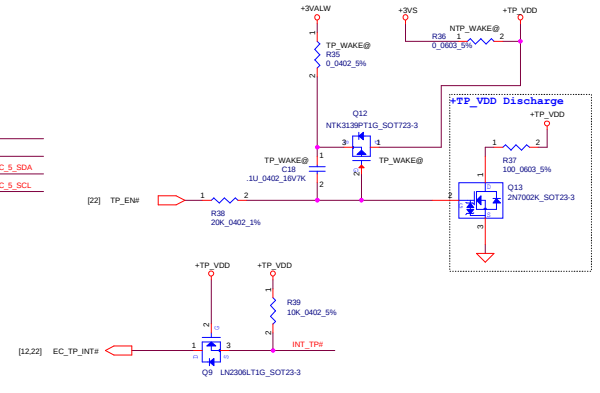


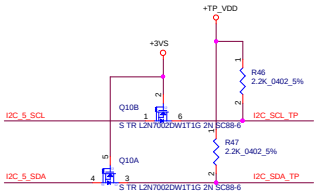
Main Func = FP

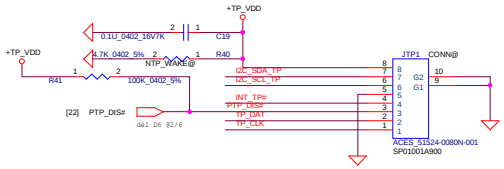


Main Func = TPAD



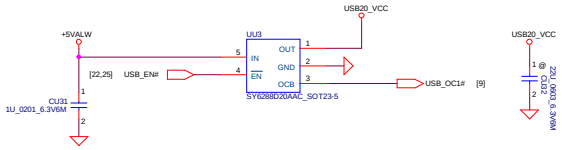




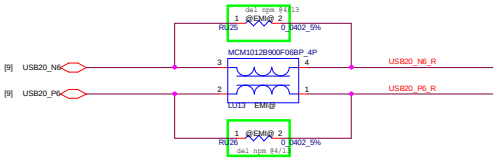


Main Func = USB2.0 + Card Reader on IO/B

SY6288D Support 2A

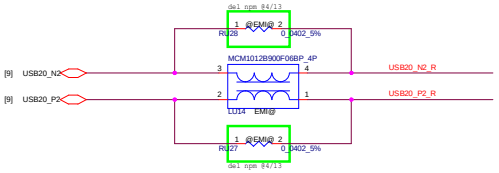


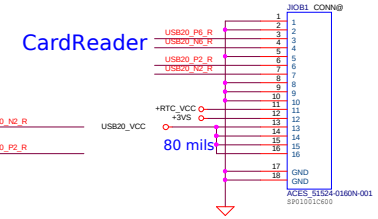
CardReader



I/O Board Connector

CardReader





Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.	
Title	KB/KBBL/TP/FP/IO Conn
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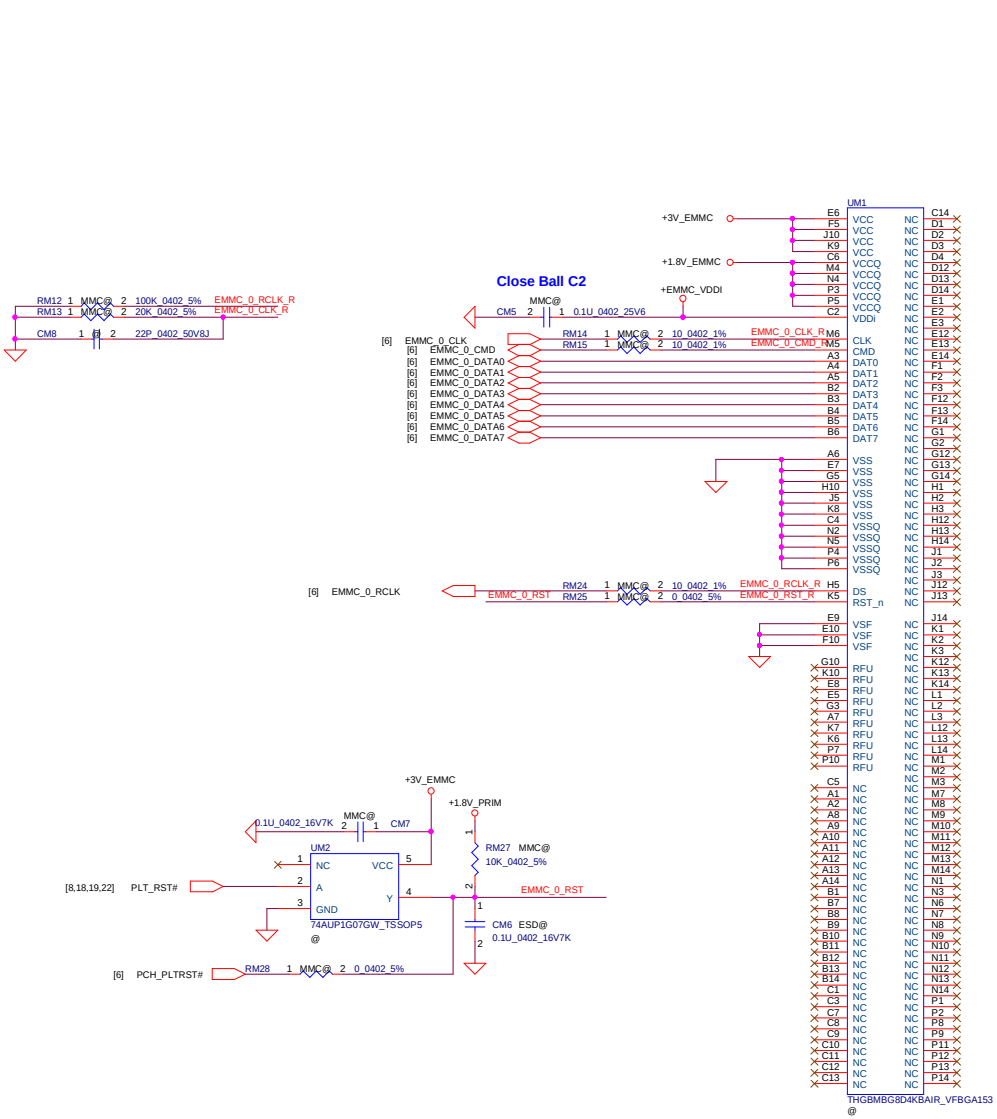
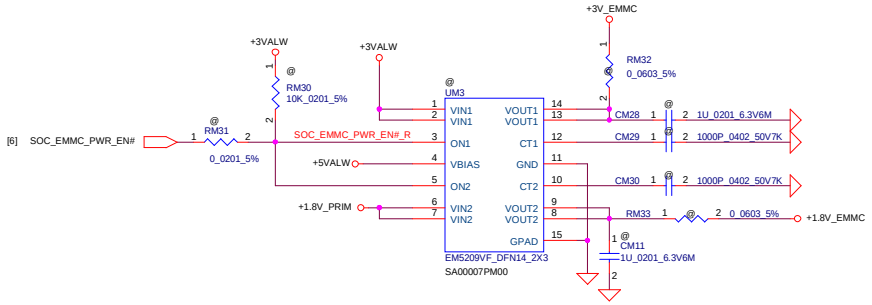
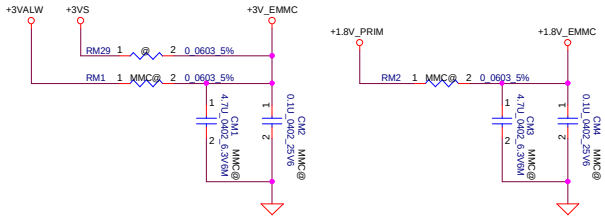
Main Func = eMMC

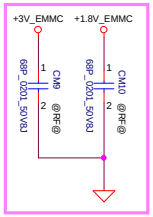






RM1,CM1,CM2: close to UM1.F5

RM2,CM3,CM4: close to UM1.P3



eMMC R1

UM1 S32G_R1@

S IC FL 32G SDINBDA4-32-859W BGA 153P
Part Number = SA0000C082L
FL 32G SDINBDA4-32-859W

UM1 S64G_R1@

S IC FL 64G SDINBDA4-64-859W BGA 153P EMMC
Part Number = SA0000B4R2L
FL 64G SDINBDA4-64-859W

UM1 H32G_R1@

S IC FL 32G H26M62002JPR FBGA 153P EMMC
Part Number = SA0000ADH1L
FL 32G H26M62002JPR

UM1 H64G_R1@

S IC FL 64G H26M74002HMR FBGA 153P
Part Number = SA0000A714L
FL 64G H26M74002HMR

eMMC R3

UM1 S32G_R3@

S IC FL 32G SDINBDA4-32-859W BGA 153P A31 !
Part Number = SA0000C083L
FL 32G SDINBDA4-32-859W

UM1 S64G_R3@

S IC FL 64G SDINBDA4-64-859W BGA 153P EMMC A31 !
Part Number = SA0000B4R3L
FL 64G SDINBDA4-64-859W

UM1 H32G_R3@

S IC FL 32G H26M62002JPR FBGA 153P A31!
Part Number = SA0000ADH2L
FL 32G H26M62002JPR

UM1 H64G_R3@

S IC FL 64G H26M74002HMR FBGA 153P A31 !
Part Number = SA0000A715L
FL 64G H26M74002HMR

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: RSV for eMMC

Size: | Document Number: LA-G094PR10 | Rev: 1.0

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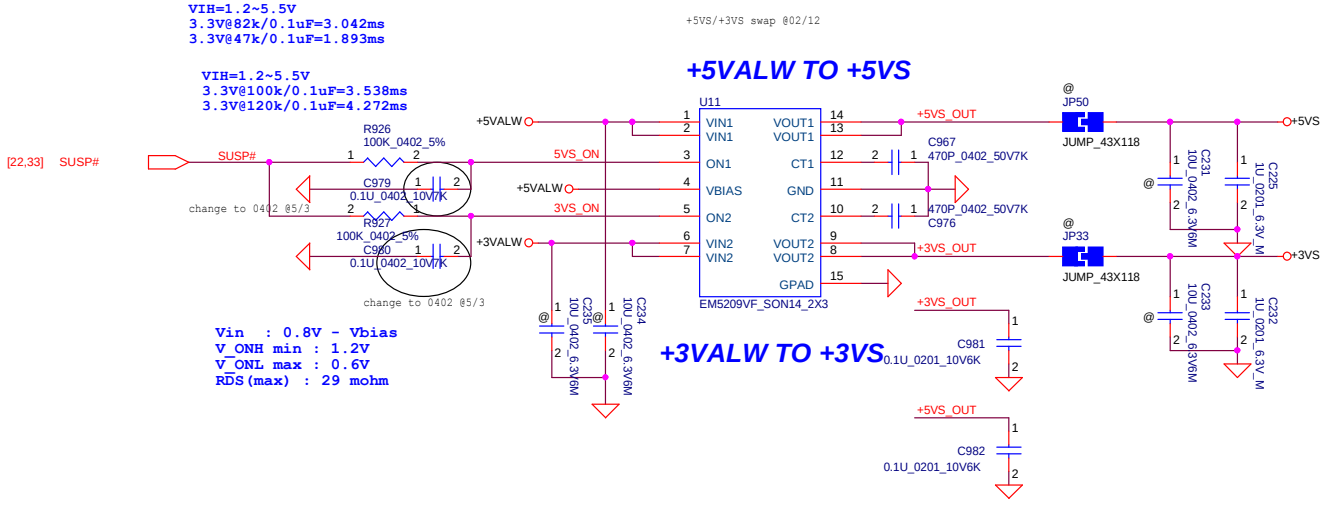

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

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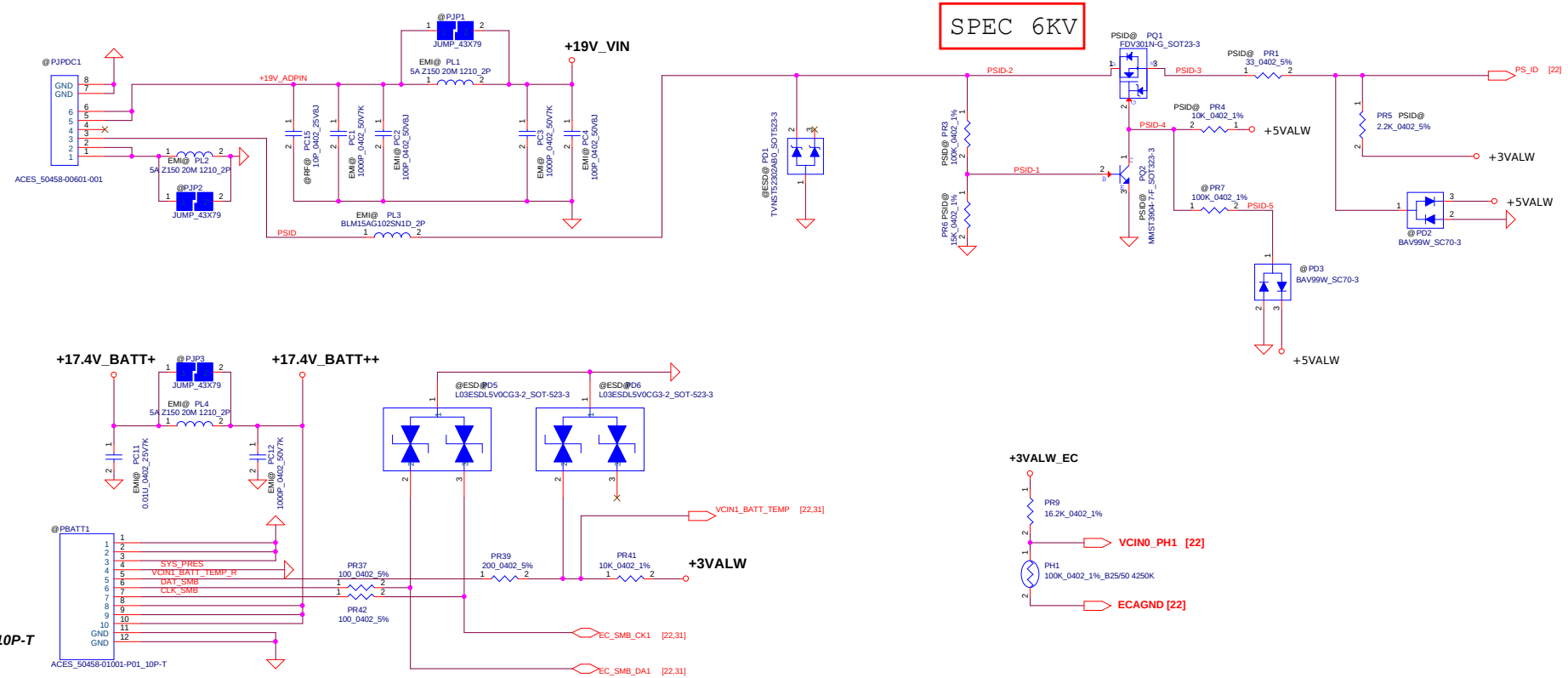
SPEC 6KV

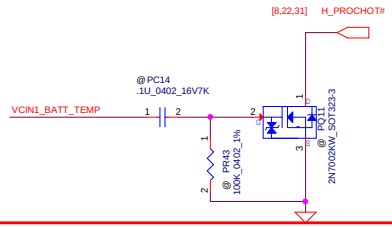
Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

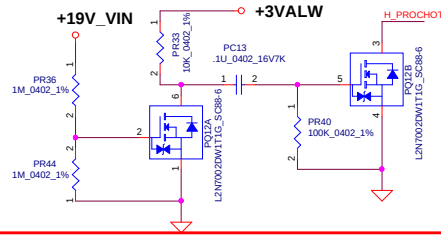
ACES_50458-01001-P01_10P-T



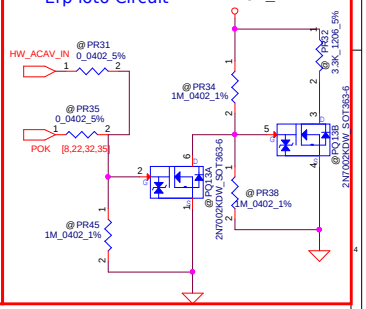
Adapter protection:
if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user



Battery protection:
asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit



DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: **PWR_DCIN/BATT CONN/OTP**

Size	Document Number	Rev
		X00

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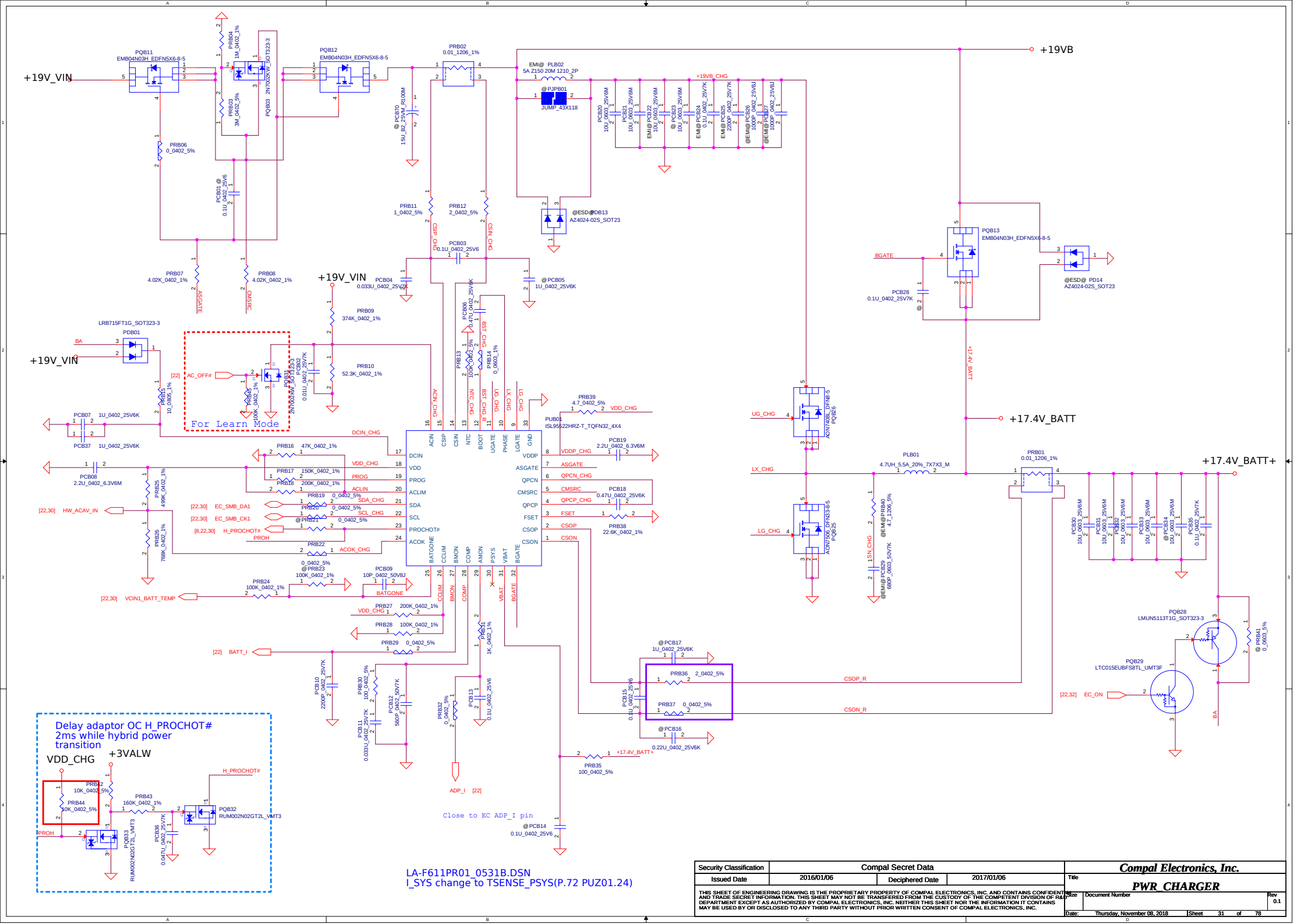
+19V_VIN
+19VB
+17.4V_BATT
+17.4V_BATT+
+3VALW
PQB11 EMB04N03H_EDFN5X6-8-5
PQB12 EMB04N03H_EDFN5X6-8-5
PRB02 0.01_1206_1%
EMI@ PLB02 5A Z150 20M 1210_2P
@PJPB01 JUMP_43X118
@ESD@DB13 AZ4024-02S_SOT23
PQB13 EMB04N03H_EDFN5X6-8-5
@ESD@ PD14 AZ4024-02S_SOT23
PQB28 0.1U_0402_25V7K
PUB01 ISL95522HRZ-T_TQFN32_4X4
PQB26 AON7408L_DFN8-5
PQB25 AON7506_DFN33-8-5
PLB01 4.7UH_5.5A_20%_7X7X3_M
PRB01 0.01_1206_1%
PQB28 LMUN5113T1G_SOT323-3
PQB29 LTC015EUBFS8TL_UMT3F
PDB01 LRB715FT1G_SOT323-3
PQB32 RUM002N02GT2L_VMT3
PQB33 RUM002N02GT2L_VMT3
For Learn Mode
Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition
VDD_CHG
H_PROCHOT#
PROH
Close to EC ADP_I pin
LA-F611PR01_0531B.DSN
I_SYS change to TSENSE_PSYS(P.72 PUZ01.24)
Security Classification
Compal Secret Data
Issued Date
2016/01/06
Deciphered Date
2017/01/06
Compal Electronics, Inc.
PWR_CHARGER
Size
Document Number
Rev
0.1
Date: Thursday, November 08, 2018
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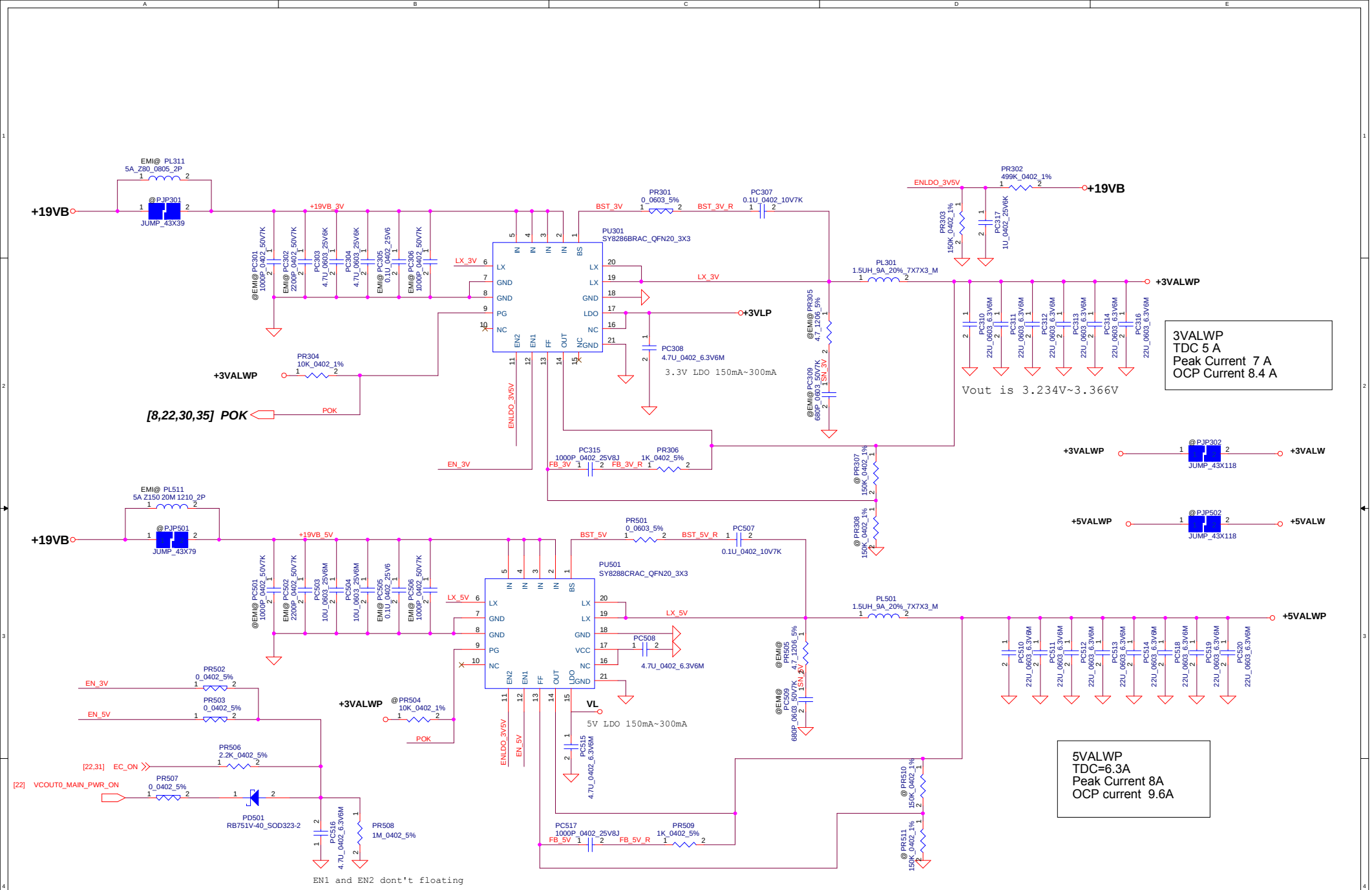

Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.

Title: **PWR_3.3VALWP/5VALWP**

Size	Document Number	Rev
		0.1(X00)

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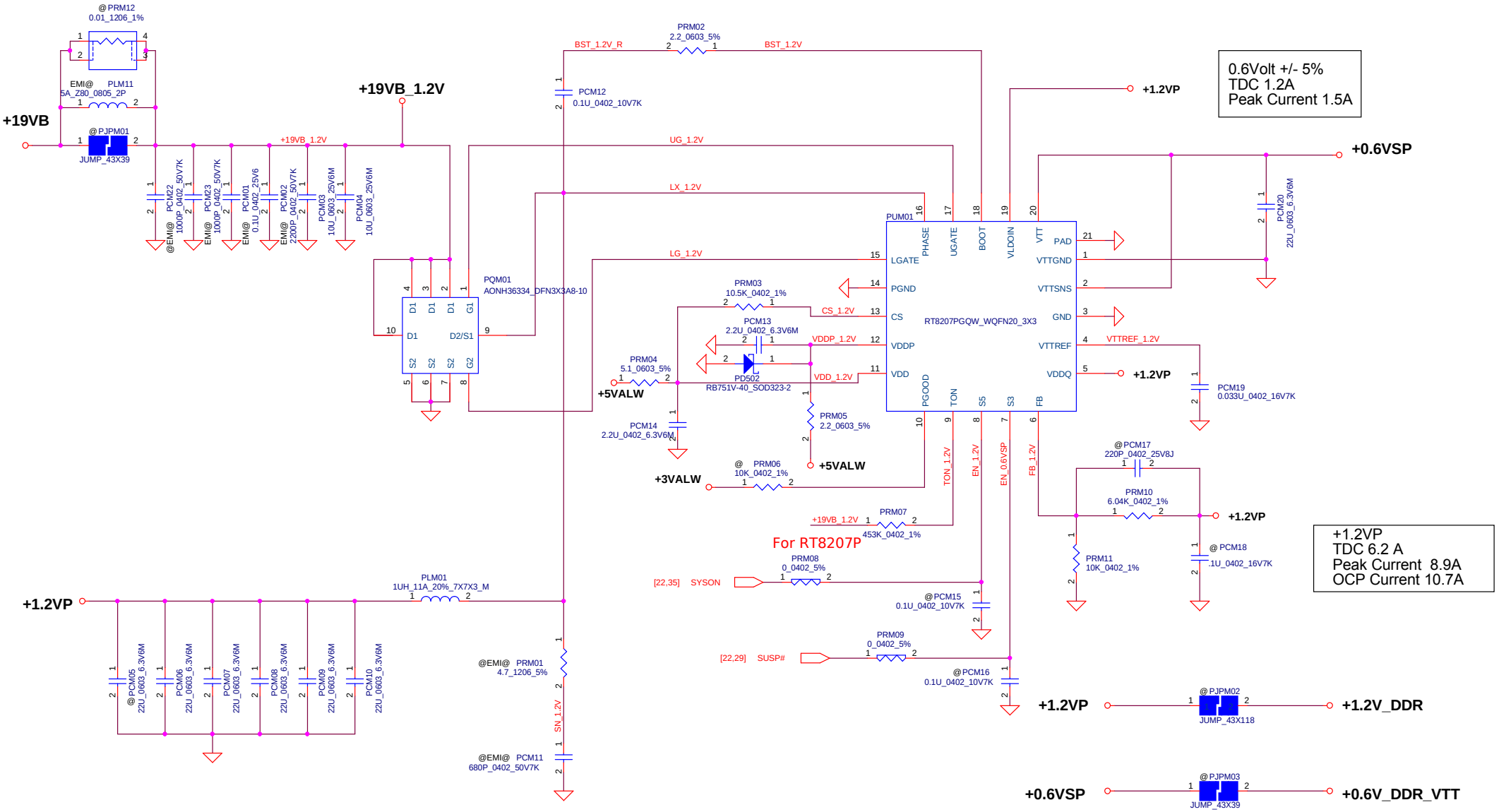

Mode	S3	S5	+1.2V_MEN	+V_DDR_REF	+0.6V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1.2V_DDR/+0.6V_DDR_VTT

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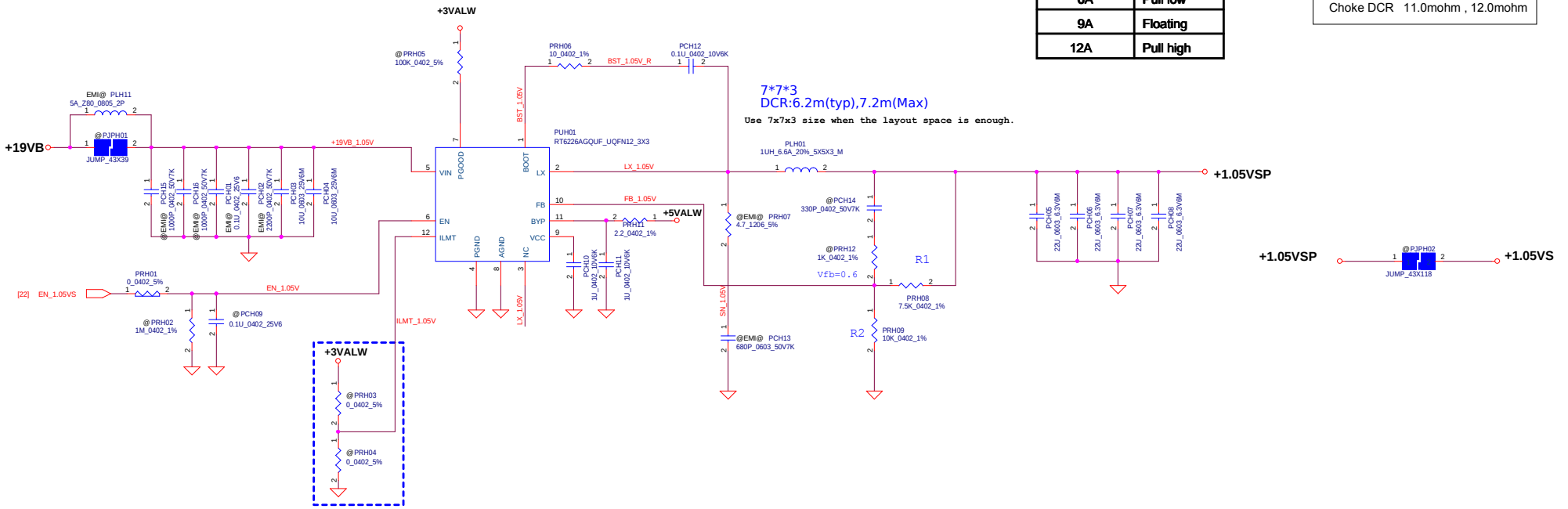
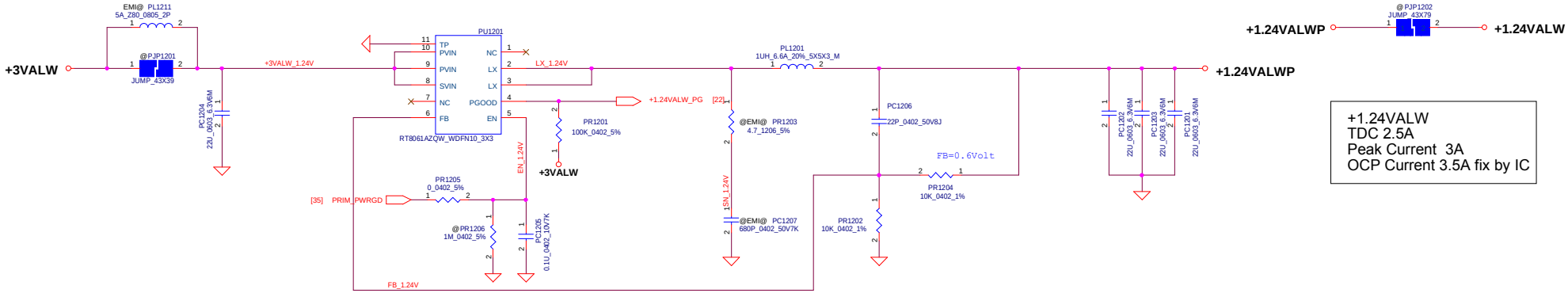
The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

+1.05VSP
TDC 5.2 A
Peak Current 6.5 A
OCP Current 9 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm





+1.24VALW
TDC 2.5A
Peak Current 3A
OCP Current 3.5A fix by IC

Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1.05VS/+1.24VALW

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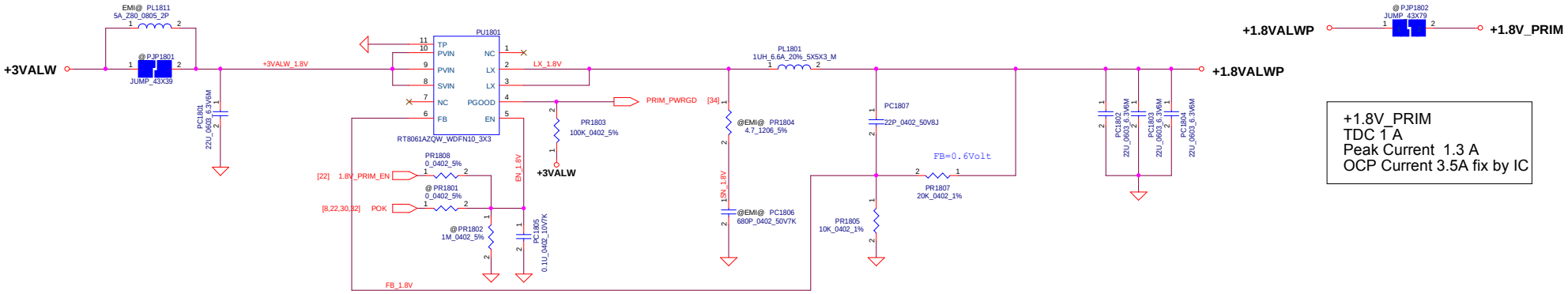
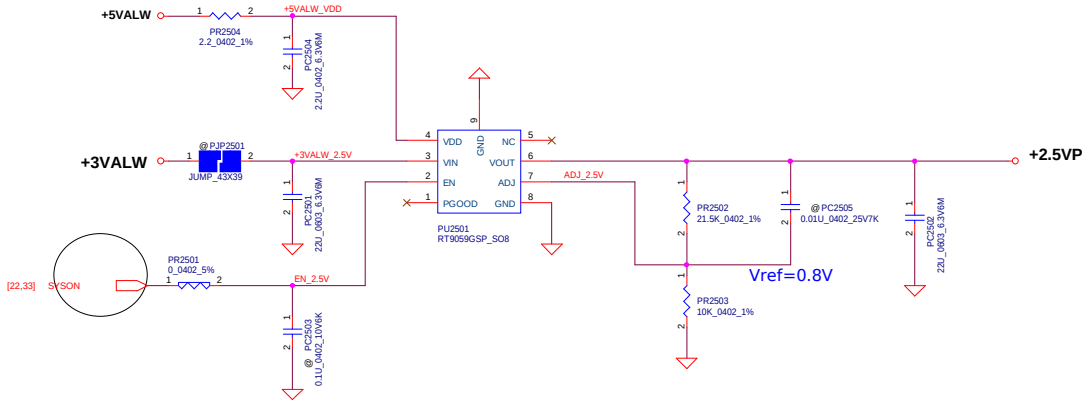


+1.8V_PRIM
TDC 1 A
Peak Current 1.3 A
OCP Current 3.5A fix by IC



+2.5V
TDC 0.45 A
Peak Current 0.57 A

Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1.8V_PRIM and +2.5V

Size: C | Document Number | Rev: X00

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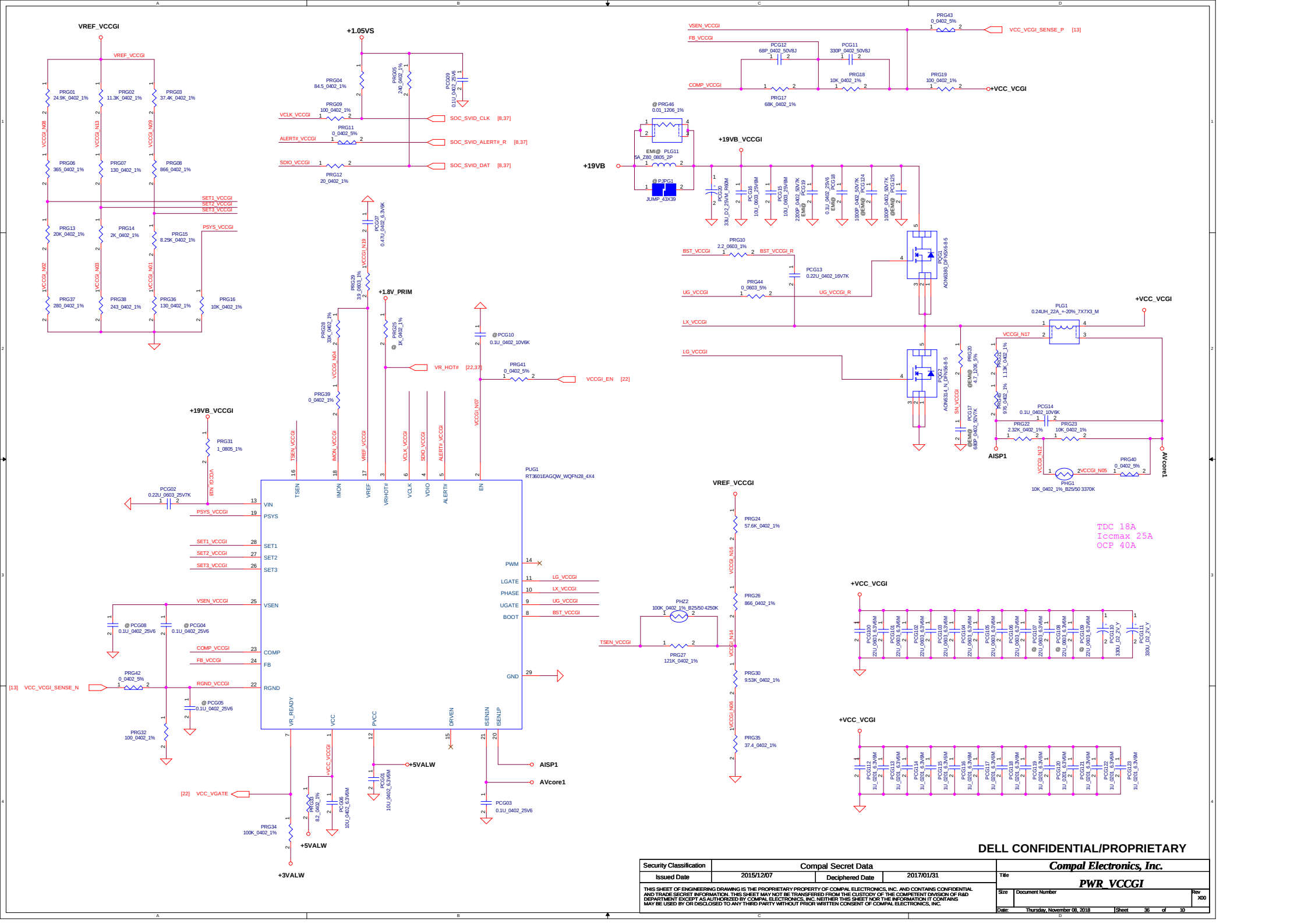

Security Classification	Compal Secret Data		
Issued Date	2015/12/07	Deciphered Date	2017/01/31

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Compal Electronics, Inc.

Title: **PWR_VCCGI**

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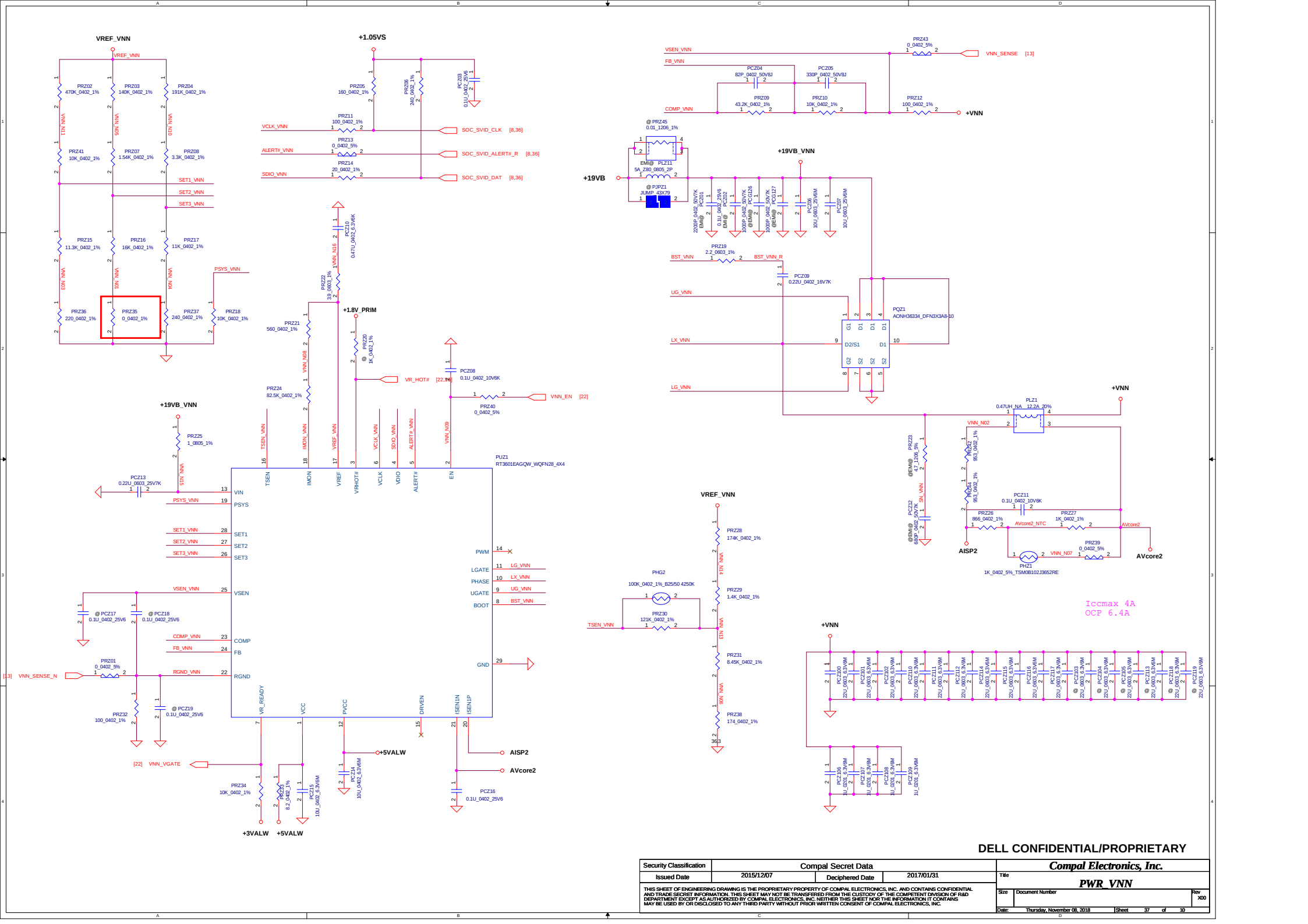

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Security Classification	Compal Secret Data		
Issued Date	2015/12/07	Deciphered Date	2017/01/31

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Compal Electronics, Inc.

Title: **PWR_VNN**

Size | Document Number | Rev X00

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P31	CHARGER	20180520	COMPAL	customer recommend	change PUB01 ver B to ver C	0.1
2	P31	CHARGER	20180628	COMPAL	MLCC downsize	Change the PRB11 from 2Ohm to 1Ohm Change the PCB07 from 1U_0603_25V to 2.2U_0402_25V Change the PCB011 from 0.022U_0402_25V to 0.033U_0402_25V Change the PCB06 and PCB18 from 0.22U_0603_25V to 0.47U_0402_25V	0.2
3	P36	VCCGI	20180628	COMPAL	Fine tune ICCMAX	Change the PRG28 from 46.4KOhm to 33khm Change the PRG39 from 100Ohm to 0Ohm	0.2
4	P36	VCCGI	20180628	COMPAL	Change SET2 for FSW adjustable for VIN=19.5V	Change the PRG02 from 3.92KOhm to 11.3KOhm Change the PRG07 from 12.1Ohm to 130Ohm Change the PRG14 from 3.57KOhm to 2KOhm Change the PRG38 from 12.1Ohm to 243Ohm	0.2
5	P36	VCCGI	20180628	COMPAL	Fine tune LL	Change the PRG17 from 59KOhm to 68KOhm Change the PRG21 from 1.37KOhm to 1.13KOhm	0.2
6	P36	VCCGI	20180628	COMPAL	Fine tune AC IMON	Change the PRG21 from 1.37KOhm to 1.13KOhm Change the PRG45 from 1.37KOhm to 976Ohm Change the PRG22 from 2.8KOhm to 2.32kOhm	0.2
7	P37	VNN	20180628	COMPAL	Change SET2 for FSW adjustable for VIN=19.5V	Change the PRZ03 from 30.1kOhm to 140kOhm Change the PRZ07 from 63.4Ohm to 1.54KOhm Change the PRZ16 from 27.4KOhm to 16KOhm Change the PRZ35 from 63.4Ohm to 0Ohm	0.2
8	P37	VNN	20180628	COMPAL	Fine tune ICCMAX	Change the PRZ24 from 64.9KOhm to 82.5KOhm Change the PRZ21 from 1.5KOhm to 560Ohm	0.2
9	P30	BATTERY	20180706	COMPAL	ESD request	Change the PD5 and PD6 from SCA00001W00 to SCA00002A00	0.3
10	P31	CHARGER	20180706	COMPAL	Design request	Change the PRB10 from 47KOhm to 52.3KOhm	0.3
11	P35	+1.8VALWP	20180706	COMPAL	HW request	Add the PR1808_0_0402_5%	0.3
12	P31	CHARGER	20180715	COMPAL	Material shortage	Add the PCB37_1U_0402_25V6K Change the PCB07 from 2.2U_0402_25V6K to 1U_0402_25V6K	0.3
13	P32	3.3/5VALWP	20180824	COMPAL	Delay start time	Add the PC317_1U_0402_25V	0.3
14	P31~P38	ALL power	20181016	COMPAL	Short pad	0 Ohm resistance change to short pad	0.4

Compal Electronics, Inc.

Title: **Changed-List PWR History**

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Version Change List (P. I. R. List)

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	BOM	Layout
Based on DVT2 0824B								
1	2018/10/8	22	RE15	Board ID change to 20K			v	
2	2018/10/24	22	DE1	change to "@ESD@"	ESD reserved		v	
3	2018/10/24	16	R16	change location R16 to F5	for hinge up protection		v	
4	2018/11/6	16	R6	0 ohm change to short pad	it's for NPI debug			v
5	2018/11/6	27	R7	0 ohm change to short pad	it's for NPI debug			v
6	2018/11/6	16	R8	0 ohm change to short pad	it's for NPI debug			v
7	2018/11/6	38	R77	0 ohm change to short pad	it's for NPI debug			v
8	2018/11/6	16	R301	0 ohm change to short pad	it's for power consumption			v
9	2018/11/6	6	RC34	0 ohm change to short pad	it's for power consumption			v
10	2018/11/6	6	RC35	0 ohm change to short pad	it's for NPI debug			v
11	2018/11/6	7	RC42	0 ohm change to short pad	it's for NPI debug			v
12	2018/11/6	13	RC126	0 ohm change to short pad	it's for power consumption			v
13	2018/11/6	13	RC127	0 ohm change to short pad	it's for power consumption			v
14	2018/11/6	13	RC128	0 ohm change to short pad	it's for power consumption			v
15	2018/11/6	13	RC129	0 ohm change to short pad	it's for power consumption			v
16	2018/11/6	13	RC130	0 ohm change to short pad	it's for power consumption			v
17	2018/11/6	13	RC131	0 ohm change to short pad	it's for power consumption			v
18	2018/11/6	13	RC132	0 ohm change to short pad	it's for power consumption			v
19	2018/11/6	13	RC133	0 ohm change to short pad	it's for power consumption			v
20	2018/11/6	13	RC134	0 ohm change to short pad	it's for power consumption			v
21	2018/11/6	13	RC135	0 ohm change to short pad	it's for power consumption			v
22	2018/11/6	13	RC136	0 ohm change to short pad	it's for power consumption			v
23	2018/11/6	12	RC1143	0 ohm change to short pad	it's for NPI debug			v
24	2018/11/6	6	RC1149	0 ohm change to short pad	it's for NPI debug			v
25	2018/11/6	15	RD4	0 ohm change to short pad	it's for NPI debug			v
26	2018/11/6	15	RD5	0 ohm change to short pad	it's for NPI debug			v
27	2018/11/6	15	RD6	0 ohm change to short pad	it's for NPI debug			v
28	2018/11/6	20	RA1	0 ohm change to short pad	it's for power consumption			v
29	2018/11/6	20	RA33	0 ohm change to short pad	it's for power consumption			v
30	2018/11/6	20	RA34	0 ohm change to short pad	it's for power consumption			v
31	2018/11/6	20	RA35	0 ohm change to short pad	it's for power consumption			v
32	2018/11/6	20	RA36	0 ohm change to short pad	it's for power consumption			v
33	2018/11/6	20	RA62	0 ohm change to short pad	it's for power consumption			v
34	2018/11/6	20	RA65	0 ohm change to short pad	it's for NPI debug			v
35	2018/11/6	22	RE5	0 ohm change to short pad	it's for NPI debug			v
36	2018/11/6	22	RE19	0 ohm change to short pad	it's for NPI debug			v
37	2018/11/6	22	RE20	0 ohm change to short pad	it's for NPI debug			v
38	2018/11/6	22	RE42	0 ohm change to short pad	it's for NPI debug			v
39	2018/11/6	18	RW25	0 ohm change to short pad	it's for NPI debug			v
40	2018/11/6	19	RL5	0 ohm change to short pad	it's for NPI debug			v
41	2018/11/6	19	RL13	0 ohm change to short pad	it's for NPI debug			v
42	2018/11/6		R17,R18,L4,RU18,RU21,LU7,LU12,RU19,RU24,LU11,LU8,LI1,LI2,LI3,LI4	Co-lay function add solder mask	DFX requirement			v
43	2018/11/8	24	RS61	change to "@"	not support devslp function		v	

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Title: Changed-List PWR History

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