LCFC Confidential

GS454/GS554 NM-D031 MB

Schematics Document

ICL U42 With DDR4+

Nvidia N16V-GM

2019-10

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Cover Page		
Size: C	Document Number: GS44D/GS54D	Rev: 0.1
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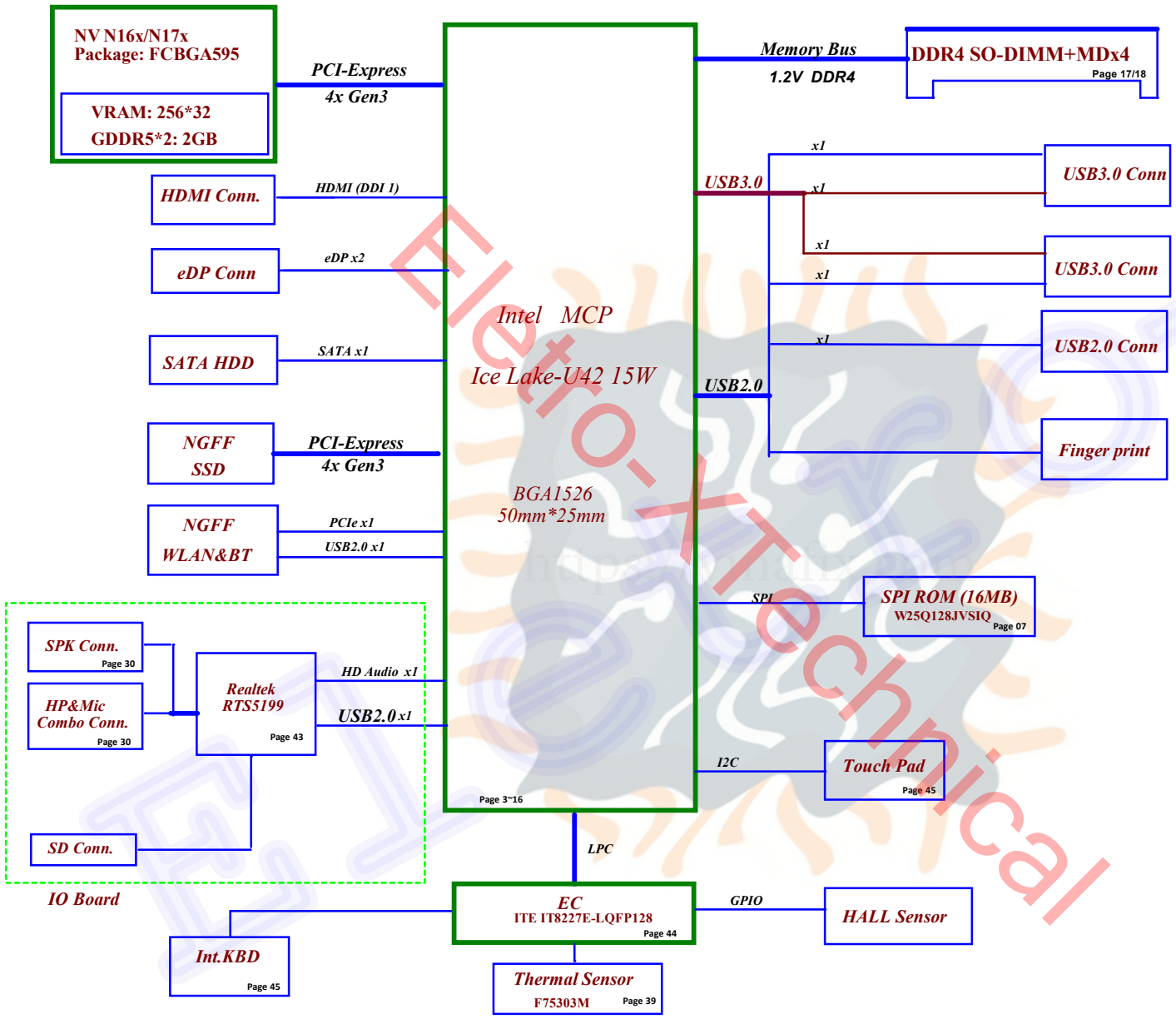

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Block Diagram

Size	Document Number	Rev
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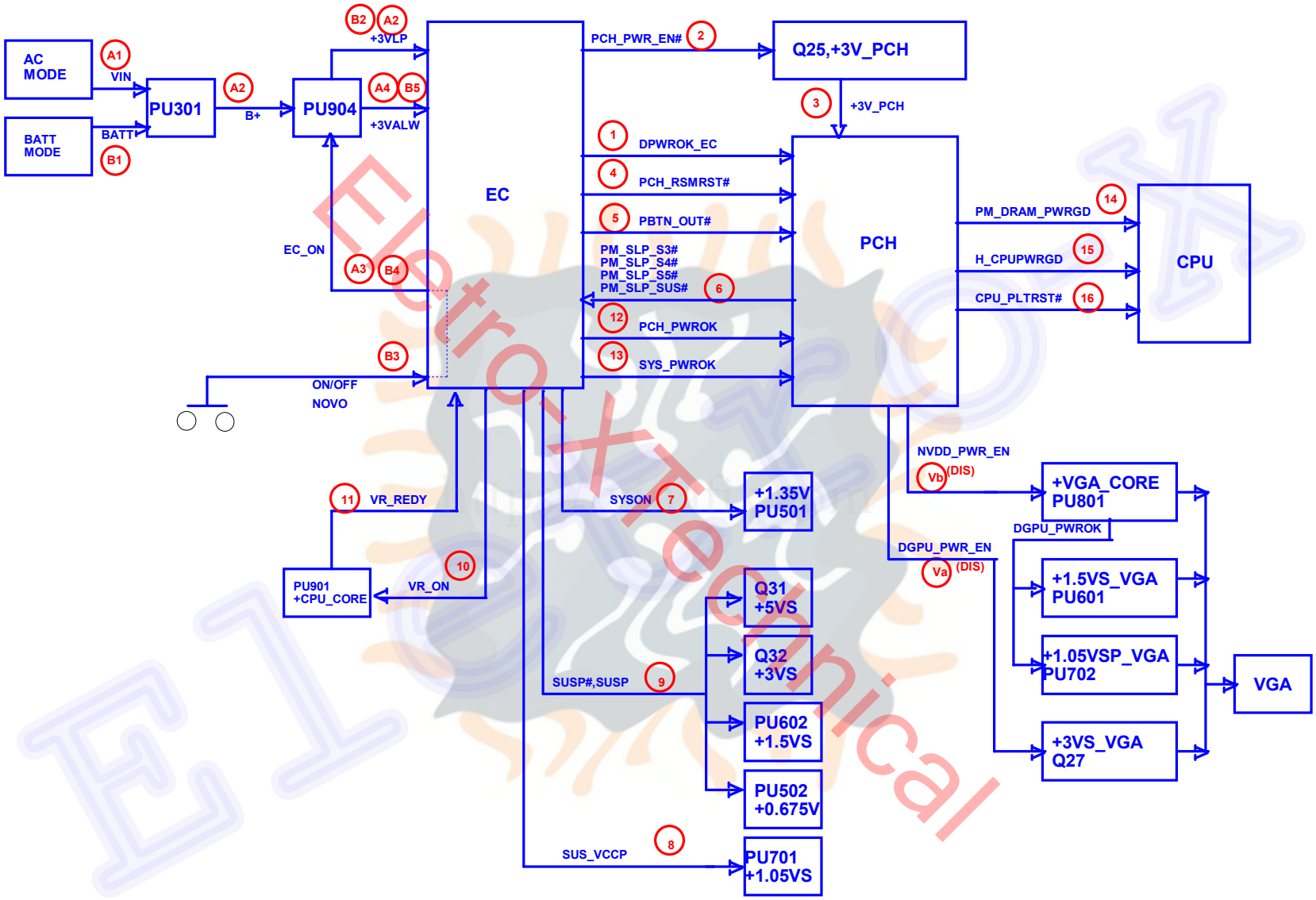

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: *Power sequence block*

Size: Custom	Document Number: GS44D/GS54D	Rev: 1.0
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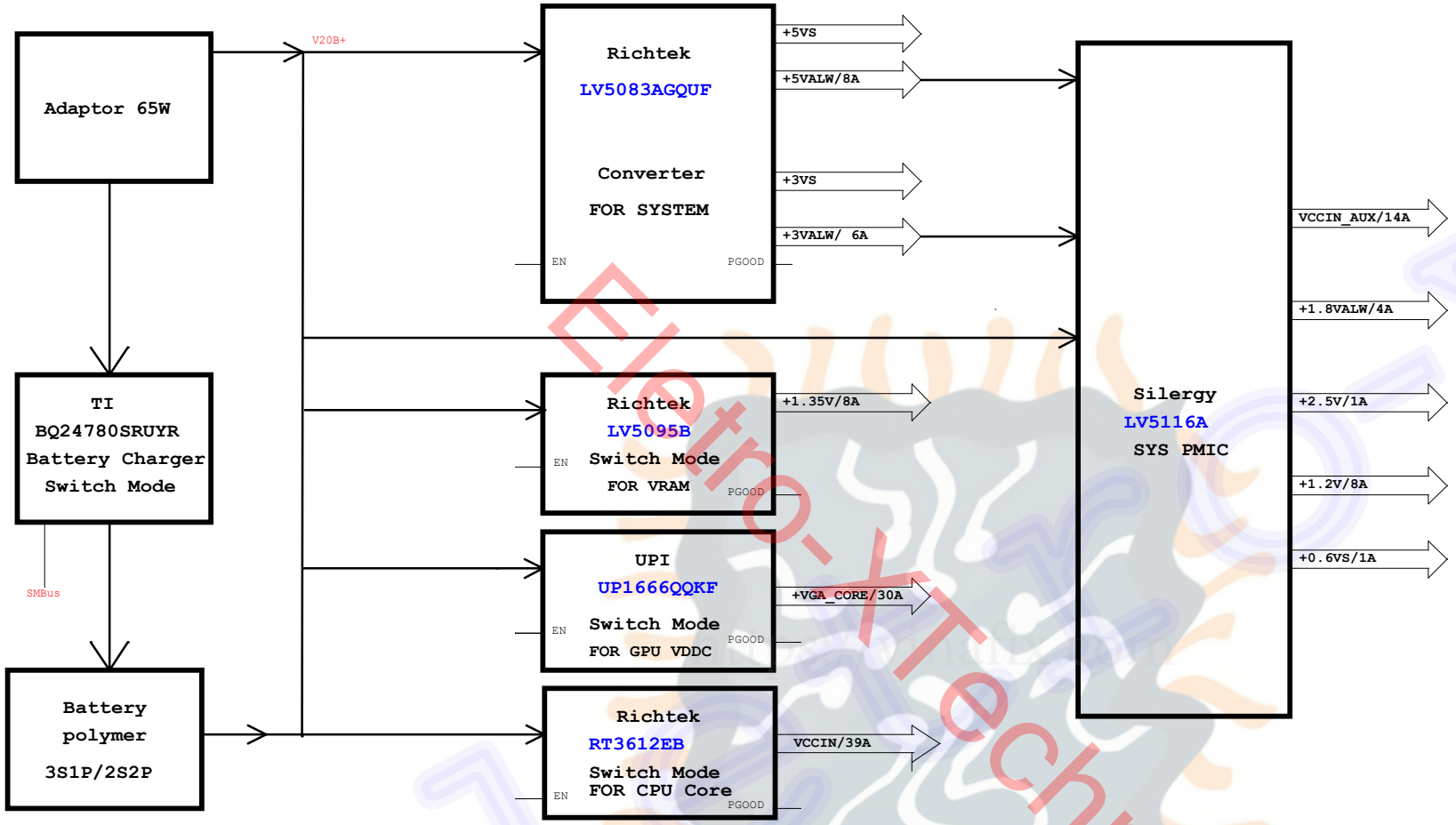

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-Power Diagram

Size	Document Number	Rev
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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ Power Plane	V9B+	+3VALW +5VALW +3VALW_PCH +1.8VALW VCC_AUX	+1.2V +2.5V_DDR +VCCST +VCCSTG	+5VS +3VS +1.8VS +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	
	6	
USB2.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	Camere
	6	Touch Screen
	7	Finger Print
	8	Card Reader
	9	USB2.0 conn
	10	Bluetooth
PCIE	5~8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13~16 X4	PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
CD@	For cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME part
UMA@	For UMA part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOuch Pad Part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8227E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8227E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8227E +3VS	X	X	V +3VG_AON	V +3VS	X	X	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8227E +3VAWL	X	X	X	V	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	X

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update

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Title: **Notes List**

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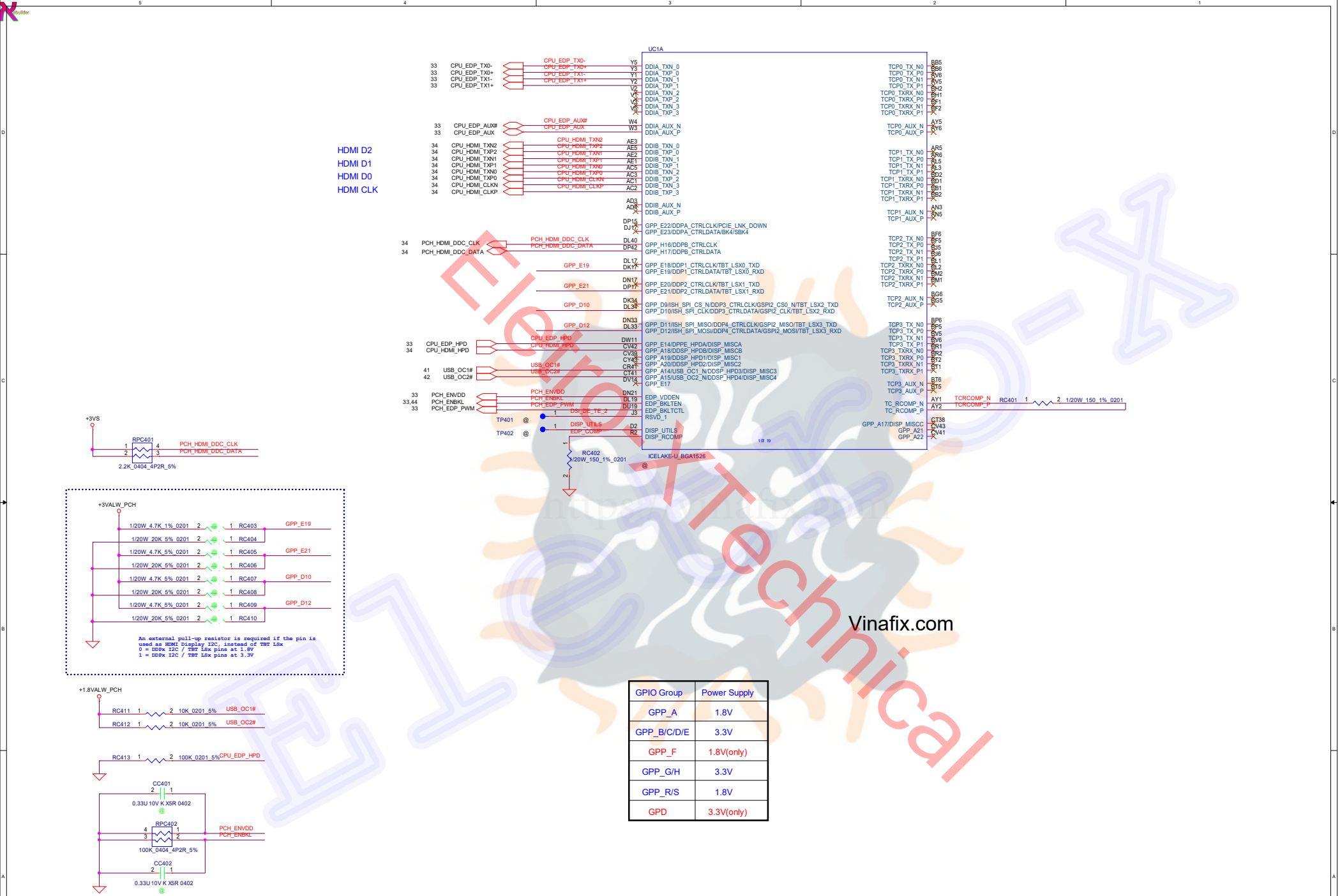

GPIO Group	Power Supply
GPP_A	1.8V
GPP_B/C/D/E	3.3V
GPP_F	1.8V(only)
GPP_G/H	3.3V
GPP_R/S	1.8V
GPD	3.3V(only)

Security Classification	LC Future Center Secret Data		
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Title			
S740-ICL			
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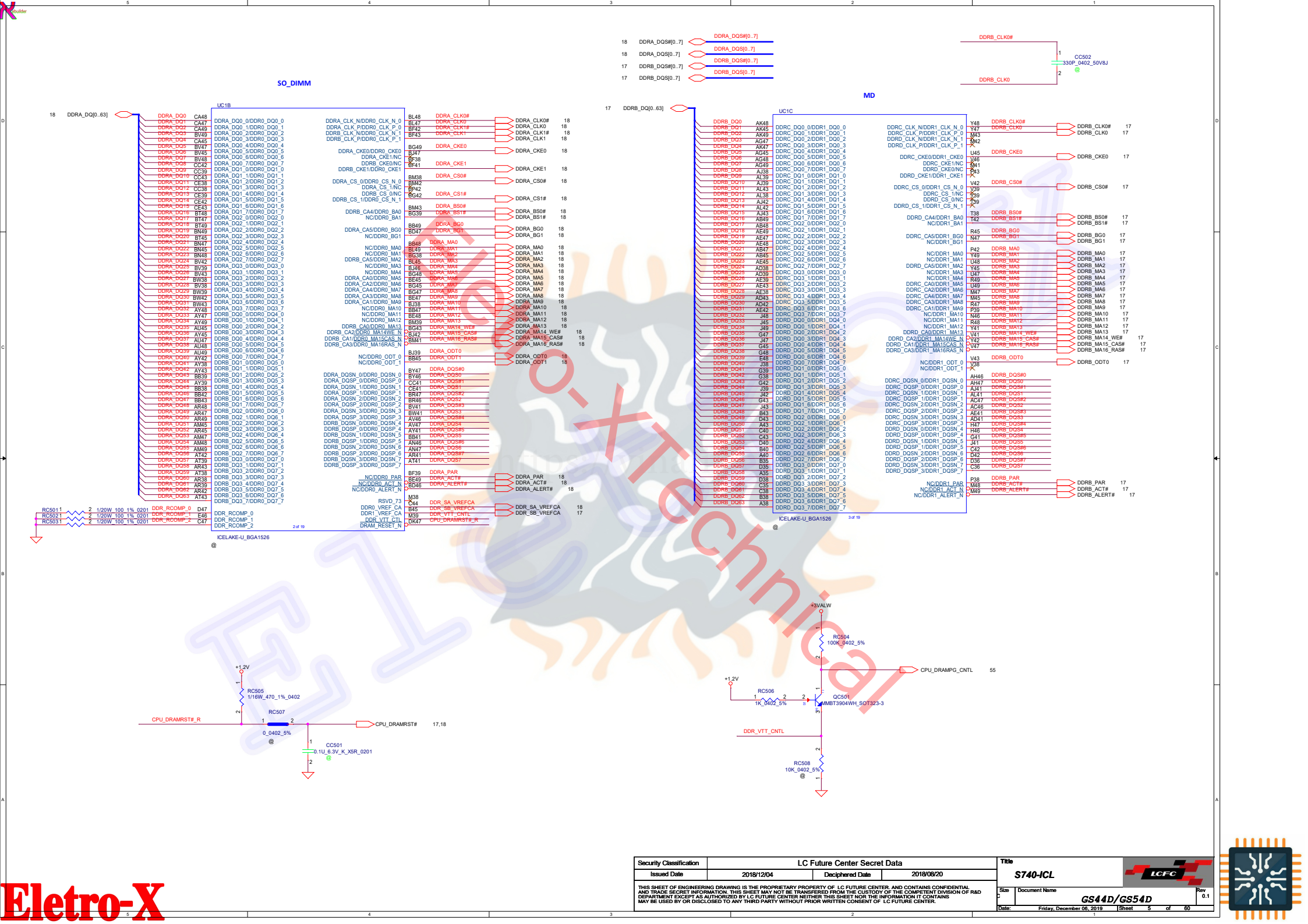

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Issued Date	2018/12/04	Deciphered Date	2019/08/20

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S740-ICL			
Size	Document Name		Rev
C	GS44D/GS54D		0.1
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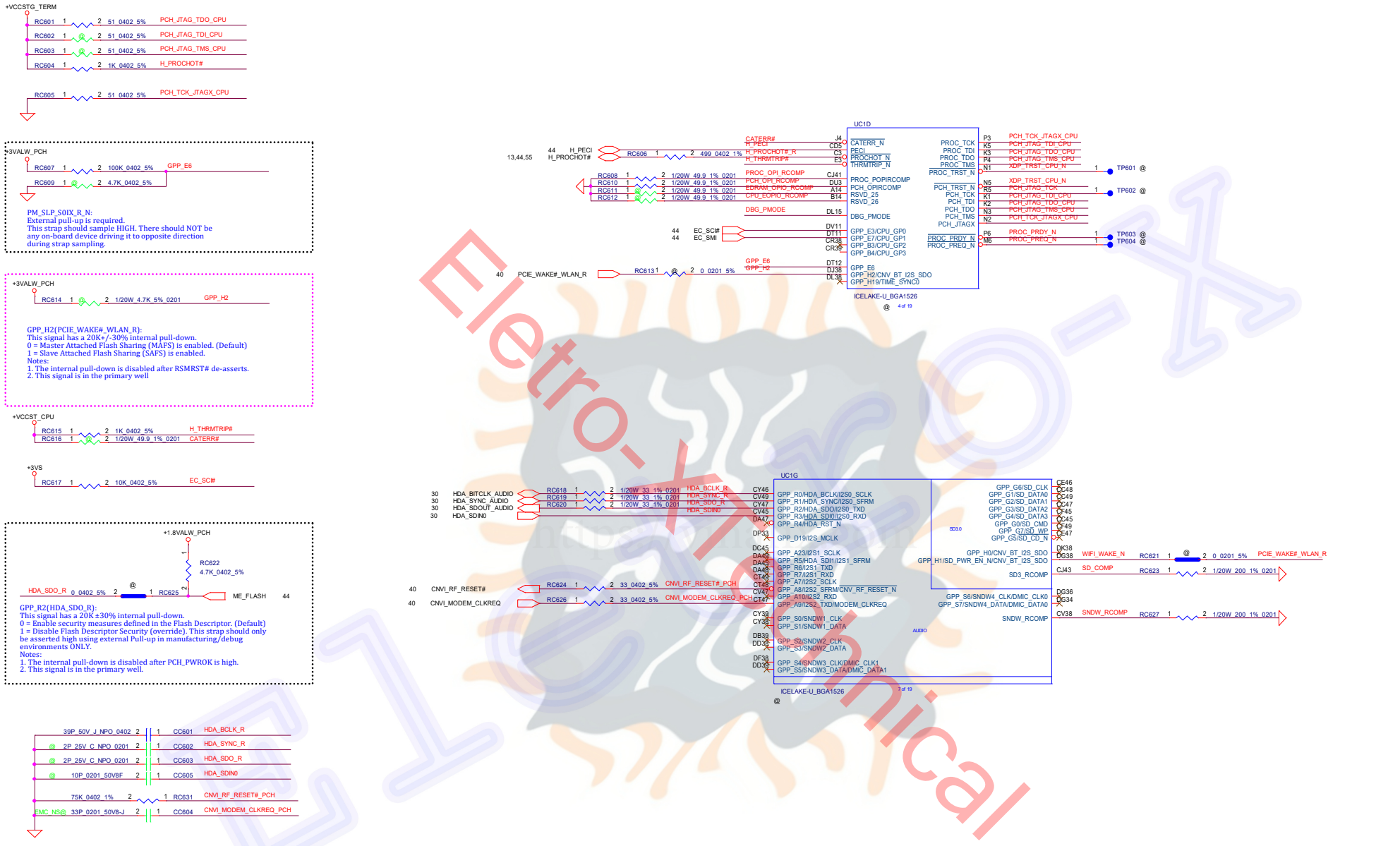

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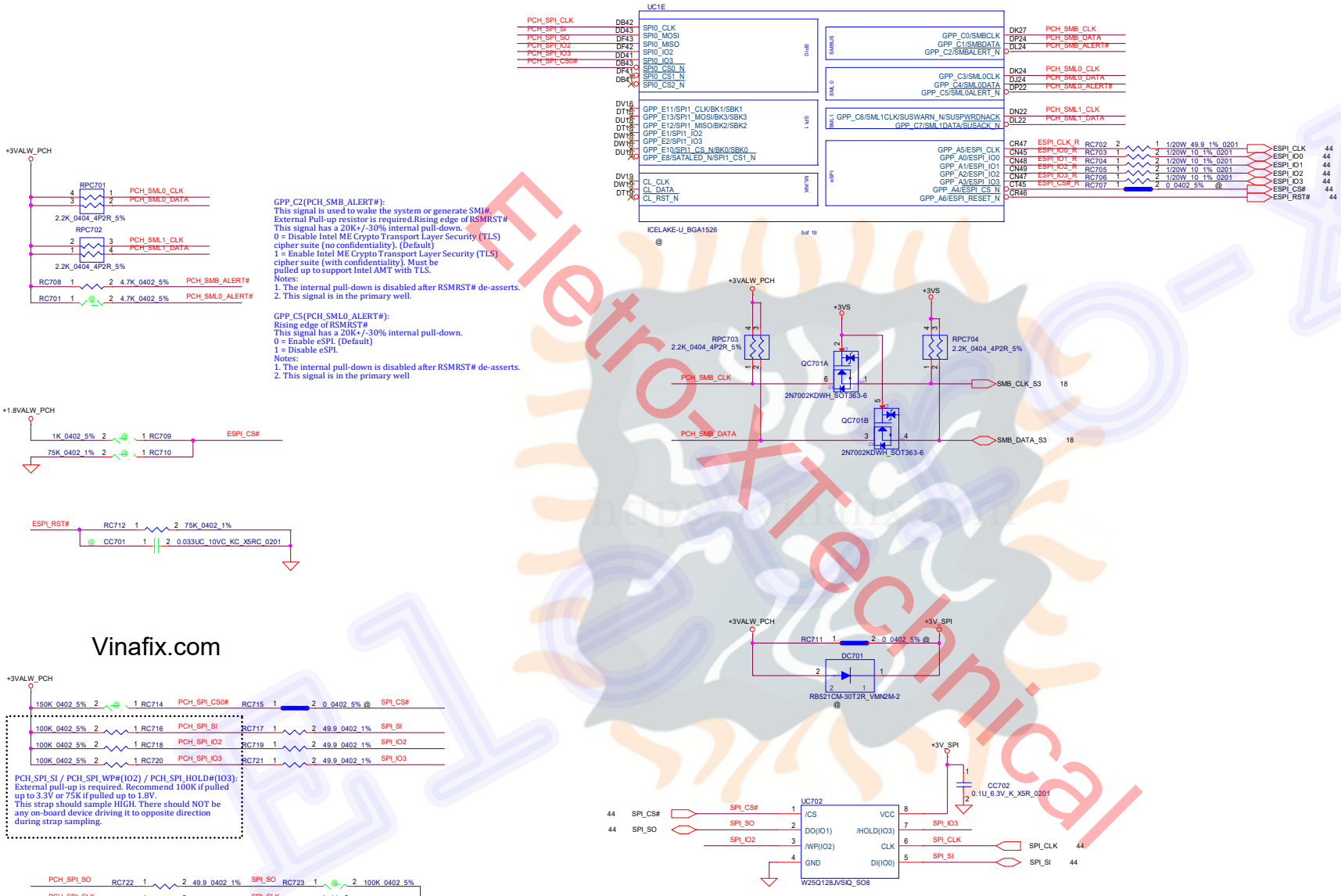

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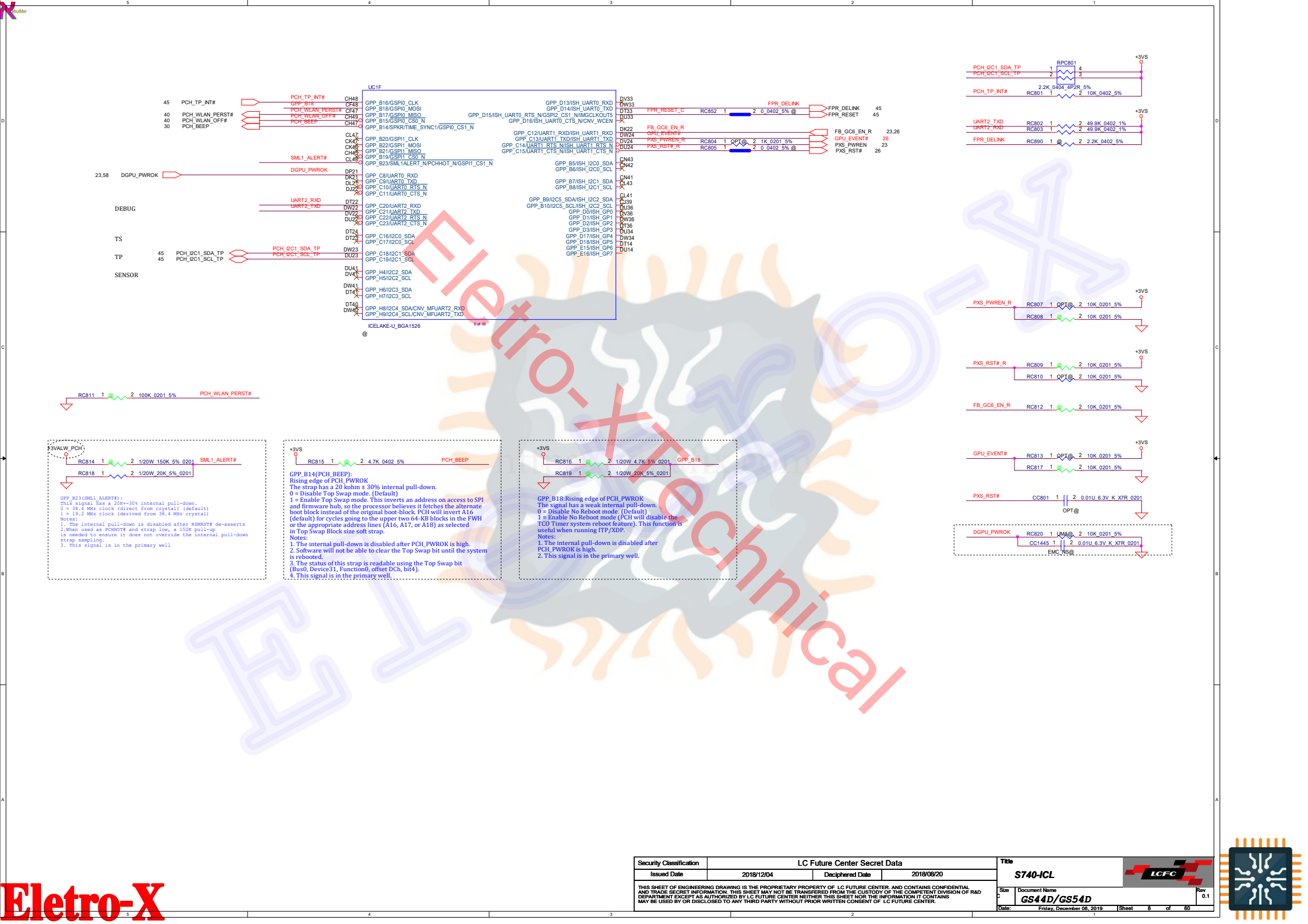

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Title	S740-ICL		
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D	GS44D/GS54D		0.1
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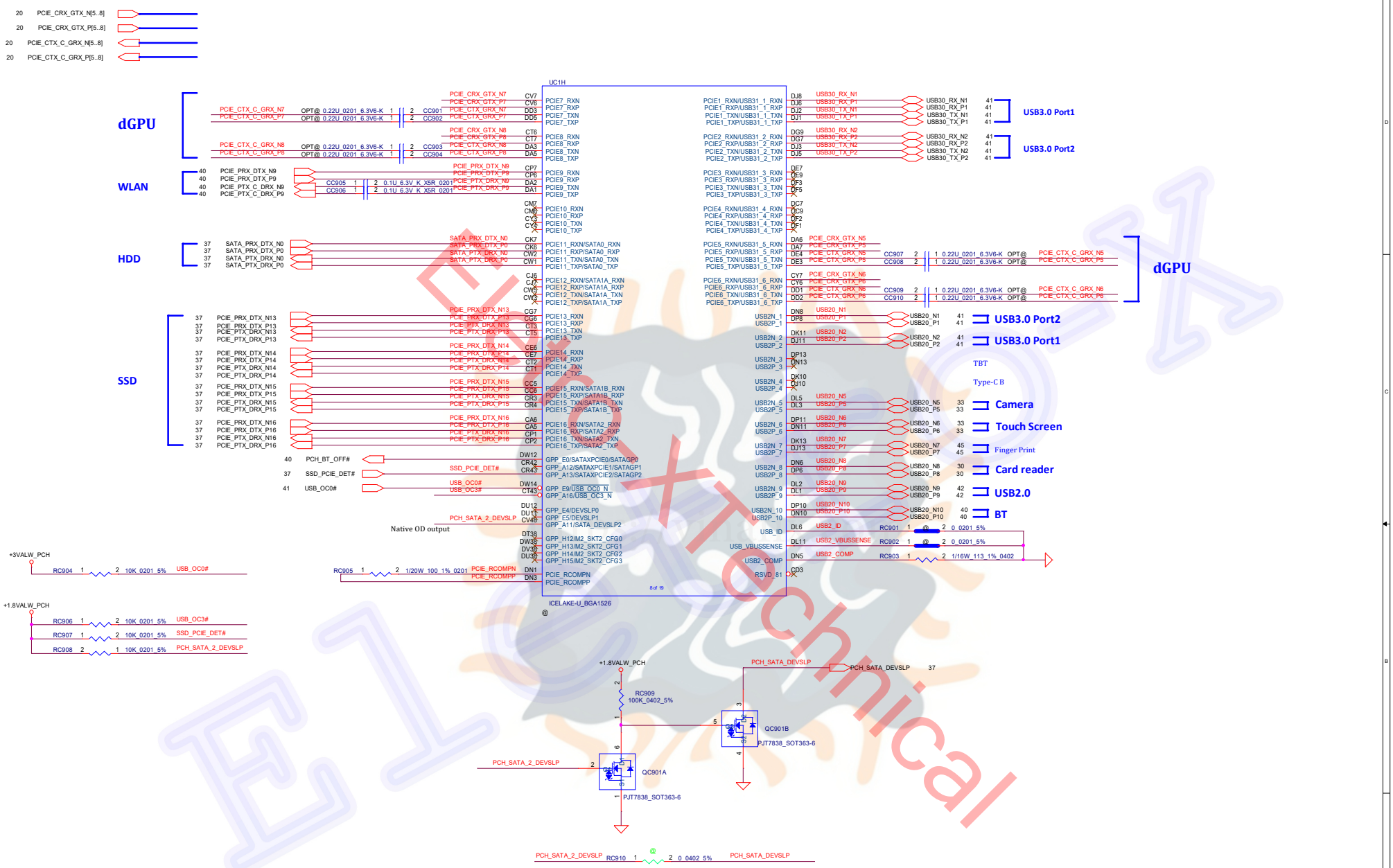

1. DEVSLP is an open-drain pin on the PCH side and is not required external pull-up orpull-down. The PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATAdevice, per DEVSLP specification). PCH will drive pin low to signal an exit fromDEVSLP state.
2. DEVSLP is supported in direct connect, mSATA/mPCIe, uSSD, M.2.
3. 1 DEVSLP pin is required to support EACH DEVSLP enabled RAID storage device.
(Example: 2 DEVSLP pins are required to support 2 DEVSLP RAID storage devices).

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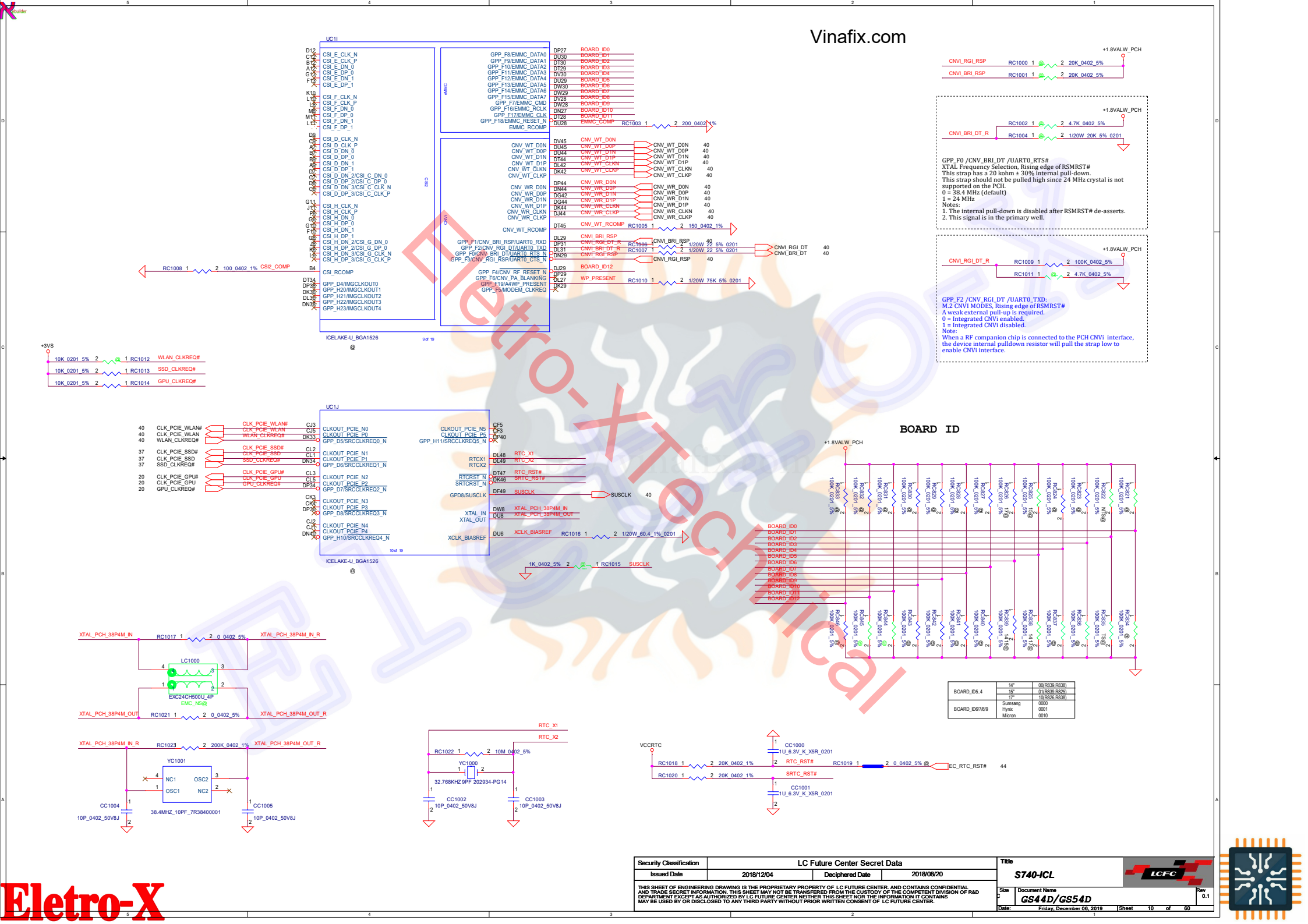

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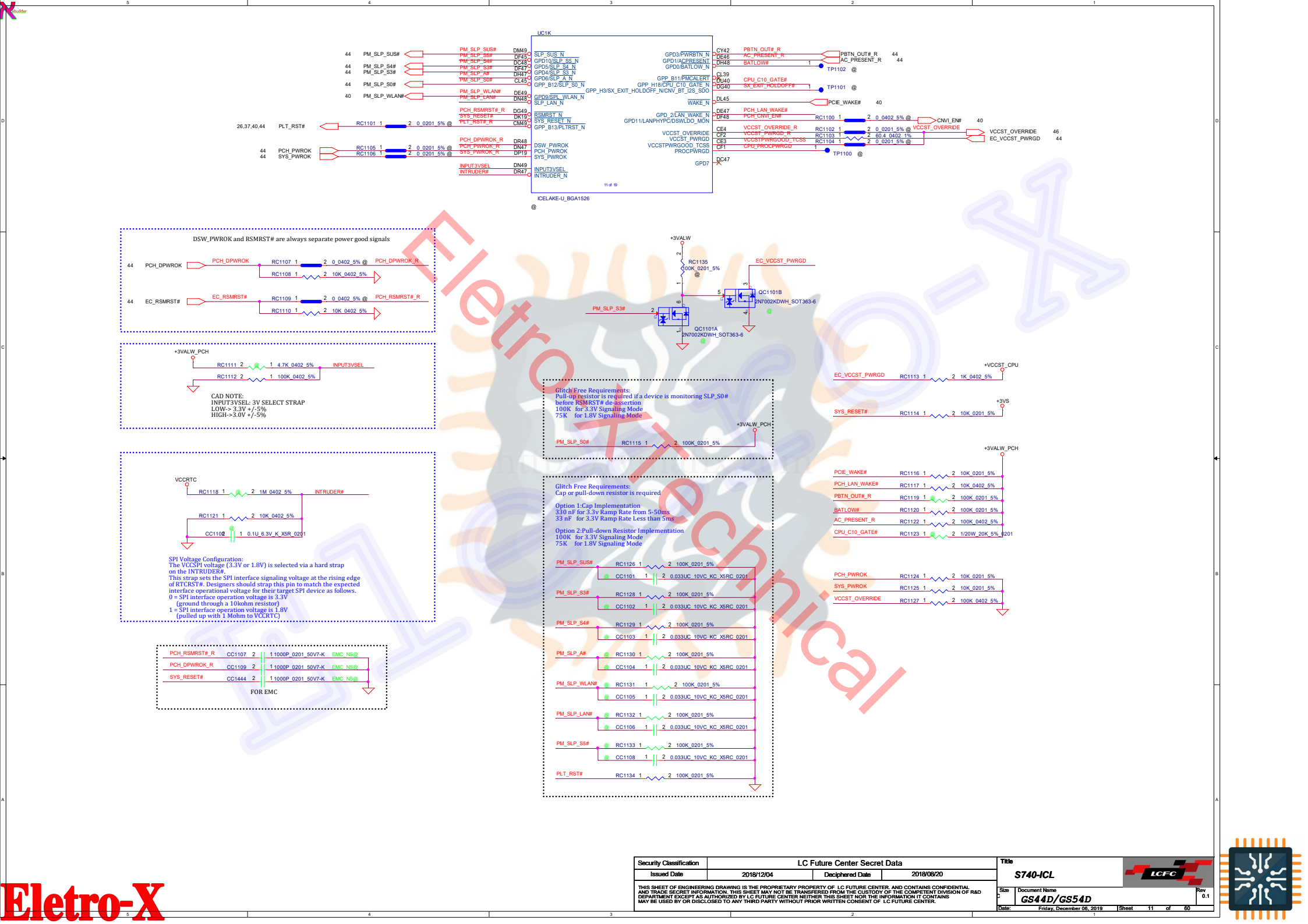

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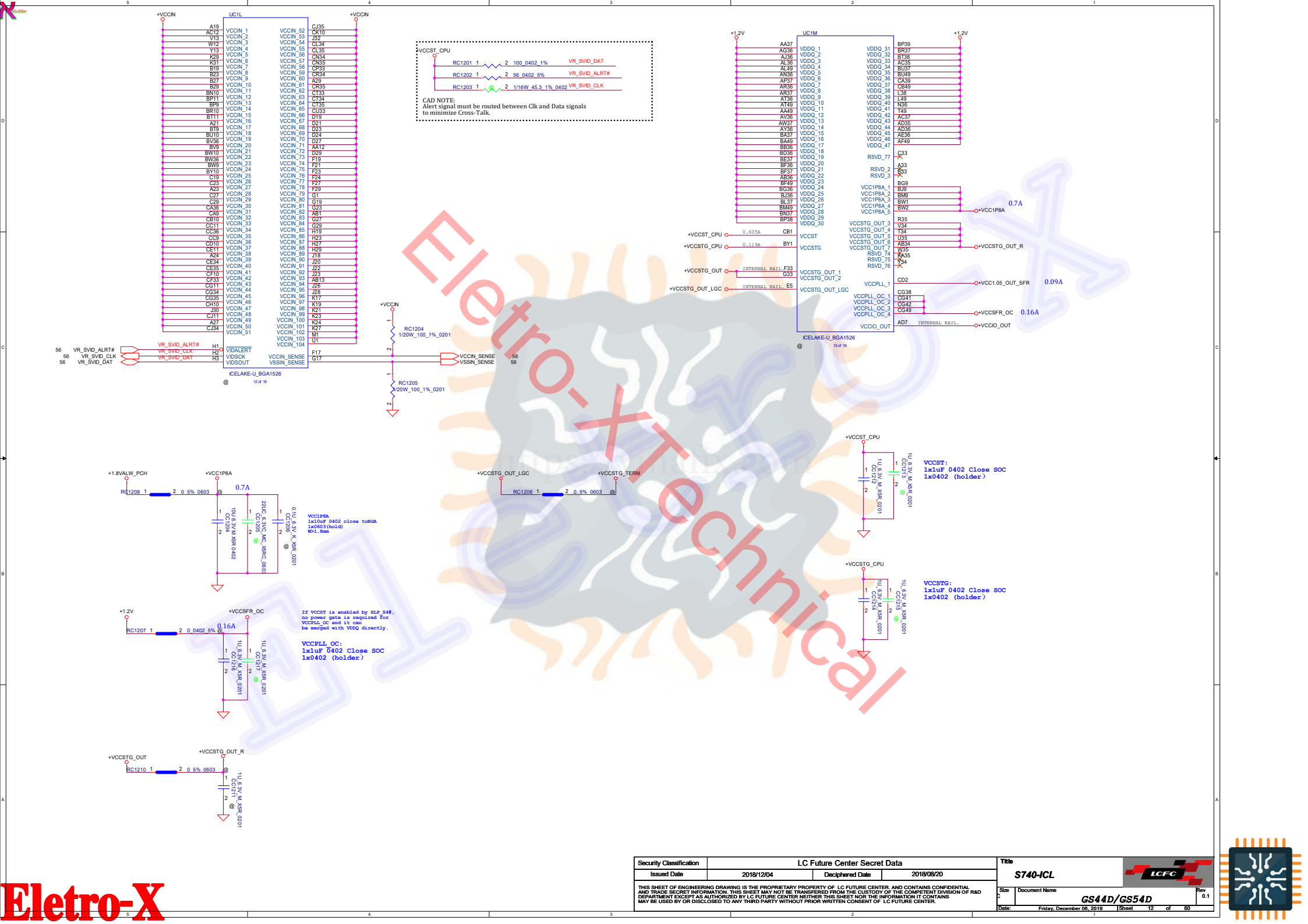

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Title	S740-ICL		
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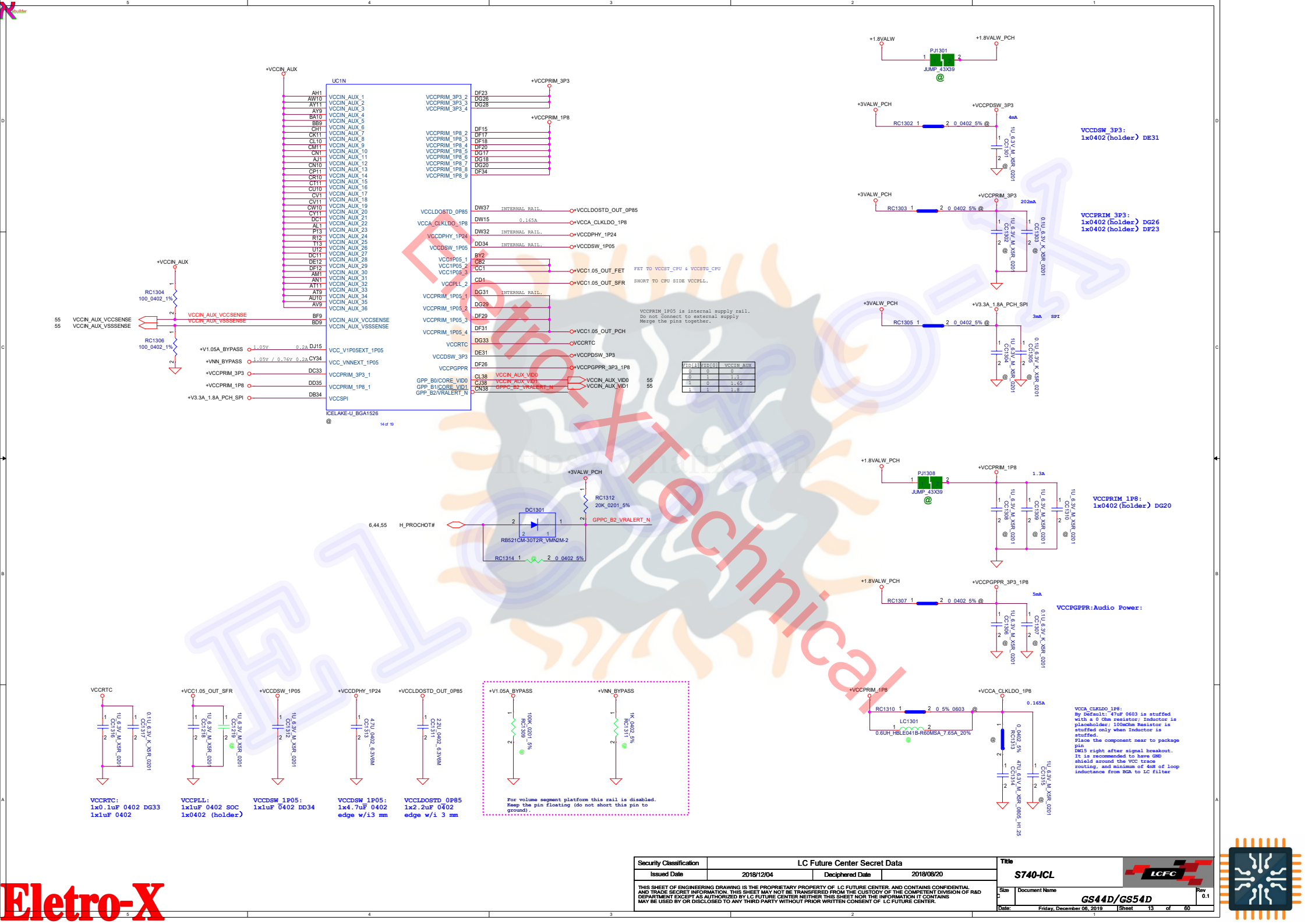

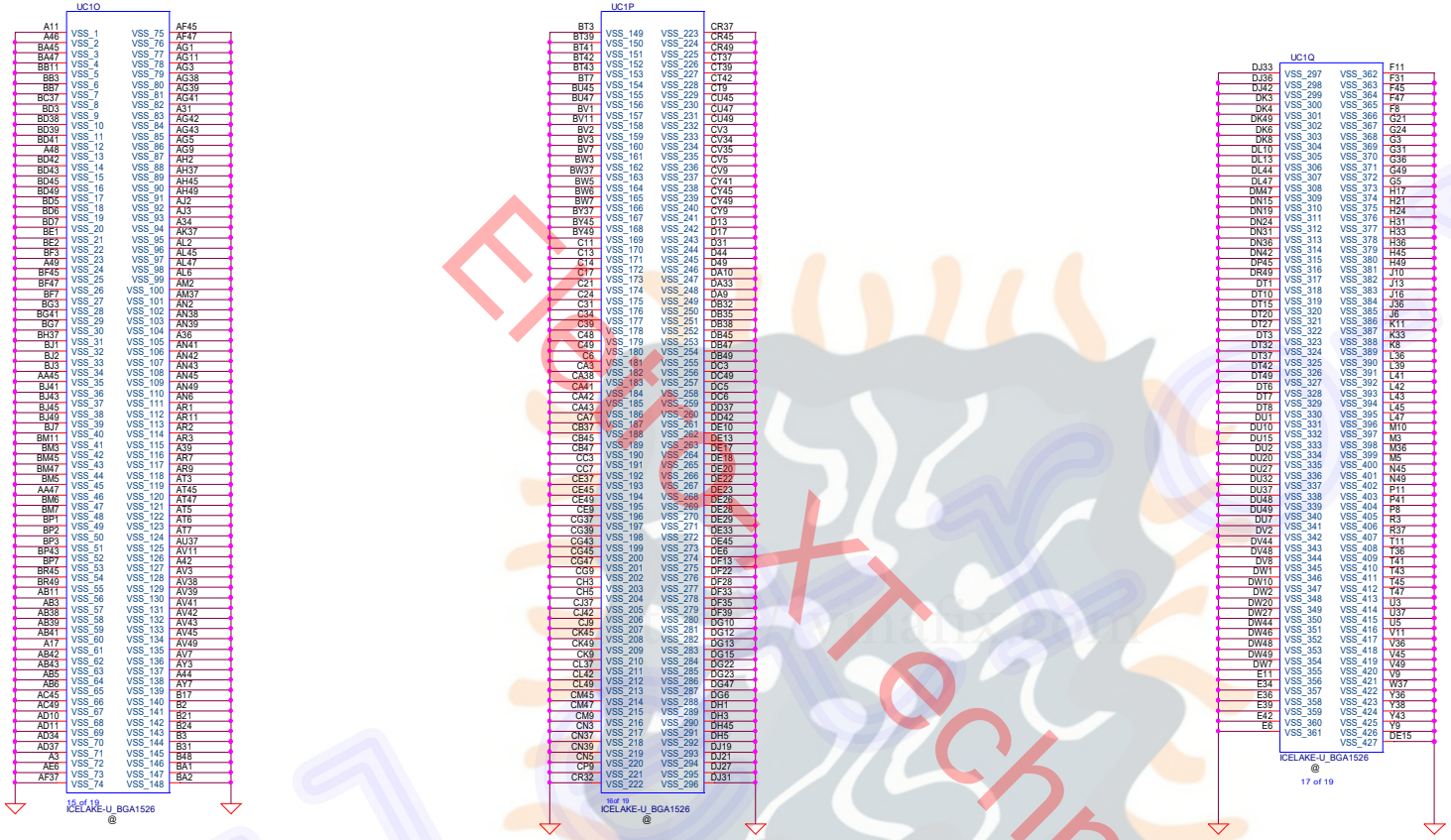

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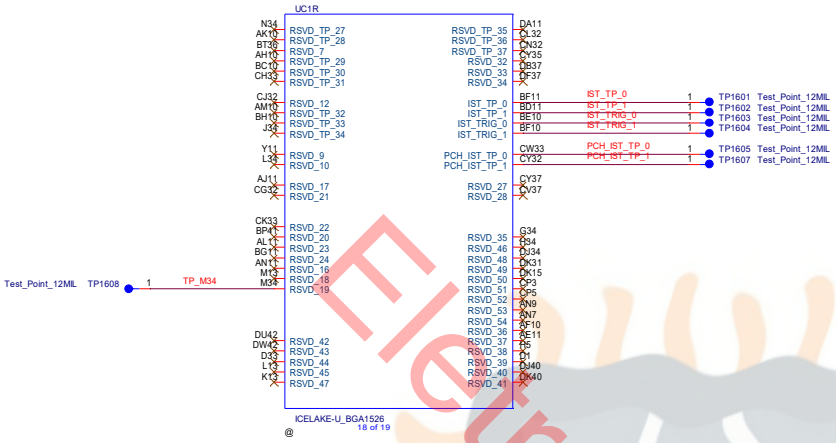
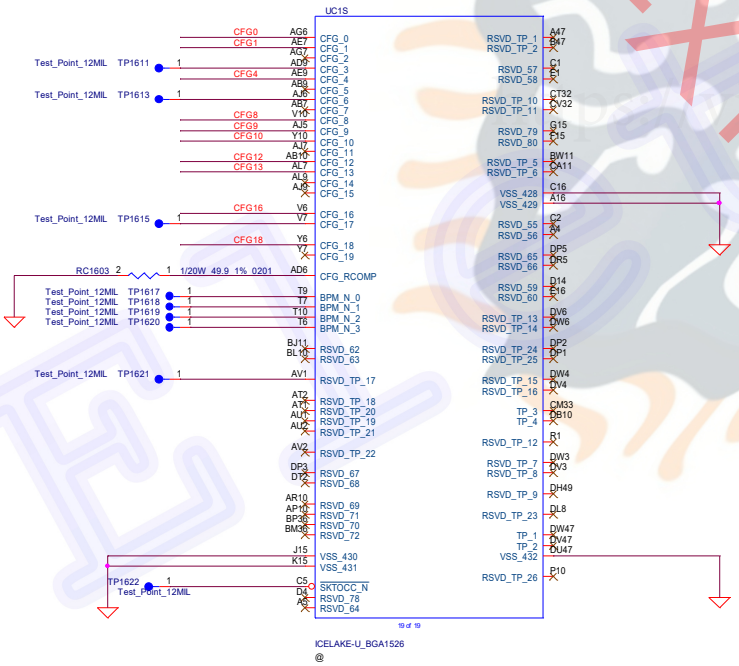
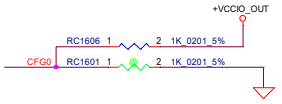


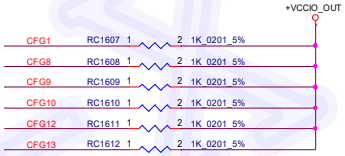


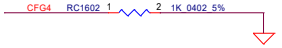
PROCESSOR CFG STRAPS



Stall reset sequence after PCU PLL lock until de-asserted

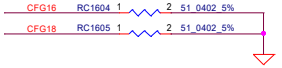
CFG0	1:Normal(Default) *
	0:Stall





Embedded Display Port Presence Strap

CFG4	1:Disable
	0:Enable(Default) *



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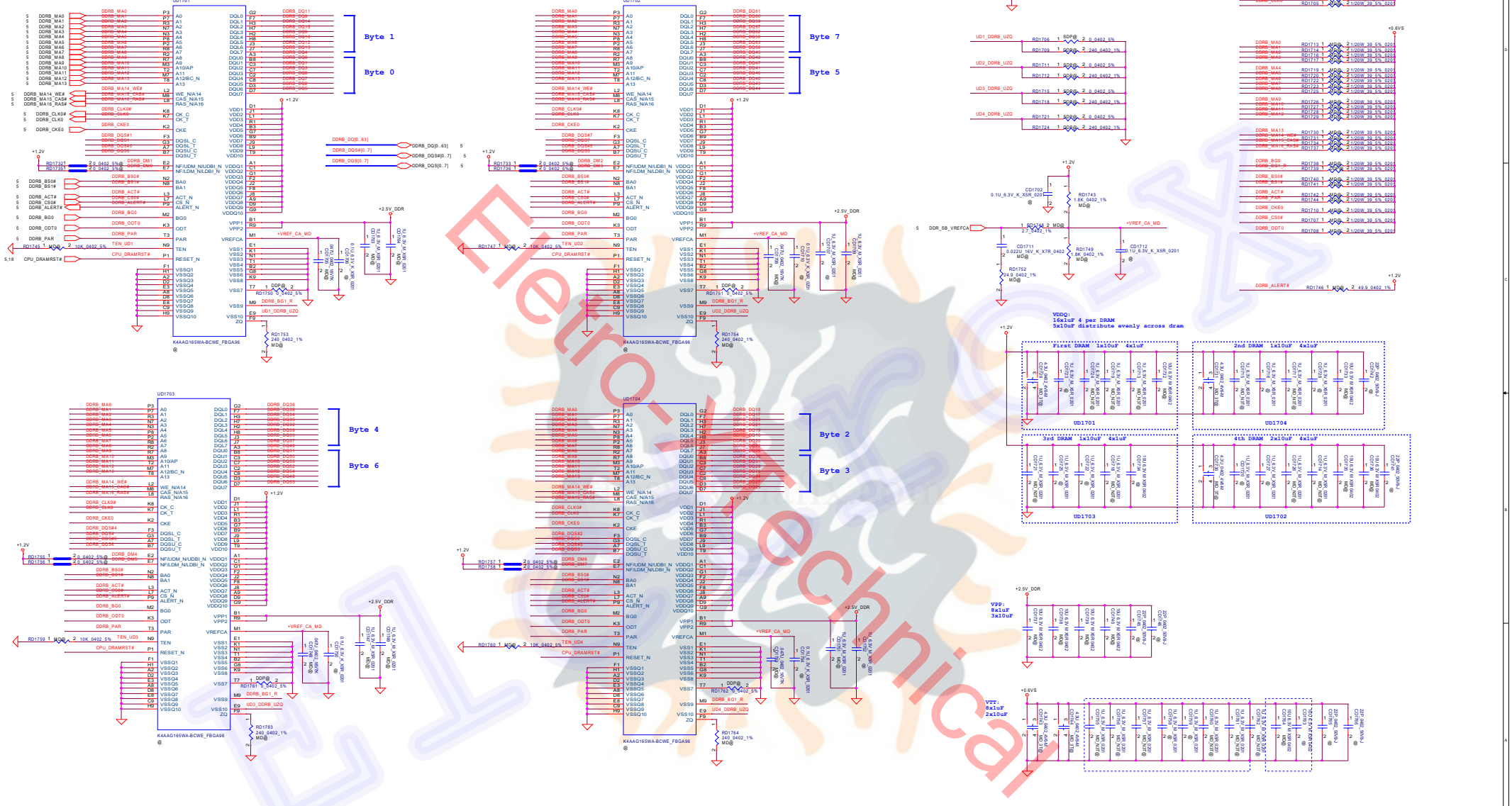
DDR4 Memory Down



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Title	DDR4 Memory Down		
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Custom		GS44D/GS54D	0.1
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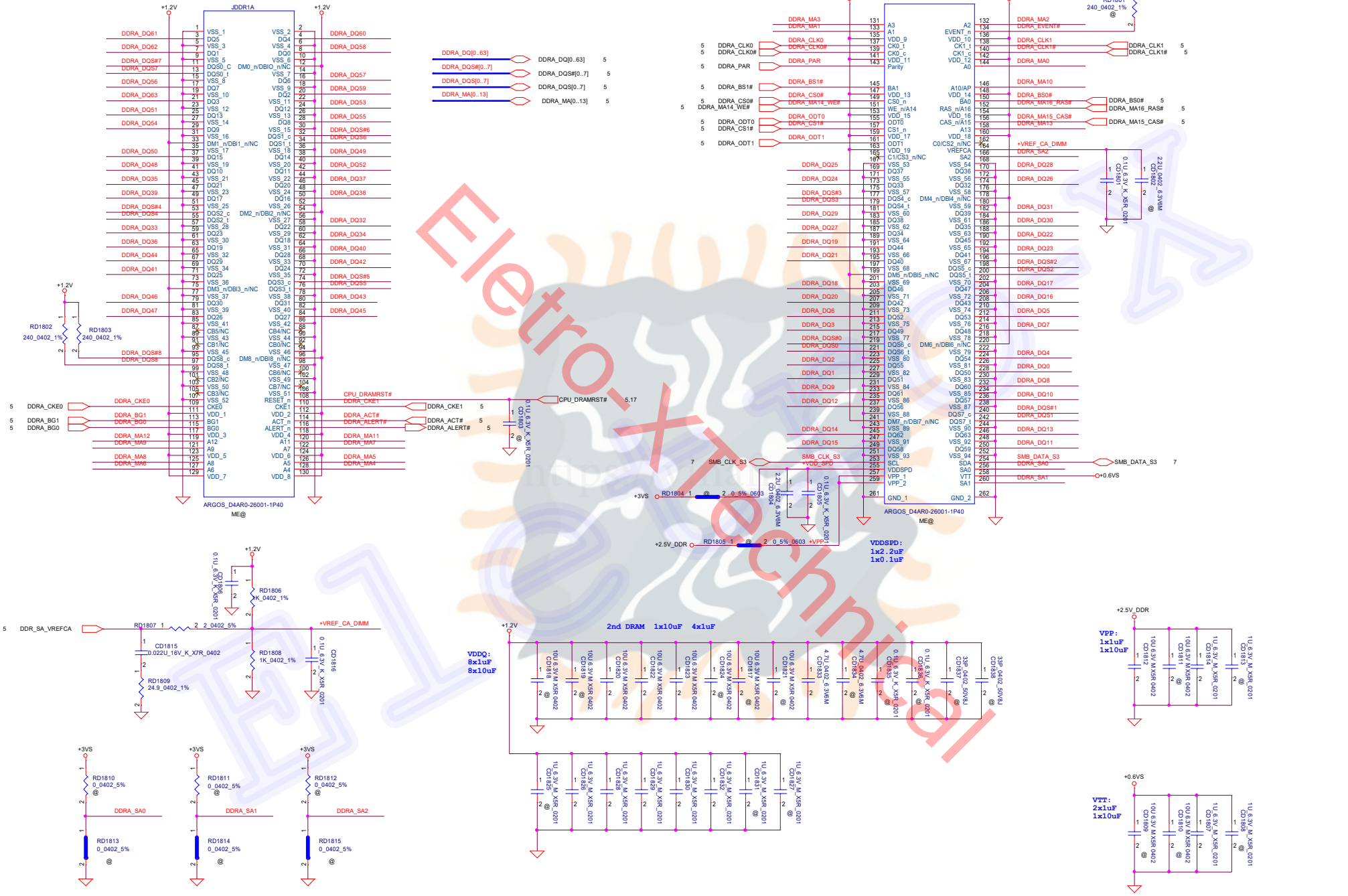
DDR4 SO-DIMM



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C	GS44D/GS54D		0.1
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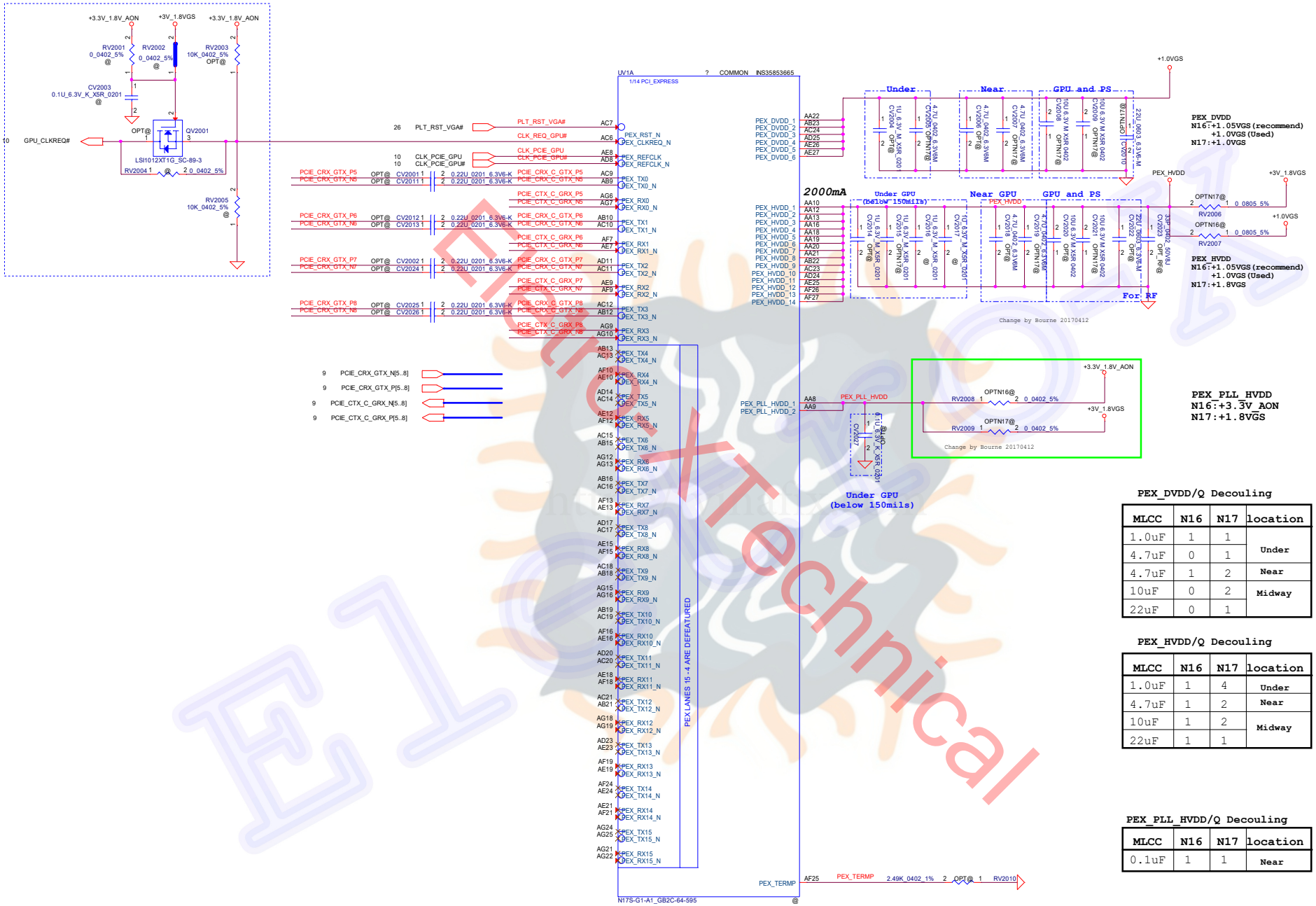

PEX_DVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	Near
10uF	0	2	Midway
22uF	0	1	

PEX_HVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

PEX_PLL_HVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Near

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_PCIE Interface

Size	Document Number	Rev
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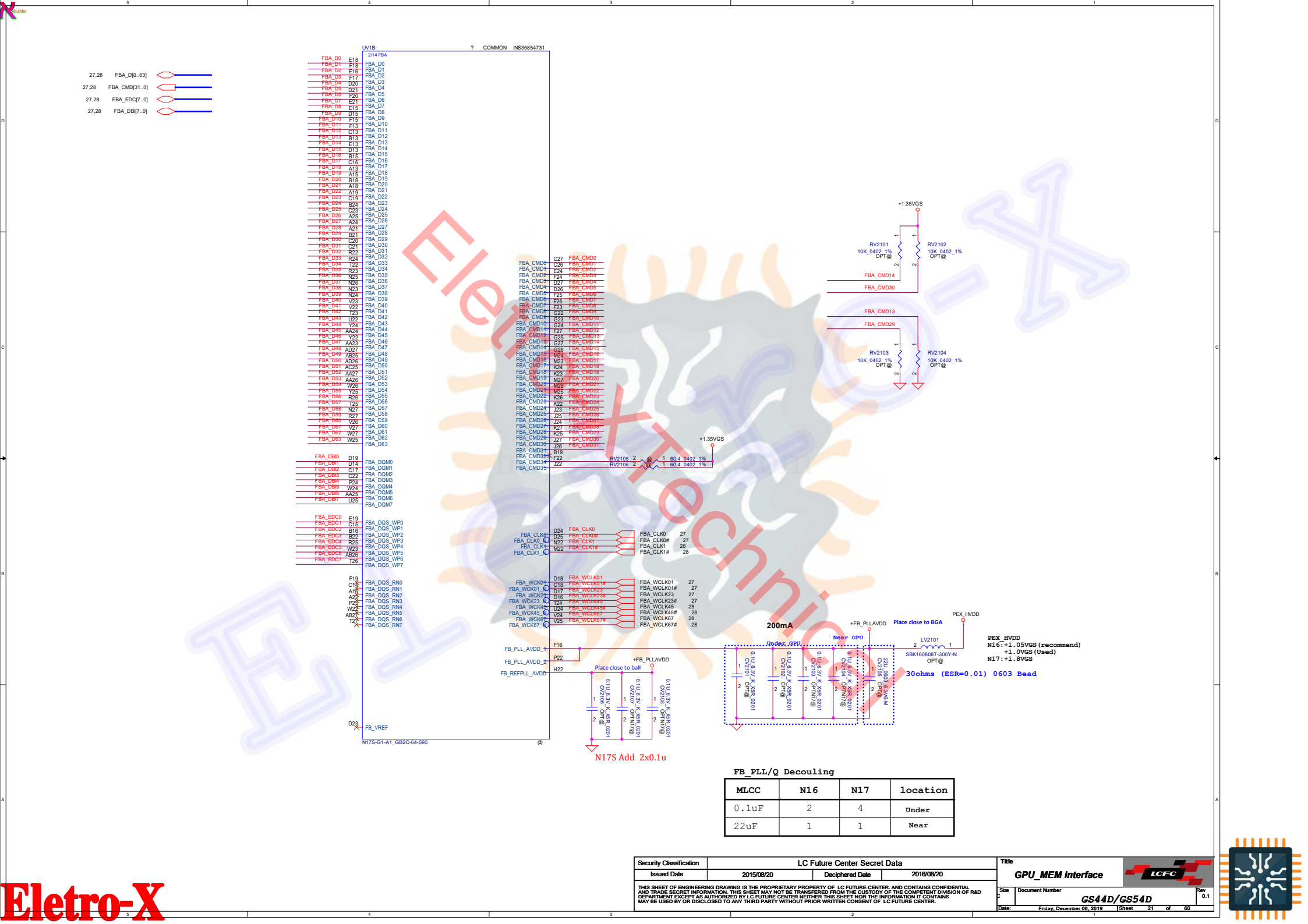

FB_PLL/Q Decouling

MLCC	N16	N17	location
0.1uF	2	4	Under
22uF	1	1	Near

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Title: GPU_MEM Interface

Size	Document Number	Rev
C	GS44D/GS54D	0.1

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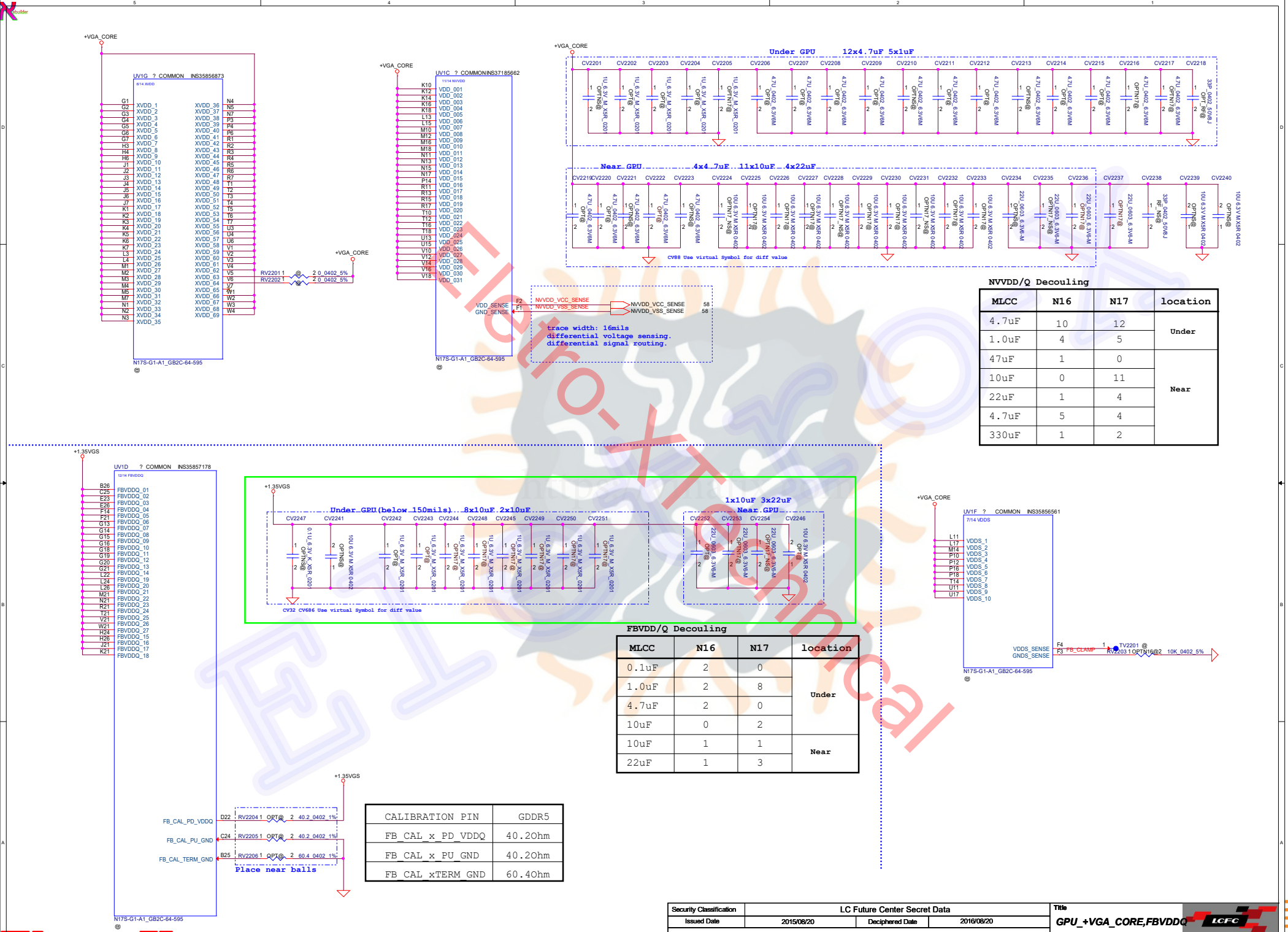

NVVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	

FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	
10uF	0	2	
10uF	1	1	Near
22uF	1	3	

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_+VGA_CORE,FBVDDQ

Size	Document Number	Rev
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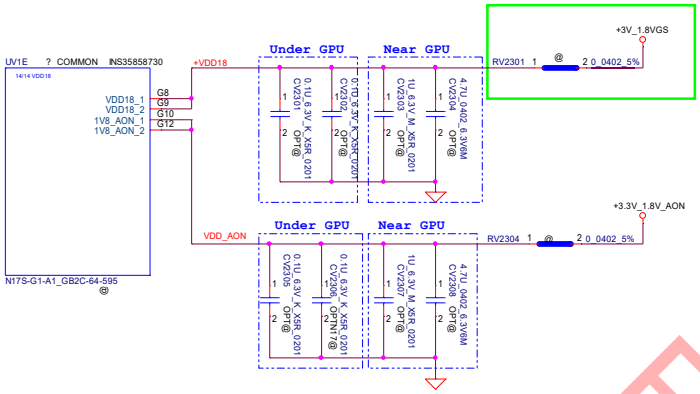
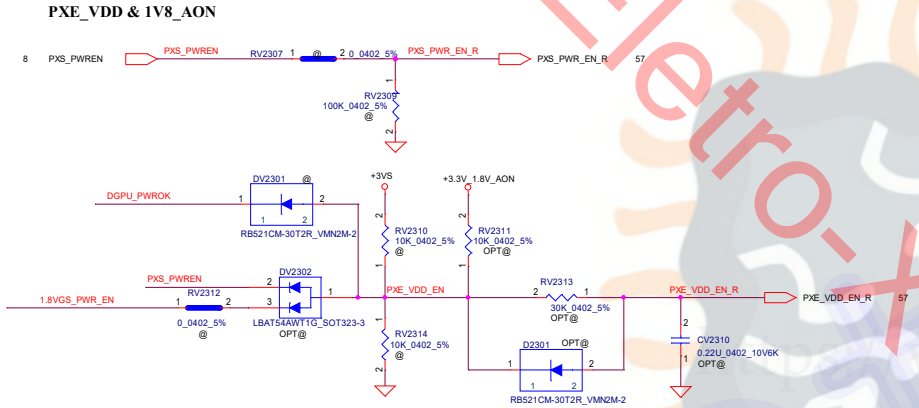
N16 3V3_MAIN(N17 VDD_18) Decouling

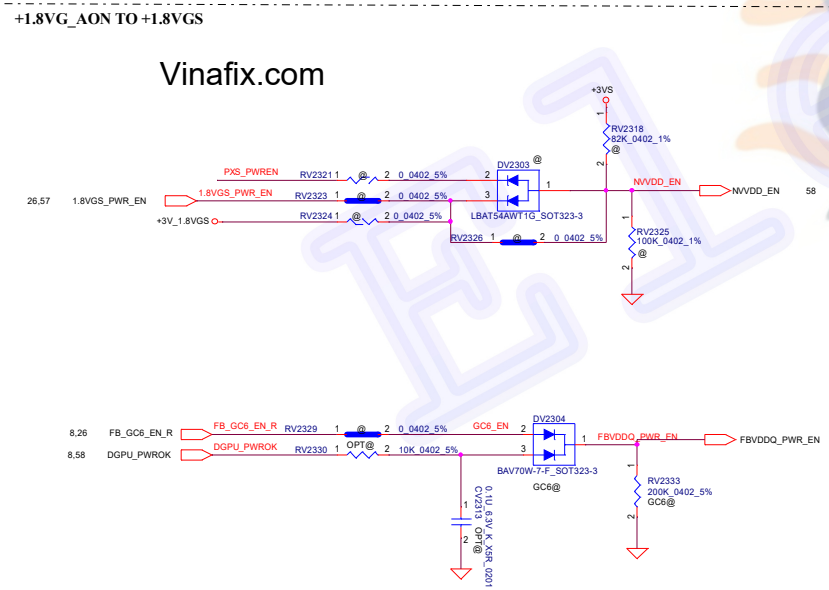
MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

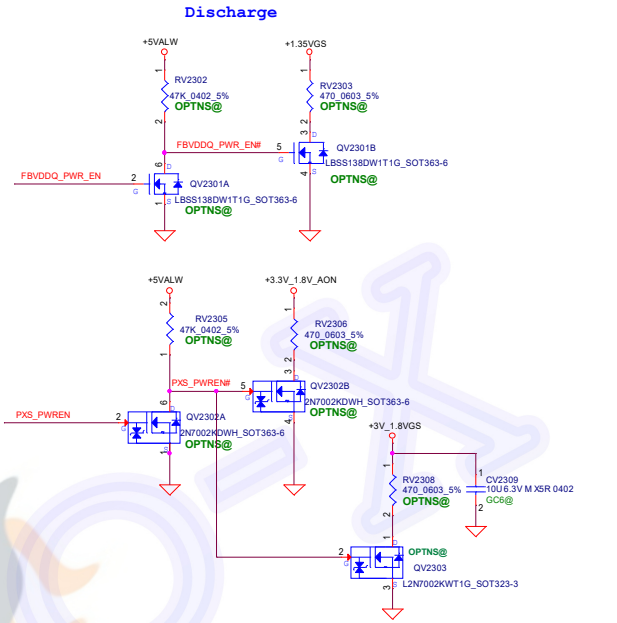
N16 3V3_AON(N17 1V8_AON) Decouling

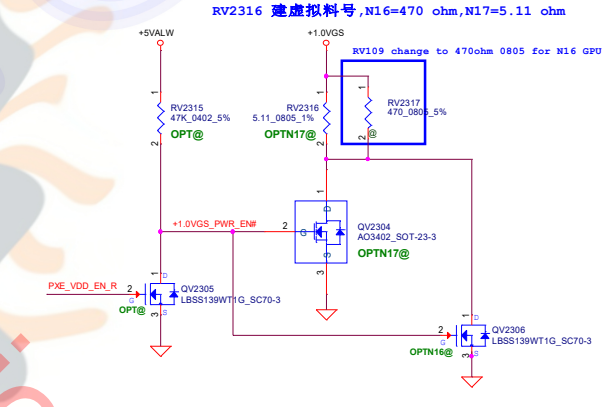
MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

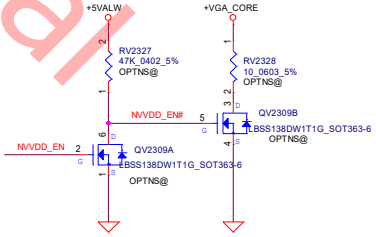






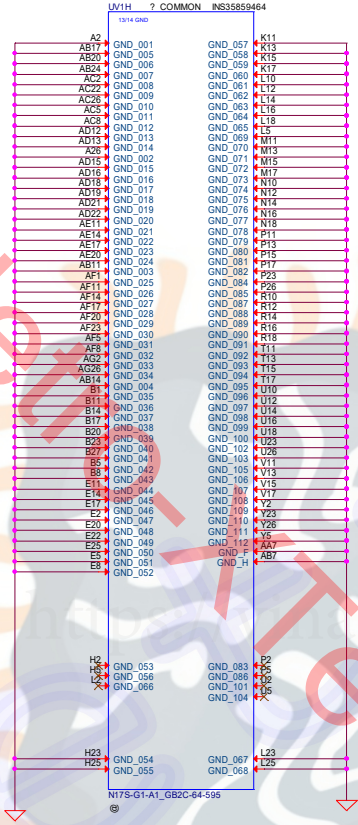






Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_AON/MAIN PWR/SEQUE		
Size C	Document Number GS44D/GS54D		Rev 0.1
Date: Friday, December 06, 2019	Sheet 23 of 60		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_GND		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
Date:	Friday, December 06, 2019	Sheet 24 of 60	

PEX_PLLVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	

PEX_PLLVDD
N16:+1.0VGS (recommend)
N17:NC

PEX_SVDD_3V3
N16:+3.3V_AON (recommend)
N17:NC

PEX_SVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	2	NA	Near

PEX_HVDD
N16:+1.05VGS (recommend)
+1.0VGS (Used)
N17:+1.8VGS

XS_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

SP_PLLVDD & VID_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

GPCPLL_AVDD/Q Decoupling

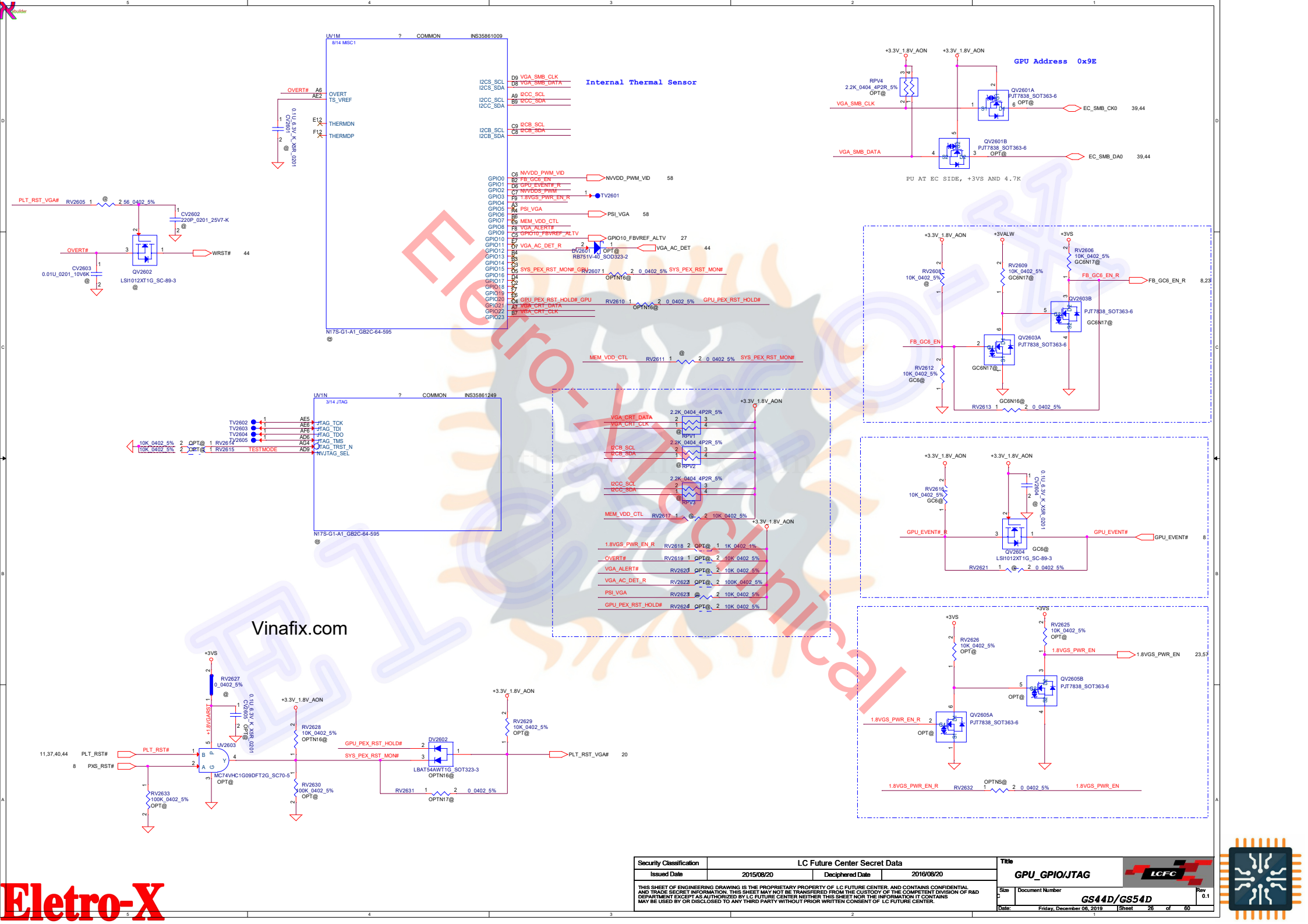
MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_STRAP/DP/HDMI

Size: C | Document Number: GS44D/GS54D | Rev: 0.1

Date: Friday, December 06, 2019 | Sheet 25 of 60


UV1M
8/14 MISC1
COMMON
INS35861009
N17S-G1-A1_GB2C-64-595
Internal Thermal Sensor
GPU Address 0x9E
PU AT EC SIDE, +3VS AND 4.7K
UV1N
3/14 JTAG
COMMON
INS35861249
N17S-G1-A1_GB2C-64-595
Vinafix.com
Eletro-X
Eletro-X Technical
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
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Title
GPU_GPIO/JTAG
Size
C
Document Number
GS44D/GS54D
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0.1
Date:
Friday, December 06, 2019
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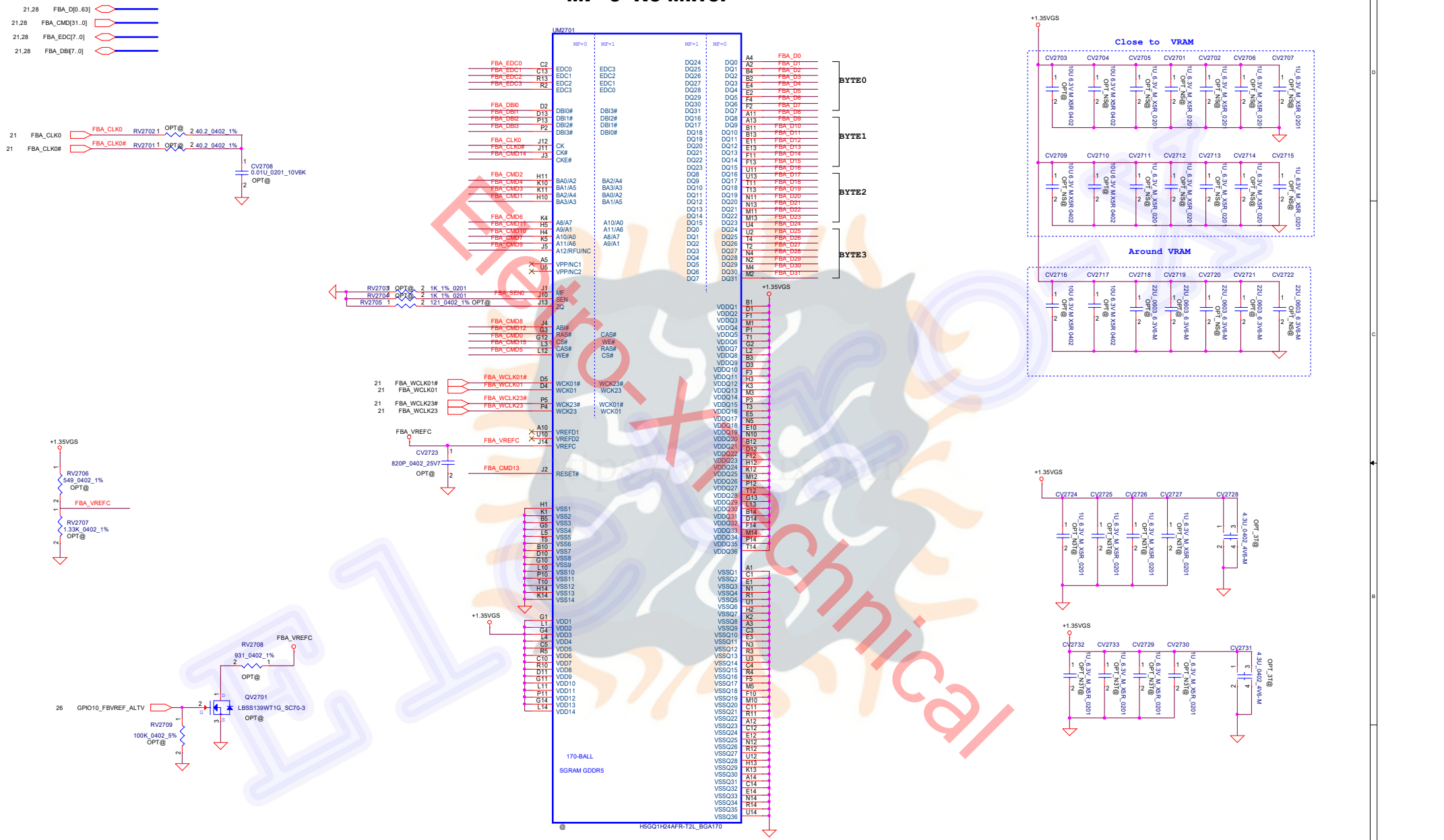
26
of
60

Lower 32 bits

MF=0 No Mirror



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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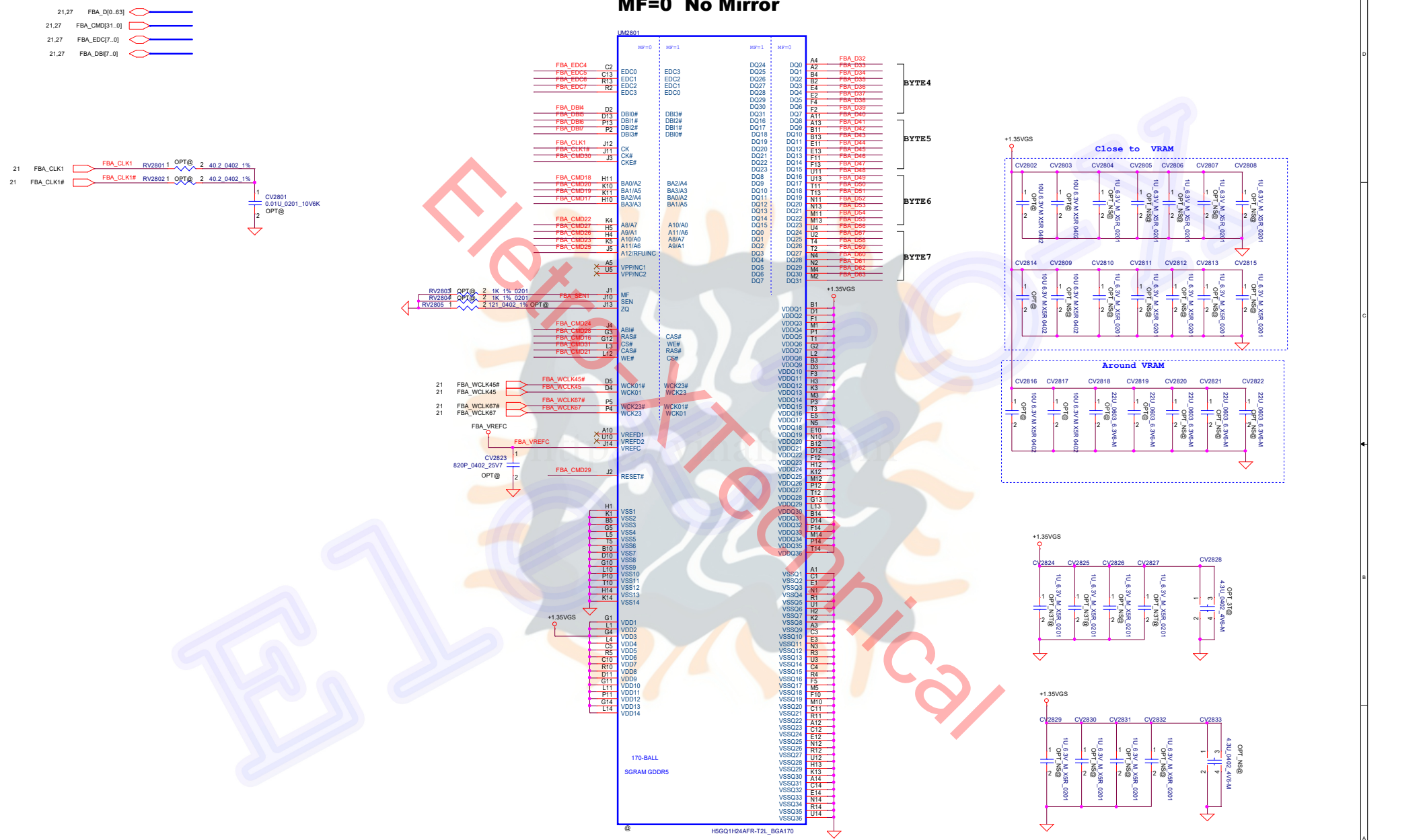
Title	GPU_GDDR5_Rank0_[31:0]		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
Date:	Friday, December 06, 2019	Sheet 27 of 60	

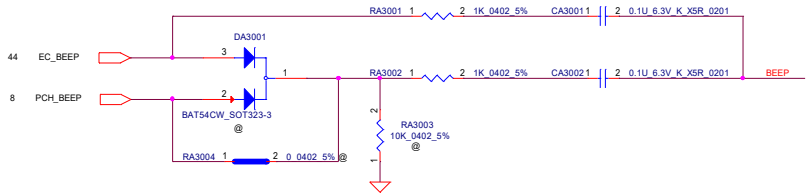
upper 32 bits

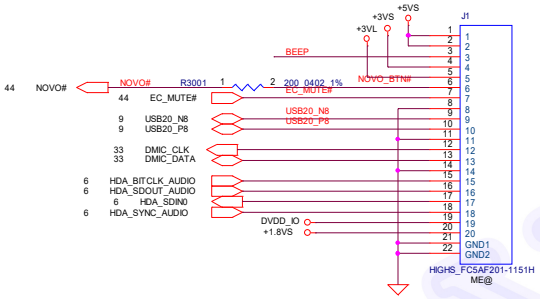
MF=0 No Mirror



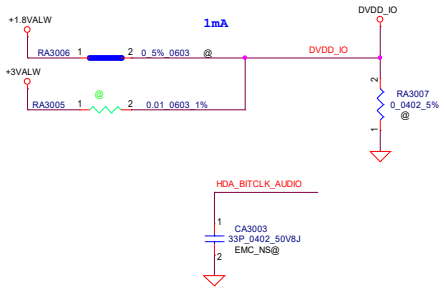
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

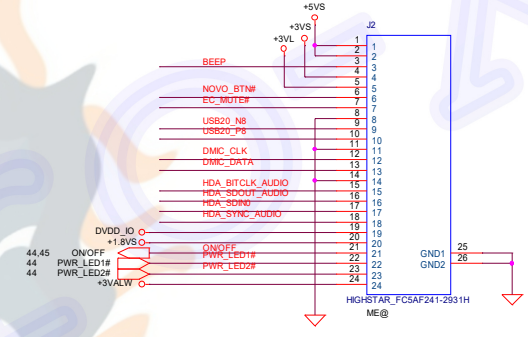
Title	GPU_GDDR5_Rank0_[64:32]		
Size C	Document Number GS44D/GS54D		Rev 0.1
Date: Friday, December 06, 2019	Sheet 28 of 60		

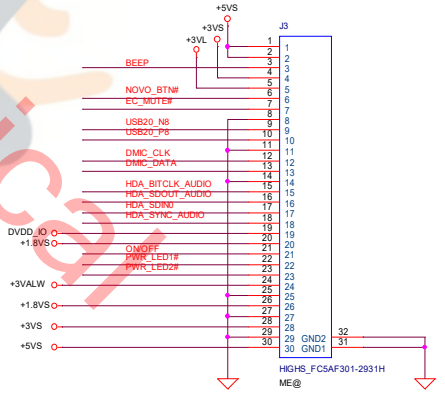




CPU HDA BUS power 1.8VALW

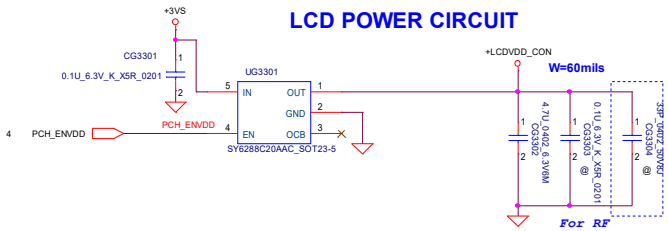


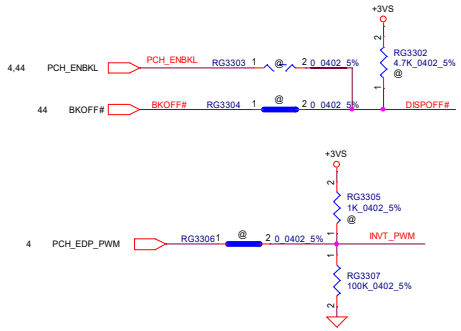


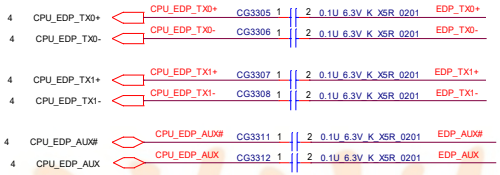


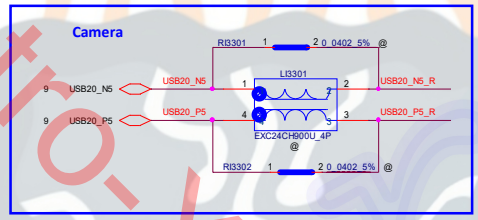
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

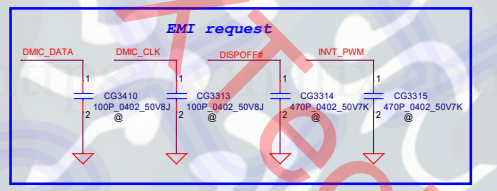
Title	CODEC_RTS5199		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
Date:	Friday, December 06, 2019	Sheet 30 of 60	

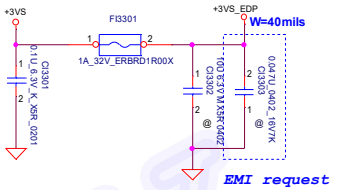


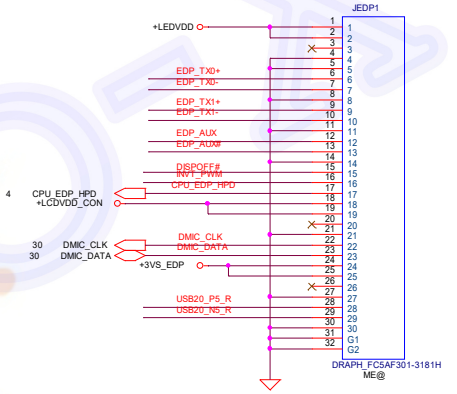






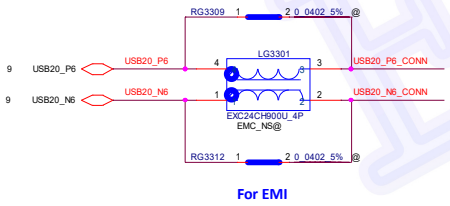


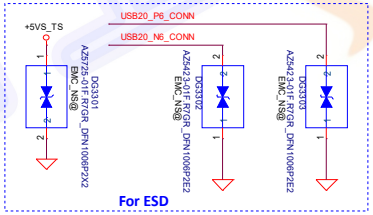


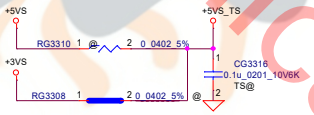


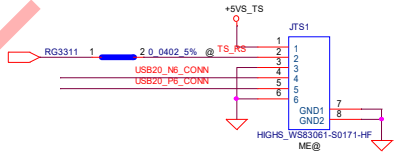
Vinafix.com

Touch Screen









Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	eDP/CAMERA.		
Size	Document Number		Rev
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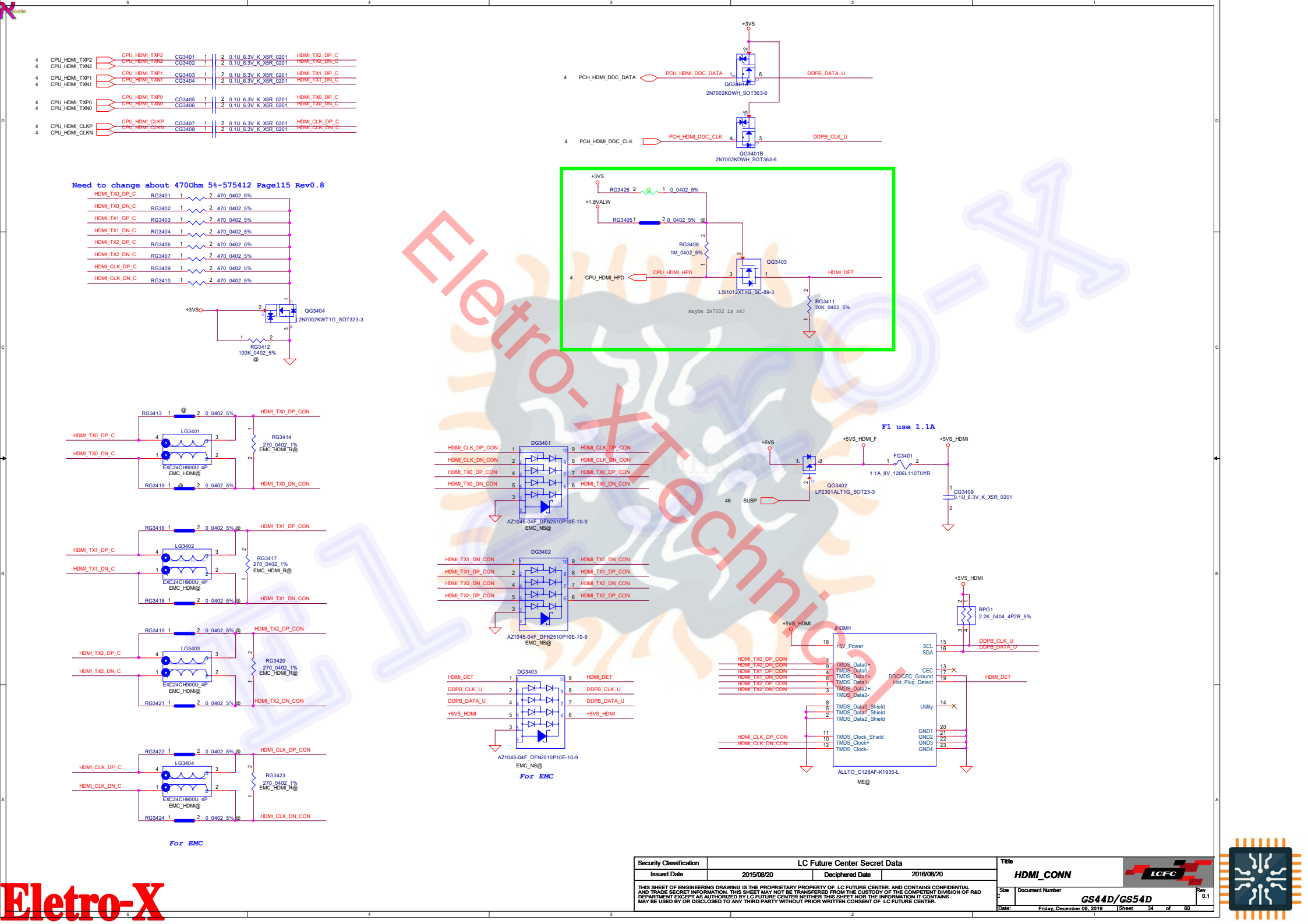

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	HDMI_CONN		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
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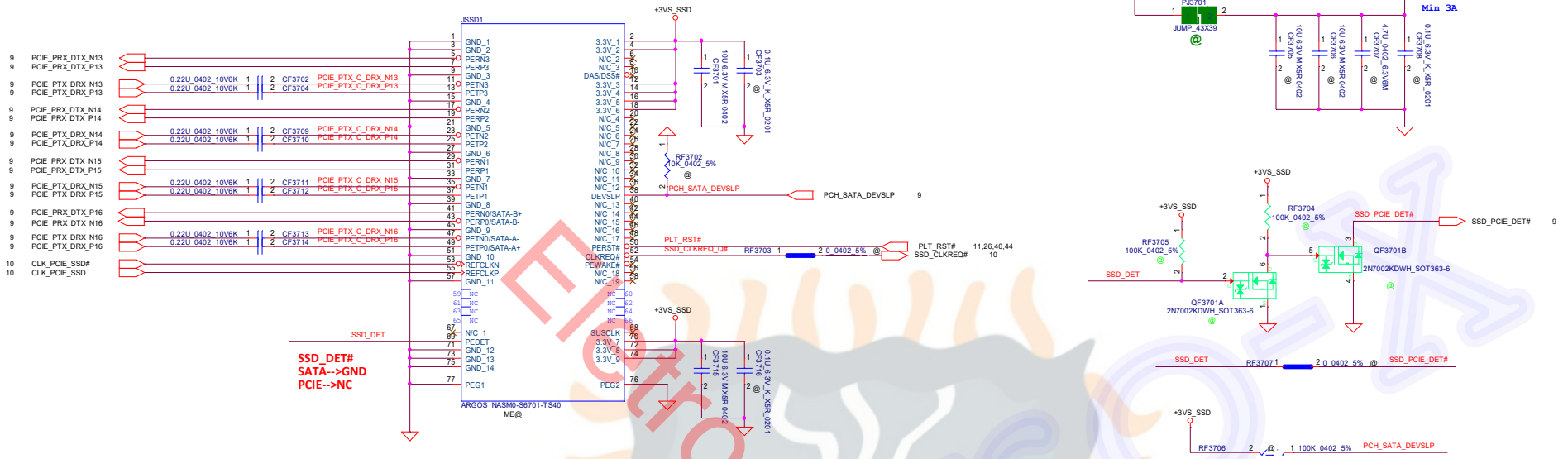
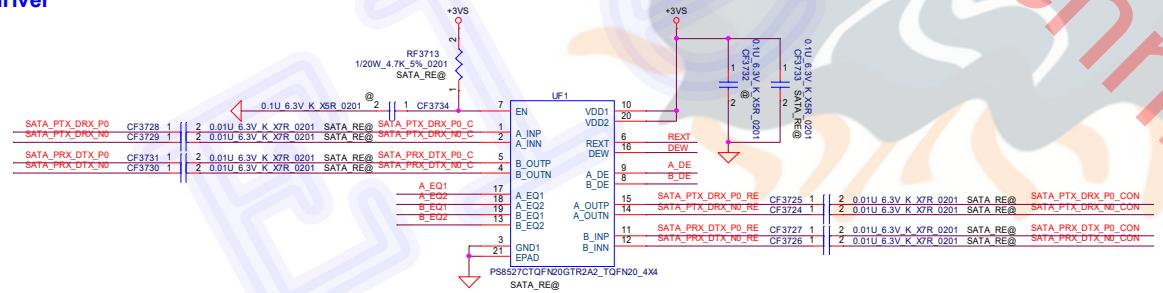
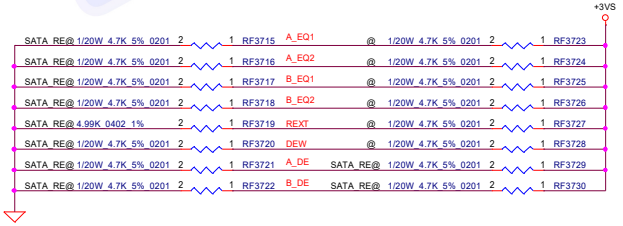
M.2 SSD

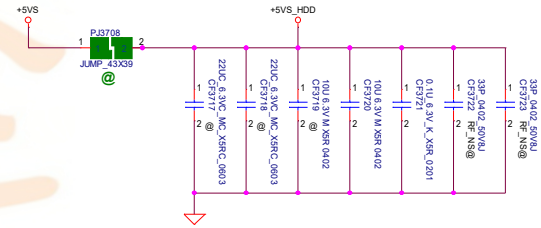


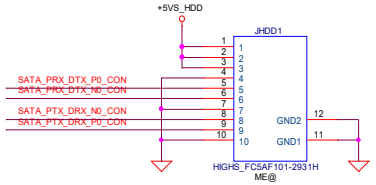
SATA

SATA Redriver









Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	NGFF_SSD_1		
Size	Document Number		Rev
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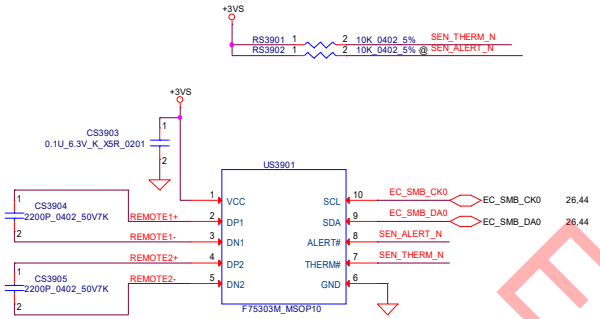
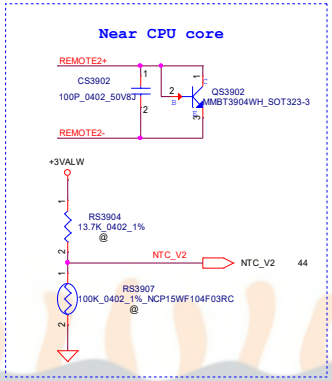
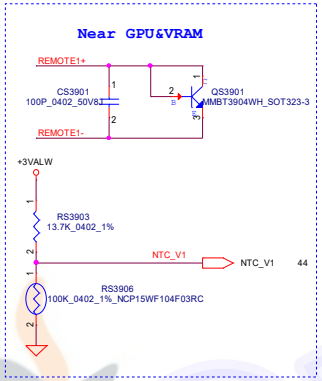
SMSC thermal sensor

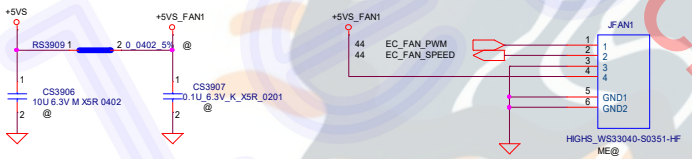






REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

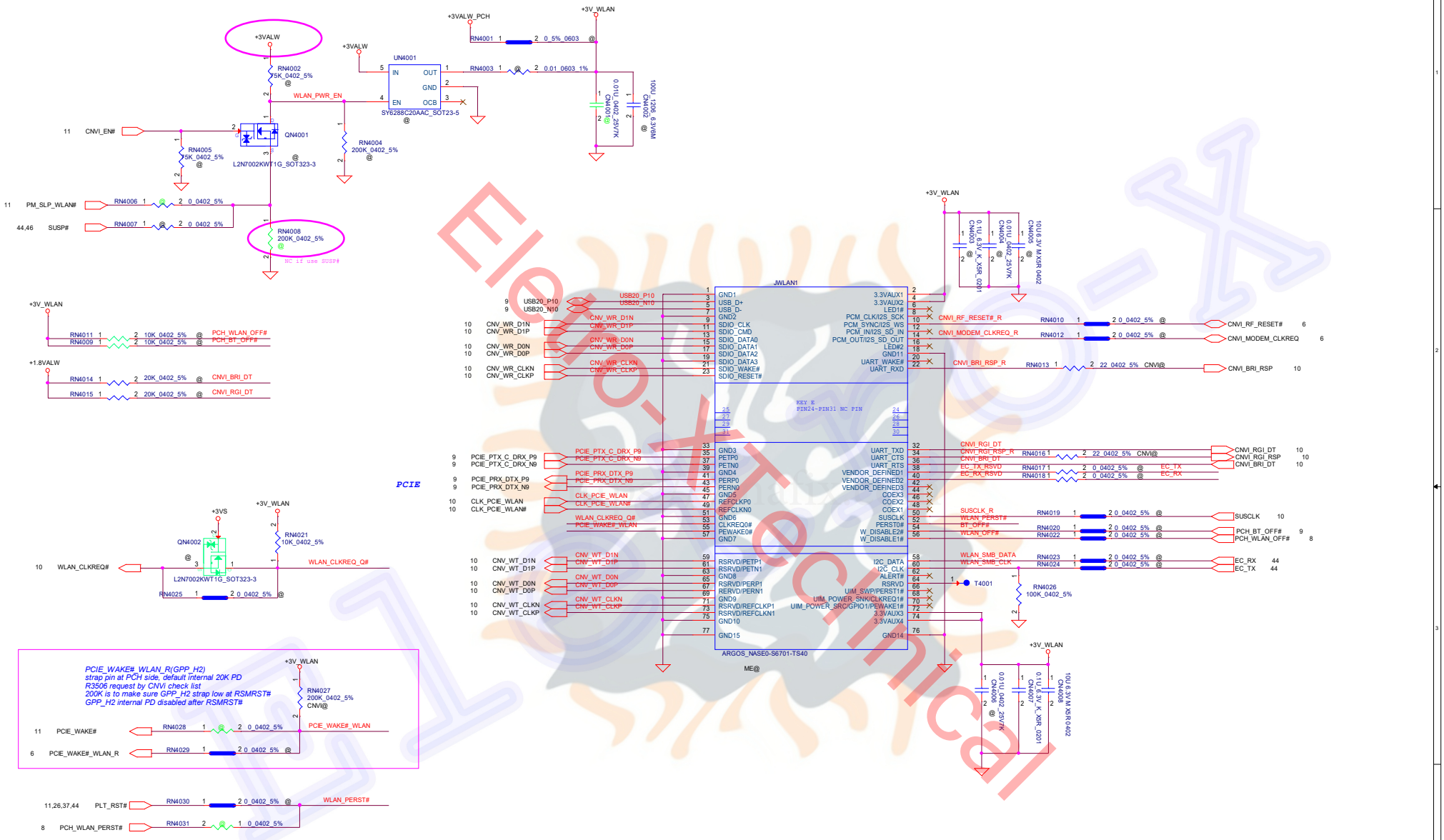
FAN Conn



Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	Thermal sensor/FAN CONN.		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
Date:	Friday, December 06, 2019	Sheet 39 of 60	

Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title: NGFF_WLAN

Size	Document Number	Rev
C	GS44D/GS54D	0.1

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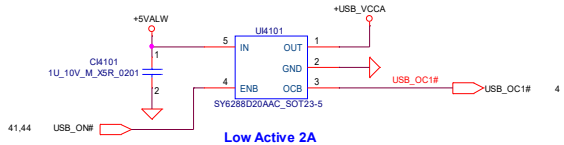
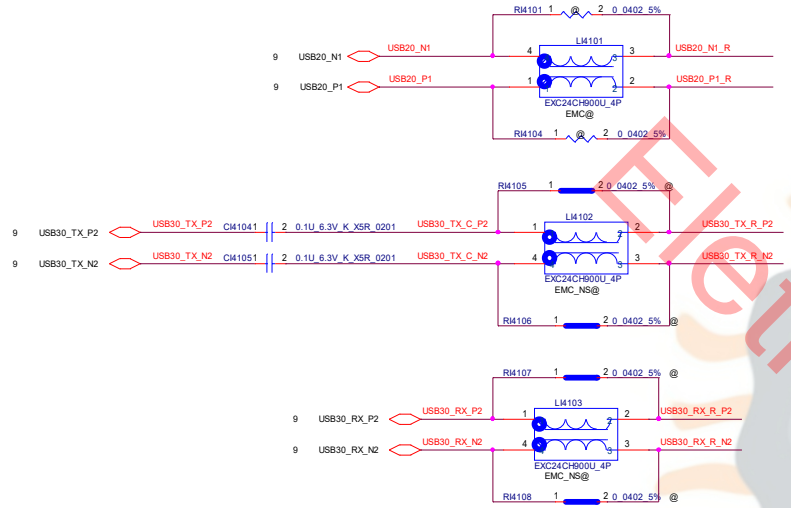
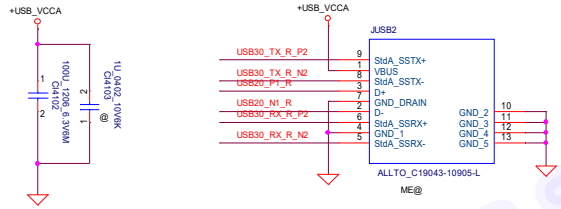
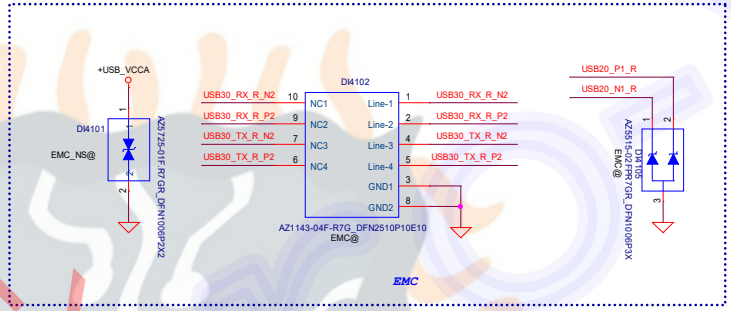
USB3.0 Port1



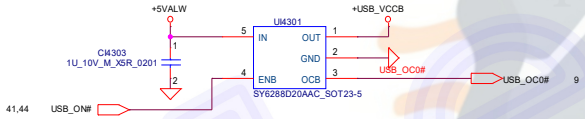
Low Active 2A



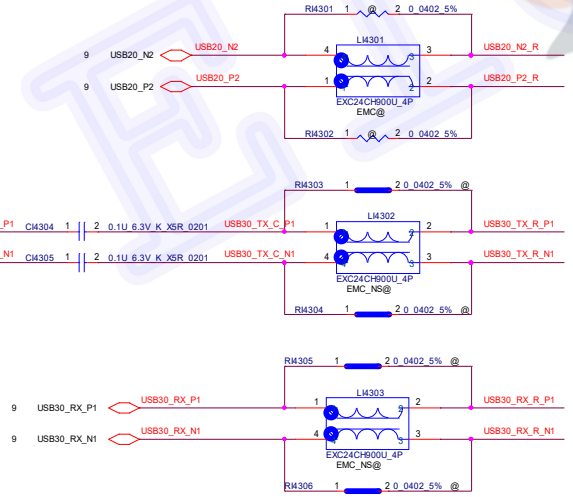


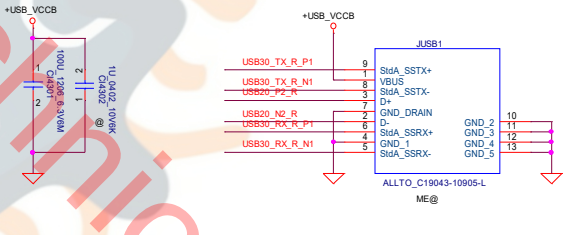


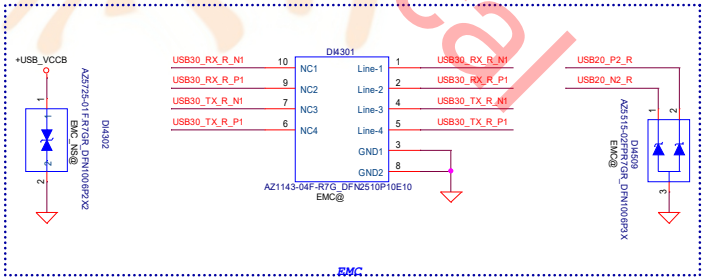
USB3.0 Port2



Low Active 2A







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: USB3 PORT_LEFT

Size	Document Number	Rev
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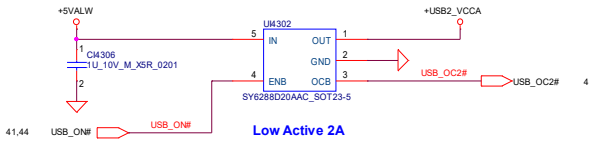
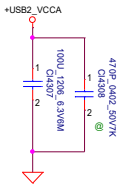
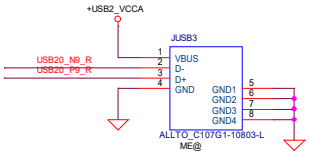
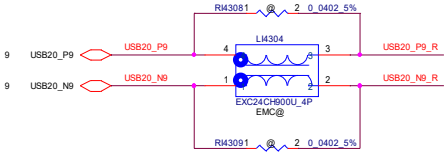
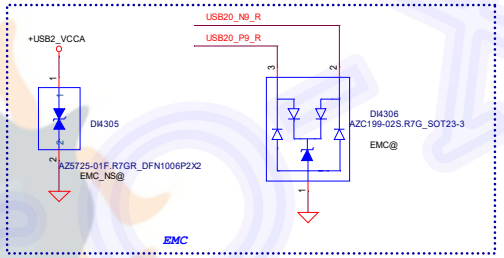
USB2.0 PORT x1





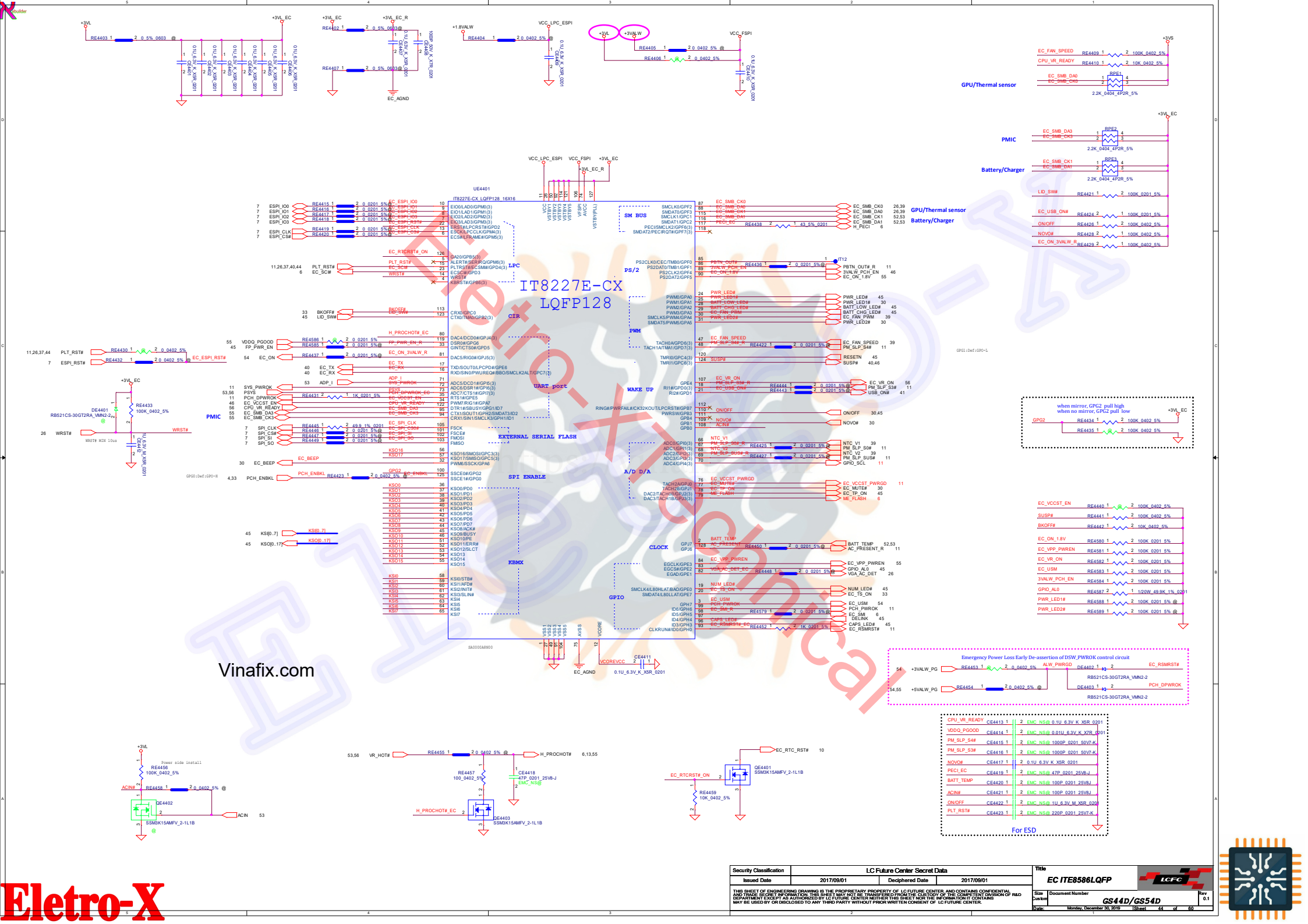






Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

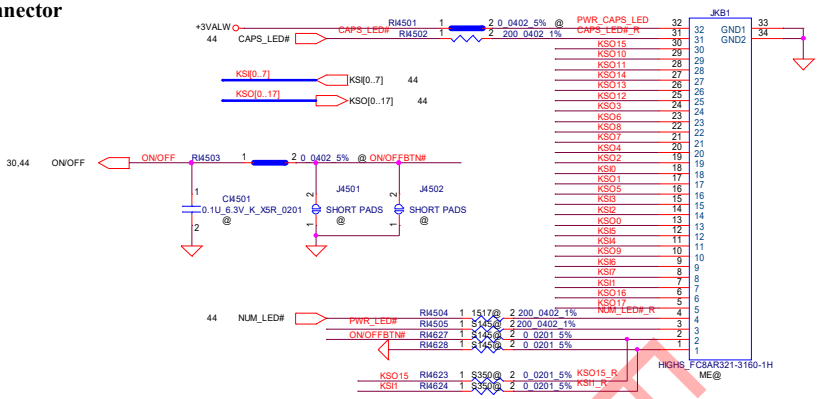
Title	USB3 Port_Right & USB2.0		
Size	Document Number		Rev
D	GS44D/GS54D		0.1
Date:	Friday, December 06, 2019	Sheet 42 of 60	



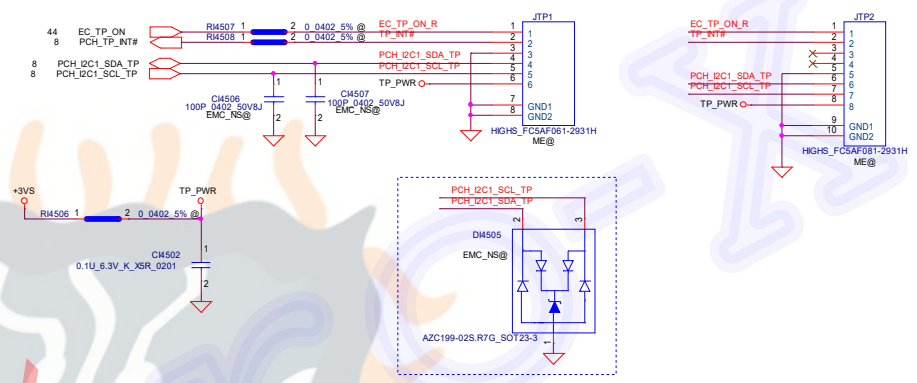
Security Classification	LC Future Center Secret Data		
Issued Date	2017/09/01	Deciphered Date	2017/09/01

Title	EC ITE8586LQFP
Size	Custom
Document Number	GS44D/GS54D
Rev	0.1
Date	Monday, December 30, 2019
Sheet	44 of 60

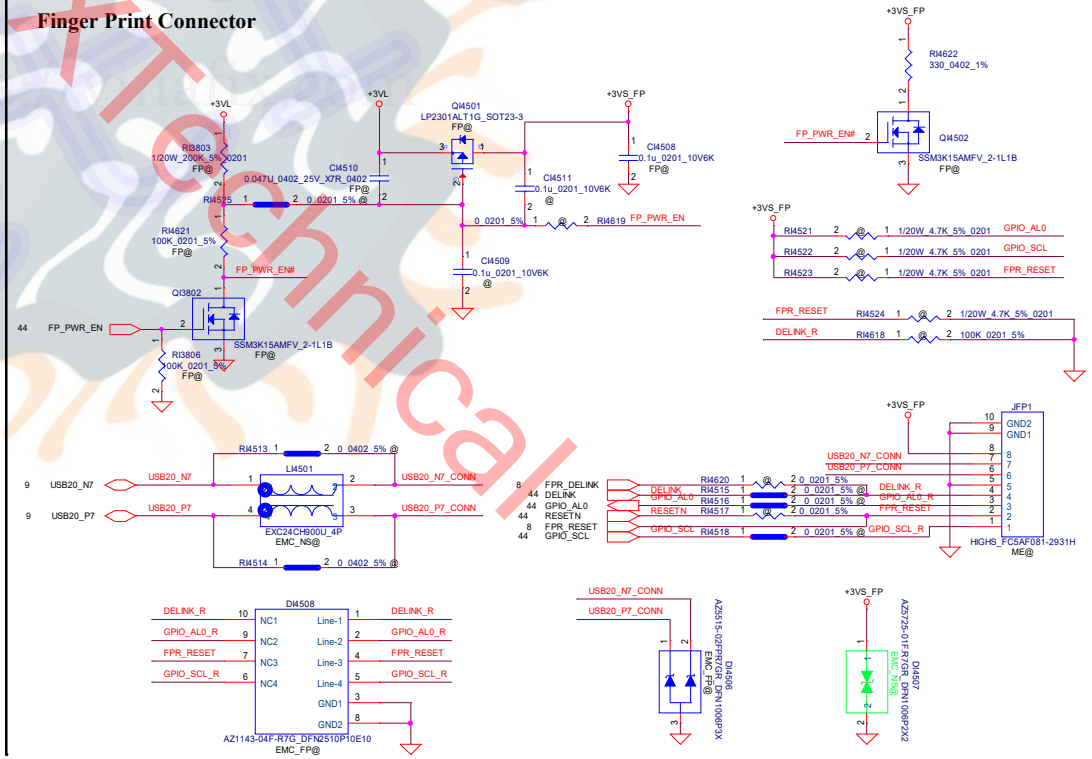
K/B Connector

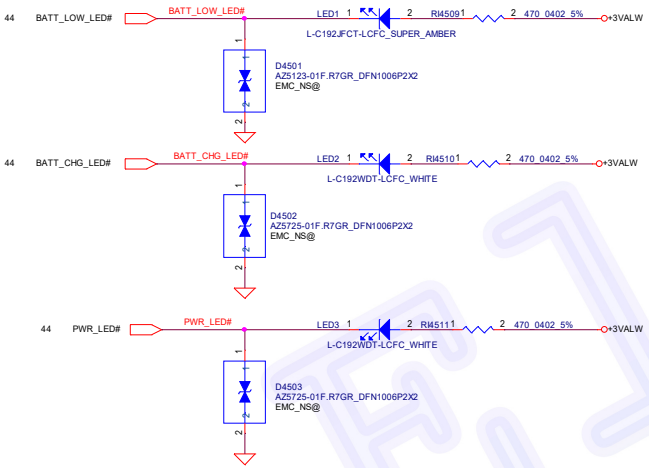


TP/B Connector

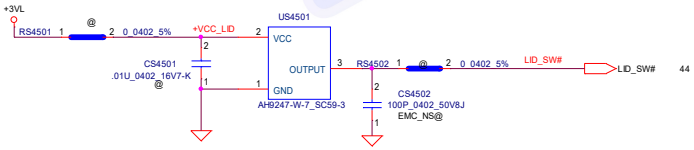


Finger Print Connector





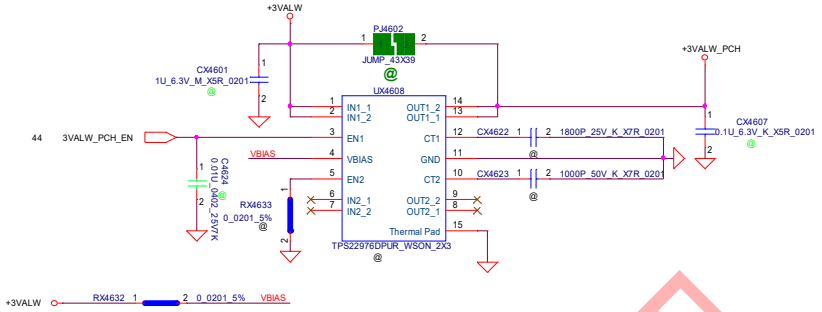
HALL Sensor



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

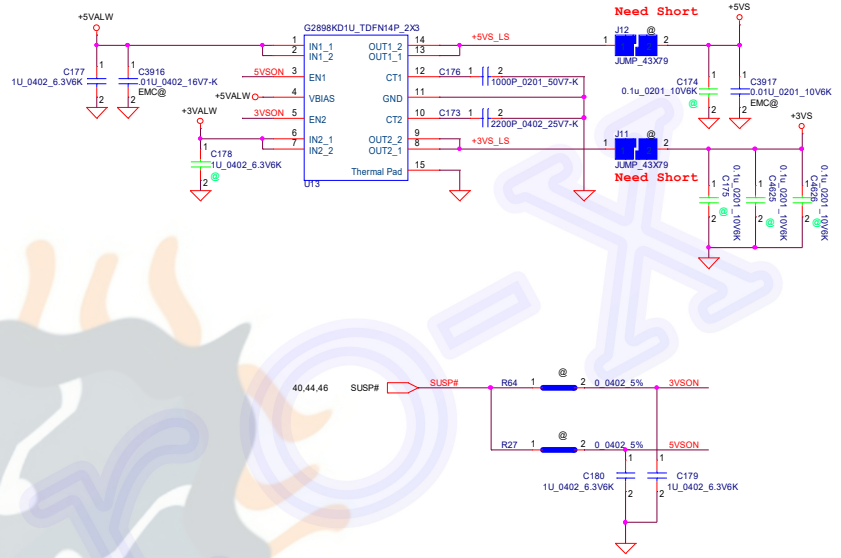
Title	KB/TP_CONN.		
Size	Document Number		Rev
D	GS44D/GS54D		0.1
Date:	Tuesday, December 10, 2019	Sheet	45 of 60

+3VALW to PCH

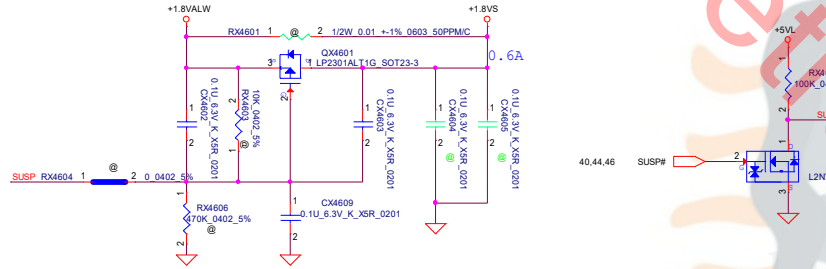


Load Switch
+5VALW To +5VS
+3VALW To +3VS

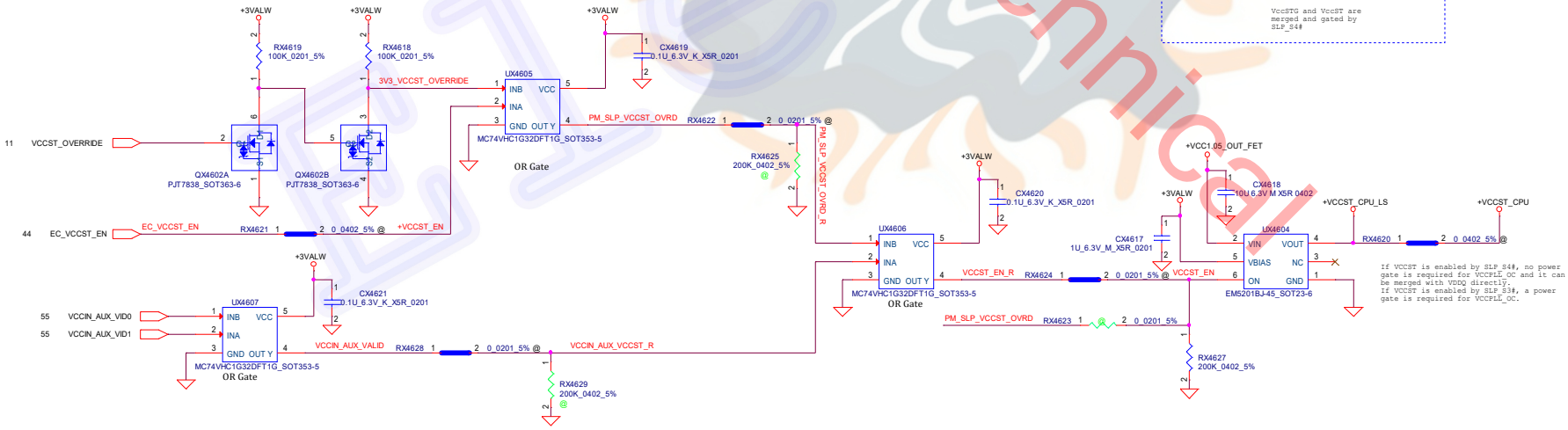
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



+1.8VALW to +1.8VS

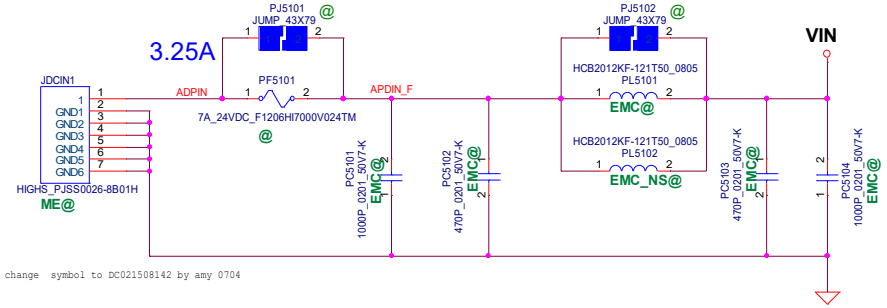


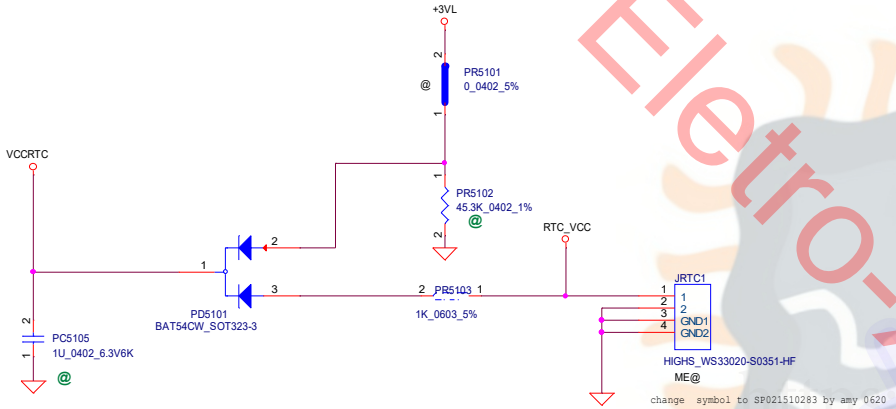
VCCST&VCCSTG



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	DC V TO VS INTERFACE		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
Date:	Tuesday, December 10, 2019	Sheet	46 of 60



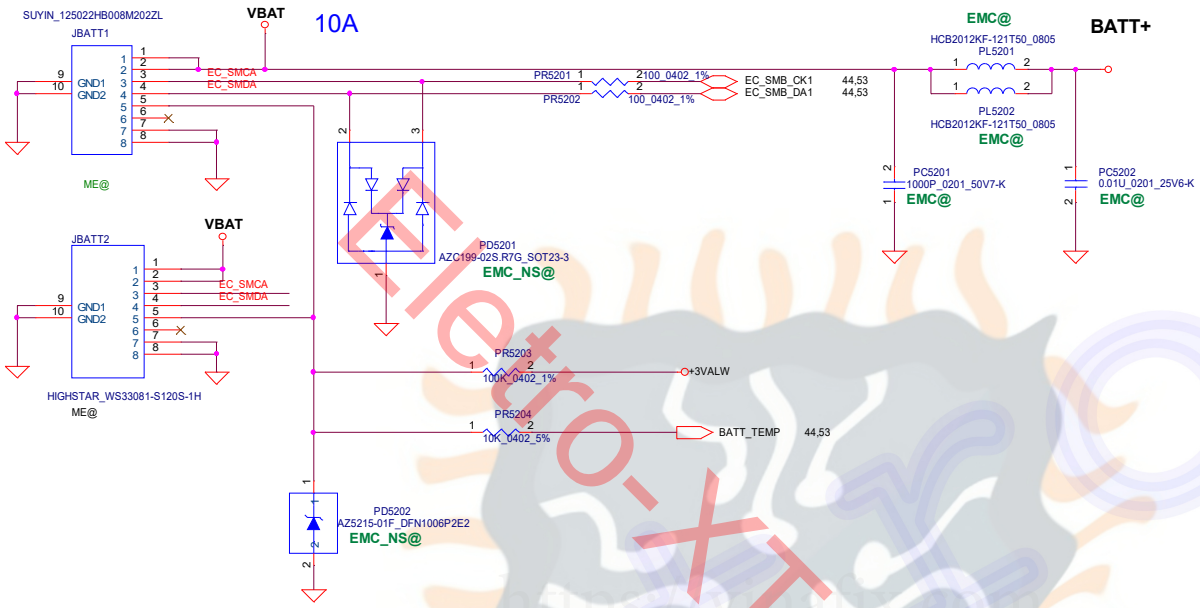


RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-DCIN / RTC charger

Size: Custom	Document Number: GS44D/GS54D	Rev: 1.0
Date: Friday, December 06, 2019	Sheet 51 of 60	

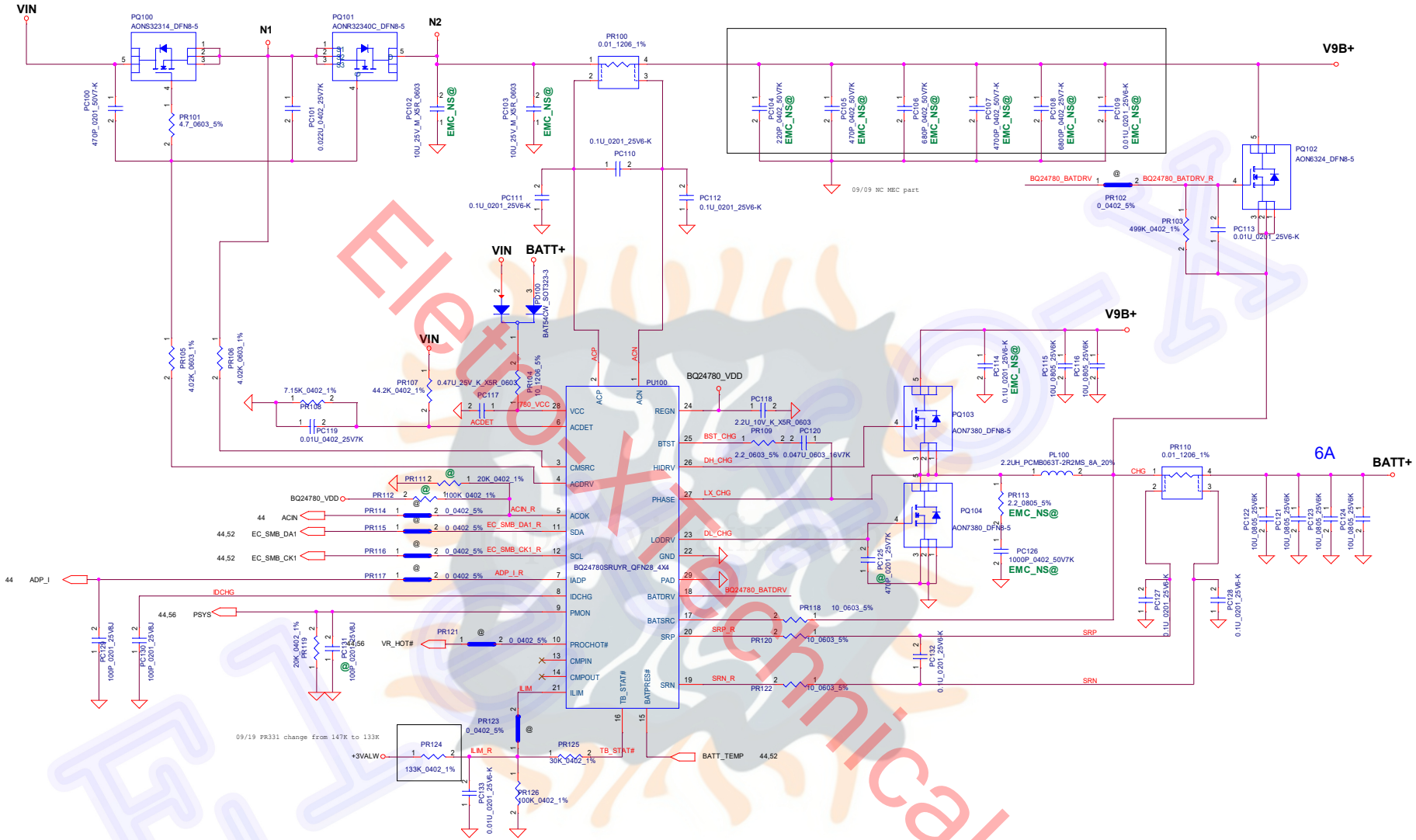


2S1P polymer battery voltage level: +5.5V ~ 8.8 V

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-BATTERY CONN/OTP

Size: Custom	Document Number: GS44D/GS54D	Rev: R0
Date: Friday, December 06, 2019	Sheet 52 of 60	



ACDECT setting 17.2V
Charge current limit HW=7A
DC discharge limit =26A
Discharge current limit HW=9A during Turbo boost

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2019/07/10

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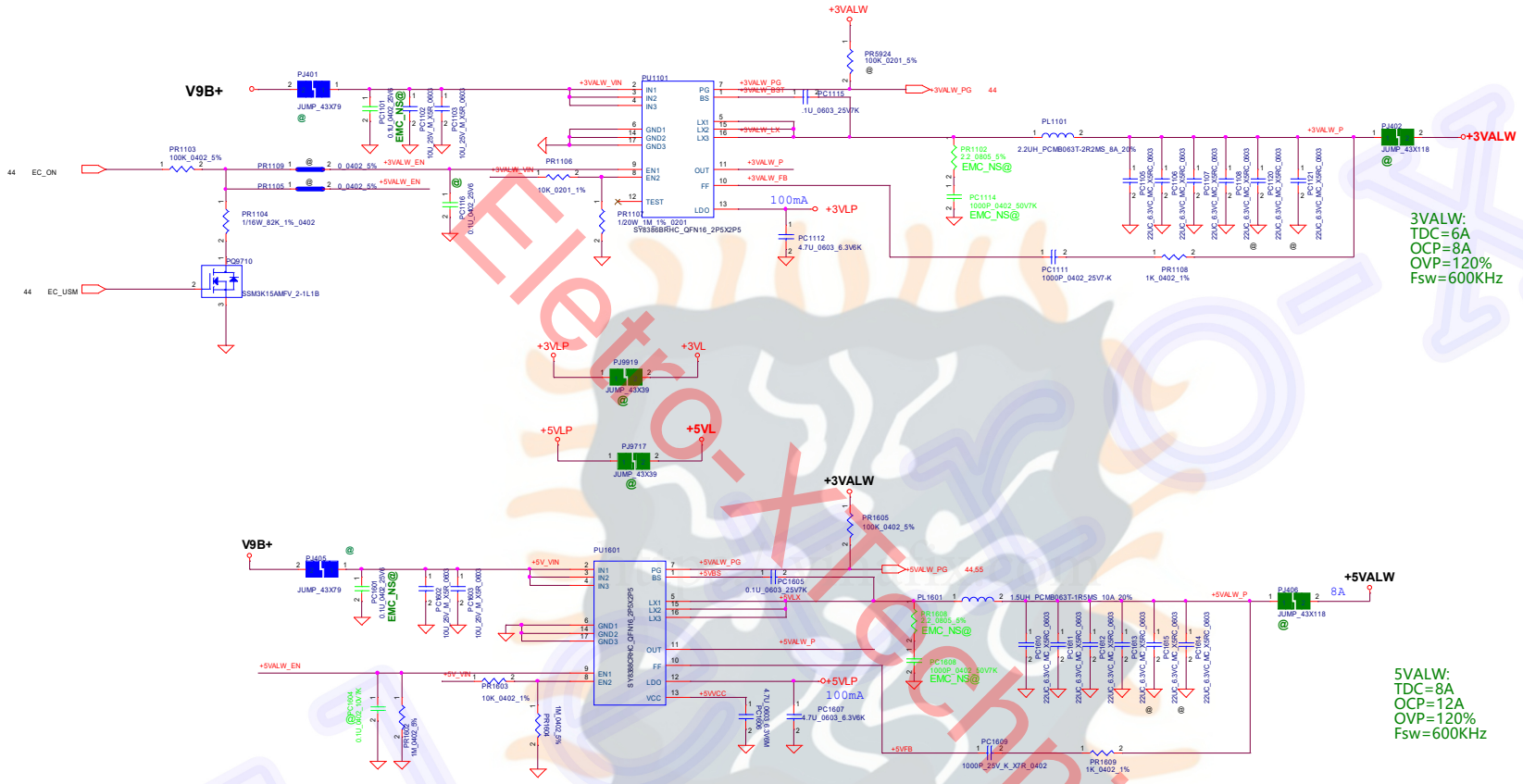
Title	PWR-CHARGER		
Size	Document Number		Rev
D	GS44D/GS54D		0.3
Date:	Friday, December 06, 2019	Sheet	53 of 1

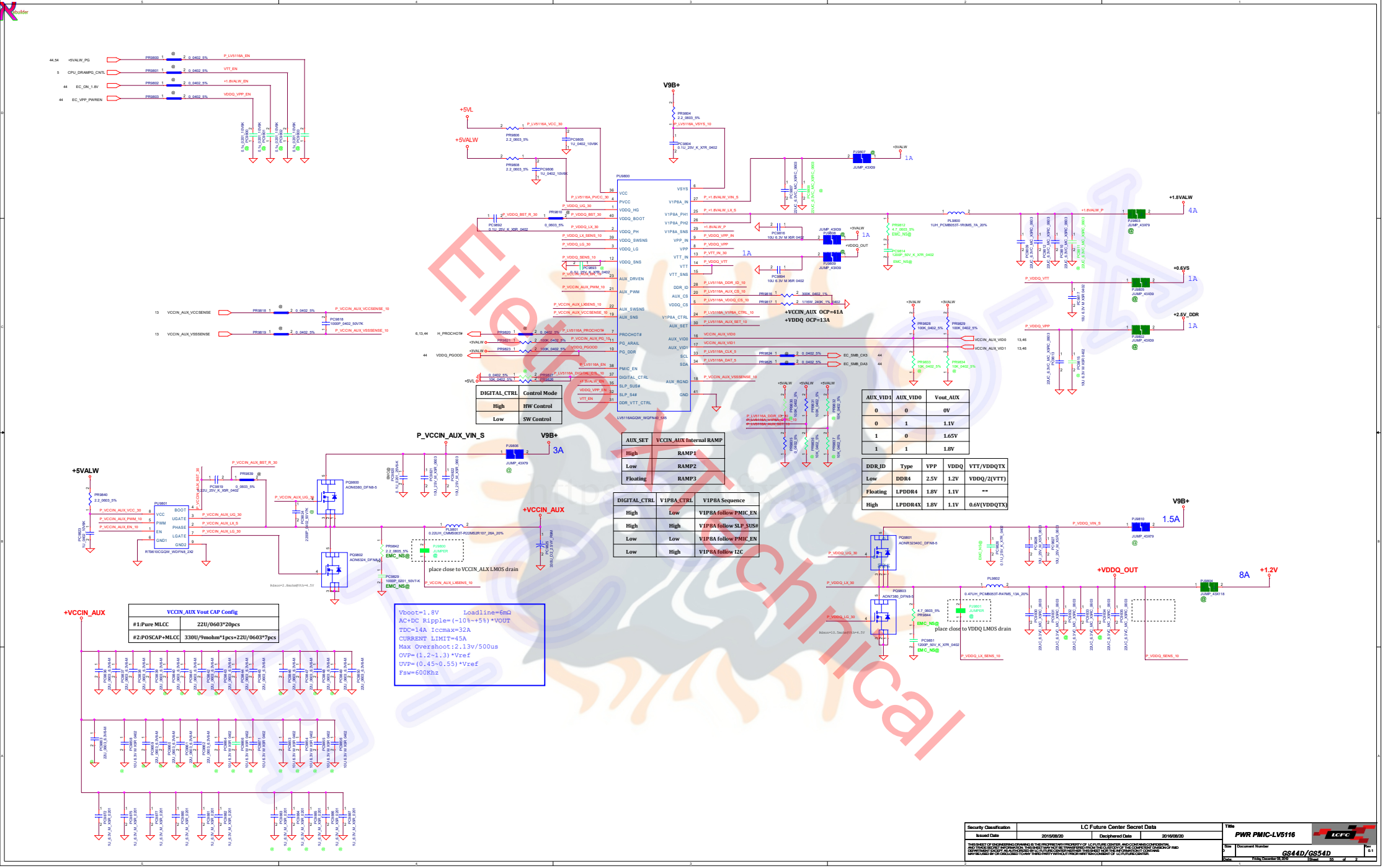


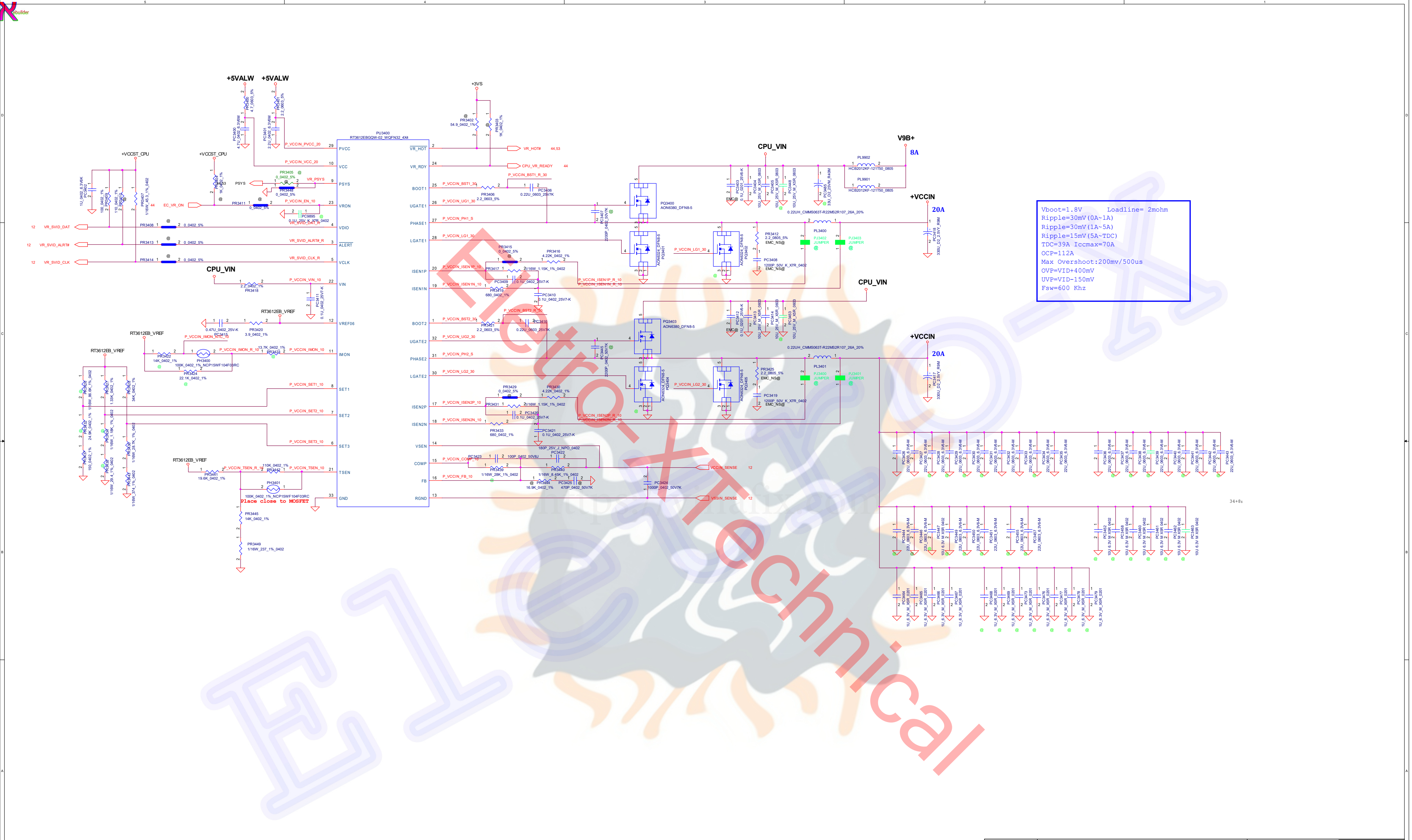
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR_3VALW/5VALW

Size: Custom | Document Number: S350 ADA | Rev: 1.0

Date: Friday, December 06, 2019 | Sheet





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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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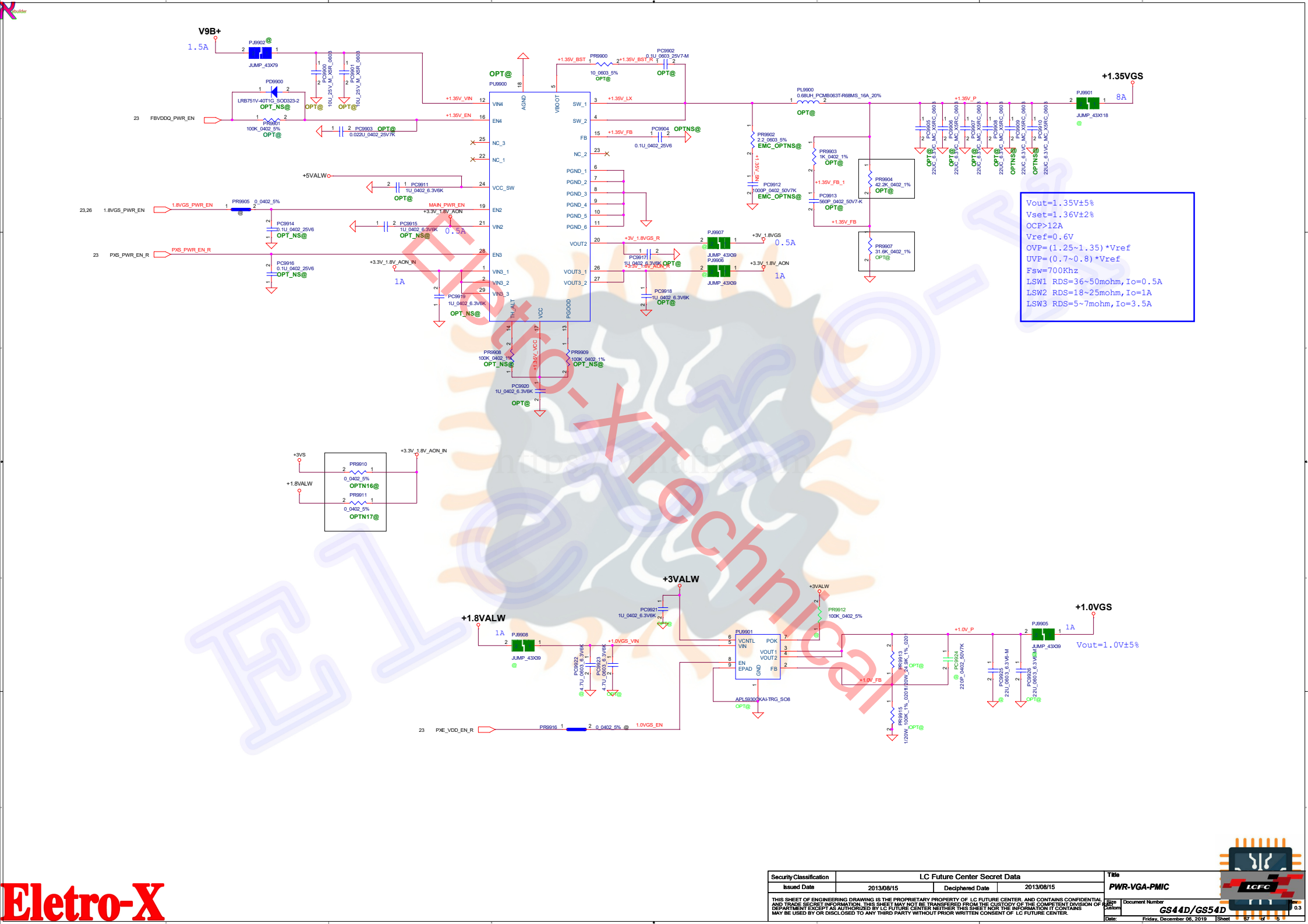
Title: PWR-CPU_CORE

Document Number: GS44D/GS54D

Rev 0.1

Date: Friday, December 06, 2019 Sheet 56 of 3



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

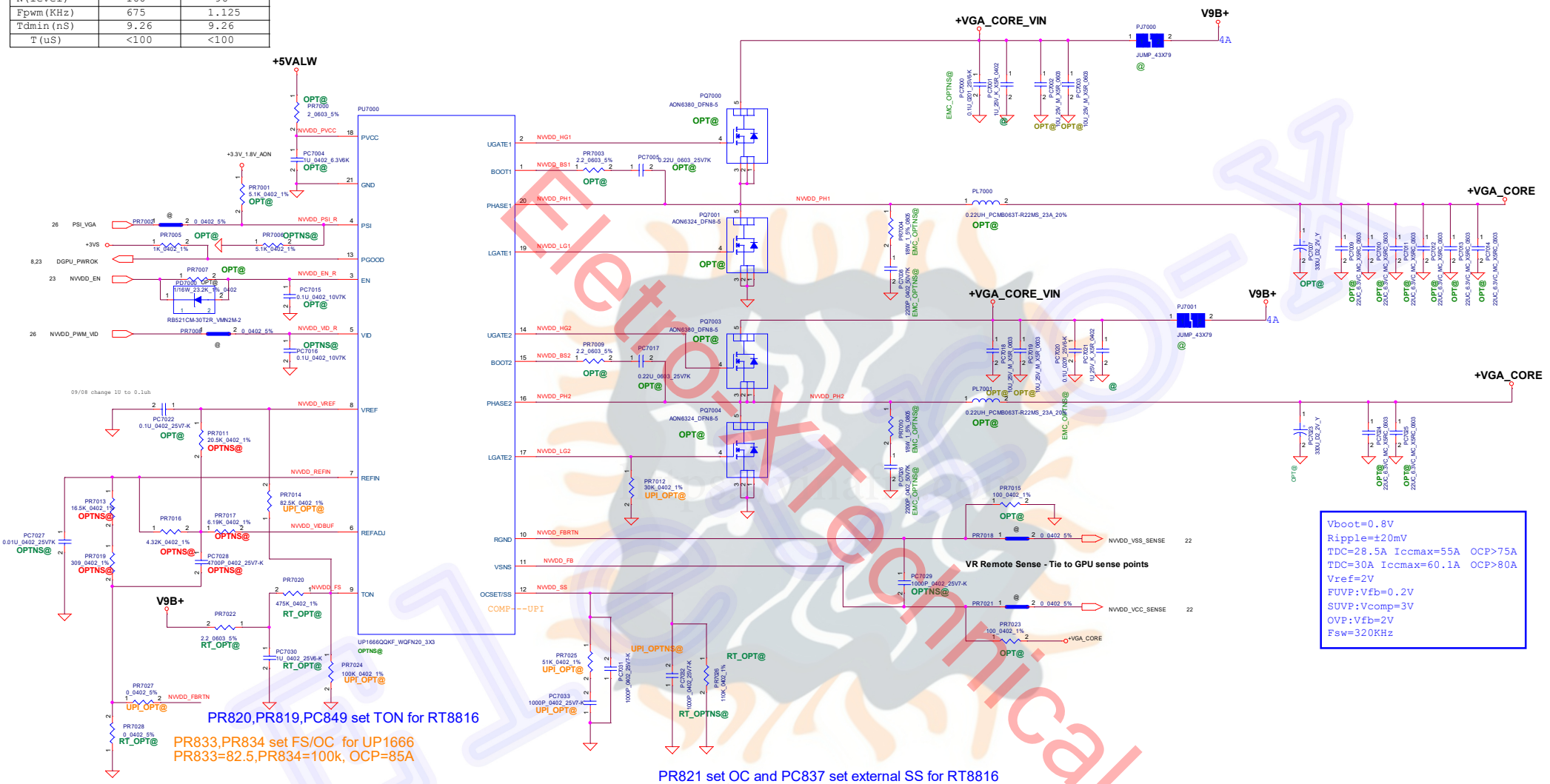
Title: PWR-VGA-PMIC

Size: Custom | Document Number: GS44D/GS54D | Rev: 0.3

Date: Friday, December 06, 2019 | Sheet 57 of 65

PWM-VID Specification		
	N17 Config	N16 Config B
Vmin(V)	0.3	0.6
Vmax(V)	1.3	1.2
Vboot(V)	0.8	0.9
Vstep(mV)	6.25	6.25
N(level)	160	96
Fpwm(KHz)	675	1.125
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1(KΩ)	PR7017	6.19	20
R2(KΩ)	PR7011	20.5	20
R3(KΩ)	PR7016	4.32	2
R4(KΩ)	PR7013	16.5	18
R5(KΩ)	PR7019	0.309	0
C(nF)	PC7028	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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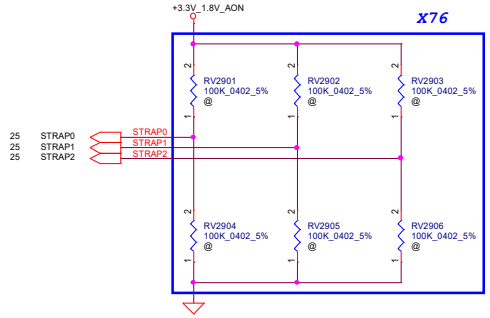
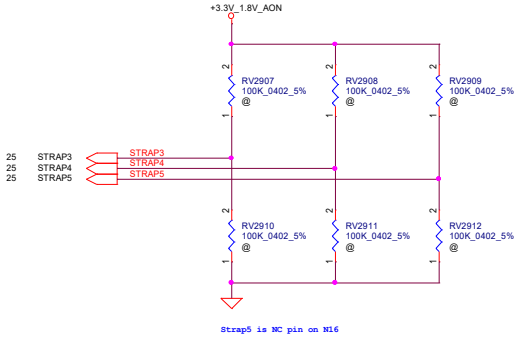
Title: PWR-VGA_CORE

Size: Custom | Document Number: GS44D/GS54D | Rev: 0.1

Date: Friday, December 06, 2019 | Sheet 58 of 4



GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L



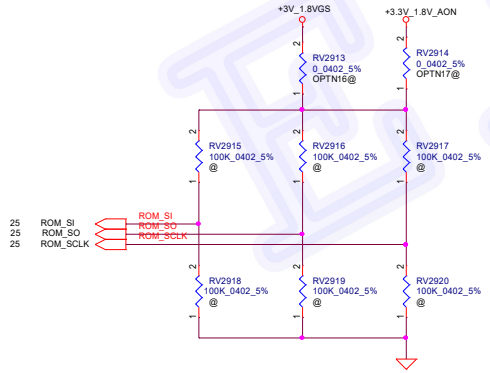
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	
N17S-G1	H	H	M	0000	1:ENABLE 0:DISABLE
N16S-GTR					SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

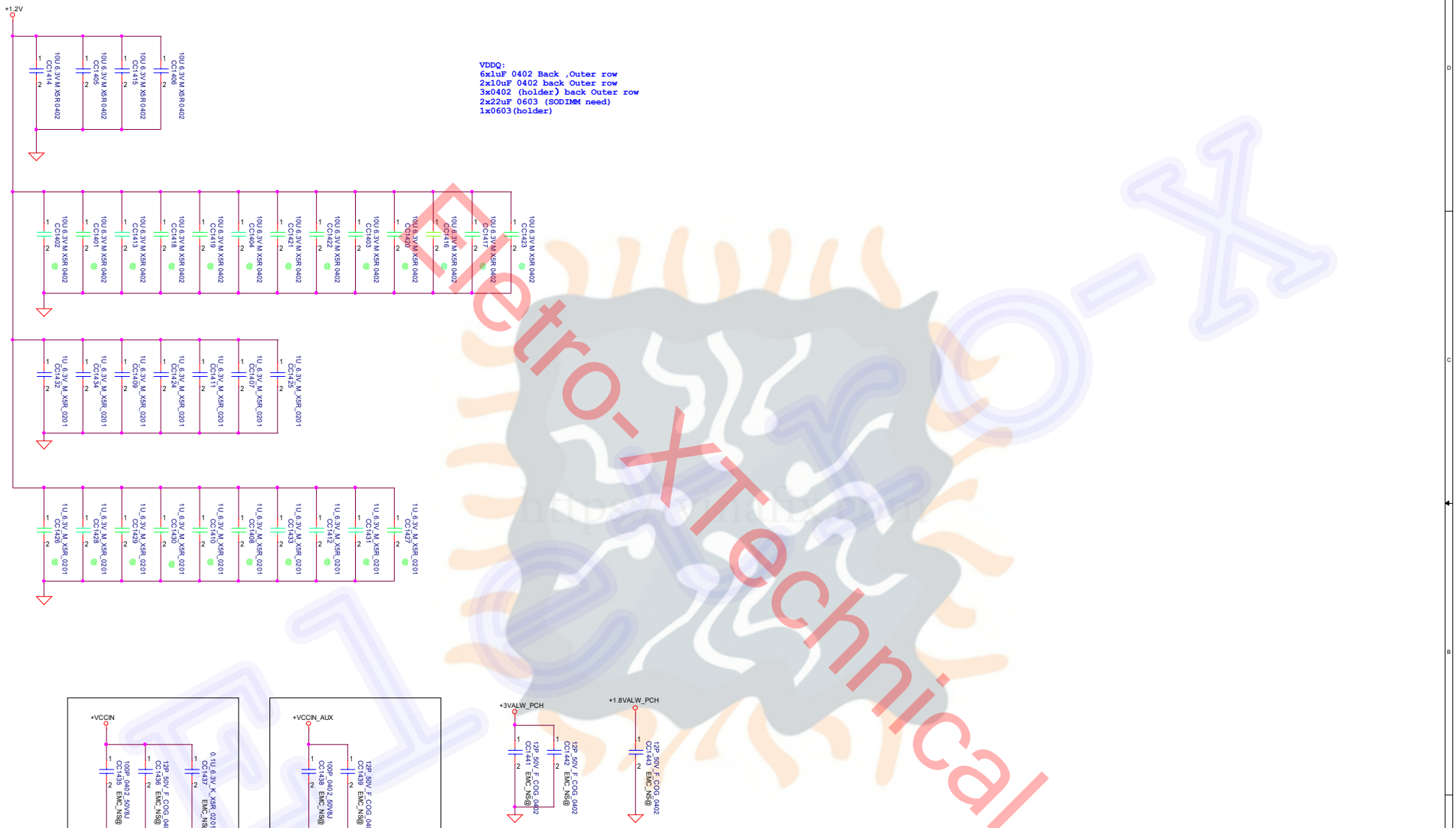
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_MISC

Size	Document Number	Rev
C	GS44D/GS54D	0.1

Date: Friday, December 06, 2019 Sheet 29 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S740-ICL		
Size	Document Name		Rev
C	GS44D/GS54D		0.1
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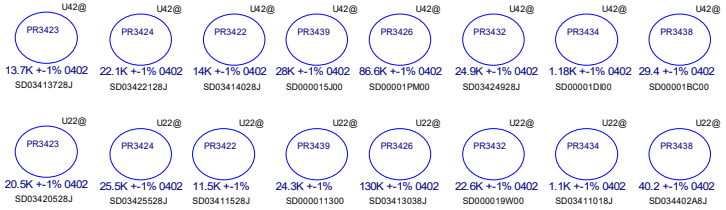
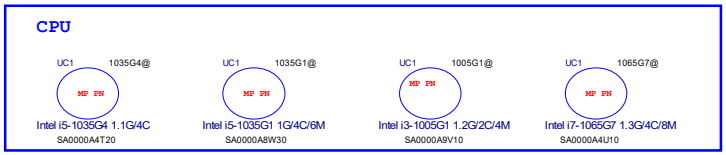
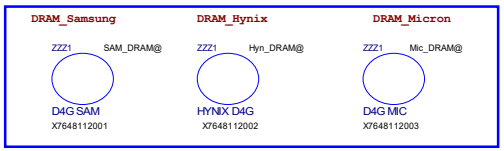
POWER

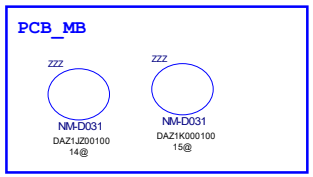


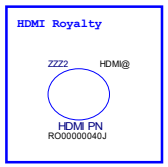
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

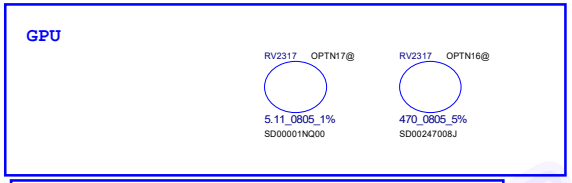
Title	POWER CHANGE LIST		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
Date:	Tuesday, December 10, 2019	Sheet 59 of 62	











Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Virtual symbol		
Size	Document Number		Rev
C	GS44D/GS54D		0.1
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PCB Fedical Mark PAD

FD4901 FD4902 FD4903 FD4904 FD4905 FD4906

CPU Thermal Hole

H4902 HOLEA — PAD_CT7P0B6P0D3P2
H4904 HOLEA — PAD_CT7P0B6P0D3P2
H4906 HOLEA — PAD_CT7P0B6P0D3P2
H4907 HOLEA — PAD_CT7P0B6P0D3P2

GPU Thermal Hole

H4903 HOLEA — PAD_CT7P0B6P0D3P2
H4905 HOLEA — PAD_CT7P0B6P0D3P2

H4908 HOLEA — PAD_C7P0D4P0
H4909 HOLEA — PAD_C7P0D4P0
H4910 HOLEA — PAD_O2P5X3P0D2P5X3P0N
H4911 HOLEA — PAD_O2P5X3P0D2P5X3P0N

H4912 HOLEA — PAD_C7P0D2P8
H4913 HOLEA — PAD_C7P0D2P8
H4914 HOLEA — PAD_C7P0D2P8
H4901 HOLEA — PAD_C10P0D8P0

H4915 HOLEA — PAD_C7P0D2P4
H4916 HOLEA — PAD_CT7P0B10P0D4P0
H4917 HOLEA — PAD_CT7P0B10P0D4P0

MD Shielding

SH4901 SPRING_FINGER_6.2X1.64
SH4902 SPRING_FINGER_6.2X1.64
SH4903 SPRING_FINGER_6.2X1.64
SH4904 SPRING_FINGER_6.2X1.64
SH4905 SPRING_FINGER_6.2X1.64
SH4906 SPRING_FINGER_6.2X1.64

SODIMM Shielding

SH4907 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4908 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4909 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4910 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4911 SHIELDING_SUL-35A2M_9P2X3P3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Hole**

LCFC

Size: B | Document Number: GS44D/GS54D | Rev: 0.1

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N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

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