Model Name: GA-P55A-UD3 *1.02*

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1156-A
05	CPU_LGA1156-B
06	CPU_LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCH_FDI,DMI,USB,PCIE,NVRAM
11	PCH DP,CLK BUFFER
12	PCH_HOST,SATA,PCI
13	PCH_GPIO,CTRL,AUDIO
14	PCH_PWR,GND
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOT
18	PCI SLOT 1,2,3
19	ITE 8720 LPC IO
20	COM, -PROHOT , DYNAMIC OC , LPT
21	Dual BIOS
22	ALC888
23	REAR AUDIO JACK
24	CLOCK GEN ICS9LPRS914
25	VCORE PWM_ISL6334ACR
26	CPU_VTT PWM_ISL6322G
27	DDR_15V & VCC1_05_PCH PWM_ISL6545CBZ

SHEET	TITLE
28	DISCRETE POWER
29	F_PANEL , F_USB , FDD
30	ATX POWER
31	Marvell 9128
32	REALTEK RTL8111D
33	TPM SLB9635TT
34	HWM,KB/MS , FAN CTRL
35	ESATA JMB362
36	IT8213-1 PATA
37	UP72022
38	TABLE LIST
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Gigabyte Technology

Title	Cover Sheet	
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Date: Friday, November 13, 2009	Sheet 1 of 38	

GA-P55A-UD3 Version: 1.02

Component value change history

Data	Change Item	Reason
EP55A-UD3P 0.2	1. CHECK +12V SHORT PAD FOR 10mil	9. LU1,LU4 RTL8111D --> RTL8111C
	2. F1_1394加蓋(包材階)	10. PCB "育富"移除
	3. ADD DR86=124K/4/1 , DR88=249K/4/1	11. ONFI指定用11SM1-600078-02R
	4. U12~U15 upi6262M --> upi6267M	12. R376 2.26K/4/1 --> 2.55K/4/1
	5. DRAM_PWROK R490=1K/4/1 , R491=3K/4/1	13. 確認上哪種upi6262 10%/upi6267?
	6. REMOVE DR138=0/4 , ADD DR139,DR141=0/4	14. FB7~FB10 REMOVE
	7. RU2指定料號:10HP4-112540-11R	15. PCH BUFFER 25MHz REMOVE "X2,C93,C94,R420"
	8. 排阻指定廠牌用WALSIN	16. BIOS 16M --> 32M (FOR ONFI ONBOARD)
2009/06/10 PBOM:0.1	1.NEW MODEL: P55-UD3P-0.1	
2009/06/24 EBOM:10A	1.ADD -RSMRST PATCH CIRCUIT R866~R868,C192,C193,Q112,Q113,3UDUAL_ICH ADD 5VSB R864,R865	
	2.CHANGE Marvel9123 gpio pin,del RR39,R10,RR67,RR65,ADD RR62	
	3.CHANGE IT8275 料號,DR84 100--->0	
	4.MARVELL 9123----->JMB363	
	5.J363/J632 PATCH POWER SEQUENCE;Q50 MOS--->BJT	
2009/07/7 PBOM:10B	1.P-BOM	
2009/07/10 PBOM:10C	1.RBC53 0.1UF----->1UF	
2009/07/16 PBOM:10D	1.移除PLL電容,BC136,BC150,BC185,BC201	
2009/07/22 PBOM:10E	1(CE2,EC32,EC37,EC38,EC23,EC36,REC3)100uf cap 6*6改成6.3*10.5mm ,因缺料	
	2.VCC3_DAC直接由VCC3經0 ohm提供	
2009/07/29 PBOM:10F	1.ADD R190 1K/4/1 FOR PCIE OVERCLOCK	
2009/08/24 EBOM:29T	1.P55-UD3P-3.0 FOR 9123/USB3.0/8213	
2009/09/9 EBOM:29A	1.CHANGE 9123;USB3.0 MP料號	
2009/10/01 EBOM:02	1.E-BOM	
2009/10/09 EBOM:10A	1.P-BOM	
2009/11/04 PBOM:10B	1.MOS HEATSINK加普料,DEL ESD3	
2009/11/09 PBOM:10c	1.修改pcb料號爲1.02	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
EP55A-UD3P 0.2	1. REMOVE AUDIO ESD	7. 1394 "IEC1" NET SWAP & SHORT PROTECT
	2. REMOVE CPU_VAXG	8. PIN HEATER CHECK
	3. PCH_CLK 改 SHORT PAD (0 ohm維持10pcs以下)	9. ITE8275 SYS_RST PATCH
	4. ITE8275 GPIO11,GPIO13 TO TURBO0/TURBO1	10. BC118,BC119 --> TBC29,TBC30
	5. F_PANEL UPDATE H2X10PANEL-1	11. BC5靠近M_BIOS PIN8 , BC6靠近M_BIOS PIN8
	6. ONFI 改 ON BOARD	12. U2 7474 REMOVE
EP55-UD4P 0.2	1.ONFI作塞孔	
2009/05/20 PCB:0.1	1.NEW MODEL: P55-UD3P-0.1由EP55A-UD3P-0.2修改	
2009/06/10 PCB:0.1	1.NEW MODEL: P55-UD3LP-0.1由P55-UD3P-0.1修改	
2009/06/24 PCB:1.0	1.P55-UD3P-1.0 2.修改文字面	
	3.ADD -RSMRST PATCH CIRCUIT,3UDUAL_ICH ADD 5VSB	
	4.ADD J362 POWER SEQUENCE PATCH CIRCUIT,VCC3&362_1.8V	
	5.MARVELL 9123--->J363(SPEC 變動)	
2009/07/07 PCB:1.01	1.修改文字面,加入crossFire X(PM-SALES REQUEST)	
	2.連帶更改FB5.CR64,RN21 short-wire----->電阻;ESD17 5VDUAL--->5VSB	
2009/08/21 PCB:2.9T	1.P55-UD3P-3.0 FOR 9123/USB3.0	
	2.實驗4層板及6層板(不同內層切割)	
2009/09/08 PCB:2.91	1.ADD PCIEX1 SLOT DETECT PIN FOR BIOS	
	2.EACH USB PORT USE ONE POLYFUSE	
	3.修正X16/X8 TURBO MODE 線路	
	4.調整PCICLK,USB_SEL GPIO GP40 TO GP23	
2009/09/18 PCB:1.0	1.修正X16 lane9接至switch for 9128/usb3.0 GNE2時可以斷開x16 slot端	
	2.版本改0.1,ALC888--->ALC889	
2009/09/21 PCB:0.1	1.由P55A-UD3P-1.0修正.SPEC 12相CPU爲8相	
	2.DEL ESATA,NEC SWITCH	
2009/10/01 PCB:0.2	1.add NEC switch,USB 2.0 switch	
2009/10/02 PCB:1.0	1.由0.2改爲1.0版	
2009/10/09 PCB:1.01	1.R_USB與RUSB30_LAN connector 互換	
2009/11/05 PCB:1.02	1.由1.0修改,移除dts logo 文字面	

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Title: BOM & PCB MODIFY HISTORY

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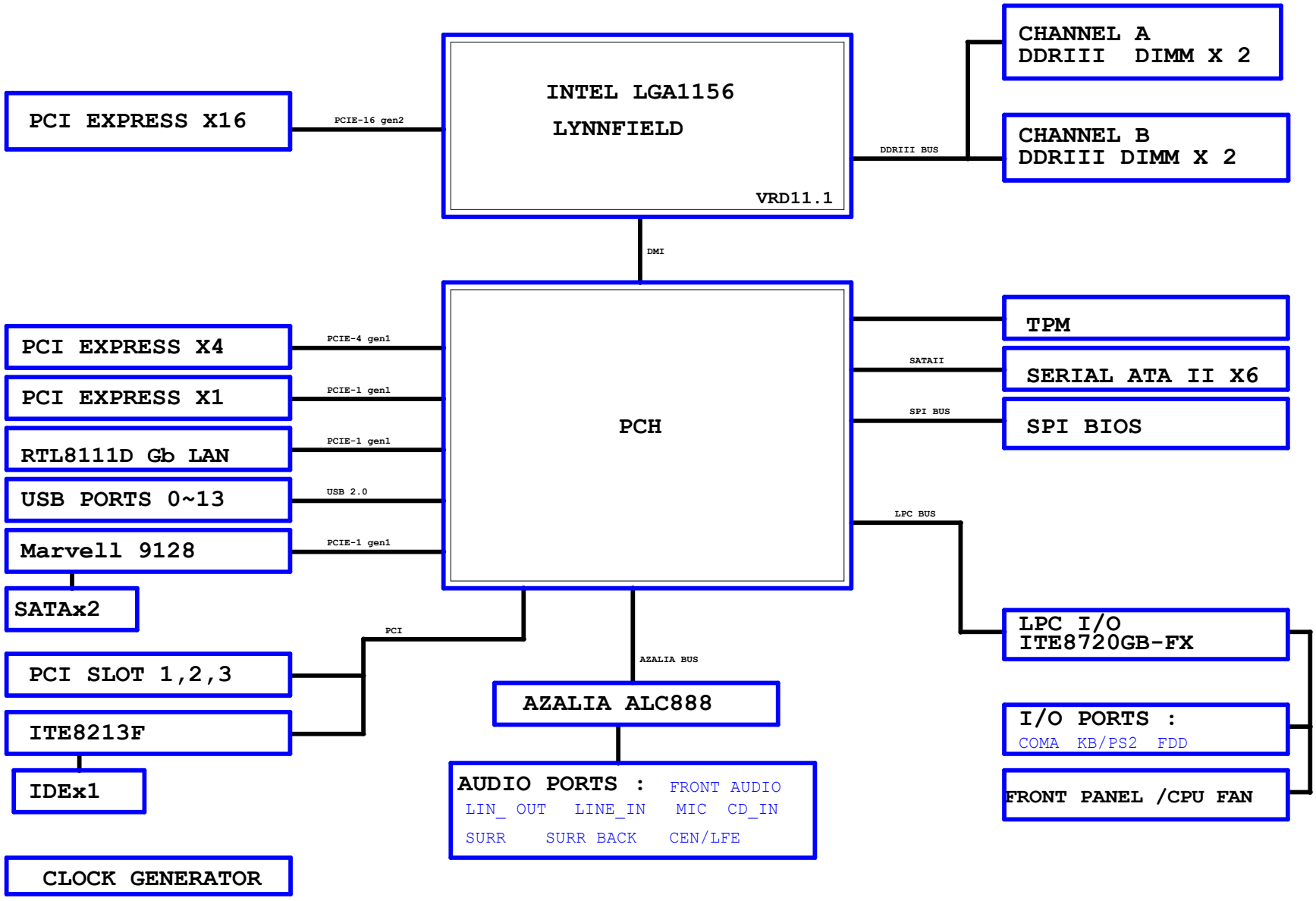
BLOCK DIAGRAM



Gigabyte Technology

Title	BLOCK DIAGRAM	
Size C	Document Number GA-P55A-UD3	Rev 1.02
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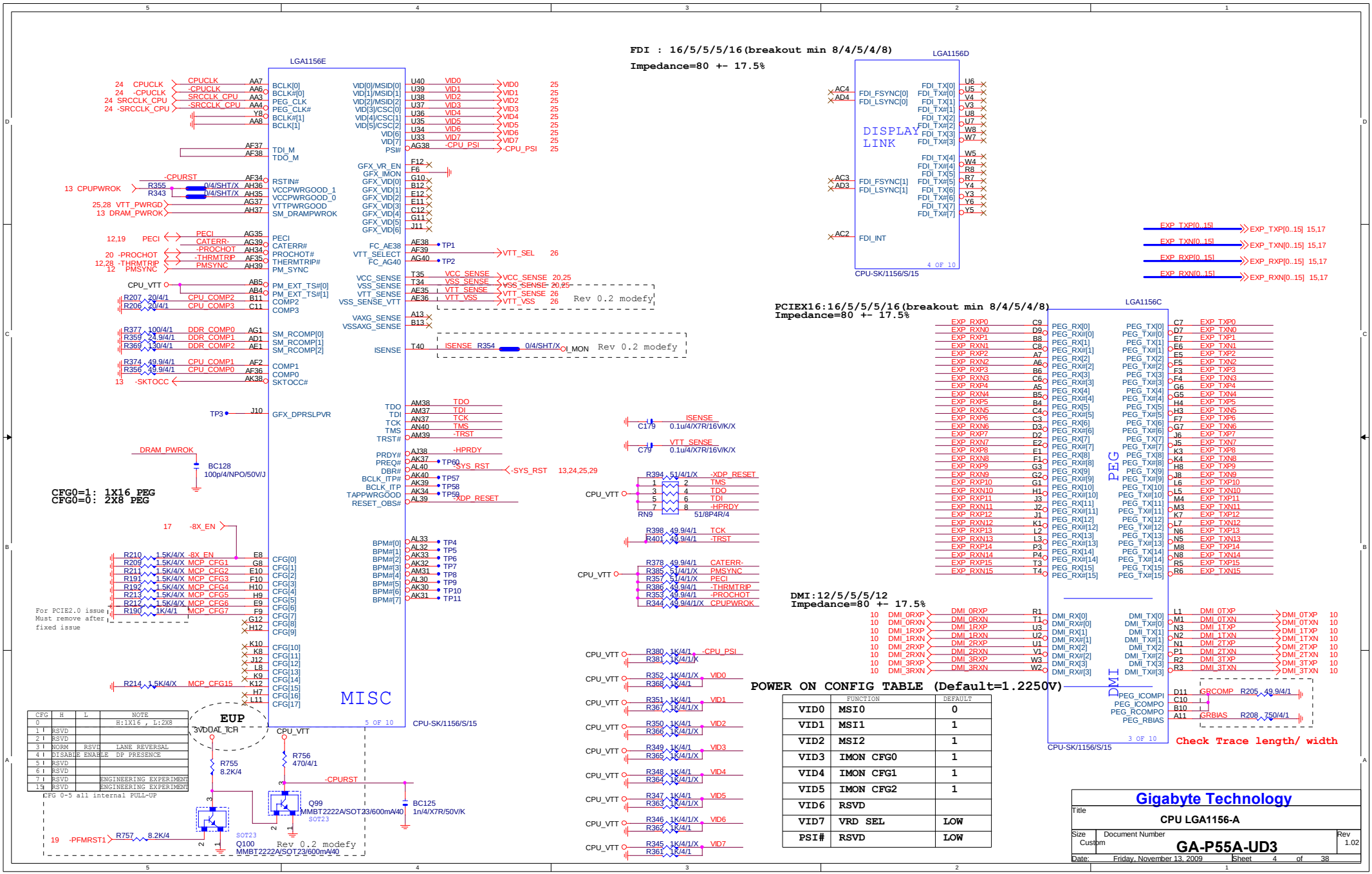

	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CFG0	1
VID4	IMON CFG1	1
VID5	IMON CFG2	1
VID6	RSVD	
VID7	VRD SEL	LOW
PSI#	RSVD	LOW

CFG	H	L	NOTE
0			H:1X16 , L:2X8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		
7	RSVD		ENGINEERING EXPERIMENT
15	RSVD		ENGINEERING EXPERIMENT

Title	CPU LGA1156-A
Size	Custom
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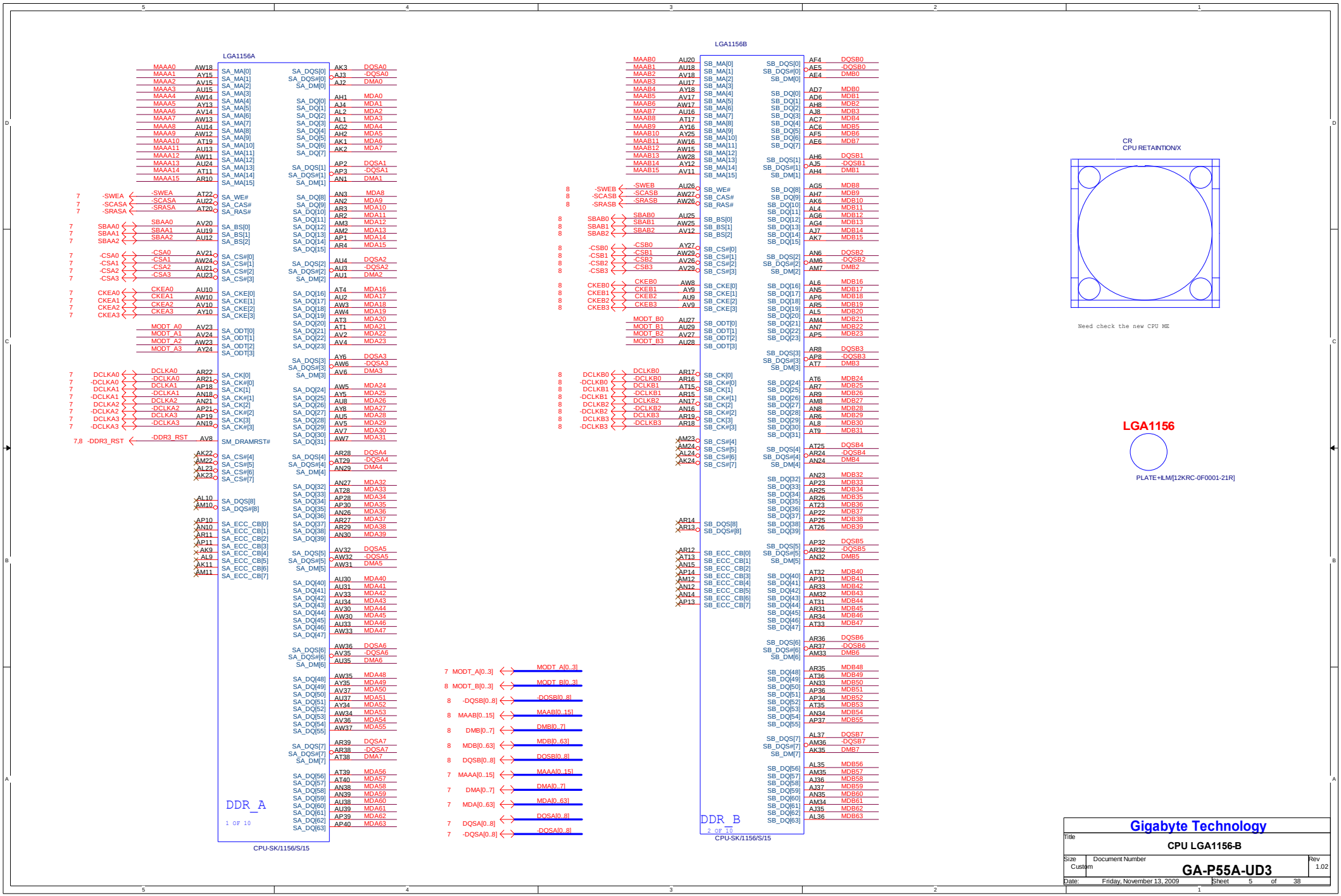

Title	CPU LGA1156-B
Size	Custom
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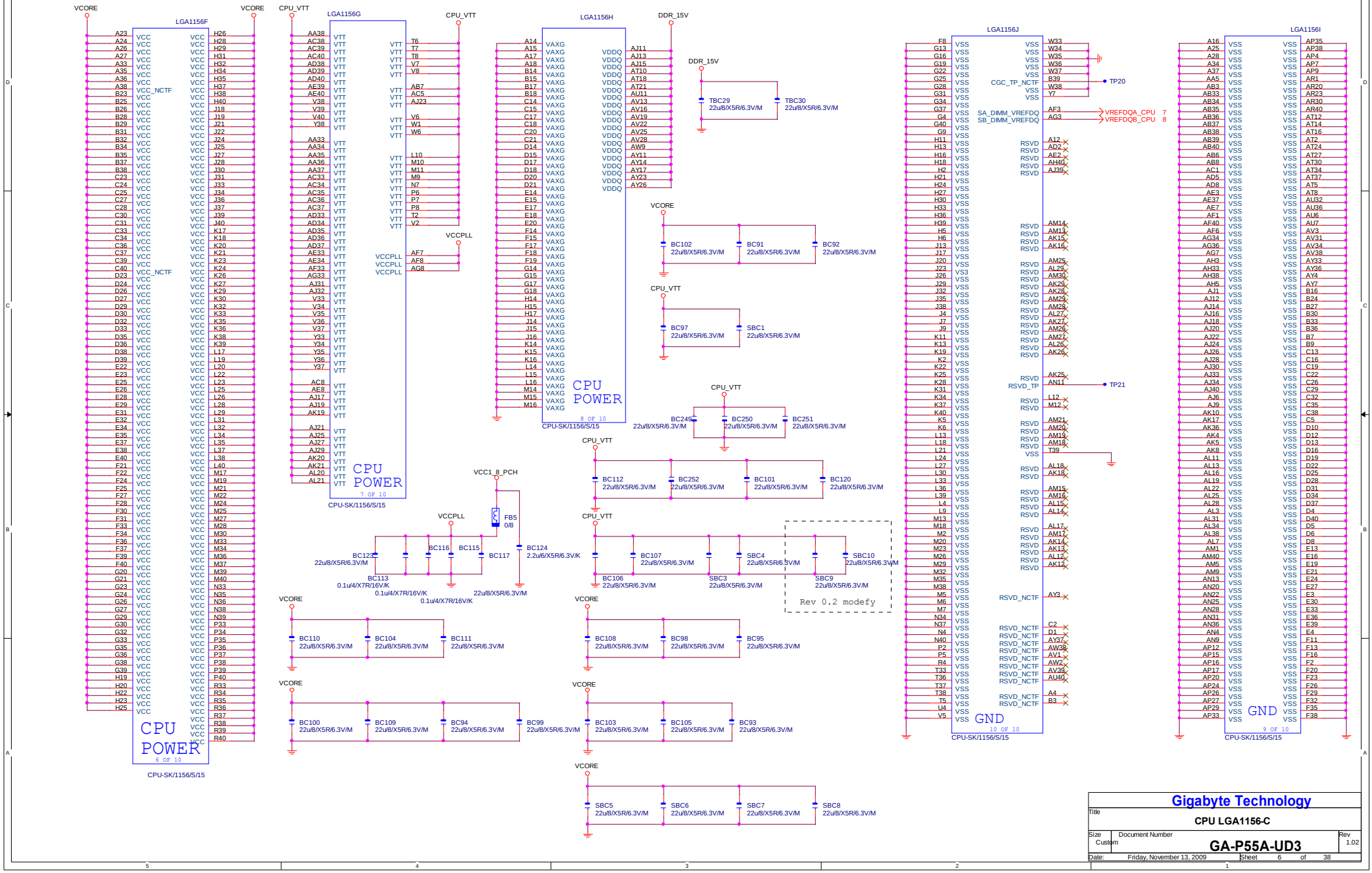

Gigabyte Technology	
Title	CPU LGA1156-C
Size: Custom	Document Number: GA-P55A-UD3
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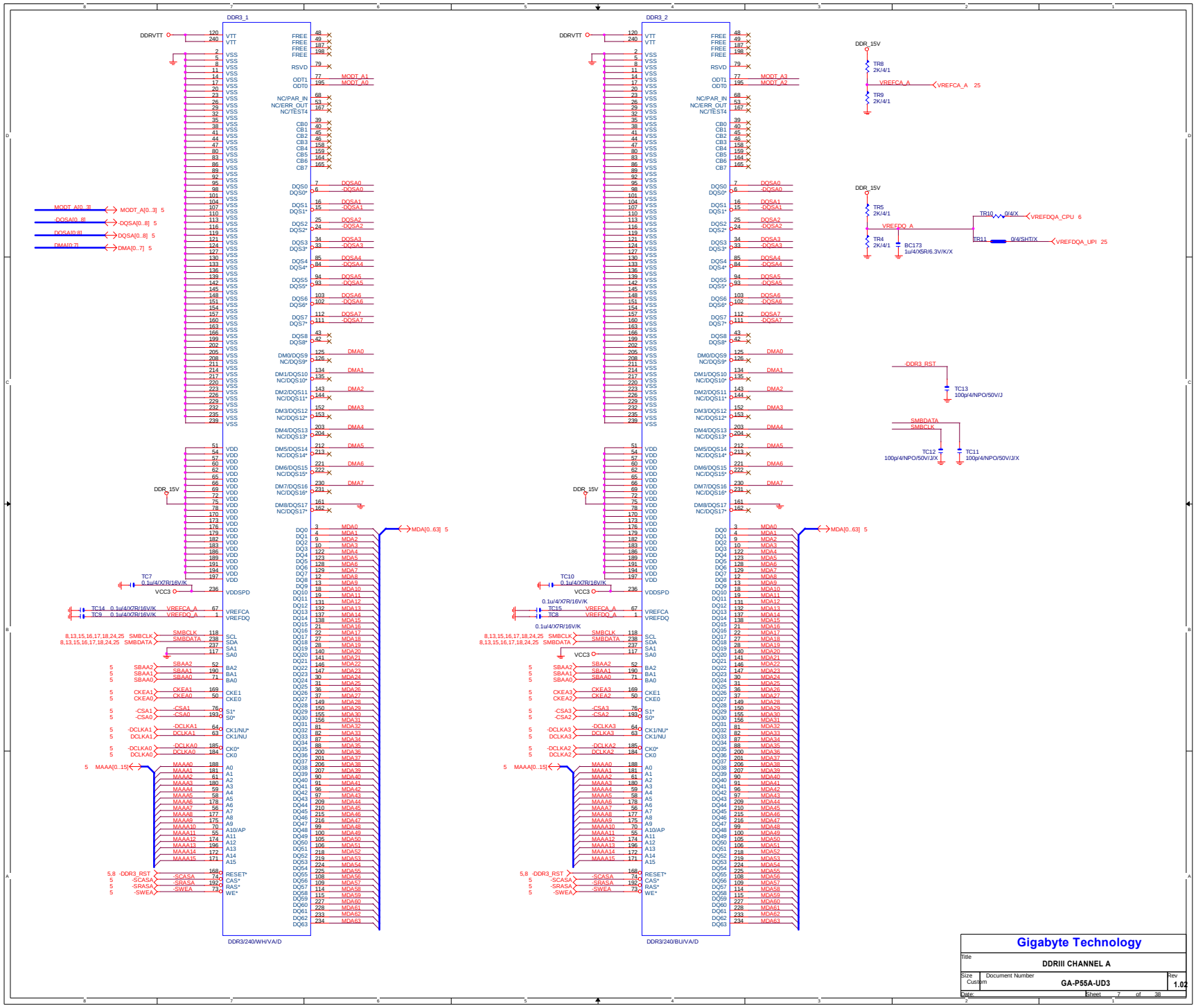
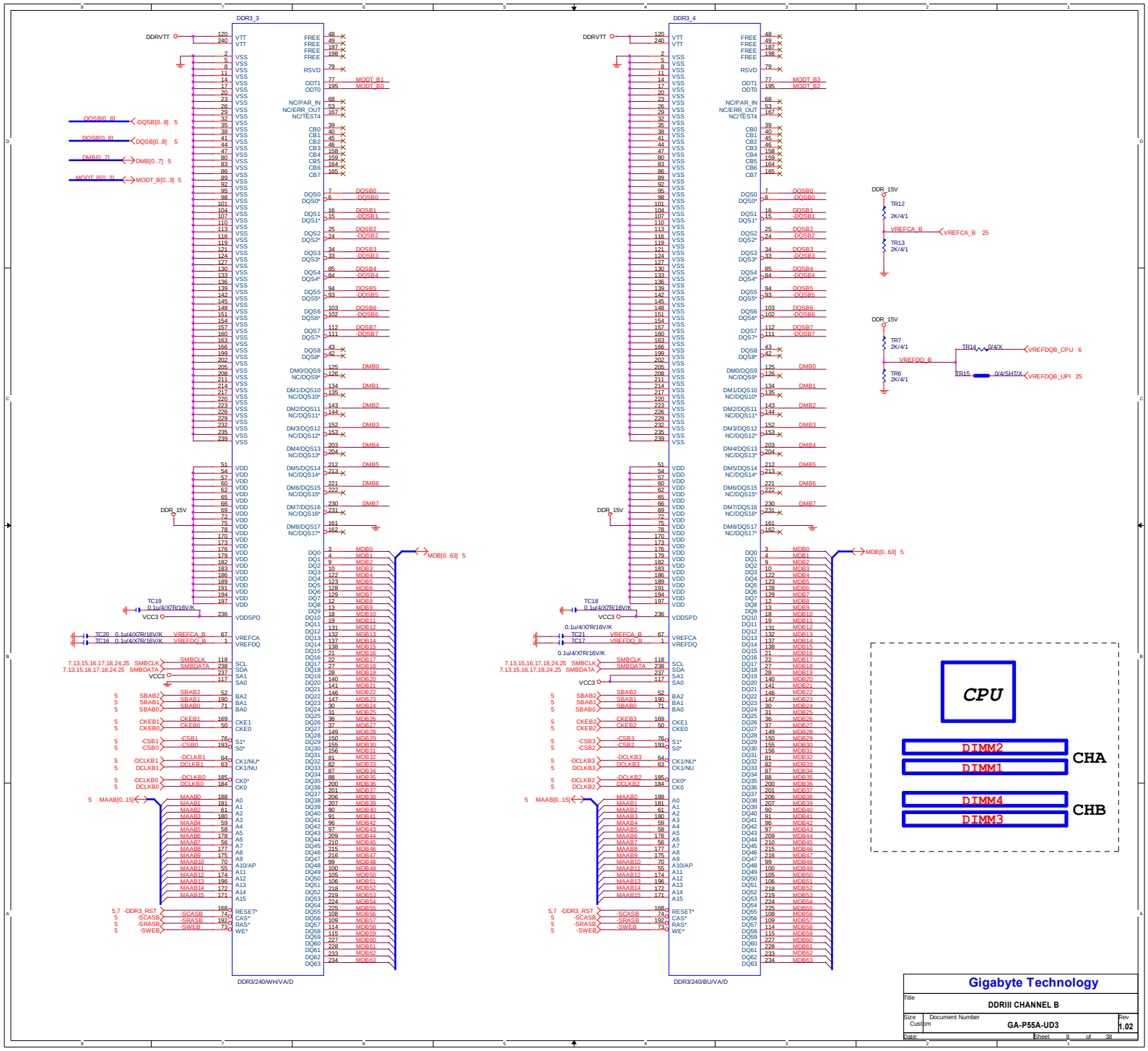
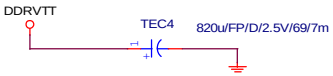
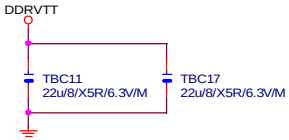
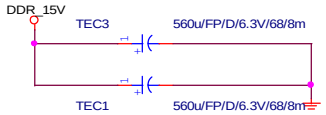


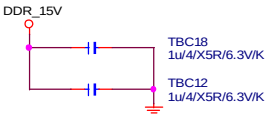


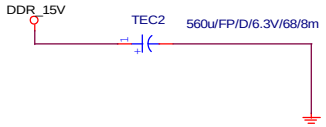
DDR TERMINATION CHANNEL A/B



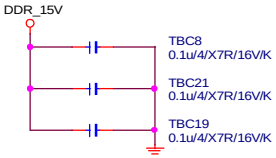




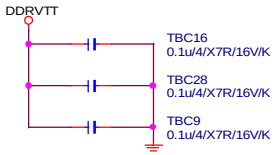


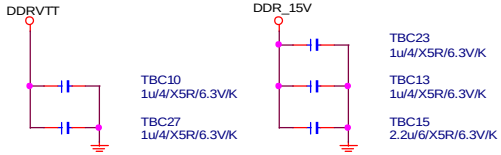


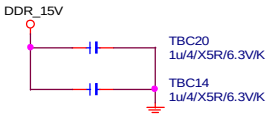
DDR15V Decouple

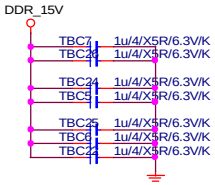


DDRVTT Decouple









Gigabyte Technology		
Title: DDRIII POWER CAP		
Size: B	Document Number: GA-P55A-UD3	Rev: 1.02
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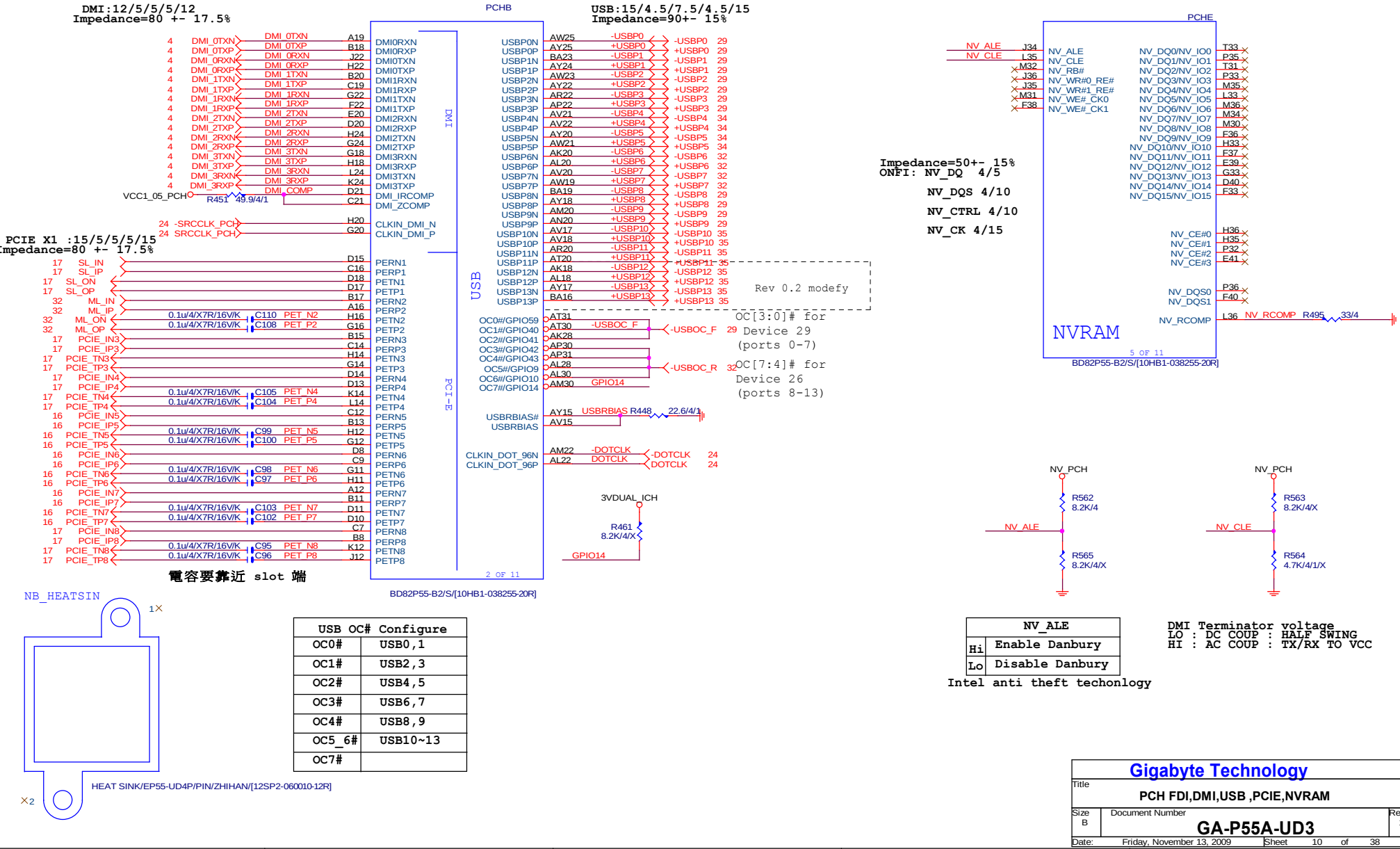
DMI:12/5/5/5/12
Impedance=80 +- 17.5%

PCIE X1 :15/5/5/5/15
Impedance=80 +- 17.5%

USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%



電容要靠近 slot 端

Rev 0.2 modefy

OC[3:0]# for Device 29 (ports 0-7)

OC[7:4]# for Device 26 (ports 8-13)

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5_6#	USB10~13
OC7#	

Impedance=50+- 15%
ONFI: NV_DQ 4/5
NV_DQS 4/10
NV_CTRL 4/10
NV_CK 4/15

NV_ALE	
Hi	Enable Danbury
Lo	Disable Danbury

Intel anti theft techonlogy

DMI Terminator voltage
LO : DC COUP : HALF SWING
HI : AC COUP : TX/RX TO VCC

Gigabyte Technology	
Title	PCH FDI,DMI,USB ,PCIE,NVRAM
Size B	Document Number GA-P55A-UD3 Rev 1.02
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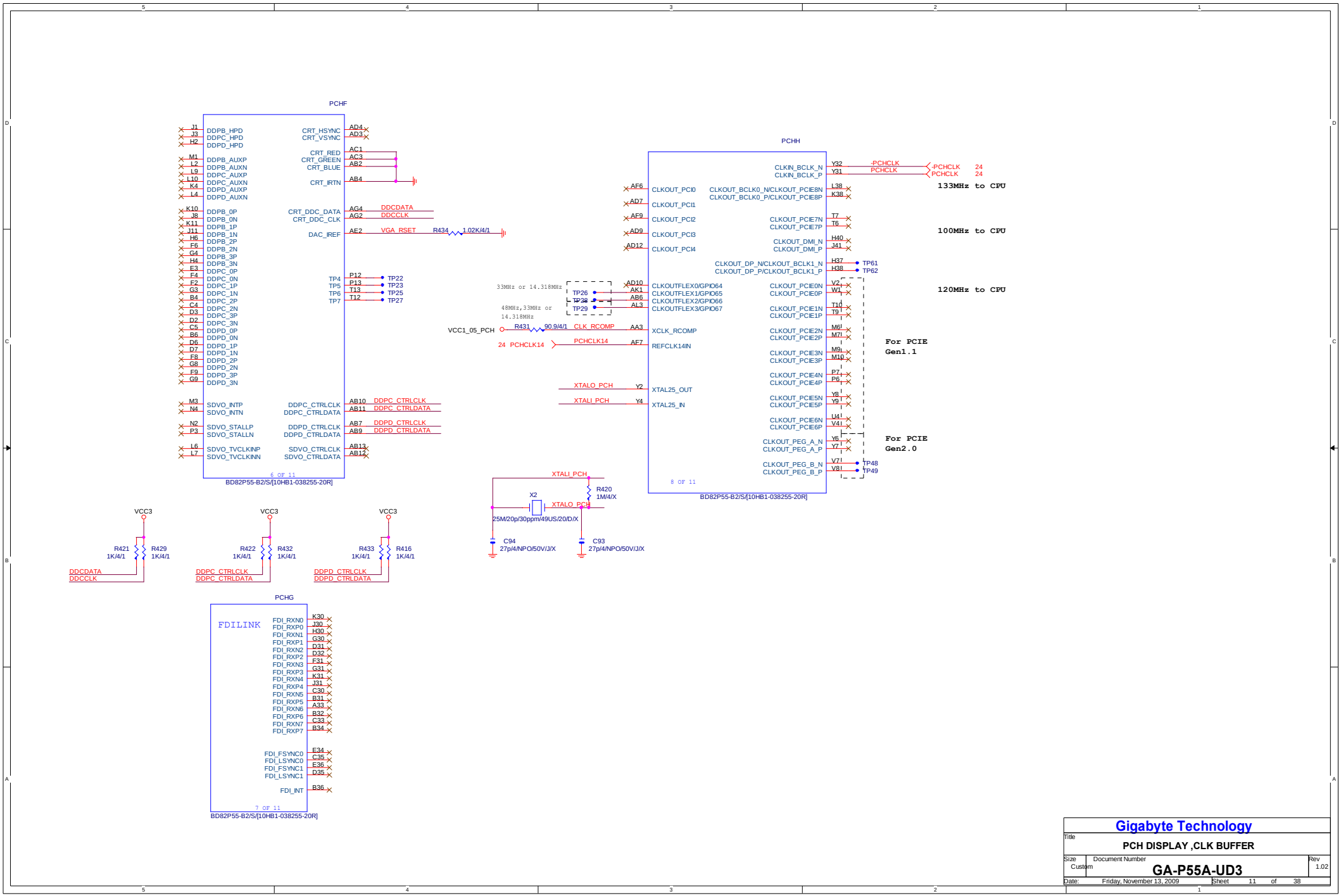

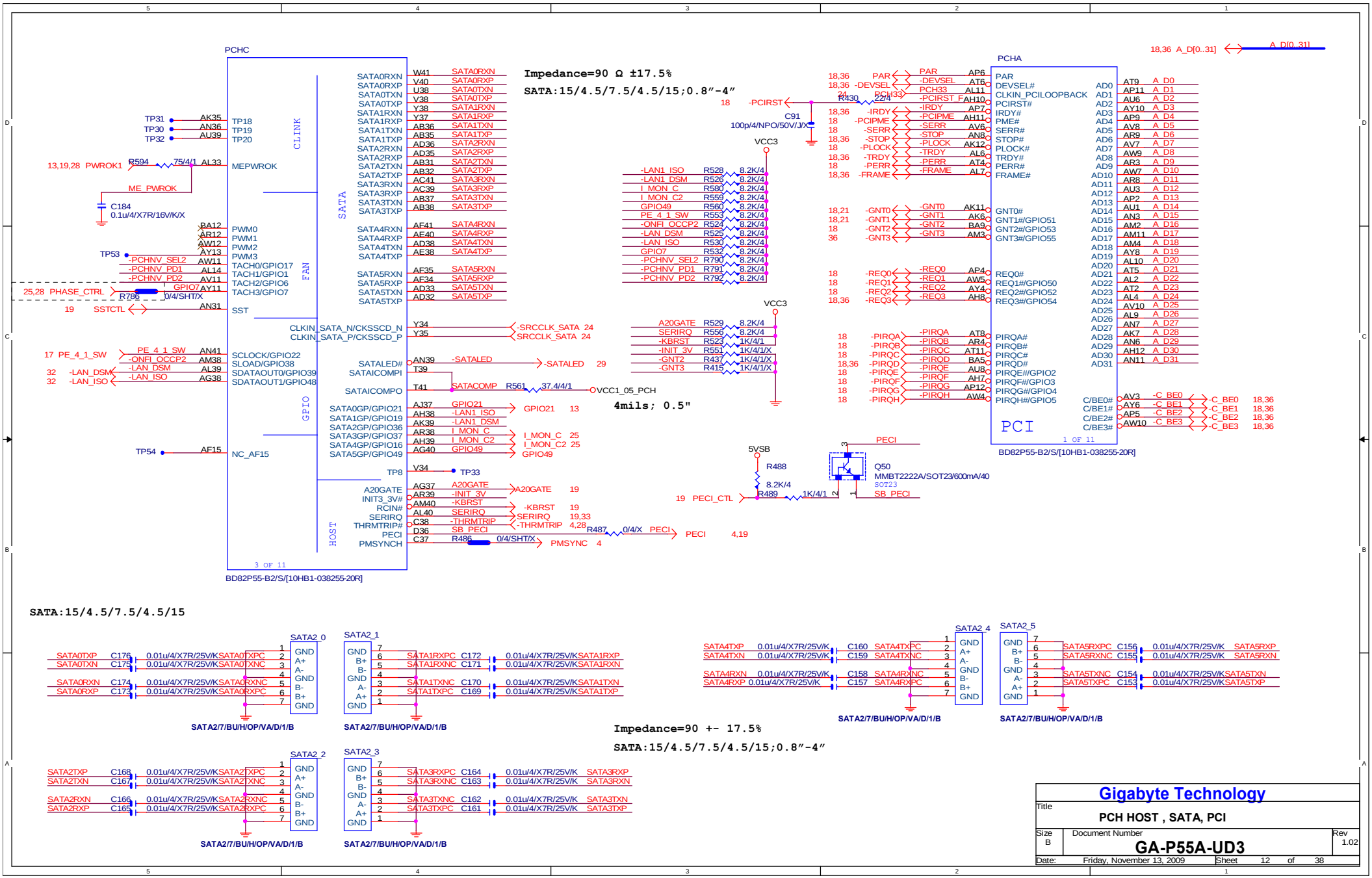

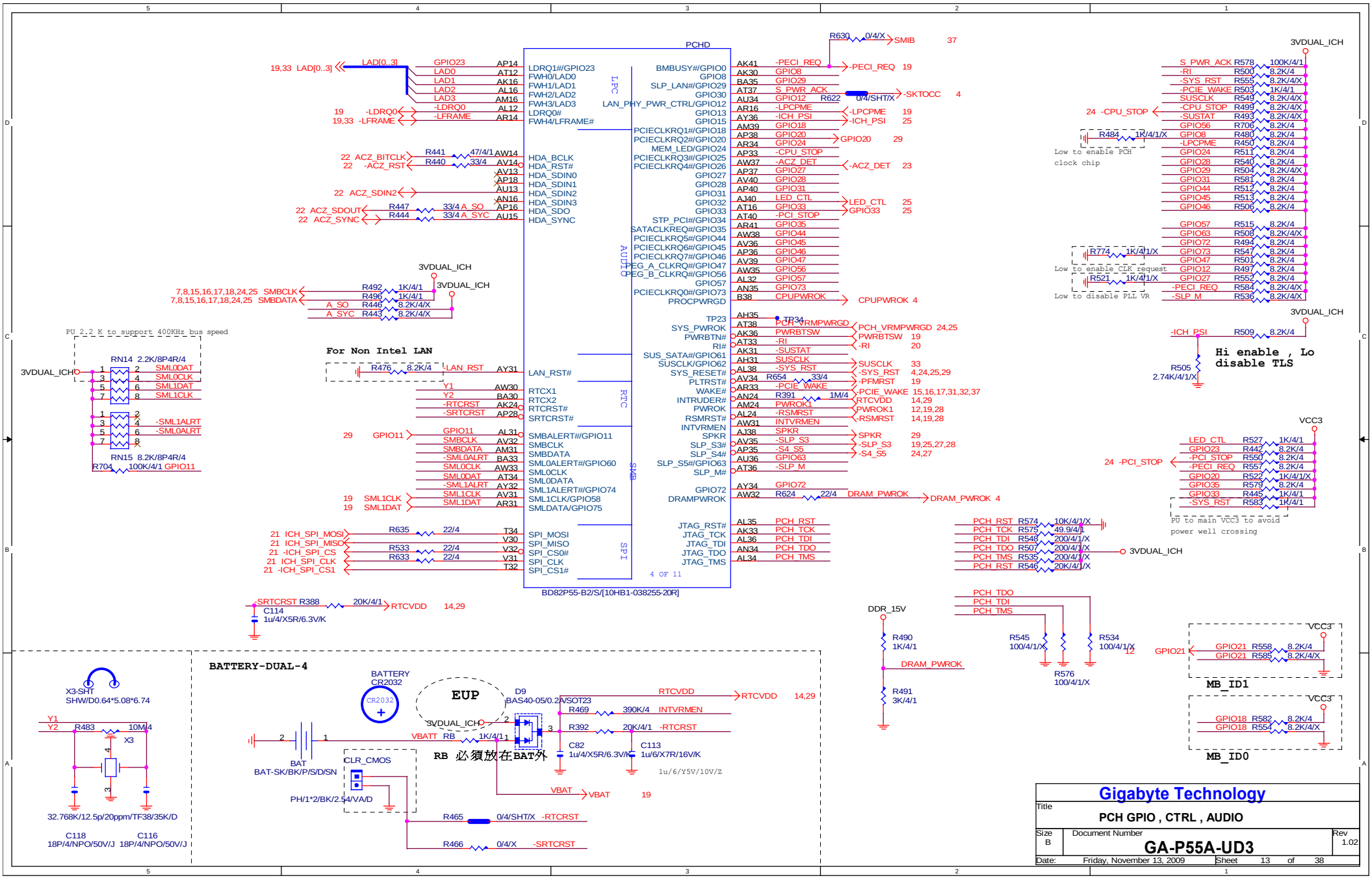

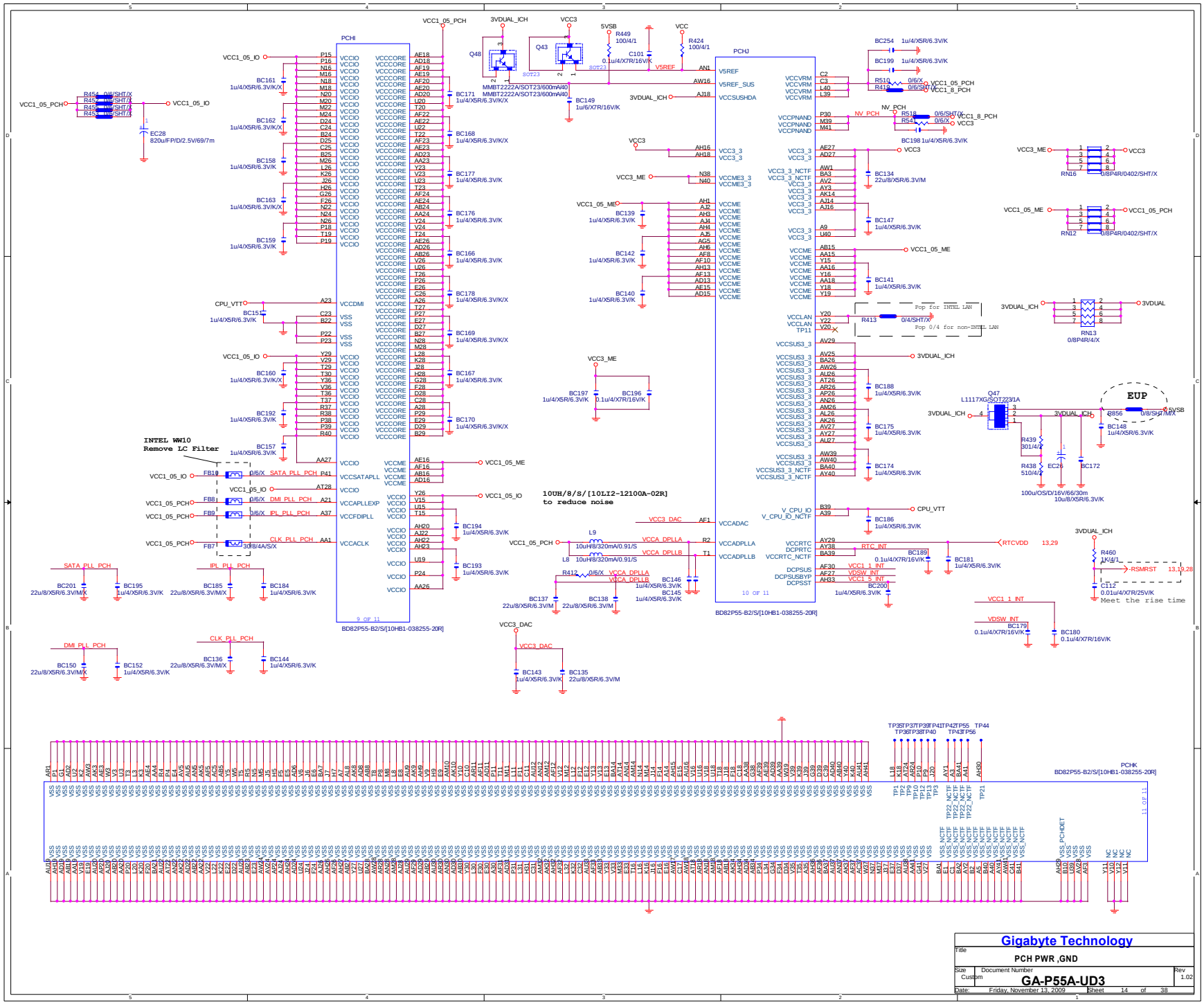

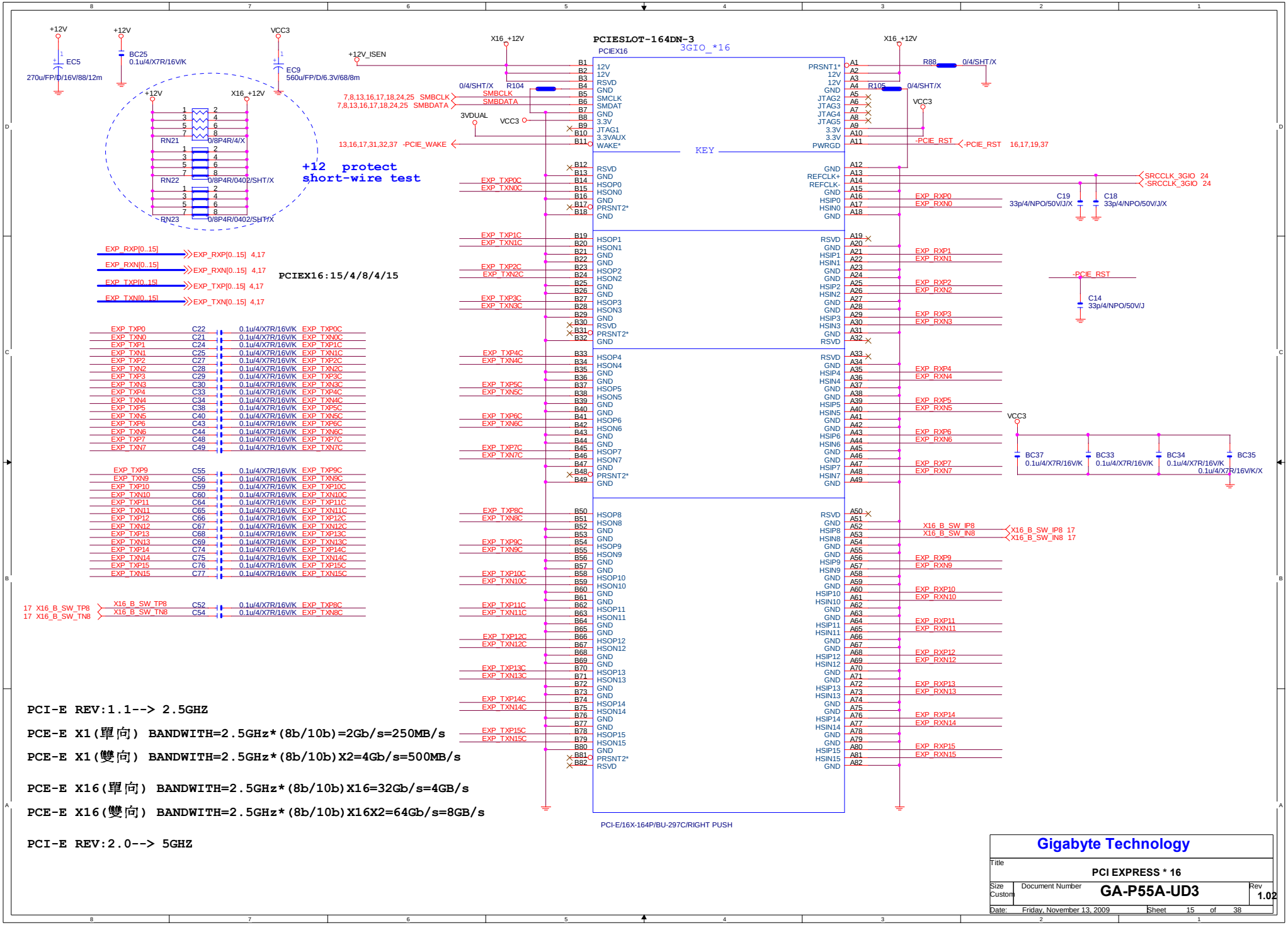

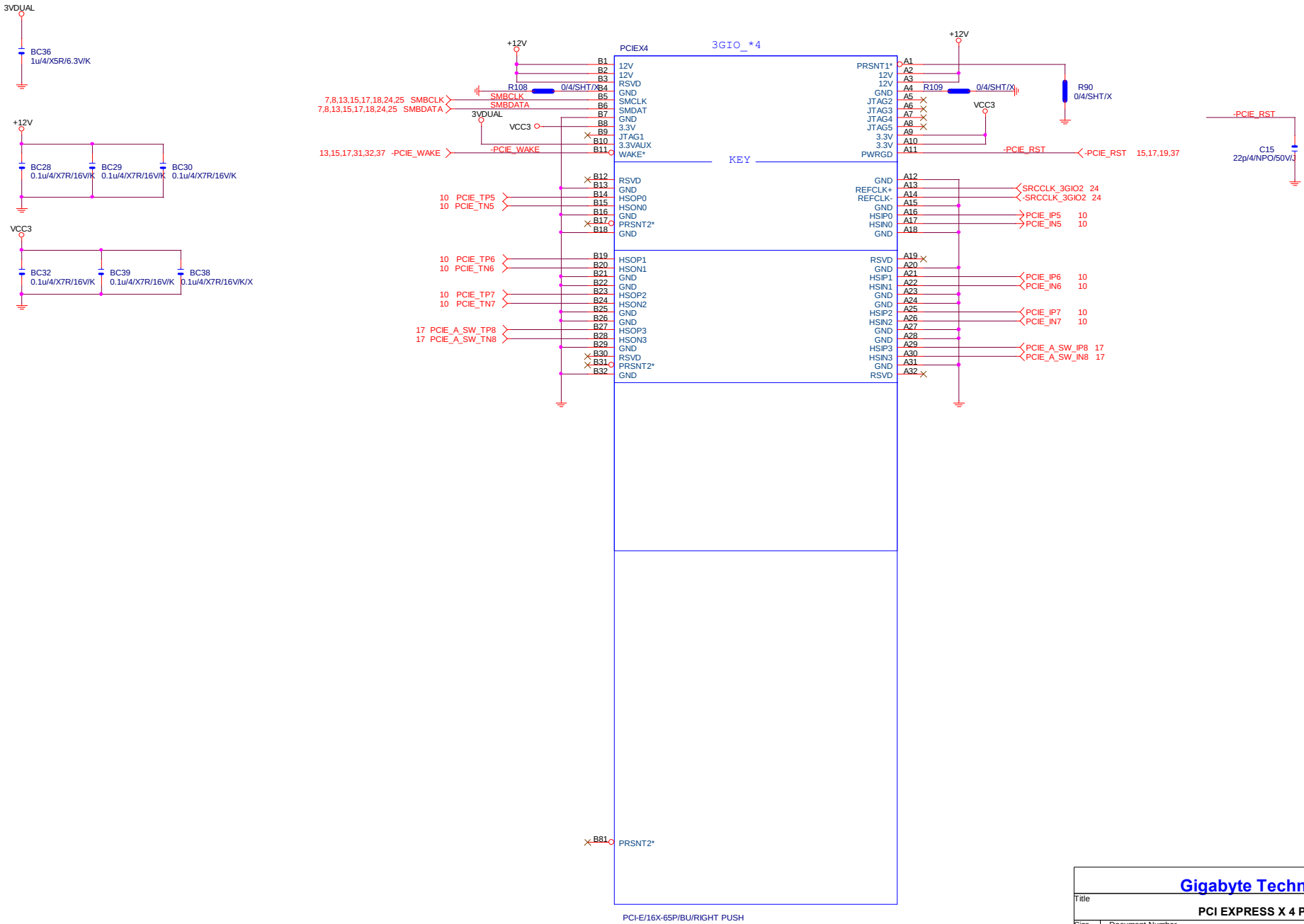

Gigabyte Technology

Title: **PCI EXPRESS X 4 PORT**

Size: Custom | Document Number: **GA-P55A-UD3** | Rev: **1.02**

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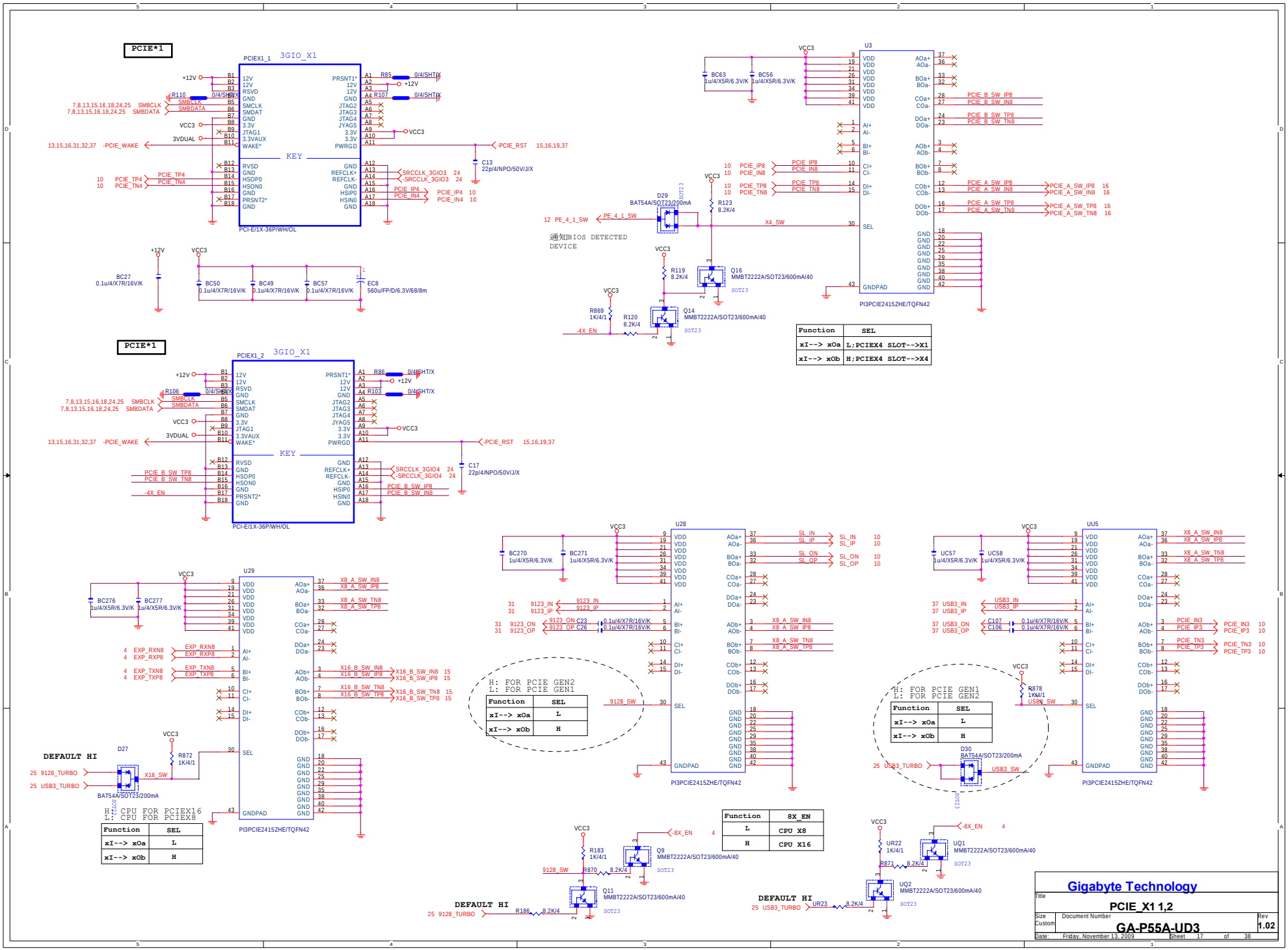

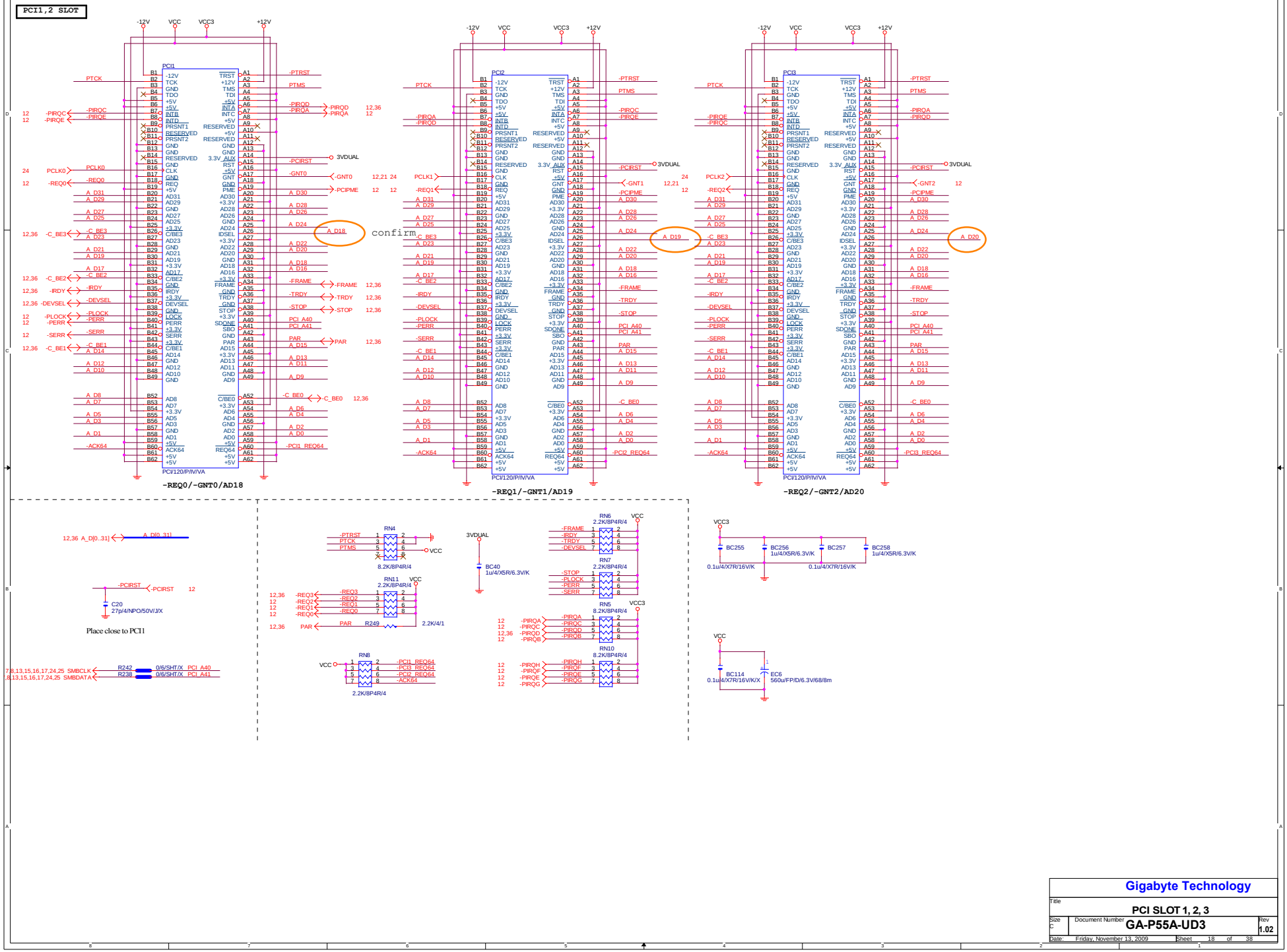

Gigabyte Technology	
Title	PCI SLOT 1, 2, 3
Size C	Document Number GA-P55A-UD3
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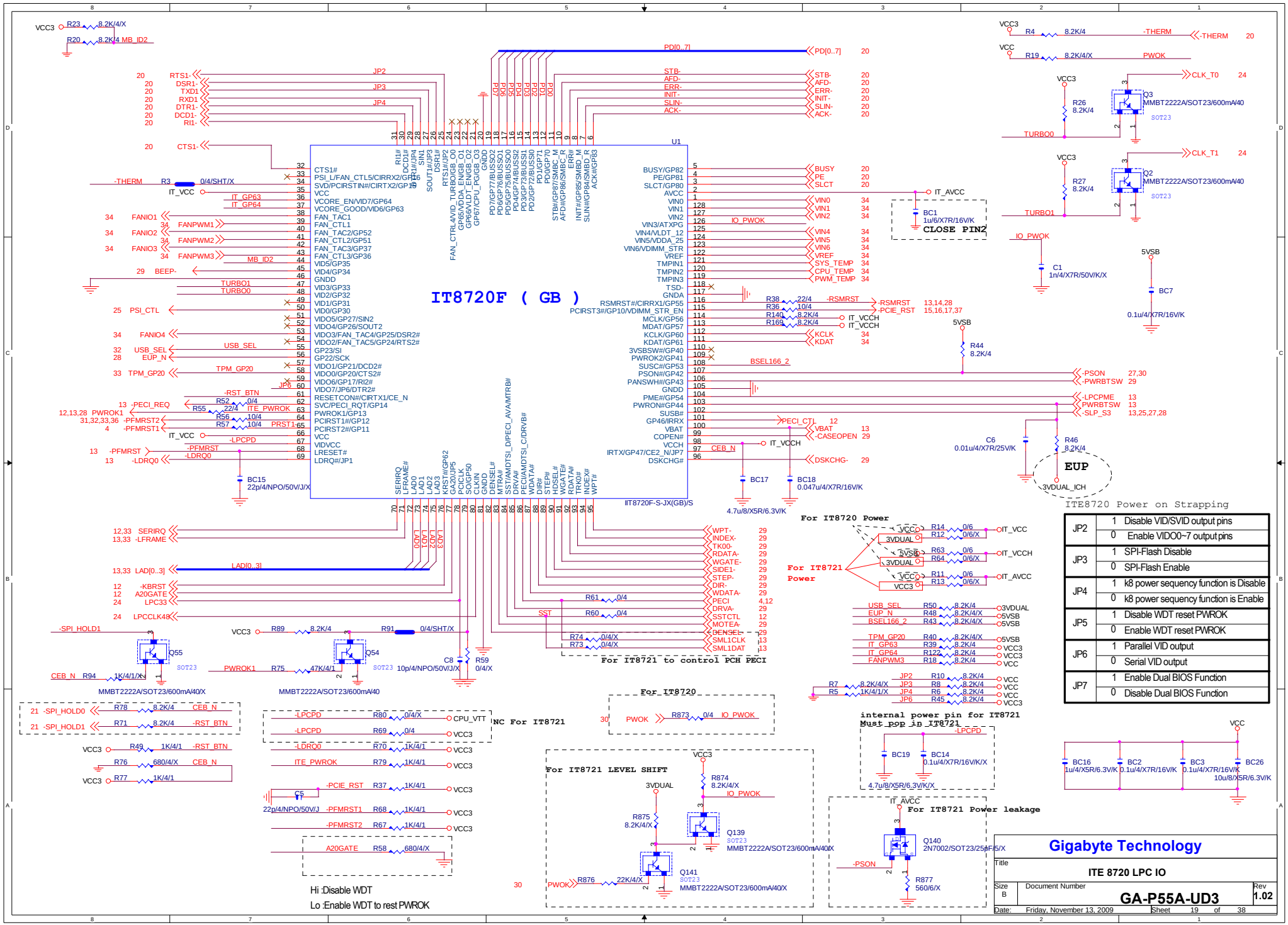

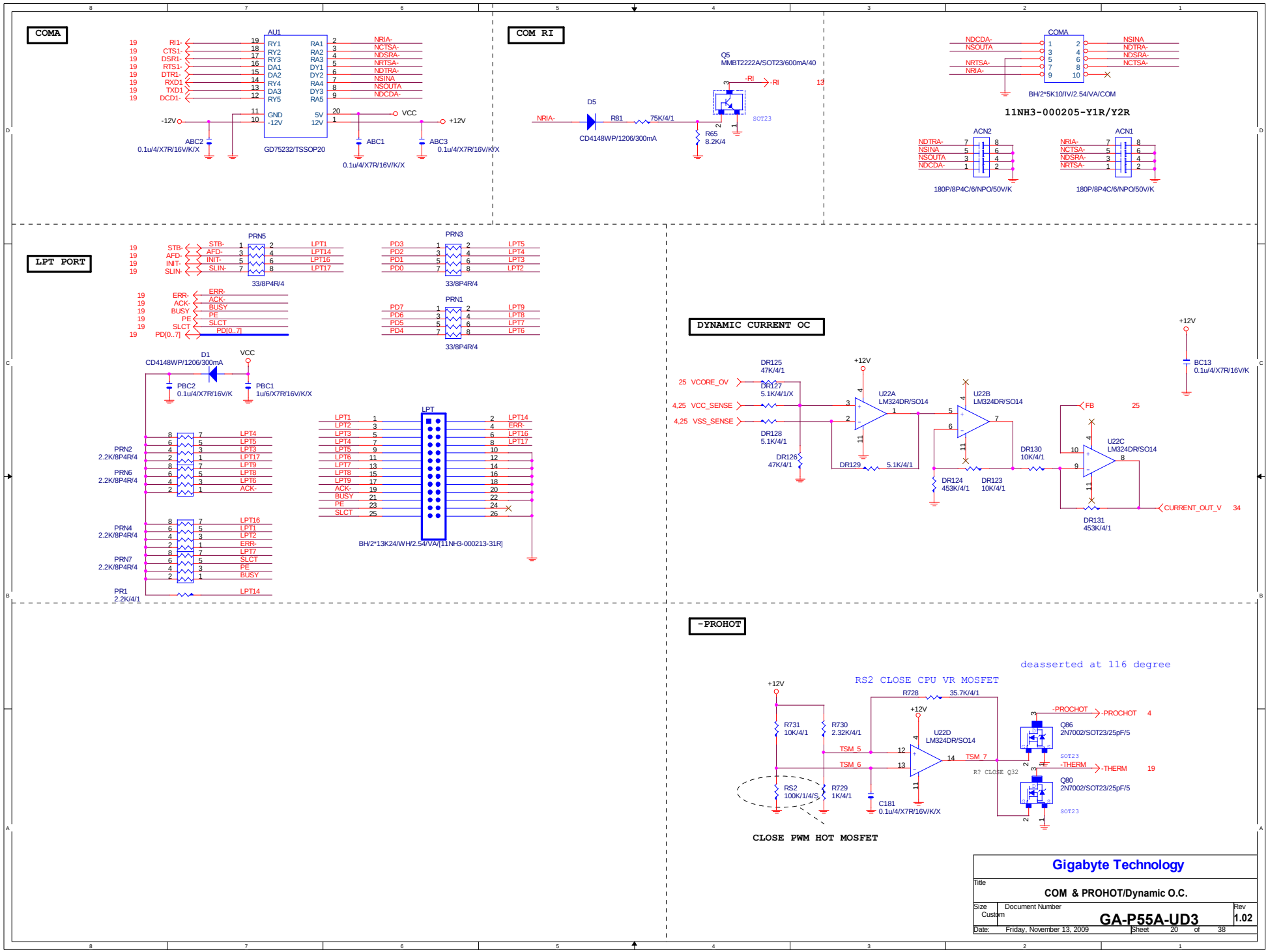

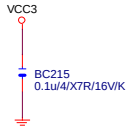

r1.0 DG;0.7 CRB

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

IC8SO-SOCKET

Gigabyte Technology			
Title: BIOS			
Size: Custom	Document Number: GA-P55A-UD3		Rev: 1.02
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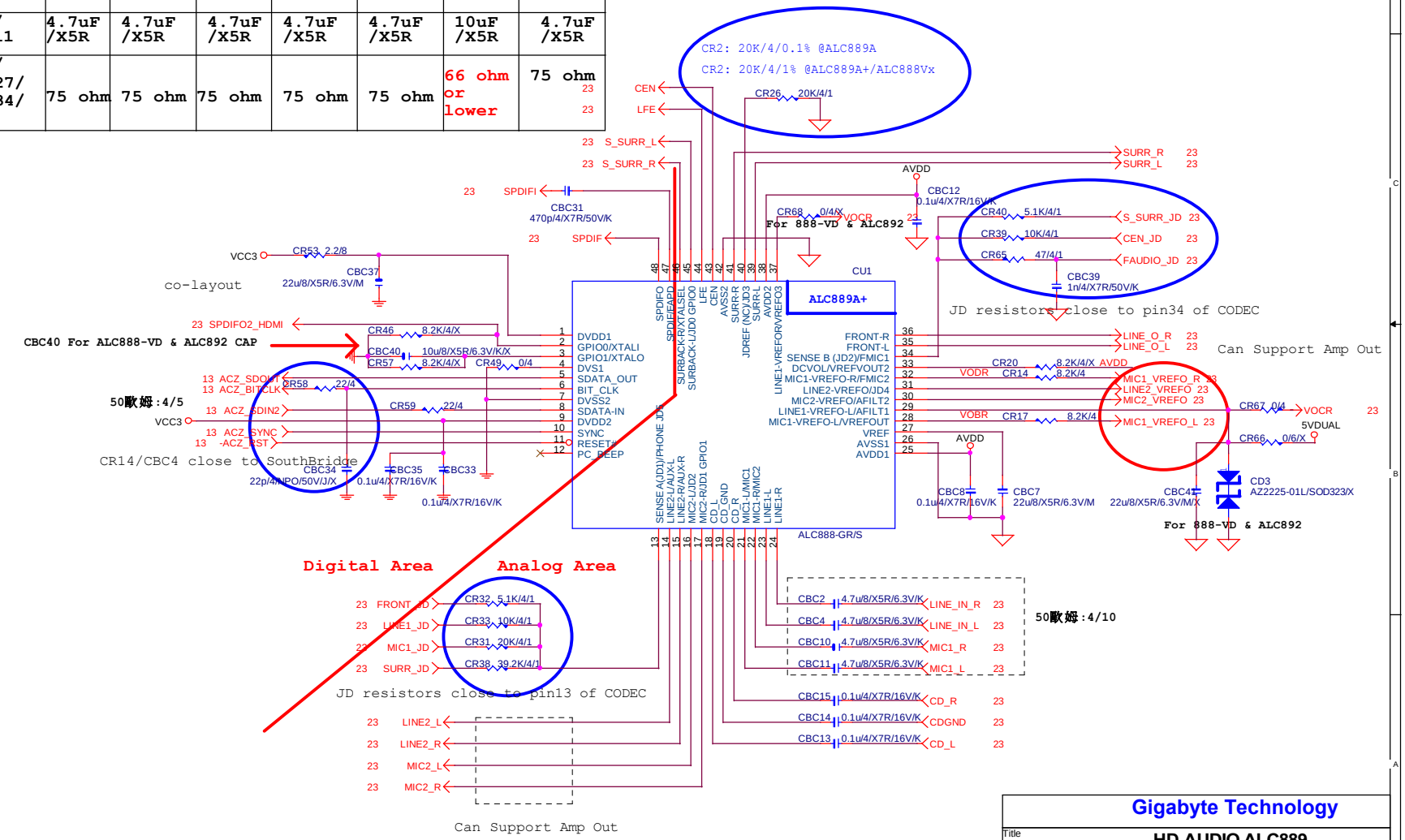
AZALIA CODEC *ALC889A+/ALC889A/ALC888Vx Colay*

	ALC883	ALC888-VA	ALC888B	ALC888-VD	ALC892	ALC889	ALC889A
CR46	X	X	X	X	X	X	O
CR57	X	X	X	X	X	X	O
CR49	O	O	X	X	X	O	O
CBC40	X	X	X	10uF/X5R	10uF/X5R	X	X
CR20	O	X	X	X	X	X	X
CR26	20K/1%	20K/1%	20K/1%	20K/1%	20K/1%	20K/1%	20K/0.1%
CR47	X	X	X	X	O	O	X
CR48	O	O	O	O	X	X	O
CBC2/CBC4/CBC5/ CBC6/CBC10/CBC11	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR1/CR3/CR10/CR12/ CR15/CR19/CR56/CR27/ CR55/CR37/CR28/CR34/ CR6/CR9/CR51/CR61	75 ohm	75 ohm	75 ohm	75 ohm	75 ohm	66 ohm or lower	75 ohm



Gigabyte Technology

Title: **HD AUDIO ALC889**

Size: Custom | Document Number: **GA-P55A-UD3** | Rev: **1.02**

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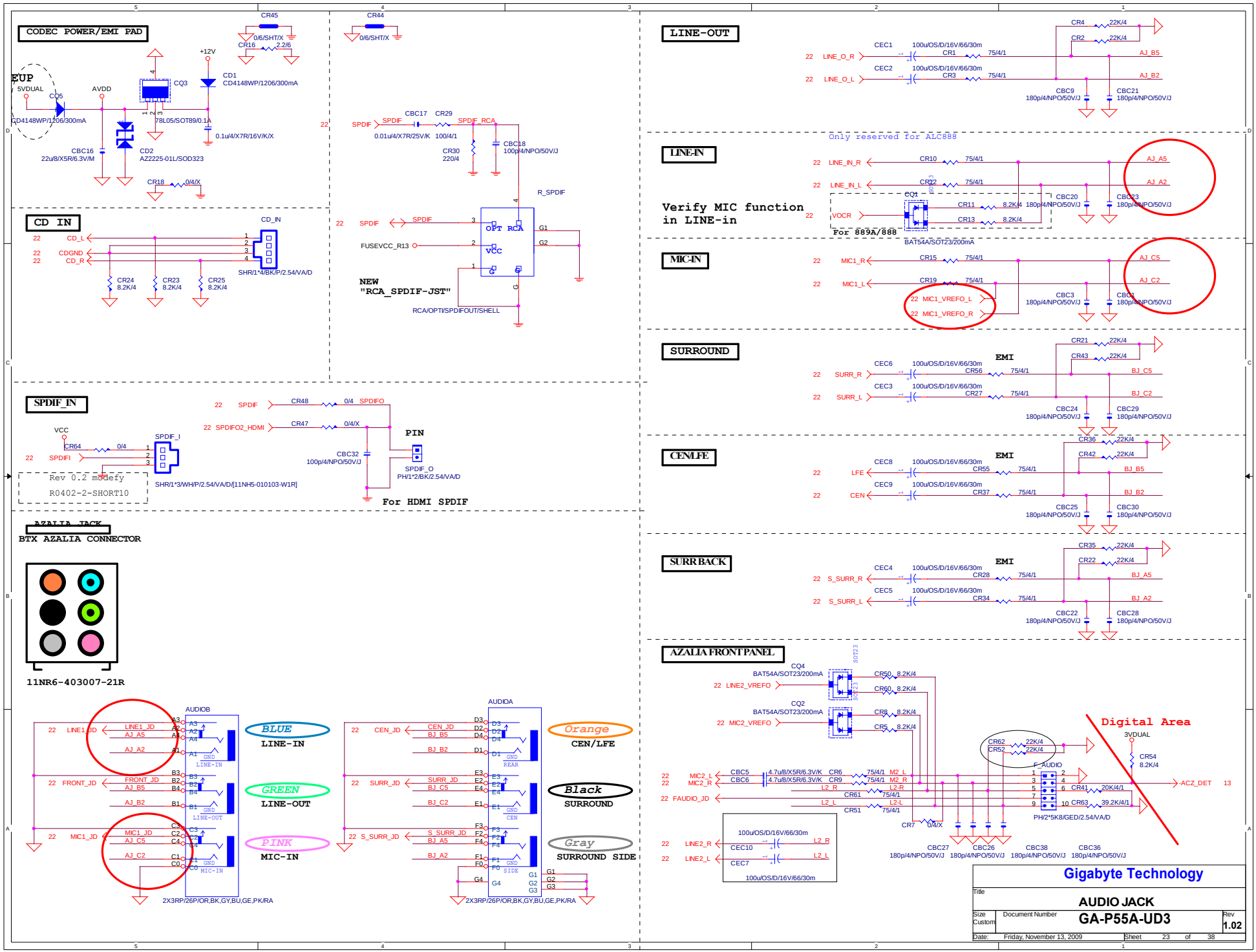
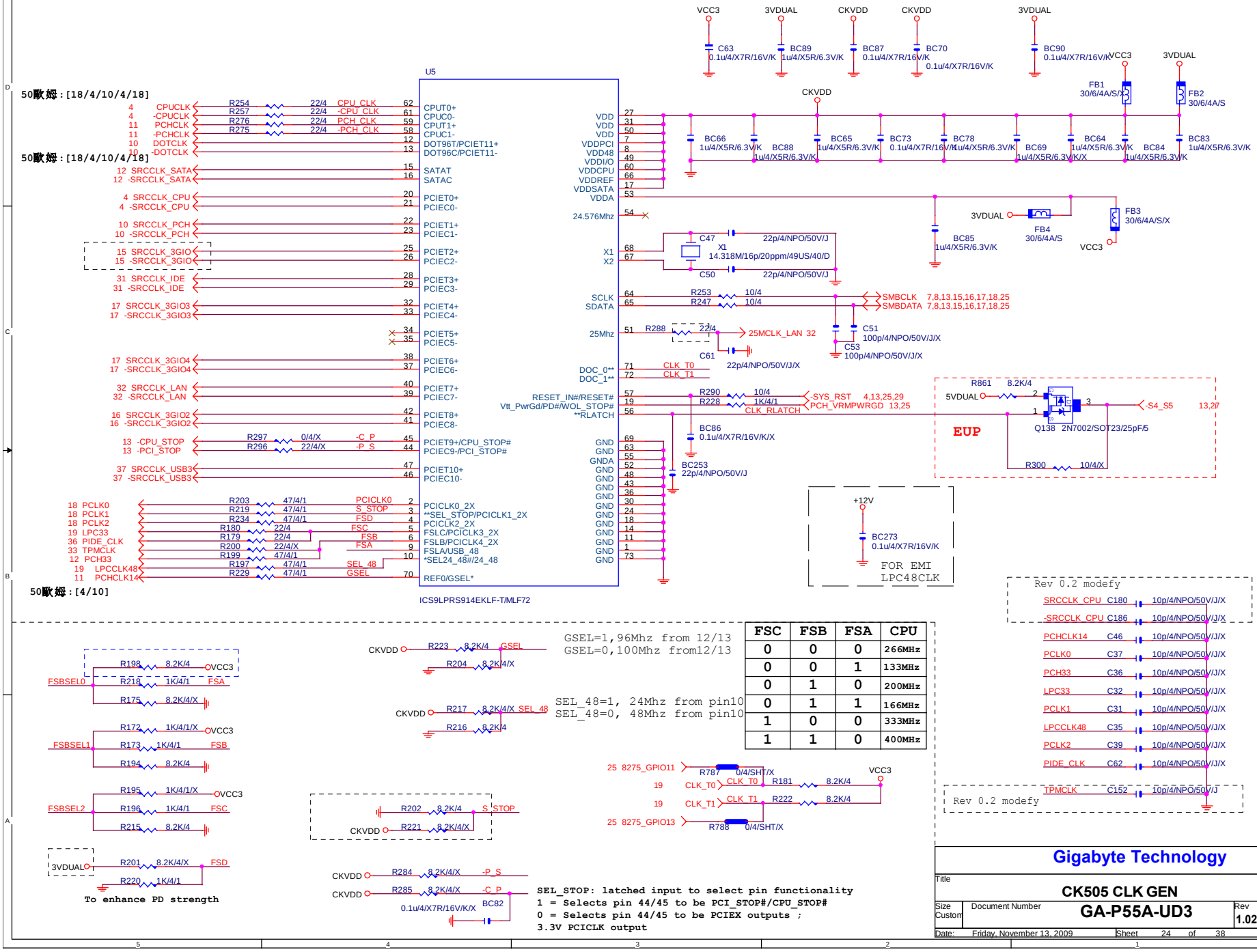


CLK GEN CK505



FSC	FSB	FSA	CPU
0	0	0	266MHz
0	0	1	133MHz
0	1	0	200MHz
0	1	1	166MHz
1	0	0	333MHz
1	1	0	400MHz

Gigabyte Technology

Title: CK505 CLK GEN

Size: Custom | Document Number: GA-P55A-UD3 | Rev: 1.02

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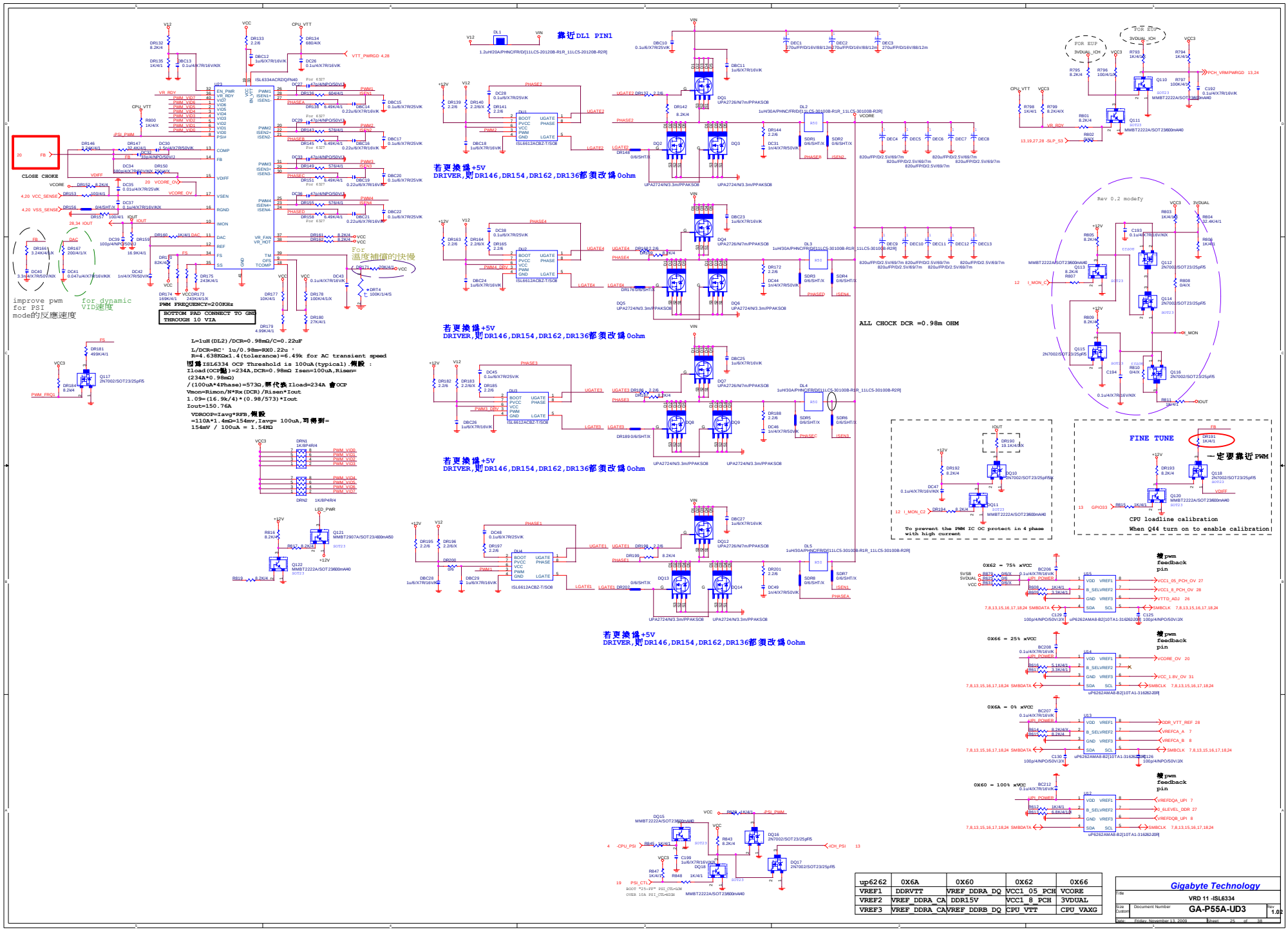
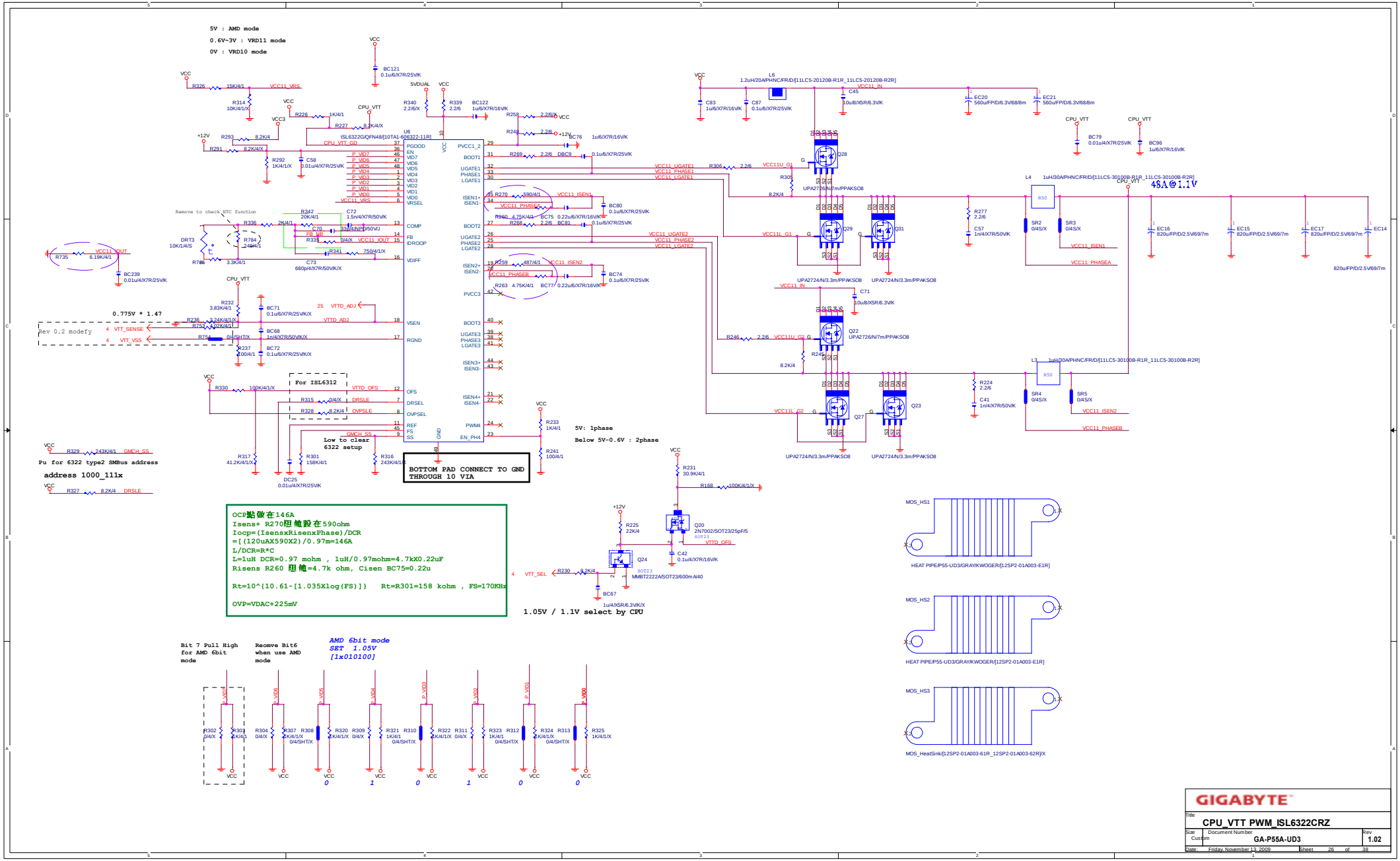
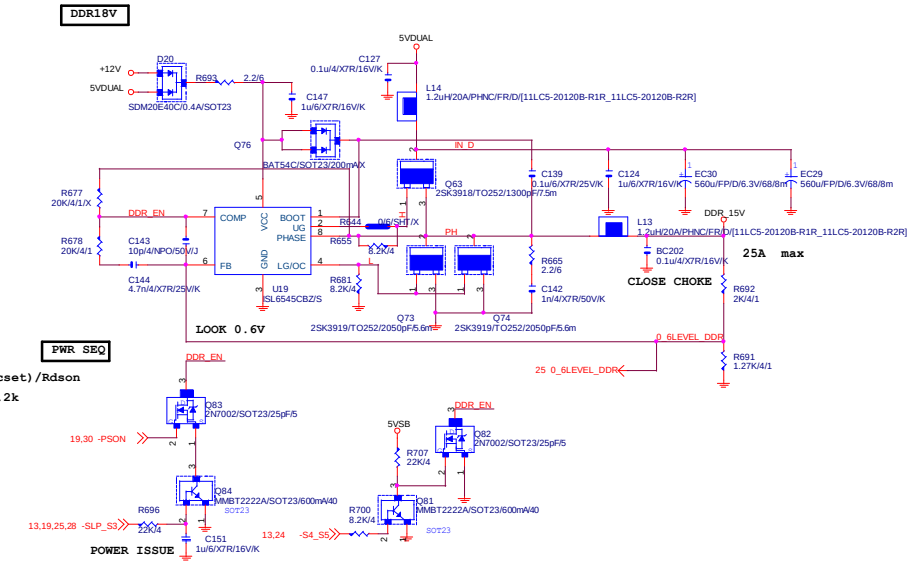
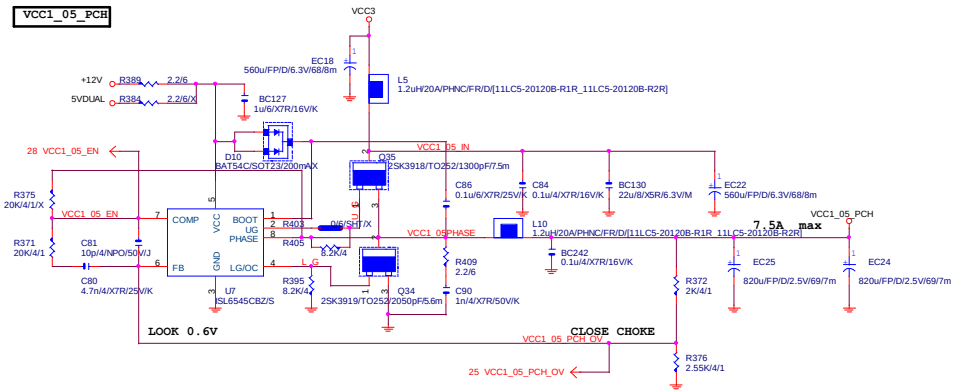


up6262	0X6A	0X60	0X62	0X66
VREF1	DDRVTT	VREF_DDRA_DQ	VCC1_05_PCH	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	3VDUAL
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	CPU_VTT	CPU_VAXG







Gigabyte Technology		
Title: DDR_15V		
Size: C	Document Number: GA-P55A-UD3	Rev: 1.02
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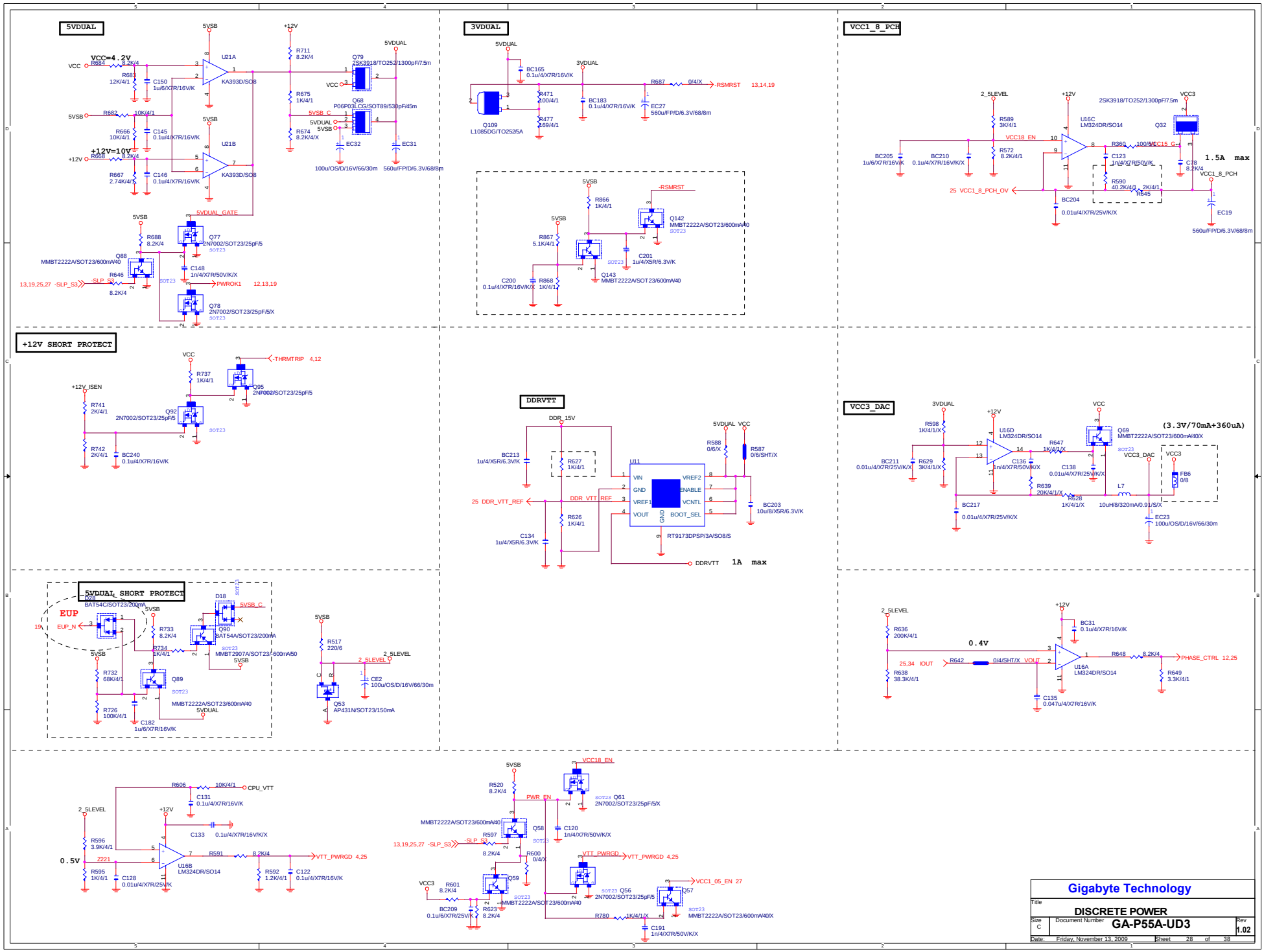
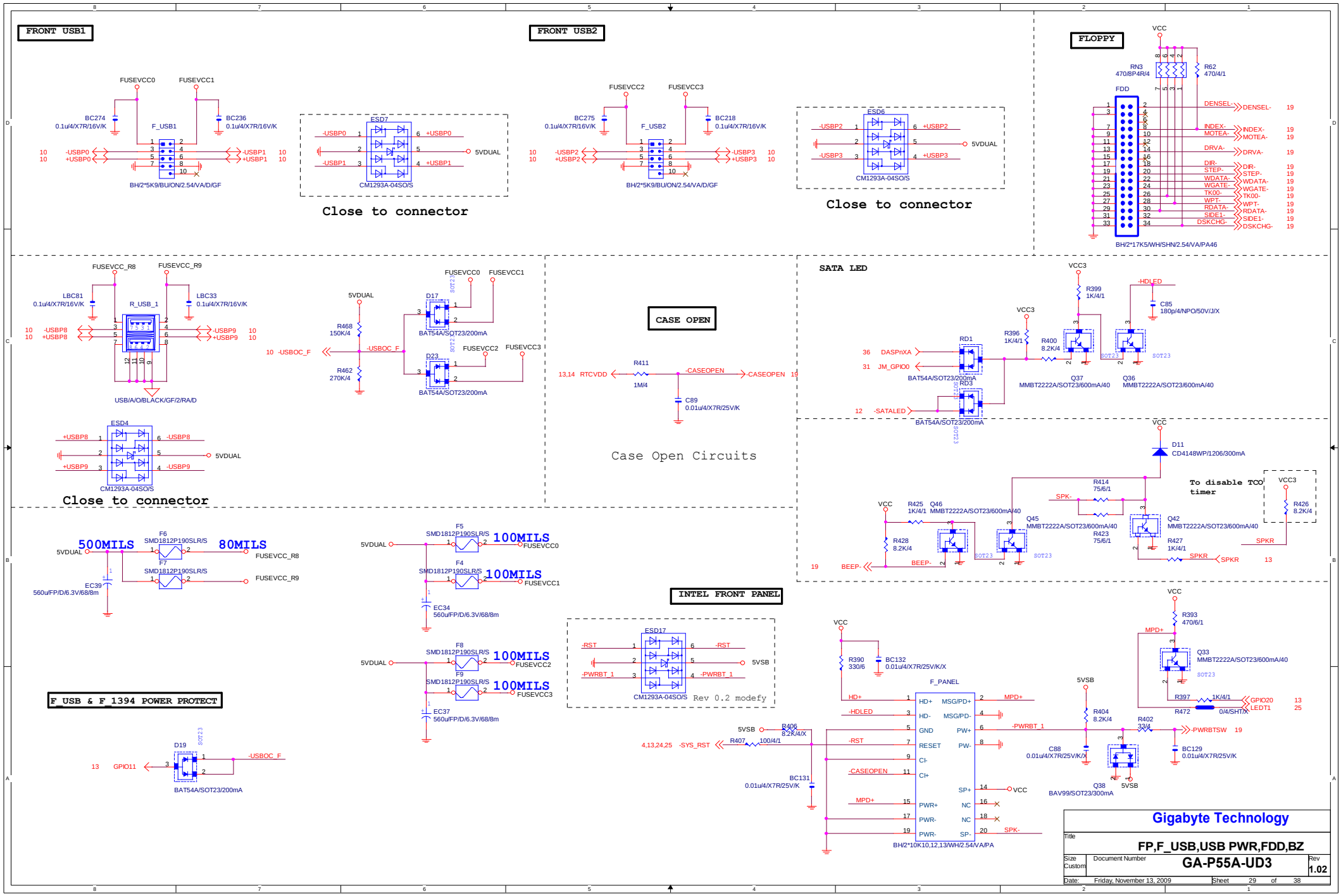
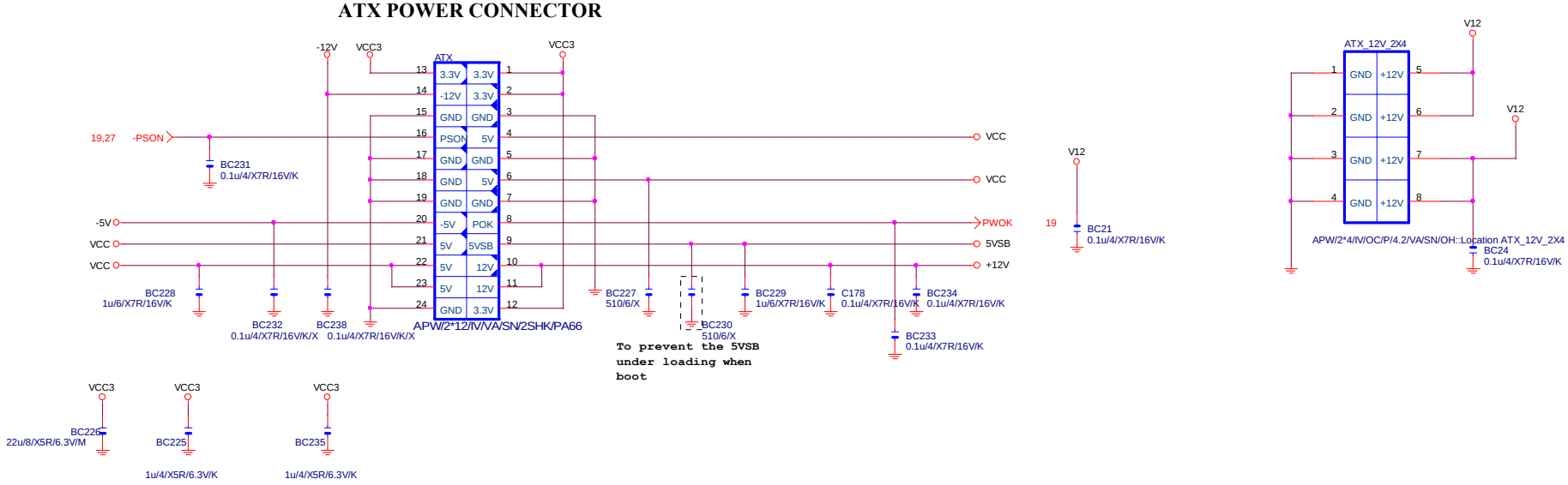
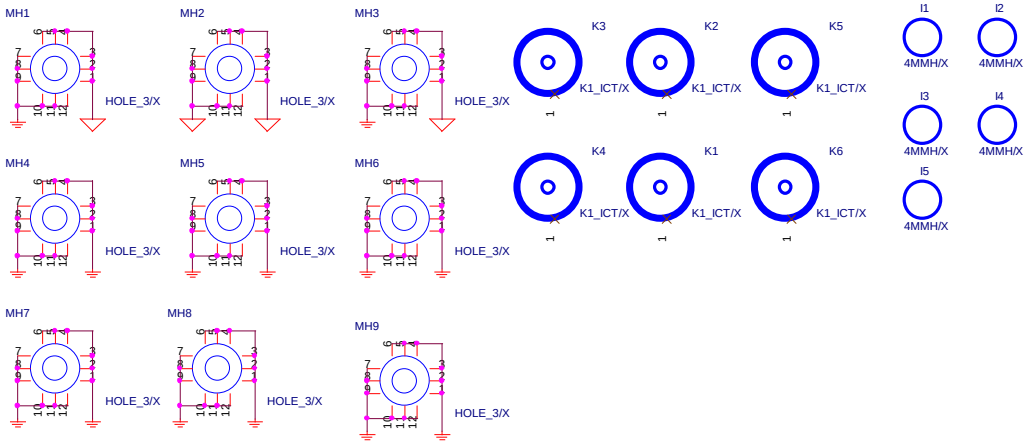




ATX POWER CONNECTOR





Gigabyte Technology			
Title: ATX POWER CONNECTOR			
Size: B	Document Number: GA-P55A-UD3		Rev: 1.02
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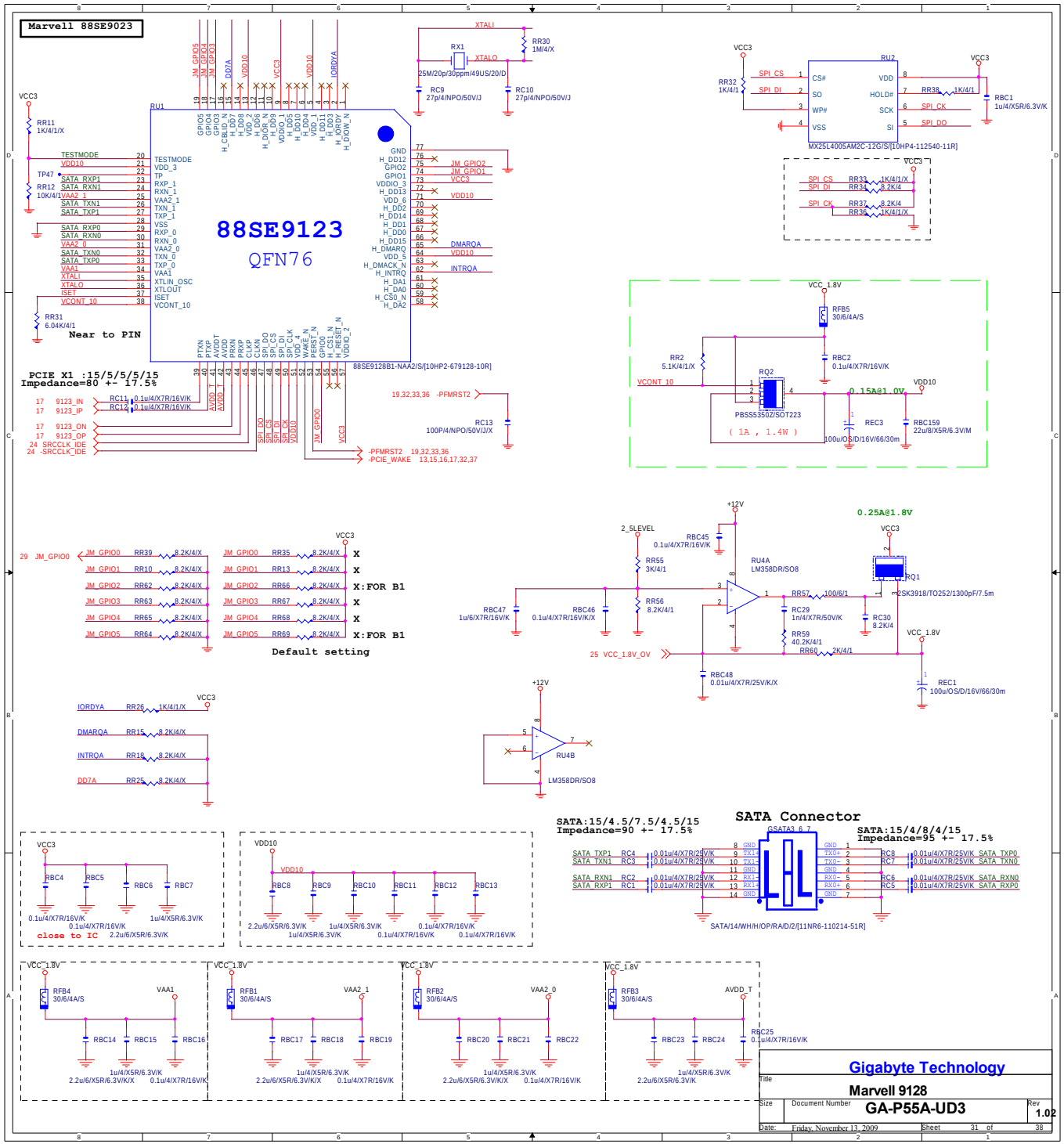

PCIE-1G LAN

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
VDD15	1.5V	1.2V

For RT8111C/D

for RT8111B N/C
for RT8111C 0 ohm (Internal Regulator)
for RT8111C N/C (external Regulator)

LU4
RTL8111D-VB-GR/S/[10HP2-408111-70R]

For RTL8111C

80歐姆:[15/5/5/5/15]

SRCCLK 50歐姆:[18/4/10/4/18]

離 PIN63 0.5cm以內

LR27離 IC越近越好

離 IC近越好

Dual Color LED

Single Color LED

P35-152-19W9

FOR CLOSE PIN1,29,37,40

距離pin1 在0.5cm以內

距離LL2 在0.5cm以內

放靠近後窗

USB30_LAN CONNECTOR

USB30_LAN
R-A USB+LAN/W TF/1G/USB3.0 UDE/[11NR6-702009-K1R]

Close to USB30_LAN

400MILS

240MILS

SEL	OE	Y+	Y-
	X	H	Hi-Z	Hi-Z
NEC	L	L	M+	M-
PCH	H	L	D+	D-

Gigabyte Technology

Title: REALTEK RTL8111D

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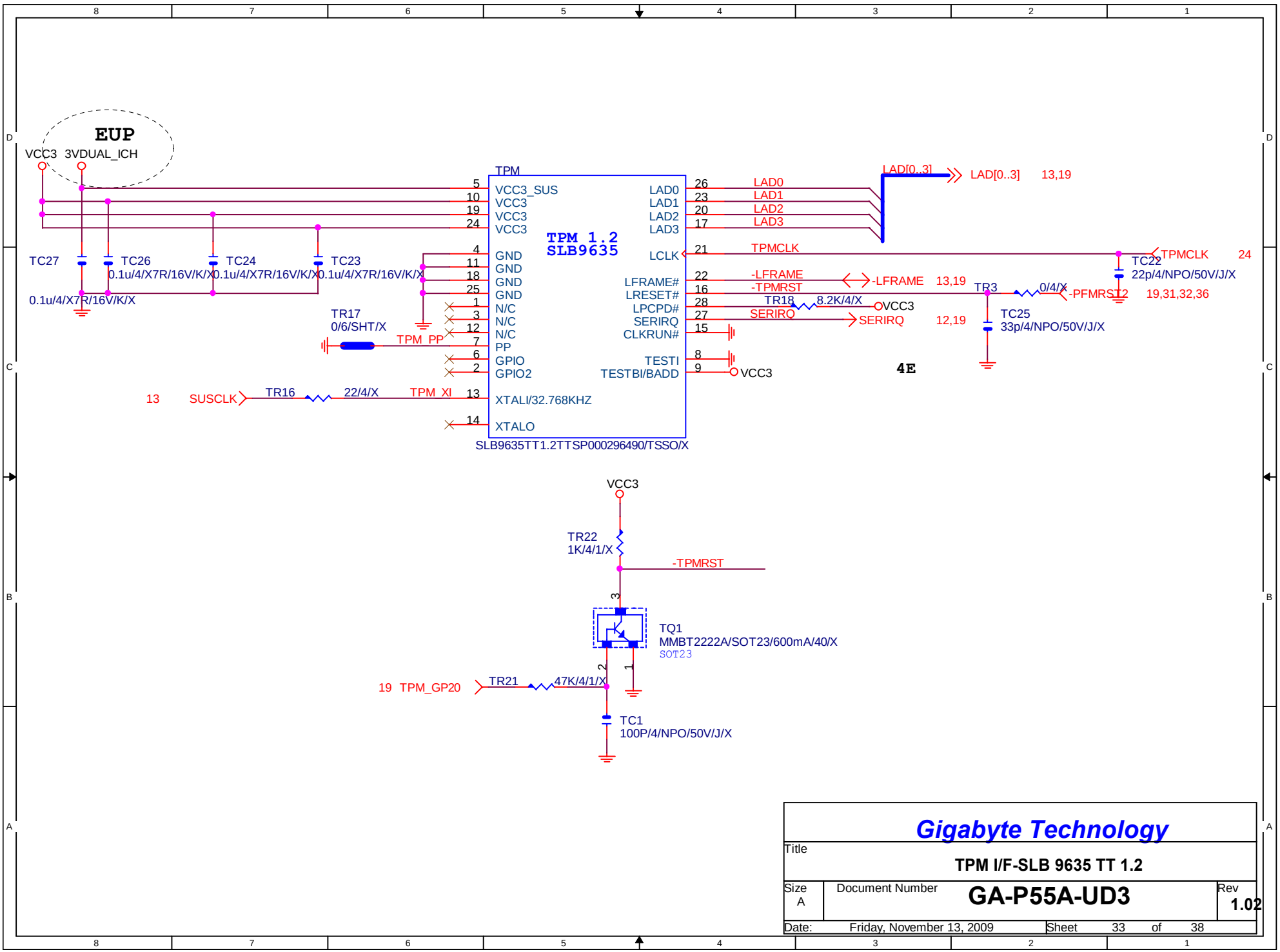

Gigabyte Technology			
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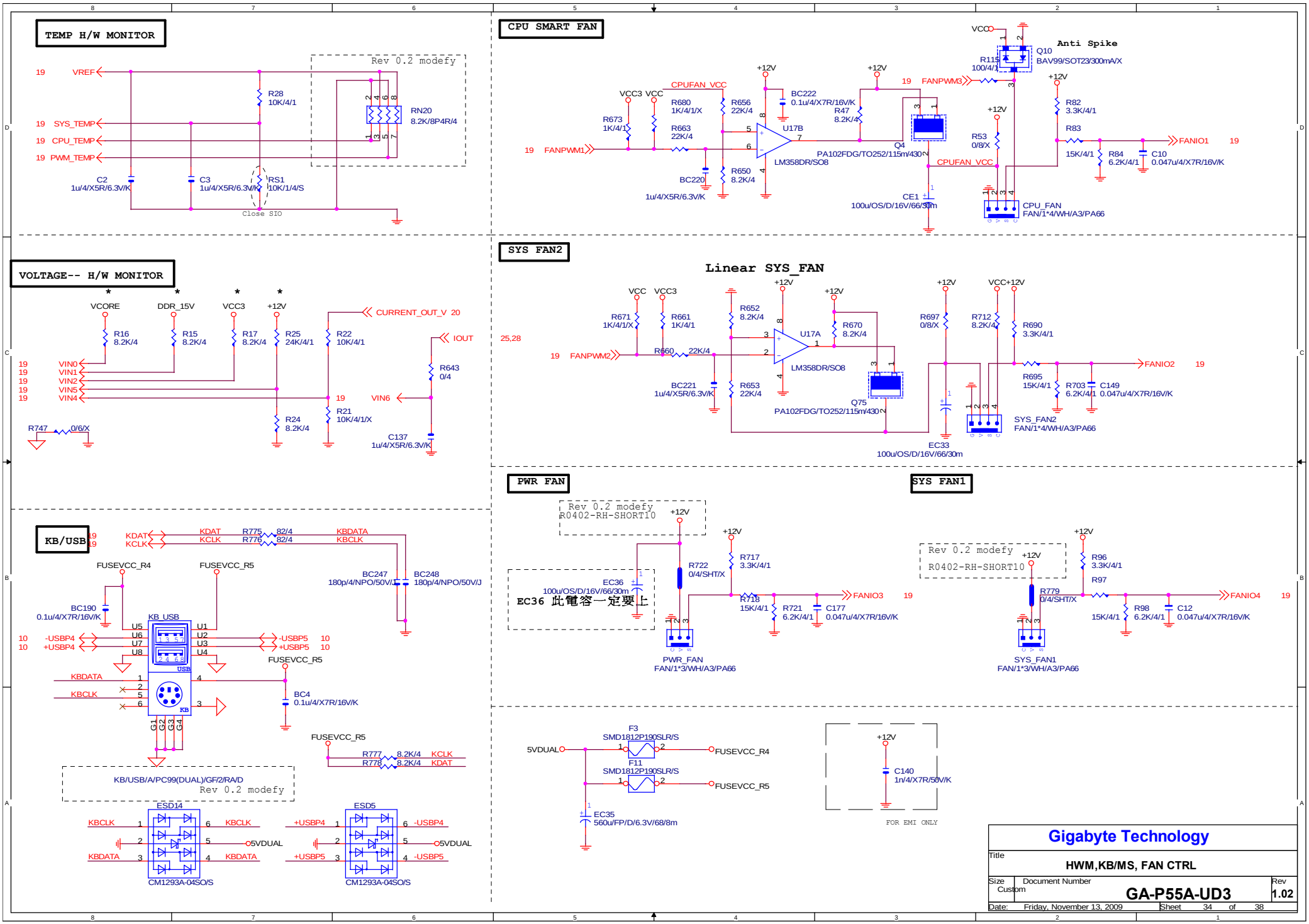
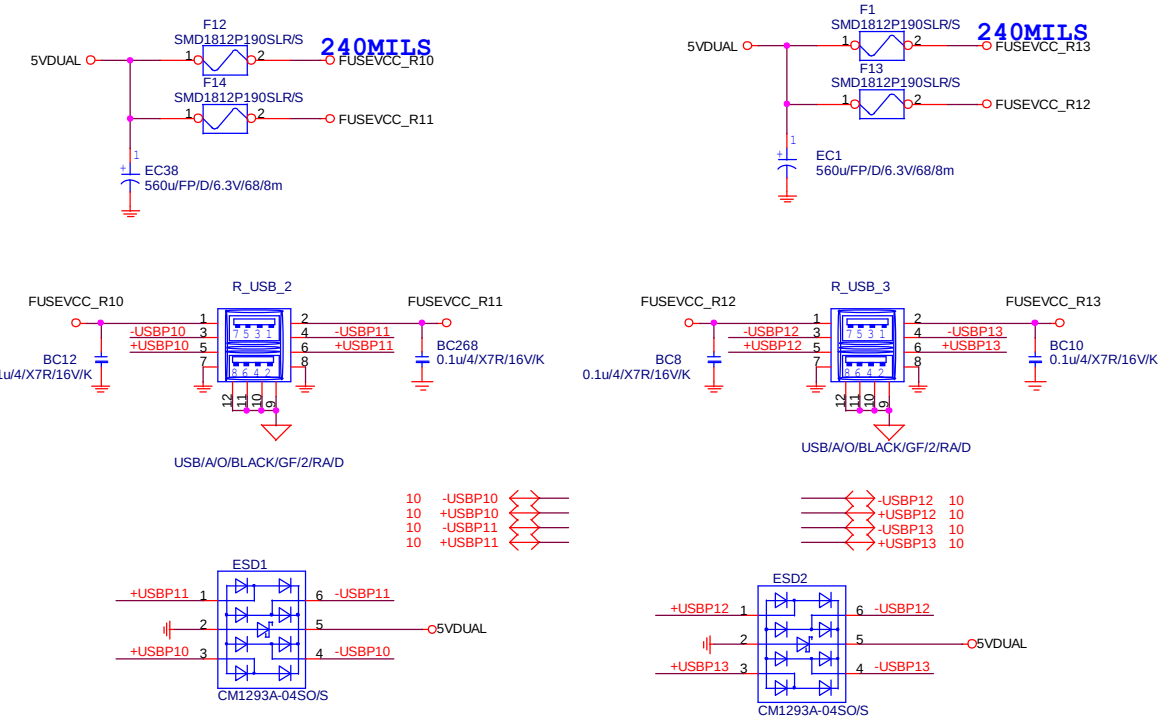
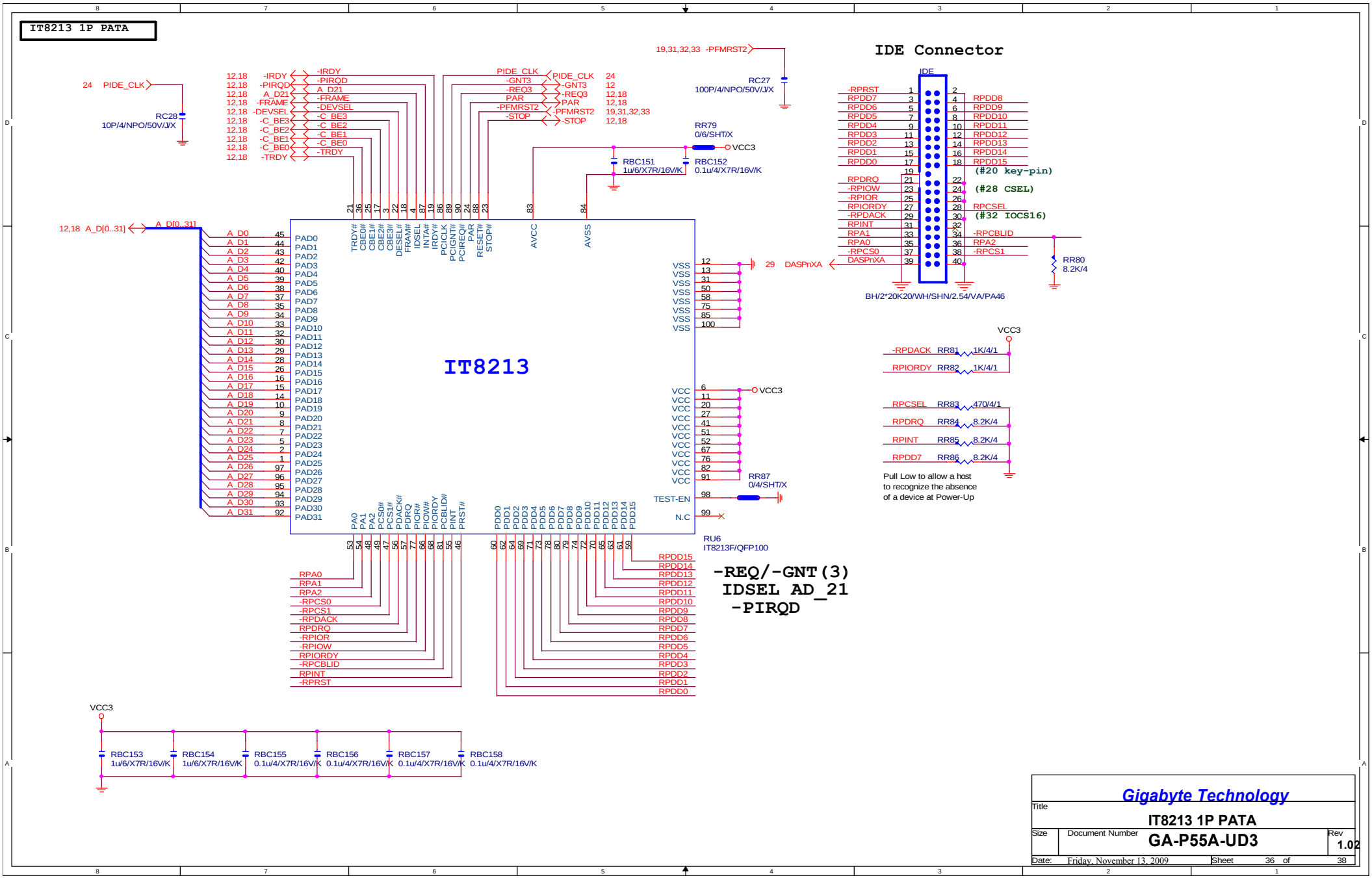
Size A	Document Number **GA-P55A-UD3**		Rev 1.02
Date: Friday, November 13, 2009	Sheet 33 of 38		

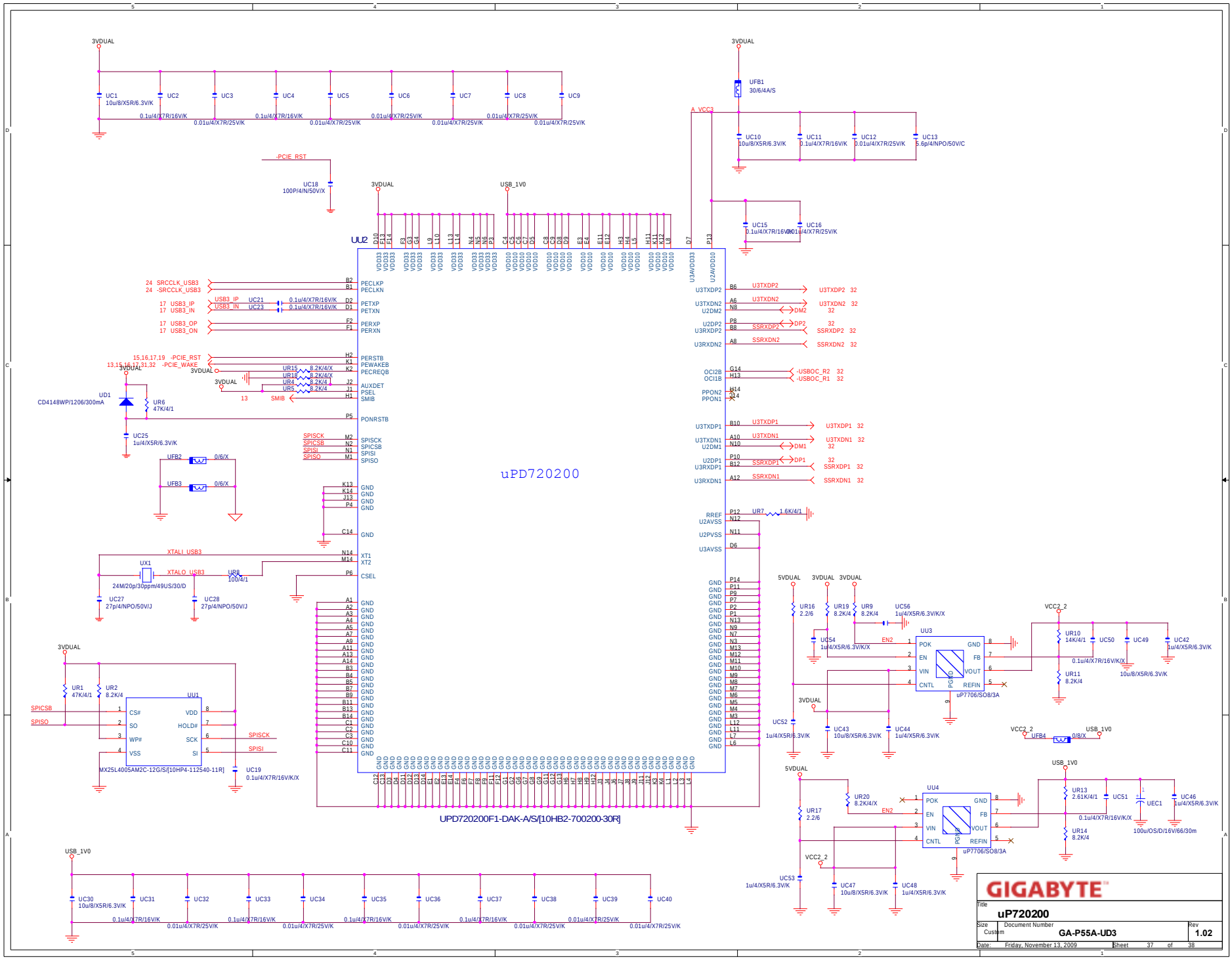




GIGABYTE

Title: R_USB		
Size: Custom	Document Number: GA-P55A-UD3	Rev: 1.02
Date: Friday, November 13, 2009	Sheet 35 of 38	





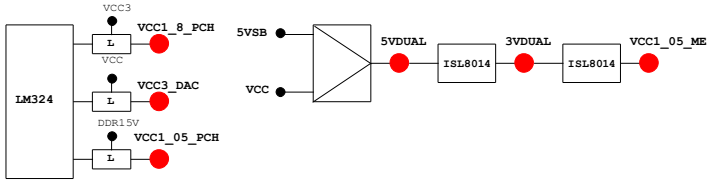
PCH GPIO LIST TABLE

PIN NAME	PWR	AFTER RTEST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

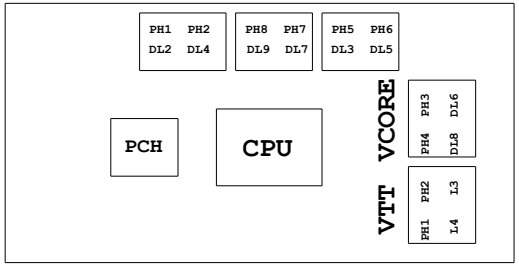
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VID03/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	空 PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology
Title: TABLE LIST
Size: C | Document Number: GA-P55A-UD3 | Rev: 1.02
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