Compal Confidential

EL4C1 & EL451 (C340/S540-14)

DIS M/B Schematic Document

Intel Whiskey Lake Processor with DDR4

MX110 (23x23mm)

2018-10-18

LA-H081P

REV :0.3

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Title	Cover Page	
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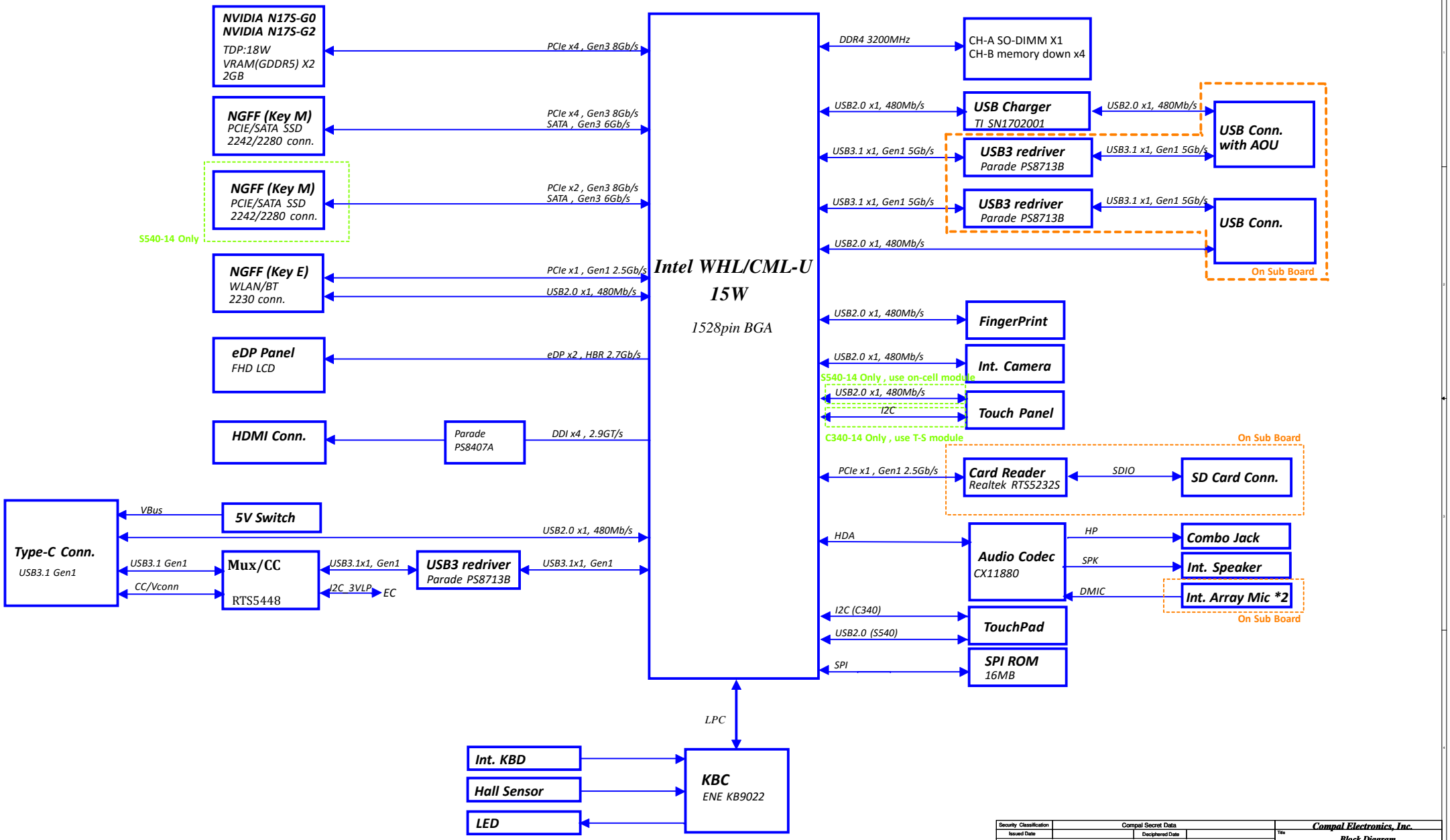

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Voltage Rails

power plane / State	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +1.05VS_VCCSTG +VCC_CORE +VCC_GT +VCC_SA +1.05VS_VCCIO +1.8VS +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
HDMI Logo	45@
Touch Screen	TS@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
Colay SATA/PCIE on M2	SSD_DET@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
Test Point	TP@
Keyboard BackLight	KBL@
	NOKBL@
Project select	S540@
	S340@
	C340@
OneKeyBattery	ONEKEY@
	NON_ONEKEY@
Intel CNVi	CNVi@
	NONCNVi@
GPU select	N17S_G0@
	N17S_G2@
	N16S@
	N17S@
Connectors	ME@

Item	BOM Structure
X4E	X4ES540@
	X4EC340@
On Board RAM	MD@
no On Board RAM	NO_MD@
On Board RAM X76 Resistors	X76RAM@
DRAM (Hynix 4GB)	H4G_S540@
DRAM (Micron 4GB)	M4G_S540@
DRAM (Samsung 4GB)	S4G_S540@
VRAM (Hynix 4GB)	H4G_VRAM@
	H4G@
	H4G_R1@
	H4G_R3@
VRAM (Samsung 4GB)	S4G_VRAM@
	S4G@
	S4G_R1@
	S4G_R3@
VRAM (Micron 4GB)	M4G_VRAM@
	M4G@
	M4G_R1@
	M4G_R3@

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	
5	
6	

PCIE Port Table

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	DGPU
7	2	
8	3	
9	3	
10	2	SSD1
11	1	
12	0	
13	0	CardReader
14	0	NGFF WLAN+BT
15	1	
16	0	SSD2

SATA Port Table

Port	
0	
1A	SSD1
1B	
2	SSD2

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h
thermal sensor	1001 101xb 21h

PCH SM Bus address

Device	Address	
DDR_JDIMM1 Touch Pad	1010 000x	A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	DGPU	BATT	CHARGER	NECP388	SODIMM	TP	PCH	G-SENSOR	THM sensor
EC_SMB_CK1 EC_SMB_DA1	NECP388 +3VL	X	V +3VALW	V +19V_VIN	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	NECP388 +3VS	V +3VS	X	X	V +3VS	X	X	V +3VS	X	V +3VS
EC_SMB_CK4 EC_SMB_DA4	NECP388 +3VS	X	X	X	X	X	X	X	V +3VS	X
SOC_SMBCLK SOC_SMBDATA	PCH +3VALW	X	X	X	X	V +3VS	V +3VS	X	X	X
SOC_SML0CLK SOC_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	PCH +3VS	V +3VS	X	X	V +3VS	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	OFF	OFF	OFF	OFF

CPU

UC1 I3_8145U@ — QQK9 W0 2.1G BGA — SA0000C6R20
UC1 I5_8265U@ — QQTG W0 1.6G BGA — SA0000C6Q20
UC1 I7_8565U@ — QQK6 W0 1.8G BGA — SA0000C6P20
UC1 I3_8145U_R3@ — SRD1V W0 2.1G — SA0000C6R30
UC1 I5_8265U_R3@ — SREJQ W0 1.6G — SA0000C6Q30
UC1 I7_8565U_R3@ — SREJP W0 1.8G — SA0000C6P30

PCB

ZZZ PCB@ — PCB 2GA LA-H081P REV0 M/B 4 — DA8001H4000

X4E X4E_S540_14 X4E_C340_14

ZZZ X4ES540@ — X4E_S540_14 — X4EAF638L5T
ZZZ X4EC340@ — X4E_C340_14 — X4EAF638L0T

GPU

UV1 N17S_G0@ — N17S-G0-A1 — SA0000CC900
UV1 N17S_G2@ — N17S-G2-A1 — SA0000CCB00

DRAM S540

ZZZ S4G_S540@ — K4A8G165WC-BCTD — X7680638L05
ZZZ H4G_S540@ — H5ANBG6NCJR-VKC — X7680638L04
ZZZ M4G_S540@ — MT40A512M16LY-075:E — X7680638L06

VRAM S540

ZZZ VH4G_S540@ — H5GC8H24AJR-R2C — X7680638L01
ZZZ VM4G_S540@ — MT51J256M32HF-80:B — X7680638L03

DRAM C340

ZZZ3 S4G_C340@ — K4A8G165WC-BCTD — X7680538L06
ZZZ2 H4G_C340@ — H5ANBG6NCJR-VKC — X7680538L04
ZZZ1 M4G_C340@ — MT40A512M16LY-075:E — X7680538L05

VRAM C340

ZZZ VH4G_C340@ — H5GC8H24AJR-R2C — X7680538L01
ZZZ VM4G_C340@ — MT51J256M32HF-80:B — X7680538L03

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Title: Notes List

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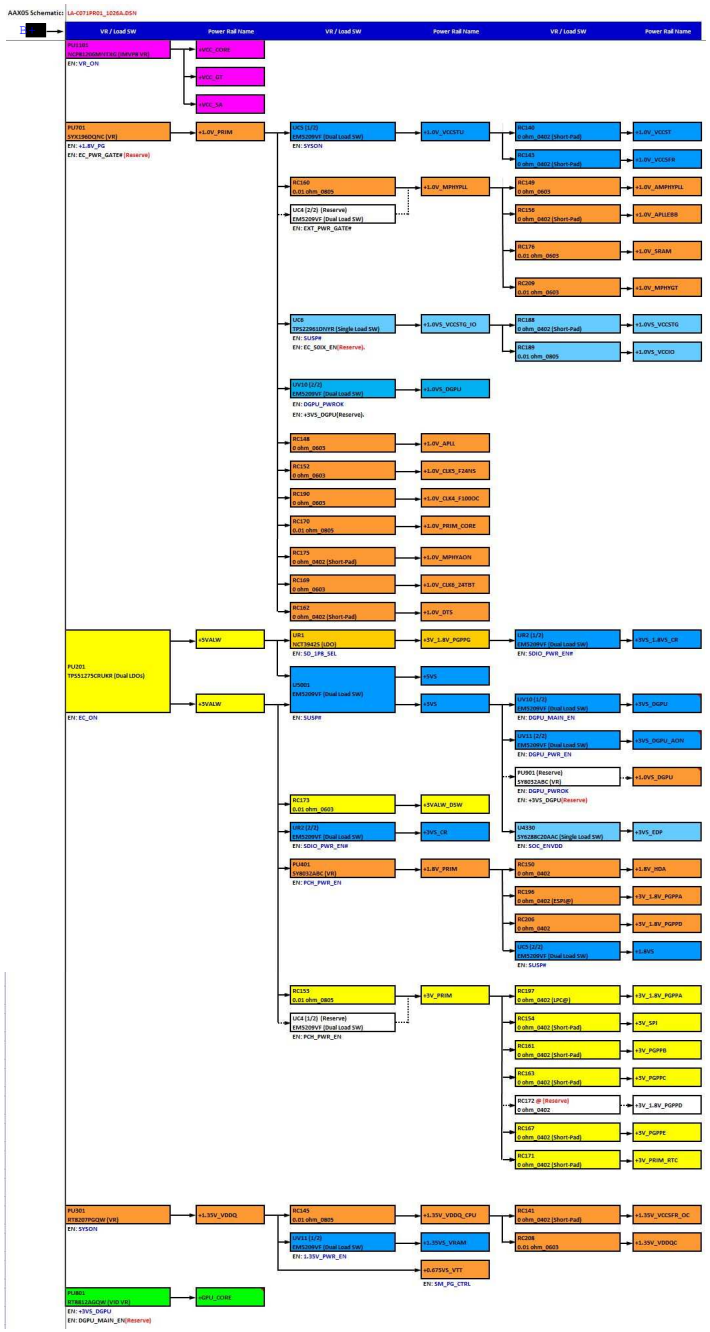
-PowerMap_KBL_DDR4_Volume_NON CS]



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Title: Power Sequence

Size	Document Number	Rev
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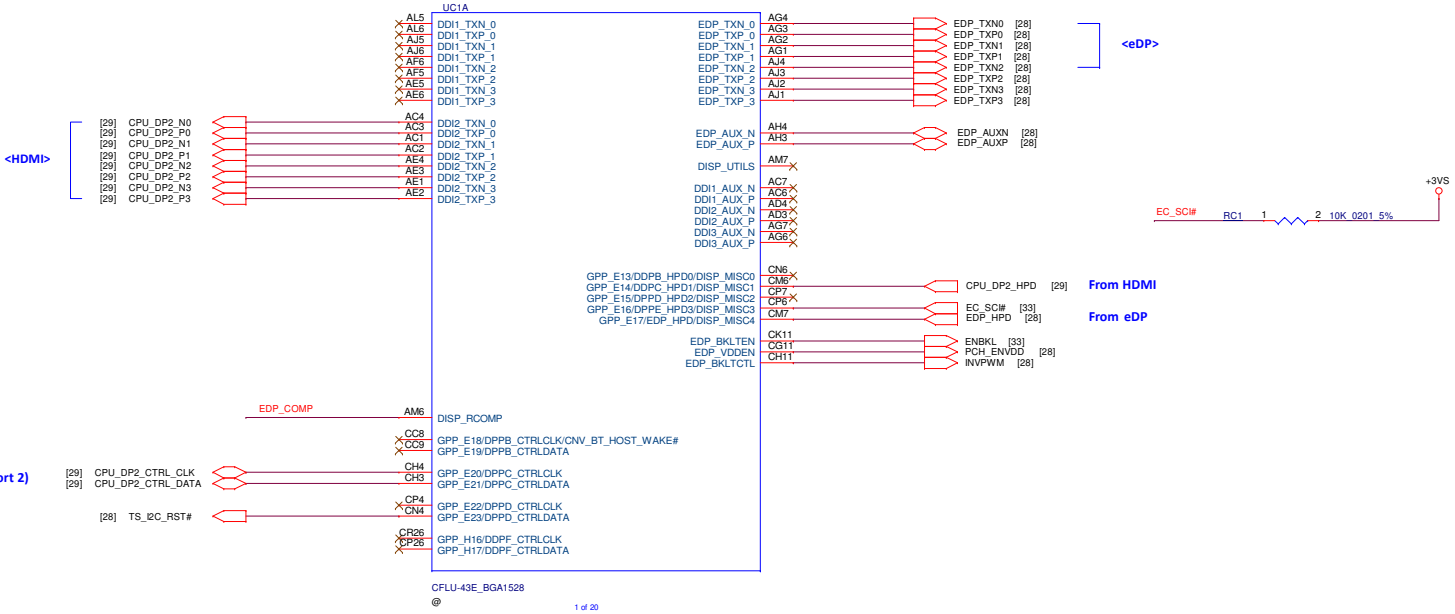
Table 5-13. DDI Disabling and Termination Guidelines

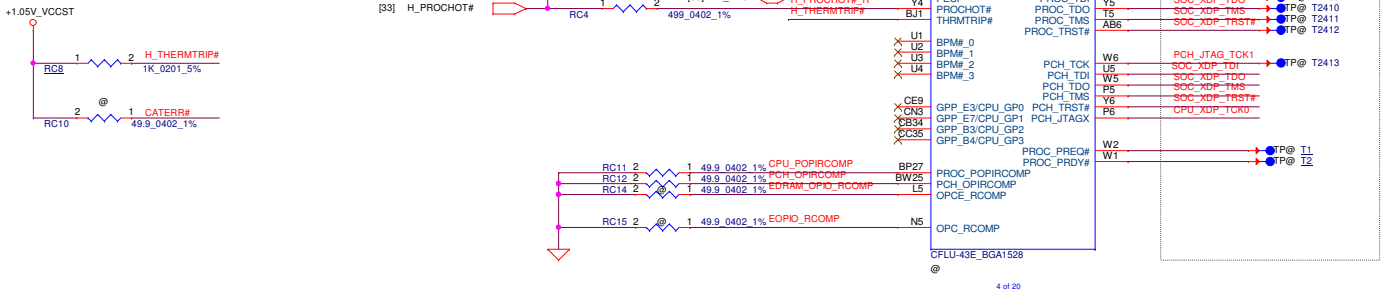
Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

< Compensation PU For eDP >

+1.05VS_VCCIO — RC2 1 — 2 — EDP_COMP — 24.9_0201_1%

Trace width=20 mils, Spacing=25mil, Max length=600mils





Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Title: WHL-U(1/12)DDI,EDP,MISC,CMC

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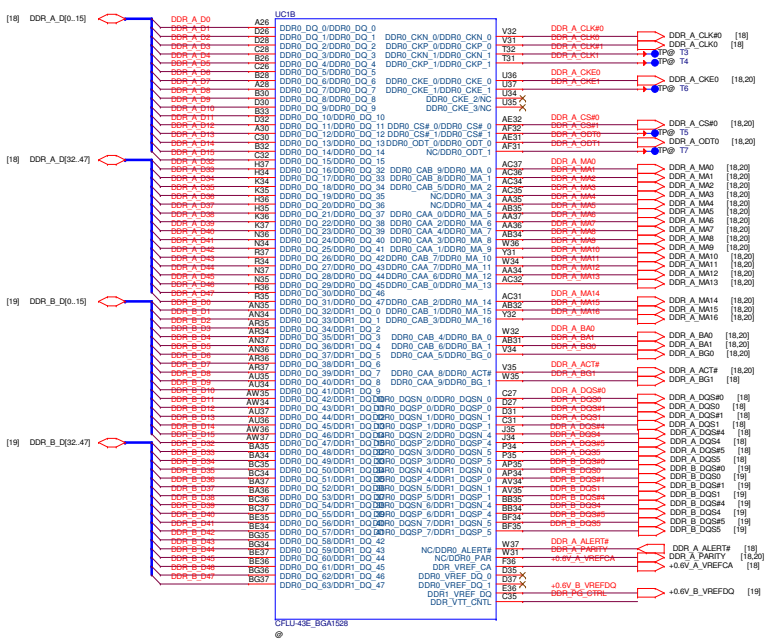
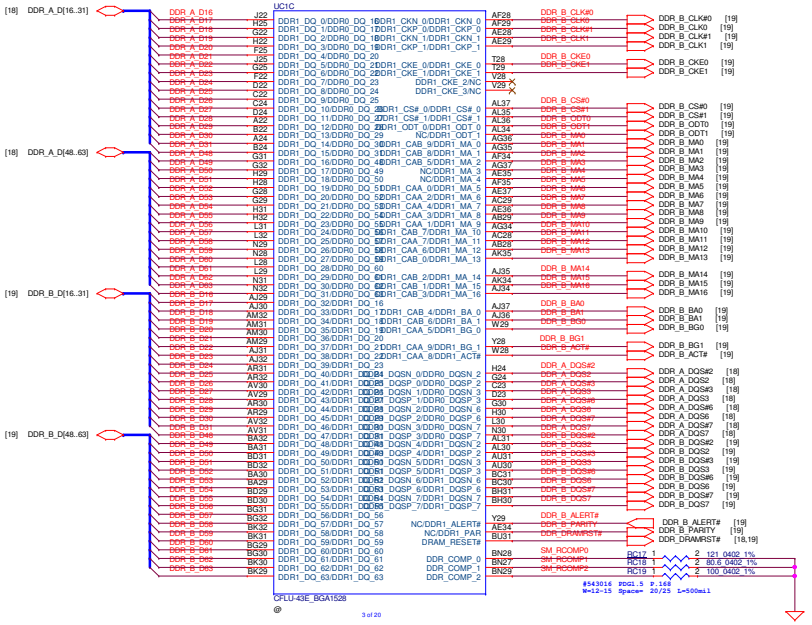
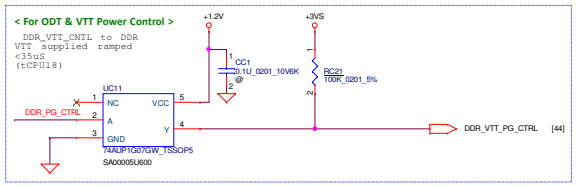
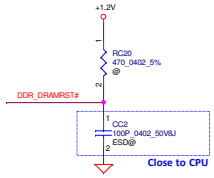
Non-Interleaved Memory



Trace width/Spacing >= 20mils







Recommended By Intel Max

Remove RC17 for SDP/DDP BOM selection by PDG

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Title: WHL-U(2/12)DDR4

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+3VALW

RC23 1 2 100K_0201_5% SOC_SPI_0_SI
RC24 1 2 100K_0201_5% SOC_SPI_0_IO2
RC25 1 2 100K_0201_5% SOC_SPI_0_IO3

Note: The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion

SML1ALERT#/ PCHHOT#/GPP_B23	•If USB 3.1 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise. •If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float. •If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

SPI ROM

UC1E

SOC_SPI_0_CLK CH37 — SPI0_CLK
SOC_SPI_0_SO CF37 — SPI0_MISO
SOC_SPI_0_SI CF36 — SPI0_MOSI
SOC_SPI_0_IO2 CF34 — SPI0_IO2
SOC_SPI_0_IO3 CG34 — SPI0_IO3
SOC_SPI_0_CS#0 CG36 — SPI0_CS0#
CG35 — SPI0_CS1#
CH34 — SPI0_CS2#

CF20 — GPP_D1/SPI1_CLK/BK1/SBK1
CG22 — GPP_D2/SPI1_MISO_IO1/BK2/SBK2
CF22 — GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
CG23 — GPP_D21/SPI1_IO2
CH23 — GPP_D22/SPI1_IO3
CG20 — GPP_D0/SPI1_CS0#/BK0/SBK0

CH7 — CL_CLK
CH8 — CL_DATA
CH9 — CL_RST#

KB_RST# — BV29 — GPP_A0/RCIN#/TIME_SYNC1
SERIRQ — BV28 — GPP_A6/SERIRQ

[33] SERIRQ

GPP_C0/SMBCLK CK14 SOC_SMBCLK — SOC_SMBCLK [19]
GPP_C1/SMBDATA CH15 SOC_SMBDATA — SOC_SMBDATA [19]
GPP_C2/SMBALERT# CJ15 SOC_SMBALERT# — TP@ T8

GPP_C3/SML0CLK CH14 SOC_SML0CLK
GPP_C4/SML0DATA CF15 SOC_SML0DATA
GPP_C5/SML0ALERT# CG15 SOC_SML0ALERT# — TP@ T9

GPP_C6/SML1CLK CN15
GPP_C7/SML1DATA CM15 — EC_SMB_CK2 [24,33,35]
GPP_B23/SML1ALERT#/PCHHOT# CC34 SOC_SML1ALERT# — EC_SMB_DA2 [24,33,35]

SMB (Link to DDR)

SML1 (Link to EC,DGPU,Thermal Sensor)

GPP_A1/LAD0/ESPI_IO0 CA29 LPC_AD0 — LPC_AD0 [33]
GPP_A2/LAD1/ESPI_IO1 BY29 LPC_AD1 — LPC_AD1 [33]
GPP_A3/LAD2/ESPI_IO2 BY27 LPC_AD2 — LPC_AD2 [33]
GPP_A4/LAD3/ESPI_IO3 BY27 LPC_AD3 — LPC_AD3 [33]
GPP_A5/LFRAME#/ESPI_CS# CA28 LPC_FRAME# — LPC_FRAME# [33]
GPP_A14/SUS_STAT#/ESPI_RESET# CA27

GPP_A9/CLKOUT_LPC0/ESPI_CLK BV32 LPC_CLK0 — RC27 1 EMI@ 2 22_0402_5% — CLK_LPC_EC [33]
GPP_A10/CLKOUT_LPC1 BV30
GPP_A8/CLKRUN# BV30 PM_CLKRUN# — PM_CLKRUN# [33]

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+3VS

RC26 1 2 10K_0201_5% KB_RST#

+3VS

RC28 1 2 8.2K_0402_5% SERIRQ

RPC1, RPC3 and RC30 are close to UC3

From SOC

SOC_SPI_0_SO RC29 1 2 33_0402_5% SOC_SPI_0_SO_R
SOC_SPI_0_CLK RC31 1 EMI@ 2 33_0402_5% SOC_SPI_0_CLK_R
SOC_SPI_0_SI RC32 1 2 33_0402_5% SOC_SPI_0_SI_R
SOC_SPI_0_IO3 RC34 1 2 33_0402_5% SOC_SPI_0_IO3_R

SOC_SPI_0_IO2 RC36 1 2 33_0402_5% SOC_SPI_0_IO2_R

From EC

[33] EC_SPI_CLK — EC_SPI_CLK RC41 1 EMI@ 2 33_0402_5% SOC_SPI_0_CLK_R
[33] EC_SPI_MOSI — EC_SPI_MOSI RC42 1 2 33_0402_5% SOC_SPI_0_SI_R
[33] EC_SPI_CS0# — EC_SPI_CS0# RC43 1 2 33_0402_5% SOC_SPI_0_CS#0
[33] EC_SPI_MISO — EC_SPI_MISO RC44 1 2 33_0402_5% SOC_SPI_0_SO_R

+3VS

EC_SMB_CK2 RC30 1 2 1K_0201_5%
EC_SMB_DA2 RC33 1 2 1K_0201_5%
SOC_SML1ALERT# 1 @ 2 RC35 150K_0402_5%
SOC_SMBCLK RC37 1 2 1K_0201_5%
SOC_SMBDATA RC38 1 2 1K_0201_5%
SOC_SML0CLK RC39 1 2 1K_0201_5%
SOC_SML0DATA RC40 1 2 1K_0201_5%

+3VS

PM_CLKRUN# 1 2 RC45 8.2K_0402_5%

< SPI ROM - 16M >

+3VALW

CC3 1 @ 2 0.1U_0201_10V K X5R

UC12

SOC_SPI_0_CS#0 1 CS# — VCC 8 — SOC_SPI_0_IO3_R
SOC_SPI_0_SO_R 2 DO(IO1) — IO 7
SOC_SPI_0_IO2_R 3 IO2 — CLK 6 — SOC_SPI_0_CLK_R
4 GND — DI(IO0) 5 — SOC_SPI_0_SI_R

W25Q128JVSIQ SOIC8P
SA00005VV20

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Title: **WHL-U(3/12)SPI,SMB,LPC,ESPI**

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< HD AUDIO >

[32] HDA_RST#_R — RC163 1 2 33_0201_5% — HDA_RST#

[32] HDA_BIT_CLK_R — RC46 1 EMI@ 2 33_0201_5% — HDA_BIT_CLK

[32] HDA_SYNC_R — RC48 1 2 33_0201_5% — HDA_SYNC

[32] HDA_SDOUT_R — RC47 1 2 33_0201_5% — HDA_SDOUT

RC49 1 @ 2 499_0402_1%

< To Enable ME Override >

[33] ME_EN — RC51 1 @ 2 0_0402_5% — HDA_SDOUT

UC1G

HDA_SYNC	BN34	HDA_SYNC/I2S0_SFRM	GPP_G0/SD_CMD	CH36
HDA_BIT_CLK	BN37	HDA_BCLK/I2S0_SCLK	GPP_G1/SD3_DATA0	CL35
HDA_SDOUT	BN36	HDA_SDO/I2S0_TXD	GPP_G2/SD3_DATA1	CL36
[32] HDA_SDIN0	BN35	HDA_SDI0/I2S0_RXD	GPP_G3/SD3_DATA2	CM35
HDA_RST#	BL36	HDA_SDI1/I2S1_RXD/SNDW1_DATA	GPP_G4/SD_DATA3	CN35
	BL35	HDA_RST#/I2S1_SCLK/SNDW1_CLK	GPP_G5/SD_CD#	CH35
	CK23	GPP_D23/I2S_MCLK	GPP_G6/SD_CLK	CK36
	BL37	I2S1_SFRM/SNDW2_CLK	GPP_G7/SD_WP	CK34
	BL34	I2S1_TXD/SNDW2_DATA		
[30] CNV_RF_RESET#	CNV_RF_RESET# CJ32	GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#		
[30] CLKREQ_CNV#	CLKREQ_CNV# CH32	GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK		
	CH29	GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ		
	CH30	GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO	GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7	BW36
			GPP_A16/SD_1P8_SEL	BY31
	CP24	GPP_D19/DMIC_CLK0/SNDW4_CLK		
	CN24	GPP_D20/DMIC_DATA0/SNDW4_DATA		
	CK25	GPP_D17/DMIC_CLK1/SNDW3_CLK	SD_1P8_RCOMP	CK33
	CJ25	GPP_D18/DMIC_DATA1/SNDW3_DATA	SD_3P3_RCOMP	CM34
[32] HDA_SPKR	HDA_SPKR CF35	GPP_B14/SPKR		

SOC_SD_RCOMP — RC50 1 2 200_0402_1%

CFLU-43E_BGA1528

@

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75K_0402_5% 1 CNVi@ 2 RC52 — CNV_RF_RESET#

Follow Jefferson Peak schematic check list.

+3VS — RC55 1 @ 2 2.2K_0402_5% — HDA_SPKR

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

+3VALW +3VS — RC58 1 @ 2 10K_0201_5% — WLBT_OFF#

+3VALW — RC164 1 @ 2 10K_0201_5% — WLBT_OFF#

TO DGPU — SOC_GPIO_C10 — RC59 1 @ 2 0_0402_5% — GPU_EVENT# — GPU_EVENT# [24]

GPP_H21 XTAL frequency select.
0: 38.4 / 19.2 MHz
1: 24MHz XTAL select.

UC1I

[30] CNV_CRX_DTX_N0	CNV_CRX_DTX_N0 CR30	CNV_WR_D0N	GPP_H18/CPU_C10_GATE#	CN27
[30] CNV_CRX_DTX_P0	CNV_CRX_DTX_P0 CP30	CNV_WR_D0P	GPP_H19/TIMESYNC_0	CM27
[30] CNV_CRX_DTX_N1	CNV_CRX_DTX_N1 CM30	CNV_WR_D1N	GPP_H21	CF25
[30] CNV_CRX_DTX_P1	CNV_CRX_DTX_P1 CN30	CNV_WR_D1P	GPP_H22	CN26
[30] CNV_CTX_DRX_N0	CNV_CTX_DRX_N0 CN32	CNV_WT_D0N	GPP_H23	CM26
[30] CNV_CTX_DRX_P0	CNV_CTX_DRX_P0 CM32	CNV_WT_D0P	GPP_F10	CK17
[30] CNV_CTX_DRX_N1	CNV_CTX_DRX_N1 CP33	CNV_WT_D1N	GPD7	BV35
[30] CNV_CTX_DRX_P1	CNV_CTX_DRX_P1 CN33	CNV_WT_D1P	GPP_F3	CN20
[30] CLK_CNV_CRX_DTX_N	CLK_CNV_CRX_DTX_N CN31	CNV_WR_CLKN	GPP_D4/IMGCLKOUT0/BK4/SBK4	CG25
[30] CLK_CNV_CRX_DTX_P	CLK_CNV_CRX_DTX_P CP31	CNV_WR_CLKP	GPP_H20/IMGCLKOUT_1	CH25
[30] CLK_CNV_CTX_DRX_N	CLK_CNV_CTX_DRX_N CP34	CNV_WT_CLKN	GPP_F12/EMMC_DATA0	CR20
[30] CLK_CNV_CTX_DRX_P	CLK_CNV_CTX_DRX_P CN34	CNV_WT_CLKP	GPP_F13/EMMC_DATA1	CM20
			GPP_F14/EMMC_DATA2	CN19
1 CNVi@ 2 RC56 150_0402_1%	CNV_WT_RCOMP CP32	CNV_WT_RCOMP_0	GPP_F15/EMMC_DATA3	CM19
	CR32	CNV_WT_RCOMP_1	GPP_F16/EMMC_DATA4	CN18
	CP20	GPP_F0/CNV_PA_BLANKING	GPP_F17/EMMC_DATA5	CR18
For MX150 [11] GC6_FB_EN1V8	GC6_FB_EN1V8 CK19	GPP_F1	GPP_F18/EMMC_DATA6	CP18
	CG17	GPP_F2	GPP_F19/EMMC_DATA7	CM18
[34] TP_INT#	CR14	GPP_C8/UART0_RXD		
	CP14	GPP_C9/UART0_TXD		
SOC_GPIO_C10	CN14	GPP_C10/UART0_RTS#	GPP_F20/EMMC_RCLK	CM16
[30] WLBT_OFF#	CM14	GPP_C11/UART0_CTS#	GPP_F21/EMMC_CLK	CP16
			GPP_F11/EMMC_CMD	CR16
	CJ17	GPP_F8/CNV_MFUART2_RXD	GPP_F22/EMMC_RESET#	CN16
	CH17	GPP_F9/CNV_MFUART2_TXD		
RC57 1 2 10K_0201_5%	SOC_A4WP_PRESENT CF17	GPP_F23/A4WP_PRESENT	EMMC_RCOMP	CK15

SOC_C10_GATE# — TP@ T10

SOC_GPP_H21 — RC53 1 2 4.7K_0201_5%

SOC_GPD7 — RC54 1 2 100K_0201_5%

+3VALW

SOC_SD_RCOMP

XTAL INPUT MODE (HVM ONLY)
LOW: XTAL INPUT IS SINGLE ENDED
HIGH: XTAL IS ATTACHED

CFLU-43E_BGA1528

@

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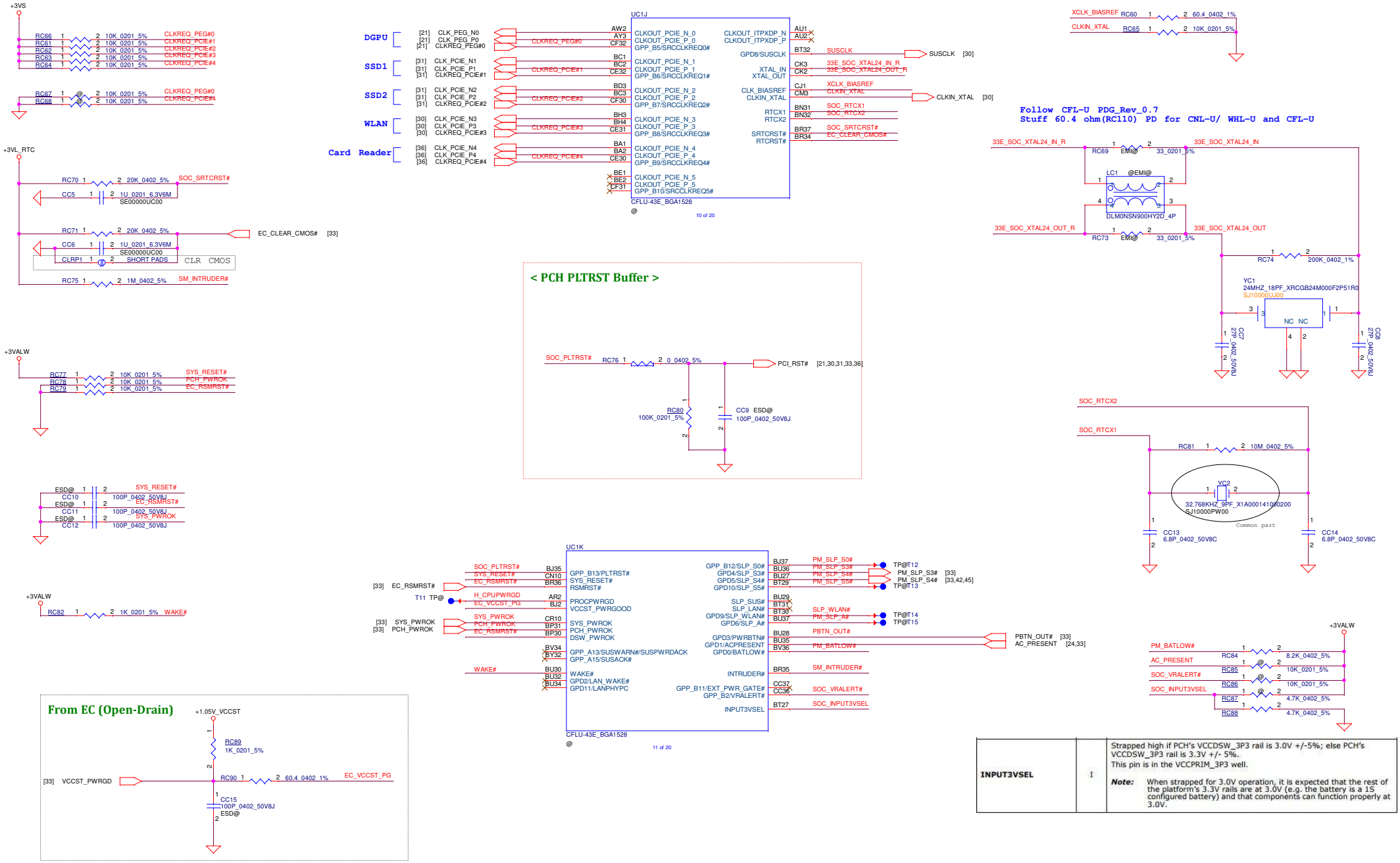
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: WHL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: LA-H081P | Rev: 0.2

Date: Monday, October 22, 2018 | Sheet 9 of 53



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: WHL-U(5/12)CLK,PM,GPIO

Size	Document Number	Rev
Custom	LA-H081P	0.2

Date: Monday, October 22, 2018 Sheet 10 of 53

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is used when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode

Capacity	Description	X76	PART NUMBER (R1)	GPP_B19 OBRAM_ID0	GPP_B20 OBRAM_ID1	GPP_B21 OBRAM_ID2
4GB	WITHOUT ON-BOARD RAM	N/A	N/A	0	0	0
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) EL451	X7680638L05	SA0000B6F00	0	0	1
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) EL4C1	X7680538L06	SA0000B6F00			
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) EL451	X7680638L04	SA0000BMN00	0	1	0
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) EL4C1	X7680538L04	SA0000BMN00			
	MICRON 2666MHz (MT40A512M16LY-075:E) EL451	X7680638L06	SA0000ARD20	0	1	1
	MICRON 2666MHz (MT40A512M16LY-075:E) EL4C1	X7680538L05	SA0000ARD20			
	N/A	N/A	N/A			

RC94 NO_MD@ 10K_0201_5%
RC95 NO_MD@ 10K_0201_5%
RC96 NO_MD@ 10K_0201_5%

+3VS
RC97 1 @ 2 4.7K_0402_5% GSPI0_MOSI
RC98 1 @ 2 150K_0402_5% GSPI1_MOSI

+3VS
RC1011 2 10K_0201_5% DGPU_PWR_EN
RC1021 2 10K_0201_5% SOC_GPIO_A7
RC1671 2 2.2K_0402_5% I2C_1_SDA
RC1681 2 2.2K_0402_5% I2C_1_SCL
RC1031 2 49.9K_0402_1% UART0_RX
RC1081 2 49.9K_0402_1% UART0_TX
RC1091 2 2.2K_0402_5% I2C_0_SDA
RC1051 2 2.2K_0402_5% I2C_0_SCL
RC106 1 @ 2 10K_0201_5% DGPU_HOLD_RST#
RC112 1 DIS@ 2 10K_0201_5%

+1.8VALW
RC113 1 @ 2 20K_0201_5% CNV_RGI_CRX_DTX
RC114 1 @ 2 20K_0201_5% CNV_BRI_CRX_DTX

CC182 1 2 100P_0402_50V8J I2C_0_SDA
CC185 1 2 100P_0402_50V8J I2C_0_SCL
CC183 1 2 100P_0402_50V8J I2C_1_SDA
CC186 1 2 100P_0402_50V8J I2C_1_SCL
CC184 1 2 100P_0402_50V8J I2C_2_SDA
CC187 1 2 100P_0402_50V8J I2C_2_SCL

Touch PAD
Touch Screen
EC sensor Hub

PCH EDS : M.2 CNV Mode Select

GPP_F6/CNV_RGI_DT

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.

+1.8VALW
RC162 2 1 20K_0201_5% CNV_RGI_CTX_DRX
NONCNVi@

CNVi RGI_DT pin gets the pull-down resistor (1K ohm) from the internal CRF module when CNVi is enabled.
There must not be any pull-down resistor connected on the board.

SOC_GPIO_B16 RC121 1 N16S@ 2 0_0201_5% GC6_FB_EN
GC6_FB_EN1V8 RC122 1 N17S@ 2 0_0201_5%
[9] GC6_FB_EN1V8
GC6_FB_EN [24,25]
TO DGPU

UC1F
[33] SENSOR_EC_INT
SOC_GPIO_A7 CC27 GPP_B15/GSPI0_CS0#
SOC_GPIO_B16 CC32 GPP_A7/PIRQA#/GSPI0_CS1#
SENSOR_EC_INT CE29 GPP_B16/GSPI0_CLK
GSPI0_MOSI CE27 GPP_B17/GSPI0_MISO
CE29 GPP_B18/GSPI0_MOSI
OBRAM_ID0 CA31 GPP_B19/GSPI1_CS0#
OBRAM_ID1 CA32 GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
OBRAM_ID2 CC29 GPP_B20/GSPI1_CLK
GSPI1_MOSI CC30 GPP_B21/GSPI1_MISO
CA30 GPP_B22/GSPI1_MOSI
[30] CNV_BRI_CRX_DTX CNV_BRI_CRX_DTX CK20 GPP_F5/CNV_BRI_RSP
[30] CNV_RGI_CTX_DRX CNV_RGI_CTX_DRX CG19 GPP_F6/CNV_RGI_DT
[30] CNV_BRI_CTX_DRX CNV_BRI_CTX_DRX CJ20 GPP_F4/CNV_BRI_DT
[30] CNV_RGI_CRX_DTX CNV_RGI_CRX_DTX CH19 GPP_F7/CNV_RGI_RSP
[30] UART0_RX CR12 GPP_C20/UART2_RXD
[30] UART0_TX CP12 GPP_C21/UART2_TXD
CN12 GPP_C22/UART2_RTS#
CM12 GPP_C23/UART2_CTS#
[34] I2C_0_SDA CM11 GPP_C16/I2C0_SDA
[34] I2C_0_SCL CN11 GPP_C17/I2C0_SCL
[28] I2C_1_SDA CK12 GPP_C18/I2C1_SDA
[28] I2C_1_SCL CJ12 GPP_C19/I2C1_SCL
[33] I2C_2_SDA CF27 GPP_H4/I2C2_SDA
[33] I2C_2_SCL CF29 GPP_H5/I2C2_SCL
CH27 GPP_H6/I2C3_SDA
CH28 GPP_H7/I2C3_SCL
CJ30 GPP_H8/I2C4_SDA
CJ31 GPP_H9/I2C4_SCL
CFLU-43E_BGA1528
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GPP_D9/ISH_SPI_CS#/GSPI2_CS0# CN22
GPP_D10/ISH_SPI_CLK/GSPI2_CLK CR22
GPP_D11/ISH_SPI_MISO/GSPI2_MISO CM22 MODEL_SETTING0
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI CP22 MODEL_SETTING1
GPP_D5/ISH_I2C0_SDA CK22
GPP_D6/ISH_I2C0_SCL CH20
GPP_D7/ISH_I2C1_SDA CH22
GPP_D8/ISH_I2C1_SCL CJ22
GPP_H10/I2C5_SDA/ISH_I2C2_SDA CJ27
GPP_H11/I2C5_SCL/ISH_I2C2_SCL CJ29
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA CM24
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL CN23
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1# CM23
GPP_D16/ISH_UART0_CTS#/SML0BALERT# CR24
GPP_C12/UART1_RXD/ISH_UART1_RXD CG12 DGPU_PWR_EN
GPP_C13/UART1_TXD/ISH_UART1_TXD CH12 DGPU_HOLD_RST#
GPP_C14/UART1_RTS#/ISH_UART1_RTS# CF12 GPU_ALL_PGOOD
GPP_C15/UART1_CTS#/ISH_UART1_CTS# CG14 DGPU_PRSNT
GPP_A18/ISH_GP0 BW35 TS_INT#
GPP_A19/ISH_GP1 BW34 DGPU_SEL0
GPP_A20/ISH_GP2 CA37 DGPU_SEL1
GPP_A21/ISH_GP3 CA36
GPP_A22/ISH_GP4 CA35
GPP_A23/ISH_GP5 CA34
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF# BW37

DGPU_PWR_EN [26,33]
DGPU_HOLD_RST# [21]
GPU_ALL_PGOOD [26]
TS_INT# [28]

+3VS
RC91 1 10K_0201_5% X76RAM@ 2 OBRAM_ID0
RC94 1 10K_0201_5% X76RAM@ 2
RC92 1 10K_0201_5% X76RAM@ 2 OBRAM_ID1
RC95 1 10K_0201_5% X76RAM@ 2
RC93 1 10K_0201_5% X76RAM@ 2 OBRAM_ID2
RC96 1 10K_0201_5% X76RAM@ 2

+3VS
RTOUCH5 1 2 TS_INT#
4.7K_0402_5%

Function	MODEL_SETTING1 (GPP_D12)	MODEL_SETTING0 (GPP_D11)
C340	0	0
S340	0	1
S540	1	0

+3VS
RC99 1 S540@ 2 10K_0201_5% MODEL_SETTING1
RC100 1 C340@ 2 10K_0201_5%
+3VS
RC107 1 S340@ 2 10K_0201_5% MODEL_SETTING0
RC104 1 C340@ 2 10K_0201_5%
RC100 S340@ 10K_0201_5%
RC104 S540@ 10K_0201_5%

Function	DGPU_PRSNT (GPP_C15)
DIS	0
UMA Only	1

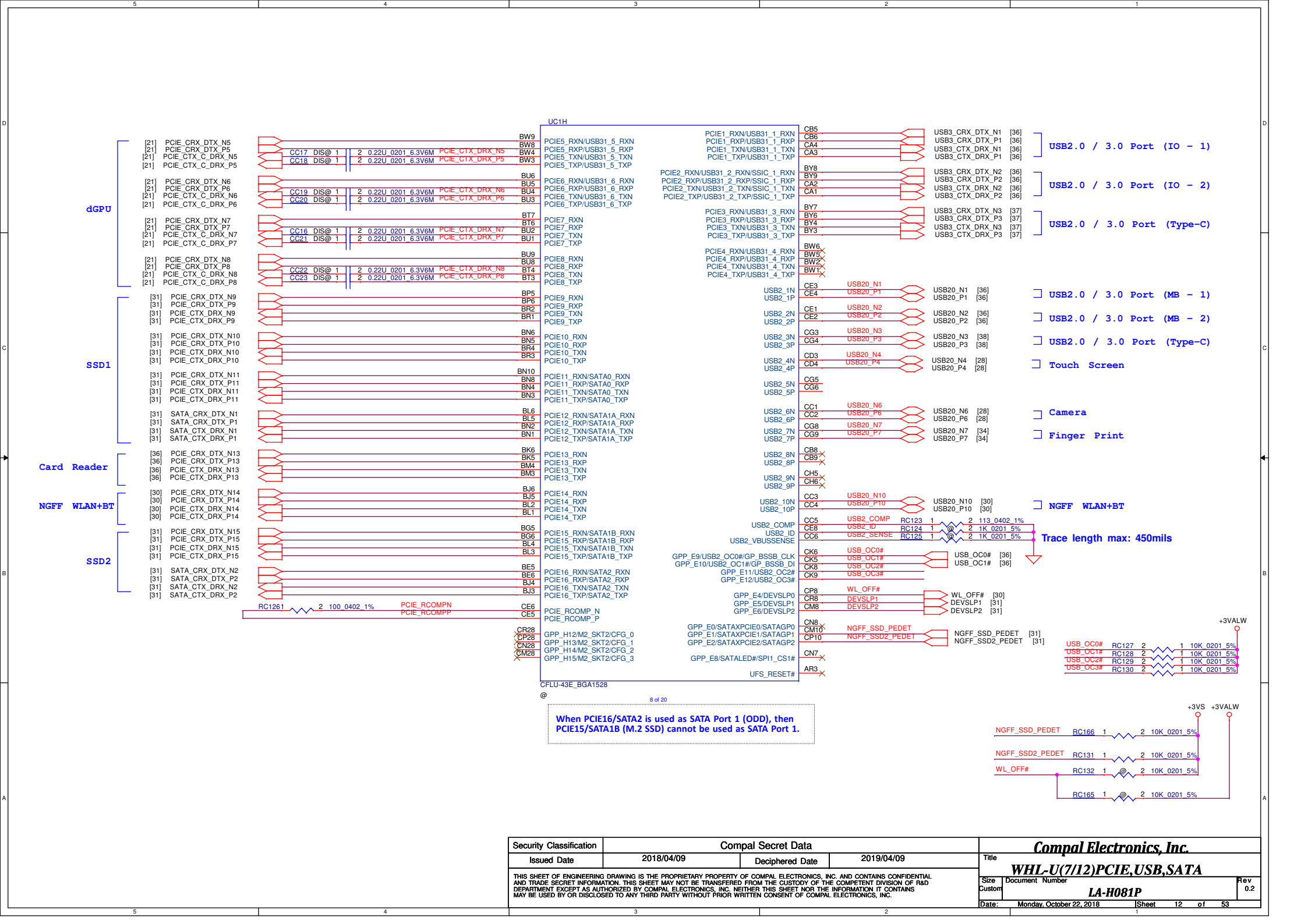
+3VS
RC115 1 UMA@ 2 10K_0201_5% DGPU_PRSNT
RC116 1 DIS@ 2 10K_0201_5%

Function	MODEL_SETTING2 (GPP_A20)
Arrary MIC	1
Single MIC	0

+3VS
RC119 1 @ 2 10K_0201_5% DGPU_SEL1
RC120 1 @ 2 10K_0201_5%
+3VS
RC160 1 @ 2 10K_0201_5% DGPU_SEL0
RC159 1 @ 2 10K_0201_5%

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.
Title: WHL-U(6/12)GPIO,I2C,GSPI
Size: Custom | Document Number: LA-H081P | Rev: 0.2
Date: Monday, October 22, 2018 | Sheet 11 of 53


UC1H
dGPU
SSD1
Card Reader
NGFF WLAN+BT
SSD2
USB2.0 / 3.0 Port (IO - 1)
USB2.0 / 3.0 Port (IO - 2)
USB2.0 / 3.0 Port (Type-C)
USB2.0 / 3.0 Port (MB - 1)
USB2.0 / 3.0 Port (MB - 2)
USB2.0 / 3.0 Port (Type-C)
Touch Screen
Camera
Finger Print
NGFF WLAN+BT
Trace length max: 450mils
CFLU-43E_BGA1528
8 of 20
When PCIE16/SATA2 is used as SATA Port 1 (ODD), then PCIE15/SATA1B (M.2 SSD) cannot be used as SATA Port 1.
+3VALW
+3VS
Compal Secret Data
Compal Electronics, Inc.
WHL-U(7/12)PCIE,USB,SATA
LA-H081P
Issued Date 2018/04/09
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+1.05VALW TO +1.05V_VCCST

I(Max) : 0.16 A(+1.05V_VCCST)
RON(Max) : 25 mohm
V drop : 0.004 V

Follow 543977_SKL_PDDG_Rev0_91
CC24 10PF ->22us(Spec:<= 65us)

+1.8VALW TO +1.8VS

I(Max) : 0.2 A(+1.8VS)
RON(Max) : 25 mohm
V drop : 0.005 V

+1.05VALW TO +1.05VS_VCCIO

I(Max) : 3.675 A(+1.05VS_VCCIO)
RON(Max) : 6.2 mohm
V drop : 0.019 V

Trace Length Match < 25 mils

change package of 1U from 0201 to 0402

change package of 1U from 0201 to 0402

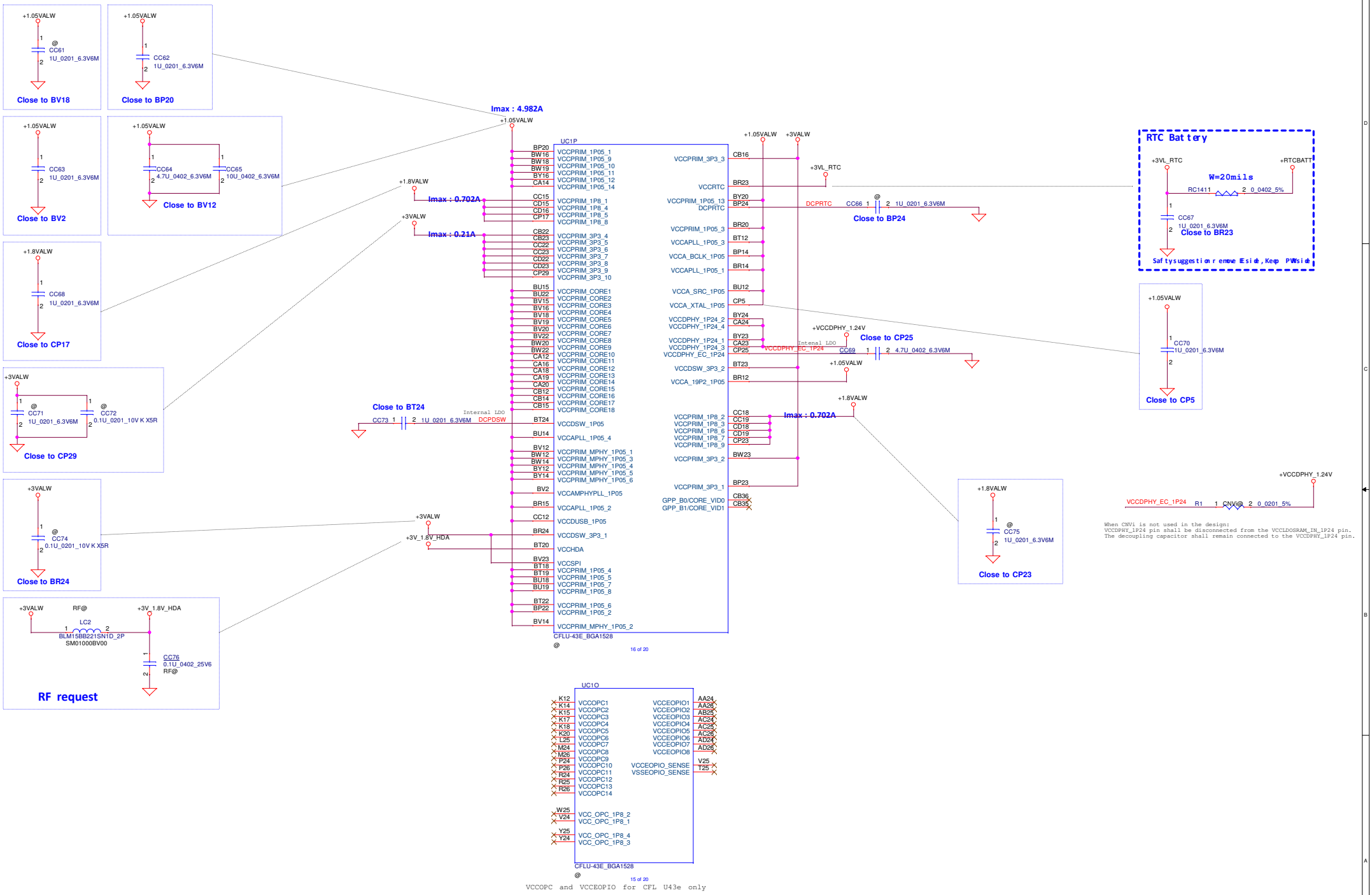
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: WHL-U(8/12)Power

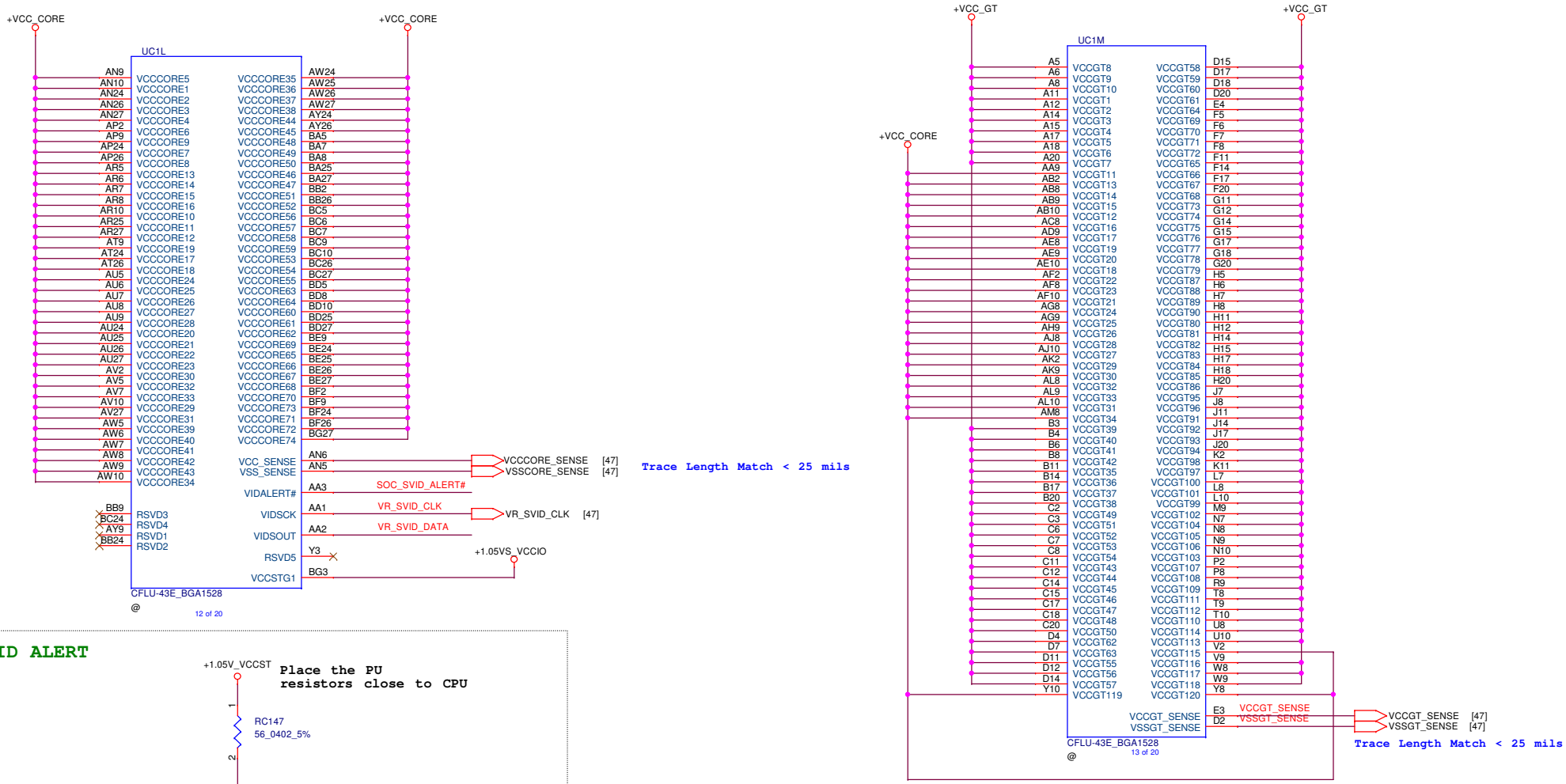
Size: Custom | Document Number: LA-H081P | Rev: 0.2

Date: Monday, October 22, 2018 | Sheet 13 of 53



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.			
Title	WHL-U(9/12)Power		
Size Custom	Document Number LA-H081P		Rev 0.2
Date: Monday, October 22, 2018	Sheet 14 of 53		



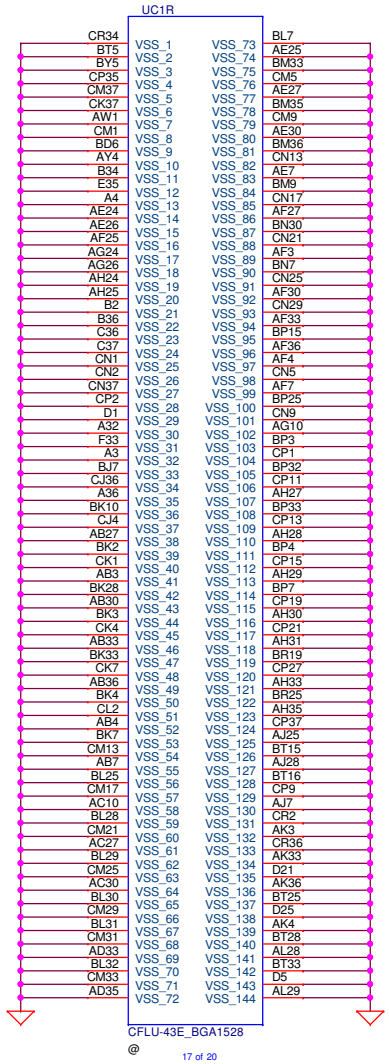
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

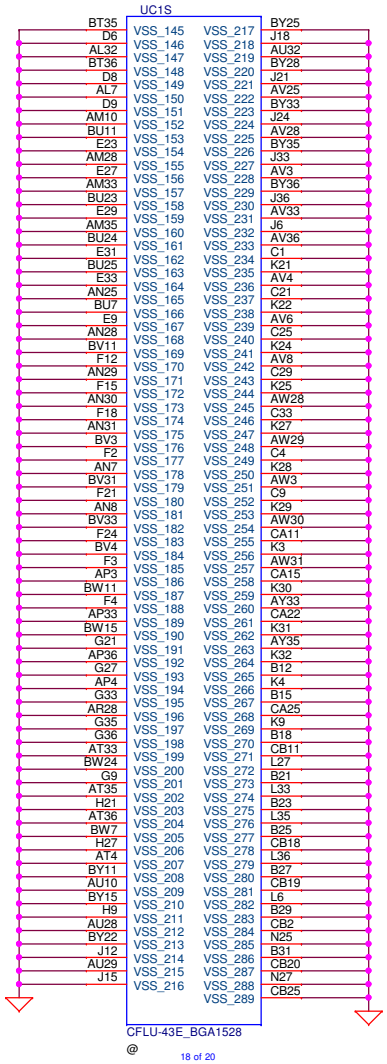
Compal Electronics, Inc.

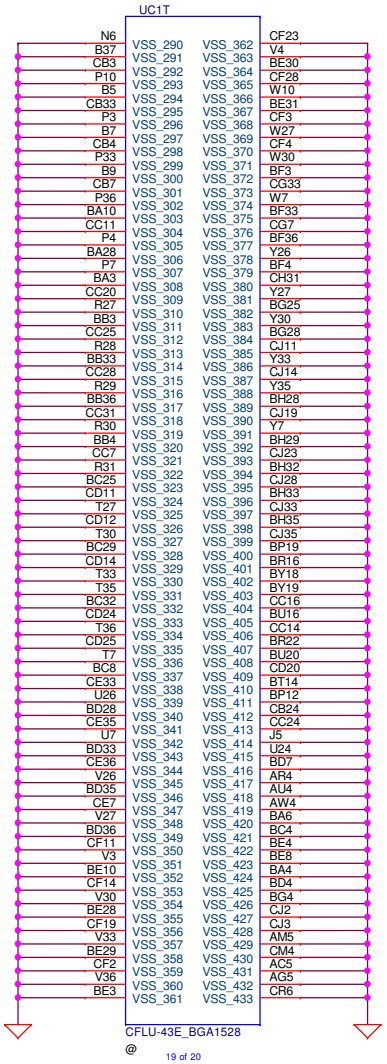
Title: WHL-U(10/12)Power,SVID

Size	Document Number	Rev
Custom	LA-H081P	0.2

Date: Monday, October 22, 2018 Sheet 15 of 53







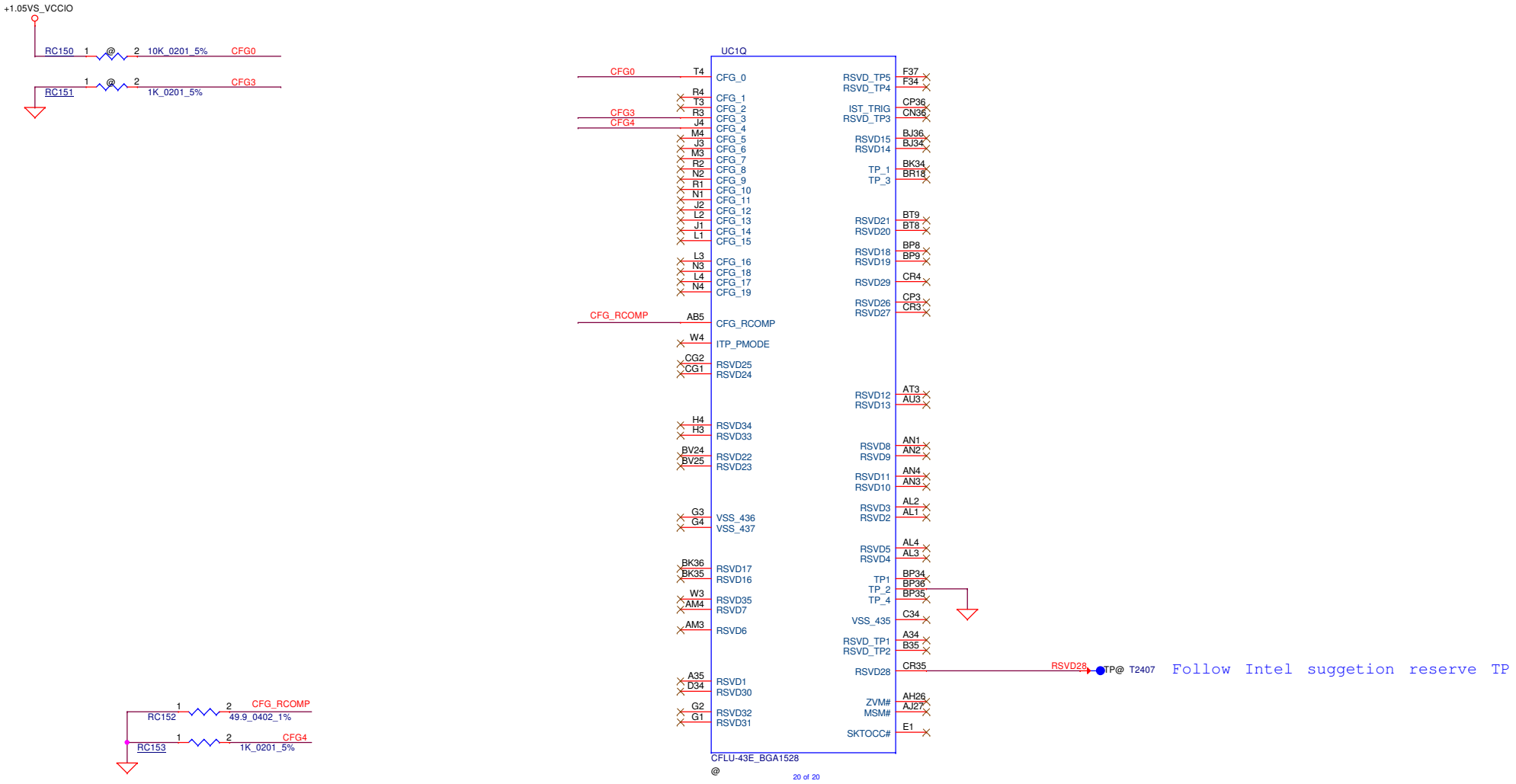
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: **WHL-U(11/12)GND**

Size	Document Number	Rev
Custom	LA-H081P	0.2

Date: Monday, October 22, 2018 | Sheet 16 of 53

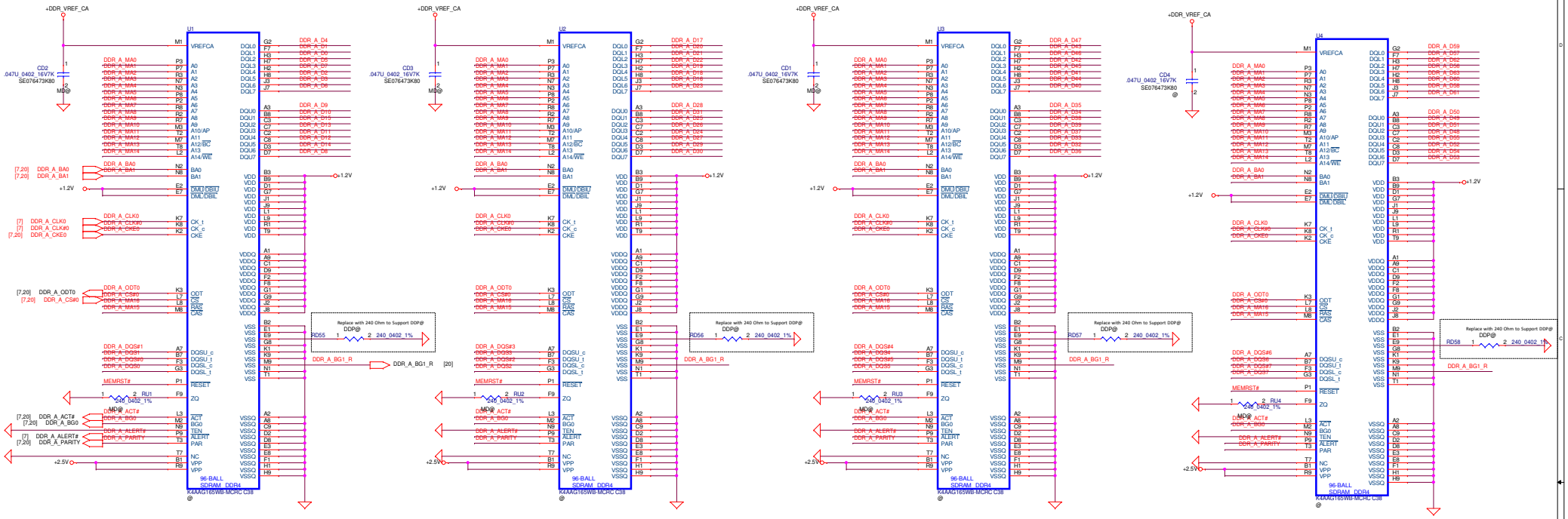


DFX Privacy Strap	
CFG3	1 : Disabled; Set DFX disable bit in debug interface MSR 0 : Enabled; Set DFX enable bit in debug interface MSR

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port at t achedt o E mbedded D sp ay port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

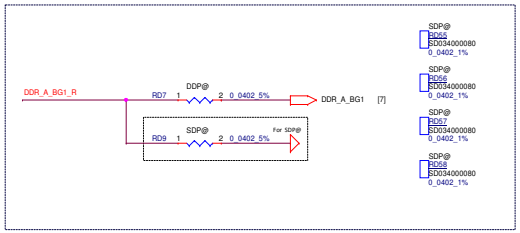
Compal Electronics, Inc.		
Title: WHL-U(12/12)CFG,RSVD		
Size: Custom	Document Number: LA-H081P	Rev: 0.2
Date: Monday, October 22, 2018	Sheet 17 of 53	

Interleaved Memory

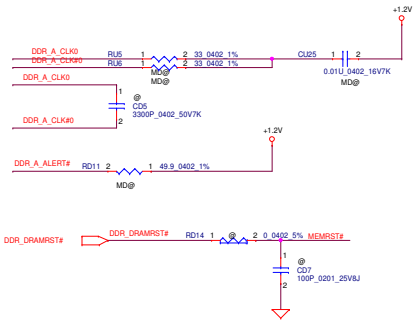


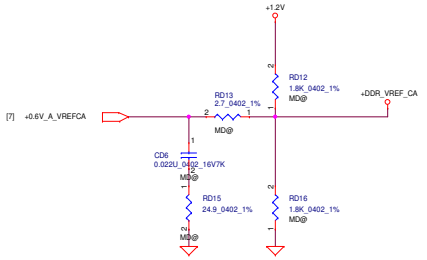
[7,20] DDR_A_MA[0..16]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_DQS[0..7]
[7] DDR_A_D[0..63]

Co-lay for SDP / DDP Memory DIE



CLOCK TERMINATION





On Board RAM - Data Mapping

U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Title	DDR4 ON BOARD CHIPS		
Size: Custom	Document Number: LA-H081P		Rev: 0.2
Date: Monday, October 22, 2018	Sheet 18 of 53		

Reverse Type

2-3A to 1 DIMMs/channel

[7] DDR_B_DQS#[0..7]
[7] DDR_B_D[0..63]
[7] DDR_B_DQS[0..7]

[7] DDR_B_MA[0..16]
[7] DDR_B_BA0 — DDR_B_BA0
[7] DDR_B_BA1 — DDR_B_BA1
[7] DDR_B_BG0 — DDR_B_BG0
[7] DDR_B_BG1 — DDR_B_BG1

[7] DDR_B_CLK0 — DDR_B_CLK0
[7] DDR_B_CLK#0 — DDR_B_CLK1
[7] DDR_B_CLK1 — DDR_B_CLK#1
[7] DDR_B_CLK#1

[7] DDR_B_CKE0 — DDR_B_CKE0
[7] DDR_B_CKE1 — DDR_B_CKE1
[7] DDR_B_CS#0 — DDR_B_CS#0
[7] DDR_B_CS#1 — DDR_B_CS#1

[8] SOC_SMBDATA — SOC_SMBDATA
[8] SOC_SMBCLK — SOC_SMBCLK

[7] DDR_B_ODT0 — DDR_B_ODT0
[7] DDR_B_ODT1 — DDR_B_ODT1

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

+1.2V

SE00000UC00 CD01 1U_0201_6.3V6M
SE00000UC00 CD02 1U_0201_6.3V6M
SE00000UC00 CD03 1U_0201_6.3V6M
SE00000UC00 CD04 1U_0201_6.3V6M
SE00000UC00 CD05 1U_0201_6.3V6M
SE00000UC00 CD06 1U_0201_6.3V6M
SE00000UC00 CD07 1U_0201_6.3V6M
SE00000UC00 CD08 1U_0201_6.3V6M
SE00000UC00 CD09 1U_0201_6.3V6M
SE00000UC00 CD10 1U_0201_6.3V6M

4 as near side of the DIMM close to VDD pins

+1.2V

SE00000UC00 CD11 1U_0201_6.3V6M
SE00000UC00 CD12 1U_0201_6.3V6M
SE00000UC00 CD13 1U_0201_6.3V6M
SE00000UC00 CD14 1U_0201_6.3V6M
SE00000UC00 CD15 1U_0201_6.3V6M
SE00000UC00 CD16 1U_0201_6.3V6M
SE00000UC00 CD17 1U_0201_6.3V6M
SE00000UC00 CD18 1U_0201_6.3V6M
SE00000UC00 CD19 1U_0201_6.3V6M
SE00000UC00 CD20 1U_0201_6.3V6M

Place these caps on the VTT plane close to DIMM

+0.6VS

SE00000UC00 CD21 1U_0201_6.3V6M
SE00000UC00 CD22 1U_0201_6.3V6M
SE00000UC00 CD23 1U_0201_6.3V6M
SE00000UC00 CD24 1U_0201_6.3V6M
SE00000UC00 CD25 1U_0201_6.3V6M
SE00000UC00 CD26 1U_0201_6.3V6M
SE00000UC00 CD27 1U_0201_6.3V6M
SE00000UC00 CD28 1U_0201_6.3V6M
SE00000UC00 CD29 1U_0201_6.3V6M
SE00000UC00 CD30 1U_0201_6.3V6M

+3VS

CD31 2.2U_0402_6.3V6M
+3VS
CD32 0.1U_0201_10V6K
close to DIMM

+2.5V

@ CD
10U_0402_6.3V6M
SE00000UD00
CD33 1U_0201_6.3V6M
SE00000UC00

JDIMM1

DDR_B_D1	1	VSS1	2	VSS2	DDR_B_D0
	3	DQ5	4	DQ4	
DDR_B_D4	5	VSS3	6	VSS4	DDR_B_D5
	7	DQ1	8	DQ0	
DDR_B_DQS#0	9	VSS5	10	VSS6	
DDR_B_DQS0	11	DQS0_c	12	DM0_n/DBI0_n	
	13	DQS0_t	14	VSS7	
DDR_B_D6	15	VSS8	16	DQ6	DDR_B_D3
	17	DQ7	18	VSS9	DDR_B_D2
DDR_B_D7	19	VSS10	20	DQ2	
	21	DQ3	22	VSS11	DDR_B_D11
DDR_B_D9	23	VSS12	24	DQ12	
	25	DQ13	26	VSS13	DDR_B_D8
DDR_B_D13	27	VSS14	28	DQ8	
	29	DQ9	30	VSS15	DDR_B_DQS#1
	31	VSS16	32	DQS1_c	DDR_B_DQS1
	33	DM1_n/DBI_n	34	DQS1_t	
DDR_B_D10	35	VSS17	36	VSS18	DDR_B_D15
	37	DQ15	38	DQ14	
DDR_B_D14	39	VSS19	40	VSS20	DDR_B_D12
	41	DQ10	42	DQ11	
DDR_B_D32	43	VSS21	44	VSS22	DDR_B_D37
	45	DQ21	46	DQ20	
DDR_B_D36	47	VSS23	48	VSS24	DDR_B_D33
	49	DQ17	50	DQ16	
	51	VSS25	52	VSS26	
DDR_B_DQS#4	53	DQS2_c	54	DM2_n/DBI2_n	
DDR_B_DQS4	55	DQS2_t	56	VSS27	DDR_B_D35
	57	VSS28	58	DQ22	
DDR_B_D39	59	DQ23	60	VSS29	DDR_B_D34
	61	VSS30	62	DQ18	
DDR_B_D38	63	DQ19	64	VSS31	DDR_B_D40
	65	VSS32	66	DQ28	
DDR_B_D45	67	DQ29	68	VSS33	DDR_B_D41
	69	VSS34	70	DQ24	
DDR_B_D44	71	DQ25	72	VSS35	DDR_B_DQS#5
	73	VSS36	74	DQS3_c	DDR_B_DQS5
	75	DM3_n/DBI3_n	76	DQS3_t	
	77	VSS37	78	VSS38	DDR_B_D46
DDR_B_D42	79	DQ30	80	DQ31	
DDR_B_D43	81	VSS39	82	VSS40	DDR_B_D47
	83	DQ26	84	DQ27	
	85	VSS41	86	VSS42	
	87	CB4/NC	88	CB5/NC	
	89	VSS43	90	VSS44	
	91	CB1/NC	92	CB0/NC	
	93	VSS45	94	VSS46	
	95	DQS8_c	96	DM8_n/DBI_n/NC	
	97	DQS8_t	98	VSS47	
	99	VSS48	100	CB6/NC	
	101	CB2/NC	102	VSS49	
	103	VSS50	104	CB7/NC	
	105	CB3/NC	106	VSS51	
	107	VSS52	108	RESET_n	DDR_B_CKE1
DDR_B_CKE0	109	CKE0	110	CKE1	
	111	VDD1	112	VDD2	
DDR_B_BG1	113	BG1	114	ACT_n	DDR_B_ACT# [7]
DDR_B_BG0	115	BG0	116	ALERT_n	DDR_B_ALERT# [7]
	117	VDD3	118	VDD4	
DDR_B_MA12	119	A12	120	A11	DDR_B_MA11
DDR_B_MA9	121	A9	122	A7	DDR_B_MA7
	123	A8	124	VDD5	
DDR_B_MA8	125	VDD5	126	A5	DDR_B_MA5
DDR_B_MA6	127	A6	128	A4	DDR_B_MA4
	129	VDD7	130	VDD8	
DDR_B_MA3	131	A3	132	A2	DDR_B_MA2
DDR_B_MA1	133	A1	134	EVENT_n/NF	
	135	VDD9	136	VDD10	
DDR_B_CLK0	137	CK0_t	138	CK1_t/NF	DDR_B_CLK1
DDR_B_CLK#0	139	CK0_c	140	CK1_c/NF	DDR_B_CLK#1
	141	VDD11	142	VDD12	
	143	PARITY	144	A0	DDR_B_MA0
DDR_B_BA1	145	BA1	146	A10/AP	DDR_B_MA10
	147	VDD13	148	VDD14	
DDR_B_CS#0	149	CS0_n	150	BA0	DDR_B_BA0
DDR_B_MA14	151	WE_n/A14	152	RAS_n/A16	DDR_B_MA16
	153	VDD15	154	VDD16	
DDR_B_ODT0	155	ODT0	156	CAS_n/A15	DDR_B_MA15
DDR_B_CS#1	157	CS1_n	158	A13	DDR_B_MA13
DDR_B_ODT1	159	VDD17	160	VDD18	
	161	ODT1	162	C0/CS2_n/NC	
	163	VDD19	164	VREFCA	
	165	C1_CS3_n,NC	166	SA2	DDR_B_SA2
	167	VSS53	168	VSS54	
DDR_B_D22	169	DQ37	170	DQ36	DDR_B_D23
DDR_B_D17	171	VSS55	172	VSS56	DDR_B_D16
	173	DQ33	174	DQ32	
DDR_B_DQS#2	175	VSS57	176	VSS58	
DDR_B_DQS2	177	DQS4_c	178	DM4_n/DBI4_n	
	179	DQS4_t	180	VSS59	
DDR_B_D19	181	VSS60	182	DQ39	DDR_B_D21
DDR_B_D18	183	DQ38	184	VSS61	DDR_B_D20
	185	VSS62	186	DQ35	
DDR_B_D24	187	DQ34	188	VSS63	DDR_B_D29
DDR_B_D28	189	VSS64	190	DQ45	DDR_B_D25
	191	DQ44	192	VSS65	
	193	VSS66	194	DQ41	
	195	DQ40	196	VSS67	DDR_B_DQS#3
	197	VSS68	198	DQS5_c	DDR_B_DQS3
	199	DM5_n/DBI5_n	200	DQS5_t	
DDR_B_D31	201	VSS69	202	VSS70	DDR_B_D27
DDR_B_D30	203	DQ46	204	DQ47	
	205	VSS71	206	VSS72	DDR_B_D26
DDR_B_D52	207	DQ42	208	DQ43	DDR_B_D49
DDR_B_D53	209	VSS73	210	VSS74	
	211	DQ52	212	DQ53	DDR_B_D48
DDR_B_DQS#6	213	VSS75	214	VSS76	
DDR_B_DQS6	215	DQ49	216	DQ48	
	217	VSS77	218	VSS78	
	219	DQS6_c	220	DM6_n/DBI6_n	
DDR_B_D55	221	DQS6_t	222	VSS79	DDR_B_D50
	223	VSS80	224	DQ54	
DDR_B_D54	225	DQ55	226	VSS81	DDR_B_D51
DDR_B_D60	227	VSS82	228	DQ50	DDR_B_D56
	229	DQ51	230	VSS83	
DDR_B_D57	231	VSS84	232	DQ60	DDR_B_D61
	233	DQ61	234	VSS85	
	235	VSS86	236	DQ57	
	237	DQ56	238	VSS87	DDR_B_DQS#7
	239	VSS88	240	DQS7_c	DDR_B_DQS7
	241	DM7_n/DBI7_n	242	DQS7_t	
	243	VSS89	244	VSS90	DDR_B_D59
DDR_B_D62	245	DQ62	246	DQ63	
DDR_B_D63	247	VSS91	248	VSS92	DDR_B_D58
	249	DQ58	250	DQ59	
SOC_SMBCLK	251	VSS93	252	VSS94	SOC_SMBDATA
+3VS	253	SCL	254	SDA	DDR_B_SA0
	255	VDDSPD	256	SA0	
	257	VPP1	258	VTT	
	259	VPP2	260	SA1	DDR_B_SA1
	261	GND1	262	GND2	

DEREN_40-42271-26001RHF
SP07001CY00
ME@

[7] DDR_B_PARITY

+1.2V
+2.5V
+0.6VS
+1.2V

DDR_DRAMRST#_R
CD17 100P_0402_50V8J ESD@
DDR_DRAMRST# [7,18]

+DIMM_VREF_DQ

+1.2V
20mil
[7] +0.6V_B_VREFDQ
RD18 2_0402_1%
CD8 0.022U_0402_16V7K
RD19 24.9_0402_1%
RD17 1K_0402_1%
RD20 1K_0402_1%
+DIMM_VREF_DQ

+1.2V
RD23 470_0402_1%
DDR_DRAMRST#_R
RD24 2_0_0402_5%
DDR_DRAMRST# [7,18]

JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)

+3VS
DDR_B_SA2
DDR_B_SA1
DDR_B_SA0
RD27 0_0402_5%
RD28 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

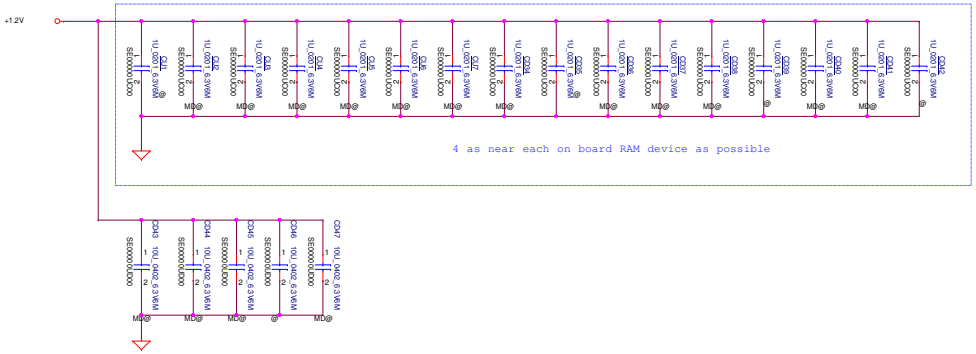
Compal Electronics, Inc.

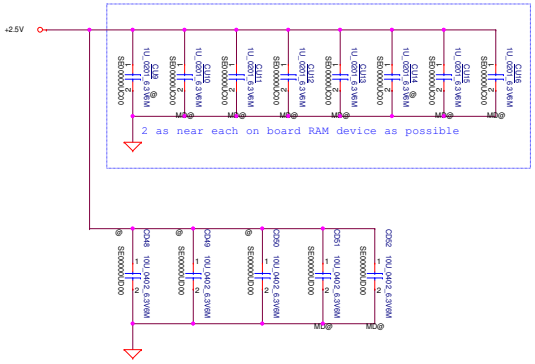
Title: **DDR4 DIMM**

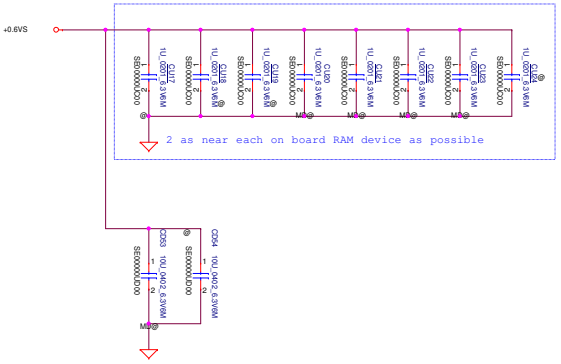
Size	Document Number	Rev
Custom	LA-H081P	0.2

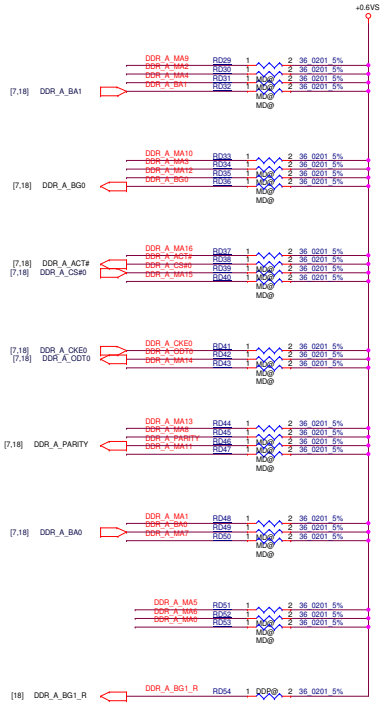
Date: Monday, October 22, 2018 Sheet 19 of 53

[7,18] DDR_A_MA[0..16]



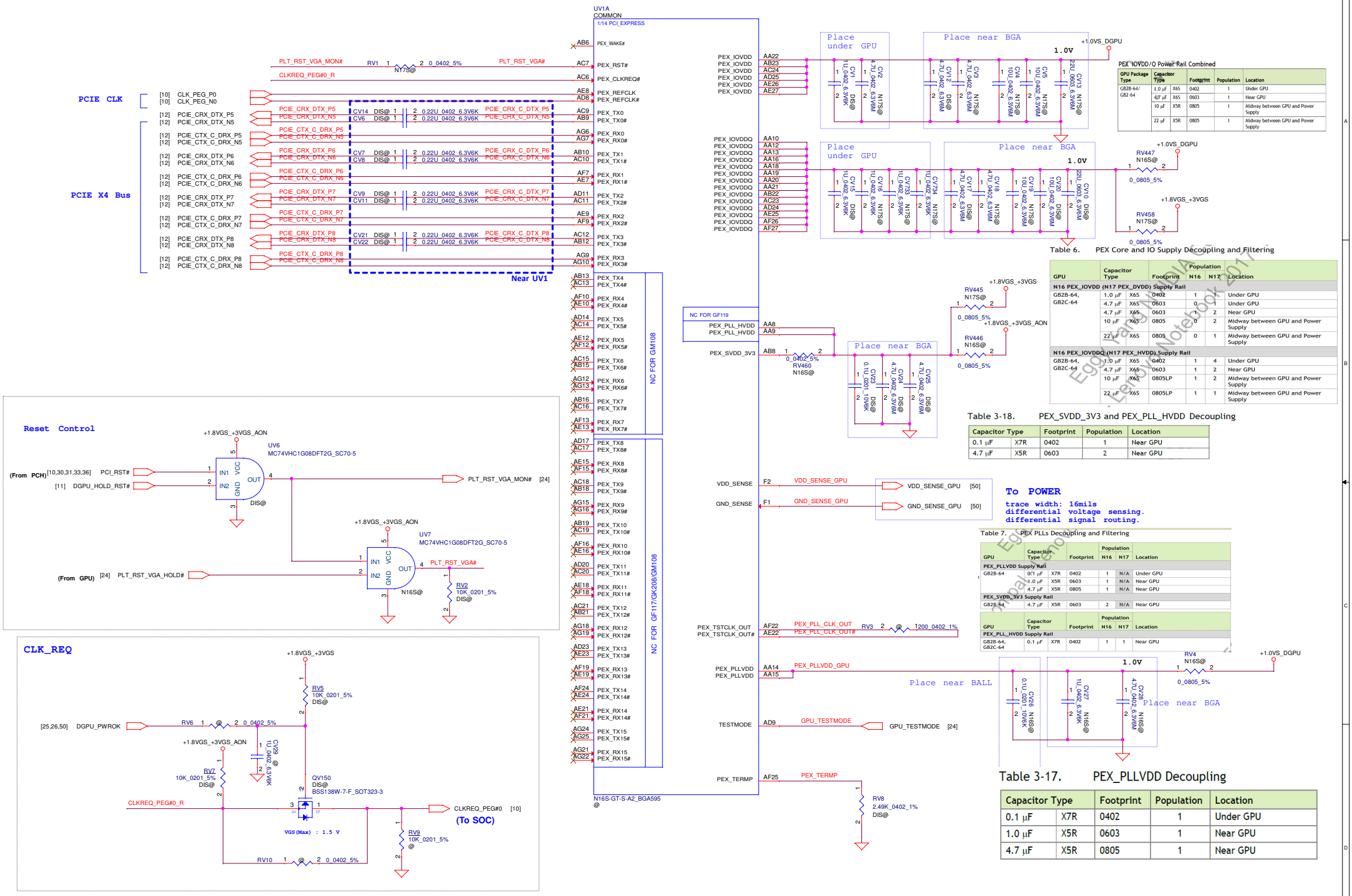






Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Title	DDR4 MISC		
Size: Custom	Document Number: LA-D562P		Rev: 0.2
Date: Monday, October 22, 2018	Sheet 20 of 53		



Capacitor Type	Footprint	Population	Location
0.1 µF	X7R	0402	1	Under GPU
1.0 µF	X5R	0603	1	Near GPU
4.7 µF	X5R	0805	1	Near GPU

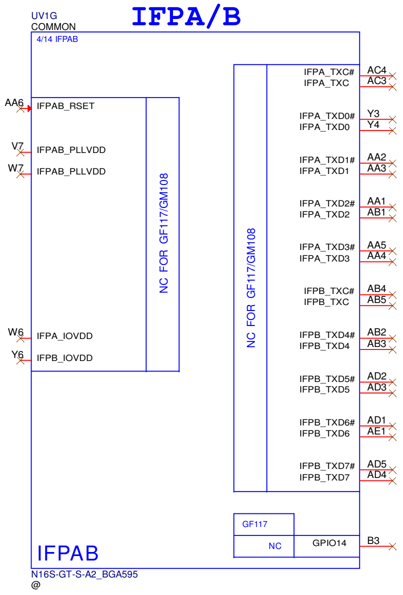
Security Classification	Compal Secret Data		
Issued Date	2017/10/27	Deciphered Date	2019/04/09

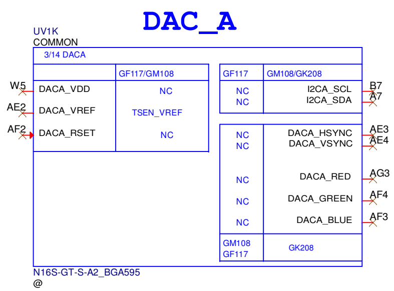
Compal Electronics, Inc.

Title: **NV(1/5)-PCIE**

Size: | Document Number: **LA-H081P** | Rev: 0.2

Date: Monday, October 22, 2018 | Sheet 21 of 53

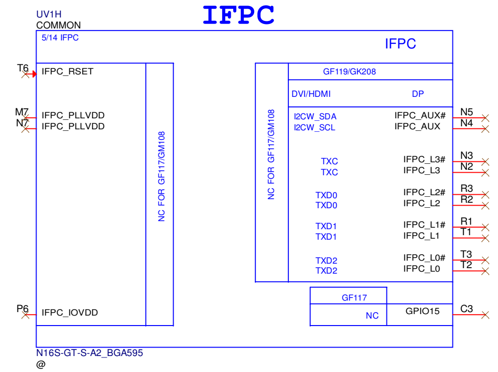


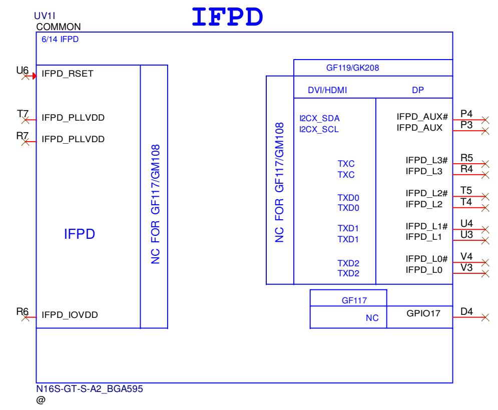


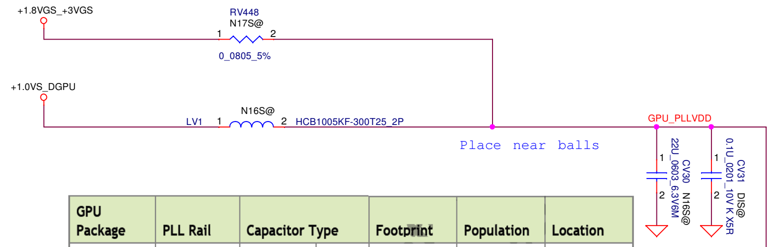
Note:
IFPC/D/E/F interface are XVDDs pin for N17S GPU, and connect them to NVDD power for improving NVDD power rail routing

Table 8. Other PLLs Power Decoupling and Filtering

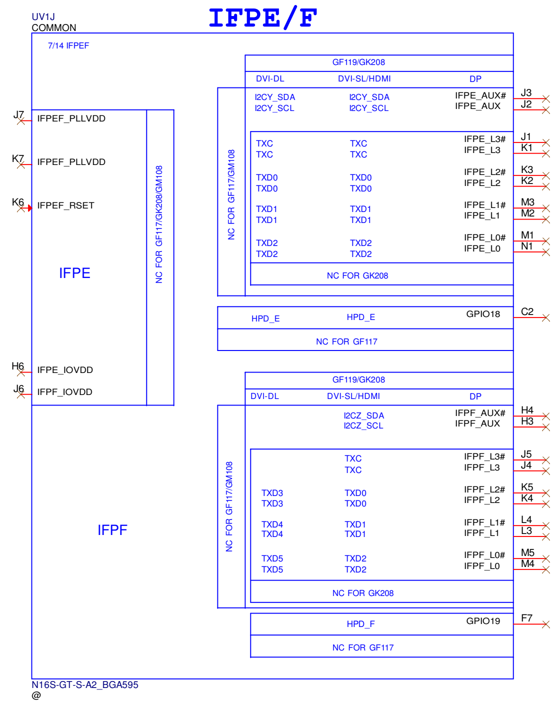
GPU	Type		Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Under GPU
	22 µF	X5R	0805	1	0	Near GPU
	Bead Type					
	L2=30 Ω (ESR=0.05 Ω)		0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	2	Under GPU
	10 µF	X5R	0603	1	0	Near GPU
	47 µF	X5R	0805	1	0	Near GPU
	Bead Type					
	L2=300 Ω (ESR=0.2 Ω)		0603	1	0	Near GPU







GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05 Ω)		0402	1	Near GPU



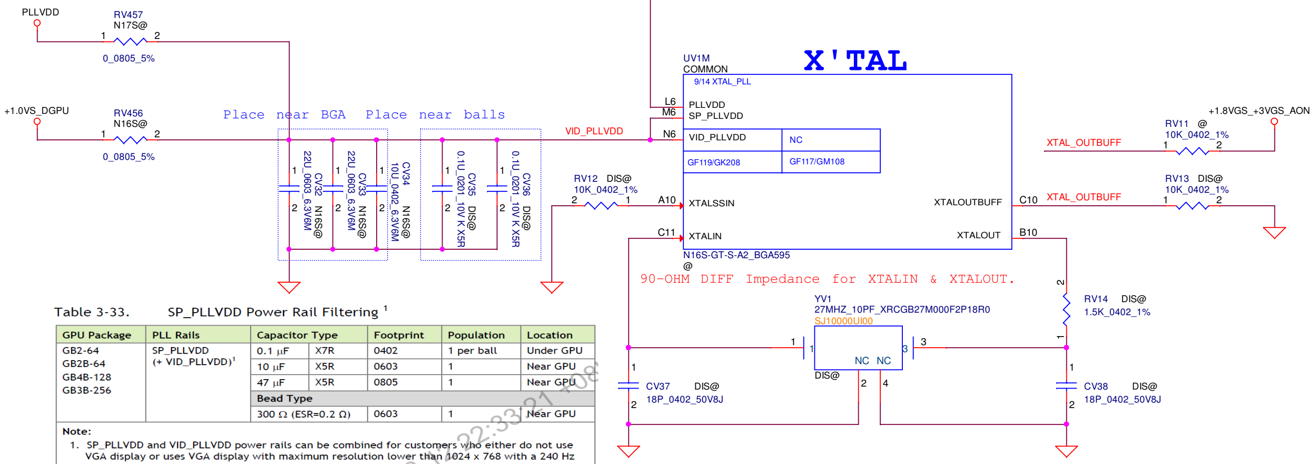


Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128, GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

Security Classification	Compal Secret Data		
Issued Date	2017/10/27	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: NV(2/5)-IFP_ABCDEF_DAC_XTAL

Size | Document Number: LA-H081P | Rev 0.2

GPU_Decoupling CAPs @ Power Page

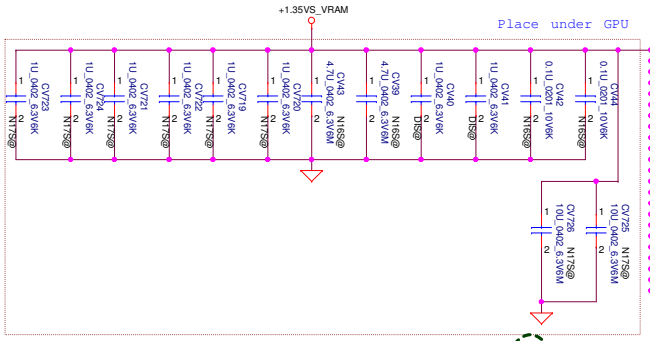
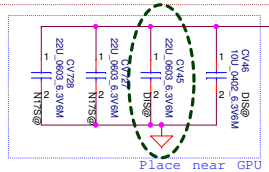


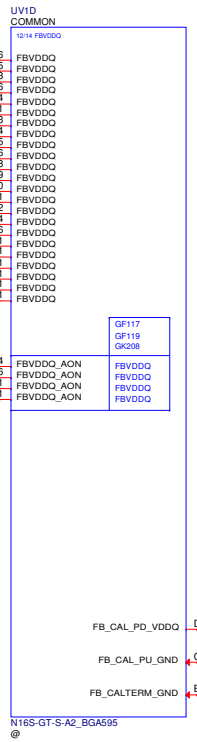
Table 4. Frame Buffer Core and IO Decoupling and Filtering

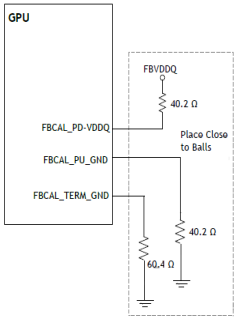
GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU



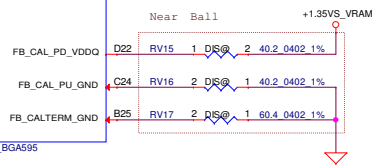
CIZ00 22uF x1 change to 10uF x2

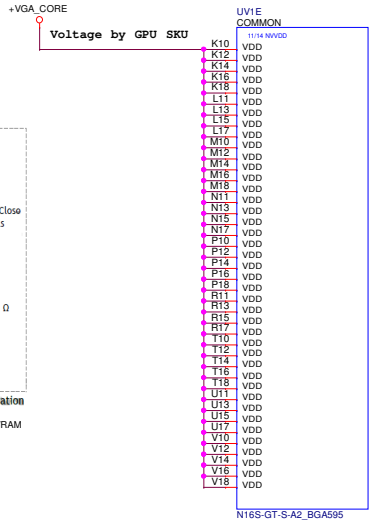
GPU Package Type	Capacitor Type	Footprint		Population	Location
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	Under GPU
	1 µF	X7R	0603	2	Under GPU
	4.7 µF	X6S	0603	2	Under GPU
	10 µF	X5R	0805	1	Near GPU
	22 µF	X5R	0805	1	Near GPU

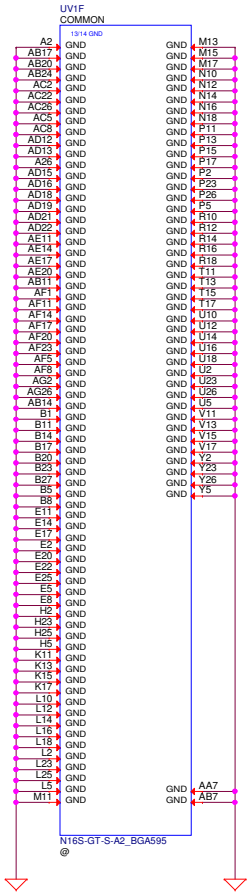


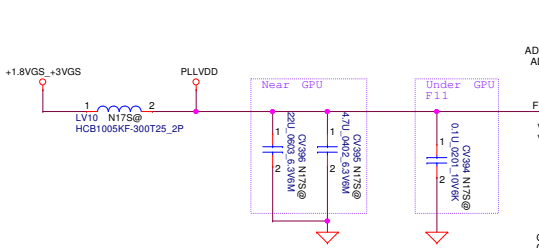


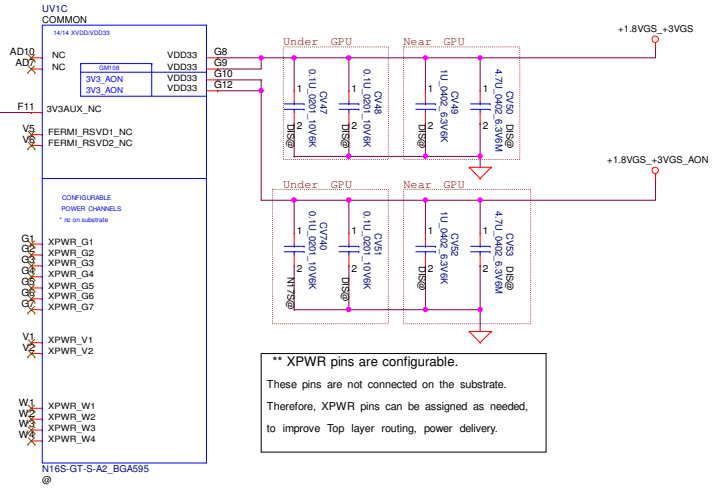
Note: Use only 1% resistors for driver calibration











** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed, to improve Top layer routing, power delivery.

NC (N17: GPCPLL_AVDD) Supply Rail						
GB2C-64	0.1 µF	X7R	0402	N/A	1	Under GPU
	4.7 µF	X6S	0603	N/A	1	Near GPU
	22 µF	X6S	0805	N/A	1	Near GPU
	Bead Type					
	L=30 Ω (ESR=0.010 Ω)		0603	N/A	1	Near GPU

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

Security Classification	Compal Secret Data		
Issued Date	2017/10/27	Deciphered Date	2019/04/09

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GPIO

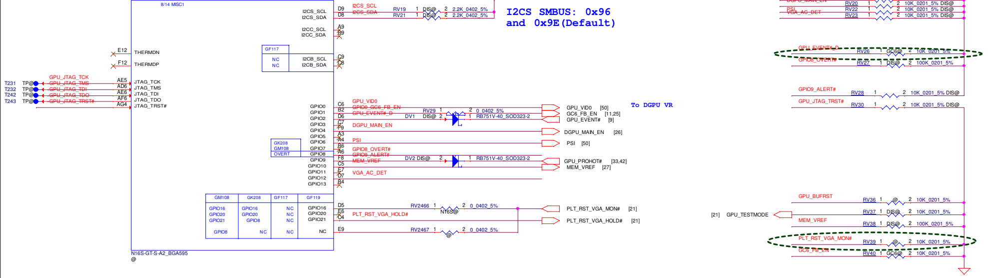
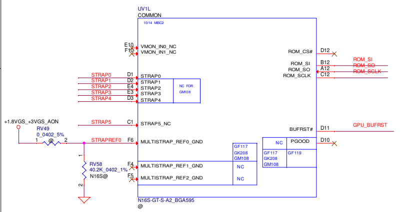


Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	GC6_FB_EN	O	FB Enable for GC6 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing for GC6 2.0, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO6	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10 kΩ pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset monitor	10 kΩ pull-up to 3V3_AON unless actively driven
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AON; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AON
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON



10.2.1 Unconnected Signals (NC)

Do not route unused I²C signals on the PCB in order to protect the GPU from outside ESD risk. If unused traces are routed, the signals should be pulled down to ground with 1.8 kΩ resistors.

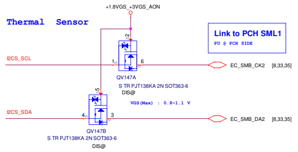
10.2.2 I²CS Slave Address

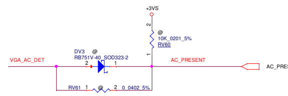
N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful I²CS Slave addresses can be used with SMB_ALT_ADDR strapping.

16.3.3 Internal Thermal Sensor Interface

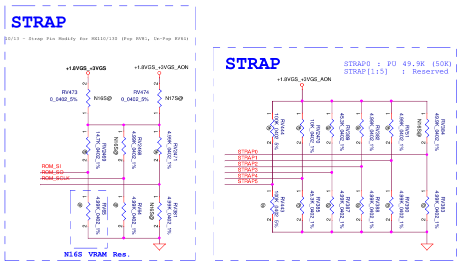
The internal thermal sensor can be accessed through the I²CS interface as described in the I²C chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the I²CS interface by the system is not supported. The default port address to access the internal thermal sensor over the I²CS is 0x9E. Table 16-1 describes the byte-wise register accessible through the I²CS interface.

Internal Thermal Sensor





STRAP



NV Suggest

GM108 SKU		
Item	N16V-GMR1(MX110)	N16S-GTR(MX130)
Device ID	0X174E	0X174D
Package	GB4B-128/GB2B-64	GB4B-128/GB2B-64
ROM_SI	Refer to N16x_RAM_Straps table	Refer to N16x_RAM_Straps table
ROM_SO	0x1000, 4.99Kohm pull high	0x1000, 4.99Kohm pull high
ROM_SCLK	0x0 for Optimus, 4.99Kohm pull down	0x0 for Optimus, 4.99Kohm pull down
Strap0	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)
Strap1 Strap2 Strap3 Strap4	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
Open_VRG SKU	B	B
NVVDD Boot Voltage	0.9V	0.9V

N17S-G0/G2 VRAM Strap

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE
0x9(LML) M2G	RV388 N17_M2G@ 100K_0402_5%	RV51 N17_M2G@ 100K_0402_5% RV390 N17_M2G@ 100K_0402_5%	RV383 N17_M2G@ 100K_0402_5%	
0xA(LMH) H2G	RV388 N17_H2G@ 100K_0402_5%	RV51 N17_H2G@ 100K_0402_5% RV390 N17_H2G@ 100K_0402_5%	RV384 N17_H2G@ 100K_0402_5%	

N17S-G1 VRAM Strap

Table 4. N17S-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]

RAM_CFG	STRAP2	STRAP1	STRAP0	
0x00(LLL) S2G	RV388 @	RV390 @	RV383 @	
0x01(LLH)				
0x02(LHL)				
0x03(LHH)				
0x04(HLL) M2G	RV382 @	RV390 @	RV383 @	
0x05(HLH) H2G	RV382 @	RV390 @	RV384 @	
0x06(HHL)				
0x07(HHH)				
0x08(LLM)				

N17S Strap

	ROM_SI	ROM_SO	ROM_SCLK	STRAP3	STRAP4	STRAP5
Strap	RV2469 N17S@ S RES 1/16W 100K +-5% 0402	RV2468 N17S@ S RES 1/16W 100K +-5% 0402	RV2471 N17S@ S RES 1/16W 100K +-5% 0402 RV381 N17S@ S RES 1/16W 100K +-5% 0402	RV387 N17S@ S RES 1/16W 100K +-5% 0402	RV385 N17S@ S RES 1/16W 100K +-5% 0402	RV443 N17S@ S RES 1/16W 100K +-5% 0402

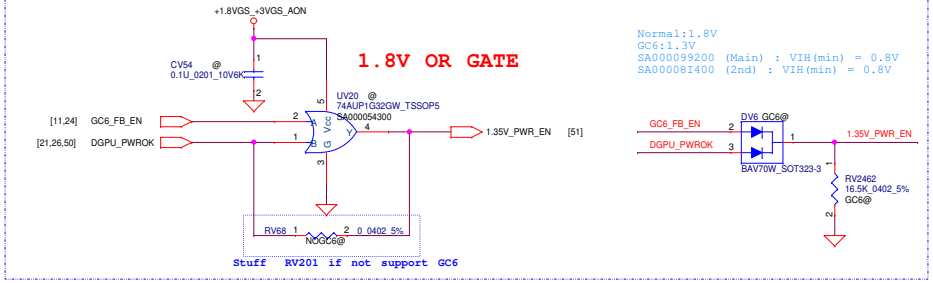
Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

For GC6



From DG-07158-001_v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

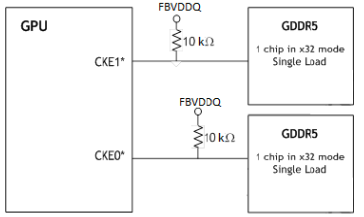


Figure 7-4. Clock Enable (CKE*) Signal Connection, ×32 Mode

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10 k Ω pull-down resistor in standard mode or in clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

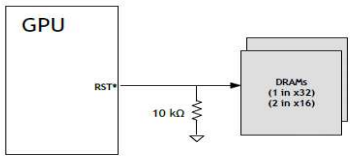


Figure 7-3. Reset Signal Connection

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

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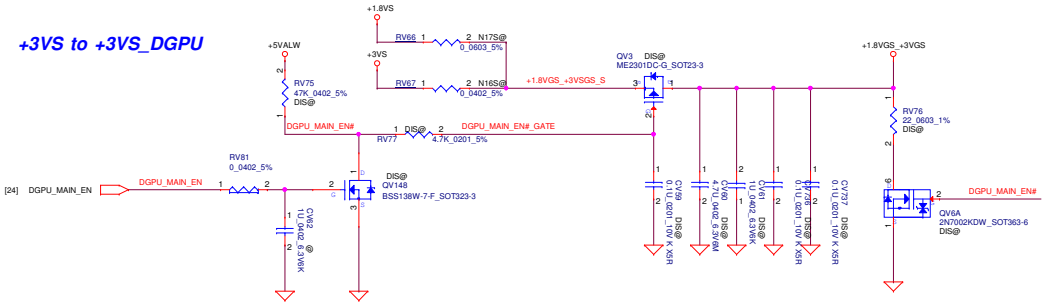
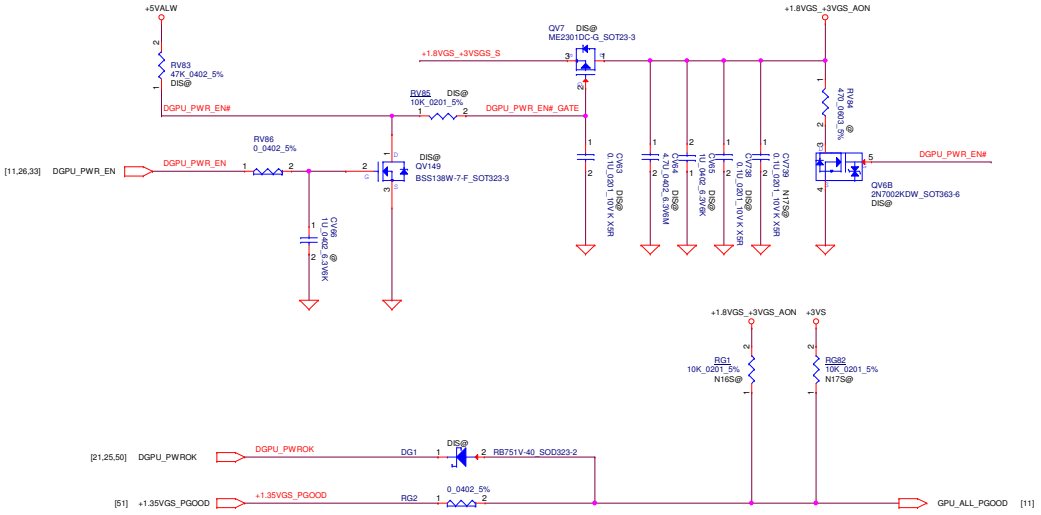
+3VS to +3VS_DGPU



+3VS to +3VS_DGPU_AON



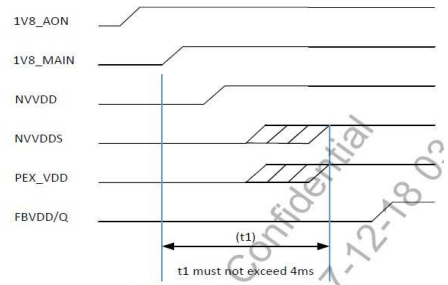
7.3.2.1 Power-Up Sequence

The following power-up sequence is required:

1V8_AON ➔ 1V8_MAIN ➔ NVVDD ➔ NVVDDS / PEX_DVDD ➔ FBVDD(Q)

- All GPU power rails must ramp up after 1V8_AON.
- FBVDD(Q) should ramp up after NVVDDS and PEX_DVDD.

All other 1.8V power rails can ramp up with 1V8_MAIN including PEX_HVDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX_DVDD.



re 7.5 Example of Power-Up Sequencing Order

7.3.2.2 Power-Down Sequence

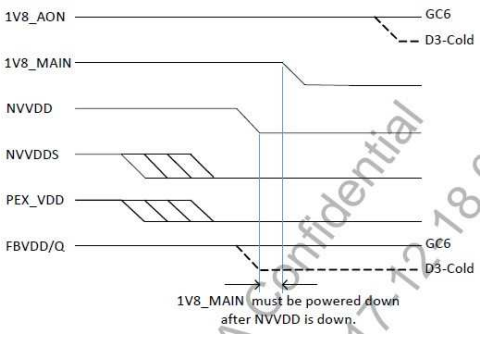
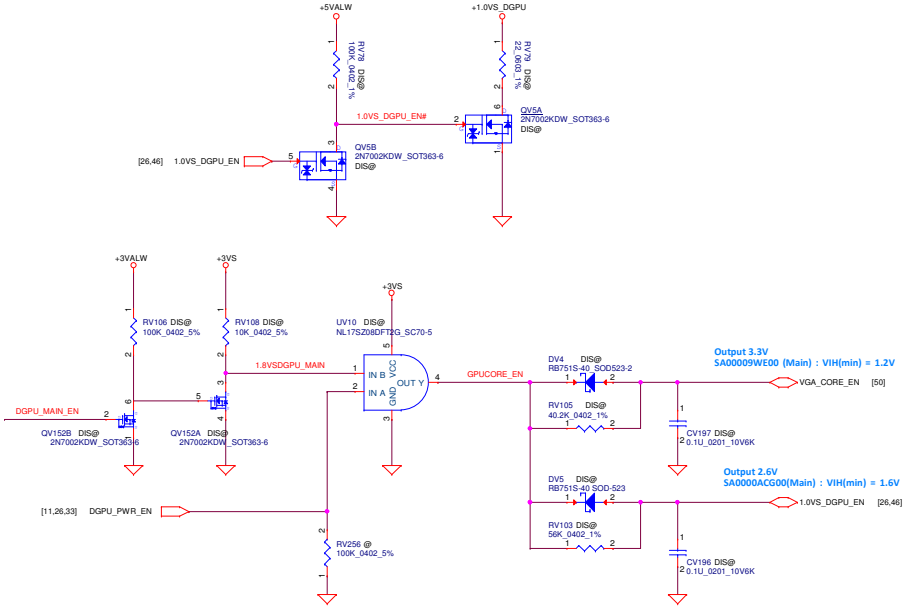


Table 7. Output EDP-Continuous

Product	NVVDD (A)	GPU FBIO — (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-LG	15.4	2.5	5.0	0.1	0.2
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-G0[6]	27.8	3.2	5.8	0.2	0.5
N17S-G2[6]	28.6	3.2	5.8	0.2	0.5



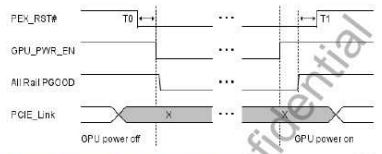


Figure 8.9 GC OFF Entry/Exit Timing Diagram

Table 8.1 GC OFF Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Security Classification	Compal Secret Data		
Issued Date	2017/10/27	Deciphered Date	2019/04/09

Compal Electronics, Inc.			
Title: DGPU_DC/DC Interface			
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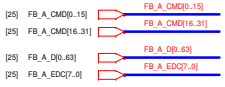
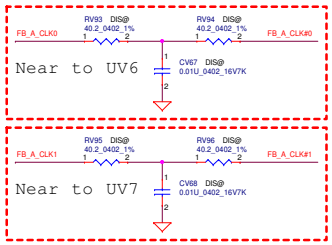
VRAM Memory Partition A

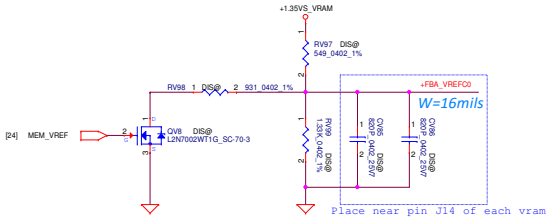
Table 7-4. GDDR5 Mode H Mapping

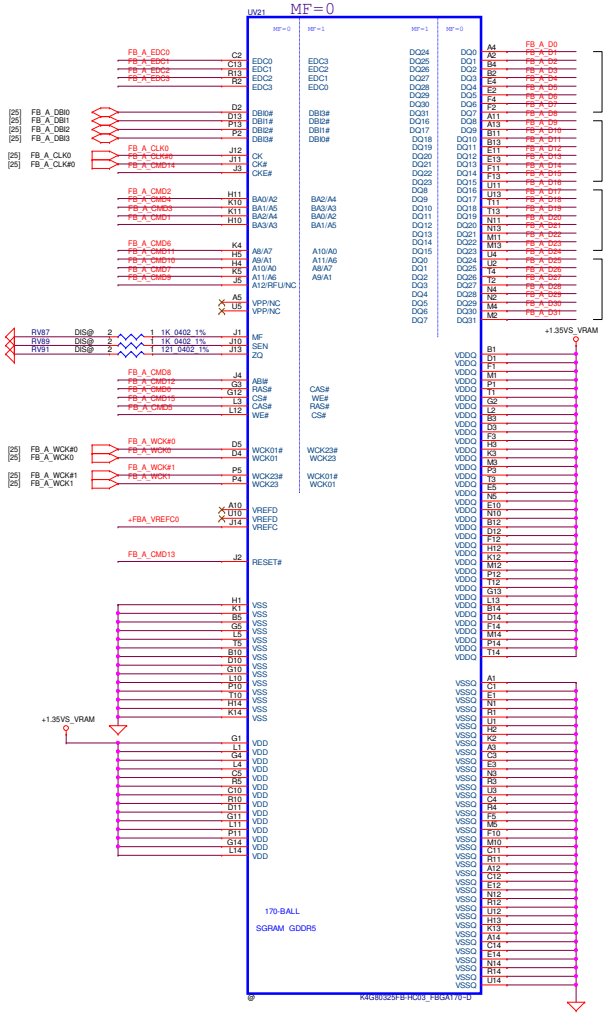
GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG2[2]		
CMD35	DEBUG1[2]		

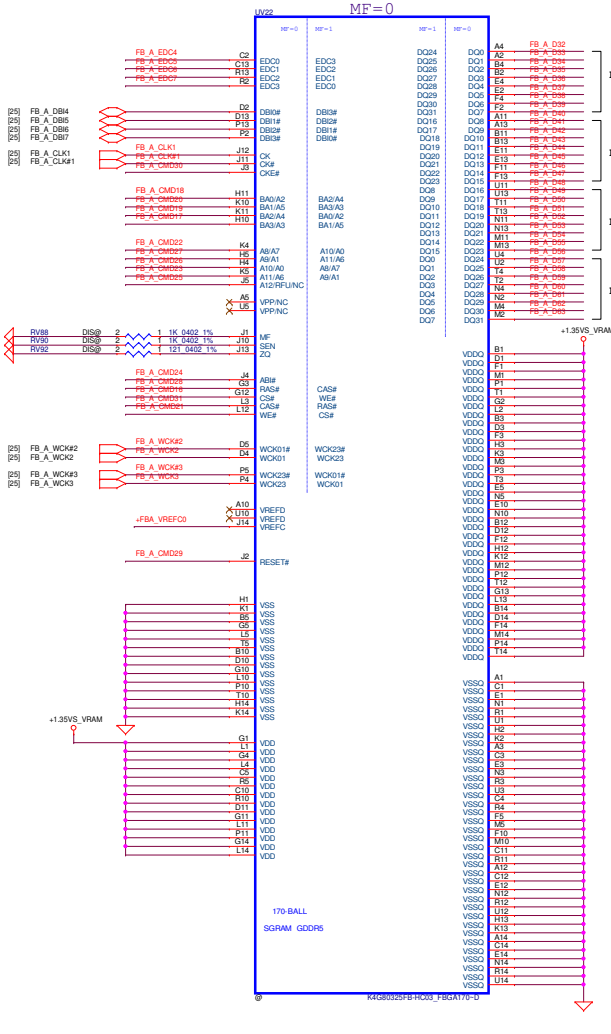
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to DRAM, see section 7.1.13.

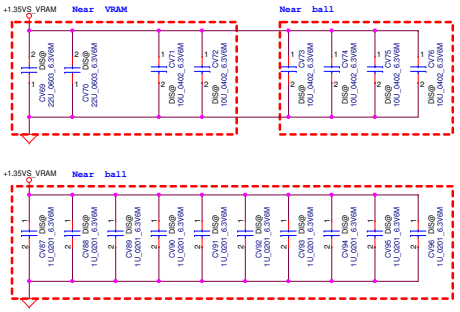


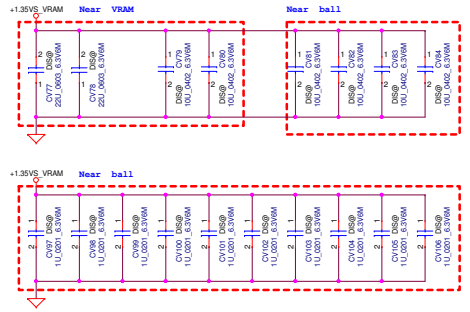












Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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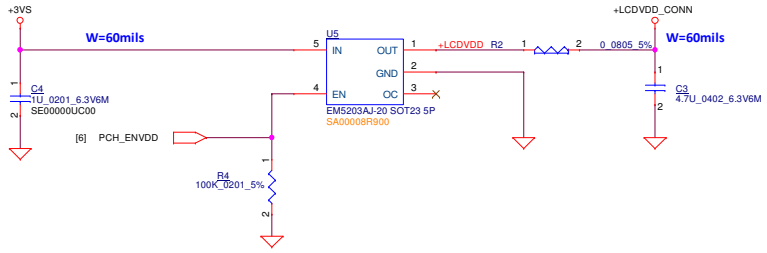
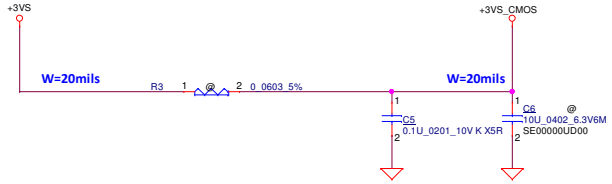
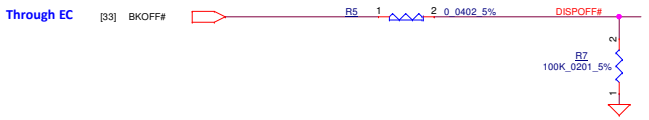
LCD POWER SWITCH



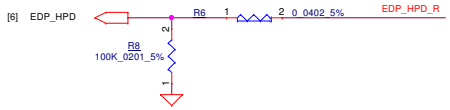
CAMERA POWER CIRCUIT



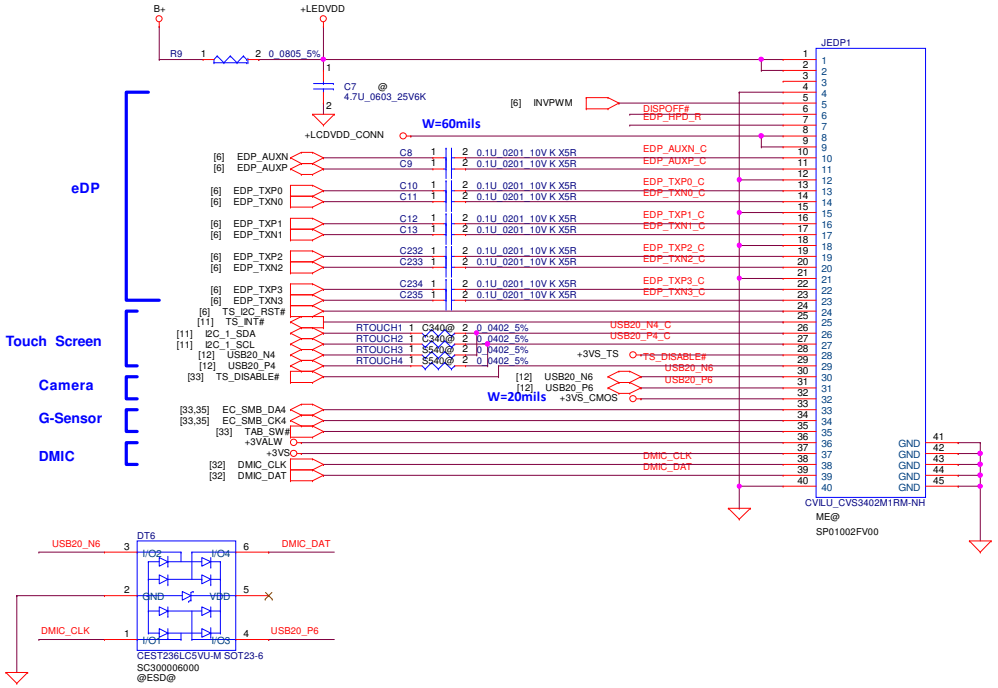
DISPLAY OFF



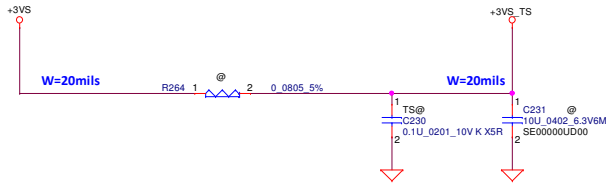
HOT PLUG DETECT



eDP CONNECTOR



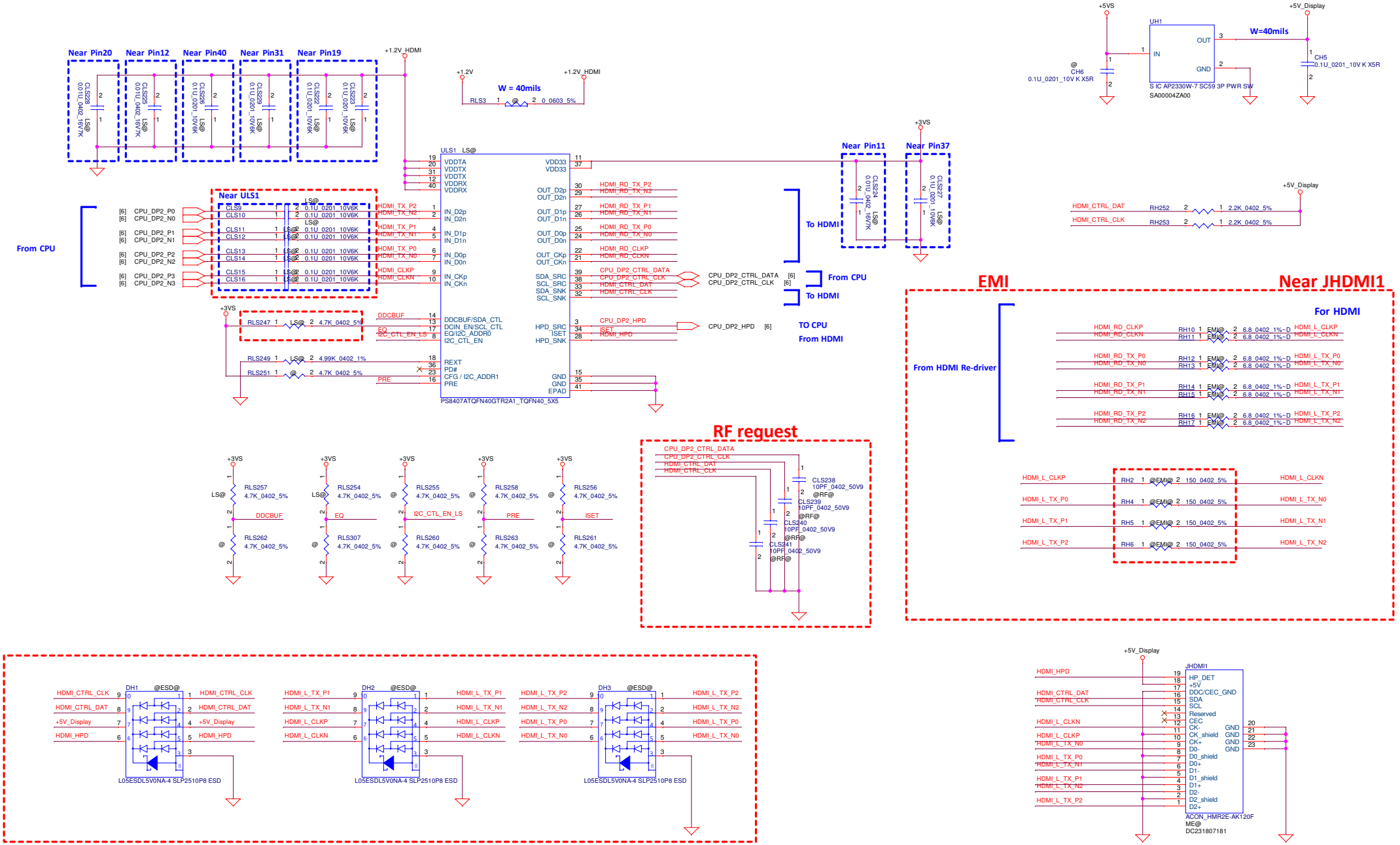
Touch Screen POWER CIRCUIT



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.			
Title: eDP / Camera / MIC			
Size: Custom	Document Number: LA-H081P		Rev: 0.2
Date: Monday, October 22, 2018	Sheet 28 of 53		

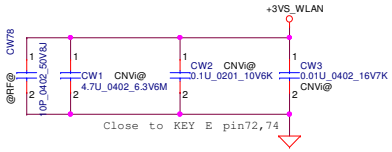
HDMI



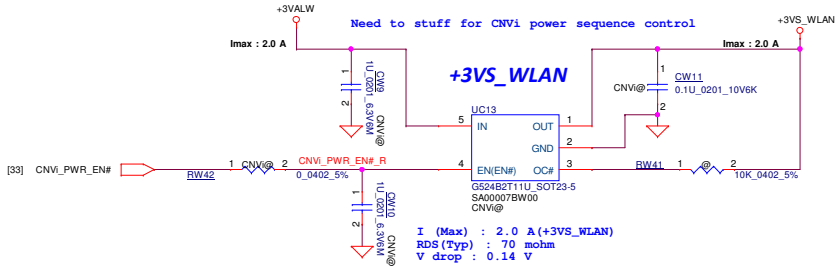
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

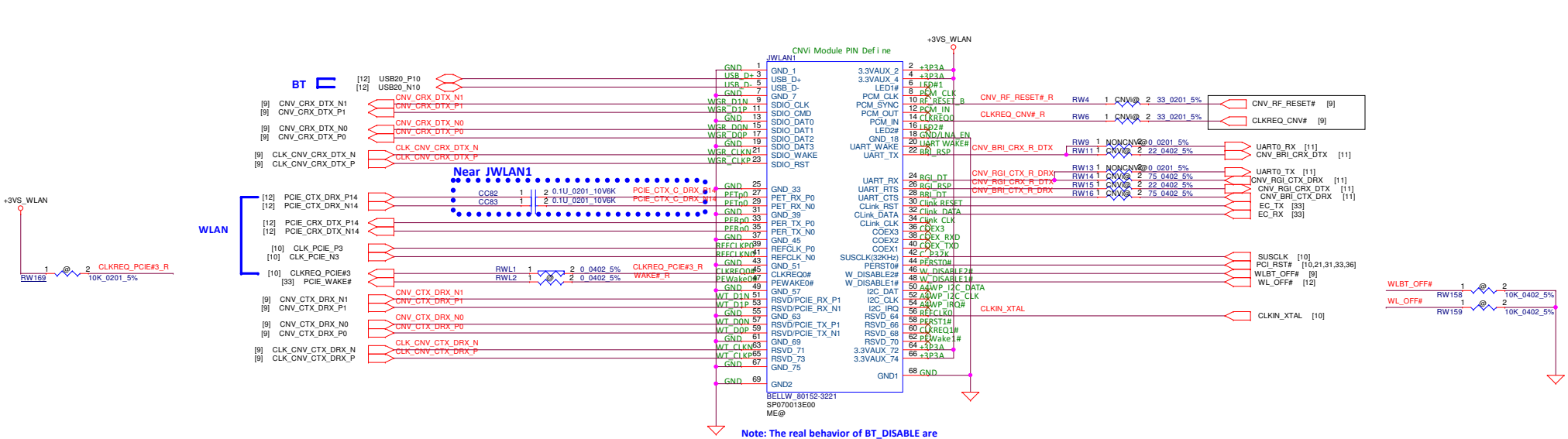
Compal Electronics, Inc.			
Title	HDMI		
Size	Document Number		Rev
Custom	LA-H081P		0.2
Date: Monday, October 22, 2018	Sheet	29 of	53

NGFF WLAN /BT(Key E)



Jefferson Peak:1360mA@peak current
Thunder_Peak_2:1100mA@peak current





Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

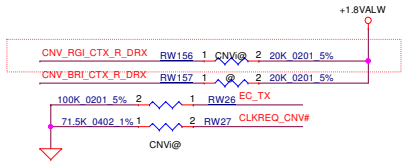
The connectivity module power supply pin shall be connected directly to thr rail DSW.
From 567240_Intel_Wireless_AC_9560_Jefferson_Peak_EPS_Rev1.1

PCH EDS : M.2 CNV Mode Select

GPP_F6/CNV_RGI_DT

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.	
Title	NGFF WLAN / BT
Size	Document Number: LA-H081P
Rev	0.2
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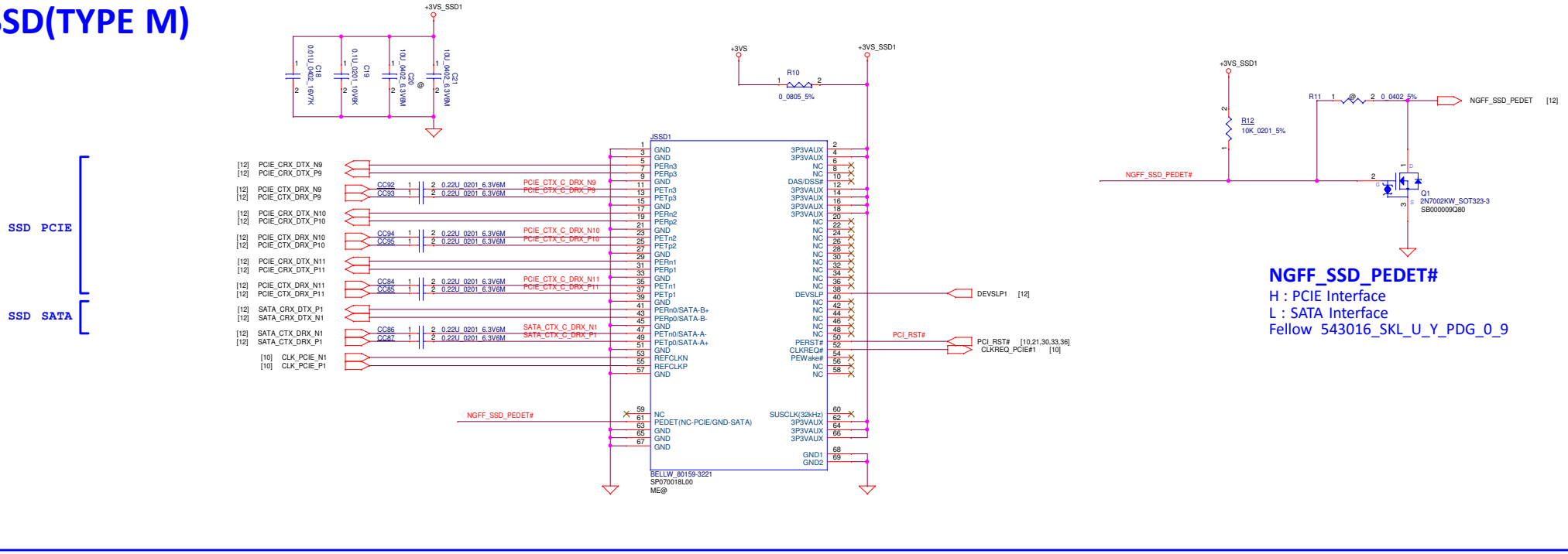
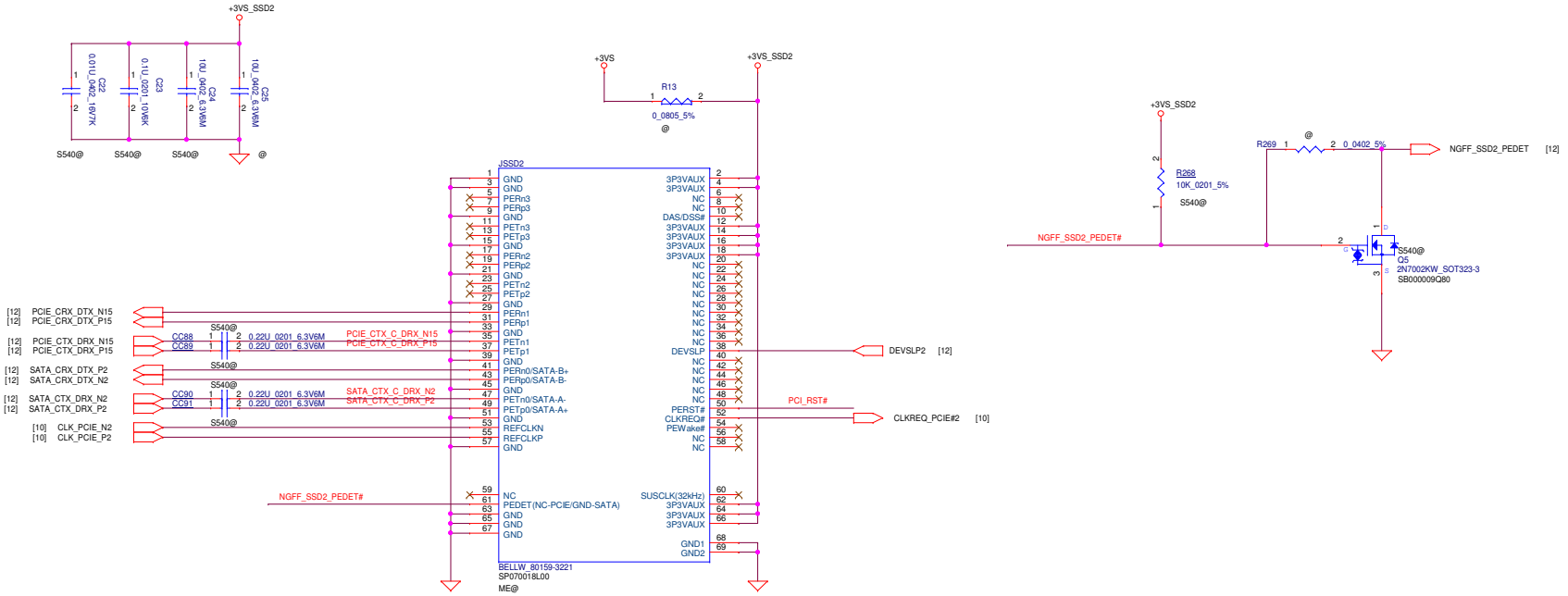
SSD(TYPE M)



NGFF_SSD_PEDET#
H : PCIE Interface
L : SATA Interface
Fellow 543016_SKL_U_Y_PDG_0_9

SSD(TYPE M)

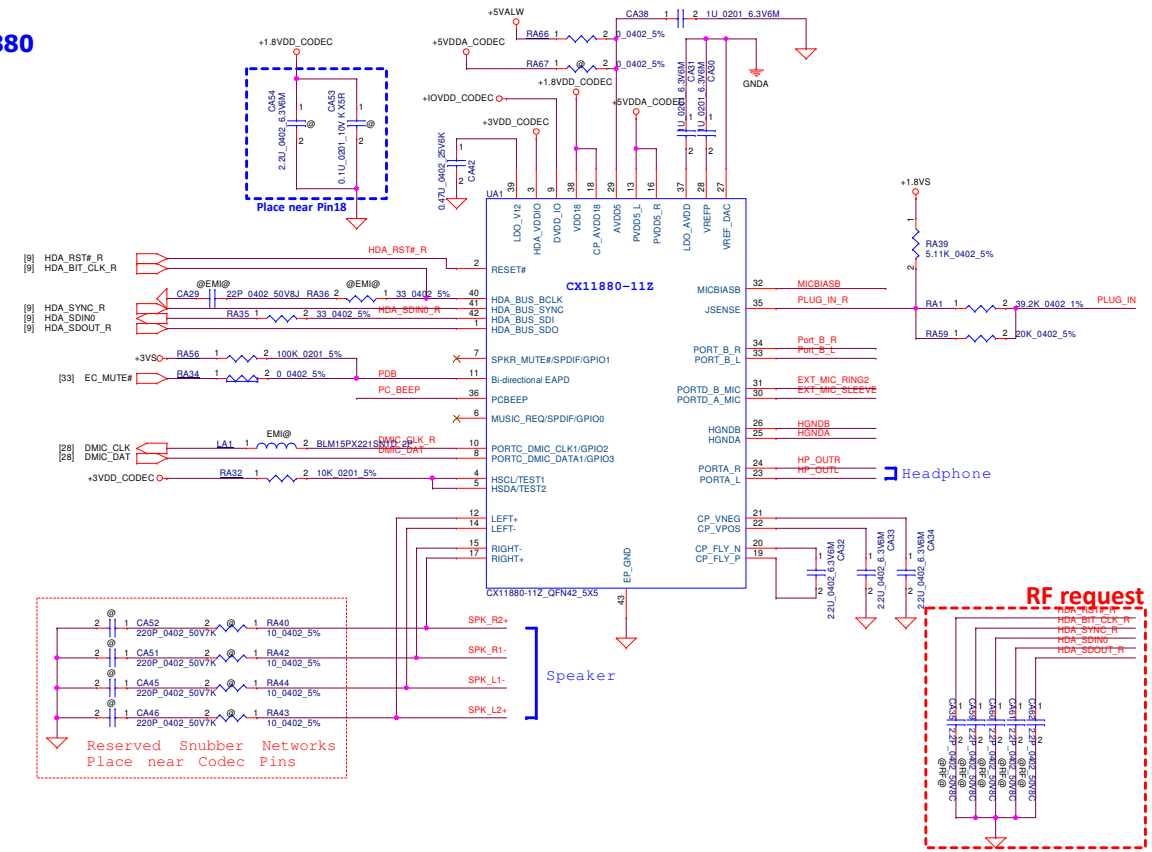


Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

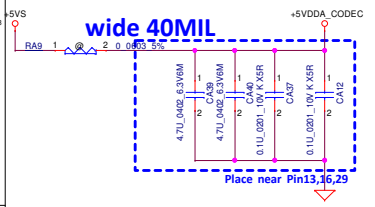
Title	SSD	
Size C	Document Number LA-H081P	Rev 0.2
Date: Monday, October 22, 2018	Sheet 31 of 53	

CX11880

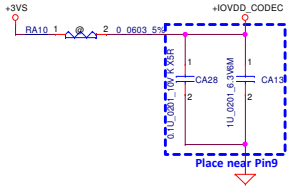


+5VS --> +5VDDA_CODEC

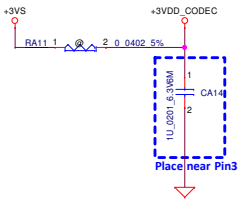
wide 40MIL



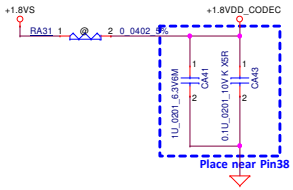
+3VS --> +IOVDD_CODEC



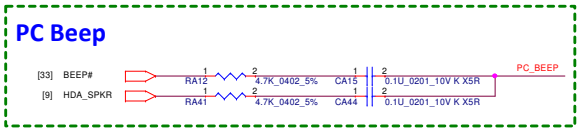
+3VS --> +3VDD_CODEC



+1.8VS --> +1.8VDD_CODEC



PC Beep



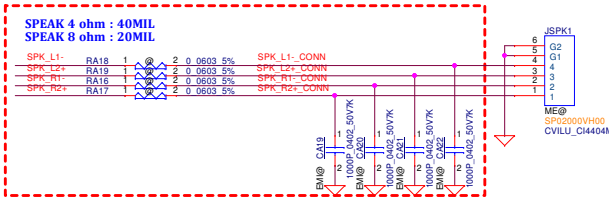
Speaker

Speaker Connector PN SP02000RR00

wide 40MIL

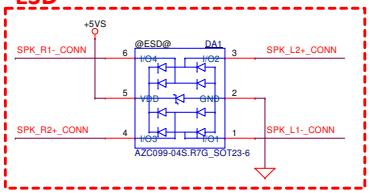
EMI

SPEAK 4 ohm : 40MIL
SPEAK 8 ohm : 20MIL

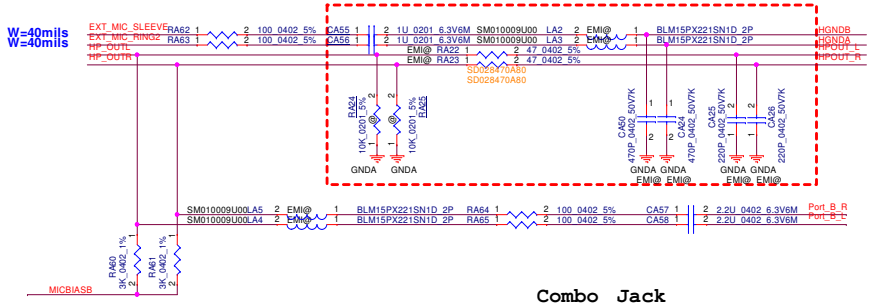


ESD protection needs to be placed near connector side

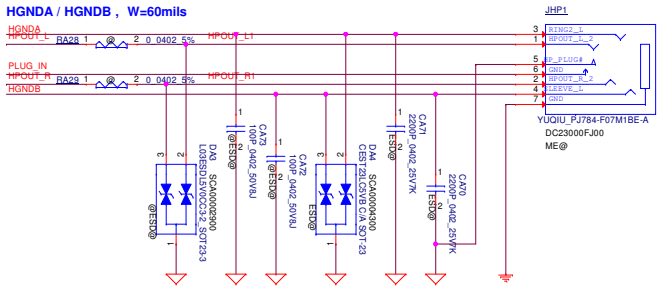
ESD



EMI



Combo Jack (Normal Open)



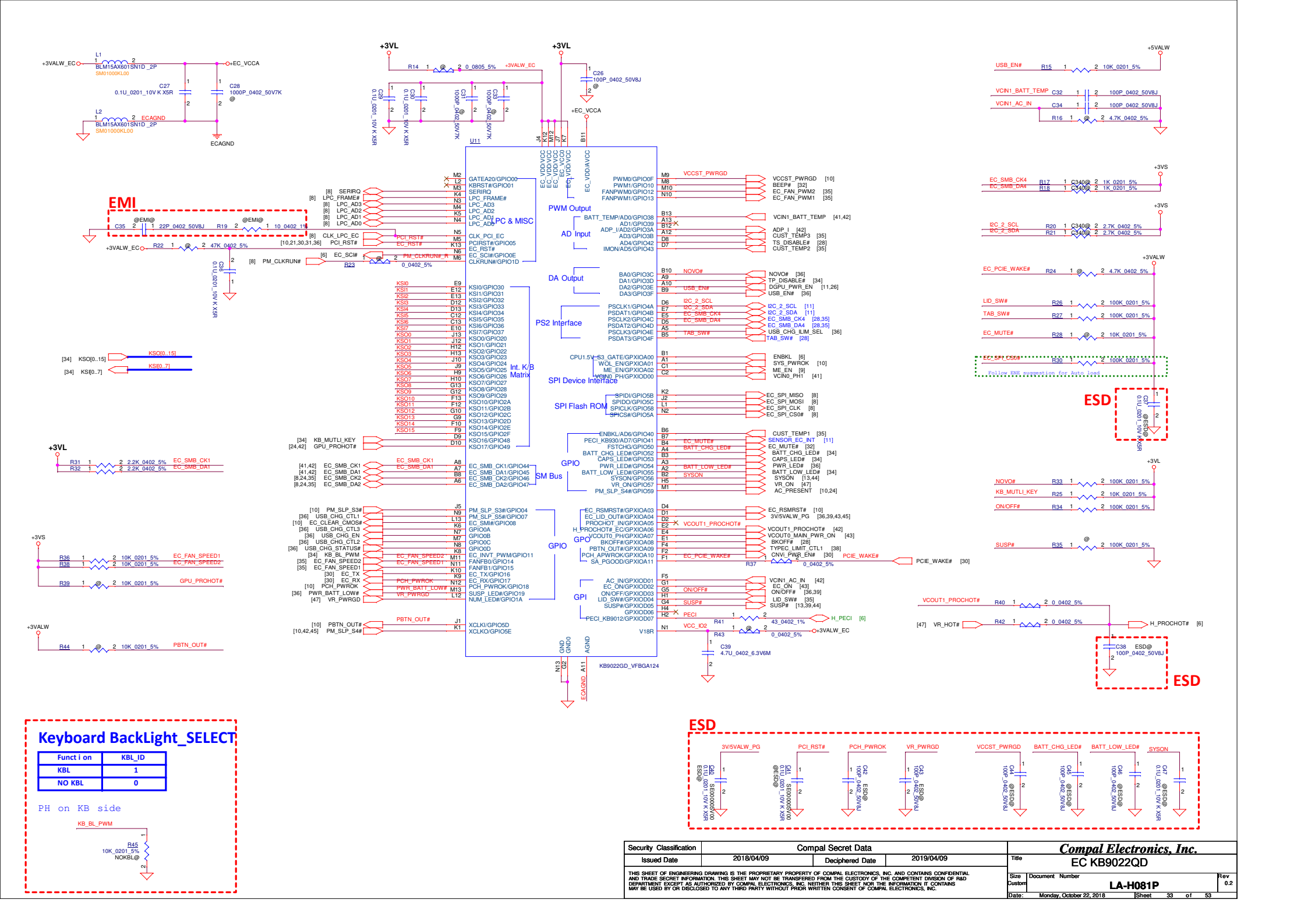
Security Classification	Compal Secret Data		
Issued Date	2018/05/04	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: HD Audio Codec_CX11880

Size	Document Number	Rev
Custom	LA-H081P	0.2

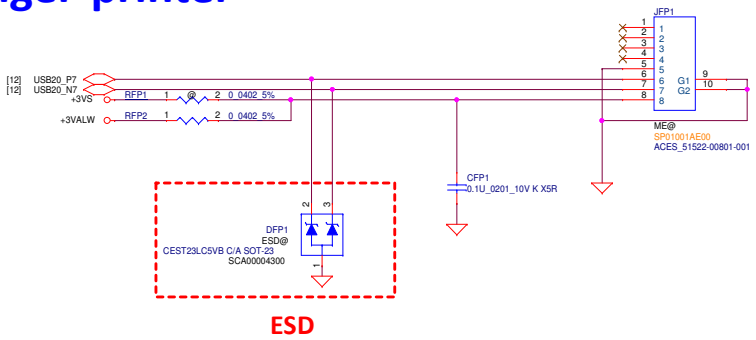
Date: Tuesday, October 23, 2018 | Sheet 32 of 53



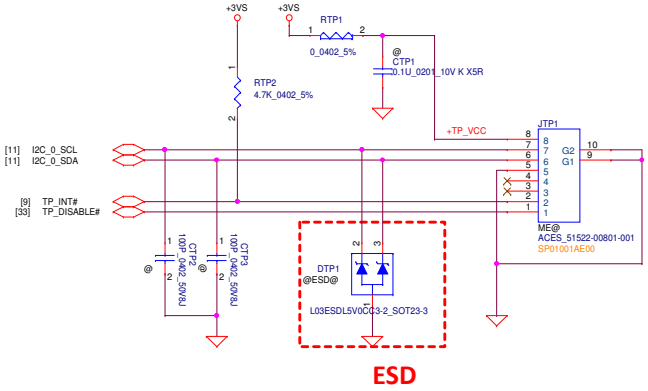
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.			
Title	EC KB9022QD		
Size: Custom	Document Number: LA-H081P		Rev: 0.2
Date: Monday, October 22, 2018	Sheet 33 of 53		

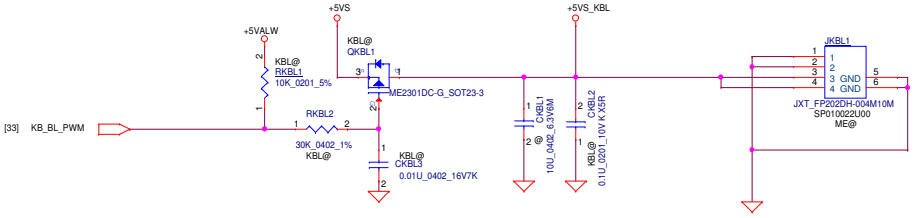
Finger printer



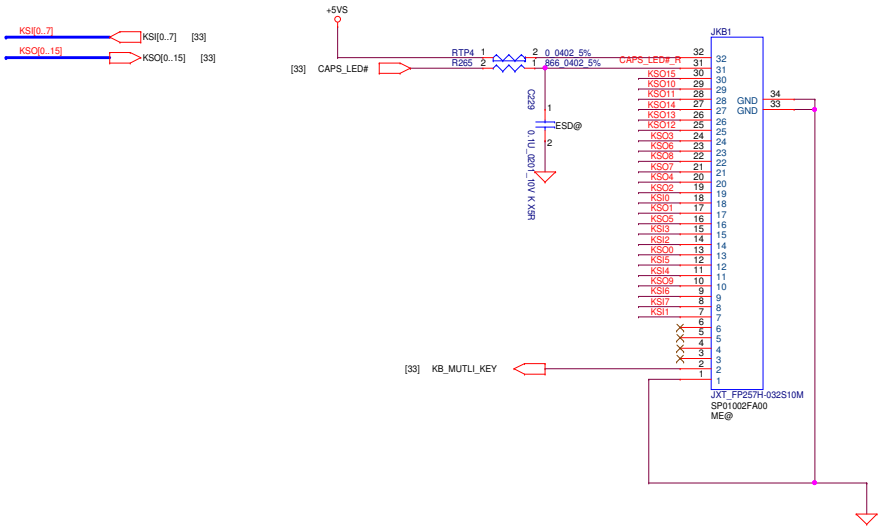
Touch Pad



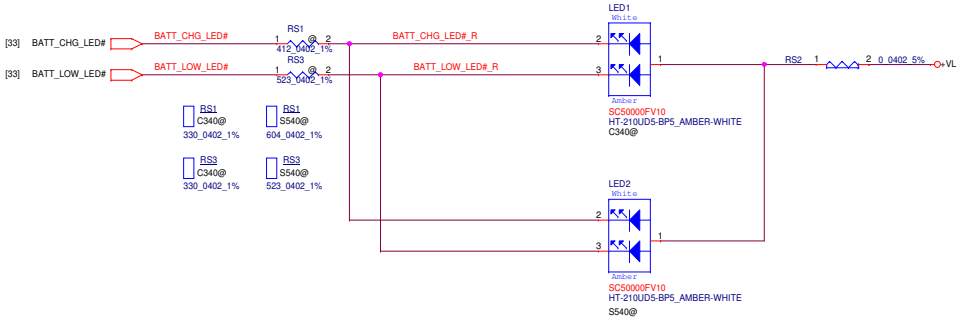
Keyboard Backlight



Keyboard



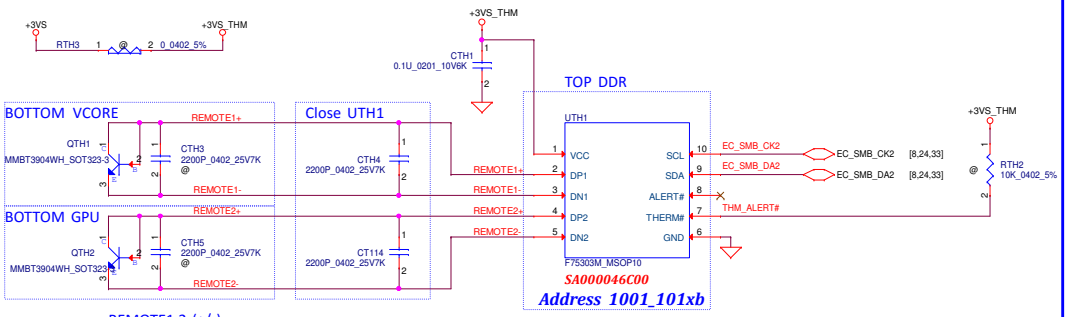
BATT LED



Security Classification	Compal Secret Data		
Issued Date	2017/5/3	Deciphered Date	2019/04/09

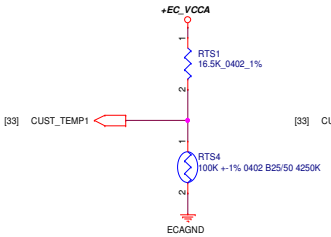
Compal Electronics, Inc.			
Title	KBL/KBD/LED/TP/HS Conn.		
Size C	Document Number LA-H081P		Rev 0.2
Date: Monday, October 22, 2018	Sheet 34 of 53		

THERMISTOR

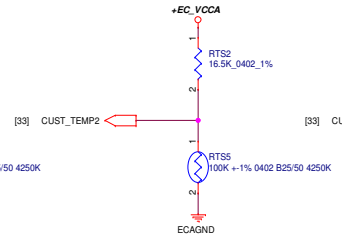


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

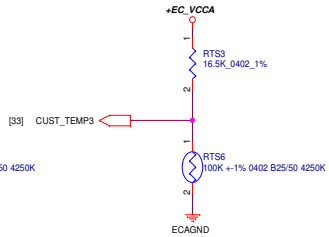
DDR4



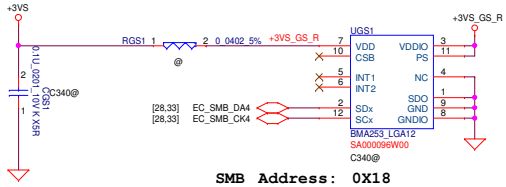
GPU_CHOKE



Charger CHOKE

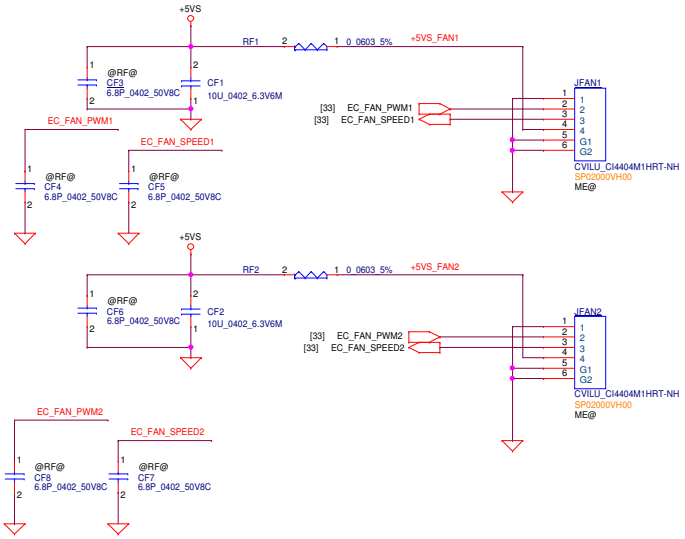


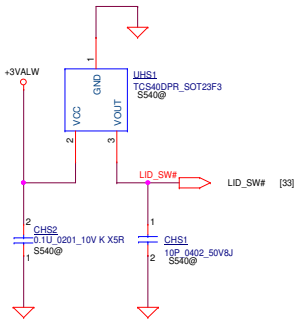
G-Sensor

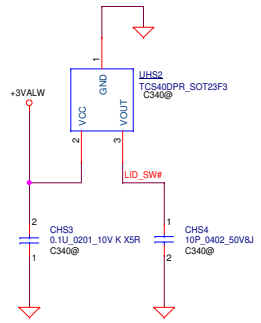


SMB Address: 0X18

FAN







Security Classification	Compal Secret Data		
Issued Date	2017/5/3	Deciphered Date	2019/04/09

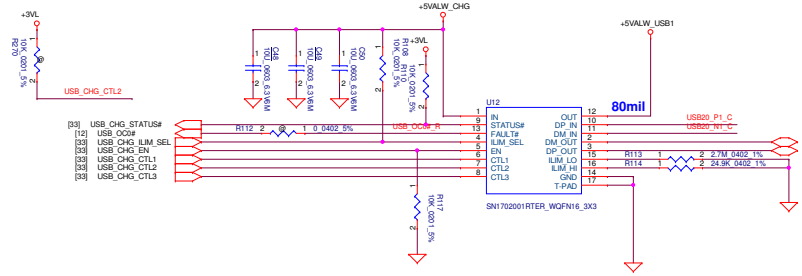
Compal Electronics, Inc.

Title: FAN / Thermal Senser

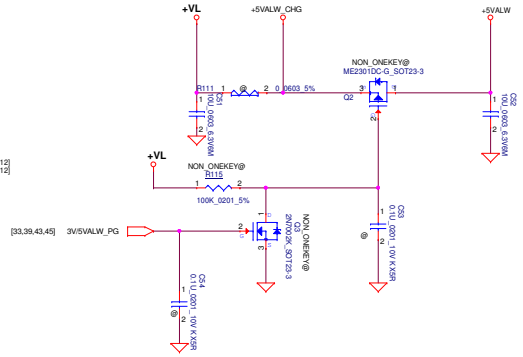
Size	Document Number	Rev
C	LA-H081P	0.2

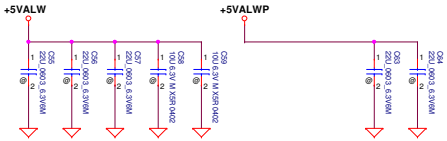
Date: Monday, October 22, 2018 Sheet 35 of 53

USB3.0_Port (AOU_Port)



USB Charge switch

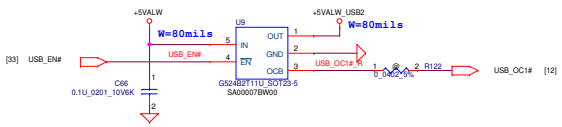




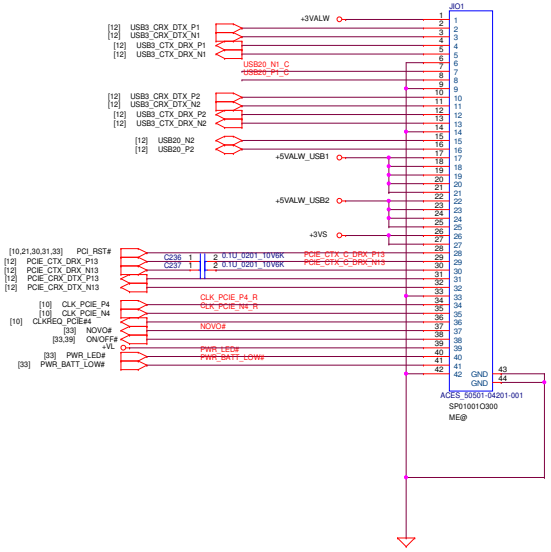
For USB Charger to improve +5VALWP power ripple

USB3.0_Port

2A/Active Low



I/O CONN



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/09	Deciphered Date 2019/04/09	Title IO board
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			Date: Monday, October 22, 2018 / Sheet 36 of 53

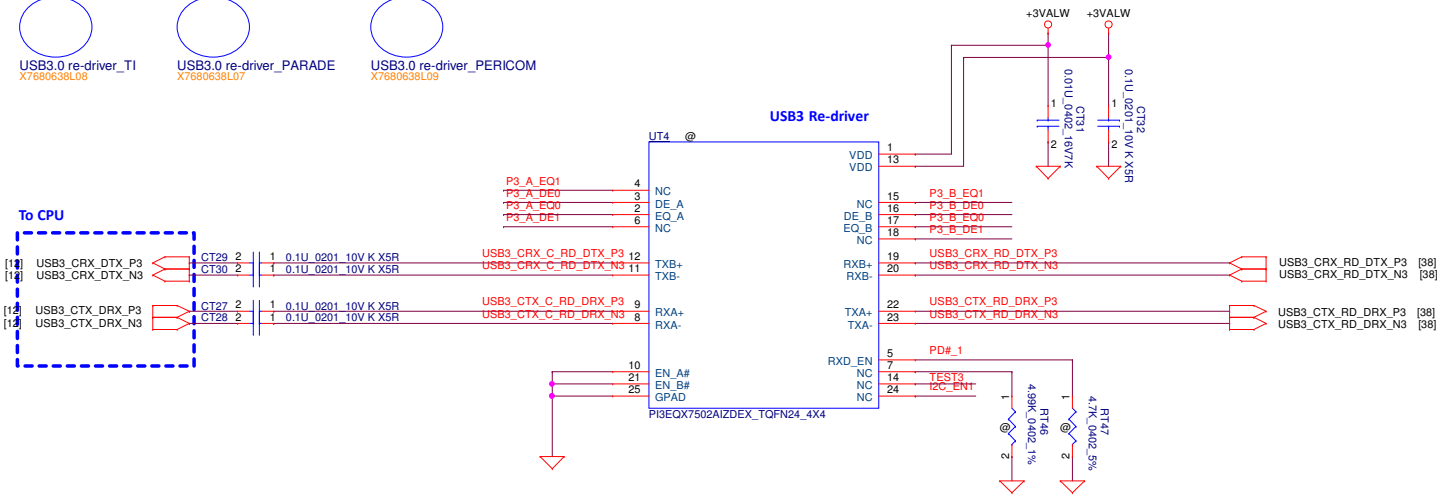
USB3.0_Port

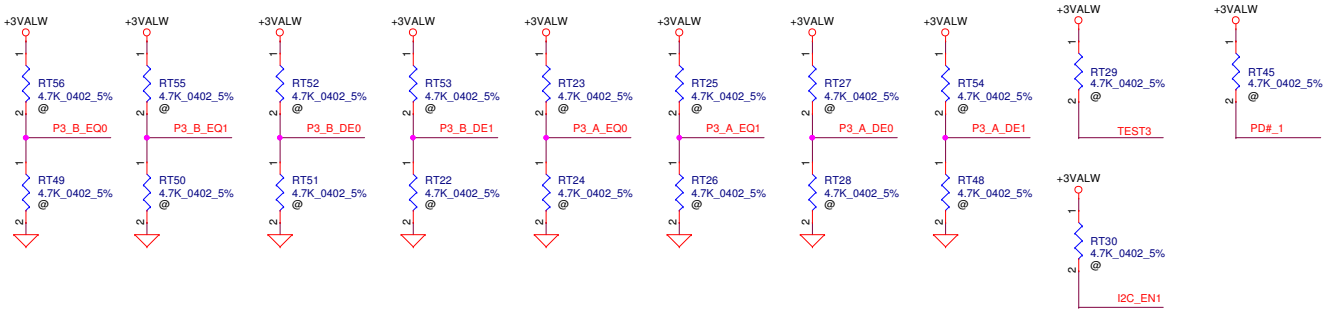
TI @	UT4 TI@ SN65LVPE502ARGER	RT48 TI@ 0_0402_5%	RT22 TI@ 0_0402_5%	RT49 TI@ 4.7K_0402_5%	RT50 TI@ 4.7K_0402_5%	RT51 TI@ 4.7K_0402_5%
PA@	UT4 PA@ PS8713BTQFN24GTR2-A2	RT25 PA@ 4.7K_0402_5%				
PE@	UT4 PE@ PI3EQX7502AIZDEX TQFN24	RT49 PE@ 4.7K_0402_5%	RT24 PE@ 4.7K_0402_5%	RT28 PE@ 4.7K_0402_5%		

ZZZ X76_TI@ — USB3.0 re-driver_TI — X76806638L08

ZZZ X76_PA@ — USB3.0 re-driver_PARADE — X76806638L07

ZZZ X76_PE@ — USB3.0 re-driver_PERICOM — X76806638L09

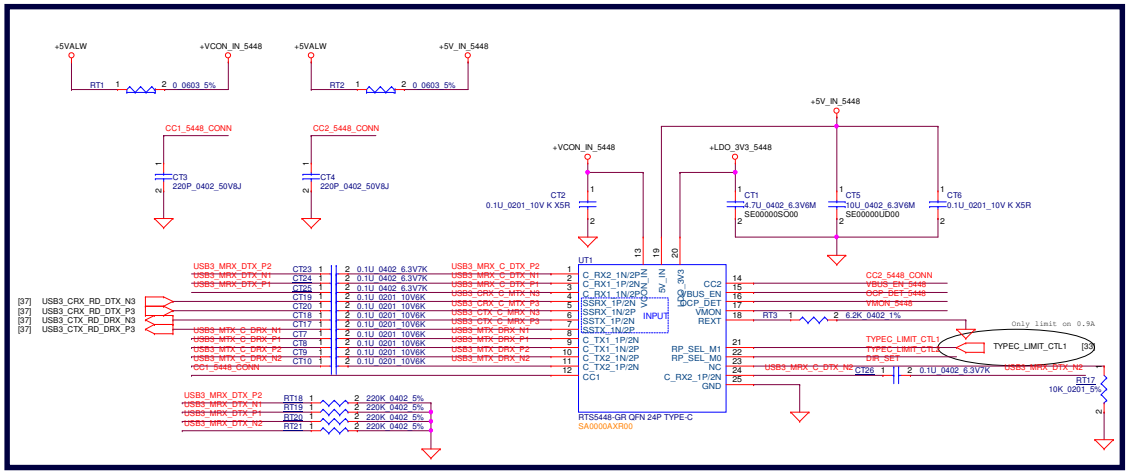




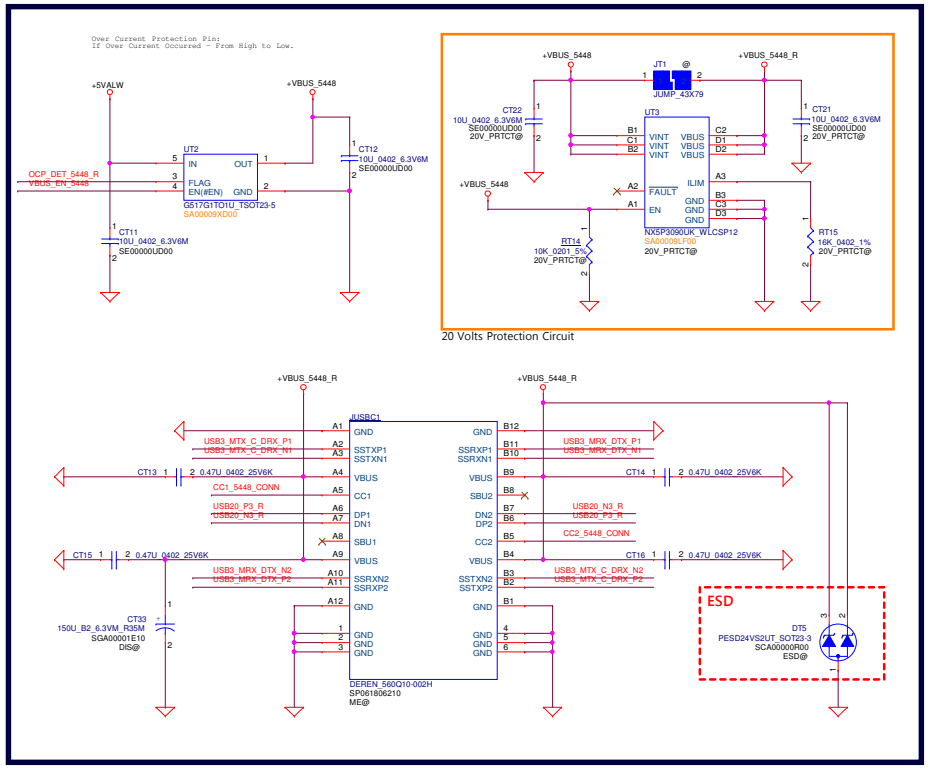
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Title	Type-C USB redriver		
Size: Custom	Document Number: LA-H081P		Rev: 0.2
Date: Monday, October 22, 2018	Sheet 37 of 53		

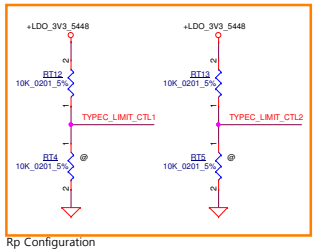
TYPE-C - CC+MUX (RTS5448-GR)



TYPE-C CONNECTOR

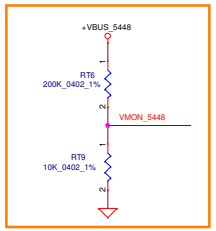


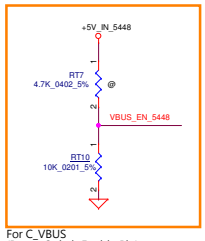
MUX MISC.



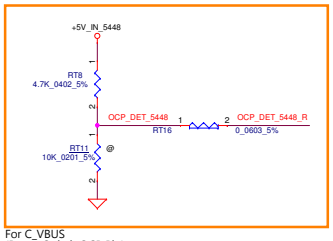
Rp Configuration

	M1	M0	Note
Rp:900mA	0	1	RT4/RT13 mount,RT12/RT5don't mount
Rp:1.5A	1	0	RT12/RT5 mount,RT4/RT13don't mount
Rp:3.0A	1	1	RT12/RT13mount,RT4/RT5 don't mount





For C_VBUS
(Power Switch Enable Pin)

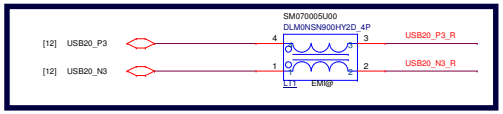


For C_VBUS
(Power Switch OCP Pin)

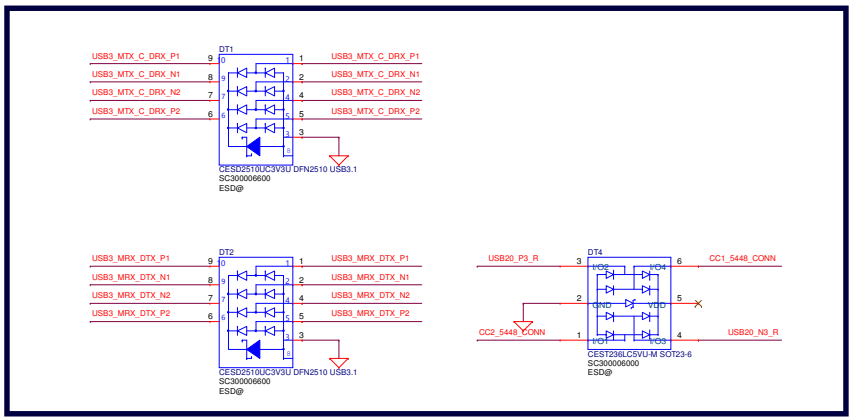
Power switch enable pin	Note
Low Active	RT7/RT10 mount
High Active	RT10 mount, RT7 don't mount

Power switch OCP pin	Note
Low Active	RT8/RT11 mount
High Active	RT11 mount, RT8 don't mount

USB2.0



ESD COMPONENTS



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: Type-C

Size: Custom | Document Number: LA-H081P | Rev: 0.2

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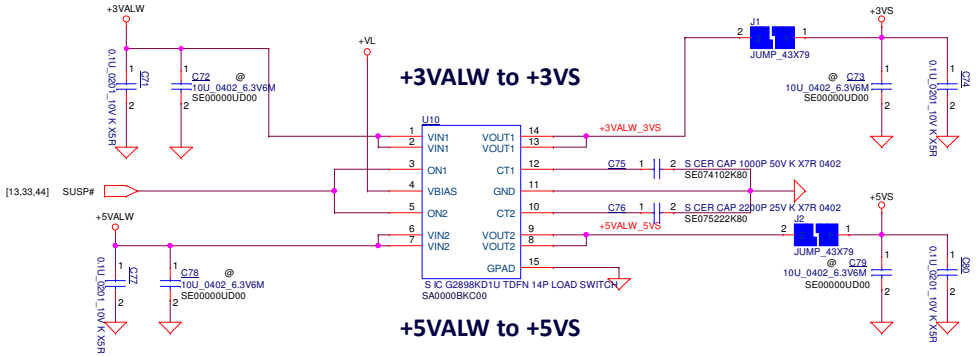
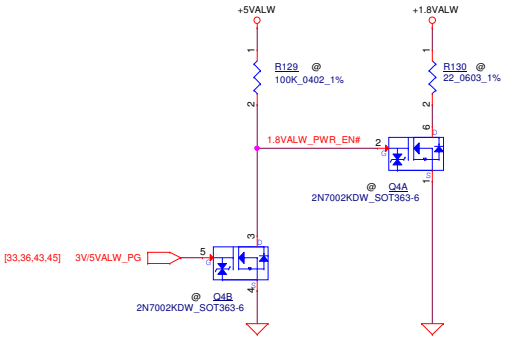
DC to DC

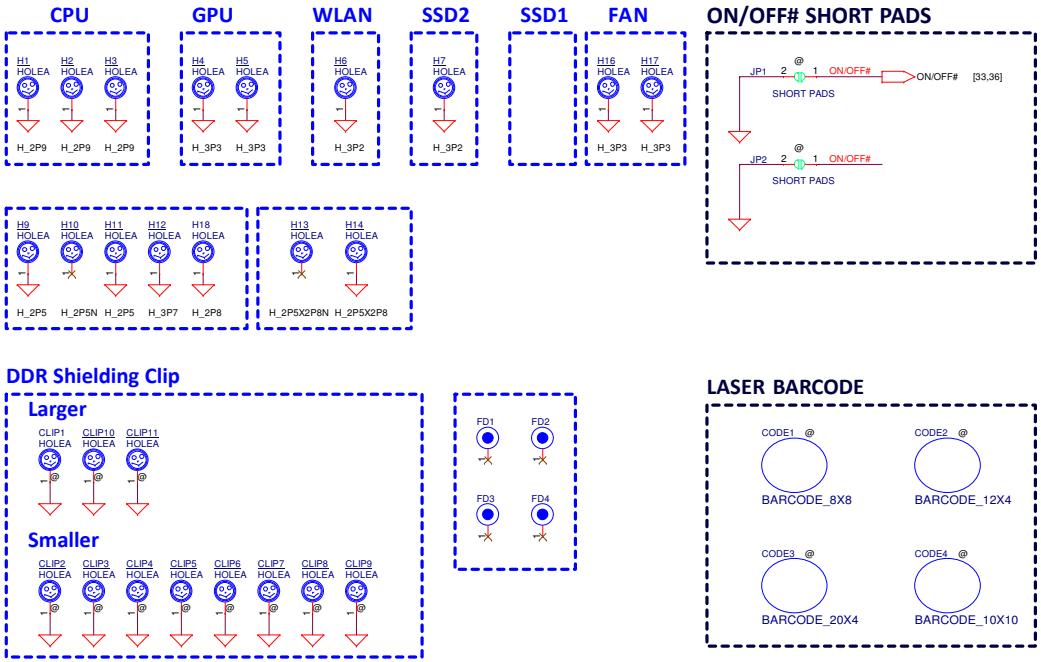


DISCHARGE CIRCUIT

For +1.8VALW Discharge



MISC.



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Compal Electronics, Inc.			
Title	DC to DC / Discharge / MISC		
Size	Document Number		Rev
Custom	LA-H081P		0.2
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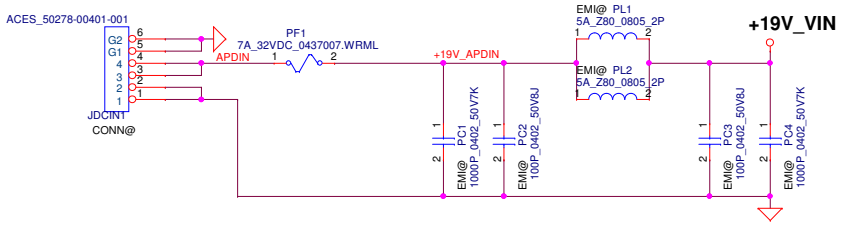
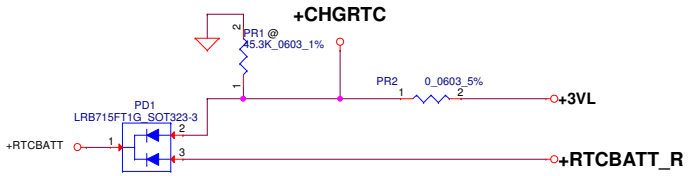




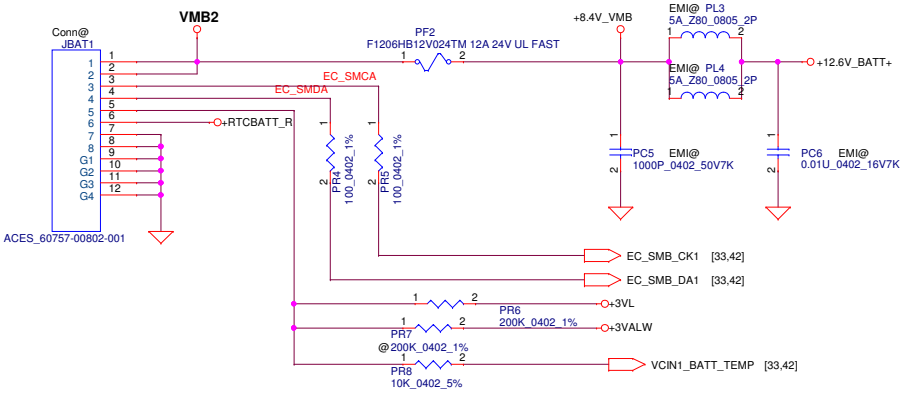
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

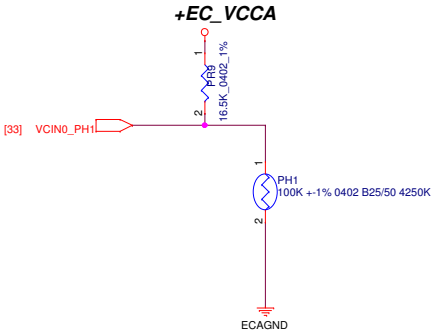
Title: **PWR- DCIN / Vin Detector**

Size	Document Number	Rev
Custom	KBL	0.1

Date: Monday, October 22, 2018 Sheet 40 of 53



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	KBL	0.1

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Module model information

ISL95520A_Hybrid_Boost_V2.mdd

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ314 L2N7002WT1G_SC70-3

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

+19V_VIN

PR301 1M_0402_1%
PR302 3M_0402_5%
PQ311 EMB04N03H_EDFN5X6-8-5

+19V_P1

PQ312 AON7506_DFN33-8-5

+19V_P2

PR303 0.01_1206_1%

@PJP301 JUMP_43X118

+19VB_CHG

PC301 10U_0603_25V6M
PC302 10U_0603_25V6M
@EM@ PC303 0.1U_0402_25V6
EM@ PC304 2200P_0402_25V7K

CSIP_CHG_R
CSIN_CHG_R
@ PR304 0_0402_5%
@ PR305 0_0402_5%
PC305 0.1U_0402_25V6

PR306 392K_0402_1%
ASGATE_CHG_R
PR307 4.02K_0402_1%
PR308 4.02K_0402_1%

PR729 and PR732 are ACDET set ting base on your project to set

PR309 100_0402_1%
+12.6V_BATT+

CMSRC_CHG
ASGATE_CHG
PC307 0.47U_0402_25V6K

PR310 49.9K_0402_1%
PC306 2200P_0402_50V7K

support Turbo boost : 2200P
no support Turbo boost : 0.1u

Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)

PC308 0.1U_0402_25V6

PQ313 AON7506_DFN33-8-5

Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)

PU301 ISL95520AHRZ-T_QFN32_4X4

PQ301 AON7408L_DFN8-5

7X7X3
Isat: 6.5A
DCR: 28mohm

PL301 4.7UH_5.5A_20%_7X7X3_M

+17.4V_BATT_CHG

PR315 0.01_1206_1%

+12.6V_BATT+

PC310 10U_0603_25V6M
PC311 10U_0603_25V6M
PC312 10U_0603_25V6M

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
==========
Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

Ipsys = KPSYS x (VADAP x IADAP + VBAT x IBAT)
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.
==========
adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

PR311 100K_0402_1%
PR314 158K_0402_1%

[33,42] VCIN1_AC_IN
[33,41] EC_SMB_DA1
[33,41] EC_SMB_CK1
[33,42] VCOUT1_PROCHOT#
[33] ADP_I

ACIN_CHG

@PR312 0_0402_5%
@PR320 0_0402_5%
@PR316 0_0402_5%
PR318 1K_0402_1%
PR321 1K_0402_1%
AMON_ISL95520
BMON_ISL95520

Close to EC.

PC316 0.1U_0402_25V6
PC317 0.1U_0402_25V6
Close to EC.

Follow adapter and battery wattage in Vsys current source.
Base on CPU Core VR design.
The resistor is pop on CPU VR schematic.

ACIN
ACOK
SDA
SCL
PROCHOT#
AMON
BMON
PSYS

BST_CHG
UG_CHG
LX_CHG
LG_CHG
VDDP_CHG
VDD_CHG
DCIN
NTC

PR313 0_0603_5%
BST_CHG_R
PC309 0.47U_0402_25V6K

PR319 4.7_0402_5%
PC313 1U_0402_16V6K
PC314 1U_0402_16V6K
PQ302 AON7506_DFN3X3-8-5
PR317 4.7_1206_5%
RF@ PC315 680P_0402_50V7K

PR323 100K_0402_1%
PR324 10_1206_5%
PD301 LRB715FT1G_SOT323-3
VF = 0.38V
PC318 1U_0603_25V6

+19V_VIN
BA

A31 connect to BA
Other team connect to bat t conn

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

PQ315 LMUN5113T1G_SOT323-3
[10,39,45] PM_SLP_S4#
PQ316 LTC015EUBFS8TL_UMT3F

For A31 only.
Turn off Charger IC on battery only.
Depend on customer design for system power consumption.

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. OX3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : OX3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : OX3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

VDD=5V
VDD_CHG
PR326 200K_0402_1%
PR327 200K_0402_1%
PR334 76.8K_0402_1%
PR335 348K_0402_1%

CCLIM_CHG
ACLIM_CHG
PROG_CHG
COMP_CHG
FSET_CHG
PR325 10K_0402_1%

Fs=729KHZ ~ +/- 15%

CSOP_CHG
PR328 2_0402_5%
CSOP_CHG_R
PC319 0.1U_0402_25V6
CSON_CHG
CSON_CHG_R
@PR332 0_0402_5%

PR329 150K_0402_1%
PC320 560P_0402_50V7K
PR330 100_0402_1%
PR331 38.3K_0402_1%
PC321 0.033U_0402_25V7K

Hybrid boost power mode
Cell = 4s

VCIN1_BATT_TEMP [33,41]
BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC_LIM = VccLIM / 64 x Rs2
==========
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ)
CC_LIM = VccLIM / 32 x Rs2
==========
AC_LIM = Vac_LIM / 32 x Rs1

Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

+3VS
Pull high on HW side

VGA@ PR1681 10K_0402_5%
VGA@ PR1680 10K_0402_5%
VGA@ PQ1660A
GPU_PROHOT# [24,33]
2N7002KDW_SOT363-6

[33,42] VCOUT1_PROCHOT#
VGA@ PQ1661 SSM3K35MFV 1N VESM

VGA@ PQ1660B
[33,42] VCIN1_AC_IN
2N7002KDW_SOT363-6

Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

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Compal Electronics, Inc.

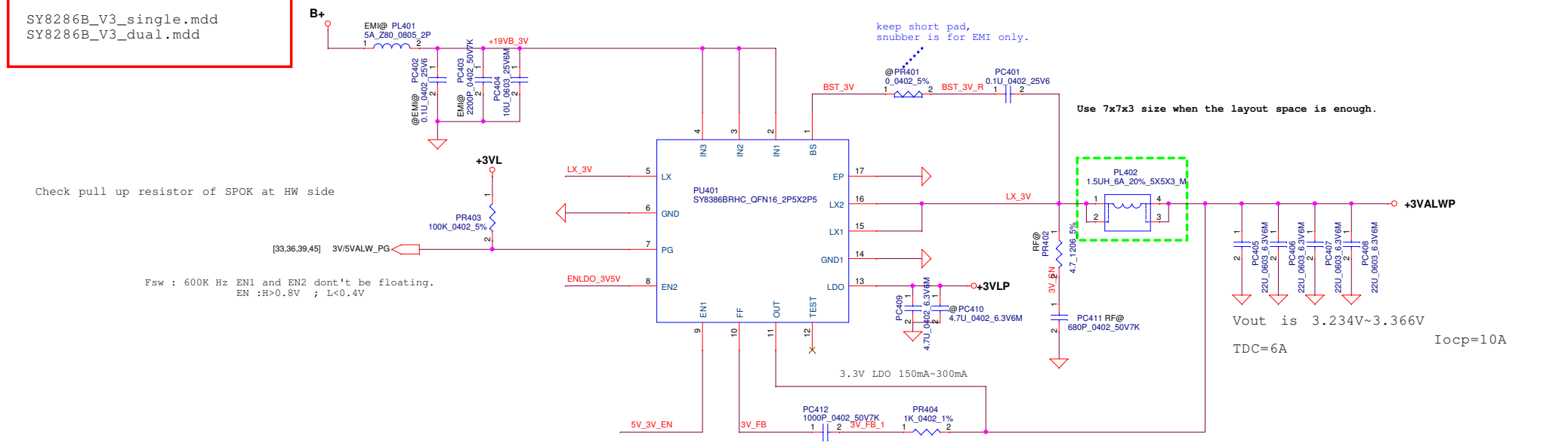
Title: PWR_CHARGER

Size | Document Number | Rev 0.1

Date: Monday, October 22, 2018 | Sheet 42 of 53

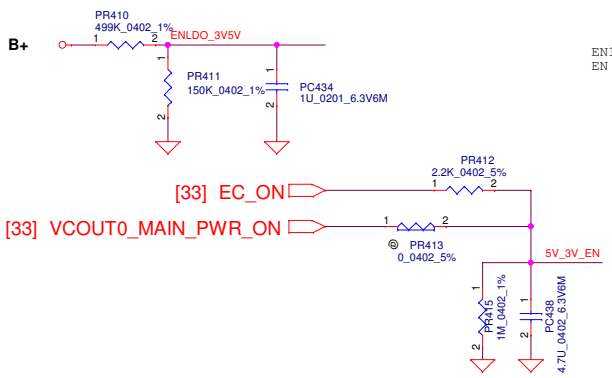
Module model information

SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd



Module model information

SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom		0.1

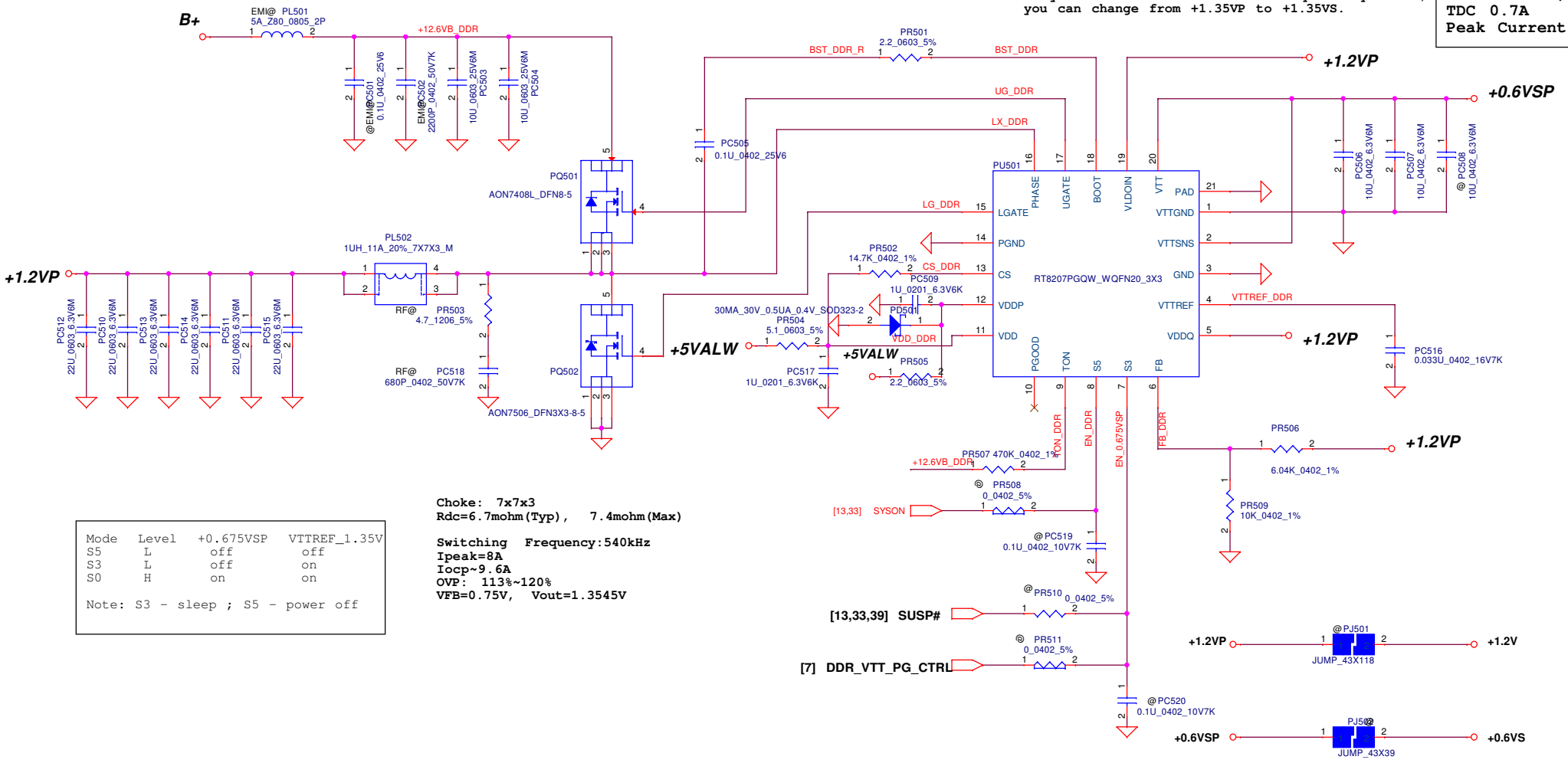
Date: Monday, October 22, 2018 | Sheet 43 of 53

Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp~9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

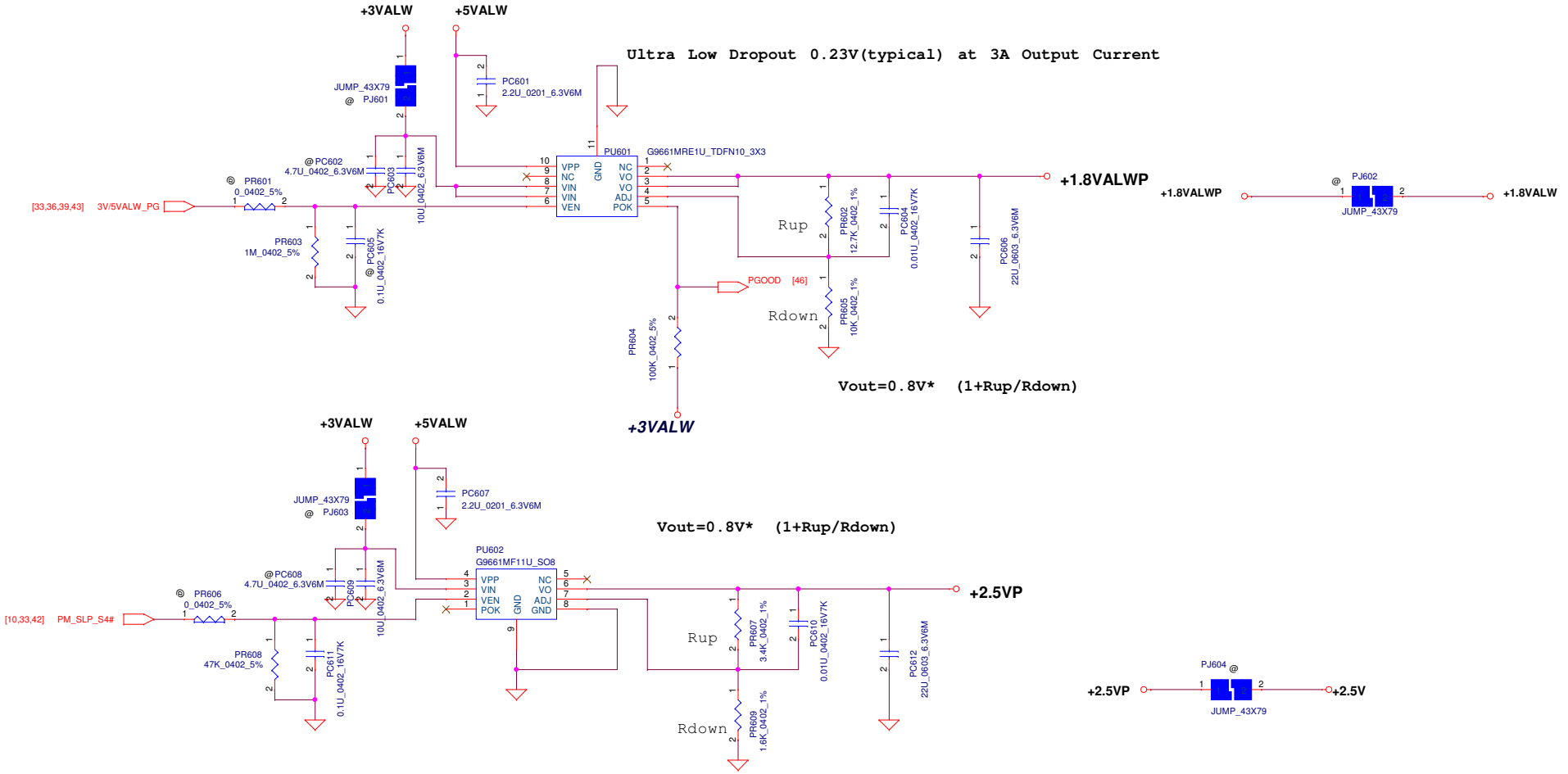
Title: RT8207P

Size: Custom | Document Number | Rev 0.1

Date: Monday, October 22, 2018 | Sheet 44 of 53

Module model information

APL5930_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

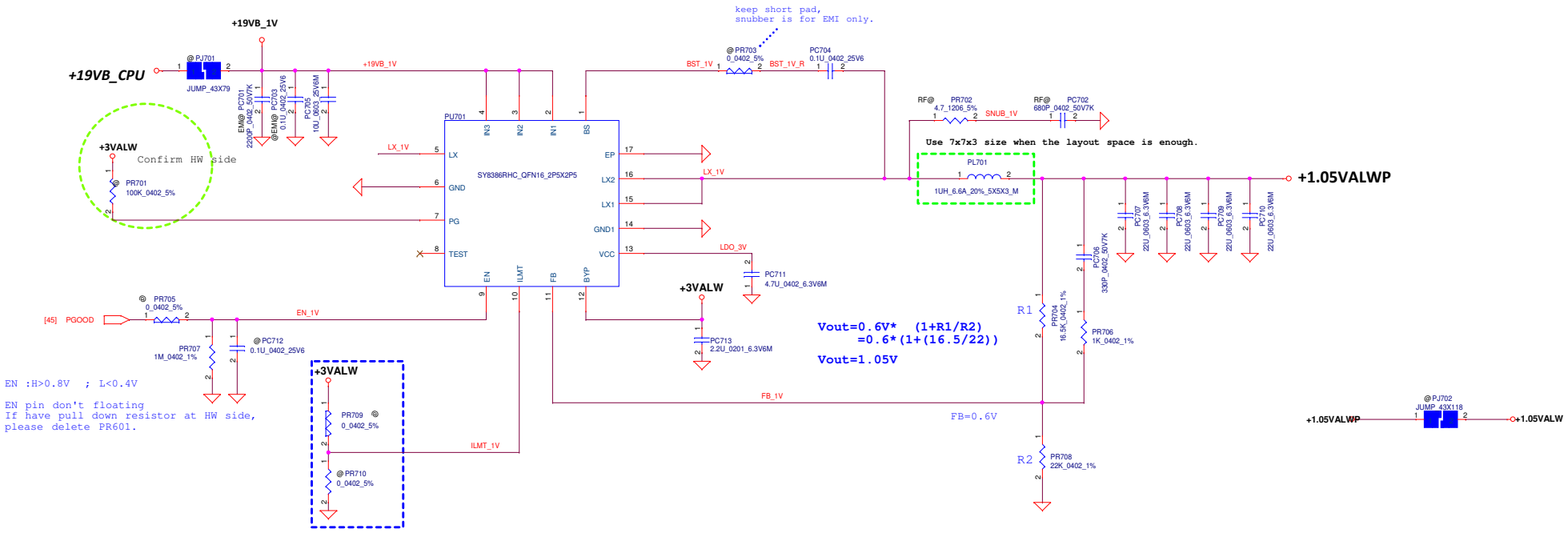
Title: APL5930

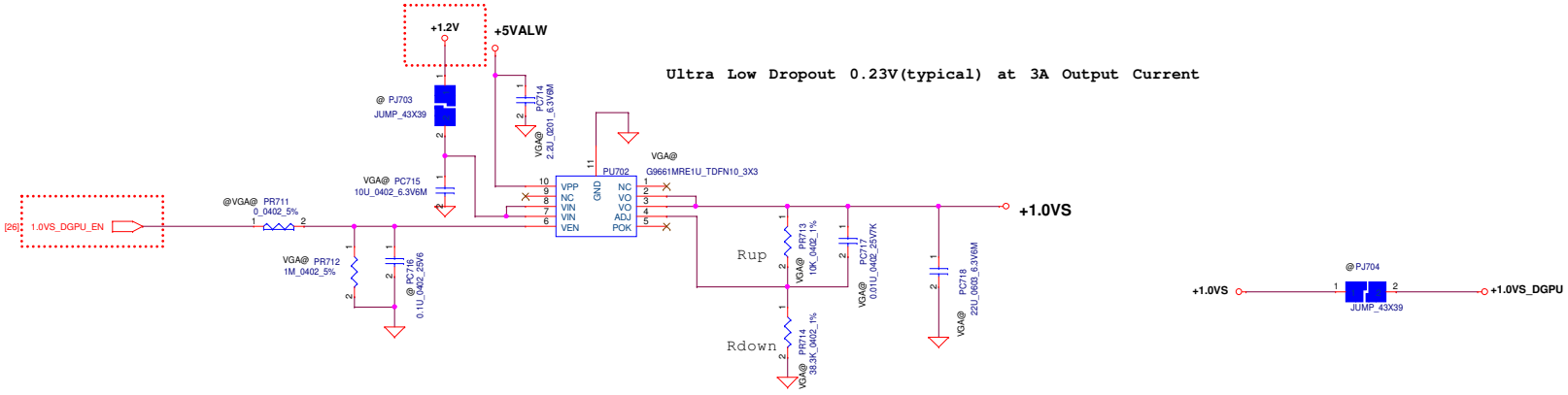
Size: Custom | Document Number: KBL | Rev: 0.1

Date: Monday, October 22, 2018 | Sheet 45 of 53

Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd





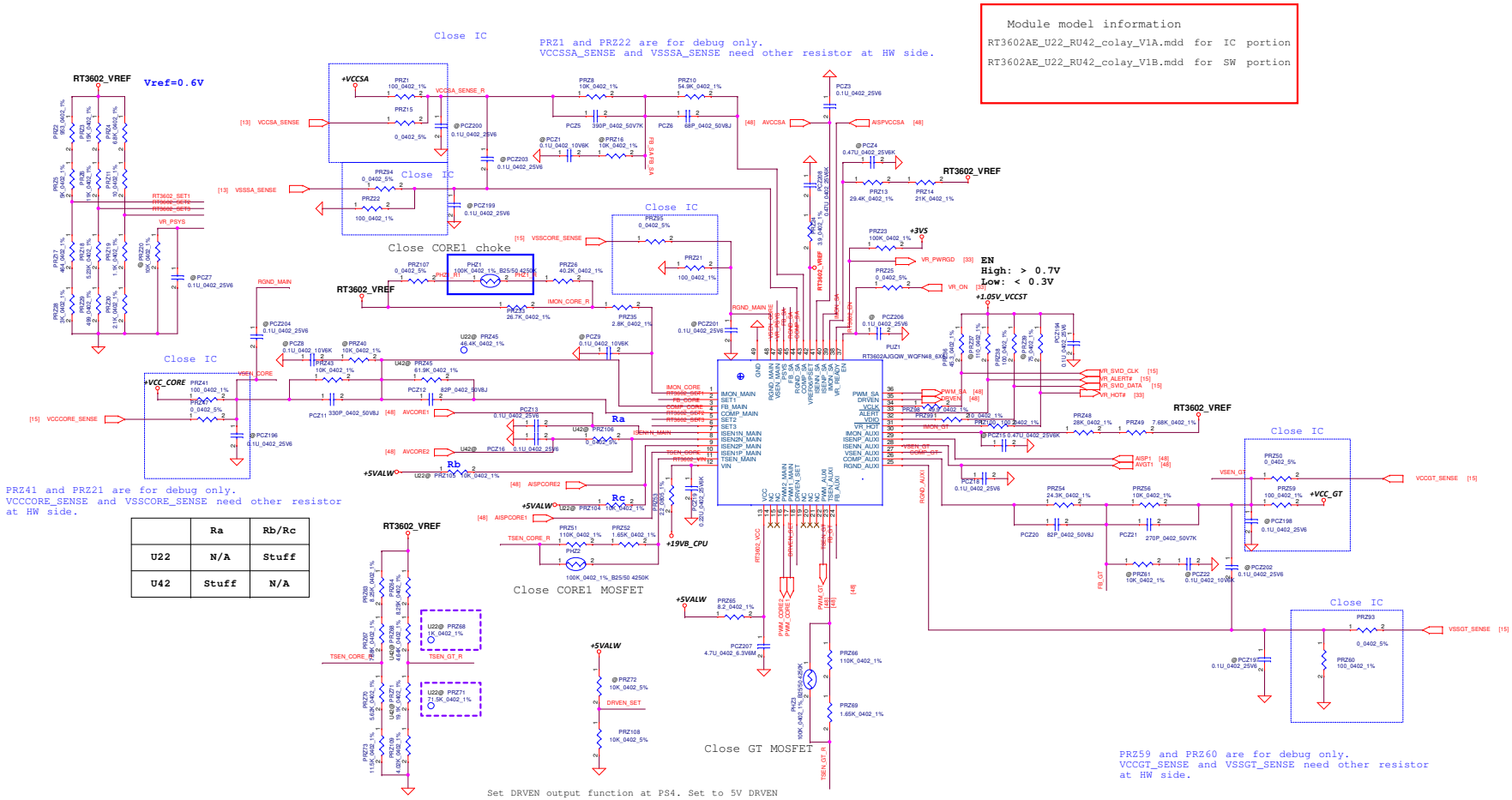
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: SY8286

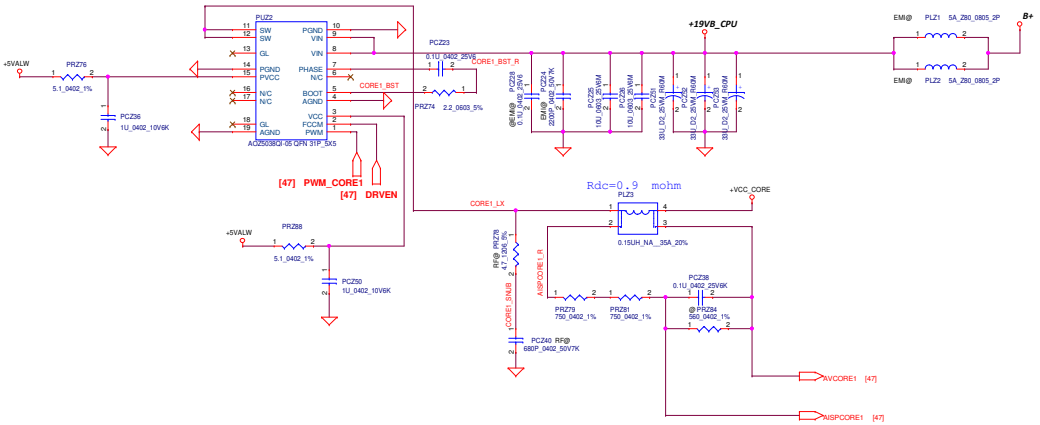
Size: C | Document Number | Rev: 0.1

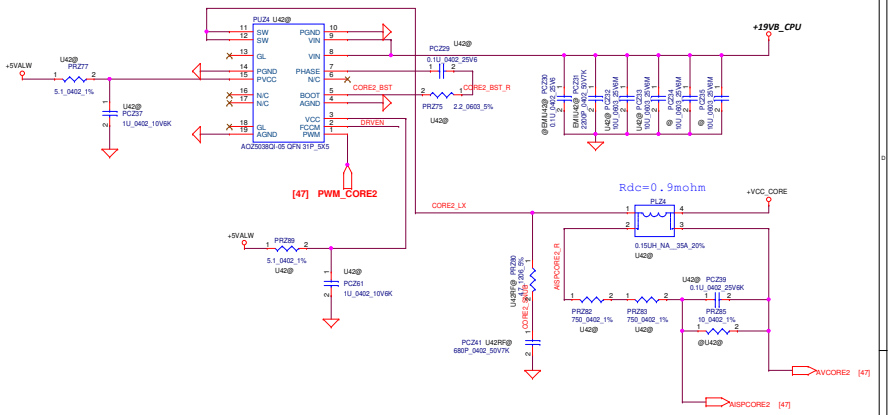
Date: Monday, October 22, 2018 | Sheet 46 of 53



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

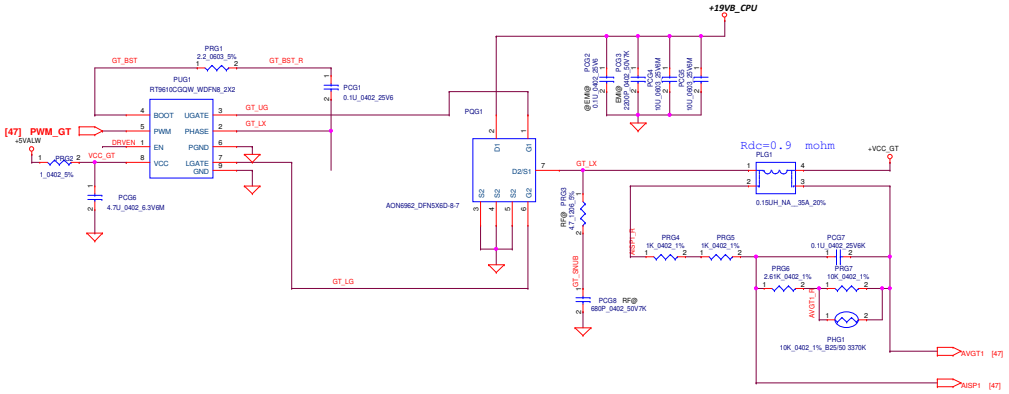
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	CPU_CORE		
Size	Document Number		Rev 0.2
Date: Monday, October 22, 2018	Sheet 47 of 53		





H/S AON6280:
R DS(ON) (at V GS =10V) < 6.8m
R DS(ON) (at V GS =4.5V) < 10.5m

L/S AON6214:
R DS(ON) (at V GS =10V) < 2.8m?
R DS(ON) (at V GS =4.5V) < 3.5m?



VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.9 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.9 mohm +/- 5%

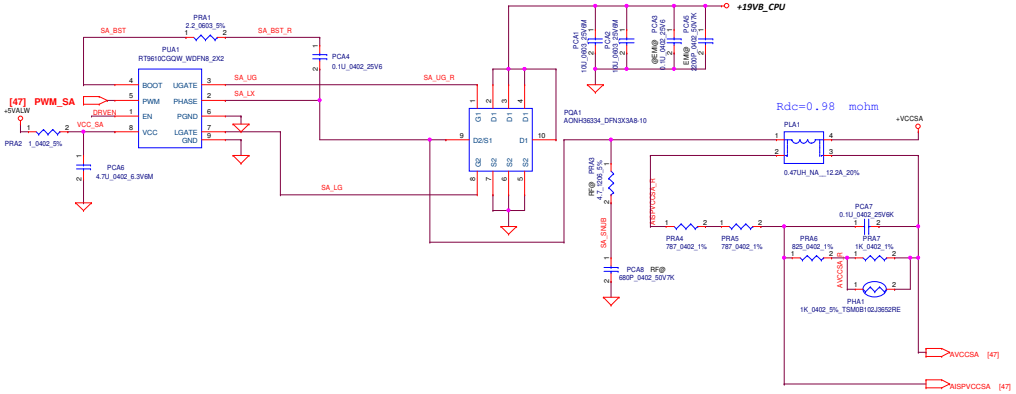
U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A

U42
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: *CPU Power stage*

Size	Document Number	Rev
		0.1

Date: Monday, October 22, 2018 Sheet 48 of 53

2017/06/06
VCORE Output Capacitor:
U42
22uF_0603*41
1uF_0201*35
330uF *2
UNPOP
22_0603*1

Security Classification	Compal Secret Data		
Issued Date	2018/10/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	EH5AW M/B LA-G521P	0.1

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R1, R2, R3, R4, R5, C are based on VGA type to set.

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

OpenVReg Configurations:(PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V
2 phase with DEM	1.08V to 1.35V
2 phase with CCM	1.6V to 5.5V

Module model information:
RT8816A-2P_NVVDDS_V2A.mdd for IC portion
RT8816A-2P_NVVDDS_V2B.mdd for SW portion

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

PSI pull up on HW side
+1.8VGS_+3VGS_AON

Remark:
1. Switching frequency setting:(Ton pin)
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2e)
=352Khz

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) * 12) / Icoset

High: >1.2V
Low: <0.55V

N16S-GTR
+VGA_CORE
EDP-Continuous 26.5A
EDP-Peak 53A
OCP min 63.6A

N17S-G1
+VGA_CORE
EDP-Continuous 29.7A
EDP-Peak 59.2A
OCP min 71.1A

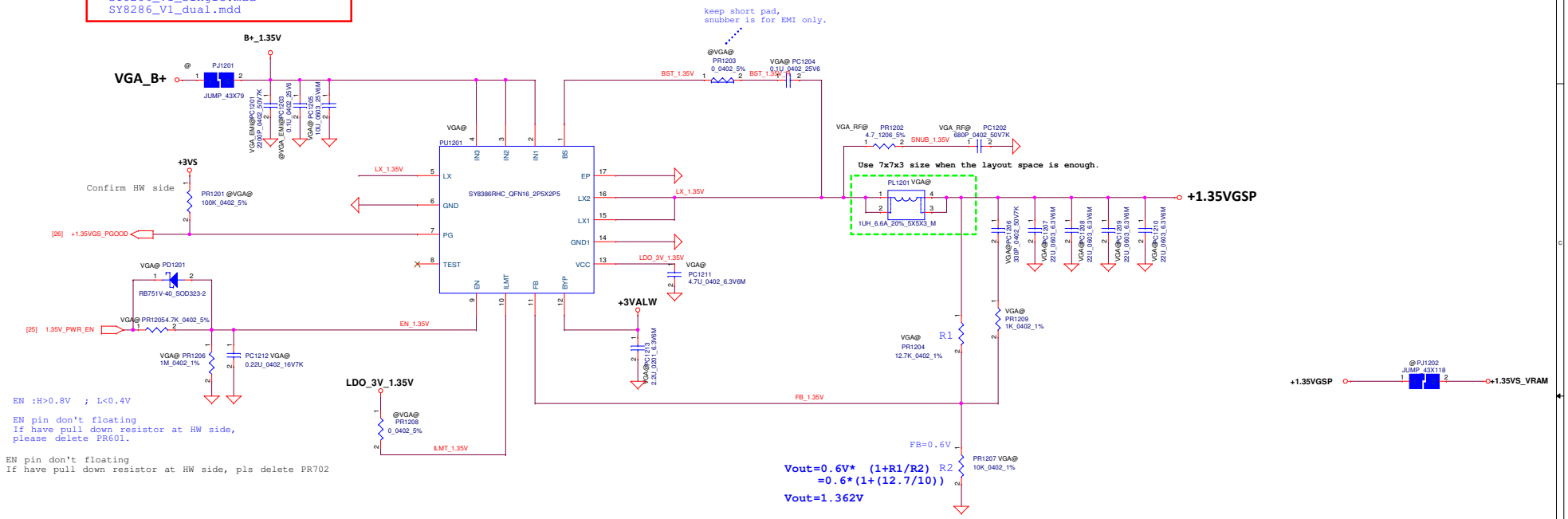
Near GPU Core
Under GPU Core
GB4-128 package

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.
Title: VGA_CORE
Size: Custom | Document Number: VGA_CORE | Rev: 0.1
Date: Monday, October 22, 2018 | Sheet 50 of 53

Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd



Security Classification	Compal Secret Data		
Issued Date	2016/6/2	Deciphered Date	2017/6/2

Compal Electronics, Inc.	
Title	VRAM-SY8286RAC
Size: Custom	Document Number: ISL62771 Module
Rev: 0.1	
Date: Monday, October 22, 2018	Sheet 51 of 53

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	To avoid shortage issue and fix BOM error		Add PR407(SD028000080,S RES 1/16W 0 +-5% 0402) Change PQ1661 PN from SB000012900 to SB000011Z00	2018/07/31	EVT
2	Modify BOM for X1 code		Change PQ314 from SB00000ST00 to SB000009Q80	2018/08/10	DVT
3	Modify BOM for X1 code		Change PC315,PC411,PC702,PC1202 from 680P_0603_50V7K to 680P_0402_50V7K	2018/08/10	DVT
4	Modify Vin detector setting for 4 cell battery		Change PR306 from 287K_0402_1% to 392K_0402_1%	2018/08/16	DVT
5	Change Battery connector P/N		Change JBATT1 to ACES 60757-00802-001	2018/08/16	DVT
6	Change +3VALWP IC solution		Change PU401 from SY8286BRAC to SY8386BRHC	2018/08/16	DVT
7	Change +1.05VALWP & +1.35VGSP IC solution		Add PR1209(SD034100180,S RES 1/16W 1K +-1% 0402) Change PU701 & PU1201 from SY8286RAC to SY8386RHC	2018/08/16	DVT
8	Charger IC Vendor suggestion		Change PR330 from 349_0402_1% to 100_0402_1% Change PC321 from 0.015U_0402_25V7K to 0.033U_0402_25V7K Change PR333 from 182K_0402_1% to 150K_0402_1%	2018/08/27	DVT
9	Follow cost down action		Change PC9120,PC9126,PC9127,PC9129 from 0.47U_0201_4V6M to 0.47U_0201_6.3V6K	2018/08/27	DVT
10	Change PQ311 P/N		Change PQ311 P/N from SB00001IL00 to SB00001C500	2018/08/27	DVT
11	Charger IC Vendor suggestion		PC307 & PC309 change from SE000005Z80(S CER CAP 0.22U 25V K X7R 0603) to SE00000WA00(S CER CAP 0.47U 25V K X5R 0402)	2018/08/27	DVT
12	Follow cost down action		PCZ19 change from SE000013J00(S CER CAP 0.22U 25V K X6S 0402) to SE000015W00(S CER CAP 0.22U 25V K X5R 0402)	2018/08/27	DVT
13	Follow cost down action		PCZ3,PCZ13,PCZ16 change from SE074104K80(S CER CAP 0.1U 50V K X7R 0402) to SE00000G880(S CER CAP 0.1U 25V K X5R 0402)	2018/08/27	DVT
14	Follow cost down action		PC505 , PC1204 change from SE00000W210(S CER CAP 0.1U 25V K X7R 0402) to SE00000G880(S CER CAP 0.1U 25V K X5R 0402)	2018/08/27	DVT
15	Fine tune for U42 CPU transent test result		Add PC9103, PC9187 ,PC9188 ,PC9189(22U_0603_6.3V6M)	2018/08/29	DVT
16	Follow HW request		Change PR826 from 100K to 10K	2018/08/29	DVT
17	Fine tune for U42 CPU transent test result		Change PRZ35 from 4.22K to 2.8K Change PCZ11 from 150p to 330p Change PRZ67 from 115 to 7.68K Change PRZ70 from 549K to 5.62K Change PRZ68 from 374 to 4.64K Change PRZ71 from 182K to 19.1K Change PRZ48 from 30K to 28K Change PRZ54 from 22.1K to 24.3K	2018/08/30	DVT
18	Fine tune for U22 CPU transent test result		Delete PC9101,PC9166,PC9167,PC9168,PC9169,PC9170,PC9171,PC9068,PC9080, PC9002,PC9003,PC9027,PC9034 for U22 CPU SKU	2018/09/05	DVT
19	To avoid RTC loos issue		Delete PR1(45.3K_0603_1%) Change PR2 from 1.5K_0603_1% to 0_0603_5%	2018/09/06	DVT
20	0 ohm change to short pad		Change PR304,PR305,PR332,PR407,PR413,PR508,PR511,PR709, PR601, PR606,PR705, PR711,PR803 to short pad	2018/10/11	PVT

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: Z_BDW | Rev: 0.1

Date: Monday, October 22, 2018 | Sheet 52 of 53

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Audio Vendor request for hum noise issue		Reserved +5VALW for AVDD5 (pin29)	2018/10/17	PVT

Compal Electronics, Inc.

Title: **EE (PWR)**

Size	Document Number	Rev
Custom	LA-H081P	0.3

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