LCFC Confidential

Dooku/Jinn 2.0

E490S/E490/R490/E590/R590

NM-911 Rev0.4 Schematic

Intel Whiskey Processor with DDR4 + PCH

R17M-P1-50

R17M-P1-70

2018-09-21 Rev0.4

Security Classification	LC Future Center Secret Data		
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Title: COVER PAGE

Size	Document Number	Rev
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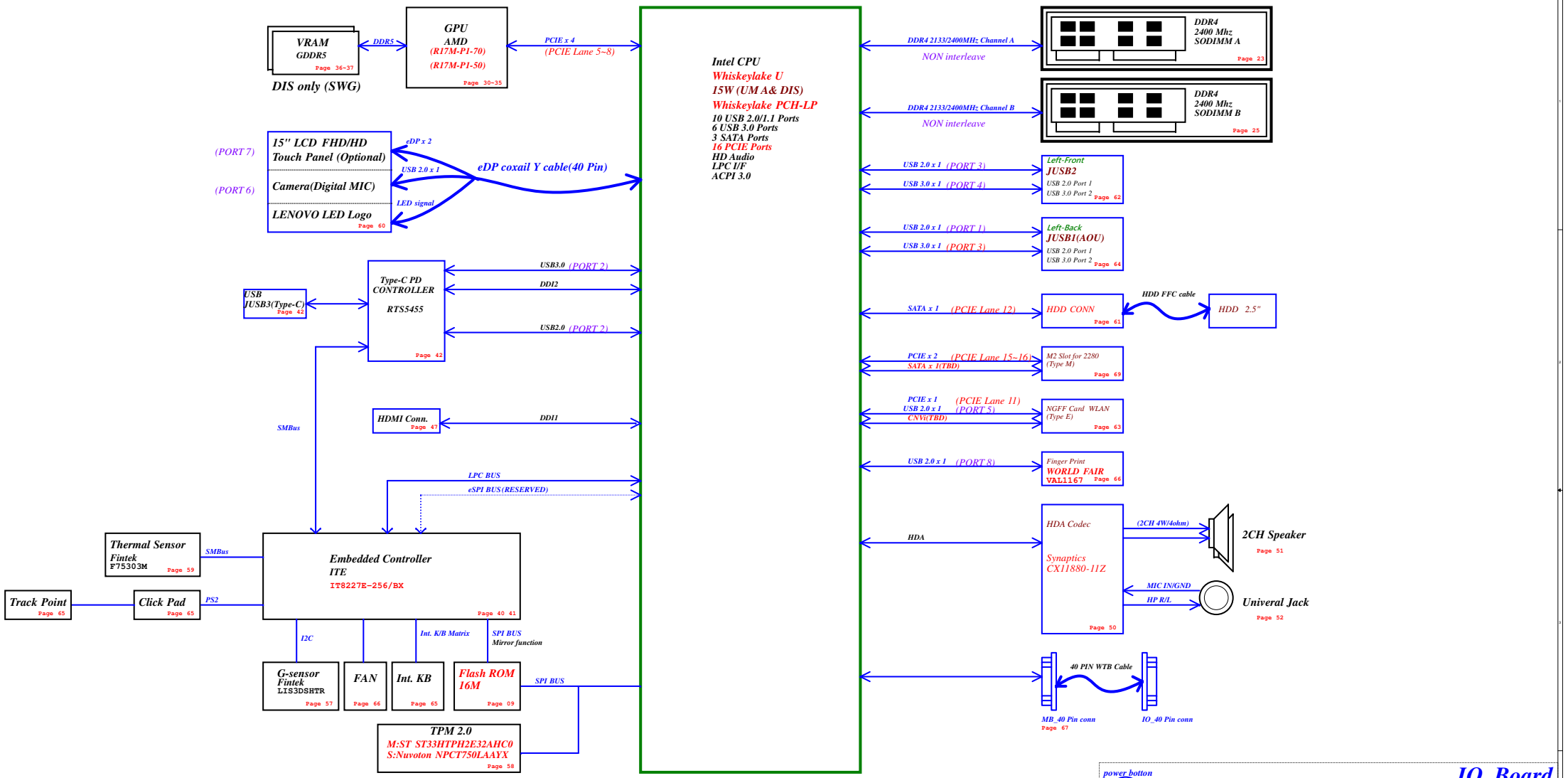

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: BZ490/500 MB-B011 | Rev: 0.4

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Voltage Rails

O --> Means ON
X --> Means OFF

Power Plane / State	B+	+1.05VALW +3VALW +1.8VALW +5VALW	+1.2V +0.6VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

	SIGNAL						
STATE	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	V +3VALW	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	V +3VS	X	V +5VS	V +3VS	X
PCH_SML0_CLK PCH_SML0_DATA	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW

HSIO Port

Port	Device
1	PCIE (Card Reader)
2	Type-C Port
3	Type-A Port Gen1 (AOU)
4	Type-A Port Gen2 (DCI)
5	PCIE (GPU)
6	PCIE (GPU)
7	PCIE (GPU)
8	PCIE (GPU)
9	PCIE (LAN)
10	N/A
11	PCIE (WLAN)
12	SATA express (SATA)
13	N/A
14	N/A
15	M.2 (PCIE)
16	M.2 (SATA)

USB2.0 Port

Port	Device
1	Type-A Port Gen1 (AOU)
2	Type-C Port
3	Type-A Port Gen2 (DCI)
4	USB port (Sub Board)
5	BT
6	Camera
7	Touch Panel
8	Finger Printer
9	N/A
10	N/A

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Title: SYSTEM LIST

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BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function with WWAN
DIS@	Discreate SKU
UMA@	UMA SKU
DPRE@	With DP re-driver
NODPRE@	Bypass DP re-driver
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
MIRROR@	For mirror function
TPM@	TPM function
X76@	GPU VRAM Setting
XDP@	XDP function
EXO@	EXO function
ME@	ME Connector
EMC@	For EMC function
EMC_NS@	For EMC function (no mount)
RF@	For RF function
RF_NS@	For RF function (no mount)
WHL@	For WHL SKU
CNL@	For CNL SKU
SW@/AUDIO@	For Audio Jack Debug Selection
14S@	To recognize 14S SKU
CD@	Reduce capacitors quantity

Title: BOM LIST

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+3VS <9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

+VCC_IO <11,18,21,71>

+3VALW_PCH <8,9,10,11,12,13,15,19>

Change to 2K for 15m test

R0502	2K_0402_5%	DDIP1_CTRLCLK	
R0503	2K_0402_5%	DDIP1_CTRLDATA	
R0504	2.2K_0201_1%	DDIP2_CTRLCLK	
R0505	2.2K_0402_5%	DDIP2_CTRLDATA	

DDIP1_HPD	R0506	@	100K_0402_5%
DDIP2_HPD	R0507		100K_0201_1%
CPU_EDP_HPD	R0508		100K_0402_5%
ENBKL	R0509		100K_0201_1%

DP port	Enable	Disable
DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ± 5% resistor	no connect
DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ± 5% resistor	no connect

UC1A

HDMI

<47>	CPU_DDI1_N2	CPU_DDI1_N2	AL5 DDI1_TXN_0
<47>	CPU_DDI1_P2	CPU_DDI1_P2	AL6 DDI1_TXP_0
<47>	CPU_DDI1_N1	CPU_DDI1_N1	AJ5 DDI1_TXN_1
<47>	CPU_DDI1_P1	CPU_DDI1_P1	AJ6 DDI1_TXP_1
<47>	CPU_DDI1_N0	CPU_DDI1_N0	AF6 DDI1_TXN_2
<47>	CPU_DDI1_P0	CPU_DDI1_P0	AF5 DDI1_TXP_2
<47>	CPU_DDI1_N3	CPU_DDI1_N3	AE5 DDI1_TXN_3
<47>	CPU_DDI1_P3	CPU_DDI1_P3	AE6 DDI1_TXP_3

USB TYPE C

<42>	CPU_DDI2_N0	CPU_DDI2_N0	AC4 DDI2_TXN_0
<42>	CPU_DDI2_P0	CPU_DDI2_P0	AC3 DDI2_TXP_0
<42>	CPU_DDI2_N1	CPU_DDI2_N1	AC1 DDI2_TXN_1
<42>	CPU_DDI2_P1	CPU_DDI2_P1	AC2 DDI2_TXP_1
<42>	CPU_DDI2_N2	CPU_DDI2_N2	AE4 DDI2_TXN_2
<42>	CPU_DDI2_P2	CPU_DDI2_P2	AE3 DDI2_TXP_2
<42>	CPU_DDI2_N3	CPU_DDI2_N3	AE1 DDI2_TXN_3
<42>	CPU_DDI2_P3	CPU_DDI2_P3	AE2 DDI2_TXP_3

EDP_TXN_0	AG4	CPU_EDP_TX0-	CPU_EDP_TX0- <60>
EDP_TXP_0	AG3	CPU_EDP_TX0+	CPU_EDP_TX0+ <60>
EDP_TXN_1	AG2	CPU_EDP_TX1-	CPU_EDP_TX1- <60>
EDP_TXP_1	AG1	CPU_EDP_TX1+	CPU_EDP_TX1+ <60>
EDP_TXN_2	AJ4		
EDP_TXP_2	AJ3		
EDP_TXN_3	AJ2		
EDP_TXP_3	AJ1		

EDP_AUX_N	AH4	CPU_EDP_AUX#	CPU_EDP_AUX# <60>
EDP_AUX_P	AH3	CPU_EDP_AUX	CPU_EDP_AUX <60>
DISP_UTILS	AM7		
DDI1_AUX_N	AC7		
DDI1_AUX_P	AC6		
DDI2_AUX_N	AD4	DDIP2_AUXN	DDIP2_AUXN <42>
DDI2_AUX_P	AD3	DDIP2_AUXP	DDIP2_AUXP <42>
DDI3_AUX_N	AG7		
DDI3_AUX_P	AG6		

GPP_E13/DDPB_HPD0/DISP_MISC0	CN6	DDIP1_HPD	DDIP1_HPD <47>
GPP_E14/DDPC_HPD1/DISP_MISC1	CM6	DDIP2_HPD	DDIP2_HPD <42>
GPP_E15/DPPD_HPD2/DISP_MISC2	CP7		
GPP_E16/DPPE_HPD3/DISP_MISC3	CP6		
GPP_E17/EDP_HPD/DISP_MISC4	CM7	CPU_EDP_HPD	CPU_EDP_HPD <60>

HDMI
USB TYPE C

EDP_BKLTEN	CK11	ENBKL	ENBKL <40>
EDP_VDDEN	CG11	PCH_ENVDD	PCH_ENVDD <60>
EDP_BKLTCTL	CH11	PCH_EDP_PWM	PCH_EDP_PWM <60>

+VCC_IO — R0501 24.9_0402_1% — EDP_COMP AM6 DISP_RCOMP

HDMI

<47>	DDIP1_CTRLCLK	DDIP1_CTRLCLK	CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
<47>	DDIP1_CTRLDATA	DDIP1_CTRLDATA	CC9 GPP_E19/DPPB_CTRLDATA
		DDIP2_CTRLCLK	CH4 GPP_E20/DPPC_CTRLCLK
		DDIP2_CTRLDATA	CH3 GPP_E21/DPPC_CTRLDATA
			CP4 GPP_E22/DPPD_CTRLCLK
			CN4 GPP_E23/DPPD_CTRLDATA
			CR26 GPP_H16/DDPF_CTRLCLK
		GPP_H17	CP26 GPP_H17/DDPF_CTRLDATA

WHISKEYLAKE-U_BGA1528
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@

eDP_RCOMP
Trace Width: 5 mils
Isolation Spacing: 25 mils
Resistor Value: 24.9 or 100 ohm 1%
Max Length: 600 mils

Pull-up to VCCIO through 24.9-ohm 1%resistor.
For CNL, it is 100 ohm 1%
Please refer to PDG Table 3-2.

Cited by 575412_WHL_U_PDG_Rev0.9

GPP_H17

Reserved
Rising edge of PCH_PWROK

+3VALW_PCH
R0510 20K_0402_5% @
GPP_H17
R0511 20K_0402_5% @

*This strap should sample LOW.
*There should NOT be any on-board device driving it to opposite direction during strap sampling.

Notes:
1. Internal PD is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

Cited by 566439_CNL_PCH_EDS_LP_Rev2p0

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Title: WHL(A)_DDI/eDP

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+2.5V +2.5V <23,24,25,26,94>

+3VALW +3VALW <9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>

+1.2V +1.2V <7,18,23,24,25,26,85>

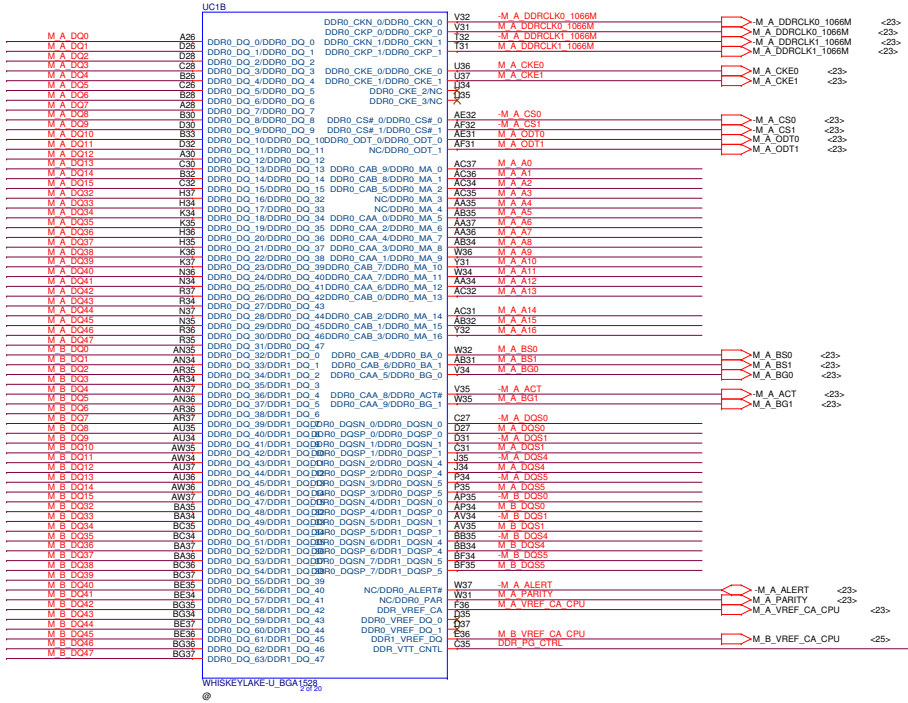
TABLE

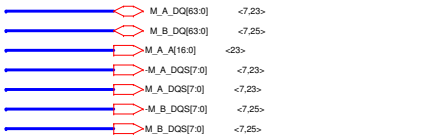
	Pin	Interleave	Non-Interleave
Block 0	A26 D26 D28 C28 B26 C26 B28 A28 B30 D30 B33 D32 A30 C30 B32 C32	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[14] DDR0_DQ[15]	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[14] DDR0_DQ[15]
Block 2	H37 H34 K34 K35 H36 H35 K36 K37 N36 N34 R37 R34 N37 N35 R36 R35	DDR0_DQ[16] DDR0_DQ[17] DDR0_DQ[18] DDR0_DQ[19] DDR0_DQ[20] DDR0_DQ[21] DDR0_DQ[22] DDR0_DQ[23] DDR0_DQ[24] DDR0_DQ[25] DDR0_DQ[26] DDR0_DQ[27] DDR0_DQ[28] DDR0_DQ[29] DDR0_DQ[30] DDR0_DQ[31]	DDR0_DQ[32] DDR0_DQ[33] DDR0_DQ[34] DDR0_DQ[35] DDR0_DQ[36] DDR0_DQ[37] DDR0_DQ[38] DDR0_DQ[39] DDR0_DQ[40] DDR0_DQ[41] DDR0_DQ[42] DDR0_DQ[43] DDR0_DQ[44] DDR0_DQ[45] DDR0_DQ[46] DDR0_DQ[47]
Block 4	AN35 AN34 AR35 AR34 AN37 AN36 AR36 AR37 AU35 AU34 AW35 AW34 AU37 AU36 AW36 AW37	DDR0_DQ[32] DDR0_DQ[33] DDR0_DQ[34] DDR0_DQ[35] DDR0_DQ[36] DDR0_DQ[37] DDR0_DQ[38] DDR0_DQ[39] DDR0_DQ[40] DDR0_DQ[41] DDR0_DQ[42] DDR0_DQ[43] DDR0_DQ[44] DDR0_DQ[45] DDR0_DQ[46] DDR0_DQ[47]	DDR1_DQ[0] DDR1_DQ[1] DDR1_DQ[2] DDR1_DQ[3] DDR1_DQ[4] DDR1_DQ[5] DDR1_DQ[6] DDR1_DQ[7] DDR1_DQ[8] DDR1_DQ[9] DDR1_DQ[10] DDR1_DQ[11] DDR1_DQ[12] DDR1_DQ[13] DDR1_DQ[14] DDR1_DQ[15]
Block 6	BA35 BA34 BC35 BC34 BA37 BA36 BC36 BC37 BE35 BE34 BG35 BG34 BE37 BE36 BG36 BG37	DDR0_DQ[48] DDR0_DQ[49] DDR0_DQ[50] DDR0_DQ[51] DDR0_DQ[52] DDR0_DQ[53] DDR0_DQ[54] DDR0_DQ[55] DDR0_DQ[56] DDR0_DQ[57] DDR0_DQ[58] DDR0_DQ[59] DDR0_DQ[60] DDR0_DQ[61] DDR0_DQ[62] DDR0_DQ[63]	DDR1_DQ[32] DDR1_DQ[33] DDR1_DQ[34] DDR1_DQ[35] DDR1_DQ[36] DDR1_DQ[37] DDR1_DQ[38] DDR1_DQ[39] DDR1_DQ[40] DDR1_DQ[41] DDR1_DQ[42] DDR1_DQ[43] DDR1_DQ[44] DDR1_DQ[45] DDR1_DQ[46] DDR1_DQ[47]

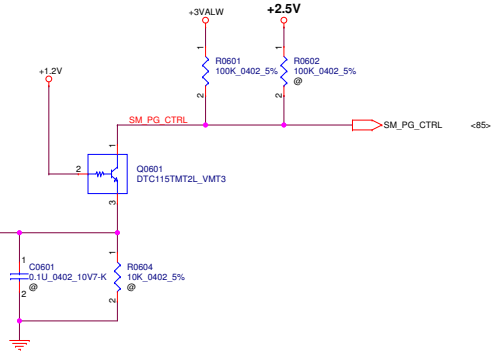
LOGIC

UC1B

WHISKEYLAKE-U_BGA1528







TABLE

	Pin	Interleave	Non-Interleave
Block 0	C27 D27 D31 C31	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]
Block 2	J35 J34 P34 P35	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]
Block 4	AP35 AP34 AV34 AV35	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]
Block 6	BB35 BB34 BF34 BF35	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AB35 W36 AA37 AB34 AA36 V34 AA34 W34 V35 W35	DDR0_MA[5] DDR0_MA[9] DDR0_MA[6] DDR0_MA[8] DDR0_MA[7] DDR0_BA[2] DDR0_MA[12] DDR0_MA[11] DDR0_MA[15] DDR0_MA[14]	DDR0_CAA[0] DDR0_CAA[1] DDR0_CAA[2] DDR0_CAA[3] DDR0_CAA[4] DDR0_CAA[5] DDR0_CAA[6] DDR0_CAA[7] DDR0_CAA[8] DDR0_CAA[9]	DDR0_MA[5] DDR0_MA[9] DDR0_MA[6] DDR0_MA[8] DDR0_MA[7] DDR0_BG[0] DDR0_MA[12] DDR0_MA[11] DDR0_ACT# DDR0_BG[1]
AC32 AB32 AC31 Y32 W32 AC34 AB31 Y31 AC36 AC37 AC35 AA35	DDR0_MA[13] DDR0_CAS# DDR0_WE# DDR0_RAS# DDR0_BA[0] DDR0_MA[2] DDR0_BA[1] DDR0_MA[10] DDR0_MA[1] DDR0_MA[0] DDR0_MA[3] DDR0_MA[4]	DDR0_CAB[0] DDR0_CAB[1] DDR0_CAB[2] DDR0_CAB[3] DDR0_CAB[4] DDR0_CAB[5] DDR0_CAB[6] DDR0_CAB[7] DDR0_CAB[8] DDR0_CAB[9] Not Used Not Used	DDR0_MA[13] DDR0_MA[15] DDR0_MA[14] DDR0_MA[16] DDR0_BA[0] DDR0_MA[2] DDR0_BA[1] DDR0_MA[10] DDR0_MA[1] DDR0_MA[0] DDR0_MA[3] DDR0_MA[4]

LOGIC

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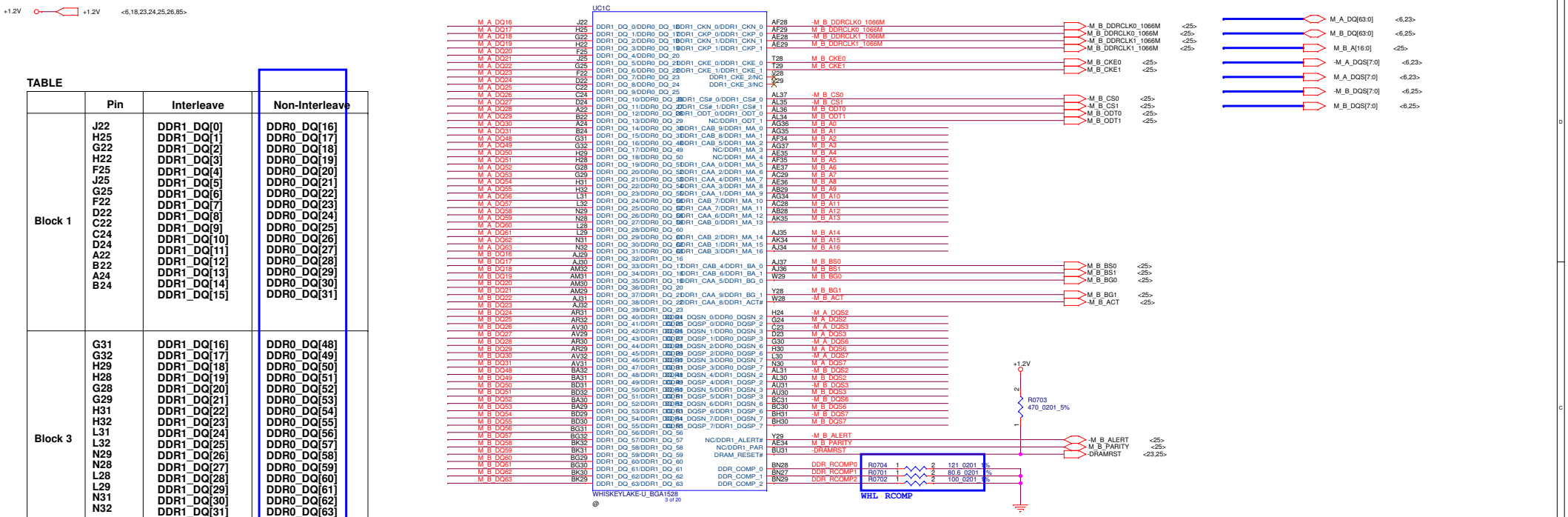

TABLE

	Pin	Interleave	Non-Interleave
Block 1	J22 H25 G22 H22 F25 J25 G25 F22 D22 C22 C24 D24 A22 B22 A24 B24	DDR1_DQ[0] DDR1_DQ[1] DDR1_DQ[2] DDR1_DQ[3] DDR1_DQ[4] DDR1_DQ[5] DDR1_DQ[6] DDR1_DQ[7] DDR1_DQ[8] DDR1_DQ[9] DDR1_DQ[10] DDR1_DQ[11] DDR1_DQ[12] DDR1_DQ[13] DDR1_DQ[14] DDR1_DQ[15]	DDR0_DQ[16] DDR0_DQ[17] DDR0_DQ[18] DDR0_DQ[19] DDR0_DQ[20] DDR0_DQ[21] DDR0_DQ[22] DDR0_DQ[23] DDR0_DQ[24] DDR0_DQ[25] DDR0_DQ[26] DDR0_DQ[27] DDR0_DQ[28] DDR0_DQ[29] DDR0_DQ[30] DDR0_DQ[31]
Block 3	G31 G32 H29 H28 G28 G29 H31 H32 L31 L32 N29 N28 L28 L29 N31 N32	DDR1_DQ[16] DDR1_DQ[17] DDR1_DQ[18] DDR1_DQ[19] DDR1_DQ[20] DDR1_DQ[21] DDR1_DQ[22] DDR1_DQ[23] DDR1_DQ[24] DDR1_DQ[25] DDR1_DQ[26] DDR1_DQ[27] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[30] DDR1_DQ[31]	DDR0_DQ[48] DDR0_DQ[49] DDR0_DQ[50] DDR0_DQ[51] DDR0_DQ[52] DDR0_DQ[53] DDR0_DQ[54] DDR0_DQ[55] DDR0_DQ[56] DDR0_DQ[57] DDR0_DQ[58] DDR0_DQ[59] DDR0_DQ[60] DDR0_DQ[61] DDR0_DQ[62] DDR0_DQ[63]
Block 5	AJ29 AJ30 AM32 AM31 AM30 AM29 AJ31 AJ32 AR31 AR32 AV30 AV29 AR30 AR29 AV32 AV31	DDR1_DQ[32] DDR1_DQ[33] DDR1_DQ[34] DDR1_DQ[35] DDR1_DQ[36] DDR1_DQ[37] DDR1_DQ[38] DDR1_DQ[39] DDR1_DQ[40] DDR1_DQ[41] DDR1_DQ[42] DDR1_DQ[43] DDR1_DQ[44] DDR1_DQ[45] DDR1_DQ[46] DDR1_DQ[47]	DDR1_DQ[16] DDR1_DQ[17] DDR1_DQ[18] DDR1_DQ[19] DDR1_DQ[20] DDR1_DQ[21] DDR1_DQ[22] DDR1_DQ[23] DDR1_DQ[24] DDR1_DQ[25] DDR1_DQ[26] DDR1_DQ[27] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[30] DDR1_DQ[31]
Block 7	BA32 BA31 BD31 BD32 BA30 BA29 BD29 BD30 BG31 BG32 BK32 BK31 BG29 BG30 BK30 BK29	DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[50] DDR1_DQ[51] DDR1_DQ[52] DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[55] DDR1_DQ[56] DDR1_DQ[57] DDR1_DQ[58] DDR1_DQ[59] DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[62] DDR1_DQ[63]	DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[50] DDR1_DQ[51] DDR1_DQ[52] DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[55] DDR1_DQ[56] DDR1_DQ[57] DDR1_DQ[58] DDR1_DQ[59] DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[62] DDR1_DQ[63]

LOGIC

TABLE

	Pin	Interleave	Non-Interleave
Block 1	H24 G24 C23 D23	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]
Block 3	G30 H30 L30 N30	DDR1_DQSN[2] DDR1_DQSP[2] DDR1_DQSN[3] DDR1_DQSP[3]	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]
Block 5	AL31 AL30 AU31 AU30	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]	DDR1_DQSN[2] DDR1_DQSP[2] DDR1_DQSN[3] DDR1_DQSP[3]
Block 7	BC31 BC30 BH31 BH30	DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]	DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AF35 AB29 AE37 AE36 AC29 W29 AB28 AC28 W28 Y28	DDR1_MA[5] DDR1_MA[9] DDR1_MA[6] DDR1_MA[8] DDR1_MA[7] DDR1_BA[2] DDR1_MA[12] DDR1_MA[11] DDR1_MA[15] DDR1_MA[14]	DDR1_CAA[0] DDR1_CAA[1] DDR1_CAA[2] DDR1_CAA[3] DDR1_CAA[4] DDR1_CAA[5] DDR1_CAA[6] DDR1_CAA[7] DDR1_CAA[8] DDR1_CAA[9]	DDR1_MA[5] DDR1_MA[9] DDR1_MA[6] DDR1_MA[8] DDR1_MA[7] DDR1_BG[0] DDR1_MA[12] DDR1_MA[11] DDR1_ACT# DDR1_BG[1]
AK35 AK34 AJ35 AJ34 AJ37 AF34 AJ36 AG34 AG35 AG36 AG37 AE35	DDR1_MA[13] DDR1_CAS# DDR1_WE# DDR1_RAS# DDR1_BA[0] DDR1_MA[2] DDR1_BA[1] DDR1_MA[10] DDR1_MA[1] DDR1_MA[0] DDR1_MA[3] DDR1_MA[4]	DDR1_CAB[0] DDR1_CAB[1] DDR1_CAB[2] DDR1_CAB[3] DDR1_CAB[4] DDR1_CAB[5] DDR1_CAB[6] DDR1_CAB[7] DDR1_CAB[8] DDR1_CAB[9] Not Used Not Used	DDR1_MA[13] DDR1_MA[15] DDR1_MA[14] DDR1_MA[16] DDR1_BA[0] DDR1_MA[2] DDR1_BA[1] DDR1_MA[10] DDR1_MA[1] DDR1_MA[0] DDR1_MA[3] DDR1_MA[4]

LOGIC

Table 3-1. RCOMP Recommendation for WHL and CFL

Interface	Pin Name	Board Rterm (Ohm)	Board Rdc (Ohm)	Note
DDR - LP3	DDR_RCOMP[0]	200Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[1]	80.6Ω ± 1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	162Ω ± 1% on pkg to VSS	N/A	
DDR - DDR4 SODIMM	DDR_RCOMP[0]	121Ω ±1% on pkg to VSS	N/A	Different RCOMP value in CNL. Refer to Table 3-2
	DDR_RCOMP[1]	80.6Ω ± 1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	100Ω ± 1% on pkg to VSS	N/A	

Table 3-2. RCOMP Recommendation for CNL

Interface	Pin Name	Board Rterm (Ohm)	Board Rdc (Ohm)	Note
DDR - DDR4 SODIMM	DDR_RCOMP[0]	100Ω ±1% on pkg to VSS	N/A	No LP3 support in CNL
	DDR_RCOMP[1]	100Ω ± 1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	100Ω ± 1% on pkg to VSS	N/A	

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Title: WHL(C)_DDR4 CH.B

LCFC

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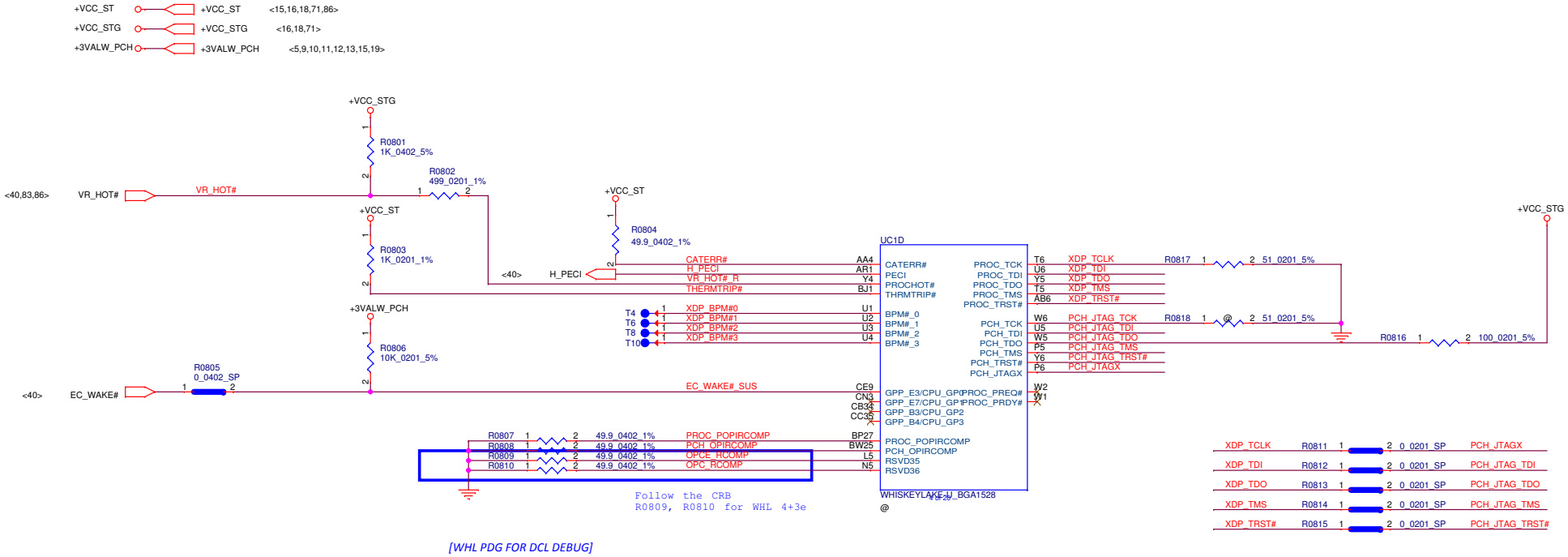

[WHL PDG FOR DCL DEBUG]

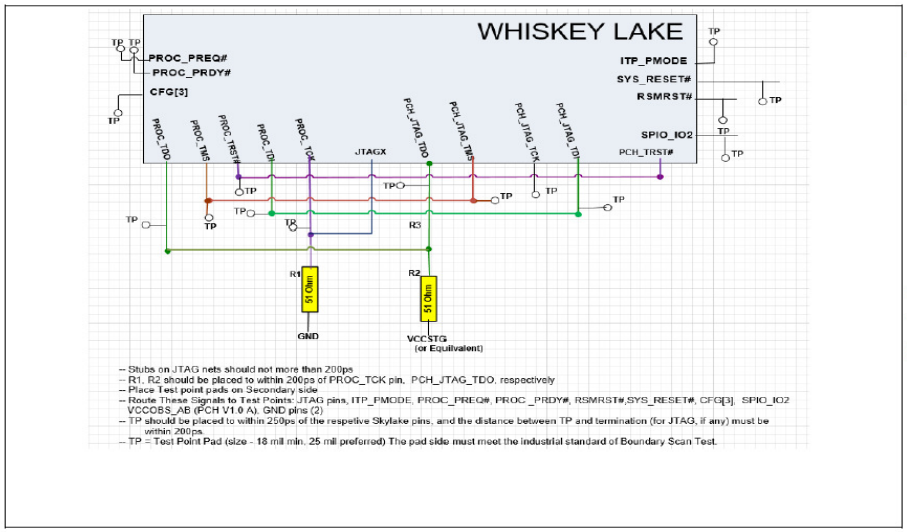

Figure 13-6. Primary Debug PortConnector Less Routing Topology

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: WHL(D)_MISC/ JTAG

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

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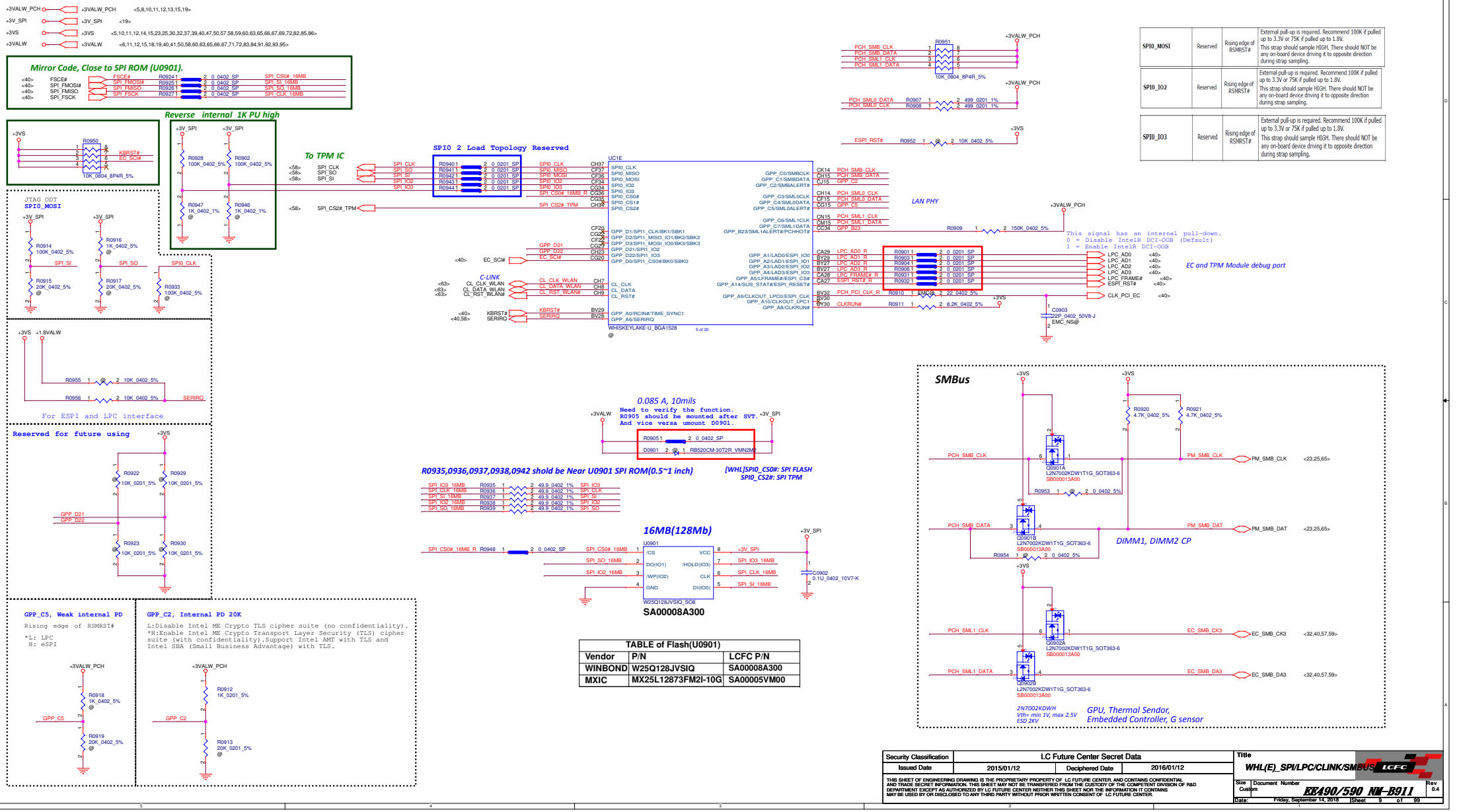

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

TABLE of Flash(U0901)

Vendor	P/N	LCFC P/N
WINBOND	W25Q128JVSIQ	SA00008A300
MXIC	MX25L12873FM2I-10G	SA00005VM00

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Title: WHL(E)_SPI/LPC/CLINK/SMBUS

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+3VALW_PCH <5,8,9,11,12,13,15,19>
+3VS <5,9,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>
+3VALW <6,9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>
+1.8VALW <9,19,38,40,50,51,63,93>

+3VALW_PCH
R1007 1 @ 2 10K_0201_5% DGPU_HOLD_RST#
R1035 1 2 100K_0201_5%

+3VS
R1026 10K_0402_5% 1 @ 2 GPP_C15
R1027 10K_0402_5% 1 @ 2 F1_LED#
R1028 10K_0402_5% 1 @ 2 F4_LED#
R1003 10K_0201_5% 1 @ 2 VGA_ON_R

+3VS
R1001 1 2 20K_0402_1% GPP_A11
<63> RF_OFF# RF_OFF#
GPP_B18
<63> BT_ON BT_ON
GPP_B22
<63> BRI_RSP_CNVI BRI_RSP_CNVI
<63> RGI_DT_CNVI RGI_DT_CNVI
<63> BRI_DT_CNVI BRI_DT_CNVI
<63> RGI_RSP_CNVI RGI_RSP_CNVI
<41,63> UART2_RX UART2_RX
<41,63> UART2_TX UART2_TX

FN, F1, F4 PD 100K, BIOS need output "High" while act i ve

<37,38,39> VGA_ON VGA_ON R1002 1 2 0_0201_SP VGA_ON_R
To VGA_CORE IC, RPC3.7
<37> DGPU_PWROK
<30> DGPU_HOLD_RST#
R1004 100K_0201_5%

UC1F

CC27	GPP_B15/GSPI0_CS0#	
CC32	GPP_A7/PIRQA#/GSPI0_CS1#	
CE26	GPP_B16/GSPI0_CLK	
CE27	GPP_B17/GSPI0_MISO	
CE29	GPP_B18/GSPI0_MOSI	
CA31	GPP_B19/GSPI1_CS0#	
CA32	GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#	
CC29	GPP_B20/GSPI1_CLK	
CC30	GPP_B21/GSPI1_MISO	
CA30	GPP_B22/GSPI1_MOSI	
CK20	GPP_F5/CNV_BRI_RSP	
CG19	GPP_F6/CNV_RGI_DT	
CJ20	GPP_F4/CNV_BRI_DT	
CH19	GPP_F7/CNV_RGI_RSP	
CR12	GPP_C20/UART2_RXD	
CP12	GPP_C21/UART2_TXD	
CN12	GPP_C22/UART2_RTS#	
CM12	GPP_C23/UART2_CTS#	
CM11		
CN11	GPP_C16/I2C0_SDA	
	GPP_C17/I2C0_SCL	
CK12	GPP_C18/I2C1_SDA	
CJ12	GPP_C19/I2C1_SCL	
CF27	GPP_H4/I2C2_SDA	
CF28	GPP_H5/I2C2_SCL	
CH27	GPP_H6/I2C3_SDA	
CH28	GPP_H7/I2C3_SCL	
CJ30	GPP_H8/I2C4_SDA	
CJ31	GPP_H9/I2C4_SCL	

GPP_D9/ISH_SPI_CS#/GSPI2_CS0#	CN22	TP_RESET_PCH	R1034 1	2 0_0201_SP	TP_RESET
GPP_D10/ISH_SPI_CLK/GSPI2_CLK	CR22	LID_CLOSE#_PCH	R1032 1	2 0_0201_SP	LID_CLOSE#
GPP_D11/ISH_SPI_MISO/GSPI2_MISO	CM22				
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI	CP22	GPP_D12			
GPP_D5/ISH_I2C0_SDA	CK22	GPP_D5			
GPP_D6/ISH_I2C0_SCL	CH20				
GPP_D7/ISH_I2C1_SDA	CH22	GPP_D7			
GPP_D8/ISH_I2C1_SCL	CJ22	PAD_DISABLE_PCH	R1033 1	2 0_0201_SP	PAD_DISABLE
GPP_H10/I2C5_SDA/ISH_I2C2_SDA	CJ27				
GPP_H11/I2C5_SCL/ISH_I2C2_SCL	CJ29				
GPP_D13/ISH_UART0_RXD	CM24	PLANARID0			
GPP_D14/ISH_UART0_TXD	CN23	PLANARID1			
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#	CM23	PLANARID2			
GPP_D16/ISH_UART0_CTS#/SML0ALERT#	CR24	PLANARID3			
GPP_C12/UART1_RXD/ISH_UART1_RXD	CG12				
GPP_C13/UART1_TXD/ISH_UART1_TXD	CH12	F1_LED#			
GPP_C14/UART1_RTS#/ISH_UART1_RTS#	CF12	F4_LED#			
GPP_C15/UART1_CTS#/ISH_UART1_CTS#	CG14	GPP_C15			
GPP_A18/ISH_GP0	BW35				
GPP_A19/ISH_GP1	BW34				
GPP_A20/ISH_GP2	CA37				
GPP_A21/ISH_GP3	CA36				
GPP_A22/ISH_GP4	CA35				
GPP_A23/ISH_GP5	CA34				
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#	BW37				

TP_RESET_PCH → TP_RESET → TP_RESET <65>
LID_CLOSE#_PCH → LID_CLOSE# → LID_CLOSE# <65>
PAD_DISABLE_PCH → PAD_DISABLE → PAD_DISABLE <65>
F1_LED# <65>
F4_LED# <65>

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@

Graphics ID

Status	PLANARID3 (GPP_D16)
UMA	0 (R1016)
DIS	1 (R1015)

Board ID

PHASE	PLANARID2 (GPP_D15)	PLANARID1 (GPP_D14)	PLANARID0 (GPP_D13)
EVT	0 (R1018)	0 (R1020)	0 (R1031)
FVT	0 (R1018)	0 (R1020)	1 (R1030)
SIT	0 (R1018)	1 (R1019)	0 (R1031)
SVT	0 (R1018)	1 (R1019)	1 (R1030)

+3VS
R1015 DIS@ 10K_0201_5%
R1017 10K_0201_5%
R1019 10K_0201_5%
R1030 10K_0201_5%
PLANARID0
PLANARID1
PLANARID2
PLANARID3
R1016 UMA@ 10K_0201_5%
R1018 10K_0201_5%
R1020 10K_0201_5%
R1031 10K_0201_5%

GPP_B22, Internal PD 20K
*L: SPI
H: LPC
+3VS
R1010 20K_0402_5% @
GPP_B22
R1011 20K_0402_5% @

+3VS
R1012 10K_0201_5% @
GPP_D5
R1013 10K_0201_5% @

GPP_D12, External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
+3VALW_PCH
R1005 100K_0201_1%
GPP_D12
R1006 10K_0201_5% @
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_B18, Internal PD 20K
*L: Disable " No Reboot" mode
H: Enable " No Reboot" mod
+3VALW_PCH
R1008 1K_0402_5% @
GPP_B18
R1009 20K_0402_5% @

GPP_D7, Reserved, Rising edge of DSW_PWROK
+3VALW_PCH
R1014 100K_0201_1%
GPP_D7
External pull-up is required. Recommend 100K.
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling

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+3VALW_PCH +3VALW_PCH <5,8,9,10,12,13,15,19>
+3VS +3VS <5,9,10,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>
+VCC_HDA +VCC_HDA <19>
+VCC_IO +VCC_IO <5,18,21,71>
+3VALW +3VALW <6,9,12,15,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>

<50> PCH_HDA_RST#
<50> PCH_HDA_SDOUT
<50> PCH_HDA_SYNC
PCH_HDA_RST#
PCH_HDA_SDOUT
PCH_HDA_SYNC
RP1101
33_0804_8P4R_5%
SD30000370T
HDA_RST#
HDA_SDOUT
HDA_SYNC

<40> ME_FLASH
R1101 1 2 0_0402_SP

<50> PCH_HDA_BCLK
PCH_HDA_BCLK
R1110 1 EMC@ 2 33_0402_5% HDA_BCLK
C1101
22P_0402_50V8-J
EMC_NS@

To enable Flash Descriptor Security Override, this signal should be pulled up to VCCHDA through a 1 KΩ to 2.2 KΩ ± 5% resistor.

+VCC_HDA
R1102 1K_0402_5% @
HDA_SDOUT
R1103 20K_0402_5% @

+VCC_IO
R1104 1K_0402_5% @
PCH_HDA_SDIN0
R1105 20K_0402_5% @

GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3_3 through a 1~8.2KΩ resistor to disable this capability

+3VS
R1106 8.2K_0402_5% @
PCH_BEEP
R1107 20K_0402_5% @

WINDU and E470 can't stuff TBD

+3VALW_PCH
R1108 1K_0402_5% @
+3VALW
R1111 100K_0201_5% @
R1112 100K_0201_5% @

UC1G
HDA_SYNC
HDA_BCLK
HDA_SDOUT
<50> PCH_HDA_SDIN0
HDA_RST#
@ TP4325
<63> RF_RESET_B_CNVI
<63> CLKREQ0_CNVI
<60> D_J_CTL
<67> CR_ID
<51> PCH_BEEP

BN34 HDA_SYNC/I2S0_SFRM
BN37 HDA_BCLK/I2S0_SCLK
BN36 HDA_SDO/I2S0_TXD
BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 GPP_D23/I2S_MCLK
BL37 I2S1_SFRM/SNDW2_CLK
BL34 I2S1_TXD/SNDW2_DATA
CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
CH32 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
CH29 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
CP24 GPP_D19/DMIC_CLK0/SNDW4_CLK
CN24 GPP_D20/DMIC_DATA0/SNDW4_DATA
CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK
CJ25 GPP_D18/DMIC_DATA1/SNDW3_DATA
CF35 GPP_B14/SPKR
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CH36 GPP_G0/SD_CMD
CL35 GPP_G1/SD3_DATA0
CL36 GPP_G2/SD3_DATA1
CM35 GPP_G3/SD3_DATA2
CN35 GPP_G4/SD_DATA3
CH35 GPP_G5/SD_CD#
CK36 GPP_G6/SD_CLK
CK34 GPP_G7/SD_WP
BW36 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
BY31 GPP_A16/SD_1P8_SEL
CK33 SD_1P8_RCOMP
CM34 SD_3P3_RCOMP
R1109 1 2 200_0402_1%

Table 3-1.RCOMP Recommendation for WHL and CFL

SD3 & EMMC	SD_1P8_RCOMP SD_3P3_RCOMP EMMC_RCOMP	200Ω ±1% to GND	<0.1	Notes: These pins can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.

+3VS
R1023 14S@ 10K_0201_5%
R1021 NTPM@ 10K_0201_5%
PLANARID4
14S_ID
R1024 14@ 10K_0201_5%
R1022 TPM@ 10K_0201_5%

Panel ID (Pin#7 Control)

Status	D_J_CTL (GPP_D19)
15"	0 (GND Low)
14"	1 (NC High)

TPM ID

Status	PLANARID4 (GPP_D18)
TPM	0 (R1022)
NTPM	1 (R1021)

14S ID

Status	14S_ID (GPP_D20)
14"	0 (R1024)
14"S	1 (R1023)

Card Reader ID (I/O Board Control)

Status	CR_ID (GPP_D17)
CRG	0
CRR	1

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+3VALW_PCH — +3VALW_PCH <5,8,9,10,11,13,15,19>

+3VS — +3VS <5,9,10,11,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

+3VALW — +3VALW <6,9,11,15,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>

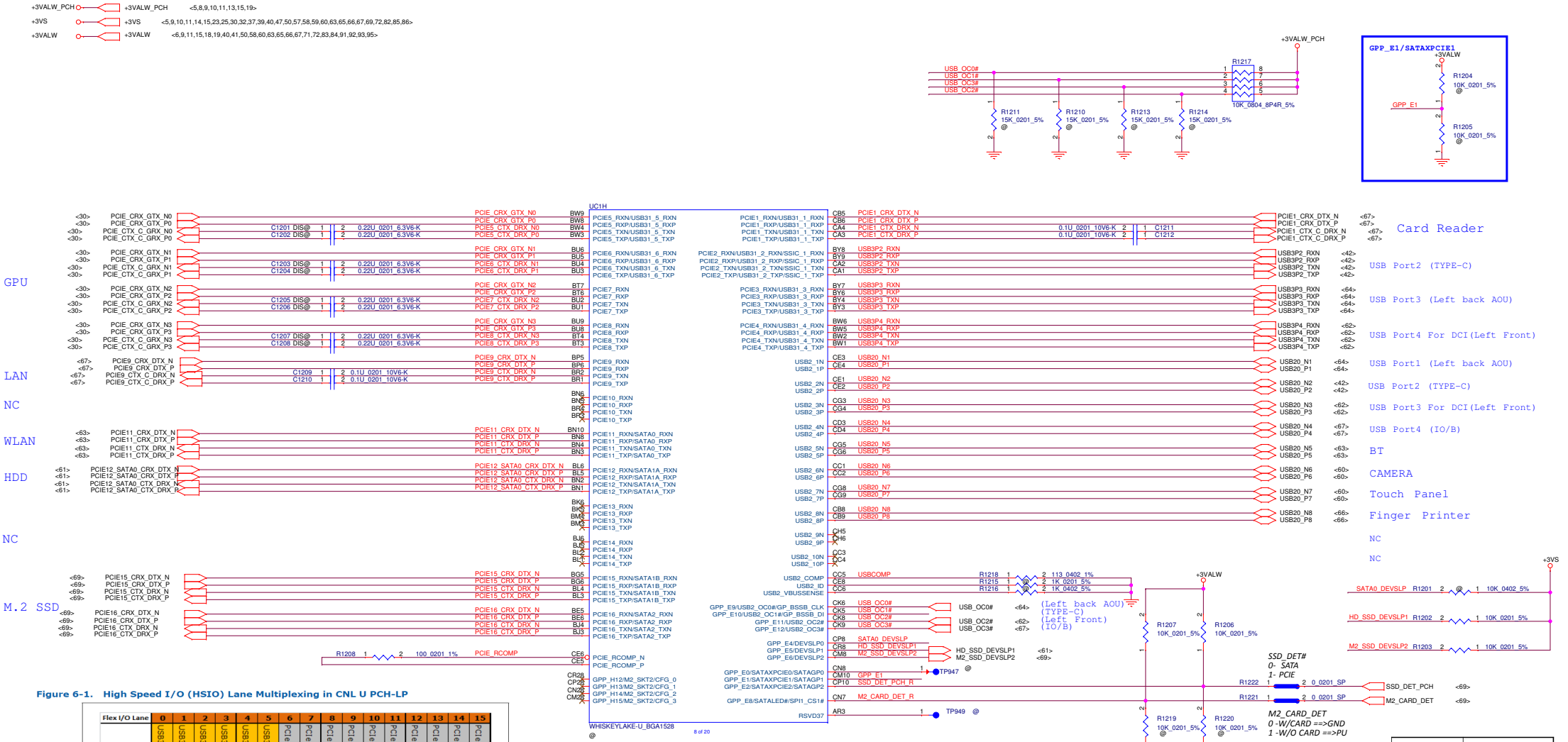

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

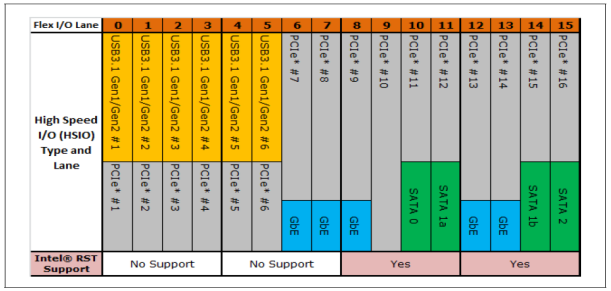

Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
										Cycle Router #2				Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP3		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

HSIO Configuration	CS19 E14/E15
PCIE 1	Media Card Controller
USB3 2	Type-C Port
USB3 3	Type-A Port-Gen1(AOU)
USB3 4	Type-A Port-Gen2(DCI)
PCIE 5 x4_L0	dGPU
PCIE 5 x4_L1	dGPU
PCIE 5 x4_L2	dGPU
PCIE 5 x4_L3	dGPU
PCIE 9	GbE PHY
PCIE 10	(Reserved)
PCIE 11	(Reserved)
SATA 1	2.5 HDD
PCIE 13	(Reserved)
PCIE 14	(Reserved)
PCIE 15 x2 L0	PCIe Optane
PCIE 15 x2 L1	PCIe Optane / SATA

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Title: WHL(H)_PCIE/ SATA/ USB3

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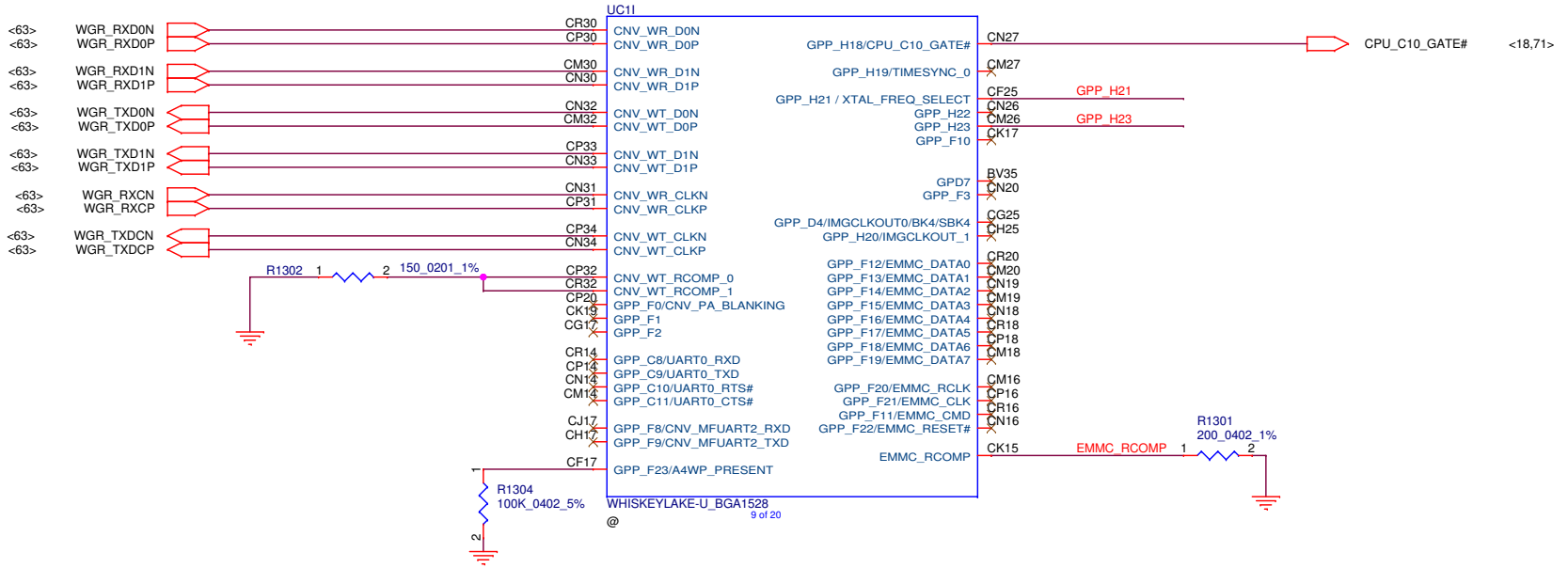
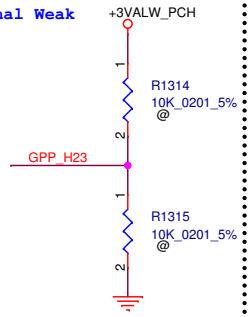
+3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

+3VALW_PCH <5,8,9,10,11,12,15,19>

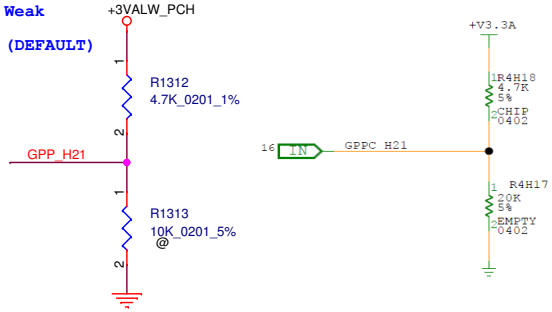


GPP_H23, Internal Weak pull-down



This strap must be configured to 0
(SAFS is disabled)
if the eSPI or LPC strap is configured to 0
(eSPI is disabled)

GPP_H21, Internal Weak pull-down
LOW: 38.4/19.2MHZ (DEFAULT)
HIGH: 24MHZ



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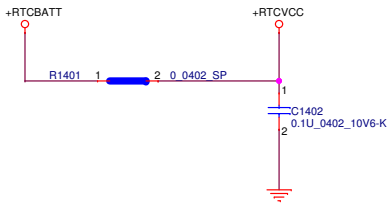
+RTCBATT +RTCBATT <66,80>

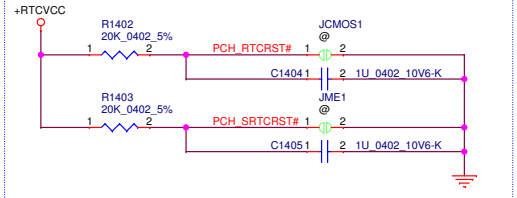
+RTCVCC +RTCVCC <15,19>

+3VS +3VS <5,9,10,11,12,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

RTC External Circuit

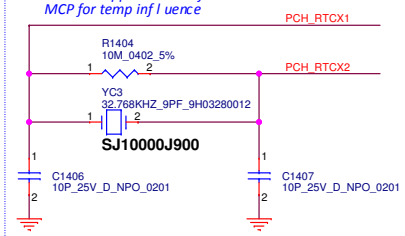
+RTCBATT, +RTCVCC
Trace width = 20mils

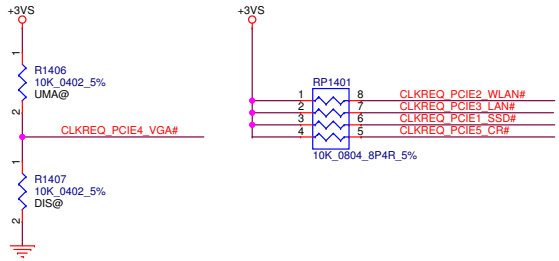


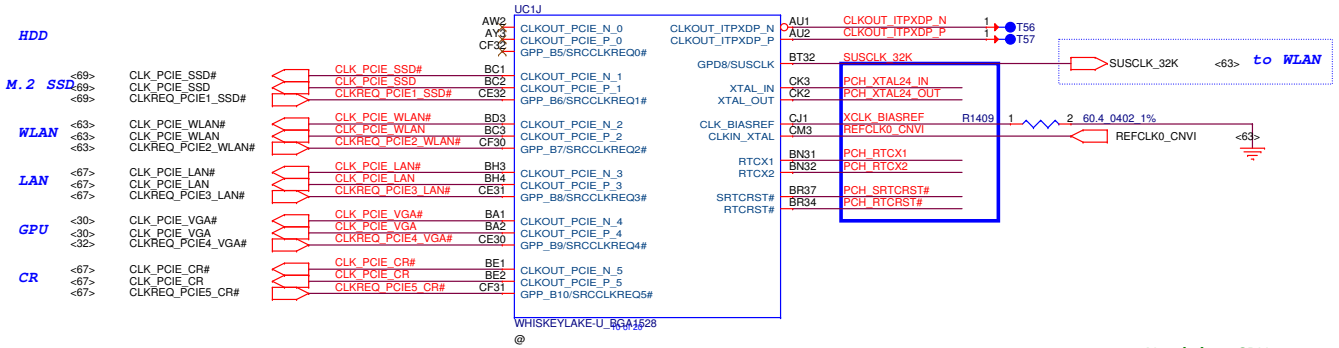


RTC Crystal

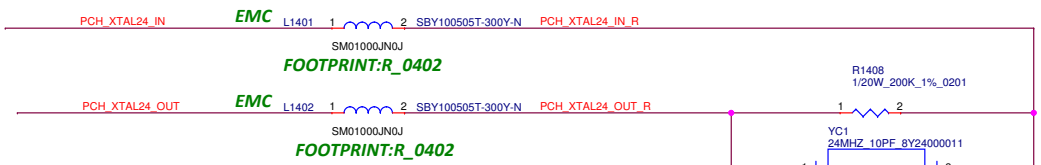
1. Space > 15mils
2. No trace under crystal
3. Place on oppsosit side of
MCP for temp inf l uence

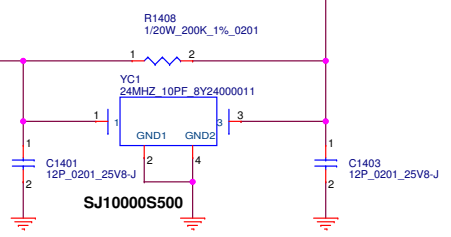






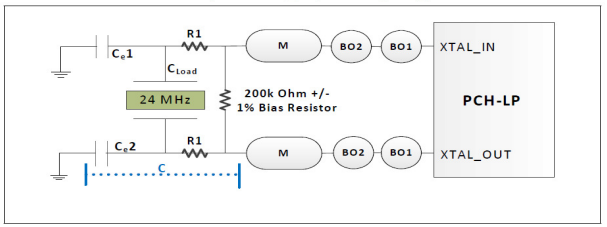
Need close CPU





7.3.2.3 WHLU PCH-LP Platform XTAL Routing Guidelines

Figure 7-7. WHL U PCH-LP Platform Crystal XTAL_IN/OUT Topology



YC1
Equivalent resistance (RR) = 30 Ohm

TABLE of XTAL (YC1)		
Vendor	P/N	LCFC P/N
TXC	8Y24000034	SJ10000S500
HARMONY	X2C024000DC1H-HU	SJ10000RR00

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+3VALW +3VALW <6,9,11,12,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>

+3VALW_PCH +3VALW_PCH <5,8,9,10,11,12,13,19>

+3VS +3VS <5,9,10,11,12,14,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

+RTCVCC +RTCVCC <14,19>

+VCC_ST +VCC_ST <8,16,18,71,86>

+3VALW

RP1501 1 8 AC_PRESENT; 2 7 BATLOW#; 3 6; 4 5

10K_0804_8P4R_5%

SD300002P0T

+3VALW

For vPRO LAN WAKE#

R1501 1 @ 2 10K_0402_5% EC_WAKE#_DSW

R1502 1 @ 2 10K_0402_5% PM_SLP_S5#

R1503 1 2 1K_0402_5% PCIE_WAKE#

+3VS

R1505 1 @ 2 10K_0201_5% SYS_RESET#

+3VALW_PCH

R1506 1 2 10K_0201_5%

R1507 1 2 10K_0402_5% EC_RSMRST#

R1508 1 @ 2 10K_0201_5% H_CPUPWRGD

R1525 1 2 10K_0402_5% PCH_PWROK

R1526 1 @ 2 10K_0402_5% PCH_SYSPWROK

R1527 1 @ 2 10K_0402_5% AC_PRESENT

Reserved for HW control

R1529 1 2 0_0402_SP

+3VALW

+VCC_ST

R1511 100K_0402_5% @

R1512 @ 100K_0402_5%

R1513 1K_0402_5%

VCCST_PWRGD

<40> VCCST_PG_EC R1509 1 @ 2 0_0402_5%

<40,86> VR_ON R1510 1 @ 2 0_0402_5%

Q1501A L2N7002KDW1T1G_SOT363-6 SB000013A00 @

Q1501B L2N7002KDW1T1G_SOT363-6 SB000013A00 @

PM_SLP_S3# 1 T1501

PM_SLP_S4# 1 T1502

PM_SLP_S5# 1 T1503

UC1K

PCH_PLT_RST# BJ35

SYS_RESET# CN10

EC_RSMRST# BR36

<40> EC_RSMRST#

H_CPUPWRGD AR2

VCCST_PWRGD R1519 1 2 60.4_0402_1% BJ2

PROCPWRGD

VCCST_PWRGOOD

<40> PCH_SYSPWROK CR10

PCH_PWROK BP31

EC_RSMRST# R1520 1 2 0_0402_SP DSW_PWROK BP30

SYS_PWROK

PCH_PWROK

DSW_PWROK

R1521 1 2 0_0402_SP SUSWARN# BV34

SUSACK# BY32

GPP_A13/SUSWARN#/SUSPWRDACK

GPP_A15/SUSACK#

<63> PCIE_WAKE# PCIE_WAKE# BU30

EC_WAKE#_DSW BU32

BU34

WAKE#

GPD2/LAN_WAKE#

GPD11/LANPHYPC

GPP_B13/PLTRST#

SYS_RESET#

RSMRST#

GPP_B12/SLP_S0# BJ37 PM_SLP_S0# 1 T1504

GPD4/SLP_S3# BU36 PM_SLP_S3# <40>

GPD5/SLP_S4# BU27 PM_SLP_S4# <40>

GPD10/SLP_S5# BT29 PM_SLP_S5# <40>

SLP_SUS# BU29 PCH_SLP_SUS# 1 T1505

SLP_LAN# BT31

GPD9/SLP_WLAN# BT30

GPD6/SLP_A# BU37 PM_SLP_A# 1 T1506

GPD3/PWRBTN# BU28 PBTN_OUT#

GPD1/ACPRESENT BU35 AC_PRESENT

GPD0/BATLOW# BV36 BATLOW#

PBTN_OUT# <40>

AC_PRESENT <40>

INTRUDER# BR35 PCH_INTRUDER# R1522 1 2 1M_0402_5%

GPP_B11/EXT_PWR_GATE# CC37 EXT_PWR_GATE#

GPP_B2/VRALERT# CC36 VRALERT# 1 T1507

INPUT3VSEL BT27 INPUT3VSEL

11 of 20

WHISKEYLAKE-U_BGA1528

@

+3VALW

R1517 100K_0402_5%

+RTCVCC

<40> PCH_PWROK R1515 1 2 0_0402_SP

<40,86> VGATE R1516 1 @ 2 0_0402_5%

1. must be always pulled-up to VCCRTC.
2. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on product i on boards.

R1523 1 2 0_0402_SP

+3VALW

U1501 @

NC VCC

IN_A

GND OUT_Y

TC7SG17FE_SON5

SA00005T00J

PCH_PLT_RST#

R1524 100K_0402_5%

PLT_RST# PLT_RST# <30,40,58,63,67,69>

C7214 0.1U_0402_16V7-K EMC_NS@

T1509

+V3.3A_DSW

3V SELECT STRAP

LOW-> 3.3V +/-5%

HIGH->3.0V +/-5%

R3F17 4.7K 5% _EMPTY 0402

INPUT3VSEL

R3F18 4.7K 5% _CHIP 0402

Follow the CRB

+3VALW

R1504 4.7K_0402_5%

INPUT3VSEL

R1514 4.7K_0402_5%

[PAGE_TITLE=PCH STRAPS]

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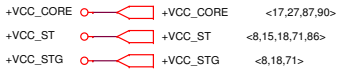
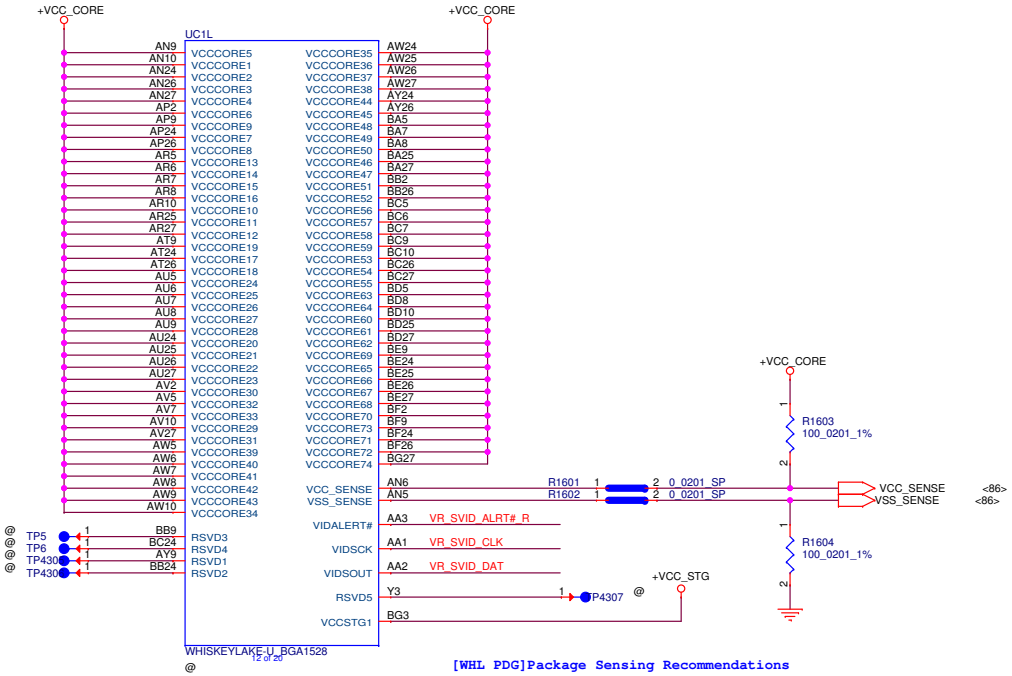


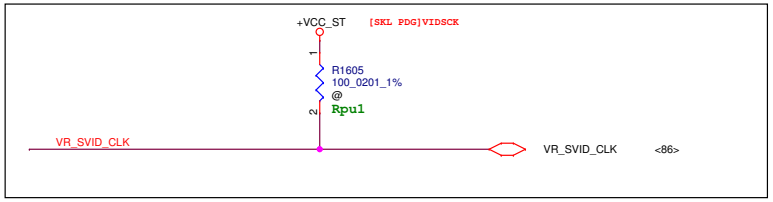


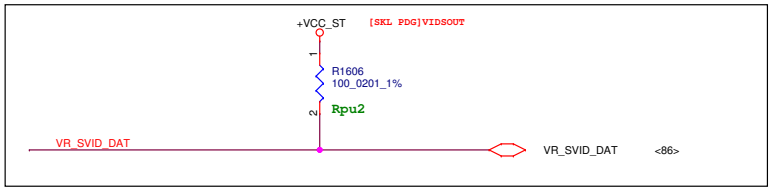
[WHL PDG]Package Sensing Recommendations

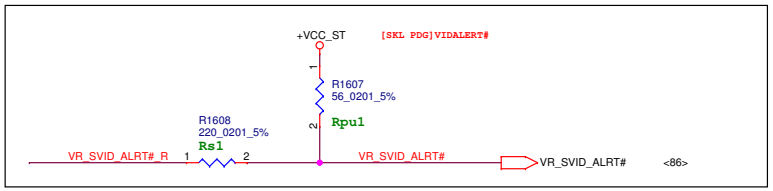
1.Trace Length Match: <25mil
2.Space: >25mil
3.Trace impedance:50ohm
4.Sense traces should be referenced to a solid ground plane
5.Avoid crossing over plane splits

[WHL PDG]SVID

VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface (SVID) used to transfer power management information between the Whiskey Lake processor and the voltage regulator controllers. Alert signal must be routed between Clk and Data signals to minimize Cross-Talk.







Topology Guidelines	
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

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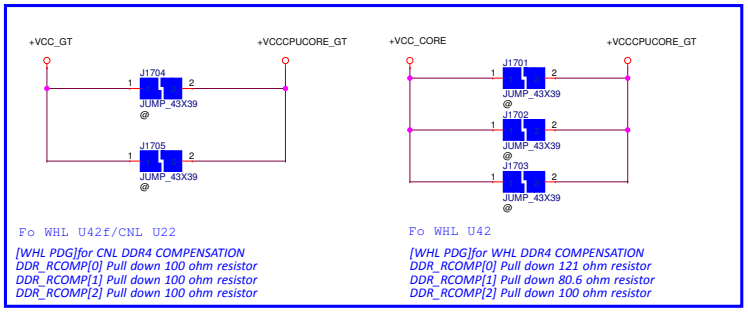
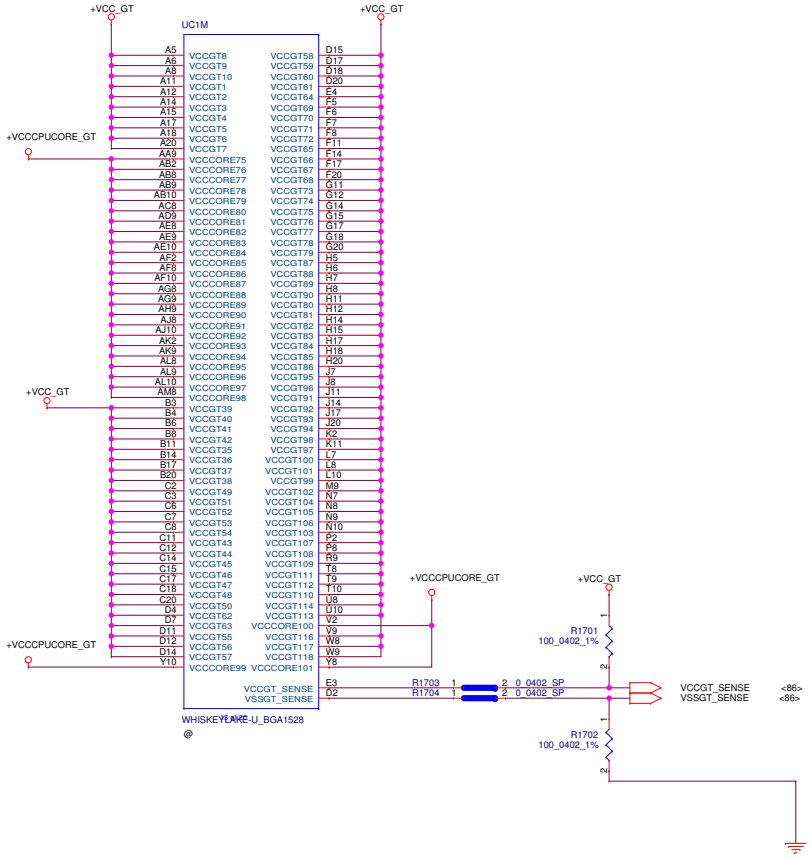
+VCC_GT — +VCC_GT <27,88,90>
+VCC_CORE — +VCC_CORE <16,27,87,90>
+VCCPUCORE_GT — +VCCPUCORE_GT <27>



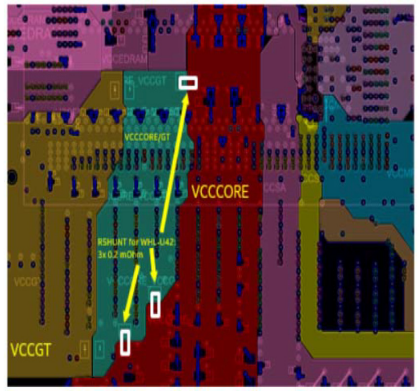


575414_WHL_Ballout List

Pin Number	CFL U43e	WHL U42 QS/Production	CNL U22/WHL-U42 ES0/1
AA9	VCCGT	VCCCORE	VCCGT
AB10	VCCGT	VCCCORE	VCCGT
AB2	VCCGT	VCCCORE	VCCGT
AB8	VCCGT	VCCCORE	VCCGT
AB9	VCCGT	VCCCORE	VCCGT
AC8	VCCGT	VCCCORE	VCCGT
AD9	VCCGT	VCCCORE	VCCGT
AE10	VCCGT	VCCCORE	VCCGT
AE8	VCCGT	VCCCORE	VCCGT
AE9	VCCGT	VCCCORE	VCCGT
AF10	VCCGT	VCCCORE	VCCGT
AF2	VCCGT	VCCCORE	VCCGT
AF8	VCCGT	VCCCORE	VCCGT
AG8	VCCGT	VCCCORE	VCCGT
AG9	VCCGT	VCCCORE	VCCGT
AH9	VCCGT	VCCCORE	VCCGT
AJ10	VCCGT	VCCCORE	VCCGT
AJ8	VCCGT	VCCCORE	VCCGT
AK2	VCCGT	VCCCORE	VCCGT
AK9	VCCGT	VCCCORE	VCCGT
AL10	VCCGT	VCCCORE	VCCGT
AL8	VCCGT	VCCCORE	VCCGT
AL9	VCCGT	VCCCORE	VCCGT
AM8	VCCGT	VCCCORE	VCCGT
V2	VCCGT	VCCCORE	VCCGT
Y10	VCCGT	VCCCORE	VCCGT
Y8	VCCGT	VCCCORE	VCCGT

Figure 11-11.Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline

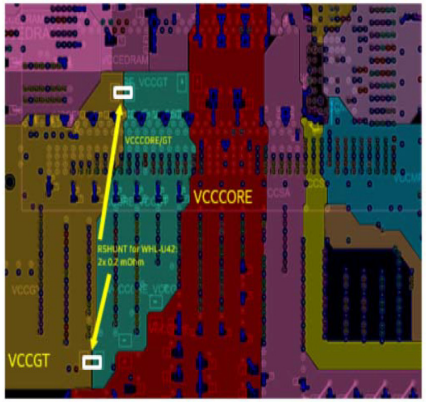
Routing guideline for RSHUNT for WHL U42



- Place 3x 0.2mOhm RSHUNT for WHL U42

Figure 11-11.Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline

Routing guideline for RSHUNT for WHL U42f/CNL U22



- Place 2x 0.2mOhm RSHUNT for WHL U42f/CNL U22

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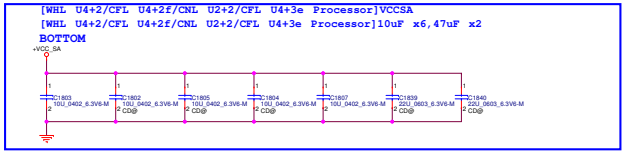
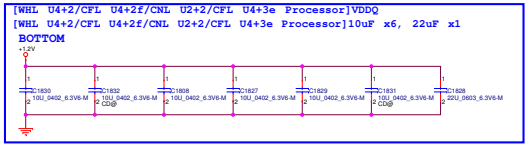
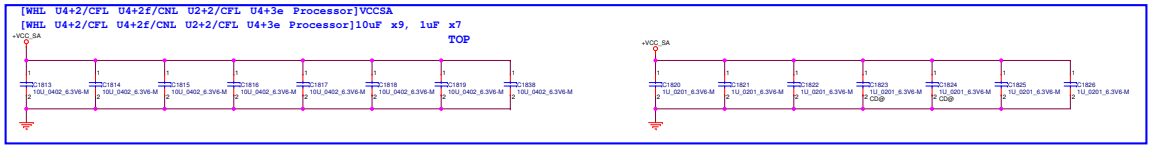
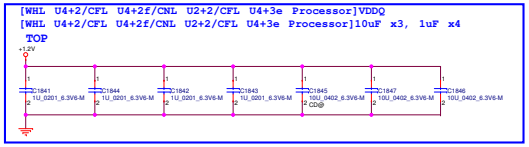
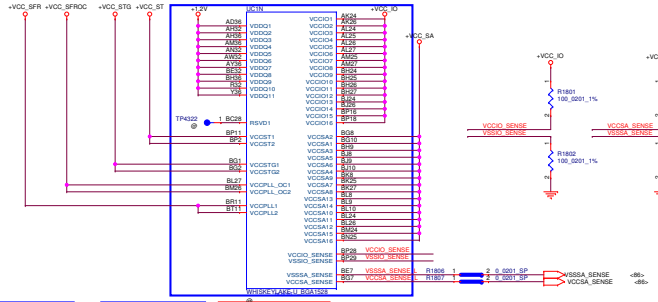


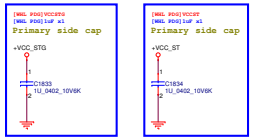


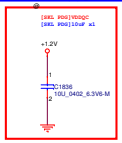


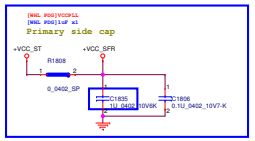




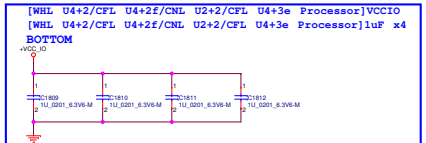
Power Rail	Description	Control
VCC	Processor IA Cores Power Rail	SVID
VccGT	Processor Graphics Power Rails	SVID
VccGTX	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
VccSA	System Agent Power Rail	SVID
VccIO	IO Power Rail	Fixed
VccST	Sustain Power Rail	Fixed
VccPLL	Processor PLLs power rail	Fixed
VDDQ	Integrated Memory Controller Power Rail	Fixed
VccOPC	Processor OPC power rail (available only in SKU' s with OPC)	Fixed
VccOPC_1P8	Processor OPC power rail (available only in SKU' s with OPC)	Fixed
VccEOPIO	Processor OPC power rail (available only in SKU' s with OPC)	Fixed

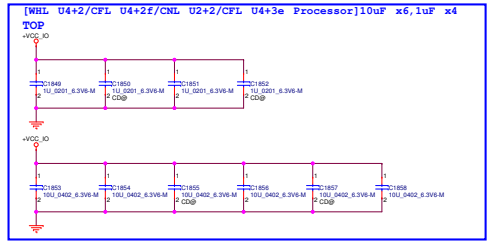


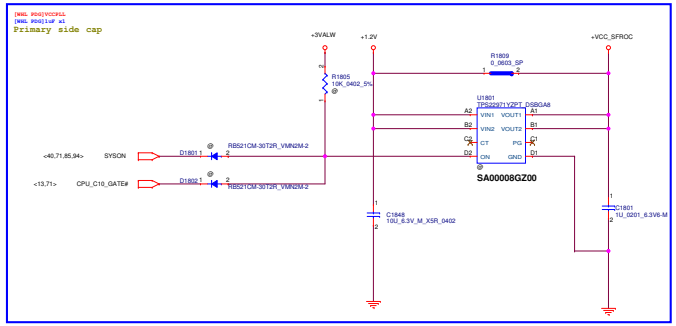




The following capacitors can be placed on as either Primary or back side cap.







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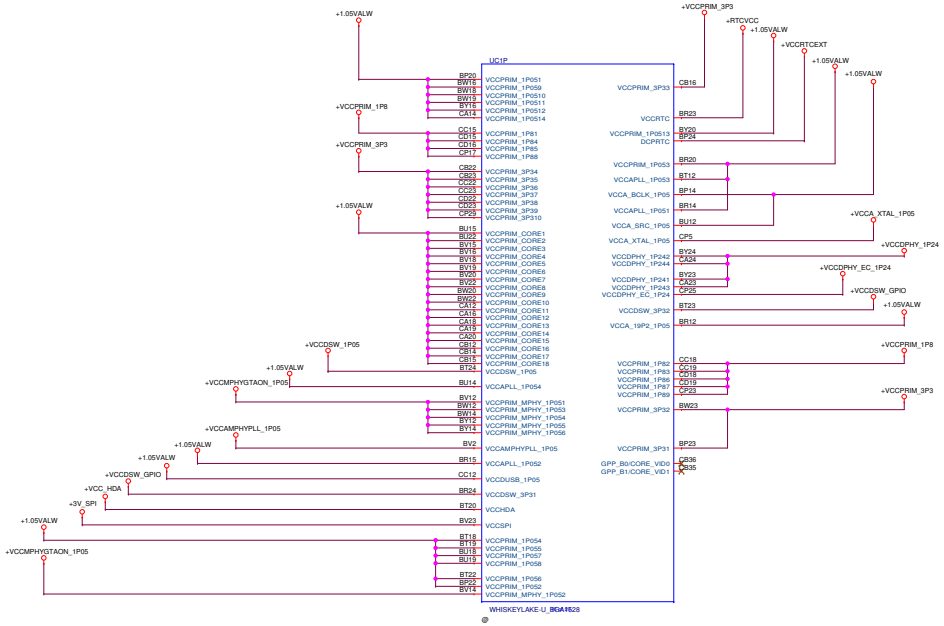


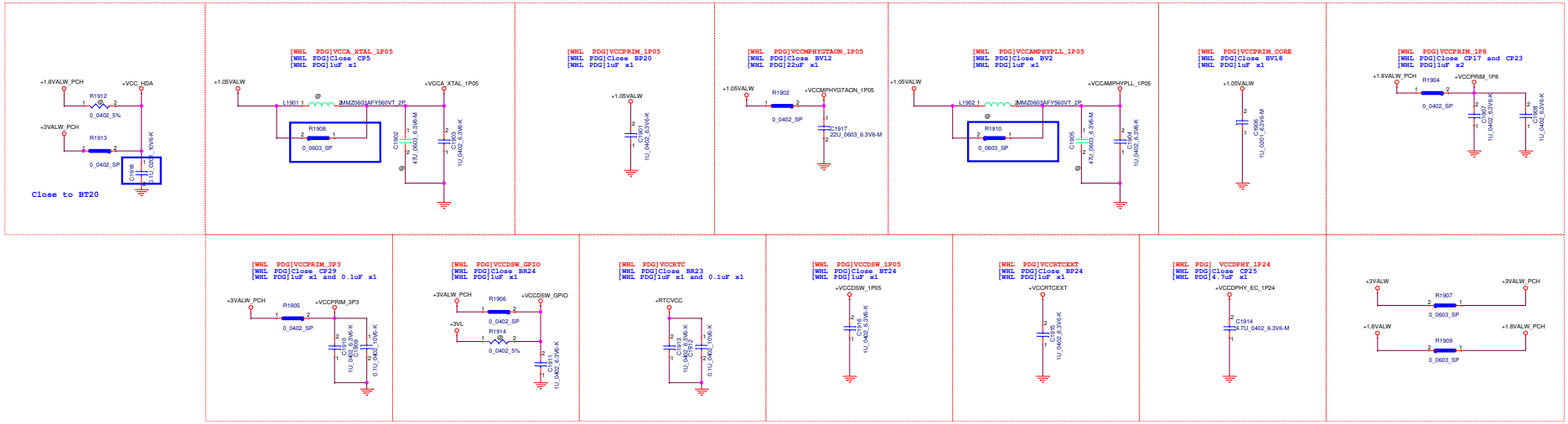
Table 10-9. Other DC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Notes
VCCPRIM_1p05	Core Logic, Ungated SRAM, I/O Blocks, USB AFE, Processor Sideband, JTAG, Thermal Sensor, MIPI* DPHY Primary WellSP	0.9975	1.05	1.1025	V	1

Table 10-9. Other DC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Notes
VCCPRIM_1P8	1.8V Primary Well	1.71	1.8	1.89	V	1
VCCPRIM_3P3	3.3V Primary Well	3.13	3.3	3.46	V	1
VCCPRIM_CORE	Core Logic Primary Well	0.9975	1.05	1.1025	V	1
VCCAMPHYPLL_1p05	Analog Supply for USB 3.0, PCIe Gen2 / Gen 3, and SATA PLL Primary Well	0.9975	1.05	1.1025	V	1
VCCAPLL_1p05	Analog Supply for OPI, USB 2.0 and Audio PLL Primary Well	0.9975	1.05	1.1025	V	1
VCCSPI (3.3V)	SPI Primary Well - 3.3V	3.13	3.3	3.46	V	1
VCCSPI (1.8V)	SPI Primary Well - 1.8V	1.71	1.8	1.89	V	1
VCCHDA (3.3V)	Intel® HD Audio Supply Primary Well_1	3.13	3.3	3.46	V	1
VCCHDA (1.8V)	Intel® HD Audio Supply Primary Well_2	1.71	1.8	1.89	V	1
VCCHDA (1.5V)	Intel® HD Audio Supply Primary Well_3	1.425	1.5	1.575	V	1
VCCDSW_3p3	Deep Sx Well for GPD and USB 2.0	3.13	3.3	3.46	V	1
VCCRTC	RTC Well Supply	2.0	3.0	3.465	V	1,2

Notes:
1. The I/O buffer supply voltage is measured at the PCH package pins. The tolerances shown in Table 10-9, "Other DC Characteristics" are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a roll off of 3db/decade above 20 MHz.
2. Maximum Crystal ESR is 50 kohm.



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Issued Date	2015/01/12	Deciphered Date	2016/01/12

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Title: WHL(O)_PW-OTHERS

Size	Document Number	Rev
Custom	EEA490/590 MM-B011	0.4

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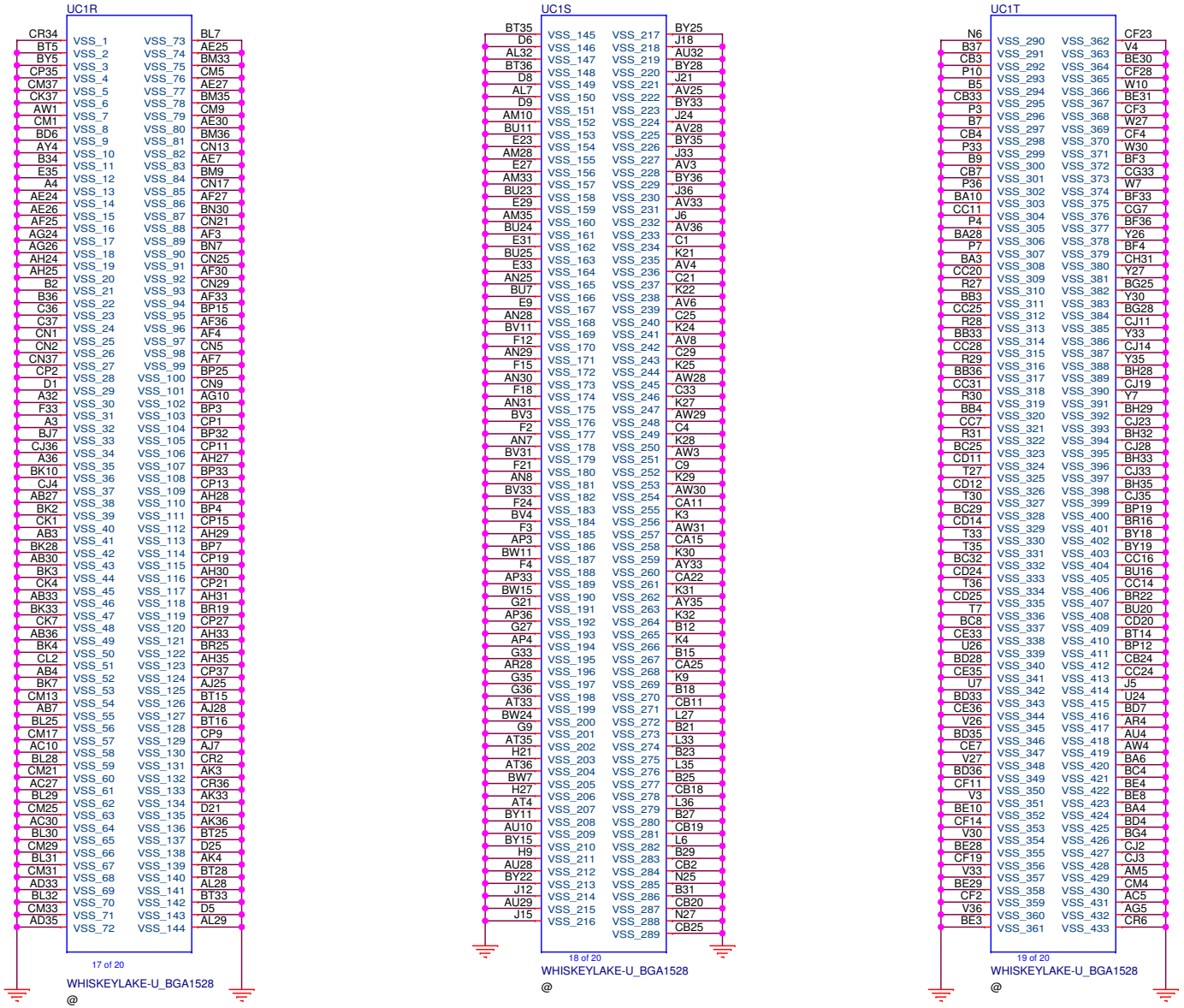

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: WHL(P/Q/R)_VSS

Size	Document Number	Rev
B	EE490/590 NM-B911	0.4

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+1.05VALW +1.05VALW <19,71,92>

+VCC_IO +VCC_IO <5,11,18,71>

CFG0 [SKL EDS]

+VCC_IO

R2101 1K_0402_5% @

CFG0

R2102 1K_0402_1% @

L:Stall.
*H:(Default) Normal Operation; No stall.

CFG4

+VCC_IO

R2103 1K_0402_5% @

CFG4

R2104 1K_0402_1%

*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

CFG3

PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)
0 : ENABLED
SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
1 : DISABLED

CFG3

R2108 1K_0402_1% @

DFXTESTMODE

+1.05VALW

R2106 1.5K_0402_5%

ITP_PMODE

R2110 1K_0402_1% @

HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED
WEAK INTERNAL PU

20180528
Change the Netname to +1.05VALW
Modified By Tony

[SKL CRB]

[SKL PDG]Route HOOK[6] to Skylake ITP_PMODE. Termination: Resistor value from 1K ohm to 3K ohm pull up to PCH_V1.0A Rail.

UC1O

CFG0 T4 CFG_0
CFG3 R3 CFG_3
CFG4 J4 CFG_4
M4 CFG_5
J3 CFG_6
M3 CFG_7
R2 CFG_8
N2 CFG_9
R1 CFG_10
N1 CFG_11
J2 CFG_12
L2 CFG_13
J1 CFG_14
L1 CFG_15
L3 CFG_16
N3 CFG_18
L4 CFG_17
N4 CFG_19

R2105 2 1 49.9_0402_1% CFG_RCOMP AB5 CFG_RCOMP

ITP_PMODE W4 ITP_PMODE

@ TP24 1 CG2 RSVD25
@ TP26 1 CG1 RSVD24

@ TP74 1 H4 RSVD34
@ TP30 1 H3 RSVD33

@ TP86 1 BV24 RSVD22
@ TP85 1 BV25 RSVD23

@ TP88 1 G3 RSVD69
@ TP87 1 G4 RSVD70

@ TP90 1 BK36 RSVD17
@ TP89 1 BK35 RSVD16

@ TP32 1 W3 RSVD35
@ TP91 1 AM4 RSVD7

@ TP92 1 AM3 RSVD71

@ TP93 1 A35 RSVD1
@ TP94 1 D34 RSVD30

@ TP95 1 G2 RSVD32
@ TP96 1 G1 RSVD31

RSVD_TP5 F37 1 TP37 @
RSVD_TP4 F34 1 TP39 @

IST_TRIG CP36 1 TP936 @
RSVD_TP3 CN36 1 TP97 @

RSVD72 BJ36 1 TP43 @
RSVD73 BJ34 1 TP45 @

TP1 BK34 1 TP49 @
TP3 BR18 1 TP51 @

RSVD74 BT9 1 TP59 @
RSVD75 BT8 1 TP60 @

RSVD76 BP8 1 TP22 @
RSVD77 BP9 1 TP23 @

RSVD29 CR4 1 TP25 @

RSVD26 CP3 1 TP27 @
RSVD27 CR3 1 TP64 @

RSVD78 AU3 1 TP66 @
RSVD79 AT3 1 TP29 @

RSVD8 AN1 1 TP31 @
RSVD9 AN2 1 TP33 @

RSVD11 AN4 1 TP34 @
RSVD10 AN3 1 TP35 @

RSVD80 AL2 1 TP67 @
RSVD81 AL1 1 TP68 @

RSVD82 AL4 1 TP54 @
RSVD83 AL3 1 TP927 @

TP2 BP34 1 TP928 @
VSS_392 BP36
TP5 BP35 1 TP929 @

RSVD68 C34 1 TP930 @

RSVD_TP1 A34 1 TP931 @
RSVD67 B35 1 TP932 @

RSVD84 CR35 1 TP933 @

RSVD66 AH26 1 TP934 @
RSVD85 AJ27 1 TP935 @

SKTOCC# E1

R2107 1 2 0_0402_SP

R2109 1 2 0_0402_SP

WHISKEYLAKE_U_BGA1528

@

TABLE

CFG0 : Stall Reset Sequence
after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled

[SKL EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM# state	VCCOPC
0V	0V
1V	1V

[SKL EDS]Minimum Speed Mode: VCCEOPIO can be connected to OPC VR in this case VCCEOPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal .
In order to achieve better power/performance it is recommended to use a separate VR for VCCEOPIO in this case VCCEOPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEOPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EOPIO interface as shown below:

ZVM# state	MSM# state	VCCEOPIO
0V	X	0V
1V	0V	0.8V
1V	1V	1V

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: WHL(S)_CFG/ RSVD

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

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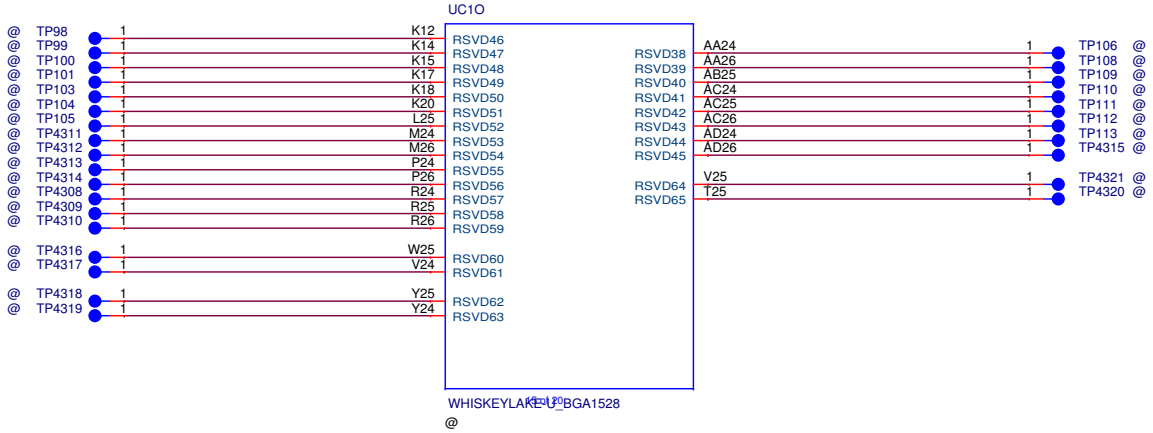

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: WHL(T)_RSVD

Size: B	Document Number: EE490/590 NM-B911	Rev: 0.4
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+3VS +3VS <5,9,10,11,12,14,15,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

+2.5V +2.5V <6,24,25,26,94>

+1.2V +1.2V <6,7,18,24,25,26,85>

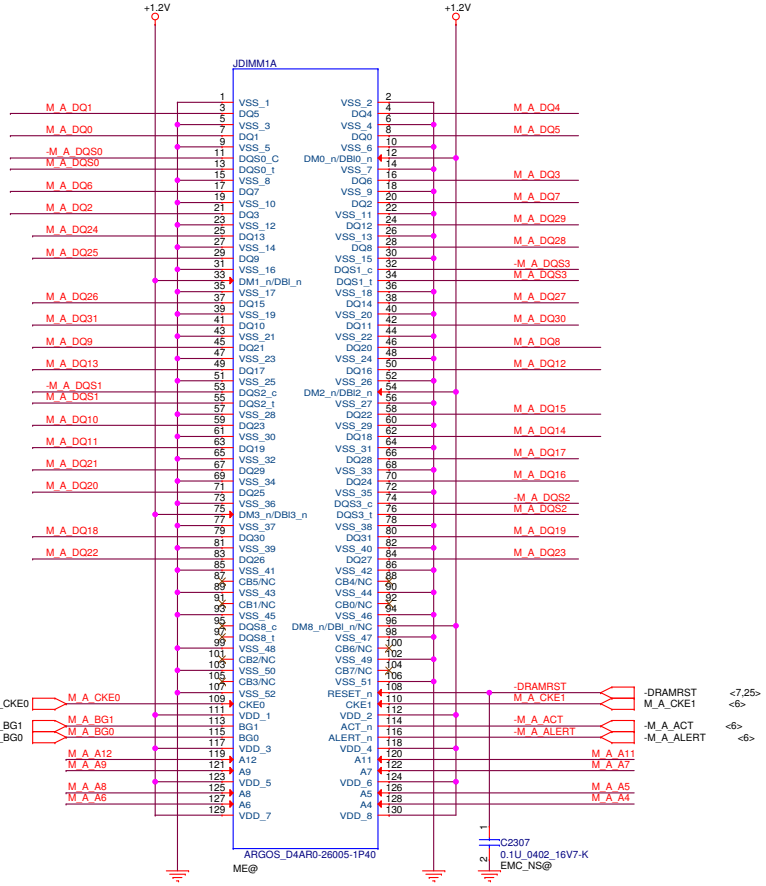
+0.6VS +0.6VS <24,25,26,85>

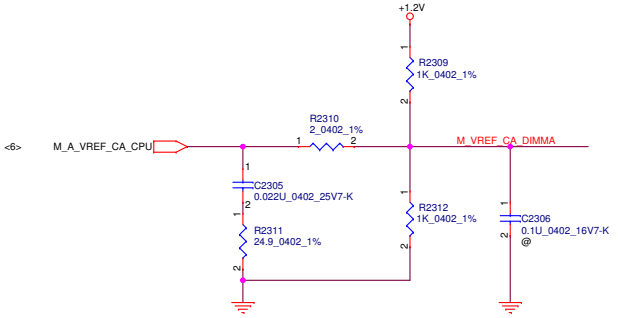
<6,7> M_A_DQ[63:0]

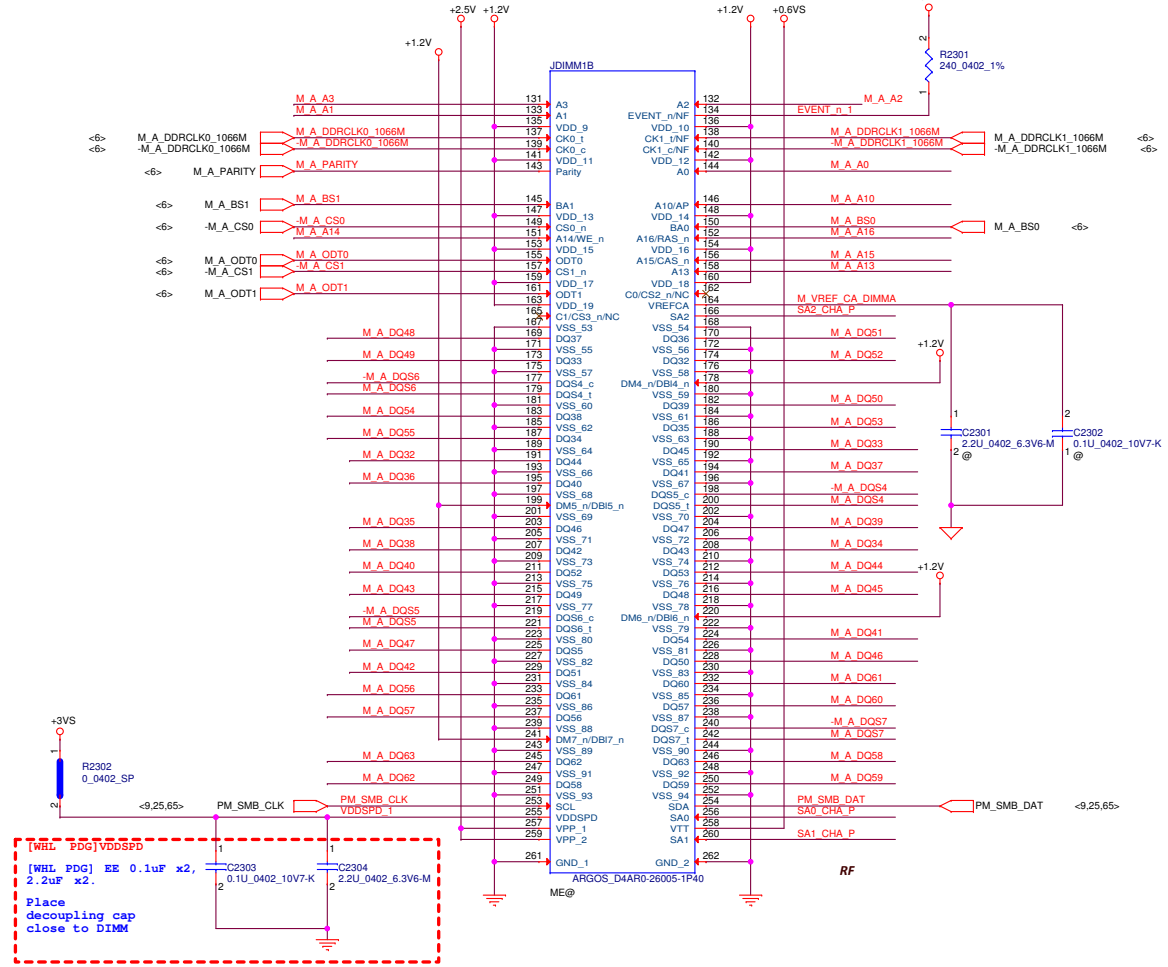
<6,7> -M_A_DQS[7:0]

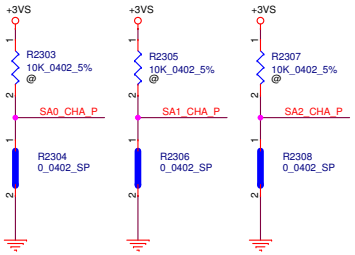
<6,7> M_A_DQS[7:0]

<6> M_A_A[16:0]









SPD Address = 0H

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: DDR4 CH-A PRIMARY

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

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+2.5V +2.5V <6,23,25,26,94>

+1.2V +1.2V <6,7,18,23,25,26,85>

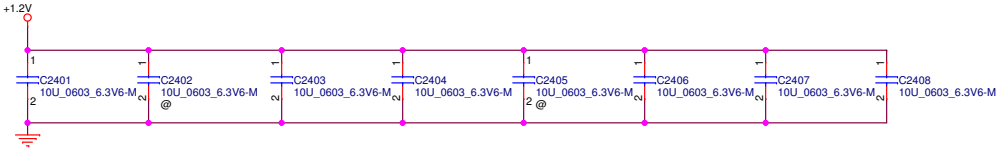
+0.6VS +0.6VS <23,25,26,85>

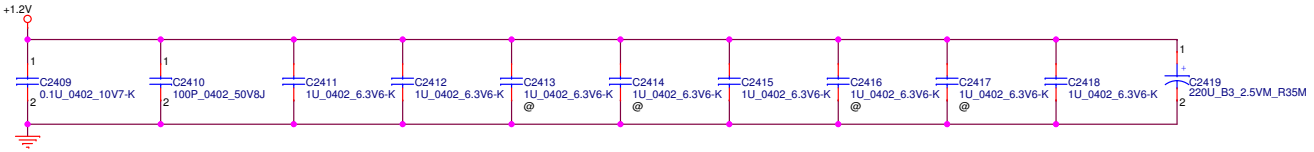
[WHL PDG]VDDQ

[WHL PDG] EE 10uF x16, 1uF x16. 330uF x1

Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

Total quantity is referring to 2 channels.



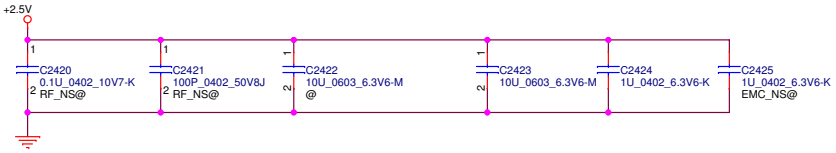


10U x 6
0.1U x 2
1U x 4
220U x 1

[WHL PDG]VPP

[WHL PDG] EE 10uF x2, 1uF x2.

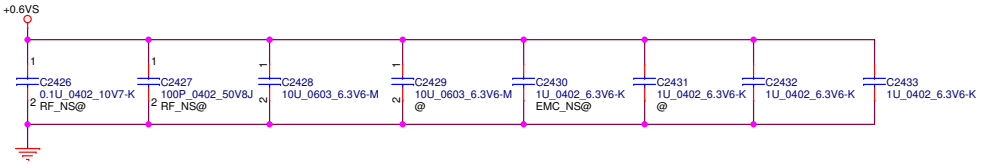
Place decoupling cap on DRAM side.



10U x 1
1U x 1

[WHL PDG]VTT

[WHL PDG] EE 10uF x2, 1uF x4.



10U x 1
1U x 2

Place decoupling on the VTT plane close to SODIMM

Total
10U x 8
0.1U x 2
1U x 7
220U x 1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DDR4 CH-A PRIMARY_P

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+3VS +3VS <5,9,10,11,12,14,15,23,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

+2.5V +2.5V <6,23,24,26,94>

+1.2V +1.2V <6,7,18,23,24,26,85>

+0.6VS +0.6VS <23,24,26,85>

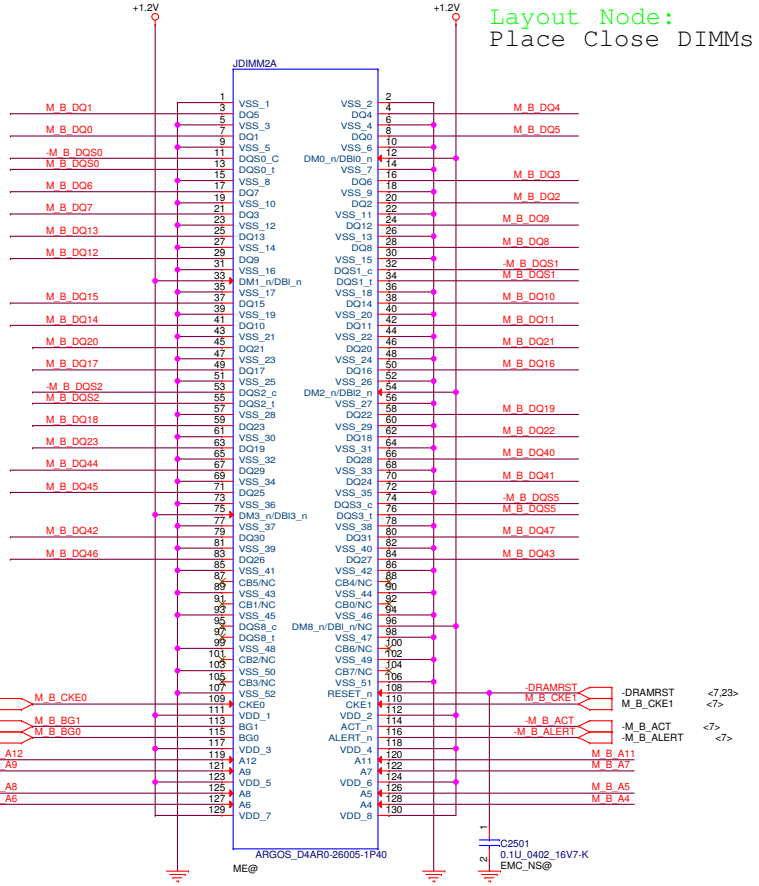
<6,7> M_B_DQ[63:0]

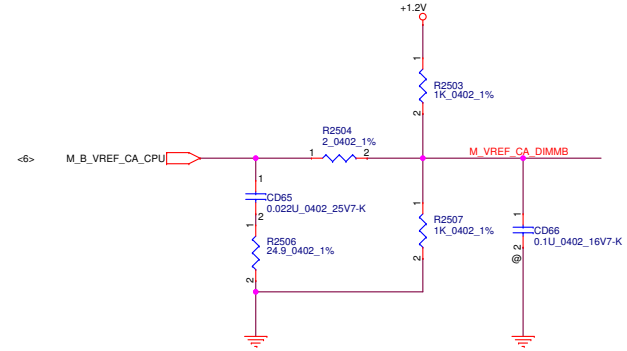
<6,7> -M_B_DQS[7:0]

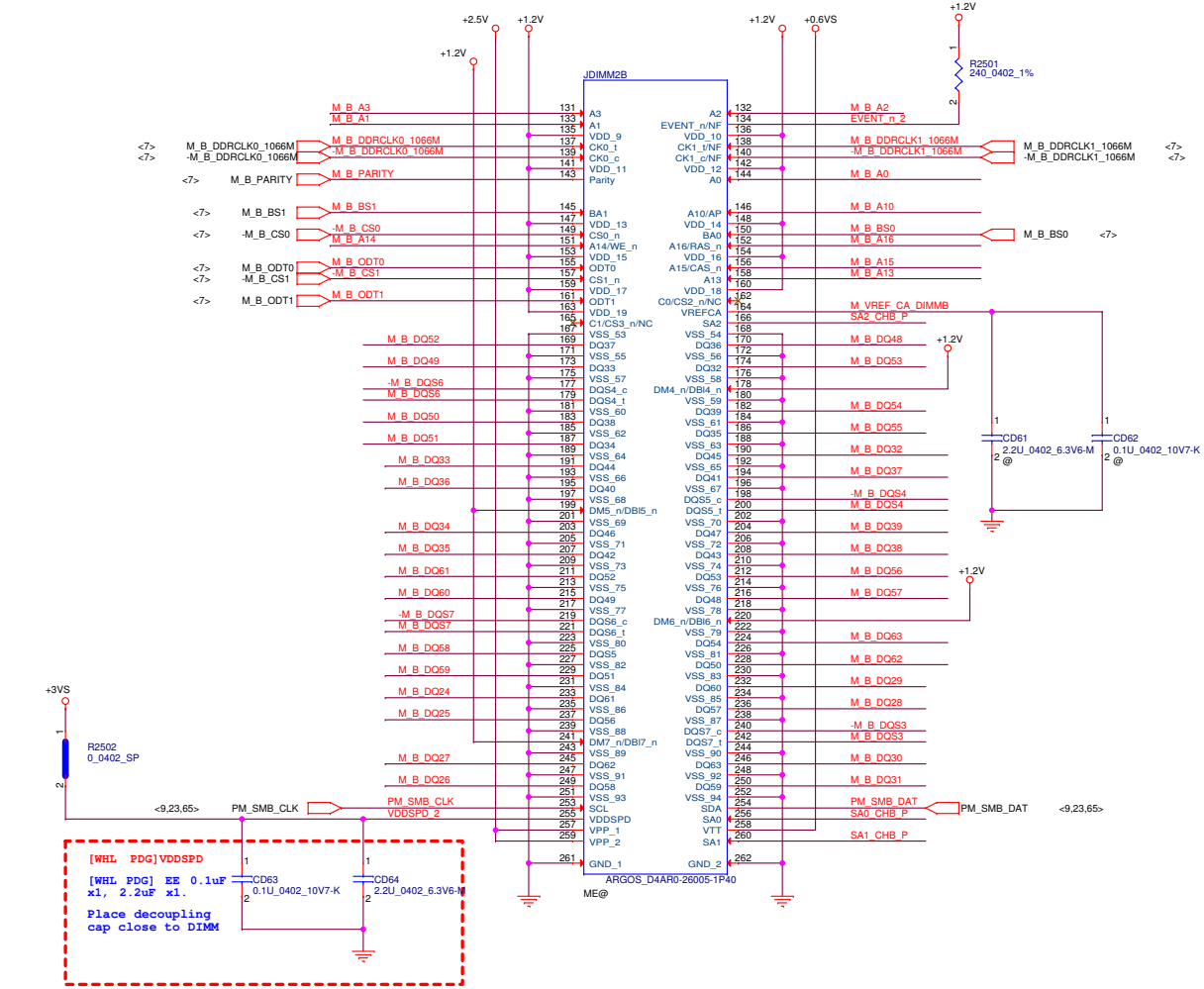
<6,7> M_B_DQS[7:0]

<7> M_B_A[16:0]

Layout Node:
Place Close DIMMs







Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: DDR4 CH-B PRIMARY

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

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+2.5V +2.5V <6,23,24,25,94>

+1.2V +1.2V <6,7,18,23,24,25,85>

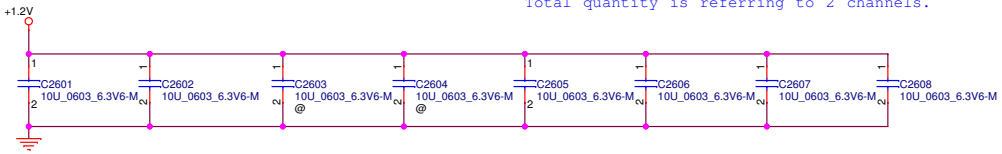
+0.6VS +0.6VS <23,24,25,85>

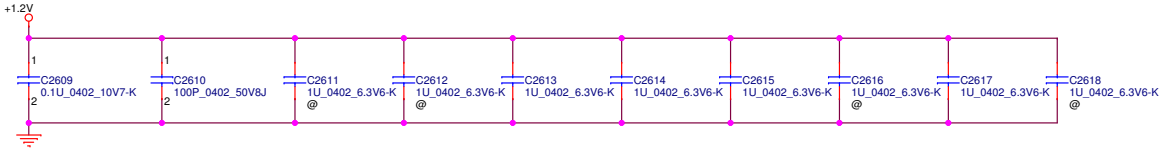
[WHL PDG]VDDQ

[WHL PDG] EE 10uF x16, 1uF x16. 330uF x1

Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

Total quantity is referring to 2 channels.



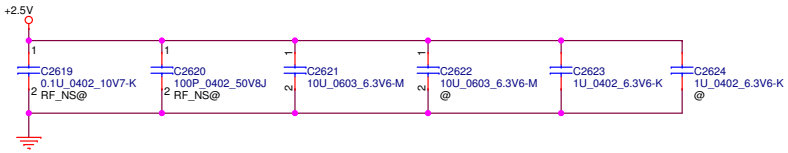


10U x 6
0.1U x 2
1U x 4

[WHL PDG]VPP

[WHL PDG] EE 10uF x2, 1uF x2.

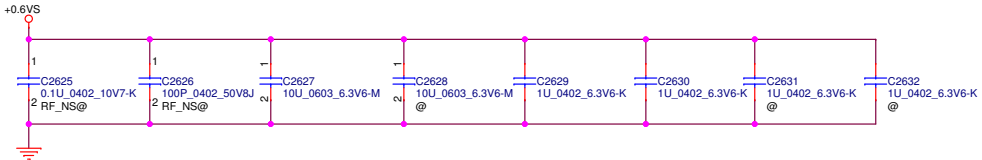
Place decoupling cap on DRAM side.



10U x 1
1U x 1

[WHL PDG]VTT

[WHL PDG] EE 10uF x2, 1uF x4.



10U x 1
1U x 2

Place decoupling on the VTT plane close to SODIMM

Total
10U x 8
0.1U x 2
1U x 7

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DDR4 CH-B PRIMARY_P

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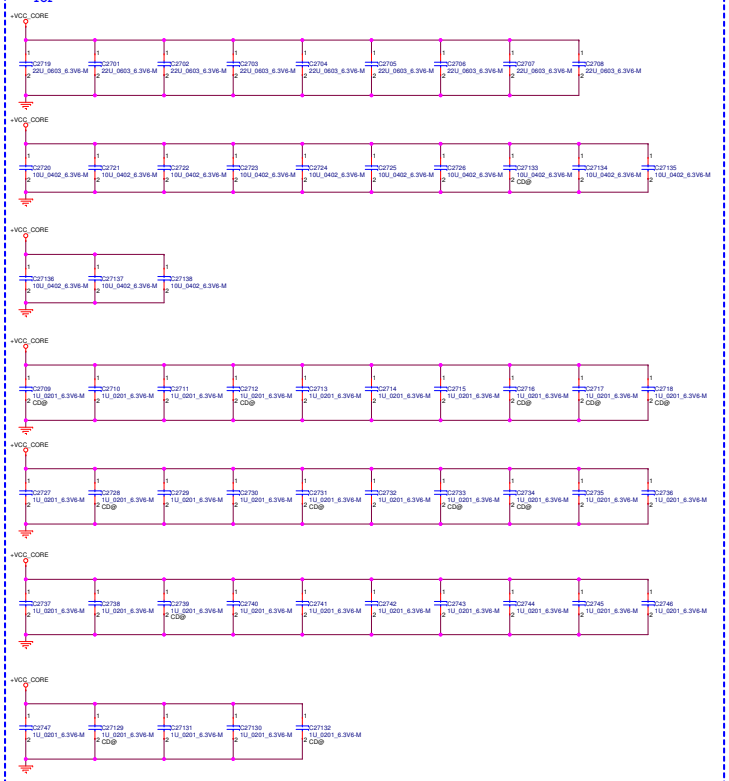
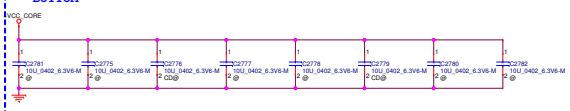
+VCC_CORE +VCC_CORE <16,17,87,90> +VCC_GT +VCC_GT <17,88,90> +VCCCPUCORE_GT +VCCCPUCORE_GT <17>

[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]VCC
[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]22uF x9,10uF x22,1uF x35,47uF x18

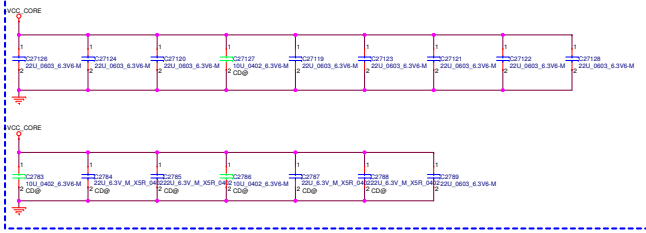
[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]10uF x14,1uF x35,22uF x9
TOP



[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]10uF x8
BOTTOM

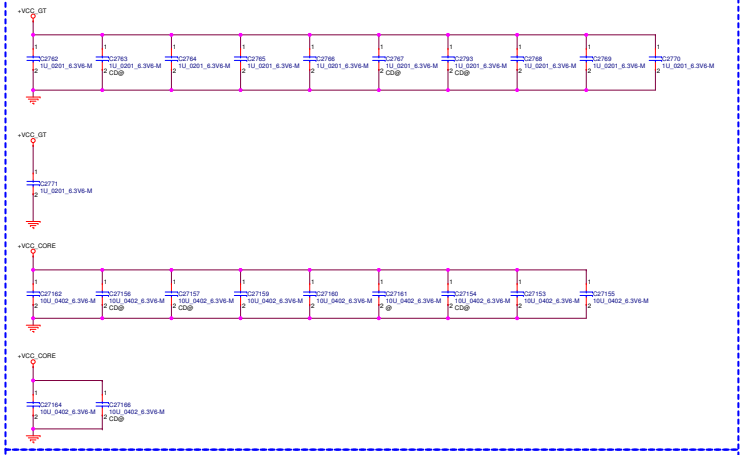


[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]47uF x18
The following capacitors can be placed on as either Primary or back side cap.

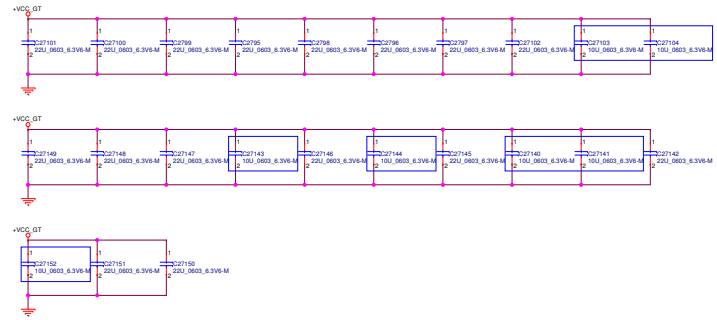


[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]VCCGT
[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]22uFx 15,10uF x15,1uF x11, 47uF x8

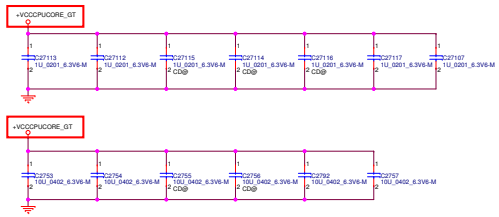
[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]10uF x15,1uF x11
TOP



[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]22uF x15,47uF x8
BOTTOM



[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]VCCcore_VCCGT_ISLAND
[WHL U4+2/CFL U4+2f/CNL U2+2/CFL U4+3e Processor]1uF x7,10uF x7
TOP



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: VCC_CORE & VCC_GT CAP

Size: D | Document Number: KX490/590 NM-B011 | Rev: 0.4

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

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Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

BLANK

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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+3VS <5,9,10,11,12,14,15,23,25,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

+3VS_VGA <32,37,38,39,91>

+1.8VS_VGA <32,34,38>

TABLE of GPU (UV3001)		
Vendor	LCFC P/N	Description
AMD(R17M-P1-70)	SA00008ED00	S IC 216-0905004 C0 FCBGA 769P GPU
AMD(R17M-P1-50)	SA00008DT10	S IC 216-0905018 C3 FCBGA 769P GPU

<12> PCIE_CTX_C_GRX_N[0..3] → PCIE_CTX_C_GRX_N[0..3]

<12> PCIE_CTX_C_GRX_P[0..3] → PCIE_CTX_C_GRX_P[0..3]

<12> PCIE_CRX_GTX_N[0..3] → PCIE_CRX_GTX_N[0..3]

<12> PCIE_CRX_GTX_P[0..3] → PCIE_CRX_GTX_P[0..3]

DIS@ support GEN3

UV3001B@ symbol2

PCIE_CTX_C_GRX_P0	AT41	PCIE_RX0P	PCIE_TX0P	AV35	PCIE_CRX_C_GTX_P0	C3008 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P0
PCIE_CTX_C_GRX_N0	AT40	PCIE_RX0N	PCIE_TX0N	AU35	PCIE_CRX_C_GTX_N0	C3001 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N0
PCIE_CTX_C_GRX_P1	AR41	PCIE_RX1P	PCIE_TX1P	AU38	PCIE_CRX_C_GTX_P1	C3002 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P1
PCIE_CTX_C_GRX_N1	AR40	PCIE_RX1N	PCIE_TX1N	AU39	PCIE_CRX_C_GTX_N1	C3003 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N1
PCIE_CTX_C_GRX_P2	AP41	PCIE_RX2P	PCIE_TX2P	AR37	PCIE_CRX_C_GTX_P2	C3004 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P2
PCIE_CTX_C_GRX_N2	AP40	PCIE_RX2N	PCIE_TX2N	AR38	PCIE_CRX_C_GTX_N2	C3005 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N2
PCIE_CTX_C_GRX_P3	AM41	PCIE_RX3P	PCIE_TX3P	AN37	PCIE_CRX_C_GTX_P3	C3006 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P3
PCIE_CTX_C_GRX_N3	AM40	PCIE_RX3N	PCIE_TX3N	AN38	PCIE_CRX_C_GTX_N3	C3007 DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N3
	AL41	PCIE_RX4P	PCIE_TX4P	AL37				
	AL40	PCIE_RX4N	PCIE_TX4N	AL38				
	AK41	PCIE_RX5P	PCIE_TX5P	AJ37				
	AK40	PCIE_RX5N	PCIE_TX5N	AJ38				
	AJ41	PCIE_RX6P	PCIE_TX6P	AG37				
	AJ40	PCIE_RX6N	PCIE_TX6N	AG38				
	AH41	PCIE_RX7P	PCIE_TX7P	AE37				
	AH40	PCIE_RX7N	PCIE_TX7N	AE38				
CLK_PCIE_VGA	AV33	PCIE_REFCLKP	PERSTB	AV41	PLT_RST_VGA#			
CLK_PCIE_VGA#	AU33	PCIE_REFCLKN	PX_EN	AC41	PX_EX	R3006 2 DIS@ 1 1K_0402_5%		
			PCIE_ZVSS	AU41	PCIE_ZVSS	R3001 1 DIS@ 2 200_0402_1%		

<14> CLK_PCIE_VGA

<14> CLK_PCIE_VGA#

REV 0.91

216-0905018-C3_FCBGA769

+3VS_VGA

R3005 10K_0402_5% @

R3007 100K_0402_5% DIS@

JTAG

+1.8VS_VGA

R3016 10K_0402_5% DIS@

R3015 10K_0402_5% DIS@

TV52

TV53

R3014 1 DIS@ 2 33_0402_5%

R3013 1 DIS@ 2 33_0402_5%

UV3001A@ symbol1

AA38	BP_0	JTAG_TDO	AF41	JTAG_TDO	TV48
AA37	BP_1	JTAG_TDI	AD40	JTAG_TDI	TV49
		JTAG_TMS	AD41	JTAG_TMS	TV50
		JTAG_TCK	AE41	JTAG_TCK	TV51
B2	TEST6	TESTEN	AE40	TESTEN	
		JTAG_TRSTB	AF40	JTAG_TRSTB	

REV 0.91

216-0905018-C3_FCBGA769

R3012 10K_0402_5% DIS@

+3VS_VGA

R3009 1K_0402_5% @

R3008 1K_0402_5% DIS@

+3VS_VGA

R3010 10K_0402_5% DIS@

R3011 1K_0402_5% @

<15,40,58,63,67,69> PLT_RST#

<10> DGPU_HOLD_RST#

R3004 1 2 0_0402_SP

R3002 0_0402_5% 1 @ 2

+3VS

U3003

1	B	VCC	5
2	A		
3	GND	Y	4

74LVC1G08GW_SOT353-1-5

DIS@

SA00005U300

PD 10K at GPU Pin

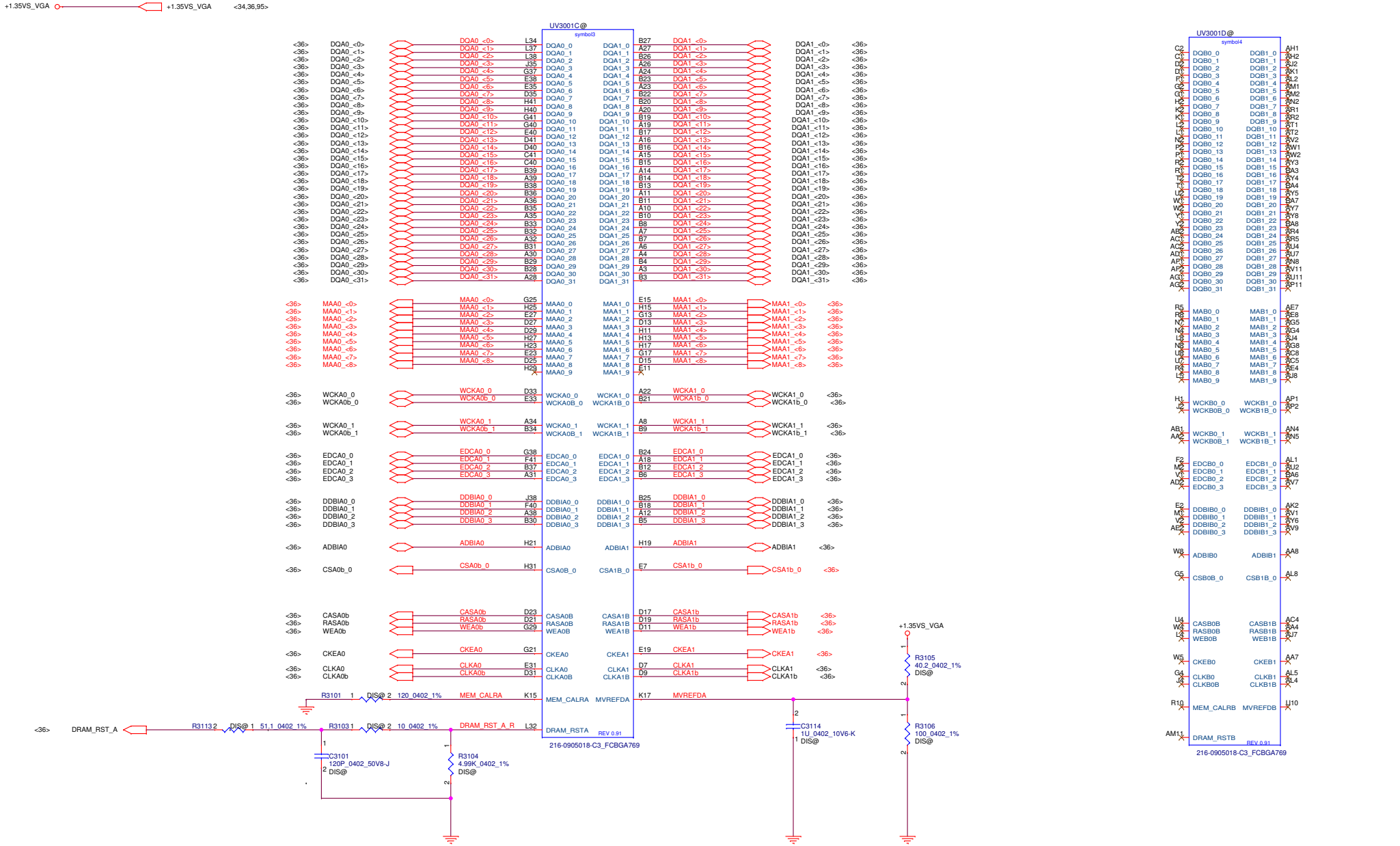
PLT_RST_VGA# <32,91>

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-P1-50(A)_PCIE

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

Date: Friday, September 14, 2018 | Sheet 30 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	R17M-P1-50(B)_VRAM I/F		
Size: Custom	Document Number: EE490/590 NM-B911		Rev: 0.4
Date: Friday, September 14, 2018	Sheet 31 of 99		

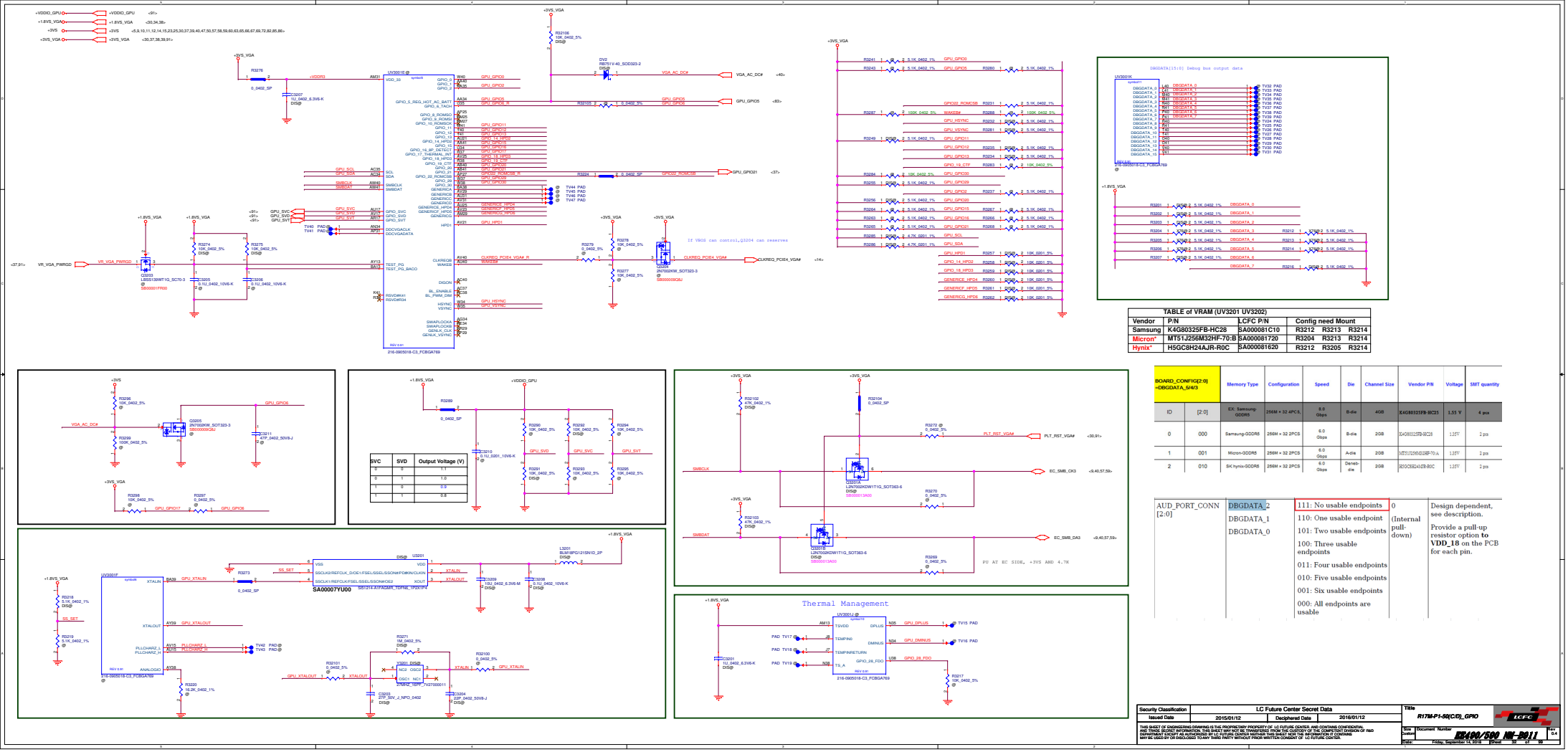


TABLE of VRAM (UV3201 UV3202)			
Vendor	P/N	LCFC P/N	Config need Mount
Samsung	K4G80325FB-HC28	SA000081C10	R3212 R3213 R3214
Micron*	MT51J256M32HF-70:B	SA000081720	R3204 R3213 R3214
Hynix*	H5GC8H24AJR-R0C	SA000081620	R3212 R3205 R3214

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

BOARD_CONFIG[2:0] =DBGDATA_5/4/3		Memory Type	Configuration	Speed	Die	Channel Size	Vendor P/N	Voltage	SMT quantity
ID	[2:0]	EX: Samsung-GDDR5	256M x 32 4PCS,	8.0 Gbps	B-die	4GB	K4G80325FB-HC25	1.55 V	4 pcs
0	000	Samsung-GDDR5	256M x 32 2PCS	6.0 Gbps	B-die	2GB	K4G80325FB-HC28	1.35V	2 pcs
1	001	Micron-GDDR5	256M x 32 2PCS	6.0 Gbps	A-die	2GB	MT51J256M32HF-70:A	1.35V	2 pcs
2	010	SK hynix-GDDR5	256M x 32 2PCS	6.0 Gbps	Deneb-die	2GB	H5GC8H24AJR-R0C	1.35V	2 pcs

AUD_PORT_CONN [2:0]	DBGDATA_2 DBGDATA_1 DBGDATA_0	111: No usable endpoints 110: One usable endpoint 101: Two usable endpoints 100: Three usable endpoints 011: Four usable endpoints 010: Five usable endpoints 001: Six usable endpoints 000: All endpoints are usable	0 (Internal pull-down)	Design dependent, see description. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin.

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

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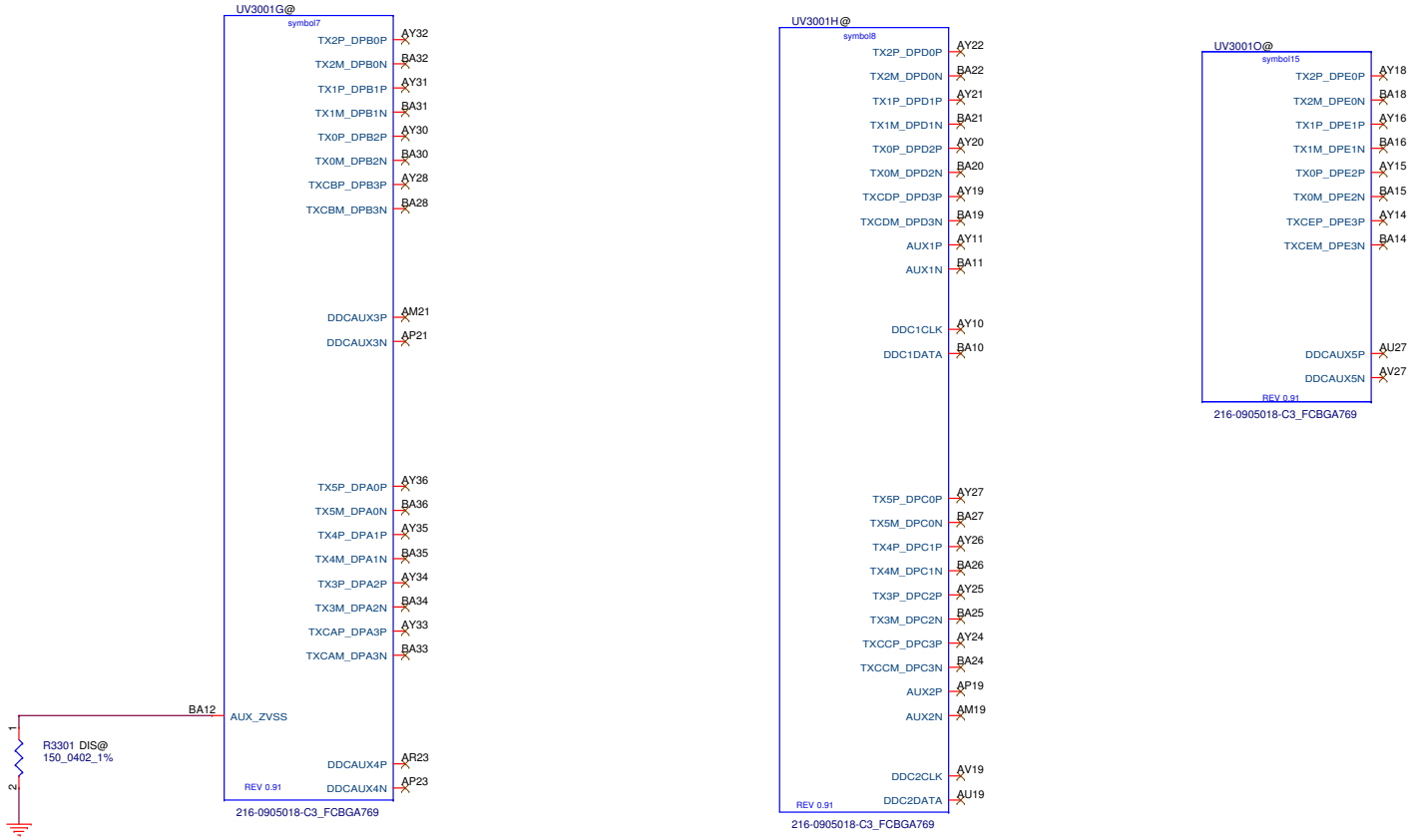
Title	R17M-P1-80(C/D)_GPIO		
Size: Custom	Document Number: R17M-P1-80(C/D)_MB_0.1		Rev: 0.4
Date: Friday, September 16, 2016	Sheet 32 of 89		



If this interface is not used, all signal outputs can be unconnected. AUX_ZVSS should always be connected.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-P1-50(E)_DIGITAL OU

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

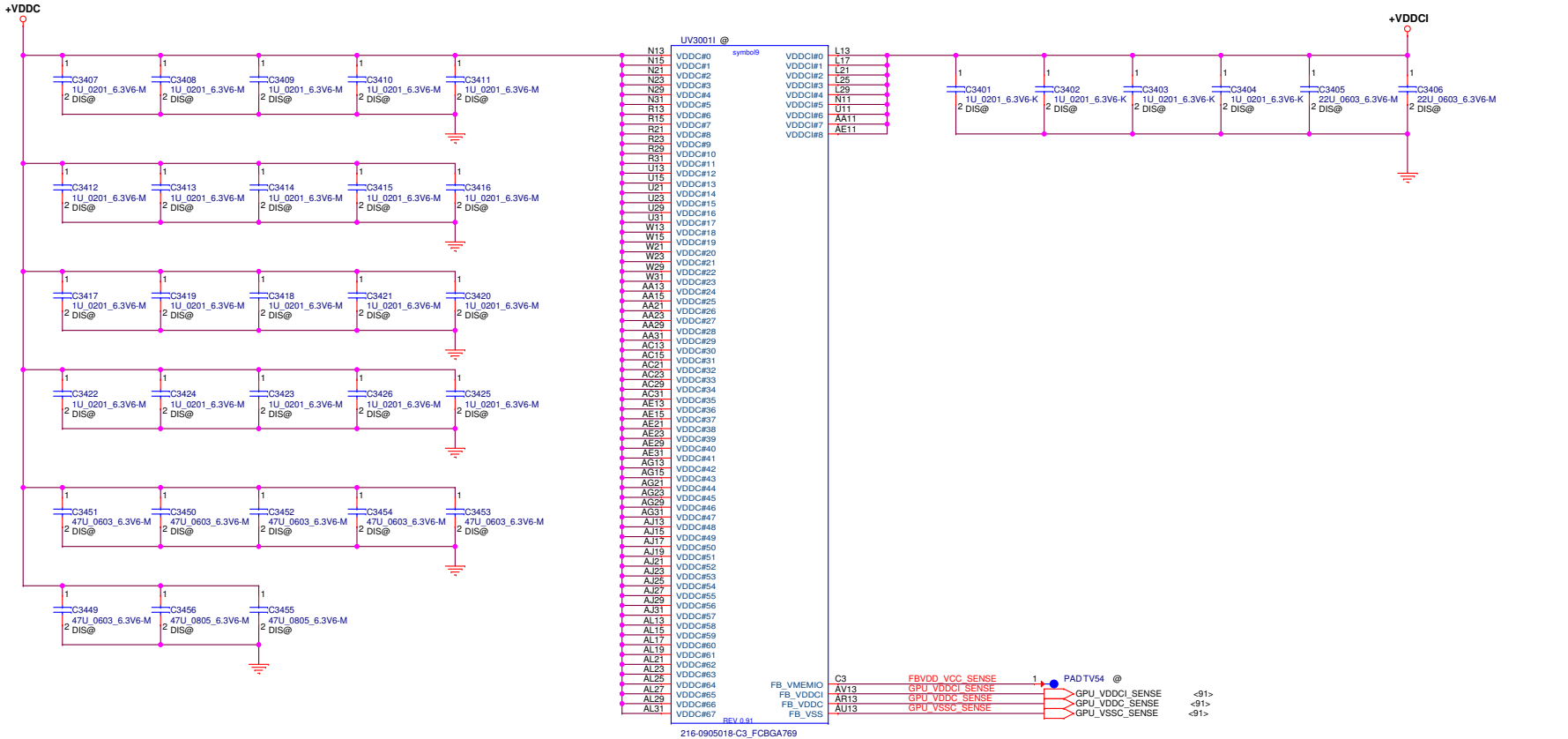
Date: Friday, September 14, 2018 Sheet 33 of 99

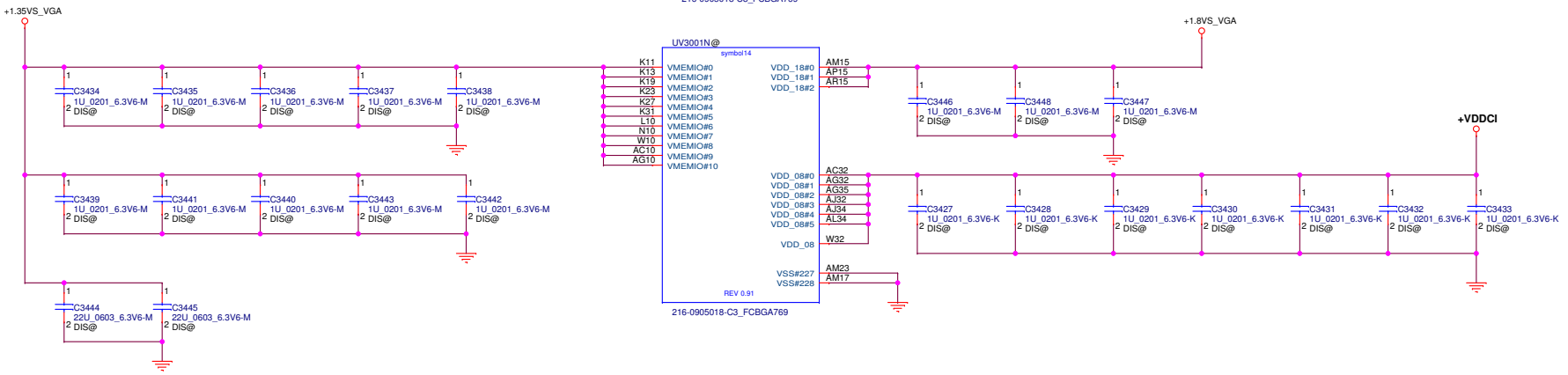
+VDDC —— +VDDC <91>

+VDDCI —— +VDDCI <91>

+1.35VS_VGA —— +1.35VS_VGA <31,36,95>

+1.8VS_VGA —— +1.8VS_VGA <30,32,38>



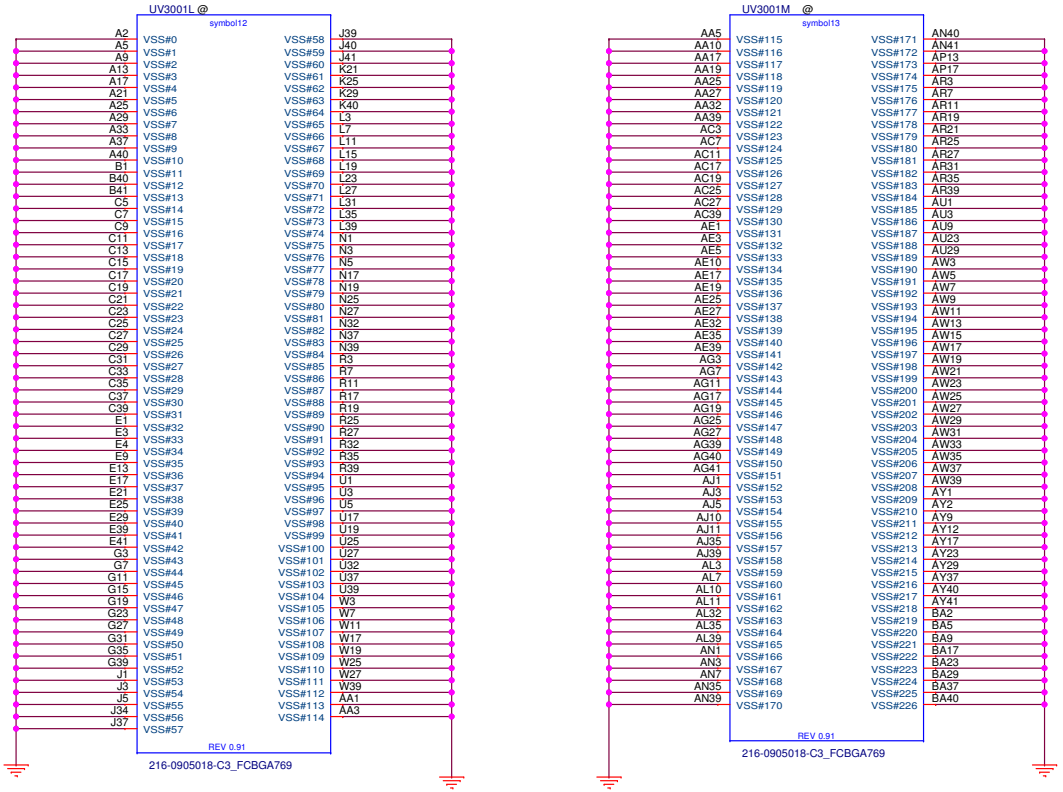


Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-P1-50(F)_PWR

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

Date: Friday, September 14, 2018 | Sheet 34 of 99

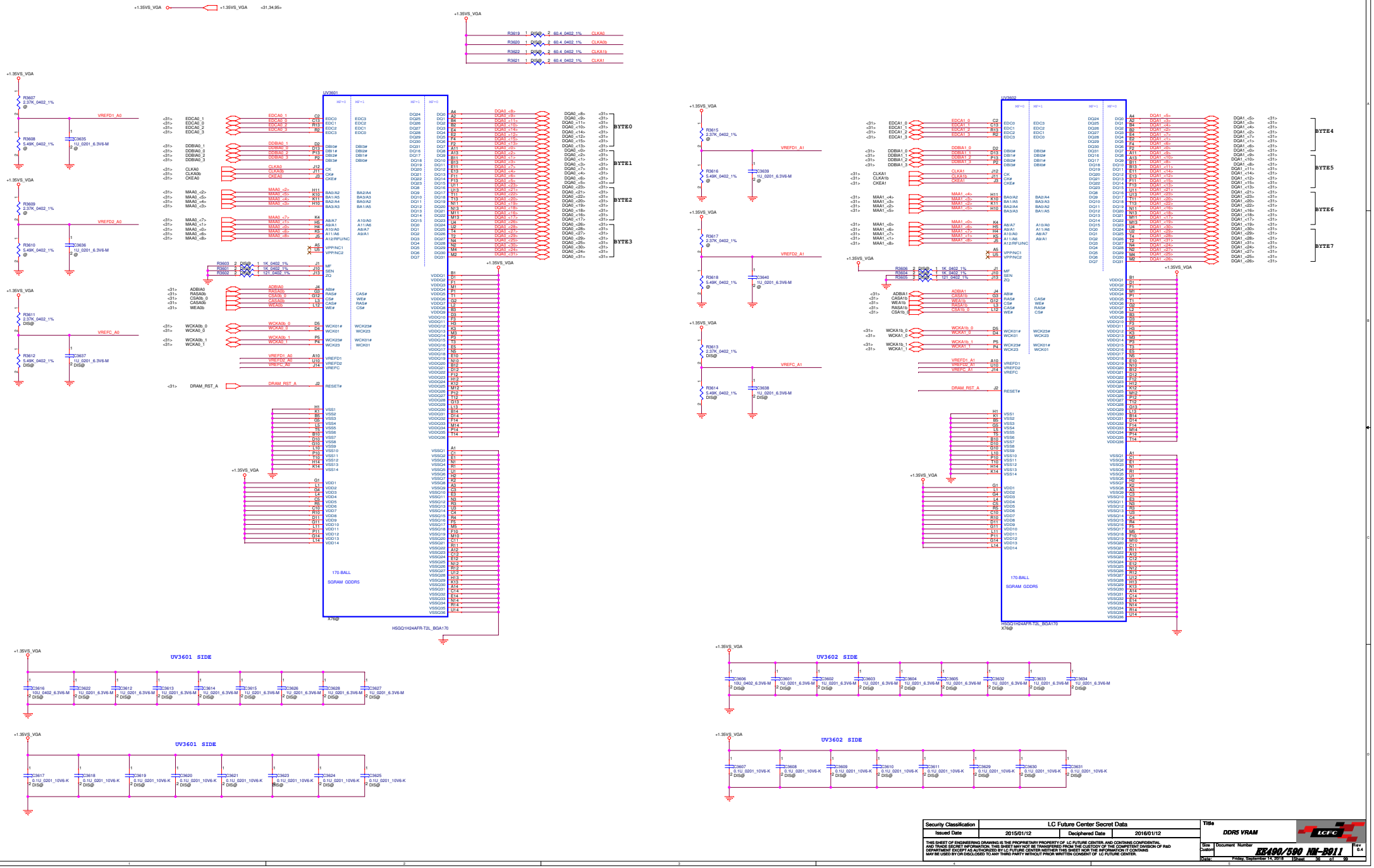


Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-P1-50(G)_VSS

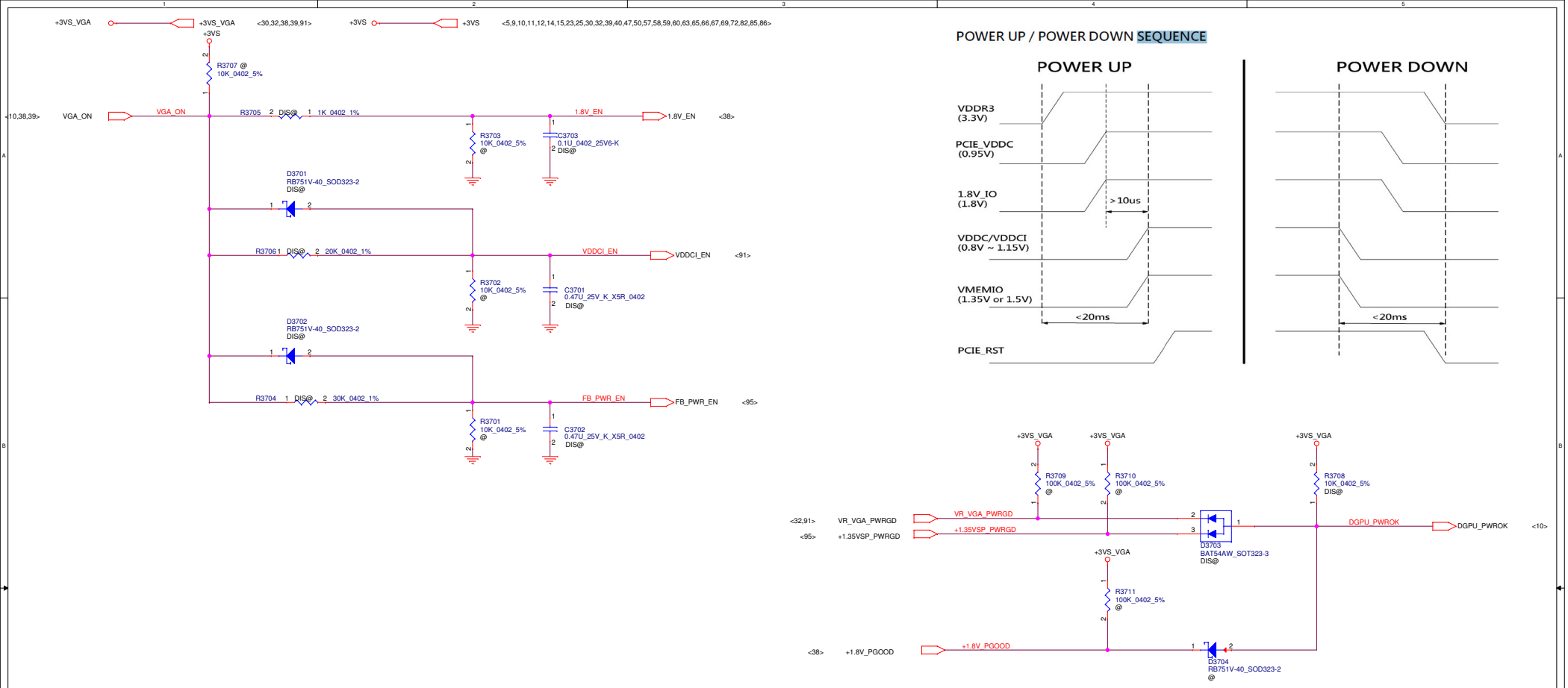
Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

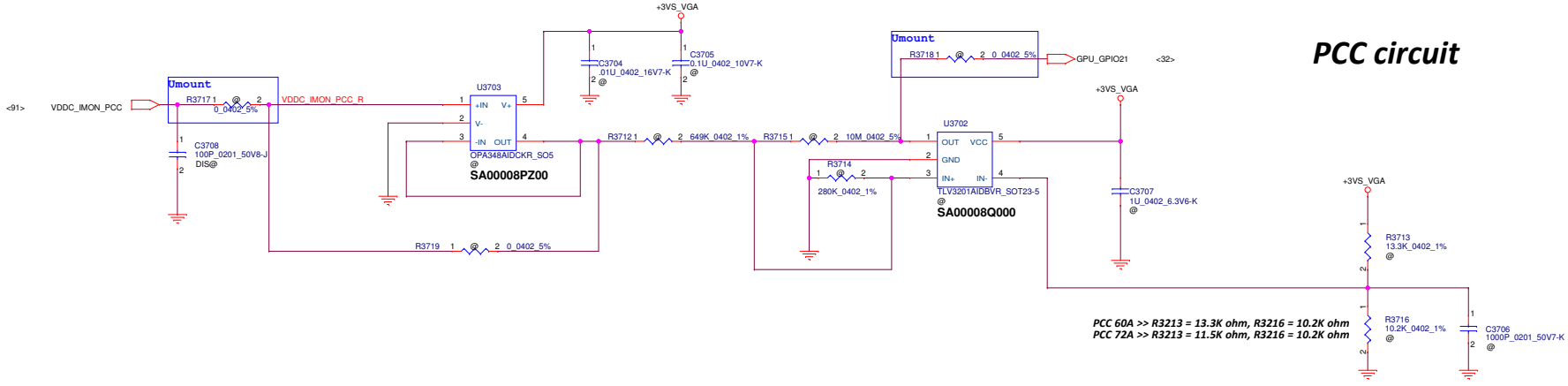
Date: Friday, September 14, 2018 Sheet 35 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	DDR5 VRAM		
Size: Custom	Document Number: EK490/590 NH-B011		Rev: 0.4
Date: Friday, September 14, 2018	Sheet 38 of 99		





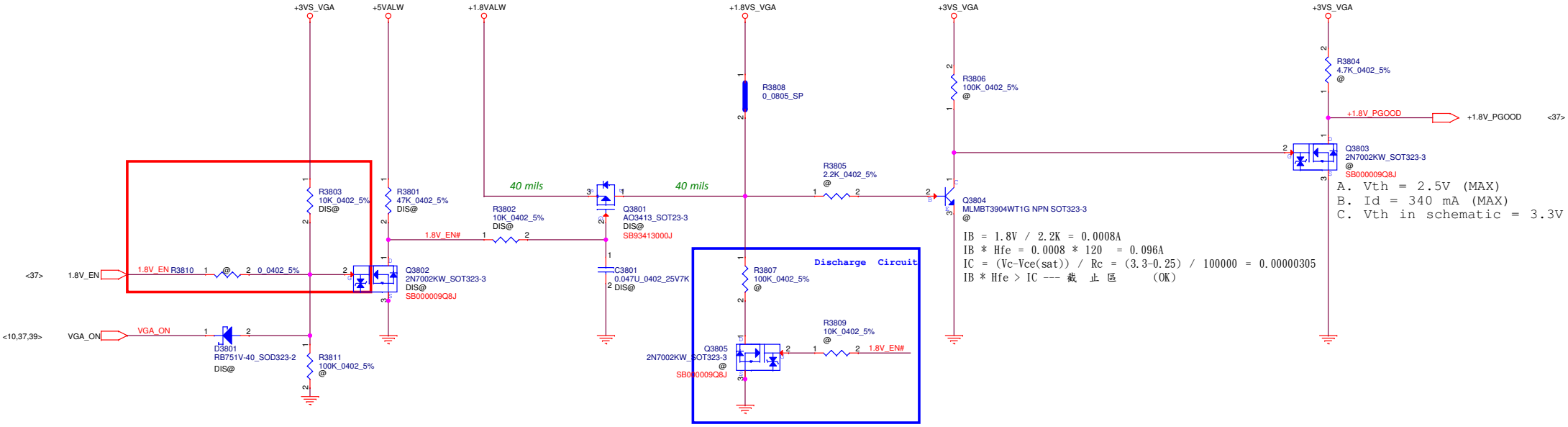
PCC circuit

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	R17M-P1-50_SEQ and PCC		
Size	Document Number		Rev
C	EE490/590 NM-B911		0.4
Date:	Friday, September 14, 2018	Sheet	37 of 99

+3VS_VGA +3VS_VGA <30,32,37,39,91>
+5VALW +5VALW <39,41,42,43,47,62,64,66,67,71,72,84,85,86,87,88,89,91,93,94>
+1.8VALW +1.8VALW <9,19,40,50,51,63,93>
+1.8VS_VGA +1.8VS_VGA <30,32,34>

+1.8VALW to +1.8VS_VGA



A. Vth = 2.5V (MAX)
B. Id = 340 mA (MAX)
C. Vth in schematic = 3.3V

IB = 1.8V / 2.2K = 0.0008A
IB * Hfe = 0.0008 * 120 = 0.096A
IC = (Vc-Vce(sat)) / Rc = (3.3-0.25) / 100000 = 0.00000305
IB * Hfe > IC --- 截 止 區 (OK)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DC V TO 1.5VS_VGA/1.8VS_VGA

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

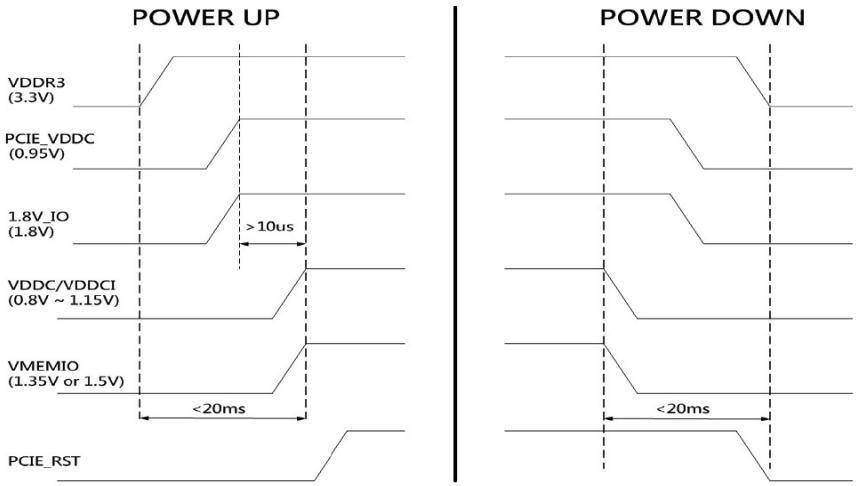
Date: Friday, September 14, 2018 Sheet 38 of 99

+3VS_VGA — +3VS_VGA <30,32,37,38,91>

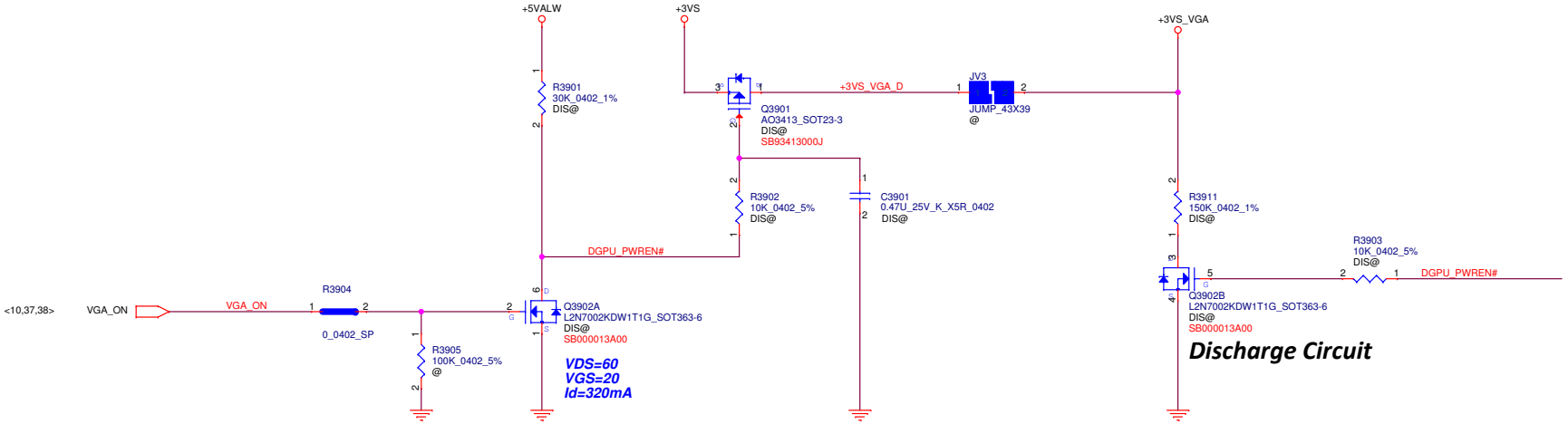
+5VALW — +5VALW <38,41,42,43,47,62,64,66,67,71,72,84,85,86,87,88,89,91,93,94>

+3VS — +3VS <5,9,10,11,12,14,15,23,25,30,32,37,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

POWER UP / POWER DOWN SEQUENCE



+3VS to +3VS_VGA

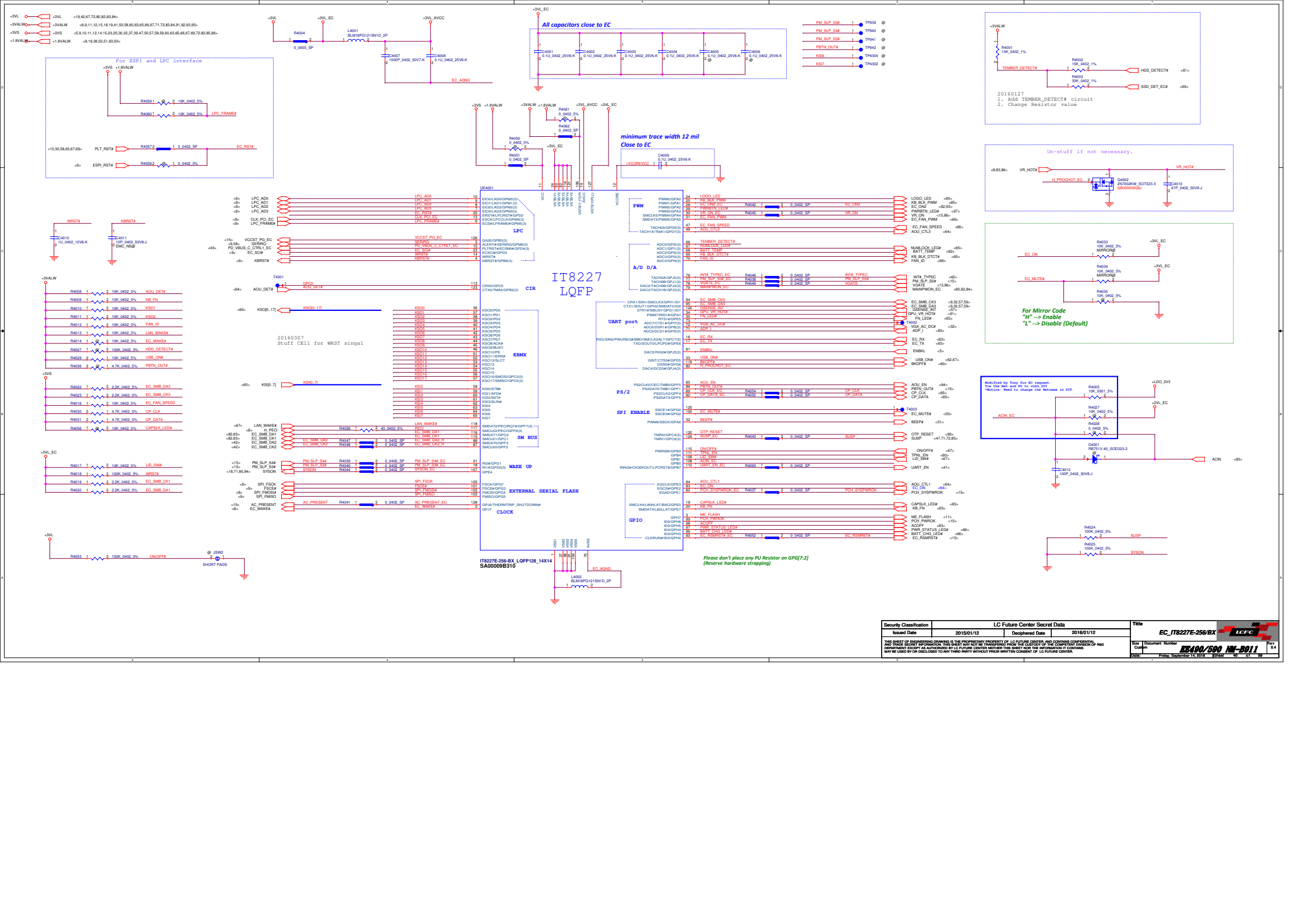


Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DC V TO 3VS_VGA/0.95VS_VGA

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

Date: Friday, September 14, 2018 | Sheet 39 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: EC_IT8227E-256/BX

Size	Document Number	Rev
Custom	EX400/500 MN-B011	0.4

Date: Friday, September 14, 2018 | Sheet 49 of 99

+3VALW ——— +3VALW <6,9,11,12,15,18,19,40,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>

+5VALW ——— +5VALW <38,39,42,43,47,62,64,66,67,71,72,84,85,86,87,88,89,91,93,94>

+5VS ——— +5VS <47,50,51,60,61,65,66,72>

LAYOUT/ROUTING GUIDELINES

1.For the ADC layout notice circuits,
a) Keep the trace away from Power, fast data bus, and CRTs. Especially PWM DC-DC control.
b) Isolate Analog and Digital ground plane.

2.For all power plane,

a)For the VSTBY circuits,

*Recommended net "VSTBY" minimum trace width 12mils.

b)For the VBAT circuits,

1) Vbat should be routed with a minimum trace width of 12 mils.

2) Please make the trace length short, and the trace width wide enough.

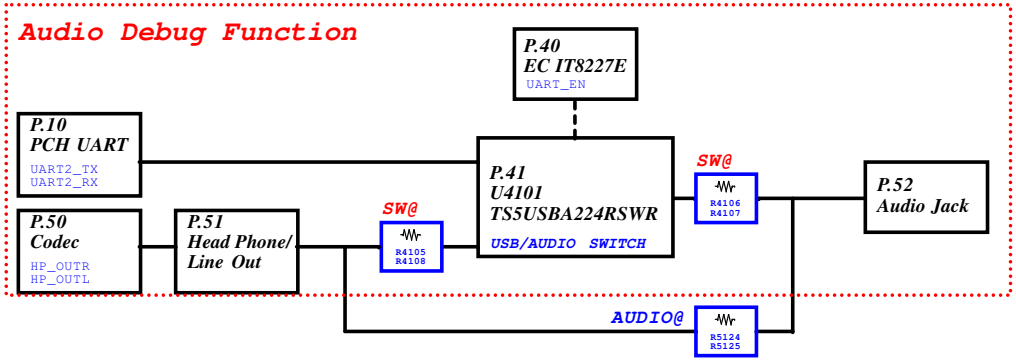
3) Isolate the pin-Vbat of EC and the pin of south bridge VCCRTC to avoid VBAT drops.

4) The capacitor connected to Diode is spare for battery installation glitch.

c)For the PLL power circuits,

Internal PLL is supplied by power pin127 of EC only and may have some filter circuit.

3.For SPI clock lines,
a) If possible, please avoid using any through-hole.
b) Do not use multiple signal layers for clock signals.
c) Please make the trace length short, and the trace width wide enough.
EC should close to PCH for HSPI signals & SPI flash should close to EC for FSPI signals.
d) The spacing to the closest neighbor should be wide enough.
e) The discrete damping resistors and capacitors are recommended.
f) Keep clock traces as straight as possible.Use arc-shaped traces instead of right-angle bends.



FUNCTION TABLE

A_{SEL}	V_{AUDIO}	V_{BUS}	L,R	D+, D–
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF(1)	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

(1) 100Ω shunt resistors are enabled in this state.

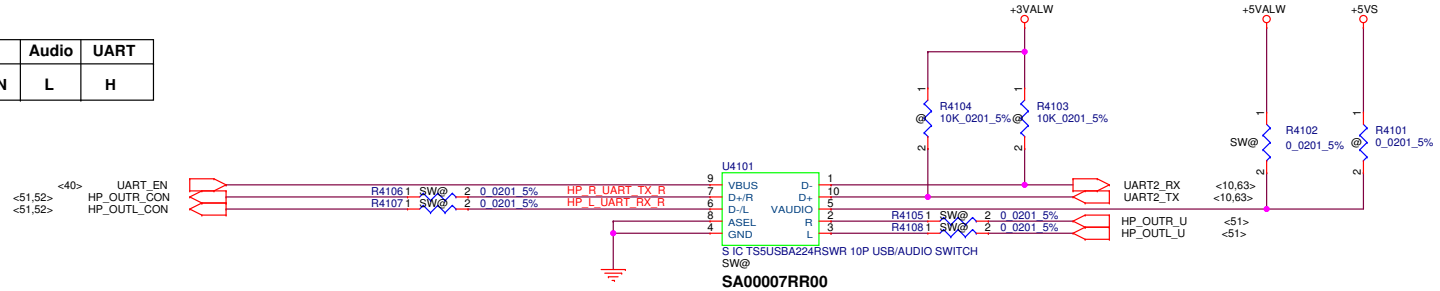
AUDIO DEBUG PORT

TABLE:

Part	Name	For NPI	For MP
U4101	SW@	ASM	NA
R4102	SW@	ASM	NA
R4105	SW@	ASM	NA
R4106	SW@	ASM	NA
R4107	SW@	ASM	NA
R4108	SW@	ASM	NA
R5124	AUDIO@	NA	ASM
R5125	AUDIO@	NA	ASM

TABLE:

Mode	Audio	UART
UART_EN	L	H



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: AUDIO DEBUG PORT

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

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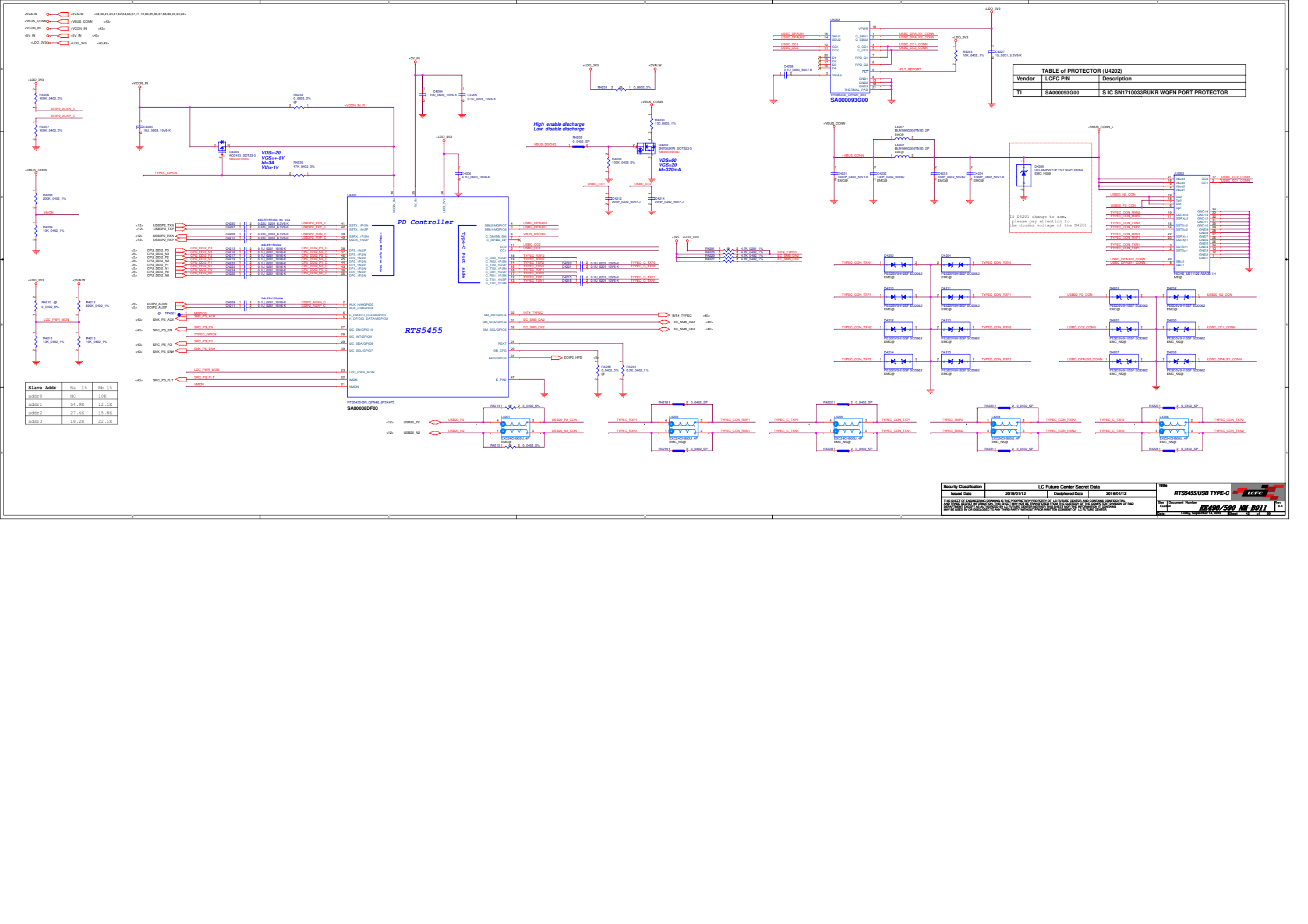
+5VALW
+VBUS_CONN
+VCON_IN
+5V_IN
+LDO_3V3
PD Controller
RTS5455
RTS5455-GR_QFN46_6P5X4P5
SA00008DF00
SA000093G00
TABLE of PROTECTOR (U4202)
Vendor
LCFC P/N
Description
TI
SA000093G00
S IC SN1710033RUKR WQFN PORT PROTECTOR
VDS=-20
VGS=+-8V
Id=-3A
Vth=-1v
VDS=60
VGS=20
Id=-320mA
High enable discharge
Low disable discharge
Slave Addr
Ra 1%
Rb 1%
addr0
NC
10K
addr1
54.9K
12.1K
addr2
27.4K
15.8K
addr3
18.2K
22.1K
Security Classification
LC Future Center Secret Data
Issued Date
2015/01/12
Deciphered Date
2016/01/12
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Title
RTS5455/USB TYPE-C
Size
Custom
Document Number
EB490/590 NM-B911
Rev
0.4
Date:
Friday, September 04, 2015
Sheet
48
of
58

+5VALW
+VBUS_CONN
VSYSTEM2
+VCON_IN
+5V_IN
+LDO_3V3

+5VALW <38,39,41,42,47,62,64,66,67,71,72,84,85,86,87,88,89,91,93,94>
+VBUS_CONN <42>
VSYSTEM2 <80,83>
+VCON_IN <42>
+5V_IN <42>
+LDO_3V3 <40,42>

+5VALW
+VCON_IN
R4339 2 1 0_0603_SP
+5V_IN
D4310
1SS355VMTE-17
Vr=80V
Ifm=225mA

+VBUS_CONN
D4311
1SS355VMTE-17
Vr=80V
Ifm=225mA
C4306
2.2U_0603_50V6-K
R4342 100K_0402_5%
U4305
IN OUT ADJ EN GND NC
SYV634DEC_DFN6_2X2
SA00008EQ00
R4305
73.2K_0402_1%
C4305
47P_0402_50V8-J
C4302
2.2U_0402_10V6-K
vref0.6V
R4338
10K_0402_1%
<40> PD_VBUS_C_CTRL1_EC
Q4304
2N7002KW_SOT323-3
SB000009Q8J
R4316
100K_0402_5%

+5VALW
C4308
100U_1206_6.3V6-M
C4307
1U_0603_25V7-K
+LDO_3V3
R4346
10K_0402_1%
<42> SRC_PS_FLT
<42> SRC_PS_EN
<42> SRC_PS_FO
R4315
100K_0402_5%
R4345
100K_0402_5%
U4301
A1 VIN1
A2 VIN2
A4 FLT#
B4 EN
C4 FO
B1 VCP1
B2 VCP2
C1 VCP3
C2 VBUS1
D1 VBUS2
D2 VBUS3
A3 ILIM
B3 GND1
C3 GND2
D3 GND3
D4 CAP
NX5P3290UKZ_WLCSP16
SA00008BS00
C4311
1000P_0201_50V7-K
R4343
16K_0402_1%
D4312
NEED PN
@PTVS24VS1UR_SOD123W2
C4312
4.7U_0805_50V6-K
close U4301.D2
+VBUS_CONN
J9
JUMP_43X118
@
3A
VSYSTEM2
J13 @
JUMP_43X118
不開鋼板
C4310
1U_0603_25V7-K
C4309
4.7U_0805_50V6-K
close U4302.B2
R4347
1M_0402_5%
@
U4302
B2 VBUS1
C2 VBUS2
D2 VBUS3
E1 VBUS4
E2 VBUS5
A1 VINT1
B1 VINT2
C1 VINT3
D1 VINT4
B3 OVLO
A2 ACK
C3 GND1
D3 GND2
E3 GND3
A3 EN#
NX20P5090UK_WLCSP15
SA00007JY00
SNK_PS_ACK
SNK_PS_EN#
<42> SNK_PS_ACK
<42> SNK_PS_EN#
+LDO_3V3
R4348
10K_0402_1%
R4351
10K_0402_1%
R4349
100K_0402_5%
@
R4350
0_0402_SP

TABLE of TypeC Load Switch (U4302)

Vendor	P/N	LCFC P/N
NXP	NX20P5090UKAZ	SA00007JY00
KINETIC	KTS1677EVH-TR	SA00009G700

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: RTS5455/POWER SWITCH
Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4
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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

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Size	Document Number	Rev
Custom	***EK490/590 NM-B911***	0.4

Date: Friday, September 14, 2018 Sheet 44 of 99

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

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Size	Document Number	Rev
D	***EX490/590 NM-B911***	0.4

Date: Friday, September 14, 2018 Sheet 45 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

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Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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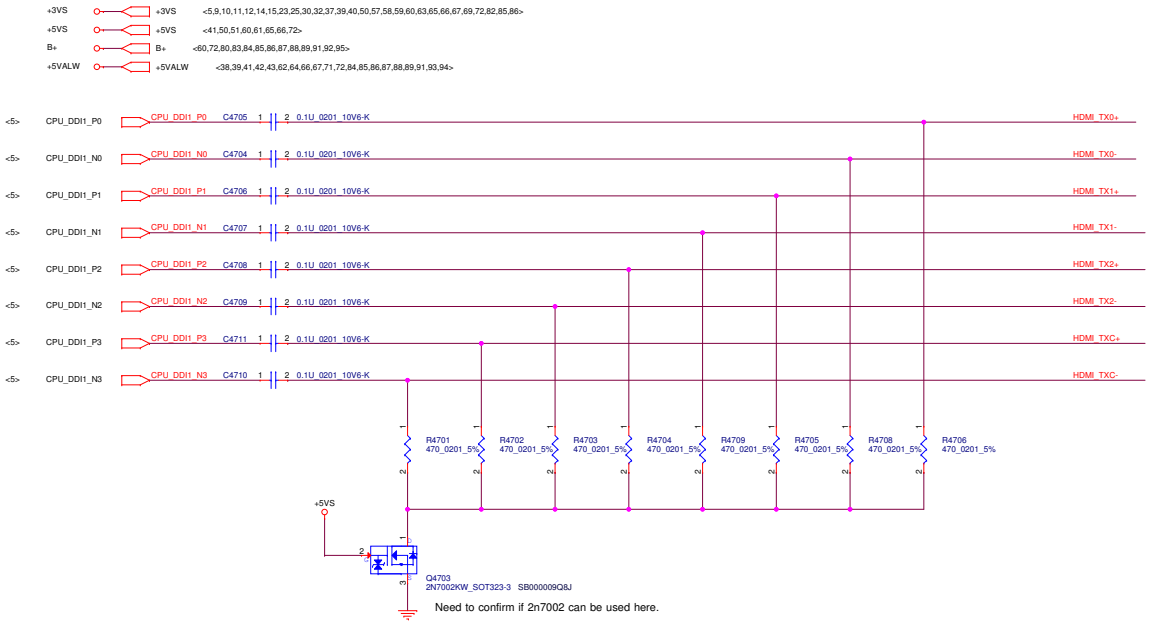
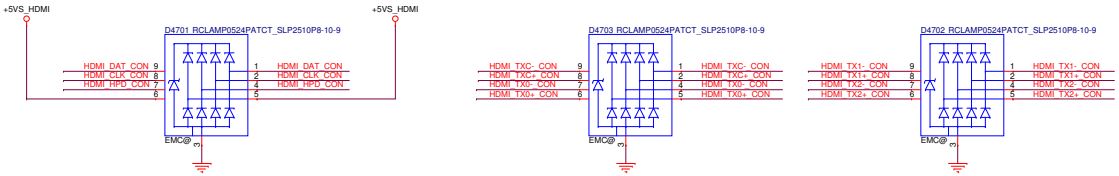
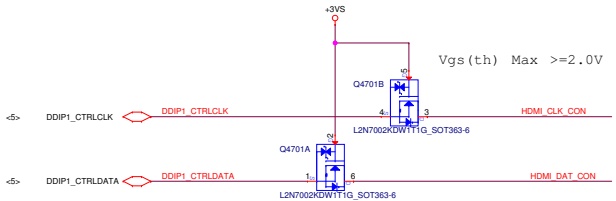






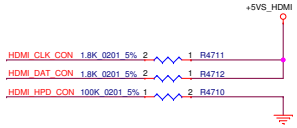


Figure 1-2. HDMI* HPD Active Level Shifter Design Recommendation

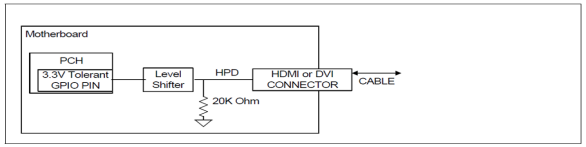
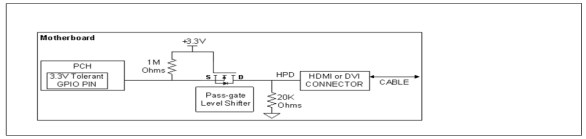
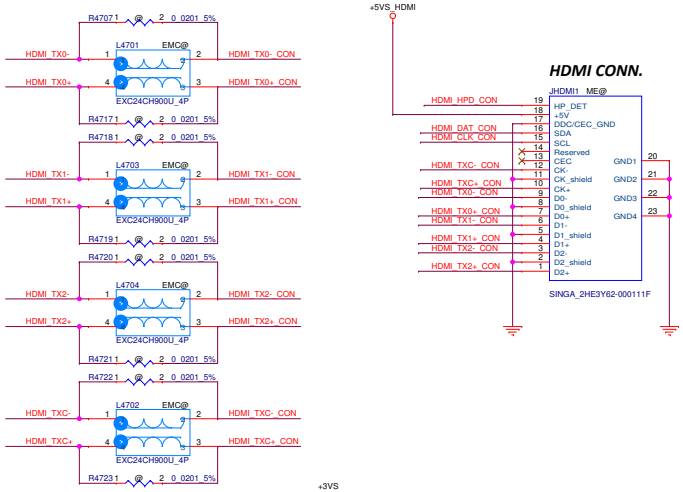


Figure 1-3. HDMI* HPD Cost Reduced Level Shifter Design Recommendation





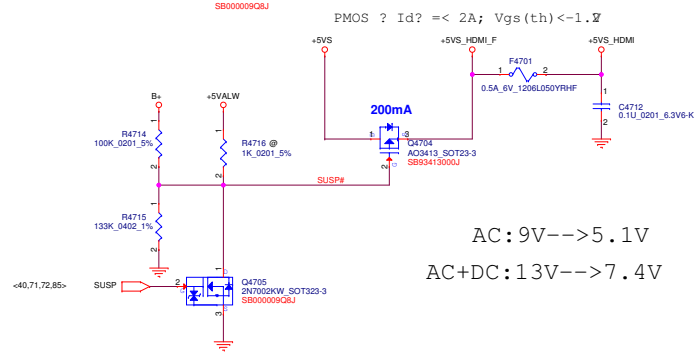


TABLE of POWER SWITCH (F4701)

	LCFC P/N	Description
LITTELFUSE	SP040005G00	S FUSE 1206L050YRHF 0.5A 6V CURUS/TUV
BOURNS	SP040005L00	S_PPTC_TH MF-NSMF050-2 0.5A 13.2V UL/TUV

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Title: **BLANK**

Size	Document Number	Rev
D	***RX490/590 NM-B911***	0.4

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Title

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+5VS +5VS <41,47,51,60,61,65,66,72>
+3VL +3VL <19,40,42,67,72,80,82,83,84>
+3VALW +3VALW <6,9,11,12,15,18,19,40,41,58,60,63,65,66,67,71,72,83,84,91,92,93,95>
+1.8VALW +1.8VALW <9,19,38,40,51,63,93>
+MICBIASB +MICBIASB <51>

Close to Pin13,16,29

+5VS — R5009 0_0603_SP — +5VS_CLASSD
C5001 10U_0603_6.3V6-M
C5002 10U_0603_6.3V6-M
C5003 0.1U_0402_10V7-K
C5004 0.1U_0402_10V7-K
C5017 0.1U_0402_10V7-K

Close to Pin3

+3VALW — R5005 0_0402_SP — +VDD_HDA
C5015 1U_0402_6.3VA-K

Close to Pin7

+3VS — R5001 0_0402_SP — +3VS_VDDO
C5011 0.1U_0402_10V7-K

EMI filter for Class D output signals
Close to Codex

SPK_L2+_R — 1/16W_15_5%_0402 — R5004 — C5005 220P_0402_50V7-J
SPK_L1-_R — 1/16W_15_5%_0402 — R5011 — C5006 220P_0402_50V7-J
SPK_R2+_R — 1/16W_15_5%_0402 — R5012 — C5007 220P_0402_50V7-J
SPK_R1-_R — 1/16W_15_5%_0402 — R5013 — C5008 220P_0402_50V7-J

Please Close to Pin9

+3VS — R5003 0_0402_SP — +3VS_VDDIO
C5013 2.2U_0402_6.3V6-M
C5014 0.1U_0402_10V7-K

+1.8VALW — R5002 0_0402_SP — +VDD18

+VDD18
C5028 2.2U_0402_6.3V6-M
C5029 0.1U_0402_10V7-K
C5023 1U_0402_6.3VA-K
GNDA

+3VS_VDDIO
C5025 0.47U_0201_25V6-K
+VDD_HDA
C5024 1U_0402_6.3VA-K
GNDA

+VDD18
C5030 2.2U_0402_6.3V6-M
C5031 0.1U_0402_10V7-K
+5VS_CLASSD

+3VS_VDDO
R5006 47K_0402_5%
D5001 RB751V-40_SOD323-2 SCS00006S00

<40> EC_MUTE# — EC_MUTE#

U5001 — SA00009AW00 — CX11880-11Z_QFN42_5X5

<11> PCH_HDA_RST#	PCH_HDA_RST#	2	RESET#
<11> PCH_HDA_BCLK	PCH_HDA_BCLK	40	BCLK
<11> PCH_HDA_SYNC	PCH_HDA_SYNC	41	SYNC
<11> PCH_HDA_SDIN0	PCH_HDA_SDIN0 R5008 33_0402_5%	PCH_HDA_SDIN0_R 42	SDI
<11> PCH_HDA_SDOUT	PCH_HDA_SDOUT	1	SDO
<51> PC_BEEP	PC_BEEP	36	PCBEEP
	SPKR_MUTE# R5015 0_0201_SP	SPKR_MUTE#_R 7	SPKR_MUTE#/SPDIF/GPIO1
<51> JSENSE	JSENSE	35	JSENSE
		6	MUSIC_REQ/SPDIF/GPIO0
<60> DMIC_CLK	DMIC_CLK R5007 EMC@ 33_0402_5%	MIC_CLK_R 10	PORTC_DMIC_CLK1/GPIO2
<60> DMIC_DATA	DMIC_DATA	8	PORTC_DMIC_DATA1/GPIO3
	C5016 680P_0402_50V7K EMC@	4	TEST1
	+VDD_HDA R5010 10K_0402_5%	5	TEST2
	C5018 2.2U_0402_6.3V6-M	FLY_P 19	CP_FLY_P
		FLY_N 20	CP_FLY_N
	SPKR_MUTE# R5014 @ 0_0201_5% EAPD_R	11	EAPD
		43	EP

W= 80mils

		18	CP_VDD18
	2.2U_0402_6.3V6-M C5026	21	CP_VNEG
	2.2U_0402_6.3V6-M C5027	22	CP_VPOS
		29	AVDD5
		13	PVDD5_LEFT
		16	PVDD5_RIGHT
SPK_L2+_R		12	PORTG_LEFT+
SPK_L1-_R		14	PORTG_LEFT-
SPK_R2+_R		17	PORTG_RIGHT+
SPK_R1-_R		15	PORTG_RIGHT-
		32	MICBIASB
PORTB_R		34	PORTB_R
PORTB_L		33	PORTB_L
EXT_MIC_B		31	PORTD_B
EXT_MIC_A		30	PORTD_A
HGNDB HGNDA		26 25	HGNDB HGNDA
HP_OUTR		24	PORTA_R
HP_OUTL		23	PORTA_L

+MICBIASB
SPK_L2+_R <51>
SPK_L1-_R <51>
SPK_R2+_R <51>
SPK_R1-_R <51>
PORTB_R <51>
PORTB_L <51>
EXT_MIC_B <51>
EXT_MIC_A <51>
Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA
HGNDB <51,52>
HGNDA <51,52>
HP_OUTR <51>
HP_OUTL <51>

W= 300mils
C5019 0.1U_0402_10V7-K EMC@
C5020 0.1U_0402_10V7-K EMC_NS@
C5021 0.1U_0402_10V7-K EMC_NS@
GNDA

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Title: CODEC-CX11880
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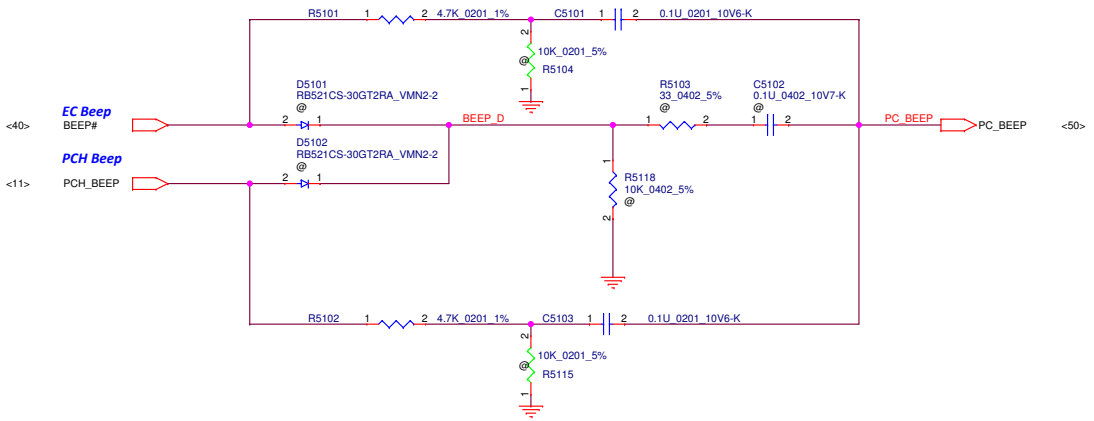
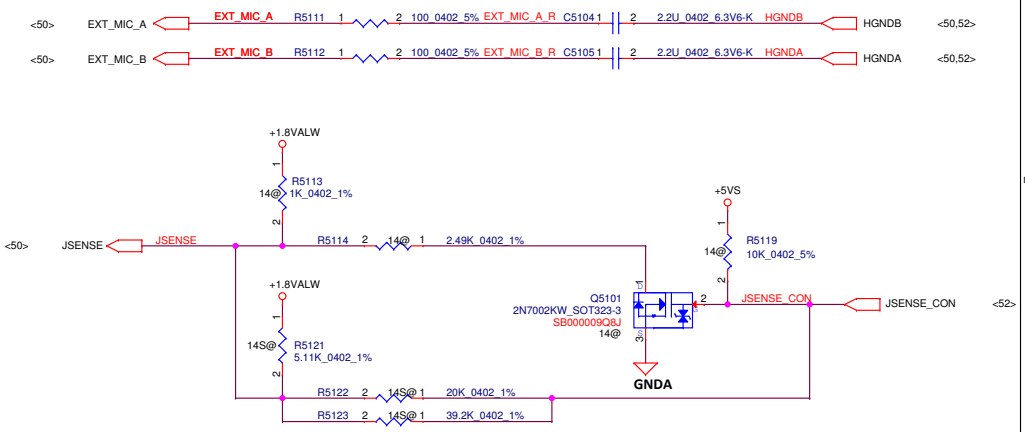
+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>
+VDD18 +VDD18 <50>
+MICBIASB +MICBIASB <50>

PC Beep

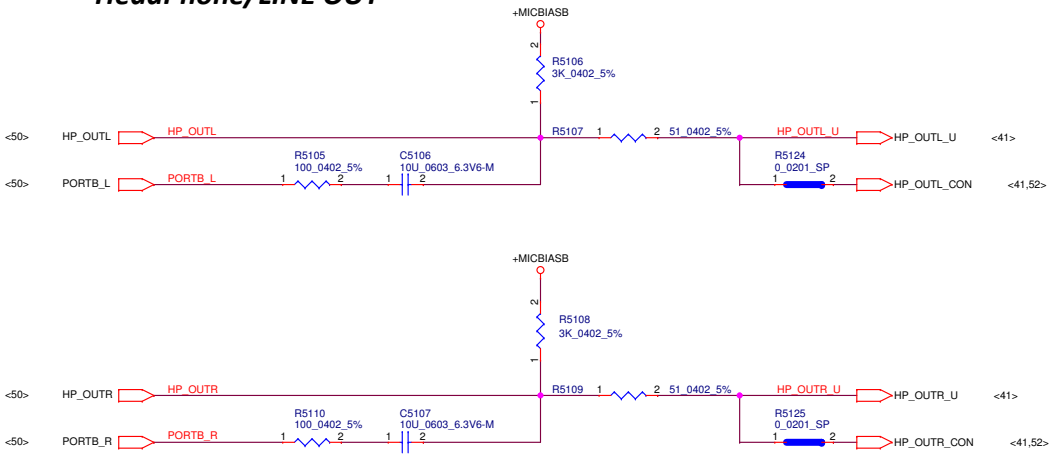


EXT. MIC/LINE IN

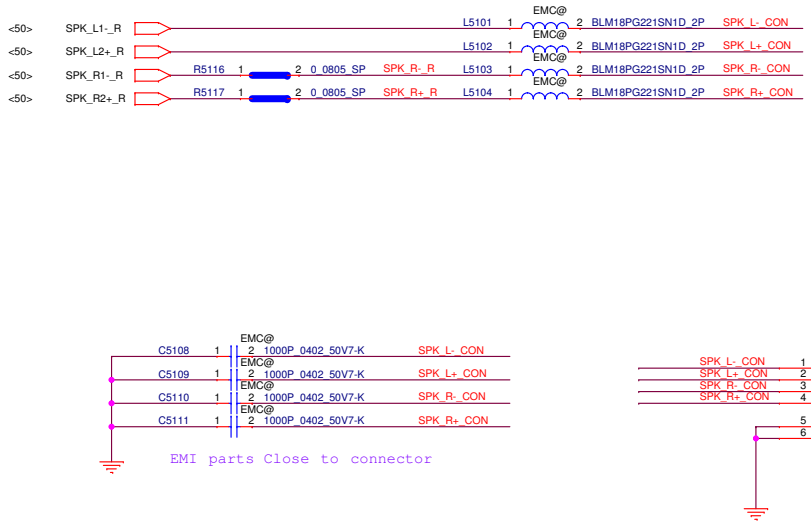
Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



HeadPhone/LINE OUT



SPK CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: HP/MIC JACK/Speaker

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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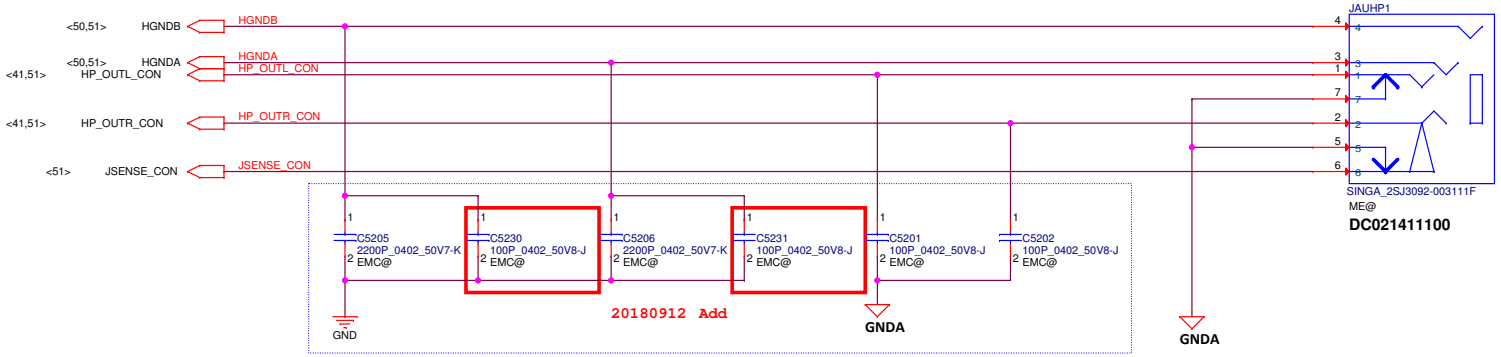
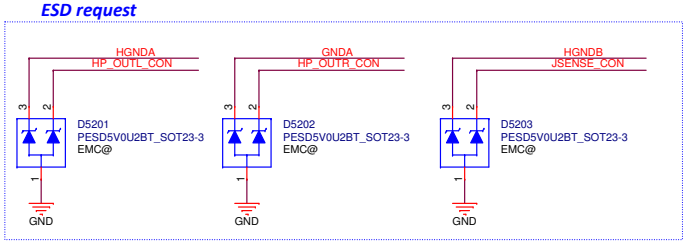
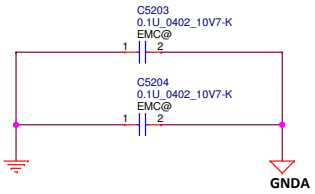
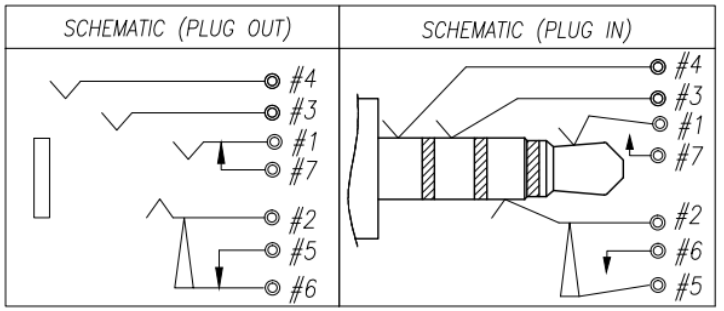


Vendor suggestion. Reserve for EMI.
Close to JAUHP.

ESD request







Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **AUDIO JACK**

Size	Document Number	Rev
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Title

GBE LAN PHY(BLANK)

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

GBE LAN SWITCH(BLANK)

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

Date: Friday, September 14, 2018 Sheet 54 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

RJ45 CONN.(BLANK)

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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Title

CARDREADER/CONN.(BLANK)

Size	Document Number	Rev
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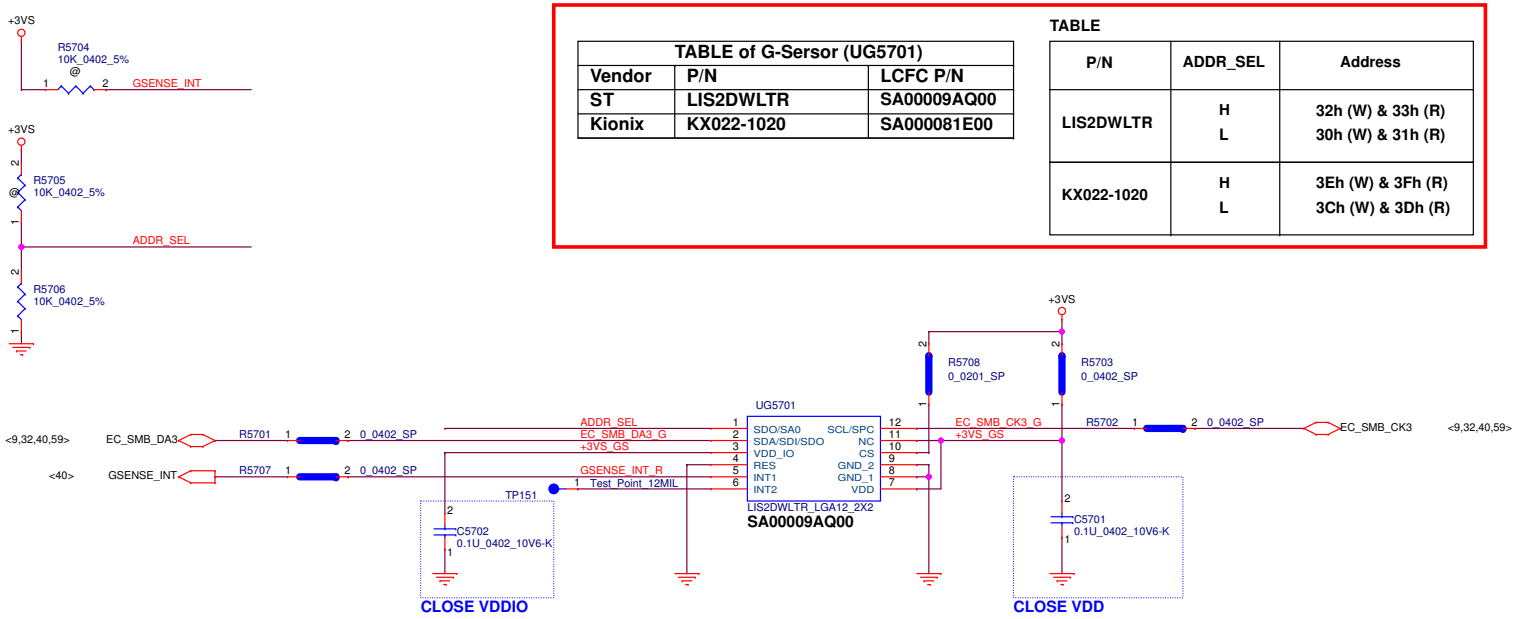
+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,58,59,60,63,65,66,67,69,72,82,85,86>

TABLE of G-Sersor (UG5701)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00

TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: G SENSOR

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

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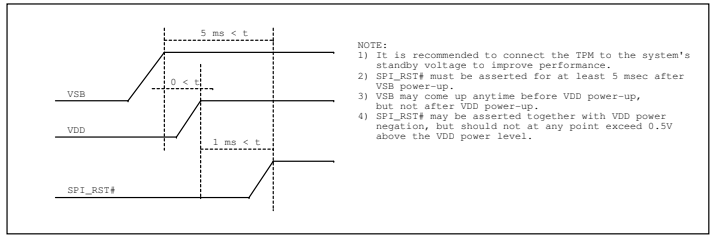
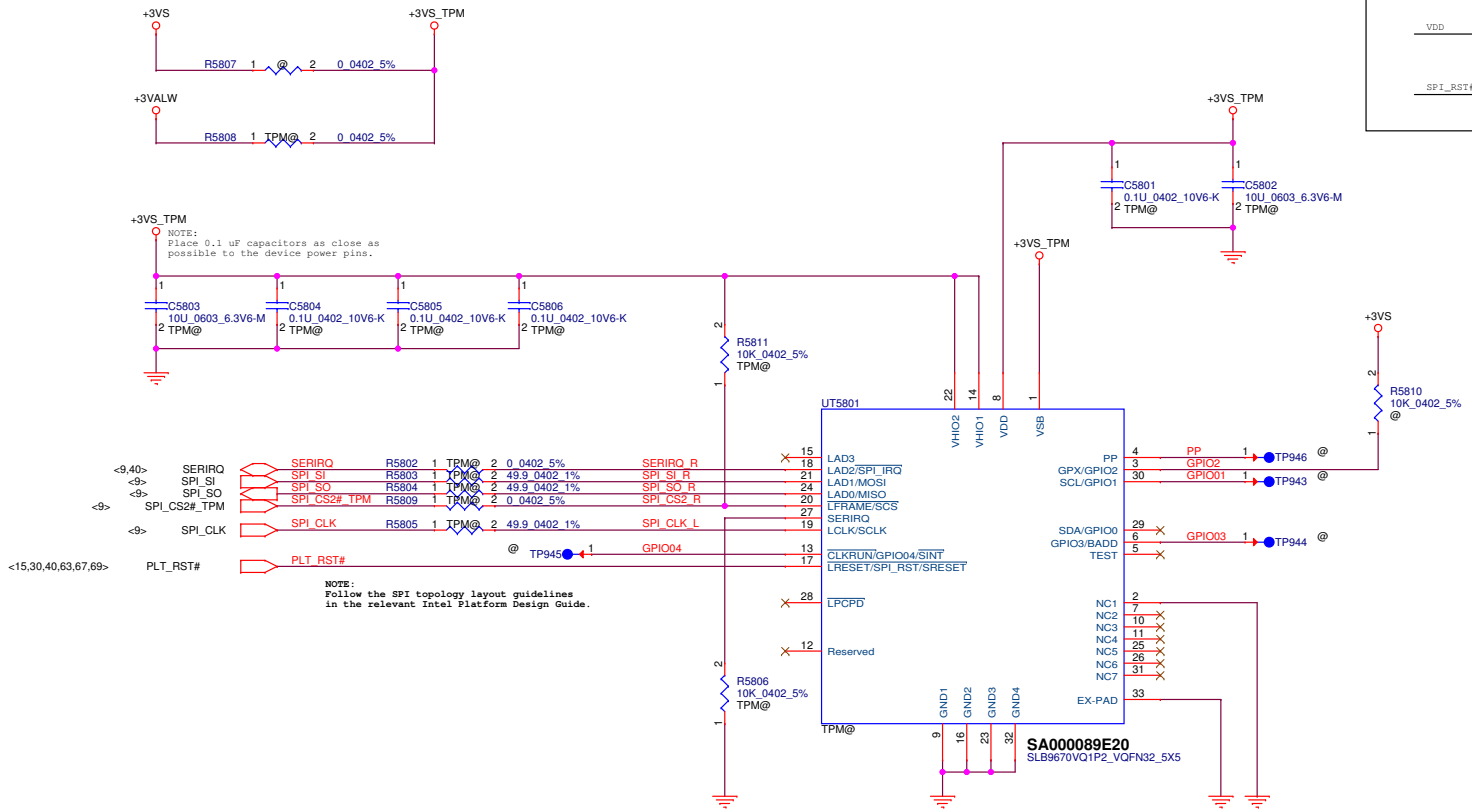
+3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,59,60,63,65,66,67,69,72,82,85,86>

+3VALW <6,9,11,12,15,18,19,40,41,50,60,63,65,66,67,71,72,83,84,91,92,93,95>

NOTE:
Check timing sequence in SDV phase.





Using Symbol of SLB9670VQ1P2

TABLE of TPM (UT5801)

Vendor	LCFC P/N	Description
ST	SA000089E20	S IC ST33HTPH2E32AHC0 VQFN 32P TPM
NUVOTON	SA00008KS10	S IC NPCT750LABYX QFN 32P TPM

TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AABB	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table

Title			
TPM			
Size: Custom	Document Number: EE490/590 NM-B911		Rev: 0.4
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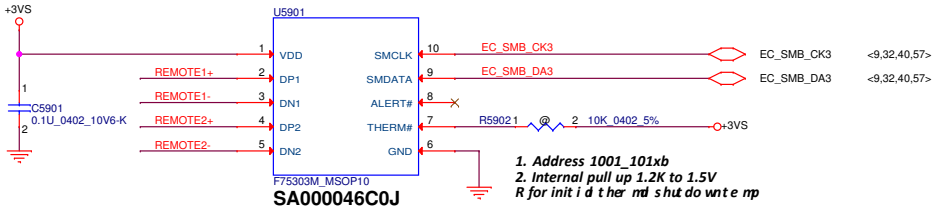
+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,60,63,65,66,67,69,72,82,85,86>

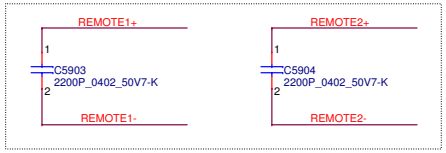
Thermal Sensor

Close to CPU

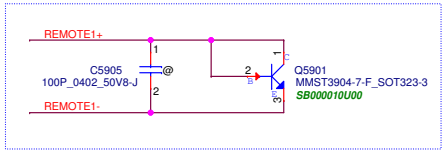


1. Address 1001_101xb
2. Internal pull up 1.2K to 1.5V
R for init i d t her mal shut do wnt e mp

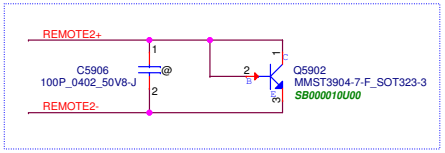
TABLE of Thermal Sensor (U5901)		
Vendor	P/N	LCFC P/N
FINTEK	F75303M	SA000046C0J
Nuvoton	NCT7719W	SA000065D00



Close to CHARGER



Close to GPU



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Trace length:<8"

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: THERMAL SENSOR

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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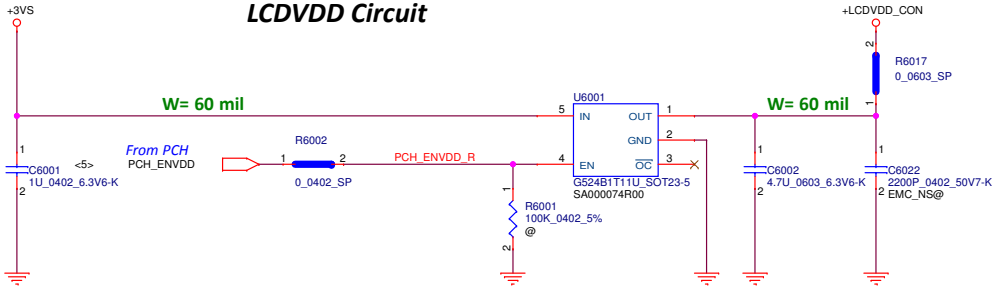
+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,63,65,66,67,69,72,82,85,86>

+5VS +5VS <41,47,50,51,61,65,66,72>

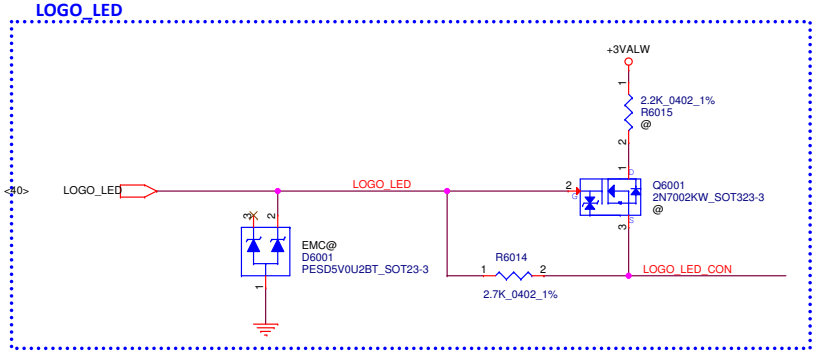
+3VALW +3VALW <6,9,11,12,15,18,19,40,41,50,58,63,65,66,67,71,72,83,84,91,92,93,95>

B+ B+ <47,72,80,83,84,85,86,87,88,89,91,92,95>

LCDVDD Circuit



LOGO_LED



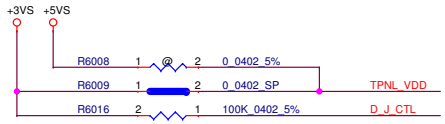
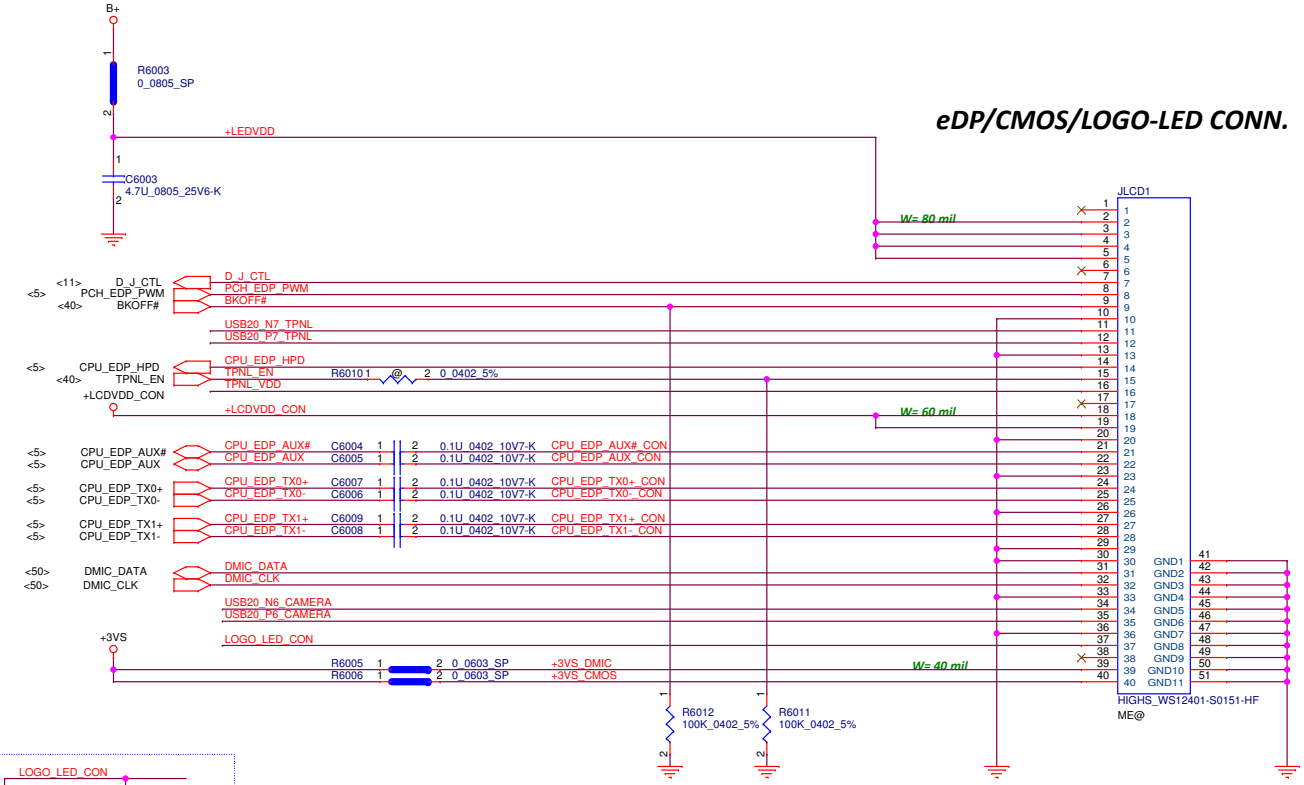
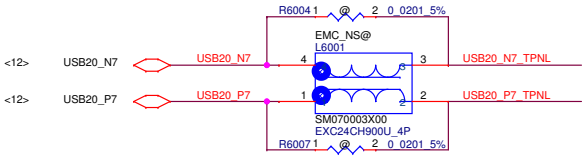


TABLE of POWER SWITCH (U6001)		
Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH

eDP/CMOS/LOGO-LED CONN.



Touch Panel



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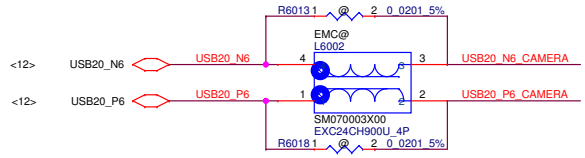
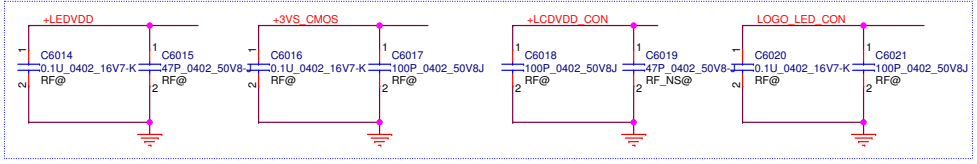


RF



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: eDP/CMOS/LOGO-LED CO

Size: Custom | Document Number: EE490/590 NM-B911 | Rev: 0.4

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+5VS +5VS <41,47,50,51,60,65,66,72>

<12> PCIE12_SATA0_CTX_DRX_P — PCIE12_SATA0_CTX_DRX_P — C6112 1 2 — 0.01U_0201_6.3V7-K — PCIE12_SATA0_CTX_DRX_P_CONN

<12> PCIE12_SATA0_CTX_DRX_N — PCIE12_SATA0_CTX_DRX_N — C6113 1 2 — 0.01U_0201_6.3V7-K — PCIE12_SATA0_CTX_DRX_N_CONN

<12> PCIE12_SATA0_CRX_DTX_P — PCIE12_SATA0_CRX_DTX_P — C6114 1 2 — 0.01U_0201_6.3V7-K — PCIE12_SATA0_CRX_DTX_P_CONN

<12> PCIE12_SATA0_CRX_DTX_N — PCIE12_SATA0_CRX_DTX_N — C6115 1 2 — 0.01U_0201_6.3V7-K — PCIE12_SATA0_CRX_DTX_N_CONN

SATA HDD CONN.

+5VS

C6101 10U_0603_10V6-K

C6102 10U_0603_10V6-K @

C6103 1U_0402_10V6-K @

C6104 0.1U_0402_25V6-K @

Change the size to 0603 for ME request
20180413 Modified by Tony

+5VS

R6102 0_0805_SP

JHDD1

PCIE12_SATA0_CTX_DRX_P_CONN
PCIE12_SATA0_CTX_DRX_N_CONN
PCIE12_SATA0_CRX_DTX_N_CONN
PCIE12_SATA0_CRX_DTX_P_CONN

<12> HD_SSD_DEVSLP1 — HD_SSD_DEVSLP1 — R6101 1 2 0_0402_SP — -CLKREQ_DEVSLP
<40> HDD_DETECT# — HDD_DETECT#

GND16 GND15

HIGHS_FC5AF141-3181H
ME@
SP011511040

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: SATA HDD CONN

Size	Document Number	Rev
B	EE490/590 NM-B911	0.4

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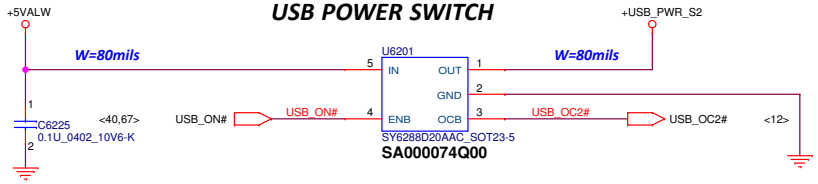
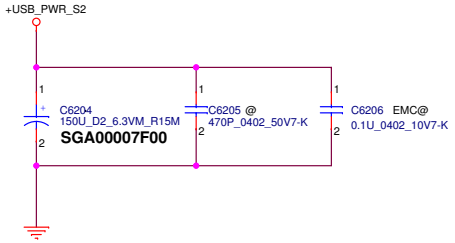
On Board (LEFT-Front)

+5VALW — +5VALW — <38,39,41,42,43,47,64,66,67,71,72,84,85,86,87,88,89,91,93,94>
+3VALW — +3VALW — <6,9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>
+USB_PWR_S2 — +USB_PWR_S2

USB POWER SWITCH





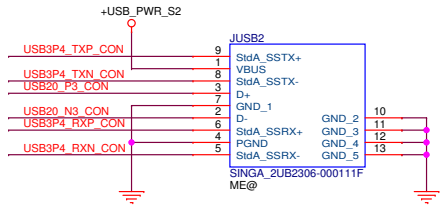
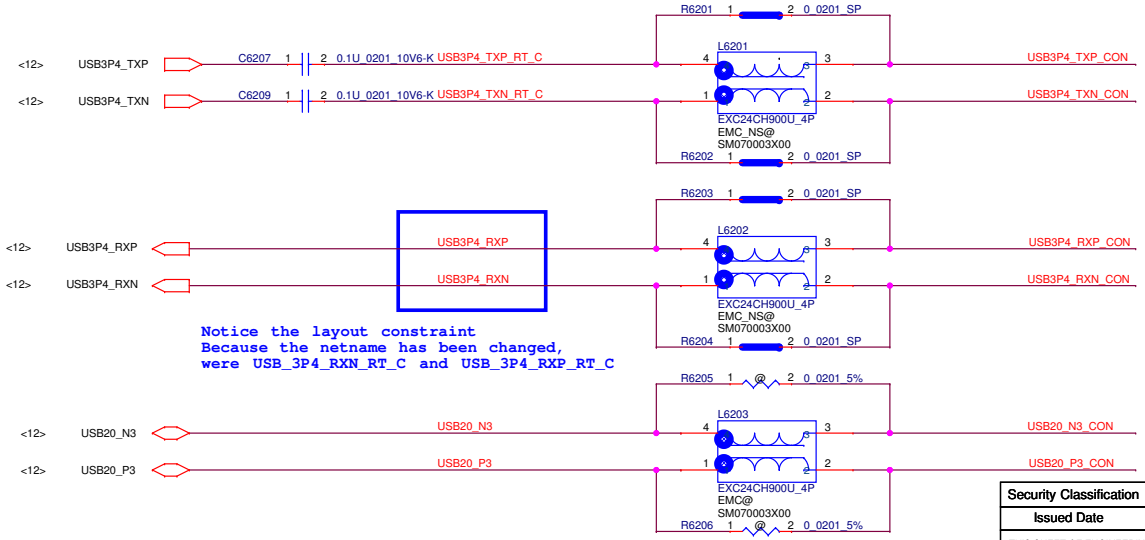
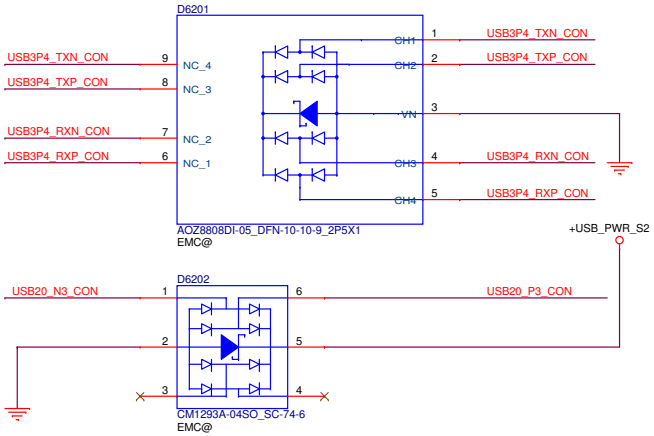


TABLE of POWER SWITCH (U6201)		
Vendor	LCFC P/N	Description
SILERGY	SA000074Q00	S IC SY6288D20AAC SOT23 5P POWER SWITCH
GMT	SA000079400	S IC G517F2T11U SOT-23 5P POWER SWITCH





Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: USB3 P2 CONN

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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KEY-E NGFF CCARD FOR WLAN

H=3.20mm Connector

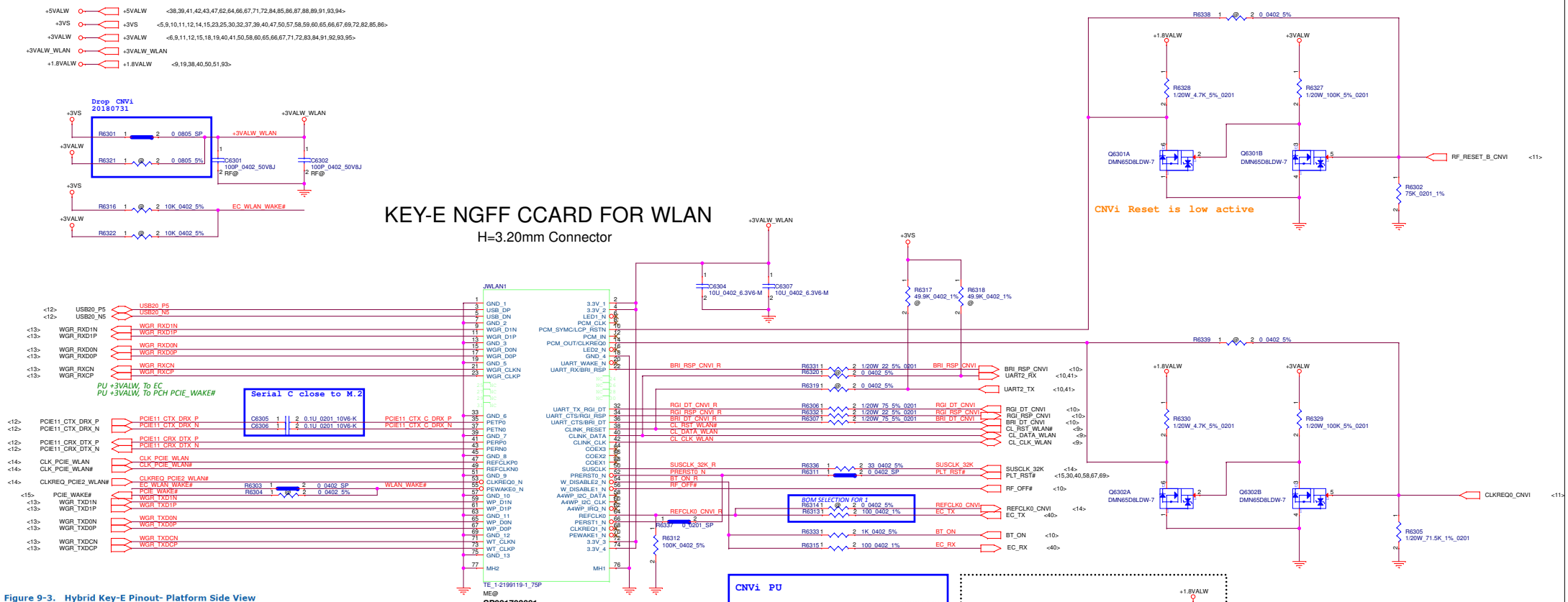

Figure 9-3. Hybrid Key-E Pinout- Platform Side View

Standard M.2 Key E	LcP Signals	LcP Signals	Standard M.2 Key E	
+V3P3A		GND		75
+V3P3A		WT_CLKP	REFCLKN1	73
PEWake 1# (IO)(0/3.3V)		WT_CLKN	REFCLKP1	71
CLKREQ1# (IO)(0/3.3V)		GND		69
PERST1# (O)(0/3.3V)		WT_D0P	PERn1	67
RESERVED	REFCLK0 (I)(1V @38.4MHz)	WT_D0N	PERp1	65
ALERT# (I)(0/1.8)	A4WP_IRQ#	GND		63
I2C_CLK (O)(0/1.8V)	A4WP_I2C_CLK	WT_D1P	PETn1	61
I2C_DATA (IO)(0/1.8)	A4WP_I2C_DATA	WT_D1N	PETp1	59
W_DISABLE1# (O)(0/3.3V)		GND		57
W_DISABLE2# (O)(0/3.3V)		PEWake0# (IO)(0/3.3V)		55
PERST0# (O)(0/3.3V)		CLKREQ0# (IO)(0/3.3V)		53
SUSCLK (32kHz) (O)(0/3.3V)	C_P32K (3.3V Tolerant)	GND		51
COEX_TXD (O)(0/1.8V)		REFCLKN0		49
COEX_RXD (O)(0/1.8V)		REFCLKP0		47
COEX3 (IO)(0/1.8V)		GND		45
CLink CLK		PERn0		43
CLink DATA		PERp0		41
CLink RESET (O)(0/3.3V)		GND		39
LPSS UART RTS (O)(0/1.8V)	/ BRI_DT (MUX'd in PCH/SoC)	PETn0		37
LPSS UART CTS (I)(0/1.8V)	/ RGI_RSP (MUX'd in PCH/SoC)	PETp0		35
LPSS UART Tx (O)(0/1.8V)	/ RGI_DT (MUX'd in PCH/SoC)	GND		33
Connector Key		Connector Key		E
Connector Key		Connector Key		
Connector Key		Connector Key		
Connector Key		Connector Key		
LPSS UART Rx (I)(0/1.8V)	/ BRI_RSP (MUX'd in PCH/SoC)	WGR_CLKP	SDIO Reset# (O)(0/1.8V)	23
UART Wake# (I)(0/3.3V)		WGR_CLKN	SDIO Wake# (I)(0/1.8V)	21
GND	GND/LNA_EN (LcP Production)	GND	SDIO DAT3 (IO)(0/1.8V)	19
LED2# (I)(OD)		WGR_D0P	SDIO DAT2 (IO)(0/1.8V)	17
PCM_OUT (O)(0/1.8V)	/ CLKREQ0 (MUX'd in PCH/SoC)	WGR_D0N	SDIO DAT1 (IO)(0/1.8V)	15
PCM_IN (I)(0/1.8V)		GND	SDIO DAT0 (IO)(0/1.8V)	13
PCM_SYNC (O)(0/1.8V)	/ RF_RESET_B (MUX'd in PCH/SoC)	WGR_D1P	SDIO CMD (IO)(0/1.8V)	11
PCM_CLK (O)(0/1.8V)		WGR_D1N	SDIO CLK (O)(0/1.8V)	9
LED1# (I)(OD)		GND		7
+V3P3A		USB_D-		5
+V3P3A		USB_D+		3
		GND		1

TABLE of WLAN(JWLAN1)		
Vendor	P/N	LCFC P/N
TE	TE_1-2199119-1_75P-T	SP021703091

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	WLAN NGFF CONN.		
Size: Custom	Document Number: EE490/590 NM-B911		Rev: 0.4
Date: Friday, September 14, 2018	Sheet 63 of 99		

On Board (LEFT-Back)

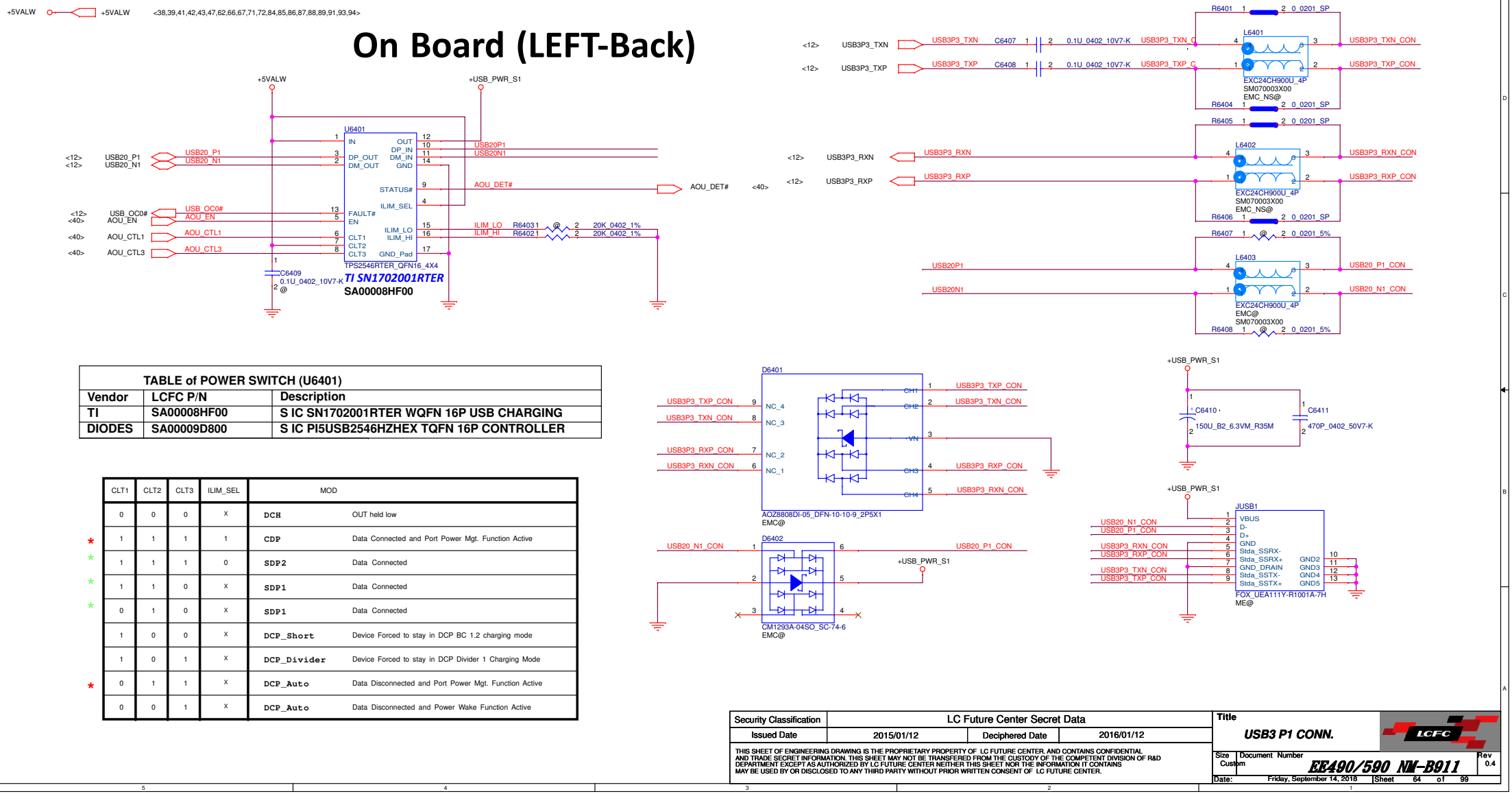

TABLE of POWER SWITCH (U6401)		
Vendor	**LCFC P/N**	**Description**
TI	**SA00008HF00**	**S IC SN1702001RTER WQFN 16P USB CHARGING**
DIODES	**SA00009D800**	**S IC PI5USB2546HZHEX TQFN 16P CONTROLLER**

	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
	0	0	0	X	**DCH**	OUT held low
*	1	1	1	1	**CDP**	Data Connected and Port Power Mgt. Function Active
*	1	1	1	0	**SDP2**	Data Connected
*	1	1	0	X	**SDP1**	Data Connected
*	0	1	0	X	**SDP1**	Data Connected
	1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	**DCP_Auto**	Data Disconnected and Port Power Mgt. Function Active
	0	0	1	X	**DCP_Auto**	Data Disconnected and Power Wake Function Active

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **USB3 P1 CONN.**

Size	Document Number	Rev
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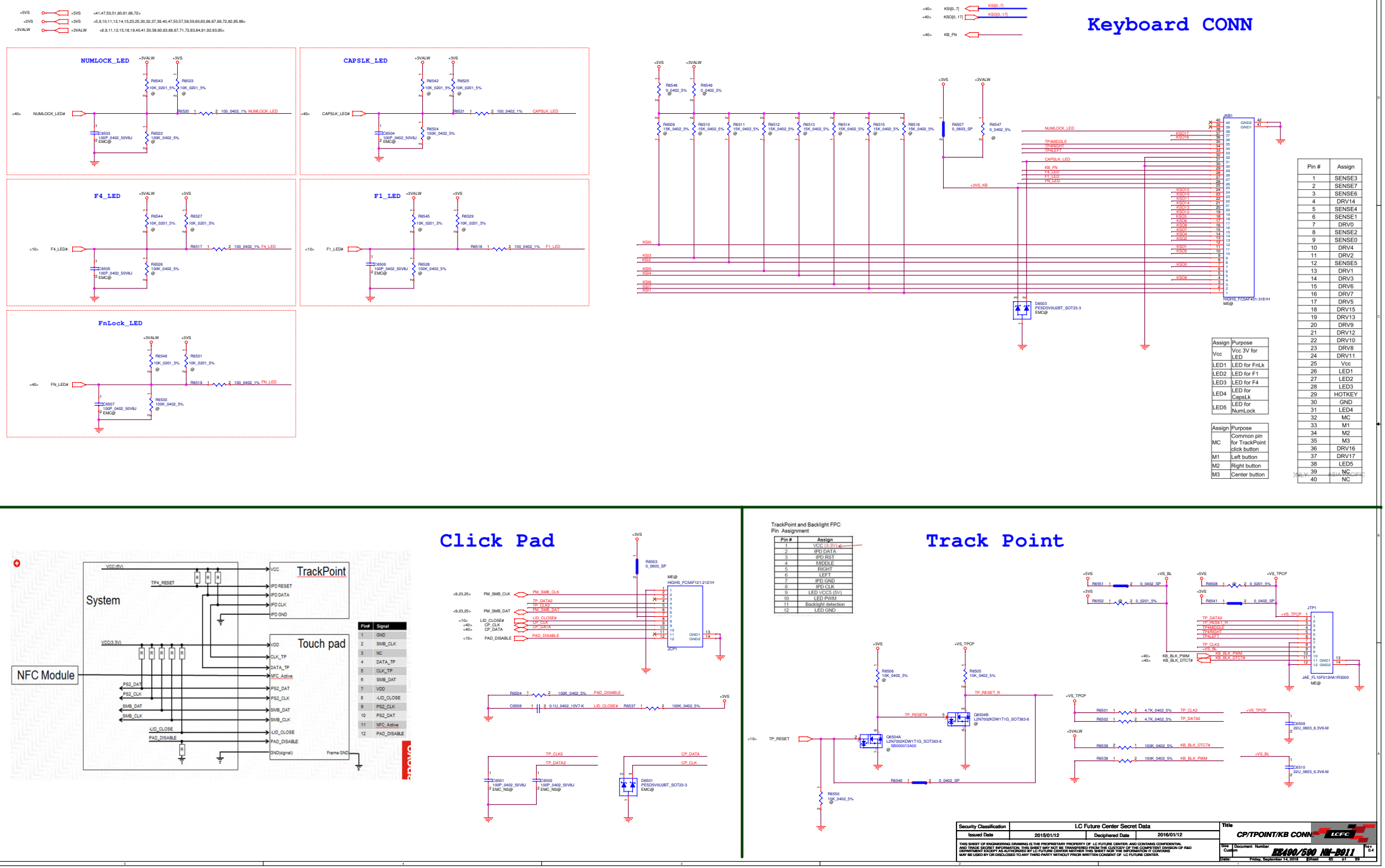
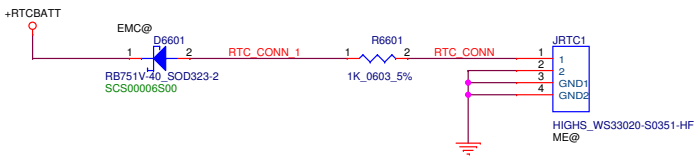
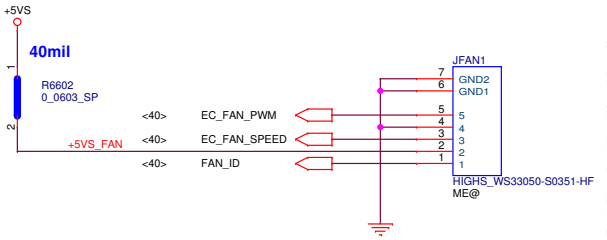

Keyboard CONN
NUMLOCK_LED
CAPSLK_LED
F4_LED
F1_LED
FnLock_LED
Click Pad
Track Point
System
NFC Module
TrackPoint
Touch pad
TrackPoint and Backlight FPC
Pin Assignment
Pin # | Assign
1 | VCC (3.3V)
2 | IPD DATA
3 | IPD RST
4 | MIDDLE
5 | RIGHT
6 | LEFT
7 | IPD GND
8 | IPD CLK
9 | LED VCC5 (5V)
10 | LED PWM
11 | Backlight detection
12 | LED GND
Pin # | Assign
1 | SENSE3
2 | SENSE7
3 | SENSE6
4 | DRV14
5 | SENSE4
6 | SENSE1
7 | DRV0
8 | SENSE2
9 | SENSE0
10 | DRV4
11 | DRV2
12 | SENSE5
13 | DRV1
14 | DRV3
15 | DRV6
16 | DRV7
17 | DRV5
18 | DRV15
19 | DRV13
20 | DRV9
21 | DRV12
22 | DRV10
23 | DRV8
24 | DRV11
25 | Vcc
26 | LED1
27 | LED2
28 | LED3
29 | HOTKEY
30 | GND
31 | LED4
32 | MC
33 | M1
34 | M2
35 | M3
36 | DRV16
37 | DRV17
38 | LED5
39 | NC
40 | NC
Assign | Purpose
Vcc | Vcc 3V for LED
LED1 | LED for FnLk
LED2 | LED for F1
LED3 | LED for F4
LED4 | LED for CapsLk
LED5 | LED for NumLock
Assign | Purpose
MC | Common pin for TrackPoint click button
M1 | Left button
M2 | Right button
M3 | Center button
Security Classification
LC Future Center Secret Data
Issued Date
2015/01/12
Deciphered Date
2016/01/12
CP/TPOINT/KB CONN
Size
Custom
Document Number
KB490/590 NM-B011
Rev
0.4
Date:
Friday, September 14, 2018
Sheet
65
of
99

+RTCBATT +RTCBATT <14,80>
+5VS +5VS <41,47,50,51,60,61,65,72>
+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,67,69,72,82,85,86>
+3VALW +3VALW <6,9,11,12,15,18,19,40,41,50,58,60,63,65,67,71,72,83,84,91,92,93,95>

RTC CONN.

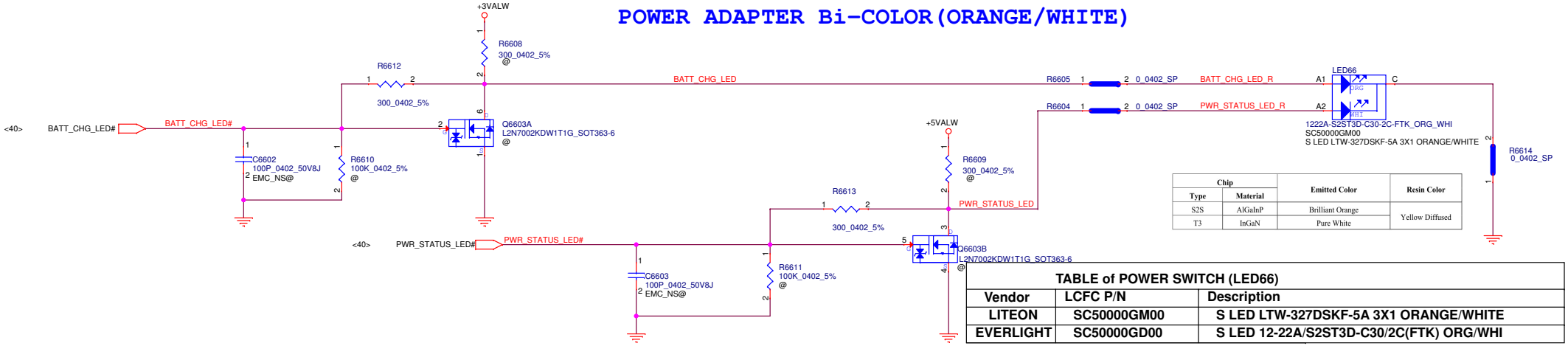


FAN CONN.



Pin No.	Signal	Note
1	ID	Fan ID
2	VCC	+5V
3	FG	2 Pulses
4	GND	–
5	PWM	PWM

POWER ADAPTER Bi-COLOR(ORANGE/WHITE)

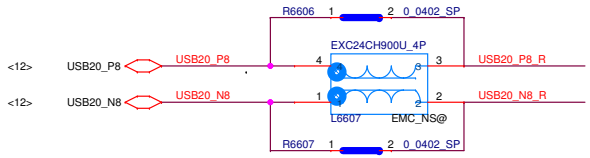


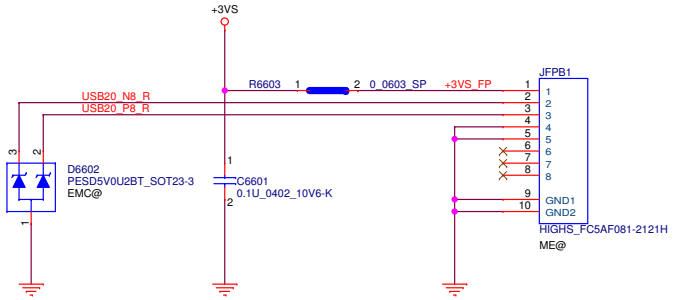
Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInP	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	

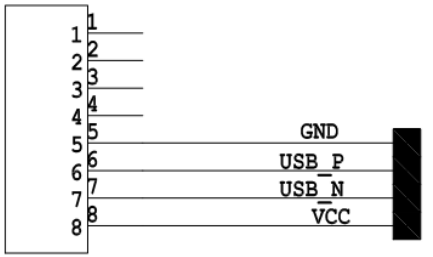
TABLE of POWER SWITCH (LED66)

Vendor	LCFC P/N	Description
LITEON	SC50000GM00	S LED LTW-327DSKF-5A 3X1 ORANGE/WHITE
EVERLIGHT	SC50000GD00	S LED 12-22A/S2ST3D-C30/2C(FTK) ORG/WHI

FingerPrint CONN.







Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: RTC/LED /FAN ,FPR CONN

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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+3VL +3VL <19,40,42,72,80,82,83,84>

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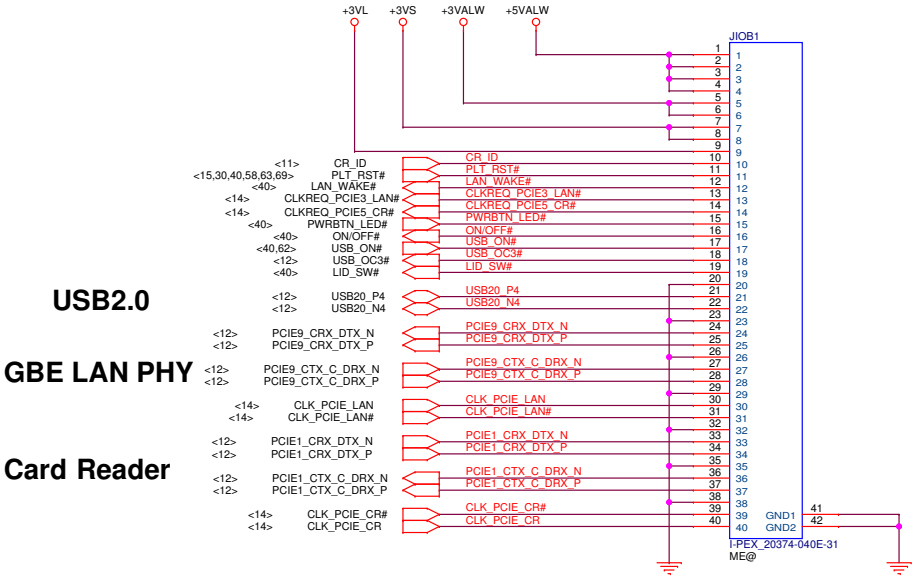
+5VALW +5VALW <38,39,41,42,43,47,62,64,66,71,72,84,85,86,87,88,89,91,93,94>

+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,69,72,82,85,86>

IO_40_Pin conn



USB2.0

GBE LAN PHY

Card Reader

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: IO BOARD CONN.

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

DOCKING CONN.

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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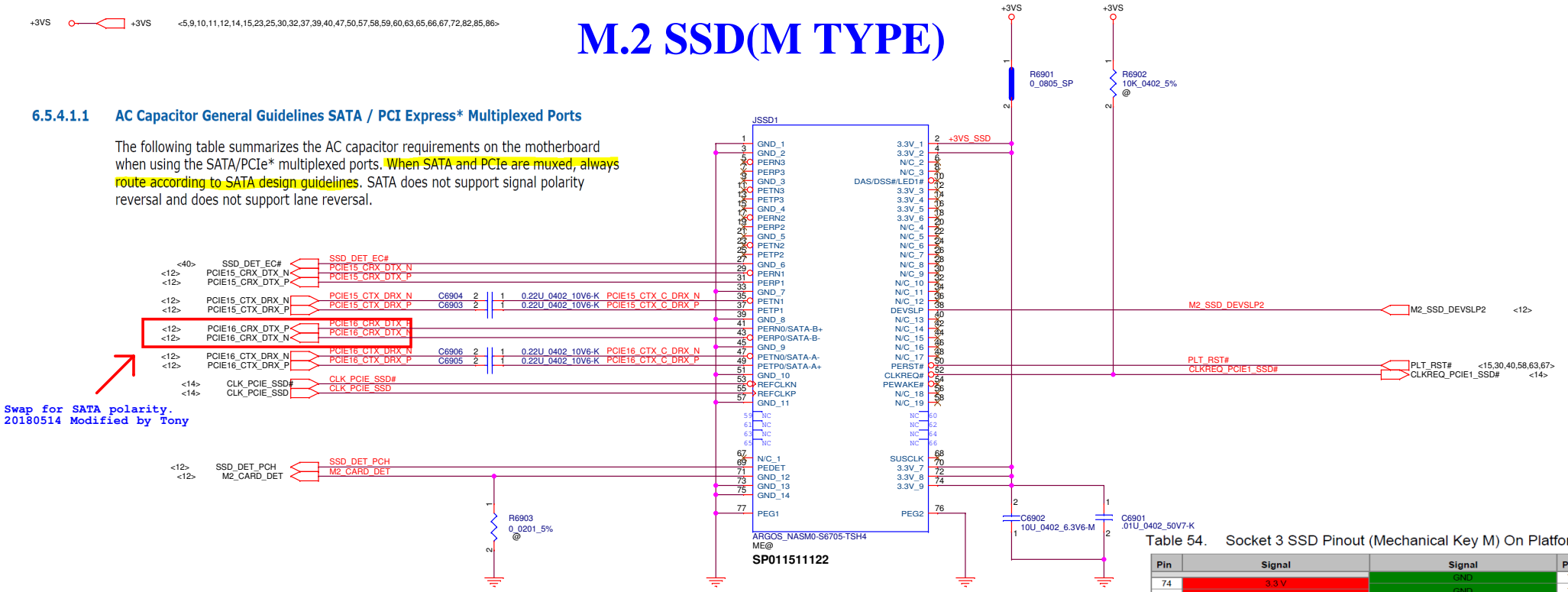
M.2 SSD(M TYPE)

+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,72,82,85,86>

6.5.4.1.1 AC Capacitor General Guidelines SATA / PCI Express* Multiplexed Ports

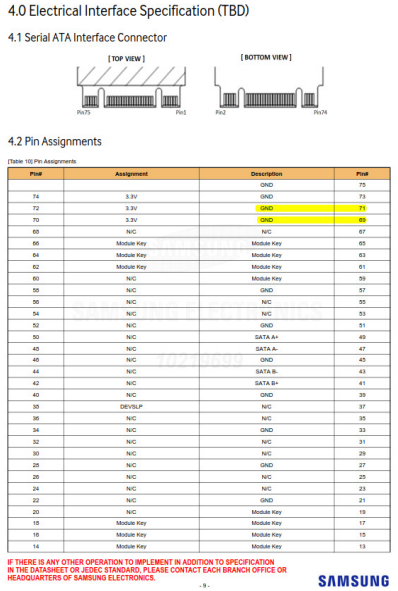
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports. When SATA and PCIe are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.



Swap for SATA polarity.
20180514 Modified by Tony

Table 6-16. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values (Sheet 1 of 2)

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

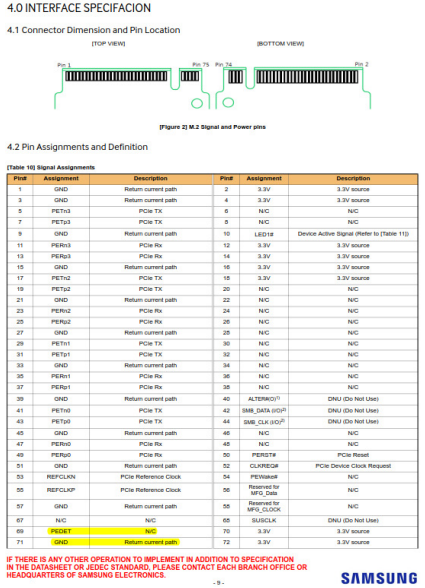

4.0 Electrical Interface Specification (TBD)

4.1 Serial ATA Interface Connector

4.2 Pin Assignments

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

SAMSUNG


4.0 INTERFACE SPECIFACION

4.1 Connector Dimension and Pin Location

[Figure 2] M.2 Signal and Power pins

4.2 Pin Assignments and Definition

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

SAMSUNG

Table 54. Socket 3 SSD Pinout (Mechanical Key M) On Platform

Pin	Signal	Signal	Pin
74	3.3 V	GND	75
72	3.3 V	GND	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	CONNECTOR Key M	NC	67
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or NC	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or NC	GND	51
50	PERST# (O)(0/3.3V) or NC	PETp0/SATA-A+	49
48	NC	PETn0/SATA-A-	47
46	NC	GND	45
44	ALERT# (I) (0/1.8V)	PERp0/SATA-B-	43
42	SMB_DATA (I/O) (0/1.8V)	PERn0/SATA-B+	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	DEVSLP (O)	PETp1	37
36	NC	PETn1	35
34	NC	GND	33
32	NC	PERp1	31
30	NC	PERn1	29
28	NC	GND	27
26	NC	PETp2	25
24	NC	PETn2	23
22	NC	GND	21
20	NC	PERp2	19
18	3.3 V	PERn2	17
16	3.3 V	GND	15
14	3.3 V	PETp3	13
12	3.3 V	PETn3	11
10	DAS/DSS (I/O)/LED_1# (I)(0/3.3V)	GND	9
8	NC	PERp3	7
6	NC	PERn3	5
4	3.3 V	GND	3
2	3.3 V	GND	1

*Notice the Pin#43 and 41 for SATA and PCIE Combo Port.
Refer to PCI Express M.2 Specification

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Title: M.2 SLOT CONN.

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Title

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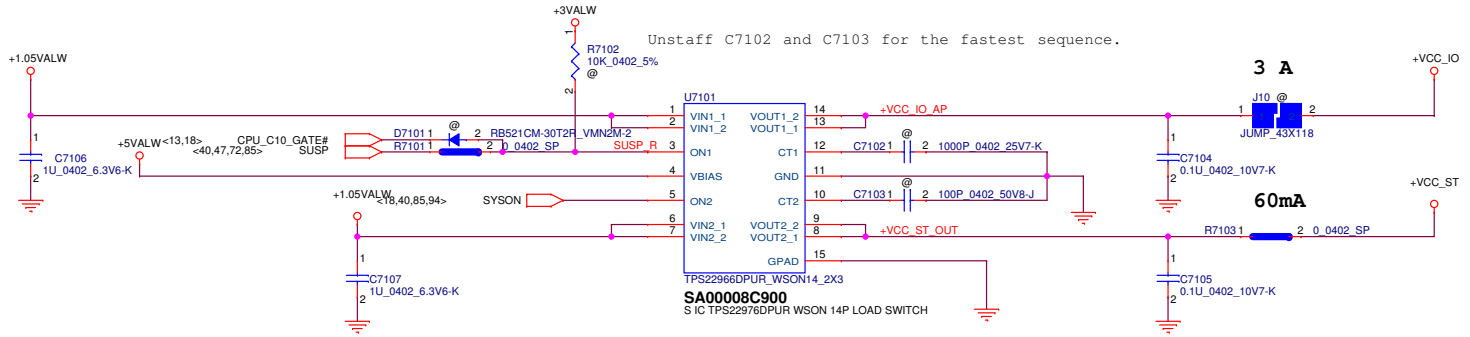
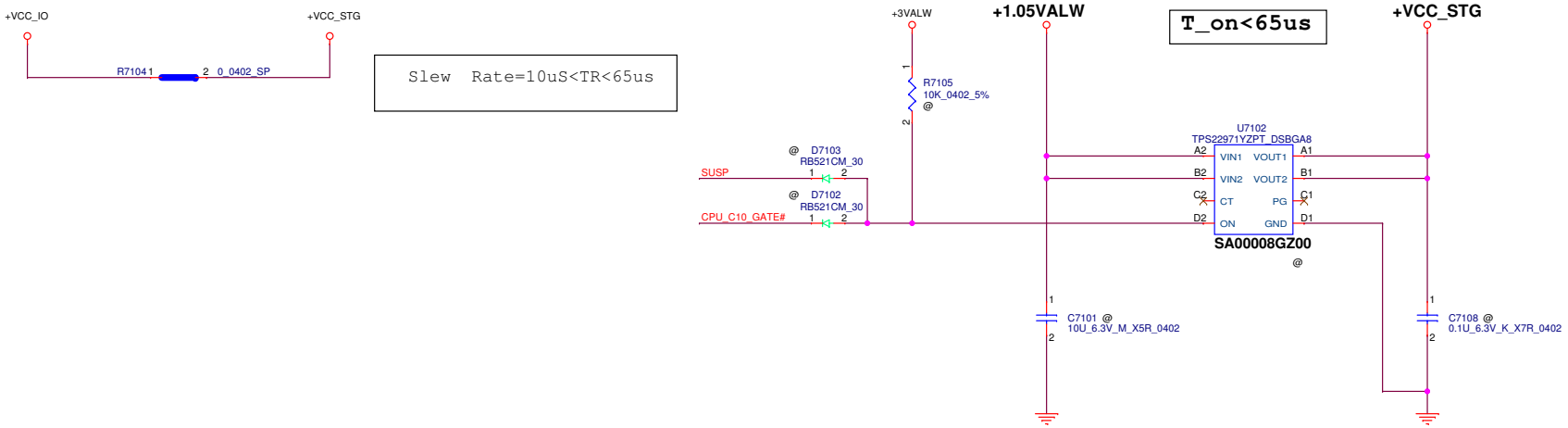
+1.05VALW	+1.05VALW	<19,21,92>
+VCC_STG	+VCC_STG	<8,16,18>
+VCC_IO	+VCC_IO	<5,11,18,21>
+5VALW	+5VALW	<38,39,41,42,43,47,62,64,66,67,72,84,85,86,87,88,89,91,93,94>
+VCC_ST	+VCC_ST	<8,15,16,18,86>
+3VALW	+3VALW	<6,9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,72,83,84,91,92,93,95>

TABLE of POWER SWITCH (U7101)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH

+1.05VALW to +VCC_IO_AP & +VCC_ST



Notice: TPS22976DPUR is common symbol with TPS22966DPUR



Title	VCCIO/VCCSTG/VCCST/+VCC	
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+5VALW — +5VALW <38,39,41,42,43,47,62,64,66,67,71,84,85,86,87,88,89,91,93,94>

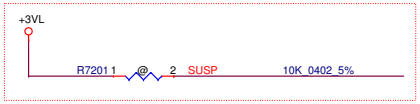
+5VS — +5VS <41,47,50,51,60,61,65,66>

+3VALW — +3VALW <6,9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,71,83,84,91,92,93,95>

+3VS — +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,82,85,86>

+3VL — +3VL <19,40,42,67,80,82,83,84>

B+ — B+ <47,60,80,83,84,85,86,87,88,89,91,92,95>



1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.

Smart Switch
+5VALW To +5VS
+3VALW To +3VS

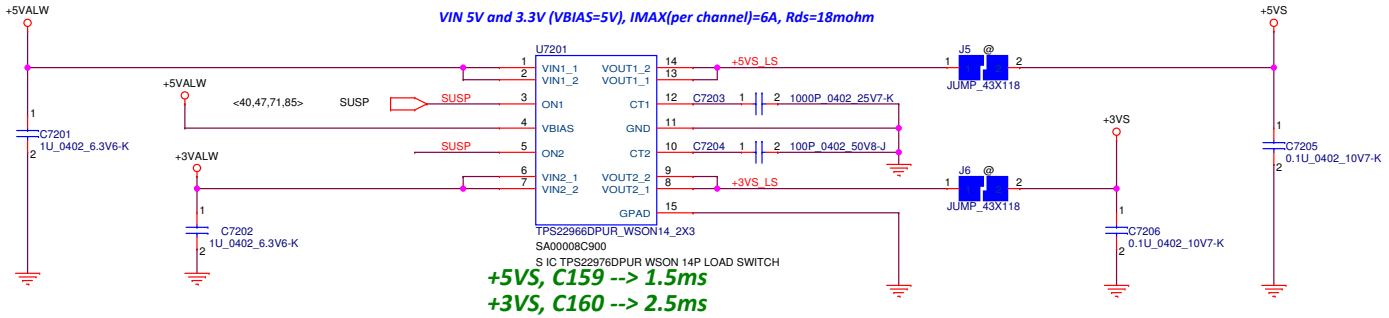
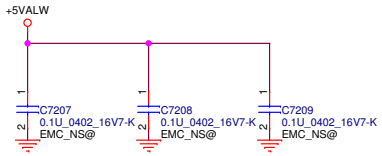
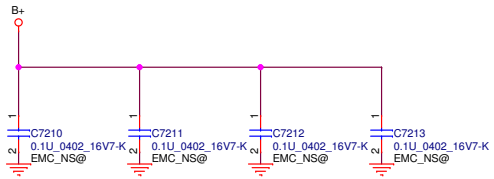


TABLE of POWER SWITCH (U7201)		
Vendor	**LCFC P/N**	**Description**
TI	**SA00008C900**	**S IC TPS22976DPUR WSON 14P LOAD SWITCH**
GMT	**SA00008F400**	**S IC G2898KD1U TDFN 14P LOAD SWITCH**





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Title: *DC V TO VS/ V-PCH*

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Screw Hole

CPU

H1 PAD_C5P0D3P4 H2 PAD_C6P0D3P4 H3 PAD_C6P0D3P4 H4 PAD_C6P0D3P4

WLAN

H24 PAD_C6P0D3P3

H5 PAD_C3P0D2P4 H6 PAD_C6P0D2P8 H7 PAD_CT6P0B8P0D2P3 H8 PAD_C8P0D2P5 H9 PAD_O2P6X3P2D2P6X3P2 H10 PAD_C2P8D2P3

H11 PAD_O2P6X3P65D2P6X3P65 H12 PAD_O2P3X2P8D2P3X2P8 H14 PAD_C8P0D2P3 H15 PAD_C2P8D2P3 H16 PAD_C2P8D2P3

H19 PAD_C2P8D2P3 H20 PAD_C6P0D2P3

H21 PAD_CT6P0B5P0D3P3

H23 PAD_C2P4D2P4N H22 PAD_O2P4X2P9D2P4X2P9N

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: SCREW HOLE

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Title

PLM BOM

Size	Document Number	Rev
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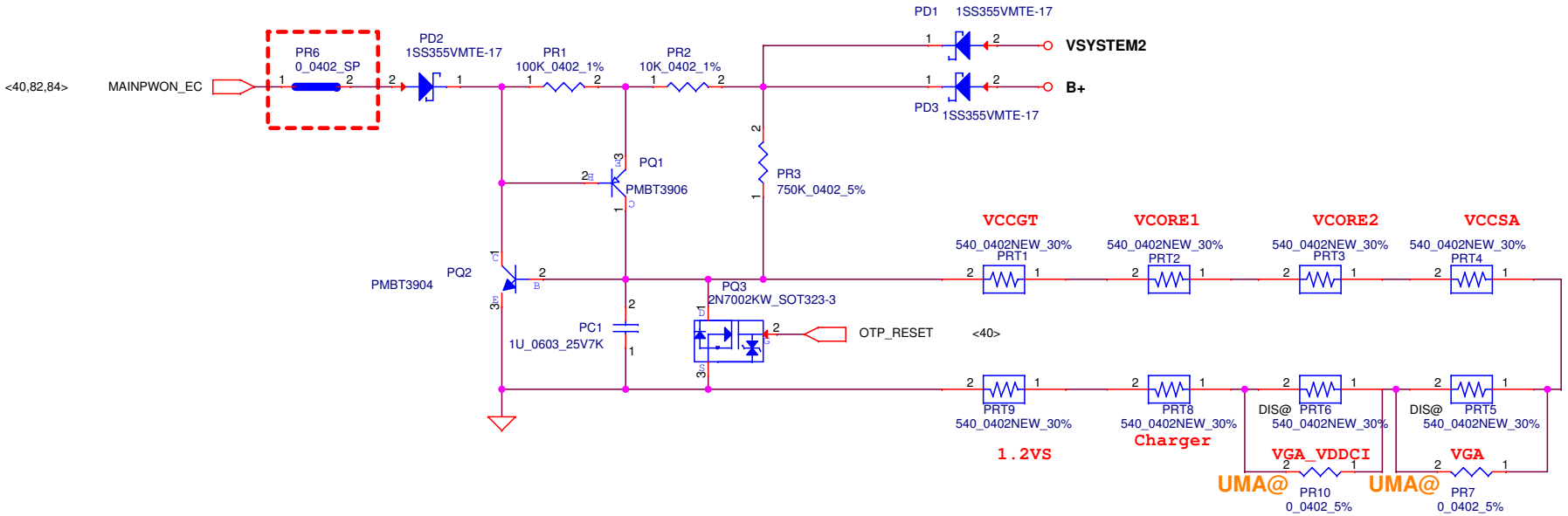
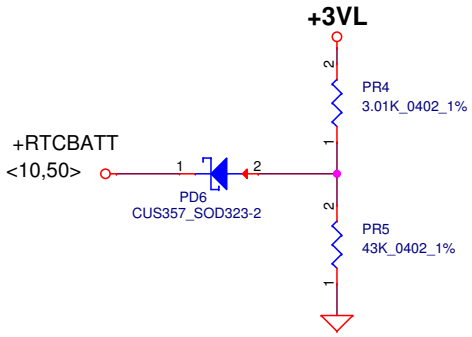


RTC Battery



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Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *VIN Detector*

Size	Document Number	Rev
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Title

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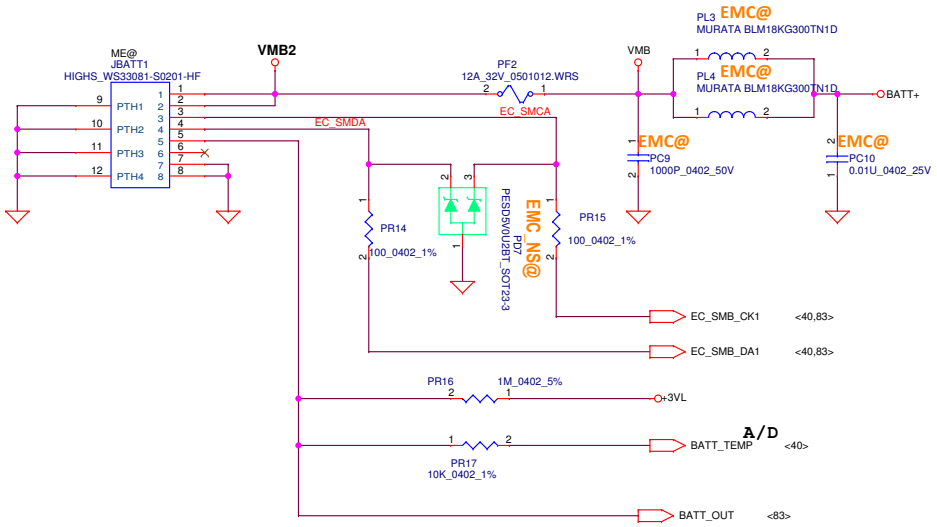
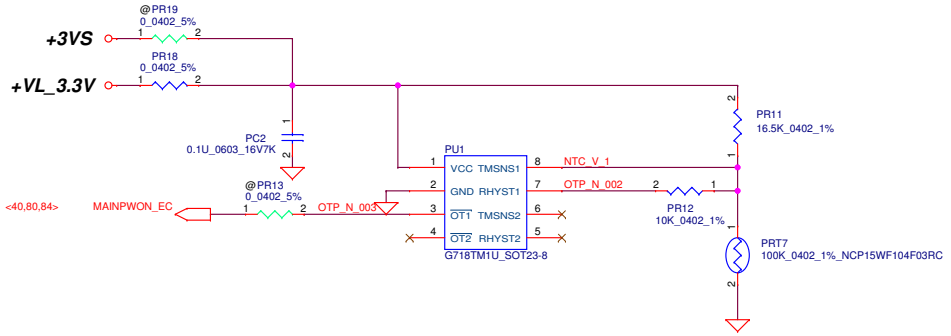


PRT7 under CPU bottom side for CPU thermal protection.
This is for thermal team request.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	BATTERY CONN/OTP		
Size: Custom	Document Number: EE490/590 NM-B911		Rev: 0.4
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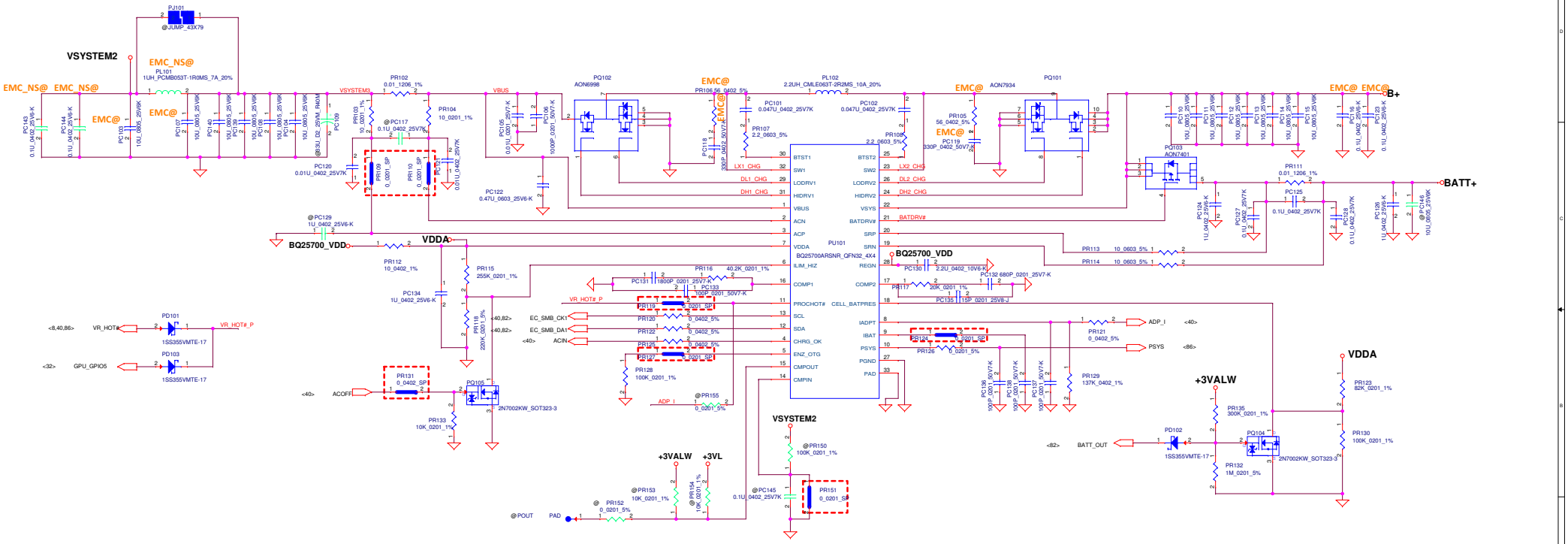

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: CHARGER

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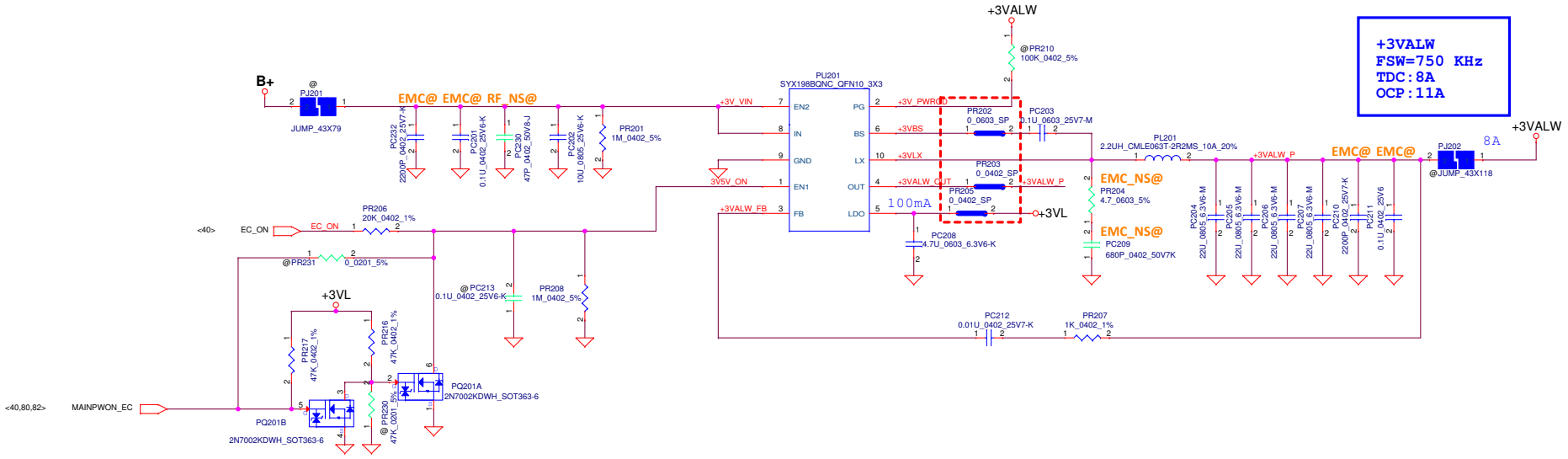

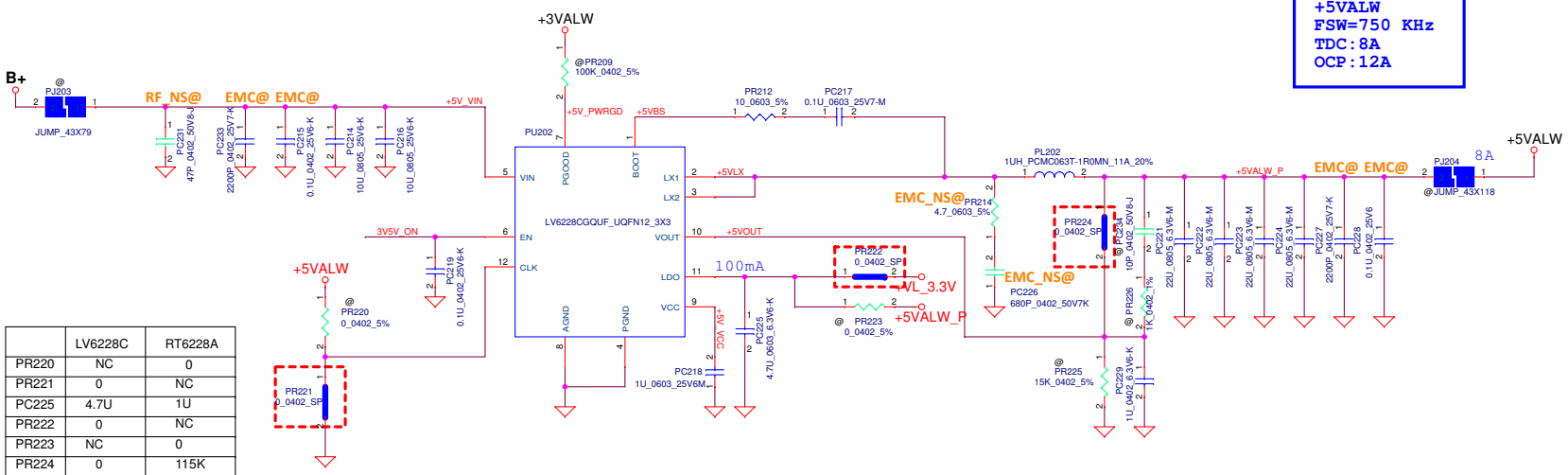

	LV6228C	RT6228A
PR220	NC	0
PR221	0	NC
PC225	4.7U	1U
PR222	0	NC
PR223	NC	0
PR224	0	115K
PR225	NC	15K
PC234	NC	10P
PR226	NC	1K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: 3VALW/5VALW

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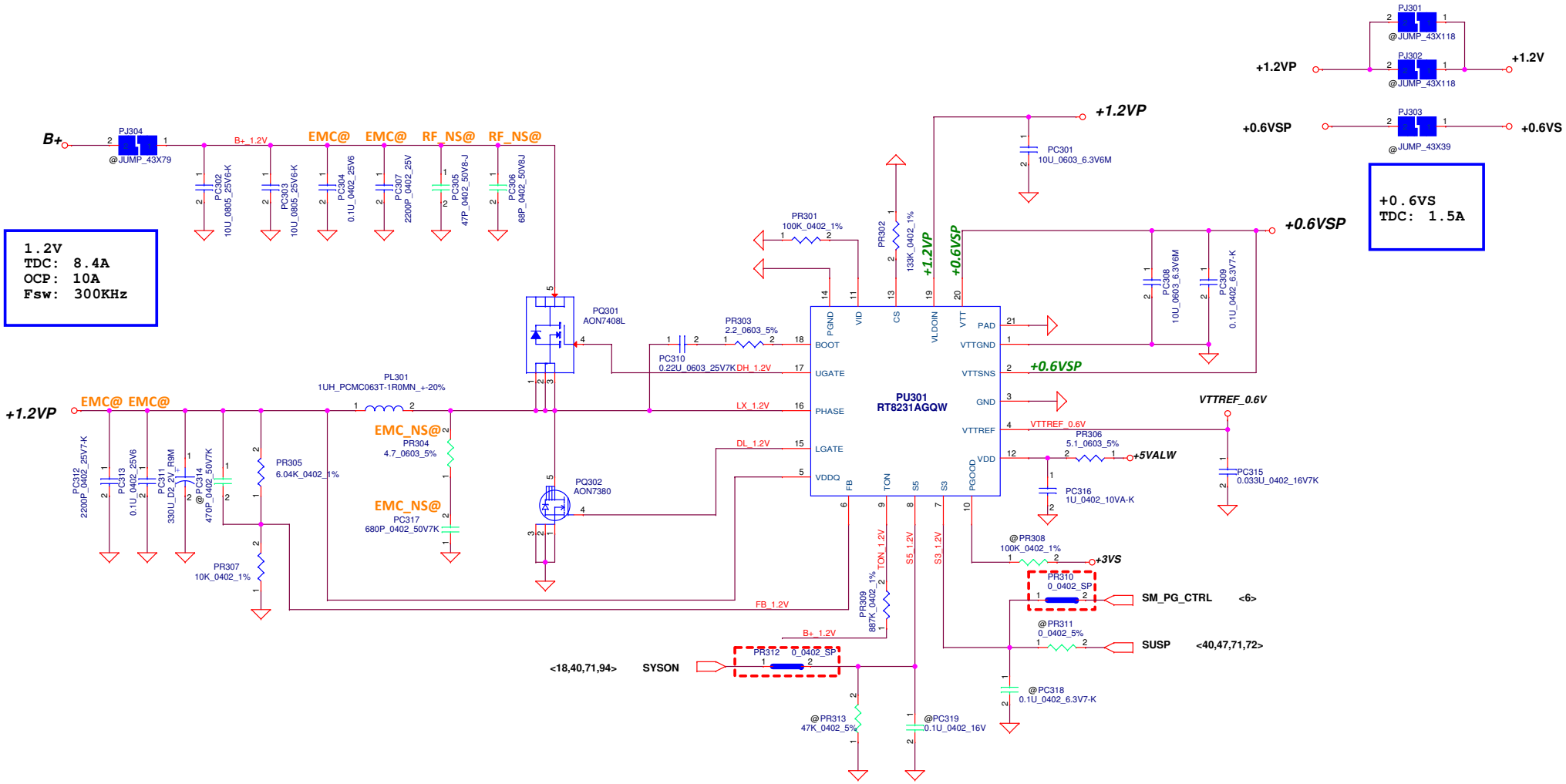
1.2V
TDC: 8.4A
OCP: 10A
Fsw: 300KHz
+0.6VS
TDC: 1.5A
PU301
RT8231AGQW
PJ304
@JUMP_43X79
PJ301
@JUMP_43X118
PJ302
@JUMP_43X118
PJ303
@JUMP_43X39
PQ301
AON7408L
PQ302
AON7380
PL301
1UH_PCMC063T-1R0MN_+-20%
PC301
10U_0603_6.3V6M
PC302
10U_0805_25V6-K
PC303
10U_0805_25V6-K
PC304
0.1U_0402_25V6
PC305
47P_0402_50V8-J
PC306
68P_0402_50V8J
PC307
2200P_0402_25V
PC308
10U_0603_6.3V6M
PC309
0.1U_0402_6.3V7-K
PC310
0.22U_0603_25V7K
PC312
2200P_0402_25V7-K
PC313
0.1U_0402_25V6
PC314
470P_0402_50V7K
PC315
0.033U_0402_16V7K
PC316
1U_0402_10VA-K
PC317
680P_0402_50V7K
@PC318
0.1U_0402_6.3V7-K
@PC319
0.1U_0402_16V
PR301
100K_0402_1%
PR302
133K_0402_1%
PR303
2.2_0603_5%
PR304
4.7_0603_5%
PR305
6.04K_0402_1%
PR306
5.1_0603_5%
PR307
10K_0402_1%
PR309
887K_0402_1%
@PR308
100K_0402_1%
PR310
0_0402_SP
@PR311
0_0402_5%
PR312
0_0402_SP
@PR313
47K_0402_5%
B+
B+_1.2V
+1.2VP
+1.2V
+0.6VSP
+0.6VS
+5VALW
+3VS
VTTREF_0.6V
EMC@
EMC_NS@
RF_NS@
PGND
VID
CS
VLDOIN
VTT
PAD
VTTGND
VTTSNS
GND
VTTREF
VDD
PGOOD
BOOT
UGATE
PHASE
LGATE
VDDQ
FB
TON
S5
S3
DH_1.2V
LX_1.2V
DL_1.2V
FB_1.2V
TON_1.2V
S5_1.2V
S3_1.2V
SM_PG_CTRL
<6>
SUSP
<40,47,71,72>
SYSON
<18,40,71,94>
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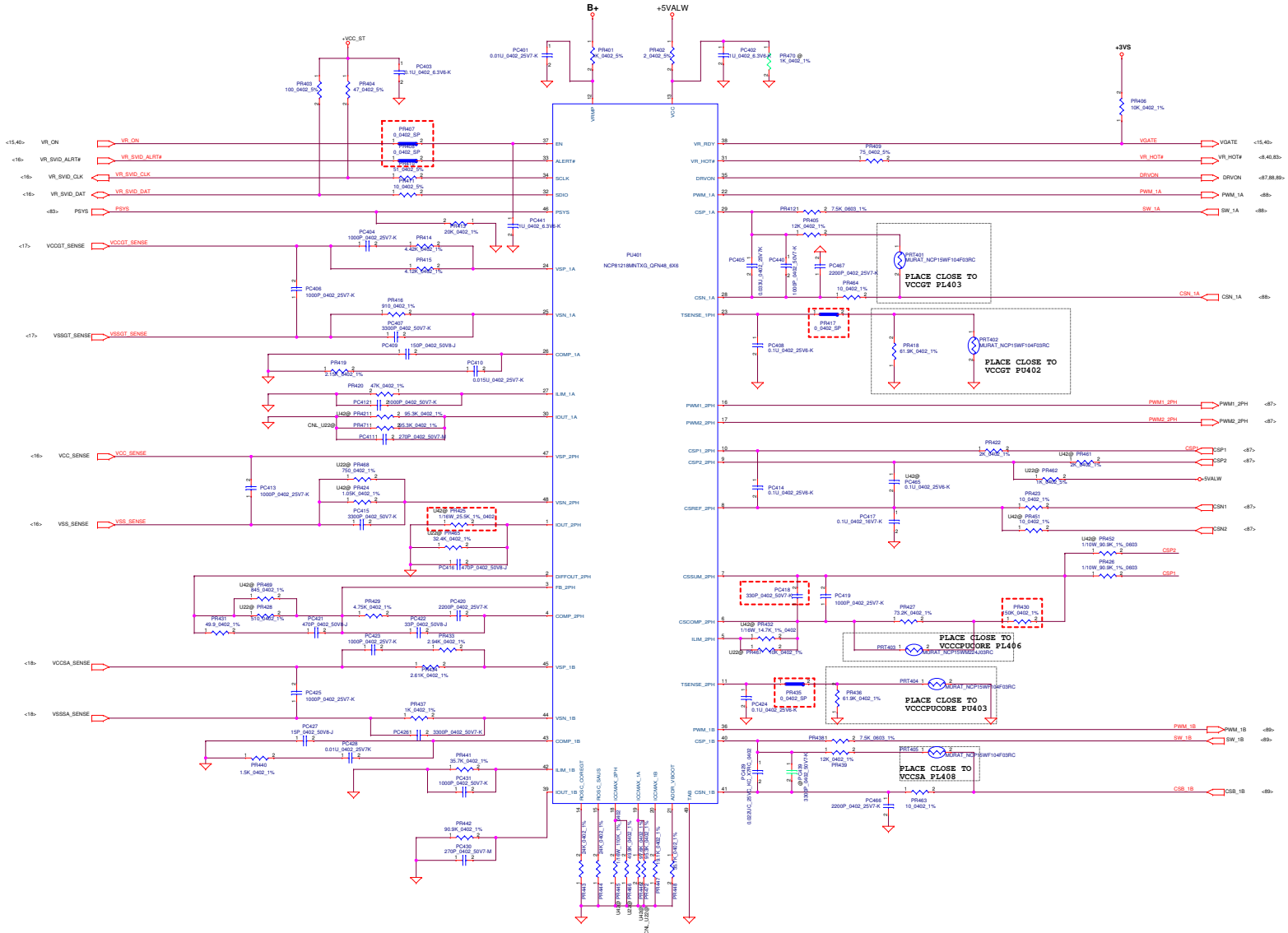

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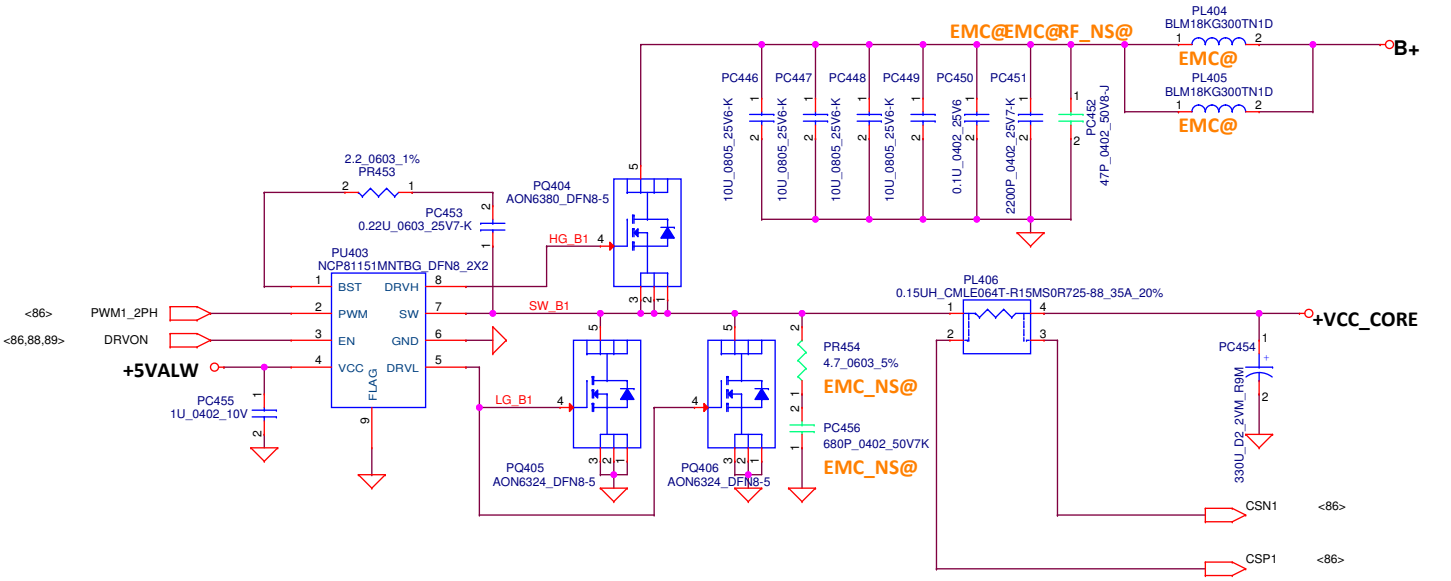
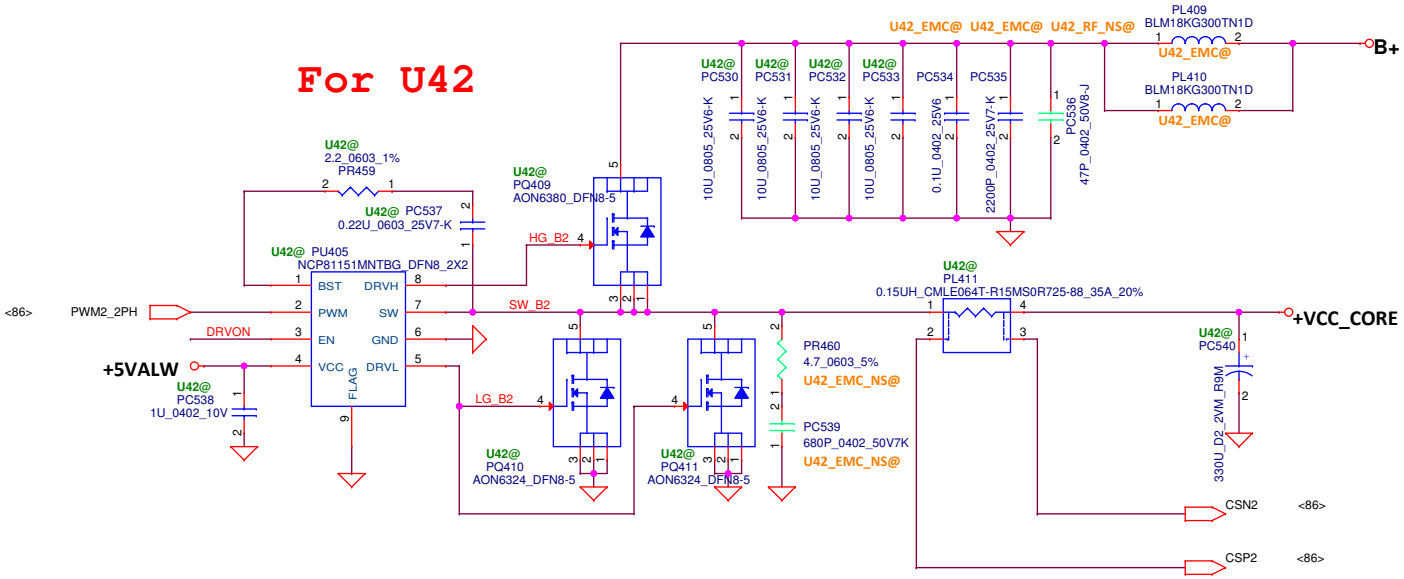


For U42

+VCC_CORE
TDC= 48A
IccMAX=70A
OCP=76A

For U22

+VCC_CORE
TDC= 21A
IccMAX=35A
OCP = 38A



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_CORE*

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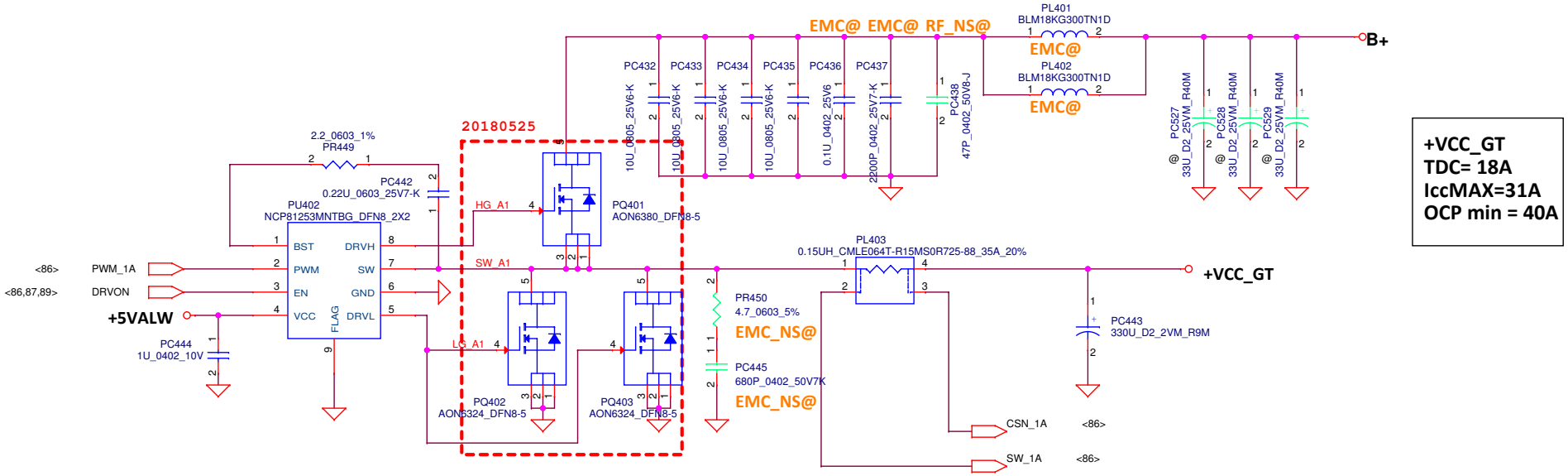

+VCC_GT
TDC= 18A
IccMAX=31A
OCP min = 40A

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_GT

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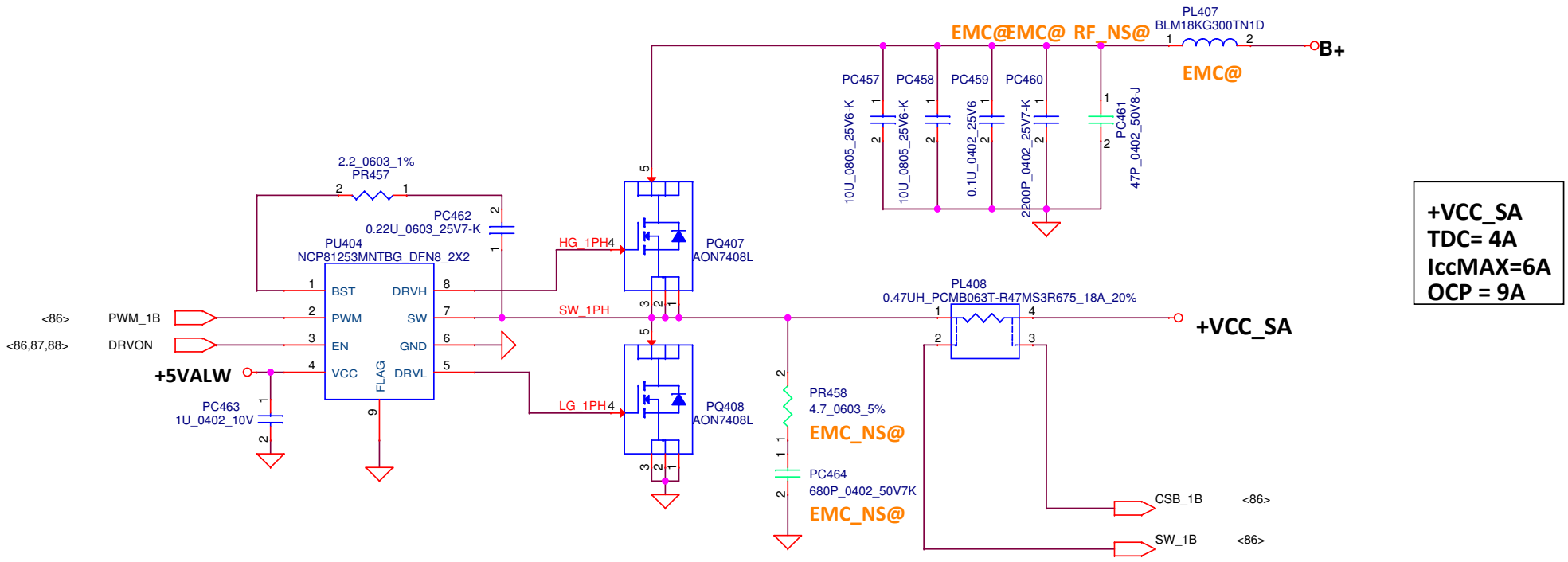

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_SA

Size: Custom	Document Number: EE490/590 NM-B911	Rev: 0.4
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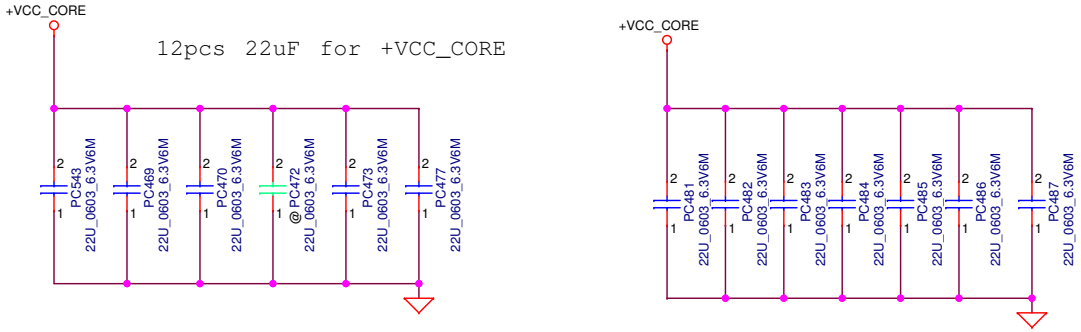

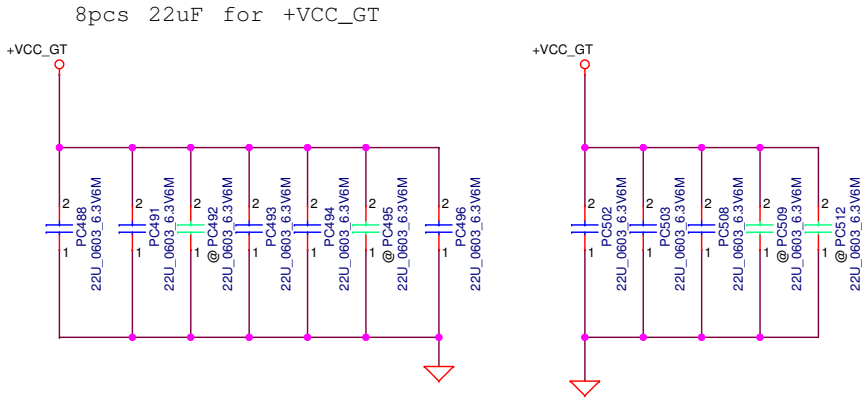

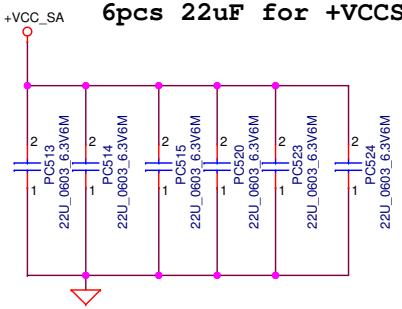

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

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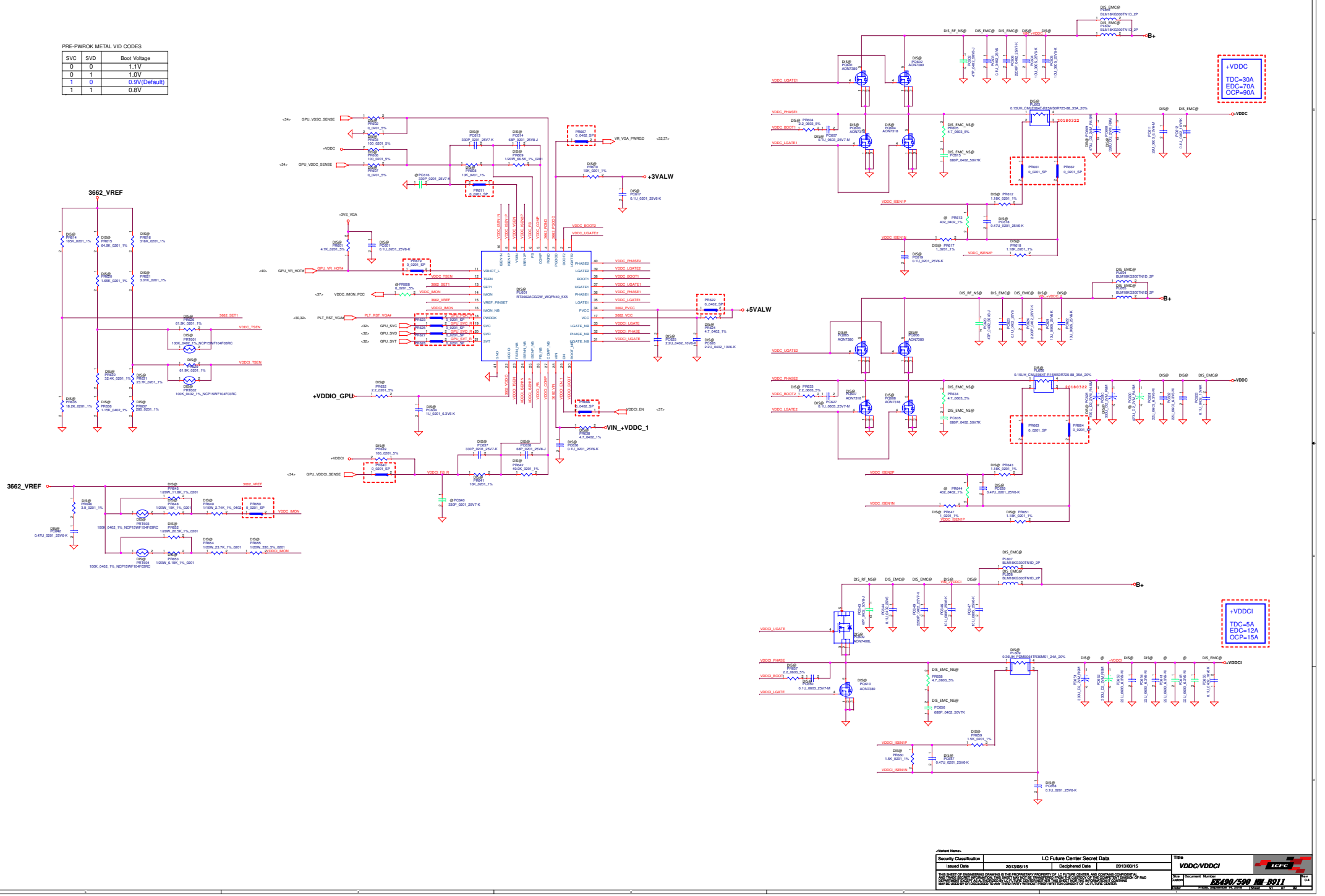
PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V



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Issued Date	2013/08/15	Deciphered Date	2013/08/15

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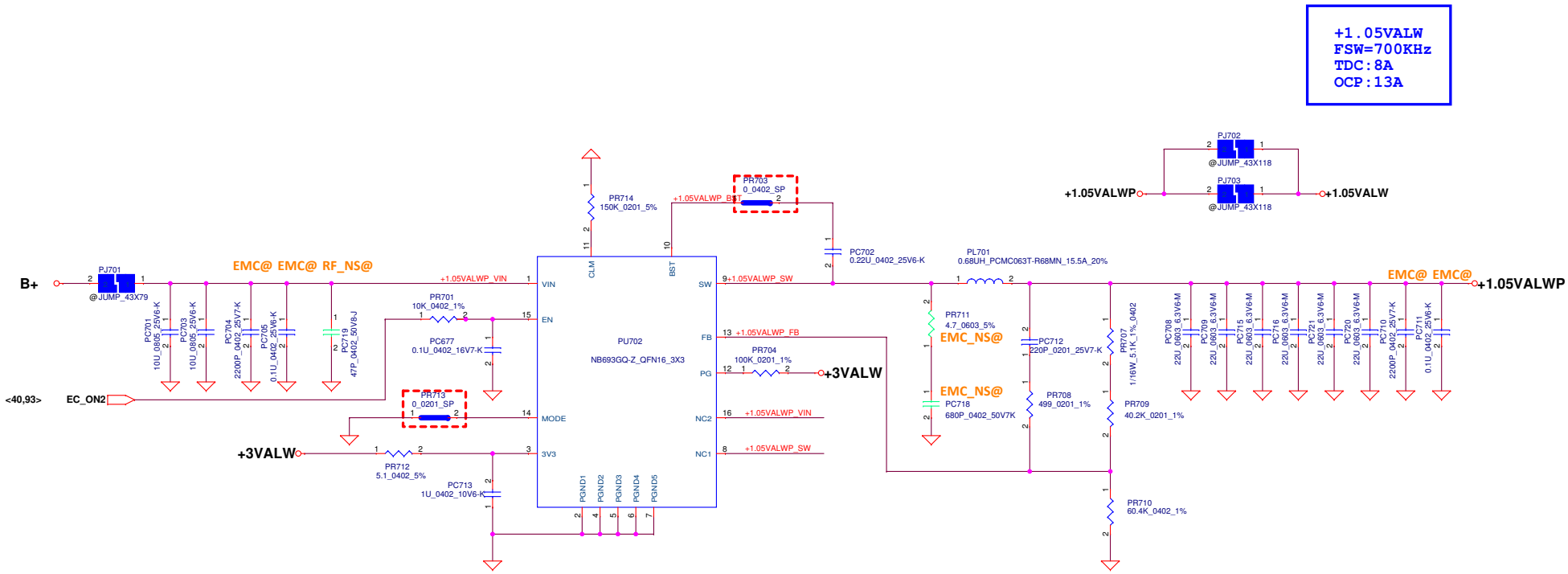

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1V

Size	Document Number	Rev
Custom	EE490/590 NM-B911	0.4

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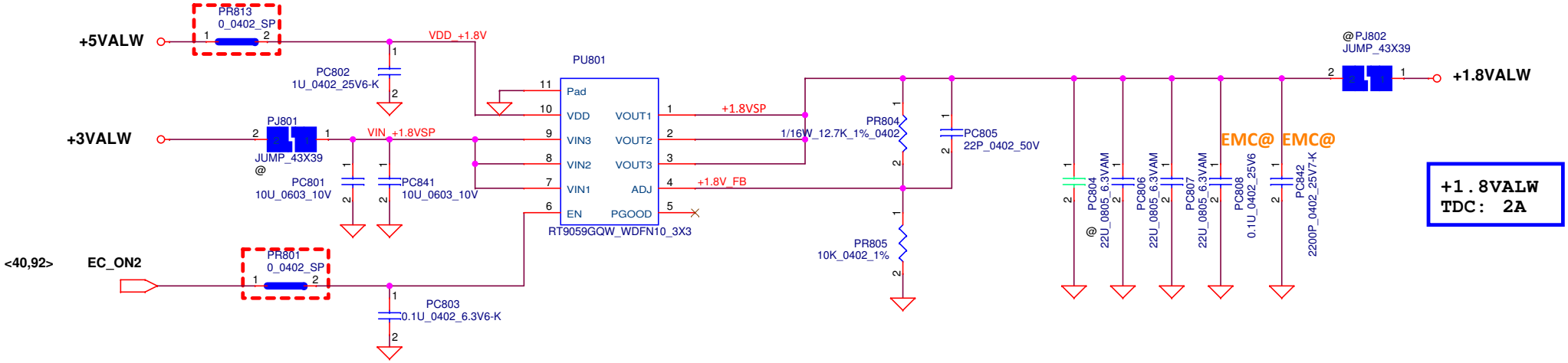

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+1.8VALW*

Size	Document Number	Rev
Custom	*EE490/590 NM-B911*	0.4

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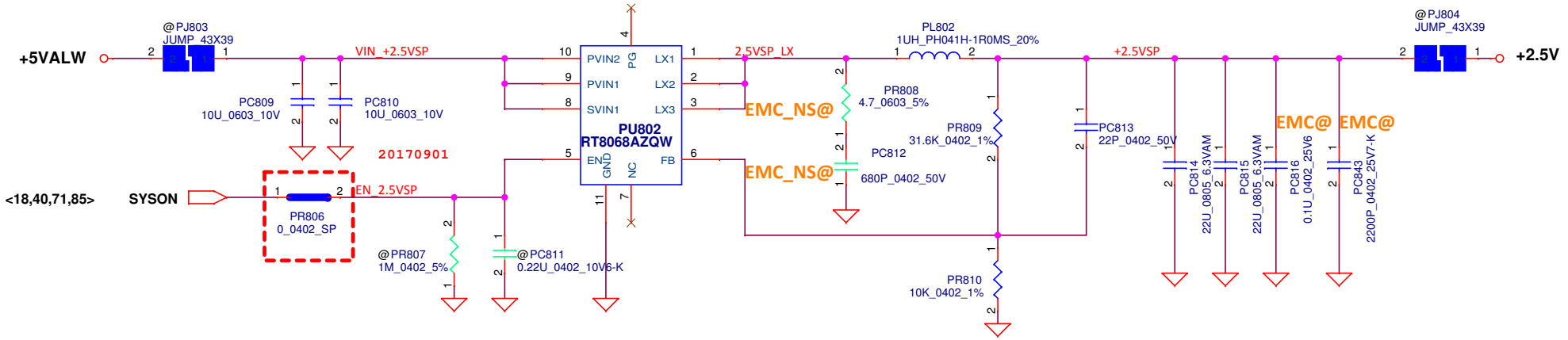
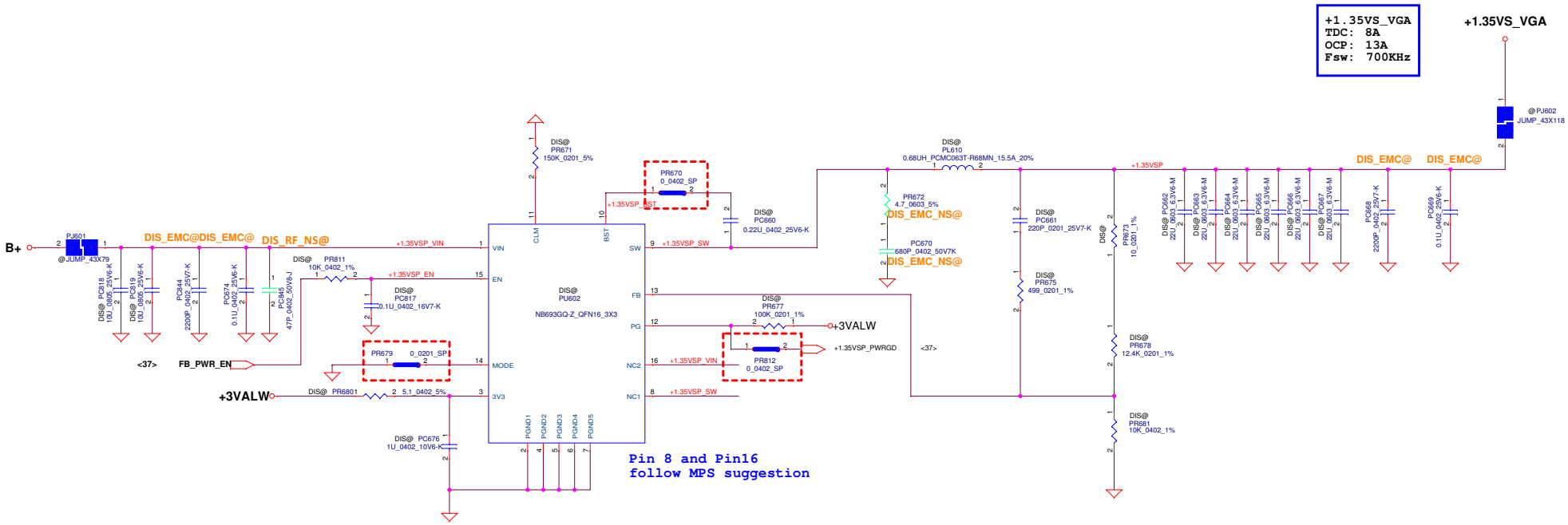


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

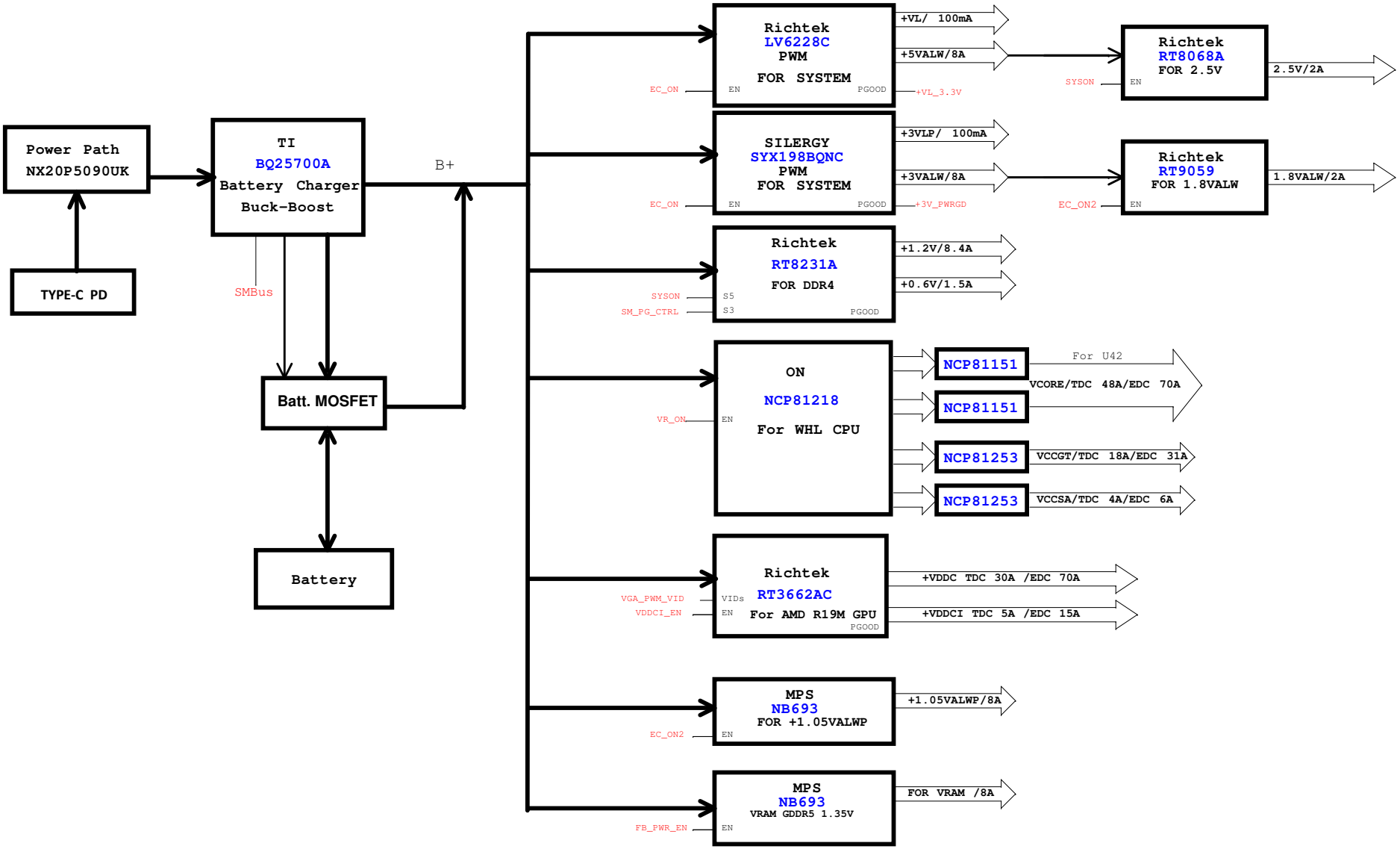
Title: +2.5V

Size: Custom	Document Number: EE490/590 NM-B911	Rev: 0.4
Date: Friday, September 14, 2018	Sheet 94 of 99	



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.35VS_VGA		
Size	Document Number		Rev
Custom	EE490/590 NM-B911		0.4
Date:	Friday, September 14, 2018	Sheet	95 of 99



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Title: *Power Block Diagram*

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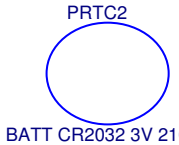

RTC@

EE480

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Title: XXXX

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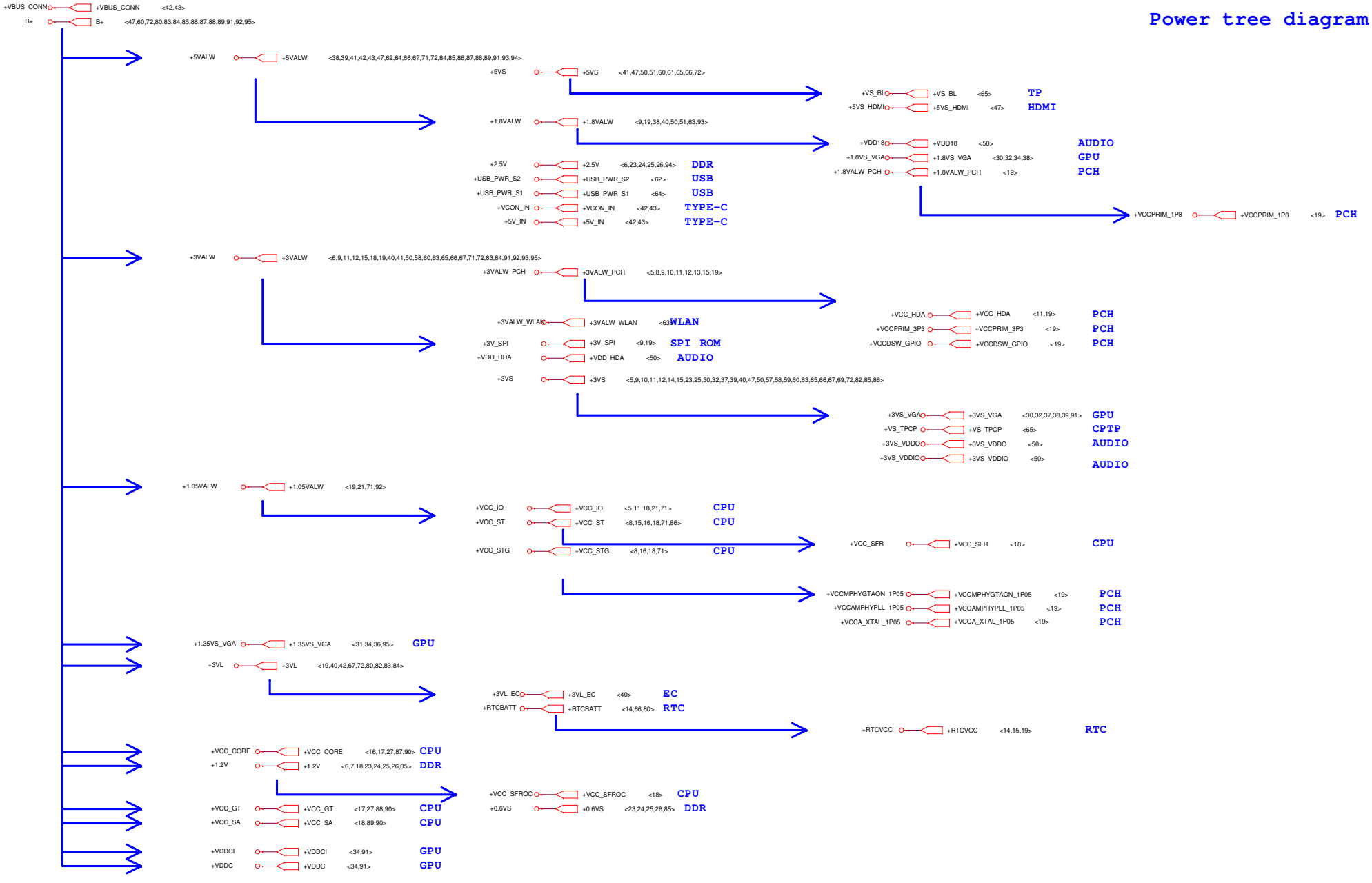
Power tree diagram



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