LCFC Confidential

KENOBI NM-A821 Rev2.0 Schematic

Intel KabyLake Processor with DDR4 + PCH-LP
NVIDA N16V-GMR GDDR3 2GB
2016-08-24 Rev2.0

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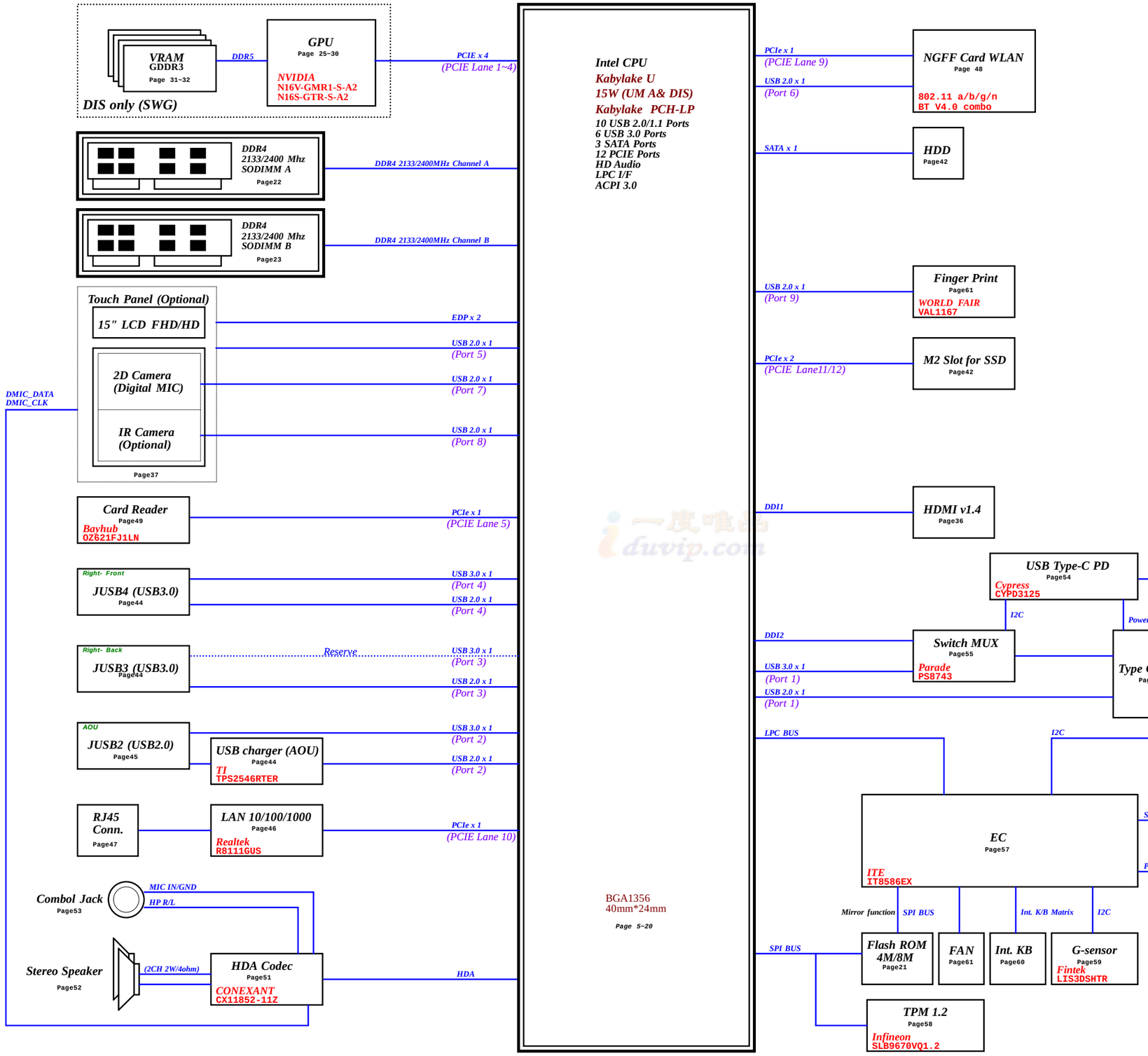
Kenobi KBL U Block Diagram



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Title	BLOCK DIAGRAM		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+ +3VL	+3VALW +5VALW +1VALW +1.8VALW	+2.5V +1.2V +VCC_STG	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VGA_CORE +3VS_VGA +1.5VS_VGA +3VS_AON +1VS_VGA +0.6VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#	SYSON
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	HIGH
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF	LOW
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF	LOW

SMBUS Control Table

	SOURCE	Main VGA	BATT (Charger)	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	LAN PHY	G sensor	USB Type-C
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580F +3VL	X	X	X	X	X	X	X	X	X	V +3VPD_VDD
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	V +3VS_GS	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	X	X	X	V +5VS	X	X	X
PCH_SML1CLK PCH_SML1DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	X	X

USB2 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3
4	JUSB4
5	Touch Panel
6	BT
7	CMOS
8	IR CAMERA
9	FP/Smart

USB3 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3
4	JUSB4

PCIE Port

Port	Device
1	GPU
2	GPU
3	GPU
4	GPU
5	CardReader
6	X
7	X
8	X
9	WLAN
10	LAN
11	M.2 SSD
12	M.2 SSD

SATA Port

Port	Device
1	HDD
2	X
3	X
4	X

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
SSD@	SSD setting
FRP@	Finger printer setting
TYPEC@	For USB Type-C function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
MIRROR@	For mirror function
NGC6@	For VGA Non GC6 function
GC6@	For VGA GC6 function

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Title: NOTE LIST

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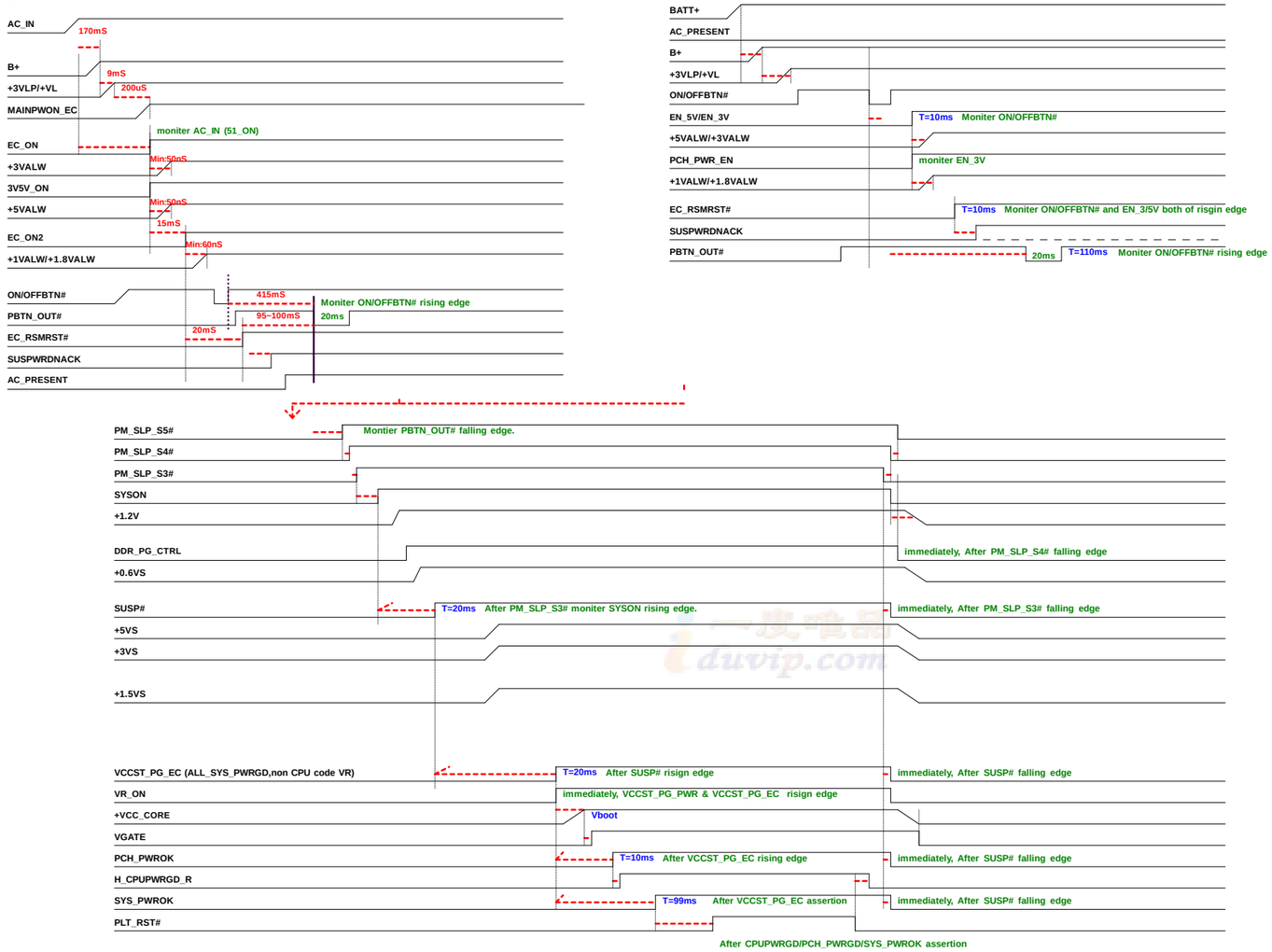
[KENOBI PWR Sequence_SKL-U_DDR4_Non-Deep Sx]

[AC Mode]



[DC Mode]

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Title	Power Sequence	
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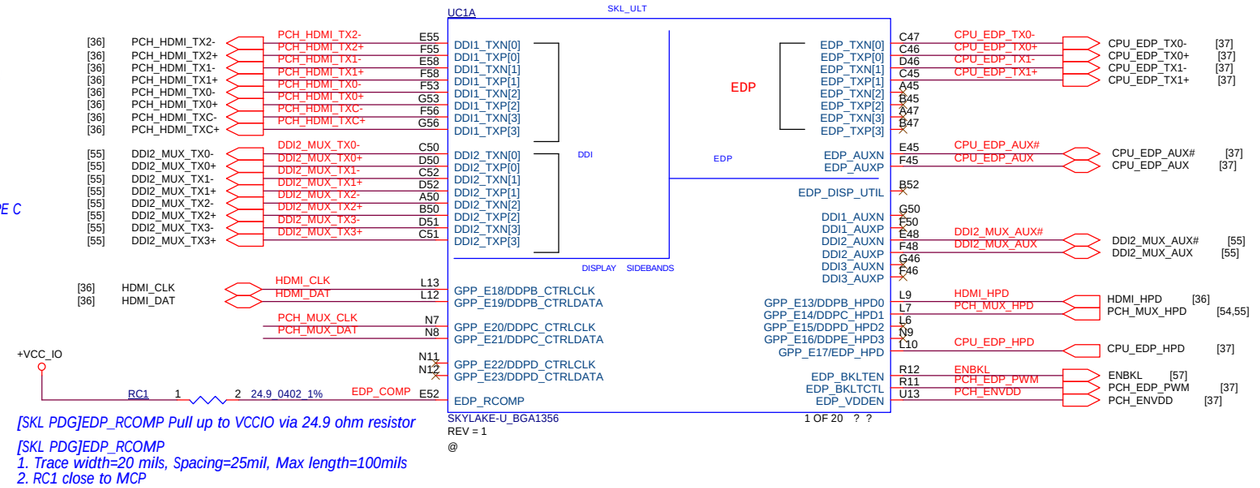
HDMI

USB TYPE C

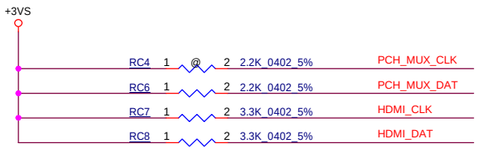


[SKL PDG]EDP_RCOMP Pull up to VCCIO via 24.9 ohm resistor

[SKL PDG]EDP_RCOMP
1. Trace width=20 mils, Spacing=25mil, Max length=100mils
2. RC1 close to MCP

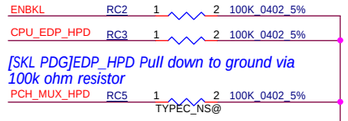
EDP

DDPB_CTRLDATA, DDPC_CTRLDATA Internal PD 20K



20160218
Staff RC7/RC8 for HDMI detect issue

DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1–3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1–3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.



[SKL PDG]EDP_HPD Pull down to ground via 100k ohm resistor

20160824
Change RC5 from @ to TYPEC_NS@
(Only for Non Type-C SKU)

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Title: **KBL(1/16):DDI/EDP**

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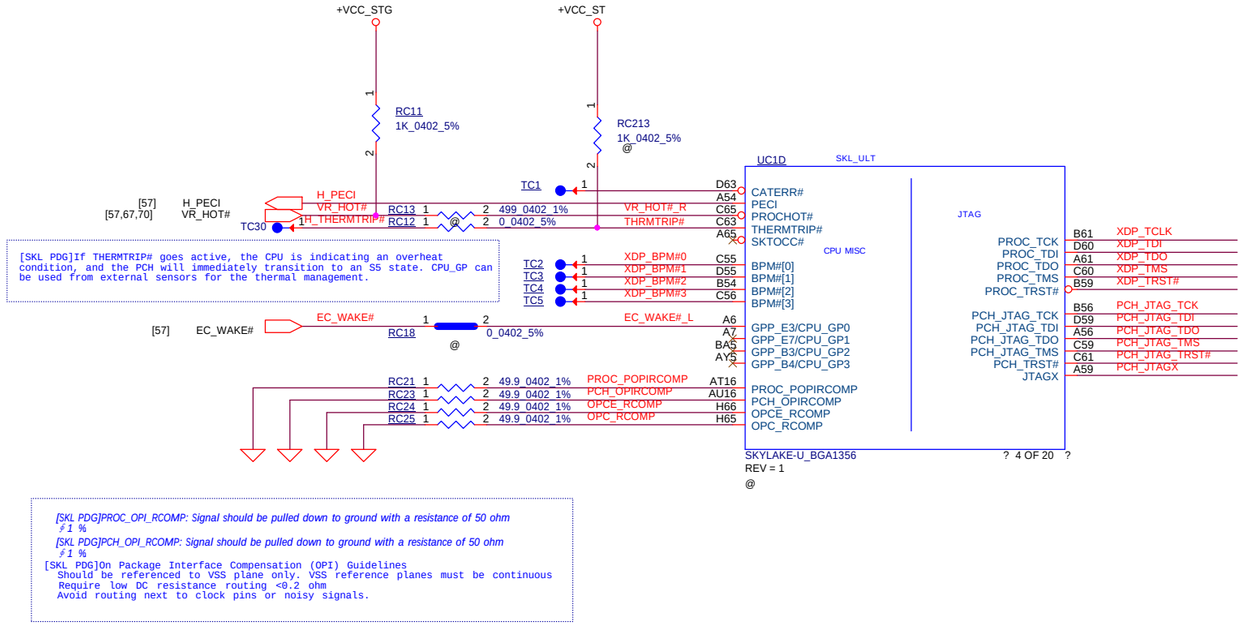
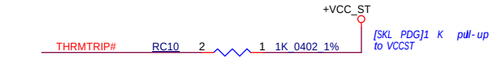
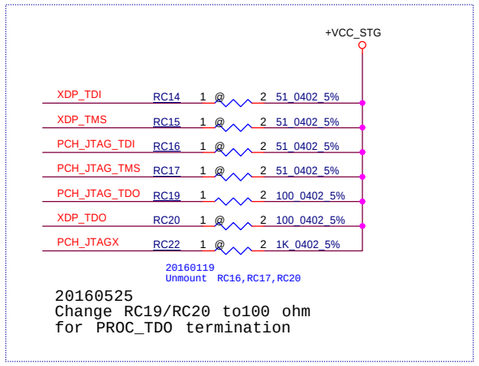


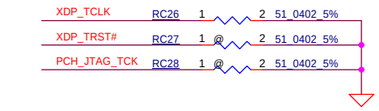
[SKL PDG]PROC_OPI_RCOMP: Signal should be pulled down to ground with a resistance of 50 ohm ≠1 %

[SKL PDG]PCH_OPI_RCOMP: Signal should be pulled down to ground with a resistance of 50 ohm ≠1 %

[SKL PDG]On Package Interface Compensation (OPI) Guidelines
Should be referenced to VSS plane only. VSS reference planes must be continuous
Require low DC resistance routing <0.2 ohm
Avoid routing next to clock pins or noisy signals.







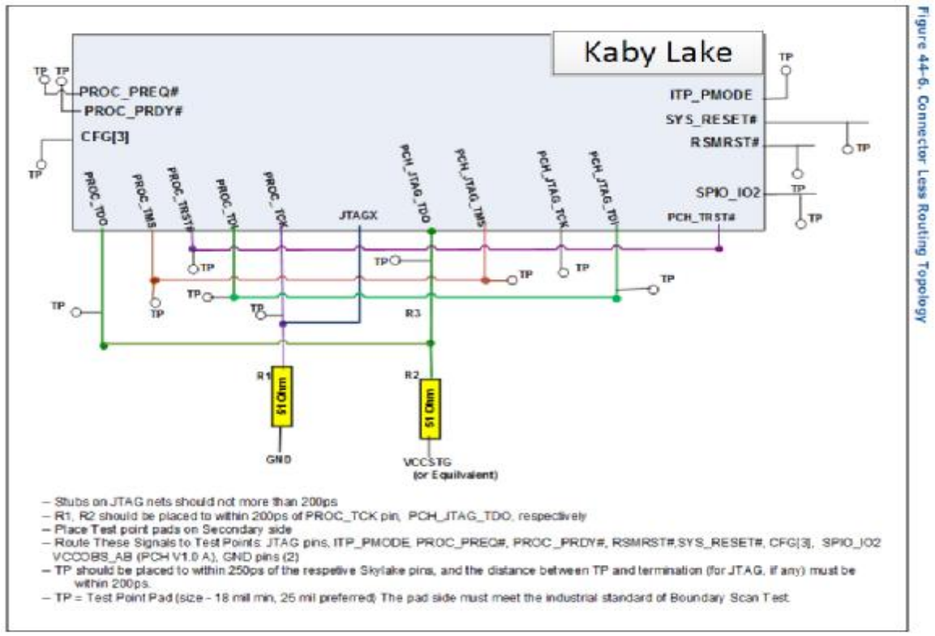
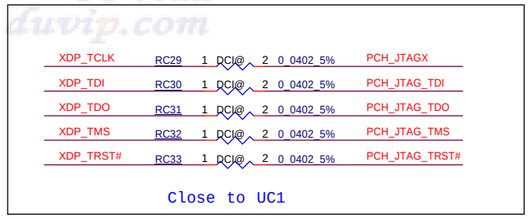


Figure 4-4-6. Connector Less Routing Topology

– Stubs on JTAG nets should not more than 200ps
– R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
– Place Test point pads on Secondary side
– Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2 VCCOBS_AB (PCH V1.0 A), GND pins (2)
– TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
– TP = Test Point Pad (size – 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.



Termination option

XDP_TCLK

PROC_TCK Termination:
51 ohm +/- 5% pull down to GNG (Ground)
Placed to within 200ps (1100 mil) or PROC_TCK pin

PCH_JTAG_TDO

PCH_JTAG_TDO Termination:
51ohm +/- 5% pull up to VccSTG or equivalent.
Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin

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Title: KBL(2/16):MISC/JTAG

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TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

[22] DDR_A_D[63..0]

UC1B SKL_ULT

DDR CH - A

SKYLAKE-U_BGA1356
REV = 1
@

2 OF 20 ?

DDR_A_MA[0..16] [22]

DDR_A_DQS#[0..7] [22]

DDR_A_DQS[0..7] [22]

DDR_A_CKE0 [22]
DDR_A_CKE1 [22]

DDR_A_CS0# [22]
DDR_A_CS1# [22]
DDR_A_ODT0 [22]
DDR_A_ODT1 [22]

DDR_A_BG0 [22]

DDR_A_ACT_N [22]
DDR_A_BG1 [22]

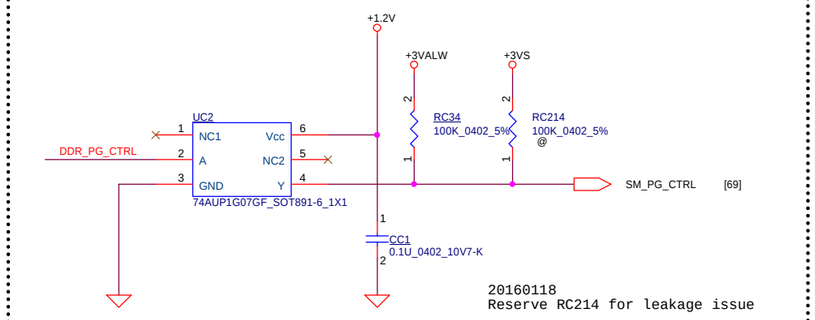
DDR_A_BA0 [22]
DDR_A_BA1 [22]

DDR_A_DDRCLK0_1866M# [22]
DDR_A_DDRCLK0_1866M [22]
DDR_A_DDRCLK1_1866M# [22]
DDR_A_DDRCLK1_1866M [22]

DDR_A_ALERT_N [22]
DDR_A_PARITY [22]

DDR4_VREF_CA_CPU_A [22]
DDR4_VREF_DQ_CPU_B [23]

TC31



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Title: KBL(3/16):DDR4 CH.A

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TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF85	DDR1_DQ[0]	DDR0_DQ[16]
	AF84	DDR1_DQ[1]	DDR0_DQ[17]
	AK85	DDR1_DQ[2]	DDR0_DQ[18]
	AK84	DDR1_DQ[3]	DDR0_DQ[19]
	AF86	DDR1_DQ[4]	DDR0_DQ[20]
	AF87	DDR1_DQ[6]	DDR0_DQ[21]
	AK87	DDR1_DQ[6]	DDR0_DQ[22]
	AK86	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF88	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH88	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF89	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH89	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT86	DDR1_DQ[16]	DDR0_DQ[48]
	AU86	DDR1_DQ[17]	DDR0_DQ[49]
	AP85	DDR1_DQ[18]	DDR0_DQ[50]
	AN85	DDR1_DQ[19]	DDR0_DQ[51]
	AN86	DDR1_DQ[20]	DDR0_DQ[52]
	AP86	DDR1_DQ[21]	DDR0_DQ[53]
	AT85	DDR1_DQ[22]	DDR0_DQ[54]
	AU85	DDR1_DQ[23]	DDR0_DQ[55]
	AT81	DDR1_DQ[24]	DDR0_DQ[56]
	AU81	DDR1_DQ[25]	DDR0_DQ[57]
	AP80	DDR1_DQ[26]	DDR0_DQ[58]
	AN80	DDR1_DQ[27]	DDR0_DQ[59]
	AN81	DDR1_DQ[28]	DDR0_DQ[60]
	AP81	DDR1_DQ[29]	DDR0_DQ[61]
	AT80	DDR1_DQ[30]	DDR0_DQ[62]
	AU80	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AR37	DDR1_DQ[38]	DDR1_DQ[22]
	AT33	DDR1_DQ[39]	DDR1_DQ[23]
	AU33	DDR1_DQ[40]	DDR1_DQ[24]
	AU30	DDR1_DQ[41]	DDR1_DQ[25]
	AT30	DDR1_DQ[42]	DDR1_DQ[26]
	AR33	DDR1_DQ[43]	DDR1_DQ[27]
	AP33	DDR1_DQ[44]	DDR1_DQ[28]
	AR30	DDR1_DQ[45]	DDR1_DQ[29]
	AP30	DDR1_DQ[46]	DDR1_DQ[30]
		DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AT22	DDR1_DQ[57]	DDR1_DQ[57]
	AU22	DDR1_DQ[58]	DDR1_DQ[58]
	AU21	DDR1_DQ[59]	DDR1_DQ[59]
	AT21	DDR1_DQ[60]	DDR1_DQ[60]
	AN22	DDR1_DQ[61]	DDR1_DQ[61]
	AP22	DDR1_DQ[62]	DDR1_DQ[62]
	AP21	DDR1_DQ[63]	DDR1_DQ[63]
	AN21		

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY45	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

[23] DDR_B_D[0..63]

UC1C

SKL_ULT

DDR_B_D0 AF65
DDR_B_D1 AF64
DDR_B_D2 AK65
DDR_B_D3 AK64
DDR_B_D4 AF66
DDR_B_D5 AF67
DDR_B_D6 AK67
DDR_B_D7 AK66
DDR_B_D8 AF70
DDR_B_D9 AF68
DDR_B_D10 AH71
DDR_B_D11 AH68
DDR_B_D12 AF71
DDR_B_D13 AF69
DDR_B_D14 AH70
DDR_B_D15 AH69
DDR_B_D16 AT66
DDR_B_D17 AU66
DDR_B_D18 AP65
DDR_B_D19 AN65
DDR_B_D20 AN66
DDR_B_D21 AP66
DDR_B_D22 AT65
DDR_B_D23 AU65
DDR_B_D24 AT61
DDR_B_D25 AU61
DDR_B_D26 AP60
DDR_B_D27 AN60
DDR_B_D28 AN61
DDR_B_D29 AP61
DDR_B_D30 AT60
DDR_B_D31 AU60
DDR_B_D32 AU40
DDR_B_D33 AT40
DDR_B_D34 AT37
DDR_B_D35 AU37
DDR_B_D36 AR40
DDR_B_D37 AP40
DDR_B_D38 AP37
DDR_B_D39 AR37
DDR_B_D40 AT33
DDR_B_D41 AU33
DDR_B_D42 AU30
DDR_B_D43 AT30
DDR_B_D44 AR33
DDR_B_D45 AP33
DDR_B_D46 AR30
DDR_B_D47 AP30
DDR_B_D48 AU27
DDR_B_D49 AT27
DDR_B_D50 AT25
DDR_B_D51 AU25
DDR_B_D52 AP27
DDR_B_D53 AN27
DDR_B_D54 AN25
DDR_B_D55 AP25
DDR_B_D56 AT22
DDR_B_D57 AU22
DDR_B_D58 AU21
DDR_B_D59 AT21
DDR_B_D60 AN22
DDR_B_D61 AP22
DDR_B_D62 AP21
DDR_B_D63 AN21

DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
DDR1_DQ[30]/DDR0_DQ[62]
DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
DDR1_DQ[33]/DDR1_DQ[17]
DDR1_DQ[34]/DDR1_DQ[18]
DDR1_DQ[35]/DDR1_DQ[19]
DDR1_DQ[36]/DDR1_DQ[20]
DDR1_DQ[37]/DDR1_DQ[21]
DDR1_DQ[38]/DDR1_DQ[22]
DDR1_DQ[39]/DDR1_DQ[23]
DDR1_DQ[40]/DDR1_DQ[24]
DDR1_DQ[41]/DDR1_DQ[25]
DDR1_DQ[42]/DDR1_DQ[26]
DDR1_DQ[43]/DDR1_DQ[27]
DDR1_DQ[44]/DDR1_DQ[28]
DDR1_DQ[45]/DDR1_DQ[29]
DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
DDR1_DQ[49]
DDR1_DQ[50]
DDR1_DQ[51]
DDR1_DQ[52]
DDR1_DQ[53]
DDR1_DQ[54]
DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]

DDR CH - B

SKYLAKE-U_BGA1356
REV = 1
@

3 OF 20 ?

DDR1_CKN[0] AN45
DDR1_CKN[1] AN46
DDR1_CKP[0] AP45
DDR1_CKP[1] AP46
DDR_B_DDRCLK0_1866M# → DDR_B_DDRCLK0_1866M# [23]
DDR_B_DDRCLK1_1866M# → DDR_B_DDRCLK1_1866M# [23]
DDR_B_DDRCLK0_1866M → DDR_B_DDRCLK0_1866M [23]
DDR_B_DDRCLK1_1866M → DDR_B_DDRCLK1_1866M [23]

DDR1_CKE[0] AN56
DDR1_CKE[1] AP55
DDR1_CKE[2] AN55
DDR1_CKE[3] AP53
DDR_B_CKE0 → DDR_B_CKE0 [23]
DDR_B_CKE1 → DDR_B_CKE1 [23]

DDR1_CS#[0] BB42
DDR1_CS#[1] AY42
DDR1_ODT[0] BA42
DDR1_ODT[1] AW42
DDR_B_CS0# → DDR_B_CS0# [23]
DDR_B_CS1# → DDR_B_CS1# [23]
DDR_B_ODT0 → DDR_B_ODT0 [23]
DDR_B_ODT1 → DDR_B_ODT1 [23]

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AY48
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AP50
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] BA48
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] BB48
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AP48
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AP52
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AN50
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AN48
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AN53
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AN52
DDR_B_MA5 → DDR_B_MA5
DDR_B_MA9 → DDR_B_MA9
DDR_B_MA6 → DDR_B_MA6
DDR_B_MA8 → DDR_B_MA8
DDR_B_MA7 → DDR_B_MA7
DDR_B_BG0 → DDR_B_BG0 [23]
DDR_B_MA12 → DDR_B_MA12
DDR_B_MA11 → DDR_B_MA11
DDR_B_ACT_N → DDR_B_ACT_N [23]
DDR_B_BG1 → DDR_B_BG1 [23]

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] BA43
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AY43
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AY44
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AW44
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] BB44
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AY47
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] BA44
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AW46
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AY46
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] BA46
DDR1_MA[3] BB46
DDR1_MA[4] BA47
DDR_B_MA13 → DDR_B_MA13
DDR_B_MA15 → DDR_B_MA15
DDR_B_MA14 → DDR_B_MA14
DDR_B_MA16 → DDR_B_MA16
DDR_B_BA0 → DDR_B_BA0 [23]
DDR_B_MA2 → DDR_B_MA2
DDR_B_BA1 → DDR_B_BA1 [23]
DDR_B_MA10 → DDR_B_MA10
DDR_B_MA1 → DDR_B_MA1
DDR_B_MA0 → DDR_B_MA0
DDR_B_MA3 → DDR_B_MA3
DDR_B_MA4 → DDR_B_MA4

DDR1_DQSN[0]/DDR0_DQSN[2] AH66
DDR1_DQSP[0]/DDR0_DQSP[2] AH65
DDR1_DQSN[1]/DDR0_DQSN[3] AG69
DDR1_DQSP[1]/DDR0_DQSP[3] AG70
DDR1_DQSN[2]/DDR0_DQSN[6] AR66
DDR1_DQSP[2]/DDR0_DQSP[6] AR65
DDR1_DQSN[3]/DDR0_DQSN[7] AR61
DDR1_DQSP[3]/DDR0_DQSP[7] AR60
DDR1_DQSN[4]/DDR1_DQSN[2] AT38
DDR1_DQSP[4]/DDR1_DQSP[2] AR38
DDR1_DQSN[5]/DDR1_DQSN[3] AT32
DDR1_DQSP[5]/DDR1_DQSP[3] AR32
DDR1_DQSN[6] AR25
DDR1_DQSP[6] AR27
DDR1_DQSN[7] AR22
DDR1_DQSP[7] AR21
DDR_B_DQS#0 → DDR_B_DQS#0
DDR_B_DQS0 → DDR_B_DQS0
DDR_B_DQS#1 → DDR_B_DQS#1
DDR_B_DQS1 → DDR_B_DQS1
DDR_B_DQS#2 → DDR_B_DQS#2
DDR_B_DQS2 → DDR_B_DQS2
DDR_B_DQS#3 → DDR_B_DQS#3
DDR_B_DQS3 → DDR_B_DQS3
DDR_B_DQS#4 → DDR_B_DQS#4
DDR_B_DQS4 → DDR_B_DQS4
DDR_B_DQS#5 → DDR_B_DQS#5
DDR_B_DQS5 → DDR_B_DQS5
DDR_B_DQS#6 → DDR_B_DQS#6
DDR_B_DQS6 → DDR_B_DQS6
DDR_B_DQS#7 → DDR_B_DQS#7
DDR_B_DQS7 → DDR_B_DQS7

DDR1_ALERT# AN43
DDR1_PAR AP43
DRAM_RESET# AT13
DDR_RCOMP[0] AR18
DDR_RCOMP[1] AT18
DDR_RCOMP[2] AU18
DDR_B_ALERT_N → DDR_B_ALERT_N [23]
DDR_B_PARITY → DDR_B_PARITY [23]
DDR4_DRAMRST_N → DDR4_DRAMRST_N
SM_RCOMP0 → RC36 1 2 121_0402_1%
SM_RCOMP1 → RC38 1 2 80.6_0402_1%
SM_RCOMP2 → RC39 1 2 100_0402_1%

[KBL PDG]for DDR4 COMPENSATION
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

DDR_B_MA[0..16] [23]

DDR_B_DQS#[0..7] [23]

DDR_B_DQS[0..7] [23]

+1.2V
RC35 2 1 470_0402_5%
DDR4_DRAMRST_N
RC37 1 2 0_0402_5%
DDR4_DRAMRST# [22,23]
@

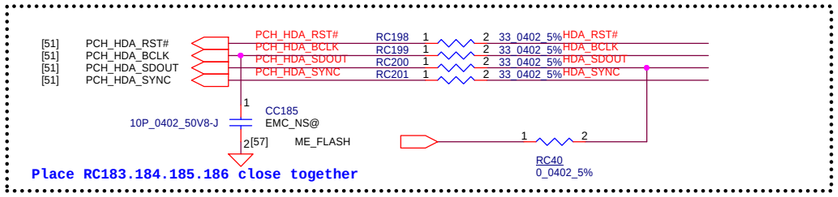
Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(4/16):DDR4 CH.B

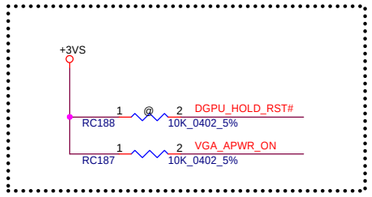
Size	Document Number	Rev
Custom	KENOBI	2.0

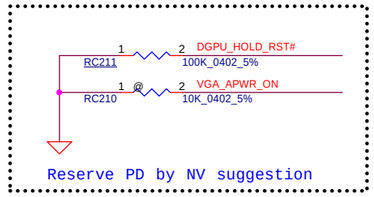
Date: Thursday, August 25, 2016 Sheet 8 of 82

[KBL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in
the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.



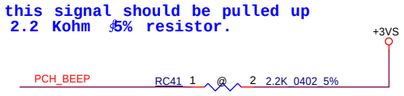
20160408
1.Unstaff RC188 and Staff RC211 with 100K resistor





Note:
SPKR (PC_BEEP) has an integrated weak pull-down resistor (20 K ohm nominal) to disable Top-Block Sway by default.

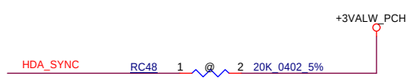
To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 Kohm ±5% resistor.

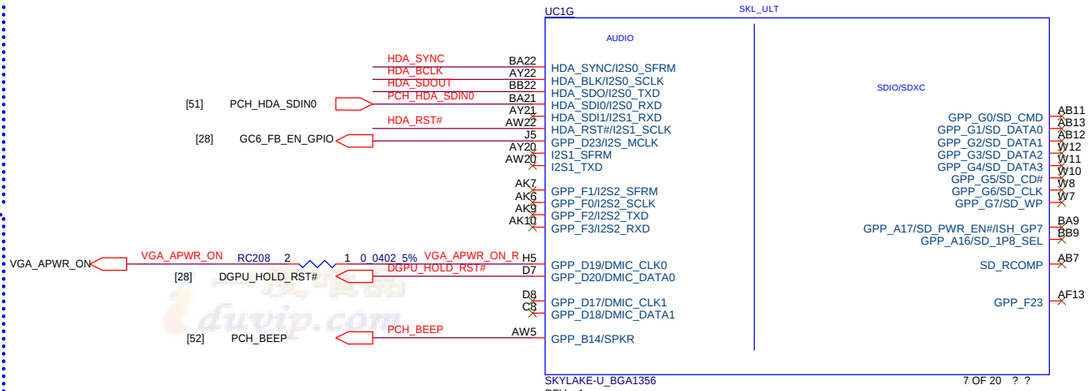


Note:
Internal PD 20K

Note:
HDA_SDO should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.

Note:
Internal PD 20K





[SKL PDG] internal SD Card

Not support internal SD card. Remove SD_RCOMP

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

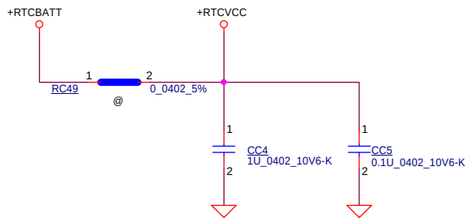
Title: KBL(5/16):HDA/SDIO

Size: Custom | Document Number: KENOBI | Rev: 2.0

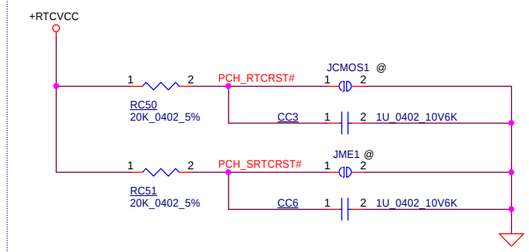
Date: Thursday, August 25, 2016 | Sheet 9 of 82

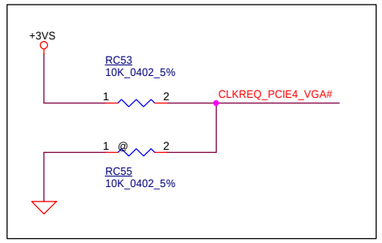
RTC External Circuit

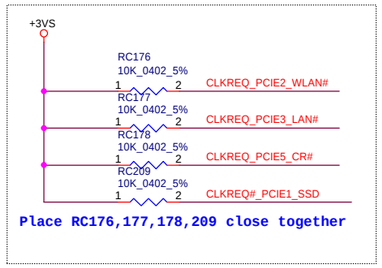
+RTCBATT, +RTCVCC
Trace width = 20mils



JCMOS, JME Setting, Need Under DDR Door







Place RC176,177,178,209 close together

UC1J — SKL_ULT — CLOCK SIGNALS

M.2 SSD	[42] CLK_PCIE_SSD#	CLK_PCIE_SSD#	B42	CLKOUT_PCIE_N1	GPP_B6/SRCCLKREQ1#
	[42] CLK_PCIE_SSD	CLK_PCIE_SSD	A42	CLKOUT_PCIE_P1	
	[42] CLKREQ#_PCIE1_SSD	CLKREQ#_PCIE1_SSD	AT7		
WLAN	[48] CLK_PCIE_WLAN#	CLK_PCIE_WLAN#	D41	CLKOUT_PCIE_N2	GPP_B7/SRCCLKREQ2#
	[48] CLK_PCIE_WLAN	CLK_PCIE_WLAN	C41	CLKOUT_PCIE_P2	
	[48] CLKREQ_PCIE2_WLAN#	CLKREQ_PCIE2_WLAN#	AT8		
LAN	[46] CLK_PCIE_LAN#	CLK_PCIE_LAN#	D40	CLKOUT_PCIE_N3	GPP_B8/SRCCLKREQ3#
	[46] CLK_PCIE_LAN	CLK_PCIE_LAN	C40	CLKOUT_PCIE_P3	
	[46] CLKREQ_PCIE3_LAN#	CLKREQ_PCIE3_LAN#	AT10		
VGA	[25] CLK_PCIE_VGA#	CLK_PCIE_VGA#	B40	CLKOUT_PCIE_N4	GPP_B9/SRCCLKREQ4#
	[25] CLK_PCIE_VGA	CLK_PCIE_VGA	A40	CLKOUT_PCIE_P4	
	[25] CLKREQ_PCIE4_VGA#	CLKREQ_PCIE4_VGA#	AU8		
CR	[49] CLK_PCIE_CR#	CLK_PCIE_CR#	E40	CLKOUT_PCIE_N5	GPP_B10/SRCCLKREQ5#
	[49] CLK_PCIE_CR	CLK_PCIE_CR	E38	CLKOUT_PCIE_P5	
	[49] CLKREQ_PCIE5_CR#	CLKREQ_PCIE5_CR#	AU7		

D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#

CLKOUT_ITPXDP_N E43
CLKOUT_ITPXDP_P E43

GPD8/SUSCLK BA17 SUSCLK_32K → SUSCLK_32K [48]

XTAL24_IN E37 PCH_XTAL24_IN
XTAL24_OUT E35 PCH_XTAL24_OUT

XCLK_BIASREF E42 DIFFCLK_BIASREF — 1 RC56 2 2.7K_0402_1% — +1VALW

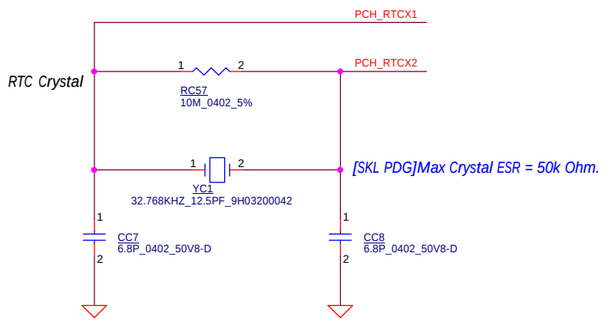
RTCX1 AM18 PCH_RTCX1
RTCX2 AM20 PCH_RTCX2

SRTCRST# AN18 PCH_SRTCRST#
RTCRST# AM16 PCH_RTCRST#

SKYLAKE-U_BGA1356
REV = 1
@
10 OF 20 ? ?

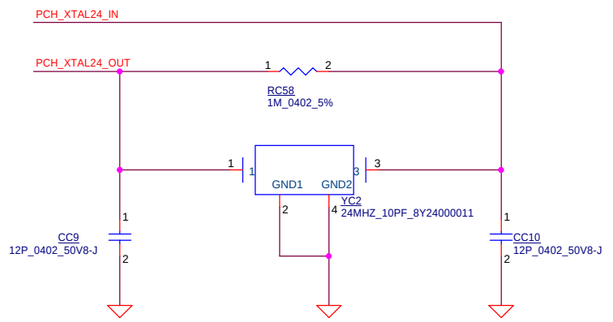
[SKL PDG]External pull-up resistor required if used for CLKREQ# functionality.

[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.



20160127
Change CC7/CC8 to 6.8p by vender suggestion

[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)



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Title	KBL(6/16):CLOCK SIGNALS		
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Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

+3VALW_PCH
SMBALERT# — RC59 1 — 2 — 1K_0402_5%

GPP_C2, Internal PD 20K

JTAG ODT

SPI0_MOSI

+3VALW_PCH
SPI_SI — RC62 1 @ 2 — 8.2K_0402_5%

+3VALW_PCH
SPI_SO — RC65 1 @ 2 — 8.2K_0402_5%

GPP_C5, Internal PD 20K

*L: LPC
H: eSPI

+3VALW_PCH
SML0ALERT# — RC67 1 @ 2 — 1K_0402_5%

close to CPU

UC1E — SKL_ULT

SPI - FLASH
[21,58] SPI_CLK — SPI_CLK — AV2 — SPI0_CLK
[21,58] SPI_SO — SPI_SO — AW3 — SPI0_MISO
[21,58] SPI_SI — SPI_SI — AV3 — SPI0_MOSI
[21] SPI_IO2 — SPI_IO2 — AW2 — SPI0_IO2
[21] SPI_IO3 — SPI_IO3 — AU4 — SPI0_IO3
[21] SPI_CS0#_8MB — SPI_CS0#_8MB — AU3 — SPI0_CS0#
[21] SPI_CS1#_4MB — SPI_CS1#_4MB — AU2 — SPI0_CS1#
[58] SPI_CS2#_TPM — SPI_CS2#_TPM — AU1 — SPI0_CS2#

SPI - TOUCH
M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C LINK
[48] CL_CLK_WLAN — G3 CL_CLK
[48] CL_DATA_WLAN — G2 CL_DATA
[48] CL_RST_WLAN# — G1 CL_RST#

LPC

SMBUS, SMLINK
R7 GPP_C0/SMBCLK — PCH_SMB_CLK
R8 GPP_C1/SMBDATA — PCH_SMB_DATA
R10 GPP_C2/SMBALERT# — SMBALERT#
R9 GPP_C3/SML0CLK
W2 GPP_C4/SML0DATA
W1 GPP_C5/SML0ALERT# — SML0ALERT#
W3 GPP_C6/SML1CLK — PCH_SML1CLK
V3 GPP_C7/SML1DATA — PCH_SML1DATA
AM7 GPP_B23/SML1ALERT#/PCHHOT# — SML1ALERT#

[25] All_GPU_PWRGD — RC107 1 — 2 0_0402_5% — All_GPU_PWRGD_R — GPU_EVENT#
[28] GPU_EVENT#
[57] EC_SCI# — EC_SCI#

[57] KBRST# — KBRST# — AW13 — GPP_A0/RCIN#
10P_0402_50V8-J — CC183 EMC_NS@ — [57,58] SERIRQ — SERIRQ — AY11 — GPP_A6/SERIRQ

GPP_A1/LAD0/ESPI_IO0 — AY13 — LPC_AD0 [57]
GPP_A2/LAD1/ESPI_IO1 — BA13 — LPC_AD1 [57]
GPP_A3/LAD2/ESPI_IO2 — BB13 — LPC_AD2 [57]
GPP_A4/LAD3/ESPI_IO3 — AY12 — LPC_AD3 [57]
GPP_A5/LFRAME#/ESPI_CS# — BA12 — LPC_FRAME# [57]
GPP_A14/SUS_STAT#/ESPI_RESET# — BA11 — SUS_STAT#
RC63 0_0402_5% — TC7

GPP_A9/CLKOUT_LPC0/ESPI_CLK — AW9 — PCH_PCI_CLK_R
GPP_A10/CLKOUT_LPC1 — AY9
GPP_A8/CLKRUN# — AW11 — CLKRUN#
RC64 22_0402_5% — CLK_PCI_EC [57]
RC66 8.2K_0402_5% — +3VS
CC184 EMC_NS@ — 10P_0402_50V8-J
Close to UC1

SKYLAKE-U_BGA1356
REV = 1
@
5 OF 20 ? ?

DIMM1, DIMM2, Security EEPROM, Click Pad

EC,dGPU,Thermal Sensor

Place RC179,180,181 close together

+3VS — +3VALW_PCH
RC179 1 — 2 10K_0402_5% SERIRQ
RC180 1 — 2 10K_0402_5% EC_SCI#
RC181 1 — 2 10K_0402_5% KBRST#
RC72 1 — 2 4.7K_0402_5% CP_SMB_CLK
RC76 1 — 2 4.7K_0402_5% CP_SMB_DAT
RC212 1 — 2 10K_0402_5% GPU_EVENT#

PCH_SMB_CLK — RC71 1 — 2 2.2K_0402_1%
PCH_SMB_DATA — RC73 1 — 2 2.2K_0402_1%
PCH_SMLICLK — RC74 1 — 2 2.2K_0402_1%
PCH_SML1DATA — RC75 1 — 2 2.2K_0402_1%

Add RC212 PU by NV suggestion

SML1ALERT# — RC77 1 @ 2 1K_0402_5%

SB00000YS00
2N7002KDWH_SOT363-6
QC1A
PCH_SMB_CLK — CP_SMB_CLK [22,23,63]
+3VS
Plan to remove QC1 after SDV
PCH_SMB_DATA — CP_SMB_DAT [22,23,63]
QC1B
2N7002KDWH_SOT363-6
SB00000YS00

SB00000YS00
2N7002KDWH_SOT363-6
QC2A
+3VS — PCH_SML1CLK — EC_SMB_CK3 [28,57,59,62]
PCH_SML1DATA — EC_SMB_DA3 [28,57,59,62]
QC2B
2N7002KDWH_SOT363-6
SB00000YS00

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Title: KBL(7/16):LPC/SPI/SMBUS/CL
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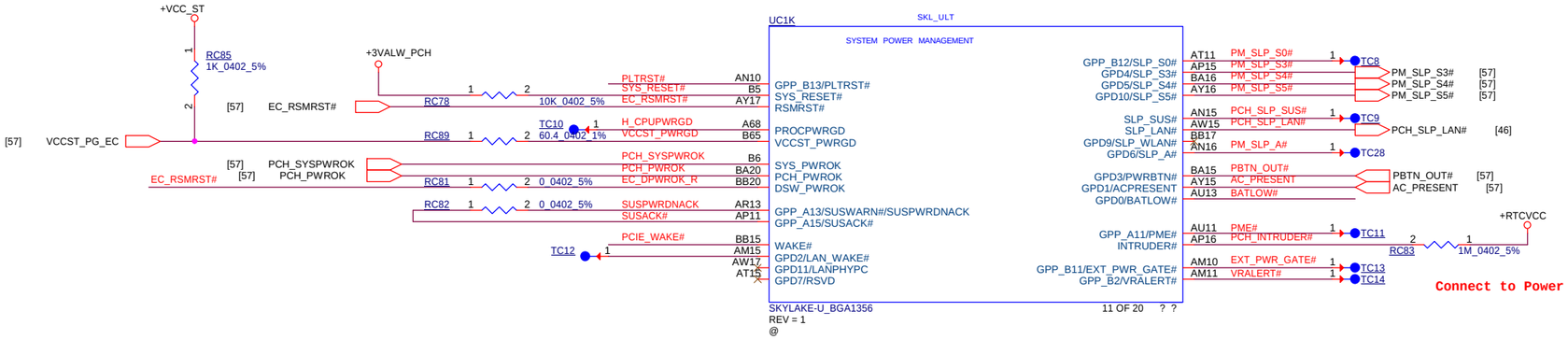
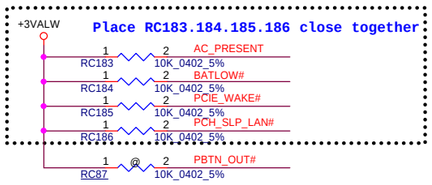
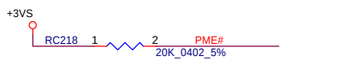
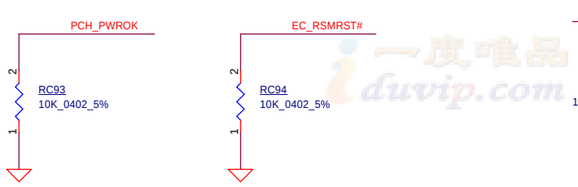
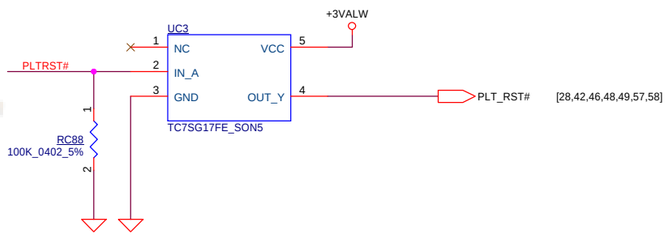






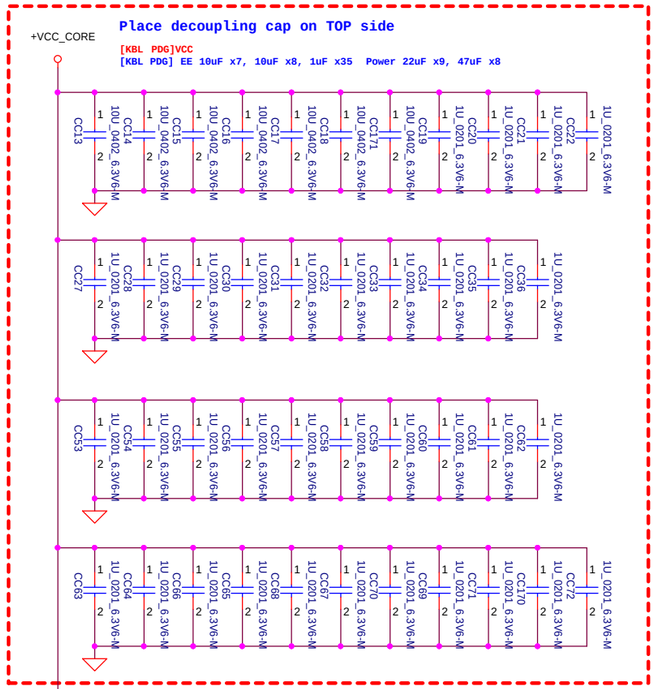
20160408
1.Add RC218 for PME# by BIOS request

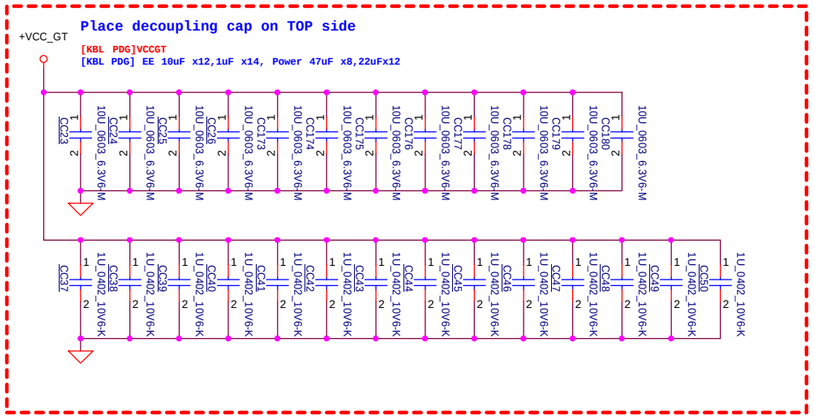


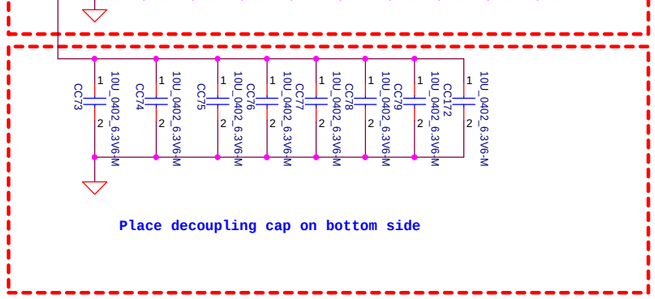


Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title	KBL(8/16):SYSTEM PM		
Size Custom	Document Number KENOBI		Rev 2.0
Date: Thursday, August 25, 2016	Sheet 12 of 82		







Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(9/16):Decoupling**

Size	Document Number	Rev
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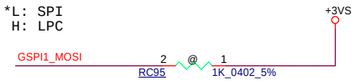
GPP_B22, Internal PD 20K

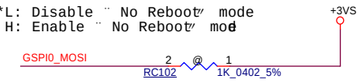
*L: SPI
H: LPC



To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 K ±5 % resistor

GPP_B18, Internal PD 20K

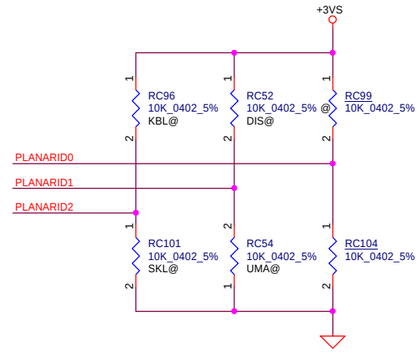
*L: Disable "No Reboot" mode
H: Enable "No Reboot" mode

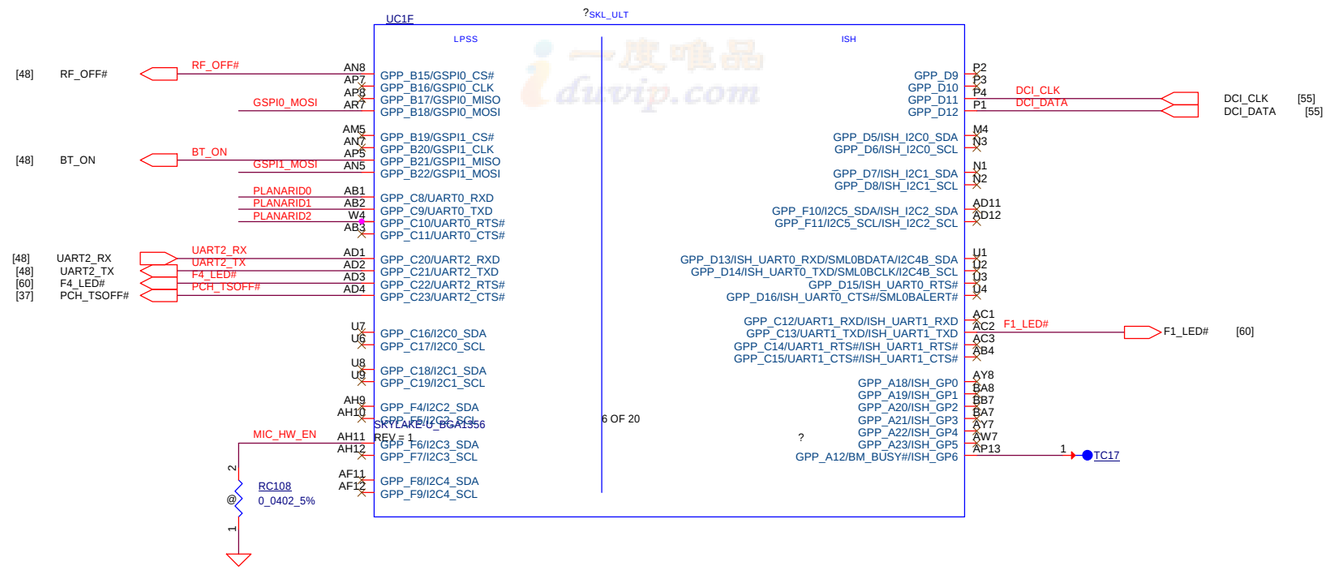


To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 K ±5 % resistor

Project ID

	PLANARID0 (GPP_C8)	PLANARID1 (GPP_C9)	PLANARID2 (GPP_C10)	
L	14"	UMA	Skylake	
H	15"	DIS	Kabylake	





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(10/16):GPIO/CPU/MISC

Size	Document Number	Rev
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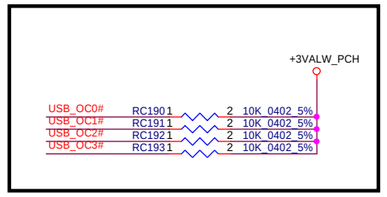
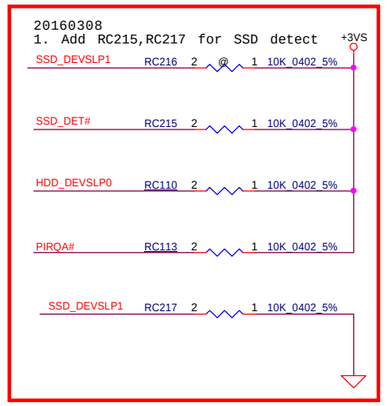
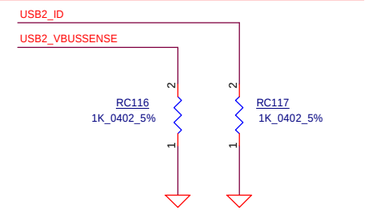
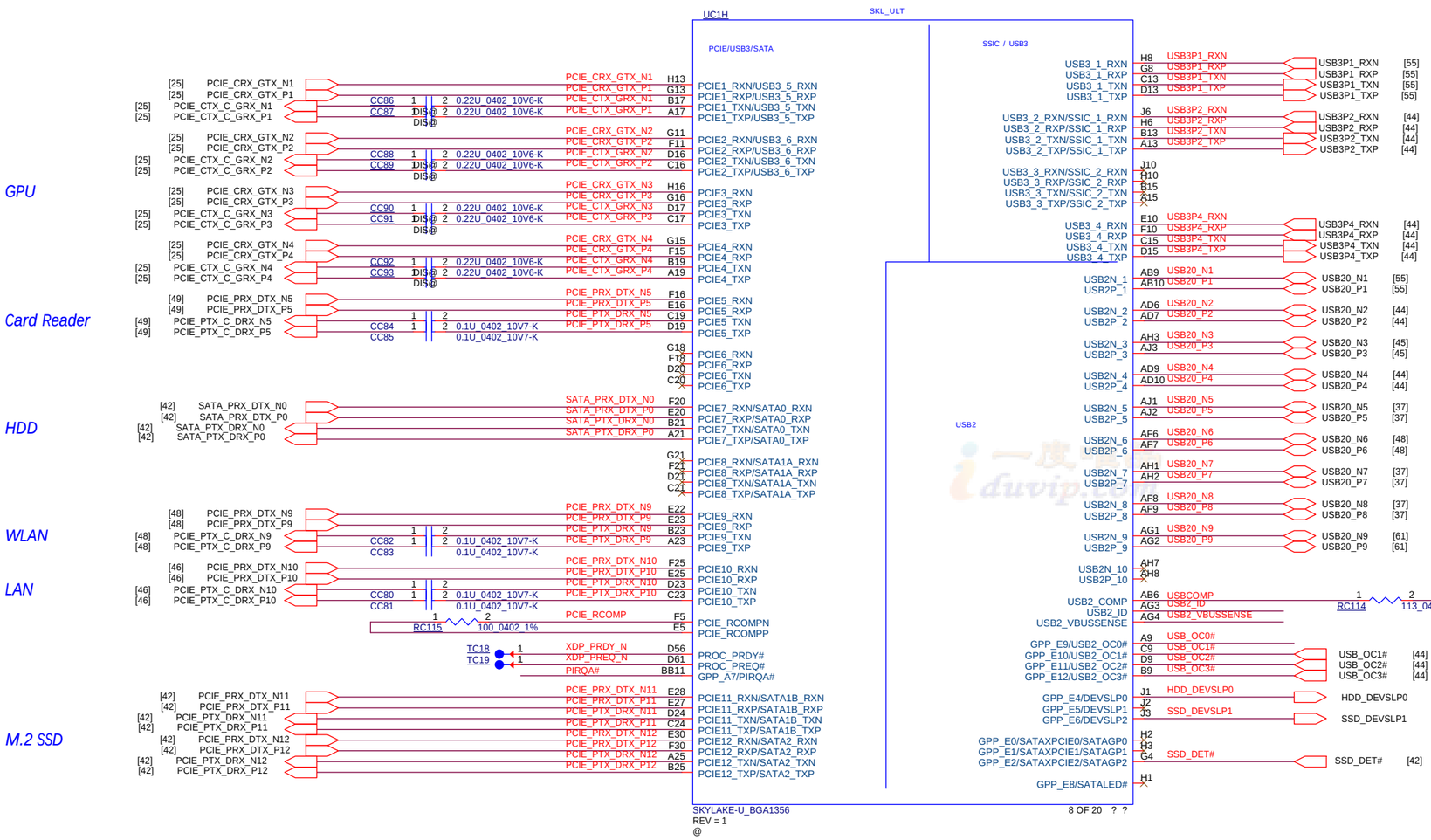
	USB Port Number
USB_OC0#	Reserve
USB_OC1#	Port2
USB_OC2#	Port3
USB_OC3#	Port4









TYPE C
On Board (Lef t)
On Board (Right-Front)
TYPE C
On Board (AOU)
On Board (Right-Back)
On Board (Right-Front)
Touch Panel
BT
CAMERA
IR CAMERA
FPR

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Title: KBL(11/16):PCIE/USB/SATA

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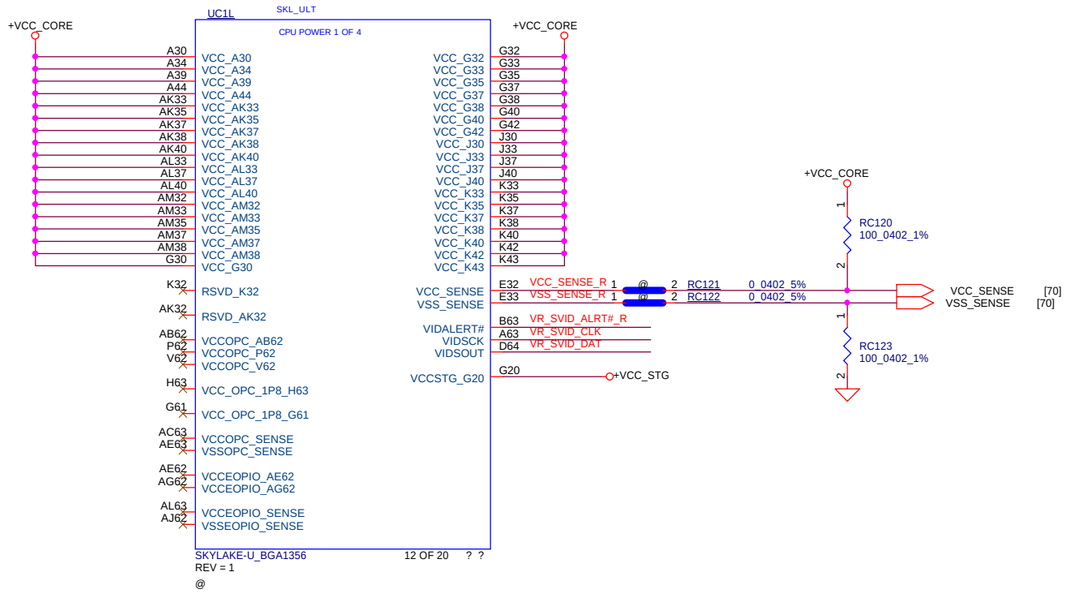
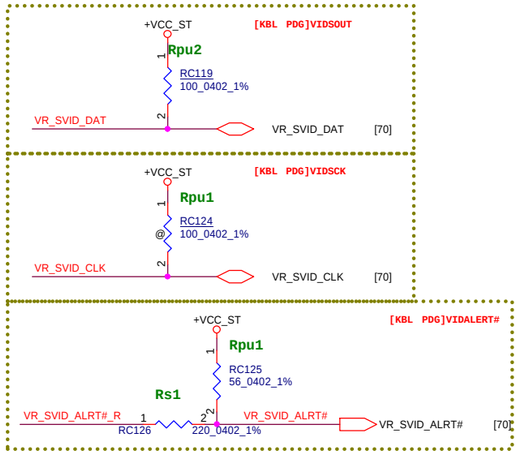
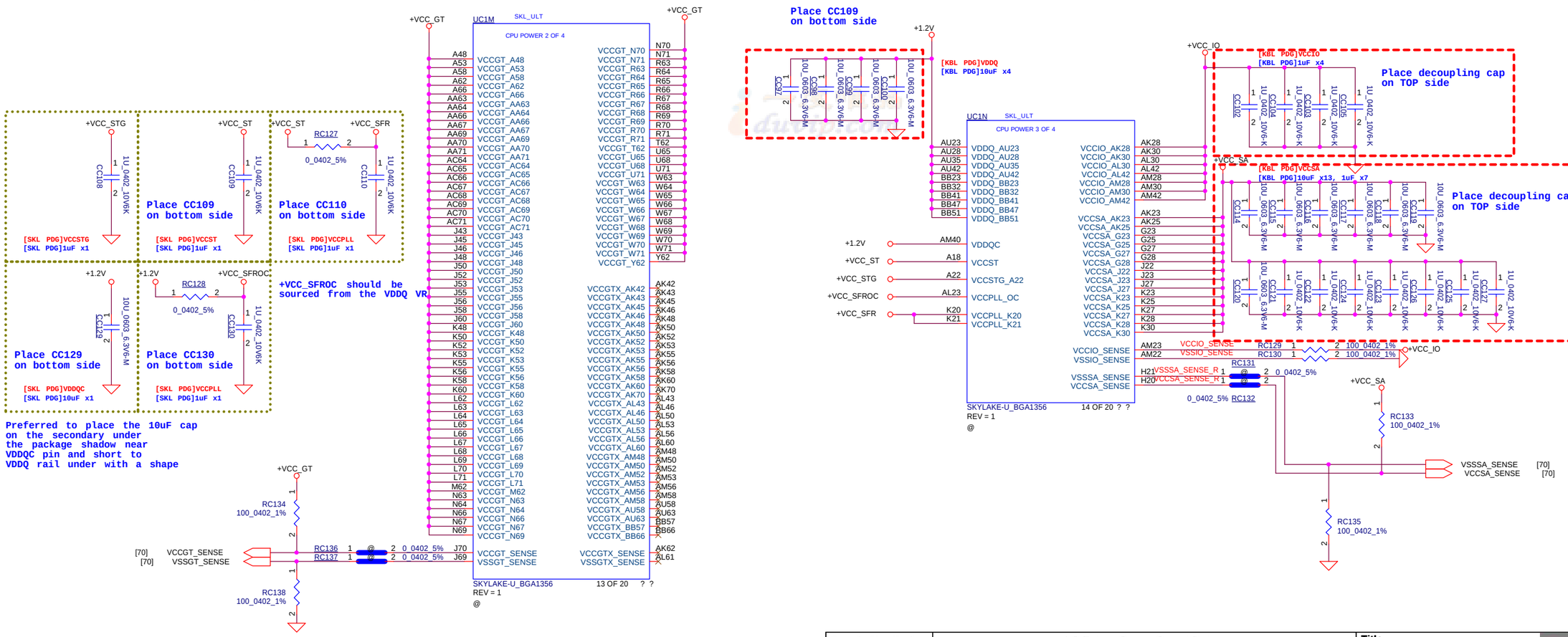
Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	







Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(12/16):POWER**

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Reserve for Sense Resistor

+1.8VALW — RC139 0_0603_5% — +1.8VALW_PCH
+3VALW — RC140 0_0805_5% — +3VALW_PCH
+1VALW — RC141 0_0805_5% — +1VALW_PCH
+1VALW — RC202 0_0805_5% — +VCC_MPHYGT

+VCC_MPHYGT — RC1451 0_0402_5% — +VCC_AMPHYPLL
+1VALW_PCH — RC1461 0_0402_5% — +1VALW_PLL

CC132 please close to N18

+VCC_MPHYGT — CC132 1U_0402_10V6K

[SKL PDG]VccAPLLEBB
[SKL PDG]1uF x1
[SKL PDG]Close N18,
Placement type:Edge<3mm(118mil)

VccMPHYGT(Mod PHY Externally Gated Primary 1.0 V: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.)

CC133 & CC134 please close to N15

+VCC_MPHYGT — CC133 1U_0402_10V6K; CC134 47U_0805_6.3V6-M

[SKL PDG]VccMPHYGT
[SKL PDG]1uF x1
[SKL PDG]Close N15,
Placement type:Edge<3mm(118mil)
[SKL PDG]47uF x1
[SKL PDG]Close N15,
Placement type:Edge<10mm(394mil)

SRAM Primary Well 1.0 V. Dedicated SRAM rail and can have on board power down gate control.

CC136 please close to AF20

+VCC_MPHYGT — @CC136 1U_0402_10V6K

[SKL PDG]VccSRAM
[SKL PDG]1uF x1
[SKL PDG]Close AF20,
Placement type:Edge<10mm(394mil)

Mod PHY Always On Primary 1.0 V: Always on primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic

CC137 please close to K17

+1VALW_PCH — CC137 1U_0402_10V6K

[SKL PDG]VccMPHYAON
[SKL PDG]1uF x1
[SKL PDG]Close K17,
Placement type:Edge<3mm(118mil)

please close to AG15 Y16 & T16

+3VALW_PCH — CC140 1U_0402_10V6K; CC141 1U_0402_10V6K; CC142 1U_0402_10V6K

Primary Well 1.0 V: For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.

CC143 please close to AB19

+1VALW_PCH — CC143 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]1uF x1
[SKL PDG]Close AB19,
Placement type:Edge<10mm(394mil)

+1VALW_PCH
CC181 22U_0603_6.3V6-M; CC131 22U_0603_6.3V6-M
CC182 22U_0603_6.3V6-M; CC135 22U_0603_6.3V6-M

UC1O — SKL_ULT — CPU POWER 4 OF 4

AB19, AB20, P18	VCCPRIM_1P0_AB19, VCCPRIM_1P0_AB20, VCCPRIM_1P0_P18	1100mA
AF18, AF19, V20, V21	VCCPRIM_CORE_AF18, VCCPRIM_CORE_AF19, VCCPRIM_CORE_V20, VCCPRIM_CORE_V21	500mA
+DCPDSW — AL1	DCPDSW_1P0	22mA
K17, L1	VCCMPHYAON_1P0_K17, VCCMPHYAON_1P0_L1	
N15, N16, N17, P15, P16	VCCMPHYGT_1P0_N15, VCCMPHYGT_1P0_N16, VCCMPHYGT_1P0_N17, VCCMPHYGT_1P0_P15, VCCMPHYGT_1P0_P16	1500mA
K15, L15	VCCAMPHYPLL_1P0_K15, VCCAMPHYPLL_1P0_L15	88mA
V15	VCCAPLL_1P0	26mA
AB17, Y18	VCCPRIM_1P0_AB17, VCCPRIM_1P0_Y18	
AD17, AD18, AJ17	VCCDSW_3P3_AD17, VCCDSW_3P3_AD18, VCCDSW_3P3_AJ17	118mA
AJ19	VCCHDA	68mA
AJ16	VCCSPI	
AF20, AF21, T19, T20	VCCSRAM_1P0_AF20, VCCSRAM_1P0_AF21, VCCSRAM_1P0_T19, VCCSRAM_1P0_T20	565mA
AJ21	VCCPRIM_3P3_AJ21	75mA
AK20	VCCPRIM_1P0_AK20	33mA
N18	VCCAPLLEBB	33mA

+PCH_CORE, +DCPDSW, +VCC_MPHYGT, +VCC_AMPHYPLL, +1VALW_PLL, +VCC_DSW3P3, +VCC_HDA, +3V_SPI0, +3VALW_PRIM

SKYLAKE-U_BGA1356 — REV = 1 — 15 OF 20

AK15, AG15, Y16, Y15, T16, AF16, AD15	VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPF, VCCPGPPG	85mA (+3VALW_PCH)
V19	VCCPRIM_3P3_V19	161mA (+1.8VALW_PCH)
T1	VCCPRIM_1P0_T1	135mA (+1VALW_PCH)
AA1	VCCATS_1P8	+1.8VALW_PCH
AK17	VCCRTCPRIM_3P3	+3VALW_RTCPRIM
AK19, BB14	VCCRTC_AK19, VCCRTC_BB14	+RTCVCC
BB10	DCPRTC (+DCPRTC)	
A14	VCCCLK1	
K19	VCCCLK2	
L21	VCCCLK3	
N20	VCCCLK4	
L19	VCCCLK5	
A10	VCCCLK6	
AN11, AN13	GPP_B0/CORE_VID0, GPP_B1/CORE_VID1	T1, T2

Primary Well 3.3 V

+3VALW_PCH — RC147 0_0402_5% — +3VALW_PRIM; CC145 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]1uF x1
[SKL PDG]Close V19,
Placement type:Edge<3mm(118mil)

HD Audio Power 3.3 V, 1.8 V, 1.5 V. For Intel High Definition Audio.

+3VALW_PCH — RC148 0_0402_5% — +VCC_HDA; CC147 1U_0402_10V6K

[SKL PDG]VccHDA
[SKL PDG]1uF x1
[SKL PDG]Close AJ19,
Placement type:Edge<10mm(394mil)

Thermal Sensor Primary Well 1.8 V

+1.8VALW_PCH — CC144 1U_0402_10V6K

[SKL PDG]VccATS
[SKL PDG]1uF x1
[SKL PDG]Close AA1,
Placement type:Edge<10mm(394mil)

Deep Sx Well 1.0 V: This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.

+DCPDSW — CC148 1U_0402_10V6K

[SKL PDG]DcpDSW
[SKL PDG]1uF x1
[SKL PDG]Close AL1,
Placement type:Edge<3mm(118mil)

RTC de-coupling capacitor only. This rail should NOT be driven.

+DCPRTC — CC146 0.1U_0402_10V6-K

[SKL PDG]DcpRTC
[SKL PDG]0.1uF x1
[SKL PDG]Close BB10,
Placement type:Edge<3mm(118mil)

+VCC_AMPHYPLL — @CC149 1U_0402_10V6K

Core Logic Primary Well: This rail scales from 0.85 V to 1.0 V.

+1VALW — RC151 0_0805_5% — +PCH_CORE; CC150 1U_0402_10V6K

[SKL PDG]VccPRIM_Core
[SKL PDG]1uF x1
[SKL PDG]Close AF18,
Placement type:Edge<10mm(394mil)

Deep Sx Well for GPD GPIOs and USB2

+3VALW_PCH — RC152 0_0402_5% — +VCC_DSW3P3

[SKL PDG]VccDSW

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+3VALW_PCH — RC150 0_0402_5% — +3VALW_RTCPRIM; CC151 1U_0402_10V6K; CC152 0.1U_0402_10V6K; CC153 0.1U_0402_10V6K

[SKL PDG]VccRTCPRIM
[SKL PDG]1uF x1,0.1uF x2
[SKL PDG]Close AK17,
Placement type:Edge<3mm(118mil)

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+RTCVCC — CC154 1U_0402_10V6K

[SKL PDG]VccRTC
[SKL PDG]1uF x1
[SKL PDG]Close AK19,
Placement type:Edge<3mm(118mil)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(13/16):POWER**

Size	Document Number	Rev
A2	KENOBI	2.0

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UC1P
SKL_ULT
GND 1 OF 3

A5	VSS_A5	VSS_AL65	AL65
A67	VSS_A67	VSS_AL66	AM13
A70	VSS_A70	VSS_AM13	AM21
AA2	VSS_AA2	VSS_AM21	AM25
AA4	VSS_AA4	VSS_AM25	AM27
AA65	VSS_AA65	VSS_AM27	AM43
AA68	VSS_AA68	VSS_AM43	AM45
AB15	VSS_AB15	VSS_AM45	AM46
AB16	VSS_AB16	VSS_AM46	AM55
AB18	VSS_AB18	VSS_AM55	AM60
AB21	VSS_AB21	VSS_AM60	AM61
AB8	VSS_AB8	VSS_AM61	AM68
AD13	VSS_AD13	VSS_AM68	AM71
AD16	VSS_AD16	VSS_AM71	AM8
AD19	VSS_AD19	VSS_AM8	AN20
AD20	VSS_AD20	VSS_AN20	AN23
AD21	VSS_AD21	VSS_AN23	AN28
AD62	VSS_AD62	VSS_AN28	AN30
AD8	VSS_AD8	VSS_AN30	AN32
AE64	VSS_AE64	VSS_AN32	AN33
AE65	VSS_AE65	VSS_AN33	AN35
AE66	VSS_AE66	VSS_AN35	AN37
AE67	VSS_AE67	VSS_AN37	AN38
AE68	VSS_AE68	VSS_AN38	AN40
AE69	VSS_AE69	VSS_AN40	AN42
AF1	VSS_AF1	VSS_AN42	AN58
AF10	VSS_AF10	VSS_AN58	AN63
AF15	VSS_AF15	VSS_AN63	AP10
AF17	VSS_AF17	VSS_AP10	AP18
AF2	VSS_AF2	VSS_AP18	AP20
AF4	VSS_AF4	VSS_AP20	AP23
AF63	VSS_AF63	VSS_AP23	AP28
AG16	VSS_AG16	VSS_AP28	AP32
AG17	VSS_AG17	VSS_AP32	AP35
AG18	VSS_AG18	VSS_AP35	AP38
AG19	VSS_AG19	VSS_AP38	AP42
AG20	VSS_AG20	VSS_AP42	AP58
AG21	VSS_AG21	VSS_AP58	AP63
AG71	VSS_AG71	VSS_AP63	AP68
AH13	VSS_AH13	VSS_AP68	AP70
AH6	VSS_AH6	VSS_AP70	AR11
AH63	VSS_AH63	VSS_AR11	AR15
AH64	VSS_AH64	VSS_AR15	AR16
AH67	VSS_AH67	VSS_AR16	AR20
AJ15	VSS_AJ15	VSS_AR20	AR23
AJ18	VSS_AJ18	VSS_AR23	AR28
AJ20	VSS_AJ20	VSS_AR28	AR35
AJ4	VSS_AJ4	VSS_AR35	AR42
AK11	VSS_AK11	VSS_AR42	AR43
AK16	VSS_AK16	VSS_AR43	AR45
AK18	VSS_AK18	VSS_AR45	AR46
AK21	VSS_AK21	VSS_AR46	AR48
AK22	VSS_AK22	VSS_AR48	AR5
AK27	VSS_AK27	VSS_AR5	AR50
AK63	VSS_AK63	VSS_AR50	AR52
AK68	VSS_AK68	VSS_AR52	AR53
AK69	VSS_AK69	VSS_AR53	AR55
AK8	VSS_AK8	VSS_AR55	AR58
AL2	VSS_AL2	VSS_AR58	AR63
AL28	VSS_AL28	VSS_AR63	AR8
AL32	VSS_AL32	VSS_AR8	AT2
AL35	VSS_AL35	VSS_AT2	AT20
AL38	VSS_AL38	VSS_AT20	AT23
AL4	VSS_AL4	VSS_AT23	AT28
AL45	VSS_AL45	VSS_AT28	AT35
AL48	VSS_AL48	VSS_AT35	AT4
AL52	VSS_AL52	VSS_AT4	AT42
AL55	VSS_AL55	VSS_AT42	AT56
AL58	VSS_AL58	VSS_AT56	AT58
AL64	VSS_AL64	VSS_AT58	

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REV = 1 ? ?

UC1O
SKL_ULT
GND 2 OF 3

AT63	VSS_AT63	VSS_BA49	BA49
AT68	VSS_AT68	VSS_BA53	BA53
AT71	VSS_AT71	VSS_BA57	BA57
AU10	VSS_AU10	VSS_BA6	BA6
AU15	VSS_AU15	VSS_BA62	BA62
AU20	VSS_AU20	VSS_BA66	BA66
AU32	VSS_AU32	VSS_BA71	BA71
AU38	VSS_AU38	VSS_BB18	BB18
AV1	VSS_AV1	VSS_BB26	BB26
AV68	VSS_AV68	VSS_BB30	BB30
AV69	VSS_AV69	VSS_BB34	BB34
AV70	VSS_AV70	VSS_BB38	BB38
AV71	VSS_AV71	VSS_BB43	BB43
AW10	VSS_AW10	VSS_BB55	BB55
AW12	VSS_AW12	VSS_BB6	BB6
AW14	VSS_AW14	VSS_BB60	BB60
AW16	VSS_AW16	VSS_BB64	BB64
AW18	VSS_AW18	VSS_BB67	BB67
AW21	VSS_AW21	VSS_BB70	BB70
AW23	VSS_AW23	VSS_C1	C1
AW26	VSS_AW26	VSS_C25	C25
AW28	VSS_AW28	VSS_C5	C5
AW30	VSS_AW30	VSS_D10	D10
AW32	VSS_AW32	VSS_D11	D11
AW34	VSS_AW34	VSS_D14	D14
AW36	VSS_AW36	VSS_D18	D18
AW38	VSS_AW38	VSS_D22	D22
AW41	VSS_AW41	VSS_D25	D25
AW43	VSS_AW43	VSS_D26	D26
AW45	VSS_AW45	VSS_D30	D30
AW47	VSS_AW47	VSS_D34	D34
AW49	VSS_AW49	VSS_D39	D39
AW51	VSS_AW51	VSS_D44	D44
AW53	VSS_AW53	VSS_D45	D45
AW55	VSS_AW55	VSS_D47	D47
AW57	VSS_AW57	VSS_D48	D48
AW6	VSS_AW6	VSS_D53	D53
AW60	VSS_AW60	VSS_D58	D58
AW62	VSS_AW62	VSS_D6	D6
AW64	VSS_AW64	VSS_D62	D62
AW66	VSS_AW66	VSS_D66	D66
AW8	VSS_AW8	VSS_D69	D69
AY66	VSS_AY66	VSS_E11	E11
B10	VSS_B10	VSS_E15	E15
B14	VSS_B14	VSS_E18	E18
B18	VSS_B18	VSS_E21	E21
B22	VSS_B22	VSS_E46	E46
B30	VSS_B30	VSS_E50	E50
B34	VSS_B34	VSS_E53	E53
B39	VSS_B39	VSS_E56	E56
B44	VSS_B44	VSS_E6	E6
B48	VSS_B48	VSS_E65	E65
B53	VSS_B53	VSS_E71	E71
B58	VSS_B58	VSS_F1	F1
B62	VSS_B62	VSS_F13	F13
B66	VSS_B66	VSS_F2	F2
B71	VSS_B71	VSS_F22	F22
BA1	VSS_BA1	VSS_F23	F23
BA10	VSS_BA10	VSS_F27	F27
BA14	VSS_BA14	VSS_F28	F28
BA18	VSS_BA18	VSS_F32	F32
BA2	VSS_BA2	VSS_F33	F33
BA23	VSS_BA23	VSS_F35	F35
BA28	VSS_BA28	VSS_F37	F37
BA32	VSS_BA32	VSS_F38	F38
BA36	VSS_BA36	VSS_F4	F4
F68	VSS_F68	VSS_F40	F40
BA45	VSS_BA45	VSS_F42	F42
		VSS_BA41	BA41

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REV = 1 ? ?

UC1R
SKL_ULT
GND 3 OF 3

F8	VSS_F8	VSS_L18	L18
G10	VSS_G10	VSS_L2	L2
G22	VSS_G22	VSS_L20	L20
G43	VSS_G43	VSS_L4	L4
G45	VSS_G45	VSS_L8	L8
G48	VSS_G48	VSS_N10	N10
G5	VSS_G5	VSS_N13	N13
G52	VSS_G52	VSS_N19	N19
G55	VSS_G55	VSS_N21	N21
G58	VSS_G58	VSS_N6	N6
G6	VSS_G6	VSS_N65	N65
G60	VSS_G60	VSS_N68	N68
G63	VSS_G63	VSS_P17	P17
G66	VSS_G66	VSS_P19	P19
H15	VSS_H15	VSS_P20	P20
H18	VSS_H18	VSS_P21	P21
H71	VSS_H71	VSS_R13	R13
J11	VSS_J11	VSS_R6	R6
J13	VSS_J13	VSS_T15	T15
J25	VSS_J25	VSS_T17	T17
J28	VSS_J28	VSS_T18	T18
J32	VSS_J32	VSS_T2	T2
J35	VSS_J35	VSS_T21	T21
J38	VSS_J38	VSS_T4	T4
J42	VSS_J42	VSS_U10	U10
J8	VSS_J8	VSS_U63	U63
K16	VSS_K16	VSS_U64	U64
K18	VSS_K18	VSS_U66	U66
K22	VSS_K22	VSS_U67	U67
K61	VSS_K61	VSS_U69	U69
K63	VSS_K63	VSS_U70	U70
K64	VSS_K64	VSS_V16	V16
K65	VSS_K65	VSS_V17	V17
K66	VSS_K66	VSS_V18	V18
K67	VSS_K67	VSS_W13	W13
K68	VSS_K68	VSS_W6	W6
K70	VSS_K70	VSS_W9	W9
K71	VSS_K71	VSS_Y17	Y17
L11	VSS_L11	VSS_Y19	Y19
L16	VSS_L16	VSS_Y20	Y20
L17	VSS_L17	VSS_Y21	Y21

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REV = 1 ? ?

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(14/16):GND

Size	Document Number	Rev
Custom	KENOBI	2.0

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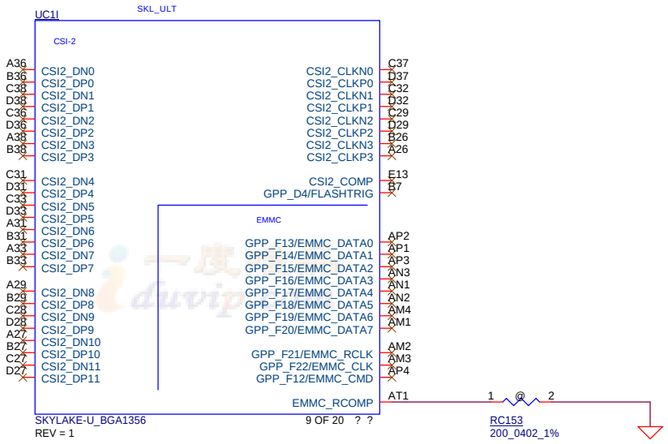

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(15/16):CSI-2/EMMC**

Size	Document Number	Rev
Custom	KENOBI	2.0

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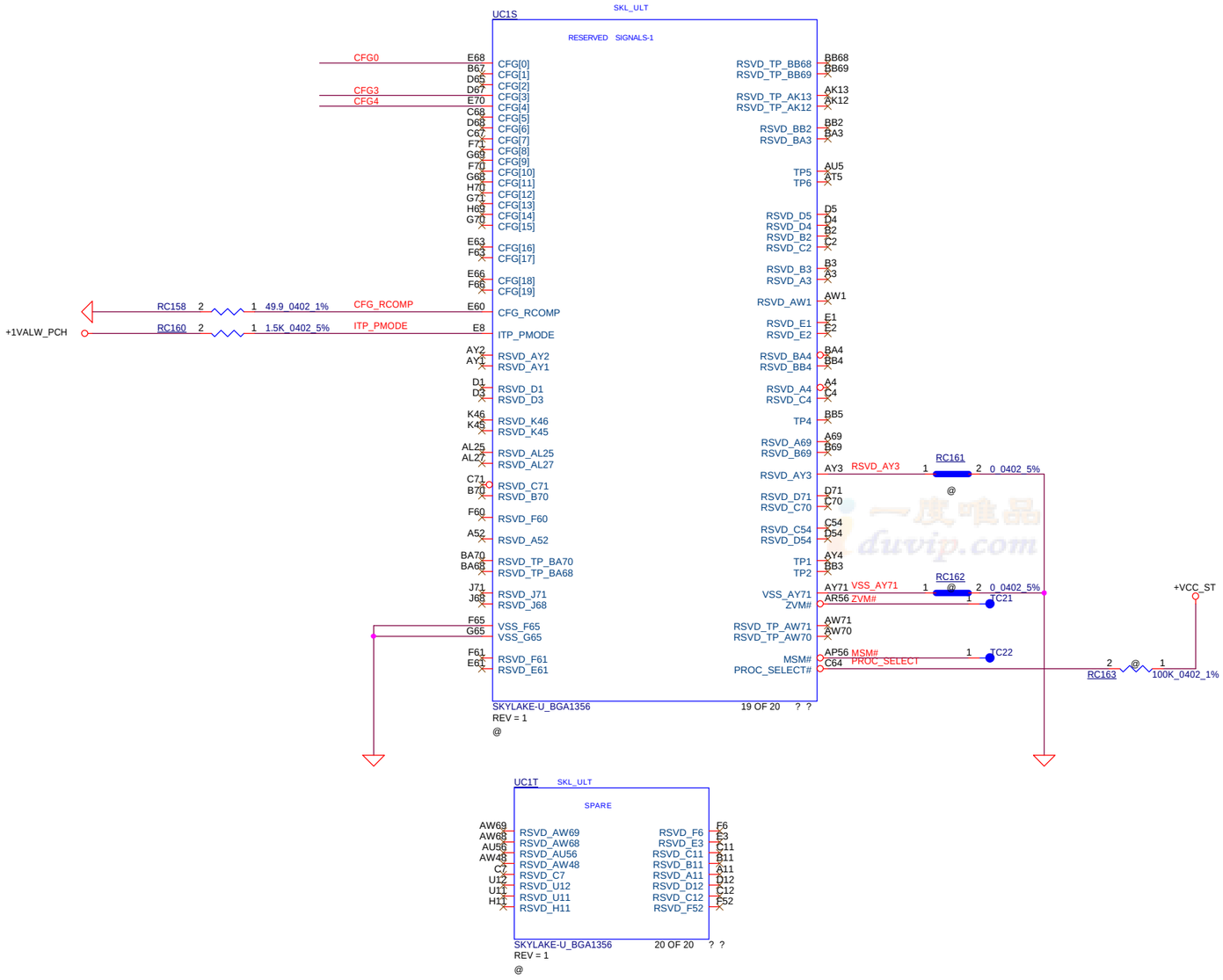

[SKL EDS]

CFG0

+VCC_IO

CFG0 — RC154 2 @ 1 1K_0402_5%

RC155 2 @ 1 1K_0402_1%

L:Stall.
*H:(Default) Normal Operation; No stall.

CFG4

+VCC_IO

CFG4 — RC156 2 @ 1 1K_0402_5%

RC157 2 1 1K_0402_1%

*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

CFG3

CFG3 — RC159 1 @ 2 1K_0402_5%

CFG3 require >= 0.5"
CPU Debug Consent Strap

TABLE

CFG0 : Stall Reset Sequence
after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(16/16):CFG/RESERVED

Size: Custom | Document Number: KENOBI | Rev: 2.0

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+3VALW — RC164 1 — 2 0_0603_5% — +3V_SPI

0.085 A

4MB(32Mb) Reserve

[11] SPI_CS0#_8MB

UC8M1 (W25Q64FVSSIQ_SO8)

1	SPI_CS0#_8MB	CS#	
2	SPI_SO_8MB	DO	
3	SPI_IO2_8MB	WP#	
4		GND	
8	+3V_SPI	VCC	
7	SPI_IO3_8MB	HOLD#	
6	SPI_CLK_8MB	CLK	
5	SPI_SI_8MB	DI	

+3V_SPI — CC156 0.1U_0402_10V7-K

Place RC194,195,196,197 close together

SPI_IO3_8MB	RC194	1	2	33_0402_5%	SPI_IO3	SPI_IO3 [11]
SPI_CLK_8MB	RC195	1	2	33_0402_5%	SPI_CLK	SPI_CLK [11,58]
SPI_SI_8MB	RC196	1	2	33_0402_5%	SPI_SI	SPI_SI [11,58]
SPI_IO2_8MB	RC197	1	2	33_0402_5%	SPI_IO2	SPI_IO2 [11]

Near SPI ROM

SPI_SO_8MB — RC165 1 — 2 33_0402_5% — SPI_SO — SPI_SO [11,58]

Mirror Code

[57]	FSCE#	RC167	1	2 0_0402_5%	SPI_CS0#_8MB
[57]	SPI_FMOSI#	RC169	1	2 0_0402_5%	SPI_SI_8MB
[57]	SPI_FMISO	RC171	1	2 0_0402_5%	SPI_SO_8MB
[57]	SPI_FSCK	RC172	1	2 0_0402_5%	SPI_CLK_8MB

Close to SPI ROM (UC8M1).

8MB(64Mb)

[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM

[11] SPI_CS1#_4MB

UC4M1 (W25Q32FVSSIQ_SO8 4M@)

1	SPI_CS1#_4MB	CS#	
2	SPI_SO_4MB	DO	
3	SPI_IO2_4MB	WP#	
4		GND	
8	+3V_SPI	VCC	
7	SPI_IO3_4MB	HOLD#	
6	SPI_CLK_4MB	CLK	
5	SPI_SI_4MB	DI	

+3V_SPI — CC157 0.1U_0402_10V7-K 4M@

Place RC203,204,205,206 close together

SPI_IO3_4MB	RC203	1	4M@	2	33_0402_5%	SPI_IO3
SPI_CLK_4MB	RC204	1	4M@	2	33_0402_5%	SPI_CLK
SPI_SI_4MB	RC205	1	4M@	2	33_0402_5%	SPI_SI
SPI_IO2_4MB	RC206	1	4M@	2	33_0402_5%	SPI_IO2

Near SPI ROM

SPI_SO_4MB — 1 4M@ RC166 2 — 33_0402_5% — SPI_SO

+3V_SPI

SPI_IO2 — RC168 2 — 1 1K_0402_5%

SPI_IO3 — 2 RC170 1 — 1K_0402_5%

SPI_IO3 — RC173 1 @ — 2 1K_0402_5%

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **SPI ROM**

Size	Document Number	Rev
Custom	KENOBI	2.0

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder
[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V
CD1 10U_0603_6.3V6-M
CD2 10U_0603_6.3V6-M
CD3 10U_0603_6.3V6-M
CD4 10U_0603_6.3V6-M
CD5 10U_0603_6.3V6-M
CD6 10U_0603_6.3V6-M
CD7 10U_0603_6.3V6-M
CD8 10U_0603_6.3V6-M
CD14 1U_0402_6.3V6-K
CD15 1U_0402_6.3V6-K
CD16 1U_0402_6.3V6-K
CD17 1U_0402_6.3V6-K
CD18 1U_0402_6.3V6-K
CD19 1U_0402_6.3V6-K
CD20 1U_0402_6.3V6-K
CD21 1U_0402_6.3V6-K
CD26 @ 330U_D2_2VM_R9M

Place decoupling cap on DRAM side.
[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+2.5V
CD9 10U_0603_6.3V6-M
CD10 10U_0603_6.3V6-M
CD11 1U_0402_6.3V6-K
CD12 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM
[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+0.6VS
CD22 10U_0603_6.3V6-M
CD23 10U_0603_6.3V6-M
CD24 1U_0402_6.3V6-K
CD63 1U_0402_6.3V6-K
CD64 1U_0402_6.3V6-K
CD65 1U_0402_6.3V6-K

DDR_A_D[0..63] [7]
DDR_A_MA[0..16] [7]
DDR_A_DQS#[0..7] [7]
DDR_A_DQS[0..7] [7]

JDIMM1A ME@
FOX_AS0A826-H4RB-7H

DDR_A_D5	1 VSS_1	2 VSS_2	DDR_A_D0
	3 DQ5	4 DQ4	
DDR_A_D1	5 VSS_3	6 VSS_4	DDR_A_D4
	7 DQ1	8 DQ0	
DDR_A_DQS#0	9 VSS_5	10 VSS_6	
DDR_A_DQS0	11 DQS0_C	12 DM0_n/DBI0_n	
	13 DQS0_t	14 VSS_7	
DDR_A_D2	15 VSS_8	16 DQ6	DDR_A_D6
	17 DQ7	18 VSS_9	
DDR_A_D7	19 VSS_10	20 DQ2	DDR_A_D3
	21 DQ3	22 VSS_11	
DDR_A_D9	23 VSS_12	24 DQ12	DDR_A_D8
	25 DQ13	26 VSS_13	
DDR_A_D12	27 VSS_14	28 DQ8	DDR_A_D13
	29 DQ9	30 VSS_15	
	31 VSS_16	32 DQS1_c	DDR_A_DQS#1
	33 DM1_n/DBI1_n	34 DQS1_t	DDR_A_DQS1
DDR_A_D10	35 VSS_17	36 VSS_18	
	37 DQ15	38 DQ14	DDR_A_D11
DDR_A_D15	39 VSS_19	40 VSS_20	
	41 DQ10	42 DQ11	DDR_A_D14
DDR_A_D16	43 VSS_21	44 VSS_22	
	45 DQ21	46 DQ20	DDR_A_D17
DDR_A_D20	47 VSS_23	48 VSS_24	
	49 DQ17	50 DQ16	DDR_A_D21
DDR_A_DQS#2	51 VSS_25	52 VSS_26	
DDR_A_DQS2	53 DQS2_c	54 DM2_n/DBI2_n	
	55 DQS2_t	56 VSS_27	
DDR_A_D23	57 VSS_28	58 DQ22	DDR_A_D22
	59 DQ23	60 VSS_29	
DDR_A_D18	61 VSS_30	62 DQ18	DDR_A_D19
	63 DQ19	64 VSS_31	
DDR_A_D25	65 VSS_32	66 DQ28	DDR_A_D29
	67 DQ29	68 VSS_33	
DDR_A_D24	69 VSS_34	70 DQ24	DDR_A_D28
	71 DQ25	72 VSS_35	
	73 VSS_36	74 DQS3_c	DDR_A_DQS#3
	75 DM3_n/DBI3_n	76 DQS3_t	DDR_A_DQS3
DDR_A_D30	77 VSS_37	78 VSS_38	
	79 DQ30	80 DQ31	DDR_A_D31
DDR_A_D26	81 VSS_39	82 VSS_40	
	83 DQ26	84 DQ27	DDR_A_D27
	85 VSS_41	86 VSS_42	
	87 CB5/NC	88 CB4/NC	
	89 VSS_43	90 VSS_44	
	91 CB1/NC	92 CB0/NC	
	93 VSS_45	94 VSS_46	
DDR_A_DQS#8	95 DQS8_c	96 DM8_n/DBI8_n/NC	
DDR_A_DQS8	97 DQS8_t	98 VSS_47	
	99 VSS_48	100 CB6/NC	
	101 CB2/NC	102 VSS_49	
	103 VSS_50	104 CB7/NC	
	105 CB3/NC	106 VSS_51	
DDR_A_CKE0	107 VSS_52	108 RESET_n	DDR4_DRAMRST# [8,23]
	109 CKE0	110 CKE1	DDR_A_CKE1 [7]
DDR_A_BG1	111 VDD_1	112 VDD_2	
DDR_A_BG0	113 BG1	114 ACT_n	DDR_A_ACT_N
	115 BG0	116 ALERT_n	DDR_A_ALERT_N
DDR_A_MA12	117 VDD_3	118 VDD_4	
DDR_A_MA9	119 A12	120 A11	DDR_A_MA11
	121 A9	122 A7	DDR_A_MA7
DDR_A_MA8	123 VDD_5	124 VDD_6	
DDR_A_MA6	125 A8	126 A5	DDR_A_MA5
	127 A6	128 A4	DDR_A_MA4
	129 VDD_7	130 VDD_8	

[7] DDR_A_CKE0
[7] DDR_A_BG1
[7] DDR_A_BG0

JDIMM1B ME@

DDR_A_MA3	131 A3	132 A2	DDR_A_MA2
DDR_A_MA1	133 A1	134 EVENT_n/NF	EVENT_n_1
	135 VDD_9	136 VDD_10	
[7] DDR_A_DDRCLK0_1866M	137 CK0_t	138 CK1_t/NF	DDR_A_DDRCLK1_1866M
[7] DDR_A_DDRCLK0_1866M#	139 CK0_c	140 CK1_c/NF	DDR_A_DDRCLK1_1866M#
DDR_A_DDRCLK0_1866M	141 VDD_11	142 VDD_12	
DDR_A_DDRCLK0_1866M#	143 Parity	144 A0	DDR_A_MA0
[7] DDR_A_PARITY			
DDR_A_BA1	145 BA1	146 A10/AP	DDR_A_MA10
[7] DDR_A_BA1	147 VDD_13	148 VDD_14	
DDR_A_CS0#	149 CS0_n	150 BA0	DDR_A_BA0
[7] DDR_A_CS0#	151 A14/WE_n	152 A16/RAS_n	DDR_A_MA16
DDR_A_MA14	153 VDD_15	154 VDD_16	
DDR_A_ODT0	155 ODT0	156 A15/CAS_n	DDR_A_MA15
DDR_A_CS1#	157 CS1_n	158 A13	DDR_A_MA13
[7] DDR_A_ODT0	159 VDD_17	160 VDD_18	
[7] DDR_A_CS1#	161 ODT1	162 C0/CS2_n/NC	
DDR_A_ODT1	163 VDD_19	164 VREFCA	M_VREF_CA_DIMMA
[7] DDR_A_ODT1	165 C1/CS3_n/NC	166 SA2	SA2_CHA_P
	167 VSS_53	168 VSS_54	
DDR_A_D37	169 DQ37	170 DQ36	DDR_A_D33
	171 VSS_55	172 VSS_56	
DDR_A_D32	173 DQ33	174 DQ32	DDR_A_D36
	175 VSS_57	176 VSS_58	
DDR_A_DQS#4	177 DQS4_c	178 DM4_n/DBI4_n	
DDR_A_DQS4	179 DQS4_t	180 VSS_59	
	181 VSS_60	182 DQ39	DDR_A_D35
DDR_A_D38	183 DQ38	184 VSS_61	
	185 VSS_62	186 DQ35	DDR_A_D34
DDR_A_D39	187 DQ34	188 VSS_63	
	189 VSS_64	190 DQ45	DDR_A_D41
DDR_A_D40	191 DQ44	192 VSS_65	
	193 VSS_66	194 DQ41	DDR_A_D45
DDR_A_D44	195 DQ40	196 VSS_67	
	197 VSS_68	198 DQS5_c	DDR_A_DQS#5
	199 DM5_n/DBI5_n	200 DQS5_t	DDR_A_DQS5
	201 VSS_69	202 VSS_70	
DDR_A_D43	203 DQ46	204 DQ47	DDR_A_D42
	205 VSS_71	206 VSS_72	
DDR_A_D46	207 DQ42	208 DQ43	DDR_A_D47
	209 VSS_73	210 VSS_74	
DDR_A_D49	211 DQ52	212 DQ53	DDR_A_D48
	213 VSS_75	214 VSS_76	
DDR_A_D52	215 DQ49	216 DQ48	DDR_A_D53
	217 VSS_77	218 VSS_78	
DDR_A_DQS#6	219 DQS6_c	220 DM6_n/DBI6_n	
DDR_A_DQS6	221 DQS6_t	222 VSS_79	
	223 VSS_80	224 DQ54	DDR_A_D54
DDR_A_D50	225 DQ55	226 VSS_81	
	227 VSS_82	228 DQ50	DDR_A_D51
DDR_A_D55	229 DQ51	230 VSS_83	
	231 VSS_84	232 DQ60	DDR_A_D57
DDR_A_D56	233 DQ61	234 VSS_85	
	235 VSS_86	236 DQ57	DDR_A_D61
DDR_A_D60	237 DQ56	238 VSS_87	
	239 VSS_88	240 DQS7_c	DDR_A_DQS#7
	241 DM7_n/DBI7_n	242 DQS7_t	DDR_A_DQS7
DDR_A_D59	243 VSS_89	244 VSS_90	
	245 DQ62	246 DQ63	DDR_A_D63
DDR_A_D58	247 VSS_91	248 VSS_92	
	249 DQ58	250 DQ59	DDR_A_D62
CP_SMB_CLK	251 VSS_93	252 VSS_94	CP_SMB_DAT
[11,23,63] CP_SMB_CLK	253 SCL	254 SDA	SA0_CHA_P
	255 VDDSPD	256 SA0	CP_SMB_DAT [11,23,63]
	257 VPP_1	258 VTT	
	259 VPP_2	260 SA1	SA1_CHA_P
	261 GND_1	262 GND_2	

FOX_AS0A826-H4RB-7H

RF

RD5 240_0402_1%
DDR_A_DDRCLK1_1866M [7]
DDR_A_DDRCLK1_1866M# [7]
DDR_A_BA0 [7]
M_VREF_CA_DIMMA
CD27 2.2U_0402_6.3V6-M
CD28 0.1U_0402_10V7-K

+3VS
RD6 10K_0402_5% @ SA0_CHA_P
RD9 0_0402_5%
RD7 10K_0402_5% @ SA1_CHA_P
RD10 0_0402_5%
RD8 10K_0402_5% @ SA2_CHA_P
RD11 0_0402_5%

SPD Address = 0H

RD12 @ 0_0402_5%

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.
CD29 0.1U_0402_10V7-K
CD30 2.2U_0402_6.3V6-M

Place decoupling cap close to DIMM

RD1 1K_0402_1%
RD2 2_0402_1%
[7] DDR4_VREF_CA_CPU_A
CD13 0.022U_0402_25V7-K
RD4 24.9_0402_1%
RD3 1K_0402_1%
CD25 @ 0.1U_0402_16V7-K

RD13 240_0402_1%
RD14 240_0402_1%
DDR_A_DQS#8
DDR_A_DQS8

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V

CD34 10U_0603_6.3V6-M
CD35 10U_0603_6.3V6-M
CD36 10U_0603_6.3V6-M
CD37 10U_0603_6.3V6-M
CD38 10U_0603_6.3V6-M
CD39 10U_0603_6.3V6-M
CD40 10U_0603_6.3V6-M
CD41 10U_0603_6.3V6-M

+1.2V

CD49 1U_0402_6.3V6-K
CD50 1U_0402_6.3V6-K
CD51 1U_0402_6.3V6-K
CD52 1U_0402_6.3V6-K
CD53 1U_0402_6.3V6-K
CD54 1U_0402_6.3V6-K
CD55 1U_0402_6.3V6-K
CD56 1U_0402_6.3V6-K
CD57 330U_D2_2VM_R9M

Place decoupling cap on DRAM side.

[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+0.6VS

CD32 10U_0603_6.3V6-M
CD33 10U_0603_6.3V6-M
CD42 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM

[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+2.5V

CD45 10U_0603_6.3V6-M
CD46 10U_0603_6.3V6-M
CD47 1U_0402_6.3V6-K
CD48 1U_0402_6.3V6-K
CD68 1U_0402_6.3V6-K
CD66 1U_0402_6.3V6-K
CD67 1U_0402_6.3V6-K

Layout Note:
Place Close DIMMs

DDR_B_D[0..63] [8]
DDR_B_MA[0..16] [8]
DDR_B_DQS#[0..7] [8]
DDR_B_DQS[0..7] [8]

JDIMM2A ME@

FOX_AS0A826-H4SB-7H
SP071407011

JDIMM2B ME@

FOX_AS0A826-H4SB-7H
SP071407011

RD19 240_0402_1%

RD20 10K_0402_5% @ SA0_CHB_P
RD21 10K_0402_5% SA1_CHB_P
RD22 10K_0402_5% @ SA2_CHB_P
RD23 0_0402_5%
RD24 0_0402_5% @
RD25 0_0402_5%

SPD Address = 2H

RD26 0_0402_5% @

CD58 2.2U_0402_6.3V6-M @
CD59 0.1U_0402_10V7-K @
CD60 0.1U_0402_10V7-K
CD61 2.2U_0402_6.3V6-M

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.

Place decoupling cap close to DIMM

RD15 1K_0402_1%
RD16 2_0402_1%
RD17 1K_0402_1%
RD18 24.9_0402_1%
CD43 0.022U_0402_25V7-K
CD44 0.1U_0402_16V7-K

RD27 240_0402_1%
RD28 240_0402_1%

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Title: DDR4 CH-B PRIMARY

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Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_AON	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VS_AON	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_AON	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_AON	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VS_AON	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VS_AON				
STRAP3	+3VS_AON				
STRAP4	+3VS_AON				

X76

GPU	FB Memory (GDDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR	Samsung	K4W4G1646E-BC1A(E-Die)256MX16	PD 24.9K SD03424928T	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5TC4G63CFR-N0C(C-Die)256Mx16	PD 30.1K SD03430128T							
	Micron	MT41J256M16LY-091G:N	PD 20K SD02820028T							

Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: *VGA NOTE*

LCFC

Size	Document Number	Rev
B	*KENOBI*	2.0

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[15] PCIE_CTX_C_GRX_N[1..4]
[15] PCIE_CTX_C_GRX_P[1..4]
PCIE_CTX_C_GRX_N[1..4]
PCIE_CTX_C_GRX_P[1..4]
[15] PCIE_CRX_GTX_N[1..4]
[15] PCIE_CRX_GTX_P[1..4]
PCIE_CRX_GTX_N[1..4]
PCIE_CRX_GTX_P[1..4]

+3VS_AON
RV19 1 2 10K_0402_5% @

UV1A
COMMON
1/14 PCI_EXPRESS

DIS@
[28] VGA_PEX_RST# VGA_PEX_RST# 1 2 RV11 0_0402_5%

[10] CLK_PCIE_VGA
[10] CLK_PCIE_VGA#
CLK_PCIE_VGA
CLK_PCIE_VGA#

PCIE_CRX_GTX_P1 CV8 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N1 CV9 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_P2 CV10 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N2 CV11 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_P3 CV12 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N3 CV13 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_P4 CV21 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N4 CV22 1 2 DIS@ 0.22U_0402_10V6-K

AB6	PEX_WAKE*_NC		
AC7	PEX_RST*		
AC6	PEX_CLKREQ*		
AE8	PEX_REFCLK		
AD8	PEX_REFCLK*		
AC9	PEX_TX0	PCIE_CRX_C_GTX_P1	
AB9	PEX_TX0*	PCIE_CRX_C_GTX_N1	
AG6	PEX_RX0	PCIE_CTX_C_GRX_P1	
AG7	PEX_RX0*	PCIE_CTX_C_GRX_N1	
AB10	PEX_TX1	PCIE_CRX_C_GTX_P2	
AC10	PEX_TX1*	PCIE_CRX_C_GTX_N2	
AF7	PEX_RX1	PCIE_CTX_C_GRX_P2	
AE7	PEX_RX1*	PCIE_CTX_C_GRX_N2	
AD11	PEX_TX2	PCIE_CRX_C_GTX_P3	
AC11	PEX_TX2*	PCIE_CRX_C_GTX_N3	
AE9	PEX_RX2	PCIE_CTX_C_GRX_P3	
AF9	PEX_RX2*	PCIE_CTX_C_GRX_N3	
AC12	PEX_TX3	PCIE_CRX_C_GTX_P4	
AB12	PEX_TX3*	PCIE_CRX_C_GTX_N4	
AG9	PEX_RX3	PCIE_CTX_C_GRX_P4	
AG10	PEX_RX3*	PCIE_CTX_C_GRX_N4	

NC FOR GM108

AB13	NC_AB13
AC13	NC_AC13
AF10	NC_AF10
AE10	NC_AE10
AD14	NC_AD14
AC14	NC_AC14
AE12	NC_AE12
AF12	NC_AF12
AC15	NC_AC15
AB15	NC_AB15
AG12	NC_AG12
AG13	NC_AG13
AB16	NC_AB16
AC16	NC_AC16
AF13	NC_AF13
AE13	NC_AE13

NC FOR GF117/GK208/GM108

AD17	NC_AD17
AC17	NC_AC17
AE15	NC_AE15
AF15	NC_AF15
AC18	NC_AC18
AB18	NC_AB18
AG15	NC_AG15
AG16	NC_AG16
AB19	NC_AB19
AC19	NC_AC19
AF16	NC_AF16
AE16	NC_AE16
AD20	NC_AD20
AC20	NC_AC20
AE18	NC_AE18
AF18	NC_AF18
AC21	NC_AC21
AB21	NC_AB21
AG18	NC_AG18
AG19	NC_AG19
AD23	NC_AD23
AE23	NC_AE23
AF19	NC_AF19
AE19	NC_AE19
AF24	NC_AF24
AE24	NC_AE24
AE21	NC_AE21
AF21	NC_AF21
AG24	NC_AG24
AG25	NC_AG25
AG21	NC_AG21
AG22	NC_AG22

N15S-GM-A1_FCBGA595

DIS@

Under GPU / Near GPU / Midway between GPU and power supply

+1VS_VGA

PEX_IOVDD_1	AA22	1U_0402_6.3VA-K CV1
PEX_IOVDD_2	AB23	4.7U_0603_6.3VA-K CV3
PEX_IOVDD_3	AC24	10U_0603_6.3V6-M CV4
PEX_IOVDD_4	AD25	22U_0603_6.3V6-M CV6
PEX_IOVDD_5	AE26	
PEX_IOVDD_6	AE27	
PEX_IOVDDQ_1	AA10	1U_0402_6.3VA-K CV14
PEX_IOVDDQ_2	AA12	4.7U_0603_6.3VA-K CV16
PEX_IOVDDQ_3	AA13	10U_0603_6.3V6-M CV18
PEX_IOVDDQ_4	AA16	22U_0603_6.3V6-M CV19
PEX_IOVDDQ_5	AA18	
PEX_IOVDDQ_6	AA19	
PEX_IOVDDQ_7	AA20	
PEX_IOVDDQ_8	AA21	
PEX_IOVDDQ_9	AB22	
PEX_IOVDDQ_10	AC23	
PEX_IOVDDQ_11	AD24	
PEX_IOVDDQ_12	AE25	
PEX_IOVDDQ_13	AF26	
PEX_IOVDDQ_14	AF27	

NVVDD Decoupling

Capacitor Type	GB2B-64 NV DG	GB2B-64 Actual
4.7uF_0603	1	1
1uF_0402	1	1
22uF_0805	1	1
10uF_0805	1	1

NC FOR GF119

PEX_PLL_HVDD_1	AA8	+3VS_AON
PEX_PLL_HVDD_2	AA9	Place near GPU
PEX_SVDD_3V3	AB8	0.1U_0402_16V7-K CV23, 4.7U_0603_6.3VA-K CV24, 4.7U_0603_6.3VA-K CV25

+VGA_CORE

RV2 100_0402_1% DIS@
RV3 100_0402_1% DIS@

VDD_SENSE	F2	GFXCORE_VDD_SENSE_D [75]
GND_SENSE	F1	GFXCORE_GND_SENSE_D [75]

to VGA CORE Power IC sense pin

RV6 @ PEX_TSTCLK AF22 PEX_TSTCLK 1 2 200_0402_5%
PEX_TSTCLK* AE22 PEX_TSTCLK#

+1VS_VGA

PEX_PLLVDD_1 AA14
PEX_PLLVDD_2 AA15
Under GPU / Near GPU
0.1U_0402_16V7-K CV26, 1U_0402_6.3VA-K CV27, 4.7U_0603_6.3VA-K CV28

TESTMODE AD9 GPU_TESTMODE
RV8 10K_0402_5% DIS@

PEX_TERMP AF25 GPU_PEX_TERMP 2 2.49K_0402_1% RV10 DIS@

+3VS_AON
DV1
DGFX_PWRGD [28,75] DGFX_PWRGD 2
VDDQPWRGD [79] VDDQPWRGD 3
1 All_GPU_PWRGD All_GPU_PWRGD [11]
BAT54AW_SOT323-3 DIS@
RV21 10K_0402_5% DIS@
+3VS
RV9222 DIS@ 10K_0402_5% VDDQPWRGD

NV Suggest
+3VS_AON
QV1 2N7002KW_SOT323-3 DIS@
[10] CLKREQ_PCIE4_VGA#
CLKREQ_VGA#
RV5 10K_0402_5% DIS@
RV9 @ 10K_0402_5%
RV139 @ 1 2 0_0402_5%

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UV1K

N15S-GM-A1_FCBGA_595P
COMMON

3/14 DACA

	GF117/GM108
NC_W5	NC
NC_AE2	TSEN_VREF
NC_AF2	NC

GF117	GM108/GK208	
NC	I2CA_SCL	B7
NC	I2CA_SDA	A7
NC	NC_AE3	AE3
NC	NC_AE4	AE4
NC	NC_AG3	AG3
NC	NC_AF4	AF4
NC	NC_AF3	AF3
GM108 GF117	GK208	

N15S-GM-A1_FCBGA595

UV1G

N15S-GM-A1_FCBGA_595P
COMMON

4/14 IFPAB

NC_AA6
NC_V7
NC_W7
NC_W6
NC_Y6

NC FOR GF117/GM108

NC_AC4 AC4
NC_AC3 AC3
NC_Y3 Y3
NC_Y4 Y4
NC_AA2 AA2
NC_AA3 AA3
NC_AA1 AA1
NC_AB1 AB1
NC_AA5 AA5
NC_AA4 AA4
NC_AB4 AB4
NC_AB5 AB5
NC_AB2 AB2
NC_AB3 AB3
NC_AD2 AD2
NC_AD3 AD3
NC_AD1 AD1
NC_AE1 AE1
NC_AD5 AD5
NC_AD4 AD4

NC FOR GF117/GM108

GF117	
NC	GPIO14 B3

IFPAB

N15S-GM-A1_FCBGA595

UV1J

N15S-GM-A1_FCBGA_595P
COMMON

7/14 IFPEF

NC_J7
NC_K7
NC_K6
NC_H6
NC_J6

IFPE

NC FOR GF117/GK208/GM108

GF119/GK208		
DVI-DL	DVI-SL/HDMI	DP
I2CY_SDA	I2CY_SDA	NC_J3 J3
I2CY_SCL	I2CY_SCL	NC_J2 J2
TXC	TXC	NC_J1 J1
TXC	TXC	NC_K1 K1
TXD0	TXD0	NC_K3 K3
TXD0	TXD0	NC_K2 K2
TXD1	TXD1	NC_M3 M3
TXD1	TXD1	NC_M2 M2
TXD2	TXD2	NC_M1 M1
TXD2	TXD2	NC_N1 N1
NC FOR GK208		

NC FOR GF117/GM108

HPD_E	HPD_E	GPIO18 C2
NC FOR GF117		

GF119/GK208		
DVI-DL	DVI-SL/HDMI	DP
	I2CZ_SDA	NC_H4 H4
	I2CZ_SCL	NC_H3 H3
TXC		NC_J5 J5
TXC		NC_J4 J4
TXD3	TXD0	NC_K5 K5
TXD3	TXD0	NC_K4 K4
TXD4	TXD1	NC_L4 L4
TXD4	TXD1	NC_L3 L3
TXD5	TXD2	NC_M5 M5
TXD5	TXD2	NC_M4 M4
NC FOR GK208		

NC FOR GF117/GM108

HPD_F		GPIO19 F7
NC FOR GF117		

IFPF

N15S-GM-A1_FCBGA595

UV1I

N15S-GM-A1_FCBGA_595P
COMMON

6/14 IFPD

NC_U6
NC_T7
NC_R7
NC_R6

IFPD

NC FOR GF117/GM108

GF119/GK208		
DVI/HDMI		DP
I2CX_SDA		NC_P4 P4
I2CX_SCL		NC_P3 P3
TXC		NC_R5 R5
TXC		NC_R4 R4
TXD0		NC_T5 T5
TXD0		NC_T4 T4
TXD1		NC_U4 U4
TXD1		NC_U3 U3
TXD2		NC_V4 V4
TXD2		NC_V3 V3

NC FOR GF117/GM108

GF117	
NC	GPIO17 D4

N15S-GM-A1_FCBGA595

UV1H

N15S-GM-A1_FCBGA_595P
COMMON

5/14 IFPC

NC_T6
NC_M7
NC_N7
NC_P6

IFPC

NC FOR GF117/GM108

GF119/GK208		
DVI/HDMI		DP
I2CW_SDA		NC_N5 N5
I2CW_SCL		NC_N4 N4
TXC		NC_N3 N3
TXC		NC_N2 N2
TXD0		NC_R3 R3
TXD0		NC_R2 R2
TXD1		NC_R1 R1
TXD1		NC_T1 T1
TXD2		NC_T3 T3
TXD2		NC_T2 T2

NC FOR GF117/GM108

GF117	
NC	GPIO15 C3

N15S-GM-A1_FCBGA595

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UV1B
N15S-GM-A1_FCBGA_595P
COMMON
2/14 FBA

[31,32] FBA_D[63..0]

FBA_D0	E18	FBA_D0
FBA_D1	F18	FBA_D1
FBA_D2	E16	FBA_D2
FBA_D3	F17	FBA_D3
FBA_D4	D20	FBA_D4
FBA_D5	D21	FBA_D5
FBA_D6	F20	FBA_D6
FBA_D7	E21	FBA_D7
FBA_D8	E15	FBA_D8
FBA_D9	D15	FBA_D9
FBA_D10	F15	FBA_D10
FBA_D11	F13	FBA_D11
FBA_D12	C13	FBA_D12
FBA_D13	B13	FBA_D13
FBA_D14	E13	FBA_D14
FBA_D15	D13	FBA_D15
FBA_D16	B15	FBA_D16
FBA_D17	C16	FBA_D17
FBA_D18	A13	FBA_D18
FBA_D19	A15	FBA_D19
FBA_D20	B18	FBA_D20
FBA_D21	A18	FBA_D21
FBA_D22	A19	FBA_D22
FBA_D23	C19	FBA_D23
FBA_D24	B24	FBA_D24
FBA_D25	C23	FBA_D25
FBA_D26	A25	FBA_D26
FBA_D27	A24	FBA_D27
FBA_D28	A21	FBA_D28
FBA_D29	B21	FBA_D29
FBA_D30	C20	FBA_D30
FBA_D31	C21	FBA_D31
FBA_D32	R22	FBA_D32
FBA_D33	R24	FBA_D33
FBA_D34	T22	FBA_D34
FBA_D35	R23	FBA_D35
FBA_D36	N25	FBA_D36
FBA_D37	N26	FBA_D37
FBA_D38	N23	FBA_D38
FBA_D39	N24	FBA_D39
FBA_D40	V23	FBA_D40
FBA_D41	V22	FBA_D41
FBA_D42	T23	FBA_D42
FBA_D43	U22	FBA_D43
FBA_D44	Y24	FBA_D44
FBA_D45	AA24	FBA_D45
FBA_D46	Y22	FBA_D46
FBA_D47	AA23	FBA_D47
FBA_D48	AD27	FBA_D48
FBA_D49	AB25	FBA_D49
FBA_D50	AD26	FBA_D50
FBA_D51	AC25	FBA_D51
FBA_D52	AA27	FBA_D52
FBA_D53	AA26	FBA_D53
FBA_D54	W26	FBA_D54
FBA_D55	Y25	FBA_D55
FBA_D56	R26	FBA_D56
FBA_D57	T25	FBA_D57
FBA_D58	N27	FBA_D58
FBA_D59	R27	FBA_D59
FBA_D60	V26	FBA_D60
FBA_D61	V27	FBA_D61
FBA_D62	W27	FBA_D62
FBA_D63	W25	FBA_D63

[31,32] FBA_DQM[7..0]

FBA_DQM0	D19	FBA_DQM0
FBA_DQM1	D14	FBA_DQM1
FBA_DQM2	C17	FBA_DQM2
FBA_DQM3	C22	FBA_DQM3
FBA_DQM4	P24	FBA_DQM4
FBA_DQM5	W24	FBA_DQM5
FBA_DQM6	AA25	FBA_DQM6
FBA_DQM7	U25	FBA_DQM7

[31,32] FBA_DQS[7..0]

FBA_DQS0	E19	FBA_DQS_WP0
FBA_DQS1	C15	FBA_DQS_WP1
FBA_DQS2	B16	FBA_DQS_WP2
FBA_DQS3	B22	FBA_DQS_WP3
FBA_DQS4	R25	FBA_DQS_WP4
FBA_DQS5	W23	FBA_DQS_WP5
FBA_DQS6	AB26	FBA_DQS_WP6
FBA_DQS7	T26	FBA_DQS_WP7

[31,32] FBA_DQS#[7..0]

FBA_DQS#0	F19	FBA_DQS_RN0
FBA_DQS#1	C14	FBA_DQS_RN1
FBA_DQS#2	A16	FBA_DQS_RN2
FBA_DQS#3	A22	FBA_DQS_RN3
FBA_DQS#4	P25	FBA_DQS_RN4
FBA_DQS#5	W22	FBA_DQS_RN5
FBA_DQS#6	AB27	FBA_DQS_RN6
FBA_DQS#7	T27	FBA_DQS_RN7

NC — FB_CLAMP
GF119

F3 GPU_FB_CLAMP
RV12 DIS@ 10K_0402_5%

FBA_CMD0	C27	FBA_CSA0#
FBA_CMD1	C26	
FBA_CMD2	E24	FBA_ODTA0
FBA_CMD3	F24	FBA_CKEA0
FBA_CMD4	D27	FBA_MA14
FBA_CMD5	D26	FBA_RST#
FBA_CMD6	F25	FBA_MA9
FBA_CMD7	F26	FBA_MA7
FBA_CMD8	F23	FBA_MA2
FBA_CMD9	G22	FBA_MA0
FBA_CMD10	G23	FBA_MA4
FBA_CMD11	G24	FBA_MA1
FBA_CMD12	F27	FBA_BA0
FBA_CMD13	G25	FBA_WE#
FBA_CMD14	G27	
FBA_CMD15	G26	FBA_CAS#
FBA_CMD16	M24	FBA_CSA1#
FBA_CMD17	M23	
FBA_CMD18	K24	FBA_ODTA1
FBA_CMD19	K23	FBA_CKEA1
FBA_CMD20	M27	FBA_MA13
FBA_CMD21	M26	FBA_MA8
FBA_CMD22	M25	FBA_MA6
FBA_CMD23	K26	FBA_MA11
FBA_CMD24	K22	FBA_MA5
FBA_CMD25	J23	FBA_MA3
FBA_CMD26	J25	FBA_BA2
FBA_CMD27	J24	FBA_BA1
FBA_CMD28	K27	FBA_MA12
FBA_CMD29	K25	FBA_MA10
FBA_CMD30	J27	FBA_RAS#
FBA_CMD31	J26	

FBA_CSA0# → FBA_CSA0# [31]
FBA_ODTA0 → FBA_ODTA0 [31]
FBA_CKEA0 → FBA_CKEA0 [31]
FBA_RST# → FBA_RST# [31,32]
FBA_BA0 → FBA_BA0 [31,32]
FBA_WE# → FBA_WE# [31,32]
FBA_CAS# → FBA_CAS# [31,32]
FBA_CSA1# → FBA_CSA1# [32]
FBA_ODTA1 → FBA_ODTA1 [32]
FBA_CKEA1 → FBA_CKEA1 [32]
FBA_BA2 → FBA_BA2 [31,32]
FBA_BA1 → FBA_BA1 [31,32]
FBA_RAS# → FBA_RAS# [31,32]

FBA_MA[0..14] [31,32]

GF117/GF119 GK208
NC — FBA_CMD32
FBA_DEBUG0 — FBA_CMD34
FBA_DEBUG1 — FBA_CMD35

B19 FBA_CMD32
F22 FBA_CMD34
J22 FBA_CMD35

RV17 @0_0402_5%
RV18 @0_0402_5%
For Debug
+1.5VS_VGA

FBA_CLK0	D24	FBA_CLKA0
FBA_CLK0*	D25	FBA_CLKA0#
FBA_CLK1	N22	FBA_CLKA1
FBA_CLK1*	M22	FBA_CLKA1#

FBA_CLKA0 → FBA_CLKA0 [31]
FBA_CLKA0# → FBA_CLKA0# [31]
FBA_CLKA1 → FBA_CLKA1 [32]
FBA_CLKA1# → FBA_CLKA1# [32]

FBA_WCK01	D18	
FBA_WCK01*	C18	
FBA_WCK23	D17	
FBA_WCK23*	D16	
FBA_WCK45	V24	
FBA_WCK45*	U24	
FBA_WCK67	V24	
FBA_WCK67*	V25	

GF119 — FB_PLLAVDD_1
NC — FB_PLLAVDD_2
FB_PLLAVDD — FB_DLLAVDD
GF117

F16 FB_PLL
P22
H22

LV3 DIS@ MPZ1608S300AT_2P~D
+1VS_VGA

0.1U_0402_16V7-K CV39 DIS@
0.1U_0402_16V7-K CV40 DIS@
0.1U_0402_16V7-K CV41 DIS@
22U_0603_6.3V6-M CV42 DIS@
Under GPU

FBA_RST#
FBA_ODTA0
FBA_ODTA1
FBA_CKEA0
FBA_CKEA1

RV13 DIS@ 10K_0402_5%
RV14 DIS@ 10K_0402_5%
RV15 DIS@ 10K_0402_5%
RV16 DIS@ 10K_0402_5%
RV20 DIS@ 10K_0402_5%

PTP1 Test_Point_12MIL
D23 FB_VREF

N15S-GM-A1_FCBGA595

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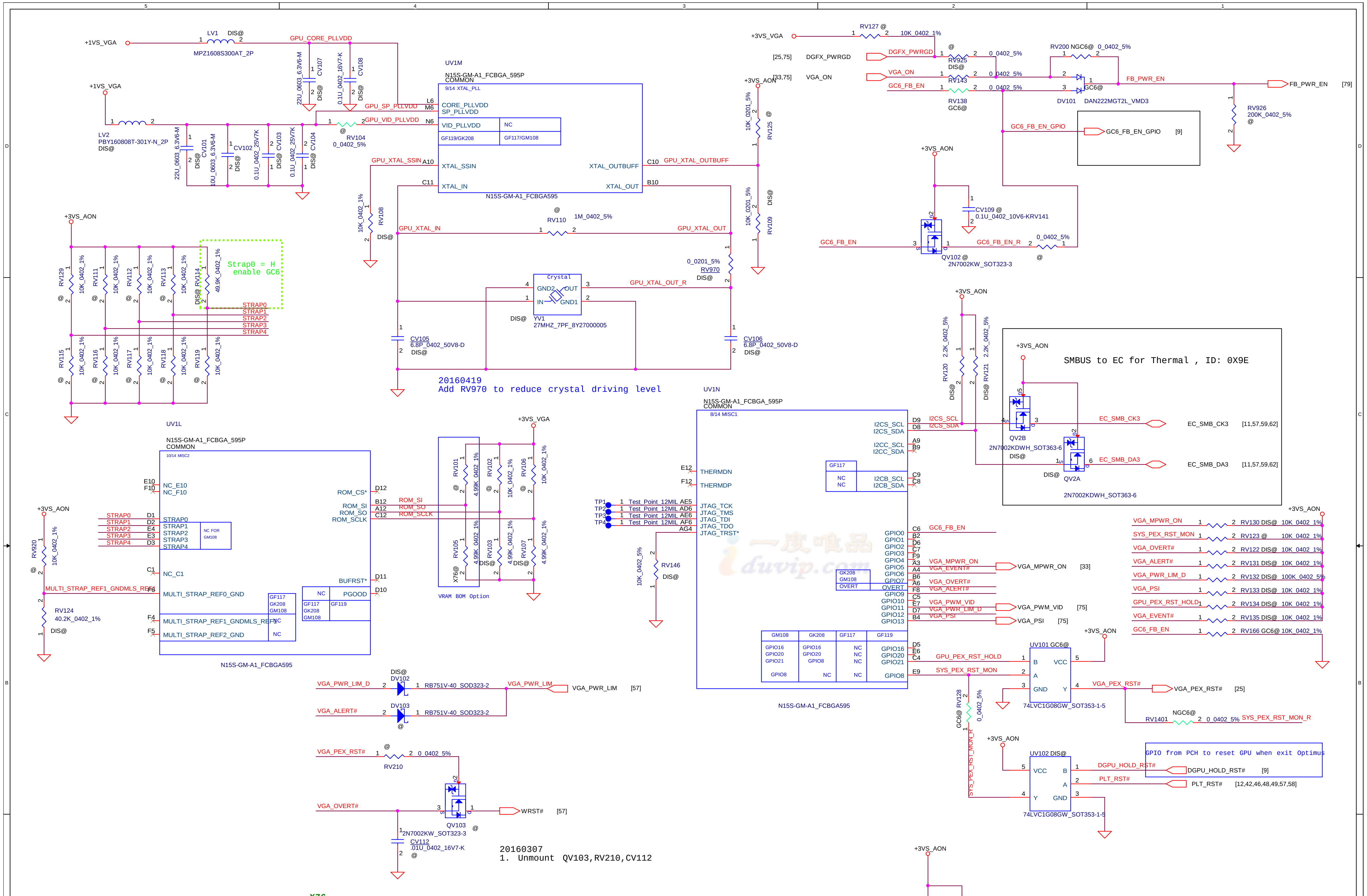

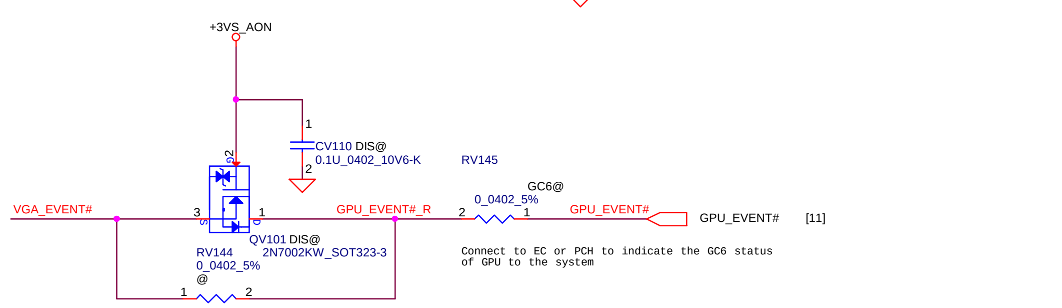

X76

GPU	FB Memory (GDDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR	Samsung	K4W4G1646E-BC1A(E-Die)256MX16	PD 24.9K SD03424928T	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5TC4G63CFR-N0C(C-Die)256Mx16	PD 30.1K SD03430128T							
	Micron	MT41J256M16LY-091G:N	PD 20K SD02820028T							

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UV1D

N15S-GM-A1_FCBGA_595P
COMMON

+1.5VS_VGA

0.1U_0402_16V7-K CV237 DIS@
0.1U_0402_16V7-K CV235 DIS@
1U_0402_6.3V7-K CV230 DIS@
1U_0402_6.3V7-K CV226 DIS@
4.7U_0603_6.3V6-K CV224 DIS@
4.7U_0603_6.3V6-K CV219 DIS@
Place under GPU

10U_0603_6.3V6-M CV206 DIS@
22U_0603_6.3V6-M CV204 DIS@
Place near GPU

12/14 FBVDDQ

B26 FBVDDQ_01
C25 FBVDDQ_02
E23 FBVDDQ_03
E26 FBVDDQ_04
F14 FBVDDQ_05
F21 FBVDDQ_06
G13 FBVDDQ_07
G14 FBVDDQ_08
G15 FBVDDQ_09
G16 FBVDDQ_10
G18 FBVDDQ_11
G19 FBVDDQ_12
G20 FBVDDQ_13
G21 FBVDDQ_14
L22 FBVDDQ_19
L24 FBVDDQ_20
L26 FBVDDQ_21
M21 FBVDDQ_22
N21 FBVDDQ_23
R21 FBVDDQ_24
T21 FBVDDQ_25
V21 FBVDDQ_26
W21 FBVDDQ_27

GF117 GF119 GK208

H24 FBVDDQ_AON_H24 FBVDDQ
H26 FBVDDQ_AON_H26 FBVDDQ
J21 FBVDDQ_AON_J21 FBVDDQ
K21 FBVDDQ_AON_K21 FBVDDQ

FB_CAL_VDDQ D22 FB_CAL_VDDQ RV203 40.2_0402_1% DIS@
FB_CAL_GND C24 FB_CAL_GND RV202 42.2_0402_1% DIS@
FB_CAL_TERM B25 FB_CAL_TERM RV201 51.1_0402_1% DIS@
+1.5VS_VGA

N15S-GM-A1_FCBGA595

UV1C

N15S-GM-A1_FCBGA_595P
COMMON

14/14 XVDD/VDD33

AD10 AD7 NC_AD10 NC_AD7 GM108
VDD33_MAIN_G8 G8
VDD33_MAIN_G9 G9
3V3_AON VDD33_AON_G10 G10
3V3_AON VDD33_AON_G12 G12
F11 NC_F11
V5 V6 FERMI_RSVD1 FERMI_RSVD2

CONFIGURABLE
POWER CHANNELS
* nc on substrate

G1 G2 G3 G4 G5 G6 G7 NC_G1 NC_G2 NC_G3 NC_G4 NC_G5 NC_G6 NC_G7
V1 V2 NC_V1 NC_V2
W1 W2 W3 W4 NC_W1 NC_W2 NC_W3 NC_W4

N15S-GM-A1_FCBGA595

Under GPU
+3VS_VGA
0.1U_0402_16V7-K CV234 DIS@
0.1U_0402_16V7-K CV236 DIS@
1U_0402_6.3V7-K CV228 DIS@
4.7U_0603_6.3V6-K CV207 DIS@

Under GPU
+3VS_AON
0.1U_0402_16V7-K CV238 DIS@
1U_0402_6.3V7-K CV232 DIS@
4.7U_0603_6.3V6-K CV215 DIS@

+VGA_CORE

1U_0402_6.3V7-K CV231 DIS@
1U_0402_6.3V7-K CV227 DIS@
1U_0402_6.3V7-K CV229 DIS@
1U_0402_6.3V7-K CV233 DIS@
4.7U_0603_6.3V6-K CV217 DIS@
4.7U_0603_6.3V6-K CV211 DIS@
4.7U_0603_6.3V6-K CV209 DIS@
4.7U_0603_6.3V6-K CV218 DIS@
4.7U_0603_6.3V6-K CV222 DIS@
4.7U_0603_6.3V6-K CV213 DIS@
4.7U_0603_6.3V6-K CV223 DIS@
4.7U_0603_6.3V6-K CV214 DIS@
4.7U_0603_6.3V6-K CV208 DIS@
4.7U_0603_6.3V6-K CV216 DIS@
Place under GPU

4.7U_0603_6.3V6-K CV212 DIS@
4.7U_0603_6.3V6-K CV220 DIS@
4.7U_0603_6.3V6-K CV221 DIS@
4.7U_0603_6.3V6-K CV210 DIS@
4.7U_0603_6.3V6-K CV225 DIS@
22U_0603_6.3V6-M CV205 DIS@
47U_0805_4V6-M CV203 DIS@
CV201 330U_D2_2V_Y DIS@
Place near GPU
check with power team for >22UF CAP placement

UV1E

N15S-GM-A1_FCBGA_595P
COMMON

11/14 NVVDD

K10 K12 K14 K16 K18 L11 L13 L15 L17 M10 M12 M14 M16 M18 N11 N13 N15 N17 P10 P12 P14 P16 P18 R11 R13 R15 R17 T10 T12 T14 T16 T18 U11 U13 U15 U17 V10 V12 V14 V16 V18
VDD_001 VDD_002 VDD_003 VDD_004 VDD_005 VDD_006 VDD_007 VDD_008 VDD_009 VDD_010 VDD_011 VDD_012 VDD_013 VDD_014 VDD_015 VDD_016 VDD_017 VDD_018 VDD_019 VDD_020 VDD_021 VDD_022 VDD_023 VDD_024 VDD_025 VDD_026 VDD_027 VDD_028 VDD_029 VDD_030 VDD_031 VDD_032 VDD_033 VDD_034 VDD_035 VDD_036 VDD_037 VDD_038 VDD_039 VDD_040 VDD_041

N15S-GM-A1_FCBGA595

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UV1F

N15S-GM-A1_FCBGA_595P
COMMON

13/14 GND

A2	GND_001	GND_071	M13
AB17	GND_005	GND_072	M15
AB20	GND_006	GND_073	M17
AB24	GND_007	GND_074	N10
AC2	GND_008	GND_075	N12
AC22	GND_009	GND_076	N14
AC26	GND_010	GND_077	N16
AC5	GND_011	GND_078	N18
AC8	GND_012	GND_079	P11
AD12	GND_013	GND_080	P13
AD13	GND_014	GND_081	P15
A26	GND_002	GND_082	P17
AD15	GND_015	GND_083	P2
AD16	GND_016	GND_084	P23
AD18	GND_017	GND_085	P26
AD19	GND_018	GND_086	P5
AD21	GND_019	GND_087	R10
AD22	GND_020	GND_088	R12
AE11	GND_021	GND_089	R14
AE14	GND_022	GND_090	R16
AE17	GND_023	GND_091	R18
AE20	GND_024	GND_092	T11
AB11	GND_003	GND_093	T13
AF1	GND_025	GND_094	T15
AF11	GND_026	GND_095	T17
AF14	GND_027	GND_096	U10
AF17	GND_028	GND_097	U12
AF20	GND_029	GND_098	U14
AF23	GND_030	GND_099	U16
AF5	GND_031	GND_100	U18
AF8	GND_032	GND_101	U2
AG2	GND_033	GND_102	U23
AG26	GND_034	GND_103	U26
AB14	GND_004	GND_104	U5
B1	GND_035	GND_105	V11
B11	GND_036	GND_106	V13
B14	GND_037	GND_107	V15
B17	GND_038	GND_108	V17
B20	GND_039	GND_109	Y2
B23	GND_040	GND_110	Y23
B27	GND_041	GND_111	Y26
B5	GND_042	GND_112	Y5
B8	GND_043		
E11	GND_044		
E14	GND_045		
E17	GND_046		
E2	GND_047		
E20	GND_048		
E22	GND_049		
E25	GND_050		
E5	GND_051		
E8	GND_052		
H2	GND_053		
H23	GND_054		
H25	GND_055		
H5	GND_056		
K11	GND_057		
K13	GND_058		
K15	GND_059		
K17	GND_060		
L10	GND_061		
L12	GND_062		
L14	GND_063		
L16	GND_064		
L18	GND_065		
L2	GND_066		
L23	GND_067		
L25	GND_068		
L5	GND_069	GND_AA7	AA7
M11	GND_070	GND_AB7	AB7

N15S-GM-A1_FCBGA595

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Title: *N16S-GT GND*

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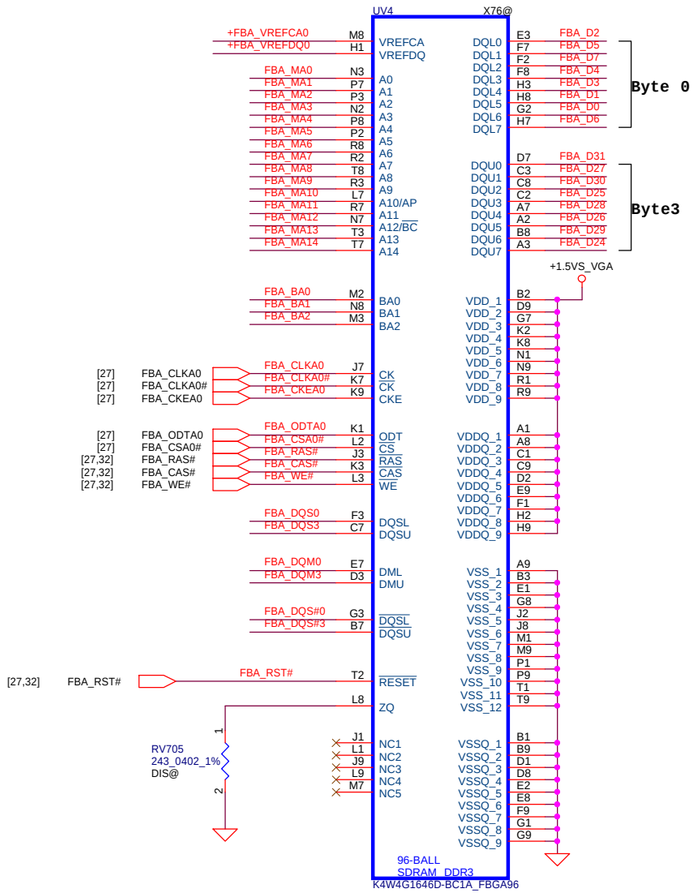
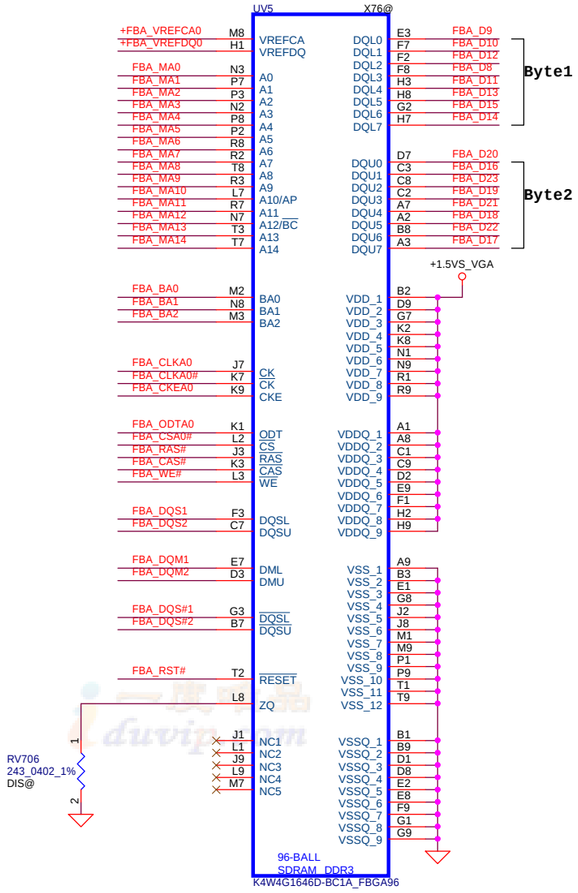
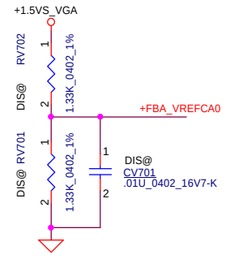
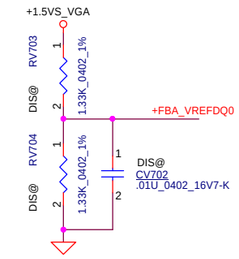
Memory Partition A - Lower 32 bits

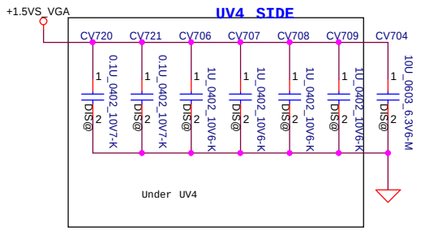


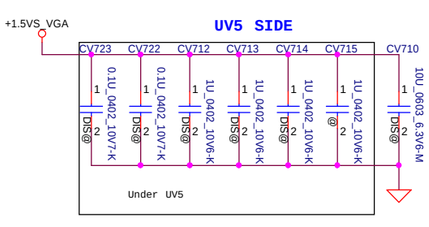


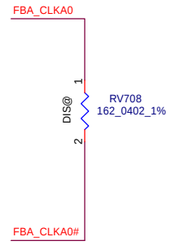
FBA_MA[14..0] [27,32]
FBA_BA[2..0] [27,32]
FBA_DQS[7..0] [27,32]
FBA_DQM[7..0] [27,32]
FBA_DQS#[7..0] [27,32]
FBA_D[0..63] [27,32]











Security Classification	LC Future Center Secret Data		
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Title	N16S-GT DDR3L VRAM L	
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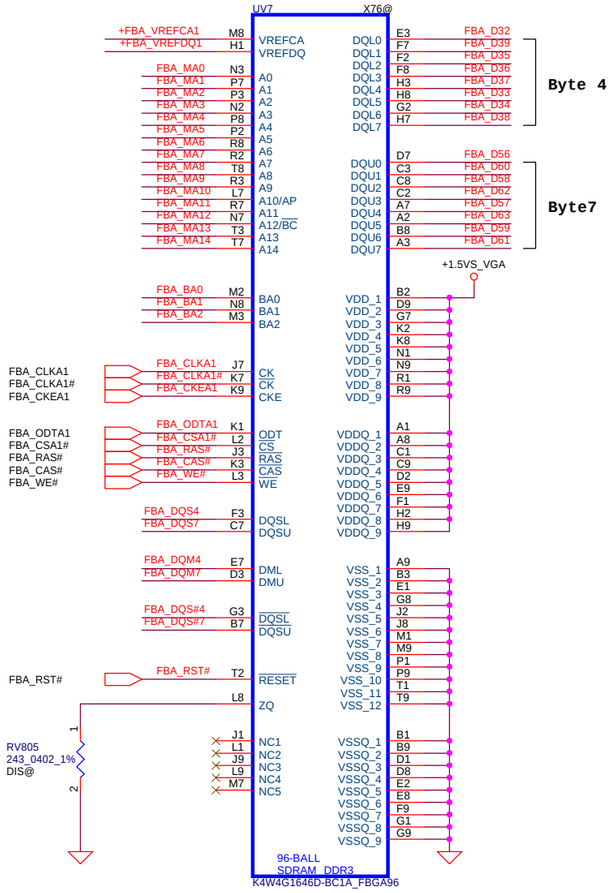
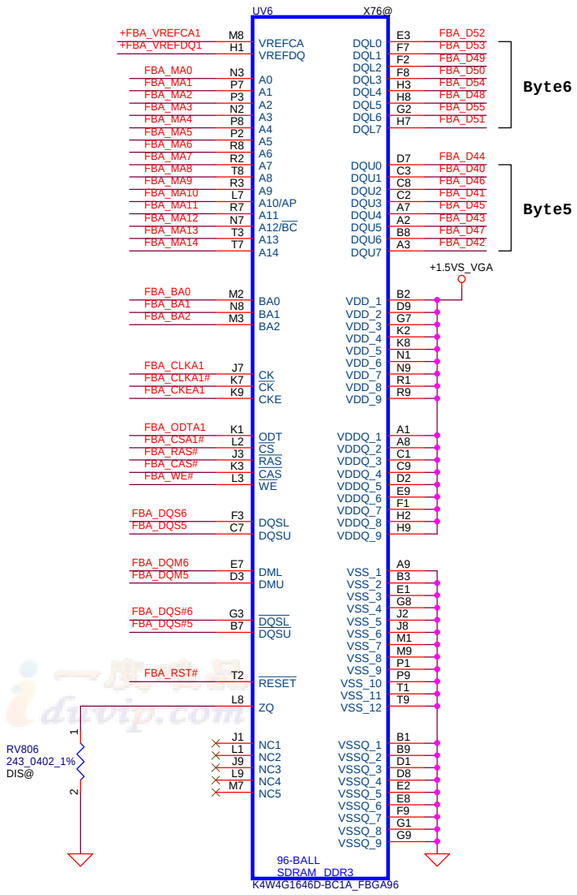
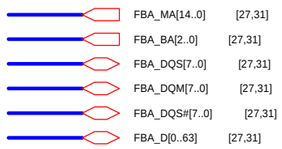
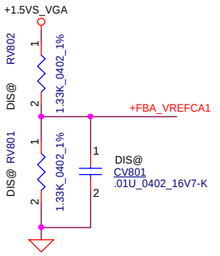
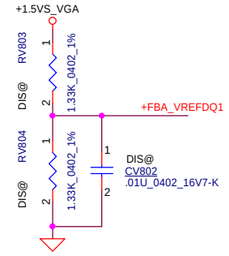
Memory Partition A - Upper 32 bits

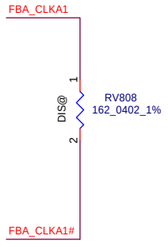


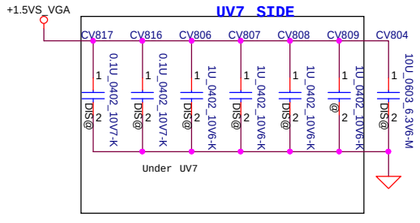


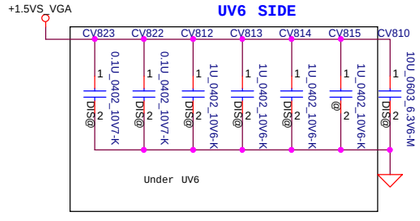












Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/28	Deciphered Date	2016/08/27

Title	N16S-GT DDR3L VRAM U		
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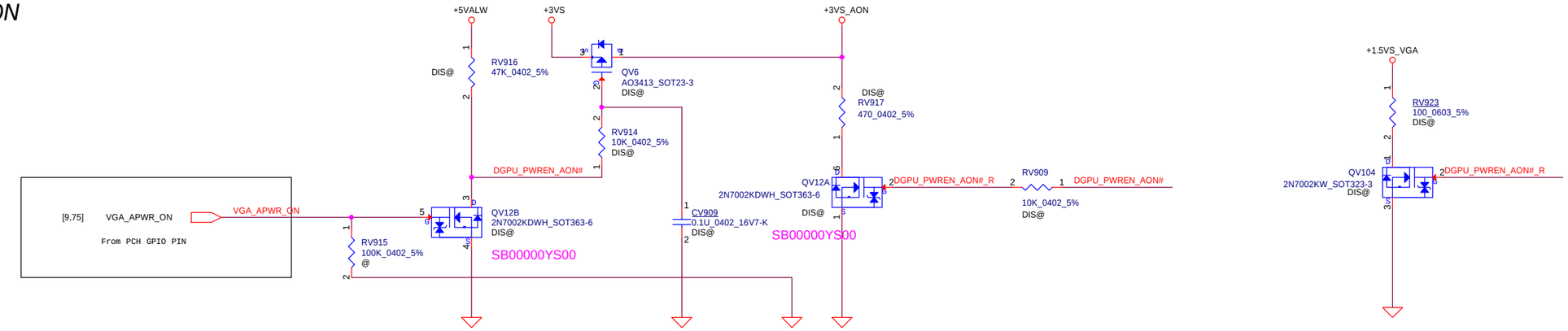
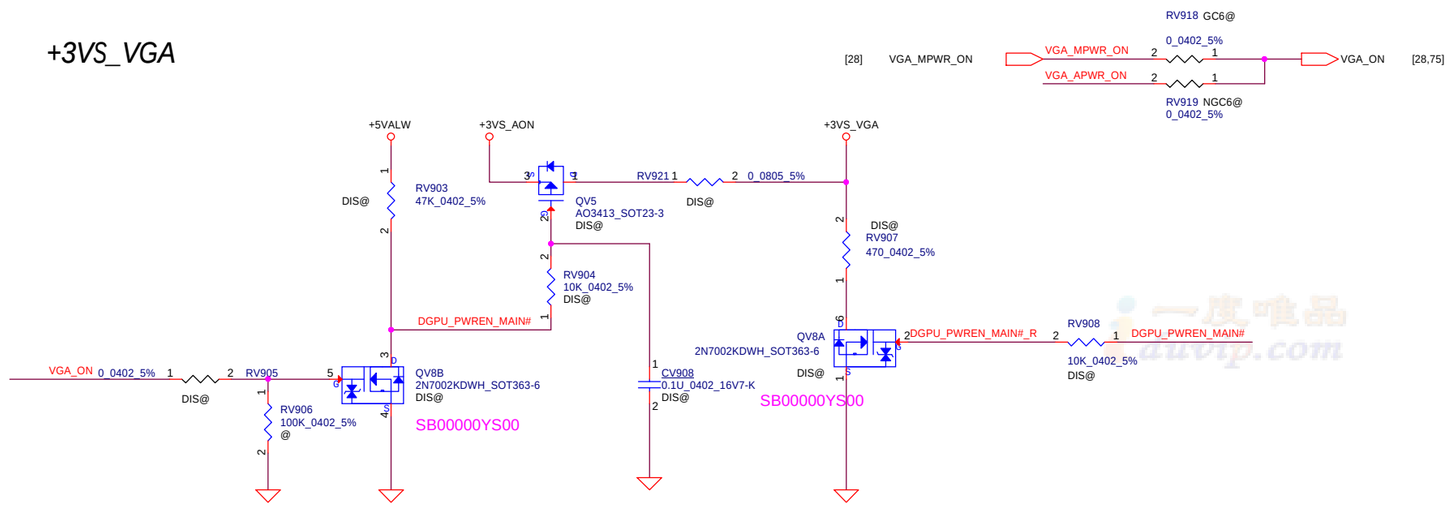
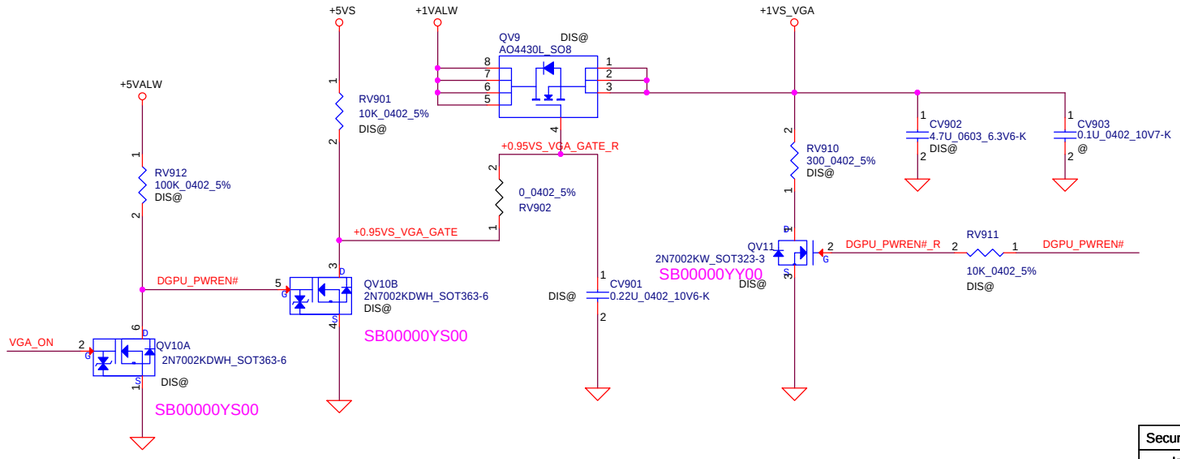
+3VS to +3VS_AON



+3VS_VGA



+1VALW to +1VS_VGA



Security Classification	LC Future Center Secret Data		
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Title	N16S-GT swich power		
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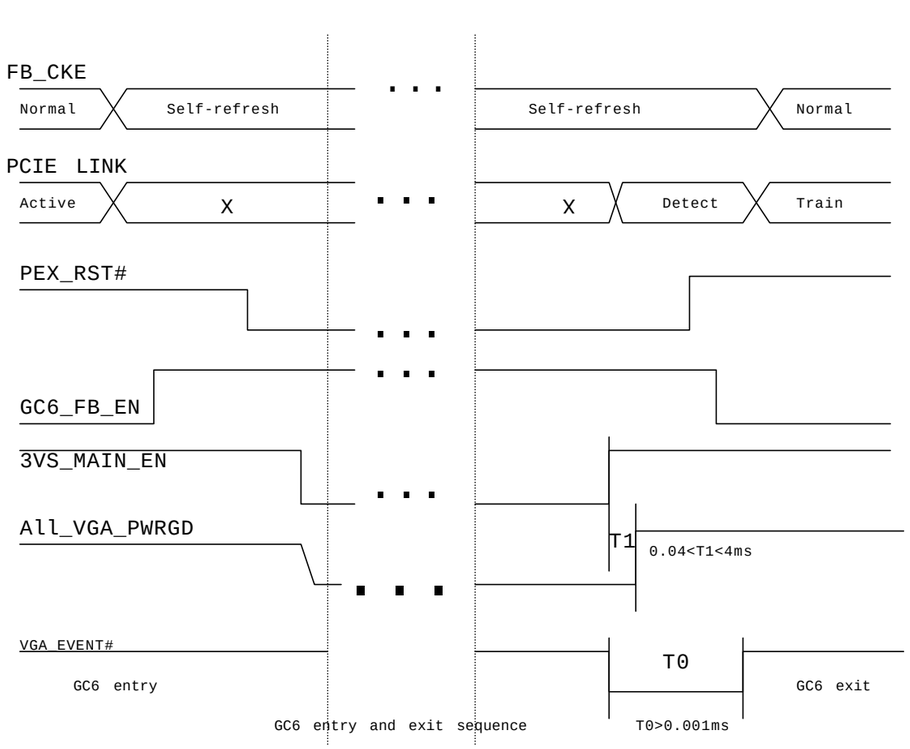
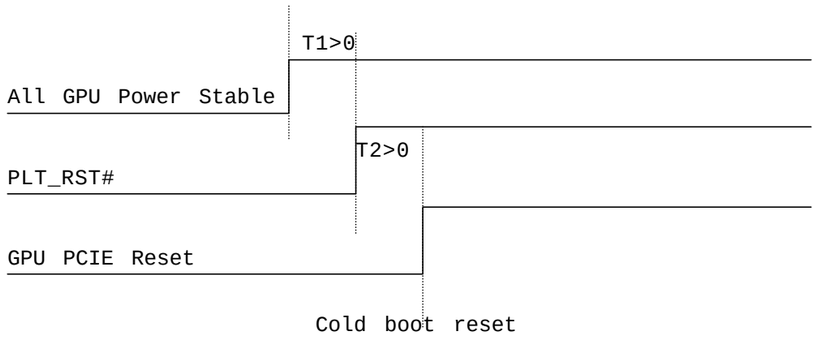
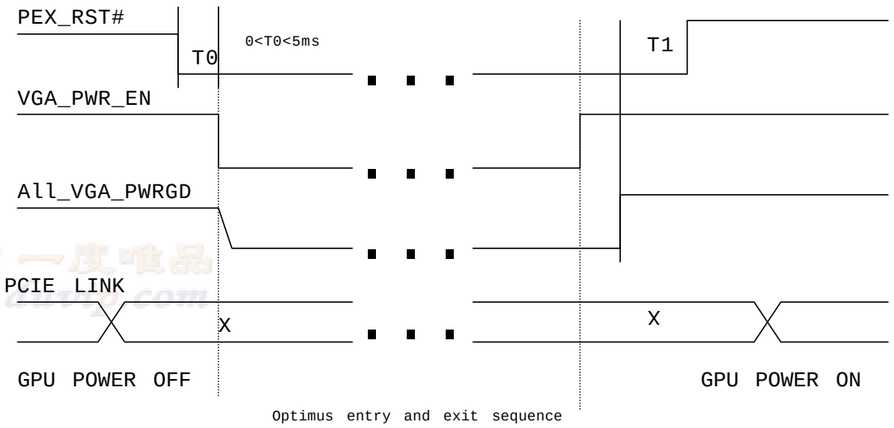
GPIO	I/O	Functional Description	I/O Termination
GPIO0	O	FB Enable for GC6 2.0, Open source	10K pull-down
GPIO1	O	Memory voltage control	Pull-up/pull down to set the FBVDD/Q boot voltage
GPIO2	O	Panel Backlight PWM Brightness Control	100K pull down
GPIO3	O	Panel Power Enable	100K pull down
GPIO4	O	Panel Backlight Enable	100K pull down
GPIO5	O	GPU Power Sequence for GC6 2.0, Open Drain	10k pull-up to 3V3_AON
GPIO6	I	GPU wake signal for GC6 2.0	10k pull-up to 3V3_AON
GPIO7	O	3D Vision L/R signal	100K pull down
GPIO8	O	System side PCIe rest monitor	10k pull-up to 3V3_AON
GPIO9	I/O	Active low thermal alert, open drain	10k pull-up to 3V3_AON
GPIO10	O	Memory VREF Control	100K pull down
GPIO11	O	GPU Core VDD PWM control signal	
GPIO12	I	AC power detect or power supply overdraw input	100k pull-up to 3V3_AON
GPIO13	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase
GPIO14	I	Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI	
GPIO15	I	Hot Plug Detect for IFPC	
GPIO16	I	Active Low Frame Lock, Open Drain	10k pull-up to 3V3_AON
GPIO17	I	Hot Plug Detect for IFPD	
GPIO18	I	Hot Plug Detect for IFPE	
GPIO19	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	
GPIO20	O	Reserved	
GPIO21	O	GPU PCIe self-reset control, Open Drain	10k pull-up to 3V3_AON
OVERT	I/O	Catastrophic Over Temperature	100k pull-up to 3V3_AON







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Title: **GPU GPIO table & sequence**

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Title: *Blank*

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Size	Document Number	Rev
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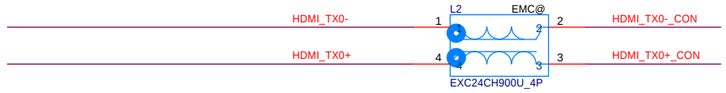
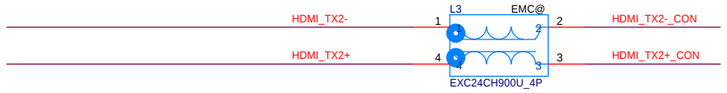
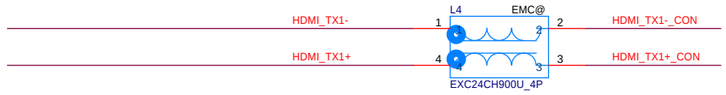
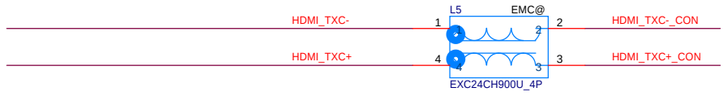
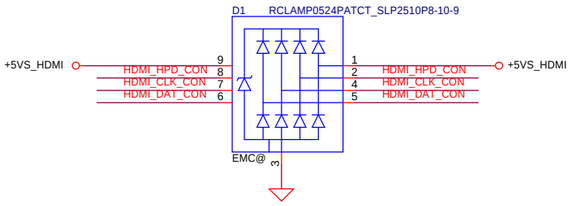
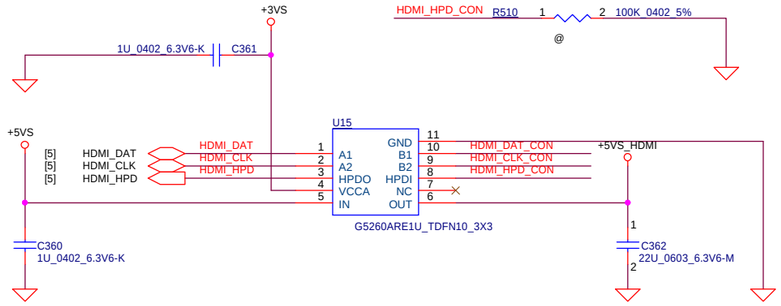


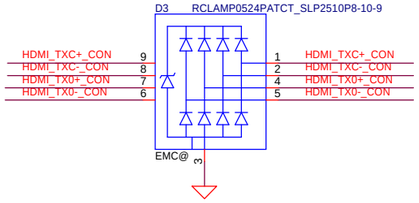


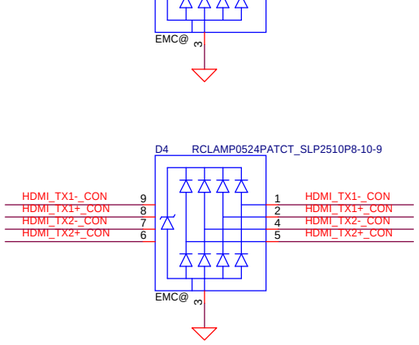


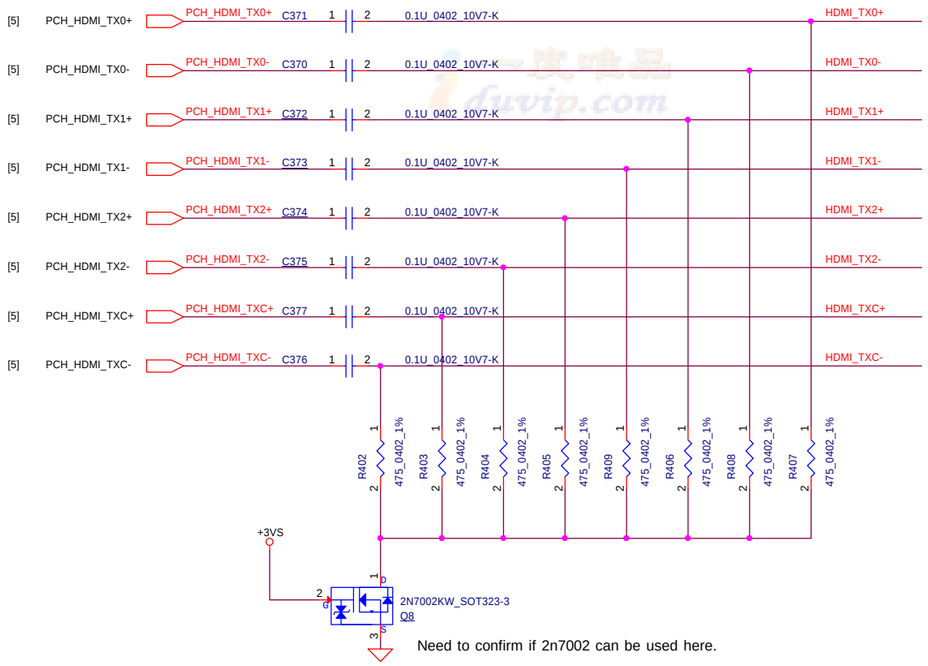




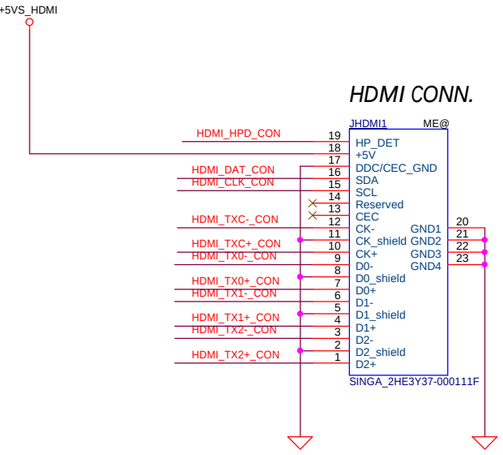








Need to confirm if 2n7002 can be used here.



HDMI CONN.

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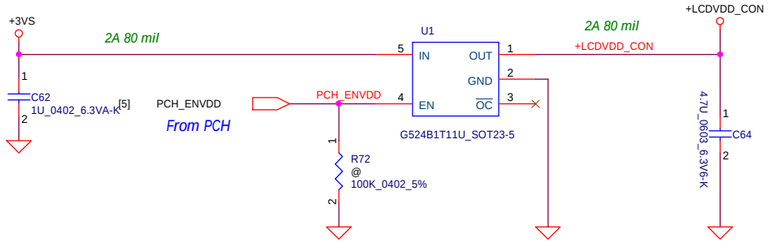
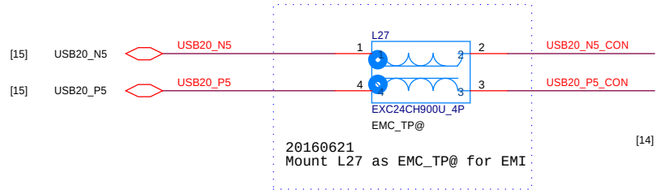
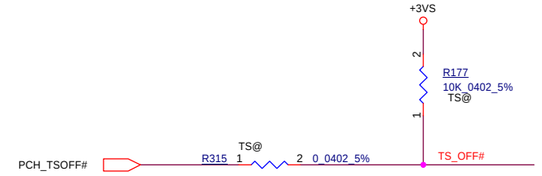
LCDVDD Circuit



Touch Panel

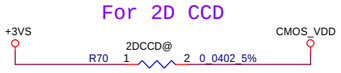


20160621
Mount L27 as EMC_TP@ for EMI

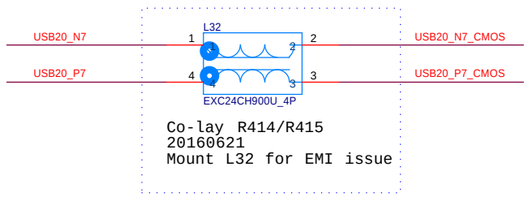


When lid# active. BIOS turn off touch screen.

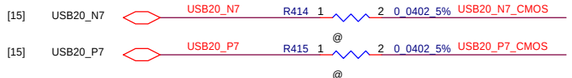
CMOS Camera



CMOS USB Port

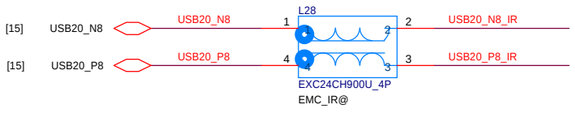


Co-lay R414/R415
20160621
Mount L32 for EMI issue

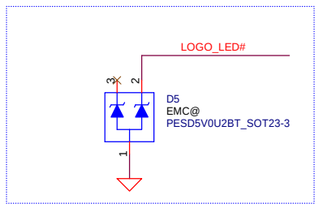


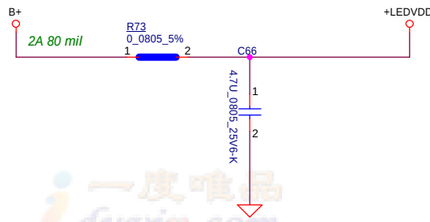
2D camera module mount choke already

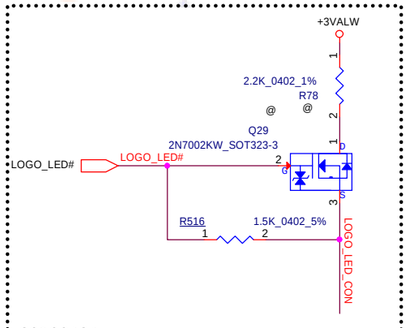
IR camera USB Port



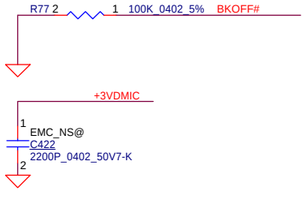
ESD request

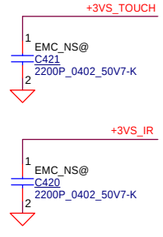




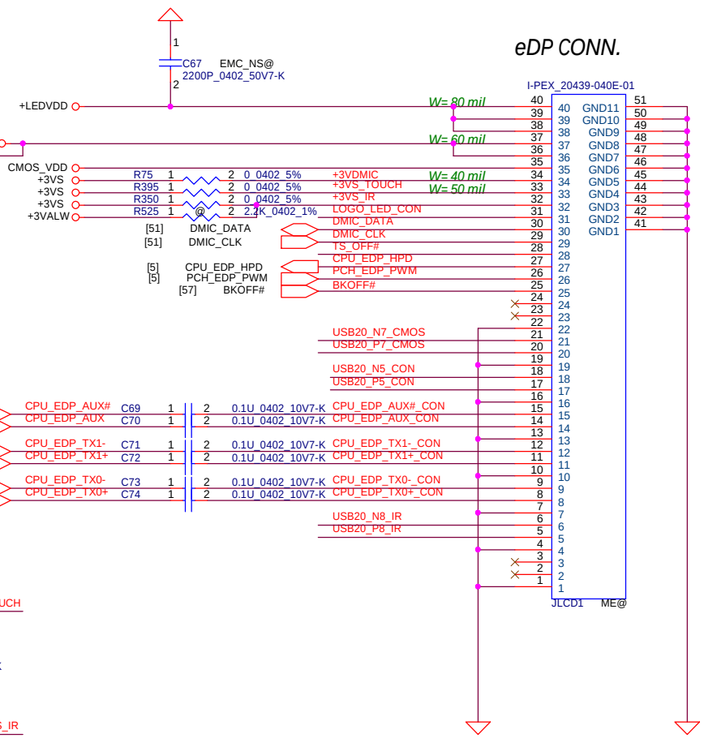


20160424
1. Change R516 from 100 to 1.5Kohm
for LED brightness





eDP CONN.



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Title: *HDMI RP*

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Title: ***CRT CONN***

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Title: *DP to VGA*

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Title: ***Mux IC***

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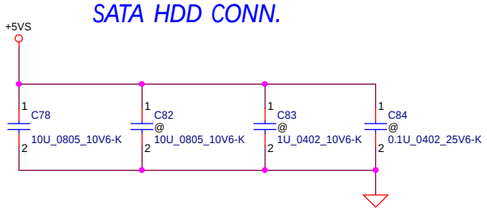
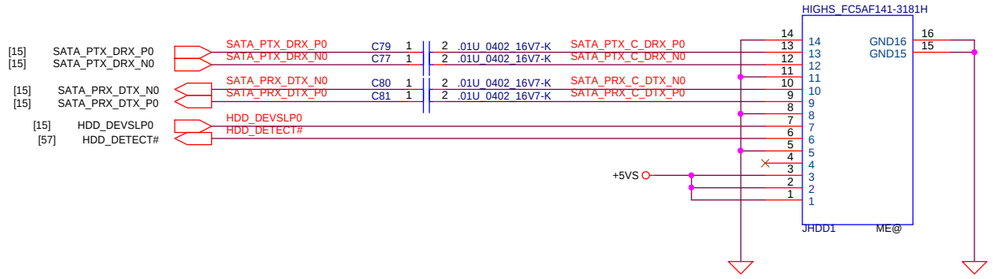
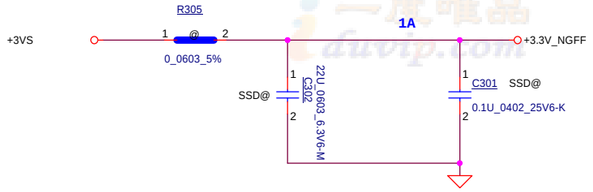
SATA HDD CONN.



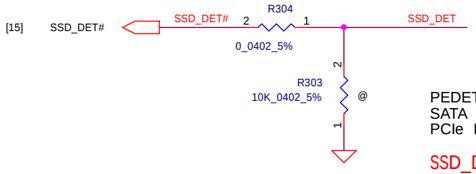
SATA HDD CONN.





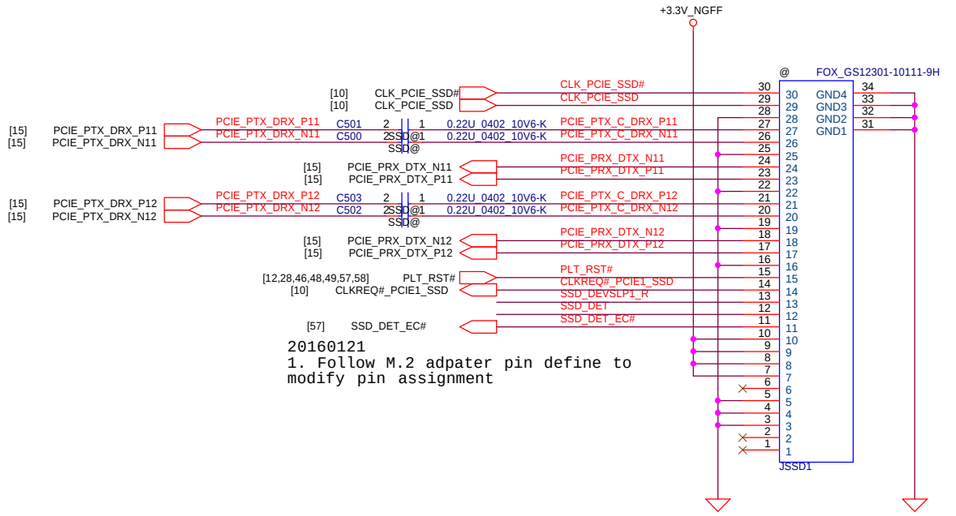
M.2 SSD(SATA/PCIE)

20160308
1. Remove R300,R301,R302 and put it to CPU side



PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open

SSD_DET#
0 - SATA
1 - PCIE



20160121
1. Follow M.2 adpater pin define to modify pin assignment

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: SATA HDD

Size	Document Number	Rev
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: ***ODD***

Size	Document Number	Rev
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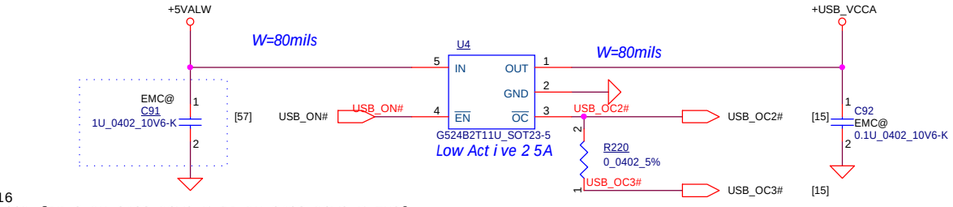
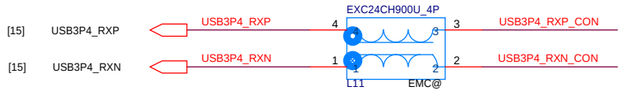
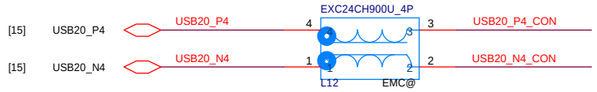
USB3 PORT4

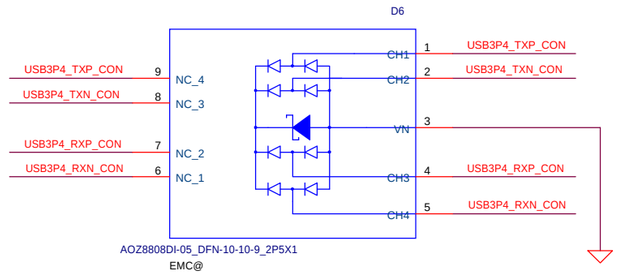
POWER SWITCH

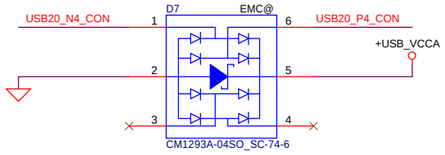


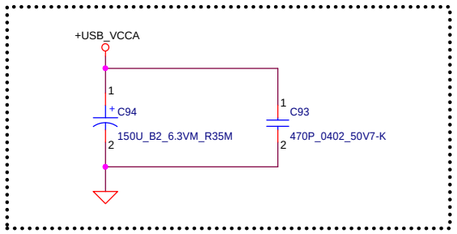
20160616
Change C91 for 0.1U_0402_10V6-K to 1U_0402_10V6-K EMC@

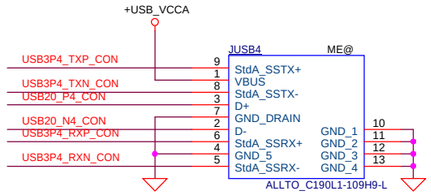




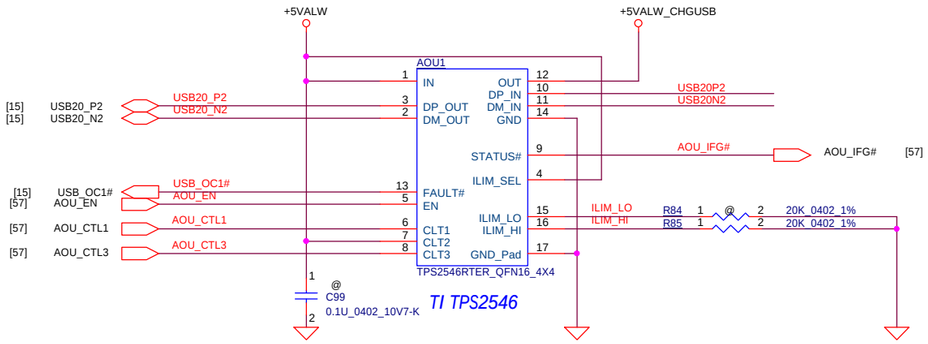




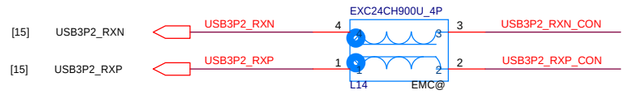


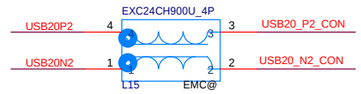


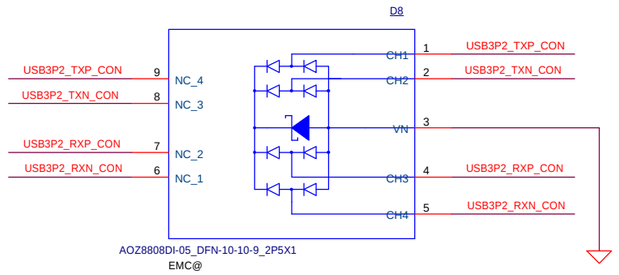
PORT2(AOU)

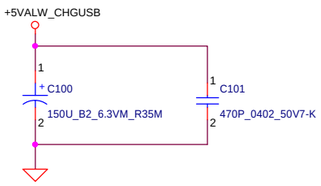


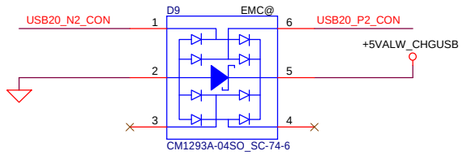
CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	**DCH**	OUT held low
1	1	1	1	**CDP**	Data Connected and Port Power Mgt. Function Active
1	1	1	0	**SDP2**	Data Connected
1	1	0	X	**SDP1**	Data Connected
0	1	0	X	**SDP1**	Data Connected
1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	**DCP_Auto**	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	**DCP_Auto**	Data Disconnected and Power Wake Function Active

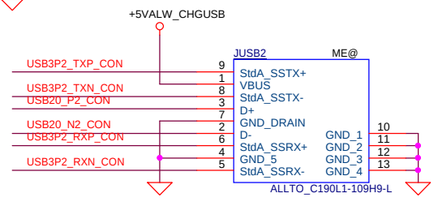












Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **USB3 PORT1/PORT2(AOU)**

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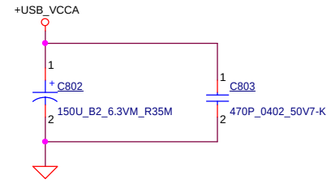
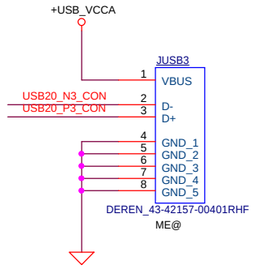
USB3 PORT3





Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title	USB PORT3		
Size: Custom	Document Number: KENOBI		Rev: 2.0
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+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 100m s

width : 40 mils

+3VALW
+3VALW_LAN
RL18 1 2 0_0805_5%
LP2301ALT1G_SOT23-3
CL7 QL2 CL8
0.1U_0402_10V7-K
CL2 4.7U_0603_6.3V6-K
CL3 4.7U_0603_6.3V6-K
CL4 0.1U_0402_10V7-K
CL5 0.1U_0402_10V7-K
Close to Pin11
Close to Pin32
Close to Pin11
Close to Pin32
[12] PCH_SLP_LAN#
RL5 1 @ 2 47K_0402_5%

+3VALW_LAN
+LAN_VDDREG
RL1 1 2 0_0603_5%
CL1 4.7U_0603_6.3V6-K
CL6 0.1U_0402_10V7-K

+3VALW_LAN
+3VS
RL2 10K_0402_5% @
QL1 2N7002KW_SOT323-3
LAN_CLKREQ#_R
CLKREQ_PCIE3_LAN# [10]
RL4 1 2 0_0402_5%

+3VALW_LAN
RL6 10K_0402_5%
[57] LAN_WAKE#
RL7 1 2 0_0402_5%
LAN_WAKE#_R

[15] PCIE_PRX_DTX_P10
[15] PCIE_PRX_DTX_N10
PCIE_PRX_DTX_P10 CL9 1 2 0.1U_0402_10V7-K PCIE_PRX_DTX_C_P10
PCIE_PRX_DTX_N10 CL10 1 2 0.1U_0402_10V7-K PCIE_PRX_DTX_C_N10

CL10 close to Pin18
CL9 close to Pin17

[12,28,42,48,49,57,58] PLT_RST#

+3VS
RL8 1K_0402_5%
ISOLATE#
RL9 15K_0402_5%

+3VALW_LAN
RL19 10K_0402_5%
LED1

TL2 RJ45_LINKUP#
TL3 LED1
TL4 RJ45_ACTIVITY#

[47] RJ45_LINKUP#
[47] RJ45_ACTIVITY#

UL1
+3VALW_LAN 11 AVDD33_1
+3VALW_LAN 32 AVDD33_2
PLT_RST# 19 PERSTB
ISOLATE# 20 ISOLATEB
LAN_WAKE#_R 21 LANWAKEB
+LAN_VDDREG 23 VDDREG
+LAN_REGOUT 24 REGOUT
RJ45_LINKUP# 25 LED2
LED1 26 LED1/GPO
RJ45_ACTIVITY# 27 LED0
LAN_XTALO 28 CKXTAL1
LAN_XTALI 29 CKXTAL2
33 GND
RTL8111GUS-CG_QFN32_4X4

AVDD10_1 3 +LAN_VDD10
AVDD10_2 8 +LAN_VDD10
AVDD10_3 30 +LAN_VDD10
DVDD10 22 +LAN_VDD10
MDIP0 1 MDI_0+ — MDI_0+ [47]
MDIN0 2 MDI_0- — MDI_0- [47]
MDIP1 4 MDI_1+ — MDI_1+ [47]
MDIN1 5 MDI_1- — MDI_1- [47]
MDIP2 6 MDI_2+ — MDI_2+ [47]
MDIN2 7 MDI_2- — MDI_2- [47]
MDIP3 9 MDI_3+ — MDI_3+ [47]
MDIN3 10 MDI_3- — MDI_3- [47]
HSIP 13 PCIE_PTX_C_DRX_P10 — PCIE_PTX_C_DRX_P10 [15]
HSIN 14 PCIE_PTX_C_DRX_N10 — PCIE_PTX_C_DRX_N10 [15]
CLKREQB 12 LAN_CLKREQ#_R
REFCLK_P 15 CLK_PCIE_LAN — CLK_PCIE_LAN [10]
REFCLK_N 16 CLK_PCIE_LAN# — CLK_PCIE_LAN# [10]
RSET 31 RSET
RL10 2.49K_0402_1%

LAN_XTALI
LAN_XTALO
YL1 25MHZ_10PF_7V25000014
OSC1 GND2 OSC2 GND1
CL11 12P_0402_50V8-J
CL12 12P_0402_50V8-J

+LAN_VDD10
+LAN_REGOUT
LL1 2.2UH_EP-22AM05B02_2A_20%
CL14 4.7U_0603_6.3V6-K
CL15 0.1U_0402_10V7-K
CL16 0.1U_0402_10V7-K
CL17 0.1U_0402_10V7-K
CL18 0.1U_0402_10V7-K
CL19 0.1U_0402_10V7-K
CL20 1U_0402_10V6-K @

Layout Note: LL1 must be within 200mil to Pin24, CL14,CL15 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

Close to Pin3, 8, 22, 30
LAYOUT NEED CHECK
Close to Pin22(Reserved)

Security Classification	LC Future Center Secret Data		
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Title: GBE LAN PHY

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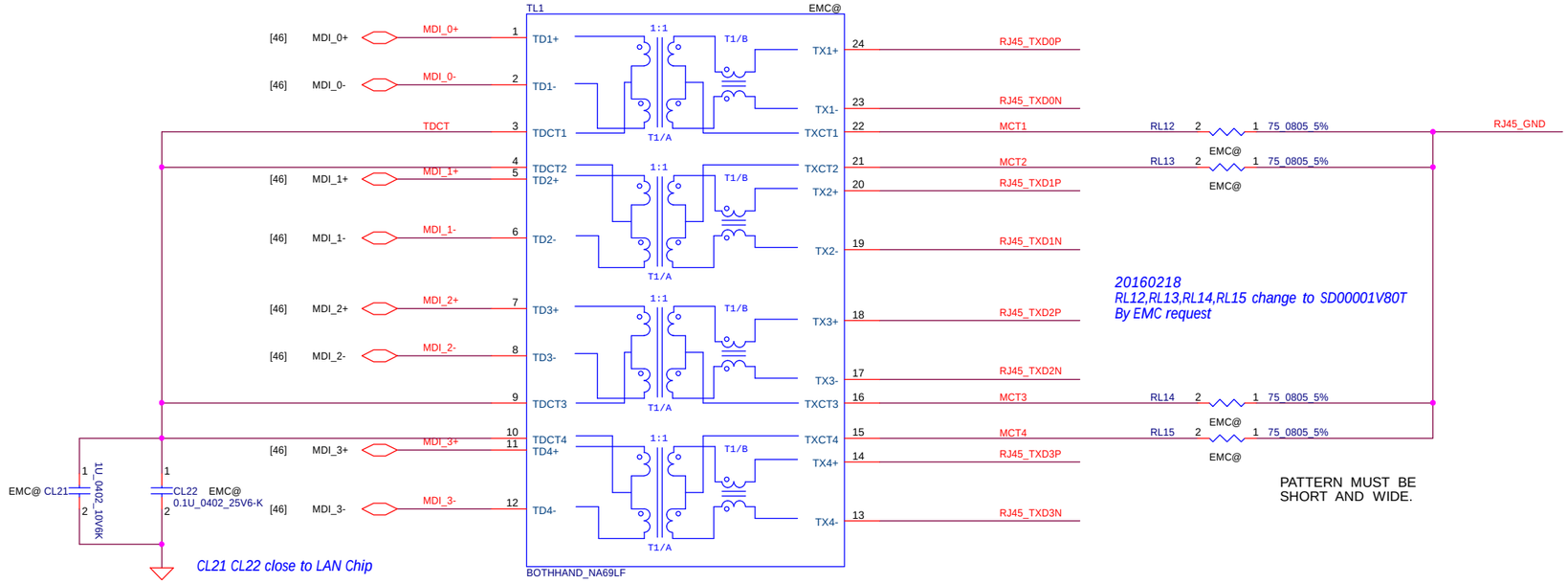
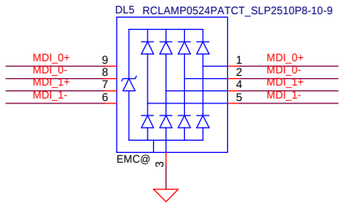
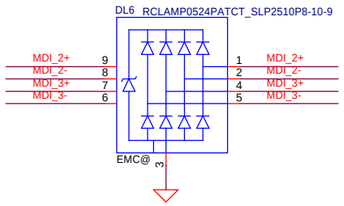
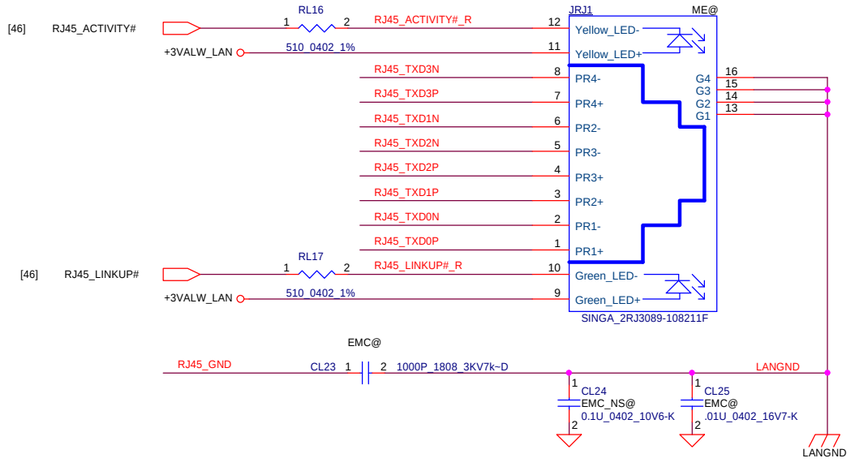






RJ-45 Conn.



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **RJ45 CONN**

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TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR

+3VS
+3VALW
+3V_WLAN
R86 1 @ 2 0_0805_5%
R87 1 2 0_0805_5%
@

+3VALW
R390 1 @ 2 10K_0402_5% EC_WLAN_WAKE#

+3VS
R312 1 2 BT_ON
10K_0402_5%
R313 1 2 RF_OFF#
10K_0402_5%

[15] USB20_P6 — USB20_P6 — L34 EMC_NS@ 1 2 — USB20_P6_CON
[15] USB20_N6 — USB20_N6 — 4 3 — USB20_N6_CON
EXC24CH900U_4P

USB20_P6 — R425 1 EMC@ 2 0_0402_5% — USB20_P6_CON
USB20_N6 — R426 1 EMC@ 2 0_0402_5% — USB20_N6_CON

For EMI choke co-lay

JWLBT1

1	GND1	3.3VAUX1	2
3	USB_D+	3.3VAUX2	4
5	USB_D-	LED1#	6
7	GND2	NC	8
9	NC	NC	10
11	NC	NC	12
13	NC	NC	14
15	NC	LED2#	16
17	MLDIR_SENSE	GND16	18
19	DP_ML3N	DP_AUXN	20
21	DP_ML3P	DP_AUXP	22
23	GND3	GND13	24
25	DP_ML2N	DP_ML1N	26
27	DP_ML2P	DP_ML1P	28
29	GND4	GND14	30
31	DP_HPD	DP_ML0N	32
33	GND5	DP_ML0P	34
35	PETP0	GND15	36
37	PETN0	VENDOR_DEFINED_1	38
39	GND6	VENDOR_DEFINED_2	40
41	PERP0	VENDOR_DEFINED_3	42
43	PERN0	COEX3	44
45	GND7	COEX2	46
47	REFCLKP0	COEX1	48
49	REFCLKN0	SUSCLK	50
51	GND8	PERST0#	52
53	CLKREQ0#	W_DISABLE2#	54
55	PEWAKE0#	W_DISABLE1#	56
57	GND9	I2C_DATA	58
59	PETP1	I2C_CLK	60
61	PETN1	ALERT#	62
63	GND10	RESERVED4	64
65	PERP1	PERST1#	66
67	PERN1	CLKREQ1#	68
69	GND11	PEWAKE1#	70
71	REFCLKP1	3.3VAUX4	72
73	REFCLKN1	3.3VAUX5	74
75	GND12		
76	PEG1	PEG2	77

ARGOS_NASA0-S6701-TS40
ME@

KEY A

+3V_WLAN
R92 1 2 100K_0402_5%

[15] PCIE_PTX_C_DRX_P9 — PCIE_PTX_C_DRX_P9
[15] PCIE_PTX_C_DRX_N9 — PCIE_PTX_C_DRX_N9
[15] PCIE_PRX_DTX_P9 — PCIE_PRX_DTX_P9
[15] PCIE_PRX_DTX_N9 — PCIE_PRX_DTX_N9
[10] CLK_PCIE_WLAN — CLK_PCIE_WLAN
[10] CLK_PCIE_WLAN# — CLK_PCIE_WLAN#
[10] CLKREQ_PCIE2_WLAN# — CLKREQ_PCIE2_WLAN#
EC_WLAN_WAKE#

CL_RST_WLAN# — CL_RST_WLAN# [11]
CL_DATA_WLAN — CL_DATA_WLAN [11]
CL_CLK_WLAN — CL_CLK_WLAN [11]

SUSCLK_32K — SUSCLK_32K [10]
PLT_RST# — PLT_RST# [12,28,42,46,49,57,58]
BT_ON_R
RF_OFF# — RF_OFF# [14]

EC_TX_R — R90 1 2 100_0402_1% — EC_RX — EC_RX [57]
R91 1 2 100_0402_1% — EC_TX — EC_TX [57]

+3VS
R420 49.9K_0402_1% @ — R421 49.9K_0402_1% @

R330 1 2 0_0402_5% — UART2_RX [14]
R331 1 2 0_0402_5% — UART2_TX [14]

BT_ON_R — R93 1 2 1K_0402_5% — BT_ON [14]

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: WWAN/WLAN NGFF CONN.

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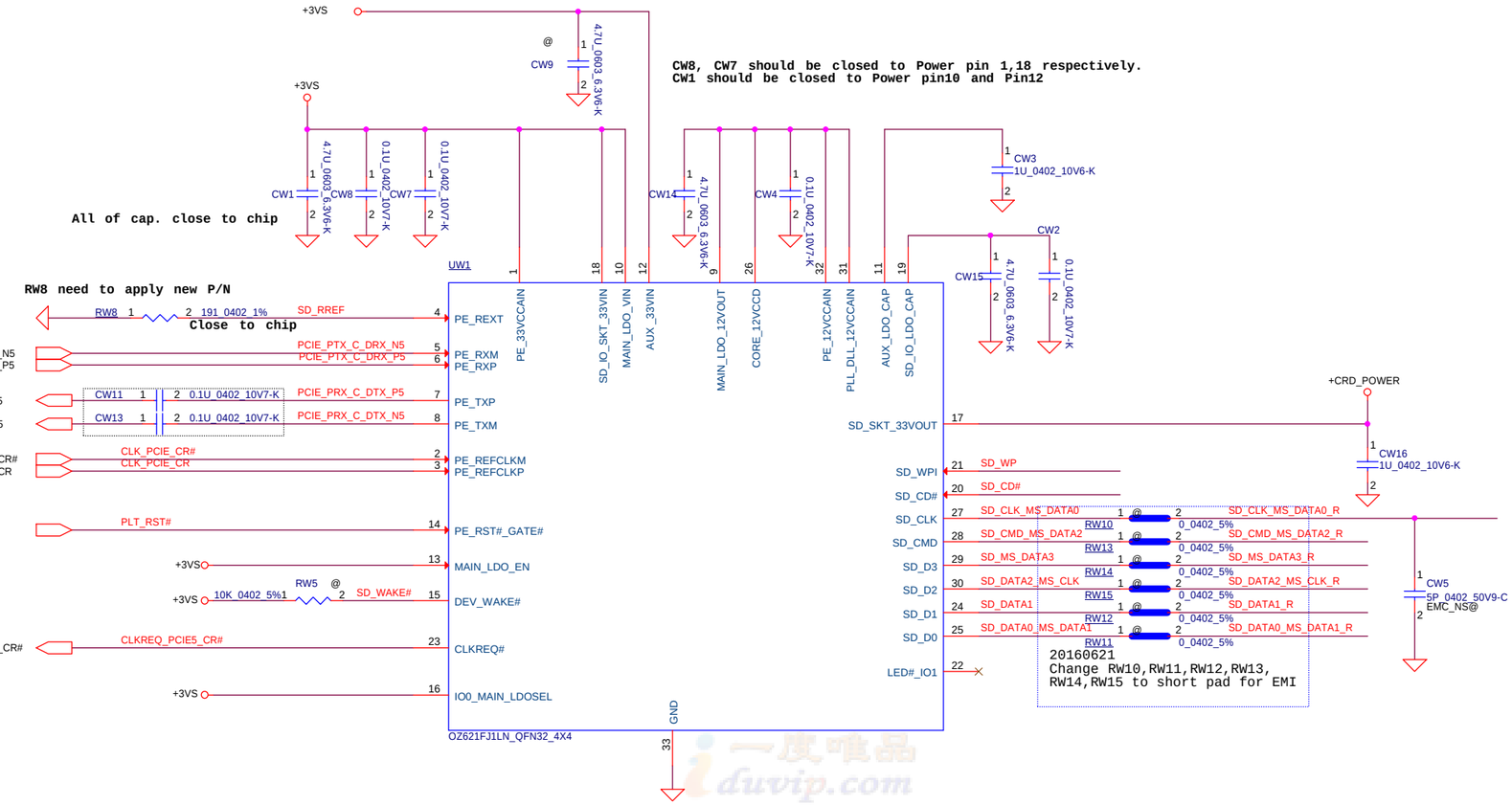

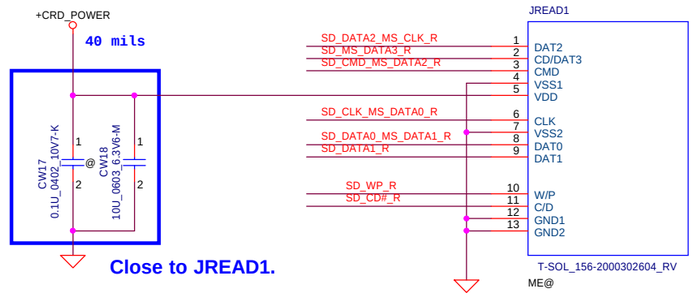

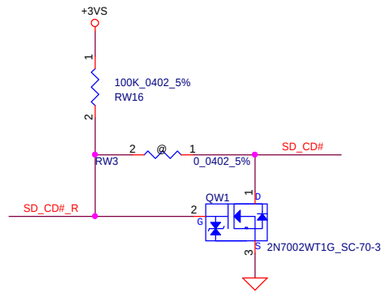

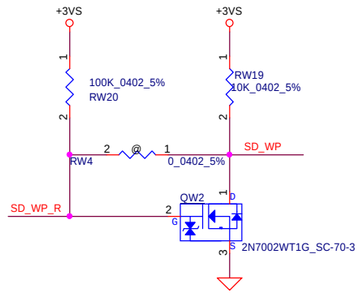

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title	Card Reader		
Size: Custom	Document Number: KENOBI		Rev: 2.0
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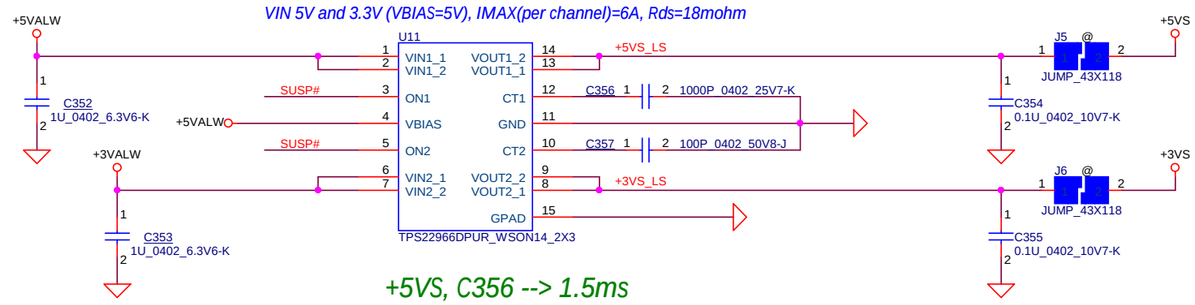
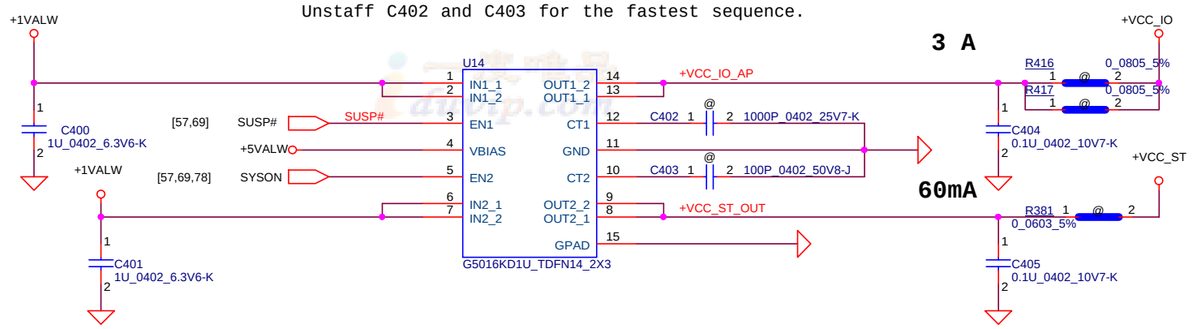
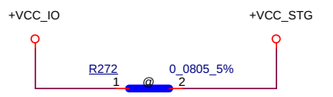
Load Switch
+5VALW To +5VS
+3VALW To +3VS



+1VALW to +VCC_IO_AP & +VCC_ST

Unstaff C402 and C403 for the fastest sequence.





Slew Rate=10uS<TR<65us

Security Classification	LC Future Center Secret Data		
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Title	DC V TO VS/ V-PCH/VM		
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+5VS
RA1 1 @ 2 0_0805_5%
CA1 4.7U_0603_10V6-K
CA2 4.7U_0603_10V6-K
CA3 0.1U_0402_10V7-K
CA4 0.1U_0402_10V7-K
+5VS_CLASSD
Close to Pin13,16

+1.8V_LDO
LDO 1V8
CA6 4.7U_0603_10V6-K
X5R CAP

+1.65V_LDO
VREF 1V65
CA7 0.1U_0402_10V7-K
CA8 1U_0402_6.3VA-K
X5R CAP

+3V_LDO
LDO 3V3
CA9 0.1U_0402_10V7-K
CA11 2.2U_0402_6.3V6-M

+3VS
CA10 0.1U_0402_10V7-K
CA10 close Pin7

+3VS_VDDO
RA2 2 1 0_0402_5%
@
CA12 0.1U_0402_10V7-K
CA12 close Pin2

+3V_AVDD_HP
+3VL
RA4 1 @ 2 0_0805_5%
CA13 1U_0402_6.3VA-K
CA13 close Pin24

+3VS_DVDD
+3VS
RA8 1 @ 2 0_0805_5%
X5R CAP, Please Close Pin18
CA16 1U_0402_6.3VA-K

UA1
CX11852
CX11852-11Z_QFN40_5X5

[9] PCH_HDA_RST# → PCH_HDA_RST# → RESET#
[9] PCH_HDA_BCLK → PCH_HDA_BCLK → BIT_CLK
[9] PCH_HDA_SYNC → PCH_HDA_SYNC → SYNC
[9] PCH_HDA_SDIN0 → RA3 33_0402_5% → PCH_HDA_SDIN0_R → SDATA_IN
[9] PCH_HDA_SDOUT → PCH_HDA_SDOUT → SDATA_OUT
[52] PC_BEEP → PC_BEEP → PC_BEEP
SPKR_MUTE# → SPKR_MUTE#
[52] JSENSE → JSENSE → JSENSE
GPIO1/PORTC_R_MIC
[37] DMIC_CLK → DMIC_CLK → RA7 33_0402_5% → MIC_CLK_R → MUSIC_REQ/GPIO0/PORTC_L_MIC
[37] DMIC_DATA → DMIC_DATA → DMIC_CLK/MUSIC_REQ/GPIO0
DMIC_DAT/GPIO1
+5VS_CLASSD → CA14 0.1U_0402_10V7-K → CLASSD_REF → CLASS-D_REF
W= 80mils
LPWR_5.0
RPWR_5.0
CA15 1U_0402_6.3V6-K → FLY_P / FLY_N
FLY_P
FLY_N
+AVEE → AVEE
HP indicate
CA17 2.2U_0402_6.3V6-M
GND
Should be connect to GNDA

FILT_1.8V, VDD_IO, VDDO_3.3, DVDD_3.3 ← +1.8V_LDO, +3VS_VDDIO, +3VS_VDDO, +3VS_DVDD
AVDD_3.3, VREF_1.65V, AVDD_5V ← +3V_LDO, +1.65V_LDO, +5VS_AVDD
LEFT+ SPK_L+ → SPK_L2+ [52]
LEFT- SPK_L- → SPK_L1- [52]
RIGHT+ SPK_R+ → SPK_R2+ [52]
RIGHT- SPK_R- → SPK_R1- [52]
MICBIASC, MICBIASB ← +MICBIASB
PORTB_R_LINE PORTB_R → PORTB_R [52]
PORTB_L_LINE PORTB_L → PORTB_L [52]
PORTD_A_MIC EXT_MIC_A → EXT_MIC_A [52]
PORTD_B_MIC EXT_MIC_B → EXT_MIC_B [52]
HGNDA → HGNDA [52,53]
HGNDB → HGNDB [52,53]
AVDD_HP ← +3V_AVDD_HP
PORTA_R HP_OUTR → HP_OUTR [52]
PORTA_L HP_OUTL → HP_OUTL [52]

20160121
Mount CA32 by EMC suggestion
CA32 150P_0402_50V8-J EMC@

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA

AGND
DGND
38 31 1 11 21

W= 300mils
EMC_NS@ CA34 0.1U_0402_10V7-K
EMC_NS@ CA33 0.1U_0402_10V7-K
EMC_NS@ CA19 0.1U_0402_10V7-K
GND
GNDA

+5VS_AVDD
RA9 1 @ 2 0_0805_5% +5VS
CA18 0.1U_0402_10V7-K
Please Close Pin28

+3VALW
0_0402_5% RA12 +3VS_VDDIO
@
CA20 0.1U_0402_10V7-K
CA20 close Pin7

+3VS_VDDO
RA10 47K_0402_5%
[57] EC_MUTE# → EC_MUTE# → DA1 → SPKR_MUTE#
RB751V-40_SOD323-2
SCS00008K00

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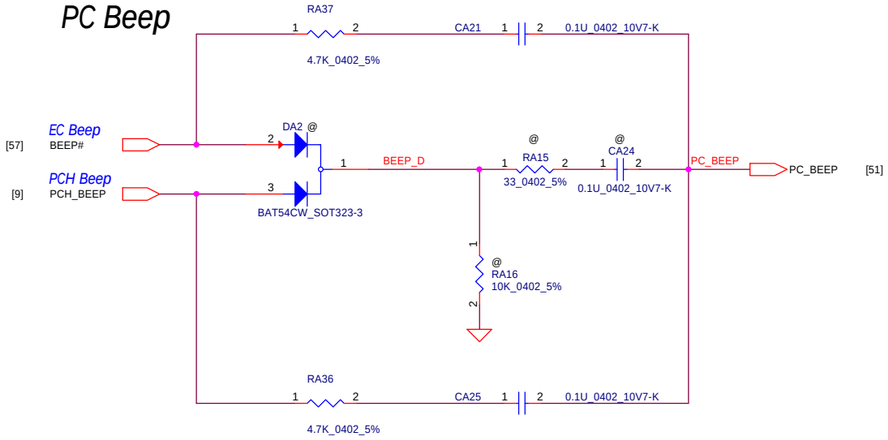
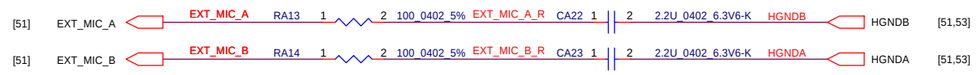
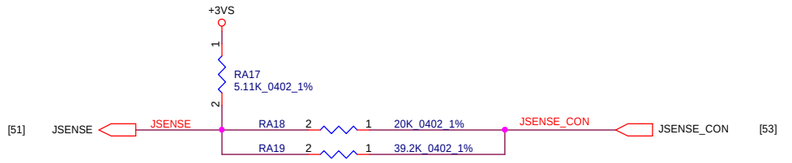
PC Beep



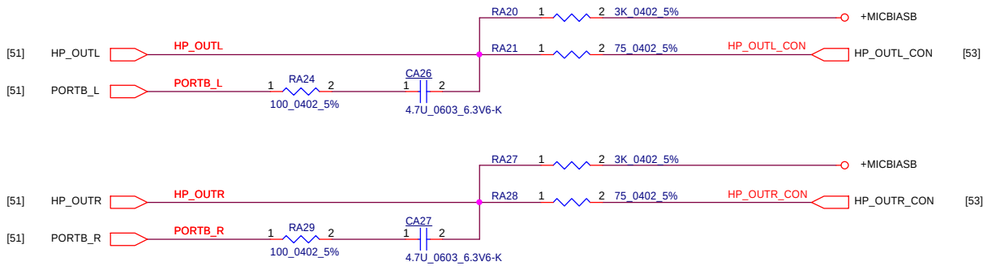
EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



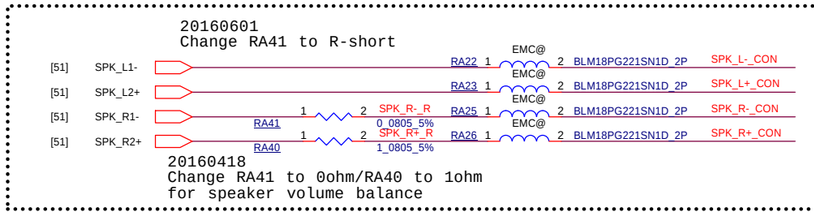


HeadPhone/LINE OUT

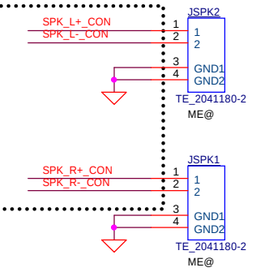


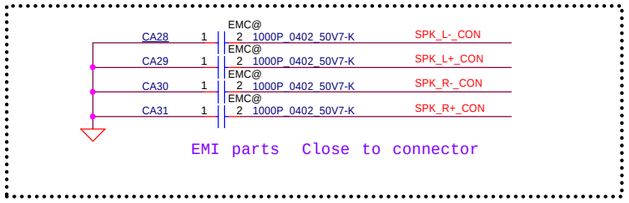
Speaker OUT

Need Lenght Match



SPK CONN.





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Title	HP/MIC JACK/Speaker		
Size	Document Number		Rev
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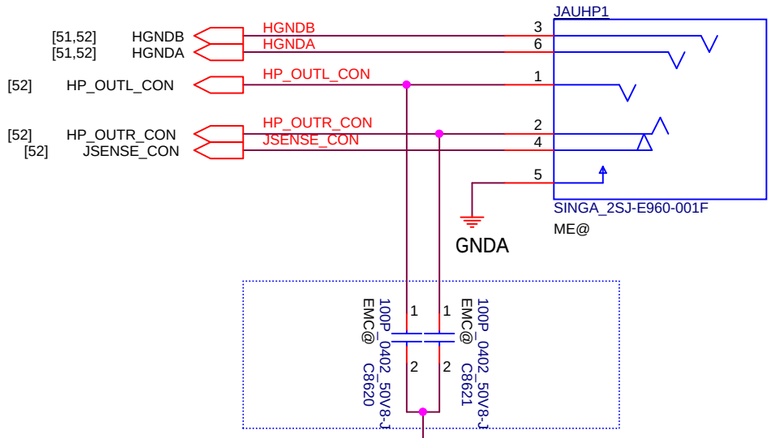
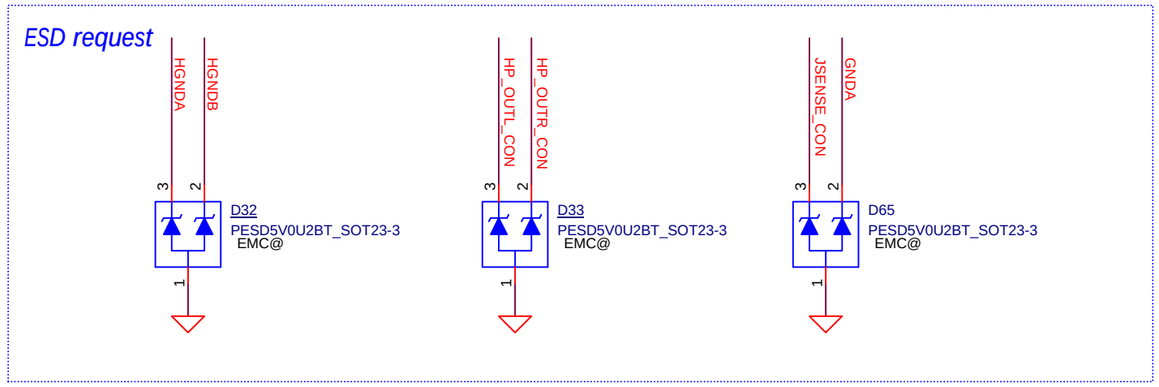
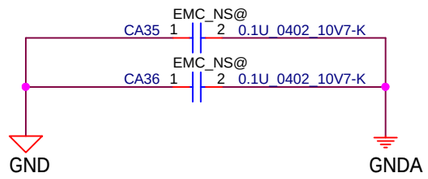


Vendor suggestion. Reserve for EMI.
Close to JAUHP.





Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: **AUDIO JACK**

Size	Document Number	Rev
B	KENOBI	2.0

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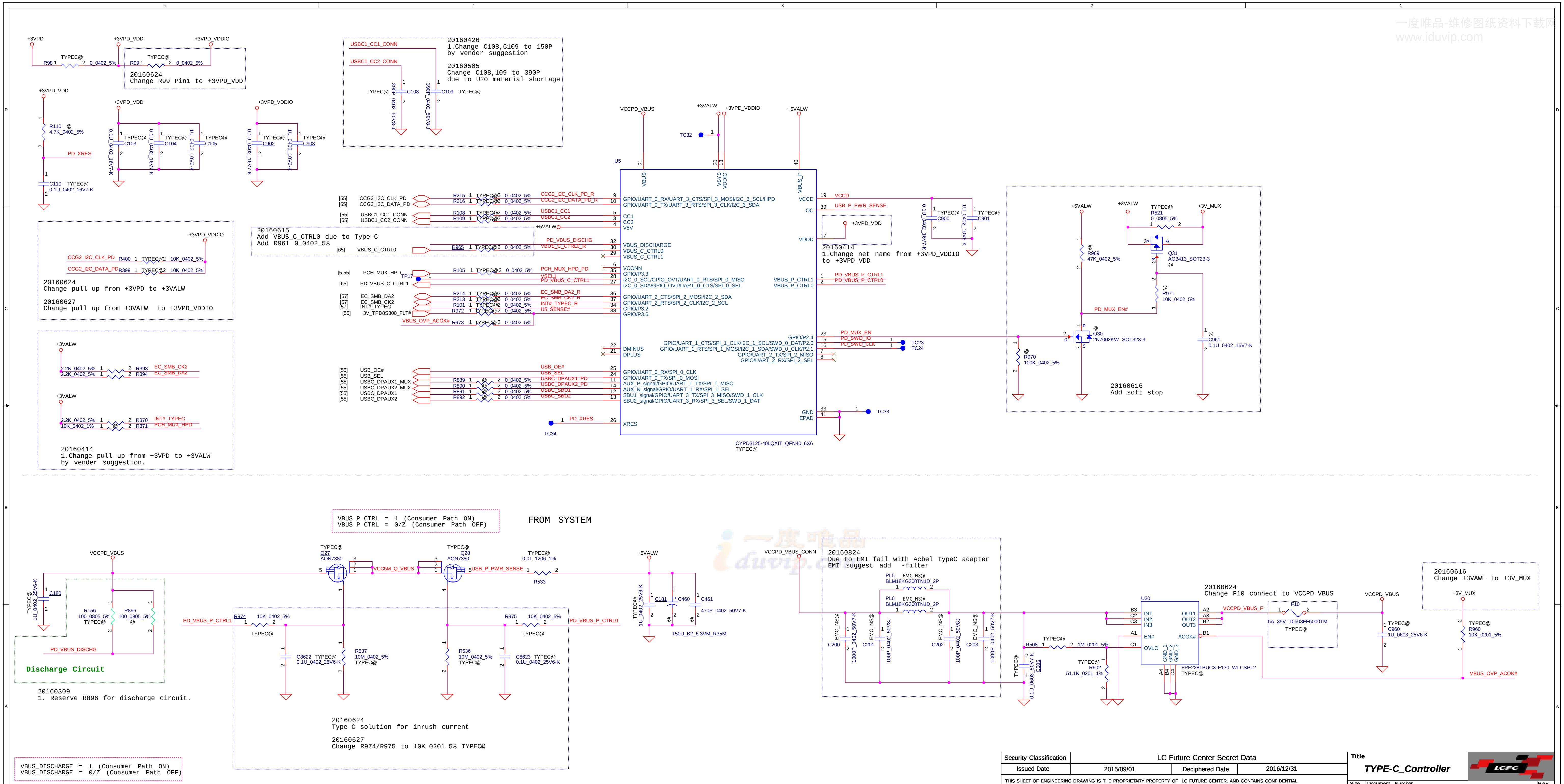

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Title: TYPE-C_Controller

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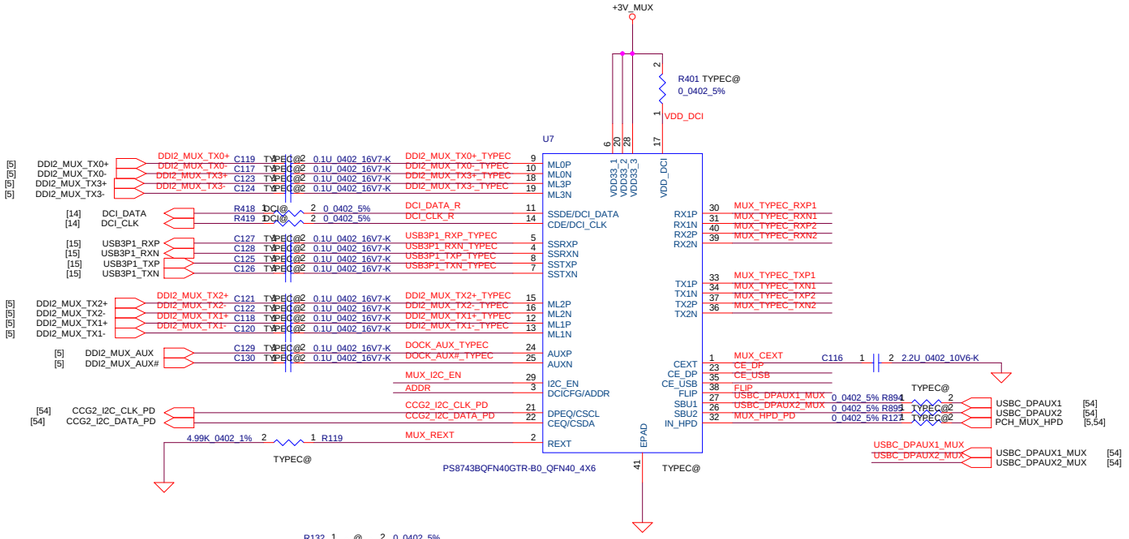
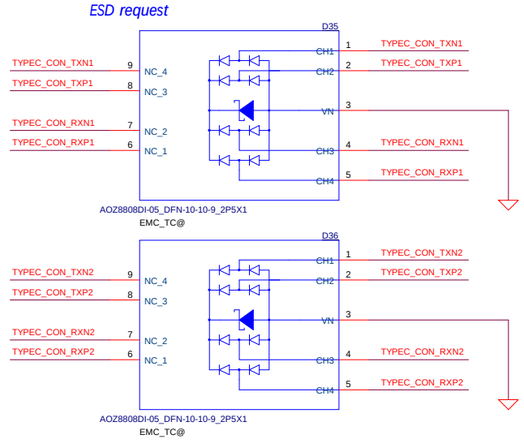
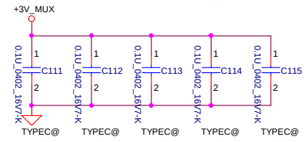
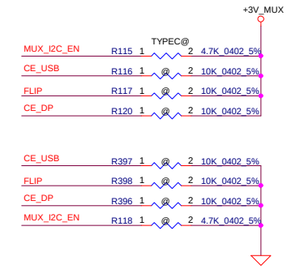
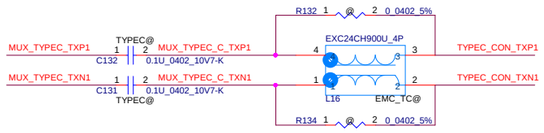


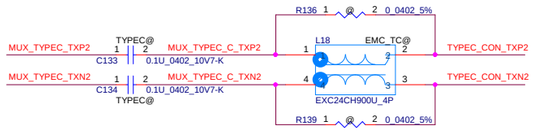
ESD request

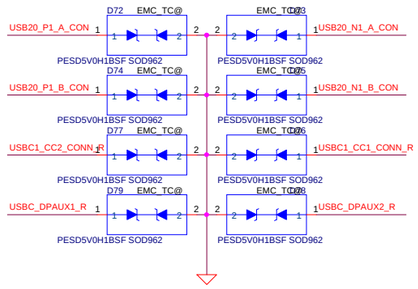


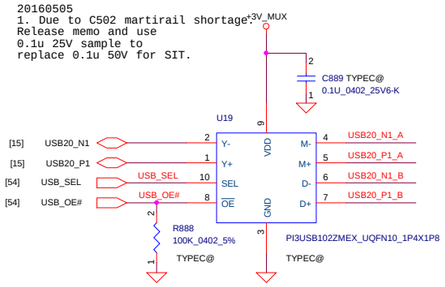


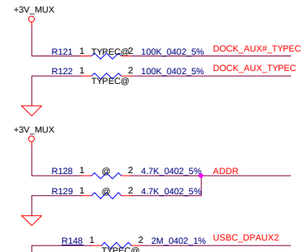




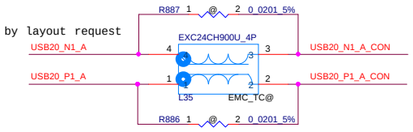


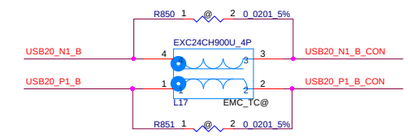


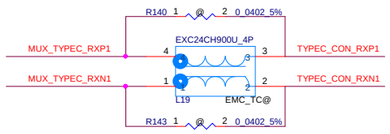


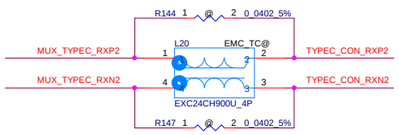


20160414
1. Swap L35 by layout request

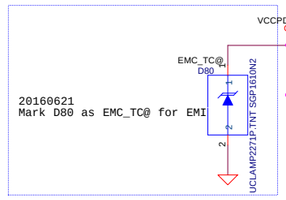






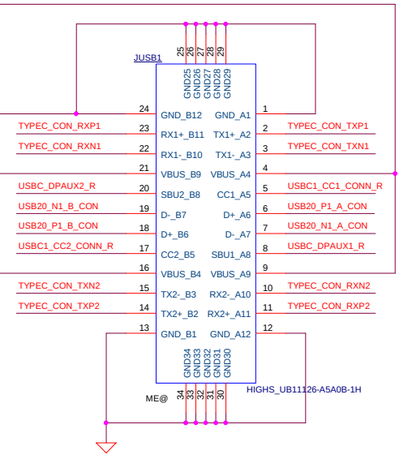


20160621
Mark D80 as EMC_TC@ for EMI



20160414
1. Delete D30,D37 and add D72~D80
for layout placement
2. Add U20 (OVP protection circuit)

20160419
1. Co-lay F11



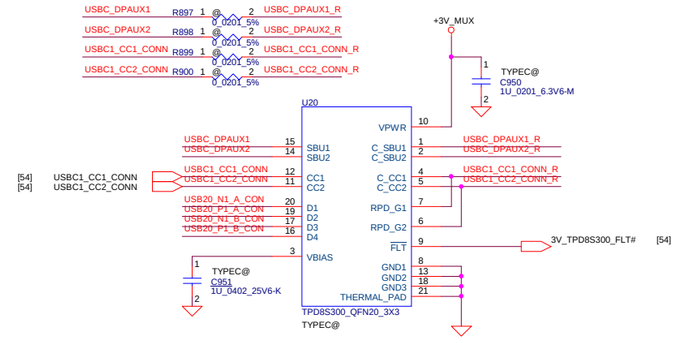
20160330
1.Add CC/SBU
protection solution

20160505
1. Unstaff U20 and staff
R897,R898,R899,R900
due to U20 martirail shortage.

201616
FLT pin into U5 pin30

20160624
1. Change VPER to +3V_MUX

20160719
1. U20 martirail prepare ready.



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Title			
TYPE-C_MUX			
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Title
DOCKING/ DCIN CONN

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20160127
1. Add TEMBER_DETECT# circuit
2. Change Resistor value

20160419
Change RE2 to 18K
for SIT board ID

Vcc	3.3V +/- 5%				
RE1	100K +/- 1%				
Board ID	RE2	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

All capacitors close to EC

Close to EC

minimum trace width 12 mil

IT8586E/AX
LQFP-128L

Please don't place any PU Resistor on GPG[7:2]
(Reserve hardware strapping)

Un-stuff if not necessary.

20160307
Stuff CE11 for WRST singal

1. Version CX : Don't Support Mirror Code
   Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
   "H" --> Enable
   "L" --> Disable (Default)
*

IT8586E-AX_LQFP128_14X14
SA00005W940

IT8586E/FX LQFP

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Title: **EC**

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A2	**KENOBI**	2.0

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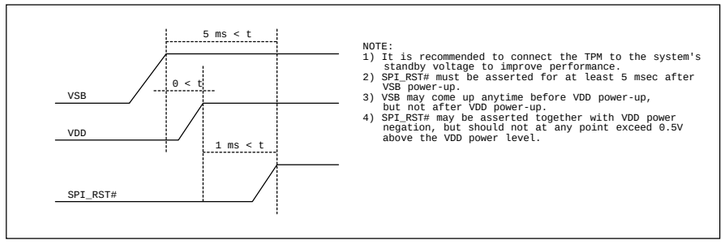
TPM IC

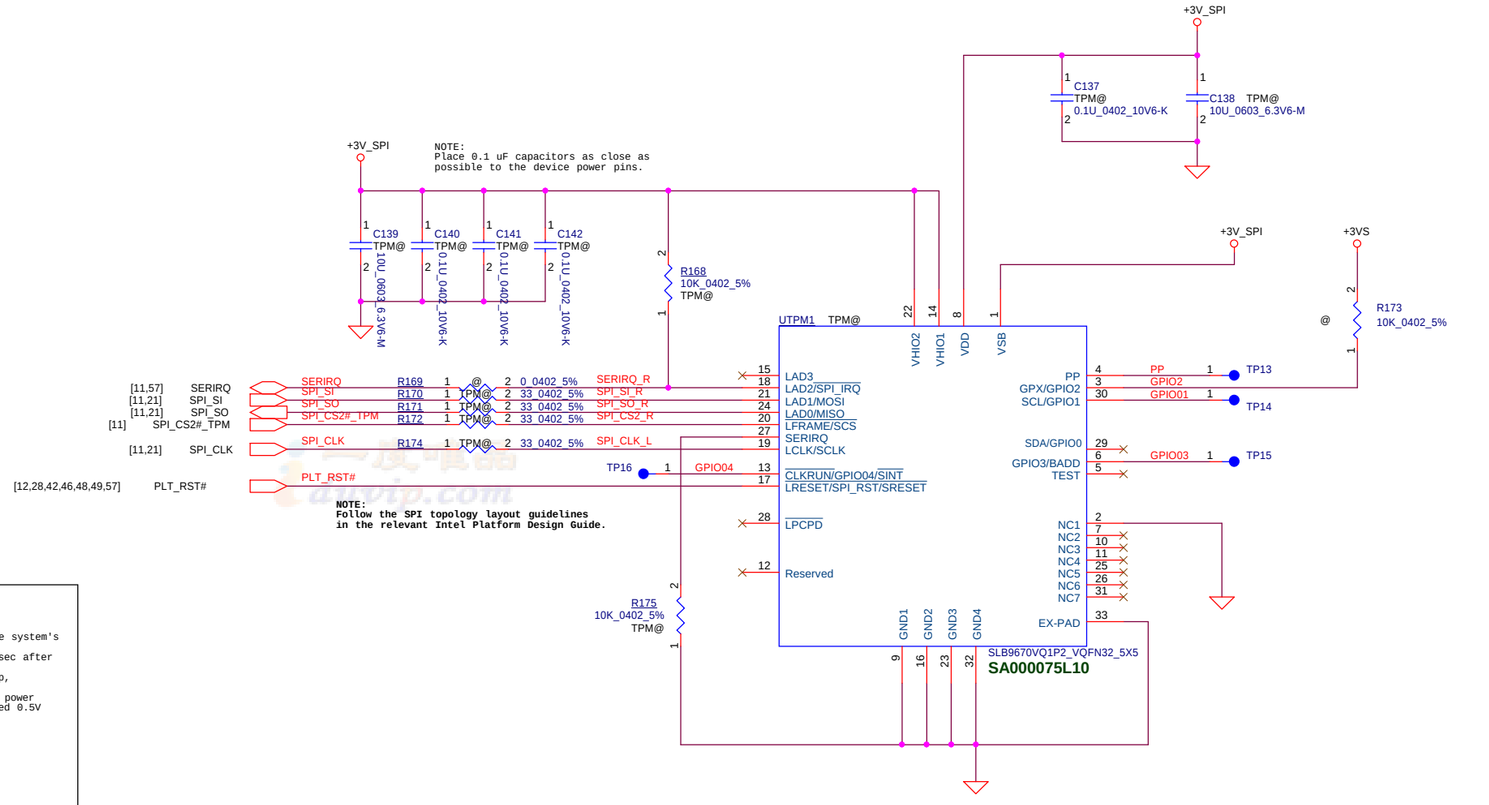
TABLE

Pin No	TCG PTP Spec (x38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table

NOTE:
Check timing sequence in SDV phase.





Security Classification	LC Future Center Secret Data		
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Title: TPM

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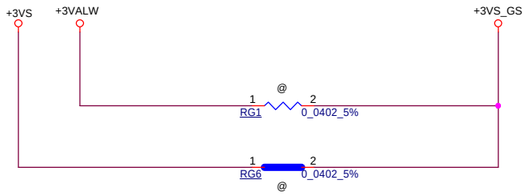


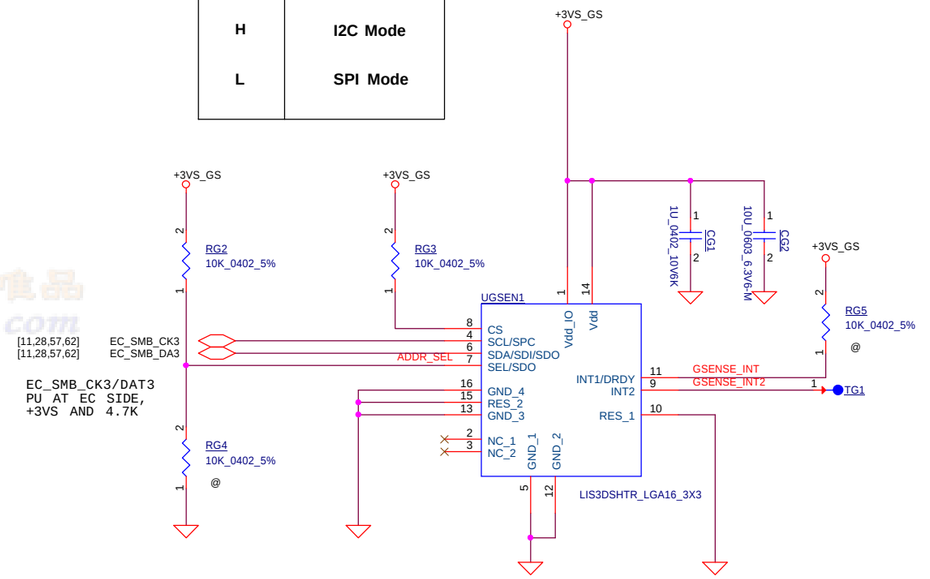
APS G-Sensor

TABLE

P/N	ADDR_SEL	Address
LIS3DSHTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title	G SENSOR		
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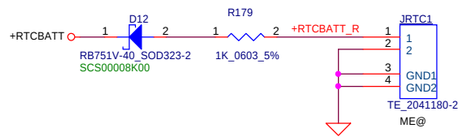
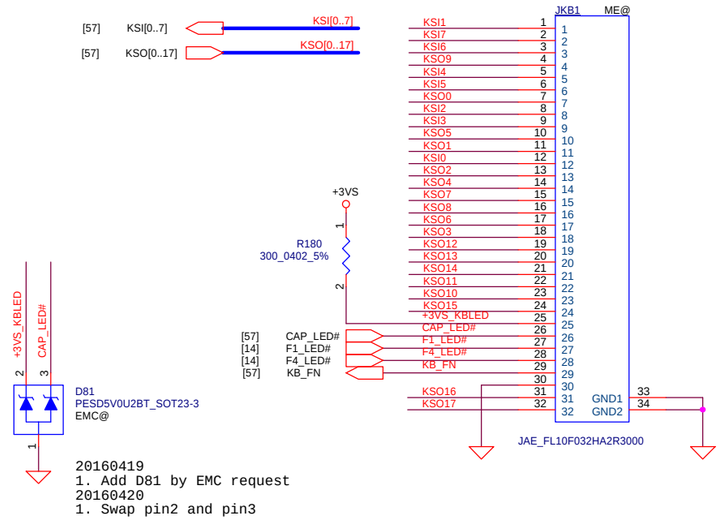
RTC CONN.



KB CONN



20160419
1. Add D81 by EMC request
20160420
1. Swap pin2 and pin3

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KB/RTC/TOUCH PAN CONN.**

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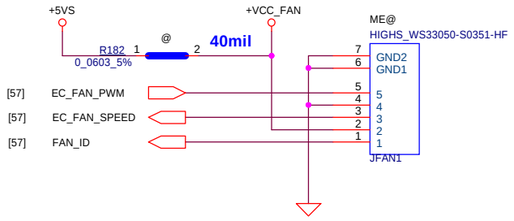
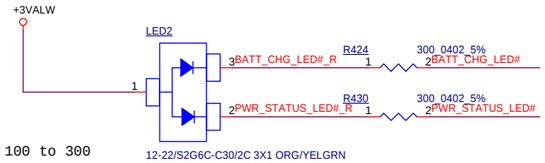
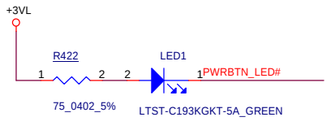
FAN CONN.

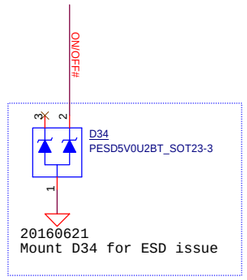


PWR BTN

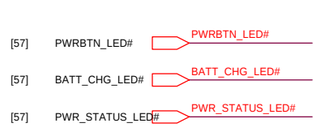


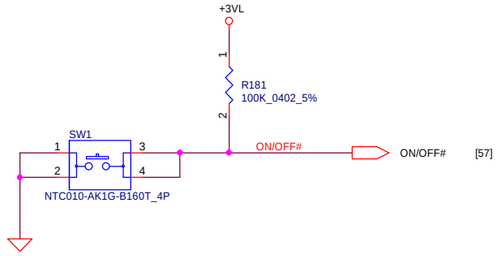
20160424
1. Change R430/R423 from 100 to 300 ohm for LED brightness
2. Change R422 from 100 to 75 ohm for LED brightness



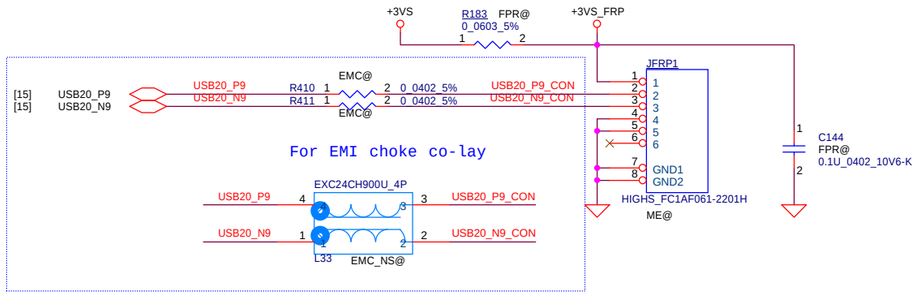


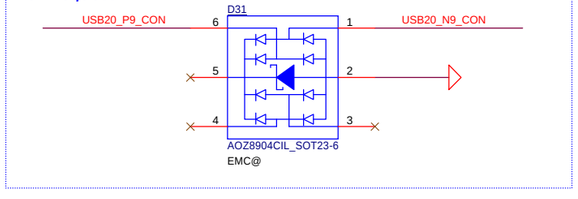
20160621
Mount D34 for ESD issue



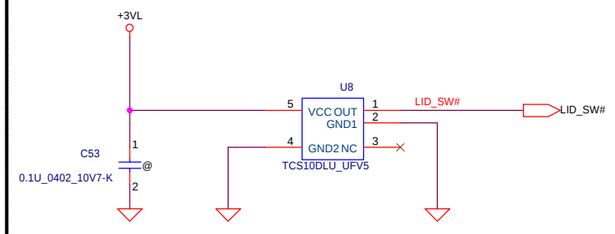


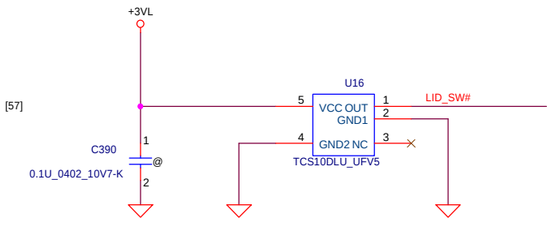
FingerPrint CONN.





Lid Switch





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Title	PBTN/LID/FP/FAN CONN.		
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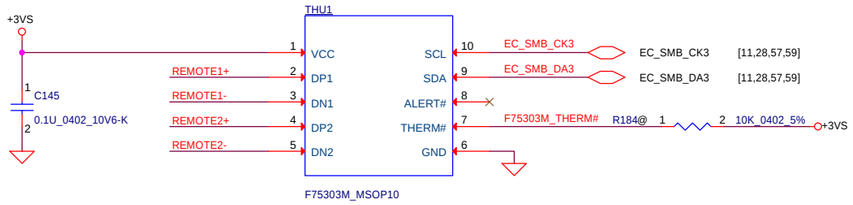
Thermal Sensor
placed near by VRAM

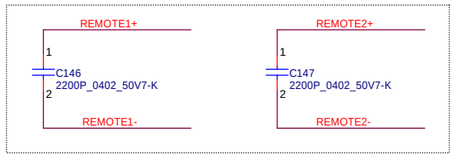


Address 1001_101xb

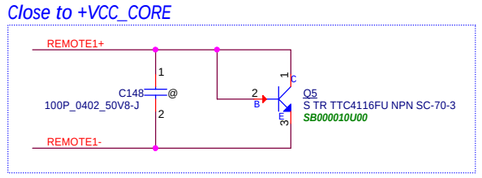
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

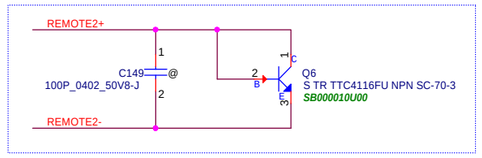
Close to U1

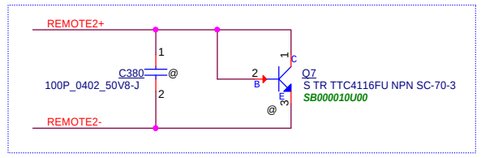


Close to +VCC_CORE



Close JDIMM1&JDIMM2





Security Classification	LC Future Center Secret Data		
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Title: ***Thermal Sensor***

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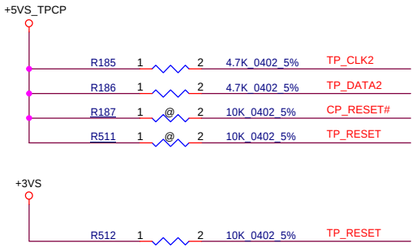
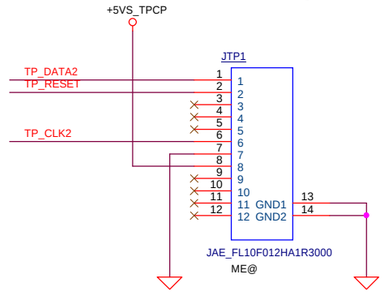
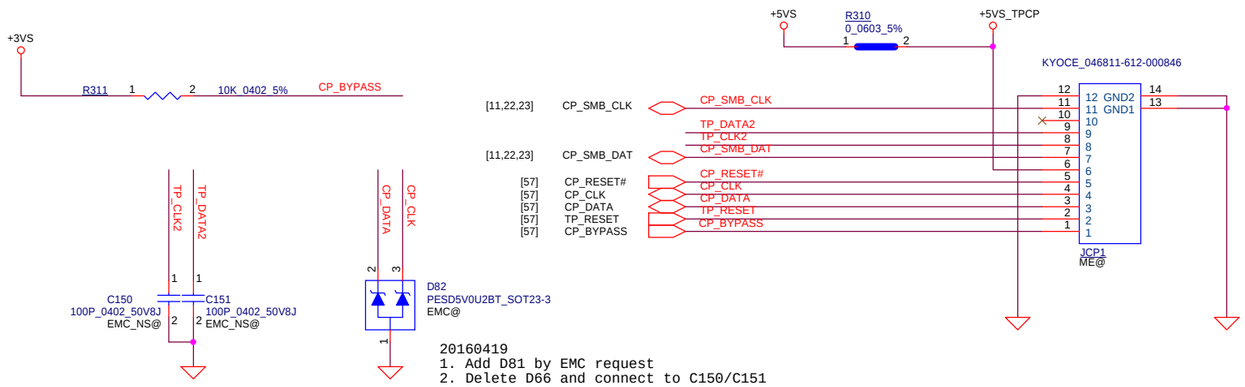
Track point





Click Pad



20160419
1. Add D81 by EMC request
2. Delete D66 and connect to C150/C151

20160414
1. Change JCP1 foot print

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: CP/TPOINTCONN.

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Screw Hole

H1 PAD_CB6P0D3P3
H2 PAD_CB6P0D3P3
H3 PAD_CB6P0D3P3
H4 PAD_CB6P0D3P3
H5 PAD_C5P0D2P5
H6 PAD_C6P0D2P5
H7 PAD_CT5P0B6P0D2P5
H8 PAD_C6P0D2P5
H9 PAD_C5P5D2P5X3P0
H10 PAD_C6P0D2P5X3P0

H11 PAD_CT5P0B6P0D2P5X3P0
H12 PAD_C6P0D2P5X3P0
H13 PAD_C6P0D2P5
H14 PAD_CT8P0B6P0D2P5
H15 PAD_CT8P0B5P0D2P5

20160419
Change H9/H10/H11/H12 footprint

H16 PAD_O3P0X2P5D3P0X2P5N

H17 PAD_C6P0D3P3
H18 PAD_CT6P0D3P2
H19 PAD_CT6P0D3P2

H20 PAD_CT6P0D3P2
H21 PAD_C6P0D2P5
H22 PAD_CT5P0B6P0D2P5
H23 PAD_SHAPET7P0X10P0CB6P0D2P5
H24 PAD_SHAPET7P0X10P0CB6P0D2P5

Center Zero

H25 H_2P5N

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **P64-PLM/SCREW HOLE**

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RTC Battery

40V PROPECTION

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Title	DCIN / VIN Detector		
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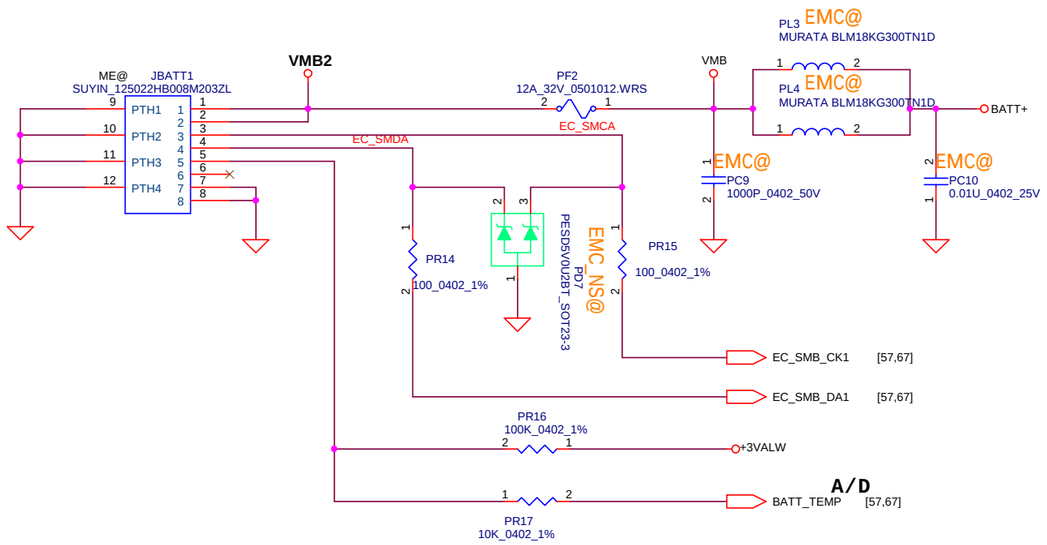
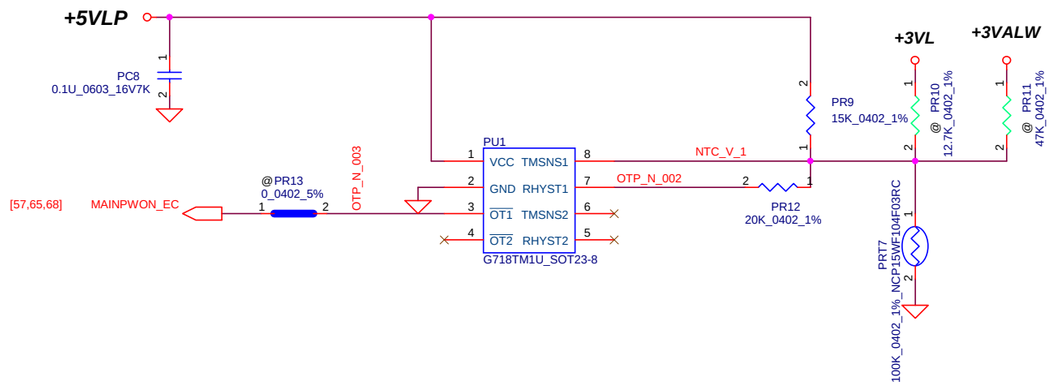


PRT7 under CPU bottom side for CPU thermal protection.
This is for thermal team request.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	***BATTERY CONN/OTP***		
Size: Custom	Document Number: ***KENOBI***		Rev: 2.0
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VSYSTEM2
EMC@
PL102
1UH_PCMB053T-1R0MS_7A_20%
PC102 10U_0805_25V6K
PC103 10U_0805_25V6K
PC136 10U_0805_25V6K
PC137 10U_0805_25V6K
PC138 33U_D2_25VM_R40M
VSYSTEM3
PR101 0.01_1206_1%
@PC108 0.1U_0402_25V7K
PC115 0.1U_0402_25V7K
@PR108 0_0402_5%
@PR111 0_0402_5%
@PR136
PC130 0.1U_0402_25V7K
PC105 1000P_0402_50V7-K
PC119 1U_0603_25V7-K
VBUS
PC104 0.01U_0402_50V7-K
PQ114 AON7380
PQ103 AON7380
PQ105 AON7380
PR102 56_0402_5%
PC117 330P_0402_50V7-K
PL101
2.2UH_PCMB063T-2R2MS_8A_20%
PC106 0.047U_0603_25V
PR106 2.2_0603_5%
PC107 0.047U_0603_25V
PR104 2.2_0603_5%
PR103 56_0402_5%
PC118 330P_0402_50V7-K
PQ104 AON7380
PQ106 AON7380
PC109 10U_0805_25V6K
PC110 10U_0805_25V6K
PC111 10U_0805_25V6K
PC112 10U_0805_25V6K
PC113 10U_0805_25V6K
PC114 10U_0805_25V6K
PC116 220P_0402_25V7-K
PC135 0.1U_0402_25V6-K
B+
PQ107 AON7409
PR110 0.01_1206_1%
PC120 1U_0603_25V7-K
PC121 0.1U_0402_25V7K
PC131 0.1U_0402_25V7K
PC132 0.1U_0402_25V7K
PC122 1U_0603_25V7-K
BATT+
PR112 10_0603_5%
PR114 10_0603_5%
BQ25700_VDD
PR113 10_0402_1%
VDDA
PR117 255K_0402_1%
PC123 1U_0603_25V7-K
PR116 220K_0402_1%
PU101
BQ25700RSNR_QFN32_4X4
BTST1 SW1 LODRV1 HIDRV1 VBUS ACN ACP VDDA ILIM_HIZ COMP1 PROCHOT# SCL SDA CHRG_OK ENZ_OTG CMPOUT CMPIN
BTST2 SW2 LODRV2 HIDRV2 VSYS BATDRV# SRP SRN REGN COMP2 CELL_BATPRES IADPT IBAT PSYS PGND PAD
LX1_CHG DL1_CHG DH1_CHG
LX2_CHG DL2_CHG DH2_CHG
BATDRV#
PR119 40.2K_0402_1%
PC125 1800P_0402_50V7-K
PC133 100P_0402_50V8-J
PC124 2.2U_0603_10V7-K
PC126 680P_0402_50V7-K
PR120 20K_0402_1%
PC134 15P_0402_50V8-J
[6,57,70] VR_HOT#
[57,66] EC_SMB_CK1
[57,66] EC_SMB_DA1
[57] ACPRN
[57] OTG
@PR121 0_0402_5%
@PR122 0_0402_5%
@PR123 0_0402_5%
@PR125 0_0402_5%
PR126 10K_0402_1%
PR135 100K_0402_5%
@PR127 0_0402_5%
@PR129 0_0402_5%
@PR130 0_0402_5%
ADP_I [57]
PSYS [70]
PC129 100P_0402_50V8-J
PC127 100P_0402_50V8-J
PC128 100P_0402_50V8-J
PR131 100K_0402_1% [57,66]
VDDA
PR118 82K_0402_1%
PR124 100K_0402_1%
BATT_TEMP
PQ111 2N7002WT1G_SC-70-3
PR128 1M_0402_5%
[57] ACOFF
@PR132 0_0402_5%
PQ112 2N7002WT1G_SC-70-3
PR133 10K_0402_1%
[65] DCIN_ATTACHED1
@PR134 0_0402_5%
PQ113 2N7002WT1G_SC-70-3

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Title: CHARGER

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+3VALW
FSW=750 KHz
TDC:8A
OCP:11A

B+ @ PJ201 JUMP_43X79

EMC@ EMC@ RF_NS@

PC232 2200P_0402_25V7-K
PC201 0.1U_0402_25V6-K
PC230 47P_0402_50V8-J
PC202 10U_0805_25V6-K
PR201 1M_0402_5%

PU201 SYX198BQNC_QFN10_3X3

EN2	7	2	PG
IN	8	6	BS
GND	9	10	LX
EN1	1	4	OUT
FB	3	5	LDO

+3V_VIN, +3V_PWRGD, +3VBS, +3VLX, +3VALW_OUT, +3VALW_FB, 3V5V_ON

@ PR202 0_0603_5% PC203 0.1U_0603_25V7-M
PR203 @ 0_0402_5%
PR205 @ 0_0402_5%
100mA
PC208 4.7U_0603_6.3V6-K
+3VL

PL201 2.2UH_PCMB063T-2R2MS_8A_20%
EMC_NS@ PR204 4.7_0603_5%
EMC_NS@ PC209 680P_0402_50V7K

PC204 22U_0805_6.3V6-M
PC205 22U_0805_6.3V6-M
PC206 22U_0805_6.3V6-M
PC207 22U_0805_6.3V6-M
PC210 2200P_0402_25V7-K
PC211 0.1U_0402_25V6

+3VALW_P
EMC@ EMC@
PJ202 8A @JUMP_43X118
+3VALW

[57] EC_ON — PR206 2.2K_0402_1%

+3VL
PR217 47K_0402_1%
PR216 47K_0402_1%
@ PC213 0.1U_0402_25V6-K
PR208 1M_0402_5%

[57,65,66] MAINPWON_EC
NTJD5121NT1G PQ201B
NTJD5121NT1G PQ201A

PC212 0.01U_0402_25V7-K
PR207 1K_0402_1%

+5VALW
FSW=750 KHz
TDC:8A
OCP:11A

+3VALW
@ PR209 100K_0402_5%
@ PR210 0_0402_5%
@ PR211 0_0402_5%
+3V_PWRGD

B+ @ PJ203 JUMP_43X79

RF_NS@ EMC@ EMC@

PC231 47P_0402_50V8-J
PC233 2200P_0402_25V7-K
PC215 0.1U_0402_25V6-K
PC214 10U_0805_25V6-K
PC216 10U_0805_25V6-K

PU202 SYX198CQNC_QFN10_3X3

IN	8	2	PG
GND	9	6	BS
VCC	5	10	LX
EN	1	4	OUT
FB	3	7	LDO

+5V_VIN, +5V_PWRGD, +5VBS, +5VLX, +5VALW_OUT, +5VFB, 3V5V_ON

@ PR212 0_0603_5% PC217 0.1U_0603_25V7-M
PC218 2+5V_VCC 1U_0603_25V6M
PR213 @ 0_0402_5%
100mA
PC225 4.7U_0603_6.3V6-K
+5VLP

PL202 2.2UH_PCMB063T-2R2MS_8A_20%
EMC_NS@ PR214 4.7_0603_5%
EMC_NS@ PC226 680P_0402_50V7K

PC219 22U_0805_6.3V6-M
PC220 22U_0805_6.3V6-M
PC221 22U_0805_6.3V6-M
PC222 22U_0805_6.3V6-M
PC223 22U_0805_6.3V6-M
PC224 22U_0805_6.3V6-M
PC227 2200P_0402_25V7-K
PC228 0.1U_0402_25V6

+5VALW_P
EMC@ EMC@
PJ204 8A @JUMP_43X118
+5VALW

PC229 6800P_0402_25V7-K
PR215 1K_0402_1%

6800pf soft start 2ms
47nf soft start 7ms

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **3VALWP/5VALWP**

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1.2V
TDC: 12A
OCP: 15A
Fsw: 300KHz

+0.6VS
TDC: 1.5A

PJ301 @JUMP_43X118
PJ302 @JUMP_43X118
+1.2VP → +1.2V
PJ303 @JUMP_43X39
+0.6VSP → +0.6VS

B+ PJ304 @JUMP_43X79
B+_1.2V
PC302 10U_0805_25V6-K
PC303 10U_0805_25V6-K
EMC@ PC304 0.1U_0402_25V6
EMC@ PC307 2200P_0402_25V
RF_NS@ PC305 47P_0402_50V8-J
RF_NS@ PC306 68P_0402_50V8J

PC301 10U_0603_6.3V6M
PR301 100K_0402_1%
PR302 255K_0402_1%
PC308 10U_0603_6.3V6M
PC309 0.1U_0402_6.3V7-K

PQ301 AON7408L
PQ302 AON7380

PL301 1UH_PCMC063T-1R0MN_+-20%
PR303 2.2_0603_5%
PC310 0.22U_0603_25V7K
DH_1.2V
LX_1.2V
DL_1.2V
FB_1.2V

PU301 RT8231AGQW
PGND, VID, CS, VLDOIN, VTT, PAD, VTTGND, VTTSNS, GND, VTTREF, VDD, PGOOD, BOOT, UGATE, PHASE, LGATE, VDDQ, FB, TON, S5, S3

VTTREF_0.6V
PR306 5.1_0603_5%
+5VALW
PC315 0.033U_0402_16V7K
PC316 1U_0402_10VA-K

@PR308 100K_0402_1% → +3VS
PR310 @0_0402_5% → SM_PG_CTRL [7]
@PR311 0_0402_5% → SUSP# [50,57]
@PC318 0.1U_0402_6.3V7-K

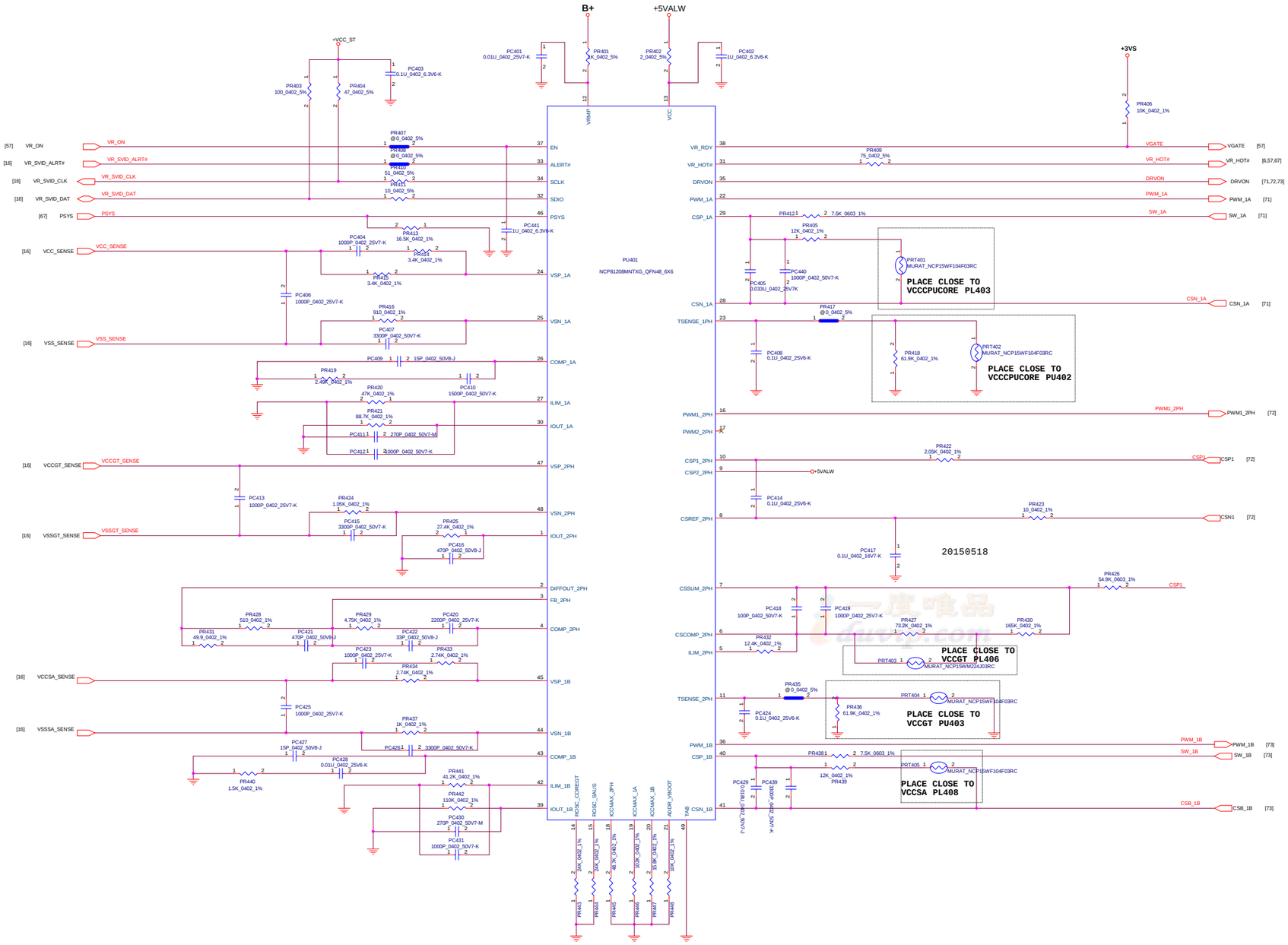
[50,57,78] SYSON
@PR312 0_0402_5%
@PR313 47K_0402_5%
@PC319 0.1U_0402_16V

PR309 887K_0402_1%

EMC@ EMC@ +1.2VP
PC312 2200P_0402_25V7-K
PC313 0.1U_0402_25V6
PC311 330U_D2_2V_R9M
PC314 @ 470P_0402_50V7K
PR305 6.04K_0402_1%
PR307 10K_0402_1%
EMC_NS@ PR304 4.7_0603_5%
EMC_NS@ PC317 680P_0402_50V7K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **+1.2V/+0.6VS**
Size: Custom | Document Number: **KENOBI** | Rev: 2.0
Date: Thursday, August 25, 2016 | Sheet 69 of 82



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

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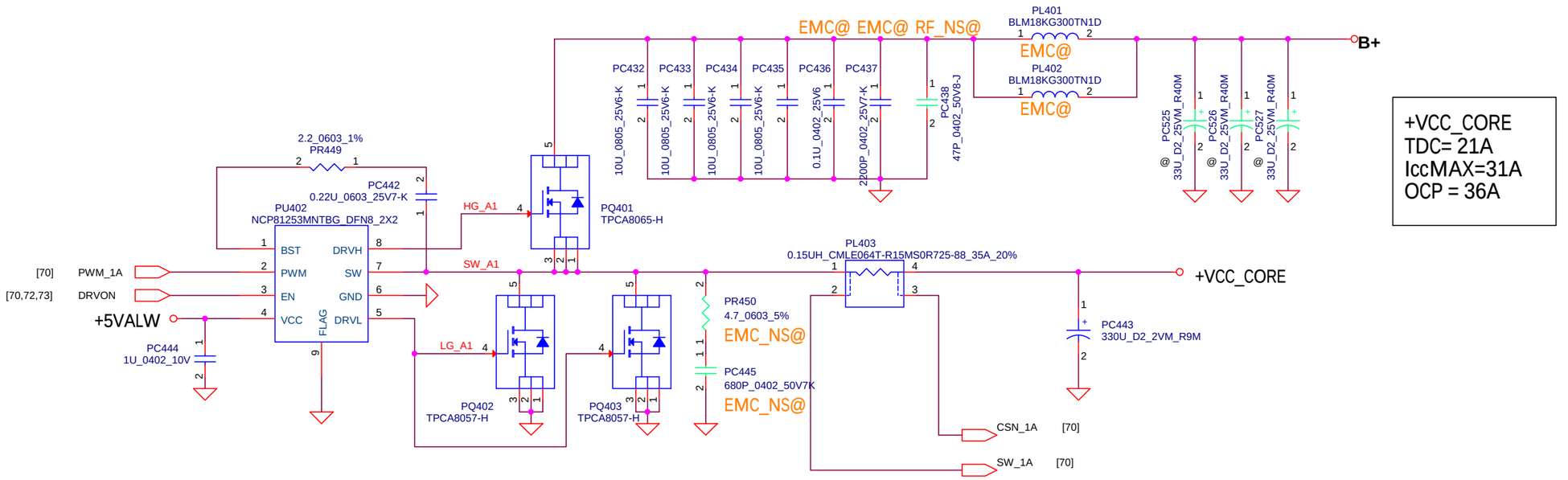
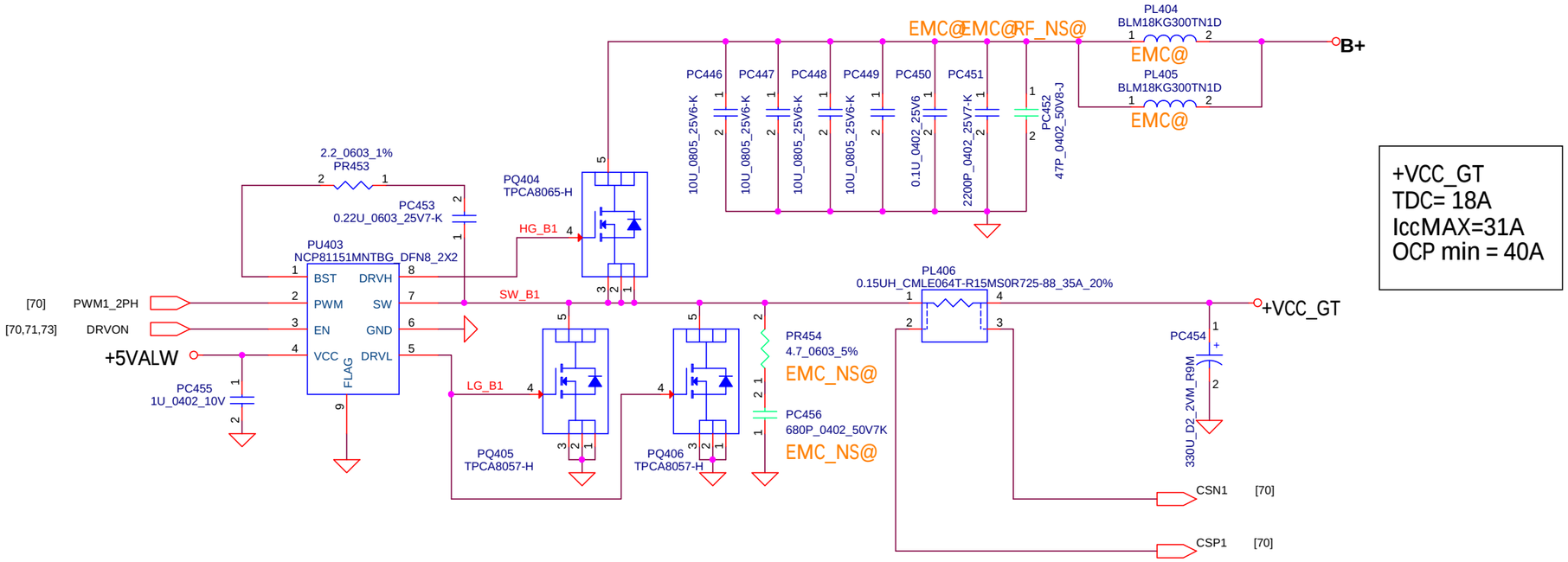
Title	IMVP8		
Size	Document Number	KENOBI	Rev 2.0
Date: Thursday, August 25, 2016	Sheet 70 of 82		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

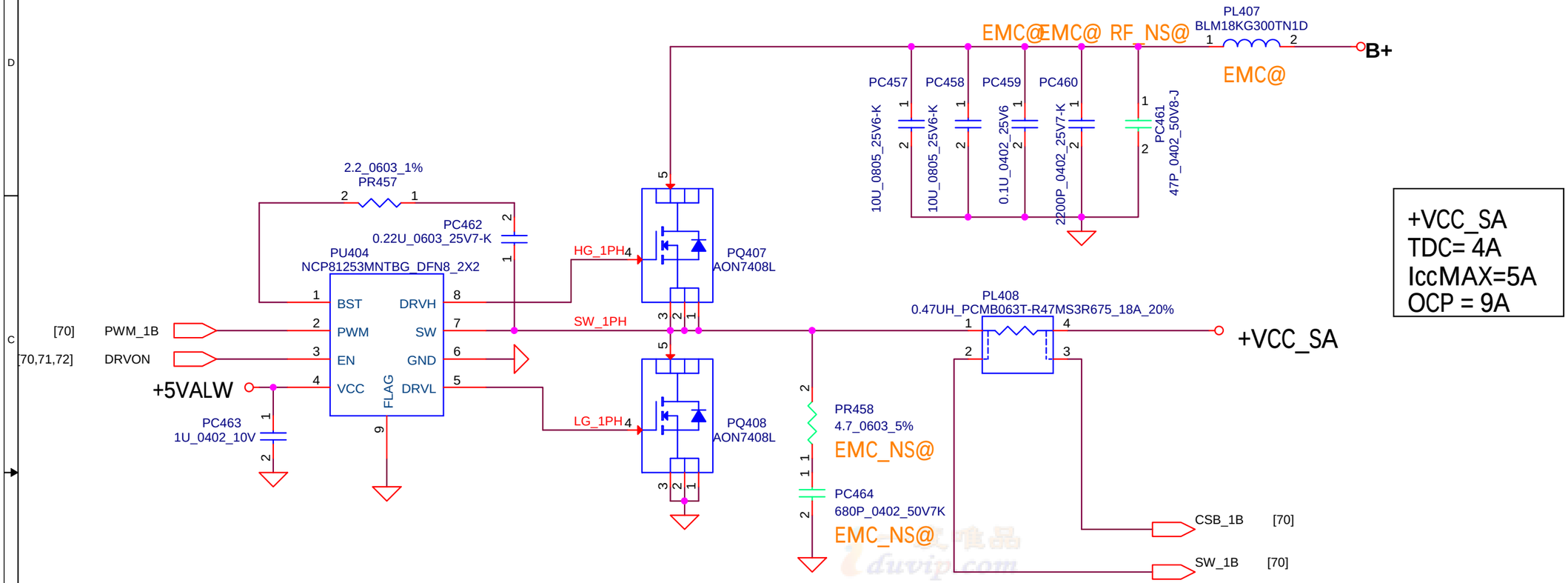
Title	+VCC_CORE		
Size: Custom	Document Number: KENOBI		Rev: 2.0
Date: Thursday, August 25, 2016	Sheet 71 of 82		



+VCC_GT
TDC= 18A
IccMAX=31A
OCP min = 40A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	*+VCC_GT*		
Size: Custom	Document Number: ***KENOBI***		Rev: 2.0
Date: Thursday, August 25, 2016	Sheet 72 of 82		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+VCC_SA		
Size	Custom	Document Number	KENOBI
Rev	2.0		
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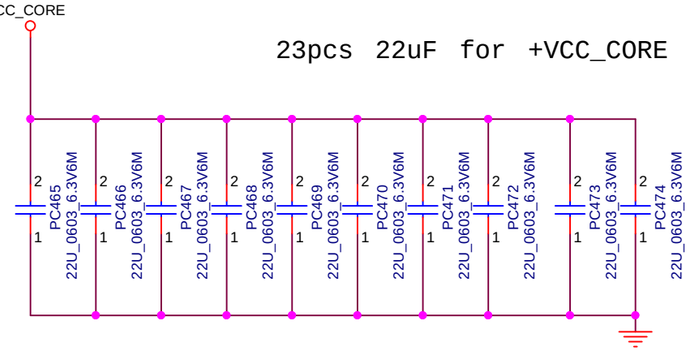
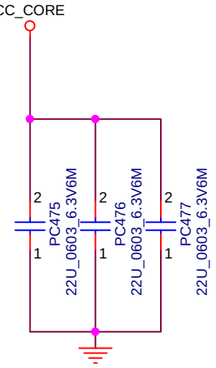
Based on PDDG rev 0.7 Table 5-1.

+VCC_CORE

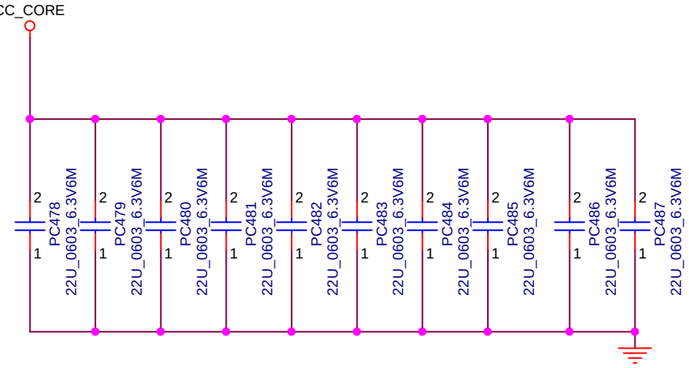
23pcs 22uF for +VCC_CORE



+VCC_CORE

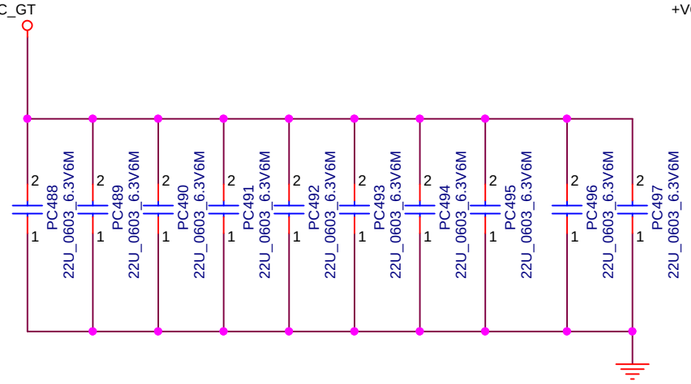


+VCC_CORE

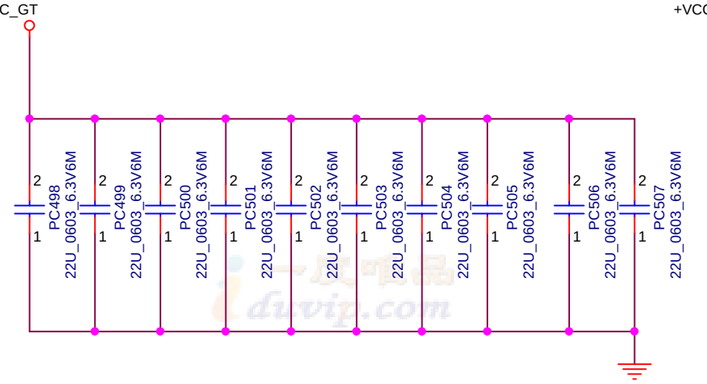


+VCC_GT

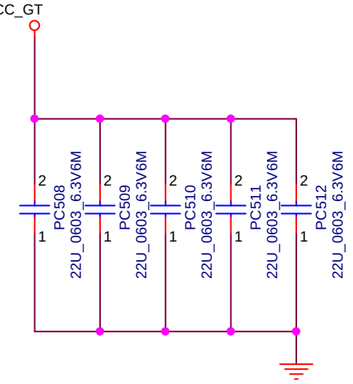
25pcs 22uF for +VCC_GT



+VCC_GT

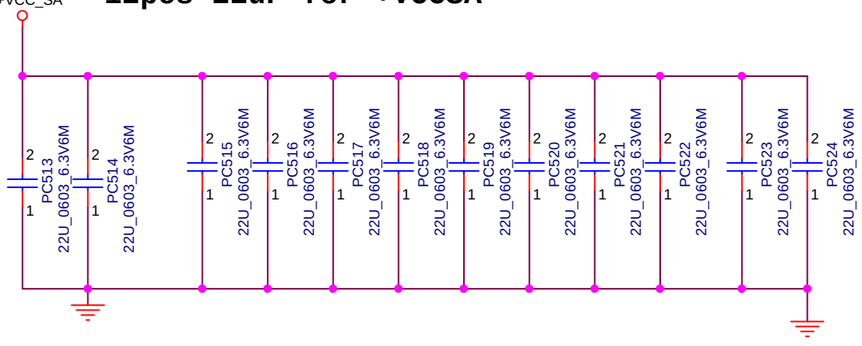


+VCC_GT



+VCC_SA

12pcs 22uF for +VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
B	KENOBI	2.0

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[28,33] VGA_ON

DIS@ PR633 10K_0402_1%

@PR601 0_0402_5% +3VS_VGA

[9,33] VGA_APWR_ON

PR602 @ 10K_0402_5%

PR604 @ 10K_0402_5%

PD601 @ CUS357_SOD323-2

PR605 @ 100K_0402_5%

DIS@ PC601 0.1U_0402_10V7-K

+3VS_AON

PR607 DIS@ 10K_0402_1%

PR609 @0_0402_5%

[28] VGA_PSI

PSI_VGA

@ PR611 10K_0402_1%

@ PC611 0.1U_0402_10V6-K

[28] VGA_PWM_VID

@PR608 0_0402_5%

EN_VGA_CORE

DIS@ PR612 20K_0402_1%

VREF_VGA

PC618 @ 2200P_0402_25V7-K

DIS@ PR613 20K_0402_1%

DIS@ PR615 2K_0402_5%

VID/BUF VID_VGA PSI_VGA

PR616 @0_0402_5%

DIS@ PR617 18K_0402_1%

PC621 DIS@ 4700P_0402_25V7K

PC620 DIS@ 0.01U_0402_25V

REFIN VREF_VGA FS

PR619 DIS@ 43K_0402_1%

[25] GFXCORE_GND_SENSE_D

[25] GFXCORE_VDD_SENSE_D

PC623 @ 1000P_0402_50V7-K

PC624 DIS@ 47P_0402_50V8-J

PR622 DIS@ 51_0402_1%

FB1_VGA

PC625 33P_0402_50V8-J

COMP_VGA

DIS@ PR624 10K_0402_1%

DIS@ PC626 100P_0402_50V8-J

FB2_VGA

DIS@ PR625 82K_0402_1%

PU601 NCP81172MNTWG_QFN24_4X4

REFIN VREF FS FBRTN FB COMP

VIDBUF VID PSI EN HG1 BST1

GND TSNS TALERT# VCC PGOOD HG2 BST2

PH1 LG1 PGND PVCC LG2 PH2

DIS@ PR628 5.9K_0402_1%

VREF_VGA

@ PRT601 100K_0402_1%_TSM0B104F4251RZ

@ PC636 0.1U_0402_10V6-K

T_ALERT_VGA TSNS_VGA VCC_VGA PG_VGA

PR629 @0_0402_5%

DGFX_PWRGD [25,28]

+5VALW

DIS@ PR630 2_0603_5%

DIS@ PC640 1U_0402_10VA-K

DIS@ PR632 10K_0402_1%

+3VALW

UGATE1_VGA BOOT1_VGA PHASE1_VGA LGATE1_VGA

DIS@ PR606 2.2_0603_5%

DIS@ PC610 0.22U_0603_25V7K

PR614 DIS@ 21K_0402_1%

PVCC_VGA

DIS@ PC622 4.7U_0603_6.3V6-K

PR621 @0_0402_5%

+5VALW

UGATE2_VGA BOOT2_VGA PHASE2_VGA LGATE2_VGA

DIS@ PR627 2.2_0603_5%

DIS@ PC635 0.22U_0603_25V7K

DIS@ PQ601 TPCA8065-H_DFN

DIS@ PQ604 TPCA8057-H_DFN

@PQ603 TPCA8057-H_DFN

DIS@ PQ605 TPCA8065-H_DFN

DIS@ PQ610 TPCA8057-H_DFN

@PQ609 TPCA8057-H_DFN

+VGA_B+

DIS_EMC@ DIS_EMC@

PC602 0.1U_0402_25V6

PC603 2200P_0402_25V

PC604 10U_0805_25V6-K

DIS@ PC605 10U_0805_25V6K

PL601 DIS_EMC@ MURATA BLM18KG300TN1D

PL602 DIS_EMC@ MURATA BLM18KG300TN1D

B+

DIS@ PL603 .22UH 20% PCME064T-R22MS0R985

DIS_EMC_NS@ PR610 4.7_0603_5%

DIS_EMC_NS@ PC619 680P_0402_50V7K

PC612 DIS@ 22U_0603_6.3V6-M

PC613 DIS@ 22U_0603_6.3V6M

PC614 DIS@ 22U_0603_6.3V6M

PC645 DIS@ 330U_D2_2VM_R9M

PC646 DIS@ 330U_D2_2VM_R9M

PC649 0.1U_0402_25V6

PC650 2200P_0402_25V7-K

+VGA_CORE

VGA_CORE Output Capacitor:
2 x 330uF SP(9mohm) +3 x 22uF(0603)

PC627 0.1U_0402_25V6

PC628 2200P_0402_25V7-K

PC629 DIS@ 10U_0805_25V6K

PC630 DIS@ 10U_0805_25V6K

PL606 DIS@ .22UH 20% PCME064T-R22MS0R985

DIS_EMC_NS@ PR631 4.7_0603_5%

DIS_EMC_NS@ PC644 680P_0402_50V7K

PC637 DIS@ 22U_0603_6.3V6M

PC638 DIS@ 22U_0603_6.3V6M

PC639 DIS@ 22U_0603_6.3V6M

PC647 DIS@ 330U_D2_2VM_R9M

PC651 DIS@ 330U_D2_2VM_R9M

+VGA_CORE

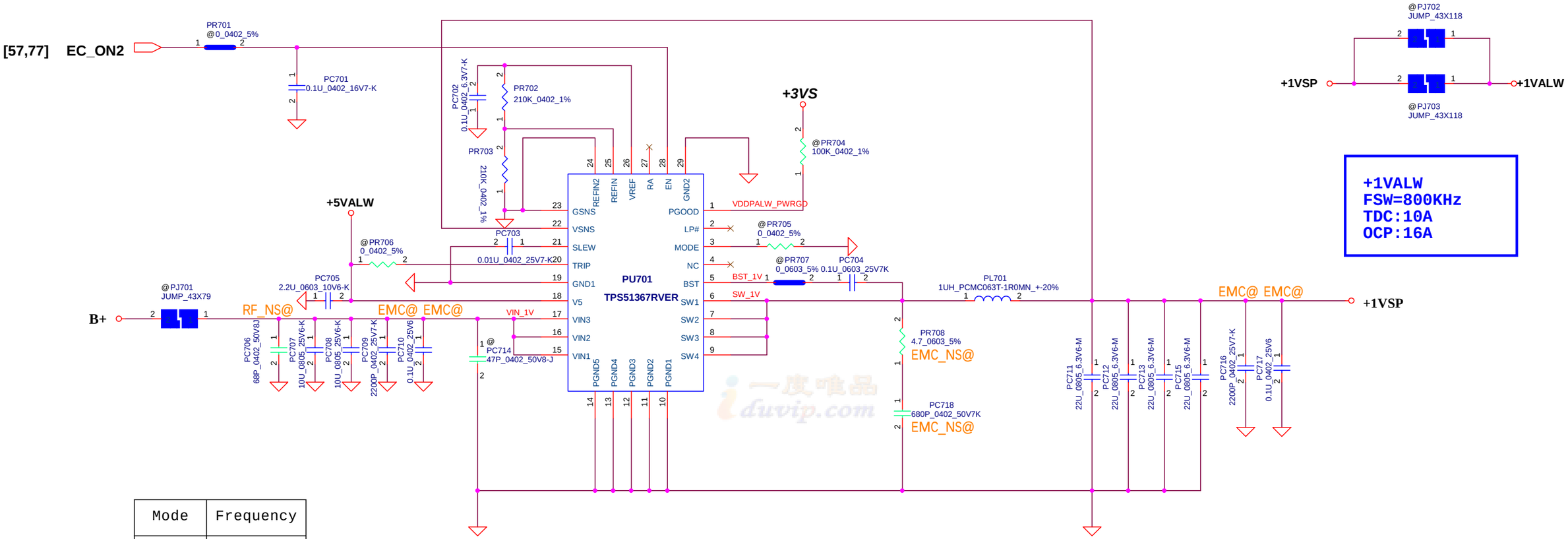
VGA_CORE Output Capacitor:
2 x 330uF SP(9mohm) +3 x 22uF(0603)

+VGA_CORE

TDC= 26A
EDC =51A
OCP = 58A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	VGA_CORE(NCP81174)		
Size	Document Number	KENOBI	Rev 2.0
Custom			
Date:	Thursday, August 25, 2016	Sheet	75 of 82



Mode	Frequency
GND	400KHz
Float	800KHz

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/08/01

Title	+1VALW		
Size	Document Number		Rev
Custom	KENOBI		2.0
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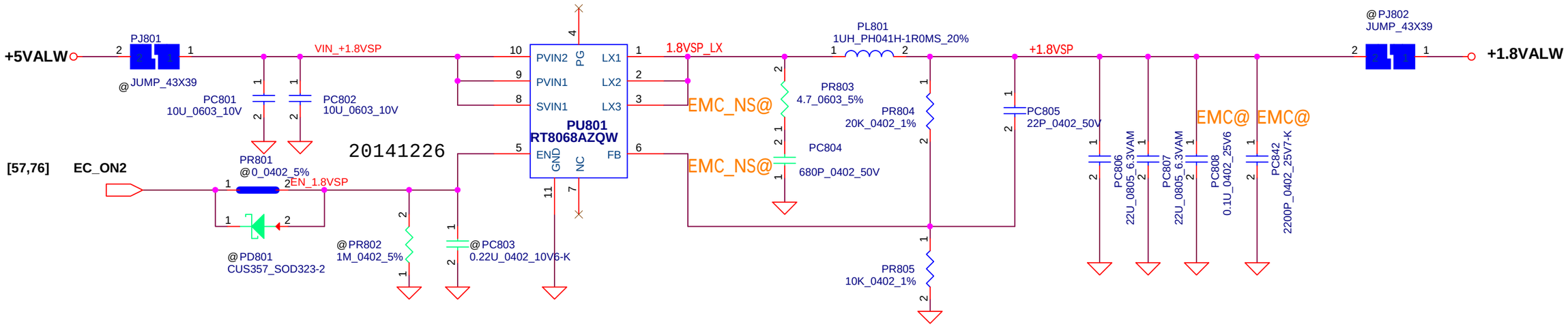
+1.8VALW
TDC: 1A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	*+1.8VALW*		
Size: Custom	Document Number: ***KENOBI***		Rev: 2.0
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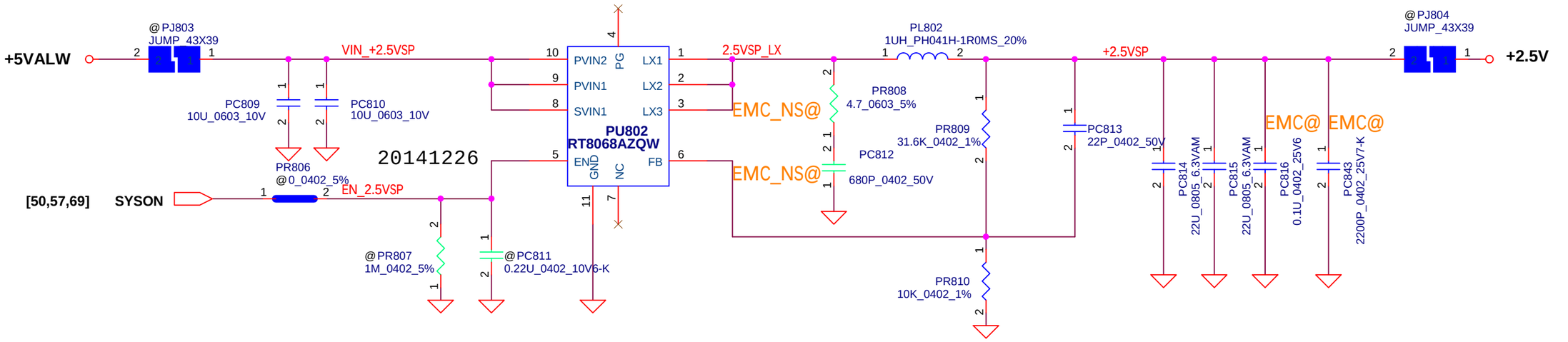
+2.5V
TDC: 2A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+2.5V	
Size: Custom	Document Number: KENOBI	Rev: 2.0
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+1.5VS_VGA
TDC: 6.8A
OCP: 12A
Fsw: 650KHz

@PD802 CUS357_SOD323-2

[28] FB_PWR_EN

DIS@ PR811 100K_0402_1%

DIS@ PR812 200K_0402_1%

DIS@ PC817 0.1U_0402_16V

B+

PJ805 @JUMP_43X79

DIS_EMC@ DIS_EMC@

DIS@ PC818 10U_0805_25V

DIS@ PC819 0.1U_0402_25V

DIS@ PC844 2200P_0402_25V7-K

PU803
SYX198DQNC
IN, EN, BS, GND, LX, ILMT, FB, BYP, PG, LDO

BS_1.5VSP

SW_1.5VSP

FB_1.5VSP

+3VALW

+3VS

@ PR814 0_0402_5%

@ PR815 100K_0402_1%

@ PR816 0_0402_5%

PR827 @0_0402_5%

[25] VDDQPWRGD

DIS@ PC820 4.7U_0402_6.3V6-M

DIS@ PC821 4.7U_0402_6.3V6-M

@PR813 0_0603_5%

DIS@ PC822 0.1U_0603_25V7K

DIS@ PL803 1UH_PCMC063T-1R0MN_+-20%

+1.5VSP

DIS_EMC@ DIS_EMC@

@PJ806 JUMP_43X118

+1.5VS_VGA

PR820 4.7_0603_5%

DIS_EMC_NS@

DIS_EMC_NS@

PC823 680P_0402_50V

DIS@ PC824 330P_0402_50V

DIS@ PR817 1K_0402_1%

PR818 30.9K_0402_1%

DIS@ PR819 20K_0402_1%

DIS@ PC825 22U_0805_6.3V6-M

DIS@ PC826 22U_0805_6.3V6-M

DIS@ PC827 22U_0805_6.3V6-M

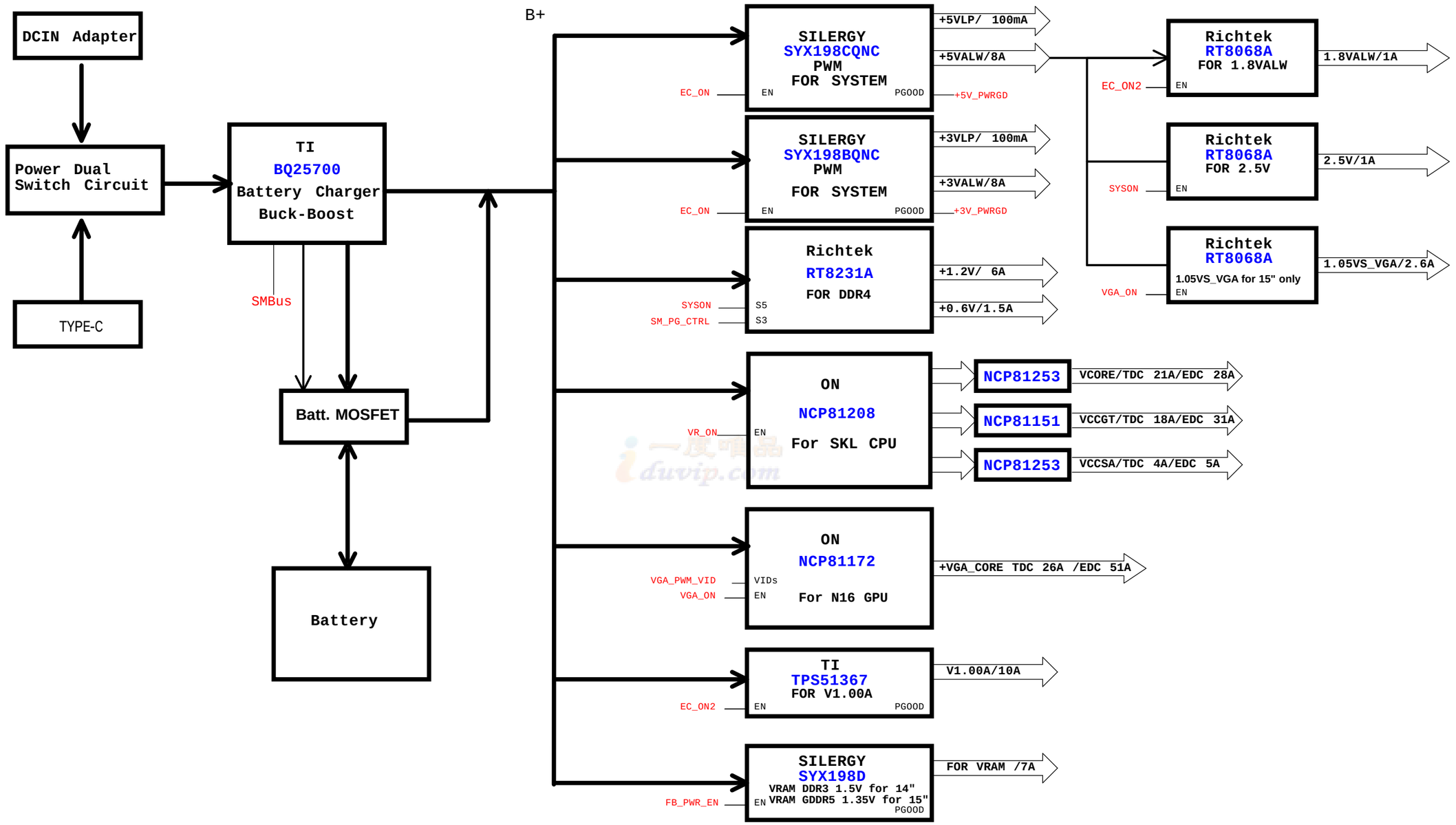
DIS@ PC828 22U_0805_6.3V6-M

PC829 2200P_0402_25V

PC830 0.1U_0402_25V6

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	*+1.5VS_VGA*		
Size Custom	Document Number	***KENOBI***	Rev 2.0
Date: Thursday, August 25, 2016	Sheet 79 of 82		



Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title	*Power Block Diagram*		
Size: Custom	Document Number: *KENOBI*		Rev: 2.0
Date: Thursday, August 25, 2016	Sheet 80 of 82		

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title

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Size	Document Number	Rev
Custom	***KENOBI***	2.0
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title

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LCFC

Size	Document Number	Rev
Custom	***KENOBI***	2.0
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