LCFC Confidential

Dooku/Jinn

E480/580

NM-B421 Rev1.0 Schematic

Intel KabyLake Processor with DDR4 + PCH

AMD R17M-P1 50/70

2017-09-12 Rev 1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: COVER PAGE

Size	Document Number	Rev
Custom	EE480/580 NM-B421	1.0

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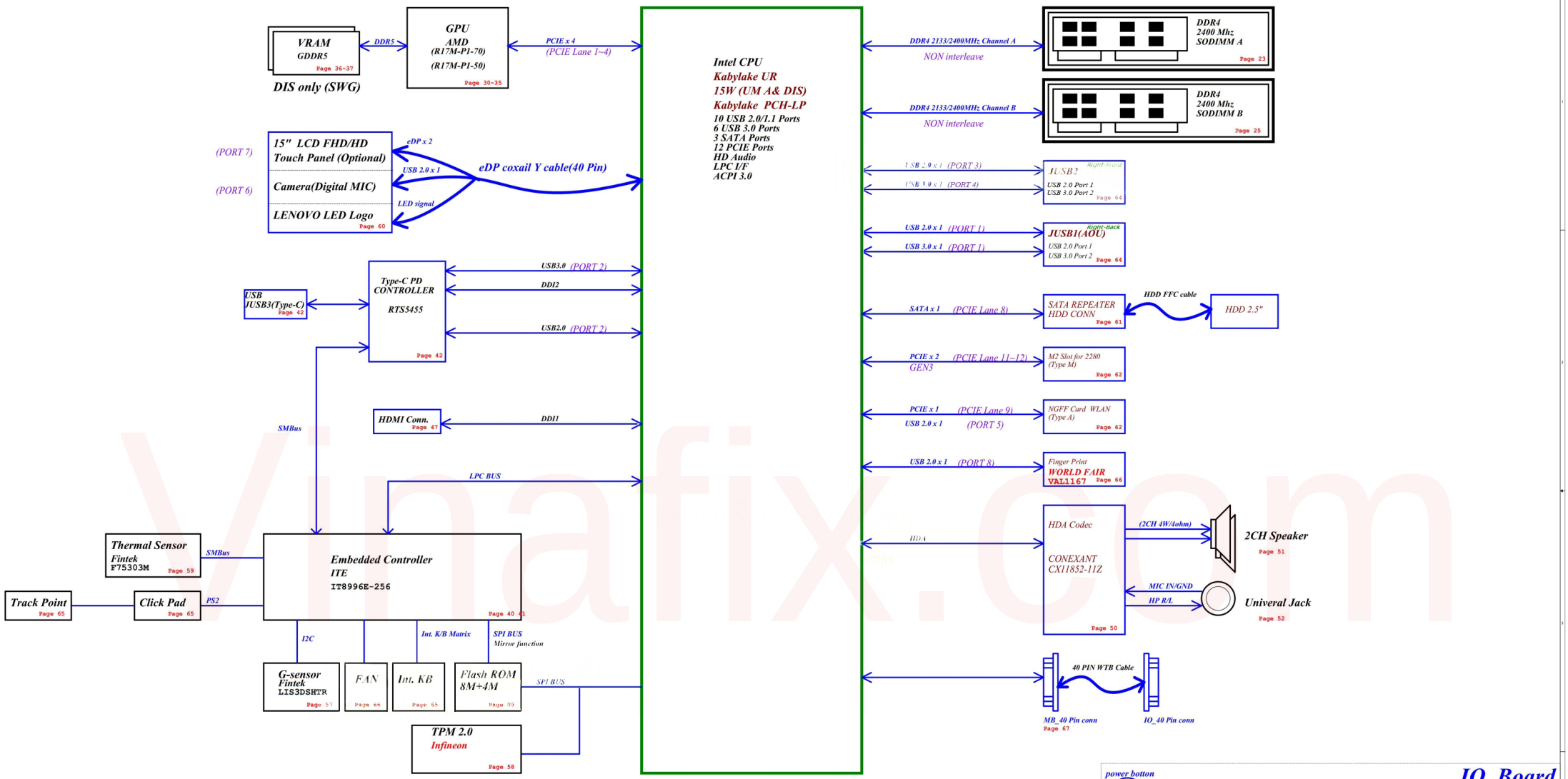

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: EB480 NM-B421 | Rev: 0.2

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Voltage Rails

O --> Means ON
X --> Means OFF

Power Plane / State	B+	+1VALW +3VALW +1.8VALW +5VALW	+1.2V +0.6VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

	SIGNAL						
STATE	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	V +3VALW	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_VGA	X	X	V +3VS	V +3VS	V +3VS	X	V +5VS	V +3VS	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_VGA	X	X	X	X	X	X	X	X	V +3VALW

HSIO Port

Port	Device
1	USB3.0 port (On Board)
2	USB3.0 port (On Board)
3	USB3.0 port (Docking)
4	USB3.0 port (Sub Board)
5	PCIE (GPU)
6	PCIE (GPU)
7	PCIE (GPU)
8	PCIE (GPU)
9	PCIE (LAN)
10	PCIE (Card Reader)
11	SATA express (PCIE)
12	SATA express (SATA)
13	PCIE (WLAN)
14	N/A
15	M.2 (PCIE)
16	M.2 (SATA)

USB2.0 Port

Port	Device
1	USB port (On Board)
2	USB port (On bBoard)
3	USB port (Docking)
4	USB port (Sub Board)
5	Smart Card
6	BT
7	Camera
8	Finger Printer
9	WWAN
10	Touch Panel

Title: SYSTEM LIST

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BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function with WWAN
DIS@	Discreate SKU
UMA@	UMA SKU
DPRE@	With DP re-driver
NODPRE@	Bypass DP re-driver
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
MIRROR@	For mirror function
TPM@	TPM function
X76@	GPU VRAM Setting
XDP@	XDP function
EXO@	EXO function
ME@	ME Connector
EMC@	For EMC function
EMC_NS@	For EMC function (no mount)
RF@	For RF function
RF_NS@	For RF function (no mount)
KBL@	For KBL-R SKU
KBLR@	For KBL SKU

Title: **BOM LIST**

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+3VS +3VS <6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>

+VCC_IO +VCC_IO <11,18,21,71>

+3VS

R0502 1 2 2K_0402_5% DDIP1_CTRLCLK

R0503 1 2 2K_0402_5% DDIP1_CTRLDATA

R0504 1 @ 2 2.2K_0201_1% DDIP2_CTRLCLK

R0505 1 2 2.2K_0402_5% DDIP2_CTRLDATA

DDIP1_HPD R0506 1 @ 2 100K_0402_5%

DDIP2_HPD R0507 1 2 100K_0201_1%

CPU_EDP_HPD R0508 1 2 100K_0402_5%

ENBKL R0509 1 2 100K_0201_1%

DP port	Enable	Disable
DDPB_CTRLDATA	pull-high	no connect
DDPC_CTRLDATA	pull-high	no connect

UC1A SKL_ULT

HDMI

<47> CPU_DDI1_N2 → DDI1_TXN[0]
<47> CPU_DDI1_P2 → DDI1_TXP[0]
<47> CPU_DDI1_N1 → DDI1_TXN[1]
<47> CPU_DDI1_P1 → DDI1_TXP[1]
<47> CPU_DDI1_N0 → DDI1_TXN[2]
<47> CPU_DDI1_P0 → DDI1_TXP[2]
<47> CPU_DDI1_N3 → DDI1_TXN[3]
<47> CPU_DDI1_P3 → DDI1_TXP[3]

USB TYPE C

<42> CPU_DDI2_N0 → DDI2_TXN[0]
<42> CPU_DDI2_P0 → DDI2_TXP[0]
<42> CPU_DDI2_N1 → DDI2_TXN[1]
<42> CPU_DDI2_P1 → DDI2_TXP[1]
<42> CPU_DDI2_N2 → DDI2_TXN[2]
<42> CPU_DDI2_P2 → DDI2_TXP[2]
<42> CPU_DDI2_N3 → DDI2_TXN[3]
<42> CPU_DDI2_P3 → DDI2_TXP[3]

DDI

HDMI

<47> DDIP1_CTRLCLK → DDIP1_CTRLCLK L13 → GPP_E18/DDPB_CTRLCLK
<47> DDIP1_CTRLDATA → DDIP1_CTRLDATA L12 → GPP_E19/DDPB_CTRLDATA

DDIP2_CTRLCLK N7 → GPP_E20/DDPC_CTRLCLK
DDIP2_CTRLDATA N8 → GPP_E21/DDPC_CTRLDATA

N11 → GPP_E22/DDPD_CTRLCLK
N12 → GPP_E23/DDPD_CTRLDATA

+VCC_IO R0501 24.9_0402_1% EDP_COMP E52 → EDP_RCOMP

DISPLAY SIDEBANDS

EDP

EDP_TXN[0] C47 CPU_EDP_TX0- → CPU_EDP_TX0- <60>
EDP_TXP[0] C46 CPU_EDP_TX0+ → CPU_EDP_TX0+ <60>
EDP_TXN[1] D46 CPU_EDP_TX1- → CPU_EDP_TX1- <60>
EDP_TXP[1] C45 CPU_EDP_TX1+ → CPU_EDP_TX1+ <60>
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 CPU_EDP_AUX# → CPU_EDP_AUX# <60>
EDP_AUXP F45 CPU_EDP_AUX → CPU_EDP_AUX <60>

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48 DDIP2_AUXN → DDIP2_AUXN <42>
DDI2_AUXP F48 DDIP2_AUXP → DDIP2_AUXP <42>
DDI3_AUXN G46
DDI3_AUXP C46

GPP_E13/DDPB_HPD0 L9 DDIP1_HPD → DDIP1_HPD <47>
GPP_E14/DDPC_HPD1 L7 DDIP2_HPD → DDIP2_HPD <42>
GPP_E15/DDPD_HPD2 L8
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 CPU_EDP_HPD → CPU_EDP_HPD <60>

EDP_BKLTEN R12 ENBKL → ENBKL <40>
EDP_BKLTCTL R11 PCH_EDP_PWM → PCH_EDP_PWM <60>
EDP_VDDEN U13 PCH_ENVDD → PCH_ENVDD <60>

HDMI
USB TYPE C

SKYLAKE-U_BGA1356 REV = 1 1 OF 20

EDP_RCOMP
1. Trace width=20 mils, Spacing=25mil, Max length=100mils
2. RC1 close to MCP
Trace Width=20mil, Spacing=25mil, Max length=100mil

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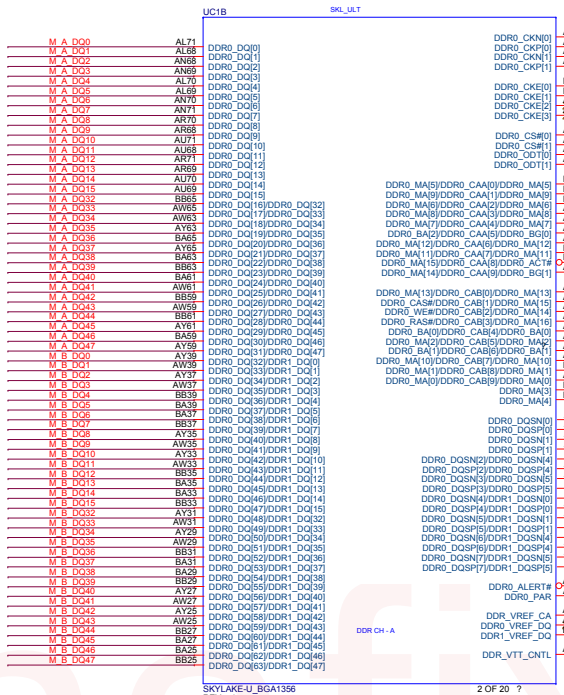
+3VS +3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>
+2.5V +2.5V <23,24,25,26,94>
+3VALW +3VALW <9,12,15,19,40,50,58,60,63,65,66,67,72,83,84,91,95>
+1.2V +1.2V <7,18,23,24,25,26,85>

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71 AL68 AN68 AN69 AL70 AL69 AN70 AN71 AR70 AR68 AU71 AU68 AR71 AR69 AU70 AU69	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[14] DDR0_DQ[15]	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[14] DDR0_DQ[15]
Block 2	BB65 AW65 AW63 AY63 BA65 AY65 BA63 BB63 BA61 AW61 BB59 AW59 BB61 AY61 BA59 AY59	DDR0_DQ[16] DDR0_DQ[17] DDR0_DQ[18] DDR0_DQ[19] DDR0_DQ[20] DDR0_DQ[21] DDR0_DQ[22] DDR0_DQ[23] DDR0_DQ[24] DDR0_DQ[25] DDR0_DQ[26] DDR0_DQ[27] DDR0_DQ[28] DDR0_DQ[29] DDR0_DQ[30] DDR0_DQ[31]	DDR0_DQ[32] DDR0_DQ[33] DDR0_DQ[34] DDR0_DQ[35] DDR0_DQ[36] DDR0_DQ[37] DDR0_DQ[38] DDR0_DQ[39] DDR0_DQ[40] DDR0_DQ[41] DDR0_DQ[42] DDR0_DQ[43] DDR0_DQ[44] DDR0_DQ[45] DDR0_DQ[46] DDR0_DQ[47]
Block 4	AY39 AW39 AY37 AW37 BB39 BA39 BA37 BB37 AY35 AW35 AY33 AW33 BB35 BA35 BA33 BB33	DDR0_DQ[32] DDR0_DQ[33] DDR0_DQ[34] DDR0_DQ[35] DDR0_DQ[36] DDR0_DQ[37] DDR0_DQ[38] DDR0_DQ[39] DDR0_DQ[40] DDR0_DQ[41] DDR0_DQ[42] DDR0_DQ[43] DDR0_DQ[44] DDR0_DQ[45] DDR0_DQ[46] DDR0_DQ[47]	DDR1_DQ[0] DDR1_DQ[1] DDR1_DQ[2] DDR1_DQ[3] DDR1_DQ[4] DDR1_DQ[5] DDR1_DQ[6] DDR1_DQ[7] DDR1_DQ[8] DDR1_DQ[9] DDR1_DQ[10] DDR1_DQ[11] DDR1_DQ[12] DDR1_DQ[13] DDR1_DQ[14] DDR1_DQ[15]
Block 6	AY31 AW31 AY29 AW29 BB31 BA31 BA29 BB29 AY27 AW27 AY25 AW25 BB27 BA27 BA25 BB25	DDR0_DQ[48] DDR0_DQ[49] DDR0_DQ[50] DDR0_DQ[51] DDR0_DQ[52] DDR0_DQ[53] DDR0_DQ[54] DDR0_DQ[55] DDR0_DQ[56] DDR0_DQ[57] DDR0_DQ[58] DDR0_DQ[59] DDR0_DQ[60] DDR0_DQ[61] DDR0_DQ[62] DDR0_DQ[63]	DDR1_DQ[32] DDR1_DQ[33] DDR1_DQ[34] DDR1_DQ[35] DDR1_DQ[36] DDR1_DQ[37] DDR1_DQ[38] DDR1_DQ[39] DDR1_DQ[40] DDR1_DQ[41] DDR1_DQ[42] DDR1_DQ[43] DDR1_DQ[44] DDR1_DQ[45] DDR1_DQ[46] DDR1_DQ[47]

LOGIC



TABLE

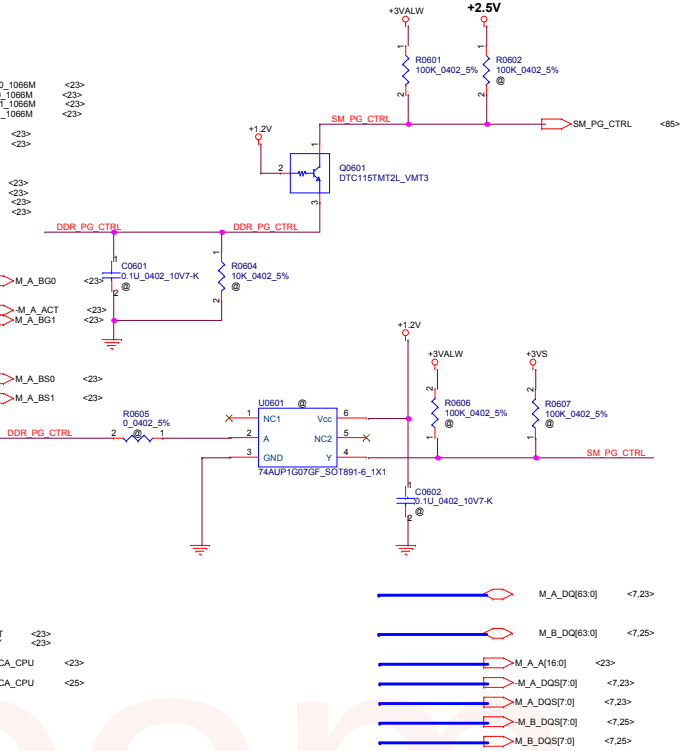
	Pin	Interleave	Non-Interleave
Block 0	AM70 AM69 AT69 AT70	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]
Block 2	BA64 AY64 AY60 BA60	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]
Block 4	BA38 AY38 AY34 BA34	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]
Block 6	BA30 AY30 AY26 BA26	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

LOGIC



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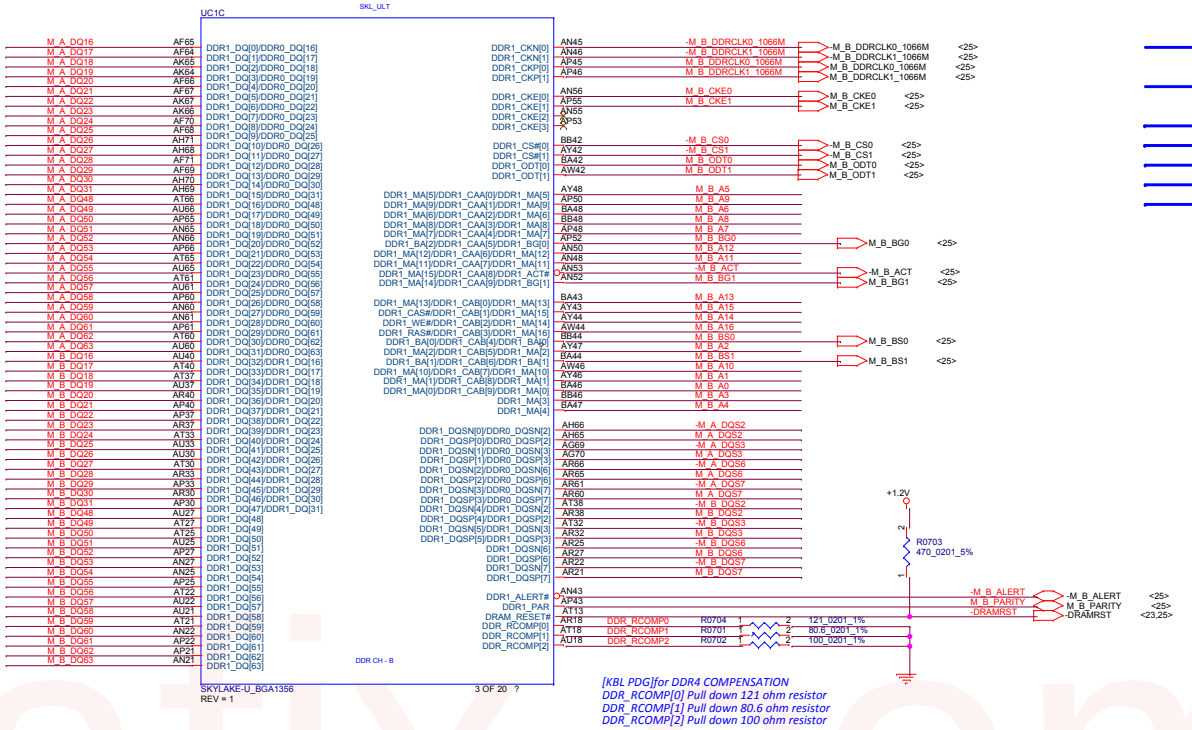

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

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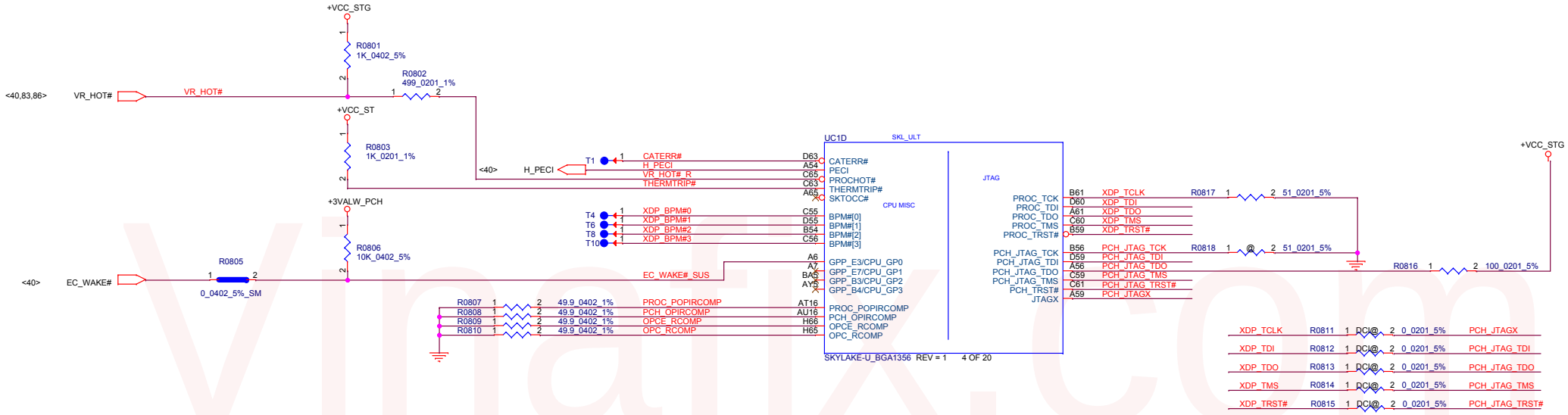
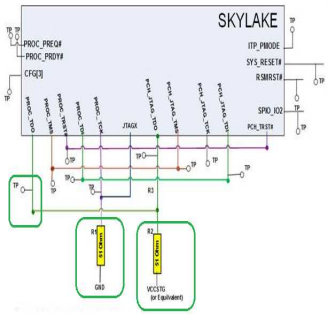
+VCC_ST +VCC_ST <15,16,18,21,71,86>

+VCC_STG +VCC_STG <16,18,71>

+3VALW_PCH +3VALW_PCH <9,10,11,12,19>



[KBL PDG FOR DCL DEBUG]



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Title: **KBL(D)_MISC/ JTAG**

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+3VALW_PCH +3VALW_PCH <8,10,11,12,19>
+3V_SPI +3V_SPI <19>
+3VS +3VS <5,6,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>

Mirror Code, Close to SPI ROM (UC8M1).

<40> FSCE# — FSCE# R0924 2 0_0402_5%_SM SPI_CS0#_8MB
<40> SPI_FMOSI# — SPI_FMOSI# R0925 2 0_0402_5%_SM SPI_SI_8MB
<40> SPI_FMISO — SPI_FMISO R0926 2 0_0402_5%_SM SPI_SO_8MB
<40> SPI_FSCK — SPI_FSCK R0927 2 0_0402_5%_SM SPI_CLK_8MB

To TPM IC

<58> SPI_CLK — SPI_CLK
<58> SPI_SI — SPI_SI
<58> SPI_SO — SPI_SO
<58> SPI_CS2#_TPM — SPI_CS2#_TPM

Reverse internal 1K PU high

R0928 1K_0402_1% R0902 1K_0402_1%
R0947 1K_0402_1% R0946 1K_0402_1%

R0950 10K_0804_8P4R_5%
SERIRQ
KBRST#
EC_SCI#

JTAG ODT
SPI0_MOSI
R0914 1K_0402_5% SPI_SI
R0916 1K_0402_5% SPI_SO
R0915 20K_0402_5% Default
R0917 20K_0402_5%

UC1E SKL_ULT

SPI - FLASH
SPI0_CLK AV2
SPI0_MISO AW3
SPI0_MOSI AV3
SPI0_IO2 AW2
SPI0_IO3 AU4
SPI0_CS0# AU3
SPI0_CS1# AU2
SPI0_CS2# AU1

SPI - TOUCH
GPP_D1/SPI1_CLK M2
GPP_D2/SPI1_MISO M3
GPP_D3/SPI1_MOSI M4
GPP_D21/SPI1_IO2 V2
GPP_D22/SPI1_IO3 V3
GPP_D0/SPI1_CS# M1

C-LINK
CL_CLK G3
CL_DATA G2
CL_RST# G1

SMBUS, SMLINK
GPP_C0/SMBCLK R7 PCH_SMB_CLK
GPP_C1/SMBDATA R8 PCH_SMB_DATA
GPP_C2/SMBALERT# R10 GPP_C2
GPP_C3/SML0CLK R9 PCH_SML0_CLK
GPP_C4/SML0DATA W2 PCH_SML0_DAT
GPP_C5/SML0ALERT# W1 GPP_C5
GPP_C6/SML1CLK W3 PCH_SML1CLK
GPP_C7/SML1DATA V3 PCH_SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23

LPC
GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME#
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT#

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 PCH_PCI_CLK_R
GPP_A10/CLKOUT_LPC1 AY9
GPP_A8/CLKRUN# AW11 CLKRUN#

GPP_A0/RCIN#
GPP_A6/SERIRQ AY11
GPP_A7/GPP_A7 AW13 KBRST#

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EC_SCI# <40>
CL_CLK_WLAN <63>
CL_DATA_WLAN <63>
CL_RST_WLAN# <63>
KBRST# <40>
SERIRQ <40,58>

LAN PHY
R0909 150K_0402_5%
FOR DCI USE

EC and TPM Module debug port
LPC_AD0 <40>
LPC_AD1 <40>
LPC_AD2 <40>
LPC_AD3 <40>
LPC_FRAME# <40>
T18
R0910 2_22_0402_5%
R0911 8.2K_0402_5%
CLK_PCI_EC <40>
C0903 22P_0402_50V8-J EMC_NS@

R0951 10K_0804_8P4R_5%
PCH_SMB_CLK
PCH_SMB_DATA
PCH_SML1CLK
PCH_SML1DATA
PCH_SML0_DAT R0907 499_0201_1%
PCH_SML0_CLK R0908 499_0201_1%
SUS_STAT# R0952 10K_0402_5%

20121218
GPP_C5, Internal PD 20K
*L: LPC
H: eSPI
R0918 1K_0402_5% GPP_C5
R0919 20K_0402_5%

Functional Strap Definitions
L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
GPP_C2, Internal PD 20K
R0912 1K_0402_5% GPP_C2
R0913 20K_0402_5%

[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM

+3VALW 0.085 A, 10mils +3V_SPI
R0905 0_0402_5%_SM

8MB(64Mb)
SPI_CS0#_8MB_R R0948 2 0_0402_5%_SM SPI_CS0#_8MB
U0901 W25Q64JVSSIQ SA000089Z00
/CS VCC
DO (IO1) IO3
IO2 CLK
GND DI (IO0)
SPI_SO_8MB SPI_IO3_8MB SPI_CLK_8MB SPI_SI_8MB
C0902 0.1U_0402_10V7-K

4MB(32Mb)
SPI_CS1#_4MB_R R0949 4MB 2 0_0402_5% SPI_CS1#_4MB
U0902 W25Q32JVSSIQ 4MB SA000089800
CS# VCC
DO HOLD#
WP# CLK
GND DI
SPI_SO_4MB SPI_IO3_4MB SPI_CLK_4MB SPI_SI_4MB
C0901 0.1U_0402_10V7-K 4MB

R0935,0936,0937,0938,0942 shold be Near U0901 SPI ROM(0.5~1 inch)
SPI_IO3_8MB R0935 33_0402_5% SPI_IO3
SPI_CLK_8MB R0936 33_0402_5% SPI_CLK
SPI_SI_8MB R0937 33_0402_5% SPI_SI
SPI_IO2_8MB R0938 33_0402_5% SPI_IO2
SPI_SO_8MB R0939 33_0402_5% SPI_SO

R0940,0941,0942,0943,0944 shold be Near U0902 SPI ROM(0.5~1 inch)
SPI_IO3_4MB R0940 33_0402_5% SPI_IO3
SPI_CLK_4MB R0942 33_0402_5% SPI_CLK
SPI_SI_4MB R0943 33_0402_5% SPI_SI
SPI_IO2_4MB R0944 33_0402_5% SPI_IO2
SPI_SO_4MB R0945 33_0402_5% SPI_SO

SMBus
R0920 4.7K_0402_5%
R0921 4.7K_0402_5%
PCH_SMB_CLK PM_SMB_CLK <23,25,65>
PCH_SMB_DATA PM_SMB_DAT <23,25,65>
Q0901A L2N7002KDW1T1G_SOT363-6 SB000013A00
R0953 0_0402_5%
Q0901B L2N7002KDW1T1G_SOT363-6 SB000013A00
R0954 0_0402_5%
DIMM1, DIMM2 CP
PCH_SML1CLK EC_SMB_CK3 <32,40,57,59>
PCH_SML1DATA EC_SMB_DA3 <32,40,57,59>
Q0902A L2N7002KDW1T1G_SOT363-6 SB000013A00
Q0902B L2N7002KDW1T1G_SOT363-6 SB000013A00
2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV
GPU, Thermal Sendor,
Embedded Controller, G sensor

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+3VALW_PCH +3VALW_PCH <8,9,11,12,19>
+3VS +3VS <5,6,9,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>
+3VALW +3VALW <6,9,12,15,19,40,50,58,60,63,65,66,67,72,83,84,91,95>

GPP_B18, Internal PD 20K
*L: Disable "No Reboot" mode
H: Enable "No Reboot" mode
+3VALW_PCH
R1008 1K_0402_5% @
GPP_B18
R1009 20K_0402_5% @

GPP_B22, Internal PD 20K
*L: SPI
H: LPC
+3VS
R1010 20K_0402_5% @
GPP_B22
R1011 20K_0402_5% @

+3VS
R1012 10K_0201_5% @
DISCRETE_PRESENCE
R1013 10K_0201_5% @

+3VALW_PCH
R1001 10K_0402_5% @
RF_OFF#
+3VS
R1002 10K_0402_5%

+3VALW_PCH +3VS
R1003 10K_0201_5% VGA_ON
R1004 4.7K_0402_5% BT_ON
R1007 @ 10K_0201_5% DGPU_HOLD_RST#
R1035 100K_0201_5%

UC1F SKL_ULT
LPSS
<63> RF_OFF# RF_OFF# AN8 GPP_B15/GSPI0_CS#
AP7 GPP_B16/GSPI0_CLK
AP8 GPP_B17/GSPI0_MISO
GPP_B18 AR7 GPP_B18/GSPI0_MOSI
AM5 GPP_B19/GSPI1_CS#
AN7 GPP_B20/GSPI1_CLK
<63> BT_ON BT_ON AP5 GPP_B21/GSPI1_MISO
GPP_B22 AN5 GPP_B22/GSPI1_MOSI
<60> D_J_CTL D_J_CTL AB1 GPP_C8/UART0_RXD
PLANARID1 AB2 GPP_C9/UART0_TXD
PLANARID2 W4 GPP_C10/UART0_RTS#
PLANARID3 AB3 GPP_C11/UART0_CTS#
<52,63> UART2_RX UART2_RX AD1 GPP_C20/UART2_RXD
<52,63> UART2_TX UART2_TX AD2 GPP_C21/UART2_TXD
PLANARID4 AD3 GPP_C22/UART2_RTS#
<60> TPNL_EN TPNL_EN AD4 GPP_C23/UART2_CTS#
FN, F1, F4 PD 100K, BIOS need output "High" while active
U7 GPP_C16/I2C0_SDA
<37,39> VGA_ON VGA_ON U6 GPP_C17/I2C0_SCL
<37> DGPU_PWROK DGPU_PWROK U8 GPP_C18/I2C1_SDA
To VGA_CORE IC, RPC3.7 <30> DGPU_HOLD_RST# DGPU_HOLD_RST# U9 GPP_C19/I2C1_SCL
AH9 GPP_F4/I2C2_SDA
AH10 GPP_F5/I2C2_SCL
AH11 GPP_F6/I2C3_SDA
AH12 GPP_F7/I2C3_SCL
AF11 GPP_F8/I2C4_SDA
AF12 GPP_F9/I2C4_SCL
SKYLAKE-U_BGA1356
REV = 1
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ISH
GPP_D9 P2
GPP_D10 P3 LID_CLOSE#_PCH R1032 1 2 0_0201_5%_SM LID_CLOSE#
GPP_D11 P4 PAD_DISABLE_PCH R1033 1 2 0_0201_5%_SM PAD_DISABLE
GPP_D12 P1 TP_RESET_PCH R1034 1 2 0_0201_5%_SM TP_RESET
LID_CLOSE# <65>
PAD_DISABLE <65>
TP_RESET <65>
M4 DISCRETE_PRESENCE
GPP_D5/ISH_I2C0_SDA N3
GPP_D6/ISH_I2C0_SCL
GPP_D7/ISH_I2C1_SDA N1
GPP_D8/ISH_I2C1_SCL N2
GPP_F10/I2C5_SDA/ISH_I2C2_SDA AD11
GPP_F11/I2C5_SCL/ISH_I2C2_SCL AD12
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA U1
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL U2
GPP_D15/ISH_UART0_RTS# U3
GPP_D16/ISH_UART0_CTS#/SML0BALERT# U4
GPP_C12/UART1_RXD/ISH_UART1_RXD AC1
GPP_C13/UART1_TXD/ISH_UART1_TXD AC2 F1_LED#
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AC3 F4_LED#
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB4 GPP_C15
F1_LED# <65>
F4_LED# <65>
GPP_A18/ISH_GP0 AY8
GPP_A19/ISH_GP1 BA8
GPP_A20/ISH_GP2 BB7
GPP_A21/ISH_GP3 BA7
GPP_A22/ISH_GP4 AY7
GPP_A23/ISH_GP5 AW7
GPP_A12/BM_BUSY#/ISH_GP6 AP13

+3VS
R1026 10K_0402_5% @ GPP_C15
R1027 10K_0402_5% @ F1_LED#
R1028 10K_0402_5% @ F4_LED#

Project/SKU ID

	PLANARID3	PLANARID2		PLANARID1 (GPP_C9)		PLANARID4 (GPP_22)
SDV	0	0	DIS (R1023)	1	NTPM(R1031)	1
FVT	0	1	UMA (R1024)	0	TPM(R1030)	0
SIT	1	0				
SVT	1	1				

+3VS
R1019 10K_0201_5%
R1021 10K_0201_5%
R1023 DIS@ 10K_0201_5%
R1031 NTPM@ 10K_0201_5%
PLANARID1
PLANARID2
PLANARID3
PLANARID4
R1020 10K_0201_5% @
R1022 10K_0201_5% @
R1024 UMA@ 10K_0201_5%
R1030 TPM@ 10K_0201_5%

Vinafix

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+3VALW_PCH +3VALW_PCH <8,9,10,12,19>
+3VS +3VS <5,6,9,10,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>
+VCC_HDA +VCC_HDA <19>
+VCC_IO +VCC_IO <5,18,21,71>

RP1101
33_0804_8P4R_5%
SD30000370T

<50> PCH_HDA_RST# PCH_HDA_RST# HDA_RST#
<50> PCH_HDA_SDOUT PCH_HDA_SDOUT HDA_SDOUT
<50> PCH_HDA_SYNC PCH_HDA_SYNC HDA_SYNC

<40> ME_FLASH R1101 1 2 0_0402_5%_SM

<50> PCH_HDA_BCLK PCH_HDA_BCLK R1110 1 EMC@ 2 33_0402_5% HDA_BCLK
C1101 22P_0402_50V8-J EMC_NS@

Processor Strapping
543016_543016_SKL_PDG_UY_1_0_pub
P780

+VCC_HDA
R1102 1K_0402_5% @
HDA_SDOUT
R1103 20K_0402_5% @

+VCC_IO
R1104 1K_0402_5% @
PCH_HDA_SDIN0
R1105 20K_0402_5% @

GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3_3 through a 1~8.2KΩ resistor to disable this capability

+3VS
R1106 8.2K_0402_5% @
PCH_BEEP
R1107 20K_0402_5% @

+3VALW_PCH
R1108 1K_0402_5% @

WINDU and E470 can't stuff TBD

UC1G
SKL_ULT
AUDIO
SDIO/SDXC

HDA_SYNC BA22 HDA_SYNC/I2S0_SFRM
HDA_BCLK AY22 HDA_BLK/I2S0_SCLK
HDA_SDOUT BB22 HDA_SDO/I2S0_TXD
<50> PCH_HDA_SDIN0 BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
HDA_RST# AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD
AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD
H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1
<51> PCH_BEEP PCH_BEEP AW5 GPP_B14/SPKR

GPP_G0/SD_CMD AB11
GPP_G1/SD_DATA0 AB13
GPP_G2/SD_DATA1 AB12
GPP_G3/SD_DATA2 W12
GPP_G4/SD_DATA3 W11
GPP_G5/SD_CD# W10
GPP_G6/SD_CLK W8
GPP_G7/SD_WP W7
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9
GPP_A16/SD_1P8_SEL BB9
SD_RCOMP AB7
R1109 1 2 200_0402_1%
GPP_F23 AF13

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Title: KBL(G)_HDA/ GPIO
Size: Custom
Document Number: EE480 NM-B421
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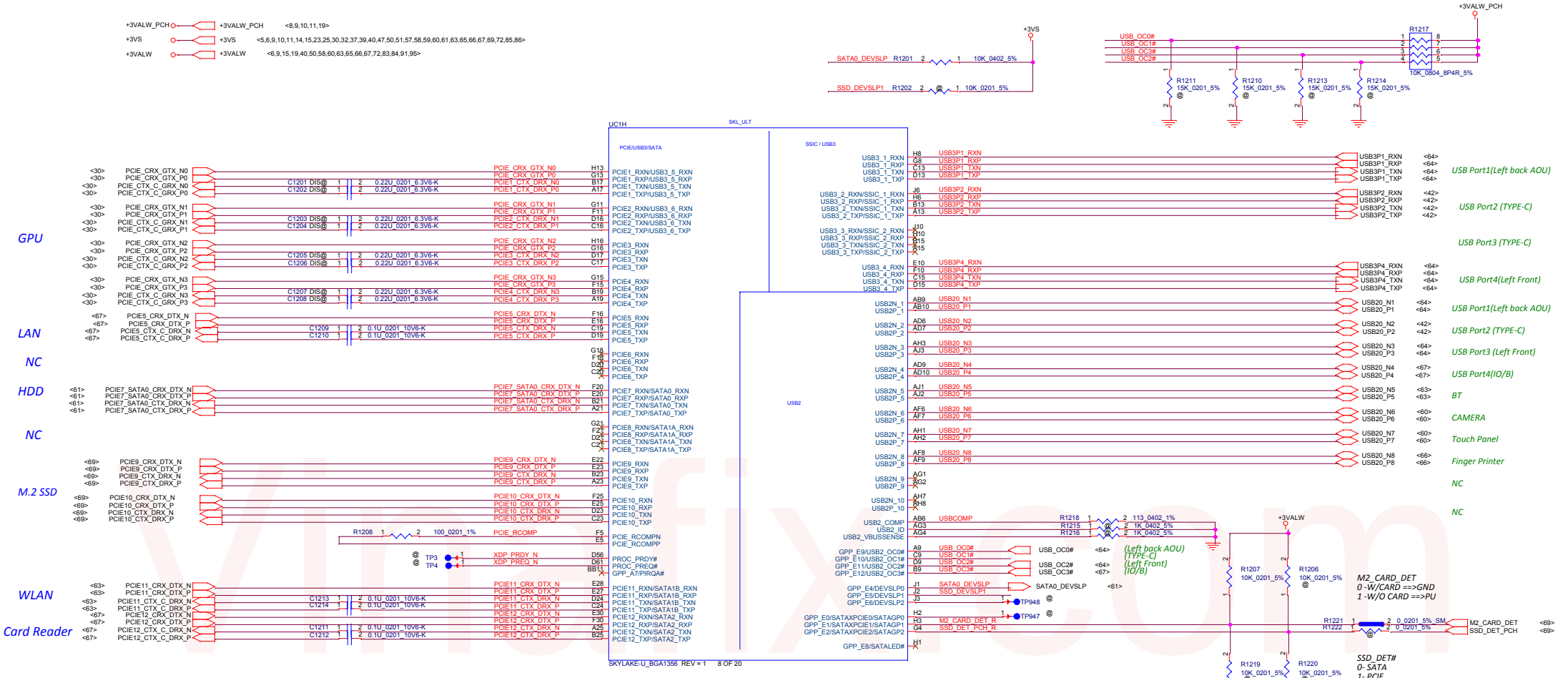

Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

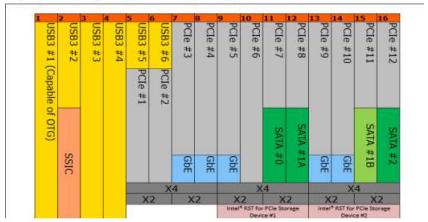

Table 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter (Sheet 1 of 2)

SKL PCH	Max Device Ports	Max Lanes	PCIe Link Config	Flexible HSIO Lanes											
				5	6	7	8	9	10	11	12	13	14	15	16
				PCIe Controller 1				PCIe Controller 2				PCIe Controller 3			
				PCI Express* Lanes											
				1	2	3	4	5	6	7	8	9	10	11	12
SKL U PCH-LP	6	12	1x4	P1				P5				P9			
			2x2	P1		P3		P5		P7		P9		P11	
			1x2+2x1	P1		P3	P4	P5		P7	P8	P9		P11	P12
			2x1+1x2	P4	P3	P1		P8	P7	P5		P12	P11	P9	
			4x1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
			1x4	P1				P5							

Reversal

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Title: KBL(H)_PCIE/ SATA/ USB3

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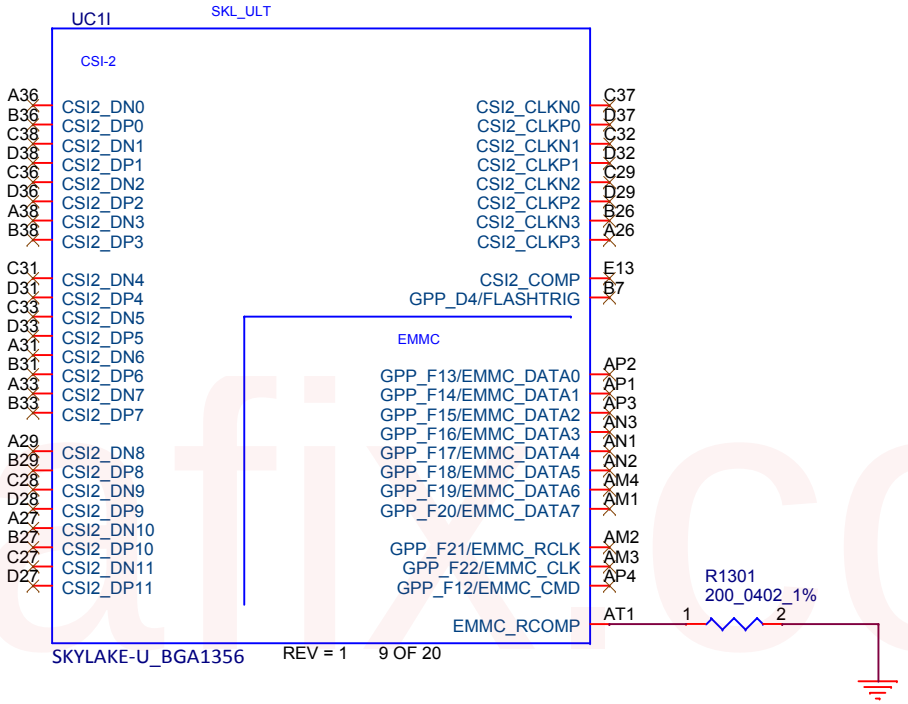

Security Classification	LC Future Center Secret Data		
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Title: **KBL(I)_CS12/ EMMC**

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+RTCBATT +RTCBATT <66,80>
+RTCVCC +RTCVCC <15,19>
+3VS +3VS <5,6,9,10,11,12,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>
+1VALW +1VALW <19,71,92>

RTC External Circuit

+RTCBATT, +RTCVCC
Trace width = 20mils

+RTCBATT
+RTCVCC
R1401 1 2 0_0402_5%_SM
near CC59 for layout
C1401 0.1U_0402_10V6-K

+RTCVCC
R1402 20K_0402_5%
PCH_RTCRST#
JCMOS1 @
C1402 1 2 1U_0402_10V6-K
R1403 20K_0402_5%
PCH_SRTCRST#
JME1 @
C1403 1 2 1U_0402_10V6-K

RTC Crystal

1. Space > 15mils
2. No trace under crystal
3. Place on oppsosit side of MCP for temp influence

PCH_RTCX1
R1404 10M_0402_5%
PCH_RTCX2
YC3 32.768KHZ_9PF_9H03280012
C1404 6.8P_0201_25V8-C
C1405 6.8P_0201_25V8-C

+3VS
R1406 10K_0402_5% UMA@
CLKREQ_PCIE4_VGA#
R1407 10K_0402_5% DIS@

+3VS
RP1401 10K_0804_8P4R_5%
CLKREQ_PCIE2_WLAN#
CLKREQ_PCIE3_LAN#
CLKREQ_PCIE1_SSD#
CLKREQ_PCIE5_CR#

UC1J SKL_ULT
CLOCK SIGNALS

HDD
M.2 SSD
<69> CLK_PCIE_SSD#
<69> CLK_PCIE_SSD
<69> CLKREQ_PCIE1_SSD#
CLK_PCIE_SSD# B42
CLK_PCIE_SSD A42
CLKREQ_PCIE1_SSD# A17
CLKOUT_PCIE_N1 D42
CLKOUT_PCIE_P1 C42
GPP_B6/SRCCLKREQ1# AR10

WLAN
<63> CLK_PCIE_WLAN#
<63> CLK_PCIE_WLAN
<63> CLKREQ_PCIE2_WLAN#
CLK_PCIE_WLAN# D41
CLK_PCIE_WLAN C41
CLKREQ_PCIE2_WLAN# AT8
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#

LAN
<67> CLK_PCIE_LAN#
<67> CLK_PCIE_LAN
<67> CLKREQ_PCIE3_LAN#
CLK_PCIE_LAN# D40
CLK_PCIE_LAN C40
CLKREQ_PCIE3_LAN# AT10
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#

GPU
<30> CLK_PCIE_VGA#
<30> CLK_PCIE_VGA
<32> CLKREQ_PCIE4_VGA#
CLK_PCIE_VGA# B40
CLK_PCIE_VGA A40
CLKREQ_PCIE4_VGA# AU8
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
GPP_B9/SRCCLKREQ4#

CR
<67> CLK_PCIE_CR#
<67> CLK_PCIE_CR
<67> CLKREQ_PCIE5_CR#
CLK_PCIE_CR# E40
CLK_PCIE_CR E38
CLKREQ_PCIE5_CR# AU7
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17
XTAL24_IN E37
XTAL24_OUT E35
XCLK_BIASREF E42
RTCX1 AM18
RTCX2 AM20
SRTCRST# AN18
RTCRST# AM16

CLKOUT_ITPXDP_N → T56
CLKOUT_ITPXDP_P → T57
SUSCLK_32K → <63> to WLAN
PCH_XTAL24_IN
PCH_XTAL24_OUT
XCLK_BIASREF
PCH_RTCX1
PCH_RTCX2
PCH_SRTCRST#
PCH_RTCRST#
+1VALW
R1409 2.71K_0402_0.5% SD00001LB1T

SKYLAKE-U_BGA1356 REV = 1 10 OF 20

Need close CPU For KBL-R U42 and KBL U22 control

PCH_XTAL24_IN
EMC L1414 KBL@ SBY100505T-300Y-N PCH_XTAL24_IN_R
SM01000JN0J
FOOTPRINT:R_0402
PCH_XTAL24_OUT
EMC L1413 KBL@ SBY100505T-300Y-N PCH_XTAL24_OUT_R
SM01000JN0J
FOOTPRINT:R_0402
R1412 1M_0201_5% KBL@
YC2 KBL@ 24MHZ_10PF_8Y24000011
GND1 GND2
C1414 12P_0201_25V8-J KBL@
C1415 12P_0201_25V8-J KBL@

Title: KBL(J)_RTC/ CLK
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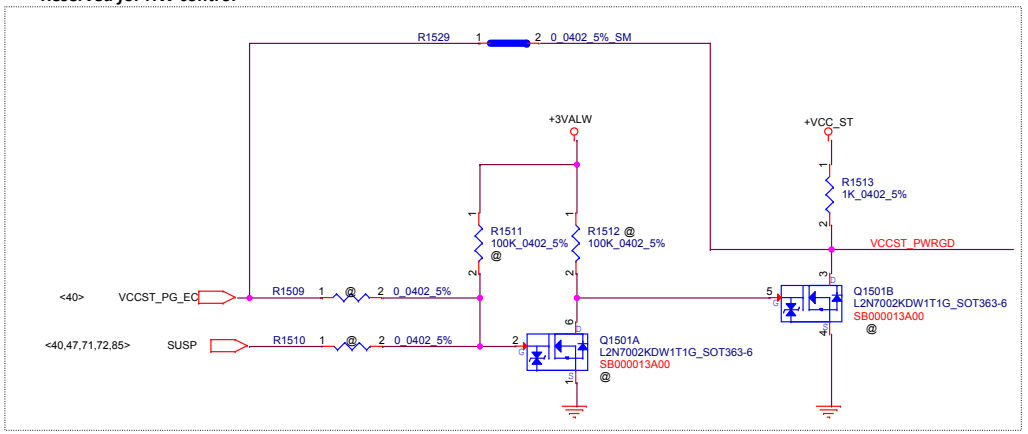
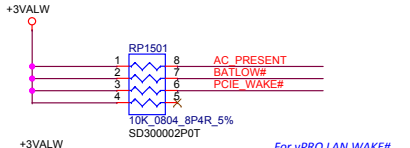
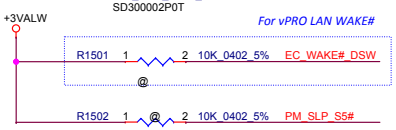
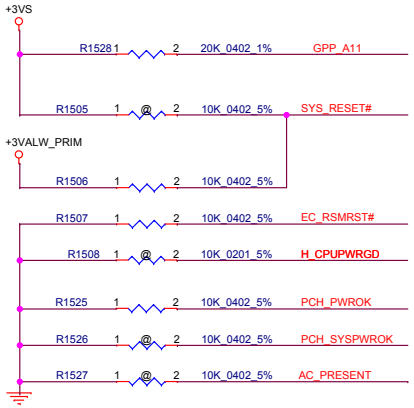
+3VALW <6,9,12,19,40,50,58,60,63,65,66,67,72,83,84,91,95>
+3VALW_PRIM <19>
+3VS <5,6,9,10,11,12,14,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>
+RTCVCC <14,19>
+VCC_ST <8,16,18,21,71,86>

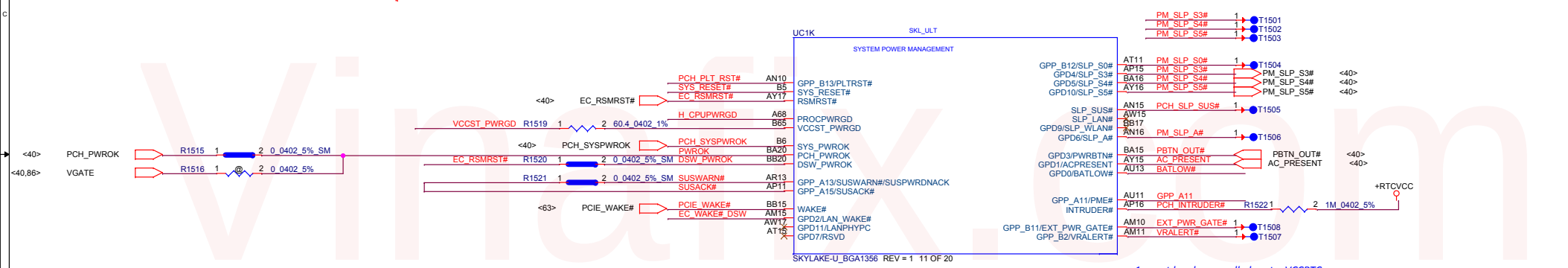
Reserved for HW control



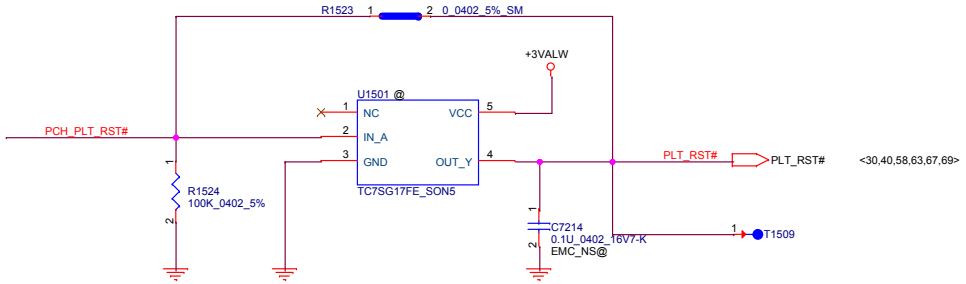








1. must be always pulled-up to VCCRTC.
2. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.



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Title: KBL(K)_SYS PM

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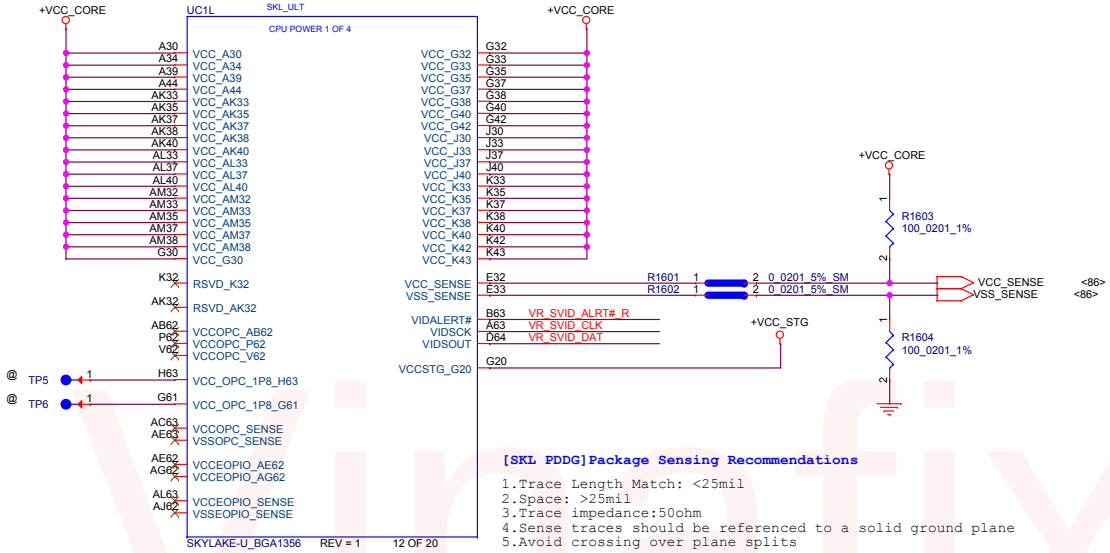
+VCC_CORE +VCC_CORE <17,27,87,90>

+VCC_ST +VCC_ST <8,15,18,21,71,86>

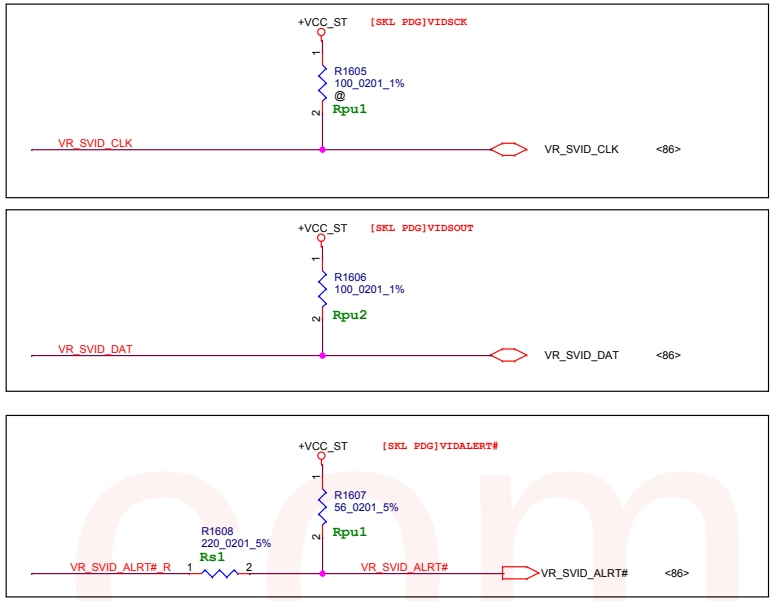


[SKL PDDG]Package Sensing Recommendations

1.Trace Length Match: <25mil
2.Space: >25mil
3.Trace impedance:50ohm
4.Sense traces should be referenced to a solid ground plane
5.Avoid crossing over plane splits

[SKL PDG]SVID

1.Alert signal must be routed between Clk and Data signals to minimize Cross-Talk.



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Title: KBL(L)_PW-VCCCORE

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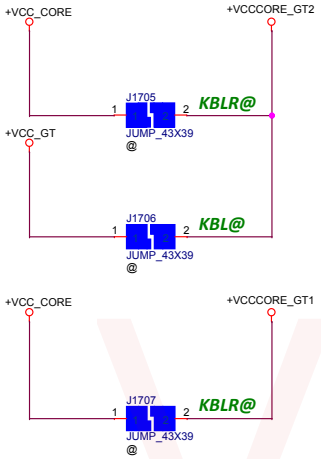
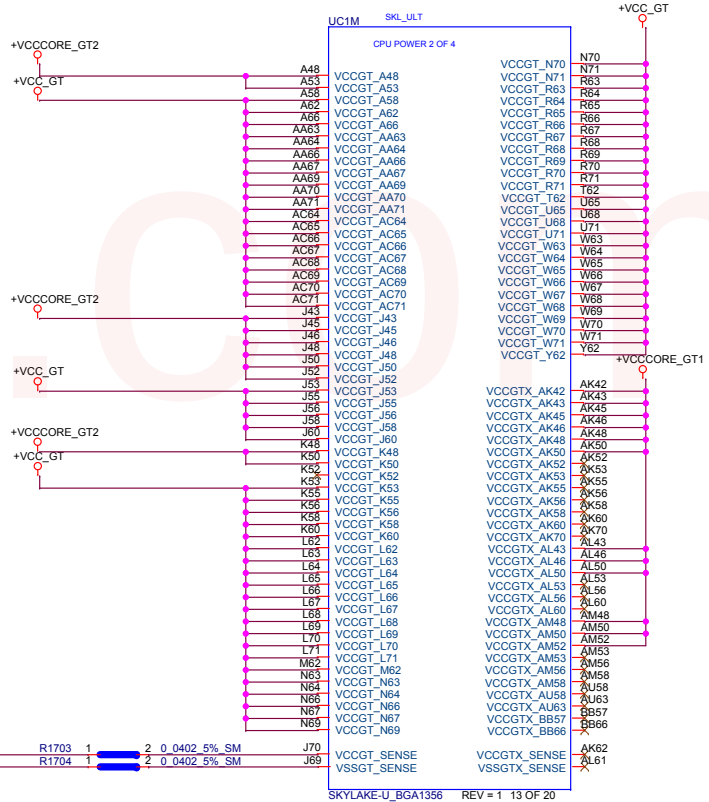
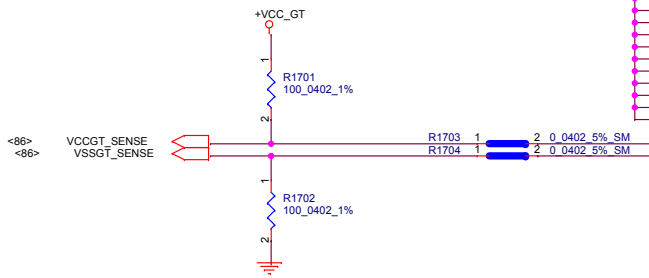
+VCC_GT — +VCC_GT <27,88,90>
+VCC_CORE — +VCC_CORE <16,27,87,90>
+VCCCORE_GT2 — +VCCCORE_GT2 <27>
+VCCCORE_GT1 — +VCCCORE_GT1 <27>

For KBL-R U42 and KBL U22 control



Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL43	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGT/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.





KBL-R U42 Only Design	Do not Connect AK52 and K52 Balls, Keep as NC
KBL-R U42 Compatible Design for (KBL-R U42/KBL U22/KBL U23e) Support	Do not Connect AK52 and K52 Balls, Keep as NC

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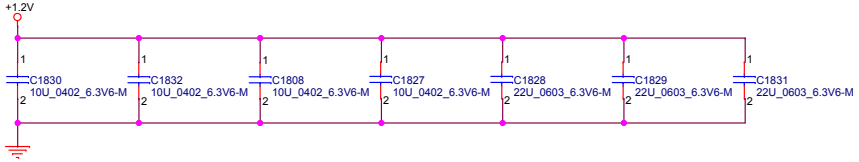
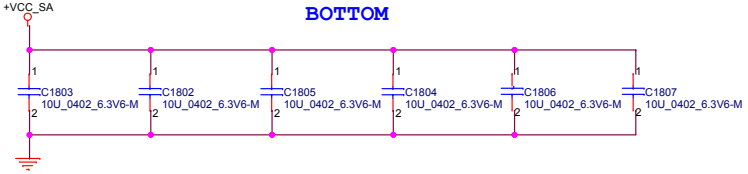
+1.2V +1.2V <6,7,23,24,25,26,85>
+VCC_IO +VCC_IO <5,11,21,71>
+VCC_SA +VCC_SA <89,90>

+VCC_STG +VCC_STG <8,16,71>
+VCC_ST +VCC_ST <8,15,16,21,71,86>

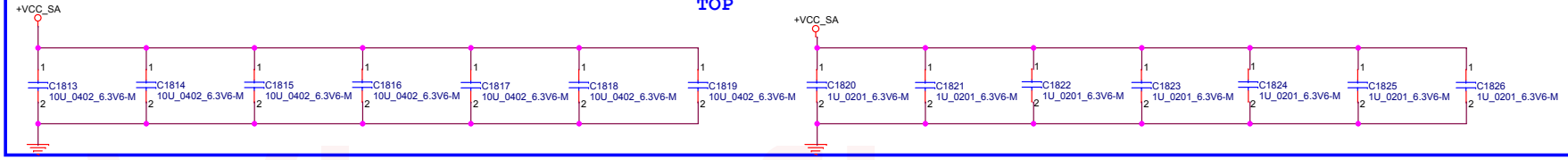
[KBL-R U4+2/KBL U2+2 Processo]VDDQ
[KBL-R U4+2/KBL U2+2 Processo]10uF x4, 22uF x3
BOTTOM

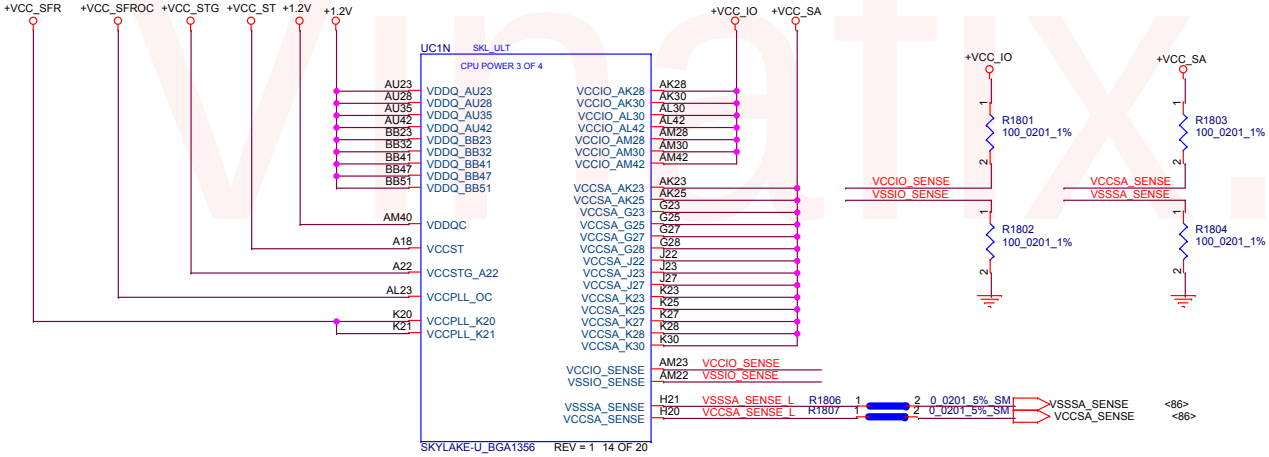


[KBL-R U4+2/KBL U2+2 ProcessoG]VCCSA
[KBL-R U4+2/KBL U2+2 Processo]10uF x6
BOTTOM



[KBL-R U4+2/KBL U2+2 ProcessoG]VCCSA
[KBL-R U4+2/KBL U2+2 Processo]10uF x7, 1uF x7
TOP





Power Rail	Description	Control
VCC	Processor IA Cores Power Rail	SVID
VccGT	Processor Graphics Power Rails	SVID
VccGTX	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
VccSA	System Agent Power Rail	SVID
VccIO	IO Power Rail	Fixed
VccST	Sustain Power Rail	Fixed
VccPLL	Processor PLLs power rail	Fixed
VDDQ	Integrated Memory Controller Power Rail	Fixed
VccOPC	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VccOPC_1P8	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VccEOPIO	Processor OPC power rail (available only in SKU's with OPC)	Fixed

[SKL PDG]VCCSTG
[SKL PDG]1uF x1
+VCC_STG
C1833 1U_0402_10V6K

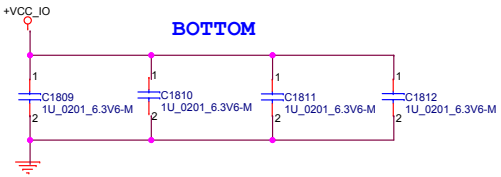
[SKL PDG]VCCST
[SKL PDG]1uF x1
Primary side cap
+VCC_ST
C1834 1U_0402_10V6K

[SKL PDG]VCCPLL
[SKL PDG]1uF x1
Primary side cap
+VCC_ST
+VCC_SFR
R1808 0_0402_5%_SM
C1835 1U_0402_10V6K

[SKL PDG]VDDQC
[SKL PDG]10uF x1
+1.2V
C1836 10U_0402_6.3V6-M

[SKL PDG]VCCPLL
[SKL PDG]1uF x1
Primary side cap
+1.2V
R1809 0_0603_5%
+VCC_SFROC
C1801 1U_0201_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processo]VCCIO
[KBL-R U4+2/KBL U2+2 Processo]1uF x4
BOTTOM



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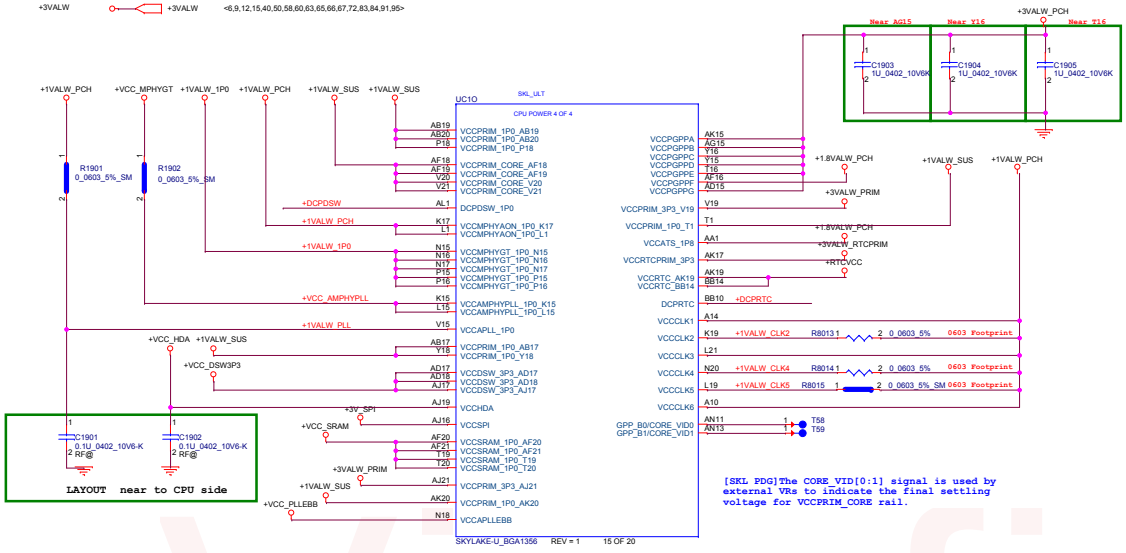
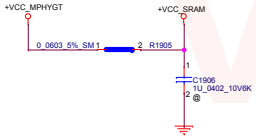
+1.2V — +1.2V <6,7,18,23,24,25,26,85>

+1VALW_PCH — +1VALW_PCH <21>
+3VALW_PCH — +3VALW_PCH <8,9,10,11,12>
+VCC_ST — +VCC_ST <8,15,16,18,21,71,86>
+3VALW_PRIM — +3VALW_PRIM <15>
+RTCVCC — +RTCVCC <14,15>
+3VALW — +3VALW <6,9,12,15,40,50,58,60,63,65,66,67,72,83,84,91,95>

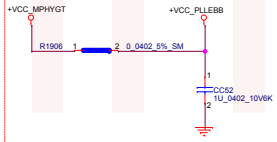
+1VALW — +1VALW <14,71,92>
+VCC_STG — +VCC_STG <8,16,18,71>
+VCC_HDA — +VCC_HDA <11>



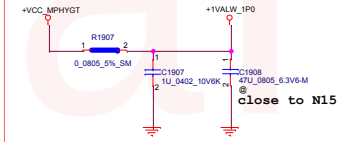
[SKL PDG]VccSRAM
[SKL PDG]Close AF20,
Placement type:Edge<10mm(394mil)
[SKL PDG]1uF x1
SRAM Primary Well 1.0 V. Dedicated SRAM rail and can have on board power down gate control.



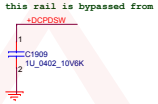
[SKL PDG]VccAPLLEBB
[SKL PDG]Close N18,
Placement type:Edge<3mm(118mil)
[SKL PDG]1uF x1



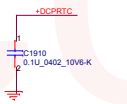
[SKL PDG]VccMPHYGT
[SKL PDG]1uF x1
[SKL PDG]47uF x1
[SKL PDG]Close N15,
Placement type:Edge<3mm(118mil)
[SKL PDG]Close N15,
Placement type:Edge<10mm(394mil)
VccMPHYGT(Mod PHY Externally Gated Primary 1.0 V: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.)



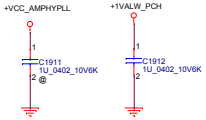
[SKL PDG]DcpDSW
[SKL PDG]Close AL1,
Placement type:Edge<3mm(118mil)
[SKL PDG]1uF x1
Deep Sx Well 1.0 V: This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.



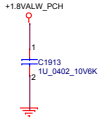
[SKL PDG]DcpRTC
[SKL PDG]Close BB10,
Placement type:Edge<3mm(118mil)
[SKL PDG]0.1uF x1
RTC de-coupling capacitor only. This rail should NOT be driven.



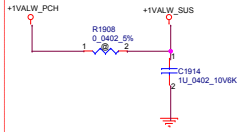
[SKL PDG]VccMPHYAON
[SKL PDG]Close K17,
Placement type:Edge<3mm(118mil)
[SKL PDG]1uF x1
Mod PHY Always On Primary 1.0 V: Always on primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic



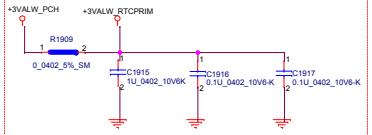
[SKL PDG]VccATS
[SKL PDG]Close AA1,
Placement type:Edge<10mm(394mil)
[SKL PDG]1uF x1
Thermal Sensor Primary Well 1.8 V



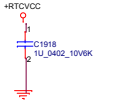
[SKL PDG]VCCPRIM
[SKL PDG]Close AB19,
Placement type:Edge<10mm(394mil)
[SKL PDG]1uF x1
Primary Well 1.0 V: For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.



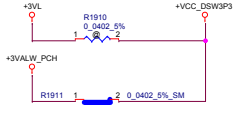
[SKL PDG]VccRTCPRIM
[SKL PDG]Close AK17,
Placement type:Edge<3mm(118mil)
[SKL PDG]1uF x1,0.1uF x2
RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

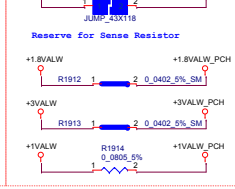


[SKL PDG]VccRTC
[SKL PDG]Close AK19,
Placement type:Edge<3mm(118mil)
[SKL PDG]1uF x1
RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

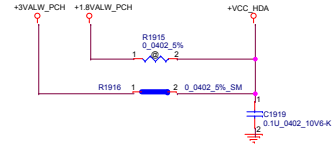


[SKL PDG]VccDSW
Deep Sx Well for GPD GPIOs and USB2

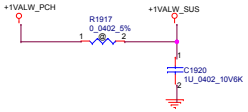




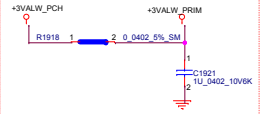
[SKL PDG]VccHDA
[SKL PDG]Close AJ19,
Placement type:Edge<10mm(394mil)
[SKL PDG]1uF x1
HD Audio Power 3.3 V, 1.8 V, 1.5 V. For Intel High Definition Audio.



[SKL PDG]VccPRIM_Core
[SKL PDG]Close AF18,
Placement type:Edge<10mm(394mil)
[SKL PDG]1uF x1
Core Logic Primary Well: This rail scales from 0.85 V to 1.0 V.



[SKL PDG]VCCPRIM
[SKL PDG]Close V19,
Placement type:Edge<3mm(118mil)
[SKL PDG]1uF x1
Primary Well 3.3 V



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

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Title: KBL(O)_PW-OTHERS

Size: Custom | Document Number: ER480 NM-B421 | Rev: 0.2

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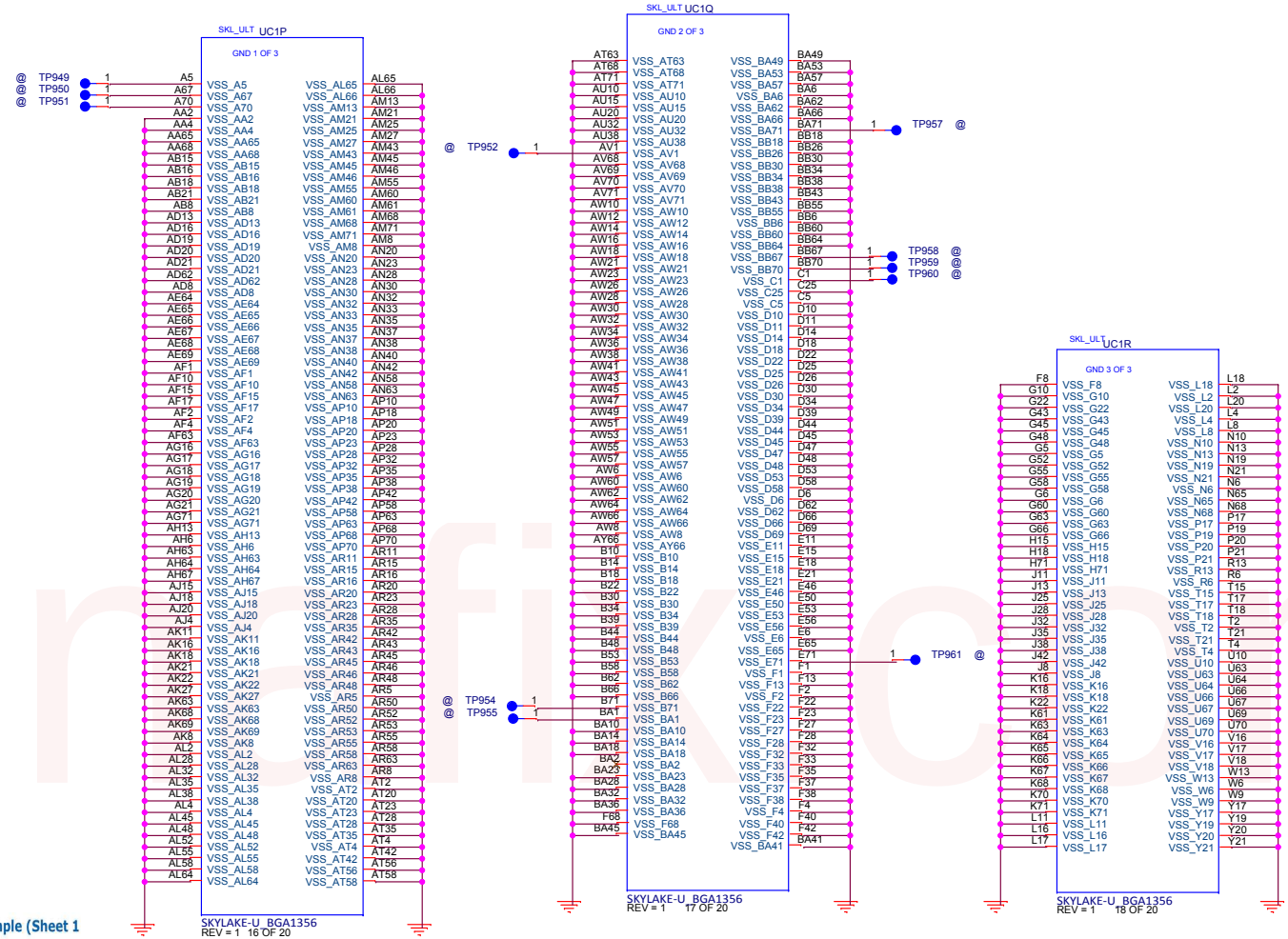

Kaby Lake R Processor Corner NCTF Motherboard Test Point Example (Sheet 1 of 2)

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	

Kaby Lake R Processor Corner NCTF Motherboard Test Point Example (Sheet 2 of 2)

Pin Number	Pin Name	Description	Corner
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: KBL(P/Q/R)_VSS

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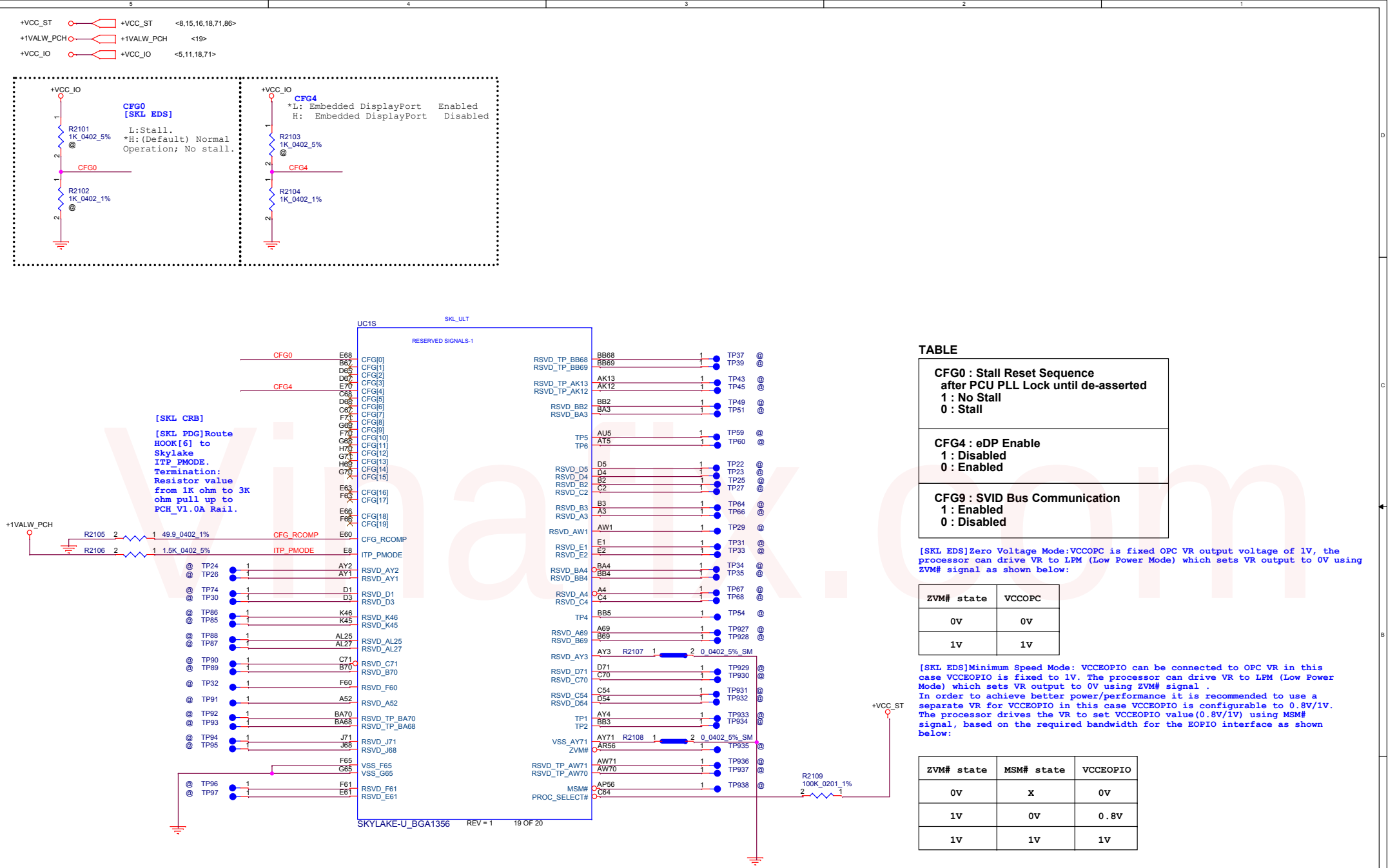

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled

[SKL EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM# state	VCCOPC
0V	0V
1V	1V

[SKL EDS]Minimum Speed Mode: VCCEOPIO can be connected to OPC VR in this case VCCEOPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal .
In order to achieve better power/performance it is recommended to use a separate VR for VCCEOPIO in this case VCCEOPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEOPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EOPIO interface as shown below:

ZVM# state	MSM# state	VCCEOPIO
0V	X	0V
1V	0V	0.8V
1V	1V	1V

Title: KBL(S)_CFG/ RSVD

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

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Need close CPU For KBL-R U42 and KBL U22 control

PCH_XTAL24_IN_NEW — EMC — L2202 — KBLR@ — SBY100505T-300Y-N — PCH_XTAL24_IN_NEW_R

SM01000JN0J

FOOTPRINT:R_0402

PCH_XTAL24_OUT_NEW — EMC — L2203 — KBLR@ — SBY100505T-300Y-N — PCH_XTAL24_OUT_NEW_R

SM01000JN0J

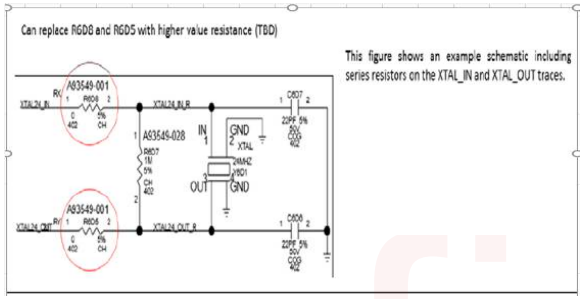
FOOTPRINT:R_0402

R2808
1M_0201_5%
KBLR@

YC1 KBLR@
24MHZ_10PF_8Y24000011
GND1 GND2

C2801
12P_0201_25V8-J
KBLR@

C2802
12P_0201_25V8-J
KBLR@



UC1T SKL_ULT

SPARE

@ TP98	1	AW69	RSVD_AW69	RSVD_F6	F6	1	TP106 @
@ TP99	1	AW68	RSVD_AW68	RSVD_E3	E3	PCH_XTAL24_IN_NEW	
@ TP100	1	AU56	RSVD_AU56	RSVD_C11	C11	1	TP108 @
@ TP101	1	AW48	RSVD_AW48	RSVD_B11	B11	1	TP109 @
	PCH_XTAL24_OUT_NEW	C7	RSVD_C7	RSVD_A11	A11	1	TP110 @
@ TP103	1	U12	RSVD_U12	RSVD_D12	D12	1	TP111 @
@ TP104	1	U11	RSVD_U11	RSVD_C12	C12	1	TP112 @
@ TP105	1	H11	RSVD_H11	RSVD_F52	F52	1	TP113 @

SKYLAKE-U_BGA1356
REV = 1 20 OF 20

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: KBL(T)_RSVD

Size: B | Document Number: EE480 NM-B421 | Rev: 0.2

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+3VS +3VS <5,6,9,10,11,12,14,15,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>

+2.5V +2.5V <6,24,25,26,94>

+1.2V +1.2V <6,7,18,24,25,26,85>

+0.6VS +0.6VS <24,25,26,85>

<6,7> M_A_DQ[63:0]

<6,7> -M_A_DQS[7:0]

<6,7> M_A_DQS[7:0]

<6> M_A_A[16:0]

JDIMM1A

ARGOS_D4AR0-26005-1P40

ME@

JDIMM1B

ARGOS_D4AR0-26005-1P40

ME@

RF

C2307 0.1U_0402_16V7-K EMC_NS@

C2303 0.1U_0402_10V7-K

C2304 2.2U_0402_6.3V6-M

[KBL PDG]VDDSPD

[KBL PDG] EE 0.1uF x1, 2.2uF x1.

Place decoupling cap close to DIMM

R2301 240_0402_1%

C2301 2.2U_0402_6.3V6-M @

C2302 0.1U_0402_10V7-K @

R2302 0_0402_5%_SM

<9,25,65> PM_SMB_CLK

PM_SMB_CLK

VDDSPD_1

PM_SMB_DAT

<9,25,65>

R2303 10K_0402_5% @

R2304 0_0402_5%_SM

R2305 10K_0402_5% @

R2306 0_0402_5%_SM

R2307 10K_0402_5% @

R2308 0_0402_5%_SM

SA0_CHA_P

SA1_CHA_P

SA2_CHA_P

R2309 1K_0402_1%

R2310 2_0402_1%

R2311 24.9_0402_1%

R2312 1K_0402_1%

C2305 0.022U_0402_25V7-K

C2306 0.1U_0402_16V7-K @

<6> M_A_VREF_CA_CPU

M_VREF_CA_DIMMA

SPD Address = 0H

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Title: DDR4 CH-A PRIMARY

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+2.5V +2.5V <6,23,25,26,94>

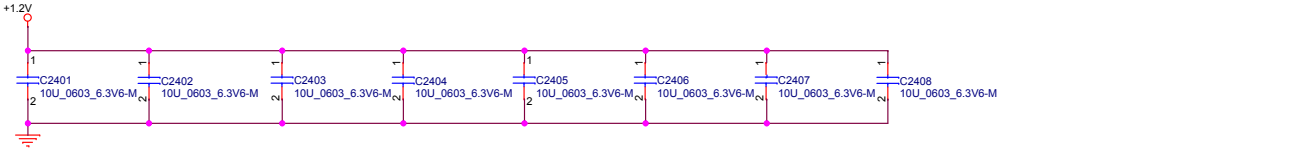
+1.2V +1.2V <6,7,18,23,25,26,85>

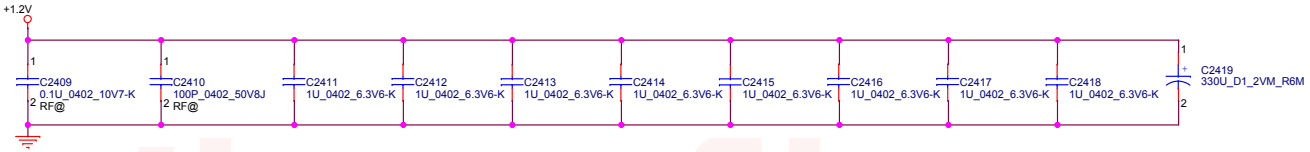
+0.6VS +0.6VS <23,25,26,85>

[KBL PDG]VDDQ

[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins. 330uF placeholder

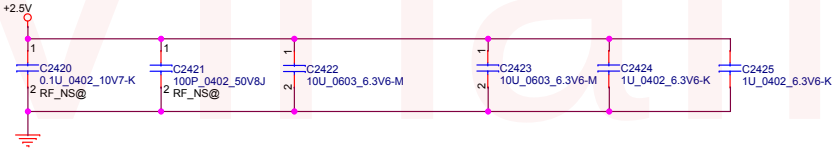




[KBL PDG]VPP

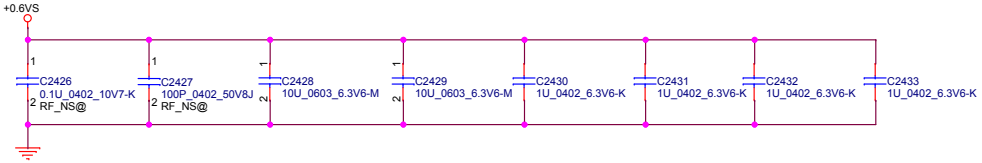
[KBL PDG] EE 10uF x2, 1uF x2.

Place decoupling cap on DRAM side.



[KBL PDG]VTT

[KBL PDG] EE 10uF x2, 1uF x4.



Place decoupling on the VTT plane close to SODIMM

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DDR4 CH-A PRIMARY_P

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

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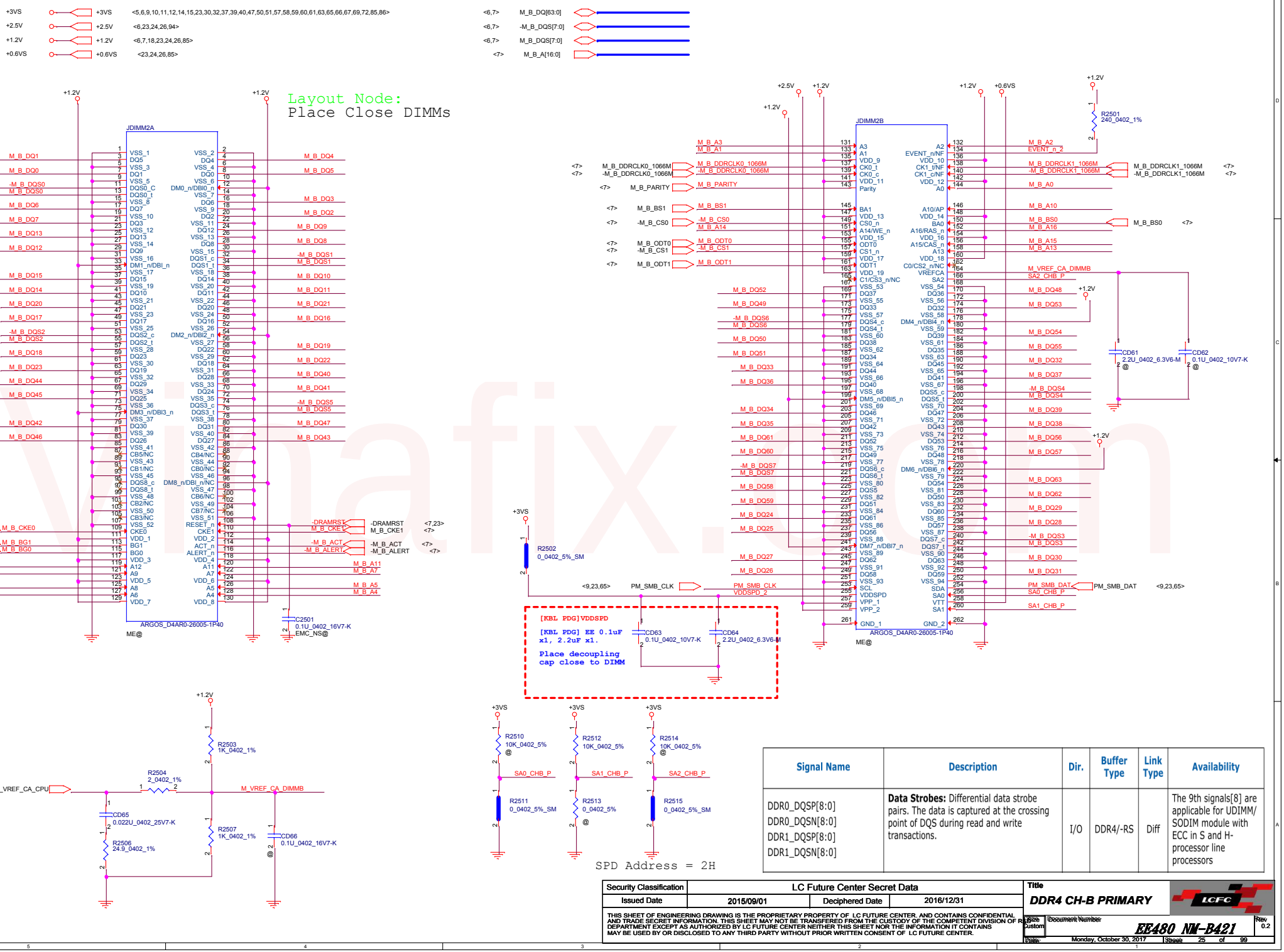

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **DDR4 CH-B PRIMARY**

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+2.5V +2.5V <6,23,24,25,94>

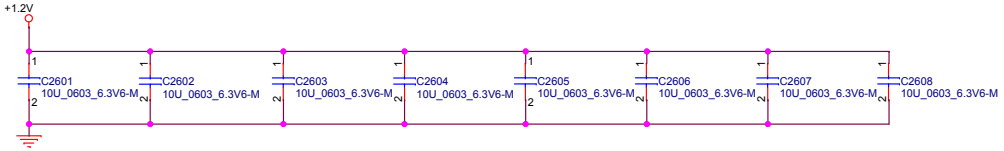
+1.2V +1.2V <6,7,18,23,24,25,85>

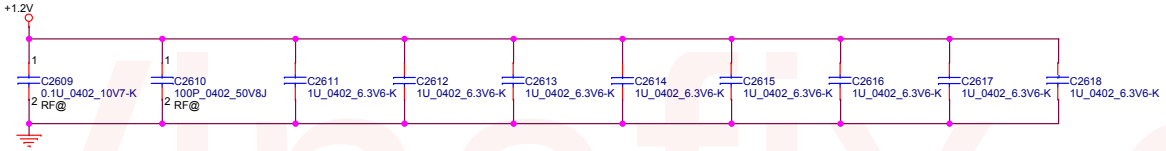
+0.6VS +0.6VS <23,24,25,85>

[KBL PDG]VDDQ

[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

Place 10uF/1uF decoupling cap, 4
near each side of the DIMM
connector close to VDD pins.
330uF placeholder

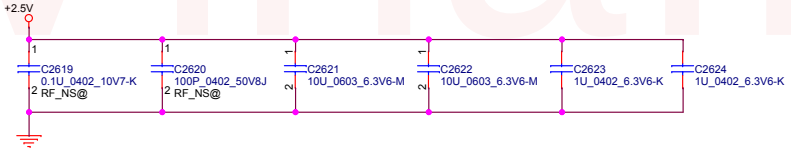




[KBL PDG]VPP

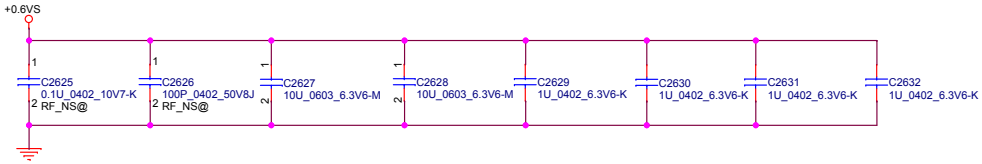
[KBL PDG] EE 10uF x2, 1uF x2.

Place decoupling cap on DRAM side.



[KBL PDG]VTT

[KBL PDG] EE 10uF x2, 1uF x4.



Place decoupling on the VTT plane close to SODIMM

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DDR4 CH-B PRIMARY_P

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

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+VCC_CORE +VCC_CORE <16,17,87,90> +VCC_GT +VCC_GT <17,88,90> +VCCCORE_GT2 +VCCCORE_GT2 <17>

+VCCCORE_GT1 +VCCCORE_GT1 <17>

[KBL-R U4+2/KBL U2+2 Processor]VCC

[KBL-R U4+2/KBL U2+2 Processor]22uF x9,10uF x8,1uF,47uF x8

BOTTOM

+VCC_CORE

C2719 22U_0603_6.3V6-M, C2701 22U_0603_6.3V6-M, C2702 22U_0603_6.3V6-M, C2703 22U_0603_6.3V6-M, C2704 22U_0603_6.3V6-M, C2705 22U_0603_6.3V6-M, C2706 22U_0603_6.3V6-M, C2707 22U_0603_6.3V6-M, C2708 22U_0603_6.3V6-M

+VCC_CORE

C2781 10U_0402_6.3V6-M, C2775 10U_0402_6.3V6-M, C2776 10U_0402_6.3V6-M, C2777 10U_0402_6.3V6-M, C2778 10U_0402_6.3V6-M, C2779 10U_0402_6.3V6-M, C2780 10U_0402_6.3V6-M, C2782 10U_0402_6.3V6-M

+VCC_CORE

C2783 22U_0603_6.3V6-M, C2784 22U_0603_6.3V6-M, C2785 22U_0603_6.3V6-M, C2786 22U_0603_6.3V6-M, C2787 22U_0603_6.3V6-M, C2788 22U_0603_6.3V6-M, C2789 22U_0603_6.3V6-M, C2790 22U_0603_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]10uF x7,1uF x31

TOP

+VCC_CORE

C2720 10U_0402_6.3V6-M, C2721 10U_0402_6.3V6-M, C2722 10U_0402_6.3V6-M, C2723 10U_0402_6.3V6-M, C2724 10U_0402_6.3V6-M, C2725 10U_0402_6.3V6-M, C2726 10U_0402_6.3V6-M

+VCC_CORE

C2747 1U_0201_6.3V6-M

+VCC_CORE

C2709 1U_0201_6.3V6-M, C2710 1U_0201_6.3V6-M, C2711 1U_0201_6.3V6-M, C2712 1U_0201_6.3V6-M, C2713 1U_0201_6.3V6-M, C2714 1U_0201_6.3V6-M, C2715 1U_0201_6.3V6-M, C2716 1U_0201_6.3V6-M, C2717 1U_0201_6.3V6-M, C2718 1U_0201_6.3V6-M

+VCC_CORE

C2727 1U_0201_6.3V6-M, C2728 1U_0201_6.3V6-M, C2729 1U_0201_6.3V6-M, C2730 1U_0201_6.3V6-M, C2731 1U_0201_6.3V6-M, C2732 1U_0201_6.3V6-M, C2733 1U_0201_6.3V6-M, C2734 1U_0201_6.3V6-M, C2735 1U_0201_6.3V6-M, C2736 1U_0201_6.3V6-M

+VCC_CORE

C2737 1U_0201_6.3V6-M, C2738 1U_0201_6.3V6-M, C2739 1U_0201_6.3V6-M, C2740 1U_0201_6.3V6-M, C2741 1U_0201_6.3V6-M, C2742 1U_0201_6.3V6-M, C2743 1U_0201_6.3V6-M, C2744 1U_0201_6.3V6-M, C2745 1U_0201_6.3V6-M, C2746 1U_0201_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]1uF XBOTTOM

+VCCCORE_GT1

C27113 1U_0201_6.3V6-M, C27112 1U_0201_6.3V6-M, C27115 1U_0201_6.3V6-M, C27114 1U_0201_6.3V6-M, C27116 1U_0201_6.3V6-M, C27117 1U_0201_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]VCCGT

[KBL-R U4+2/KBL U2+2 Processor]10uF x10,1uF x12

TOP

+VCC_GT

C2752 10U_0402_6.3V6-M, C2753 10U_0402_6.3V6-M, C2754 10U_0402_6.3V6-M, C2755 10U_0402_6.3V6-M, C2756 10U_0402_6.3V6-M, C2792 10U_0402_6.3V6-M

+VCC_GT

C2757 10U_0402_6.3V6-M, C2758 10U_0402_6.3V6-M, C2759 10U_0402_6.3V6-M, C2760 10U_0402_6.3V6-M, C2761 10U_0402_6.3V6-M, C2791 10U_0402_6.3V6-M

+VCC_GT

C2762 1U_0201_6.3V6-M, C2763 1U_0201_6.3V6-M, C2764 1U_0201_6.3V6-M, C2765 1U_0201_6.3V6-M, C2766 1U_0201_6.3V6-M, C2767 1U_0201_6.3V6-M, C2793 1U_0201_6.3V6-M

+VCC_GT

C2768 1U_0201_6.3V6-M, C2769 1U_0201_6.3V6-M, C2770 1U_0201_6.3V6-M, C2771 1U_0201_6.3V6-M, C2773 1U_0201_6.3V6-M, C2774 1U_0201_6.3V6-M, C2794 1U_0201_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]10uF x7,47uF x3

BOTTOM

+VCC_GT

C27101 22U_0603_6.3V6-M, C27100 22U_0603_6.3V6-M, C2799 22U_0603_6.3V6-M, C2795 22U_0603_6.3V6-M, C2798 22U_0603_6.3V6-M, C2796 22U_0603_6.3V6-M, C2797 22U_0603_6.3V6-M

+VCC_GT

C27102 22U_0603_6.3V6-M, C27103 22U_0603_6.3V6-M, C27104 22U_0603_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]1uF X5

BOTTOM

+VCCCORE_GT2

C27107 1U_0201_6.3V6-M, C27105 1U_0201_6.3V6-M, C27108 1U_0201_6.3V6-M, C27106 1U_0201_6.3V6-M, C27109 1U_0201_6.3V6-M

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: VCC_CORE & VCC_GT CAP

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **BLANK**

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **BLANK**

Size	Document Number	Rev
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+3VS <5,6,9,10,11,12,14,15,23,25,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>

+3VS_VGA <32,37,38,39,91>

+1.8VS_VGA <32,34,38>

TABLE of GPU (UV3001)		
Vendor	LCFC P/N	Description
AMD(R17M-P1-70)	SA00008ED00	S IC 216-0905004 C0 FCBGA 769P GPU
AMD(R17M-P1-50)	SA00008DT00	S IC 216-0905018 C3 FCBGA 769P GPU

DIS@ support GEN3

<12> PCIE_CTX_C_GRX_N[0..3] PCIE_CTX_C_GRX_N[0..3]

<12> PCIE_CTX_C_GRX_P[0..3] PCIE_CTX_C_GRX_P[0..3]

<12> PCIE_CRX_GTX_N[0..3] PCIE_CRX_GTX_N[0..3]

<12> PCIE_CRX_GTX_P[0..3] PCIE_CRX_GTX_P[0..3]

UV3001B@ symbol2

PCIE_CTX_C_GRX_P0	AT41	PCIE_RX0P	PCIE_TX0P	AV35	PCIE_CRX_C_GTX_P0	C3008	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P0
PCIE_CTX_C_GRX_N0	AT40	PCIE_RX0N	PCIE_TX0N	AU35	PCIE_CRX_C_GTX_N0	C3001	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N0
PCIE_CTX_C_GRX_P1	AR41	PCIE_RX1P	PCIE_TX1P	AU38	PCIE_CRX_C_GTX_P1	C3002	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P1
PCIE_CTX_C_GRX_N1	AR40	PCIE_RX1N	PCIE_TX1N	AU39	PCIE_CRX_C_GTX_N1	C3003	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N1
PCIE_CTX_C_GRX_P2	AP41	PCIE_RX2P	PCIE_TX2P	AR37	PCIE_CRX_C_GTX_P2	C3004	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P2
PCIE_CTX_C_GRX_N2	AP40	PCIE_RX2N	PCIE_TX2N	AR38	PCIE_CRX_C_GTX_N2	C3005	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N2
PCIE_CTX_C_GRX_P3	AM41	PCIE_RX3P	PCIE_TX3P	AN37	PCIE_CRX_C_GTX_P3	C3006	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_P3
PCIE_CTX_C_GRX_N3	AM40	PCIE_RX3N	PCIE_TX3N	AN38	PCIE_CRX_C_GTX_N3	C3007	DIS@ 1	2 0.22U_0402_10V6-K	PCIE_CRX_GTX_N3
	AL41	PCIE_RX4P	PCIE_TX4P	AL37					
	AL40	PCIE_RX4N	PCIE_TX4N	AL38					
	AK41	PCIE_RX5P	PCIE_TX5P	AJ37					
	AK40	PCIE_RX5N	PCIE_TX5N	AJ38					
	AJ41	PCIE_RX6P	PCIE_TX6P	AG37					
	AJ40	PCIE_RX6N	PCIE_TX6N	AG38					
	AH41	PCIE_RX7P	PCIE_TX7P	AE37					
	AH40	PCIE_RX7N	PCIE_TX7N	AE38					
<14> CLK_PCIE_VGA	AV33	PCIE_REFCLKP	PERSTB	AV41	PLT_RST_VGA#				
<14> CLK_PCIE_VGA#	AU33	PCIE_REFCLKN	PX_EN	AC41	PX_EX	R3006 2	DIS@ 1	1K_0402_5%	
			PCIE_ZVSS	AU41	PCIE_ZVSS	R3001 1	DIS@ 2	200_0402_1%	

REV 0.91

216-0905018-C3_FCBGA769

+3VS_VGA

R3005 10K_0402_5% @

R3007 100K_0402_5% DIS@

JTAG

+1.8VS_VGA

R3016 10K_0402_5% DIS@

R3015 10K_0402_5% DIS@

TV52 TV53

R3014 1 DIS@ 2 33_0402_5%

R3013 1 DIS@ 2 33_0402_5%

UV3001A@ symbol1

AA38	BP_0	JTAG_TDO	AF41	JTAG_TDO	TV48
AA37	BP_1	JTAG_TDI	AD40	JTAG_TDI	TV49
		JTAG_TMS	AD41	JTAG_TMS	TV50
		JTAG_TCK	AE41	JTAG_TCK	TV51
B2	TEST6	TESTEN	AE40	TESTEN	
		JTAG_TRSTB	AF40	JTAG_TRSTB	

REV 0.91

216-0905018-C3_FCBGA769

R3012 10K_0402_5% DIS@

+3VS_VGA

R3009 1K_0402_5% @

R3008 1K_0402_5% DIS@

+3VS_VGA

R3010 10K_0402_5% DIS@

R3011 1K_0402_5% @

<15,40,58,63,67,69> PLT_RST#

R3004 1 2 0_0402_5%_SM

<10> DGPU_HOLD_RST#

R3002 0_0402_5% 1 @ 2

+3VS

U3003

B		VCC	5
A			
GND		Y	4

74LVC1G08GW_SOT353-1-5

DIS@

SA00005U300

PD 10K at GPU Pin

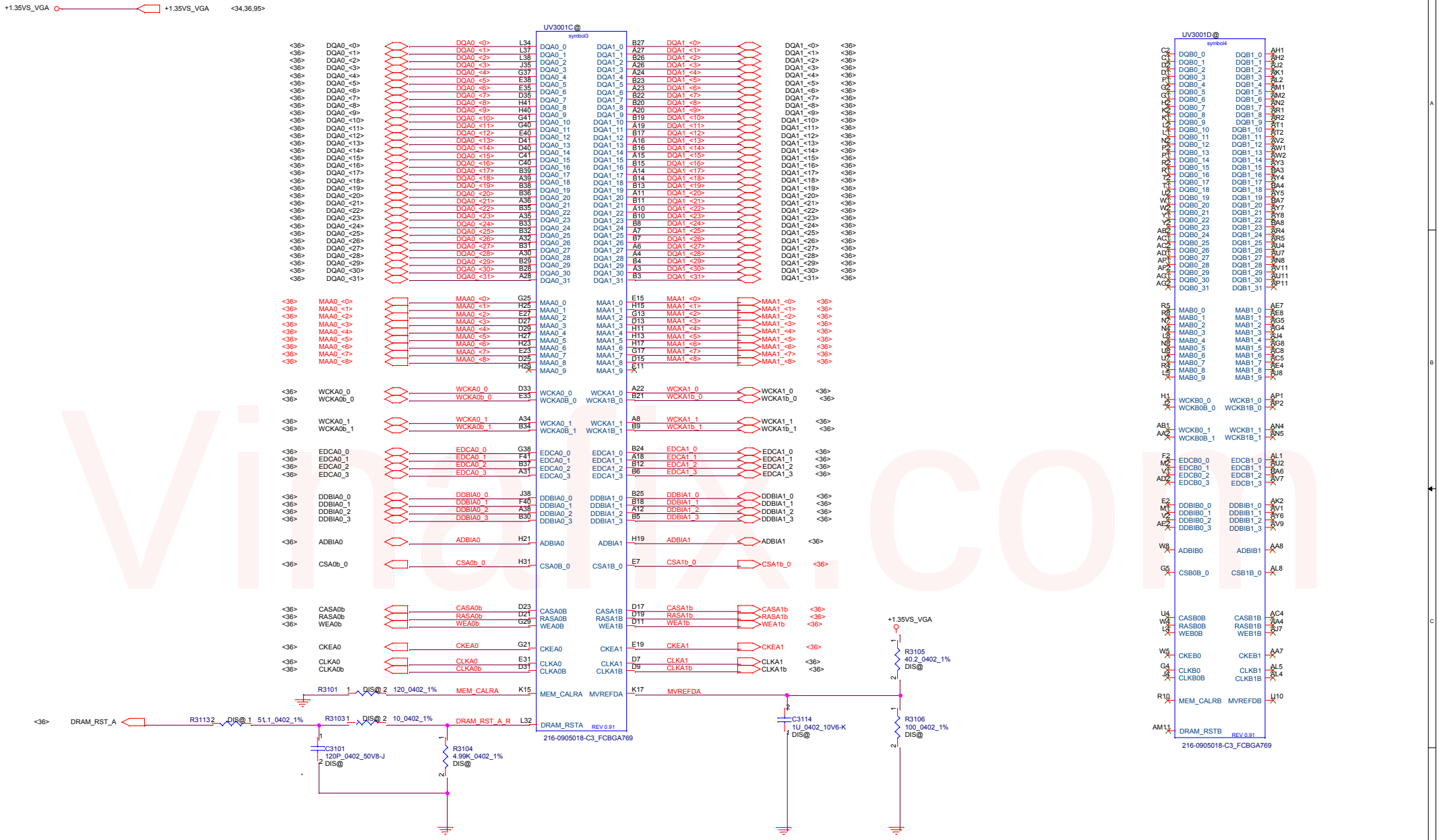
PLT_RST_VGA# <32,91>

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-P1-50(A)_PCIE

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

Date: Monday, October 30, 2017 | Sheet 30 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-P1-50(B)_VRAM I/F

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

Date: Monday, October 30, 2017 | Sheet 34 of 99

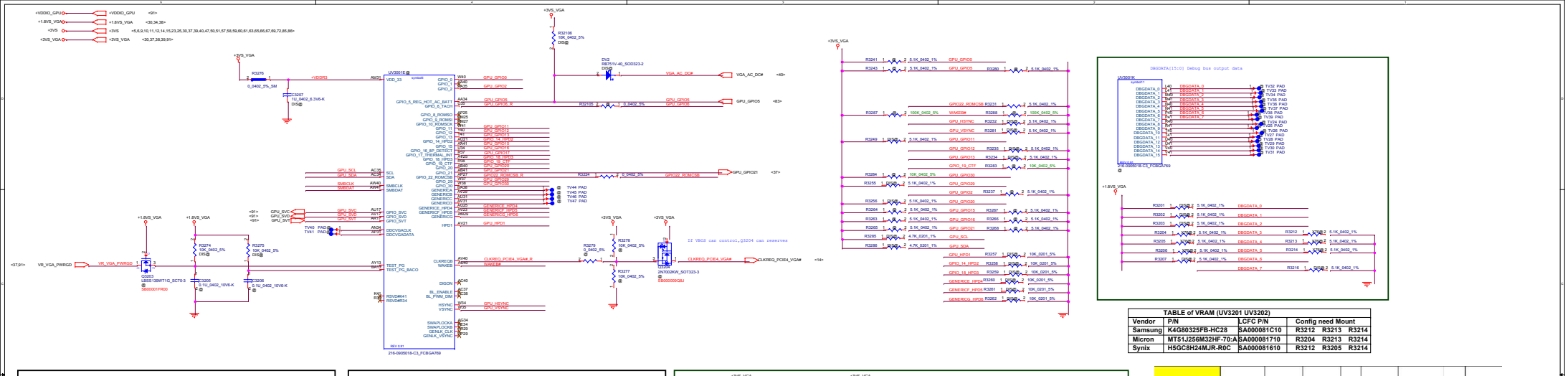
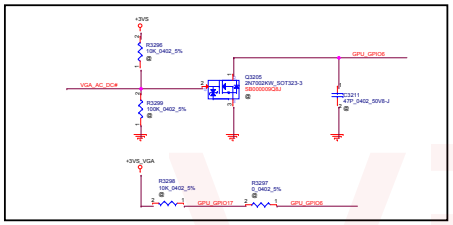
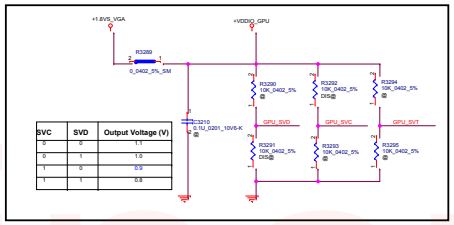
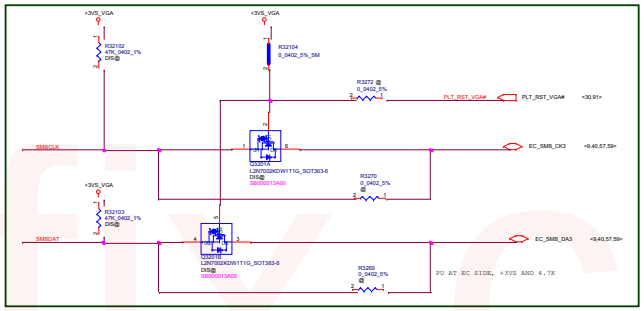


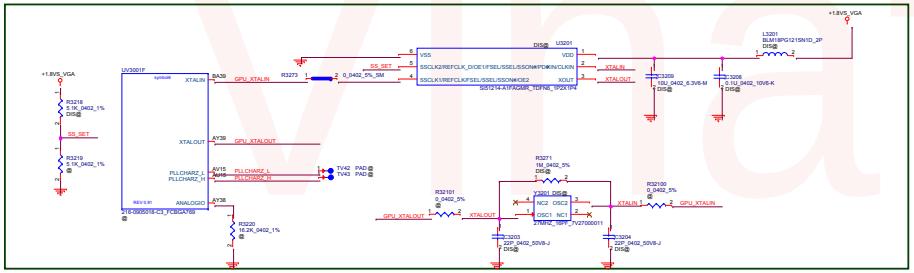
TABLE of VRAM (UV3201 UV3202)			
Vendor	P/N	LCFC P/N	Config need Mount
Samsung	K4G80325FB-HC28	SA000081C10	R3212 R3213 R3214
Micron	MT51J256M32HF-70:A	SA000081710	R3204 R3213 R3214
Synix	H5GC8H24MJR-R0C	SA000081610	R3212 R3205 R3214

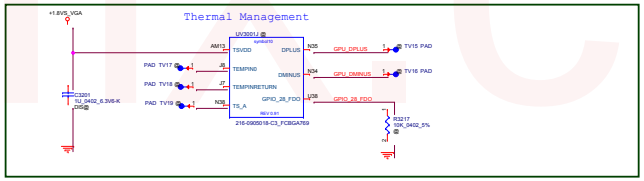




SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8







BOARD_CONFIG[2:0] =DBGDATA_5/4/3	Memory Type	Configuration	Speed	Die	Channel Size	Vendor P/N	Voltage	SMT quantity
ID	[2:0]	EX: Samsung-GDDR5	256M x 32 4PCS,	8.0 Gbps	B-die	4GB	K4G80325FB-HC25	1.55 V	4 pcs
0	000	Samsung-GDDR5	256M x 32 2PCS	6.0 Gbps	B-die	2GB	K4G80325FB-HC28	1.35V	2 pcs
1	001	Micron-GDDR5	256M x 32 2PCS	6.0 Gbps	A-die	2GB	MT51J256M32HF-70:A	1.35V	2 pcs
2	010	SK hynix-GDDR5	256M x 32 2PCS	6.0 Gbps	Deneb-die.	2GB	H5GC8H24MJR-R0C	1.35V	2 pcs

AUD_PORT_CONN [2:0]	DBGDATA_2 DBGDATA_1 DBGDATA_0	111: No usable endpoints 110: One usable endpoint 101: Two usable endpoints 100: Three usable endpoints 011: Four usable endpoints 010: Five usable endpoints 001: Six usable endpoints 000: All endpoints are usable	0 (Internal pull-down)	Design dependent, see description. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

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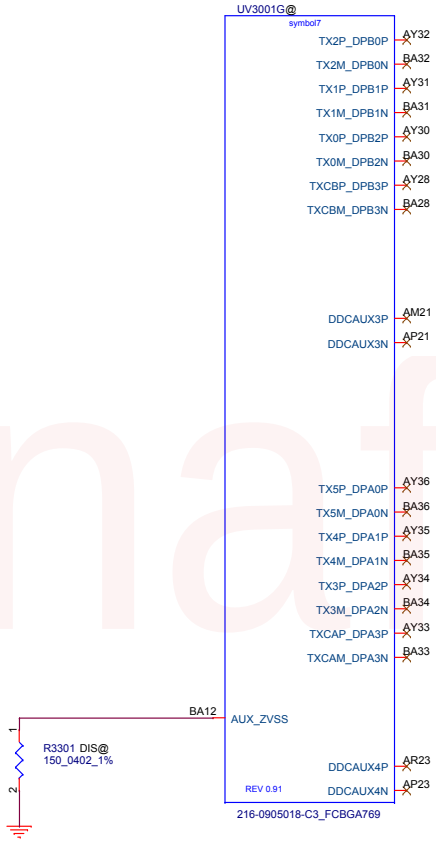
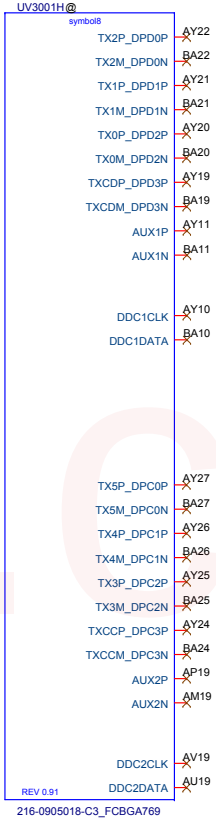
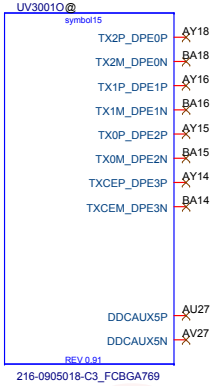
Title: R17M-P1-50(C/D)_GPIO

Size: C | Document Number: KX480 MB-PA31 | Rev: 0.2

Date: Monday, October 30, 2017 | Sheet: 49 of 69







If this interface is not used, all signal outputs can be unconnected. AUX_ZVSS should always be connected.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	R17M-P1-50(E)_DIGITAL OU	
Size: Custom	Document Number: EE480 NM-B421	Rev: 0.2
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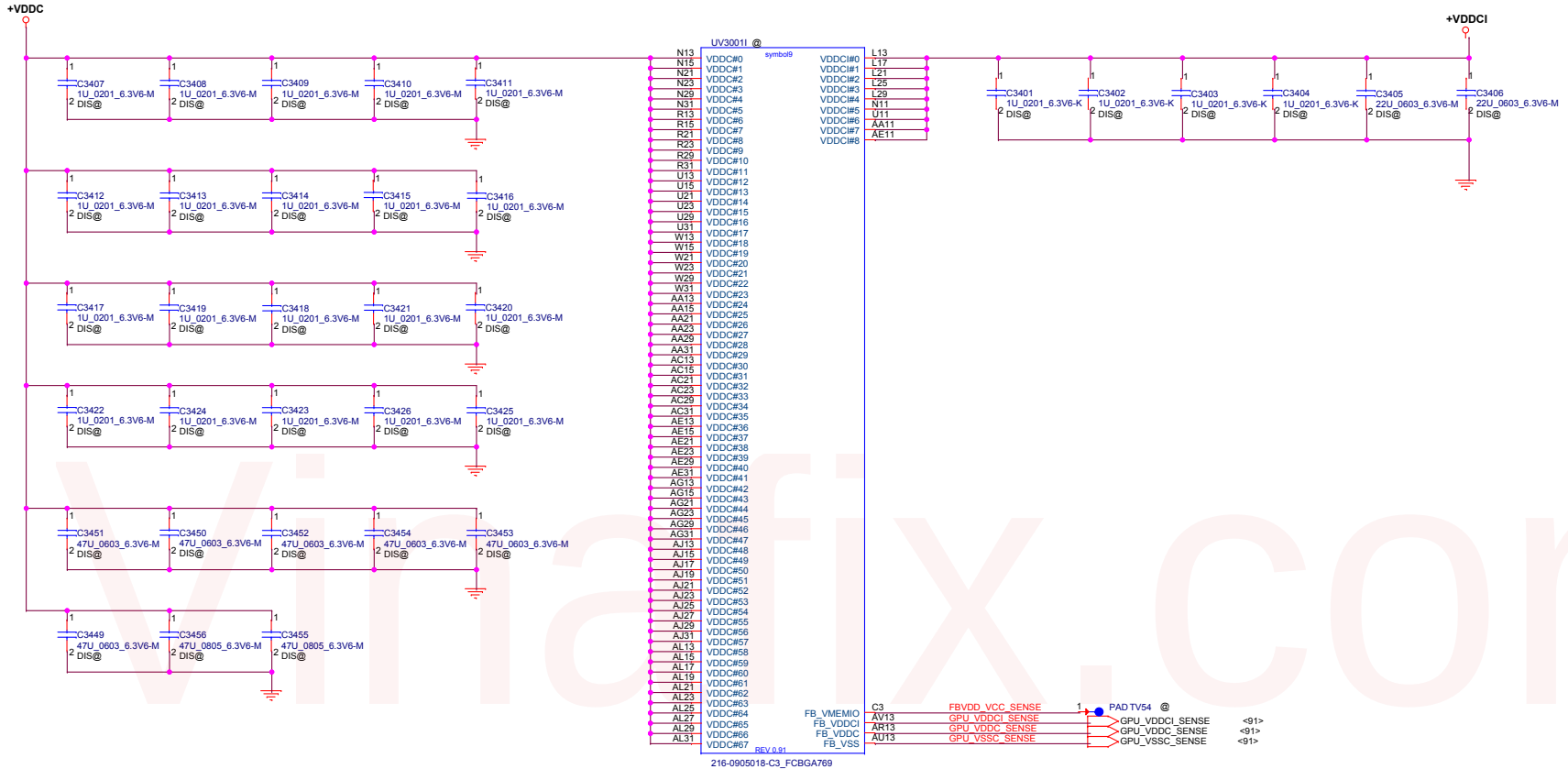
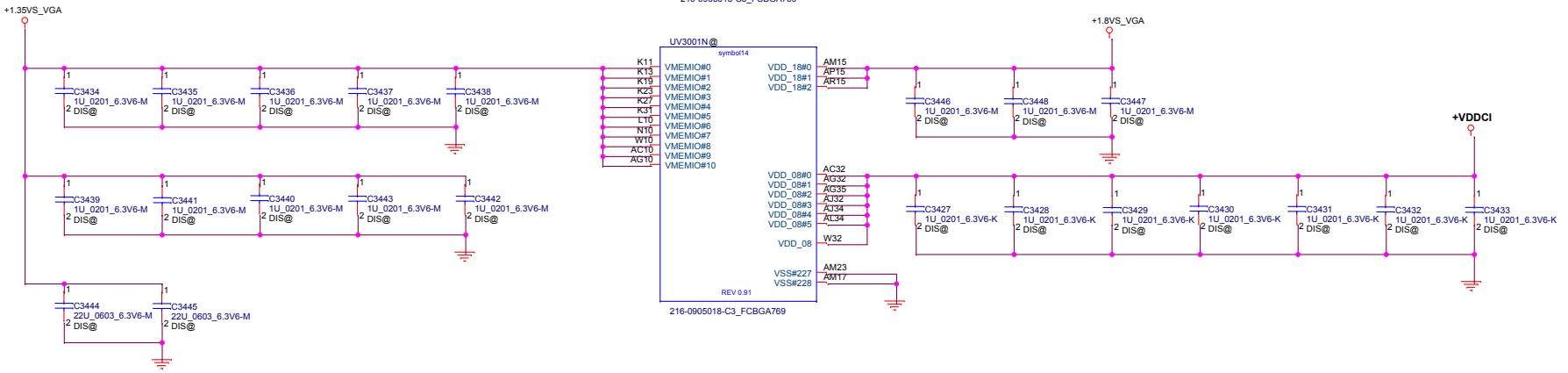
+VDDC +VDDC <91>

+VDDCI +VDDCI <91>

+1.35VS_VGA +1.35VS_VGA <31,36,95>

+1.8VS_VGA +1.8VS_VGA <30,32,38>





Title			
R17M-P1-50(F)_PWR			
Size: Custom	Document Number: EE480 NM-B421		Rev: 0.2
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Title: R17M-P1-50(G)_VSS

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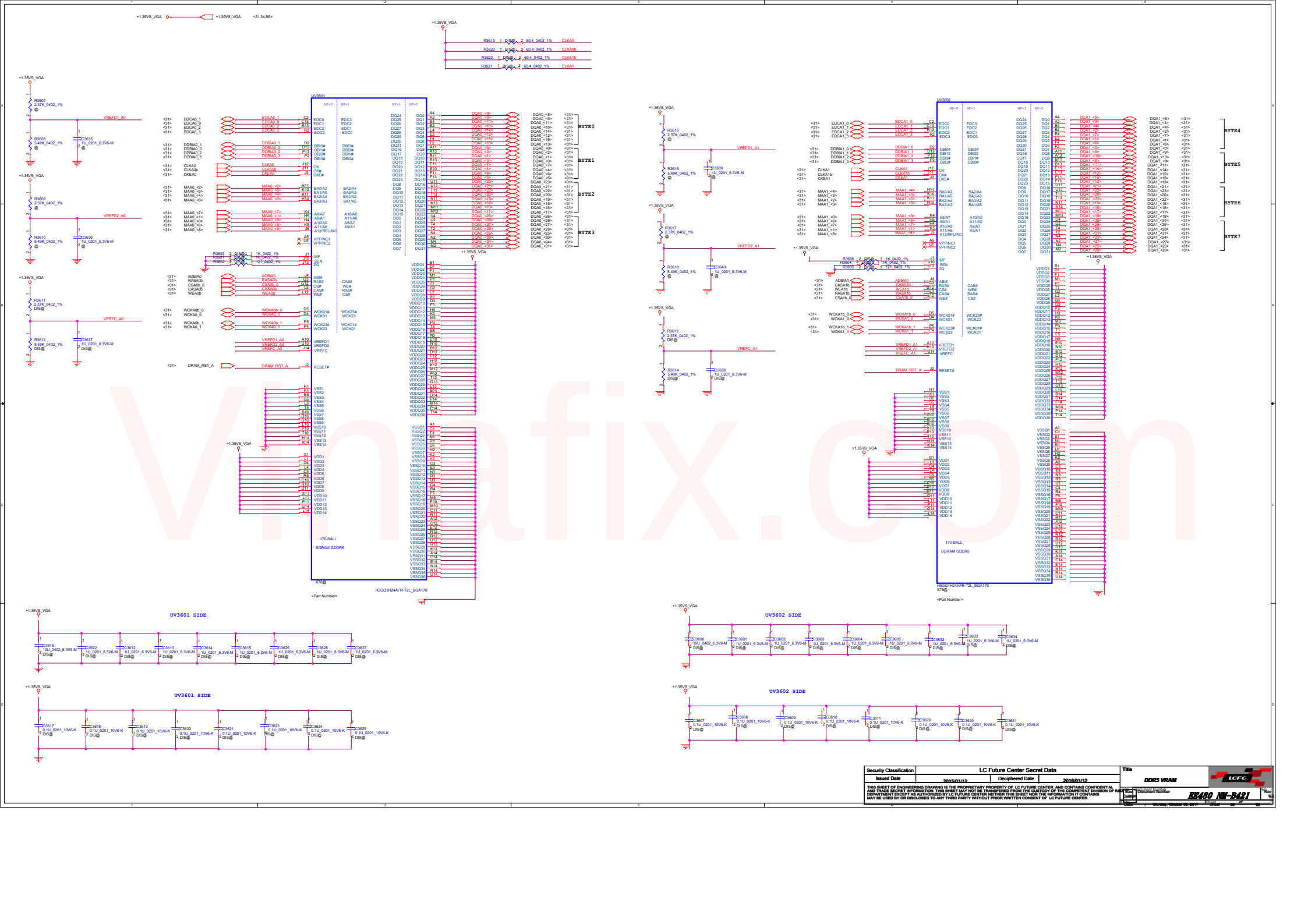

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/13	Deciphered Date	2016/01/13

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Title: DDR3 VRAM

Document Number: KK490 NM-B421

Rev: 0.2

Date: Monday, October 05, 2015

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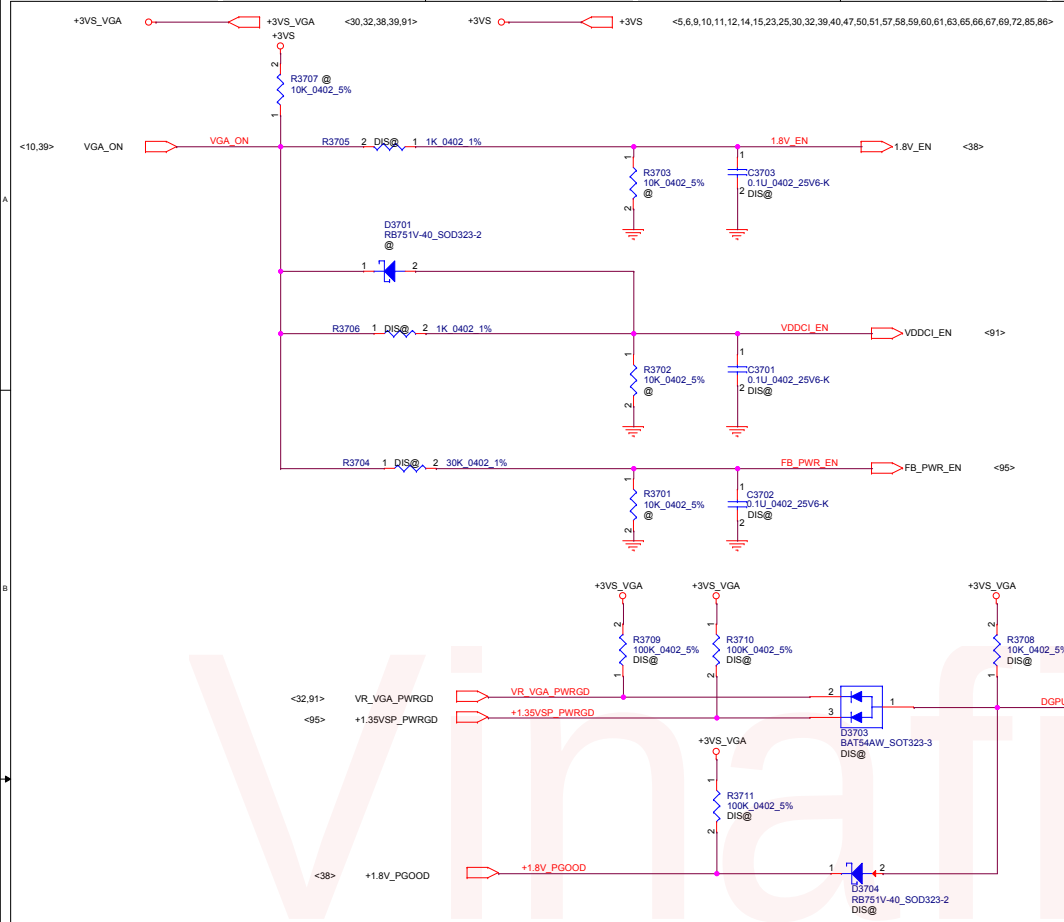

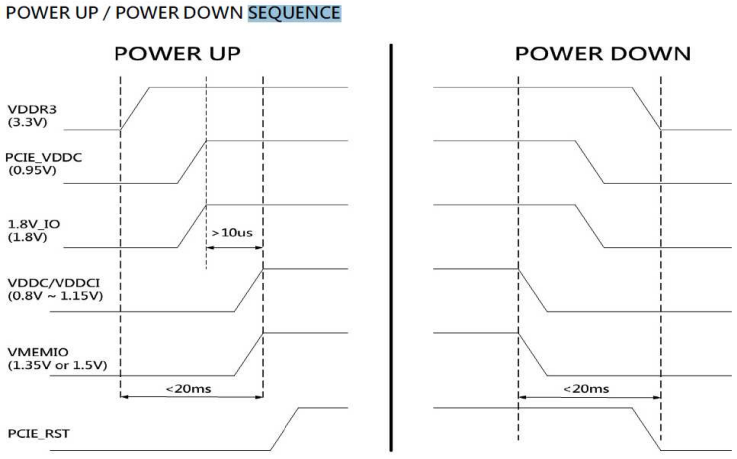

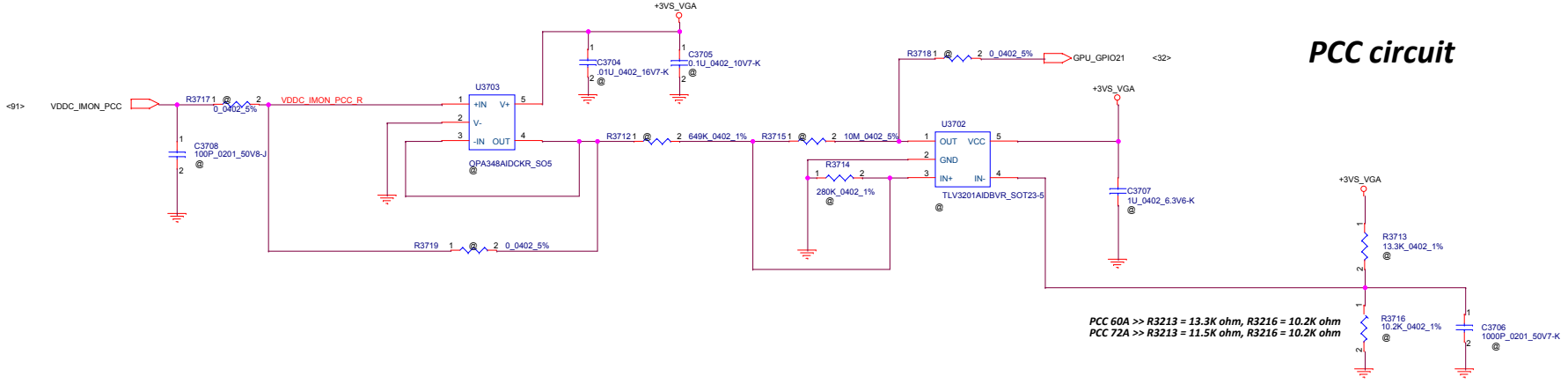

PCC circuit

PCC 60A >> R3213 = 13.3K ohm, R3216 = 10.2K ohm
PCC 72A >> R3213 = 11.5K ohm, R3216 = 10.2K ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	DDR5 VRAM BLANK		
Size C	Document Number EE480 NM-B421		Rev 0.2
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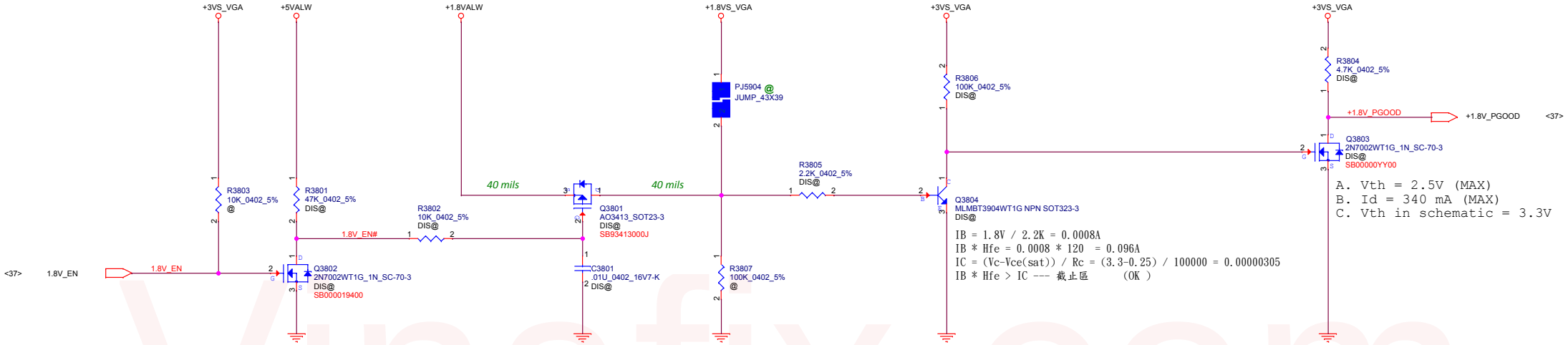
+3VS_VGA → +3VS_VGA <30,32,37,39,91>
+5VALW → +5VALW <39,42,43,47,64,66,67,71,72,84,85,86,87,88,89,91,93,94>
+1.8VALW → +1.8VALW <19,93>
+1.8VS_VGA → +1.8VS_VGA <30,32,34>

+1.8VALW to +1.8VS_VGA



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DC V TO 1.5VS_VGA/1.8VS_VGA

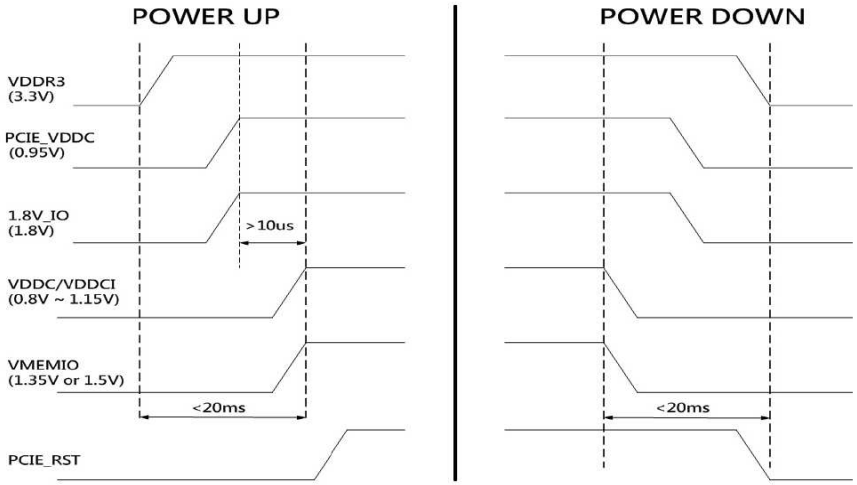
Size: Custom	Document Number: EE480 NM-B421	Rev: 0.2
Date: Monday, October 30, 2017	Sheet 38 of 99	

+3VS_VGA — +3VS_VGA <30,32,37,38,91>

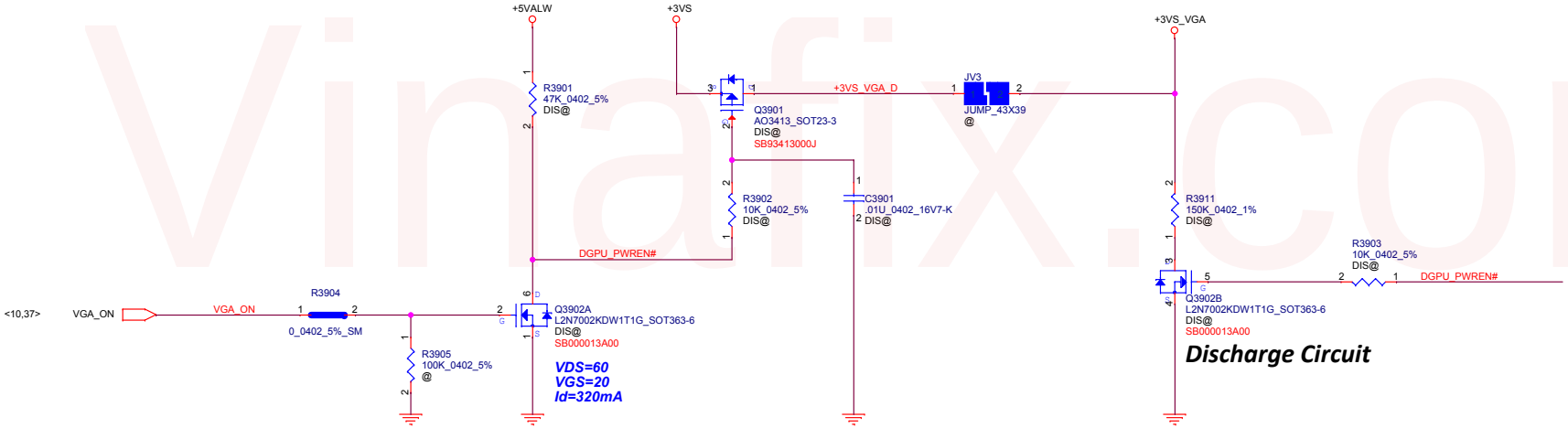
+5VALW — +5VALW <38,42,43,47,64,66,67,71,72,84,85,86,87,88,89,91,93,94>

+3VS — +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>

POWER UP / POWER DOWN SEQUENCE



+3VS to +3VS_VGA



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DC V TO 3VS_VGA/0.95VS_VGA

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

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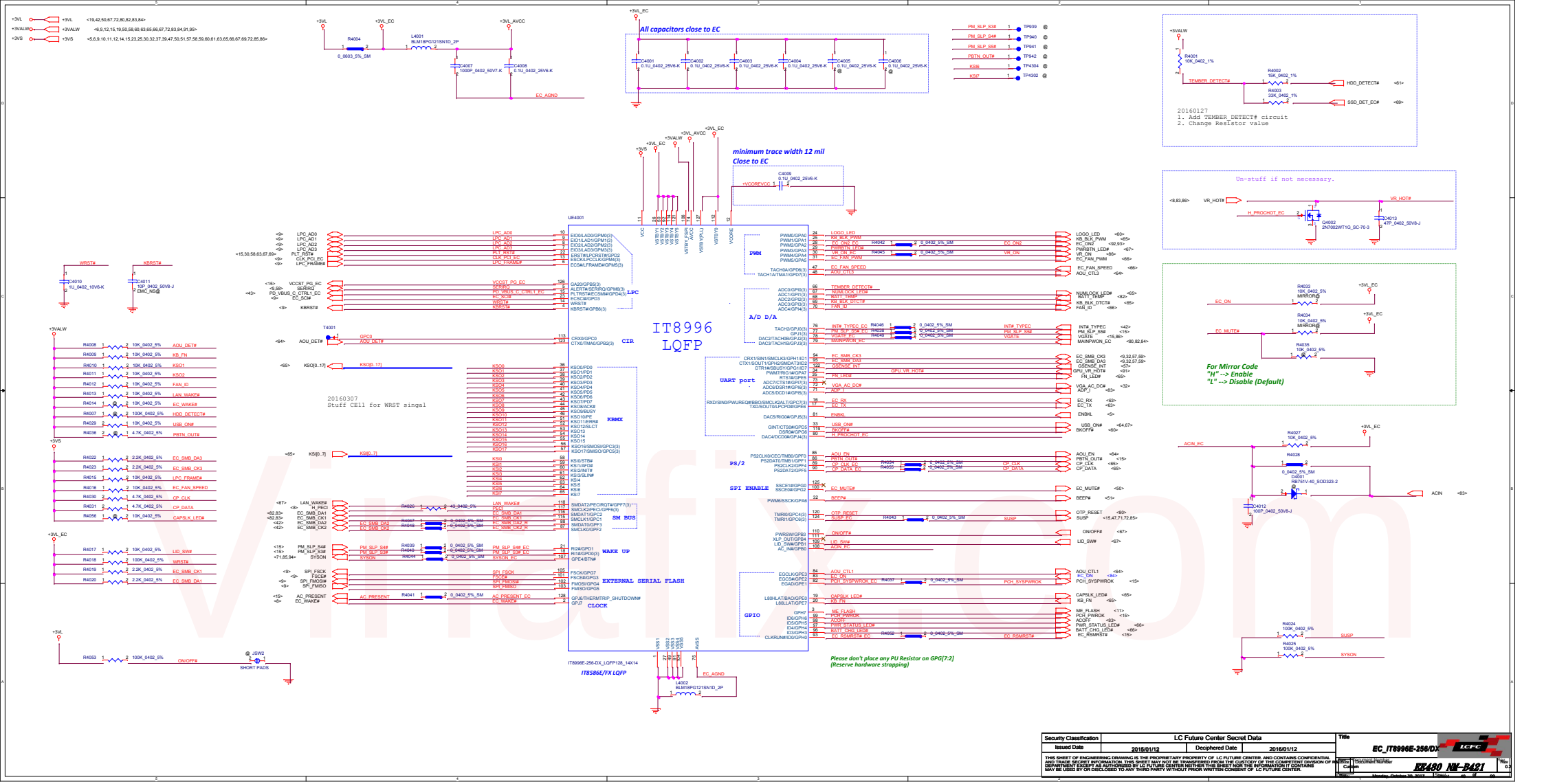

Title: EC_IT8996E-256/DX
Size: C | Document Number: KR480 NM-B421 | Rev: 0.5
Custom
Date: Monday, October 26, 2015 | Sheet 1 of 46

LAYOUT/ROUTING GUIDELINES

1.For the ADC layout notice circuits,
a) Keep the trace away from Power, fast data bus, and CRTs. Especially PWM DC-DC control.
b) Isolate Analog and Digital ground plane.

2.For all power plane,

a)For the VSTBY circuits,

*Recommended net "VSTBY" minimum trace width 12mils.

b)For the VBAT circuits,

1) Vbat should be routed with a minimum trace width of 12 mils.

2) Please make the trace length short, and the trace width wide enough.

3) Isolate the pin-Vbat of EC and the pin of south bridge VCCRTC to avoid VBAT drops.

4) The capacitor connected to Diode is spare for battery installation glitch.

c)For the PLL power circuits,

Internal PLL is supplied by power pin127 of EC only and may have some filter circuit.

3.For SPI clock lines,
a) If possible, please avoid using any through-hole.
b) Do not use multiple signal layers for clock signals.
c) Please make the trace length short, and the trace width wide enough.
EC should close to PCH for HSPI signals & SPI flash should close to EC for FSPI signals.
d) The spacing to the closest neighbor should be wide enough.
e) The discrete damping resistors and capacitors are recommended.
f) Keep clock traces as straight as possible.Use arc-shaped traces instead of
right-angle bends.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: EC_IT8996E-256/DX

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

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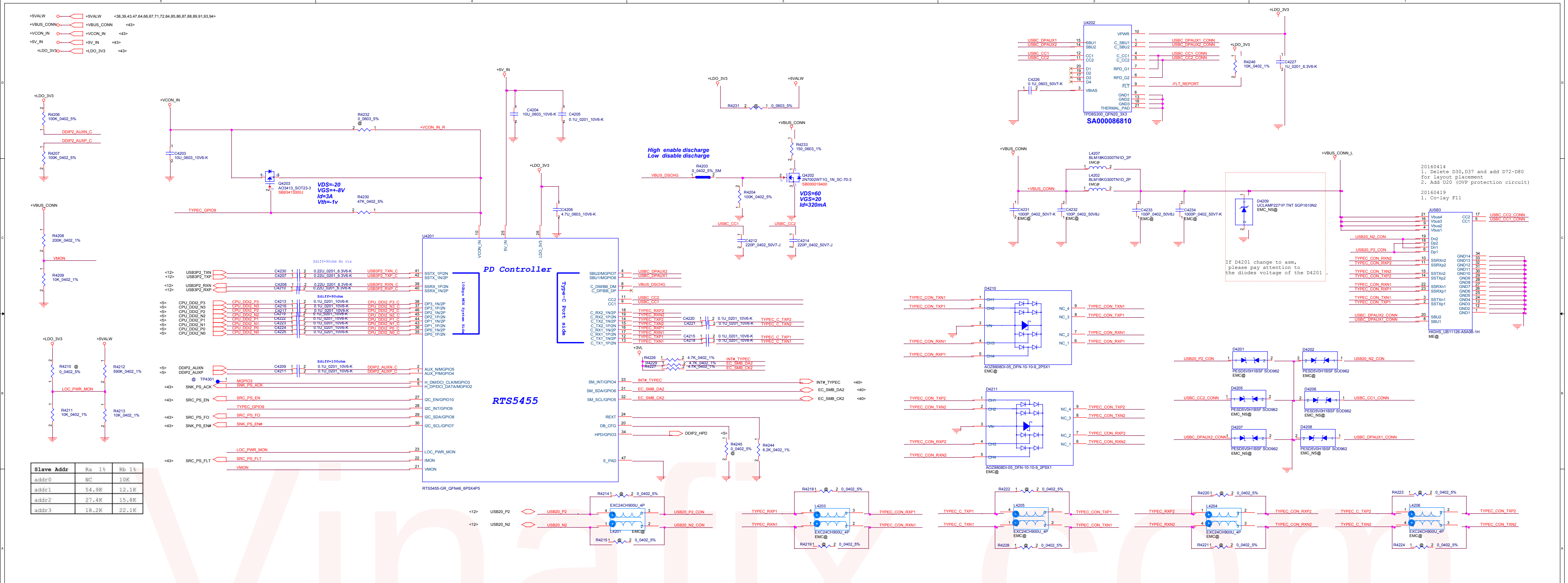
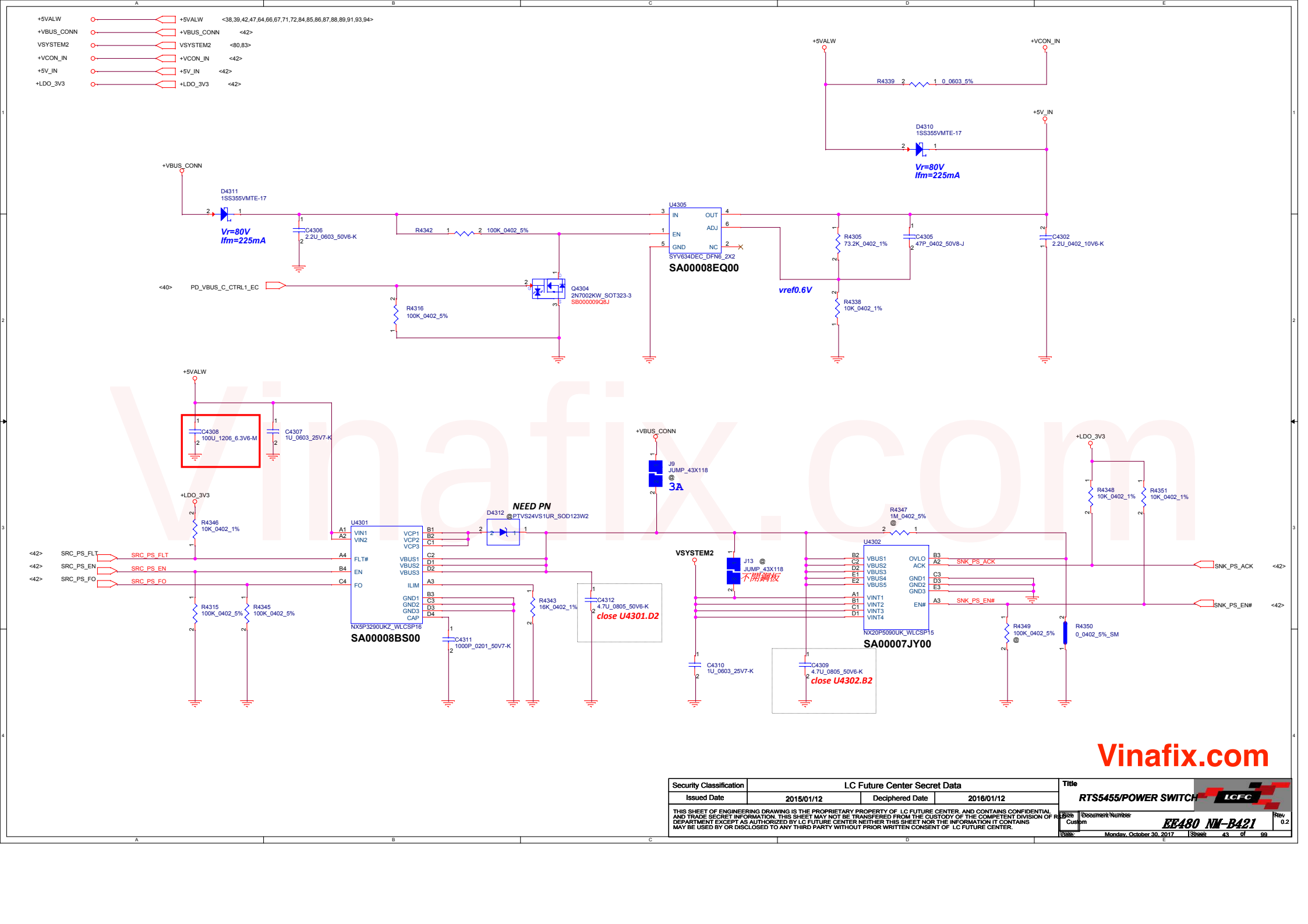


Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: RTS5455/USB TYPE-C

Size: Custom | Document Number: EE480 NM-B421 | Rev 0.2



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: RTS5455/POWER SWITCH

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: BLANK

Size: Custom	Document Number: EK460 NM-B421	Rev: 0.2
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: BLANK

Size	Document Number	Rev
D	EK460 NM-B421	0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **BLANK**

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

Date: Monday, October 30, 2017 Sheet 46 of 99

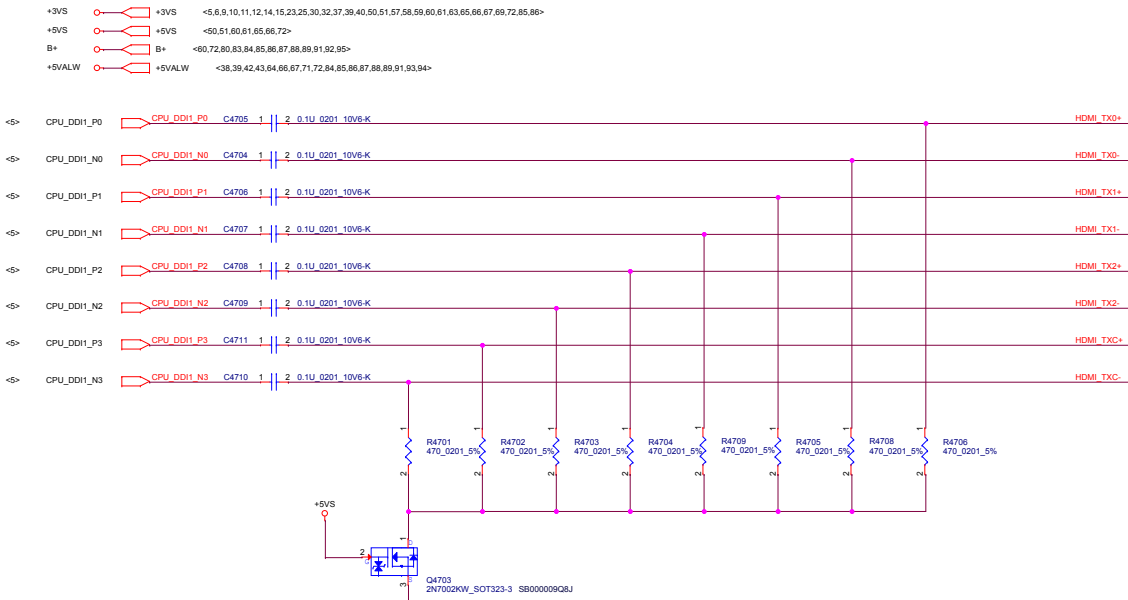


Figure 7-12. HDMI 1.4* HPD Active Level Shifter Design Recommendation

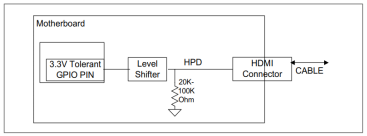
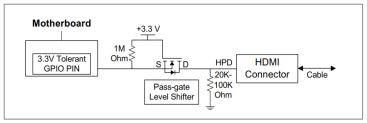
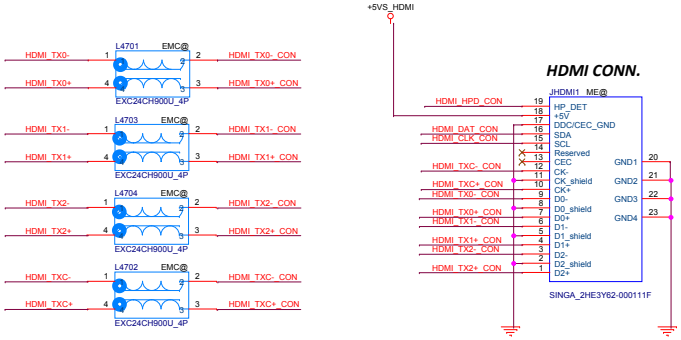
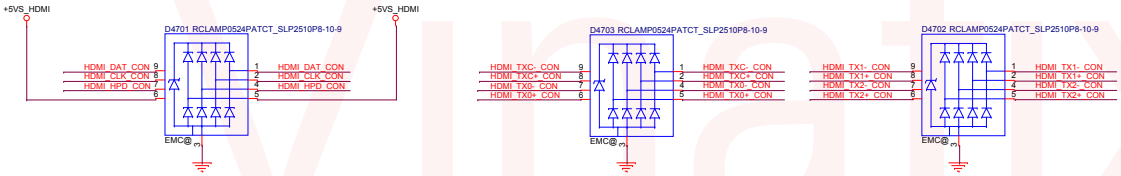


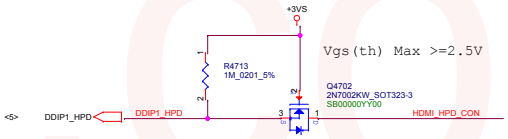
Figure 7-13. HDMI 1.4* HPD Cost Reduced Level Shifter Design Recommendation

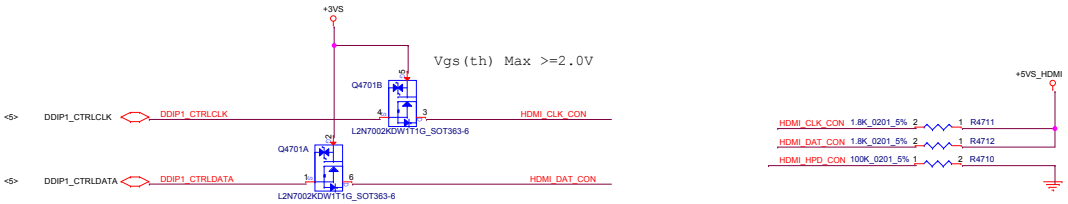


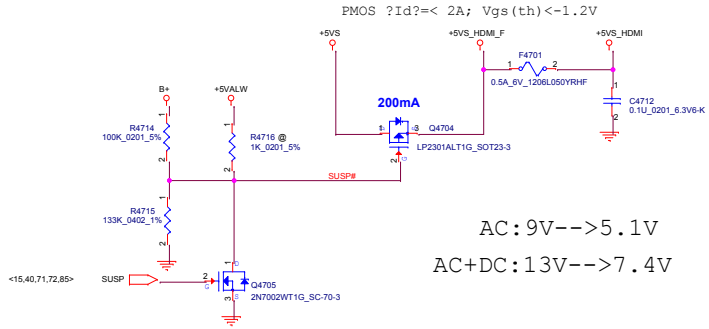
Note: 3.3V transistor gate supply must turn off when CPU power is turned off.











Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	HDMI CONN		
Size: Custom	Document Number: EB480 NM-B421		Rev: 0.2
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: BLANK

Size: D | Document Number: EK460 NM-B421 | Rev: 0.2

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Security Classification	LC Future Center Secret Data		
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Title: BLANK

Size	Document Number	Rev
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+5VS +5VS <47,51,60,61,65,66,72>

+3VL +3VL <19,40,42,67,72,80,82,83,84>

+3VALW +3VALW <6,9,12,15,19,40,58,60,63,65,66,67,72,83,84,91,95>

Close to Pin13,16

+5VS — R5009 0_0805_5%_SM — +5VS_CLASSD

C5001 4.7U_0603_10V6-K, C5002 4.7U_0603_10V6-K, C5003 0.1U_0402_10V7-K, C5004 0.1U_0402_10V7-K

Please Close Pin28

+5VS — R5004 0_0402_5%_SM — +5VS_AVDD

C5014 0.1U_0402_10V7-K

CA20 close Pin7

+3VALW — R5005 0_0402_5%_SM — +3VS_VDDIO

C5015 0.1U_0402_10V7-K

CA12 close Pin2

+3VS — R5001 0_0402_5%_SM — +3VS_VDDO

C5011 0.1U_0402_10V7-K

X5R CAP, Please Close Pin18

+3VS — R5003 0_0805_5%_SM — +3VS_DVDD

C5013 1U_0402_6.3VA-K

CA13 close Pin24

+3VL — R5002 0_0805_5%_SM — +3V_AVDD_HP

C5012 1U_0402_6.3VA-K

LDO 1V8

+1.8V_LDO

C5005 4.7U_0603_10V6-K S CER CAP 4.7U 10V K X5R 0603 **X5R CAP**

VREF 1V65

+1.65V_LDO

C5006 0.1U_0402_10V7-K, C5007 1U_0402_6.3VA-K S CER CAP 1U 6.3V K X6S 0402 **X5R CAP**

GNDA

LDO 3V3

+3V_LDO

C5008 0.1U_0402_10V7-K, C5009 2.2U_0402_6.3V6-M

GNDA

CA10 close Pin7

+3VS

C5010 0.1U_0402_10V7-K

+3VS_VDDO — R5006 47K_0402_5% — D5001 RB751V-40_SOD323-2 SCS00006S00

<40> EC_MUTE# — EC_MUTE#

<11> PCH_HDA_RST# — PCH_HDA_RST#

<11> PCH_HDA_BCLK — PCH_HDA_BCLK

<11> PCH_HDA_SYNC — PCH_HDA_SYNC

<11> PCH_HDA_SDIN0 — PCH_HDA_SDIN0 — R5008 33_0402_5% — PCH_HDA_SDIN0_R

<11> PCH_HDA_SDOUT — PCH_HDA_SDOUT

<51> PC_BEEP — PC_BEEP — SPKR_MUTE#

<51> JSENSE — JSENSE

<60> DMIC_CLK — DMIC_CLK — R5007 EMC@ 33_0402_5% — MIC_CLK_R

<60> DMIC_DATA — DMIC_DATA

C5016 150P_0402_50V8-J EMC@

+5VS_CLASSD W= 80mils — C5017 0.1U_0402_10V7-K — CLASSD_REF

+AVEE — C5018 1U_0402_6.3V6-K — FLY_P, FLY_N

C5022 2.2U_0402_6.3V6-M HP indicate

Should be connect to GNDA

UA5001 CX11852

RESET#, BIT_CLK, SYNC, SDATA_IN, SDATA_OUT, PC_BEEP, SPKR_MUTE#, JSENSE, GPIO1/PORTC_R_MIC, MUSIC_REQ/GPIO0/PORTC_L_MIC, DMIC_CLK/MUSIC_REQ/GPIO0, DMIC_DAT/GPIO1, CLASS-D_REF, LPWR_5.0, RPWR_5.0, FLY_P, FLY_N, AVEE, GND

FILT_1.8V, VDD_IO, VDDO_3.3, DVDD_3.3, AVDD_3.3, VREF_1.65V, AVDD_5V, LEFT+, LEFT-, RIGHT+, RIGHT-, MICBIASC, MICBIASB, PORTB_R_LINE, PORTB_L_LINE, PORTD_A_MIC, PORTD_B_MIC, HGNDA, HGNDB, AVDD_HP, PORTA_R, PORTA_L

+1.8V_LDO +3VS_VDDIO +3VS_VDDO +3VS_DVDD +3V_LDO +1.65V_LDO +5VS_AVDD

+MICBIASB +3V_AVDD_HP

SPK_L2+ / SPK_L1- → SPK_L2+ / SPK_L1- <51>

SPK_R2+ / SPK_R1- → SPK_R2+ / SPK_R1- <51>

PORTB_R / PORTB_L → PORTB_R / PORTB_L <51>

EXT_MIC_A / EXT_MIC_B → EXT_MIC_A / EXT_MIC_B <51>

HGNDA / HGNDB → HGNDA / HGNDB <51,52>

Apple --> EXT_MIC_A, HGNDB

Nokia --> EXT_MIC_B, HGNDA

HP_OUTR / HP_OUTL → HP_OUTR / HP_OUTL <51>

CX11852-11Z_QFN40_5X5

SA00007B100

W= 300mils

C5019 0.1U_0402_10V7-K EMC@

C5020 0.1U_0402_10V7-K EMC_NS@

C5021 0.1U_0402_10V7-K EMC_NS@

GNDA

LAYOUT GND/AGND RECOMMEND

AGND, DGND

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: CODEC-CX11852

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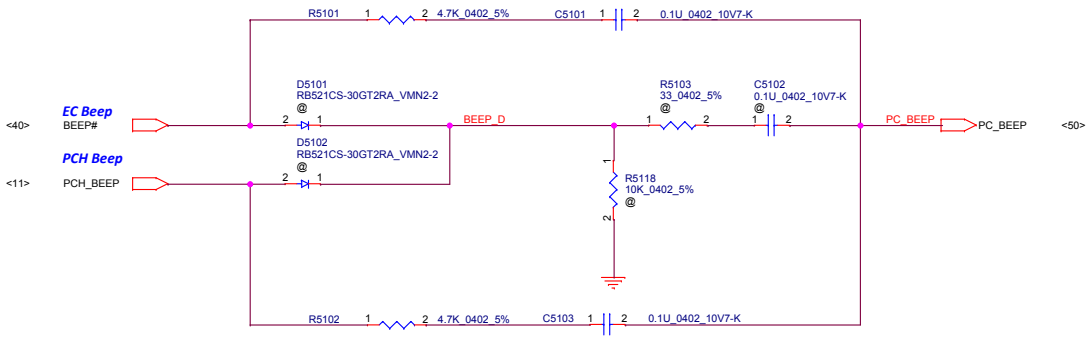
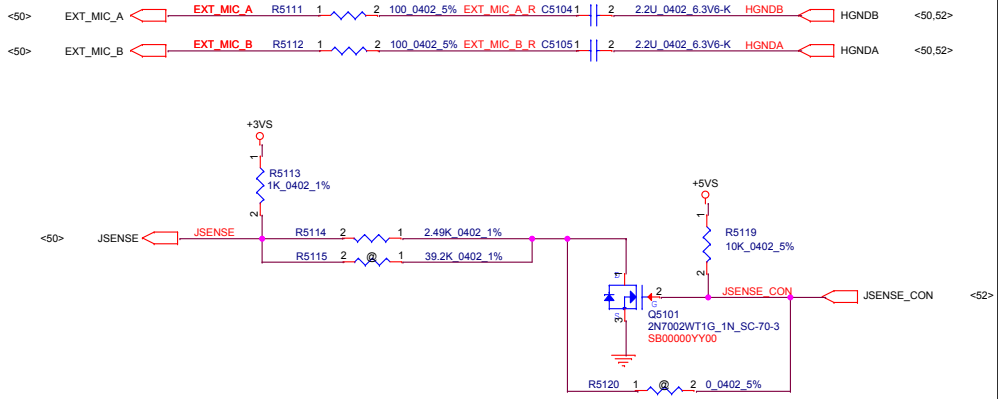
+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,61,63,65,66,67,69,72,85,86>

PC Beep

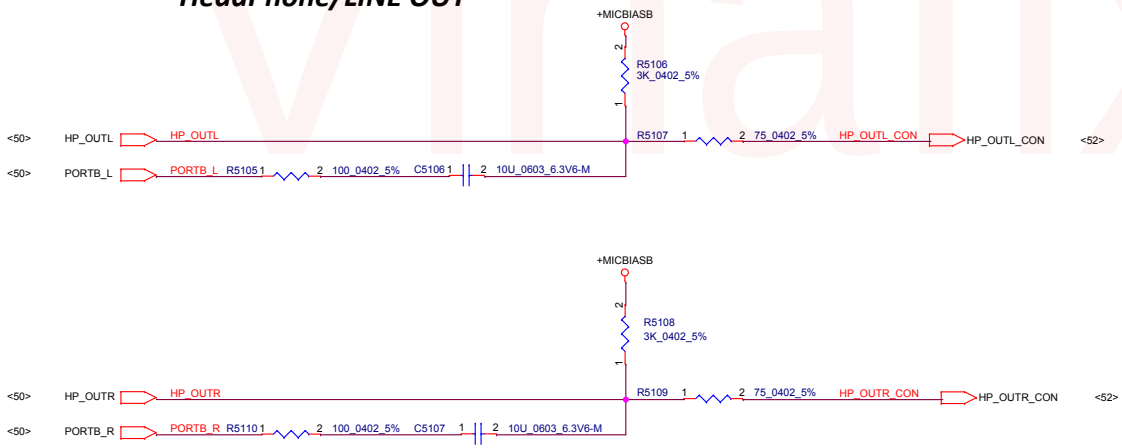


EXT. MIC/LINE IN

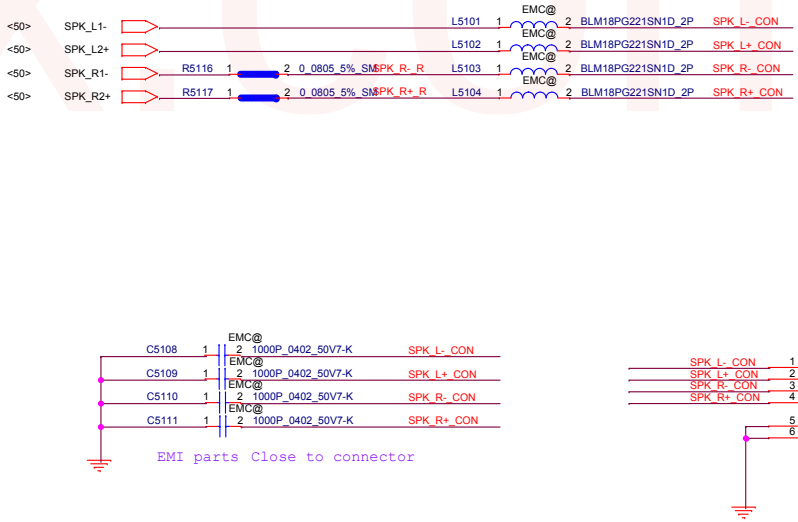
Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



HeadPhone/LINE OUT



SPK CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: HP/MIC JACK/Speaker

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2
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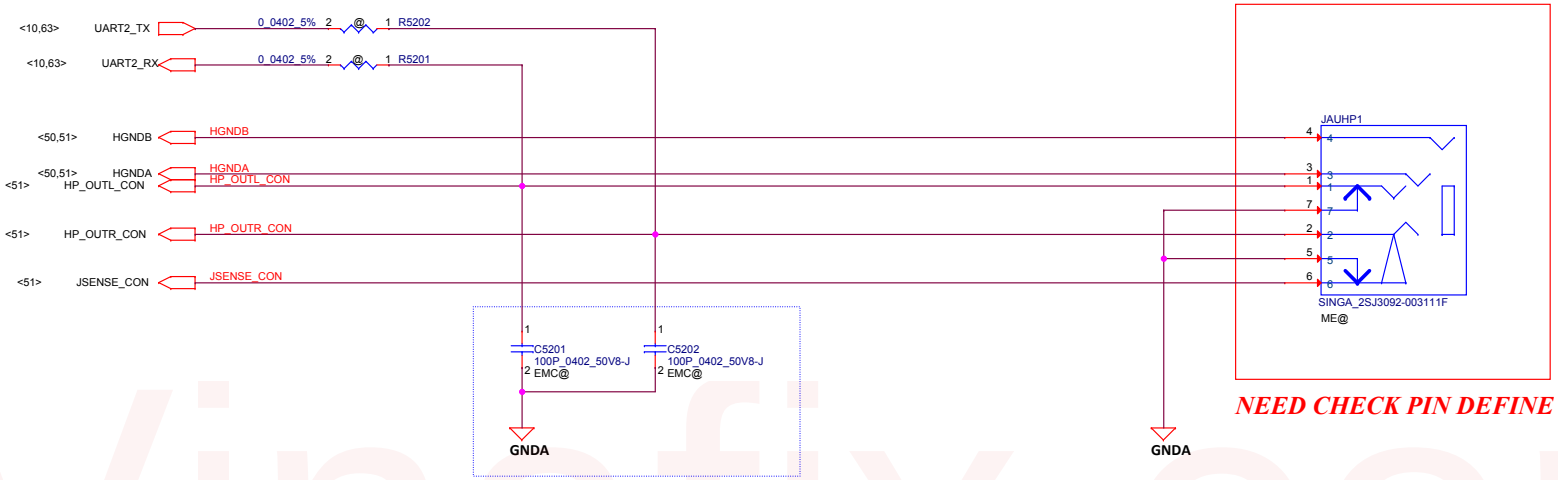
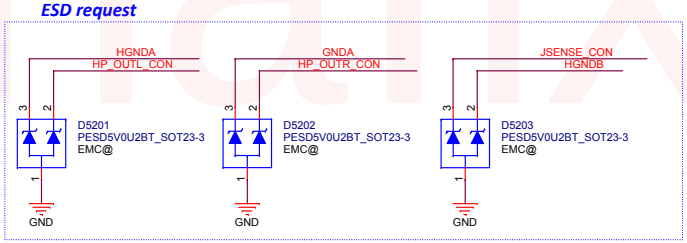
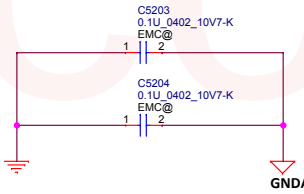


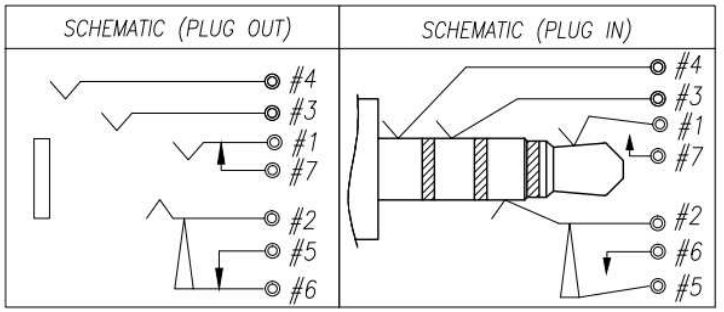
NEED CHECK PIN DEFINE

Vendor suggestion. Reserve for EMI.
Close to JAUHP.

ESD request







Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **AUDIO JACK**

Size	Document Number	Rev
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Title

GBE LAN PHY(BLANK)

Size: Custom	Document Number: EE480 NM-B421	Rev: 0.2
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

GBE LAN SWITCH(BLANK)

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: RJ45 CONN.(BLANK)

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

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Security Classification	LC Future Center Secret Data		
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Title: CARDREADER/CONN.(BLANK)

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

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+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,58,59,60,61,63,65,66,67,69,72,85,86>

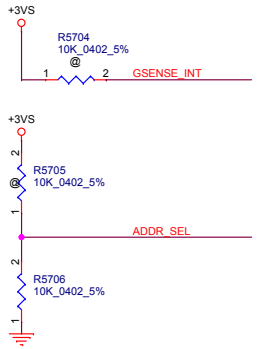
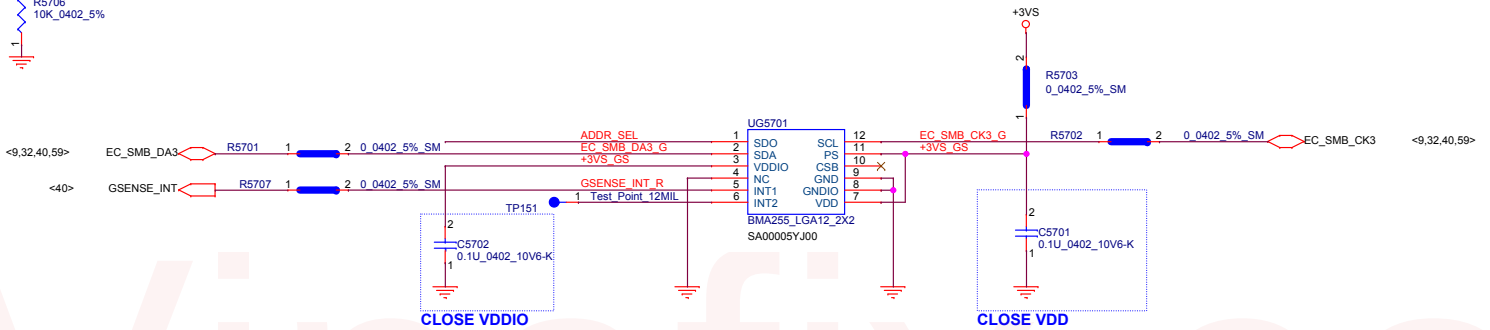


TABLE of G-Sersor (UG5701)		
Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00

TABLE

P/N	ADDR_SEL	Address
BMA255	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: G SENSOR

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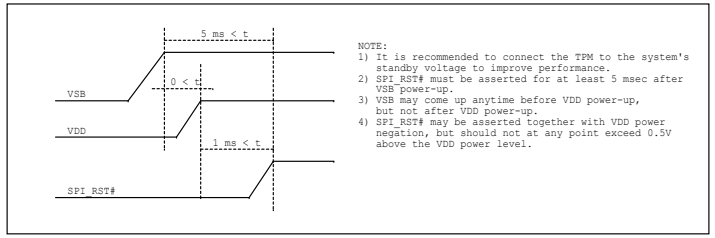
TABLE of TPM (UT5801)		
Vendor	LCFC P/N	Description
Infineon	SA000075L40	S IC SLB9670VQ2.0FW7.61 VQFN 32P TPM
ST	SA000089E10	S IC ST33HTPH2E32AHB4 VQFN 32P TPM

NOTE:
Check timing sequence in SDV phase.



TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table

Title: TPM

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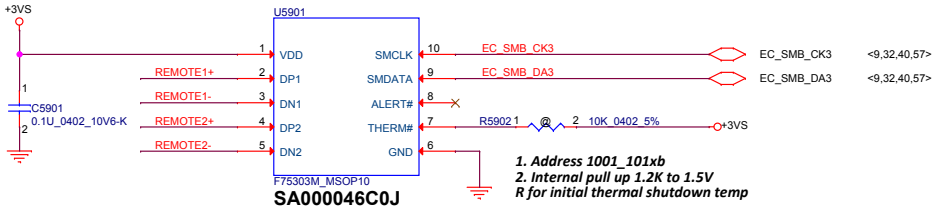
+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,60,61,63,65,66,67,69,72,85,86>

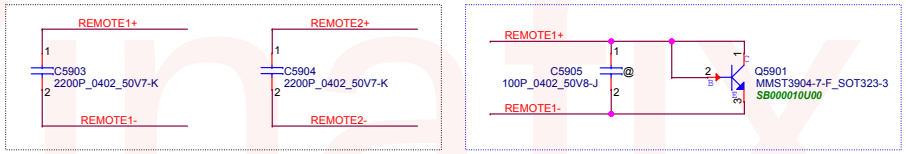
Thermal Sensor

Close to CPU

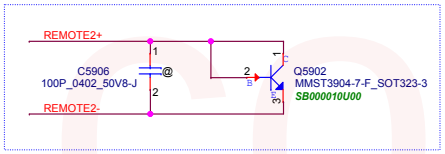


1. Address 1001_101xb
2. Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

Close to CHARGER



Close to GPU



Trace width/space:10/10 mil
Trace length:<8"

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: THERMAL SENSOR

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

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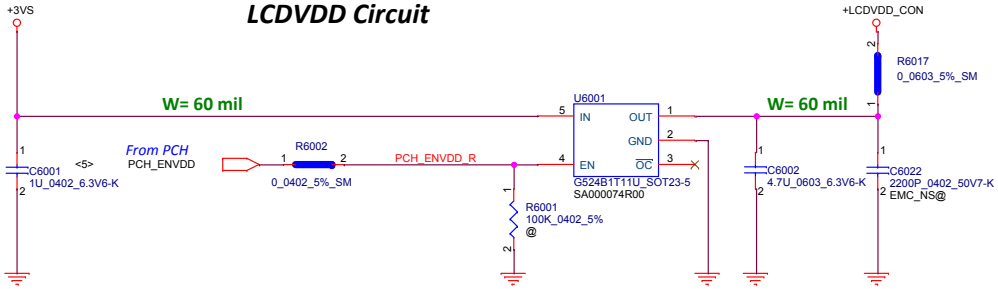
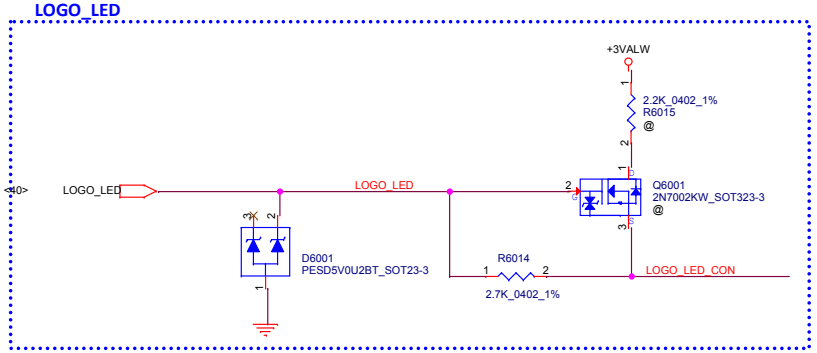
+3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,61,63,65,66,67,69,72,85,86>

B+ <47,72,80,83,84,85,86,87,88,89,91,92,95>

LCDVDD Circuit



LOGO_LED



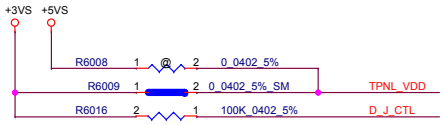
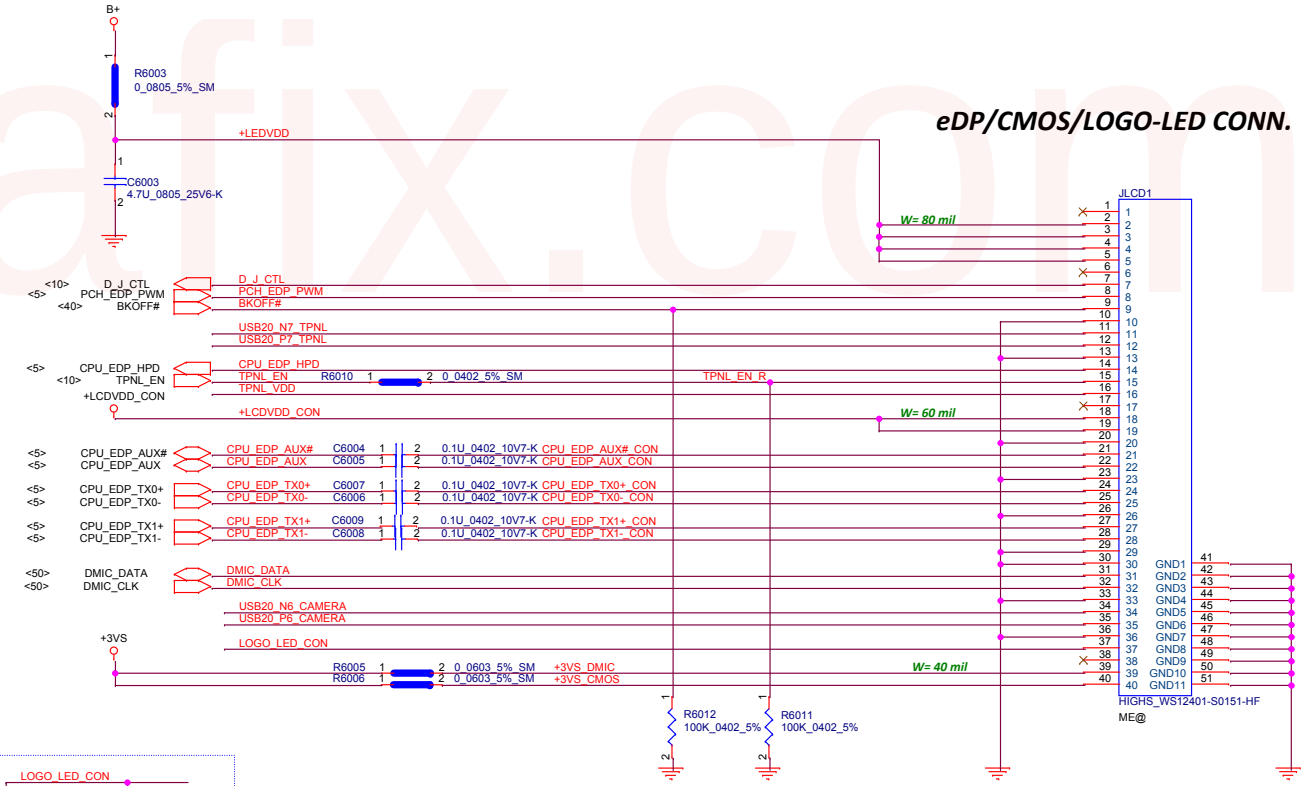
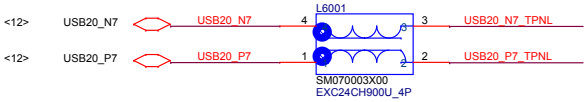


TABLE of POWER SWITCH (U6001)		
Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH

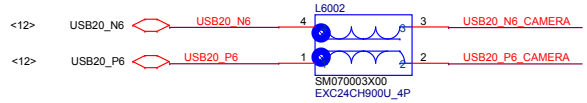
eDP/CMOS/LOGO-LED CONN.



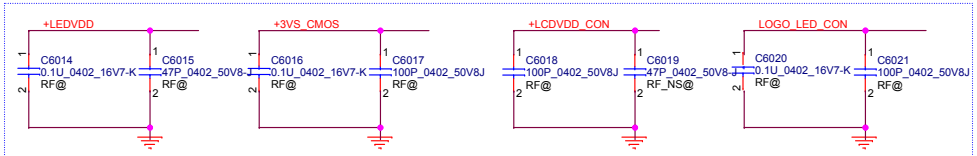
Touch Panel



CAMERA



RF



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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: eDP/CMOS/LOGO-LED CONN

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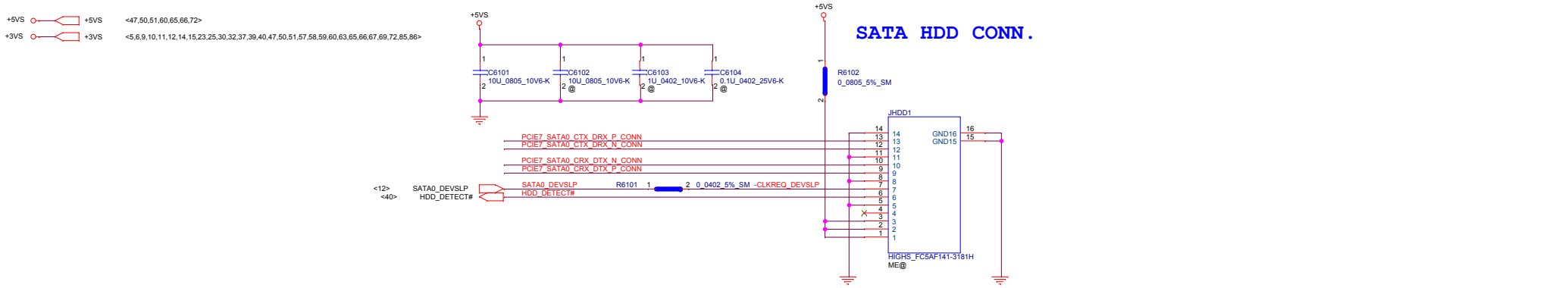
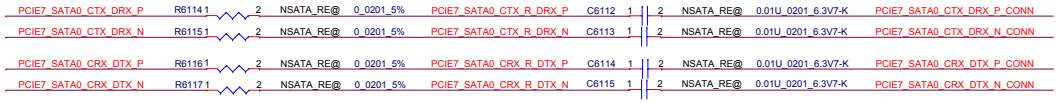
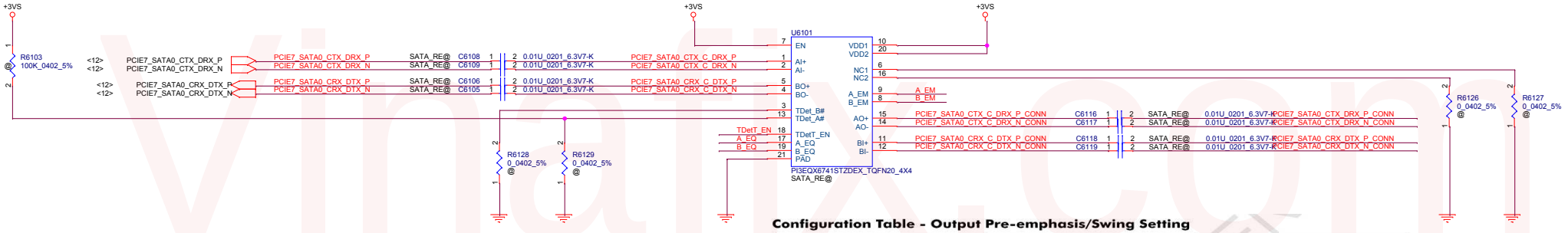
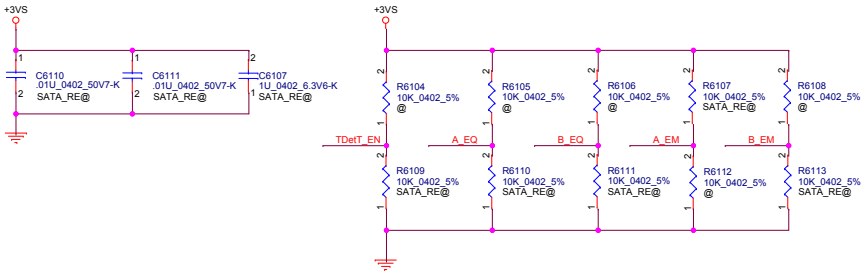




	Diodes	TI	Comment
Pin	PI3EQX6741ST	LVCP601	
3	Tdet_B#	GND	Connect to ground
6	NC	DEW2	Connect to ground and reserve pull-up with 4.7K to 3.3V
13	Tdet_A#	GND	Connect to ground
16	NC	DEW1	Connect to ground and reserve pull-up with 4.7k to 3.3V
18	TDeT_EN	GND	Connect to ground

SATA REDRIVER





Configuration Table - Output Pre-emphasis/Swing Setting

A_EM/B_EM	3 Gb/s	6 Gb/s
0	600mV pp	600mV pp
1	500mV pp + 3dB Pre-emphasis	600mV pp + 1.5dB Pre-emphasis

Configuration Table - Input Equalizer

A_EQ/B_EQ	1.5 Gb/s	3 Gb/s	6Gb/s
0	1 dB	2.5 dB	3 dB
floating	2.5 dB	5 dB	6 dB
1	4 dB	7.5 dB	9 dB

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: SATA HDD CONN/REDRIVE

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Title: SATA(BLANK)

Size	Document Number	Rev
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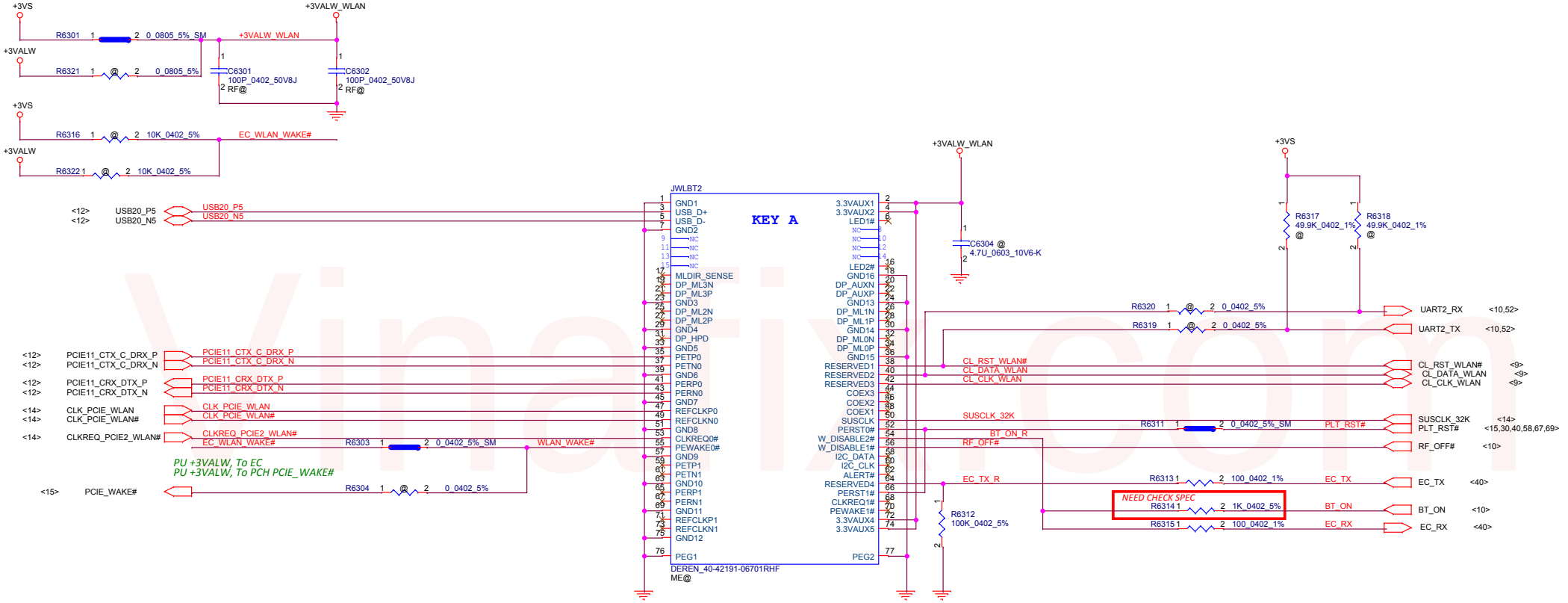
+5VALW +5VALW <38,39,42,43,47,64,66,67,71,72,84,85,86,87,88,89,91,93,94>

+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,65,66,67,69,72,85,86>

+3VALW +3VALW <6,9,12,15,19,40,50,58,60,65,66,67,72,83,84,91,95>

TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: WWAN/WLAN NGFF CONN.

LCFC

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On Board (LEFT-Front)

+5VALW +5VALW <38,39,42,43,47,66,67,71,72,84,85,86,87,88,89,91,93,94>
+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,72,85,86>

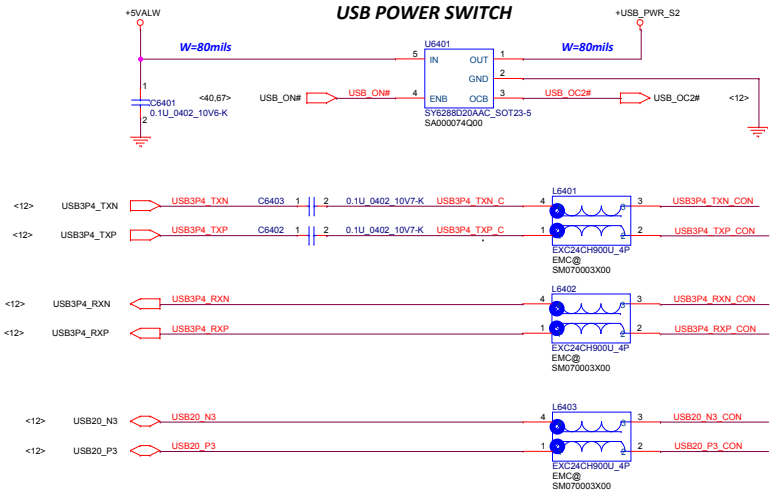
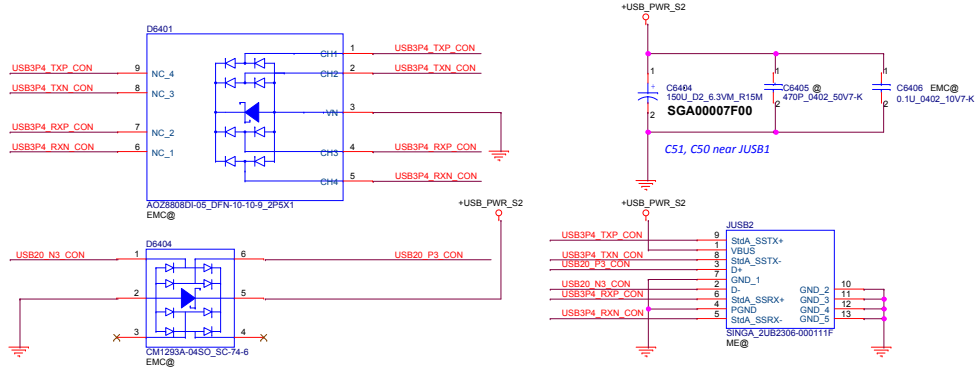
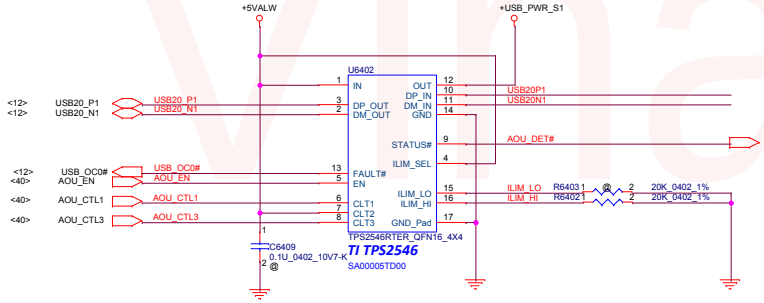


TABLE of POWER SWITCH (U6401)		
Vendor	LCFC P/N	Description
SILERGY	SA000074Q00	S IC SY6288D20AAC SOT23 5P POWER SWITCH
GMT	SA000079400	S IC G517F2T11U SOT-23 5P POWER SWITCH



On Board (LEFT-Back)



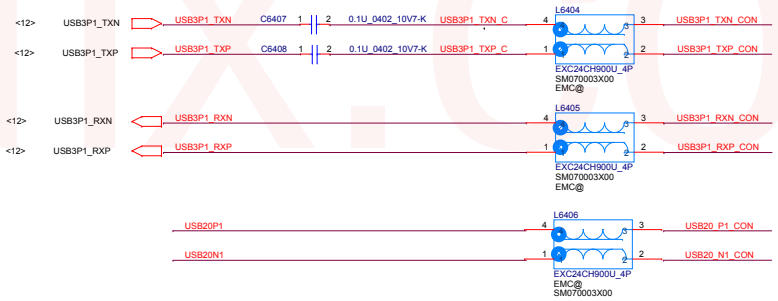
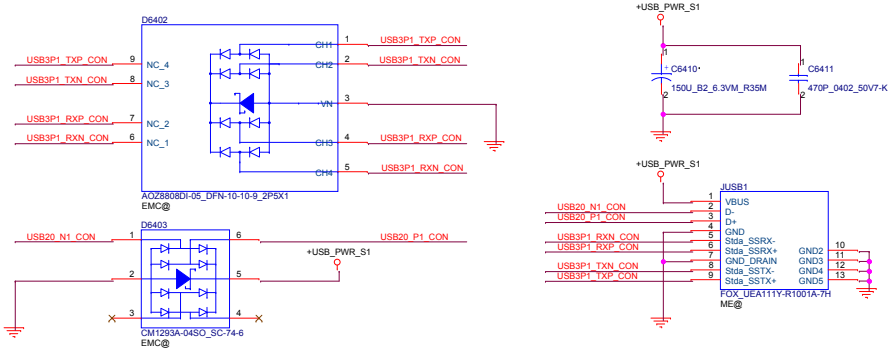


TABLE of POWER SWITCH (U6401)		
Vendor	LCFC P/N	Description
TI	SA00005TD00	S IC TPS2546RTER QFN 16P USB CHARGING
Pericom	SA000066I00	S IC PI5USB2546ZHEX TQFN 16P CONTROLLER

	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
	0	0	0	X	DCH	OUT held low
*	1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
*	1	1	1	0	SDP2	Data Connected
*	1	1	0	X	SDP1	Data Connected
*	0	1	0	X	SDP1	Data Connected
	1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
	0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active



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Issued Date	2015/01/12	Deciphered Date	2016/01/12

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Title: USB3 P1/2 CONN.

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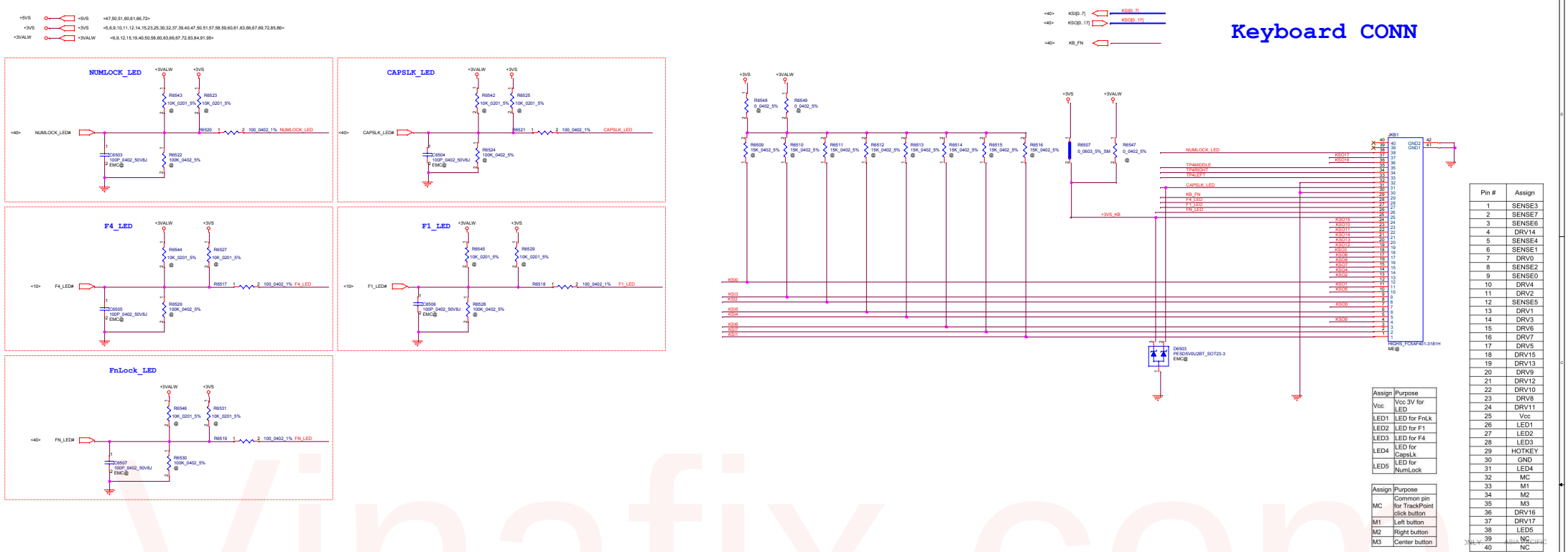
Keyboard CONN

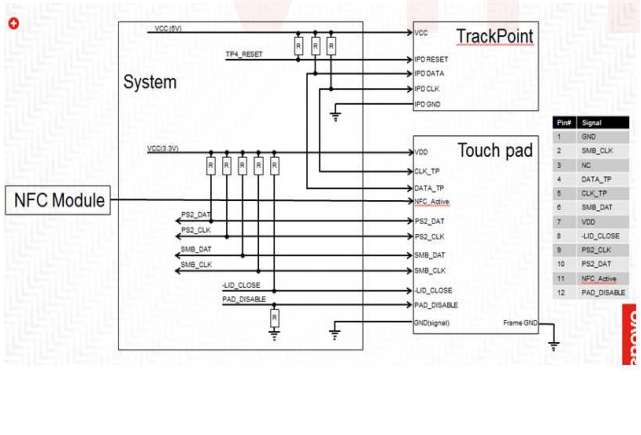


Pin #	Assign
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	MC
33	M1
34	M2
35	M3
36	DRV16
37	DRV17
38	LED5
39	NC
40	NC

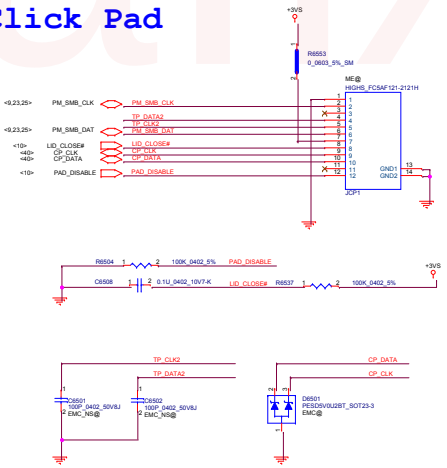
Assign	Purpose
Vcc	Vcc 3V for LED
LED1	LED for FnLk
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLk
LED5	LED for NumLock

Assign	Purpose
MC	Common pin for TrackPoint click button
M1	Left button
M2	Right button
M3	Center button

Click Pad



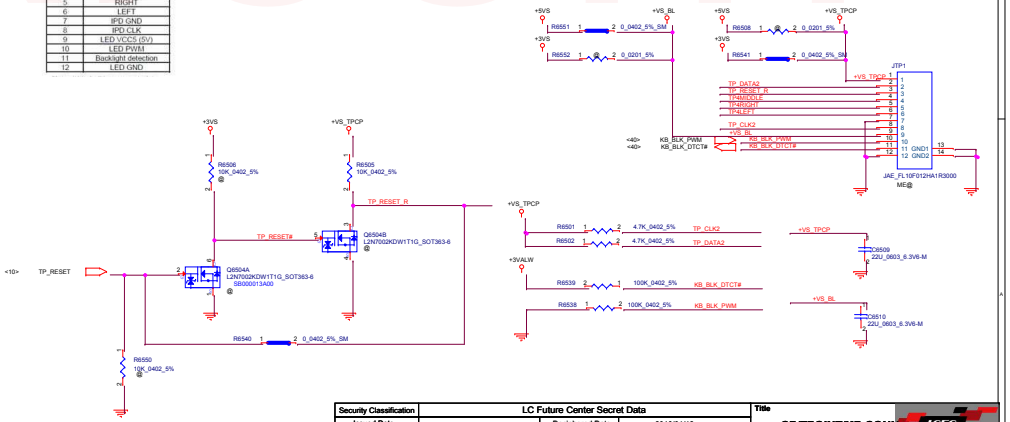
Pin#	Signal
1	GND
2	SMB_CLK
3	NC
4	DATA_TP
5	CLK_TP
6	SMB_DAT
7	VDD
8	LID_CLOSE
9	PS2_CLK
10	PS2_DAT
11	NFC_Active
12	PAD_DISABLE



Track Point

TrackPoint and Backlight FPC
Pin Assignment

Pin #	Assign
1	VCC (3.3V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND



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Title: CP/TPOINT/KB CONN

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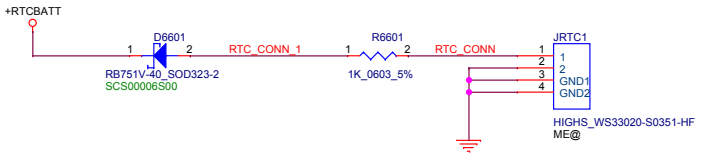
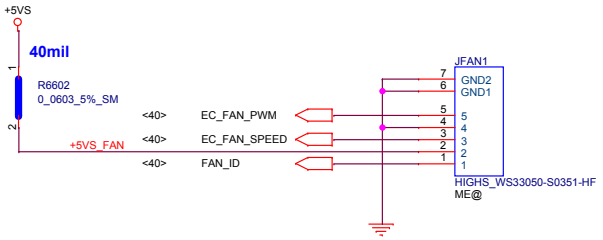
+RTCBATT +RTCBATT <14,80>
+5VS +5VS <47,50,51,60,61,65,72>
+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,67,69,72,85,86>
+3VALW +3VALW <6,9,12,15,19,40,50,58,60,63,65,67,72,83,84,91,95>

RTC CONN.

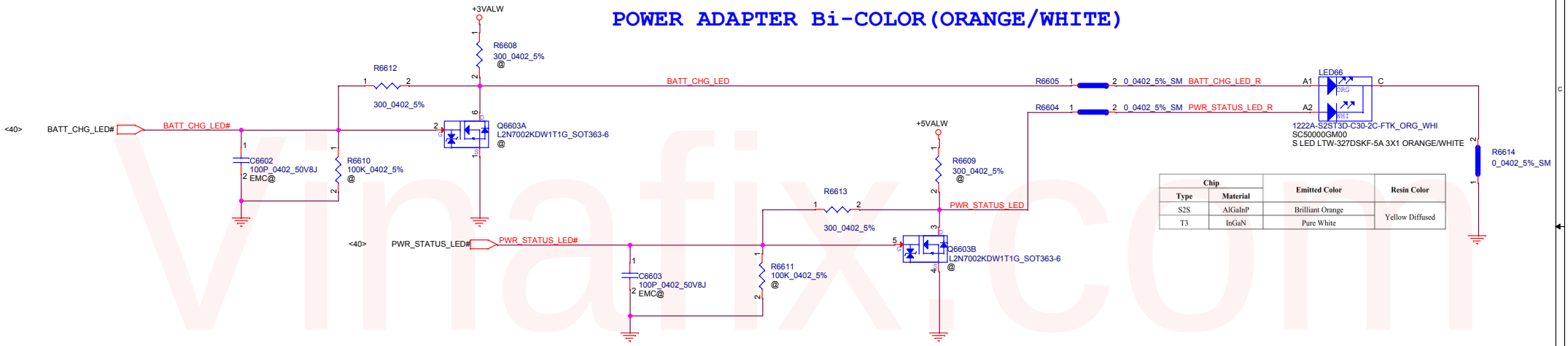


FAN CONN.



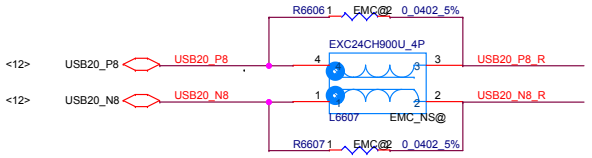
Pin No.	Signal	Note
1	ID	Fan ID
2	VCC	+5V
3	FG	2 Pulses
4	GND	–
5	PWM	PWM

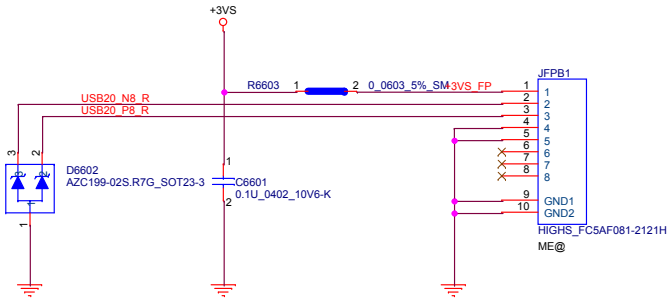
POWER ADAPTER Bi-COLOR(ORANGE/WHITE)

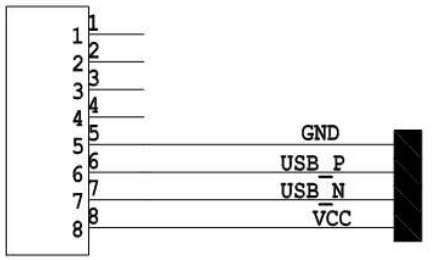


Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInP	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	

FingerPrint CONN.







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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: RTC/LED /FAN ,FPR CONN.

Size	Document Number	Rev
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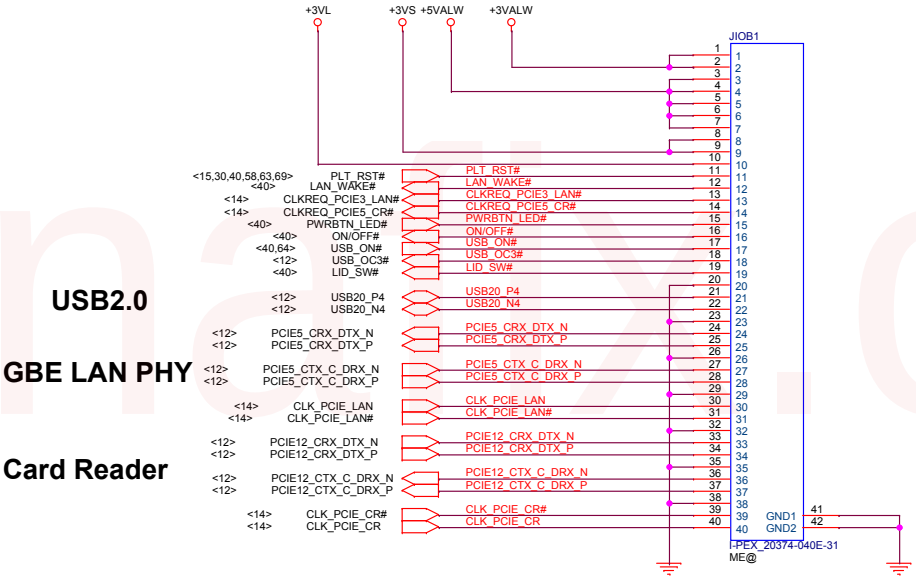
+3VL +3VL <19,40,42,50,72,80,82,83,84>

+3VALW +3VALW <6,9,12,15,19,40,50,58,60,63,65,66,72,83,84,91,95>

+5VALW +5VALW <38,39,42,43,47,64,66,71,72,84,85,86,87,88,89,91,93,94>

+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,69,72,85,86>

IO_40_Pin conn



USB2.0

GBE LAN PHY

Card Reader

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: IO BOARD CONN.

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **DOCKING CONN.**

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+3VS +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,72,85,86>

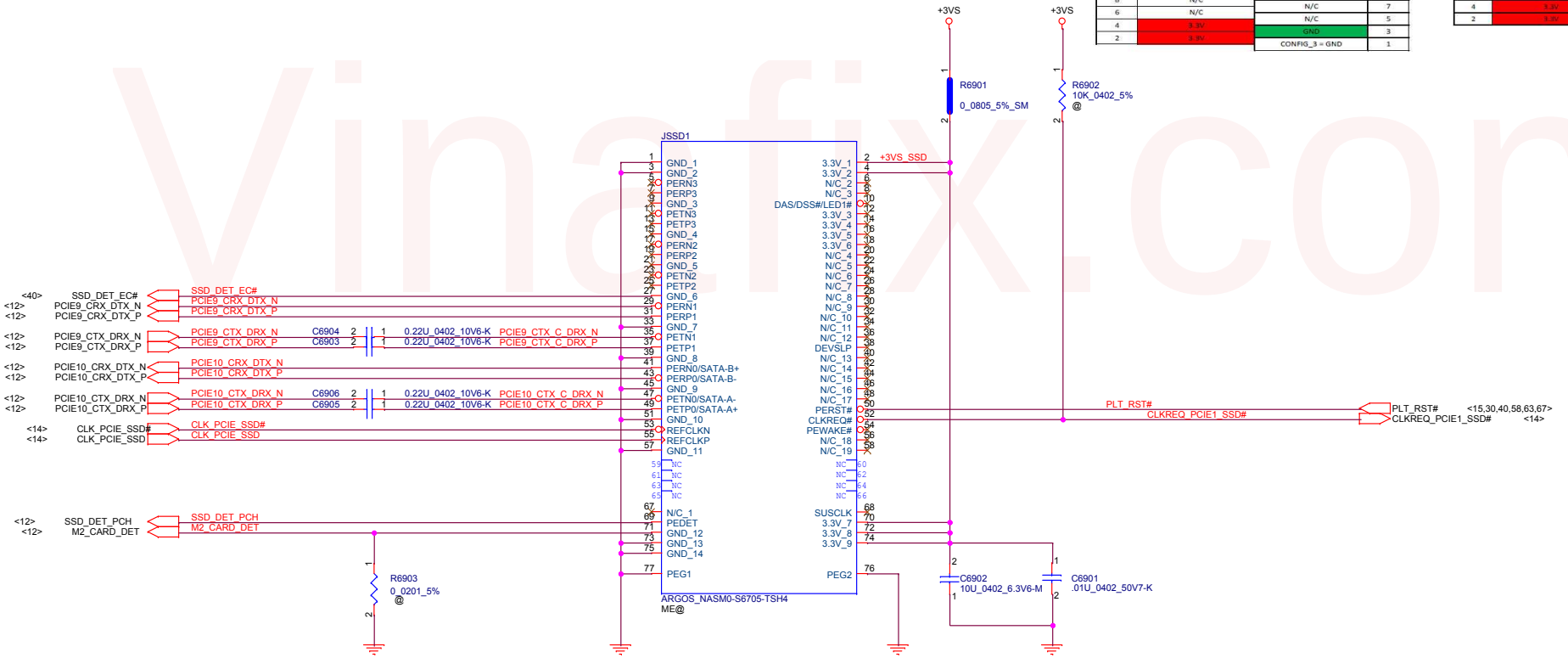
M.2 SSD(M TYPE)

Table 32. Socket 2 PCIe-based SSD Module Pinout

74	3.3V		CONFIG_2 = GND	75
72	3.3V		GND	73
70	3.3V		GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)		CONFIG_1 = NC	69
	Module Key		N/C	67
	Module Key		Module Key	
	Module Key		Module Key	
	Module Key		Module Key	
	Module Key		Module Key	
58	Reserved for MFG Clock		GND	57
56	Reserved for MFG Data		REFCLKP	55
54	PEWake# (IO)(0/3.3V)		REFCLKN	53
52	CLKREQ# (IO)(0/3.3V)		GND	51
50	PERST# (I)(0/3.3V)		PERp0	49
48	N/C		PERn0	47
46	N/C		GND	45
44	N/C		PETp0	43
42	N/C		PETn0	41
40	N/C		GND	39
38	DEVSLP (I)		PERp1	37
36	N/C		PERn1	35
34	N/C		GND	33
32	N/C		PETp1	31
30	N/C		PETn1	29
28	N/C		GND	27
26	N/C		N/C	25
24	N/C		N/C	23
22	N/C		CONFIG_0 = GND	21
20	N/C		Module Key	
	Module Key		Module Key	
	Module Key		Module Key	
	Module Key		Module Key	
	Module Key		Module Key	
10	DAS/DSS# (IO)		N/C	11
8	N/C		N/C	9
6	N/C		N/C	7
4	3.3V		N/C	5
2	3.3V		GND	3
			CONFIG_3 = GND	1

Table 35. Socket 3 PCIe-based Module Pinout

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	PEDET (NC-PCIe)	69
	Module Key	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved/MFG Clock	GND	57
56	Reserved/MFG Data	REFCLKP	55
54	PEWake# (IO)(0/3.3V)	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	N/C	PERn0	47
46	N/C	GND	45
44	N/C	PETp0	43
42	N/C	PETn0	41
40	N/C	GND	39
38	DEVSLP (I)	PERp1	37
36	N/C	PERn1	35
34	N/C	GND	33
32	N/C	PETp1	31
30	N/C	PETn1	29
28	N/C	GND	27
26	N/C	PERp2	25
24	N/C	PERn2	23
22	N/C	GND	21
20	N/C	PETp2	19
18	3.3V	PETn2	17
16	3.3V	GND	15
14	3.3V	PERp3	13
12	3.3V	PERn3	11
10	DAS/DSS# (IO)	GND	9
8	N/C	PETp3	7
6	N/C	PETn3	5
4	3.3V	GND	3
2	3.3V	GND	1



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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: M.2 SLOT CONN.

Size: Custom	Document Number: EE480_NM-B421	Rev: 0.2
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Security Classification	LC Future Center Secret Data		
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Title: BLANK

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+1VALW +1VALW <14,19,92>

+VCC_STG +VCC_STG <8,16,18>

+VCC_IO +VCC_IO <5,11,18,21>

+5VALW +5VALW <38,39,42,43,47,64,66,67,72,84,85,86,87,88,89,91,93,94>

+VCC_ST +VCC_ST <8,15,16,18,21,86>

+1VALW to +VCC_IO_AP & +VCC_ST

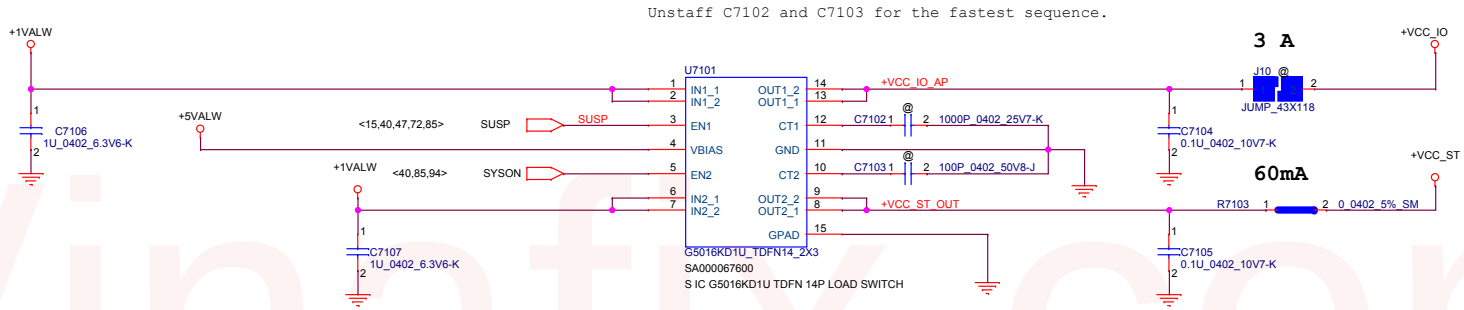
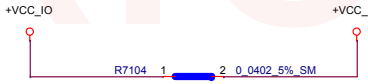


TABLE of POWER SWITCH (U7101)		
Vendor	LCFC P/N	Description
GMT	SA000067600	S IC G5016KD1U TDFN 14P LOAD SWITCH
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH



Slew Rate=10uS<TR<65us

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: VCCIO/VCCSTG/VCCST

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.2

Date: Monday, October 30, 2017 | Sheet 71 of 99

+5VALW — +5VALW <38,39,42,43,47,64,66,67,71,84,85,86,87,88,89,91,93,94>

+5VS — +5VS <47,50,51,60,61,65,66>

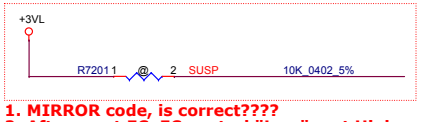
+3VALW — +3VALW <6,9,12,15,19,40,50,58,60,63,65,66,67,83,84,91,95>

+3VS — +3VS <5,6,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,51,57,58,59,60,61,63,65,66,67,69,85,86>

+3VALW_PCH — +3VALW_PCH <8,9,10,11,12,19>

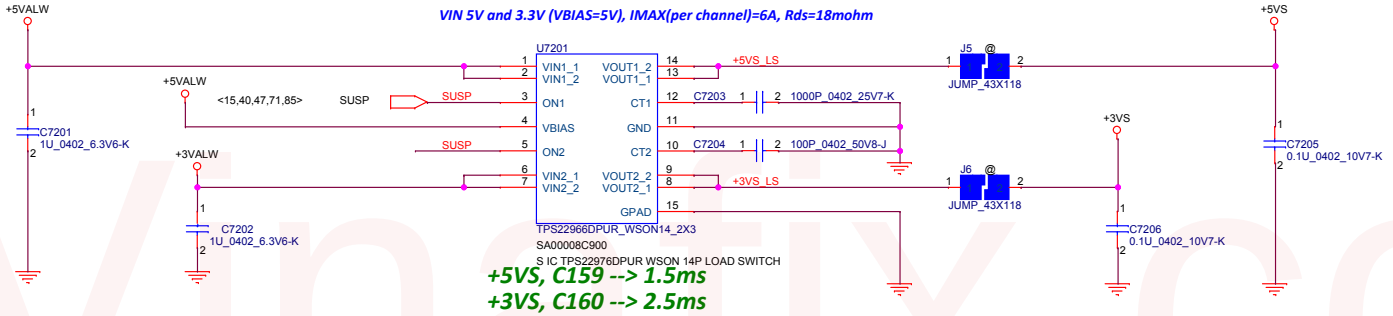
+3VL — +3VL <19,40,42,50,67,80,82,83,84>

+1VALW_SUS — +1VALW_SUS <19>



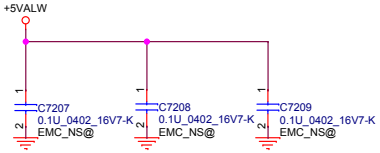
1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.

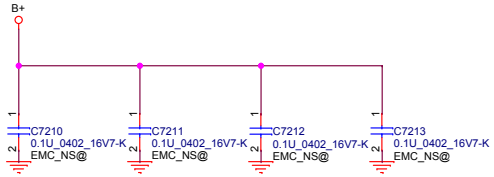
Smart Switch
+5VALW To +5VS
+3VALW To +3VS



+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms

TABLE of POWER SWITCH (U7201)		
Vendor	**LCFC P/N**	**Description**
TI	**SA00008C900**	**S IC TPS22976DPUR WSON 14P LOAD SWITCH**
GMT	**SA000067600**	**S IC G5016KD1U TDFN 14P LOAD SWITCH**





Title: **DC V TO VS/ V-PCH**

Size: Custom | Document Number: **EE480 NM-B421** | Rev: 0.2

Date: Monday, October 30, 2017 | Sheet 72 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **BLANK**

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

Date: Monday, October 30, 2017 Sheet 73 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **BLANK**

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

Date: Monday, October 30, 2017 Sheet 74 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **BLANK**

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

Date: Monday, October 30, 2017 Sheet 75 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: *BLANK*

Size	Document Number	Rev
Custom	*EE480 NM-B421*	0.2

Date: Monday, October 30, 2017 | Sheet 76 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: BLANK

Size	Document Number	Rev
C	EE480 NM-B421	0.2

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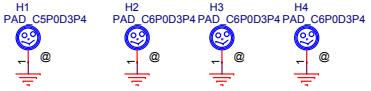
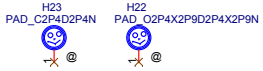
Screw Hole

CPU



WLNN



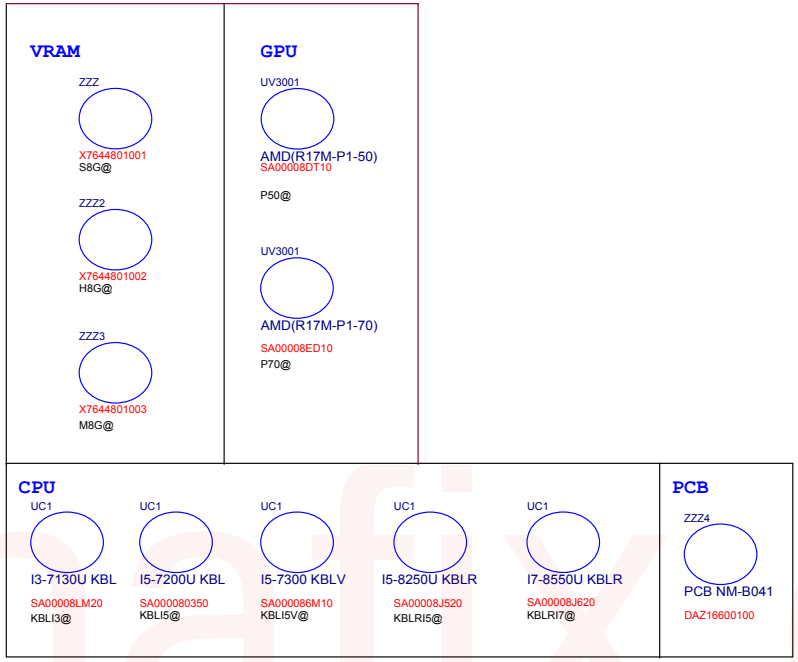
PCB Fedical Mark PAD

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: SCREW HOLE

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

Date: Monday, October 30, 2017 Sheet 78 of 99

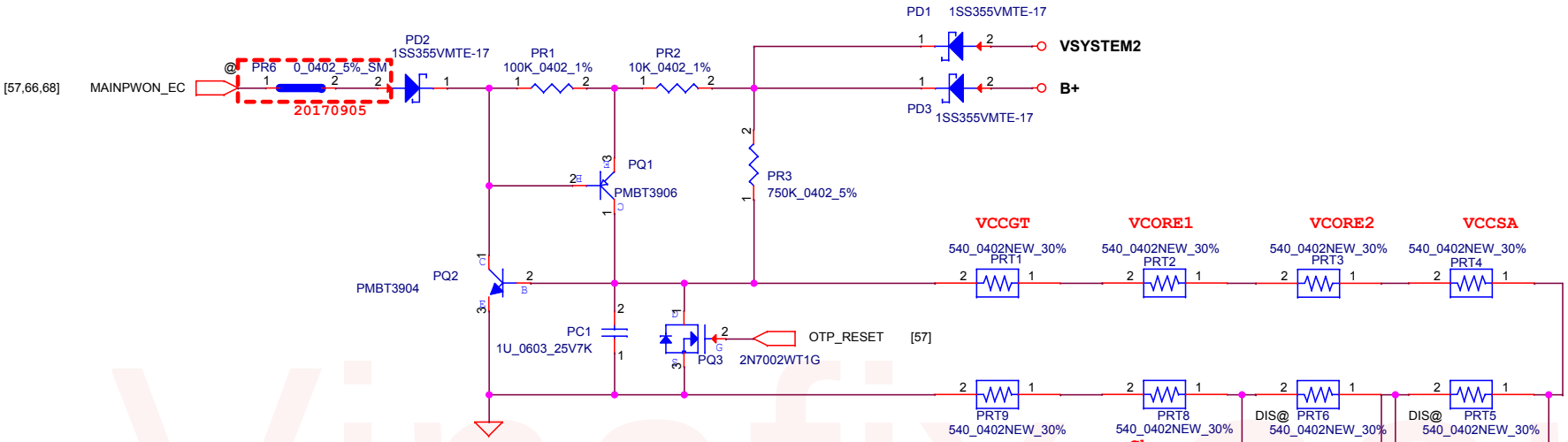


Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/12/31

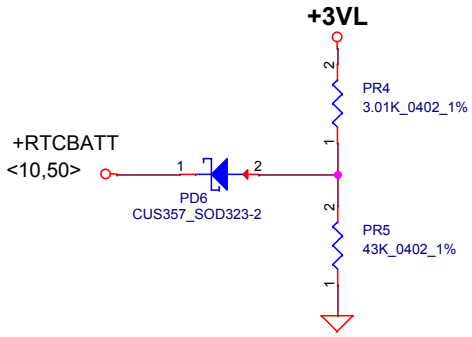
Title: **PLM BOM**

Size	Document Number	Rev
Custom	EE480 NM-B421	0.2

Date: Monday, October 30, 2017 Sheet 79 of 99



RTC Battery



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *VIN Detector*

Size: Custom | Document Number: *EE480 NM-B421* | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet 80 of 99

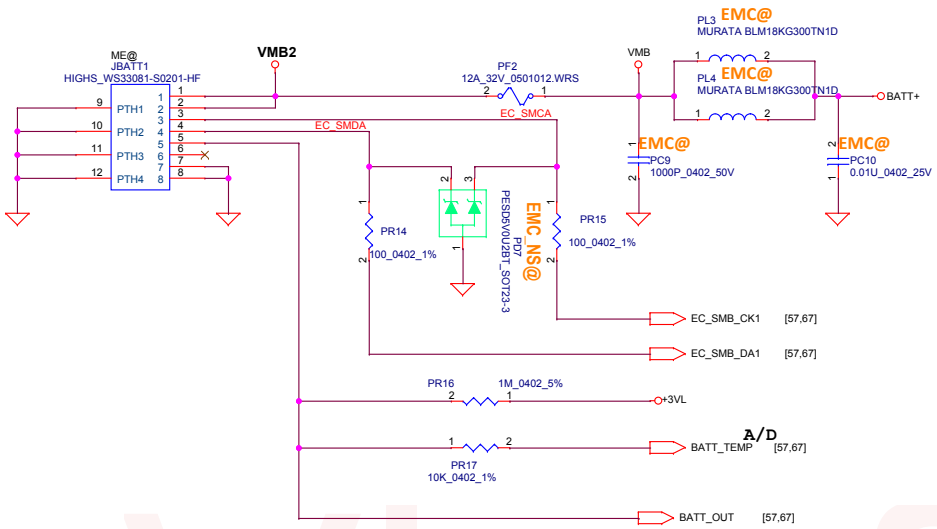
BLANK

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

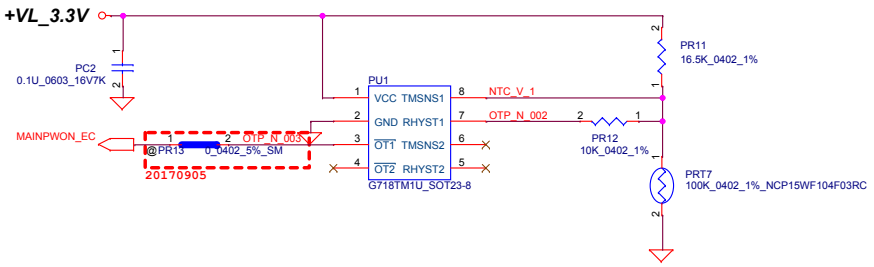
Title: XXXX

Size	Document Number	Rev
Custom	EE480 NM-B421	2.0

Date: Monday, October 30, 2017 | Sheet 81 of 99



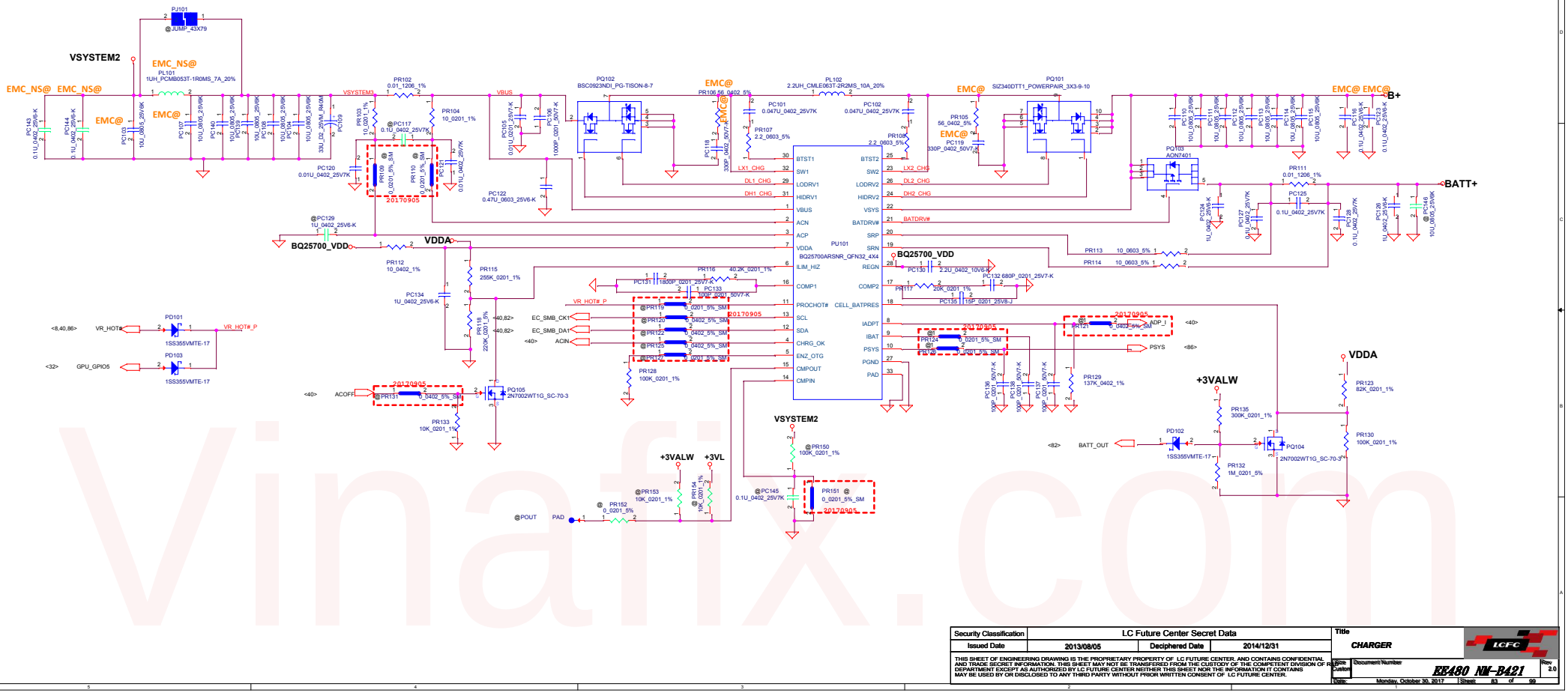
PRT7 under CPU bottom side for CPU thermal protection. This is for thermal team request.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: ***BATTERY CONN/OTP***

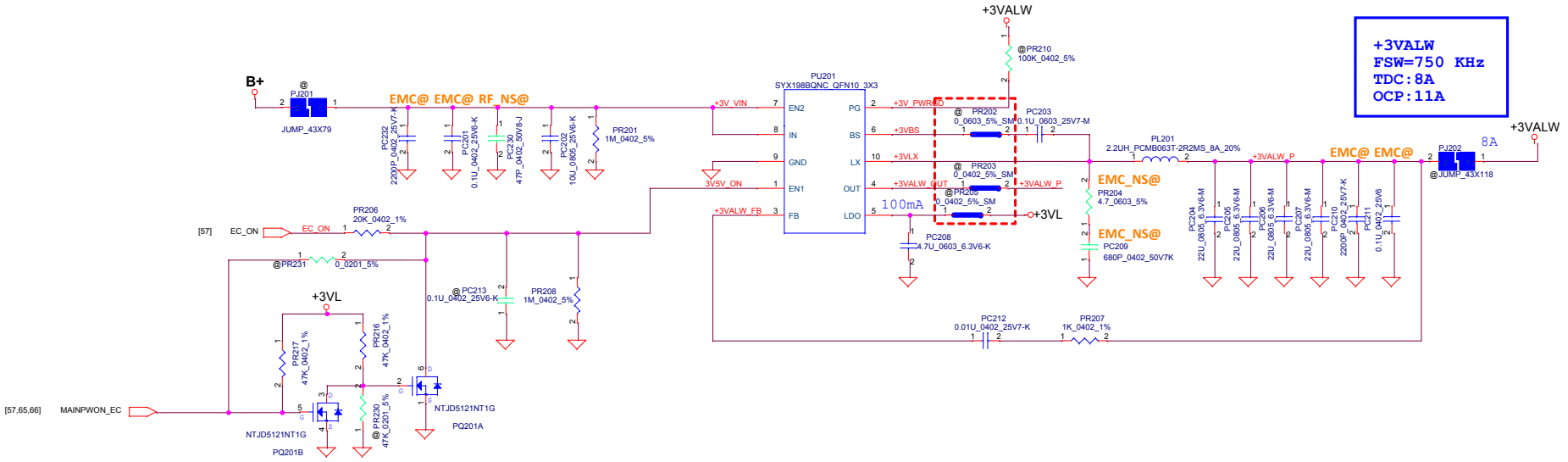
Size: Custom	Document Number: ***EE480 NM-B421***	Rev: 2.0
Date: Monday, October 30, 2017	Sheet 82 of 99	

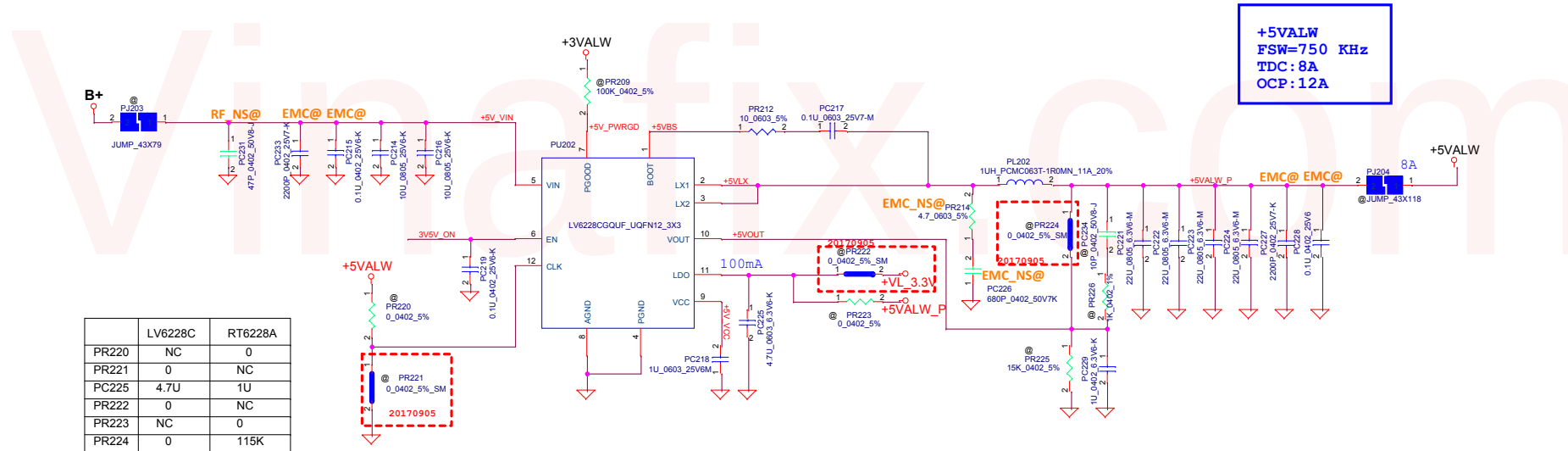


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: CHARGER

Size: Custom	Document Number: EE480 NM-B421	Rev: 2.0
Date: Monday, October 30, 2017	Sheet 83 of 99	





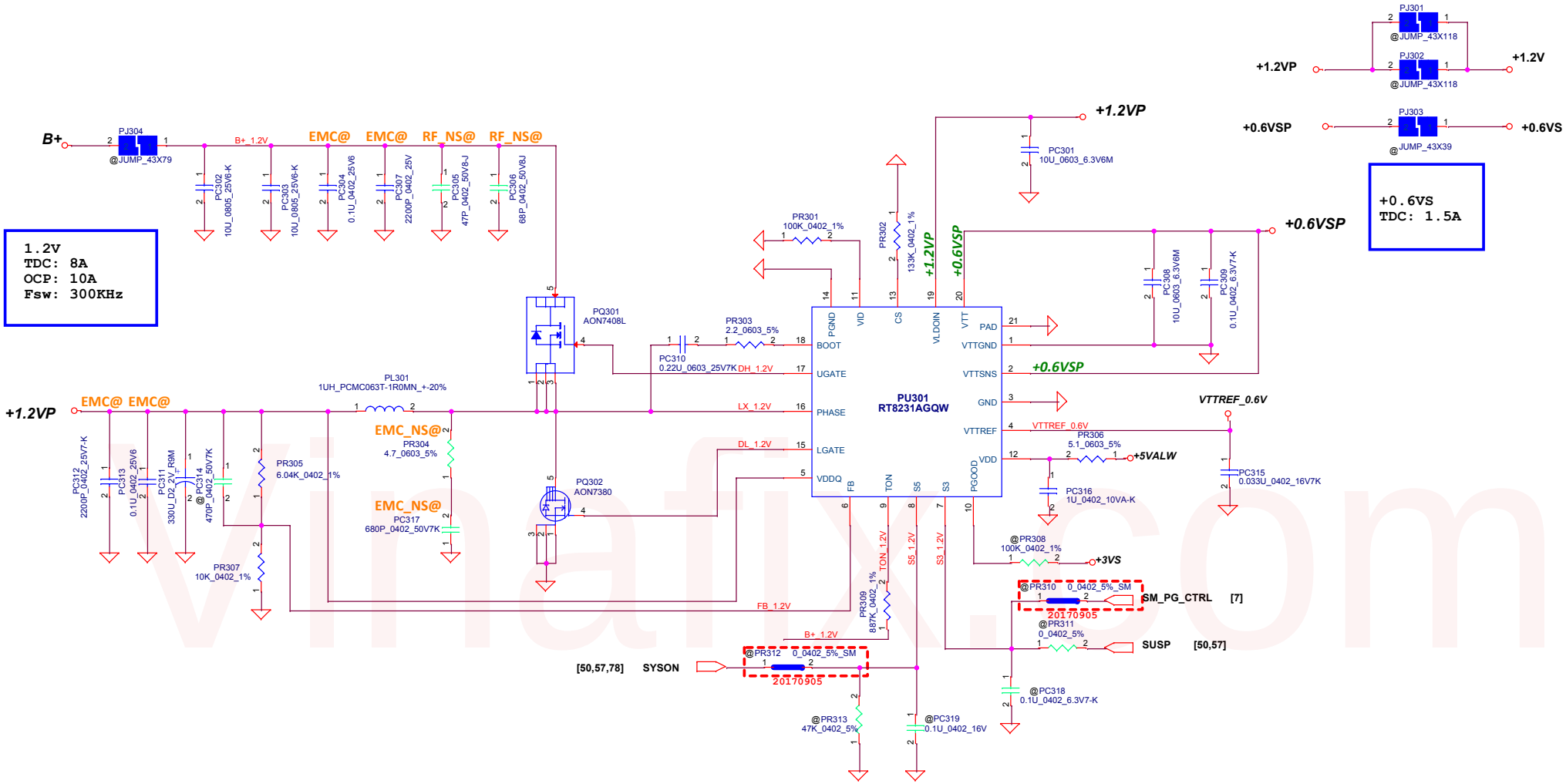
	LV6228C	RT6228A
PR220	NC	0
PR221	0	NC
PC225	4.7U	1U
PR222	0	NC
PR223	NC	0
PR224	0	115K
PR225	NC	15K
PC234	NC	10P
PR226	NC	1K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: 3VALWP/5VALWP

Size: Custom | Document Number: EE480 NM-B421 | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet 84 of 99

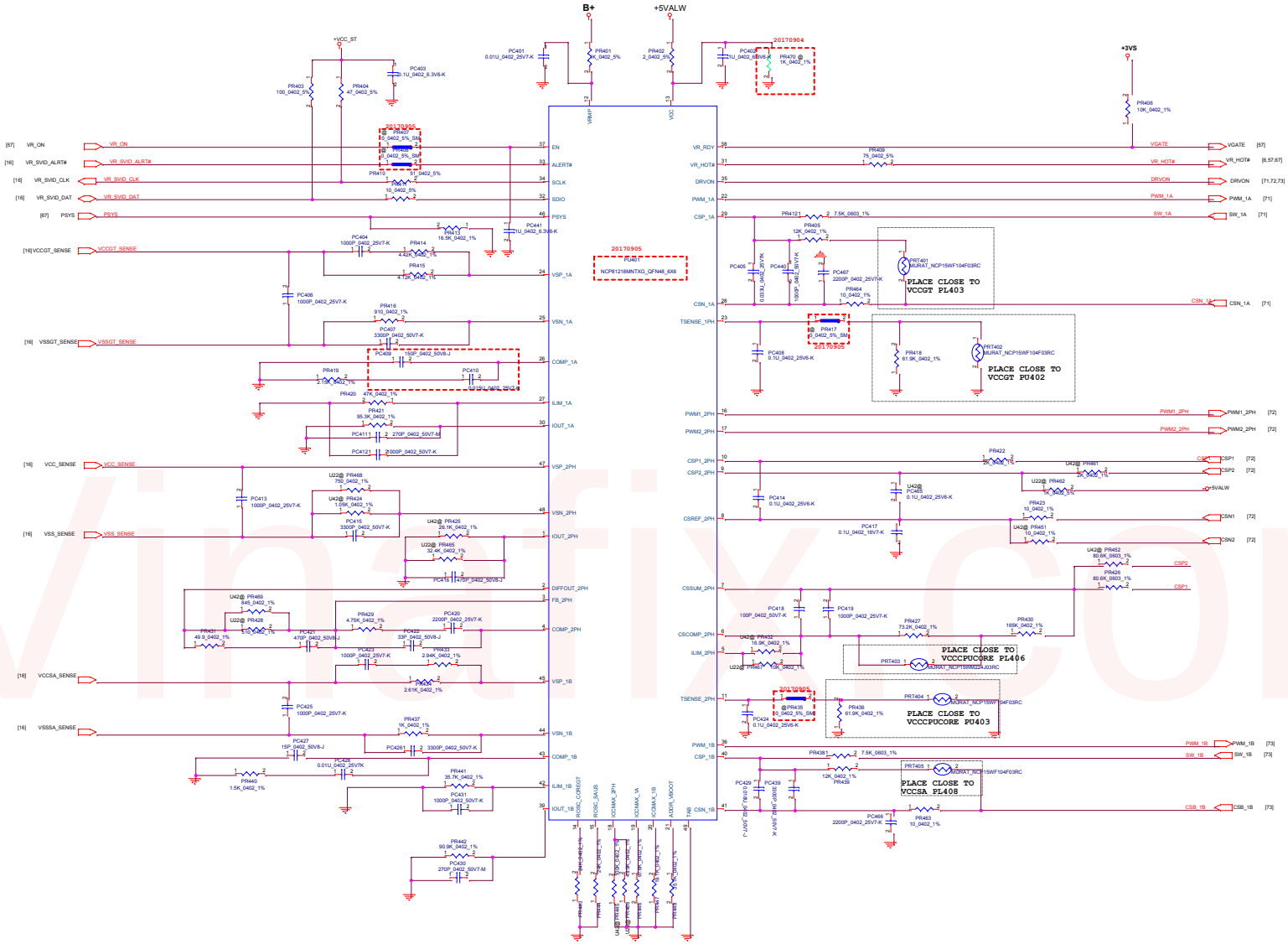


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.2V/+0.6VS

Size: Custom | Document Number: EE480 NM-B421 | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet 85 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: IMVP8

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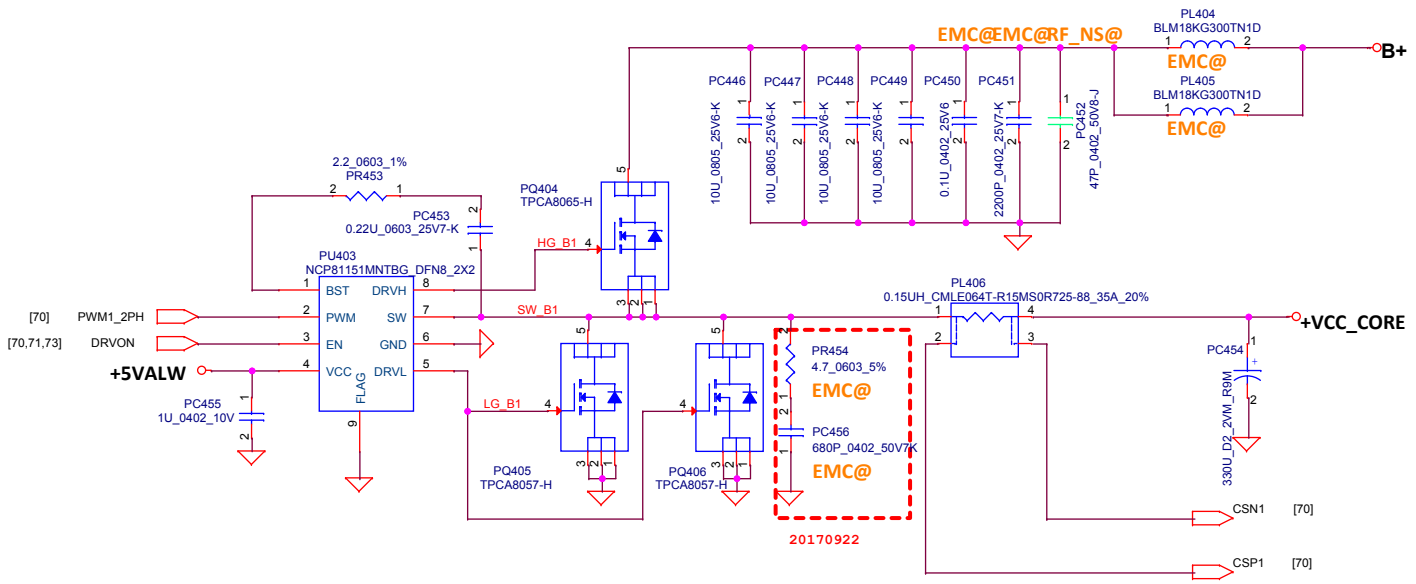
Size: D | Document Number: EX480 NM-B431 | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet: 44 of 60



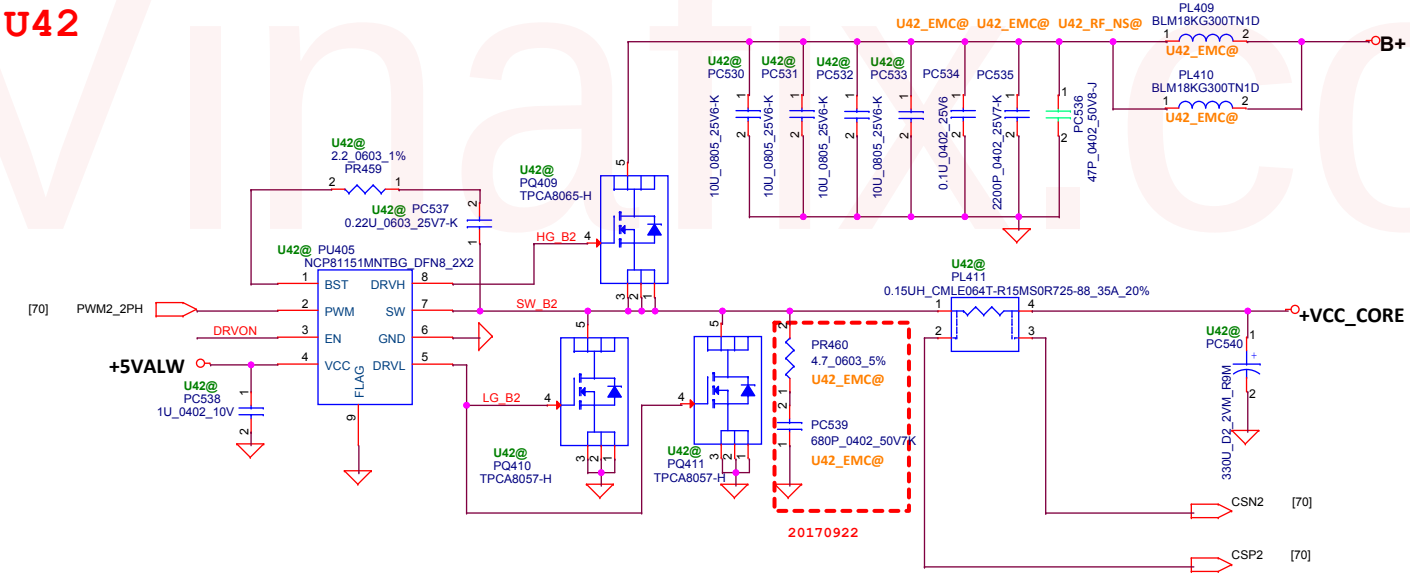
For U42

+VCC_CORE
TDC= 42A
IccMAX=64A
OCP=70A

For U22

+VCC_CORE
TDC= 21A
IccMAX=31A
OCP = 36A

For U42

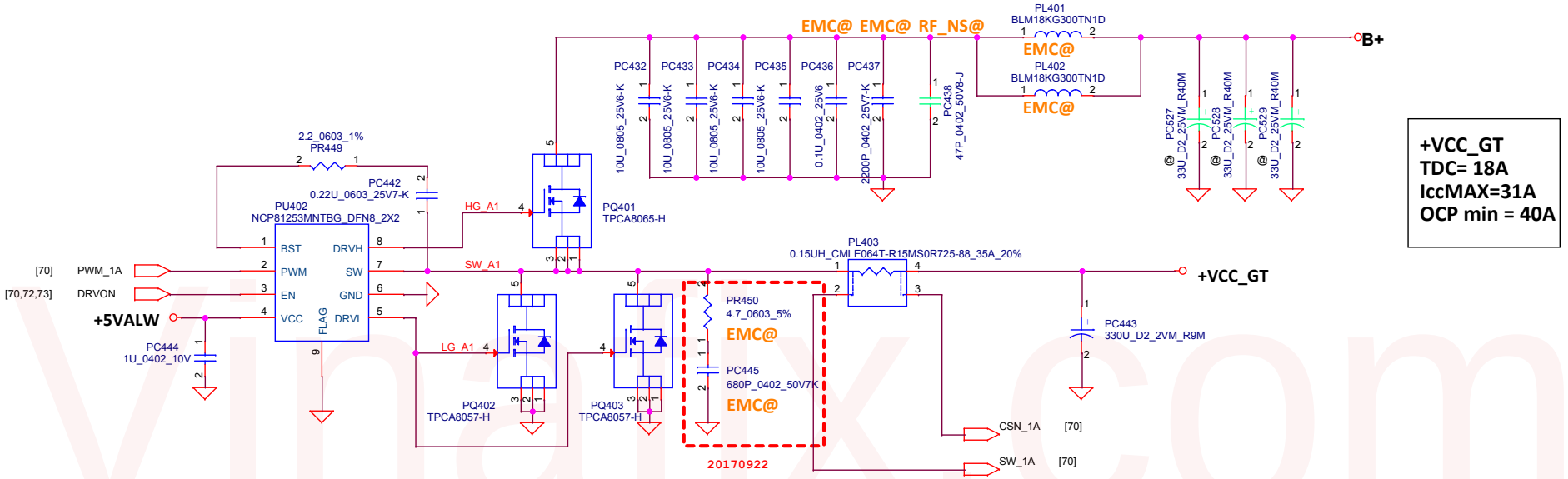


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_CORE

Size: Custom | Document Number: EE480 NM-B421 | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet 87 of 99

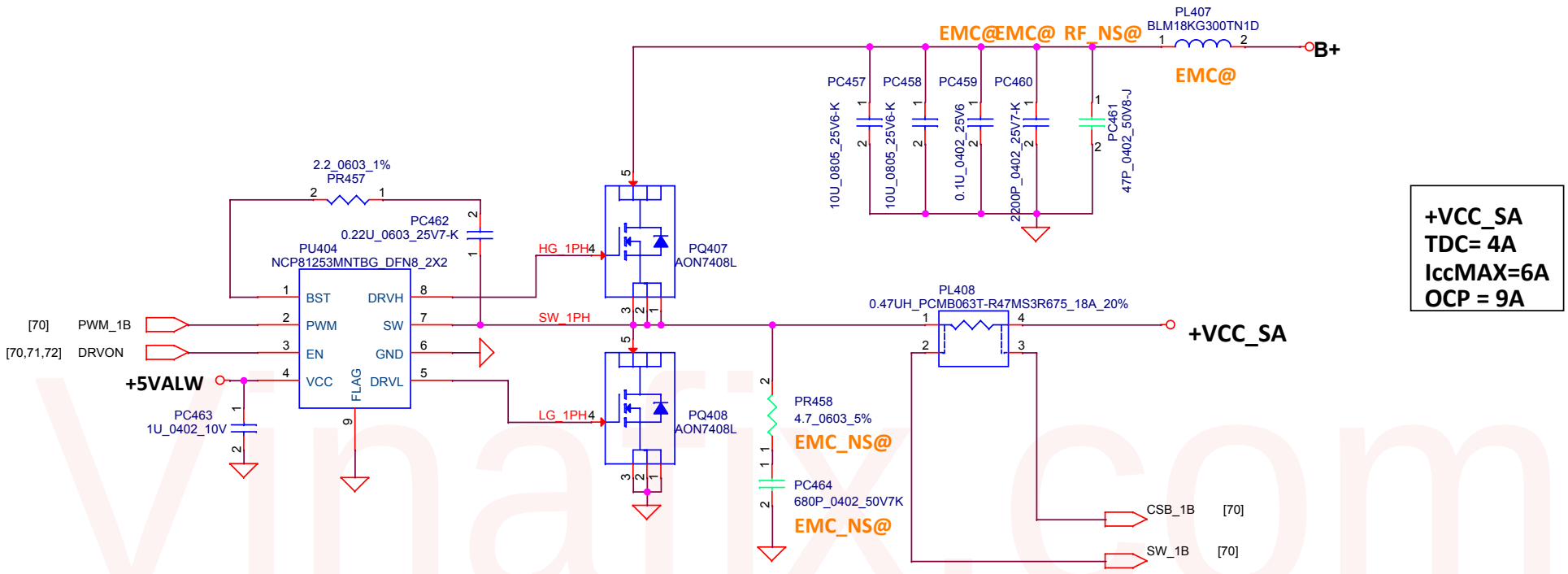


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_GT

Size: Custom | Document Number: EE480 NM-B421 | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet 88 of 99

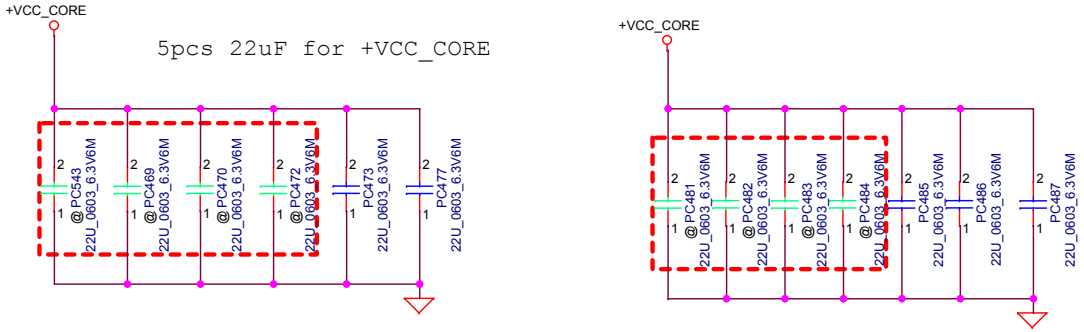


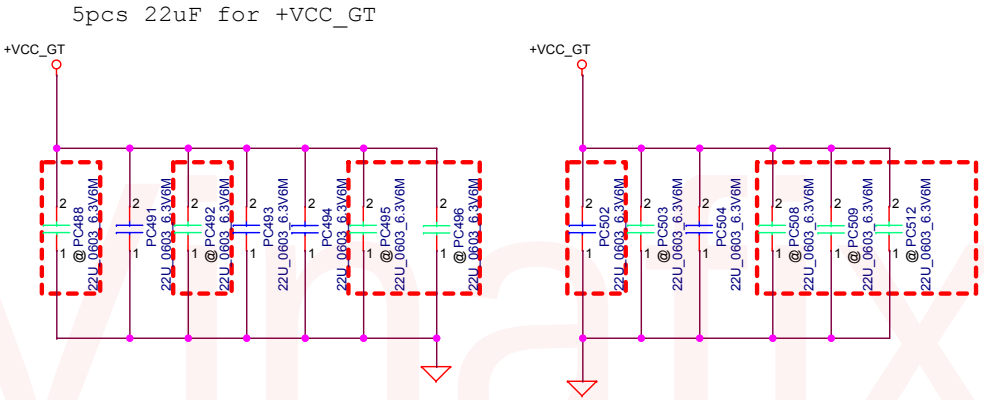
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

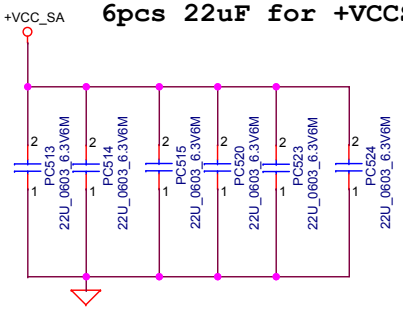
Title: +VCC_SA

Size: Custom | Document Number: EE480 NM-B421 | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet 89 of 99







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

Size: B	Document Number: EE480 NM-B421	Rev: 2.0
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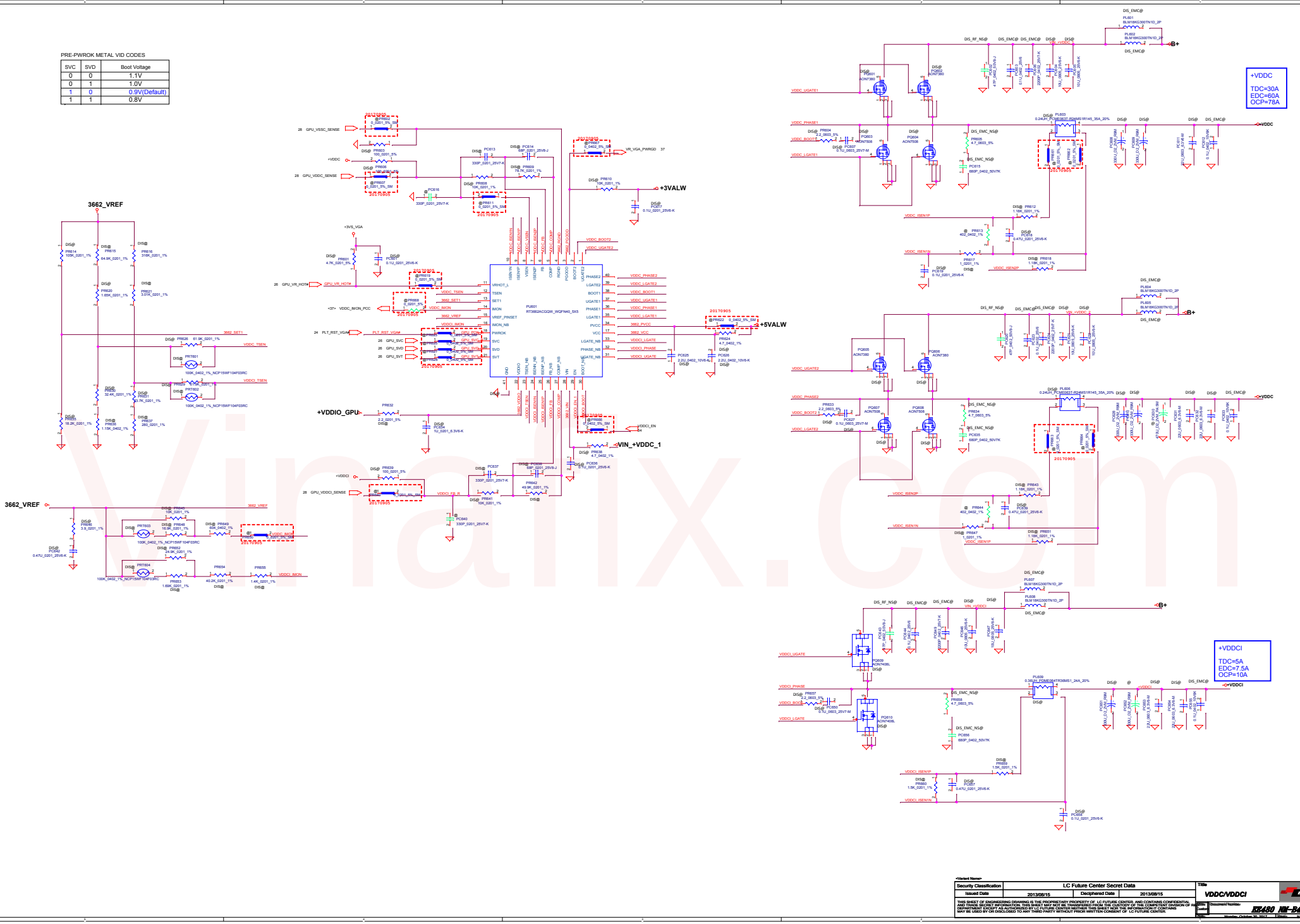
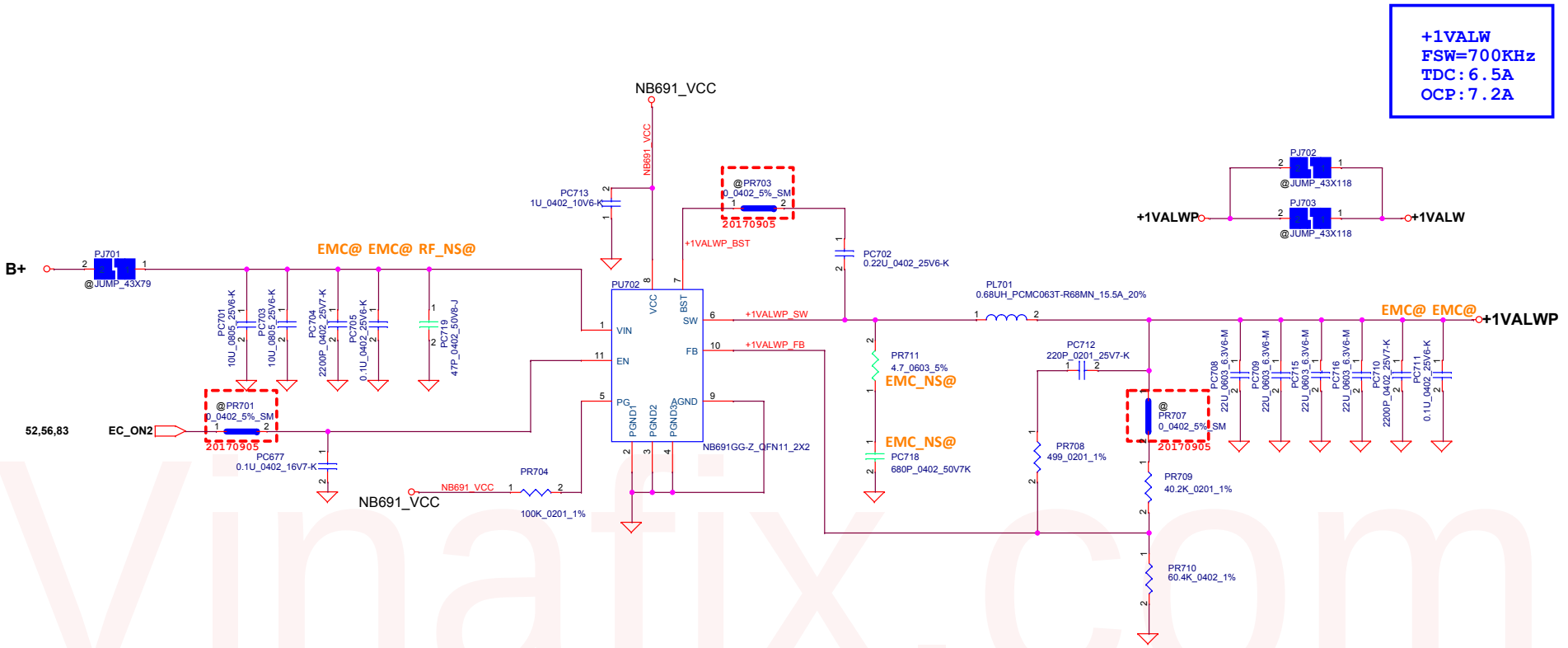
PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V



<Variant Name>			
Security Classification	LC Future Center Secret Data		Title: VDDC/VDDCI
Issued Date	2013/08/15	Deciphered Date	2013/08/15
Drawn By:	Document Number: KK480 NM-B481		Rev: 0.1
Date: Monday, October 14, 2013	Sheet 44 of 46		

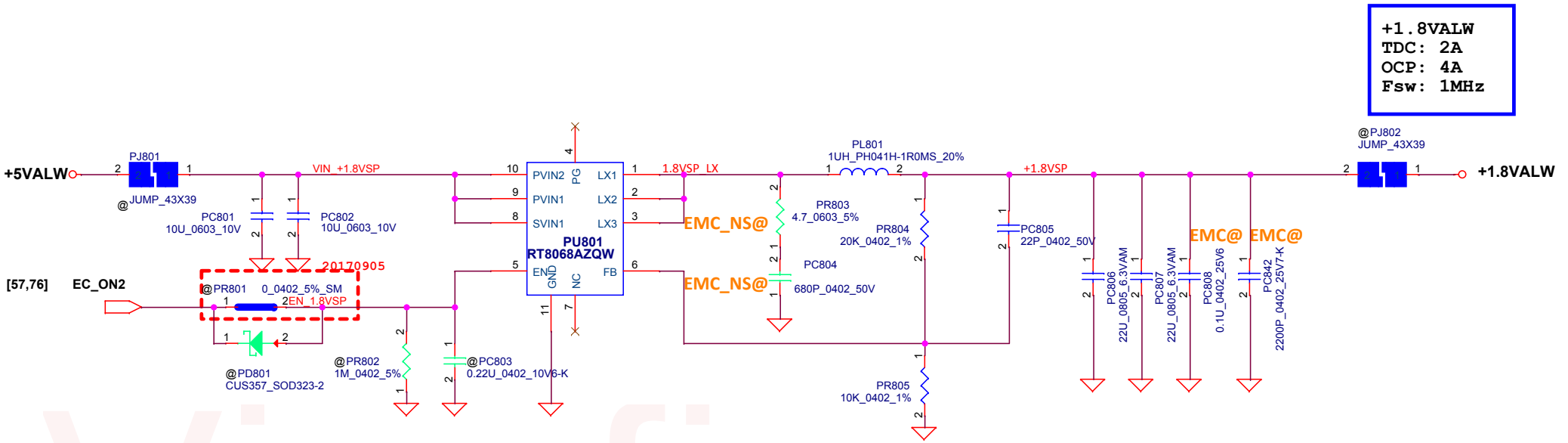


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1V

Size: Custom | Document Number: EE480 NM-B421 | Rev: 0.1

Date: Monday, October 30, 2017 | Sheet 92 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.8VALW

Size	Document Number	Rev
Custom	EE480 NM-B421	2.0

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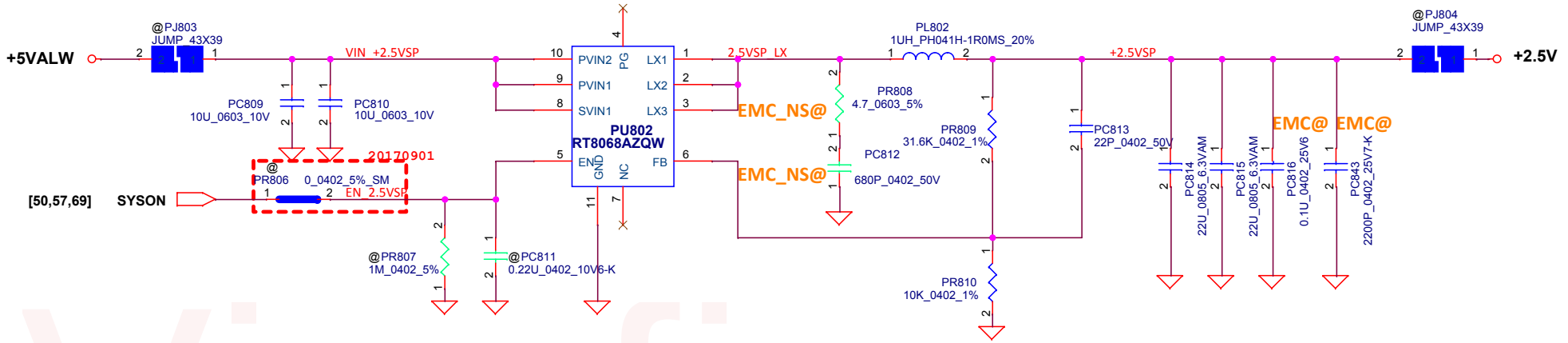
+2.5V
TDC: 2A
OCP: 4A
Fsw: 1MHz

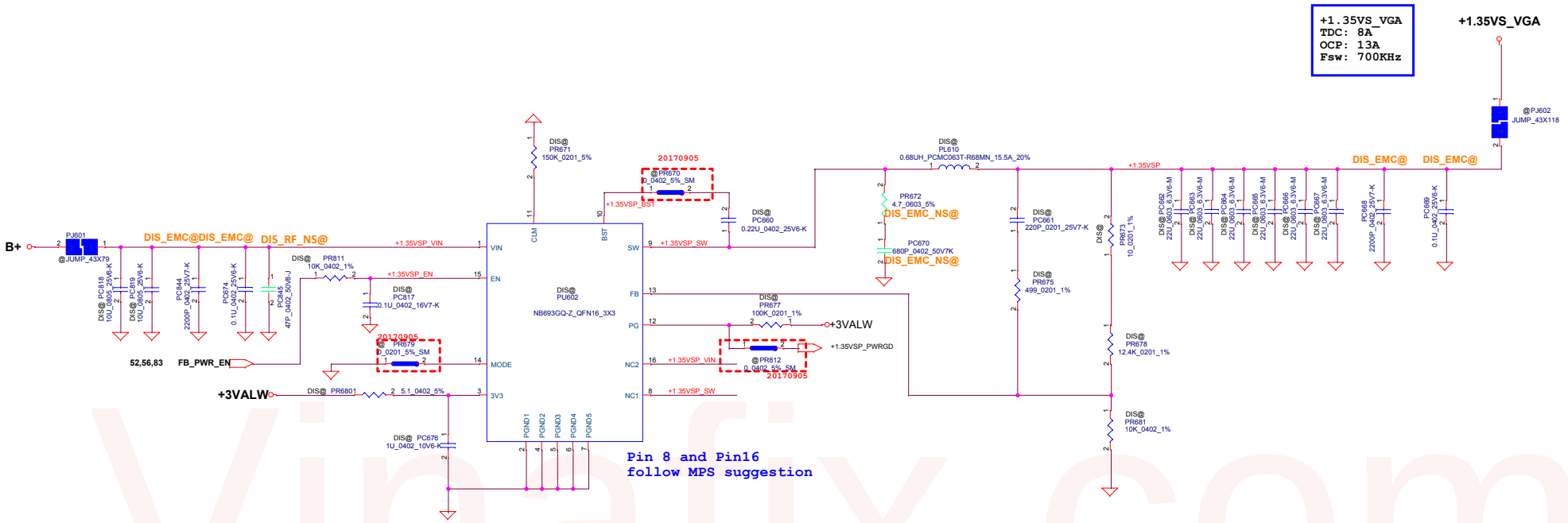


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +2.5V

Size	Document Number	Rev
Custom	EE480 NM-B421	2.0

Date: Monday, October 30, 2017 Sheet 94 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

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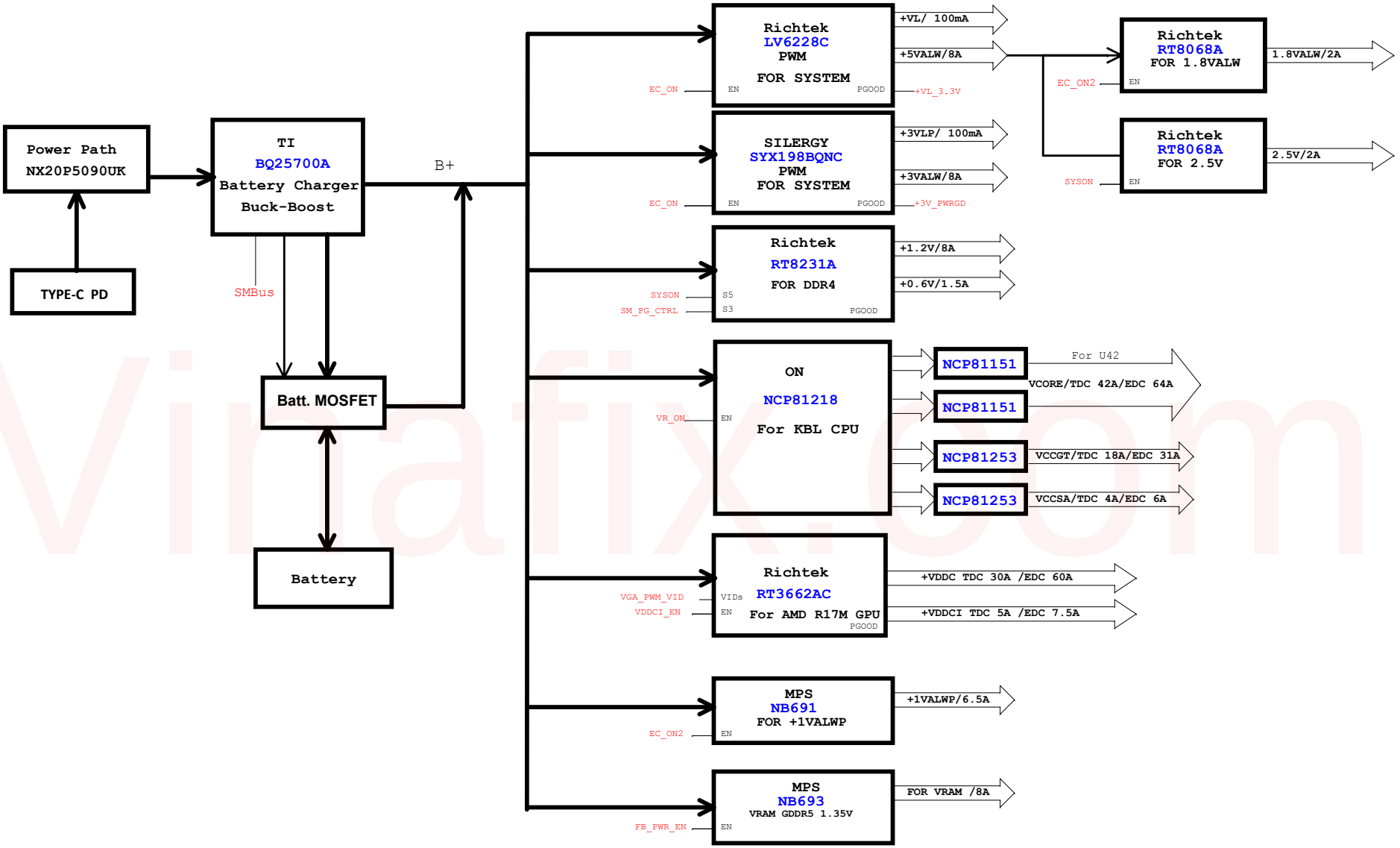
Title: +1.35VS_VGA

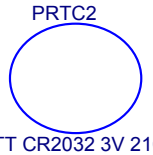
Size: Custom | Document Number: EE480 NM-B421 | Rev: 2.0

Date: Monday, October 30, 2017 | Sheet 65 of 99



Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title	Power Block Diagram		
Size: Custom	Document Number: EE480 NM-B421		Rev: 2.0
Date: Monday, October 30, 2017	Sheet 96 of 99		



RTC@

EE480

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, October 30, 2017	Sheet 97 of 99	

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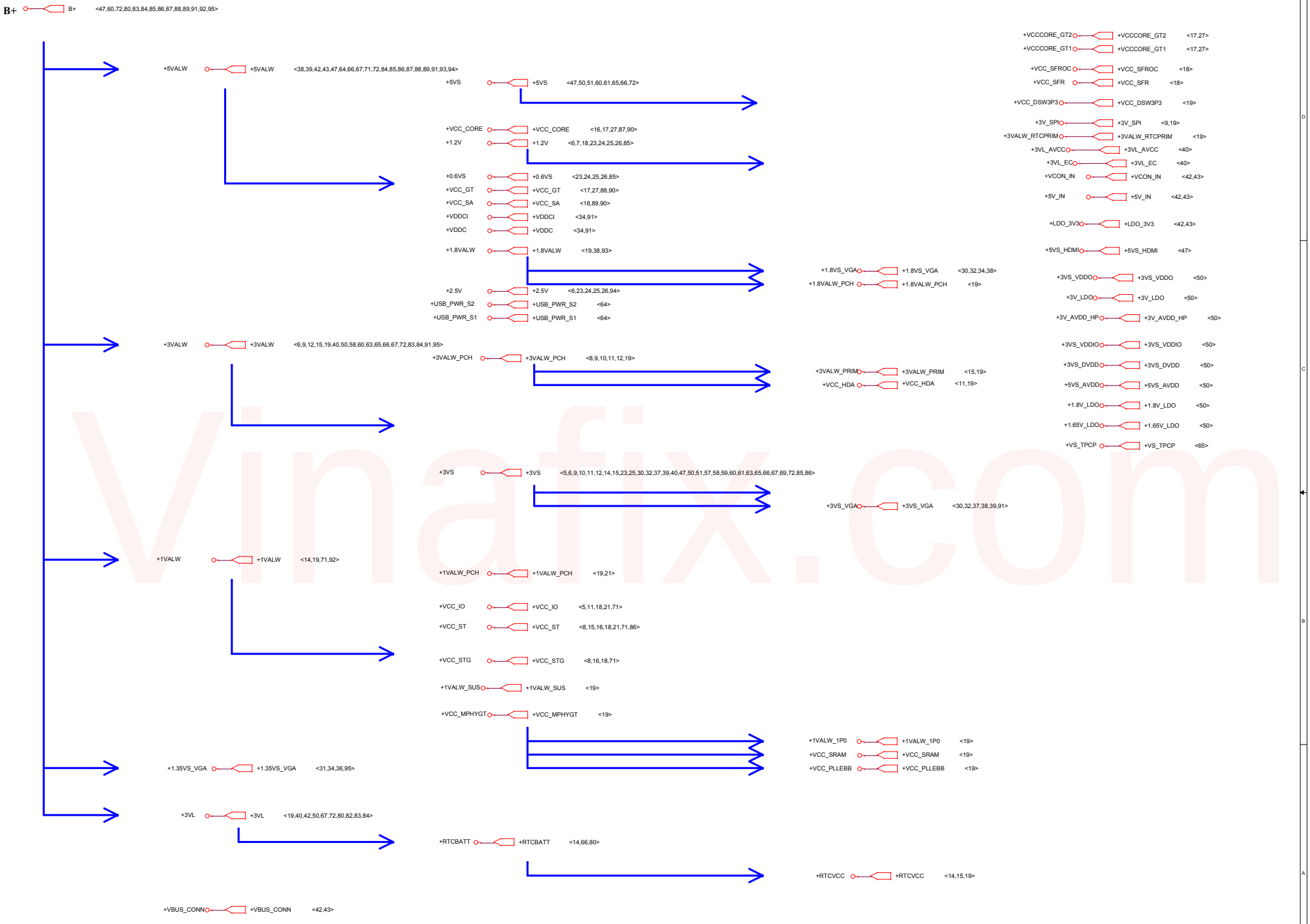
Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: XXXX

Size	Document Number	Rev
Custom	EE480 NM-B421	2.0

Date: Monday, October 30, 2017 | Sheet 98 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/08	Deciphered Date	2013/11/08

Title	LOAD BOM ONLY		
Size C	Document Number		Rev 0.2
Date: Monday, October 30, 2017	Sheet 99 of 99		

LCFC Confidential

Dooku

E480

NS-B421 Rev1.0 Schematic

Intel KBL-R Processor with DDR4

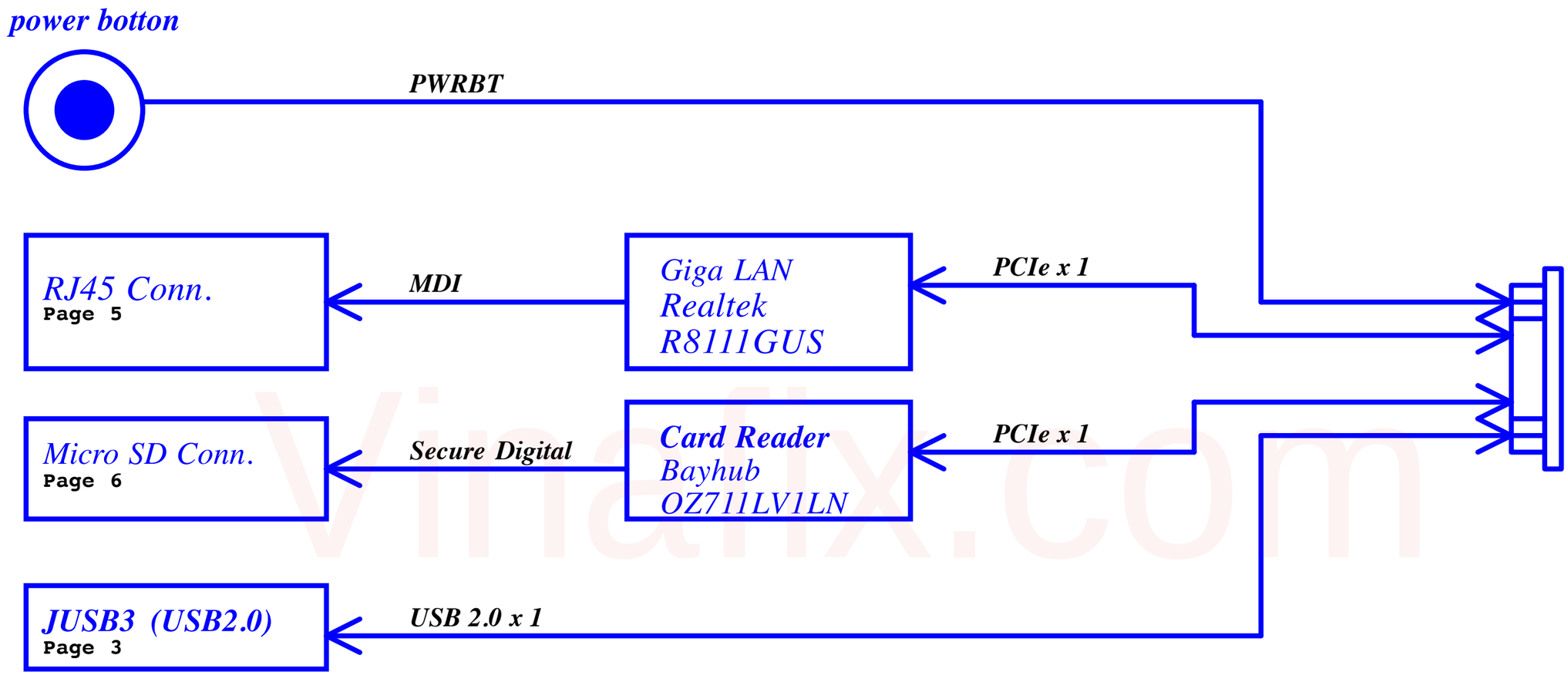
AMD R17M-P1-50/70

2017-09-27 Rev1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/17	Deciphered Date	2017/12/31

Title	COVER PAGE	
Size: Custom	Document Number: E480 NS-B421	Rev: 1.0
Date: Wednesday, September 27, 2017	Sheet 1 of 7	

IO_Board



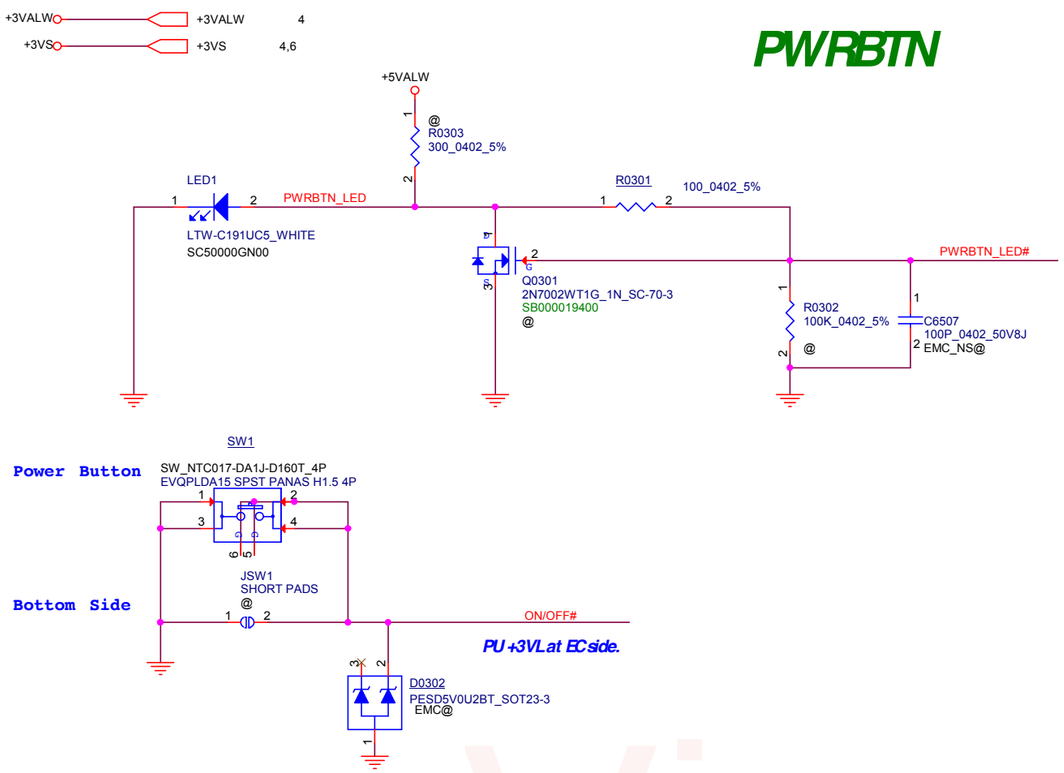
Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/17	Deciphered Date	2017/12/31

Title: **BLOCK DIAGRAM**

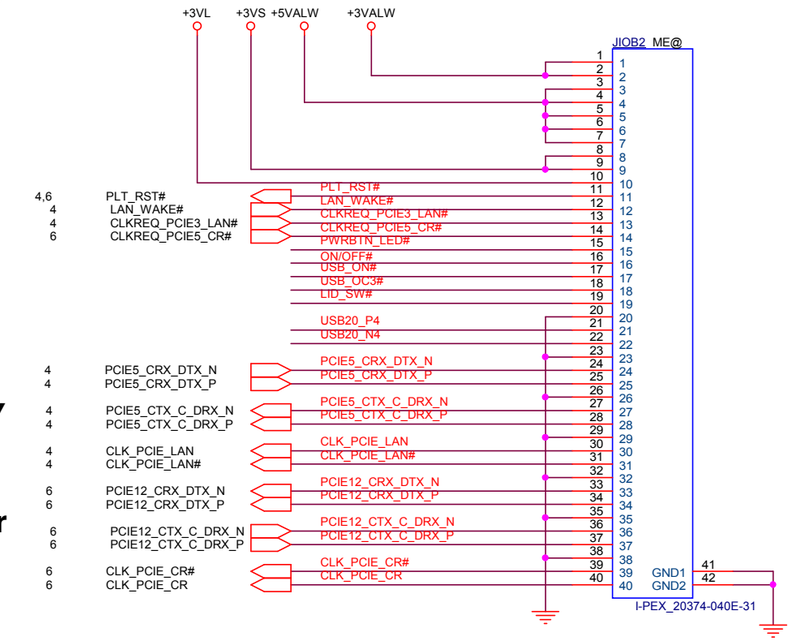
LCFC

Size: Custom	Document Number: E480 NS-B421	Rev: 1.0
Date: Wednesday, September 27, 2017	Sheet 2 of 7	

PWRBTN



IO_40_Pin conn

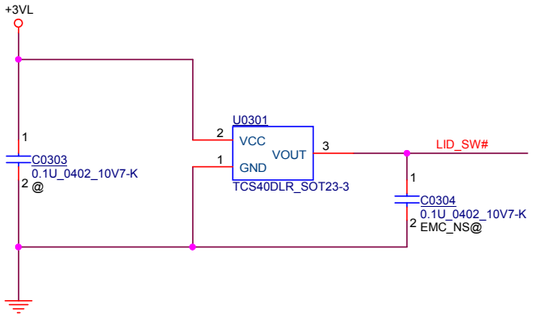


USB2.0

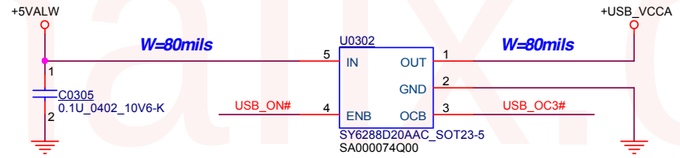
GBE LAN PHY

Card Reader

Lid Switch



JUSB4(USB2.0)



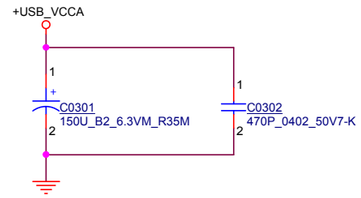
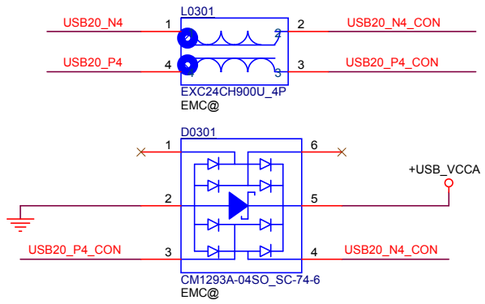
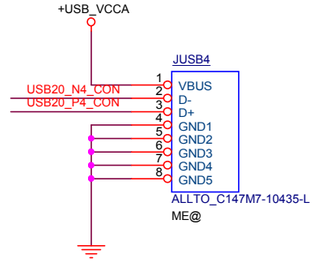


TABLE of POWER SWITCH (U0302)		
Vendor	LCFC P/N	Description
SILERGY	SA000074Q00	S IC SY6288D20AAC SOT23 5P POWER SWITCH
GMT	SA000079400	S IC G517F2T11U SOT-23 5P POWER SWITCH





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Title			
PBTN/FAN CONN.			
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+3VALW <-> +3VALW 3

+3VS <-> +3VS 3,6

+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms<spec<100m s

+3VALW -- R0402 0_0805_SM (@) -- +3VALW_LAN

width : 40 mils

+3VALW_LAN:
- C0402 4.7U_0603_6.3V6-K (@) — Close to Pin11
- C0403 4.7U_0603_6.3V6-K (@) — Close to Pin32
- C0404 0.1U_0402_10V7-K — Close to Pin11
- C0405 0.1U_0402_10V7-K — Close to Pin32

+3VALW_LAN -- R0404 10K_0402_5% (@) -- LAN_CLKREQ#_R

+3VS -- Q0401 2N7002KW_SOT323-3 (@) -- CLKREQ_PCIE3_LAN# 3

R0405 0_0402_SM (@)

+3VALW_LAN -- R0407 10K_0402_5% (@) -- LAN_WAKE#_R

3 LAN_WAKE# -- R0408 0_0402_SM -- LAN_WAKE#_R

CL10 close to Pin18
CL9 close to Pin17

3 PCIE5_CRX_DTX_P
3 PCIE5_CRX_DTX_N
PCIE5_CRX_DTX_P -- C0409 0.1U_0402_10V7-K -- PCIE5_CRX_C_DTX_P
PCIE5_CRX_DTX_N -- C0410 0.1U_0402_10V7-K -- PCIE5_CRX_C_DTX_N
3,6 PLT_RST# -- PLT_RST#

+3VS -- R0409 1K_0402_5% -- ISOLATE#
ISOLATE# -- R0411 15K_0402_5% -- +3VS

+3VALW_LAN -- R0412 10K_0402_5% (@) -- LED1

TL2 RJ45_LINKUP#
TL3 LED1
TL4 RJ45_ACTIVITY#

5 RJ45_LINKUP#
5 RJ45_ACTIVITY#

UL0401 RTL8111GUS-CG_QFN32_4X4

+3VALW_LAN	11	AVDD33_1	
+3VALW_LAN	32	AVDD33_2	
PCIE5_CRX_C_DTX_P	17	HSOP	
PCIE5_CRX_C_DTX_N	18	HSON	
PLT_RST#	19	PERSTB	
ISOLATE#	20	ISOLATEB	
LAN_WAKE#_R	21	LANWAKEB	
+LAN_VDDREG	23	VDDREG	
+LAN_REGOUT	24	REGOUT	
RJ45_LINKUP#	25	LED2	
LED1	26	LED1/GPO	
RJ45_ACTIVITY#	27	LED0	
LAN_XTALO	28	CKXTAL1	
LAN_XTALI	29	CKXTAL2	
	33	GND	

AVDD10_1	3	+LAN_VDD10	
AVDD10_2	8	+LAN_VDD10	
AVDD10_3	30	+LAN_VDD10	
DVDD10	22	+LAN_VDD10	
MDIP0	1	MDI_0+	MDI_0+ 5
MDIN0	2	MDI_0-	MDI_0- 5
MDIP1	4	MDI_1+	MDI_1+ 5
MDIN1	5	MDI_1-	MDI_1- 5
MDIP2	6	MDI_2+	MDI_2+ 5
MDIN2	7	MDI_2-	MDI_2- 5
MDIP3	9	MDI_3+	MDI_3+ 5
MDIN3	10	MDI_3-	MDI_3- 5
HSIP	13	PCIE5_CTX_C_DRX_P	PCIE5_CTX_C_DRX_P 3
HSIN	14	PCIE5_CTX_C_DRX_N	PCIE5_CTX_C_DRX_N 3
CLKREQB	12	LAN_CLKREQ#_R	
REFCLK_P	15	CLK_PCIE_LAN	CLK_PCIE_LAN 3
REFCLK_N	16	CLK_PCIE_LAN#	CLK_PCIE_LAN# 3
RSET	31	RSET	

RSET -- R0406 2.49K_0402_1%

+3VALW_LAN -- 0_0603_SM -- R0403 -- +LAN_VDDREG
- C0401 4.7U_0603_6.3V6-K
- C0406 0.1U_0402_10V7-K

LAN_XTALI -- Y0401 (OSC1, GND1, GND2, OSC2) 25MHZ_10PF_7V25000014 -- LAN_XTALO
- C0411 12P_0402_50V8-J
- C0412 10P_0402_50V8-J

Change from 12PF to 10PF as vendor suggest on 20170508

+LAN_VDD10 -- L0401 2.2UH_EP-22AM05B02_2A_20% -- +LAN_REGOUT

Layout Note: L0401 must be within 200mil to Pin24, C0414,C0415 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

+LAN_VDD10:
- C0414 4.7U_0603_6.3V6-K
- C0415 0.1U_0402_10V7-K
- C0416 0.1U_0402_10V7-K — Close to Pin3, 8, 22, 30
- C0417 0.1U_0402_10V7-K
- C0418 0.1U_0402_10V7-K — LAYOUT NEED CHECK
- C0419 0.1U_0402_10V7-K
- C0420 1U_0402_10V6-K (@) — Close to Pin22(Reserved)

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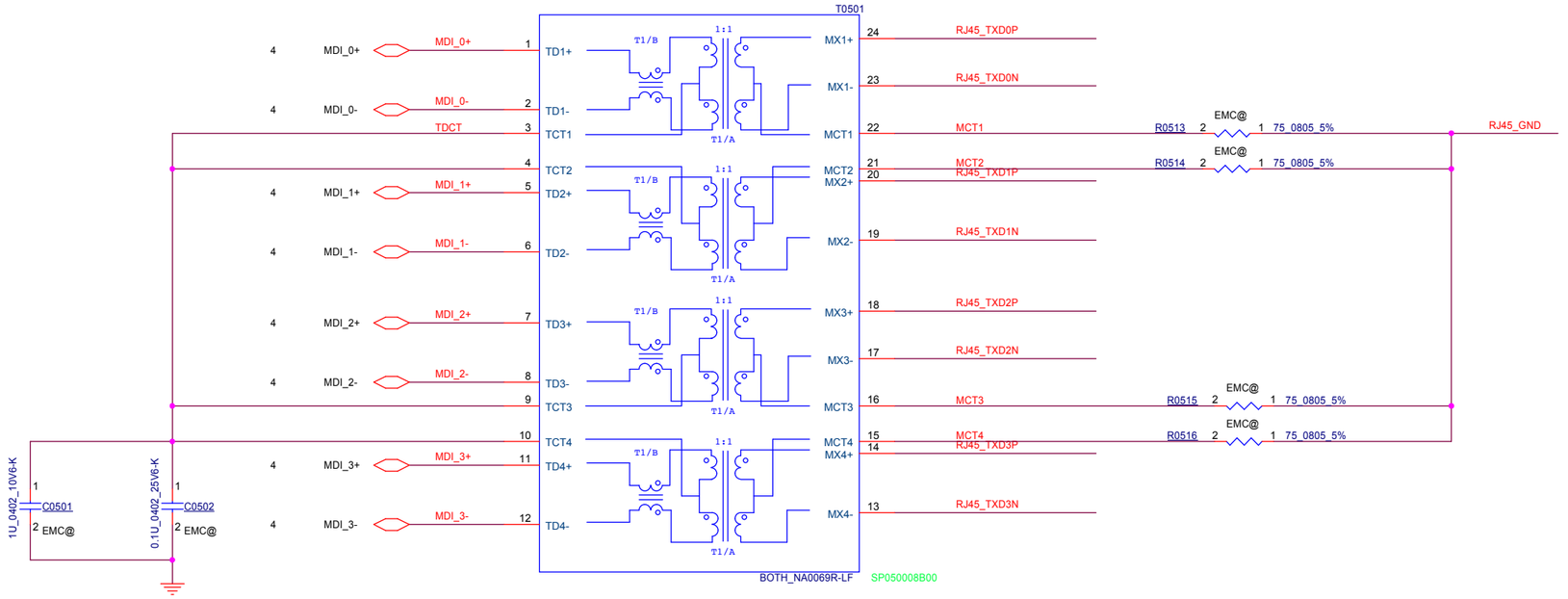


C0501, C0502 close to LAN Chip

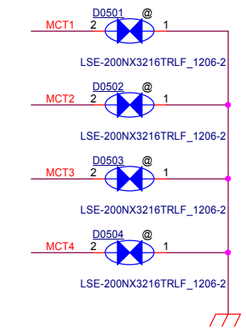
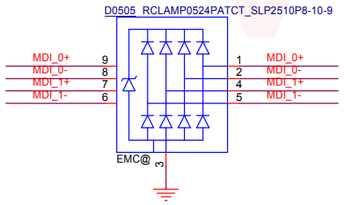
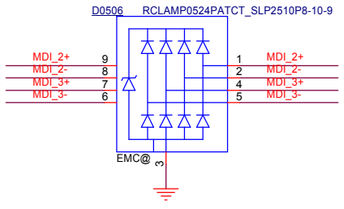
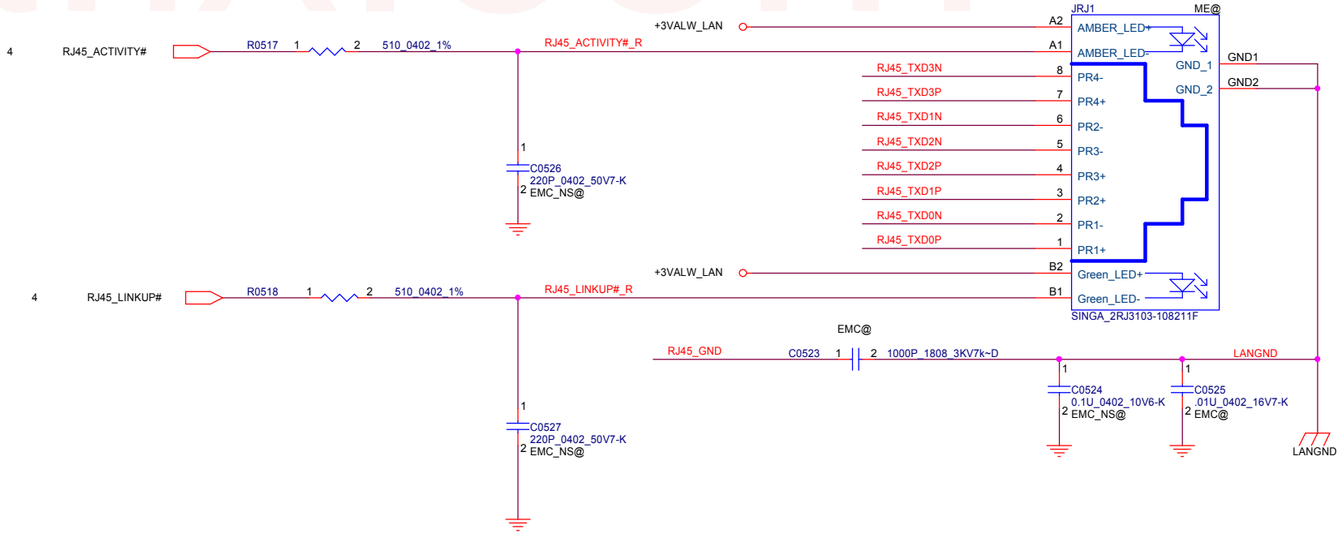


Table of X-FORM (U0501)		
Vendor	LCFC PN	Description
BOTHHAND	SP050008B00	S X'FORM_ NA0069R LF LAN







RJ-45 Conn.

Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/17	Deciphered Date	2017/12/31

Title: **RJ45 CONN**

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Custom	E480_NS-B421	1.0
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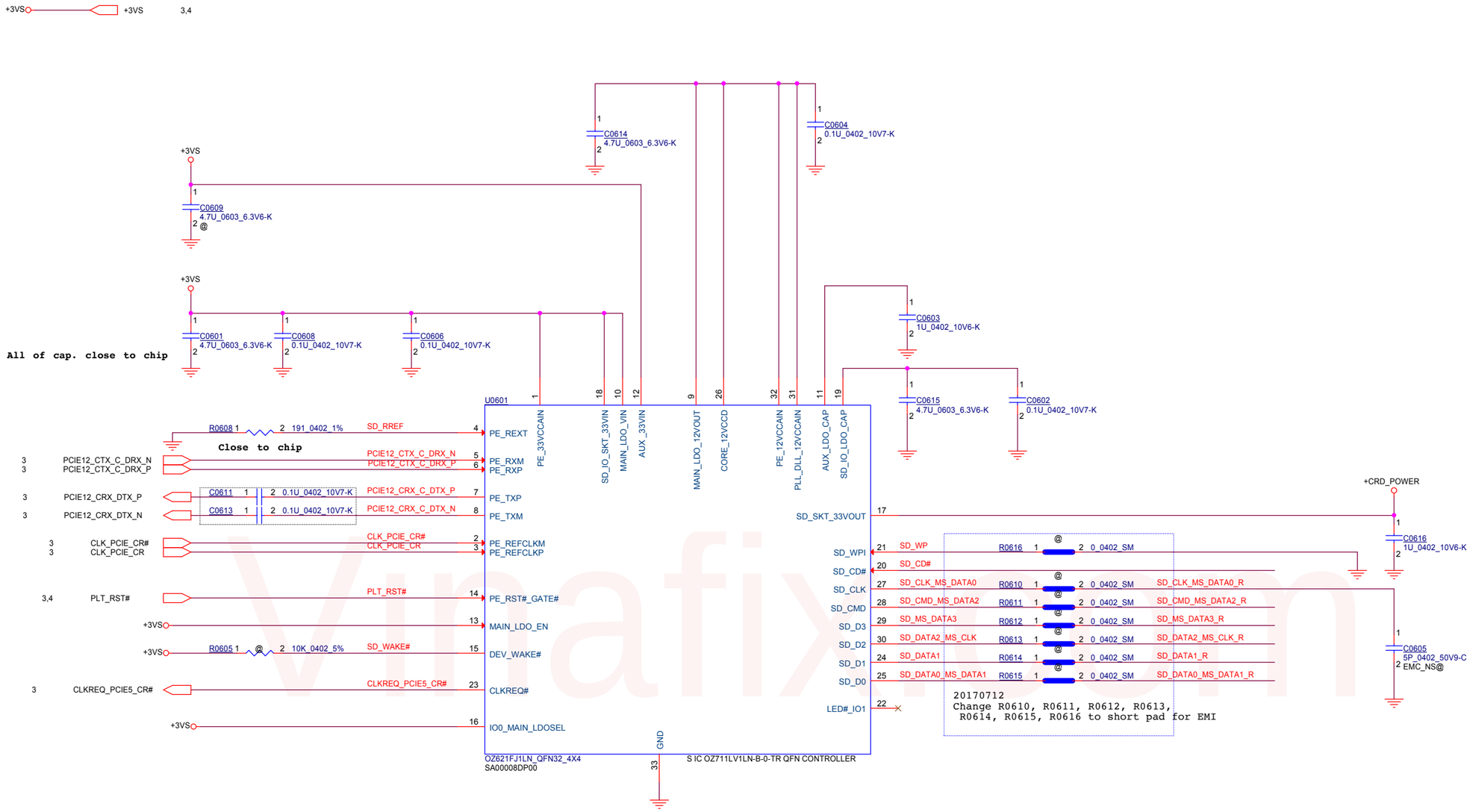

Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/17	Deciphered Date	2017/12/31

Title: **Card Reader**

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+5VALW — +5VALW 3
+3VALW — +3VALW 3,4
+3VS — +3VS 3,4,6
+3VL — +3VL 3

H1
PAD_C3P6D2P6

H2
PAD_C6P0D2P3

H3
PAD_C8P0D2P3

H4
PAD_C3P0D2P3

H5
PAD_C6P0D3P3

H6
PAD_C6P0D2P8

NH1
PAD_O2P7X3P3D2P7X3P3N

H7
PAD_C6P0D3P5

H8
PAD_C5P0D2P3

Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/17	Deciphered Date	2017/12/31

Title: *Screw Hole*

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