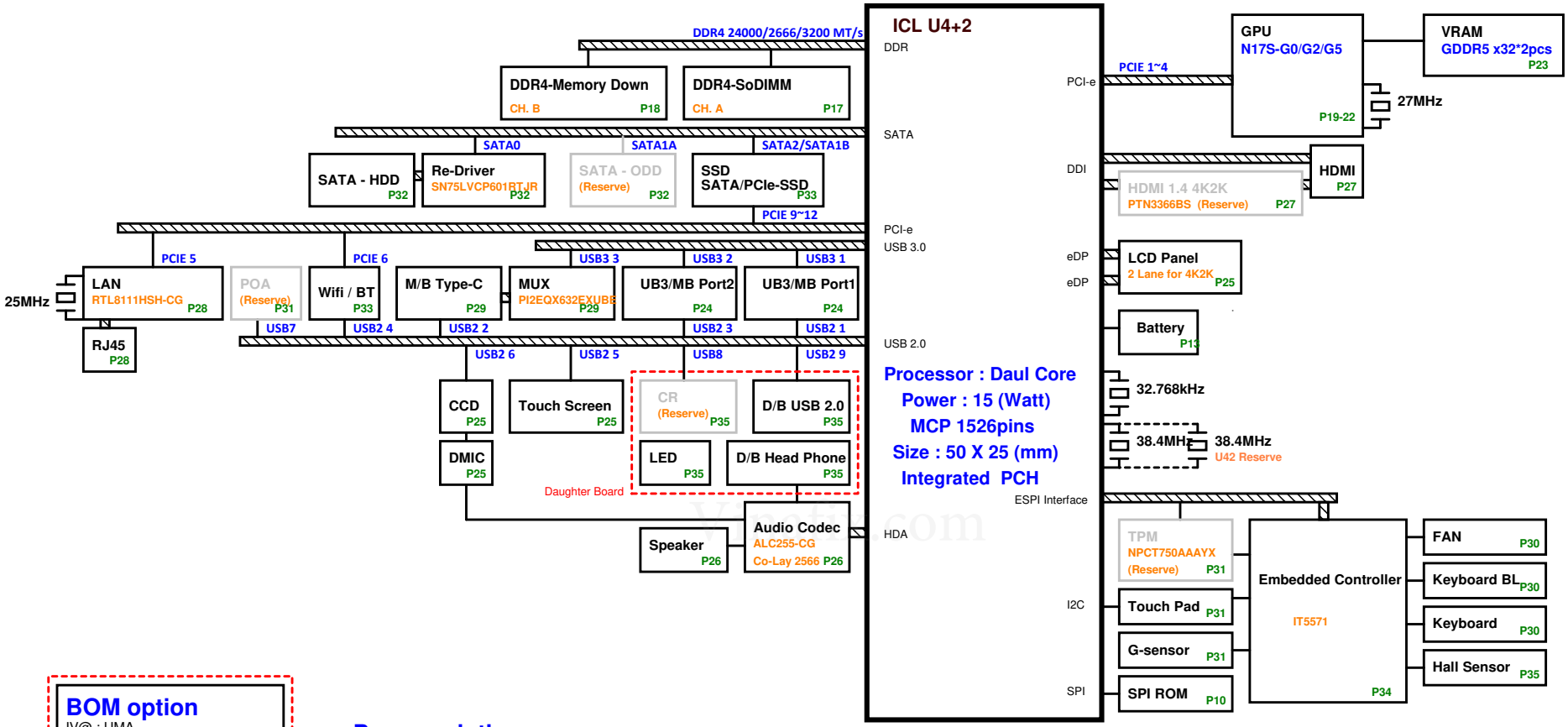
ZAUI ICE lake series Platform Block Diagram (DIS/UMA)

01



BOM option

IV@ : UMA
EV@ : DIS
TPC@ : Type-C function
TPC_N@ :No Type-C function
TSI@ : Touch screen I2C
TPM@ : Trusted Platform Module
PBA@ : Finger Print on touch pad
KBL@ : Keyboard back light
GS@ : G-Sensor function
GS_N@ : No G-Sensor function
SSD@ : Solid State Disk
ODD@ : Optical Disc Drive
EMC@ : eMMC function
RAM@ : On Board Memory
SP@ : Power & VGA
HDD_R@ : Hard Disc Redriver
HDD_N@ : NO Hard Disc Redriver
CNV@ : Intel WIFI
CNV_N@ :NO Intel WIFI
HDMI_R@ : HDMI Redirver
HDMI_N@ : No HDMI Redirver
Debug@ : for Debug Card
255@ : Codec 255
256@ : Codec 256
FOR15_17@ : Panel 15 or 17 inch
FOR14@ : Panel 14 inch

Power solution

Batery Charger BQ24780SRUYR P37	+VCCIN_AUX RT9610CGQW P42	+VGPU_CORE RT8813DGQW P46
+3VPCU/+5VPCU RT6258CGQUF P38	+VCCIN_and RT9610CGQW P43	+1.35V_GFX G5335QT2U P47
+3V/+5V JW7110DFNC P38	+VCCSA RT9610CGQW P43	+1V8_AON JW7110DFNC P48
+1V_S5 G5335QT2U P39	+1.8V_S5 JW5213DFND P44	+1.03_GFX G9336ADJTP1U P48
+1.2VSUS RT8231BGQW G9661MF11U P40	+1.5V JW5222RSOTB P44	Thermal protection TMP708AIDBVR P44

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	Block Diagram	3A

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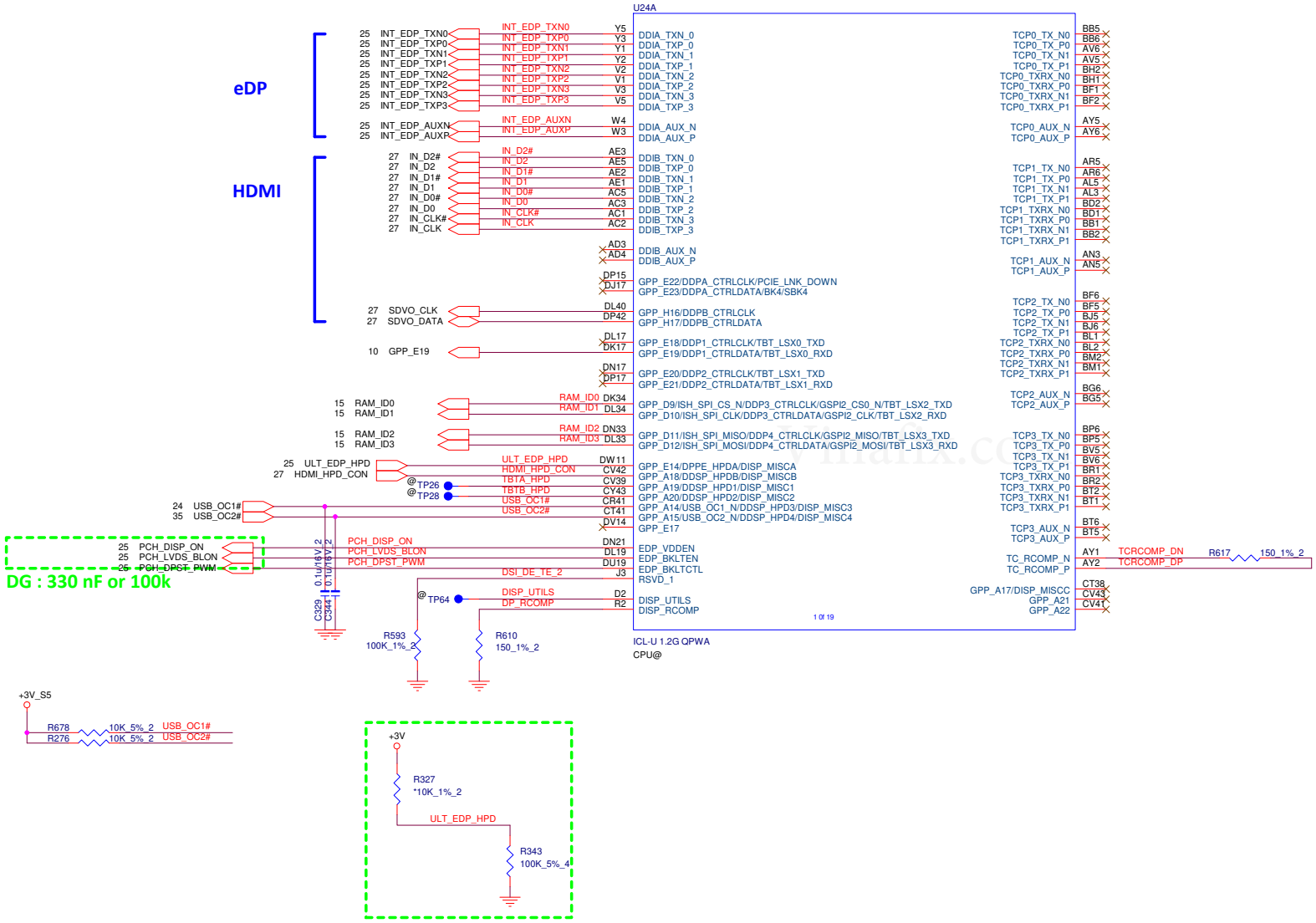

+3V_S5 6,8,10,11,13,14,15,16,28,29,30,33,34,37,40,41

Quanta Computer Inc.		
PROJECT : ZAUI		
Size	Document Number: ICL-U 1/14 (DDI/TBT/eDP)	Rev: 3A
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ICELAKE Processor DDR4

03

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
3,18 M_B_DQSN[7:0]
3,18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
3,18 M_B_DQ[63:0]

DDR CHANNEL A/B

U24B

LPDDR4 DDR4 NIL

M_A_DQ0	CA48	DDRA_DQ0_0/DDR0_DQ0_0	BL48		M_A_CLKN0	17
M_A_DQ1	CA47	DDRA_DQ0_1/DDR0_DQ0_1	BL47		M_A_CLKP0	17
M_A_DQ2	CA49	DDRA_DQ0_2/DDR0_DQ0_2	BF42		M_A_CLKN1	17
M_A_DQ3	BV49	DDRB_CLK_N/DDR0_CLK_N_1	BF43		M_A_CLKP1	17
M_A_DQ4	CA45	DDRB_CLK_P/DDR0_CLK_P_1				
M_A_DQ5	BV47	DDRA_DQ0_4/DDR0_DQ0_4	BG49			
M_A_DQ6	BV45	DDRA_DQ0_5/DDR0_DQ0_5	DDRA_CKE0/DDR0_CKE0	BJ47	M_A_CKE0	17
M_A_DQ7	BV48	DDRA_DQ0_6/DDR0_DQ0_6	DDRA_CKE1/NC	BF38		
M_A_DQ8	CC42	DDRA_DQ0_7/DDR0_DQ0_7	DDRB_CKE0/NC	BF41		
M_A_DQ9	CC39	DDRA_DQ1_0/DDR0_DQ1_0	DDRB_CKE1/DDR0_CKE1		M_A_CKE1	17
M_A_DQ10	CC43	DDRA_DQ1_1/DDR0_DQ1_1	BM38			
M_A_DQ11	CE38	DDRA_DQ1_2/DDR0_DQ1_2	DDRA_CS_0/DDR0_CS_N_0	BM42	M_A_CS#0	17
M_A_DQ12	CC38	DDRA_DQ1_3/DDR0_DQ1_3	DDRA_CS_1/NC	BP42		
M_A_DQ13	CE39	DDRA_DQ1_4/DDR0_DQ1_4	DDRB_CS_0/NC			
M_A_DQ14	CE42	DDRA_DQ1_5/DDR0_DQ1_5	DDRB_CS_1/DDR0_CS_N_1	BG42	M_A_CS#1	17
M_A_DQ15	CE43	DDRA_DQ1_6/DDR0_DQ1_6				
M_A_DQ16	BT48	DDRA_DQ1_7/DDR0_DQ1_7	DDRB_CA4/DDR0_BA0	BM43	M_A_BS#0	17
M_A_DQ17	BT47	DDRA_DQ2_0/DDR0_DQ2_0	NC/DDR0_BA1	BG39	M_A_BS#1	17
M_A_DQ18	BT49	DDRA_DQ2_1/DDR0_DQ2_1				
M_A_DQ19	BN49	DDRA_DQ2_2/DDR0_DQ2_2	DDRA_CA5/DDR0_BG0	BB49	M_A_BG#0	17
M_A_DQ20	BT45	DDRA_DQ2_3/DDR0_DQ2_3	NC/DDR0_BG1	BD47	M_A_BG#1	17
M_A_DQ21	BN47	DDRA_DQ2_4/DDR0_DQ2_4				
M_A_DQ22	BN45	DDRA_DQ2_5/DDR0_DQ2_5	NC/DDR0_MA0	BB48 M_A_A0	M_A_A0	17
M_A_DQ23	BN48	DDRA_DQ2_6/DDR0_DQ2_6	NC/DDR0_MA1	BL49 M_A_A1	M_A_A1	17
M_A_DQ24	BV42	DDRA_DQ2_7/DDR0_DQ2_7	DDRB_CA5/DDR0_MA2	BG38 M_A_A2	M_A_A2	17
M_A_DQ25	BV39	DDRB_DQ3_0/DDR0_DQ3_0	NC/DDR0_MA3	BL45 M_A_A3	M_A_A3	17
M_A_DQ26	BV43	DDRB_DQ3_1/DDR0_DQ3_1	NC/DDR0_MA4	BJ46 M_A_A4	M_A_A4	17
M_A_DQ27	BW38	DDRB_DQ3_2/DDR0_DQ3_2	DDRA_CA0/DDR0_MA5	BG48 M_A_A5	M_A_A5	17
M_A_DQ28	BV38	DDRB_DQ3_3/DDR0_DQ3_3	DDRA_CA2/DDR0_MA6	BE45 M_A_A6	M_A_A6	17
M_A_DQ29	BW39	DDRB_DQ3_4/DDR0_DQ3_4	DDRA_CA4/DDR0_MA7	BG45 M_A_A7	M_A_A7	17
M_A_DQ30	BW42	DDRB_DQ3_5/DDR0_DQ3_5	DDRA_CA3/DDR0_MA8	BG47 M_A_A8	M_A_A8	17
M_A_DQ31	BW43	DDRB_DQ3_6/DDR0_DQ3_6	DDRA_CA1/DDR0_MA9	BE47 M_A_A9	M_A_A9	17
M_A_DQ32	AY48	DDRB_DQ3_7/DDR0_DQ3_7	NC/DDR0_MA10	BJ38 M_A_A10	M_A_A10	17
M_A_DQ33	AY47	DDRB_DQ0_0/DDR0_DQ4_0	NC/DDR0_MA11	BB47 M_A_A11	M_A_A11	17
M_A_DQ34	AY49	DDRB_DQ0_1/DDR0_DQ4_1	NC/DDR0_MA12	BE48 M_A_A12	M_A_A12	17
M_A_DQ35	AU45	DDRB_DQ0_2/DDR0_DQ4_2	DDRB_CA0/DDR0_MA13	BM39 M_A_A13	M_A_A13	17
M_A_DQ36	AY45	DDRB_DQ0_3/DDR0_DQ4_3	DDRB_CA2/DDR0_MA14WE_N	BG43	M_A_WE#	17
M_A_DQ37	AU47	DDRB_DQ0_4/DDR0_DQ4_4	DDRB_CA1/DDR0_MA15CAS_N	BJ42	M_A_CAS#	17
M_A_DQ38	AU48	DDRB_DQ0_5/DDR0_DQ4_5	DDRB_CA3/DDR0_MA16RAS_N	BM41	M_A_RAS#	17
M_A_DQ39	AU49	DDRB_DQ0_6/DDR0_DQ4_6				
M_A_DQ40	AY42	DDRB_DQ0_7/DDR0_DQ4_7	NC/DDR0_ODT_0	BJ39	M_A_DIM0_ODT0	17
M_A_DQ41	AY38	DDRB_DQ1_0/DDR0_DQ5_0	NC/DDR0_ODT_1	BB45	M_A_DIM0_ODT1	17
M_A_DQ42	AY43	DDRB_DQ1_1/DDR0_DQ5_1				
M_A_DQ43	BB39	DDRB_DQ1_2/DDR0_DQ5_2	DDRA_DQSN_0/DDR0_DQSN_0	BY47 M_A_DQSN0		
M_A_DQ44	AY39	DDRB_DQ1_3/DDR0_DQ5_3	DDRA_DQSP_0/DDR0_DQSP_0	BY46 M_A_DQSP0		
M_A_DQ45	BB38	DDRB_DQ1_4/DDR0_DQ5_4	DDRA_DQSN_1/DDR0_DQSN_1	CC41 M_A_DQSN1		
M_A_DQ46	BB42	DDRB_DQ1_5/DDR0_DQ5_5	DDRA_DQSP_1/DDR0_DQSP_1	CE41 M_A_DQSP1		
M_A_DQ47	BB43	DDRB_DQ1_6/DDR0_DQ5_6	DDRA_DQSN_2/DDR0_DQSN_2	BR47 M_A_DQSN2		
M_A_DQ48	AR48	DDRB_DQ1_7/DDR0_DQ5_7	DDRA_DQSP_2/DDR0_DQSP_2	BR46 M_A_DQSP2		
M_A_DQ49	AR47	DDRB_DQ2_0/DDR0_DQ6_0	DDRA_DQSN_3/DDR0_DQSN_3	BV41 M_A_DQSN3		
M_A_DQ50	AR49	DDRB_DQ2_1/DDR0_DQ6_1	DDRA_DQSP_3/DDR0_DQSP_3	BW41 M_A_DQSP3		
M_A_DQ51	AM45	DDRB_DQ2_2/DDR0_DQ6_2	DDRB_DQSN_0/DDR0_DQSN_4	AV46 M_A_DQSN4		
M_A_DQ52	AR45	DDRB_DQ2_3/DDR0_DQ6_3	DDRB_DQSP_0/DDR0_DQSP_4	AV47 M_A_DQSP4		
M_A_DQ53	AM47	DDRB_DQ2_4/DDR0_DQ6_4	DDRB_DQSN_1/DDR0_DQSN_5	AY41 M_A_DQSN5		
M_A_DQ54	AM48	DDRB_DQ2_5/DDR0_DQ6_5	DDRB_DQSP_1/DDR0_DQSP_5	BB41 M_A_DQSP5		
M_A_DQ55	AM49	DDRB_DQ2_6/DDR0_DQ6_6	DDRB_DQSN_2/DDR0_DQSN_6	AN46 M_A_DQSN6		
M_A_DQ56	AT42	DDRB_DQ2_7/DDR0_DQ6_7	DDRB_DQSP_2/DDR0_DQSP_6	AN47 M_A_DQSP6		
M_A_DQ57	AT39	DDRB_DQ3_0/DDR0_DQ7_0	DDRB_DQSN_3/DDR0_DQSN_7	AR41 M_A_DQSN7		
M_A_DQ58	AR43	DDRB_DQ3_1/DDR0_DQ7_1	DDRB_DQSP_3/DDR0_DQSP_7	AT41 M_A_DQSP7		
M_A_DQ59	AT38	DDRB_DQ3_2/DDR0_DQ7_2				
M_A_DQ60	AR38	DDRB_DQ3_3/DDR0_DQ7_3	NC/DDR0_PAR	BF39 M_A_PARITY	M_A_PARITY	17
M_A_DQ61	AR39	DDRB_DQ3_4/DDR0_DQ7_4	NC/DDR0_ACT_N	BE49	M_A_ACT#	17
M_A_DQ62	AR42	DDRB_DQ3_5/DDR0_DQ7_5	NC/DDR0_ALERT_N	BD46 M_A_ALERT#	M_A_ALERT#	17
M_A_DQ63	AT43	DDRB_DQ3_6/DDR0_DQ7_6				
		DDRB_DQ3_7/DDR0_DQ7_7	RSVD_73	M38		
			DDR0_VREF_CA	C44 SM_VREF	SM_VREF	17
			DDR1_VREF_CA	B45 SMDDR_VREF_DQ1_M3	SMDDR_VREF_DQ1_M3	18
			DDR_VTT_CTL	M39 DDR_VTT_CTRL	TP59	
			DRAM_RESET_N	DK47 DDR_DRAMRST#_R		

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R576 100_1%_2 DDR_RCOMP0 D47
R575 100_1%_2 DDR_RCOMP1 E46
R577 100_1%_2 DDR_RCOMP2 C47

DDR_RCOMP_0
DDR_RCOMP_1
DDR_RCOMP_2

ICL-U 1.2G QPWA
CPU@

For CH:A

DDR CHANNEL C/D

U24C

LPDDR4 DDR4 NIL

M_B_DQ0	AK48	DDRC_DQ0_0/DDR1_DQ0_0	Y48		M_B_CLKN0	18
M_B_DQ1	AK45	DDRC_DQ0_1/DDR1_DQ0_1	Y47		M_B_CLKP0	18
M_B_DQ2	AK49	DDRC_DQ0_2/DDR1_DQ0_2	DDRC_CLK_N/DDR1_CLK_N_0	M43		
M_B_DQ3	AG47	DDRC_DQ0_3/DDR1_DQ0_3	DDRC_CLK_P/DDR1_CLK_P_0	M42		
M_B_DQ4	AK47	DDRC_DQ0_4/DDR1_DQ0_4	DDRD_CLK_N/DDR1_CLK_N_1			
M_B_DQ5	AG45	DDRC_DQ0_5/DDR1_DQ0_5	DDRD_CLK_P/DDR1_CLK_P_1	U45		
M_B_DQ6	AG48	DDRC_DQ0_6/DDR1_DQ0_6	DDRC_CKE0/DDR1_CKE0	V46	M_B_CKE0	18
M_B_DQ7	AG49	DDRC_DQ0_7/DDR1_DQ0_7	DDRC_CKE1/NC	M41		
M_B_DQ8	AJ38	DDRC_DQ1_0/DDR1_DQ1_0	DDRD_CKE0/NC	P43		
M_B_DQ9	AL39	DDRC_DQ1_1/DDR1_DQ1_1	DDRD_CKE1/DDR1_CKE1			
M_B_DQ10	AJ39	DDRC_DQ1_2/DDR1_DQ1_2	DDRC_CS_0/DDR1_CS_N_0	V42		
M_B_DQ11	AL43	DDRC_DQ1_3/DDR1_DQ1_3	DDRC_CS_1/NC	V39	M_B_CS#0	18
M_B_DQ12	AL38	DDRC_DQ1_4/DDR1_DQ1_4	DDRD_CS_0/NC	Y39		
M_B_DQ13	AJ42	DDRC_DQ1_5/DDR1_DQ1_5	DDRD_CS_1/DDR1_CS_N_1	T39		
M_B_DQ14	AL42	DDRC_DQ1_6/DDR1_DQ1_6				
M_B_DQ15	AJ43	DDRC_DQ1_7/DDR1_DQ1_7	DDRD_CA4/DDR1_BA0	T38		
M_B_DQ16	AB49	DDRC_DQ2_0/DDR1_DQ2_0	NC/DDR1_BA1	T42	M_B_BS#0	18
M_B_DQ17	AB48	DDRC_DQ2_1/DDR1_DQ2_1			M_B_BS#1	18
M_B_DQ18	AE49	DDRC_DQ2_2/DDR1_DQ2_2	DDRC_CA5/DDR1_BG0	R45		
M_B_DQ19	AE47	DDRC_DQ2_3/DDR1_DQ2_3	NC/DDR1_BG1	N47	M_B_BG#0	18
M_B_DQ20	AE48	DDRC_DQ2_4/DDR1_DQ2_4			M_B_BG#1	18
M_B_DQ21	AB47	DDRC_DQ2_5/DDR1_DQ2_5	NC/DDR1_MA0	P42 M_B_A0		
M_B_DQ22	AB45	DDRC_DQ2_6/DDR1_DQ2_6	NC/DDR1_MA1	Y49 M_B_A1	M_B_A0	18
M_B_DQ23	AE45	DDRC_DQ2_7/DDR1_DQ2_7	DDRD_CA5/DDR1_MA2	U48 M_B_A2	M_B_A1	18
M_B_DQ24	AD38	DDRC_DQ3_0/DDR1_DQ3_0	NC/DDR1_MA3	Y45 M_B_A3	M_B_A2	18
M_B_DQ25	AD39	DDRC_DQ3_1/DDR1_DQ3_1	NC/DDR1_MA4	U47 M_B_A4	M_B_A3	18
M_B_DQ26	AE39	DDRC_DQ3_2/DDR1_DQ3_2	DDRC_CA0/DDR1_MA5	R49 M_B_A5	M_B_A4	18
M_B_DQ27	AE43	DDRC_DQ3_3/DDR1_DQ3_3	DDRC_CA2/DDR1_MA6	U49 M_B_A6	M_B_A5	18
M_B_DQ28	AE38	DDRC_DQ3_4/DDR1_DQ3_4	DDRC_CA4/DDR1_MA7	M47 M_B_A7	M_B_A6	18
M_B_DQ29	AD43	DDRC_DQ3_5/DDR1_DQ3_5	DDRC_CA3/DDR1_MA8	M45 M_B_A8	M_B_A7	18
M_B_DQ30	AD42	DDRC_DQ3_6/DDR1_DQ3_6	DDRC_CA1/DDR1_MA9	R47 M_B_A9	M_B_A8	18
M_B_DQ31	AE42	DDRC_DQ3_7/DDR1_DQ3_7	NC/DDR1_MA10	P39 M_B_A10	M_B_A9	18
M_B_DQ32	J48	DDRD_DQ0_0/DDR1_DQ4_0	NC/DDR1_MA11	N46 M_B_A11	M_B_A10	18
M_B_DQ33	J45	DDRD_DQ0_1/DDR1_DQ4_1	NC/DDR1_MA12	R48 M_B_A12	M_B_A11	18
M_B_DQ34	J49	DDRD_DQ0_2/DDR1_DQ4_2	DDRD_CA0/DDR1_MA13	Y41 M_B_A13	M_B_A12	18
M_B_DQ35	G47	DDRD_DQ0_3/DDR1_DQ4_3	DDRD_CA2/DDR1_MA14WE_N	V41	M_B_A13	18
M_B_DQ36	J47	DDRD_DQ0_4/DDR1_DQ4_4	DDRD_CA1/DDR1_MA15CAS_N	Y42	M_B_WE#	18
M_B_DQ37	G45	DDRD_DQ0_5/DDR1_DQ4_5	DDRD_CA3/DDR1_MA16RAS_N	V47	M_B_CAS#	18
M_B_DQ38	G48	DDRD_DQ0_6/DDR1_DQ4_6			M_B_RAS#	18
M_B_DQ39	E48	DDRD_DQ0_7/DDR1_DQ4_7	NC/DDR1_ODT_0	V43		
M_B_DQ40	J38	DDRD_DQ1_0/DDR1_DQ5_0	NC/DDR1_ODT_1	V38	M_B_DIM0_ODT0	18
M_B_DQ41	G39	DDRD_DQ1_1/DDR1_DQ5_1				
M_B_DQ42	G38	DDRD_DQ1_2/DDR1_DQ5_2	DDRC_DQSN_0/DDR1_DQSN_0	AH46 M_B_DQSN0		
M_B_DQ43	G42	DDRD_DQ1_3/DDR1_DQ5_3	DDRC_DQSP_0/DDR1_DQSP_0	AH47 M_B_DQSP0		
M_B_DQ44	J39	DDRD_DQ1_4/DDR1_DQ5_4	DDRC_DQSN_1/DDR1_DQSN_1	AJ41 M_B_DQSN1		
M_B_DQ45	J42	DDRD_DQ1_5/DDR1_DQ5_5	DDRC_DQSP_1/DDR1_DQSP_1	AL41 M_B_DQSP1		
M_B_DQ46	G43	DDRD_DQ1_6/DDR1_DQ5_6	DDRC_DQSN_2/DDR1_DQSN_2	AC47 M_B_DQSN2		
M_B_DQ47	J43	DDRD_DQ1_7/DDR1_DQ5_7	DDRC_DQSP_2/DDR1_DQSP_2	AC46 M_B_DQSP2		
M_B_DQ48	B43	DDRD_DQ2_0/DDR1_DQ6_0	DDRC_DQSN_3/DDR1_DQSN_3	AE41 M_B_DQSN3		
M_B_DQ49	D43	DDRD_DQ2_1/DDR1_DQ6_1	DDRC_DQSP_3/DDR1_DQSP_3	AD41 M_B_DQSP3		
M_B_DQ50	A43	DDRD_DQ2_2/DDR1_DQ6_2	DDRD_DQSN_0/DDR1_DQSN_4	H47 M_B_DQSN4		
M_B_DQ51	C40	DDRD_DQ2_3/DDR1_DQ6_3	DDRD_DQSP_0/DDR1_DQSP_4	H46 M_B_DQSP4		
M_B_DQ52	C43	DDRD_DQ2_4/DDR1_DQ6_4	DDRD_DQSN_1/DDR1_DQSN_5	G41 M_B_DQSN5		
M_B_DQ53	D40	DDRD_DQ2_5/DDR1_DQ6_5	DDRD_DQSP_1/DDR1_DQSP_5	J41 M_B_DQSP5		
M_B_DQ54	B40	DDRD_DQ2_6/DDR1_DQ6_6	DDRD_DQSN_2/DDR1_DQSN_6	C42 M_B_DQSN6		
M_B_DQ55	A40	DDRD_DQ2_7/DDR1_DQ6_7	DDRD_DQSP_2/DDR1_DQSP_6	D42 M_B_DQSP6		
M_B_DQ56	B35	DDRD_DQ3_0/DDR1_DQ7_0	DDRD_DQSN_3/DDR1_DQSN_7	D36 M_B_DQSN7		
M_B_DQ57	D35	DDRD_DQ3_1/DDR1_DQ7_1	DDRD_DQSP_3/DDR1_DQSP_7	C36 M_B_DQSP7		
M_B_DQ58	A35	DDRD_DQ3_2/DDR1_DQ7_2				
M_B_DQ59	D38	DDRD_DQ3_3/DDR1_DQ7_3	NC/DDR1_PAR	P38 M_B_PARITY	M_B_PARITY	18
M_B_DQ60	C35	DDRD_DQ3_4/DDR1_DQ7_4	NC/DDR1_ACT_N	M48 M_B_ACT#	M_B_ACT#	18
M_B_DQ61	C38	DDRD_DQ3_5/DDR1_DQ7_5	NC/DDR1_ALERT_N	M49 M_B_ALERT#	M_B_ALERT#	18
M_B_DQ62	B38	DDRD_DQ3_6/DDR1_DQ7_6				
M_B_DQ63	A38	DDRD_DQ3_7/DDR1_DQ7_7				

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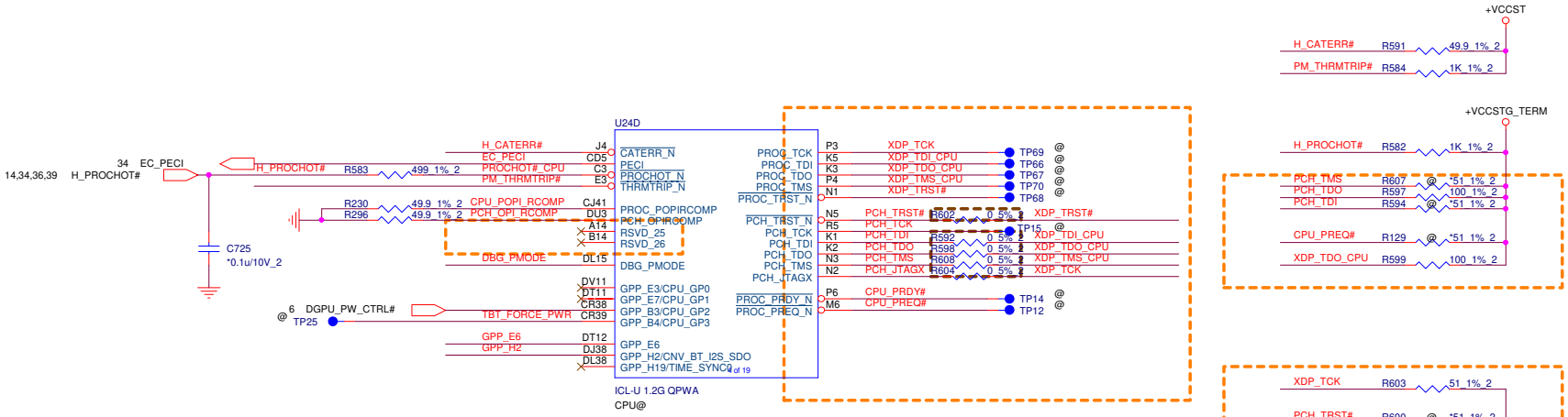
ICL-U 1.2G QPWA
CPU@

+1.2VSUS
R278 470_1%_2
DDR_DRAMRST#_R
R282 0_5%_2
DDR4_DRAMRST# 17,18
@ C353 *0.1u/10V_2

+3V_S5 2,6,8,10,11,13,14,15,16,28,29,30,33,34,37,40,41
+1.2VSUS 5,16,17,18,38,44

Quanta Computer Inc.
PROJECT : ZAUI

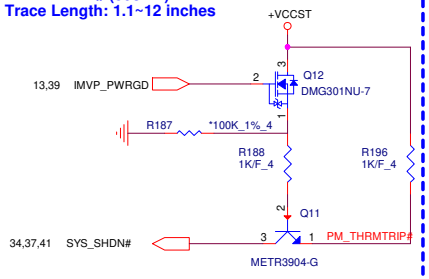
Size	Document Number	Rev
	ICL-U 2/14 (LPDDR4 I/F)	3A
Date: Monday, November 04, 2019	Sheet 3 of 47	



Strap pin

10 DBG_PMODE — DBG_PMODE
10 GPP_E6 — GPP_E6
10 GPP_H2 — GPP_H2

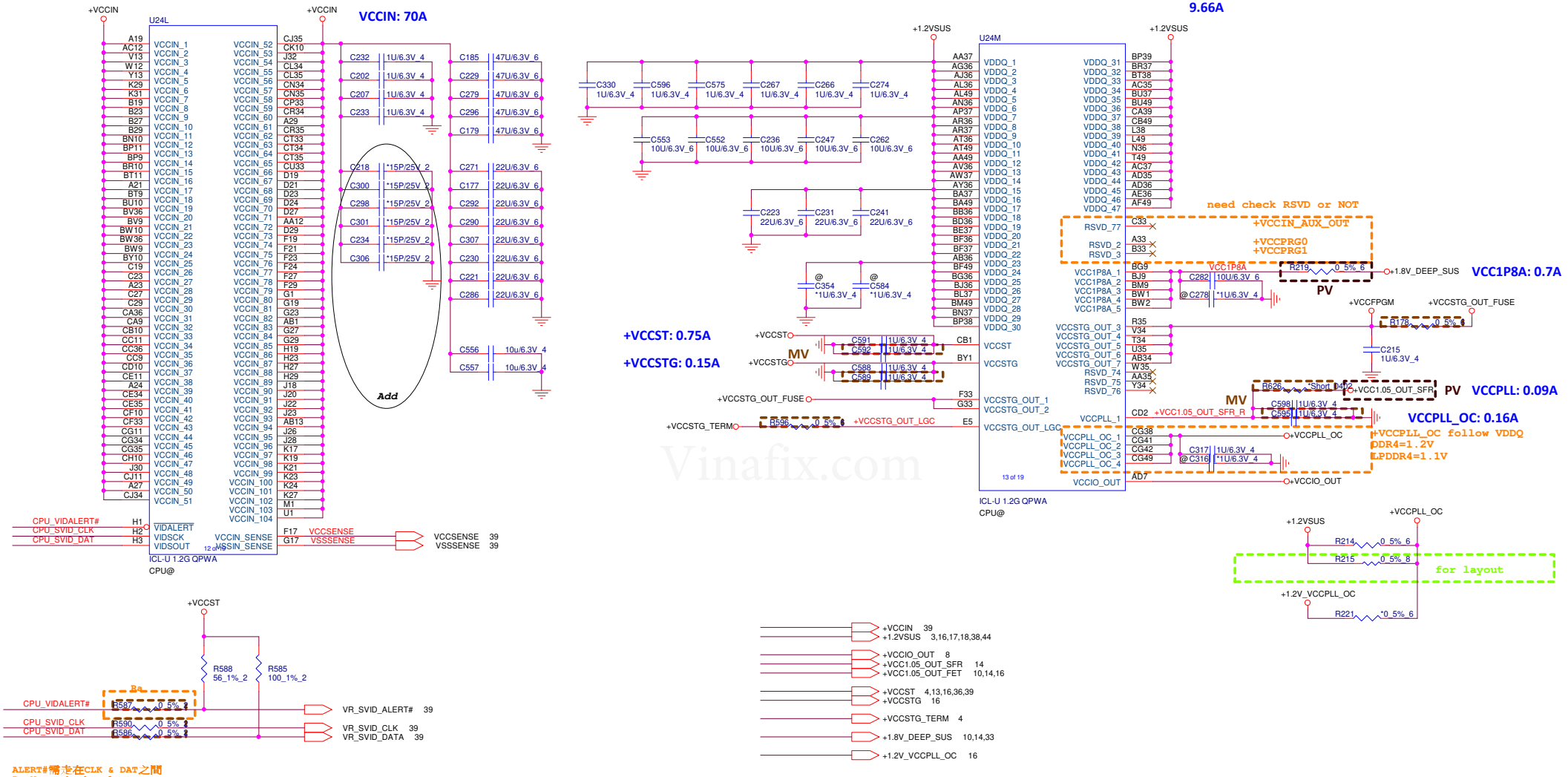
THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches



+VCCSTG_TERM 5
+VCCST 5,13,16,36,39
+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,41,42,43,44

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 3/14 (CPU MISC/JTA)	3A
Date: Monday, November 04, 2019	Sheet 4 of 47	



Quanta Computer Inc.	PROJECT : ZAUI
Size	Document Number: ICL-U 4/14 (VCCIN/VDDQ) — Rev 3A
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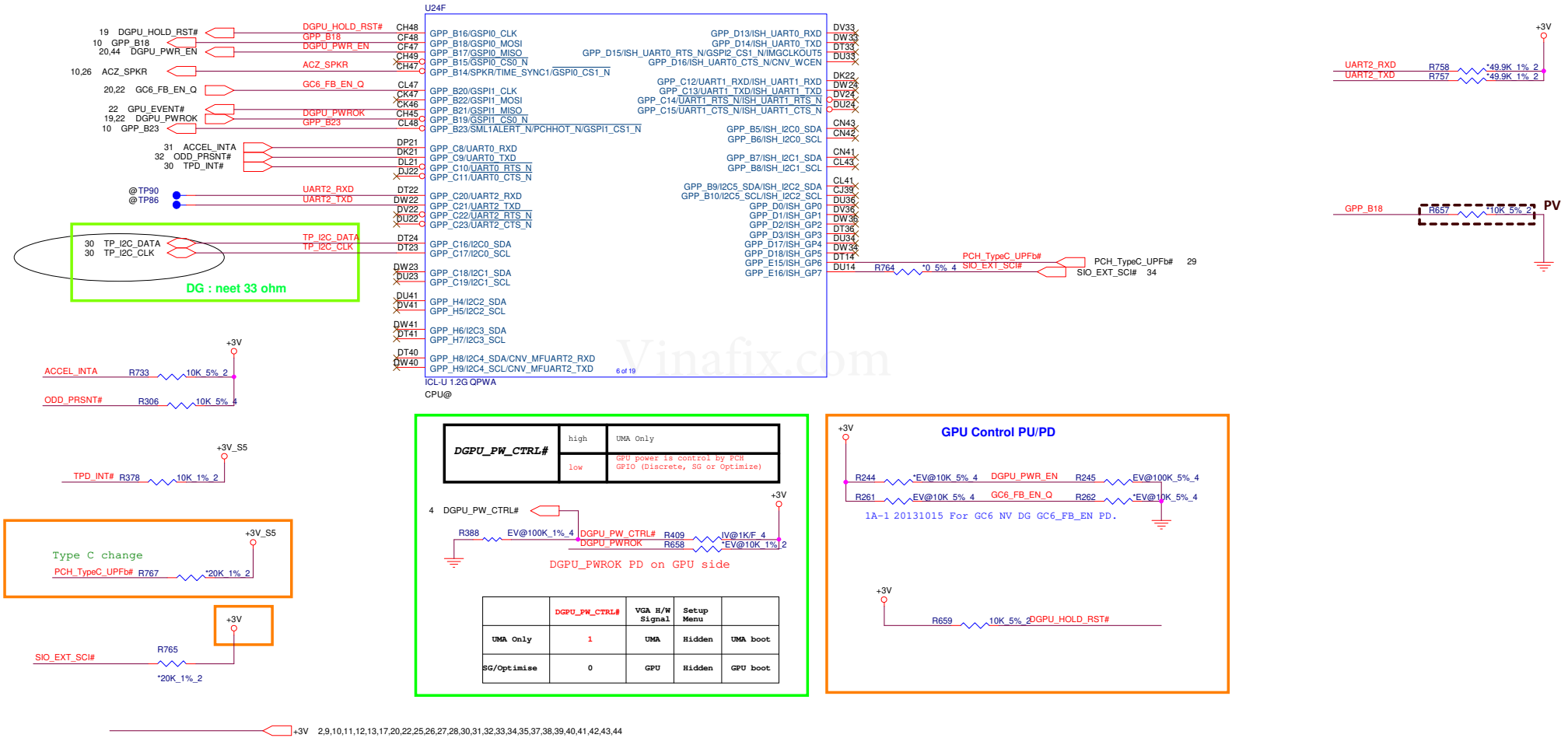
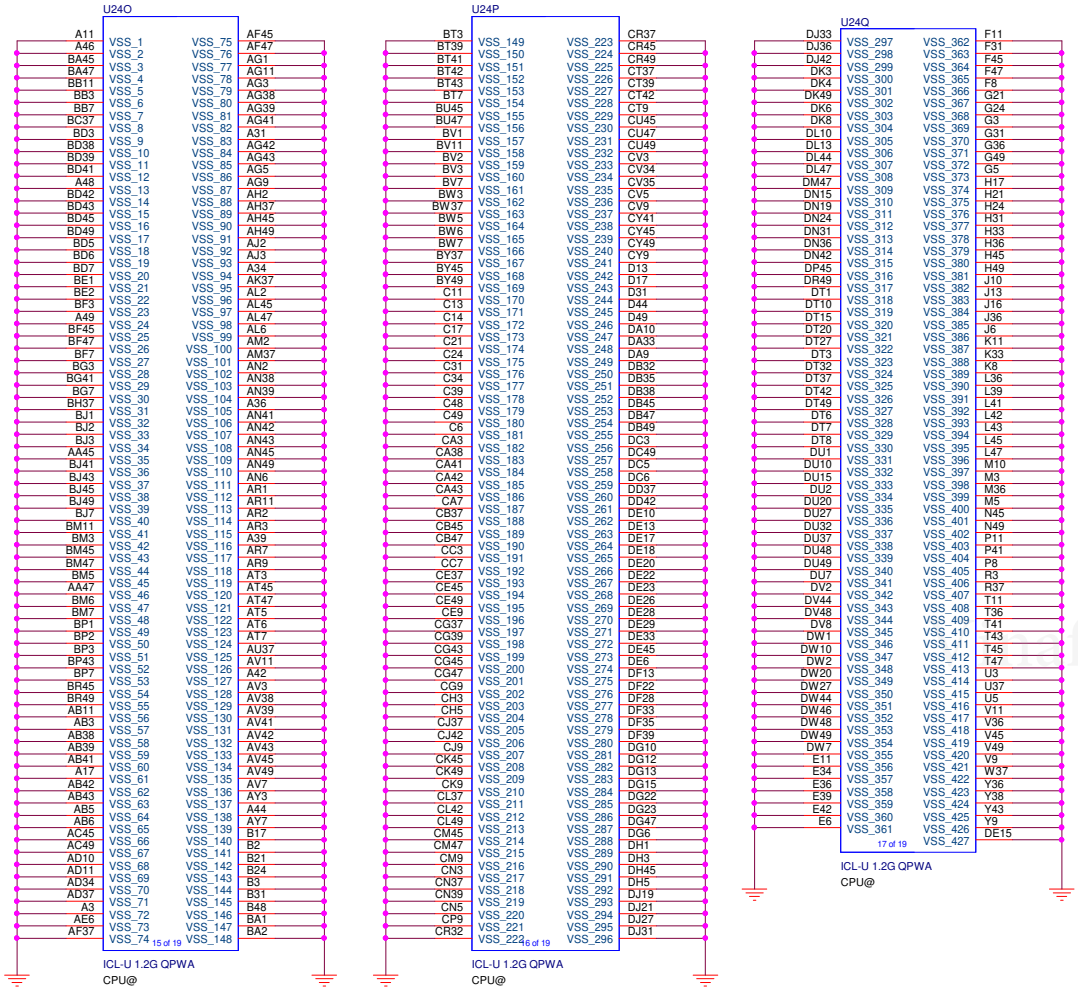
PD 75K WLAN side
need Check with BIOS



Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 5/14 (I2C/ISH)	3A

Date: Monday, November 04, 2019 Sheet 6 of 47

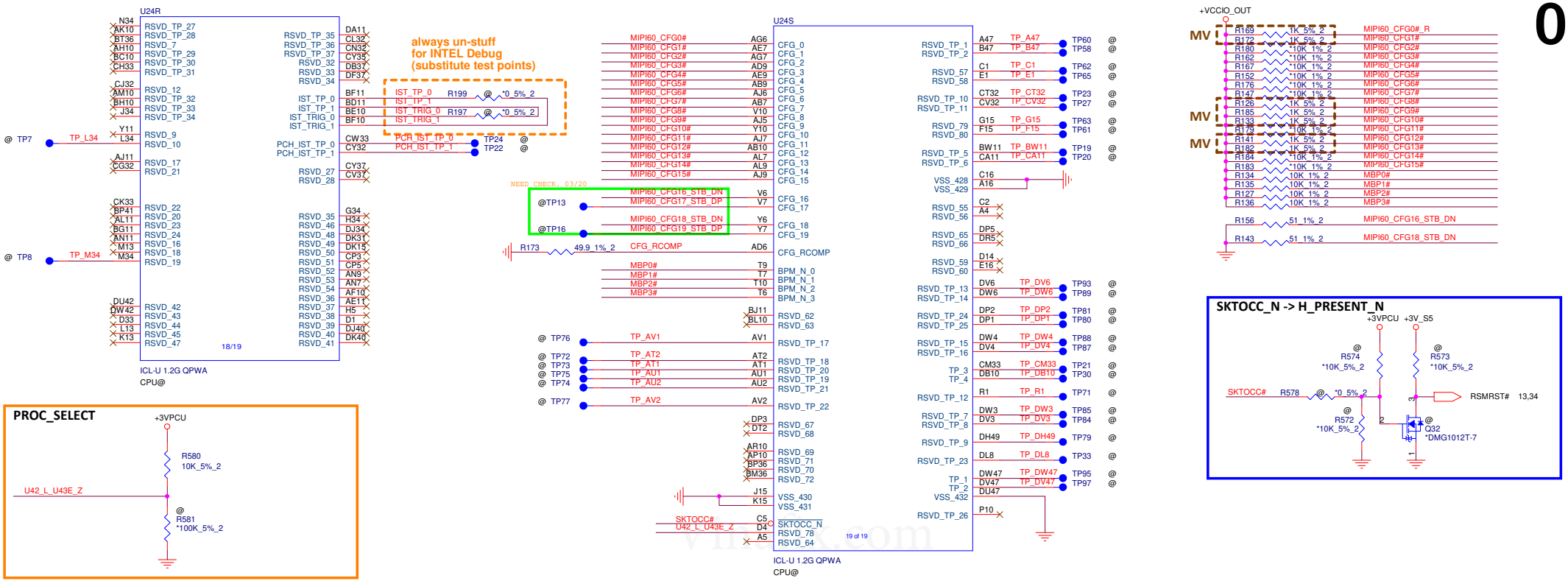


Quanta Computer Inc.

PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 6/14 (GND)	3A

Date: Monday, November 04, 2019 Sheet 7 of 47



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

CFG0

1: (DEFAULT) NORMAL OPERATION; NO STALL

MIPI60_CFG0# — R170 0_5%_2 — MIPI60_CFG0#_R — TP17

MV

R168 *1K_5%_2

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

CFG2

1: (DEFAULT)NORMAL OPERATION

0: LANE REVERSAL

MIPI60_CFG2# — R181 *1K_5%_2

PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

CFG4

1: DISABLED

AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT

0: ENABLED

NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

MIPI60_CFG4# — R166 1K_5%_2

PEG DEFER TRAINING

CFG7

1: (DEFAULT) PEG TRAIN IMMEEDIATELY FOLLOWING XXRESETB DEASSERTION

0: PEG WAIT FOR BIOS FOR TRAINING

MIPI60_CFG7# — R146 *1K_5%_2

NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG9

1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT

0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

MIPI60_CFG9# — R186 *1K_5%_2

PCH/ PCH LESS MODE SELECTION

CFG1

1: (DEFAULT) NORMAL OPERATION

0: PCH-LESS MODE

MIPI60_CFG1# — R171 *1K_5%_2

PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

CFG3

1: DISABLED

0: ENABLED

SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

MIPI60_CFG3# — R161 *1K_5%_2

PCIE PORT BIFURCATION STRAPS

CFG[6:5]

11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED

10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED

01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED

00 DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

MIPI60_CFG5# — R151 *1K_5%_2

MIPI60_CFG6# — R174 *1K_5%_2

ALLOW THE USE OF NOA ON LOCKED UNITS

CFG8

1: DISABLED(DEFAULT): IN THHIS CASE, NOA WILL BE DISABLE IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS

0: ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

MIPI60_CFG8# — R125 *1K_5%_2

SAFE MODE BOOT

CFG10

1: POWER FEATURES ACTIVATED DURING RESETT

0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

MIPI60_CFG10# — R132 *1K_5%_2

DMI AC COUPLING - JUST A PLACE HOLDER. NOT APPLICABLE FOR ULX-ULT

CFG11

1:(DEFAULT)DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED

0: DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

MIPI60_CFG11# — R177 *1K_5%_2

PM SYNC LEGACY

CFG12

1: (DEFAULT) PMSYNC 2.0

0: LEGACY

MIPI60_CFG12# — R140 *1K_5%_2

PMSYNC AYNC MODE- PM SYNC

CFG13

1: (DEFAULT)SYNCHCRONOUS (1 24 MHZ CYCLE PER BIT)

0: ASYNC - 4-24MHZ CYCLES PER BIT

MIPI60_CFG13# — R193 *1K_5%_2

MIPI60_CFG14# — R192 *1K_5%_2

MIPI60_CFG15# — R191 *1K_5%_2

+VCCIO_OUT 5

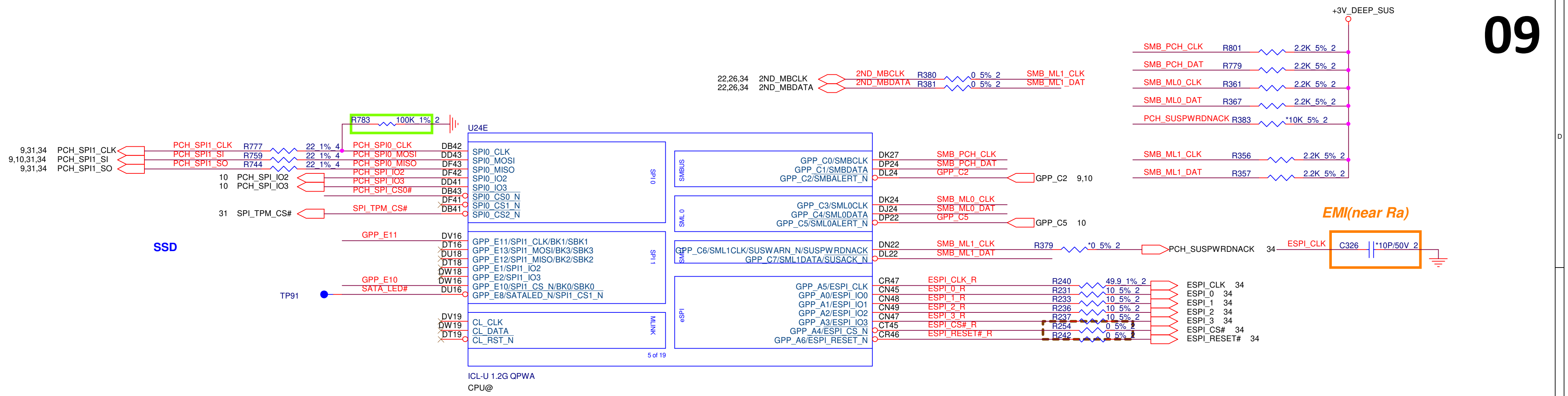
+3VPCU 12,16,25,26,28,30,31,34,35,36,37

+3V_S5 2,6,10,11,13,14,15,16,28,29,30,33,34,37,40,41

Quanta Computer Inc.

PROJECT : ZAUI

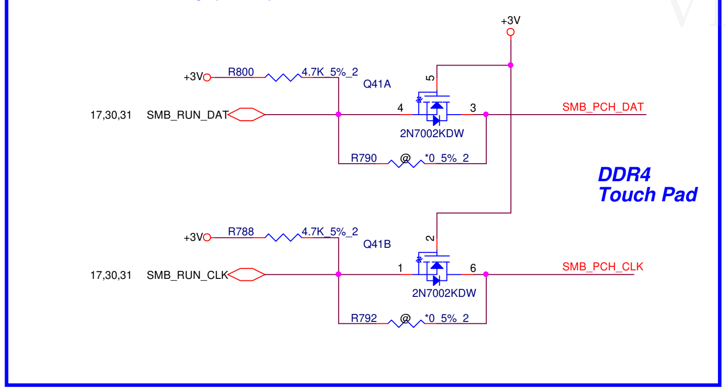
Size	Document Number	Rev
	ICL-U 7/14 (RSVD/XDP)	3A
Date: Monday, November 04, 2019	Sheet 8 of 47	



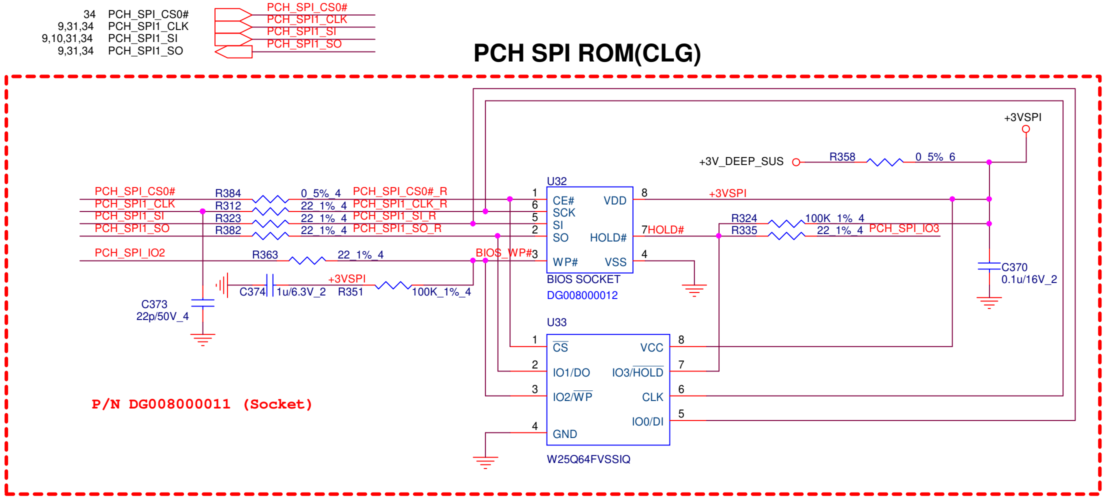
PCH SPI ROM(CLG)

Vender		Size	P/N	
Kabylake POA 3.3V	MXIC	16M	AKE3DZN0Z03	MX25L12873FM2I-10G
	Winbond	16M	AKE3DF-KN01	W25Q128JVSIQ
	GigaDevice	16M	AKE3DZN0Q02	GD25B127DSIGR

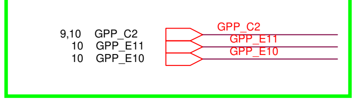
SMBus/Pull-up(CLG)



PCH SPI ROM(CLG)



strap pin



+3V 2,6,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,41,42,43,44

+3V_DEEP_SUS 10,14

Quanta Computer Inc.

PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 8/14 (SMBus/SPI)	3A

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TOP SWAP OVERRIDE

High: TOP SWAP ENABLED
Low: DISABLED
WEAK INTERNAL PD 20K

GPP_B14/SPKR

6,26 ACZ_SPKR — ACZ_SPKR — +3V — @R664 *4.7K_5%_2 — @R665 *20K_1%_2

(RSVD) XTAL INPUT MODE

High: XTAL INPUT IS SINGLE ENDED
Low: XTAL IS ATTACHED
WEAK INTERNAL PD 20K

13 GPD7 — GPD7 — +3V_S5 — @R413 *4.7K_5%_2 — @R405 *20K_1%_2

GPD7

NO REBOOT

High: NO REBOOT
Low: REBOOT ENABLED
WEAK INTERNAL PD 20K

GPP_B18/GSPI0_MOSI

6 GPP_B18 — GPP_B18 — +3V — @R655 *4.7K_5%_2 — @R656 *20K_1%_2

This strap has no internal pull-up or pull-down.
0 = DDP1 I2C / TBT_LSX0 pins at 1.8V
1 = DDP1 I2C / TBT_LSX0 pins at 3.3V

GPP_E19

2 GPP_E19 — +3V_DEEP_SUS — @R304 *4.7K_5%_2 — R301 20K_1%_2

TLS CONFIDENTIALITY

HIGH - TLS CONFIDENTIALITY ENABLE
LOW - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K

GPP_C2/SMBALERT#

9 GPP_C2 — GPP_C2 — +3V_DEEP_SUS — R346 4.7K_5%_2 — @R303 *20K_1%_2

(RSVD) A0 PERSONALITY STRAP

High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_IO3

9 PCH_SPI_IO3 — PCH_SPI_IO3 — +3V_DEEP_SUS — R721 100K_5%_2 — @R722 *4.7K_5%_2

ESPI OR EC LESS

HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED
WEAK INTERNAL PD 20K

GPP_C5/SML0ALERT#

9 GPP_C5 — GPP_C5 — +3V_DEEP_SUS — @R347 *4.7K_5%_2 — R334 20K_1%_2

(RSVD) JTAG ODT DISABLE

High: JTAG ODT Enable
Low: JTAG ODT Disable
External pull-up is required.

GPP_E6

4 GPP_E6 — GPP_E6 — +3V_DEEP_SUS — R760 100K_5%_2 — @R736 *4.7K_5%_2

MAF/SAF STRAP

High: SAF ENABLE
Low: MAF ENABLE
WEAK INTERNAL PD 20K

GPP_H2

4 GPP_H2 — GPP_H2 — +3V_DEEP_SUS — @R415 *2.2K_5%_2 — @R408 *20K_1%_2

(RSVD) BOOT HALT

High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_MOSI

9,31,34 PCH_SPI1_SI — PCH_SPI1_SI — MV R755 0_5%_2 — XDP_PCH_SPI0_SI — TP96 — +3V_DEEP_SUS — R771 100K_5%_2 — @R778 *4.7K_5%_2

(RSVD) ITP PMODE

High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K

ITP_PMODE

4 DBG_PMODE — TP34 — +VCC1.05_OUT_FET — R300 1K_5%_2 — @R290 *20K_1%_2

STRAP FOR SPI 1.8V/3.3V SELECTION

High: SPI voltage is 1.8V
Low: SPI voltage is 3.3V

INTRUDER#

13 INTRUDER# — INTRUDER# — +3V_RTC — R712 *1M_5%_2 — R713 10K_5%_2

CPUNSSC CLOCK FREQ

High: 19.2MHz CLOCK FROM INTERNAL DIVIDER
Low: 38.4MHz CLOCK FROM DIRECT CRYSTAL (Default)
WEAK INTERNAL PD 20K

GPP_B23/SML1ALERT#

6 GPP_B23 — GPP_B23 — +3V_DEEP_SUS — @R663 *4.7K_5%_2 — @R666 *20K_1%_2

(RSVD) CONSENT STRAP

High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_IO2

9 PCH_SPI_IO2 — PCH_SPI_IO2 — MV R723 0_5%_2 — XDP_PCH_SPI0_IO2 — TP92 — +3V_DEEP_SUS — R753 100K_5%_2 — @R743 *4.7K_5%_2

XTAL FREQUENCE SEL

High: 24MHZ
(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
Low: 38.4MHZ (DEFAULT)
WEAK INTERNAL PD 20K

GPP_F0

12,33 CNV_BRI_DT — CNV_BRI_DT — +1.8V_DEEP_SUS — @R353 *4.7K_5%_2 — @R337 *20K_1%_2

3V SELECT STRAP

High: 3.0V +/-5%
Low: 3.3V +/-5%

13 INPUT3VSEL — INPUT3VSEL — +3V_DEEP_SUS — @R705 *4.7K_5%_2 — R706 100K_5%_2

Flash Descriptor Security Override

High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K

GPP_R2

13 ACZ_SDOUT — ACZ_SDOUT — +3V_DEEP_SUS — @R677 *4.7K_5%_2

34 ME_WR# — R679 1K_5%_2

XTAL INPUT FREQUENCY [0]

HVM ONLY

00: DIVIDE BYPASS
01: DIVIDE BY 2 (HVM: 38.4MHZ INPUT)
10: DIVIDE BY 10 (HVM: 250MHZ INPUT)
11: DIVIDE BY 4 (BI: 100MHZ INPUT)
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

GPP_E10

9 GPP_E10 — +1.8V_DEEP_SUS +3V_DEEP_SUS — R747 20K_1%_2 — @R735 *20K_1%_2 — @R725 *20K_1%_2

XTAL INPUT FREQUENCY [1]

HVM ONLY

00: DIVIDE BYPASS
01: DIVIDE BY 2 (HVM: 38.4MHZ INPUT)
10: DIVIDE BY 10 (HVM: 250MHZ INPUT)
11: DIVIDE BY 4 (BI: 100MHZ INPUT)
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

GPP_E11

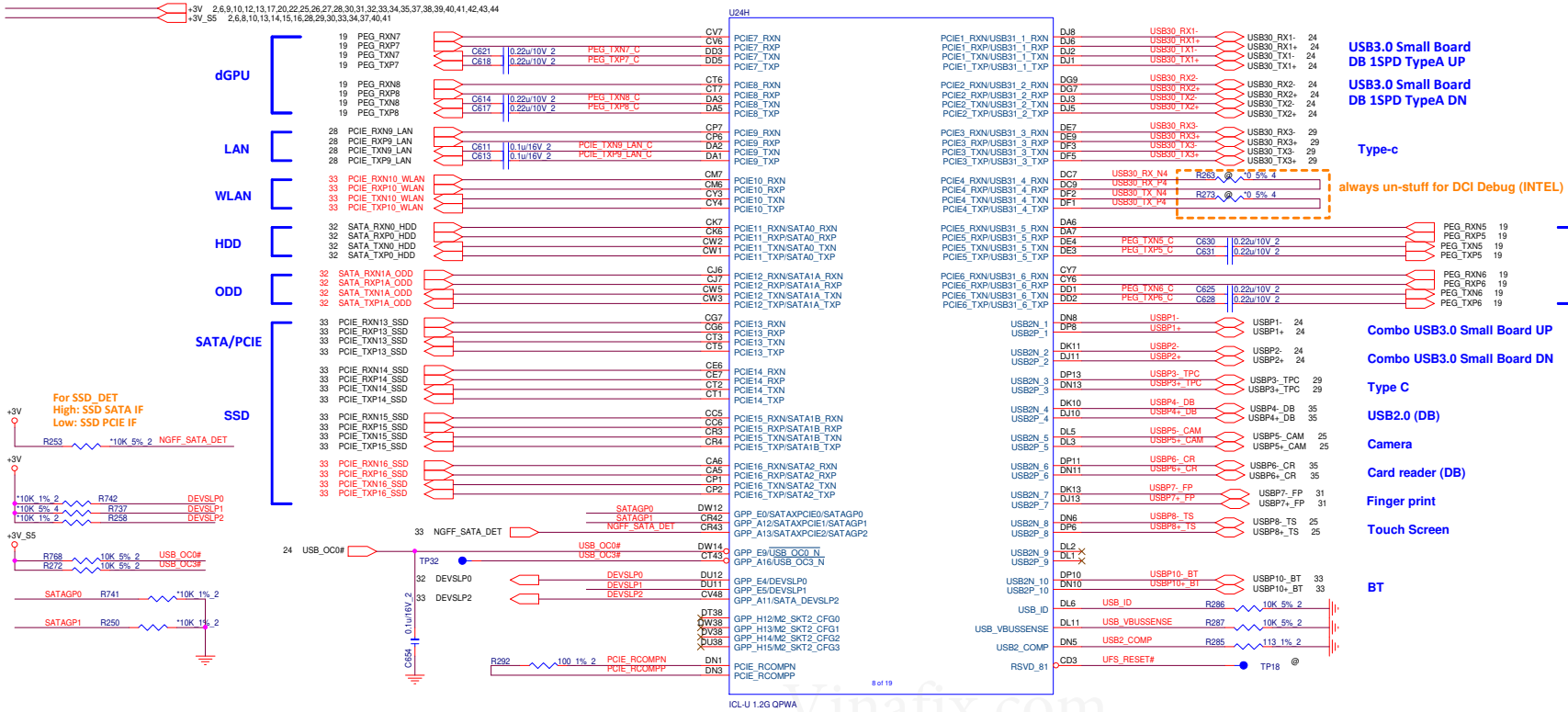
9 GPP_E11 — +1.8V_DEEP_SUS +3V_DEEP_SUS — R750 20K_1%_2 — @R739 *20K_1%_2

+1.8V_DEEP_SUS 5,14,33
+3V 2,6,9,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,41,42,43,44
+3V_S5 2,6,8,11,13,14,15,16,28,29,30,33,34,37,40,41
+3V_DEEP_SUS 9,14
+VCC1.05_OUT_FET 14,16

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 9/14 (HW STRAP)	3A

Date: Monday, November 04, 2019 Sheet 10 of 47



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port5	dGPU	Port0	VGA
Port6	dGPU	Port1	SSD
Port7	dGPU	Port2	Un-used
Port8	dGPU	Port3	Un-used
Port9	LAN	Port4	LAN
Port10	WLAN	Port5	WLAN
Port11	HDD		
Port12	ODD		
Port13	PCIE SSDx4		
Port14	PCIE SSDx4		
Port15	PCIE SSDx4		
Port16	PCIE SSDx4 /SATA SSD		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 Type A
PORT-2	USB3.0 Type A
PORT-3	Type C
PORT-4	NC

SATAGP1:GPP_E1 - SATA#1/PCIE#8
SATA => High < Base U>
PCIE => Low

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 Type A
PORT-2	Cobime USB3.0 Type A
PORT-3	Type C
PORT-4	USB 2.0 Small board
PORT-5	Camera
PORT-6	Card reader
PORT-7	Finger Print
PORT-8	Touch Screen
PORT-9	NC
PORT-10	BT (CNVI)

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 10/14(USB/PCIE/SAT)	3A

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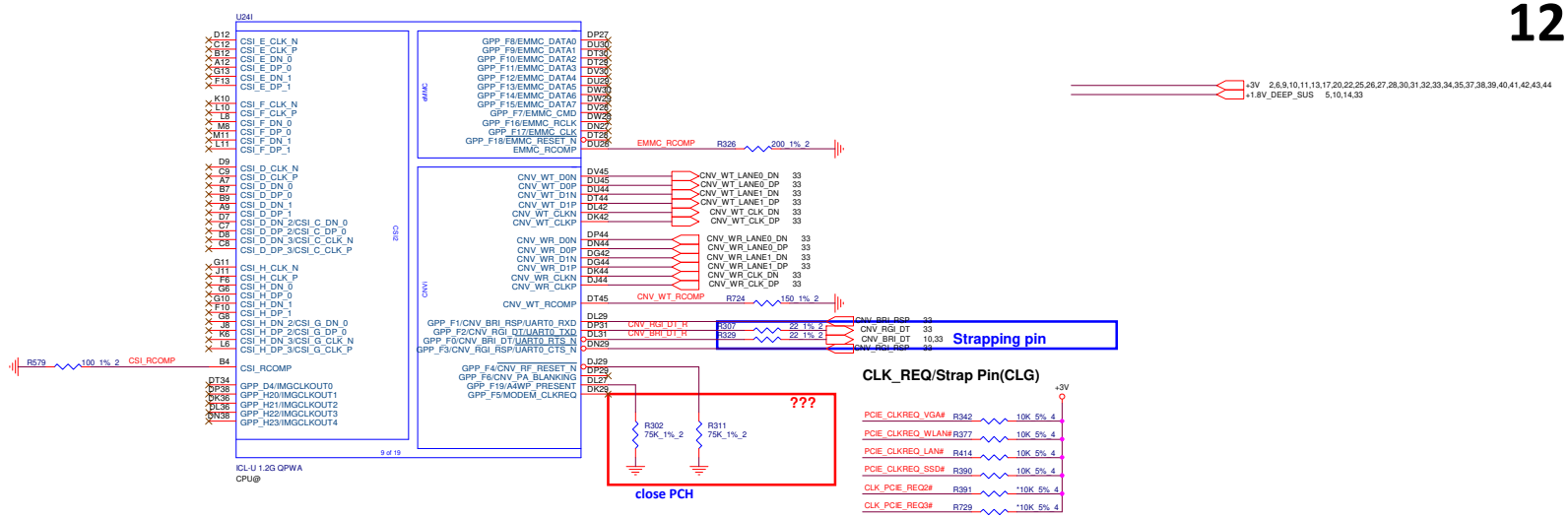
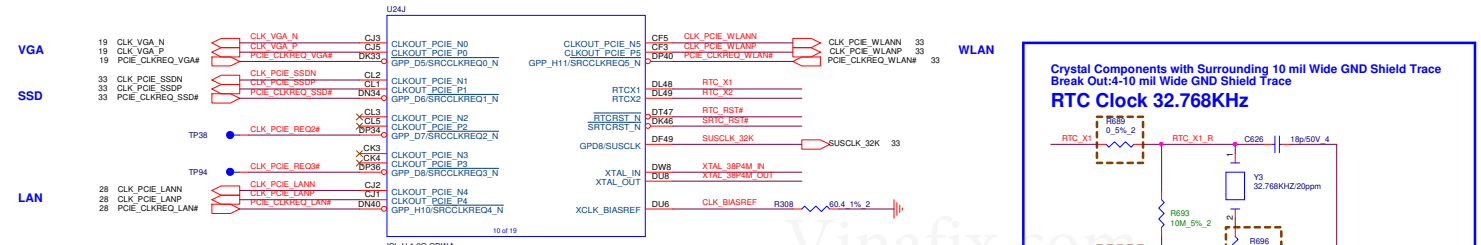
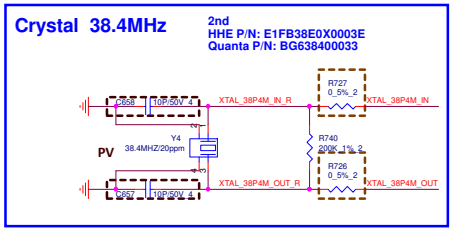
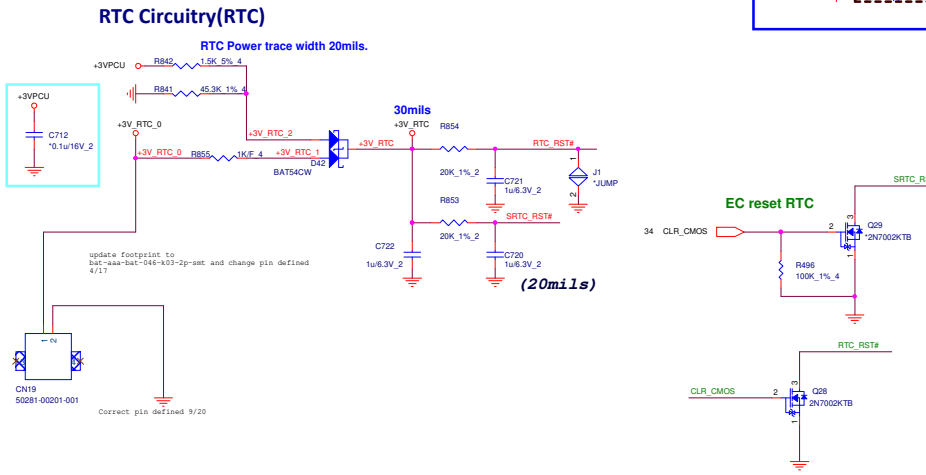
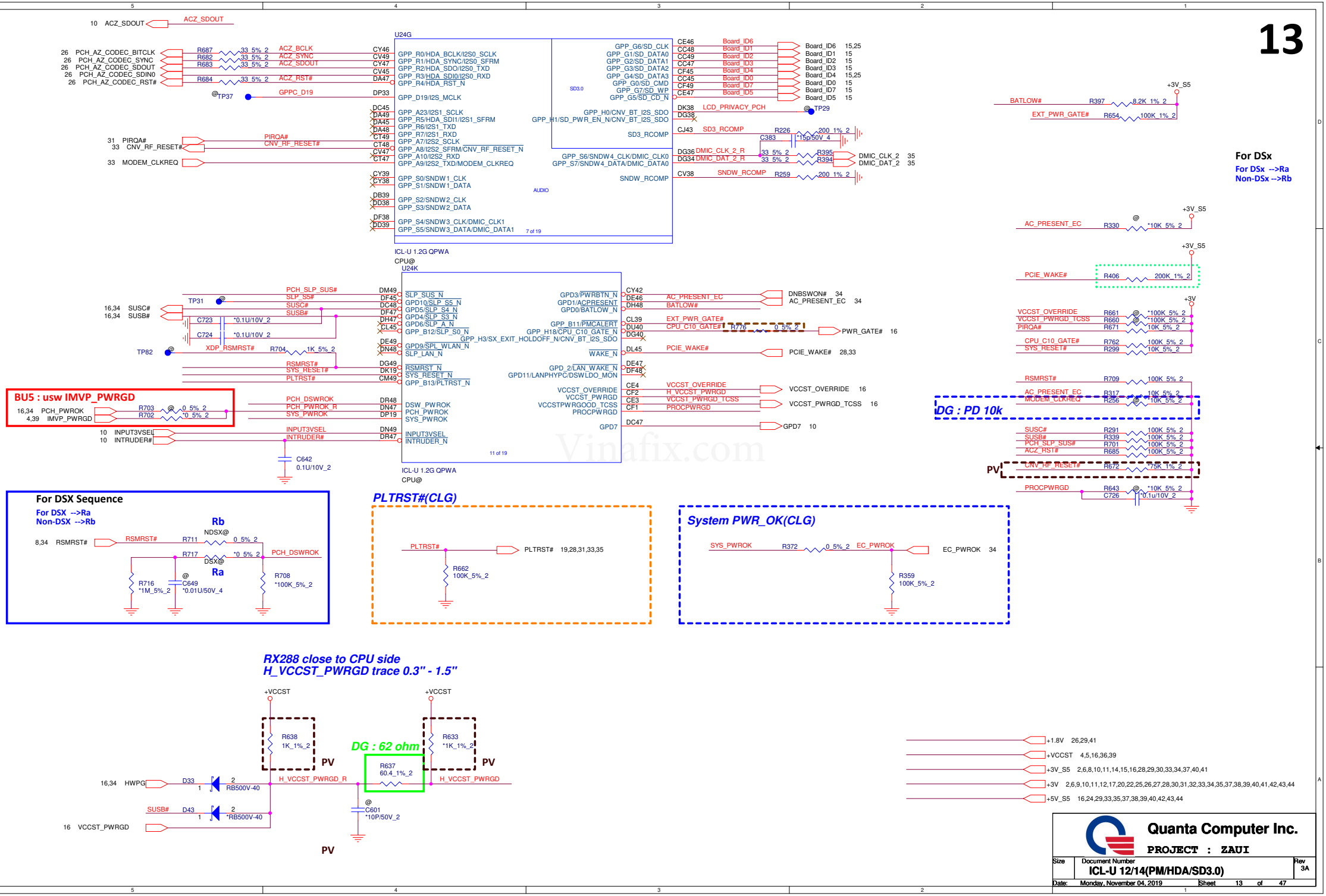








Quanta Computer Inc.
PROJECT : ZAUI
Size | Document Number: ICL-U 11/14(CSI/CNVI/CLK) | Rev: 3A
Date: Monday, November 04, 2019 | Sheet 12 of 47



Quanta Computer Inc.	
PROJECT : ZAUI	
Size	Document Number: ICL-U 12/14(PM/HDA/SD3.0) — Rev: 3A
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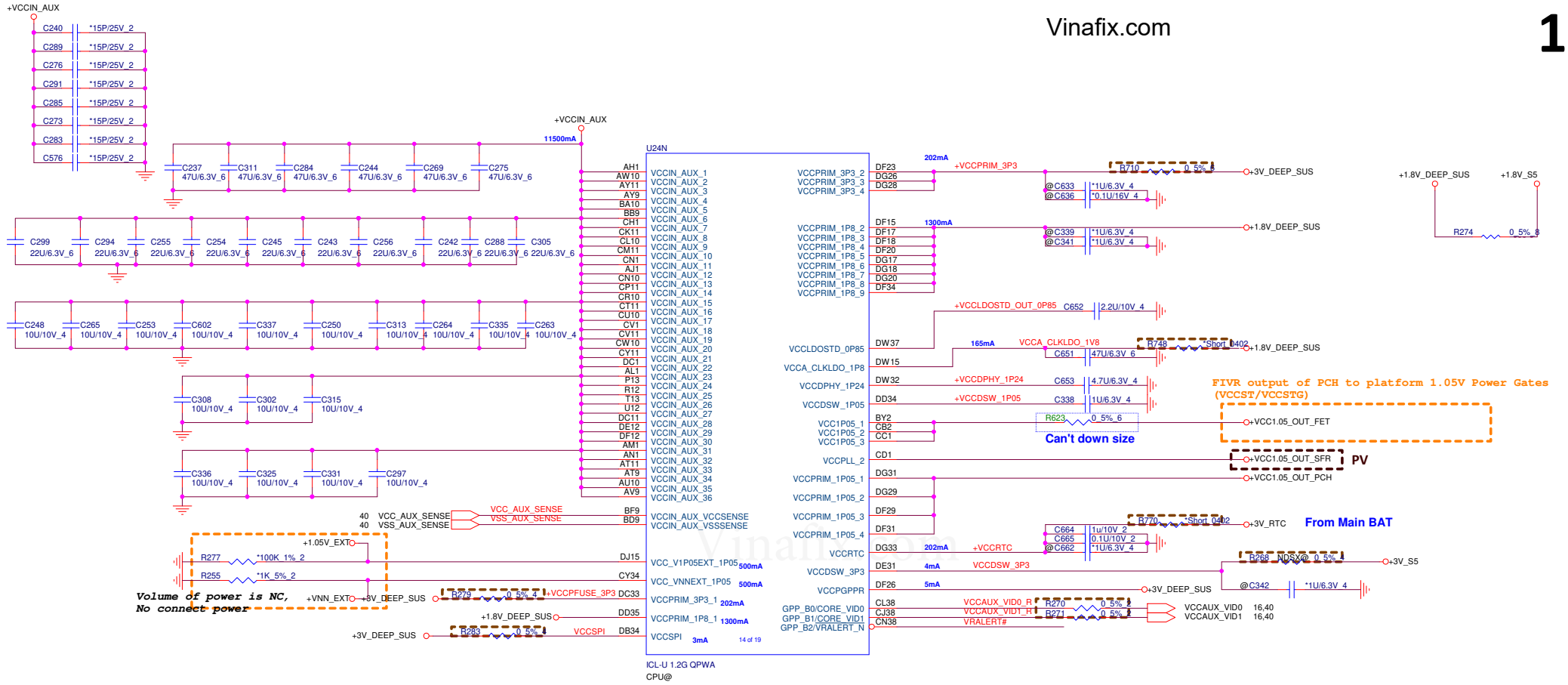
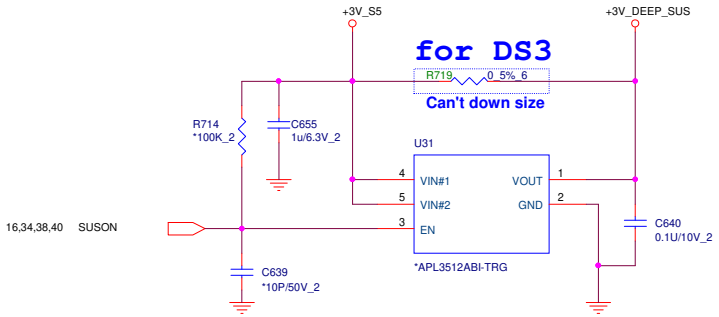
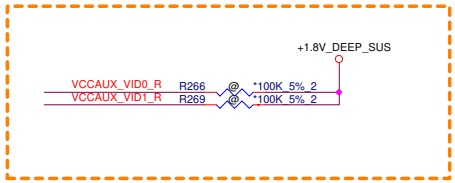
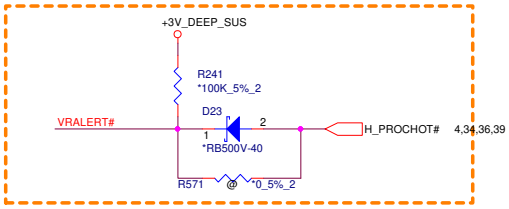
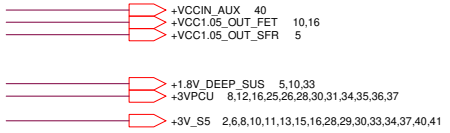










Quanta Computer Inc.

PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 13/14(PCH POWER)	3A

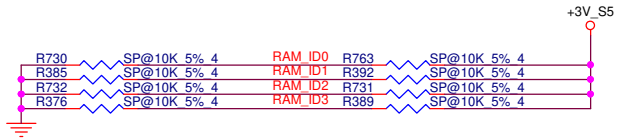
Date: Monday, November 04, 2019 Sheet 14 of 47

+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,41,42,43,44
+3V_S5 2,6,8,10,11,13,14,16,28,29,30,33,34,37,40,41

2 RAM_ID0 → RAM_ID0
2 RAM_ID1 → RAM_ID1
2 RAM_ID2 → RAM_ID2
2 RAM_ID3 → RAM_ID3

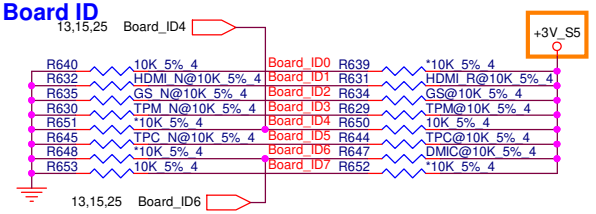
13,15,25 Board_ID6 → Board_ID6
13 Board_ID1 → Board_ID1
13 Board_ID2 → Board_ID2
13 Board_ID3 → Board_ID3
13,15,25 Board_ID4 → Board_ID4
13 Board_ID0 → Board_ID0
13 Board_ID7 → Board_ID7
13 Board_ID5 → Board_ID5

RAM ID



ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	Hynix 8Gb	H5AN8G6NCJR-VKC	AKD5QGSTW13
0	0	0	1	Micron 8Gb	MT40A512M16LY-075:E	AKD5LZSTL24
0	0	1	0	Micron 8Gb	MT40A512M16TB-062E:J	AKD5QGSTL23
0	0	1	1	Samsung 8Gb	K4A8G165WC-BCTD	AKD5QGST512
1	1	1	1	With out on board memory		

Board ID



	Low	High
BOARD_ID0	Non eMMC	eMMC
BOARD_ID1	HDMI_N@	HDMI_R@
BOARD_ID2	Non G-sensor(GS_N@)	G-sensor(GS@)
BOARD_ID3	Non TPM(TPM_N@)	TPM(TPM@)
BOARD_ID4	Non Touch panel	Touch panel (Control by Cable)
BOARD_ID5	Non Type-C(TPC_N@)	Type-C(TPC@)
BOARD_ID6	Single MIC(Cable control)	Dual MIC (DMIC@)
BOARD_ID7	Reserved (Default)	Reserve

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	ICL-U 14/14 (Board ID)	3A

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Volume Segment
ICL U42

Volume Segment
VCCST: 0.65A
<= 65us full load ready

C10: turn off VCCPLL_OC , VCCIO , VCCSTG

<= 240us, full load ready
TDC:0.26A

fine tune <65usec

fine tune <65usec

VCCST_CPU GENERATION

VCCSTG: 0.15A

VCCST PWRGD CRB is via +1.05V PG

B2A
S0->S5 & S0->S3
Power of sequence 1us
SUSB# -> VCCST_PWRGD

Shortpad change to 60.4 ohm. 11/6

Stuff 1000P/50V

Reserve 1000P/50V

Rev:D change to shortpad

PROJECT : G7AL
Quanta Computer Inc.

BU5

Size	Document Number	Rev
C	+1.0V/+VCCSTPLL	1A

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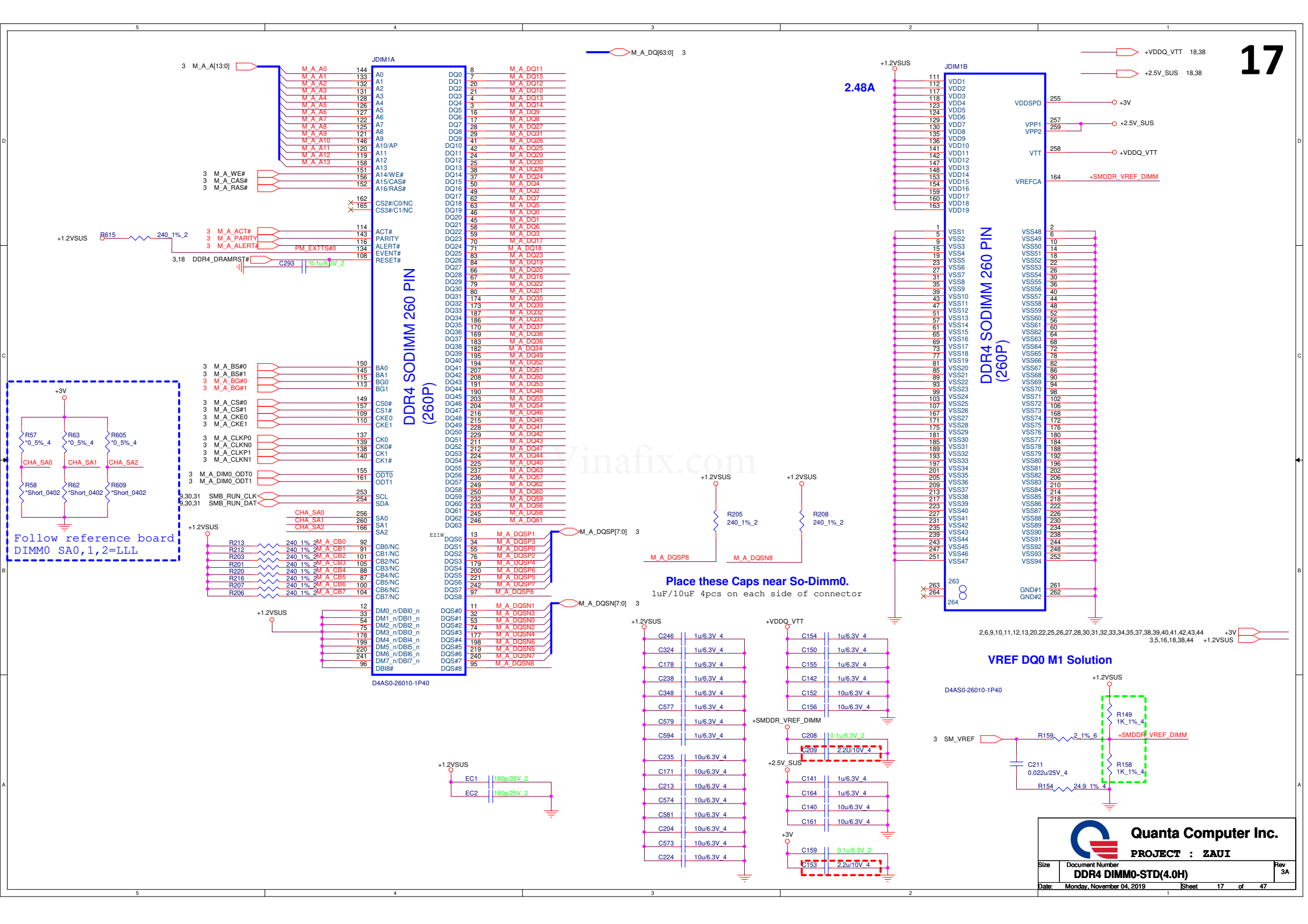
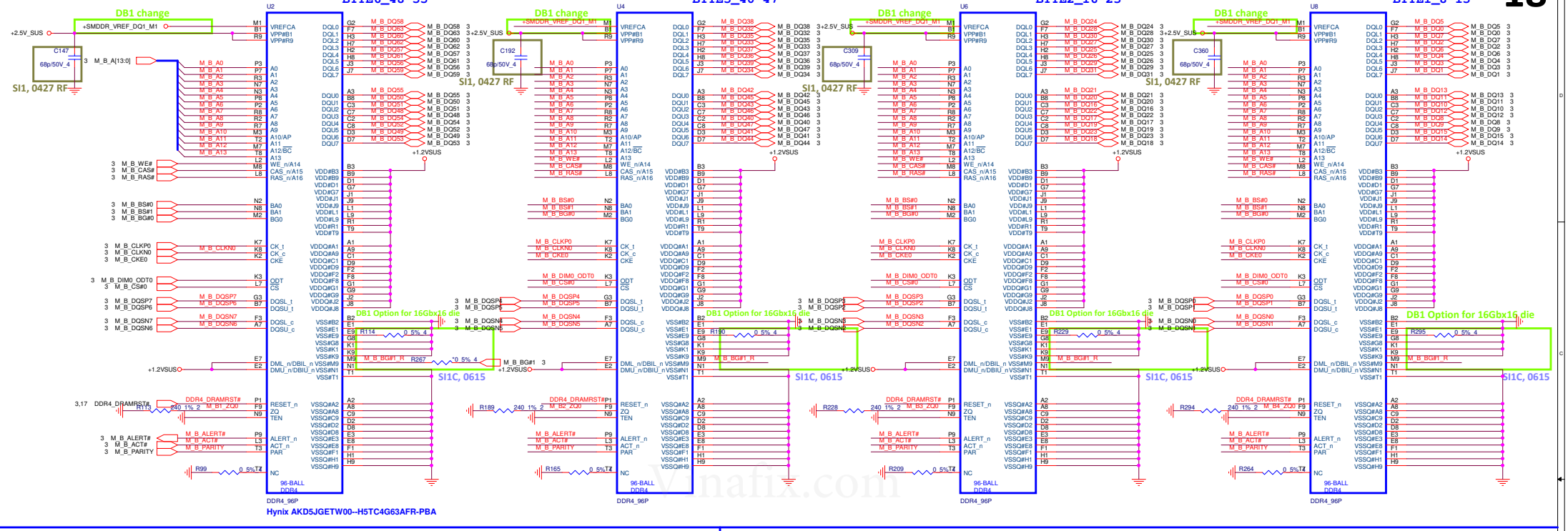

JDIM1A
DDR4 SODIMM 260 PIN (260P)
D4AS0-26010-1P40
JDIM1B
DDR4 SODIMM 260 PIN (260P)
2.48A
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
Quanta Computer Inc.
PROJECT : ZAUI
DDR4 DIMM0-STD(4.0H)
Monday, November 04, 2019



Vendor	P/N	Vendor P/N
MIC 16G	AKD5EG0TL00	MT40A1G16HBA-083E:A
Elpida		
SAMSUNG		

DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS

M_B_BG#1_R R120 0_5%_4

DB1 Option for 16Gbx16 die
Close DDR ball

M_B_BS#1 delete 36 ohm put it back later

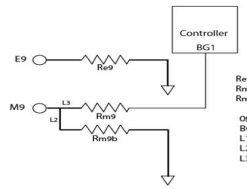
DB1 12/11, close memory

DB1 1/18, close cpu

DB1 12/11, close memory

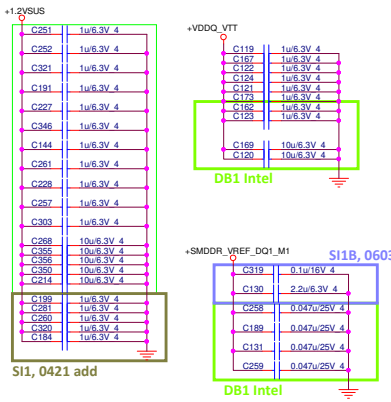
Memory 8G & Memory 16G TABLE

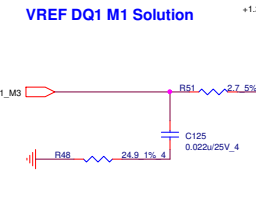
	Memory 8G	Memory 16G
R278	0Ω CS00002JB38	240Ω CS12402FB03
R279	0Ω CS00002JB38	240Ω CS12402FB03
R280	0Ω CS00002JB38	240Ω CS12402FB03
R281	0Ω CS00002JB38	240Ω CS12402FB03
R282	UNINSTAL	INSTAL
R283	UNINSTAL	INSTAL
R284	UNINSTAL	INSTAL
R285	UNINSTAL	INSTAL
R290	INSTAL	UNINSTAL
R291	INSTAL	UNINSTAL
R292	INSTAL	UNINSTAL
R293	INSTAL	UNINSTAL

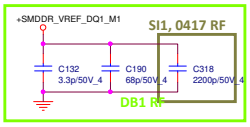


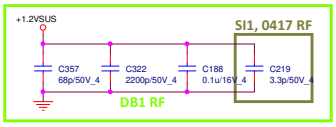
Place these Caps near Channel B

1uF/10uF 4pcs on each side of connector









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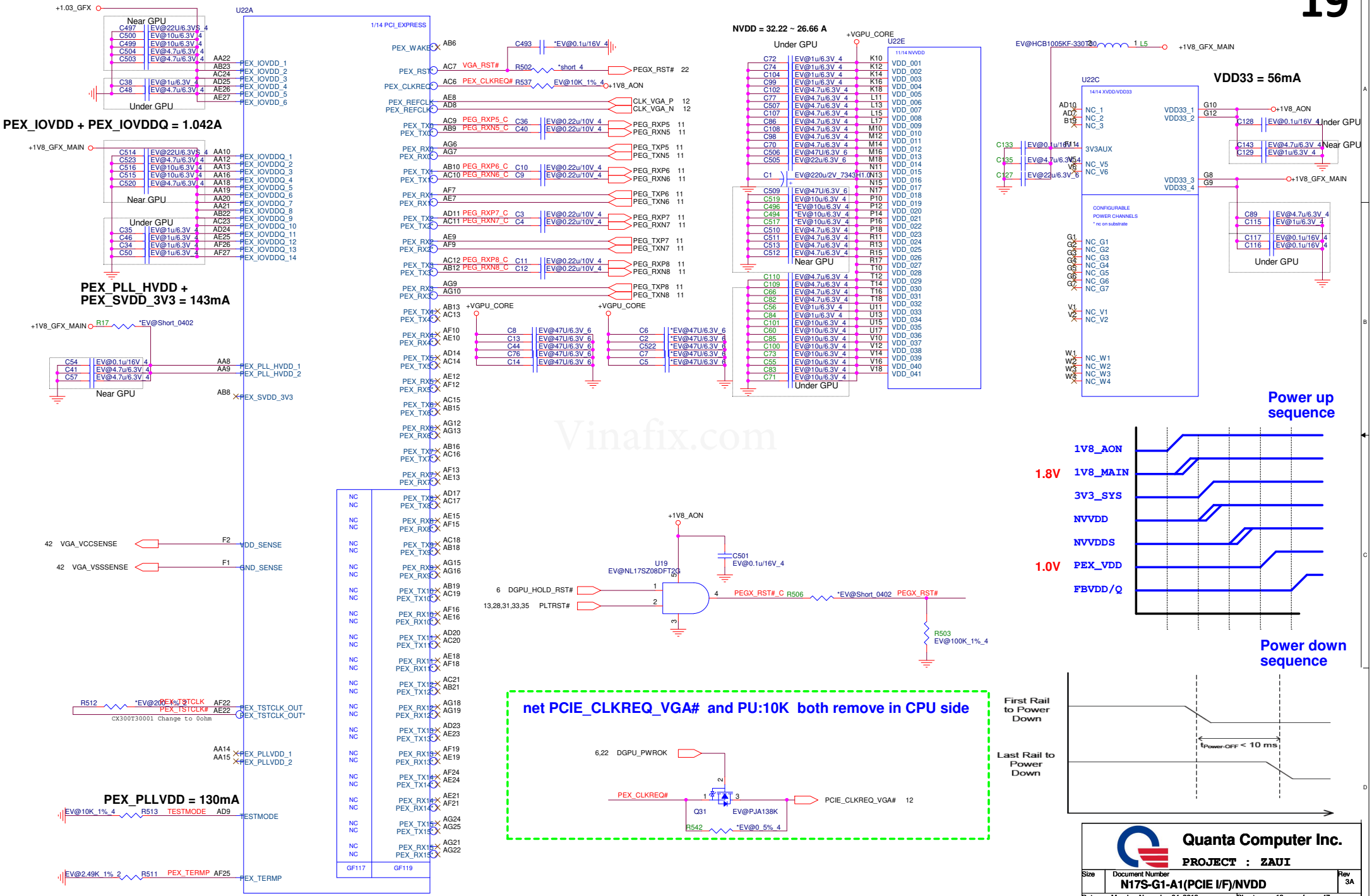
PROJECT : ZAUI

Size	Document Number	Rev
	DDR4 Memory Down (CH. B)	3A
Date: Monday, November 04, 2019	Sheet 18 of 47	


PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Near GPU
Under GPU
U22A
U22E
U22C
1/14 PCI_EXPRESS
11/14 NVVDD
14/14 XVDD/VDD33
+1.03_GFX
+1V8_GFX_MAIN
+1V8_AON
+VGPU_CORE
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDD_6
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_PLL_HVDD_1
PEX_PLL_HVDD_2
PEX_SVDD_3V3
PEX_PLLVDD_1
PEX_PLLVDD_2
PEX_TERMP
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*
TESTMODE
VDD_SENSE
GND_SENSE
VGA_VCCSENSE
VGA_VSSSENSE
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
VGA_RST#
PEX_CLKREQ#
PEGX_RST#
CLK_VGA_P
CLK_VGA_N
PEG_RXP5
PEG_RXN5
PEG_TXP5
PEG_TXN5
PEG_RXP6
PEG_RXN6
PEG_TXP6
PEG_TXN6
PEG_RXP7
PEG_RXN7
PEG_TXP7
PEG_TXN7
PEG_RXP8
PEG_RXN8
PEG_TXP8
PEG_TXN8
PEX_TERMP
CX300T30001 Change to 0ohm
net PCIE_CLKREQ_VGA# and PU:10K both remove in CPU side
DGPU_HOLD_RST#
PLTRST#
DGPU_PWROK
PEGX_RST#_C
PCIE_CLKREQ_VGA#
Power up sequence
Power down sequence
1V8_AON
1V8_MAIN
3V3_SYS
NVVDD
NVVDDS
PEX_VDD
FBVDD/Q
1.8V
1.0V
First Rail to Power Down
Last Rail to Power Down
tPower-OFF < 10 ms
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PROJECT : ZAUI
N17S-G1-A1(PCIE I/F)/NVDD
Monday, November 04, 2019
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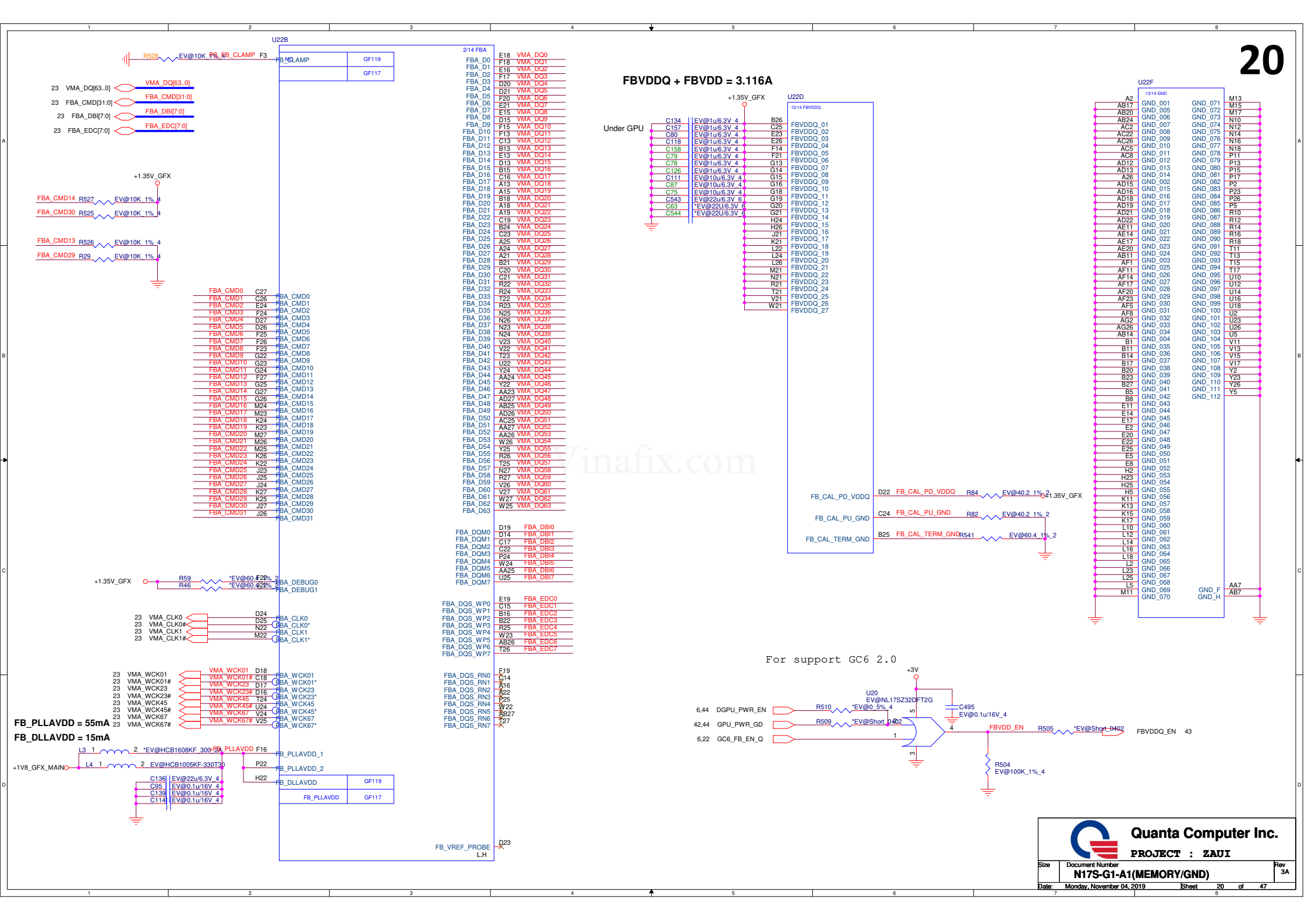

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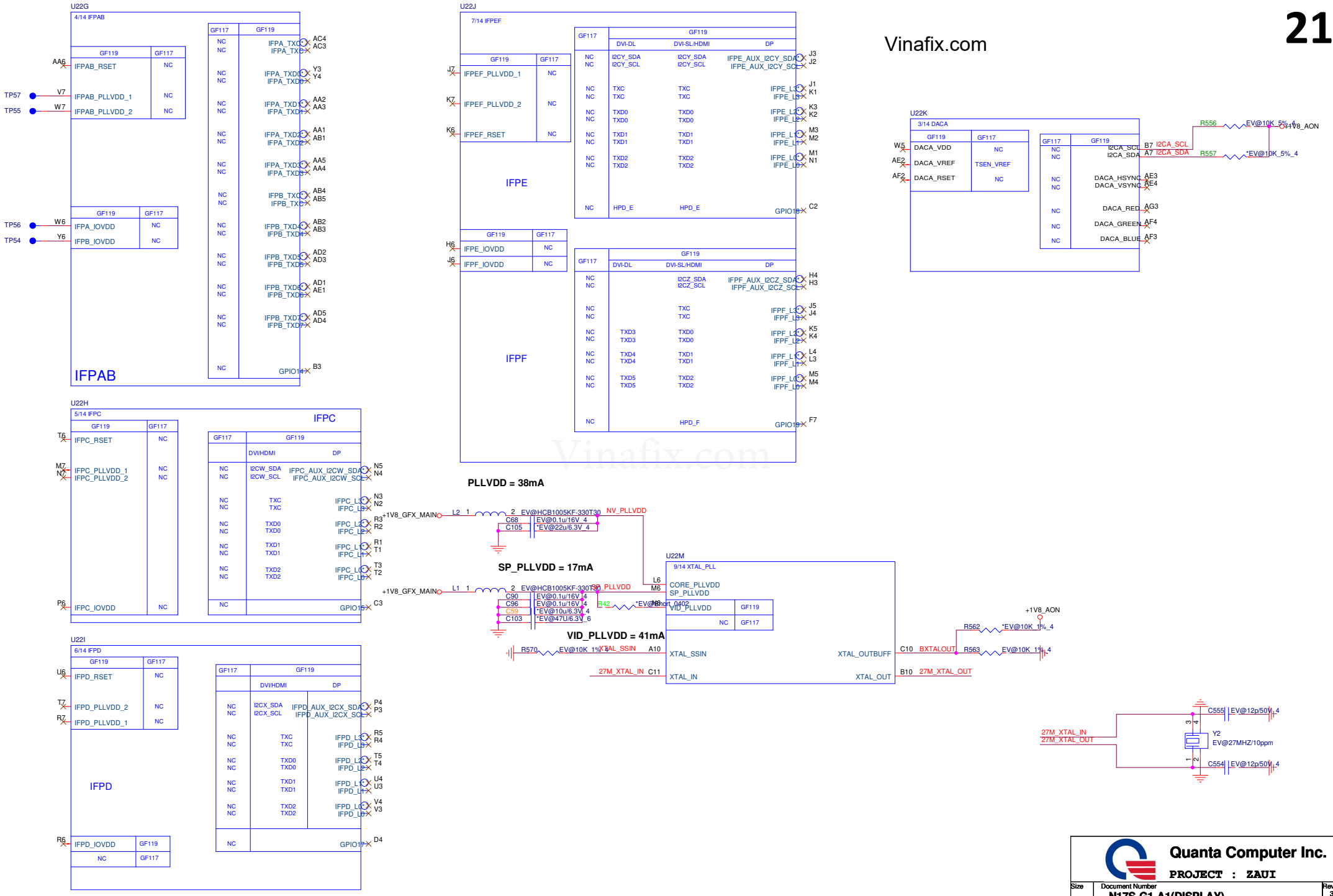
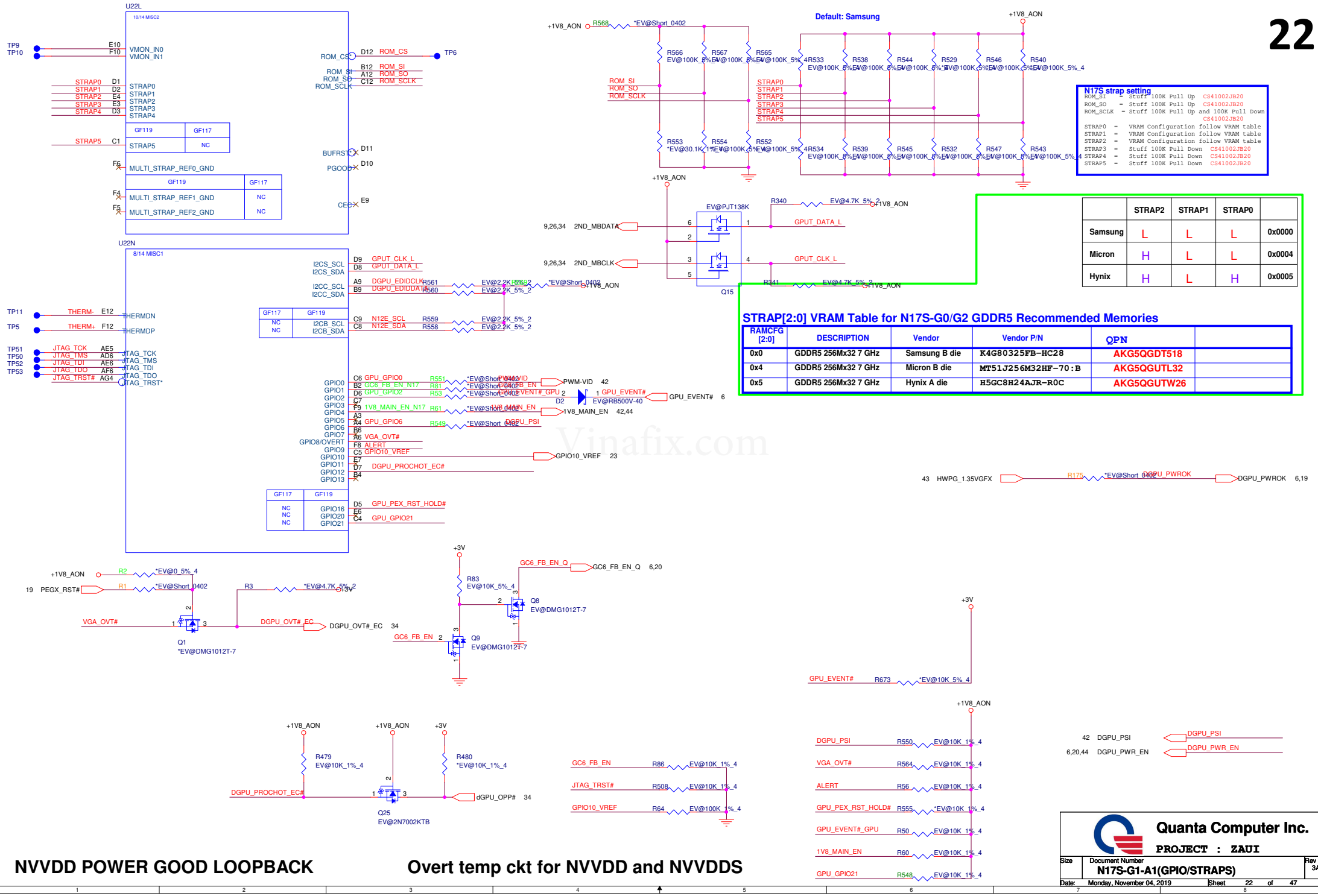
PROJECT : ZAUI

Size	Document Number	Rev
	N17S-G1-A1(MEMORY/GND)	3A

Date: Monday, November 04, 2019 Sheet 20 of 47



Quanta Computer Inc.	
PROJECT : ZAUI	
Size	Document Number: N17S-G1-A1(DISPLAY) — Rev: 3A
Date: Monday, November 04, 2019	Sheet 21 of 47


U22L
10/14 MISC2
VMON_IN0
VMON_IN1
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
STRAP5
MULTI_STRAP_REF0_GND
MULTI_STRAP_REF1_GND
MULTI_STRAP_REF2_GND
ROM_CS
ROM_SI
ROM_SO
ROM_SCLK
BUFRST#
PGOOD
CEC
U22N
8/14 MISC1
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
N12E_SCL
N12E_SDA
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8/OVERT
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPU_PEX_RST_HOLD#
Default: Samsung
N17S strap setting
STRAP[2:0] VRAM Table for N17S-G0/G2 GDDR5 Recommended Memories
RAMCFG [2:0]
DESCRIPTION
Vendor
Vendor P/N
QPN
0x0
GDDR5 256Mx32 7 GHz
Samsung B die
K4G80325FB-HC28
AKG5QGDT518
0x4
GDDR5 256Mx32 7 GHz
Micron B die
MT51J256M32HF-70:B
AKG5QGUTL32
0x5
GDDR5 256Mx32 7 GHz
Hynix A die
H5GC8H24AJR-R0C
AKG5QGUTW26
STRAP2
STRAP1
STRAP0
Samsung
Micron
Hynix
0x0000
0x0004
0x0005
EV@PJT138K
Q15
Q1
*EV@DMG1012T-7
Q8
EV@DMG1012T-7
Q9
EV@DMG1012T-7
Q25
EV@2N7002KTB
EV@RB500V-40
PWM-VID
1V8_MAIN_EN
GPU_EVENT#
GPIO10_VREF
DGPU_PROCHOT_EC#
DGPU_PSI
DGPU_PWROK
DGPU_OVT#_EC
dGPU_OPP#
GC6_FB_EN_Q
GC6_FB_EN
JTAG_TRST#
GPIO10_VREF
DGPU_PWR_EN
NVVDD POWER GOOD LOOPBACK
Overt temp ckt for NVVDD and NVVDDS
Quanta Computer Inc.
PROJECT : ZAUI
Size
Document Number
N17S-G1-A1(GPIO/STRAPS)
Rev
3A
Date: Monday, November 04, 2019
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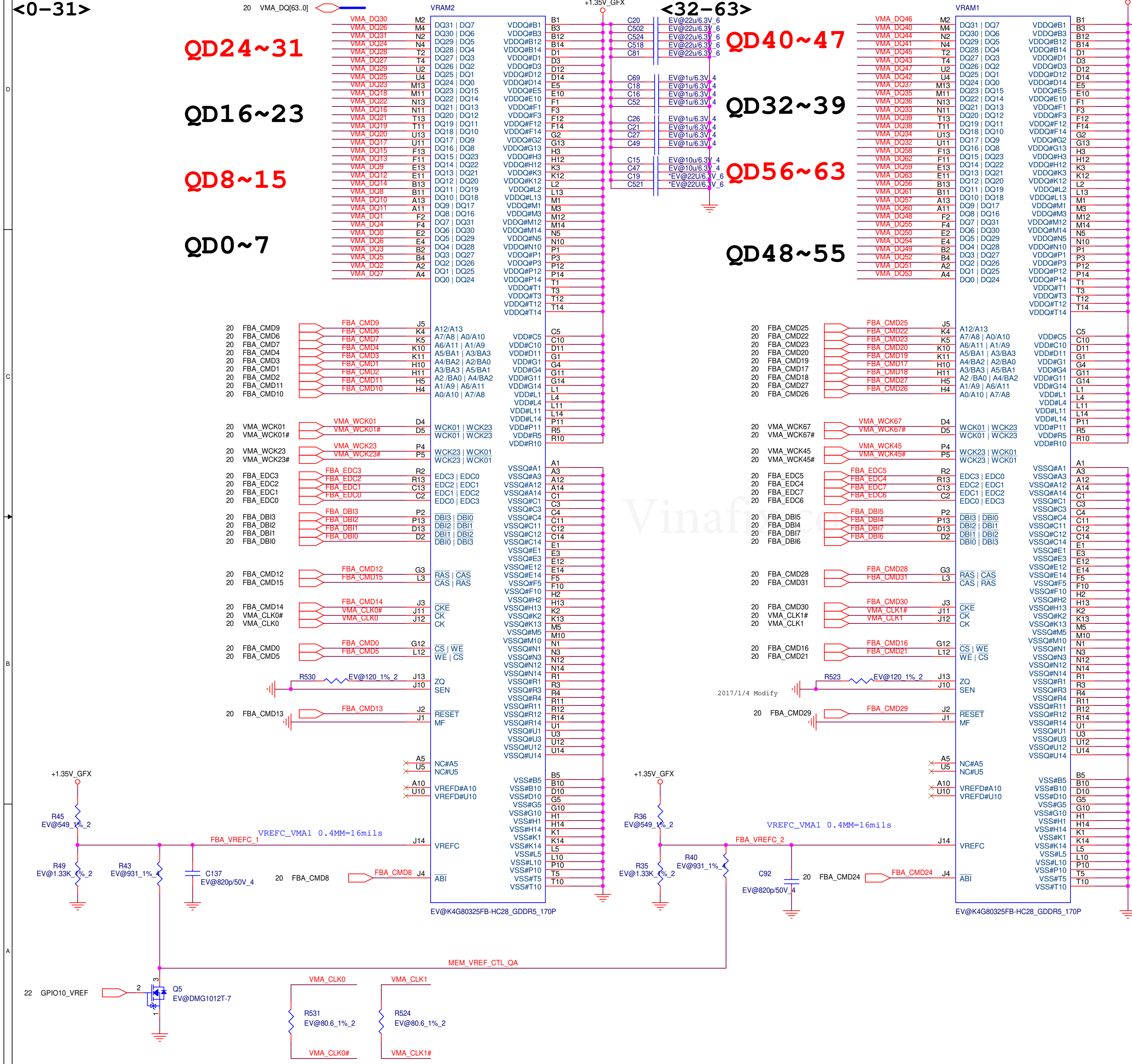
MF=0 Non-mirrored

Channel 0 MF=0 Non-mirrored <0-31>

CHANNEL A: 2G/4G GDDR5

Channel 0 MF=0 Non-mirrored <32-63>



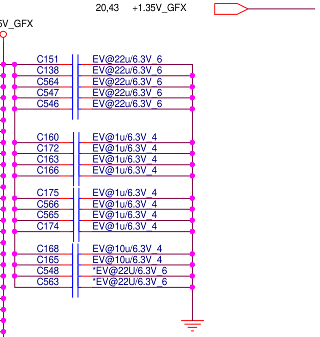


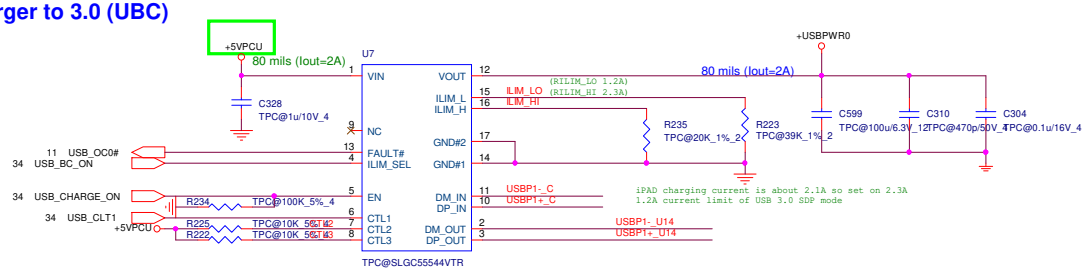
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

USB Charger to 3.0 (UBC)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

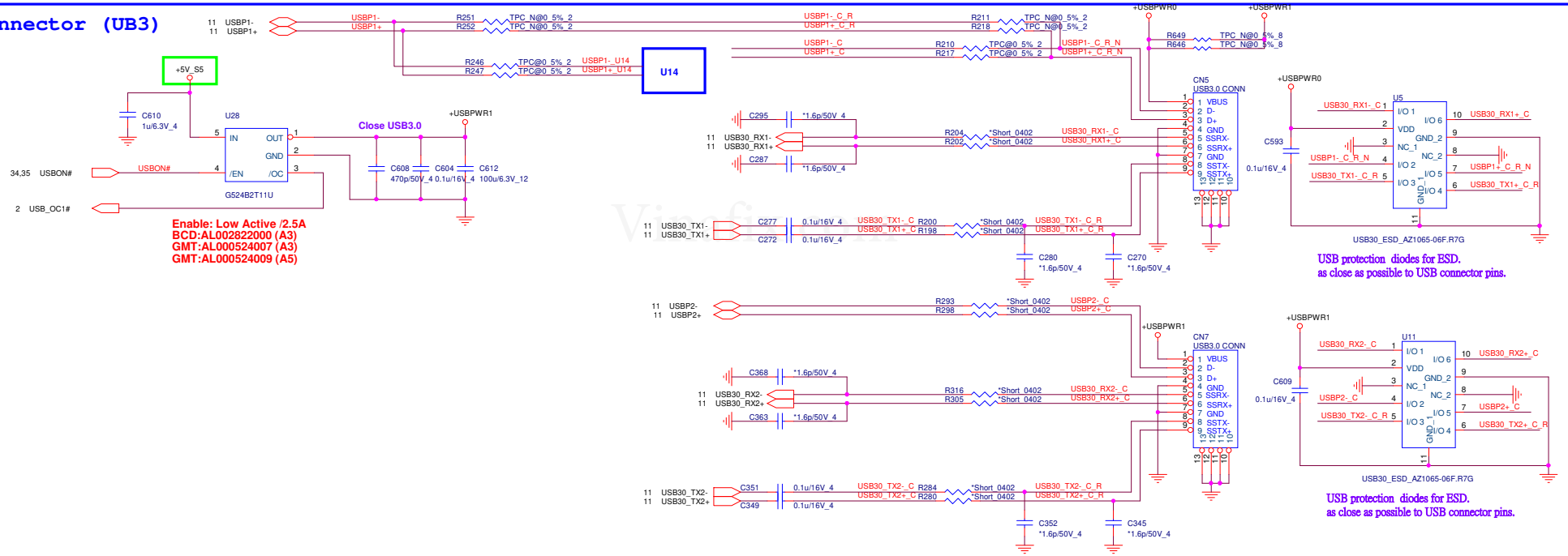
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

+5VPCU 26,37,44
+5V_S5 16,29,33,35,37,38,39,40,42,43,44
+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,41,42,43,44

USB 3.0 Connector (UB3)



CAP close to different CONN

Quanta Computer Inc.		
PROJECT : ZAUI		
Size	Document Number	Rev
	USB3/Charger	3A
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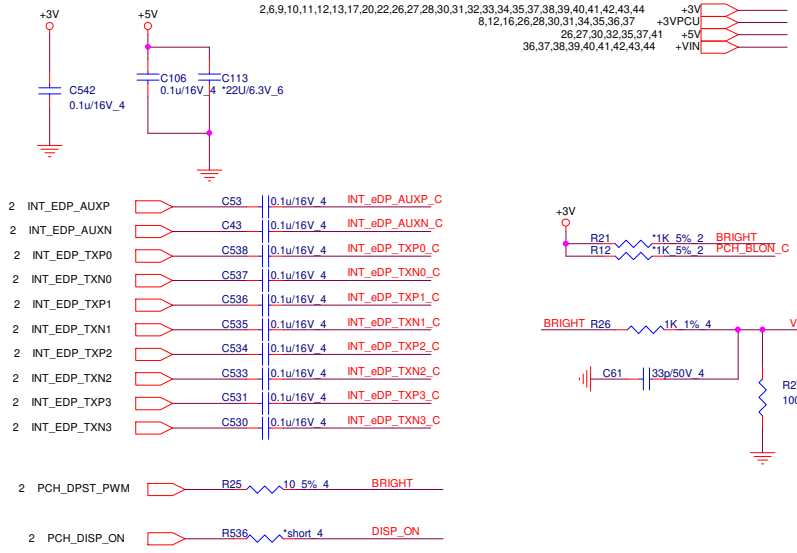

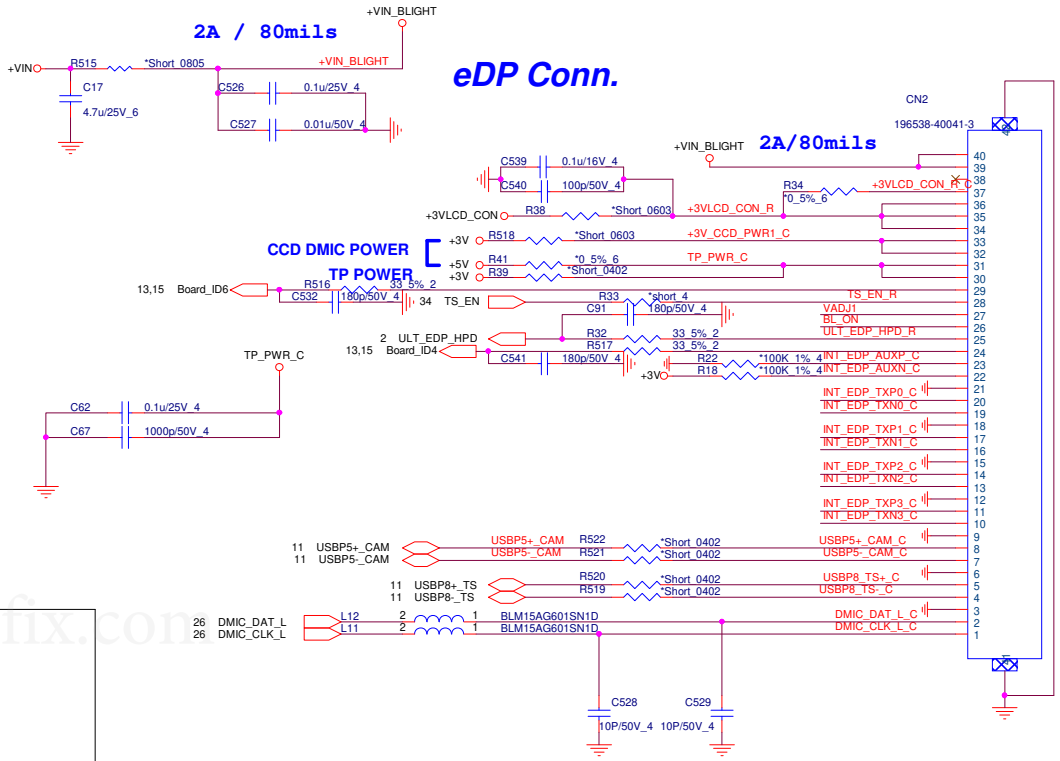

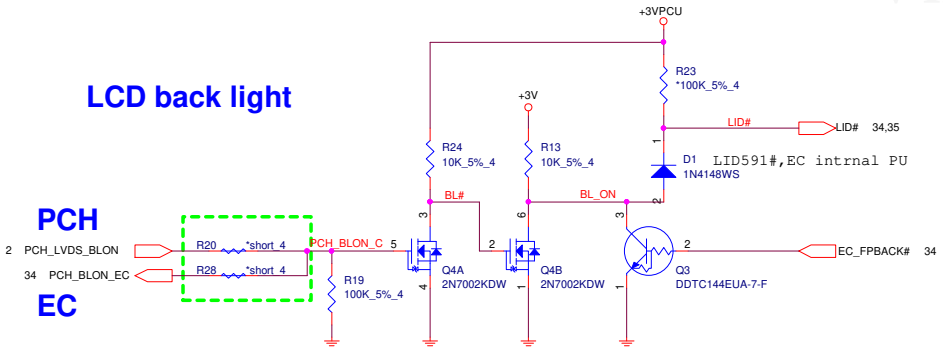

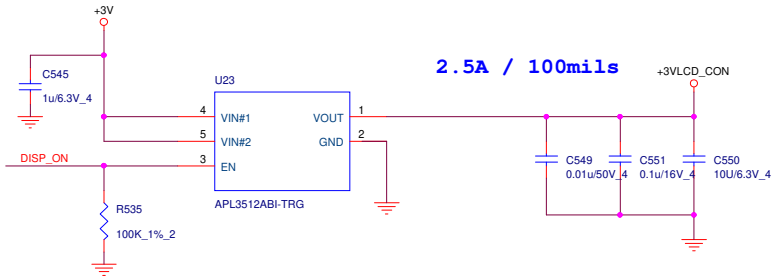

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	eDP CONN/LID/CAM/D-MIC/TS	3A
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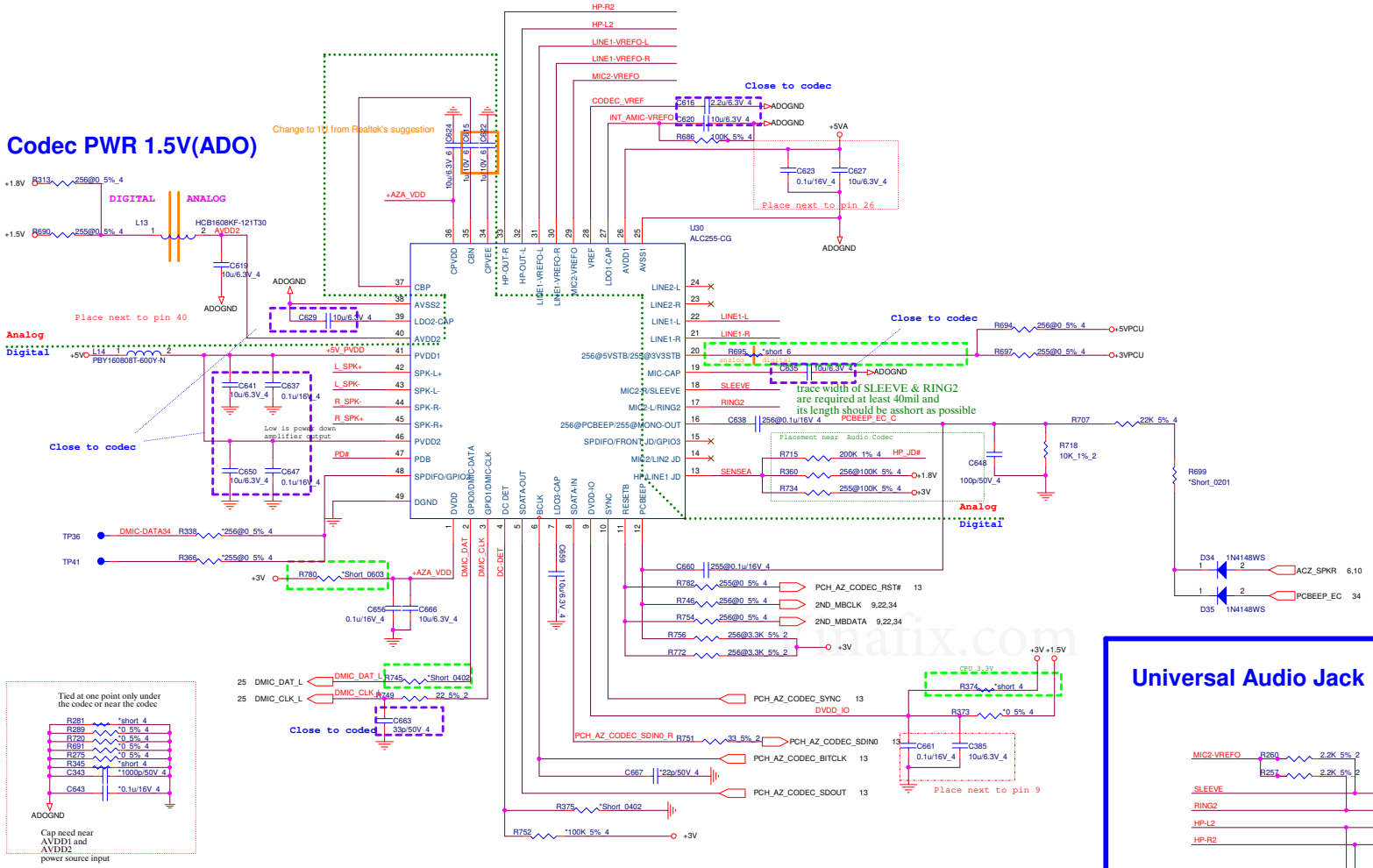
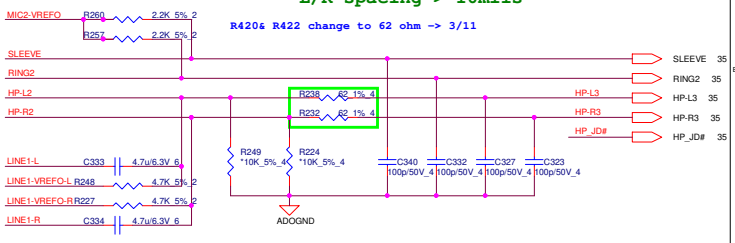
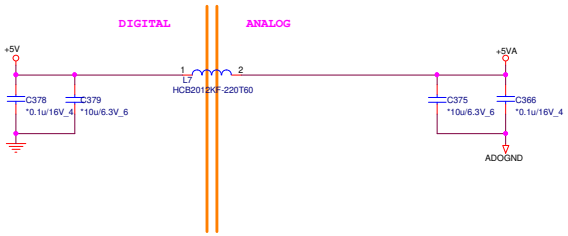
Codec(ADO)



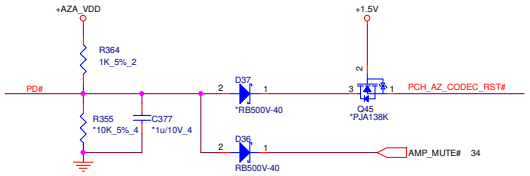
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



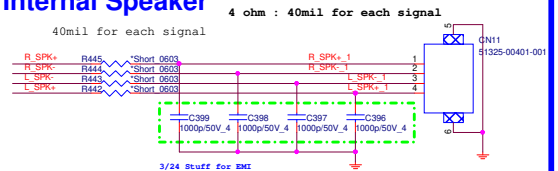
Codec PWR 5V(ADO)



Mute(ADO)



Internal Speaker



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PROJECT : ZAUI

Size	Document Number	Rev
	Audio Codec/HP/SPK/Hole	3A

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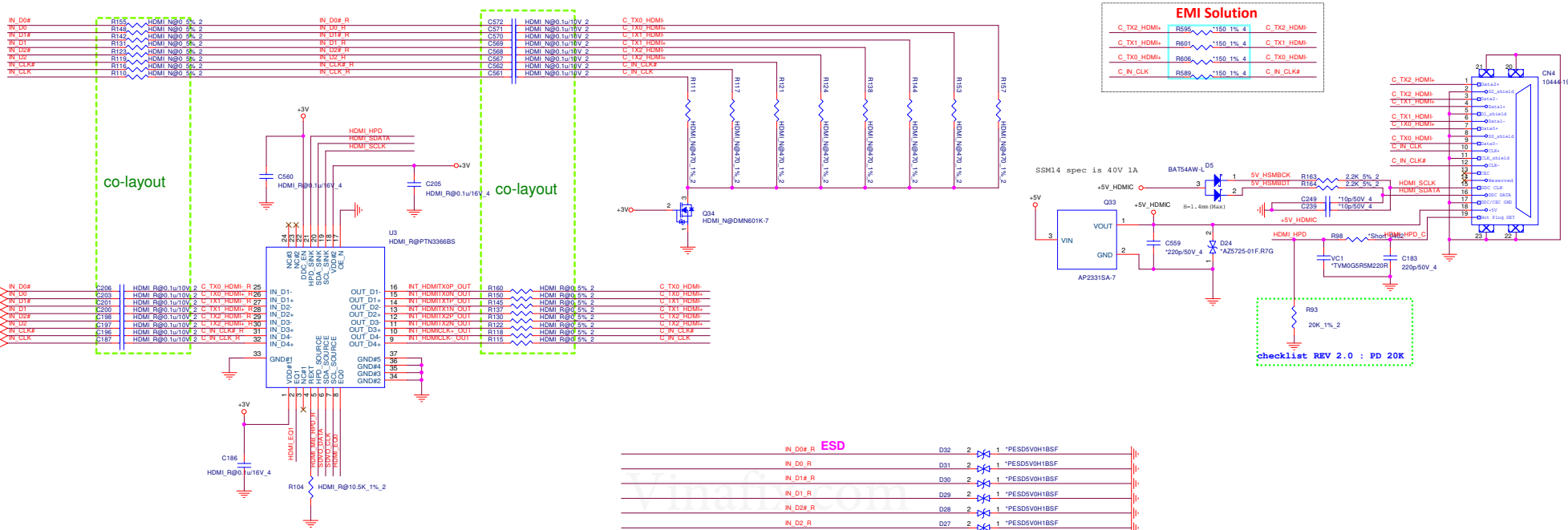
HDMI CONN



HDMI

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

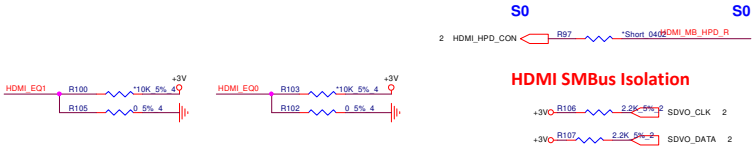
From PCH

ESD

The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

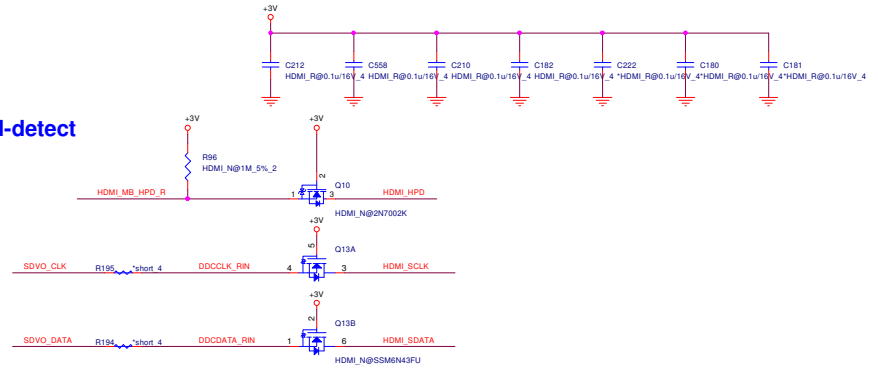
Table 5. Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB



HDMI SMBus Isolation

HDMI-detect



Quanta Computer Inc.	
PROJECT : ZAUI	
Size	Document Number: HDMI/AMP HPA022642RTJR
Rev	3A
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LAN RTL8111HSH-CG

For LDO mode support
RTL8107ESH-CG/RTL8111HSH-CG
Stuff: La, Ca ,Cb

* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬度> 60mil

+1.05V_LAN_REGOUT — R4 La *Short_0805 — C22 0.1u/16V_4

+1.05V_LAN

PIN3	PIN8	PIN30	PIN22	PIN22	PIN22
Cc	Cd	Ce	Cf	Cg	Ch
C64 0.1u/16V_4	C58 0.1u/16V_4	C65 0.1u/16V_4	C45 0.1u/16V_4	C93 1u/6.3V_4	C39 0.1u/16V_4

LAN_AMBLED# TP4
LAN_LED1 TP2
LAN_LED2 TP3

if ISOLATEB pin pull-low,
the LAN chip will not drive it's PCI-E outputs
(excluding PCIE_WAKE# pin)

+1.05V_LAN
R6 2.49K_1%_4
+3V_LAN
LAN_AMBLED#
LAN_WLED#

+3V
R31 1K_5%_2
ISOLATEB
R30 15K_1%_2

U1 RTL8111HSH-CG

33 GND

Add 9 GND VIAs with thermal PAD

LAN_XTAL1 — R16 10_5%_4 — XTAL1
Y1 25MHZ/30ppm
R15 680_5%_4 — XTAL2
C33 15p/50V_4
C32 15p/50V_4

MDI0+ 1	MDIP0	REGOUT 24	+1.05V_LAN_REGOUT
MDI0- 2	MDIN0	VDDREG 23	+3V_LAN
3	AVDD10#1	DVDD10 22	+1.05V_LAN
MDI1+ 4	MDIP1	LANWAKEB 21	PCIE_WAKE# 13,33
MDI1- 5	MDIN1	ISOLATEB 20	ISOLATEB
MDI2+ 6	MDIP2	PERSTB 19	PLTRST#
MDI2- 7	MDIN2	HSON 18	PCIE_TXN_LAN_L C88 0.1u/16V_4 PCIE_TXN9_LAN 11
8	AVDD10#2	HSOP 17	PCIE_TXP_LAN_L C94 0.1u/16V_4 PCIE_TXP9_LAN 11

PLTRST# 13,19,31,33,35

MDIP3 MDIN3 AVDD33#1 CLKREQB HSIP HSIN REFCLK_P REFCLK_N
9 10 11 12 13 14 15 16

MDI3+ MDI3-
+3V_LAN — PCIE_REQ_LAN#_R
PCIE_TXN9_LAN PCIE_TXP9_LAN
CLK_PCIE_LANN 12
CLK_PCIE_LANP 12
PCIE_TXN9_LAN 11
PCIE_TXP9_LAN 11

For GbE
* Place RTL8111HSH-CG AL008111014
For 10/100
* Place RTL8107ESH-CG AL008107000

Leakage circuit (MPC)

CLK_PCIE_REQ4# have PU 10k.
+3V — R52 *10K_5%_4 — +3V — R55 10K_5%_4
MAIN POWER(3V_S0)
S0 12 PCIE_CLKREQ_LAN#
Q6 2N7002K
R44 10K_5%_4
PCIE_REQ_LAN#_R

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8107ESH-CG/RTL8111HSH-CG

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

+3V_LAN

PIN11	PIN32	PIN11	PIN32
C42 0.1u/16V_4 Cj	C51 0.1u/16V_4 Ck	C30 *4.7u/6.3V_4 Cm	C31 *4.7u/6.3V_4 Cn

For Giga：Ub

Ub
U21 NS892407

MDI2+ 2	TD1+	MX1+ 23	MDI2+_1
MDI2- 3	TD1-	MX1- 22	MDI2-_1
MDI3- 5	TD2+	MX2+ 20	MDI3-_1
MDI3+ 6	TD2-	MX2- 19	MDI3+_1
MDI0- 8	TD3+	MX3+ 17	MDI0-_1
MDI0+ 9	TD3-	MX3- 16	MDI0+_1
MDI1- 11	TD4+	MX4+ 14	MDI1-_1
MDI1+ 12	TD4-	MX4- 13	MDI1+_1
TRA_V_DAC 1	TCT1	MCT1 24	LAN_MCTG0 Ra R11 75_1%_8
TRA_V_DAC 4	TCT2	MCT2 21	LAN_MCTG1 Rb R10 75_1%_8
TRA_V_DAC 7	TCT3	MCT3 18	LAN_MCTG2 Rc R8 75_1%_8
TRA_V_DAC 10	TCT4	MCT4 15	LAN_MCTG3 Rd R9 75_1%_8
25	GND		

C97 0.01u/50V_4
For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00
For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd
C525 10p/3KV_1808

RJ45
CN3 2RJ1622-001111F

MDI3-_1	8	9	11
MDI3+_1	7		
MDI1-_1	6		
MDI2-_1	5		
MDI2+_1	4		
MDI1+_1	3		
MDI0-_1	2		
MDI0+_1	1	10	12

2018/11/06
Need change ther footprint

Reserve IOAC No Stuff

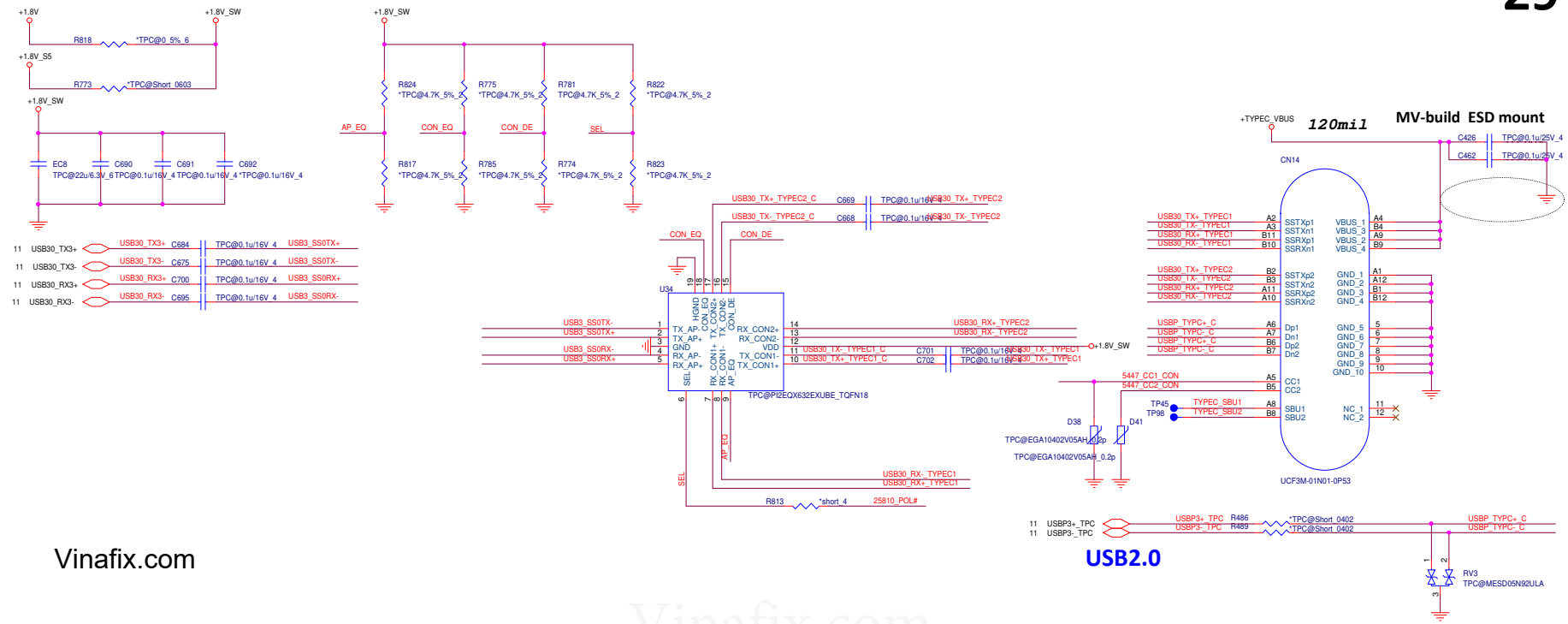
+3VPCU — Q2 AO3413 — +3V_LAN — +3V_S5
R5 100K_5%_4
C28 0.1u/16V
34 LANPWR#
R14 10K_5%_4
C37 1000p/50V_4
R7 2.2_1%_8
C23 10u/6.3V_6
C25 0.1u/16V_4
C24 *0.1u/16V_4
C29 *0.1u/16V_4

Quanta Computer Inc.
PROJECT : ZAUI

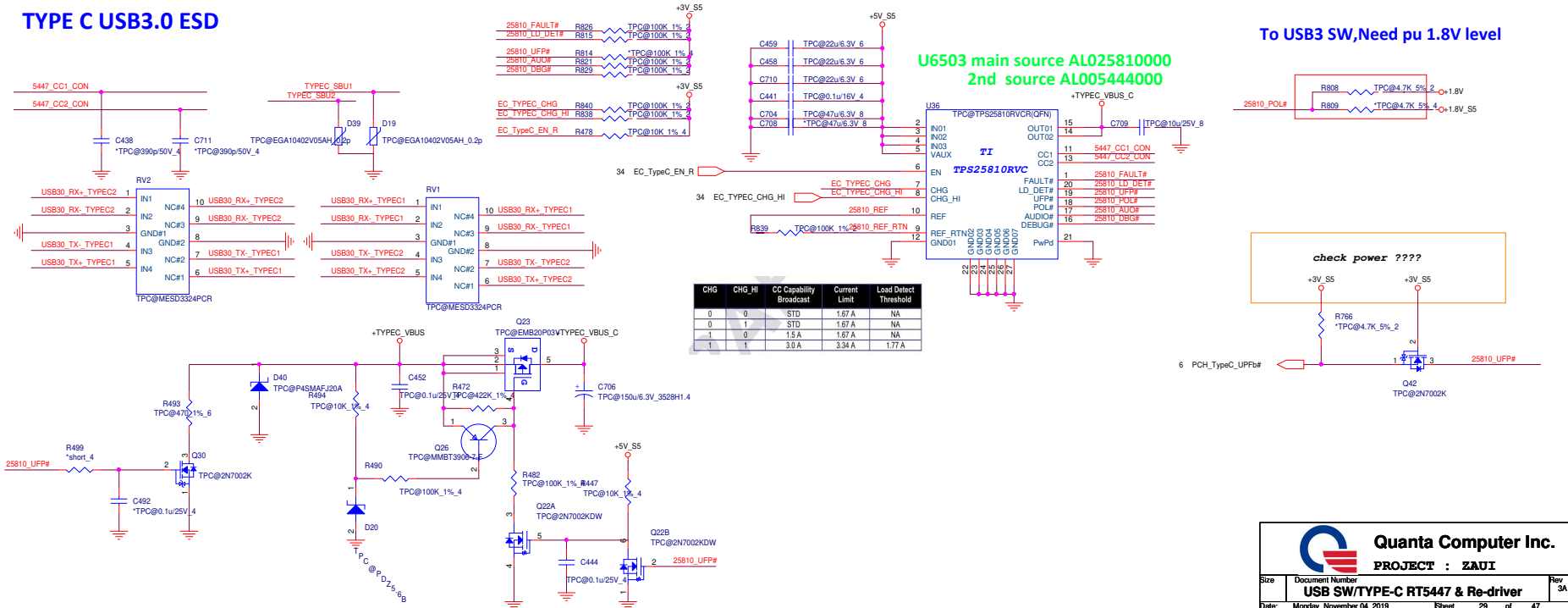
Size	Document Number	Rev
	LAN RTL8166EH/RTL8111HSH	3A

Date: Monday, November 04, 2019 Sheet 28 of 47

TYPE C and MUX PI2EQX632EXUBE



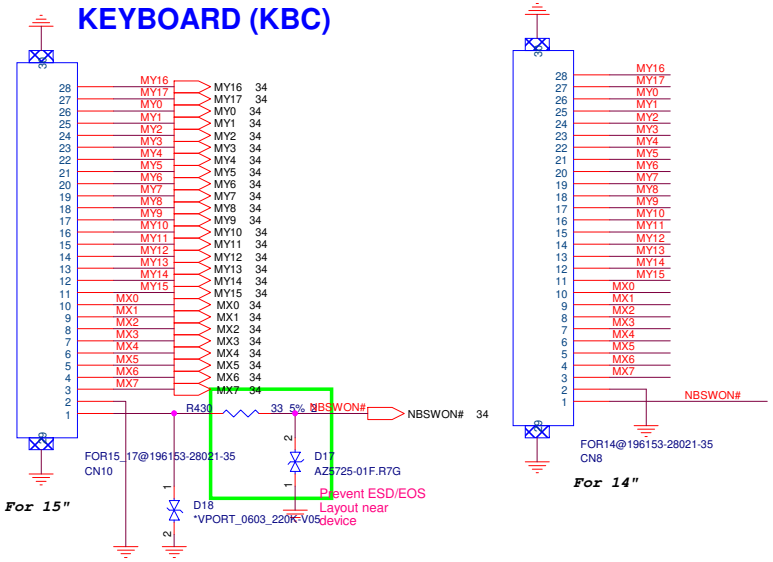
TYPE C USB3.0 ESD

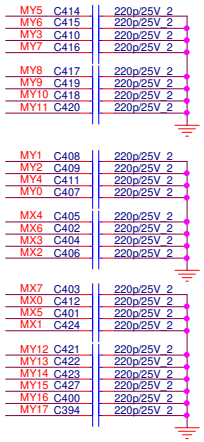


CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

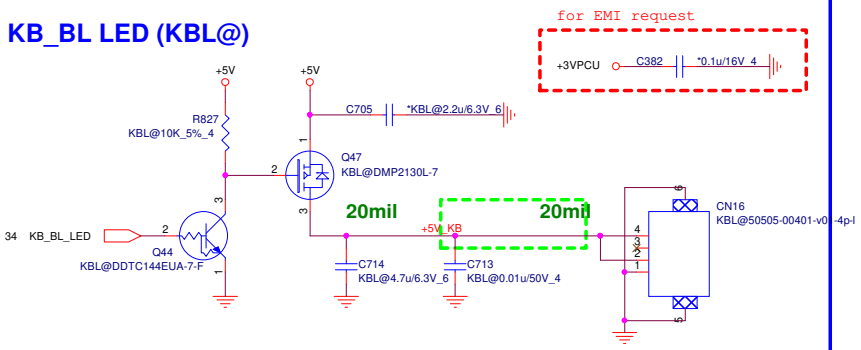
Quanta Computer Inc.
PROJECT : ZAUI
Size | Document Number: USB SW/TYPE-C RT5447 & Re-driver | Rev 3A
Date: Monday, November 04, 2019 | Sheet 29 of 47

KEYBOARD (KBC)

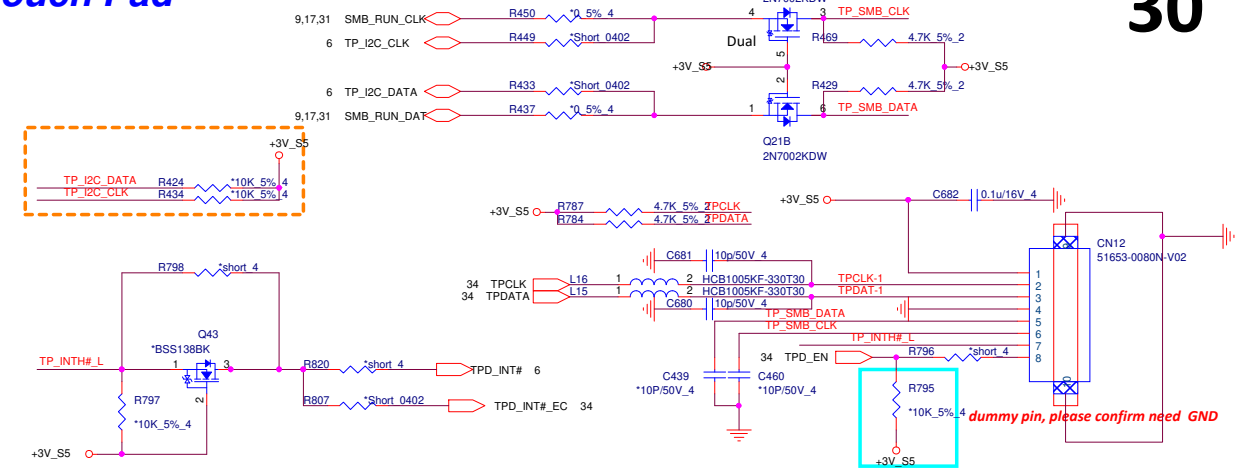




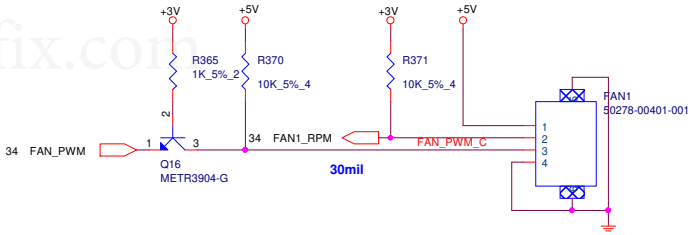
KB_BL LED (KBL@)



Touch Pad



FAN check pin define



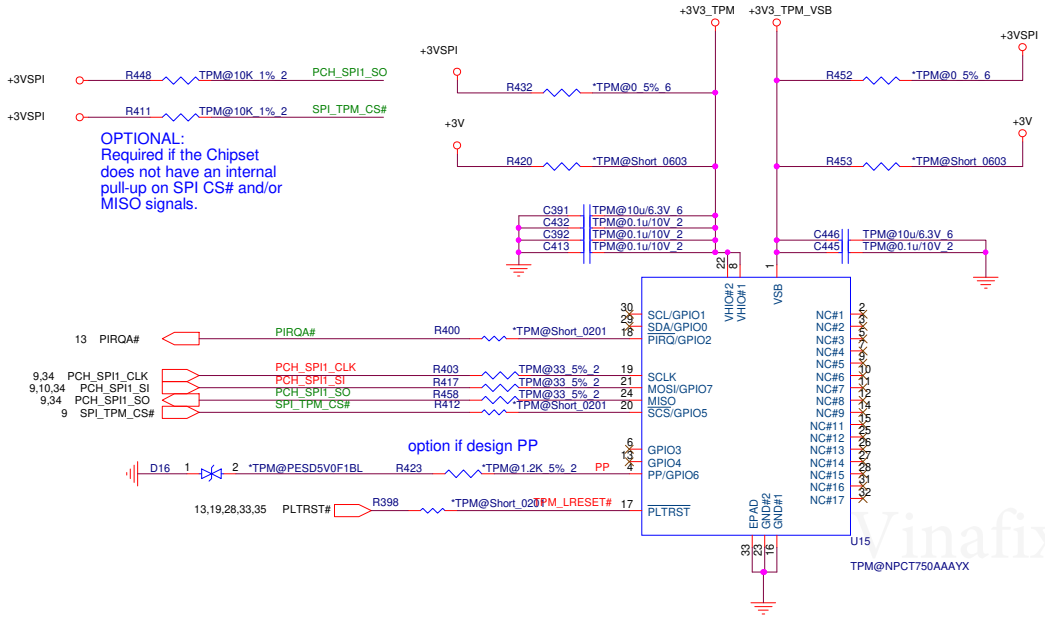
Quanta Computer Inc.

PROJECT : ZAUI

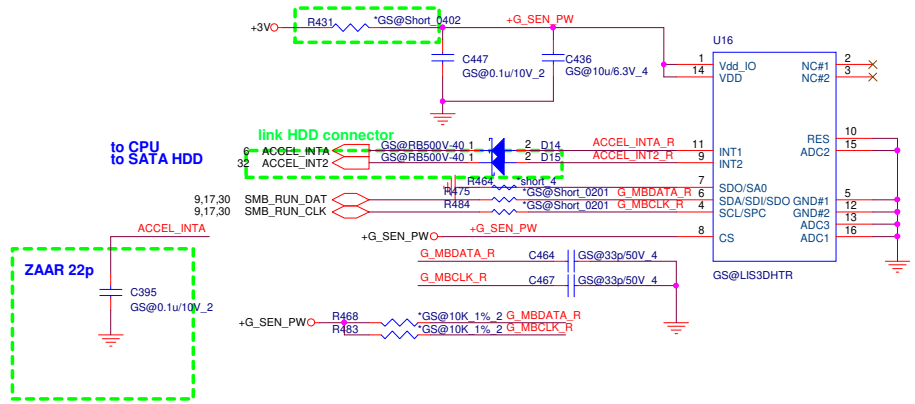
Size	Document Number	Rev
	KB/TP/FAN	3A

Date: Monday, November 04, 2019 Sheet 30 of 47

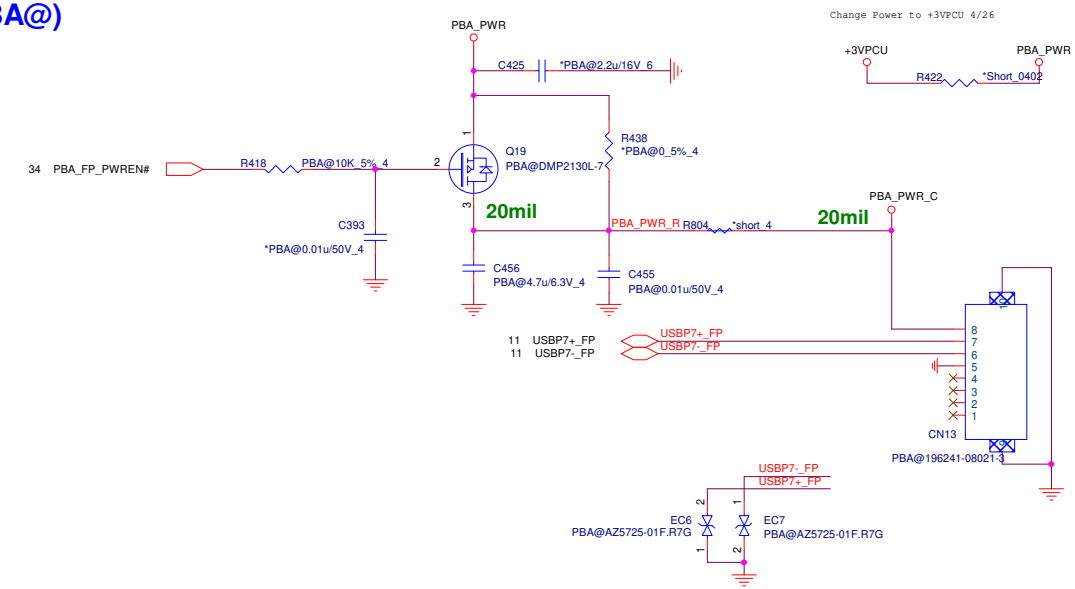
TPM NPCT750



G-sensor (GS@)



PBA (PBA@)



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PROJECT : ZAUI

Size	Document Number	Rev
	TPM/G-Sensor/PBA	3A

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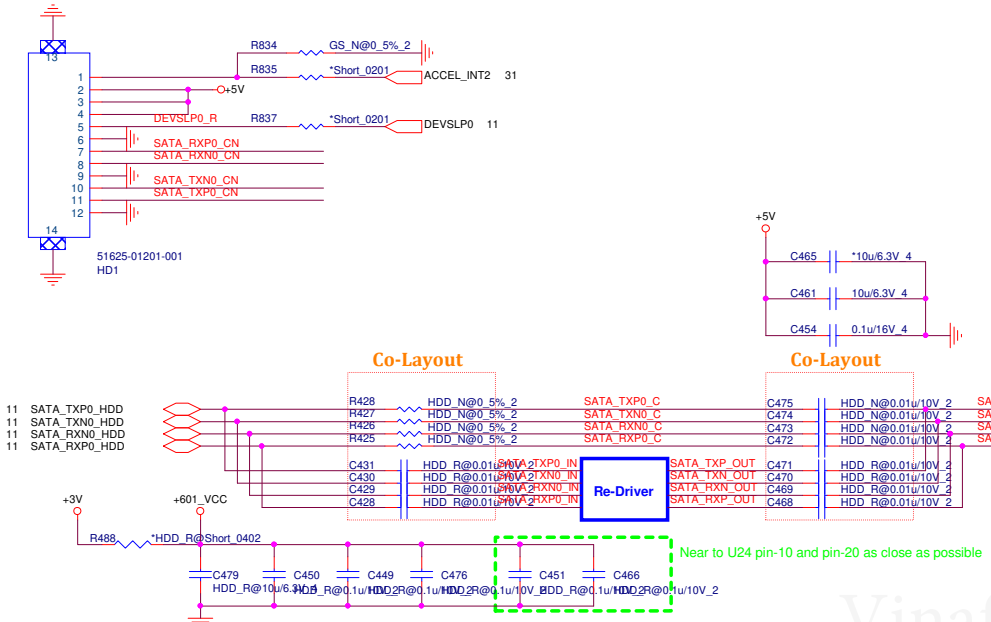
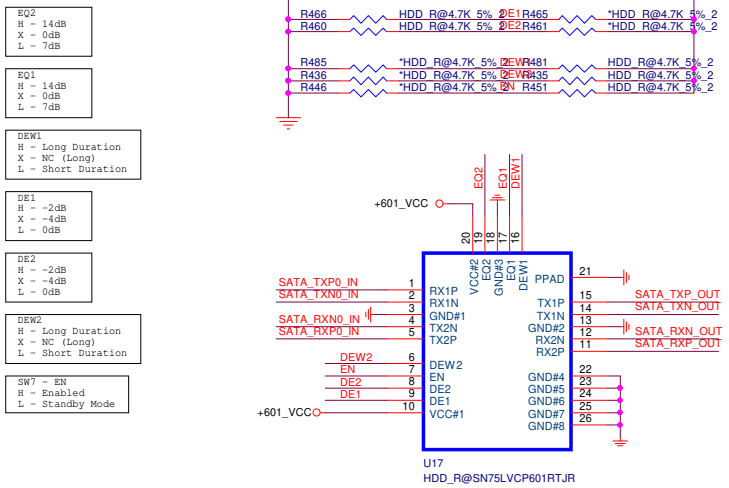
SATA HDD & LED

16,24,29,33,35,37,38,39,40,42,43,44 +5V_S5
25,26,27,30,35,37,41 +5V
2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,33,34,35,37,38,39,40,41,42,43,44 +3V
2,6,8,10,11,13,14,15,16,28,29,30,33,34,37,40,41 +3V_S5

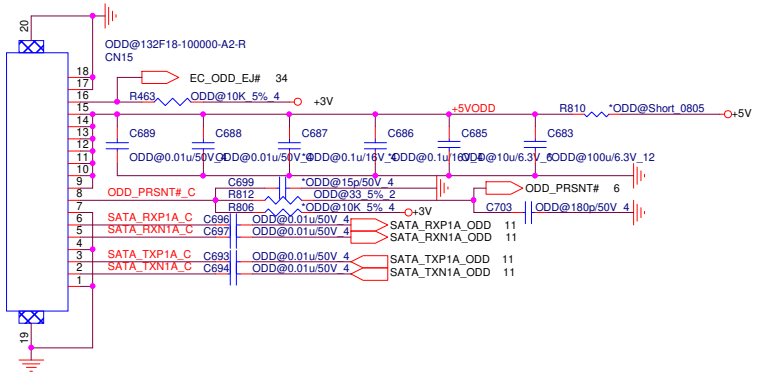
32



SATA HDD Re-driver



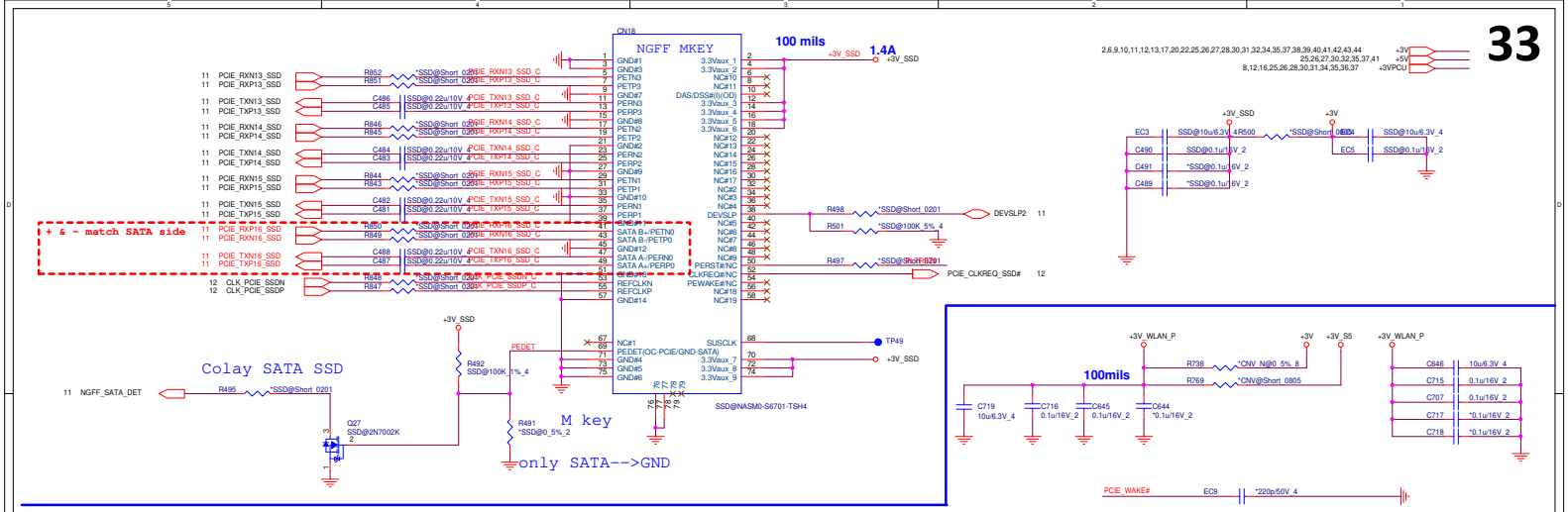
SATA ODD (ODD@)



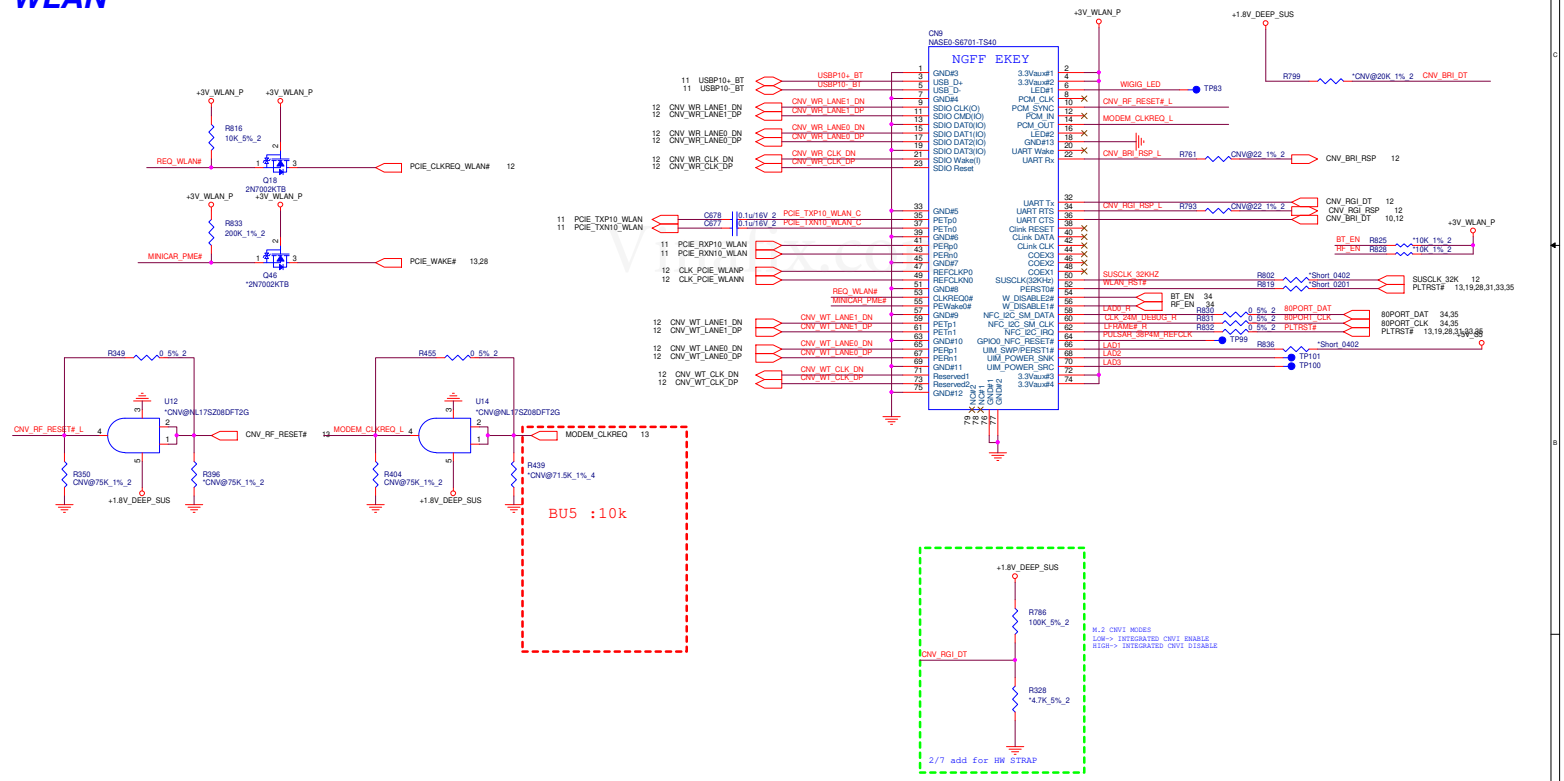
Quanta Computer Inc.

PROJECT : ZAUI

Size	Document Number	Rev
	HDD/ ODD	3A
Date: Monday, November 04, 2019	Sheet 32 of 47	

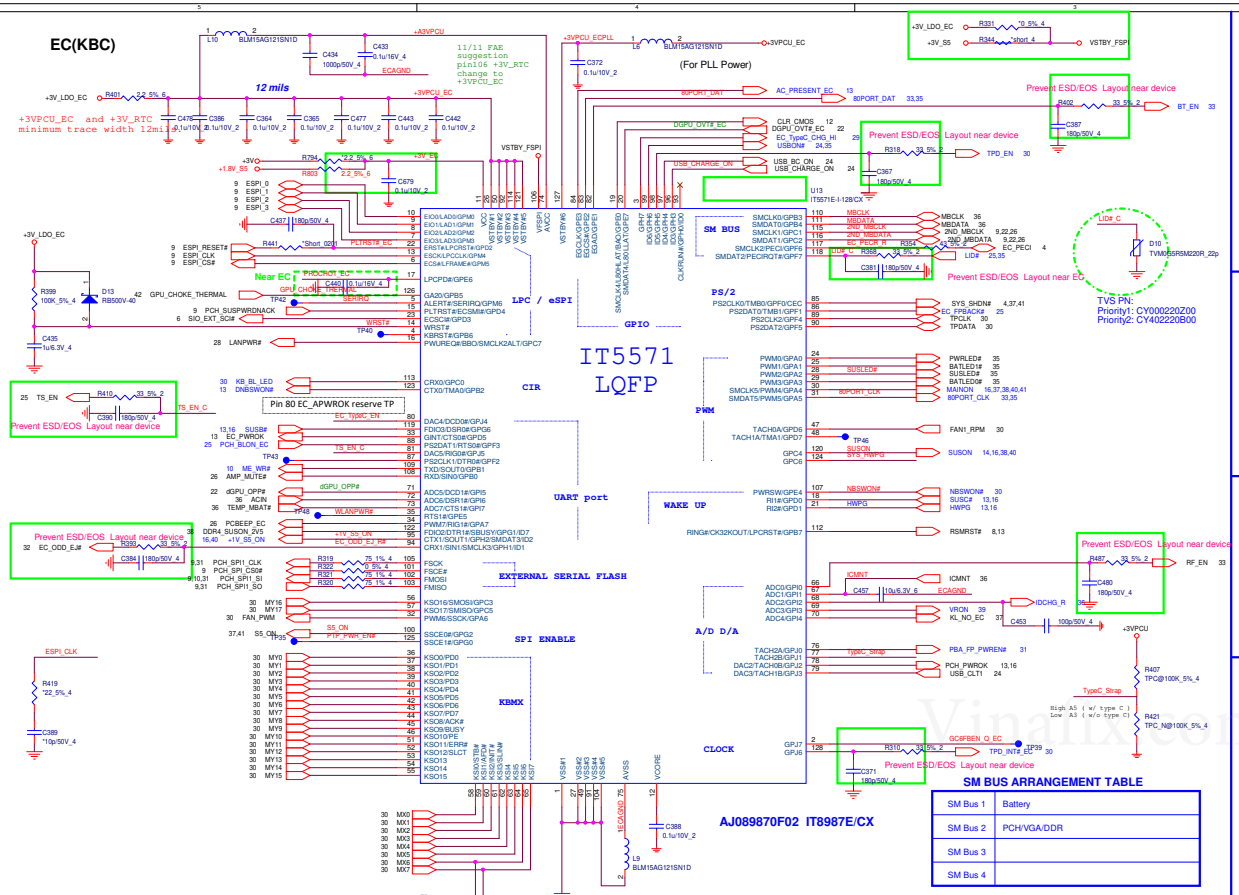


WLAN



Quanta Computer Inc.			
PROJECT : ZAUI			
Size	Document Number		Rev
	HDD/WLAN(NGFF)		3A
Date: Monday, November 04, 2019		Sheet 33 of 47	

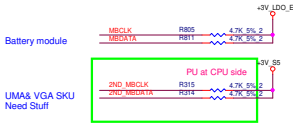
EC(KBC)



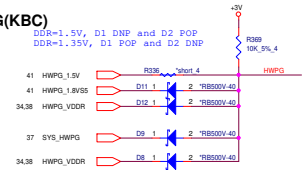
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA/DDR
SM Bus 3	
SM Bus 4	

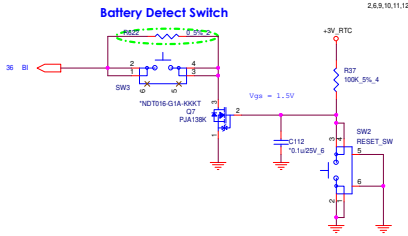
SM BUS PU(KBC)



HWPG(KBC)



Reset SW (FSW)



Quanta Computer Inc.			
PROJECT : ZAUI			
Size	Document Number		Rev
	KBC IT8987		3A
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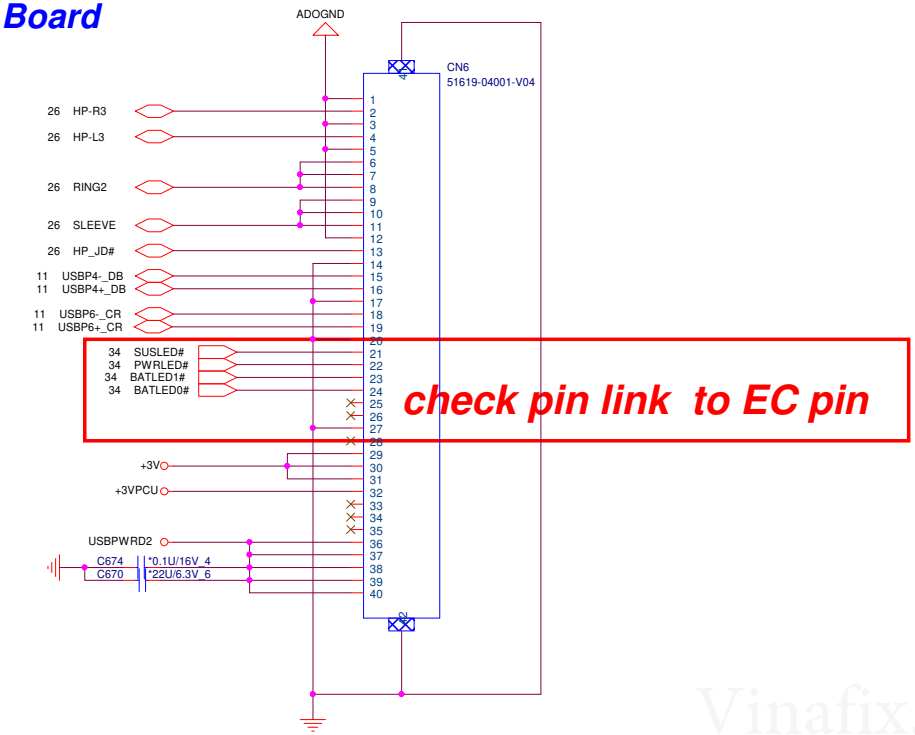
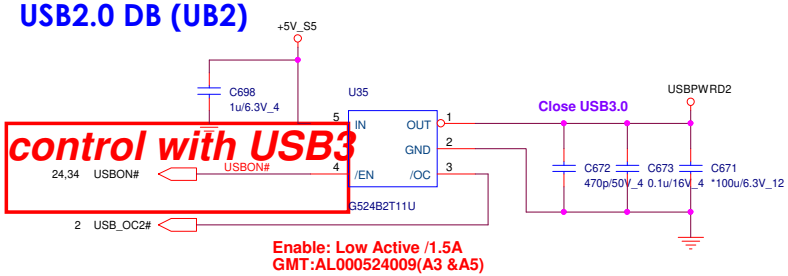
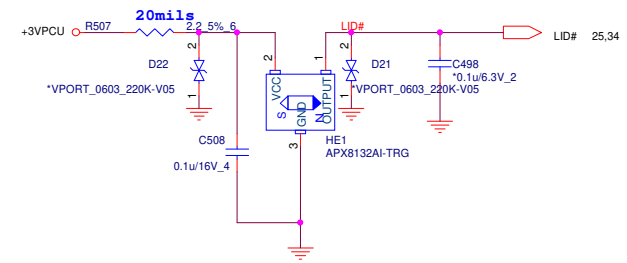
USB Board

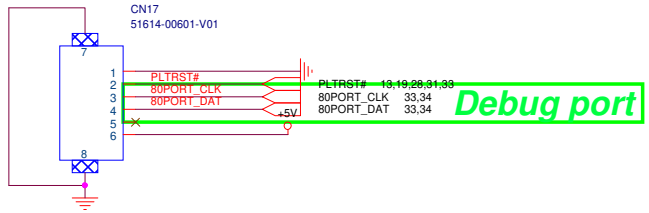


USB2.0 DB (UB2)

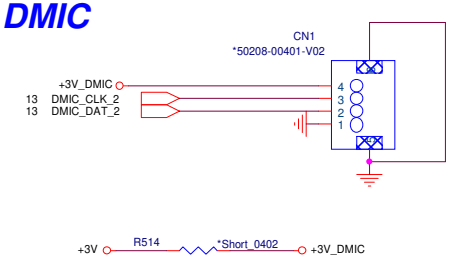


Hall Sensor





DMIC

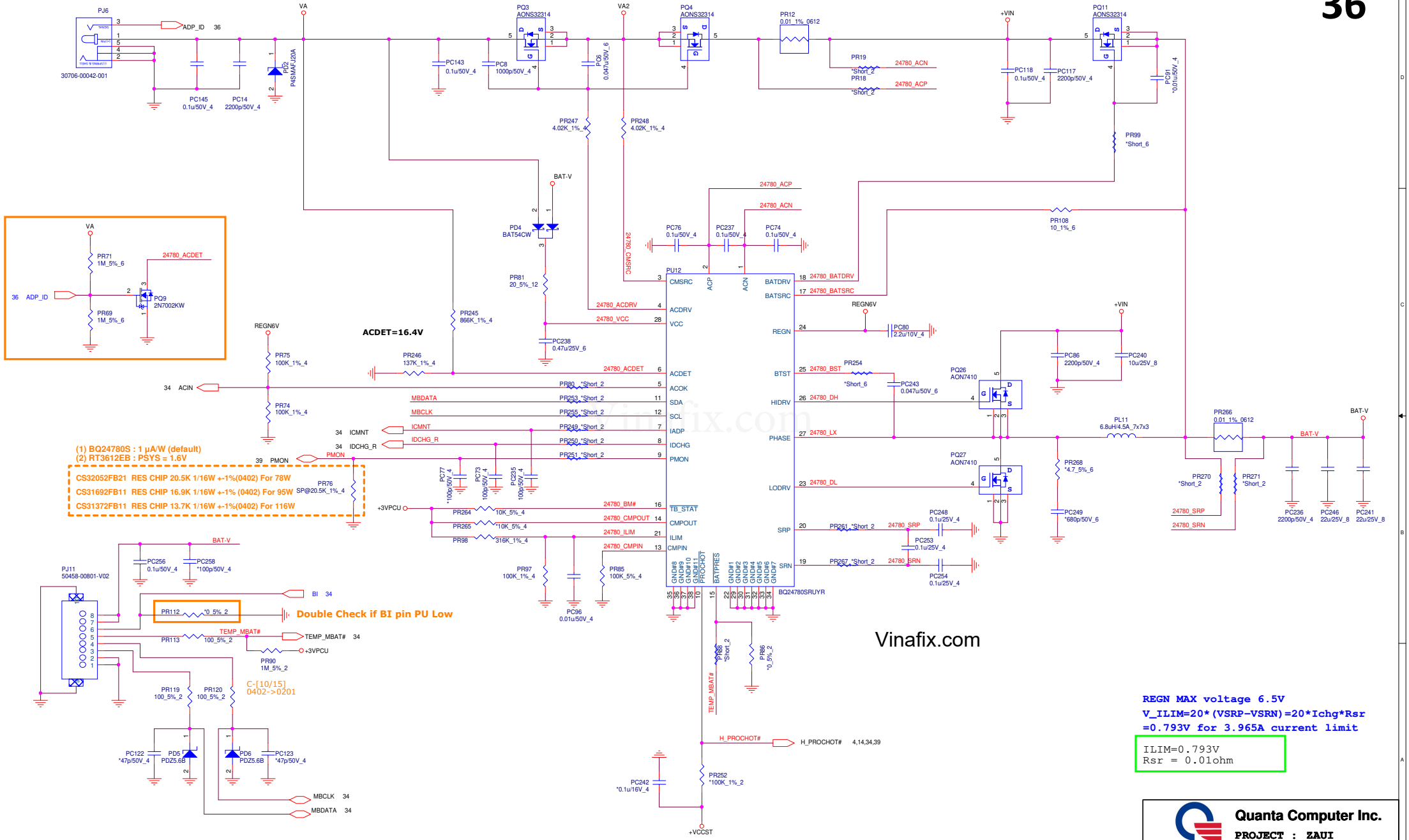


Quanta Computer Inc.

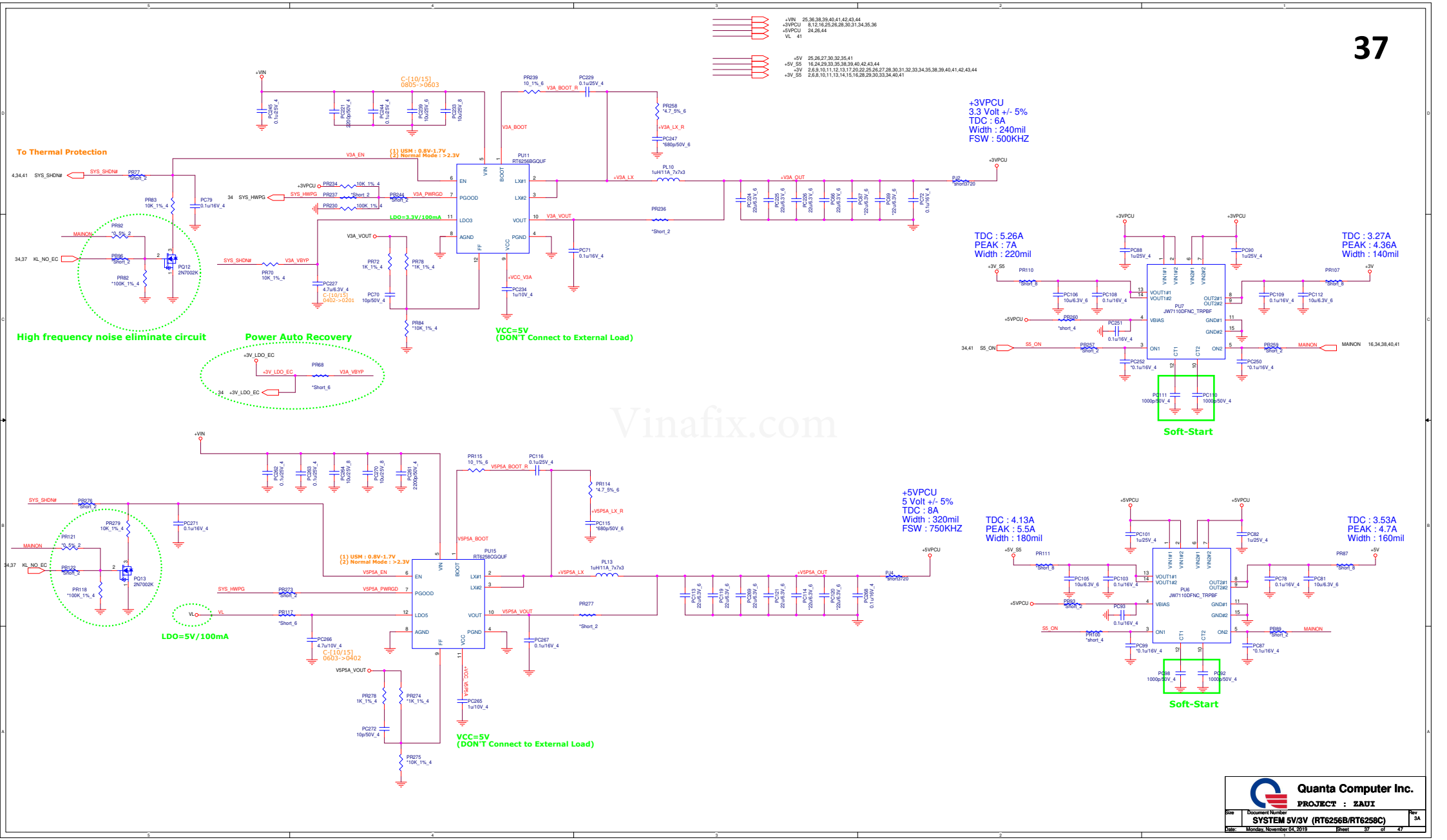
PROJECT : ZAUI

Size	Document Number	Rev
	USB DB/Hall sensor/DMIC	3A

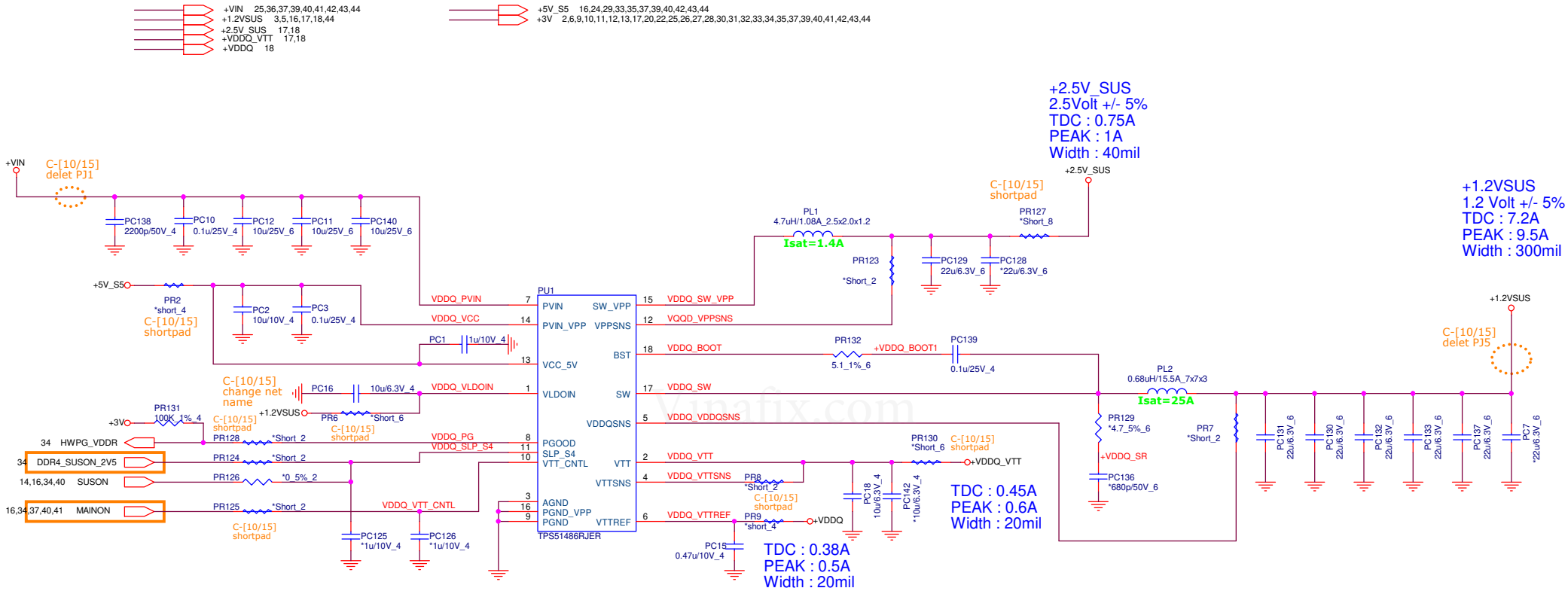
Date: Monday, November 04, 2019 Sheet 35 of 47



Quanta Computer Inc.			
PROJECT : ZAUI			
Size	Document Number		Rev
	Charger (BQ24780S)		3A
Date: Monday, November 04, 2019		Sheet 36 of 47	



Quanta Computer Inc.			
PROJECT : ZAUI			
Size	Document Number		Rev
	SYSTEM 5V/3V (RT6256B/RT6258C)		3A
Date: Monday, November 04, 2019	Sheet 37 of 47		



	VTT_CNTL	SLP_S4	+1.2VSUS	+2.5VSUS	REF	VTT
S0	1	1	ON	ON	ON	ON
S3	0	1	ON	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF	OFF

Quanta Computer Inc.

PROJECT : ZAUI

Size	Document Number	Rev
	DDR4_+1.2VSUS (TPS51486)	3A

Date: Monday, November 04, 2019 Sheet 38 of 47

+VIN 25,36,37,38,40,41,42,43,44
+VCCIN 5
+VCCST 4,5,13,16,36
+5V_S5 16,24,29,33,35,37,38,40,42,43,44
+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,40,41,42,43,44

RT3612EBGQW-03

PU4

VIN 22 RT3612_VIN
UGATE1 26 RT3612_UG1
BOOT1 25 RT3612_BOOT1
PHASE1 27 RT3612_PHASE1
LGATE1 28 RT3612_LG1
UGATE2 32 RT3612_UG2
BOOT2 1 RT3612_BOOT2
PHASE2 31 RT3612_PHASE2
LGATE2 30 RT3612_LG2
ISEN1P 20 RT3612_ISEN1P
ISEN1N 19 RT3612_ISEN1N
ISEN2P 17 RT3612_ISEN2P
ISEN2N 18 RT3612_ISEN2N
VSEN 14 RT3612_VSEN
COMP 15 RT3612_COMP
FB 16 RT3612_FB
RGND 13 RT3612_RGND
EPAD 33
VCC 10
PVCC 29
VREF06 12
TSEN 21 RT3612_TSEN
SET1 8 RT3612_SET1
SET2 7 RT3612_SET2
SET3 6 RT3612_SET3
VR_READY 24 RT3612_VR_READY
VRHOT 2 RT3612_VRHOT
VCLK 5 RT3612_VCLK
VDIO 4 RT3612_VDIO
ALERT 3 RT3612_ALERT#
VRON 23 RT3612_VRON
PSYS 9 RT3612_PSYS
IMON 11 RT3612_IMON

+VCCST
C-[10/15] shortpad
PR200 *short_4
PR205 100_1%_2
PR204 *75_1%_2
PR206 45.3_1%_2
PR203 *10K_1%_2
PC200 0.1u/6.3V_2
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
H_PROCHOT#

+5V_S5
PR207 6.2_5%_6
RT3612_VCC
PC61 4.7u/6.3V_4
PR186 2.2_5%_6
RT3612_PVCC
PC58 2.2u/10V_4

+VREF06_RT3612
PR208 52.3K_1%_2
PR201 9.31K_1%_2
PR199 22.1K_1%_2
PR178 10K_1%_2
SET1_1
SET2_1
SET3_1
TSEN_1
PR209 110_1%_2
PR202 182_1%_2
PR194 200_1%_2
PR181 348_1%_2
C-[10/15] 0402->0201
For temp level adjust
PR196 15K_1%_2
PR198 8.06K_1%_2
PR197 20K_1%_2
PR177 40.2K_1%_2
SET1_2
SET2_2
SET3_2
TSEN_2
PR189 348_1%_2
PR193 60.4_1%_2
PR192 301_1%_2
PR180 402_1%_2

+VREF06_RT3612
PR57 3.9_5%_4
VREF_RC
PC60 0.47u/6.3V_4
Close to Phase1 Mosfet
PR160 100K_NTC_4_1%
PINSET_TSEN
PR47 10_1%_2
PR52 110K_1%_2

PR55 10K_1%_2
+3V
C-[10/15] shortpad
4,13 IMVP_PWRGD — PR53 *Short_2 — RT3612_VR_READY
4,14,34,36 H_PROCHOT# — PR60 *Short_2 — RT3612_VRHOT
5 VR_SVID_CLK — PR63 *Short_2 — RT3612_VCLK
5 VR_SVID_DATA — PR62 *Short_2 — RT3612_VDIO
5 VR_SVID_ALERT# — PR61 *Short_2 — RT3612_ALERT#
34 VRON — PR46 *Short_2 — RT3612_VRON
PC192 *0.1u/6.3V_2

(1) RT3612EB : PSYS = 1.6V
(2) Double Check PMON Setting with charger

LL/IMON Compesation

36 PMON — PR195 *Short_2 — RT3612_PSYS
C-[10/15] 0402->0201
PR188 *10K_1%_2
PC199 *0.1u/6.3V_2

Close to Phase1 Inductor
+VREF06_RT3612
PR191 6.49K_1%_4
IMONCPU_1
PR161 100K_NTC_4_1%
NTC1N_R
PR58 15.8K_1%_4
RT3612_IMON
PR190 17.4K_1%_4

PR172 2.2_5%_6
PC191 0.22u/25V_4
C-[10/15] 0603->0402

PQ20 AOE6936
PR170 1_5%_6
PC55 0.1u/25V_4
Don't Connect Pin2 to Phase
PR173 *2.2_5%_6
SN_VCORE1
PC188 *2200p/25V_2

PQ21 AOE6936
PR187 1_5%_6
PC59 0.1u/25V_4
Don't Connect Pin2 to Phase
PR179 *2.2_5%_6
SN_VCORE2
PC194 *2200p/25V_2

PC197 10u/25V_8
PC189 10u/25V_8
PC177 10u/25V_8
PC181 *10u/25V_8
PC174 0.1u/25V_4
PC190 2200p/50V_4
PC173 0.1u/25V_4
C-[10/15] delet PJ9
+VIN
PC180 *15u/25V_3528H1.9

DCR=1.1m-ohm+/-7%
PL7 0.24uH/28A_7x7x3
Isat=35A
PR165 *Short_2
PR164 *Short_2
ISEN1P
ISEN1N
+VCCIN
PC52 22u/6.3V_6
PC162 *22u/6.3V_6
PC30 *22u/6.3V_6
PC203 *22u/6.3V_6
PC201 *22u/6.3V_6

PC196 10u/25V_8
PC204 10u/25V_8
PC207 10u/25V_8
PC202 *10u/25V_8
PC193 0.1u/25V_4
PC182 2200p/50V_4
PC205 0.1u/25V_4

DCR=1.1m-ohm+/-7%
PL8 0.24uH/28A_7x7x3
Isat=35A
PR183 *Short_2
PR182 *Short_2
PC54 22u/6.3V_6
PC166 *330u/2.5V_7343H1.9
PC164 *330u/2.5V_7343H1.9
PC163 330u/2.5V_7343H1.9
PC165 *330u/2.5V_7343H1.9

Recommand output cap:
a. 1pcs 330uF/2.5V_9m_cap
b. 13pcs 22uF/6.3V MLCC includ EE side
c. Reserve 4pcs 22uF/6.3V MLCC

PR174 2.43K_1%_4
PR171 3.32K_1%_4
ISEN1P_1
PR49 680_1%_2
PR48 3.83K_1%_4
PC51 0.1u/25V_4
PC186 0.1u/25V_4
C-[10/15] 0402->0201

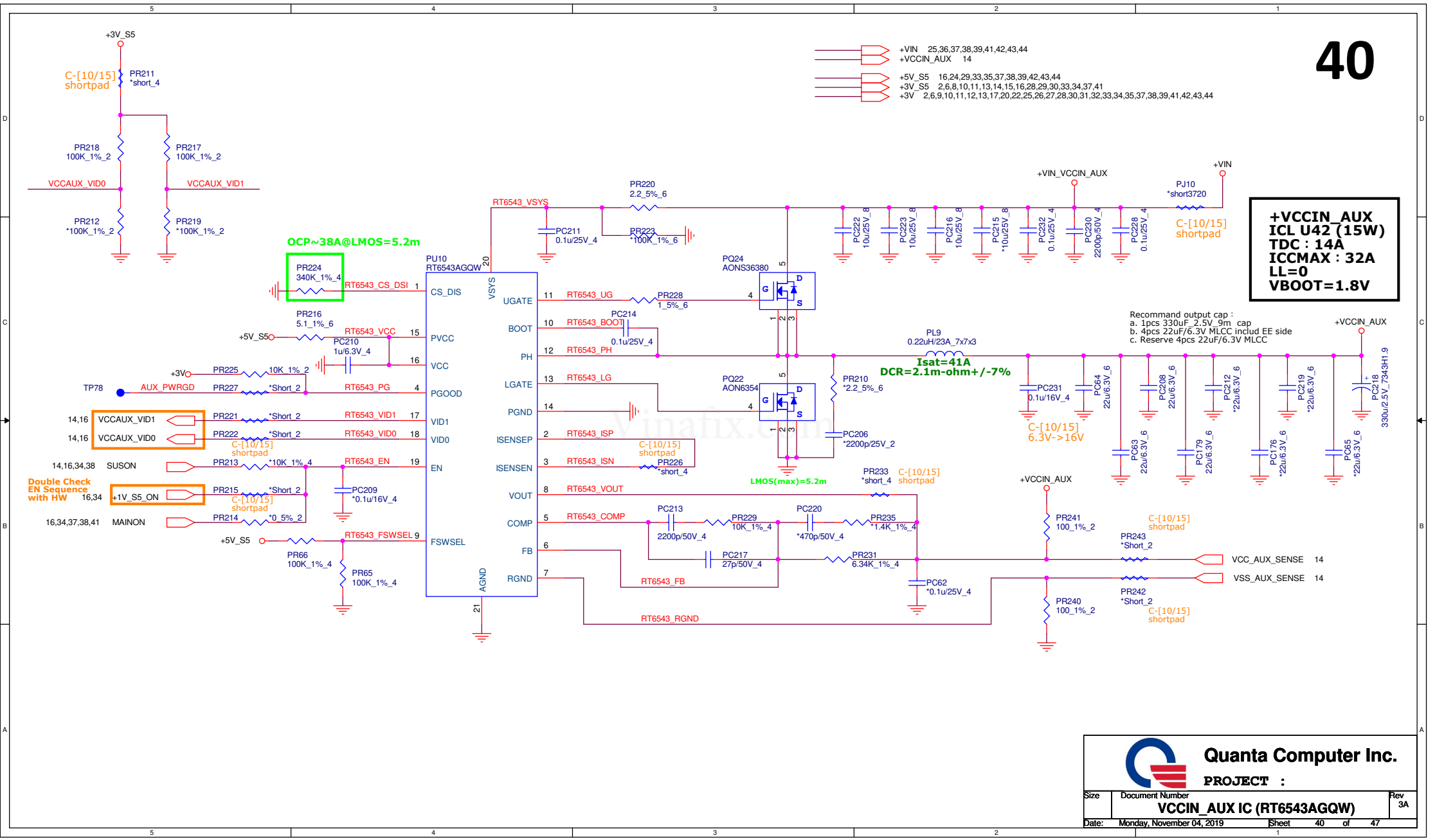
PR176 2.43K_1%_4
PR175 3.32K_1%_4
ISEN2P_1
PR50 680_1%_2
PR51 3.83K_1%_4
PC49 0.1u/25V_4
PC187 0.1u/25V_4
C-[10/15] 0402->0201

PC195 *100p/50V_4
PC56 82p/50V_4
PC53 330p/50V_4
PR56 21.5K_1%_4
PR54 10K_1%_4
PC57 *100p/50V_4
PC198 *100p/50V_4
C-[10/15] 0402->0201
PR159 100_1%_2
PR184 *Short_2
+VCCIN
PR185 *Short_2
PR162 100_1%_2
C-[10/15] 0402->0201
VCCSENSE 5
VSSSENSE 5

+VCC_CORE
ICE-L U42 Performance (15W)

TDC : 39A
ICCMAX : 70A
LL=2m
VBOOT= 1.8V

Quanta Computer Inc.
PROJECT :
Size | Document Number: CPU VR IC (RT3612EBGQW-03) | Rev 3A
Date: Monday, November 04, 2019 | Sheet 39 of 47


40
+VIN 25,36,37,38,39,41,42,43,44
+VCCIN_AUX 14
+5V_S5 16,24,29,33,35,37,38,39,42,43,44
+3V_S5 2,6,8,10,11,13,14,15,16,28,29,30,33,34,37,41
+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,41,42,43,44
+VCCIN_AUX ICL U42 (15W)
TDC : 14A
ICCMAX : 32A
LL=0
VBOOT=1.8V
OCP~38A@LMOS=5.2m
Isat=41A
DCR=2.1m-ohm+/-7%
LMOS(max)=5.2m
Recommand output cap :
a. 1pcs 330uF_2.5V_9m cap
b. 4pcs 22uF/6.3V MLCC includ EE side
c. Reserve 4pcs 22uF/6.3V MLCC
Double Check EN Sequence with HW
PU10 RT6543AGQW
CS_DIS
PVCC
VCC
PGOOD
VID1
VID0
EN
FSWSEL
VSYS
UGATE
BOOT
PH
LGATE
PGND
ISENSEP
ISENSEN
VOUT
COMP
FB
RGND
AGND
PQ24 AONS36380
PQ22 AON6354
PL9 0.22uH/23A_7x7x3
VCC_AUX_SENSE 14
VSS_AUX_SENSE 14
Quanta Computer Inc.
PROJECT :
VCCIN_AUX IC (RT6543AGQW)
Size
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Rev 3A
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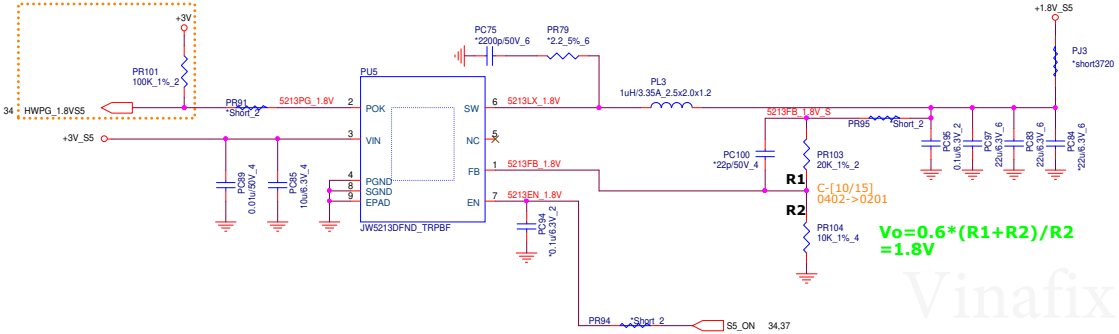
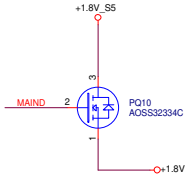
+3V_S5 2,6,8,10,11,13,14,15,16,28,29,30,33,34,37,40
+1.8V_S5 14,29,34,44
+1.8V 26,29
+1.5V 26
+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,42,43,44
VL 37

+VIN 25,36,37,38,39,40,42,43,44
+5V 25,26,27,30,32,35,37

+1.8V_S5
1.8Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 120mil

Double check PU high with HW

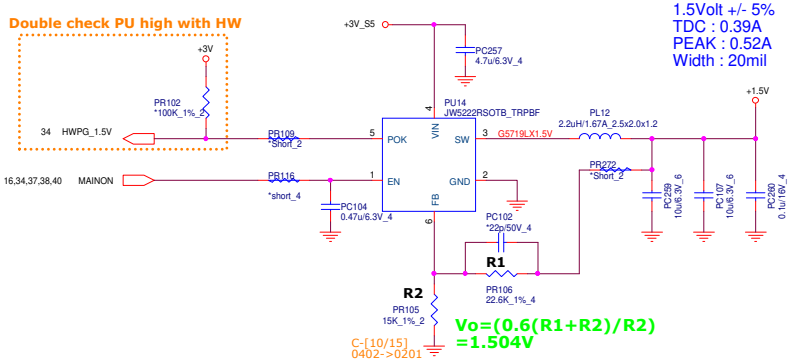




TDC : 0.3A
PEAK : 0.4A
Width : 20mil

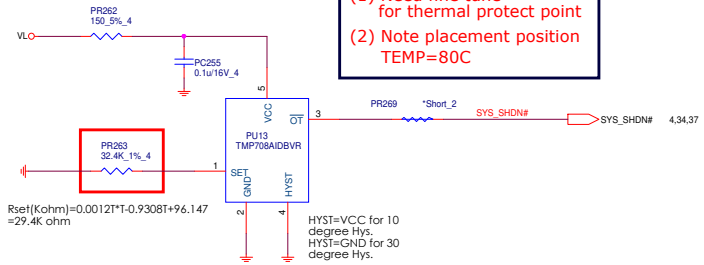
+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil

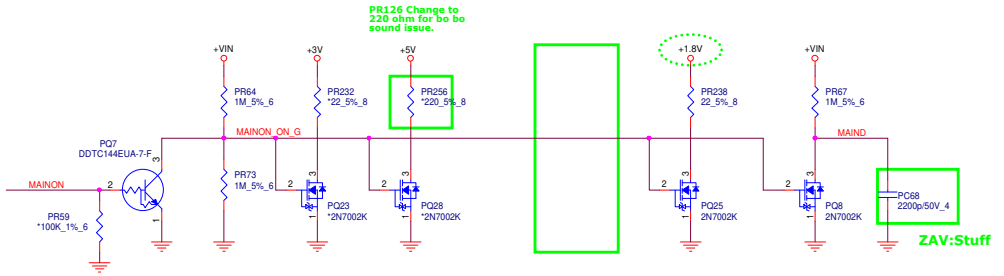
Double check PU high with HW



Thermal protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=80C





Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	+1.8V_S5/+1.5V/Thermal Protect	3A
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VGPU_CORE

+VIN 25,36,37,38,39,40,41,43,44
+VGPU_CORE 19
+5V_S5 16,24,29,33,35,37,38,39,40,43,44
+1V8_AON 19,21,22,44
+1V8_GFX_MAIN 19,20,21,44
GPU_CHOKE_THERMAL 34,42

PU2 EV@RT8813DGQW

Fsw: 300KHz

VREF=2V

Don't Connect Pin2 to Phase

Rds(on)=3mohm(MAX)

Isat=40A
DCR(MAX)=2.8mohm

OCP=85A

routing in parallel

RT8813DGQW	
PSI	Mode
0V ~ 0.4V	1 Phase DCM
0.8V ~ 1V	1 Phase CCM
1.4V-5.5V	2 /3Phase CCM

NV17 Config : Type2+	
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	0.309K
C	4.7nF

N17S-G3

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:28.6A
EDP-P:60.3A
OCP:85A
FSW:300KHz

N17S-G2-A1(25W/GDDR5)=MX250

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:28.6A
EDP-P:60.3A
OCP:85A
FSW:300KHz

N17S-G5

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:35A
EDP-P:69.6A
OCP:85A
FSW:300KHz

N17S-G0-A1(25W/GDDR5)=MX230

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:27.8A
EDP-P:42A
OCP:85A
FSW:300KHz

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	+NVVDD (RT8813DGQW)	3A
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+VIN 25,36,37,38,39,40,41,42,44
+1.35V_GFX 20,23
+5V_S5 16,24,29,33,35,37,38,39,40,42,44
+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,41,42,44

1.35V_GFX

N17S-G0-A1 (25W/GDDR5) =MX230 N17S-G2-A1 (25W/GDDR5) =MX250 N17S-G3	N17S-G5
EDP-C:5.8A EDP-P:7.4A	EDP-C:7.1A EDP-P:7.6A

43

Fsw=550KHz

PR168 EV@100K_1%_4
PC185 *EV@0.01u/50V_4
+VIN
C-[10/15] 0805->0603
PC184 EV@10u/25V_6
PC47 *EV@0.1u/25V_4
PC48 EV@2200p/50V_4
G5335-TON-2
PU9
NC
TON
V+#1
V+#2
V+#3
V+#4
+5V_S5
PR155 EV@10_5%_6
G5335-VCC-2
VCC
PC170 EV@10u/6.3V_6
Double check PU high with HW
+3V
PR158 EV@100K_1%_2
22 HWPG_1.35VGFX
PR157 *Short_2
G5335-PWRGD-2
PGOOD
+5V_S5
PR43 *EV@0_5%_2
G5335-PFM-2
PFM
G5335-AGND-2
PR44 *Short_2
Pulse-Skipping Mode
G5335-EN-2
EN
PR154 EV@2.2_5%_6
PC171 EV@0.1u/25V_4
BST
G5335-BST-2
LX#1
LX#2
LX#3
LX#4
LX#5
LX#6
G5335-LX-2
PL6 EV@0.68uH/15.5A_7x7x3
Isat=25A
DCR(typ)=5mohm
PR156 *EV@4.7_5%_6
PC172 *EV@680p/50V_6
PGND#1
PGND#2
PGND#3
PGND#4
PGND#5
AGND
G5335-AGND-2
+1.35V_GFX
PJ8 *short3720
PR41 *Short_2
PC183 *EV@1000p/50V_4
PR167 EV@6.49K_1%_4
R1
R2
PR169 EV@9.31K_1%_2
C-[10/15] 0402->0201
G5335-AGND-2
PC169 EV@22u/6.3V_6
PC44 EV@22u/6.3V_6
PC42 *EV@22u/6.3V_6
PC43 EV@0.1u/16V_4
PC168 EV@22u/6.3V_6
PC45 EV@22u/6.3V_6
PC46 EV@22u/6.3V_6
PC167 *EV@22u/6.3V_6
Vo=0.8*(R1+R2)/R2
=1.357V
VFB=0.8V
20 FBVDDQ_EN
PR163 EV@2.2K_5%_2
C-[10/15] 0402->0201
44 1.03_GFX_PGD
PR166 *EV@0_5%_4
G5335-SS-2
SS
FB
G5335-FB-2
PC178 EV@0.22u/10V_4
PC175 EV@0.01u/6.3V_2
G5335-AGND-2
G5335-AGND-2
PR45 *Short_4
G5335-AGND-2
EV@G5335QT2U

+1.35V_GFX
+5V_S5
PR39 EV@22_5%_6
PR40 EV@100K_1%_4
PQ5 EV@2N7002K
C-[10/15] 0402->0201
PR42 EV@1M_5%_2
G5335-EN-2
PQ6 EV@DMG1012T-7

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	+FBVDDQ_MEM (G5335QT2U)	3A
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+3V 2,6,9,10,11,12,13,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,41,42,43
+1.8V_S5 14,29,34,41
+1V8_GFX_MAIN 19,20,21,42
+1V8_AON 19,21,22,42
+5VPCU 24,26,37
+VIN 25,36,37,38,39,40,41,42,43
+1.2VSUS 3,5,16,17,18,38
+1.03_GFX 19
+5V_S5 16,24,29,33,35,37,38,39,40,42,43

N17S-G0
N17S-G2

+1.8V_MAIN
TDC : 0.9A
PEAK : 1.2A
Width : 40mil

+1.8V_S5
PC38 EV@1u/25V_4
PC37 EV@1u/25V_4
+1V8_GFX_MAIN
PR34 *Short_8
PC31 EV@10u/6.3V_6
PC32 EV@0.1u/16V_4
+5VPCU
PR37
PC40 *Short_0402 EV@0.1u/16V_4
22,42 1V8_MAIN_EN
PR36 *Short_0402
PC39 *EV@820p/50V_4
PU3
VIN1#1 VIN1#2 VIN2#1 VIN2#2
VOUT1#1 VOUT1#2
VBIAS
ON1
CT1 CT2
EV@JW7110DFNC_TRPBF
OUT2#1 OUT2#2
GND#1 GND#2
ON2
PC33 EV@1000p/50V_4
PC34 EV@1000p/50V_4
PC41 EV@0.1u/16V_4
PR38 *Short_0402
DGPU_PWR_EN 6,20
1V8_AON_S
PR35 *Short_8
PC36 EV@0.1u/16V_4
PC35 EV@10u/6.3V_6
+1V8_AON

N17S-G0
N17S-G2

+1.8V_AON
TDC : 0.75A
PEAK : 1A
Width : 40mil

+VIN
+1V8_GFX_MAIN
PR1 EV@1M_5%_6
PR5 EV@22_5%_8
PQ1 EV@LTC044EUBFS8TL
1V8_MAIN_EN
+1V8_MAIN_EN_G
PR4 *EV@100K_1%_6
PR3 EV@1M_5%_6
PQ2 EV@2N7002KW

+1.2VSUS
PQ19 EV@AON7408
PC159 EV@0.1u/16V_4
PC160 EV@10u/6.3V_6
PC157 EV@10u/6.3V_6
PC155 EV@10u/6.3V_6
PC156 EV@0.1u/16V_4
9336DRV

N17S-G0
N17S-G2

+1V
TDC : 0.9A
PEAK : 1.1A
Width : 40mil

+1.03_GFX
PJ7 *short3720
PR141 EV@5.6_5%_8
PQ17 EV@2N7002K
+5V_S5
PR145 EV@100K_1%_2 C-[10/15] 0402->0201
PR146 EV@1M_5%_2 C-[10/15] 0402->0201
PQ18 EV@DMG1012T-7

Double check PU high with HW

+1V8_AON
PR148 EV@10K_1%_2
43 1.03_GFX_PGD
PR147 *Short_0201
PU8 EV@G9336ADJTP1U
PGD EN VCC GND DRV ADJ
20,42 GPU_PWR_GD
PR153 *Short_0402
PC158 *EV@0.1u/16V_4
+5VPCU
PC151 EV@0.1u/16V_4
PR152 EV@47_1%_4
PC161 EV@0.01u/50V_4
PR149 EV@133_1%_4
9336ADJ
R1
R2
PR150 EV@124_1%_4
+1.03_GFX
N17S : Vo=(1+R1/R2)*0.5=1.03V

+3V
PR151 EV@10K_1%_4
PD7 EV@1SS355
PQ15 EV@2N7002K

	R1	R2
N17S	133 ohm	124 ohm

Quanta Computer Inc.
PROJECT : ZAUI

Size	Document Number	Rev
	+1.8V_AON/+1V_GFX (AOZ1331DI)	3A

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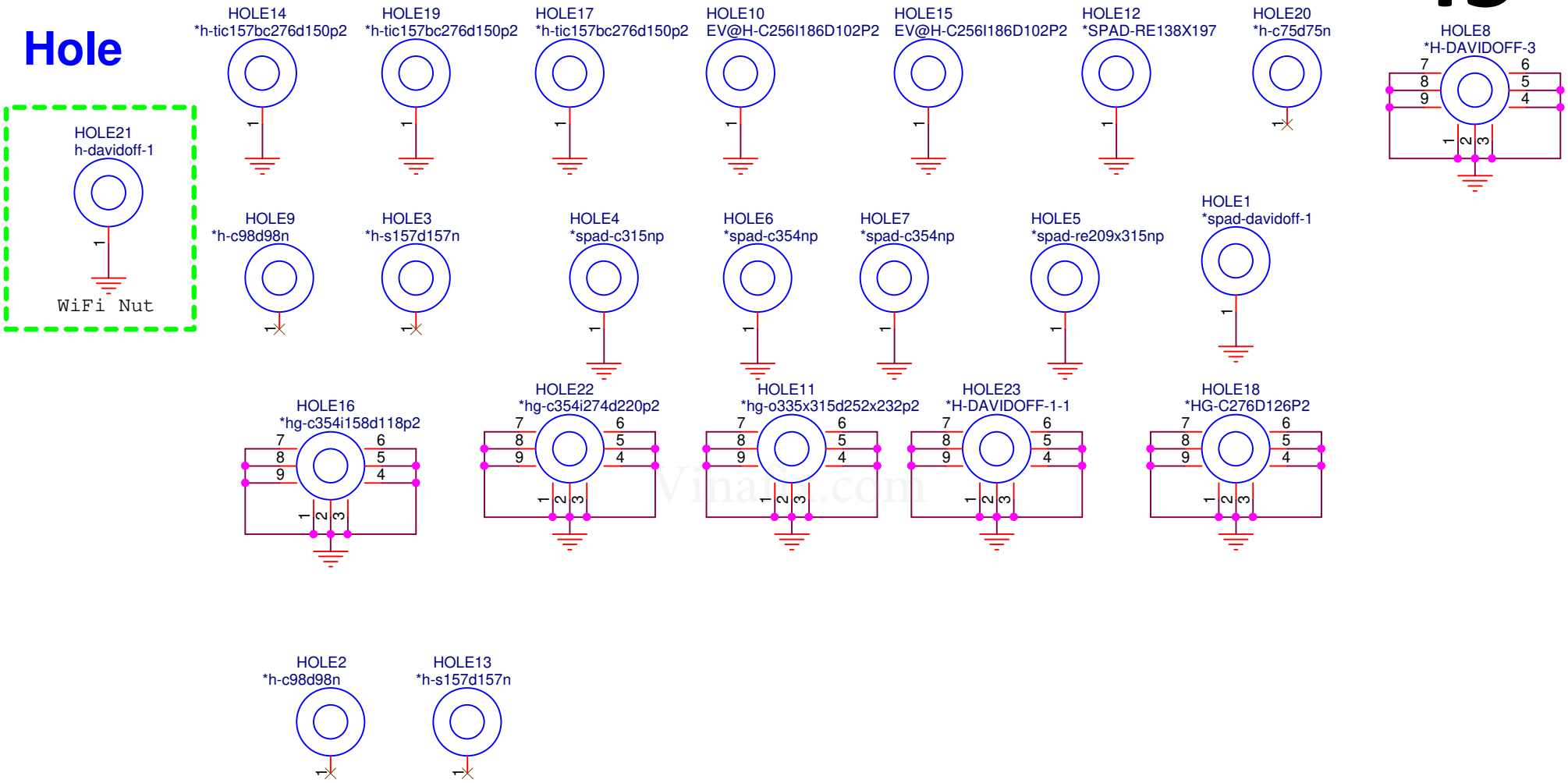
Hole



Quanta Computer Inc.		
PROJECT : ZAUI		
Size	Document Number: Hole	Rev: 3A
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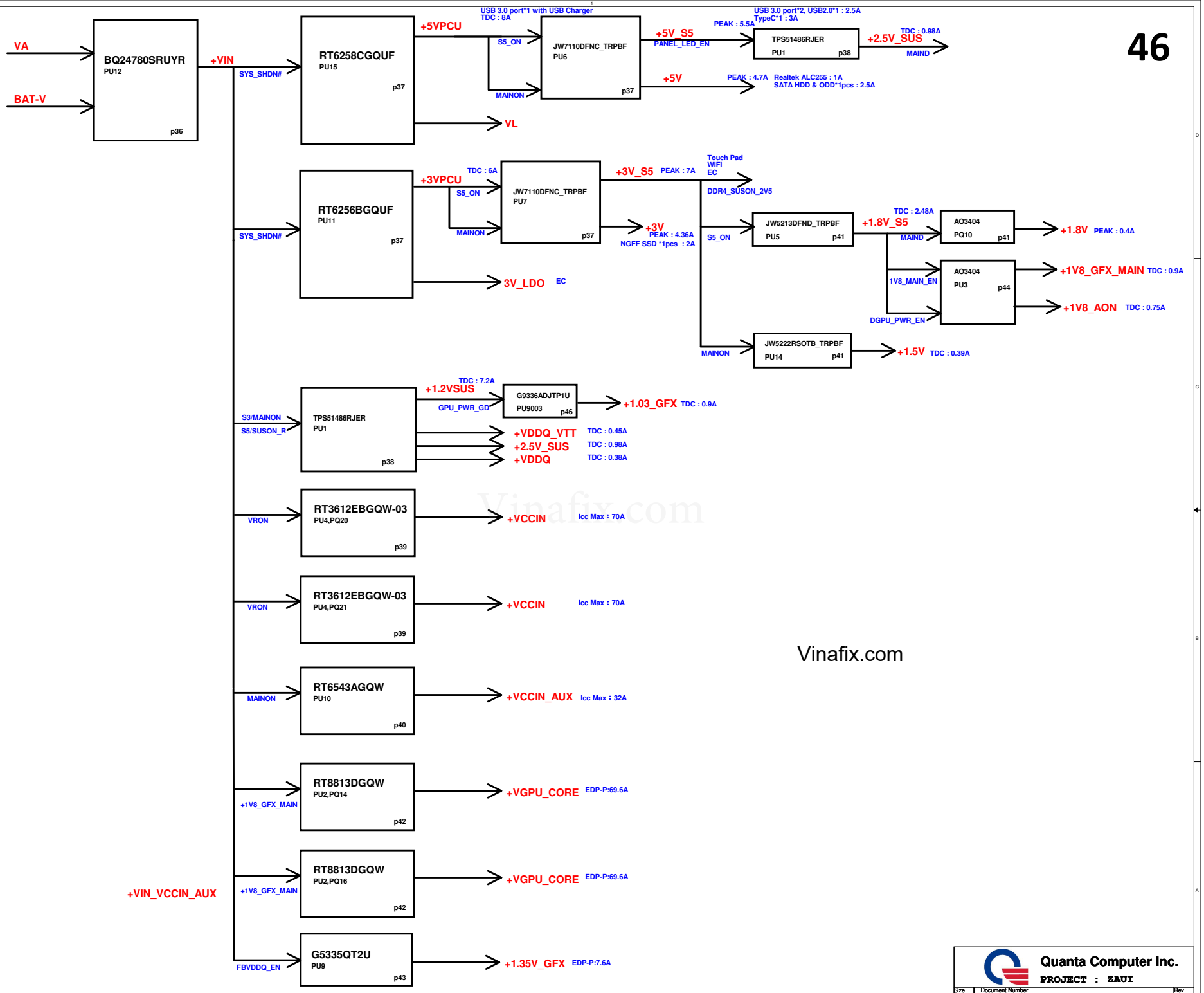

Quanta Computer Inc.

PROJECT : ZAUI

Size	Document Number	Rev
	Power Tree	3A

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Stage	Date	CHANGE LIST
A	10/31	1. change HDD redriver net name page 32 2.DEVSLP2 unstuff R551 page 12 3.Change Q9 (PCIE_CLKREQ_VGA#) design follow ZAAR page 19
	11/01	1. change VGA VMA_CLK1# VMA_CLK0# VMA_CLK0 VMA_CLK1 80.6 ohm page 23
	11/05	1.DGPU_PROCHOT_EC# PU 10K follow ZAAR page 22 2. PR9026 and PR9031 LAYOUT should be place at power side page 44
	11/12	1.remove FAN2_RPM no used page 34 2.remove RP1 and RP2 no used page 30
	11/13	1.Add C6618 , C6621, C6620, C6619,C6622,C6623 page 30
	11/19	1.Add R735 and R25371 for codec R255 page 26
	11/22	2.R294 unstuff for DDR 2. Add HOLE20 and HOLE21 page 47 for ME 3. PR9267 stuff for POWER
C	12/18	1. stuff R558 R560 , unstuff R557 R561 for touch pad 2.R68 short pad and C3 unstuff and SW1 unstuff for cost down
	12/28	1.Mount PR9085 by 0 ohm and Del PR9012 for POWER 2. Add Board_ID6 for BIOS
	1/04	1.Unstuff R220 R221 R222 C248 for cost down
	1/07	1.PU EC_TYPEC_EN_R 10K for TYPE-C SPEC 2.remove UFP# PU +3VPCU for TYPE-C SPEC
MP	01/17	1. Add net name CNV_RGI_DT_R and CNV_BRI_DT_R for layout constrain
	01/21	1.25810_POL# change to PU 1.8V and remove 25810_POL# PU 3V_S5 for type-c SPEC
	02/01	1. Add R25513 , R25514 for A3 and A5 TPC for bom option
	02/19	1.change R25517 and R25518 to 0201 for layout 2. Unstuff CN38 and CN24 no used for cost down
	02/21	1.R215 unstuff for leakage current 2.Add R25519 (2.2_5%_6) for Leason Learn
	02/25	1.change R25500 Value toTPC@ , change R25499 Value to TPC_N@ for BOM option
	02/26	1.R951 change to 45.3K.follow ZAU 2.HDMI EMI Res unstuff.for for cost down 3.R212 unstuff , R213stuff for leakage issue 4.R98 unstuff for leakage issue 5.R77,R78,R80 short pad for cost 6. Reserve R25520 SERIRQ +3V_S5 Pull high 10K for Leakage issue 7.change R25485 value to GS_N@ for BOM option 8.R378 unstuff EC push pull this pin for leakage issue
	03/05	1.Add C20001 C20002 , R25521 , R25522 , D13091 , D13092 for lesson learn 2.R663 R662 unstuff intel SPEC no require 3.Update it unstuff D33 , stuff D34 for keyboard ESD 4.unstuff R25436 because Bios internal PU so for cost down 5. unstuff R378 & R212 & R94 & R98 & R134 for leakage current
	03/06	1. change R507 to 11.3k for HDMI redriver 2. stuff R748/R749 and un-stuff R746/R74 for HDMI equalizer setting
	03/12	1.change PR3021 to 32.4K for thermal temp 2.Unstuff PR6416 because already PU at EC side 3.Remove D61 , short R25523 for cost down 4.change R507 10.5K for HDMI setting
	06/13	1.change R25321 from short pad to 0 ohm
	06/26	1.Update on board RAM table add samsung 8GB