COMPAL CONFIDENTIAL

MODEL NAME : CAZ10

PCB NO : LA-E122P

BOM P/N : 431A4D31L0X

Steamboat 12"/13" NonAR

Kabylake U

2016-11-09

REV : 1.0 (A00)

@ : Nopop Component

EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CXDP@ : XDP Component
CONN@ : Connector Component
ESPI@ : ESPI interface Component
LPC@ : External ESPI Component (SHD)

MB PCB

Part Number	Description
DA800187010	PCB 1S5 LA-E122P REV0 MB NON-AR 1

Layout Dell logo

REV:A00
PWB:

Power CKT : 1107

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Title: Cover Sheet

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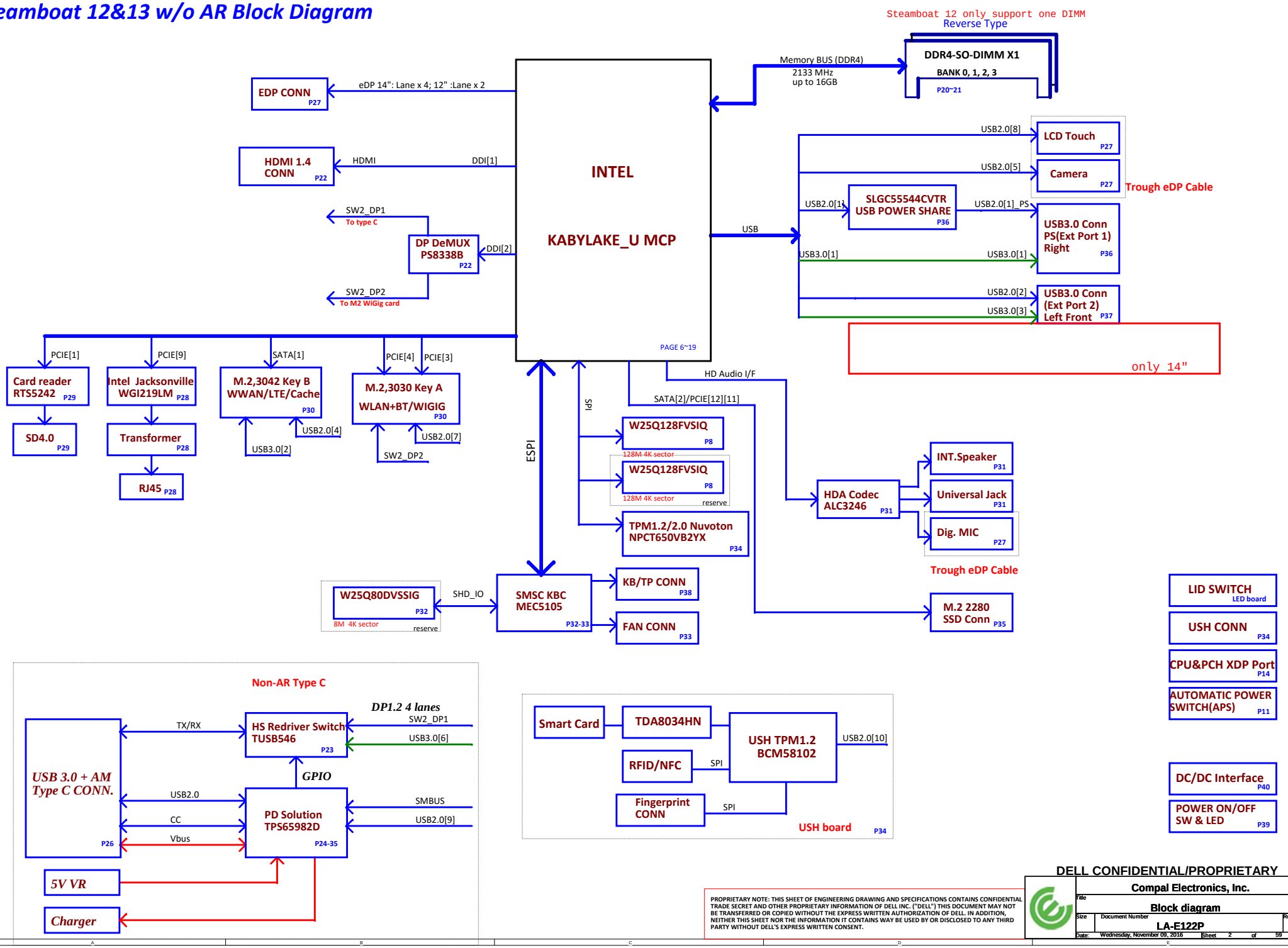
Steamboat 12&13 w/o AR Block Diagram



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Title	Block diagram
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NonAR config

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.0mm +-10%)			39.4		41.40000
					1.05156

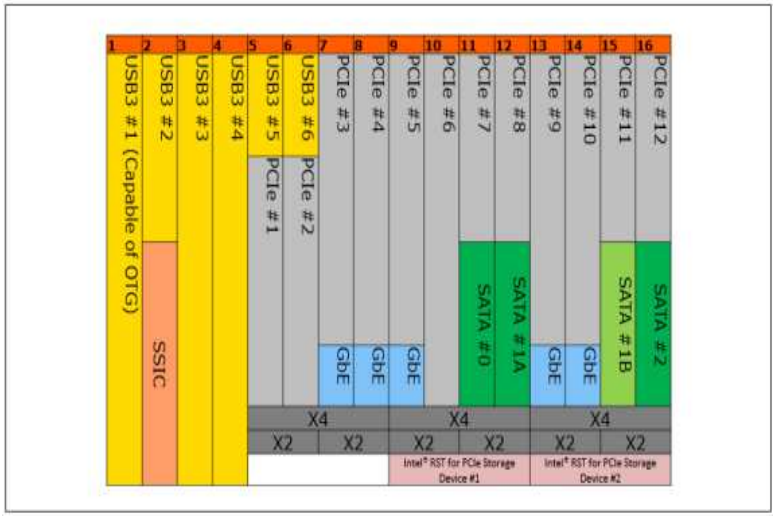
AR use 1086PP
Non AR use 1080PP

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left Front
USB3.0-4				JUSB3-->Left Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader (PCIE)
USB3.0-6		PCIE-2		Type-C Port
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	NA
		PCIE-8	SATA-1	M.2 3042(SATA Cache)
		PCIE-9		LOM
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Left Front
3	JUSB3-->Left Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	Type-C Port
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



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Title: Port assignment

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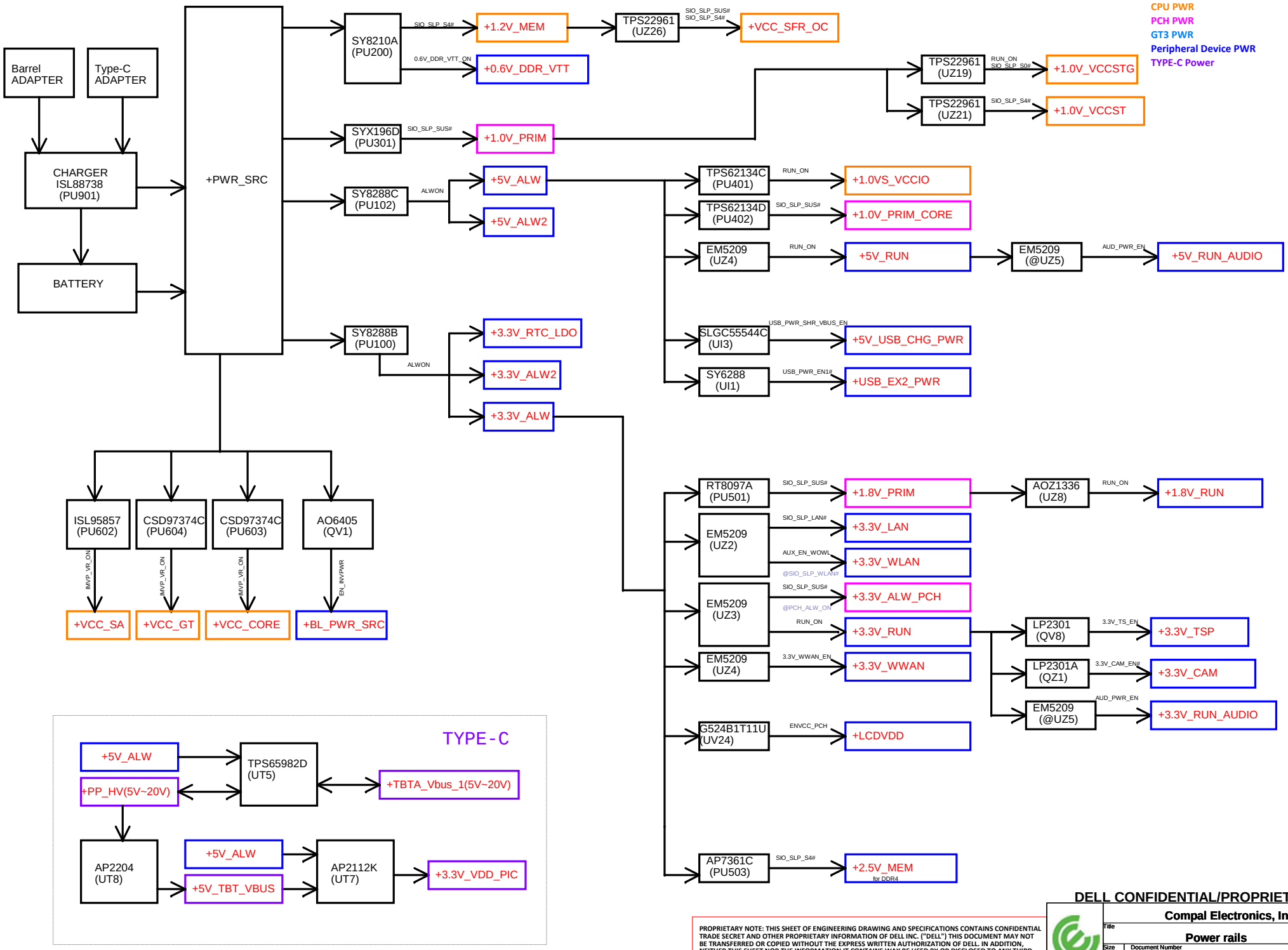

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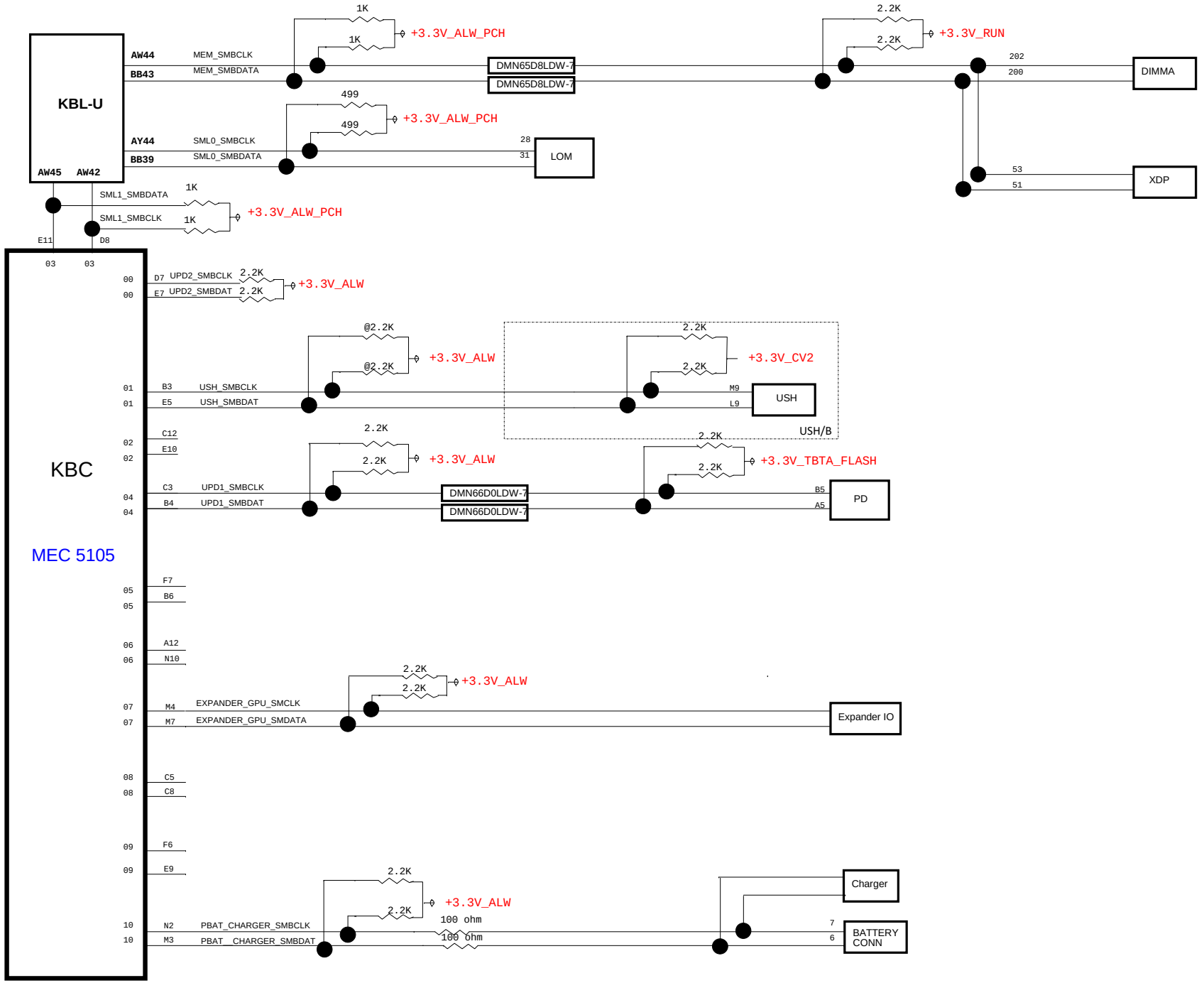

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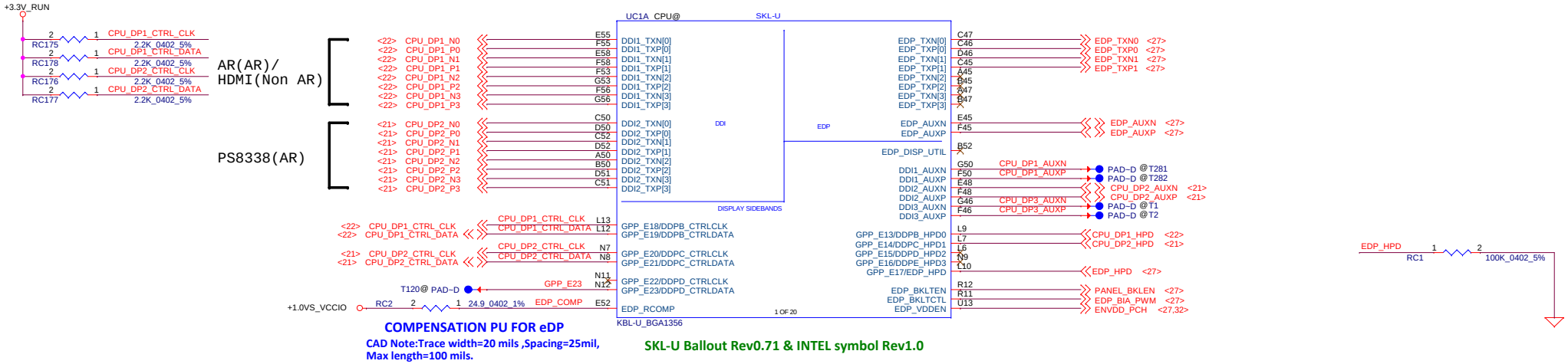
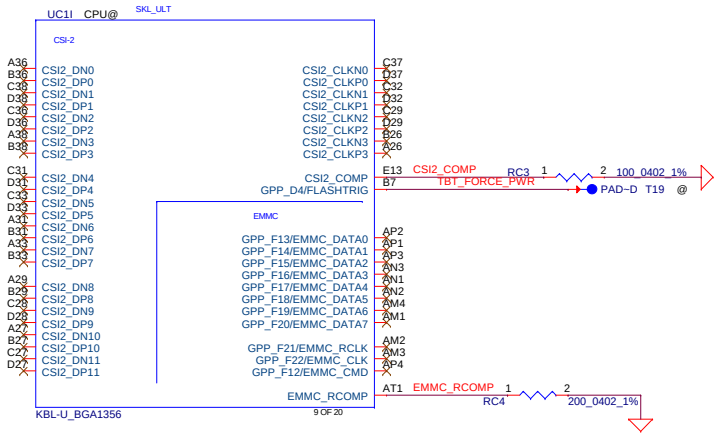


COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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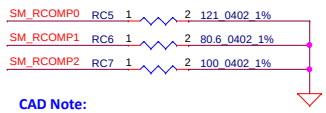
For DDR4

DDR4, Ballout for side by side(Interleave)

DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Title: CPU (2/14)

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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

UC1E CPU@ SKL-U

SPI - FLASH
SPI - TOUCH
C LINK
SMBUS, SMLINK
LPC

KBL-U_BGA1356 5 OF 20

+1.8V?

SOFTWARE TAA

RF Request

Place close CPU side

128Mb Flash ROM

W25Q128FVSIQ_SO8

E-T_6705K-Y20N-00L

JSPI1 CONN@

TLS CONFIDENTIALITY
HIGH | ENABLE
LOW(DEFAULT) | DISABLE
WEAK INTERNAL 20K PD

EC interface
HIGH | ESPI
LOW(DEFAULT) | LPC
WEAK INTERNAL 20K PD

EXI BOOT STALL BYPASS
HIGH | ENABLED
LOW(DEFAULT) | DIABLED
WEAK INTERNAL PD

CHECK LPC_CLK FOR DEBUG CARD?

Reserve

03/02:follow Intel MOW_2015WW06

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Title: CPU (3/14)

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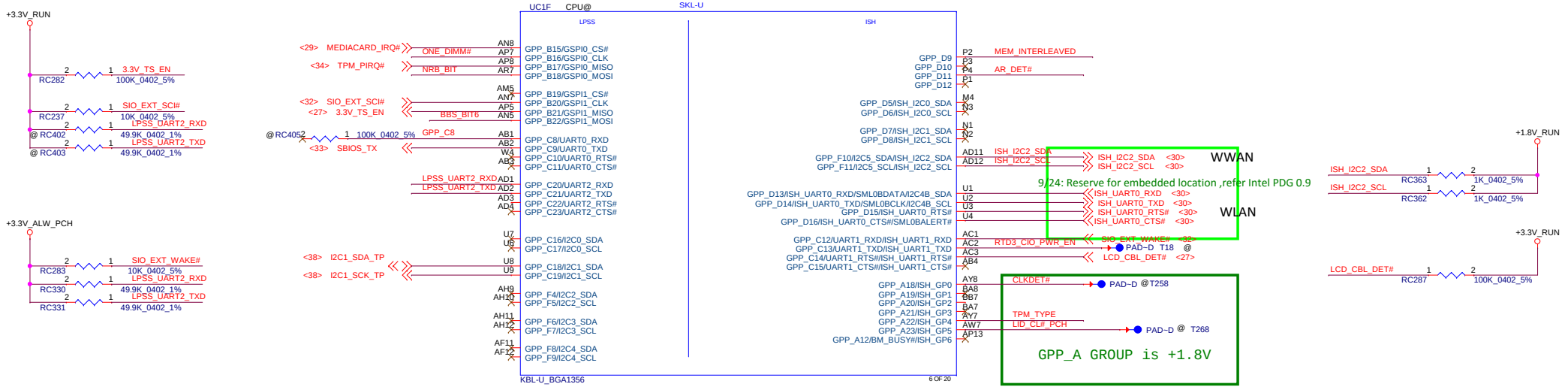
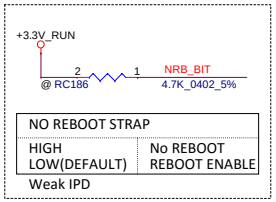
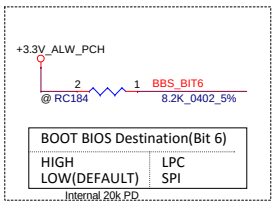
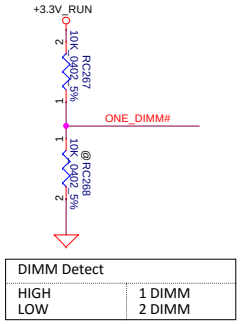
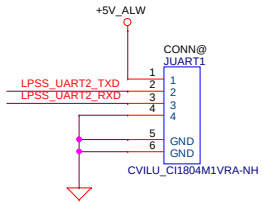
For BR/SB

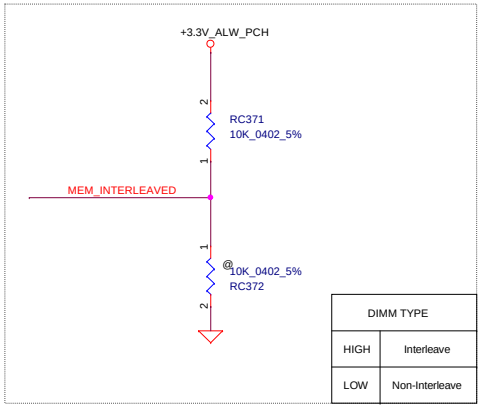


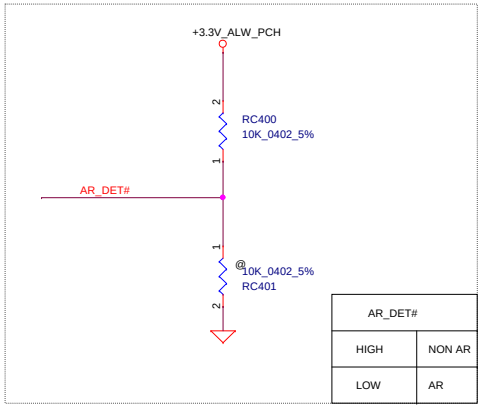












Reserved TPM_TYPE @RC349 100_0402_1%

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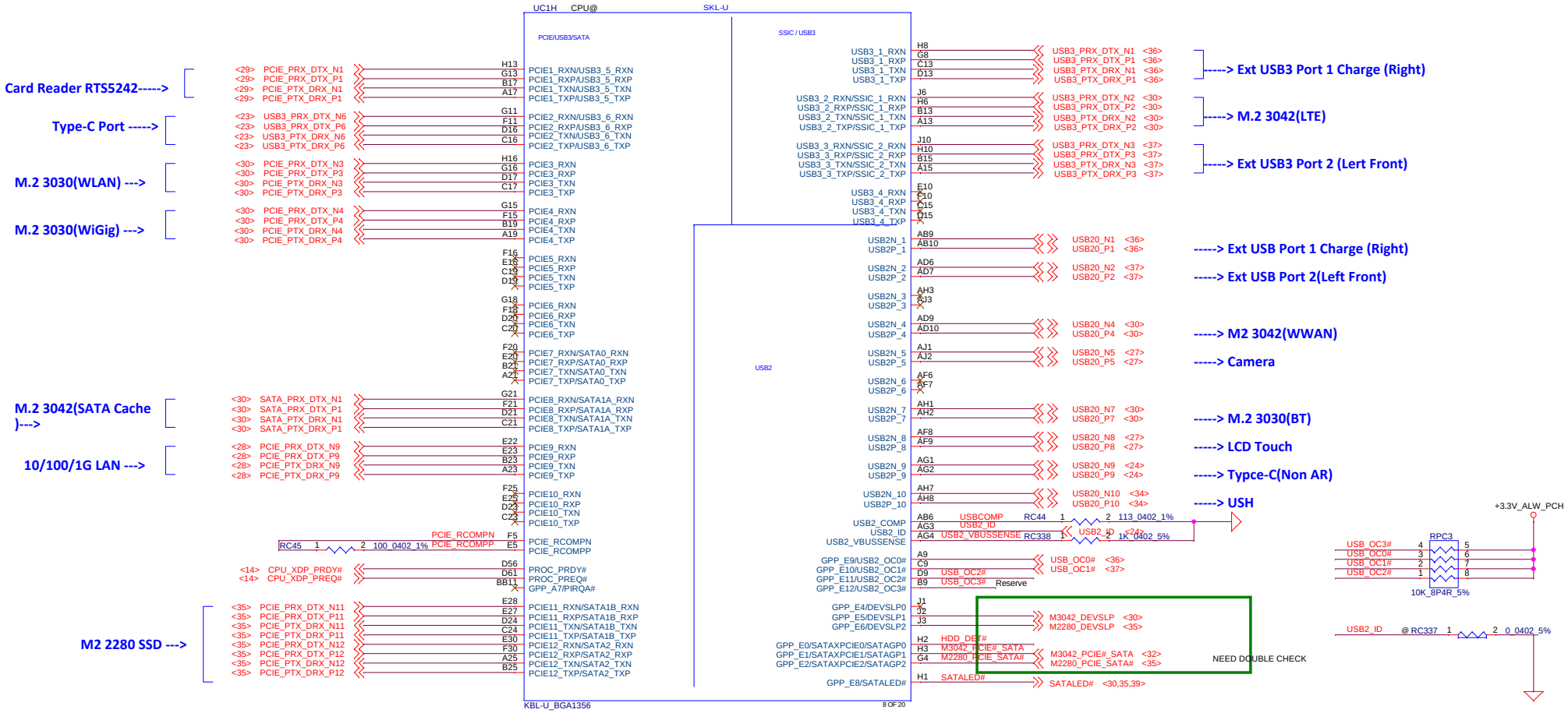
For NON AR, Steamboat



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Title: CPU (5/14)

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For SB/KW w/o AR

UC1J CPU@ SKL_ULT

CLOCK SIGNALS

Cardreader--->
WLAN--->
WIGIG--->
M.2 SDD--->
LAN--->

KBL-U_BGA1356

10 OF 20

XTAL24_IN
XTAL24_OUT
YC1 24MHZ_12PF_X3G024000DC1H
For Skylake,YC1 24 MHz (50 Ohm ESR)
For Cannonlake,YC1 38.4 MHz (30 Ohm ESR)
546765_546765_2014WW48_Skylake_MOW_Rev_1_0

PCH_RTCX1
PCH_RTCX2
YC2 32.768KHZ_12.5PF_9H03200042
ESR MAX=50k ohm

SHORT PADS-D
@CMOS1
CMOS1 must take care short & touch risk on layout placement

8/21 can change to 10K for merge to RP

UC1K CPU@ SKL-U

SYSTEM POWER MANAGEMENT

KBL-U_BGA1356

11 OF 20

connect to VCCMPHYGTAON_1P0 enable pin

JAPS1 CONN@
CVILU_CF4218FH0R0-05-NH

ESD Request:place near CPU side

RC215

POP	NO Support Deep sleep
DE-POP	Support Deep sleep

if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)

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Title: CPU (6/14)		
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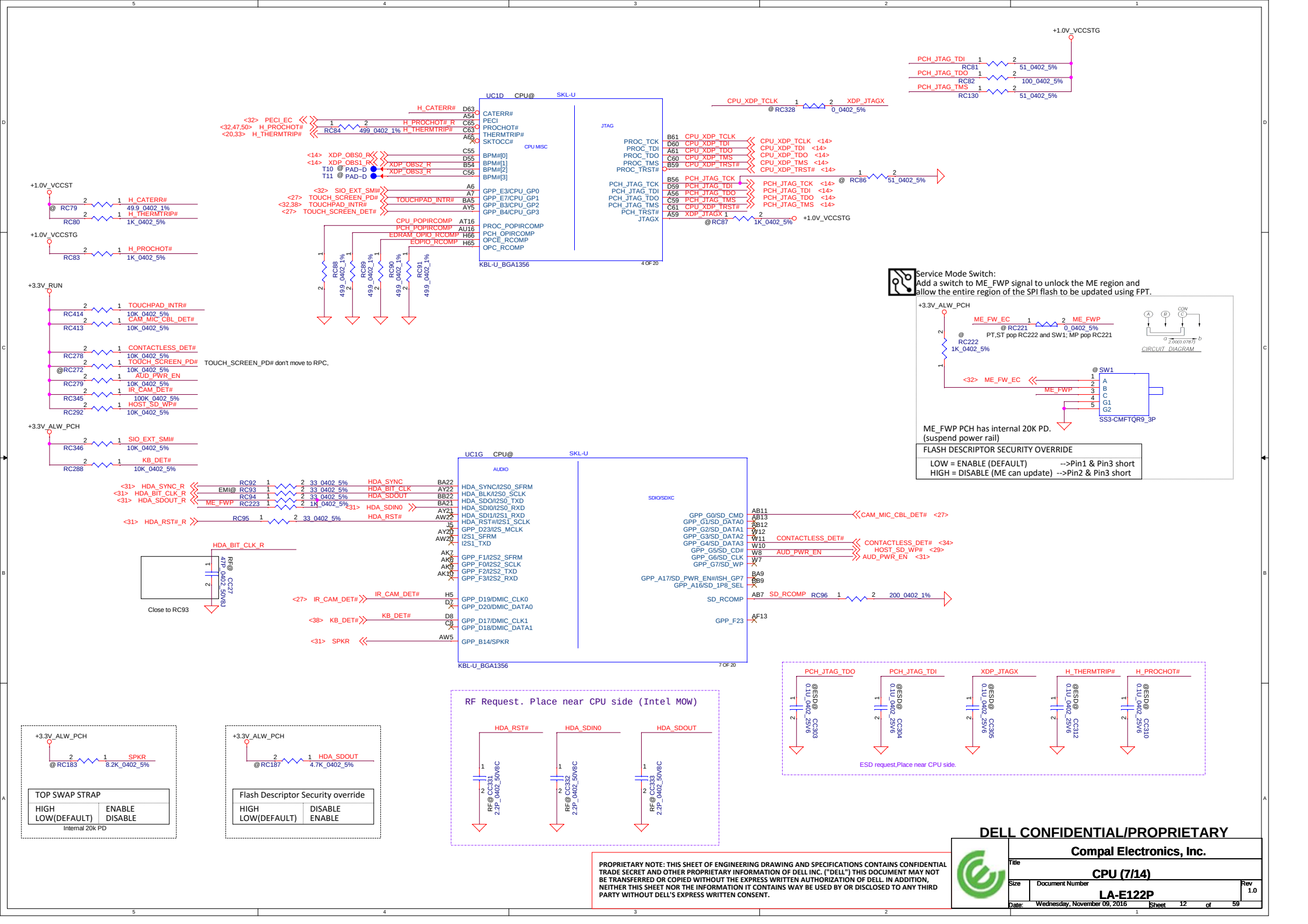

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Title: CPU (7/14)

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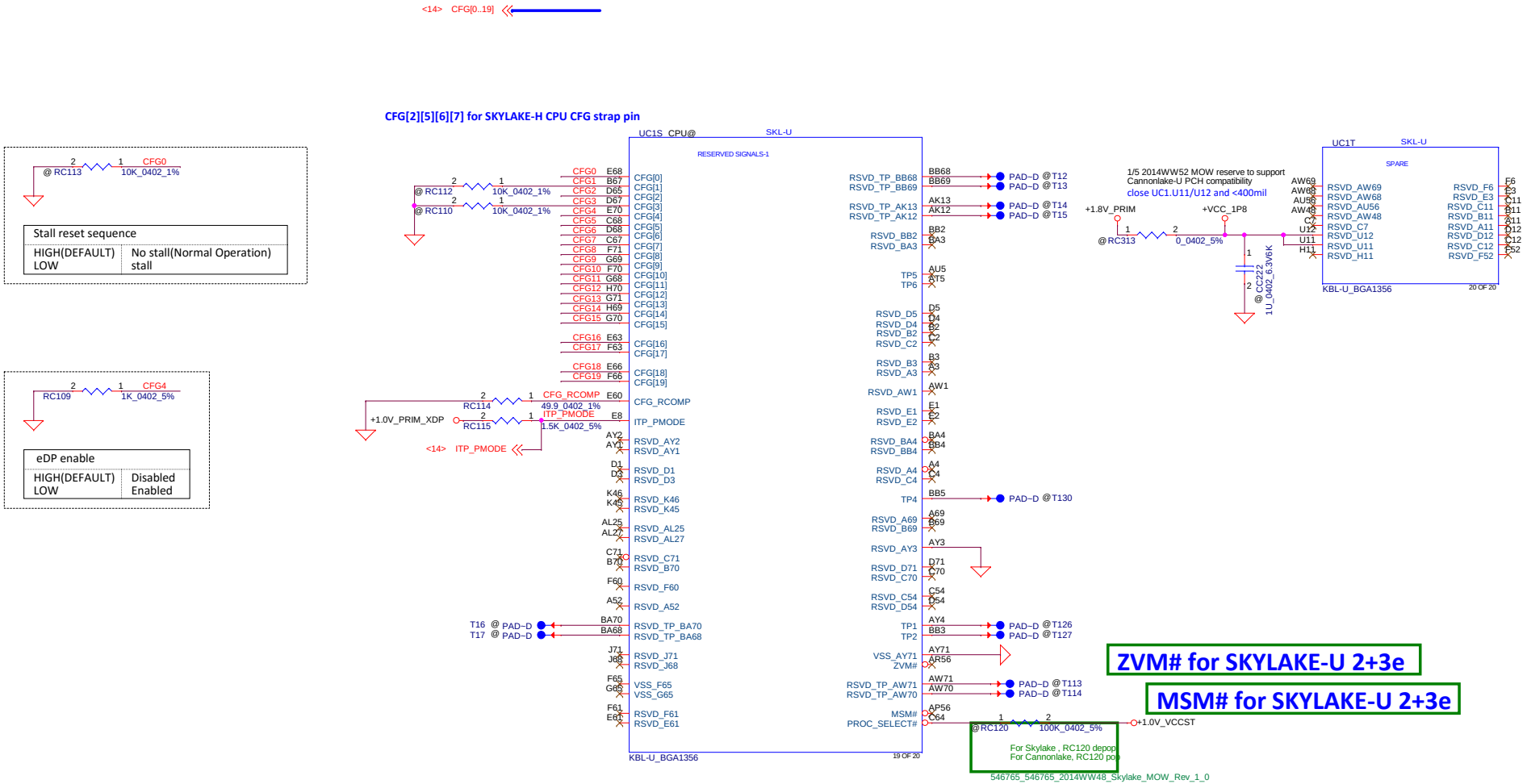

Stall reset sequence	
HIGH(DEFAULT)	No stall(Normal Operation)
LOW	stall

eDP enable	
HIGH(DEFAULT)	Disabled
LOW	Enabled

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Title: CPU (8/14)

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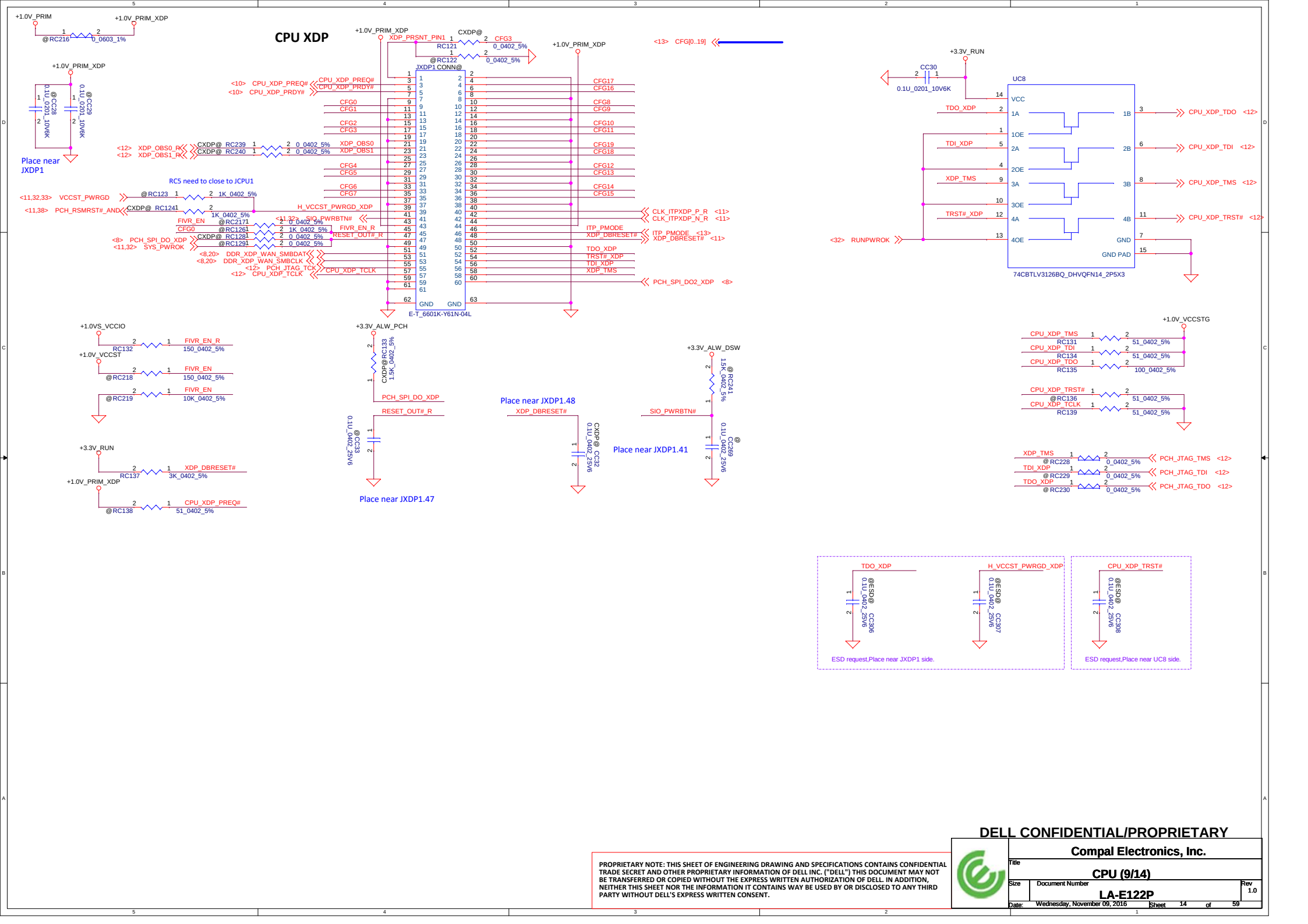

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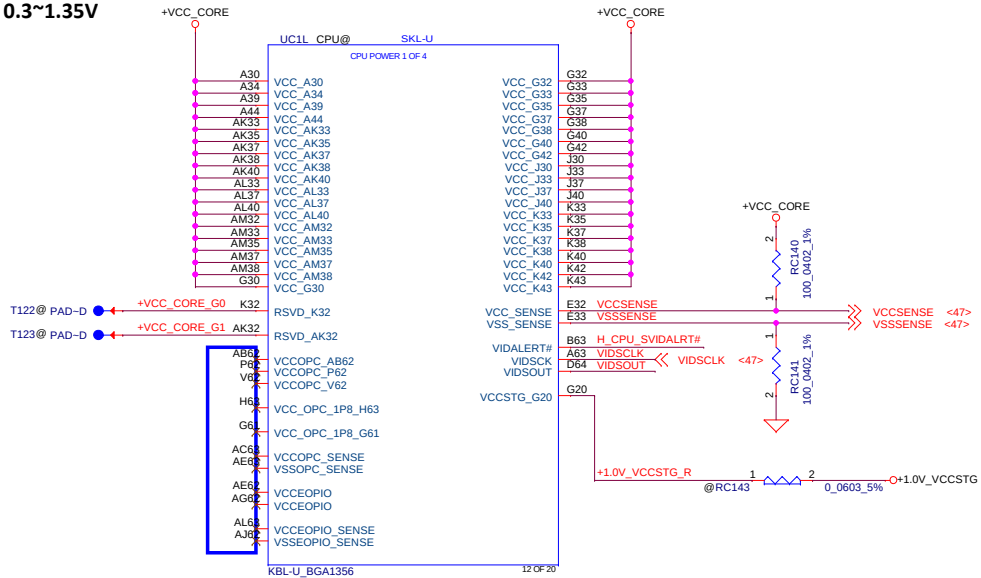
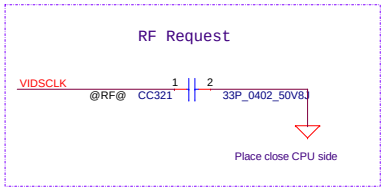
+VCC_CORE: 0.3~1.35V

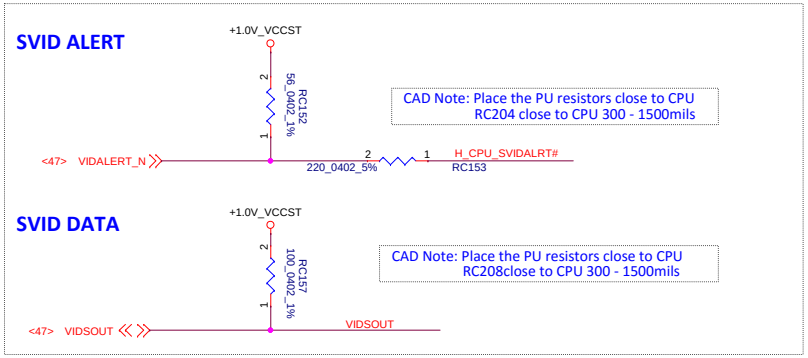


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e (w/ on package cache)





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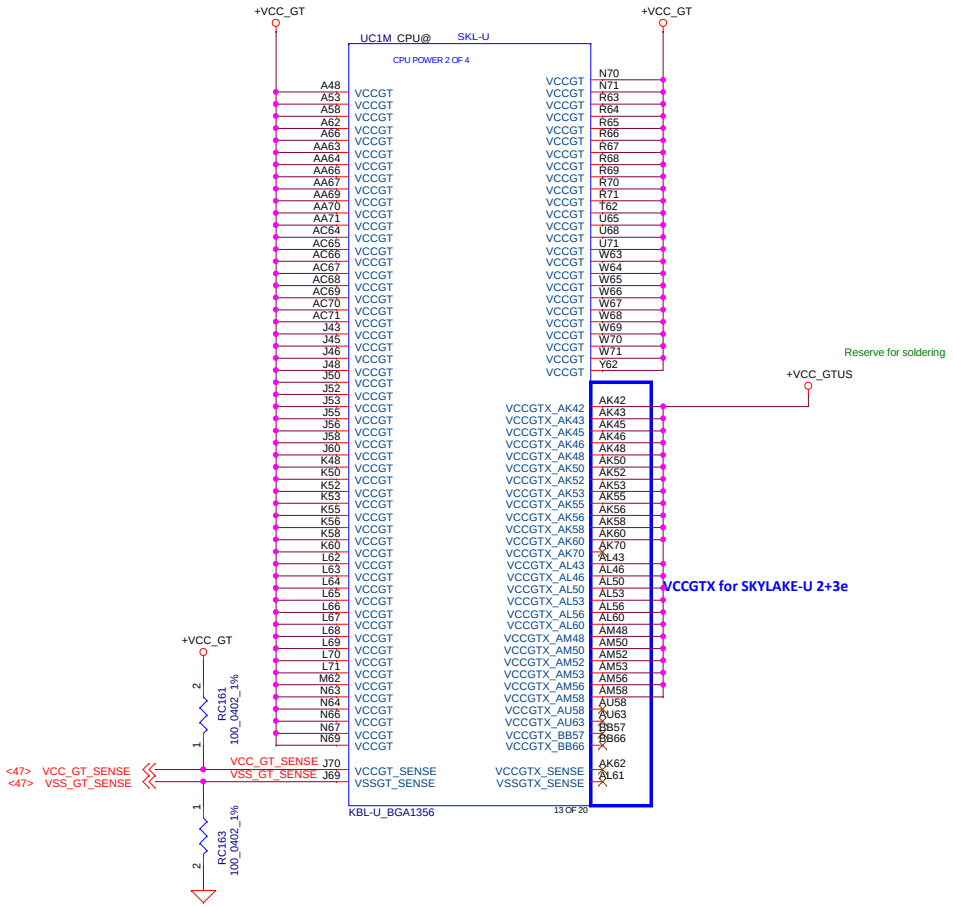
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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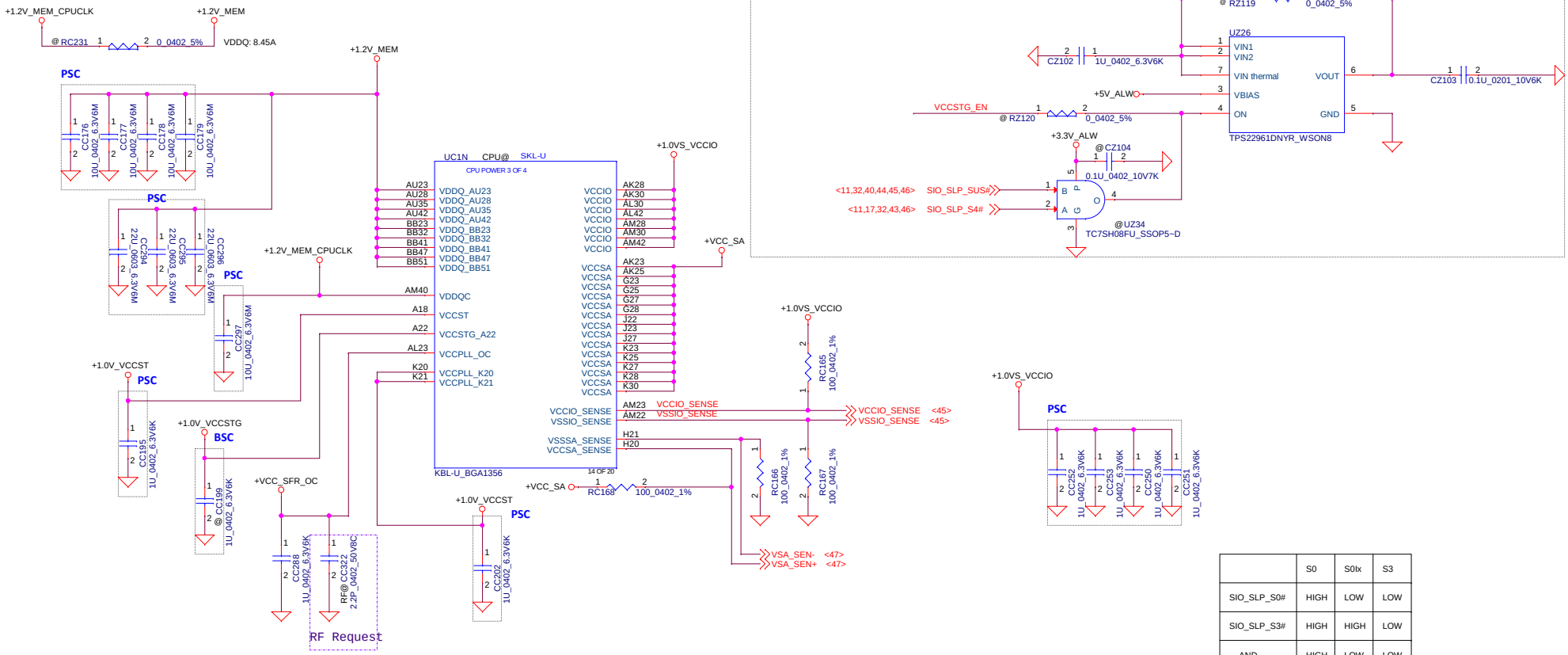
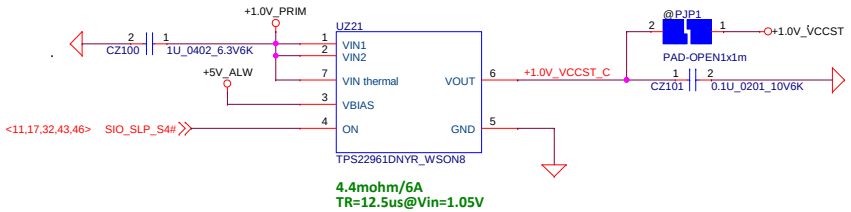


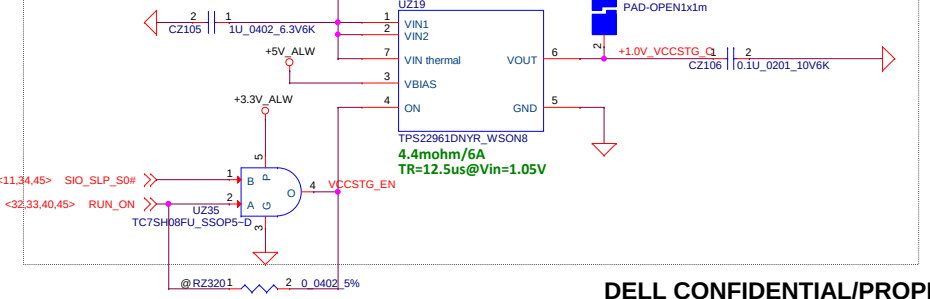
+VCCPLL_OC source

	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

+1.0V_VCCST source



+1.0V_VCCSTG source



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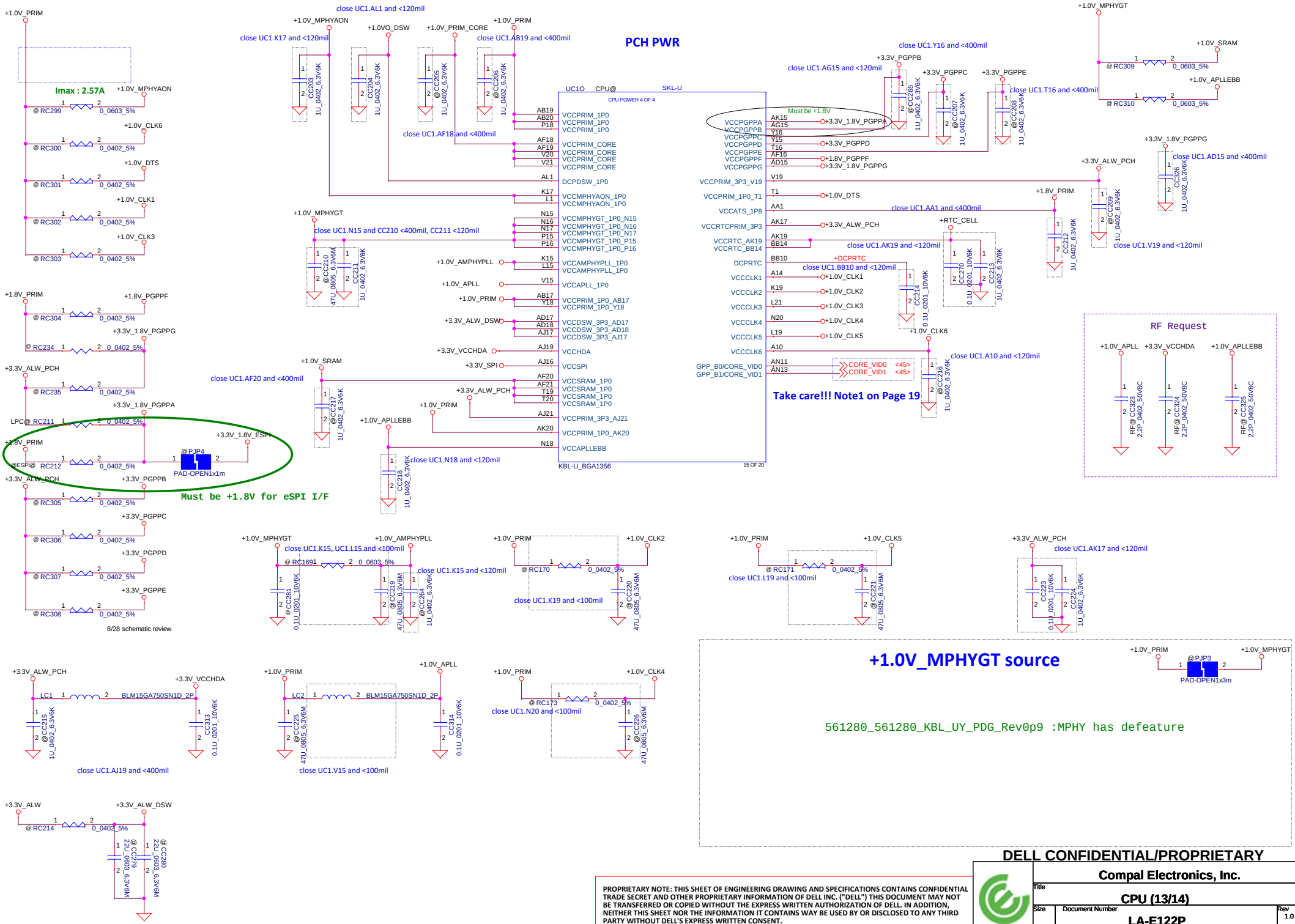

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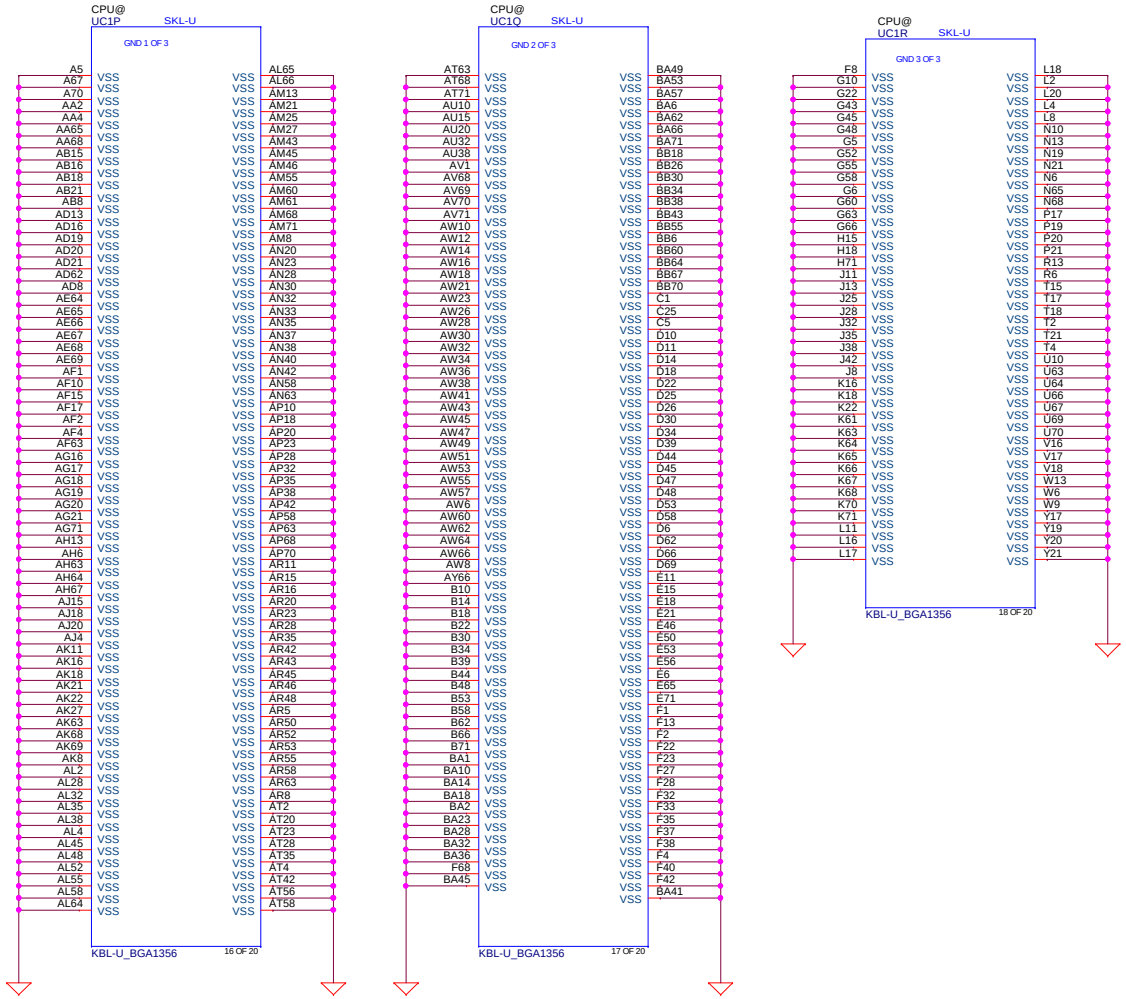
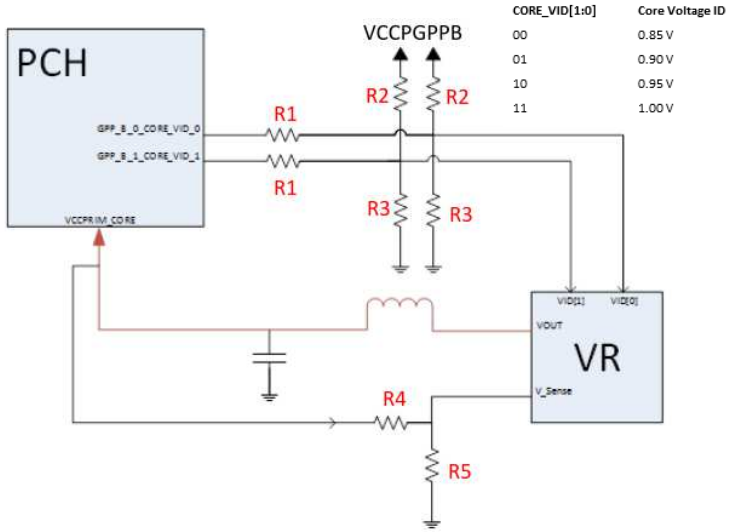


Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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Title: CPU (14/14)

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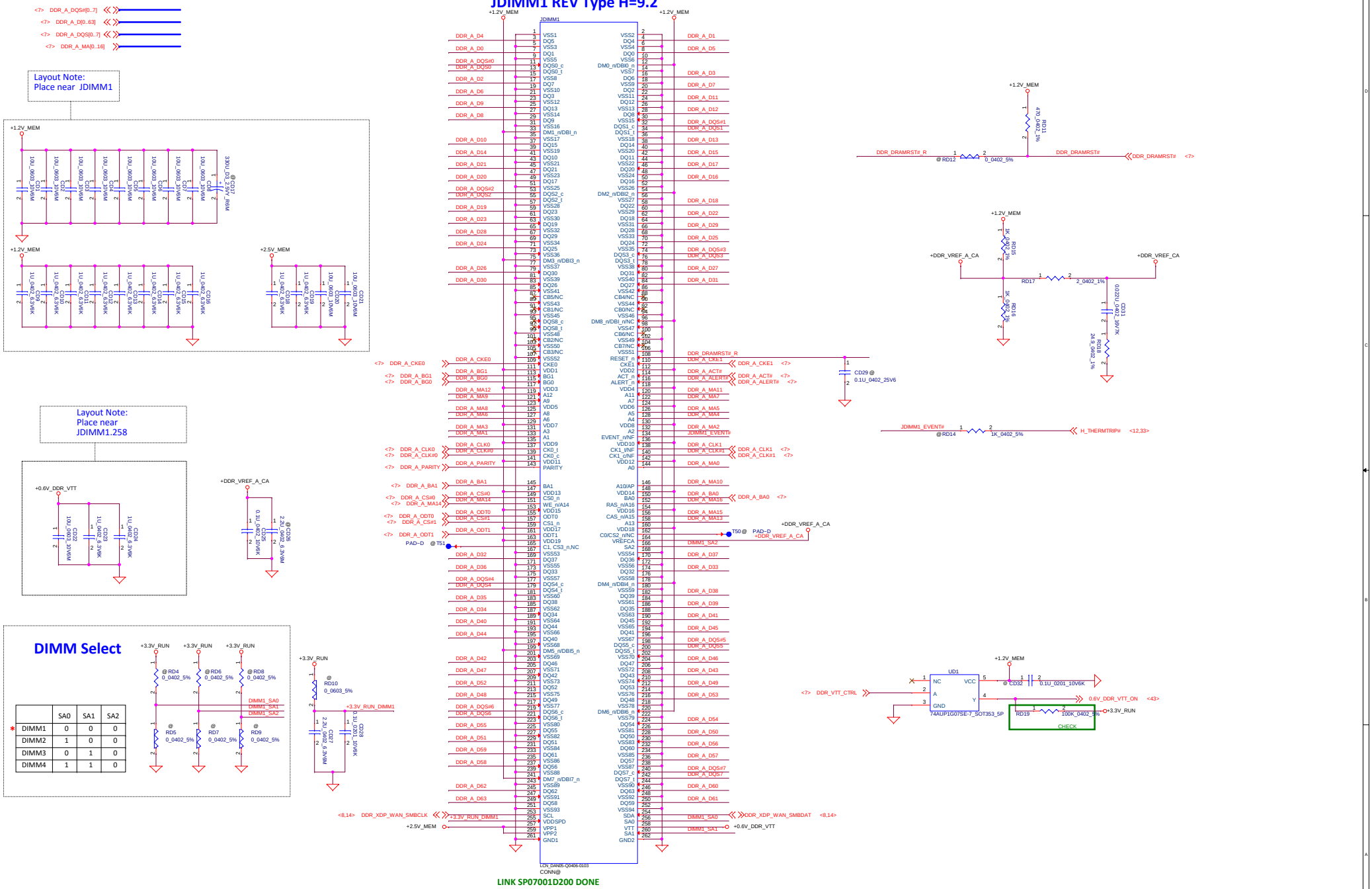
For DDR4

JDIMM1 REV Type H=9.2



LINK SP07001D200 DONE

DELL CONFIDENTIAL/PROPRIETARY

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Compal Electronics, Inc.	
Title	DDR4
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Date:	Wednesday, November 09, 2016
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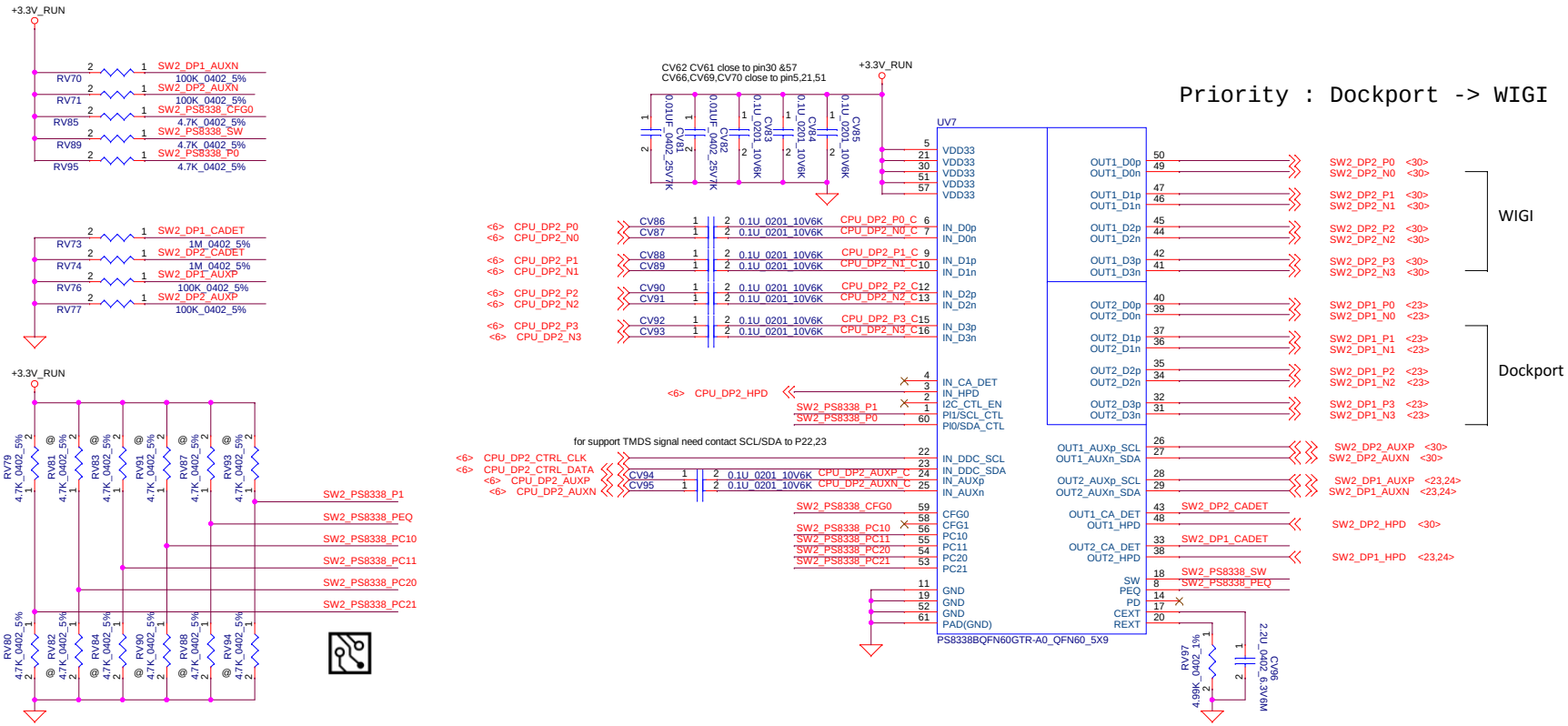
For Steamboat12/14 &Kirkwood



Priority : Dockport -> WIGI

Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged
SW = H: Port2 has higher priority when both ports are plugged (default)

vender suggest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M:LLEQ, compensate channel loss up to 8.5dB @HBR2

PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

Compal Electronics, Inc.

Title: DP SW2 PS8338

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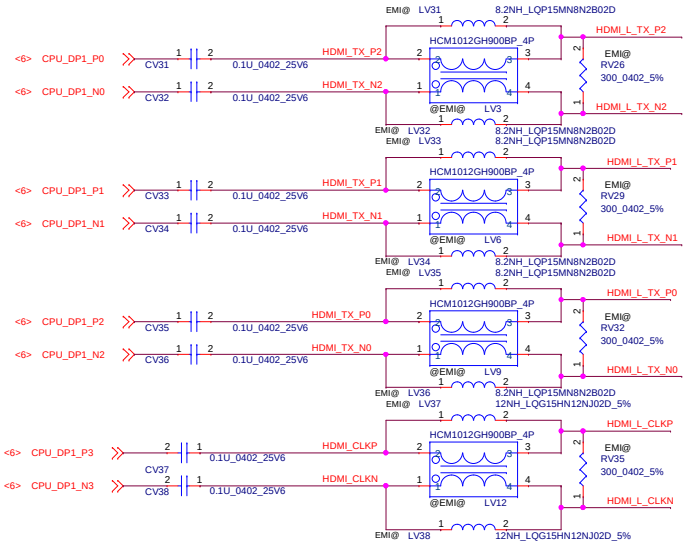
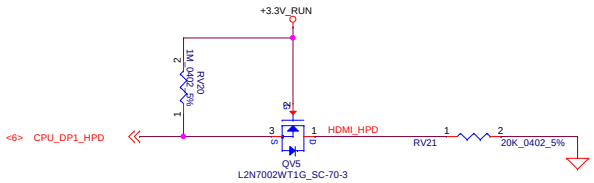
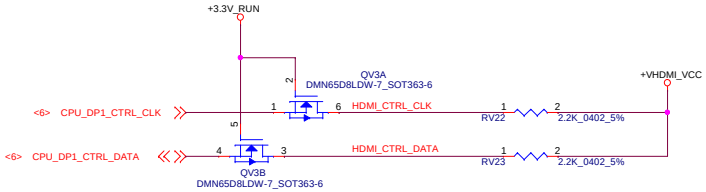
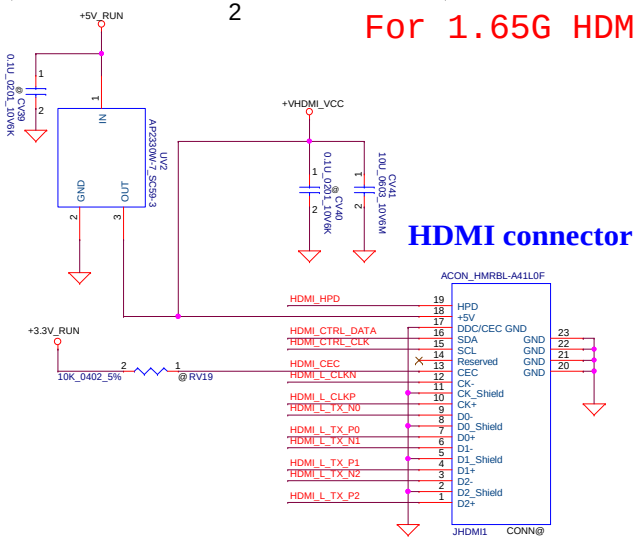
For 1.65G HDMI from CPU

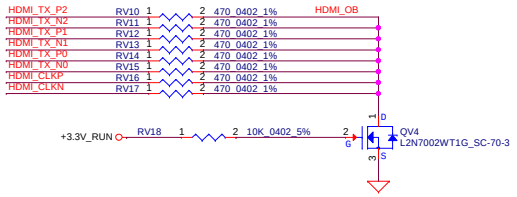








LINK DC231604012 (temp) DONE



Compal Electronics, Inc.

Title: HDMI CONN

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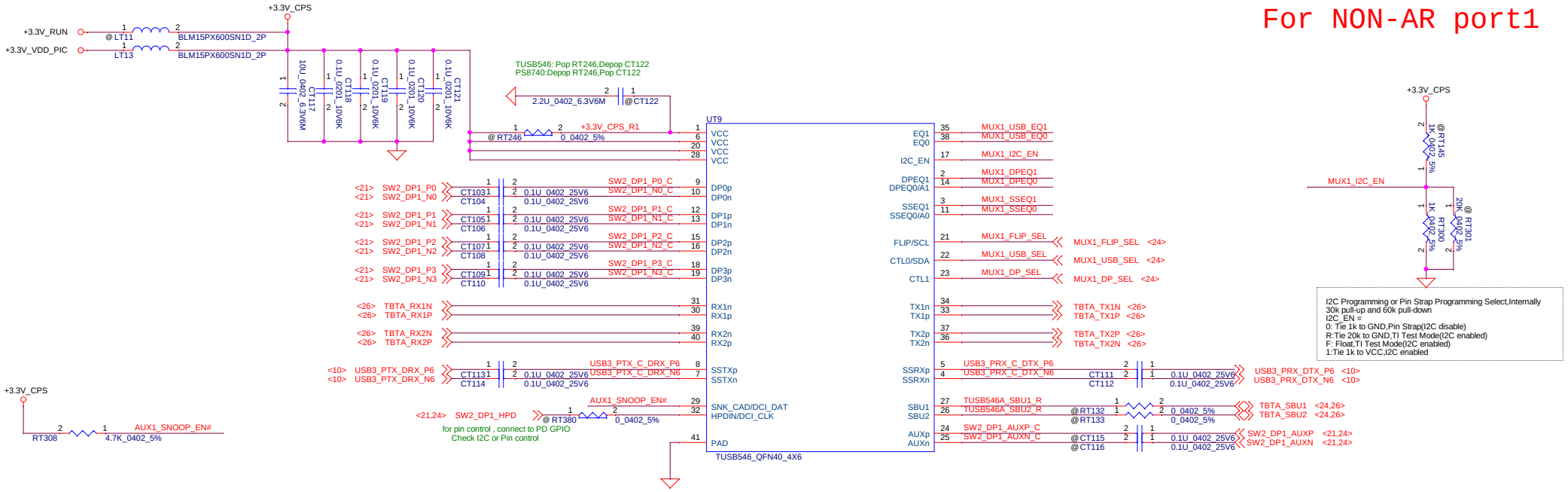
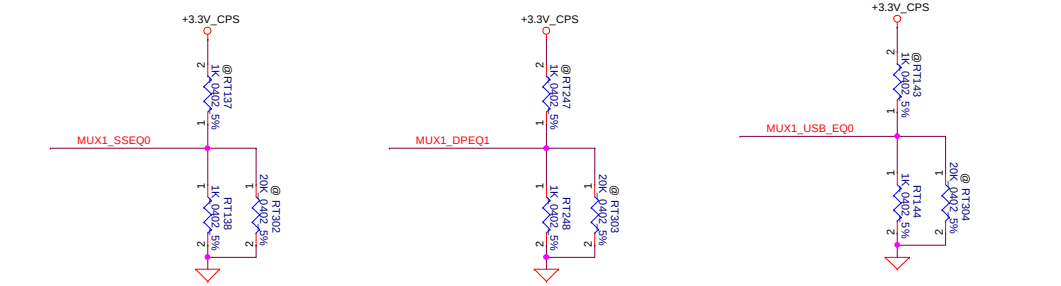
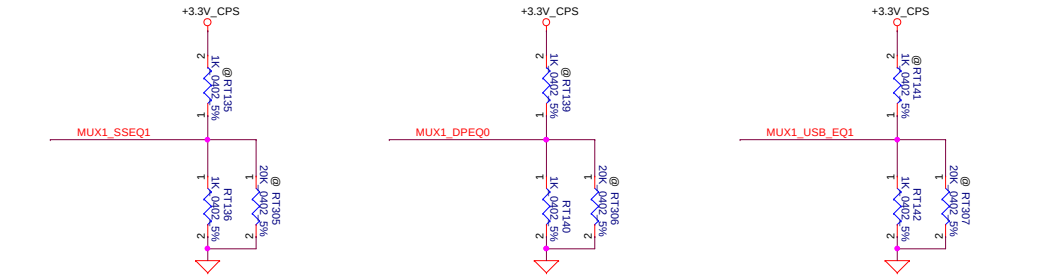
For NON-AR port1







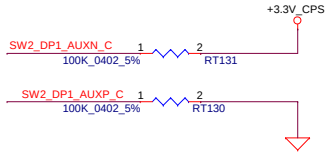


Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Compal Electronics, Inc.

Title: DP/USB3 Repeater SW TUSB546

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For NON-AR port1

DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.5A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Need Link TPS65982D

Compal Electronics, Inc.

Title: [Type C]PD Controller TI

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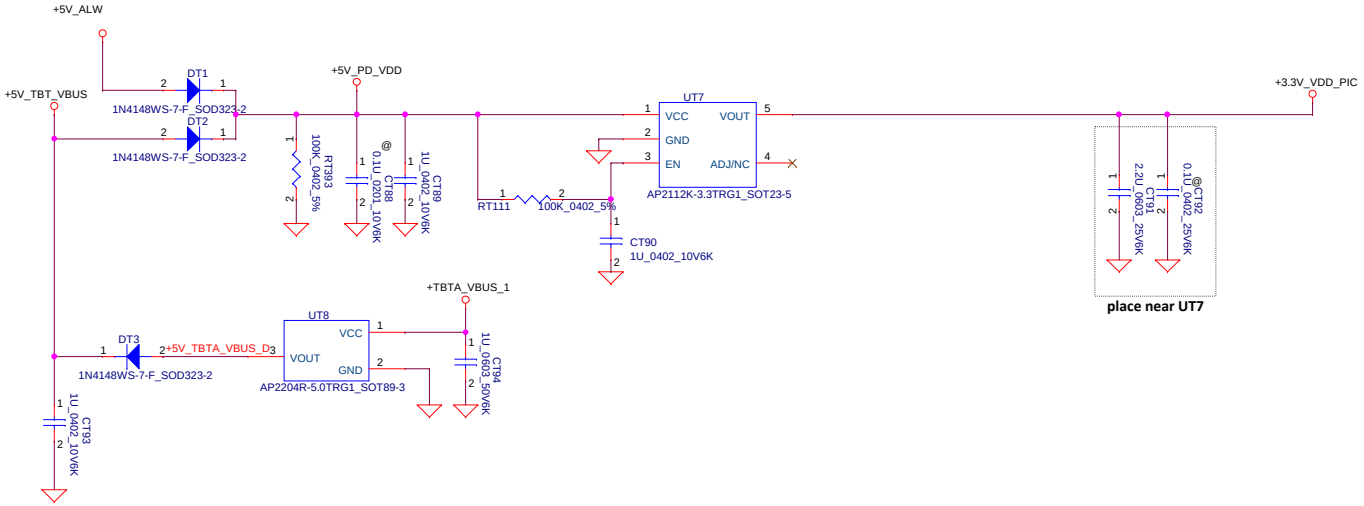

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Title: [Type C]PD Power

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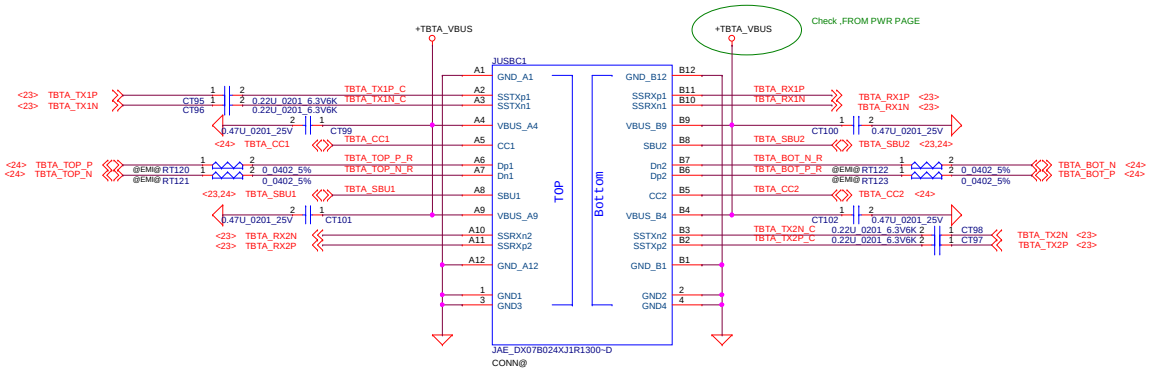
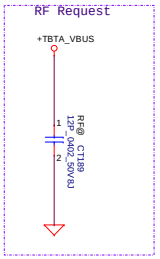
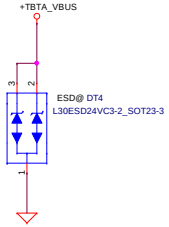
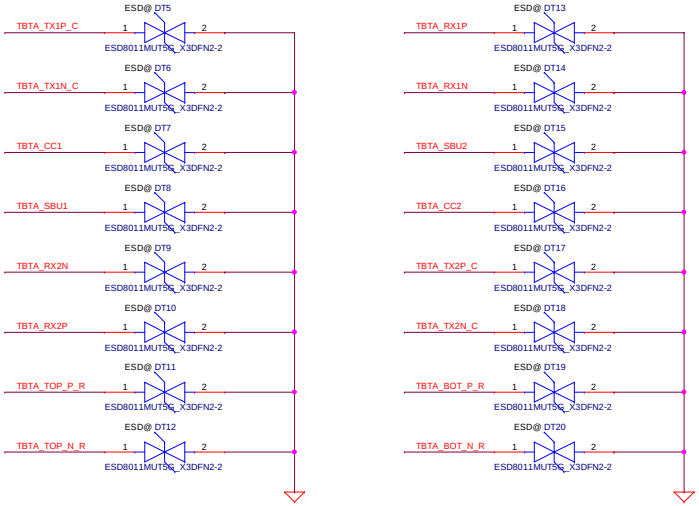
For NON AR Config

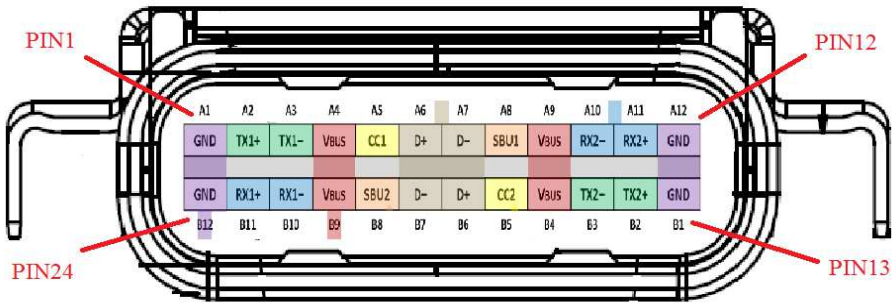






Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done





Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

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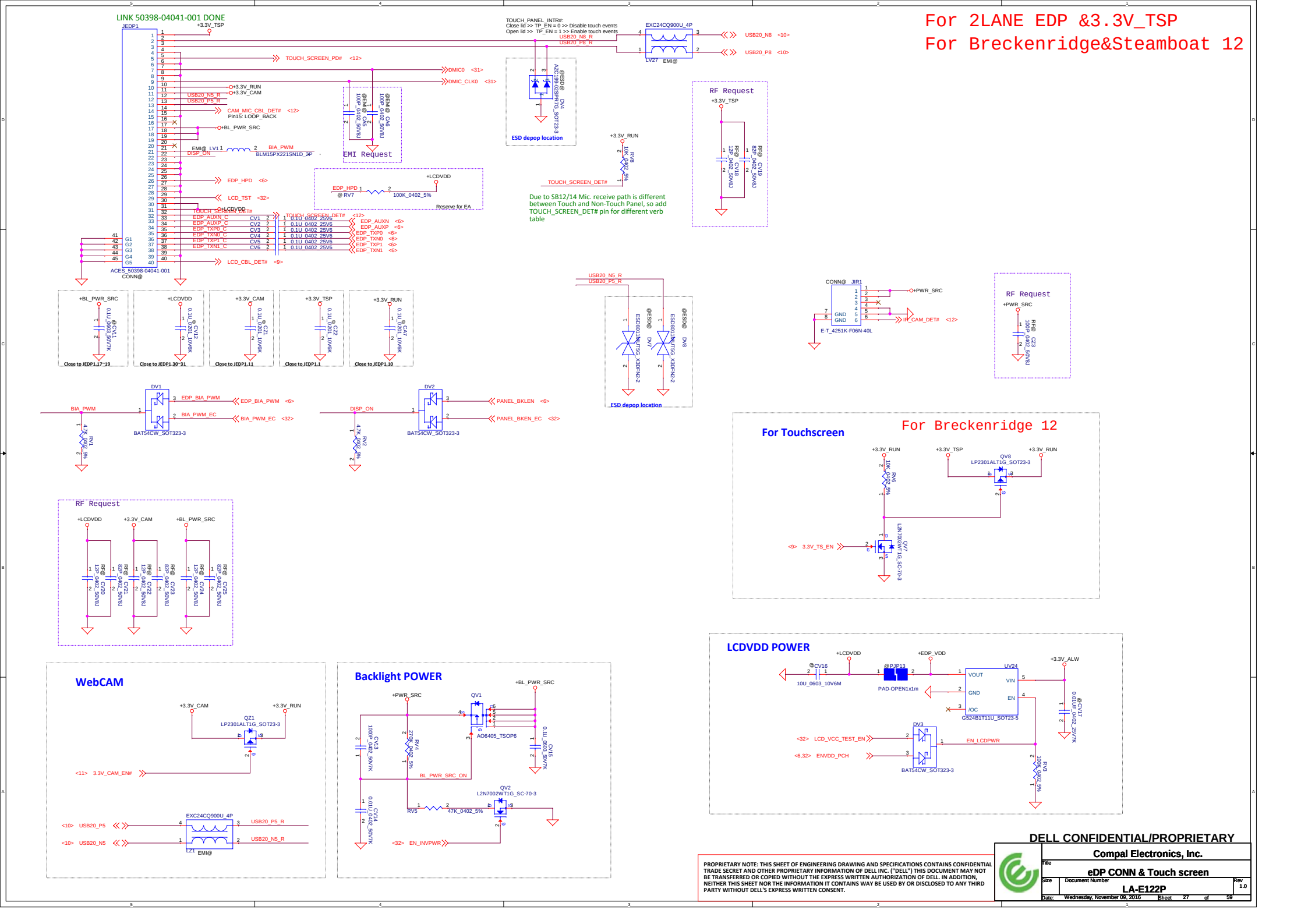
For 2LANE EDP &3.3V_TSP
For Breckenridge&Steamboat 12
LINK 50398-04041-001 DONE
JEDP1
ACES_50398-04041-001
CONN@
TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events
EXC24CQ900U_4P
LV27
EMI@
ESD depop location
EMI Request
RF Request
Due to SB12/14 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table
Reserve for EA
For Touchscreen
For Breckenridge 12
WebCAM
Backlight POWER
LCDVDD POWER
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Compal Electronics, Inc.
eDP CONN & Touch screen
LA-E122P
Wednesday, November 09, 2016
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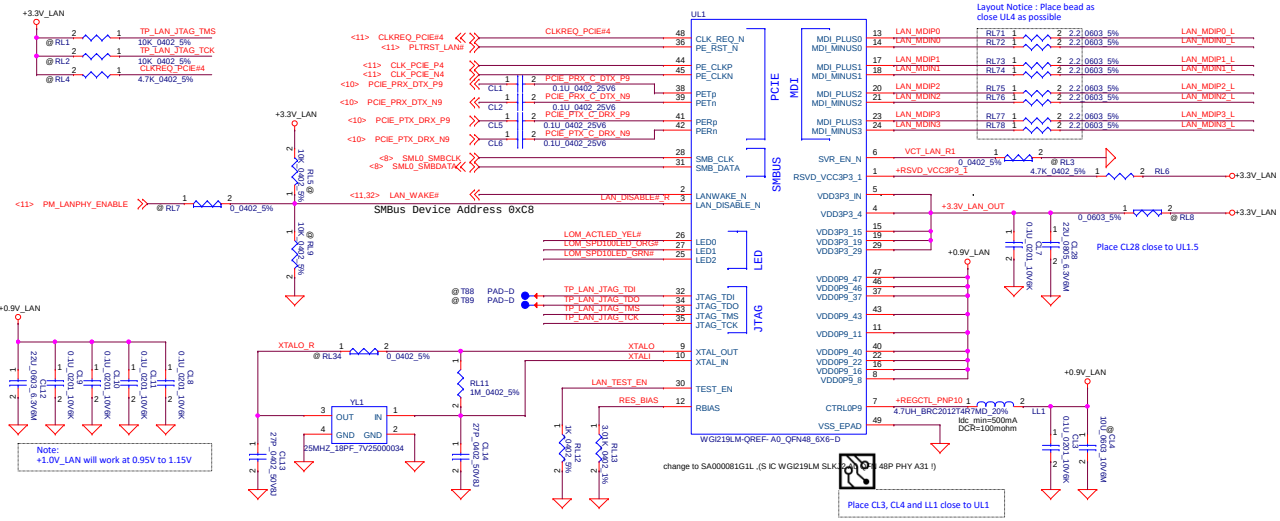
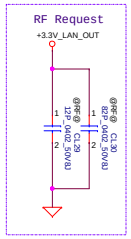
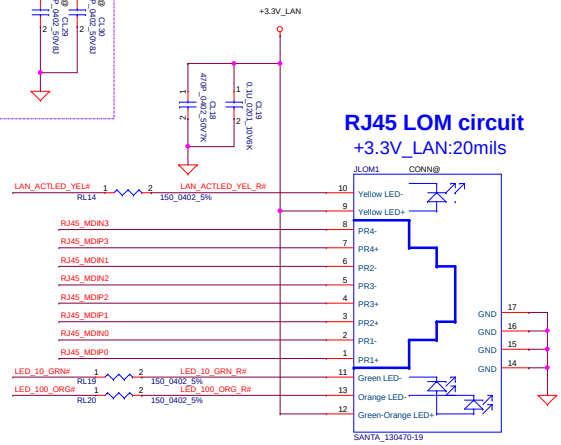
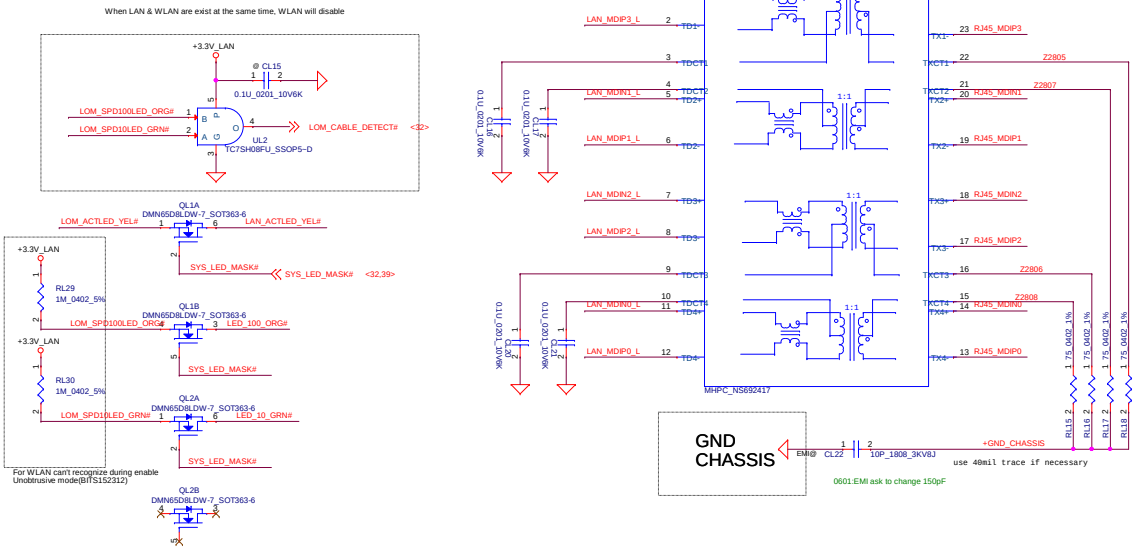






Link DC231603220 (temp) DONE



Compal Electronics, Inc.

Title: LAN Clarkvillie & RJ45

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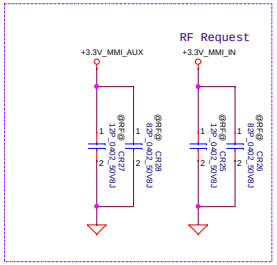
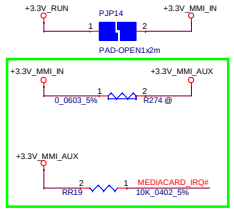
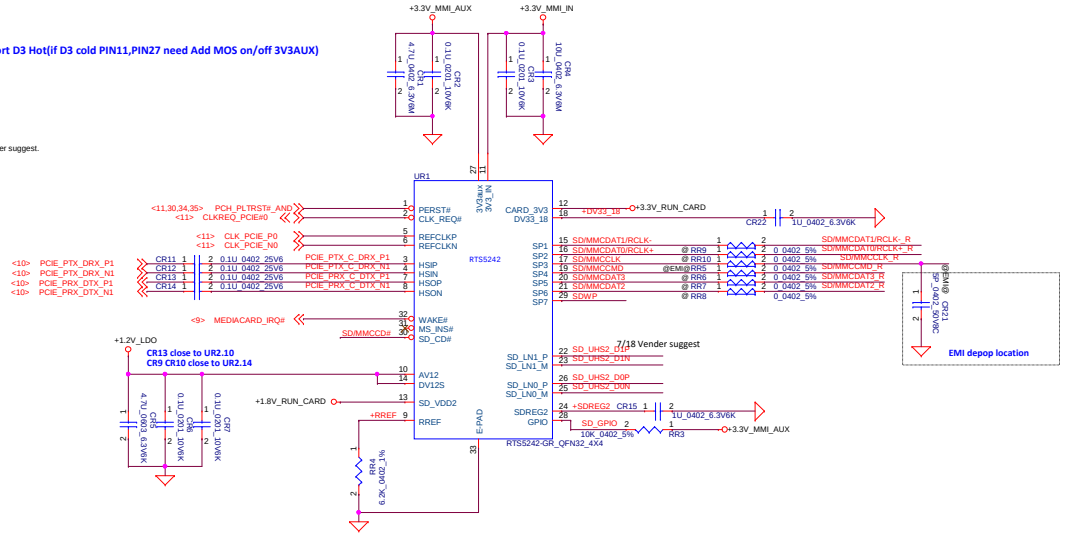
For PCIE Interface

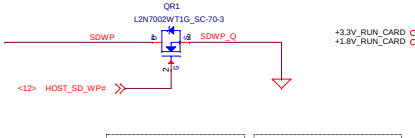


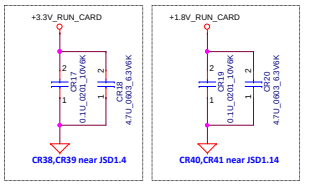


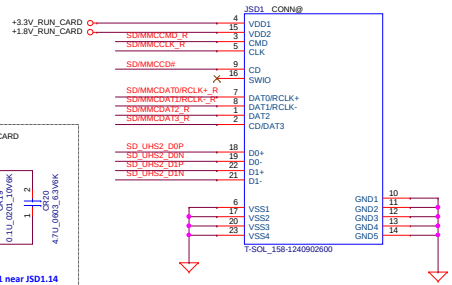
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	Low	Low	Write Enable
Low	Low	High	Write Protect(FW LOCK)







LINK SP071603151 (temp) DONE

Compal Electronics, Inc.

Title: Card Reader RTS5242

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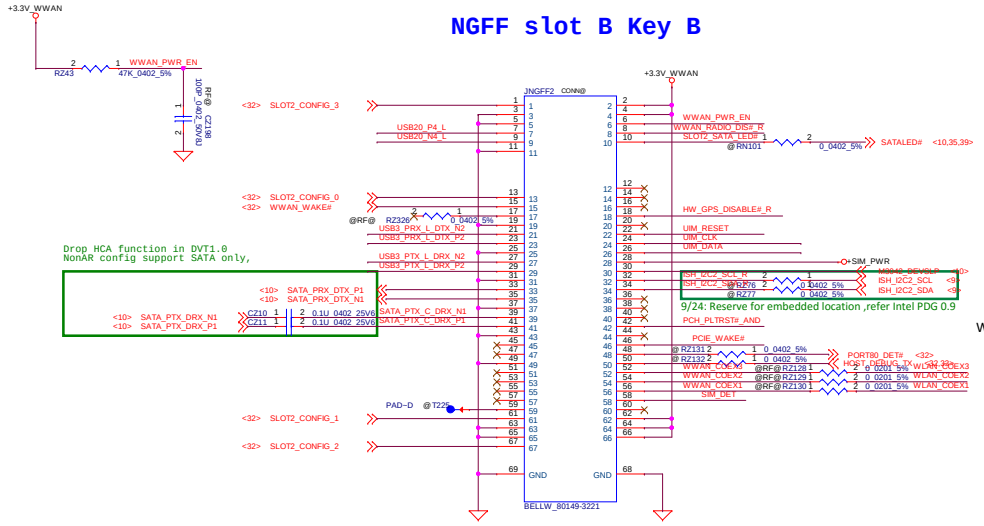
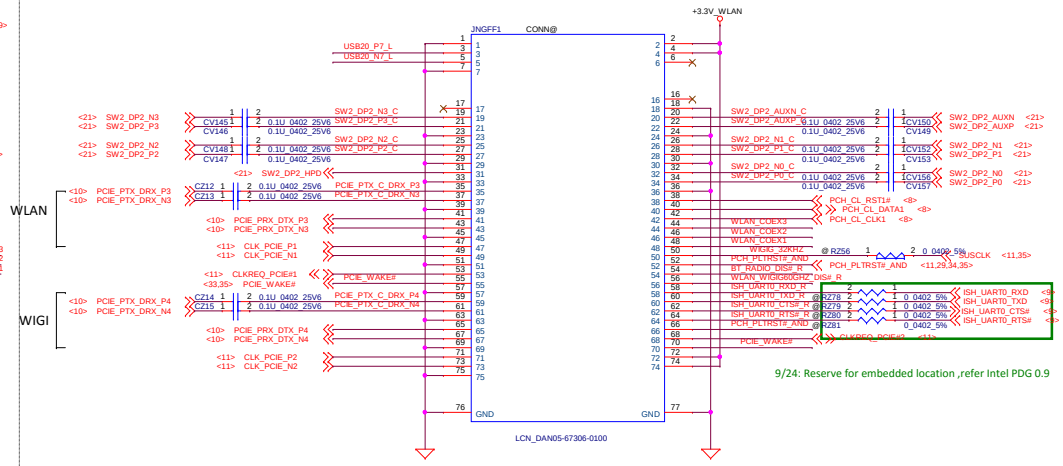
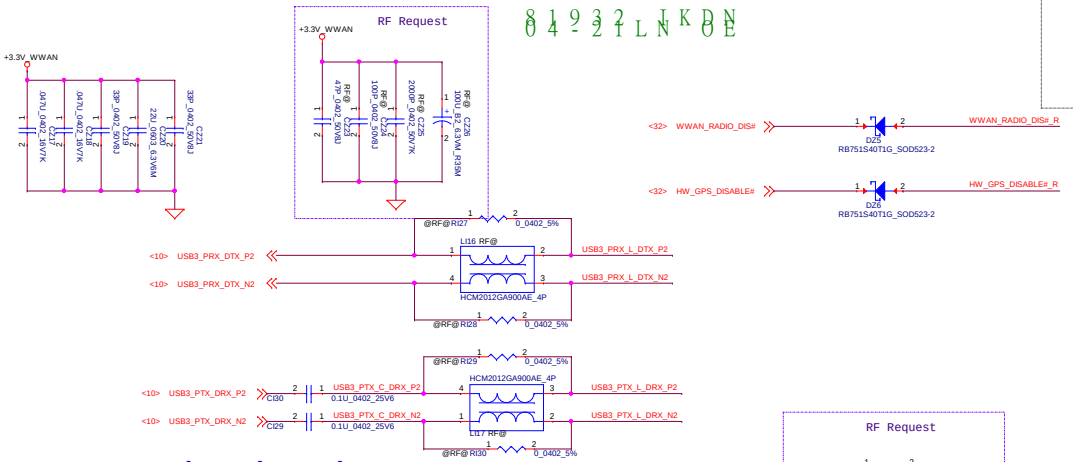
for no AR,Brekenridge 12/14/15 UMA/Steamboat

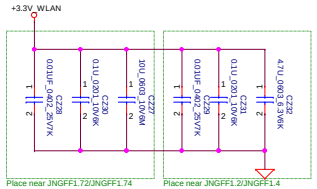
NGFF slot B Key B



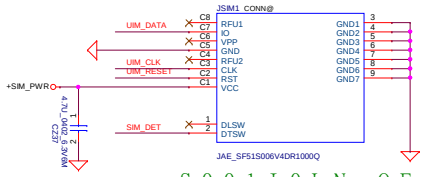
NGFF slot A Key A

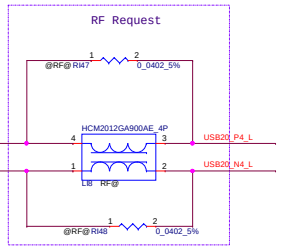


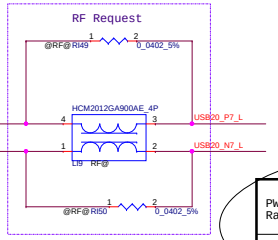


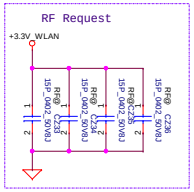


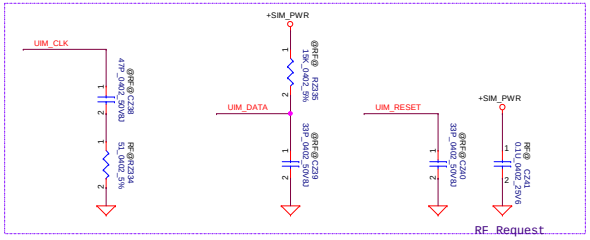
SIM Card Push-Push











STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

Compal Electronics, Inc.

Title: NGFF Card

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

JSPK1 CONN@

ACES_50278-0040N-001

Link SP02001CE00 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 13.

Add for solve pop noise and detect issue

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

UA1

ALC3246-CG_MQFN48_6X6

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

RF Request

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

JHP1 CONN@

Normal

Open

Only BR15U UMA use LA2,LA3,because 6L

Link DC23000DG10 DONE

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.	
Title	Codec ALC3246
Size	C
Document Number	LA-E122P
Rev	1.0
Date:	Wednesday, November 09, 2016
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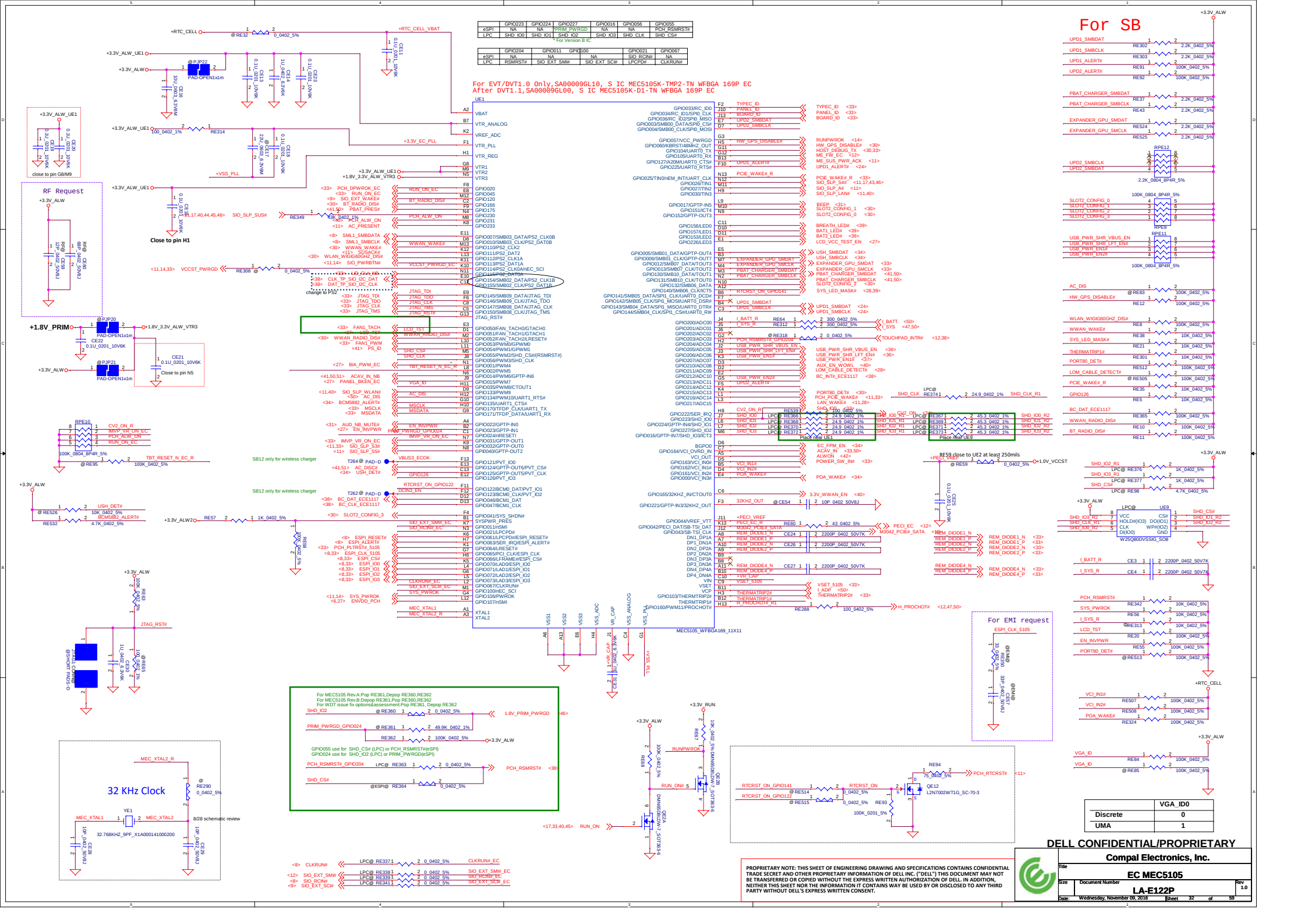


	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

	VGA_ID0
Discrete	0
UMA	1

For SB

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

WDT option	
MEC5105 rev.B	Pop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348 Depop RE362, RE536, RE537
MEC5105 rev.C	Pop RE362, RE536 Depop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348, RE537

RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

PD_ACE_DET# rise time is measured from 5%~68%.

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

RE300	CE47	PANEL SIZE
* 240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

PANEL_ID rise time is measured from 5%~68%.

CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V

GPIO223 is OD. When EC fetches the code, set GPIO223 to Low.

To prevent backdrive to PCH_DPWROK_EC when AC is plugged before +3.3V_ALW ramps up.

In DC mode, ACAV_IN is LOW. This circuit doesn't affect PCH_DPWROK.
In AC mode, 1. ACAV_IN is high. GPIO223 is tri-state. QE13B is ON. QE13A can prevent backdrive to PCH_DPWROK.
2. EC fetches code and the drives GPIO223 to LOW to turn off QE13B. When QE13B is off, un-plug/plug AC will not affect DSW_DPWROK.
3. When WDT occurs, GPIO223 is tri-state (EC reset). ACAV_IN charges CE503. When AC is removed, ACAV_IN goes LOW immediately. QE13B still keeps on according to RC discharging rate. PCH_DPWROK is LOW because ACAV_IN is LOW.

Rest=1.58K , Tp=96 degree???

Link 50271-0040N-001 DONE

Thermal diode mapping

5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

CHECK

Control Byte

0	1	0	0	A2	A1	A0	R/W

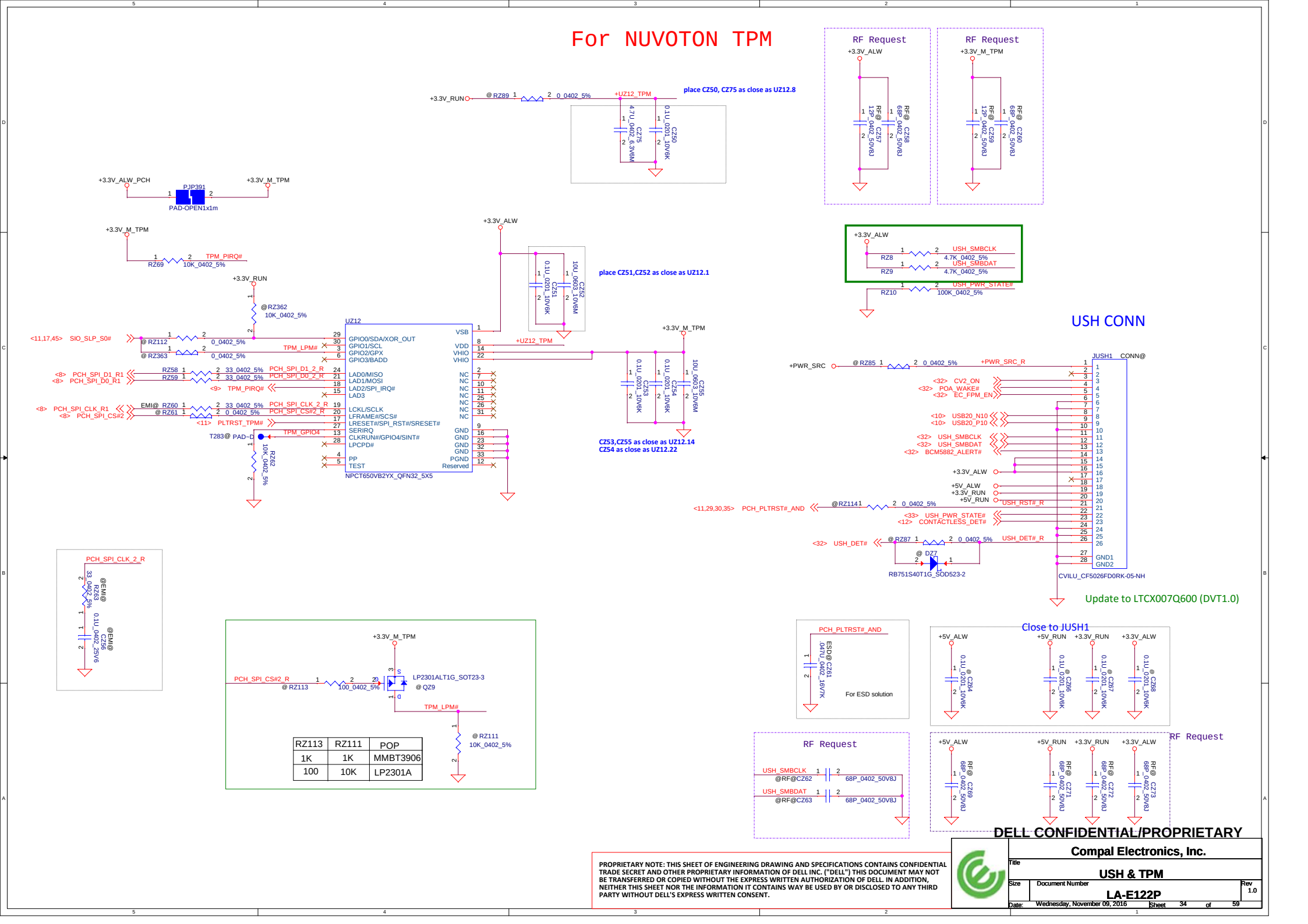
R/W = 0 = Write
R/W = 1 = Read

SMBus address 0x40

Link Microchip MCP23008 SA0000ADQ00 OK (9/6)

Title: MEC5105 support
Size: Document Number: LA-E122P
Rev: 1.0
Date: Wednesday, November 09, 2016 Sheet 33 of 59

For NUVOTON TPM



Compal Electronics, Inc.

Title: USH & TPM

Size | Document Number: LA-E122P | Rev: 1.0

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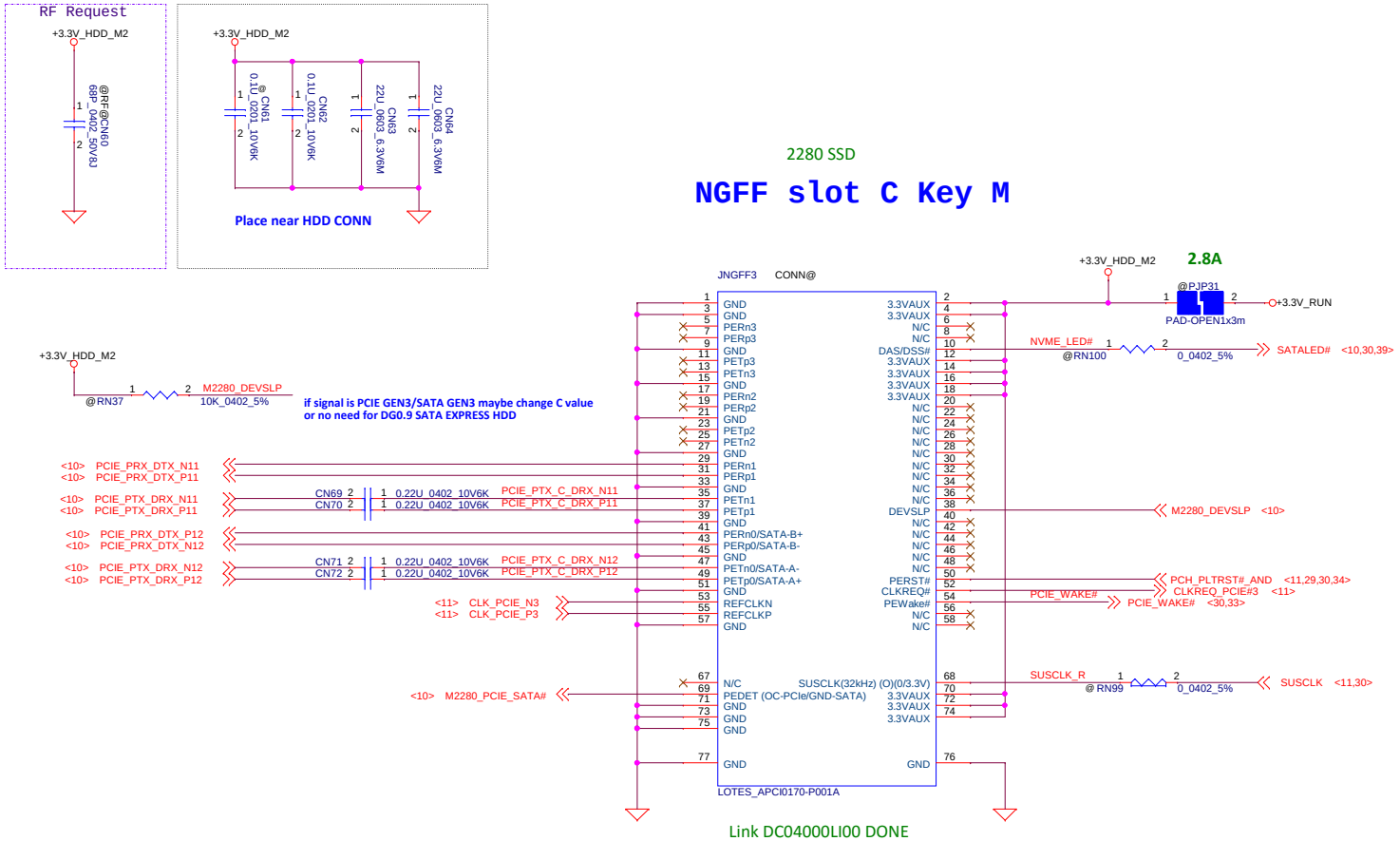
For Brekenridge 12/14/15 UMA/Steamboat

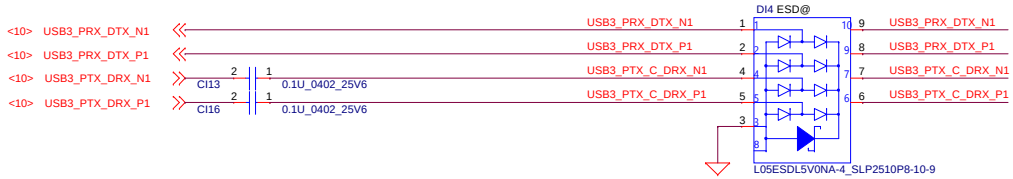


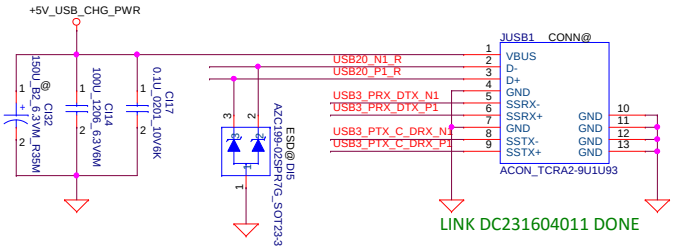
Compal Electronics, Inc.

Title: M2 2280 Socket

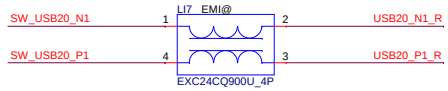
Size | Document Number: LA-E122P | Rev: 1.0

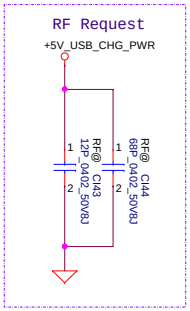
Date: Wednesday, November 09, 2016 | Sheet 35 of 59

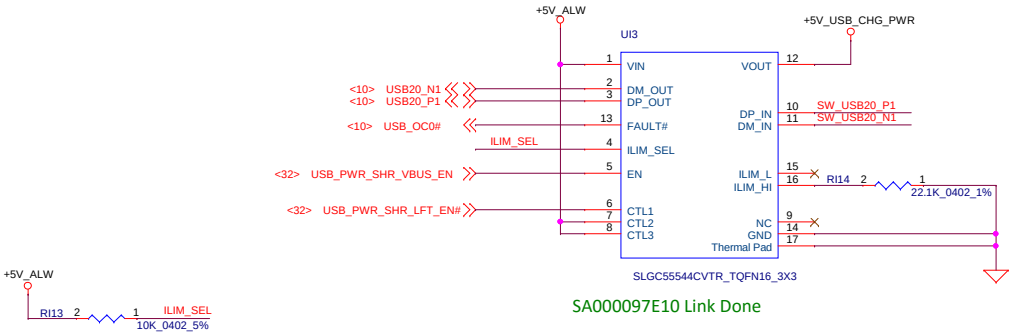




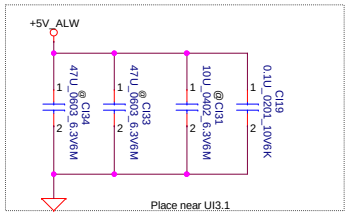
LINK DC231604011 DONE







SA000097E10 Link Done



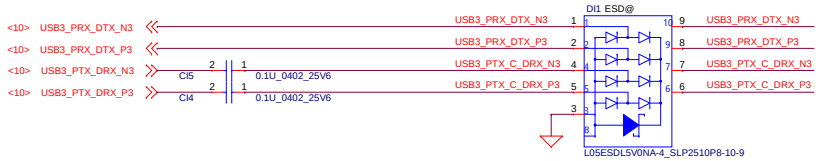
Compal Electronics, Inc.

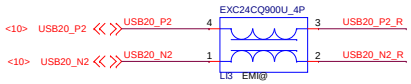
Title: JUSB1+PS

Size | Document Number: LA-E122P | Rev: 1.0

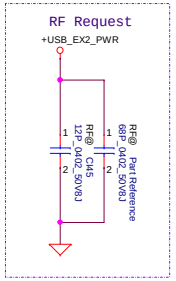
Date: Wednesday, November 09, 2016 | Sheet 36 of 59

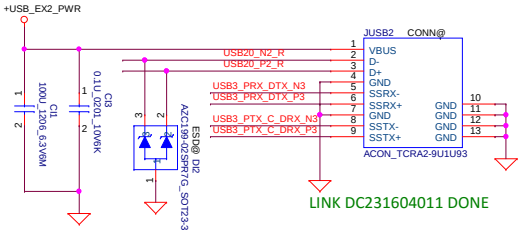
For Breckenridge/Steamboat 12&Kirkwood



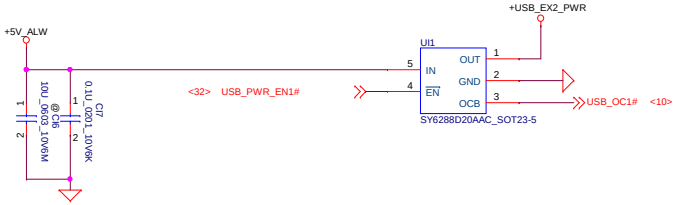


DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm





LINK DC231604011 DONE



Compal Electronics, Inc.

Title: JUSB2

Size | Document Number: LA-E122P | Rev: 1.0

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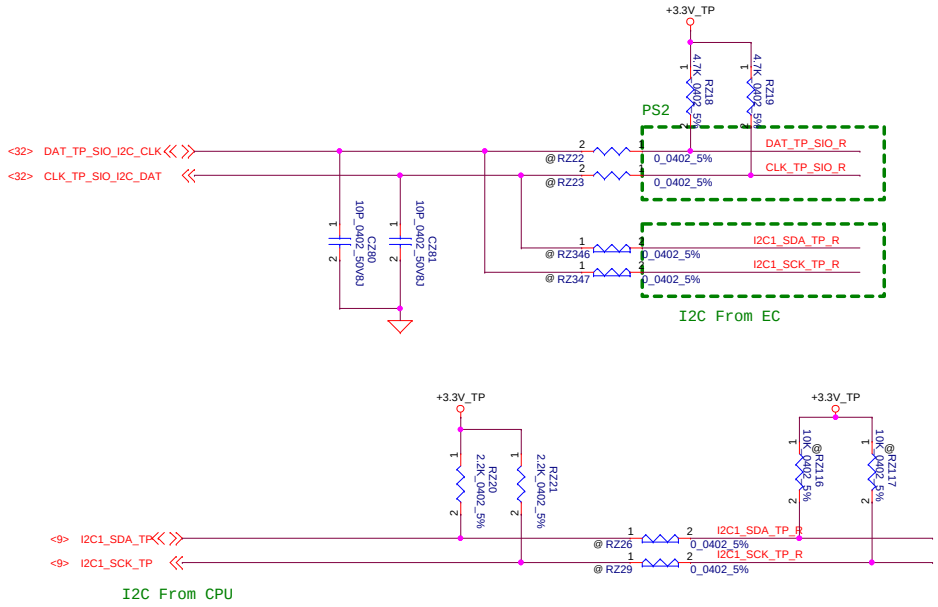
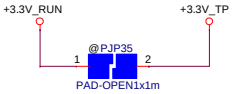
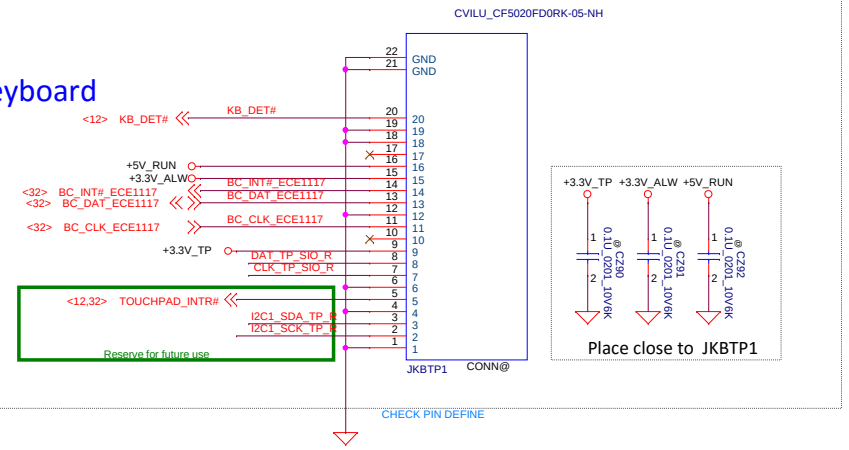
Touch Pad



Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



Keyboard



@EDP Cable nonTS_HD/FHD-HD Cam

Part Number	Description
DC02C00E000	H-CONN SET 1S5 MB-LCD-CAMERA NTS FHD

@EDP Cable nonTS_FHD-IR

Part Number	Description
DC02C00E100	H-CONN SET 1S5 MB-LCD-CAMERA-IR NTS FHD

@EDP Cable TS_TS-FHD-HD Cam

Part Number	Description
DC02C00E200	H-CONN SET 1S5 MB-LCD-CAMERA-TS FHD

@LED Cable

Part Number	Description
DC02002LT00	H-CONN SET 1S5 MB-LED/B

@FP FFC

Part Number	Description
NBX00023000	FFC 12P F P0.5 PAD=0.3 56MM MB-FP 1S5

@TP FFC

Part Number	Description
NBX00022Y00	FFC 20P F P0.5 PAD=0.3 92MM MB-TP 1S5

@USH Board FFC

Part Number	Description
NBX00022Z00	FFC 26P F P0.5 PAD=0.3 81.6MM MB-USH 1S5

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

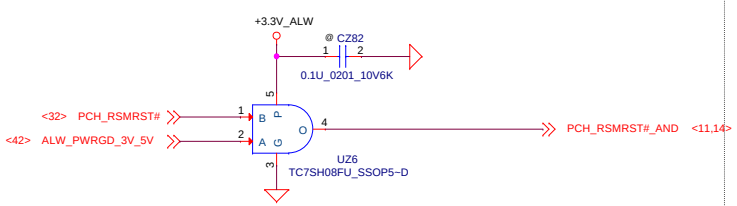
@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

RSMRST circuit



Compal Electronics, Inc.

Title: Keyboard

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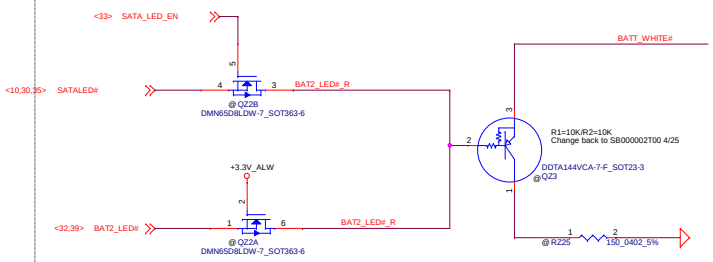
HDD LED MUX

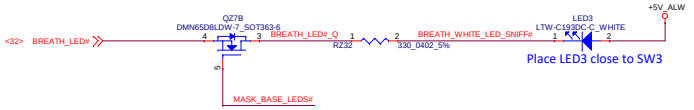
means EC can switch battery white led and HDD LED by hot key "Fn+H"

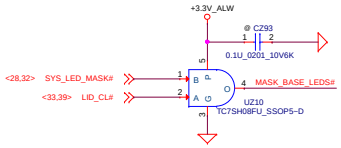


Battery LED

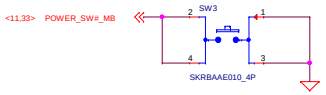
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

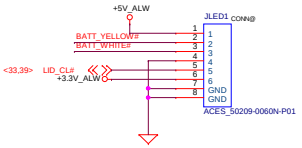




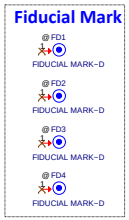
POWER & INSTANT ON SWITCH



LED board CONN

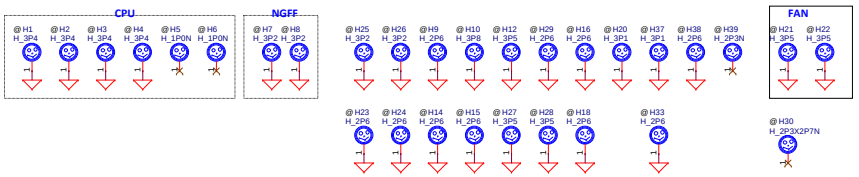


Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



Compal Electronics, Inc.

Title: PAD, LED

Size: | Document Number: LA-E122P | Rev: 1.0

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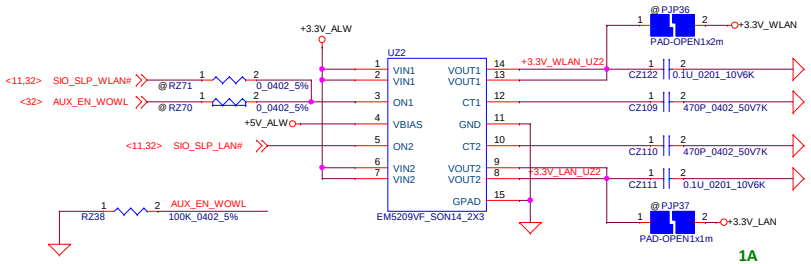
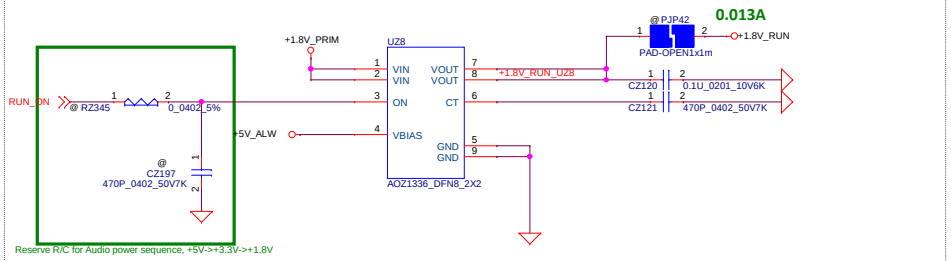
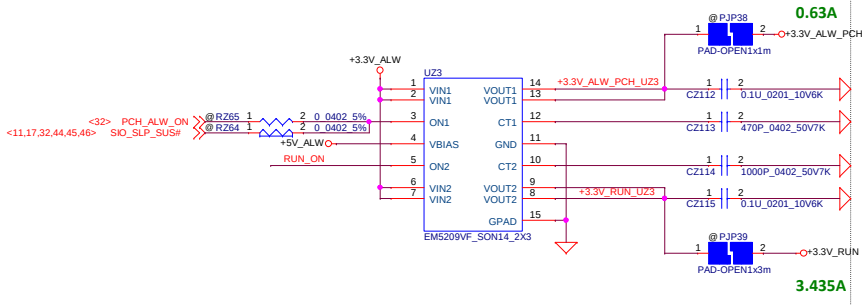
+3.3V_WLAN/+3.3V_LAN source



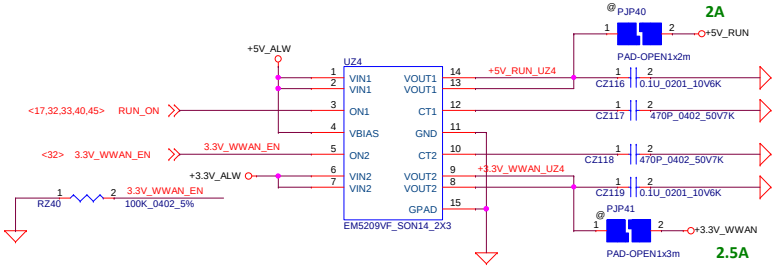
+1.8V_RUN source

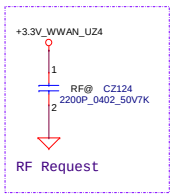


+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source



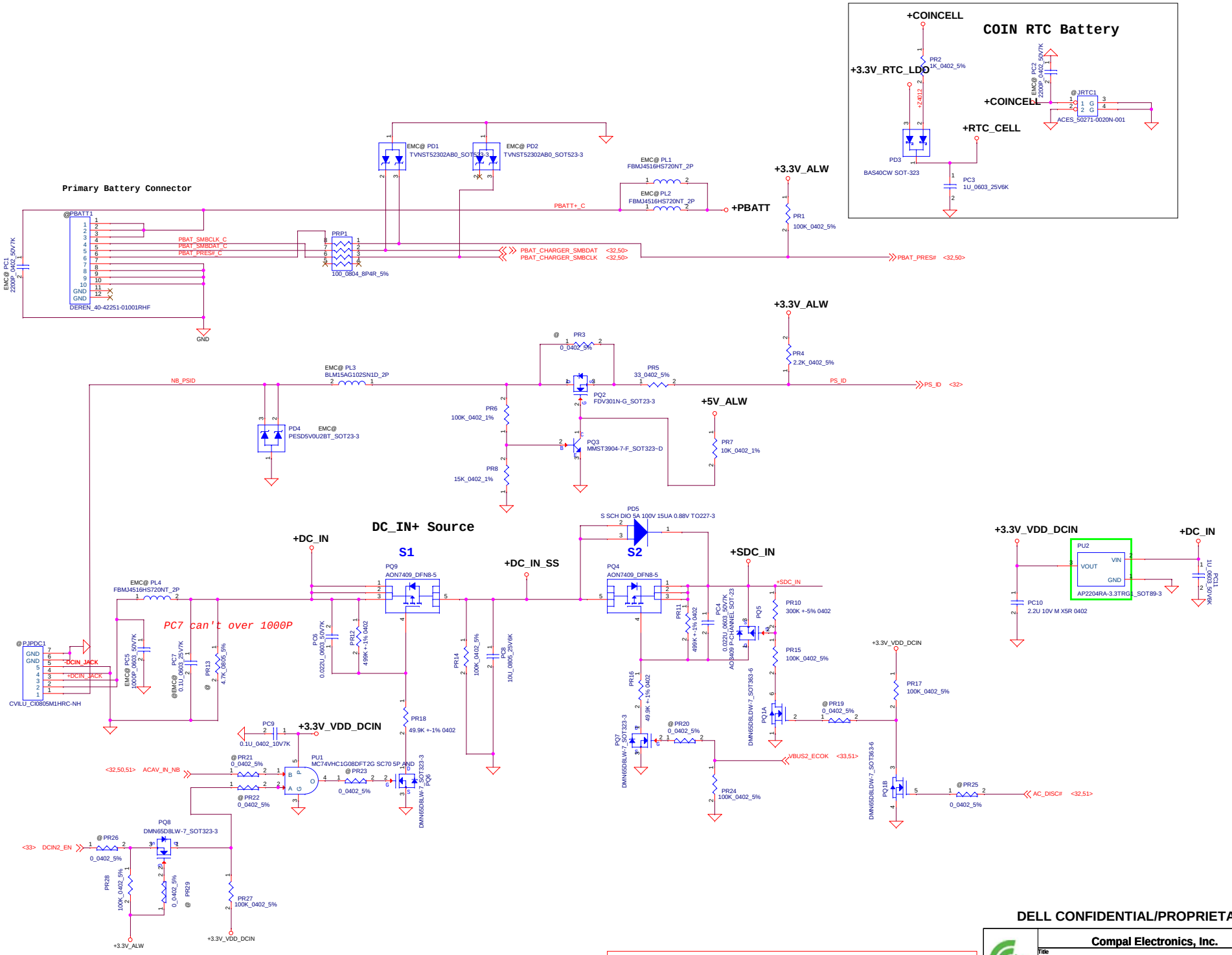


Compal Electronics, Inc.

Title: Power control

Size | Document Number: LA-E122P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 40 of 59



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	+DCIN
Size	Document Number: LA-E121P
Rev	1.0
Date:	Wednesday, November 09, 2016
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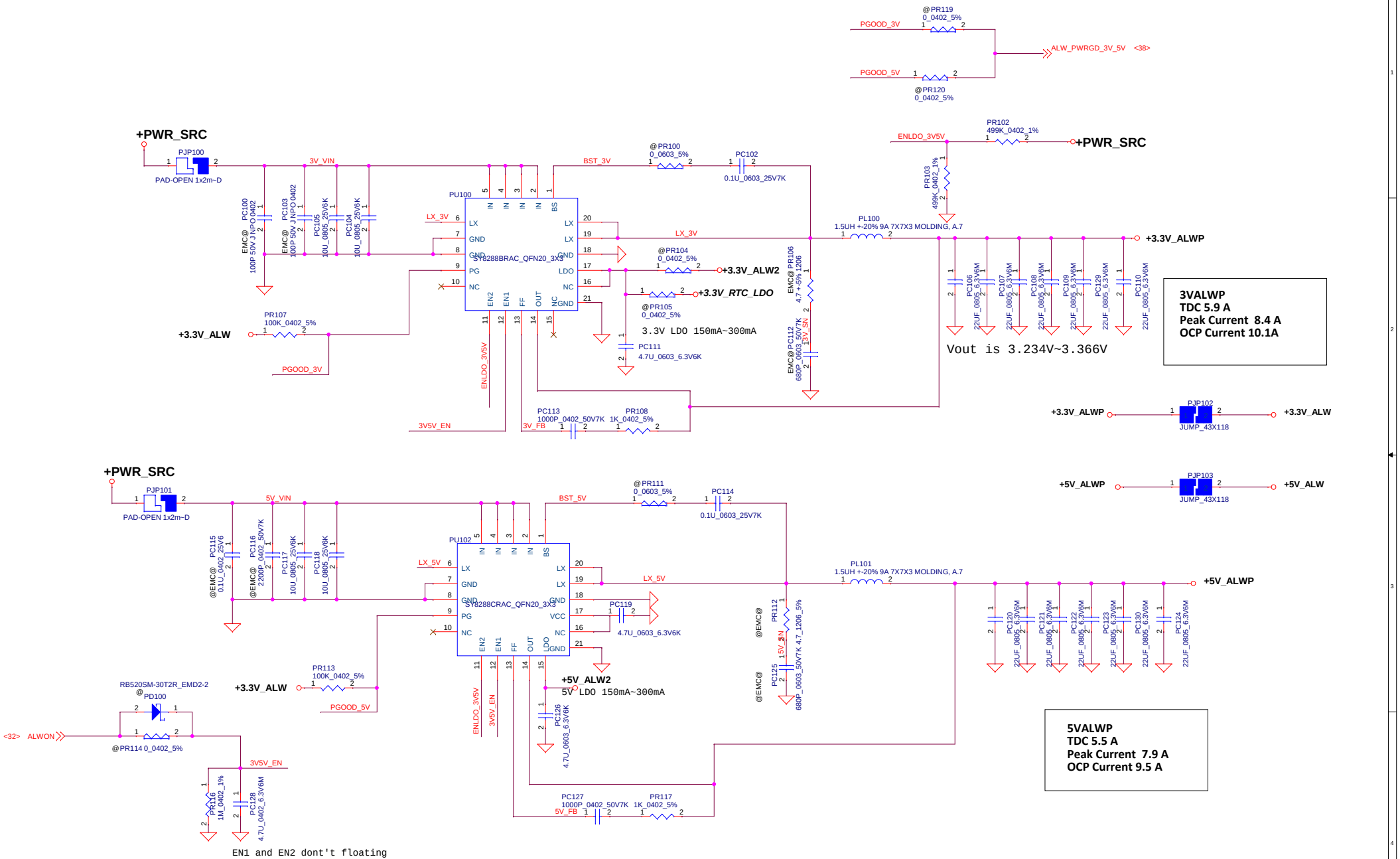
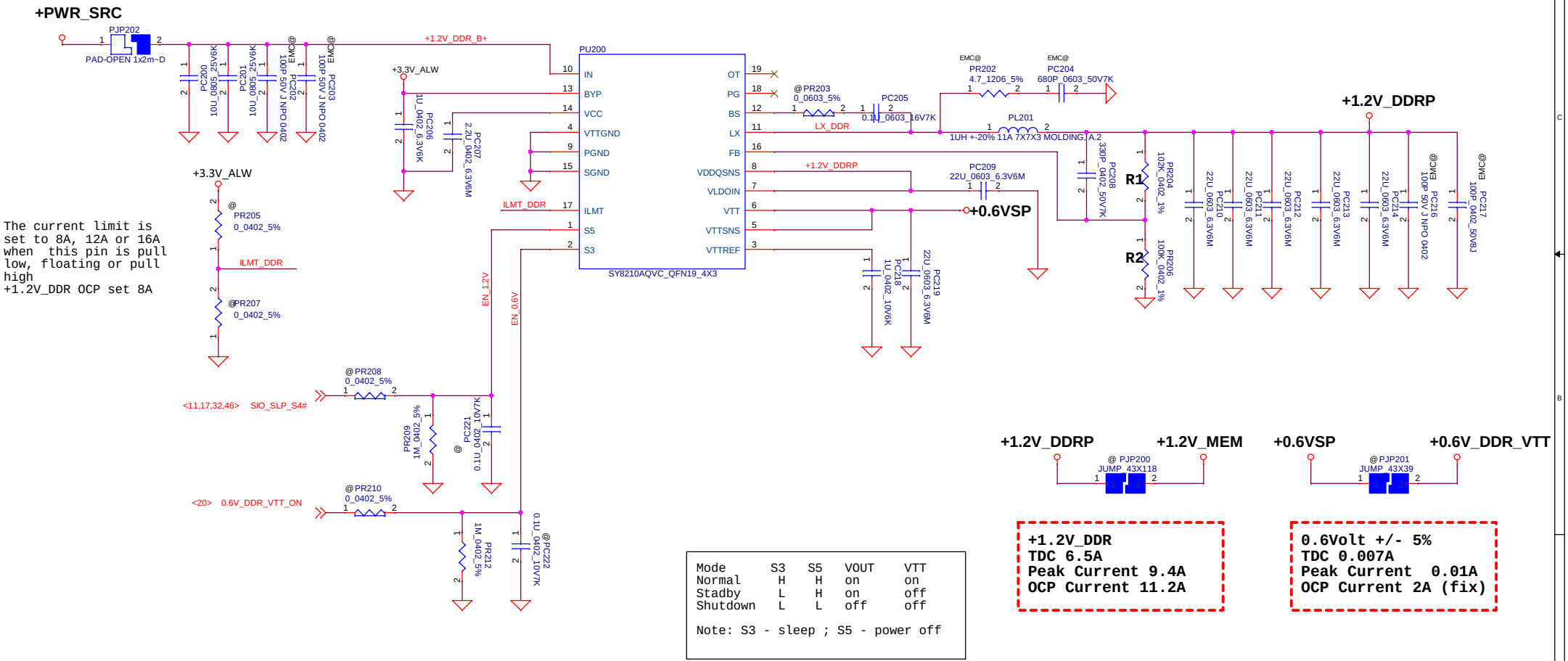


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: +5V_ALW/3.3V_ALW		
Size	Document Number: LA-E121P	Rev: 1.0
Date: Wednesday, November 09, 2016	Sheet 42 of 59	



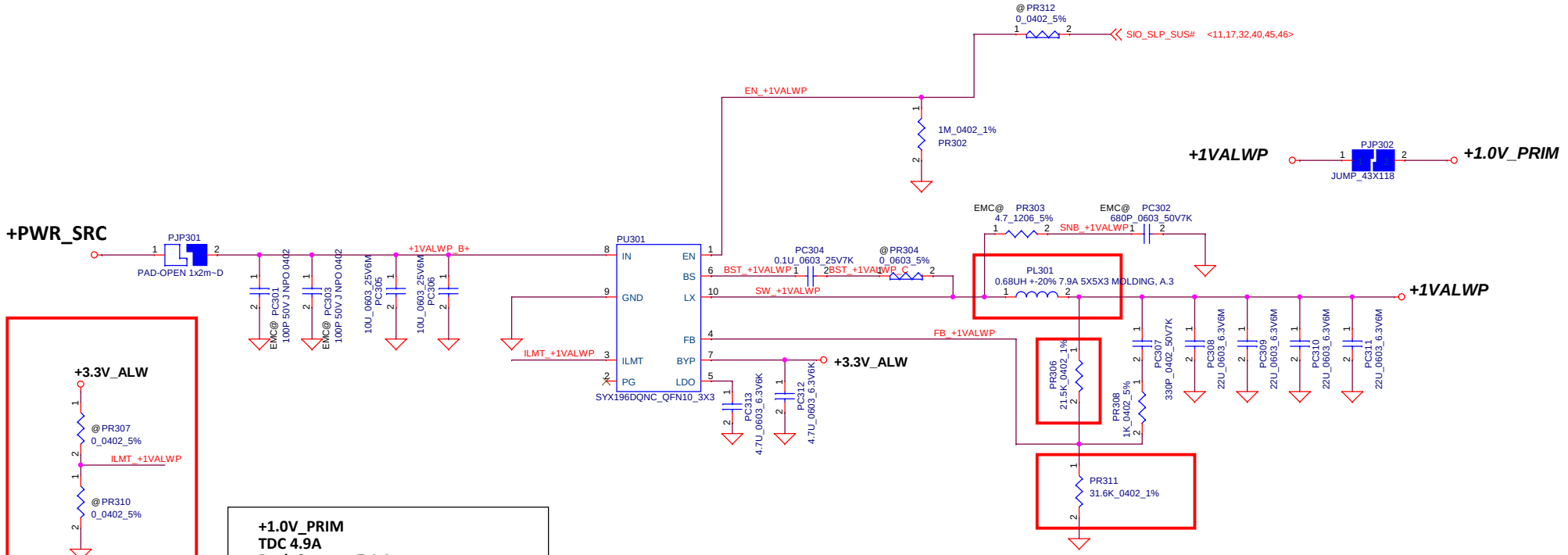
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

Size | Document Number: LA-E121P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 43 of 59



+1.0V_PRIM
TDC 4.9A
Peak Current 7.1 A
OCP Current 8.6A

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

Compal Electronics, Inc.

Title	+1VALWP	
Size	Document Number: LA-E121P	Rev: 1.0
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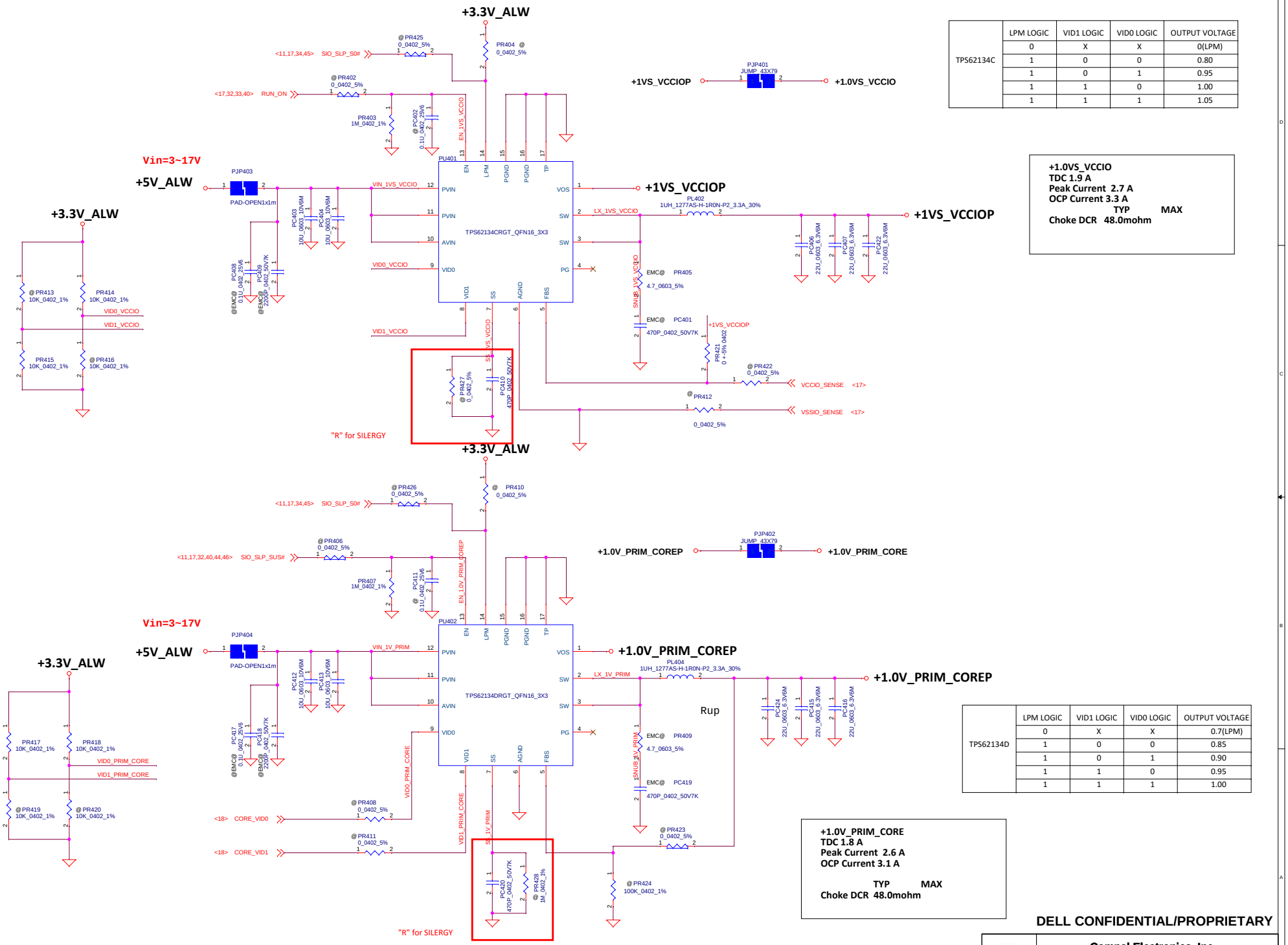

TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A

	TYP	MAX
Choke DCR	48.0mohm	

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A

	TYP	MAX
Choke DCR	48.0mohm	

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title	+1VS_VCCIOP/+1.0V_PRIM_COREP	
Size	Document Number: LA-E121P	Rev: 1.0
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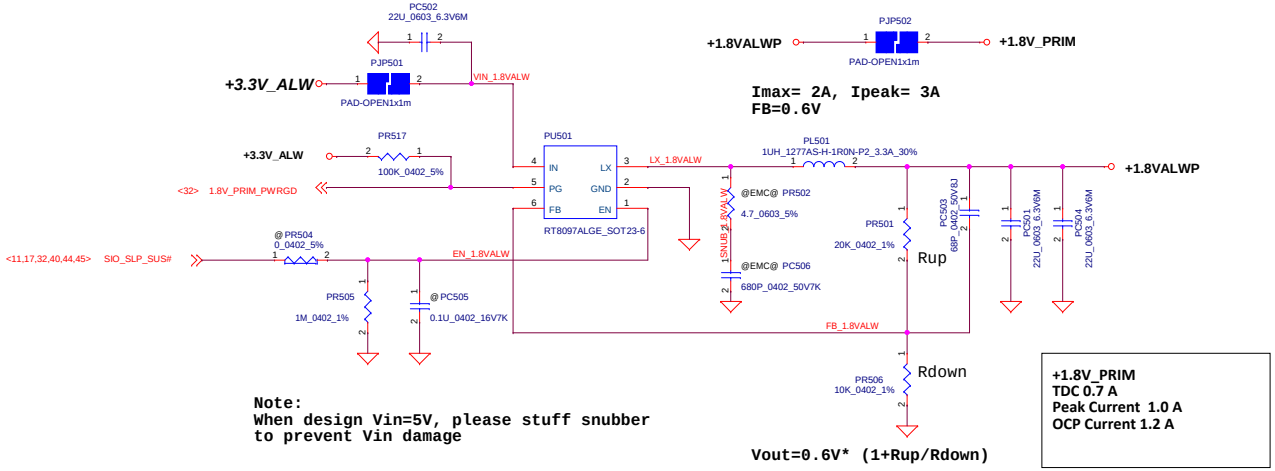

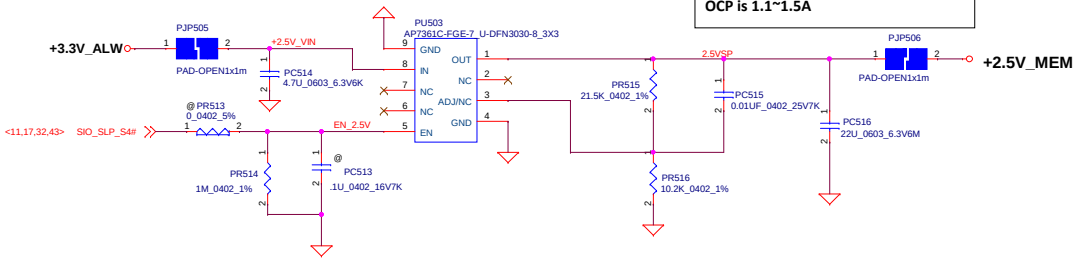

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Title: +1.8VALWP/+1.5VSP

Size | Document Number: LA-E121P | Rev: 1.0

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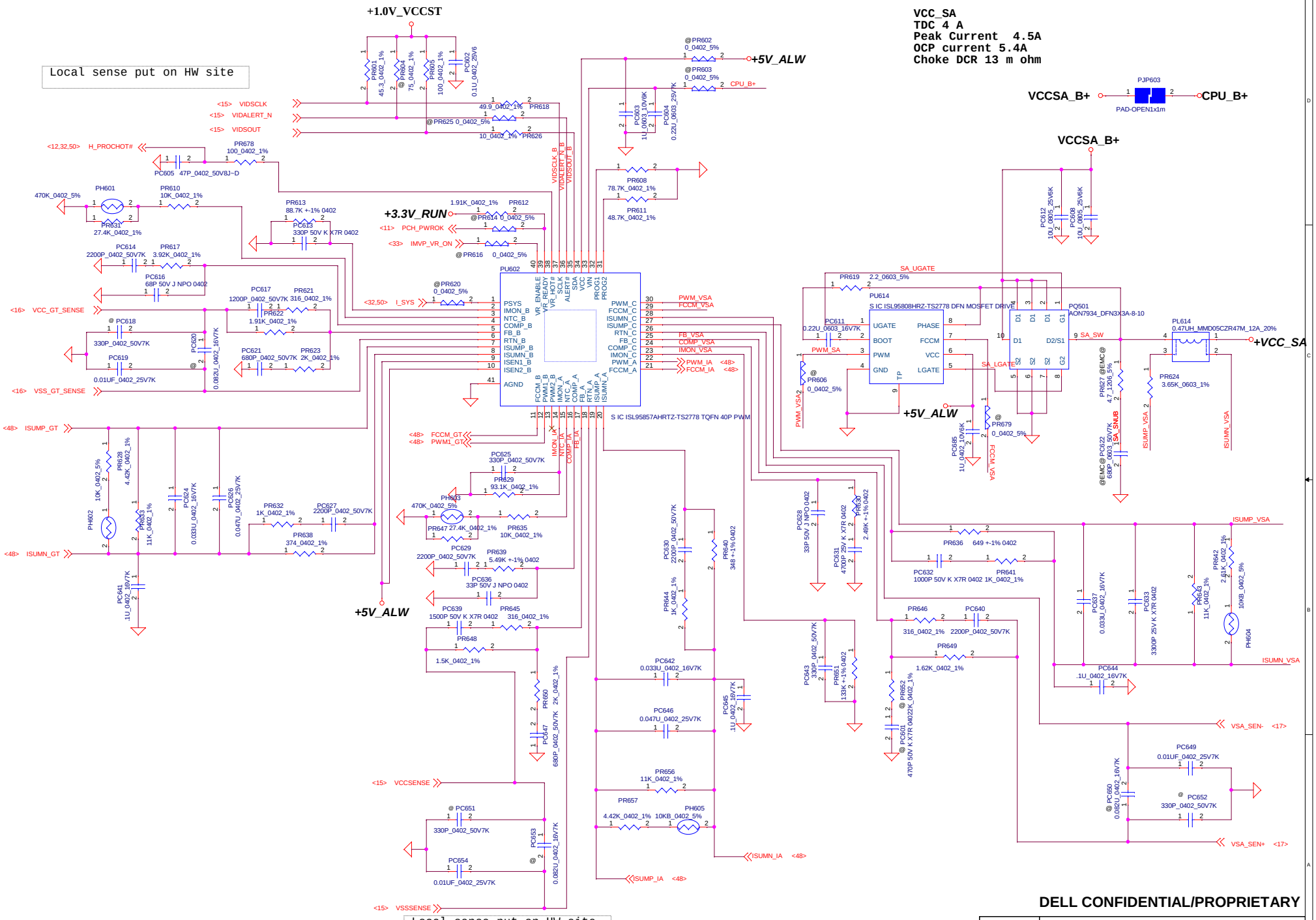
+1.0V_VCCST
Local sense put on HW site
VCC_SA
TDC 4 A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm
VCCSA_B+
CPU_B+
PJP603
PAD-OPEN1x1m
+5V_ALW
+3.3V_RUN
PU602
S IC ISL95857AHRTZ-TS2778 TQFN 40P PWM
PU614
S IC ISL95808HRZ-TS2778 DFN MOSFET DRIVE
PQ501
AON7934_DFN3X3A-8-10
+VCC_SA
Local sense put on HW site
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PWR_VCORE_ISL95857
LA-E121P
Rev 1.0
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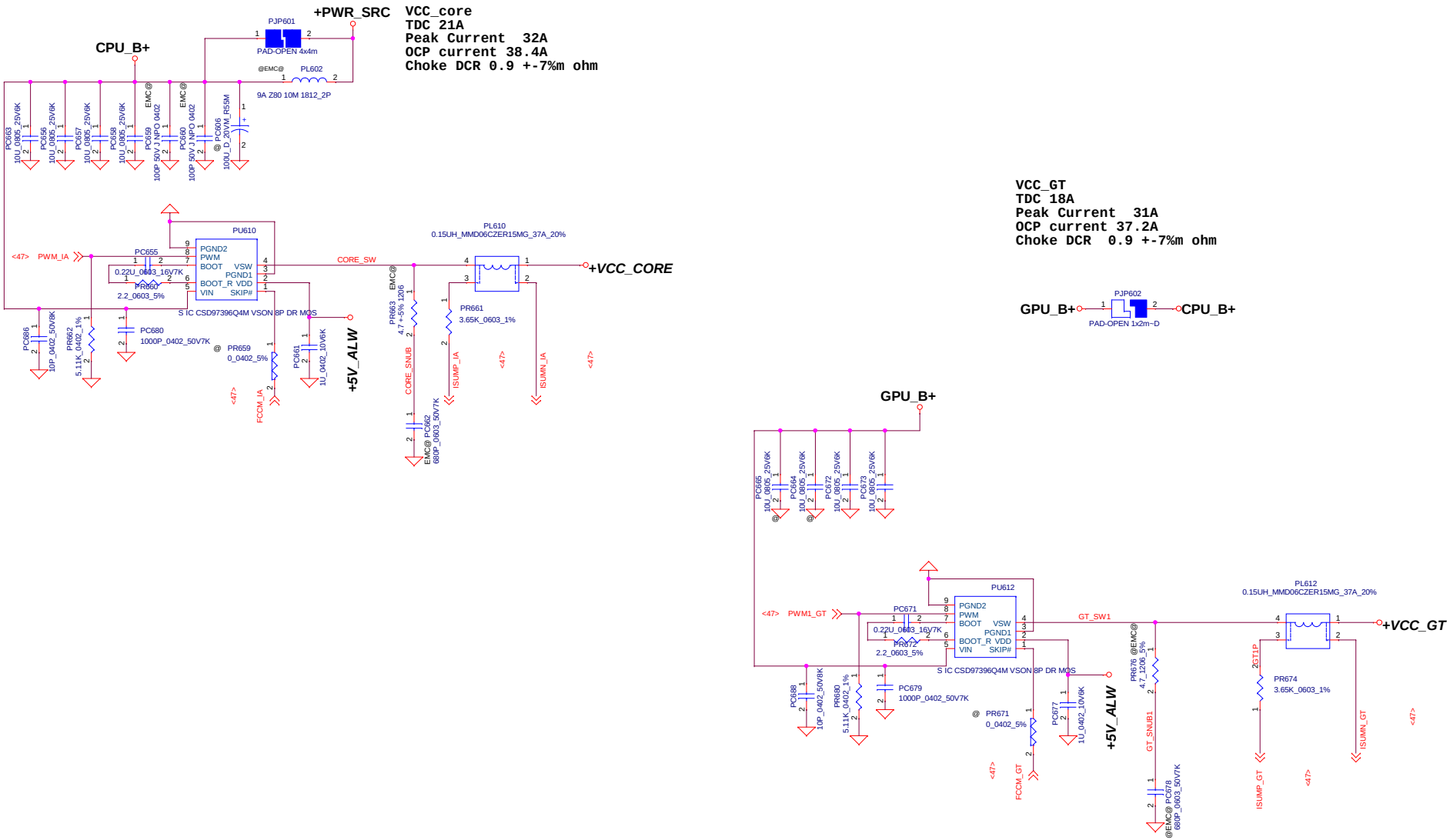

Compal Electronics, Inc.

Title: PWR_VCORE_ISL95857

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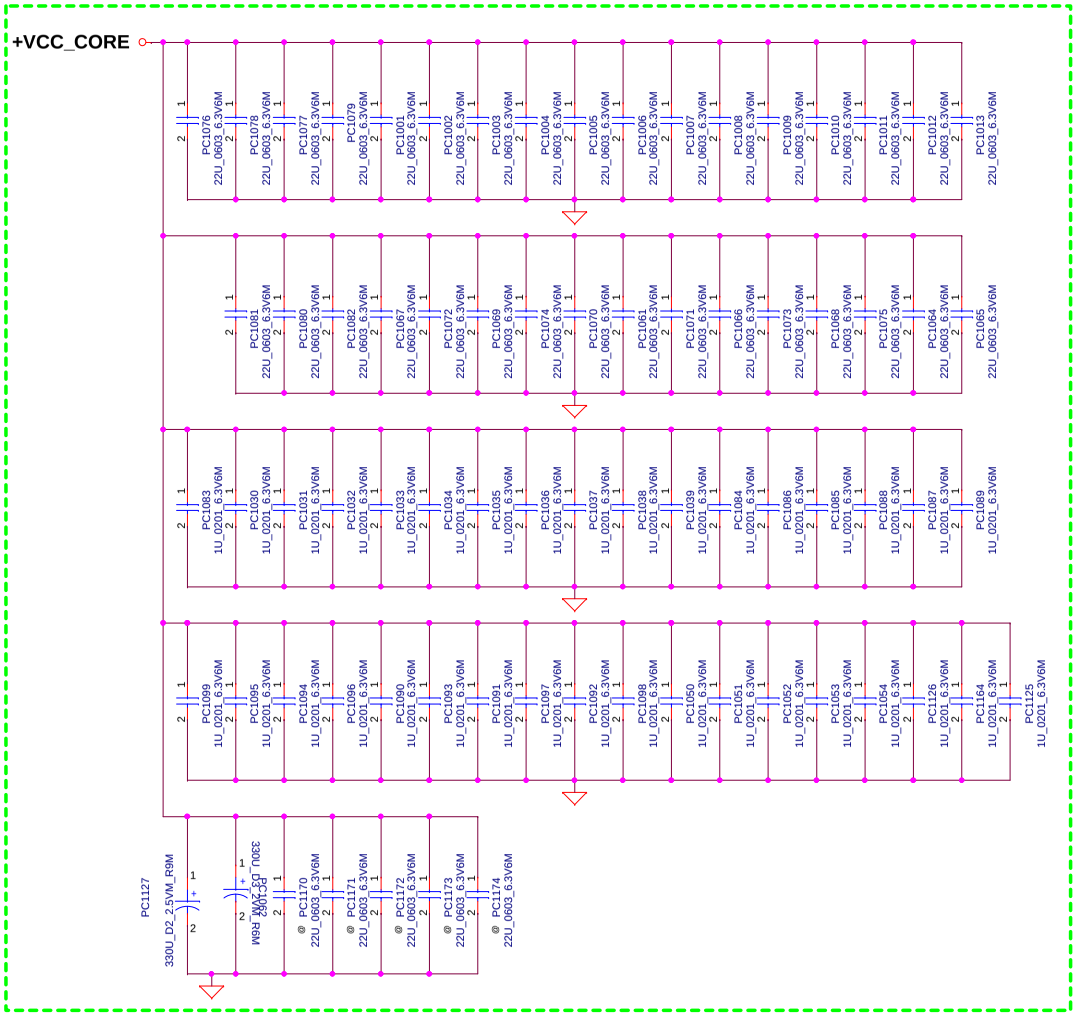
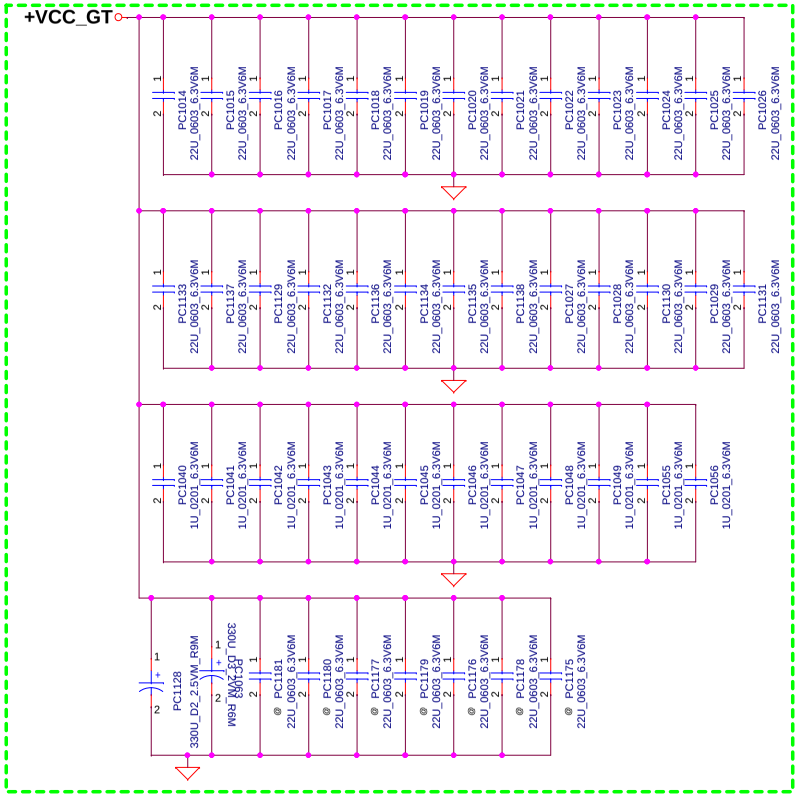
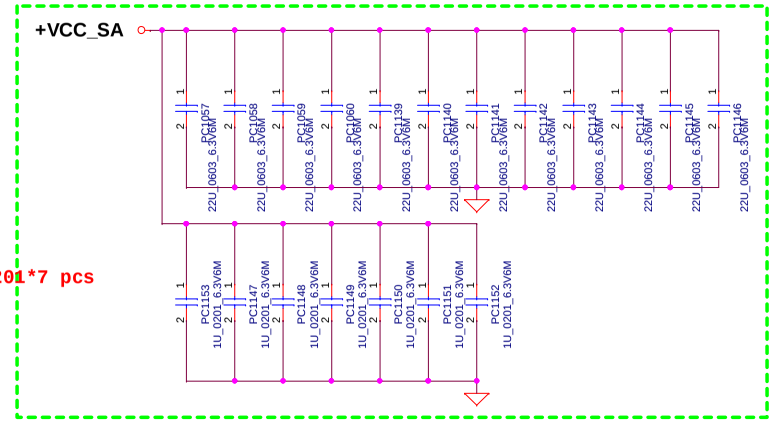
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs



VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs



VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs



DELL CONFIDENTIAL/PROPRIETARY

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Title: PROCESSOR DECOUPLING

Size | Document Number: LA-E121P | Rev: 1.0

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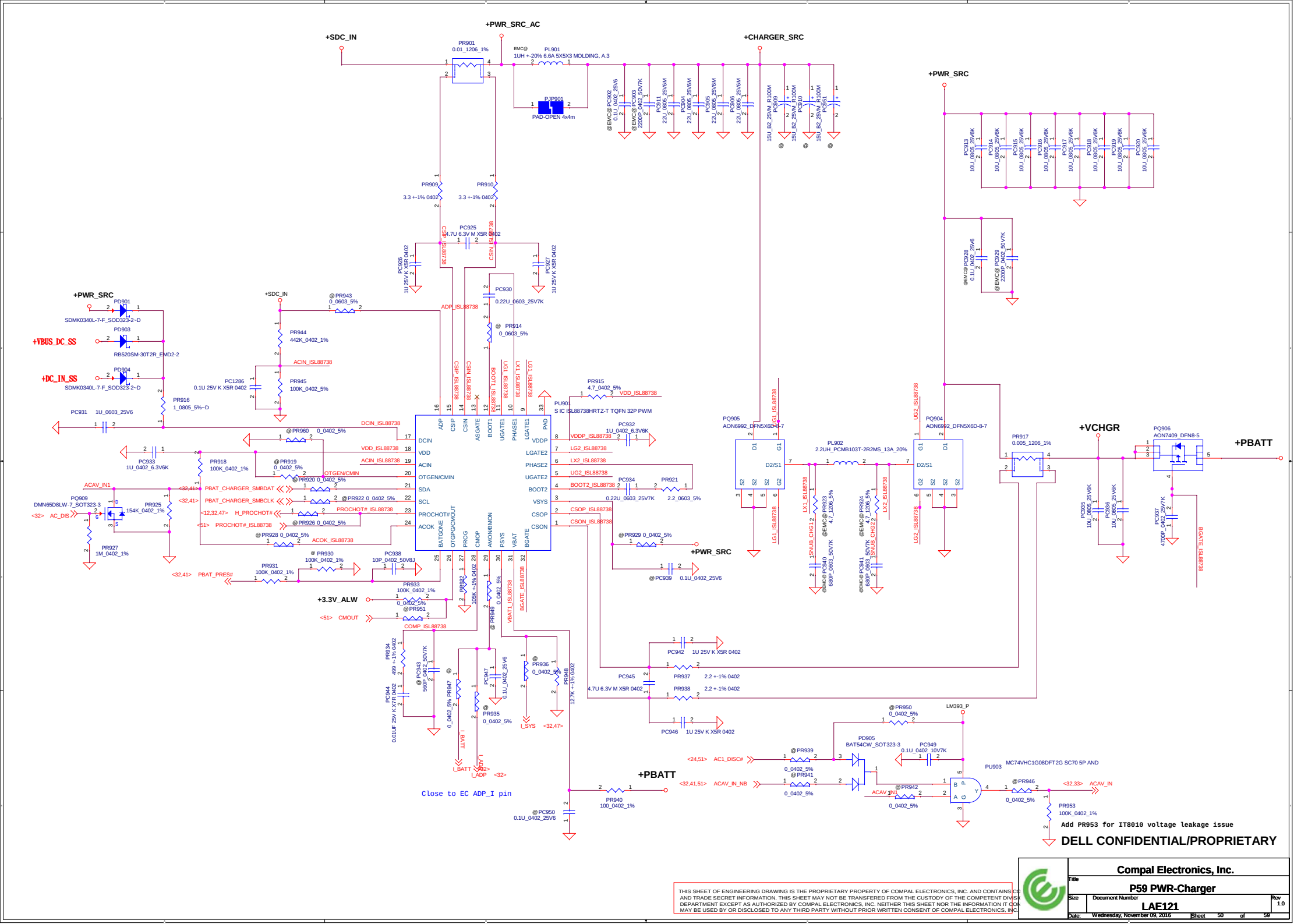
+SDC_IN
+PWR_SRC_AC
+CHARGER_SRC
+PWR_SRC
+VBUS_DC_SS
+DC_IN_SS
+3.3V_ALW
+PBATT
+VCHGR
PU901
S IC ISL88738HRTZ-T TQFN 32P PWM
PU903
MC74VHC1G08DFT2G SC70 5P AND
PD905
BAT54CW_SOT323-3
LM393_P
PL901
1UH +-20% 6.6A 5X5X3 MOLDING, A.3
PL902
2.2UH_PCMB103T-2R2MS_13A_20%
PJP901
PAD-OPEN 4x4m
Close to EC ADP_I pin
Add PR953 for IT8010 voltage leakage issue
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Compal Electronics, Inc.
P59 PWR-Charger
LAE121
Wednesday, November 09, 2016
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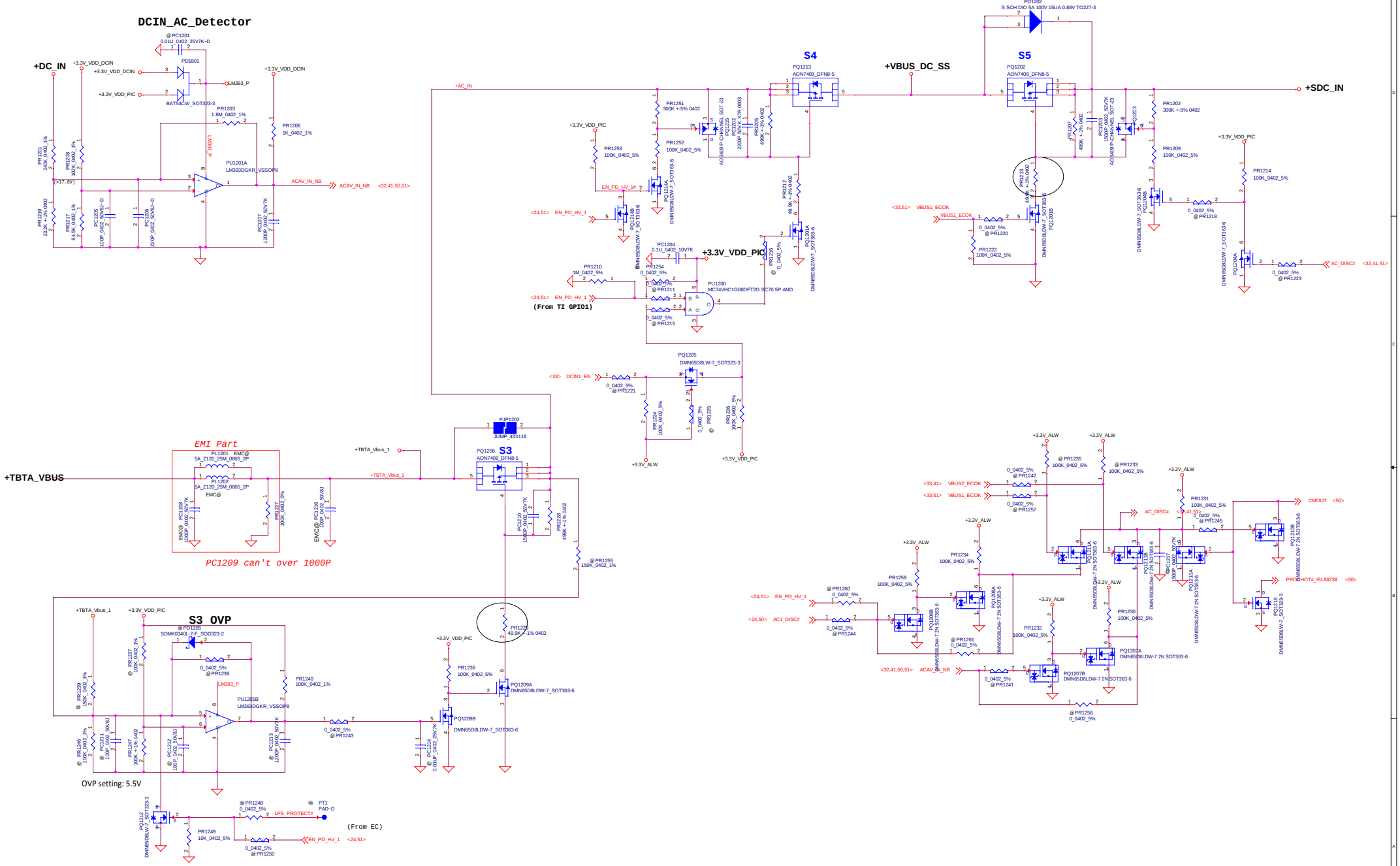

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	Change CPU VR version	2016 05/24	Compal	change solution version to fix PS4 funciton issue	change ISL95857HRTZ to ISL95857AHRTZ	X01
2	59 60	CHARGER 1Type-C PD Selector	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Charger: Add PR960 and depop PR919 let the PU901.20 CMIN connect to GND, add 1 net PROCHOT#_ISL88738 TypeC: Add PQ1216 to drive the PROCHOT# and PC1217 to do the reserve.	X01
3	60	Change the S4 fast turn off circuit to avoid the leakage	2016 05/30	Compal	Change the S4 fast turn off circuit to avoid the leakage	Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN	X01
4	60	Fine tune the DC-IN detect voltage	2016 06/13	Compal	For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V	PR1219 change from 22.6K to 23.2K. SD034232280	X01
5	57	location alignment	2016 06/13	Compal	location alignment	VCCSA change the PU606 to PU614 and PL601 to PL614 IA change the PU603 to PU610 and PL603 to PL610 GT change the PU604 to PU612 and PL604 to PL612	X01
6	59	Decrease the charger input leakage voltage	2016 06/13	Compal	To decrease the charger input leakage voltage for TypeC AC	Change the PD903 from SCS0340L010 to SCS00006C00.	X01
7	56	Regulate VR	2016 06/13	Compal	Regulate VR load line	PR651 change to 124K ohm SD034124380,PR613 change to 88.7k ohm SD034887280, PC601 change to 470pF SE074471K80, PC639 change to 1500pF SE074152K80, PR639 change to 5.49K ohm, SD034549180, PC636 change to 33pF SE071330J80	X01
8	50	MOS leakage problem	2016 06/17	Compal	To solve the MOS leakage problem to avoid the error active	PR12, PR11, PR1205, PR1207 and PR1228 change to 499K from 1M ohm PR16, PR18, PR1212, PR1213 and PR1229 change to 49.9K from 1M ohm PR10, PR1251 and PR1202 change to 300K from 100K ohm.	X02
9	60	Reserve the OVP function	2016 07/01	Compal	Reserve the OVP function to protect the typeC device	Depop PJP1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212, PD1205, PC1213, PC1214 and PR1248 Change the PR1247 from 200K_0402_1% to 100K_0402_5% ohm Re-modify the S11 OVP description to S3 OVP.	X02
10	50	MOS leakage problem	2016 07/01	Compal	To solve the MOS leakage problem to avoid the error active	PR10 change to 300K from 100K ohm	X02
11	59	Change Charger version	2016 07/02	Compal	Charger IC update version	Change the charger solution version to SA00009VW20	X02
12	59	Change Charger version	2016 07/14	Compal	Charger IC update version	Change the PC926, PC927, PC942 and PC946 from @ to 1uF/0402 Change the PC925 and PC945 from 1uF to 4.7uF/0402 Change the PR909 and PR910 from 1 Ohm to 3.3 Ohm. Change the PC944 from 47nF to 10nF. Change the PR934 from 0 Ohm to 499 Ohm Change PR932 from 118K to 105K	X02
13	59	Change Charger version	2016 07/19	Compal	Charger IC update version	Connect PD901 to PWR_SRC the charger output Add PC937	X02
14	59	Change Charger version	2016 08/11	Compal	Charger IC update version	Add PC1286 (CAP 0.1U 25V K X5R 0402)	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	56	SA OVP	2016 08/30	Compal	SA OVP when C status change	1.Change PC633 to 3300P 2.Change PR630 to 2.49K 3.Change PC628 to 33P 4.Change PC632 to 1000P 5.Change PC631 to 4700P 6.Remove PC601 7.Remove PR652 8.Change PL614 to SH000015M00, (S COIL .47UH) 9. Change PR636 to 649 10. Change PR651 to 133K	X03
16	54	Enable LPM mode	2016 08/30	Compal	Enable low power mode	1. Remove PR410 2. Add PR426	X03
17	59	For IT8010 voltage leakage issue	2016 09/02	Compal	Add PR953 for IT8010 voltage leakage issue	Add PR953 100K	X03
18	60	Modify symbol to 2nd source	2016 09/08	Compal	Modify PD1202,PD5 to 2nd source because vendor EOL	Modify PD1202,PD5 to 2nd source(SCS00005X00) because vendor EOL	X03
19	57	RF request	2016 09/08	Compal	RF need to add BOM in SB	Add snubber and D-cap capacitance 1.PC659/PC660 need add 100pf 2.PR663 need add 4.7//PC662 need add 680pf	X03
20	52	RF request	2016 09/08	Compal	RF need to add BOM in SB	Add snubber and D-cap capacitance 1.PC202/PC203/PC216/PC217 need add 100pf 2.PR202 need add 4.7//PC204 need add 680pf	X03
21	51	RF request	2016 09/08	Compal	RF need to add BOM in SB	Add snubber and D-cap capacitance 1.PC100/PC103 need add 100pf 2.PR106 need add 4.7//PC112 need add 680pf	X03
22	53	RF request	2016 09/08	Compal	RF need to add BOM in SB	Add snubber and D-cap capacitance 1.PC301/PC303 need add 100pf 2.PR303 need add 4.7//PC302 need add 680pf	X03
23	59	For EMI request	2016 09/08	Compal	EMI need to add PL901 in SB	Add PL901	X03
24	56	Fine tune for IC register	2016 09/29	Compal	Fine tune for IC register	PR640 Change 348	X03
25	59	PWR_CHARGER	2016 10/03	Compal	Pmax change need to modify Rpsys	Change PR948 to 13.3K	X03
26	54	For Max Power 125W	2016 10/04	Compal	Because Pmax change , so modify Rpsys	1. VCCIO use local sense: PR421 change to 0 ohm, de-pop PR422,PR412 2. VCCIO change to 0.95V: De-pop PR413,PR416, pop PR415,PR414	X03
27	51	+5V voltage droop	2016 10/04	Compal	5V_ALW toType-C connector exist voltage droop problem, need add a resistor on fb net	Add PR121 in 5V ALW fb	X03

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
28	50	BOM change to common P/N.	2016 10/21	Compal	Change PD1202,PD5 to common P/N.	PD1202,PD5 Change to : SCS00009T00 - S SCH DIO 5A 100V 15UA 0.88V TO227-3	A00

Version Change List (P. I. R. List) LA-E122P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	24	[Type C]PD Controller TI	2016/05/23	EE	UT5.D6 need to PD for TI suggestion	Pop RT101	0.2(X01)
2	23	DP/USB3 Repeater SW TUSB546	2016/05/23	EE	TI TUSB546 sample change to ES3	Chagne UT9 from SA00009R700 to SA00009R710	0.2(X01)
3	24	[Type C]PD Controller TI	2016/05/23	EE	Schematic align	Add net name UT5.B2 : MUX1_FLIP_SEL_R UT5.C2 : EN_PD_HV_1_R UT5.D10 : PD1_GPIO2 UT5.G11 : AC1_DISC#_R UT5.C10 : SW2_DP1_HPD_R UT5.E10 : OTG_ID UT5.G10 : PD1_GPIO6 UT5.D7 : PD1_GPIO7	0.2(X01)
4	25	[Type C]PD Power	2016/05/23	EE	TypeC PD solution (dead battery mode)	RT111 change from 10K to 100K (SD028100380) CT90 change from 100P to 1U (SE00000QL10)	0.2(X01)
5	31	Codec ALC3246	2016/05/23	EMI	EMI request	CA2/CA3 change from 2200P to 330P (SE000006I80)	0.2(X01)
6	23	DP/USB3 Repeater SW TUSB546	2016/05/23	EE	DP_AUX go through PD ,not TUSB546	Depop RT132, RT133, CT115, CT116	0.2(X01)
7	24	[Type C]PD Controller TI	2016/05/23	EE	DP_AUX go through PD ,not TUSB546	Pop RT108, RT109, CT80, CT81	0.2(X01)
8	39	PAD, LED	2016/05/23	EE	Remove HDD LED MUX feature	Add RZ361 and depop QZ3, QZ2, RZ25	0.2(X01)
9	23	DP/USB3 Repeater SW TUSB546	2016/05/23	EE	Disable AUX snoop feature	Pop RT308	0.2(X01)
10	32	EC MEC5105	2016/05/23	EE	Schematic align	Add net VCI_IN1# and add PU RE507 Add net VCI_IN2# and add PU RE508	0.2(X01)
11	33	EC MEC5105	2016/05/23	EE	Schematic align for SB12 only	Add net USB_PWR_EN2# and PU RPE11.4	0.2(X01)
12	10	CPU (5/14)	2016/05/23	EE	Schematic align for SB12 only	Add net USB_OC2# and PU RPC3.1	0.2(X01)
13	34	USH & TPM	2016/05/23	EE	Atmel request for current TPM silicon	Add CZ74 (pop) and RZ72(depop) for UZ12.7	0.2(X01)
14	9	CPU (4/14)	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Add net MEDIACARD_IRQ# to UC1.AN8	0.2(X01)
15	29	Card Reader	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Cardreader schematic change from RTS5330 (USB) to RTS5242 (PCIE)	0.2(X01)
16	10	CPU (5/14)	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Change net from USB3.0 port 5 to PCIE port1 Delete USB2.0 port 6	0.2(X01)
17	10	CPU (5/14)	2016/05/23	EE	No support M.2 3042 (HCA), but keep SATA cache for nonAR config	Change net from PCIE port 10 to SATA port1	0.2(X01)
18	11	CPU (6/14)	2016/05/23	EE	No support M.2 3042 (HCA), but keep SATA cache for nonAR config	Assign CLKREQ_PCIE#0 to Cardreader	0.2(X01)
19	30	NGFF Card	2016/05/23	EE	No support M.2 3042 (HCA), but keep SATA cache for nonAR config	Change net from PCIE port 10 to SATA port1	0.2(X01)
20	35	M2 2280 Socket	2016/05/23	EE	Remove HDD LED MUX feature	Depop RN100	0.2(X01)
21	30	NGFF Card	2016/05/23	EE	Remove HDD LED MUX feature	Depop RN101	0.2(X01)
22	32	EC MEC5105	2016/05/23	EE	PORT80_DET#	Change location RE510 to RE512 Reserve RE513 100k (SD028100380) to GND	0.2(X01)

Version Change List (P. I. R. List) LA-E122P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	6	CPU (1/14)	2016/05/23	EE	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182 Add test point T281/T282 for CPU_DP1_AUXN and CPU_DP1_AUXP	0.2(X01)
24	17	CPU (12/14)	2016/05/23	EE	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
25	32	EC MEC5105	2016/05/24	EE	Schematic align	Delete RE506 and reserve PD 100K RE95 for TBT_RESET_N_EC_R	0.2(X01)
26	39	PAD, LED	2016/05/24	ME	MB ME drawing change	H20/H37 change to H_3P1, H10 change to H_3P8, H26 change to H_3P2	0.2(X01)
27	32	EC MEC5105	2016/05/25	EE	Symbol pin name change	UE1.C1 pin name change to GPIO024_nRESETI	0.2(X01)
28	24	[Type C]PD Controller TI	2016/05/25	EE	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)
29	23	DP/USB3 Repeater SW TUSB546	2016/05/25	EE	Symbol pin name change	UT9.29 pin name change to SNK_CAD/DCI_DAT UT9.32 pin name change to HPDIN/DCI_CLK	0.2(X01)
30	34 38	USH & TPM Keyboard	2016/05/25	ME	Connector update	JUSH1 change to LTCX007Q600 JKBTP1 change to LTCX007Q500	0.2(X01)
31	6	CPU (1/14)	2016/05/31	EE	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
32	23	DP/USB3 Repeater SW TUSB546	2016/05/31	EE	Schematic align	SW2_DP1_HPD Add RT380 place near TUSB546	0.2(X01)
33	39	PAD, LED	2016/05/31	ME	MB ME drawing change	Add H39 H_2P3N and change H25 to H_3P2	0.2(X01)
34	30	NGFF Card	2016/06/01	EE	Intel reviwe result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
35	28	LAN Clarkvillie & RJ45	2016/06/01	EE	EMI request	Change CL22 from 1500P to 150P (SE00000FA80)	0.2(X01)
36	31	Codec ALC3246	2016/06/01	EE	Audio EA modify (meet GS mark)	Change RA7, RA8 from 24.9ohm to 16.2ohm (SD00001U900)	0.2(X01)
37	11	CPU (6/14)	2016/06/01	EE	Crystal EA modify	Change CC21, CC22 from 15pf to 12pf	0.2(X01)
38	34	USH & TPM	2016/06/01	EE	TPM change to Nuvoton NPCT650JBAYX	All page	0.2(X01)
39	34	USH & TPM	2016/06/04	EE	Vendor schematic review	UZ12 change to NPCT650JB2YX (SA00008EL70) Add CZ75 4.7uF (SE00000SO00) for +UZ12_TPM	0.2(X01)
40	12	CPU (7/14)	2016/06/04	RF	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
41	30	NGFF Card	2016/06/04	RF	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
42	31	Codec ALC3246	2016/06/04	ESD	ESD request	Change LA10, LA11 to SM01000OZ00	0.2(X01)
43	27	eDP CONN& Touch screen	2016/06/04	EMI	EMI request	Change LV1 to SM01000NY00	0.2(X01)
44	30	NGFF Card	2016/06/06	EE	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
45	34	USH & TPM	2016/06/07	EE	Schematic align	Change loaction RZ90 to RZRZ362	0.2(X01)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
46	34	USH & TPM	2016/06/14	EE	TPM pre-config	Reserve RZ363 ohm for GPIO2 and SIO_SLP_S3#	0.2(X01)
47	23	DP/USB3 Repeater SW TUSB546	2016/06/14	EE	Schematic align	Change net name from MUX1_LP_EN to AUX1_SNOOP_EN#	0.2(X01)
48	12	CPU (7/14)	2016/06/14	RF	RF request	Change CC27 from 22pf to 47pf (SE071470J80)	0.2(X01)
49	21	HDMI CONN	2016/06/14	EMI	EMI request	Change RV33,RV34 to 12nH (SHI0000PJ00) Change RV24,RV25,RV27,RV28,RV30,RV31 (SHI0000QS00) Change RV26,RV29,RV32,RV35 to SHI0000PJ00 to 300ohm (SD028300080)	0.2(X01)
50	20	DDR4	2016/06/14	EE	2nd source align	Change UD1 from SA00007WE00 to SA00007UR00	0.2(X01)
51	23	DP/USB3 Repeater SW TUSB546	2016/06/14	EE	2nd source align	Change LT11 from SM01000MS00 to SM01000MO00	0.2(X01)
52	32	EC MEC5105	2016/07/13	EE	For MEC5105K-D1-TN EC sample	Change UE1 to SA00009GL00 & Depop RE361,Pop RE360,RE362	0.3(X02)
53	34	USH & TPM	2016/07/13	EE	TPM pre-config	Pop RZ363 and depop (@) RZ111,RZ112, RZ113,QZ9	0.3(X02)
54	33	EC MEC5105 Support	2016/07/13	EE	Board ID	Change RE79 to 62Kohm (SD028620280)	0.3(X02)
55	32	EC MEC5105	2016/07/13	EE	GPIO map update	1.UE1.F11 add RTCRST_ON_GPIO122 & reserve RE515@ to QE12.2 2.UE1.B6 change to RTCRST_ON_GPIO141 and add RE514 to QE12.2	0.3(X02)
56	31	Codec ALC3246	2016/07/13	EE	ESD request (2nd source align)	Change LA10, LA11 back to SM01000NA00	0.3(X02)
57	34	USH & TPM	2016/07/13	EE	USH BOM modify	1.RZ10 changed to 100K -Let USH_PWR_STATE# keep low at S5 2.DZ7 depop and pop RZ87 - X8 have no difference JUSH1 pin define with X7	0.3(X02)
58	30	NGFF Card	2016/07/13	EE	Symbol error	Re-link JSIM1 symbol and change SIM_DET to JSIM1.2	0.3(X02)
59	24	[Type C]PD Controller TI	2016/07/13	EE	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
60	33	EC MEC5105 Support	2016/07/13	EE	Vendor schematic review	Add net WRST# to UE2.4 and CE500 1uf (SE000000K80)	0.3(X02)
61	21	HDMI CONN	2016/07/13	EMI	EMI request	1. Change RV24 to LV31, RV25 to LV32, RV27 to LV33, RV28 to LV34, RV30 to LV35, RV31 to LV36 and from SHI0000QS00 to SHI0000QT00 2. Change RV33 to LV37, RV34 to LV38 and from SHI0000PJ00 to SHI00006Q00	0.3(X02)
62	11	CPU (6/14)	2016/07/18	EE	Sync up schematic with AR	Add PU RC190 to CLKREQ_PCIE#5	0.3(X02)
63	39	PAD, LED	2016/07/20	EE	Intel suggestion	H5, H6 cnage from 1.1mm to 1.0mm	0.3(X02)
64	31	eDP CONN & Touch screen	2016/07/20	EMI	EMI request to solve EMI noise at Headphone	Add RA38, RA39 to AGND and DGND	0.3(X02)
65	28	LAN Clarkvillie & RJ45	2016/07/21	EMI	EMI request	Change CL22 from 150P to 10P (SE167100J80)	0.3(X02)
66	33	EC MEC5105 Support	2016/07/21	EE	Vendor schematic review	Add RE523 0 ohm for UE2 power pin soft start	0.3(X02)
67	27	eDP CONN & Touch screen	2016/07/22	ESD	ESD request	Reserve the ESD diode DV7 on USB20_N5 and USB_P5 for system damage issue	0.3(X02)
68	27	eDP CONN & Touch screen	2016/07/25	ESD	ESD request (layout limit)	Change DV7 to DV7 and DV8 (SC40000AR00)	0.3(X02)
69	32	EC MEC5105	2016/07/25	EE	Vendor schematic review	Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT Change RPE12.2 to RE524 (10Kohm) for EXPANDER_GPU_SMCLK	0.3(X02)
70	25	[Type C]PD Power	2016/07/25	EE	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)

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71	33	EC MEC5105 Support	2016/08/01	EE	Vendor schematic review	Change RE14,RE15,RE18 from 100k ohm to 10k ohm	0.3(X02)
72	38	Keyboard	2016/08/01	EE	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
73	14	CPU (9/14)	2016/08/01	EE	Intel suggestion	Change RC137 from 1k ohm to 3k ohm	0.3(X02)
74	11	CPU (6/14)	2016/08/01	EE	Intel suggestion	Depop RC190	0.3(X02)
75	34	USH & TPM	2016/09/06	EE	TPM change NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.4(X03)
76	33 32	EC MEC5105 Support EC MEC5105	2016/09/06	EE	Expander I/O change to Microchip MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.4(X03)
77	32	EC MEC5105 Support	2016/09/06	EE	Board ID	Change RE79 to 33kohm (SD028330280)	0.4(X03)
78	33	EC MEC5105 Support	2016/09/06	EE	EC watchdog reserve	Add QE13,RE530,RE531	0.4(X03)
79	32	EC MEC5105	2016/09/06	EE	Schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.4(X03)
80	32	EC MEC5105	2016/09/08	EE	EC request for GPIO setting	Reserve RE505 PU for LOM_CABLE_DETECT# Add RE532 PU for BCM5882_ALERT#	0.4(X03)
81	34	USH & TPM	2016/09/13	EE	EC request for GPIO setting	Pop RZ8, RZ9 for USH_SMBCLK and USH_SMBDAT	0.4(X03)
82	33	EC MEC5105 Support	2016/09/13	EE	EC watchdog delete	Delete QE13,RE530,RE531	0.4(X03)
83	31	Codec ALC3246	2016/09/13	RF	RF request	Pop CA54 82pf for DMIC_CLK0	0.4(X03)
84	39	PAD, LED	2016/09/13	ME	ME request (LED brightness)	Change RZ361 from 150ohm to 100ohm (SB12 only)	0.4(X03)
85	33	EC MEC5105 Support	2016/09/26	EE	Dell request	Reserve RE536/RE537 for resistors for PCH_DPWROK circuit	0.5(X04)
86	32	EC MEC5105	2016/09/26	EE	WDT schematic option 2	Use Option2: pop RE361 / depop RE362	0.5(X04)
87	23	DP/USB3 Repeater SW TUSB546	2016/09/26	EE	BITS296634/287982-Cannot wake on LAN via Type-C to LAN dongle	Add LT13 for +3.3V_VDD_PIC and depop LT11 Change +3.3V_RUN to +3.3V_CPS for this page	0.5(X04)
88	33	EC MEC5105 Support	2016/09/29	EE	WDT schematic	Add QE13, CE503, RE530	0.5(X04)
89	33	EC MEC5105 Support	2016/09/30	EE	Board ID	Change RE79 to 8.2kohm (SD028820180)	0.5(X04)
90	33	EC MEC5105 Support	2016/09/30	EE	BITS294007-Sometimes need to press power button twice to power on system	Change CE12 to 2.2uf and RE33 to 1Kohm	0.5(X04)
91	23	DP/USB3 Repeater SW TUSB546	2016/09/30	EE	Schematic align	Reserve RT399~RT402 (0ohm) for TBT RX	0.5(X04)
92	32	EC MEC5105	2016/10/05	EE	Prevent EOS issue on MEC5105	Add 100ohm serial resistor on CV2_ON close to UE1.H8	0.5(X04)
93	23	DP/USB3 Repeater SW TUSB546	2016/10/05	EE	Schematic align (BME)	Remove RT399~RT402 (0ohm) for TBT RX	0.5(X04)

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94	33	EC MEC5105 Support	2016/11/04	EE	Board ID	Change RE79 to 4.3kohm (SD028820180)	1.0(A00)
95	32	EC MEC5105	2016/11/04	EE	MEC5105 change from revB to revC	Change MEC5105 CPN to SA00009GL30 Depop RE361,Pop RE362	1.0(A00)
96	33	EC MEC5105 Support	2016/11/04	EE	MEC5105 revC WDT schematic	Pop RE536, Depop QE13, CE503, RE530, UE7, CE5,CE6, RE348	1.0(A00)
97	All	All page	2016/11/04	EE	0 ohm short pad	Change 0 ohm to short pad	1.0(A00)
98	12	CPU (7/14)	2016/11/04	EE	Service Mode Switch remove	Depop SW1, RC222 and pop RC221	1.0(A00)
99	24	[Type C]PD Controller TI	2016/11/04	EE	TI PD CC1/CC2 CAP change	Change CT85,CT86 to 820pf (SE000003W00)	1.0(A00)

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